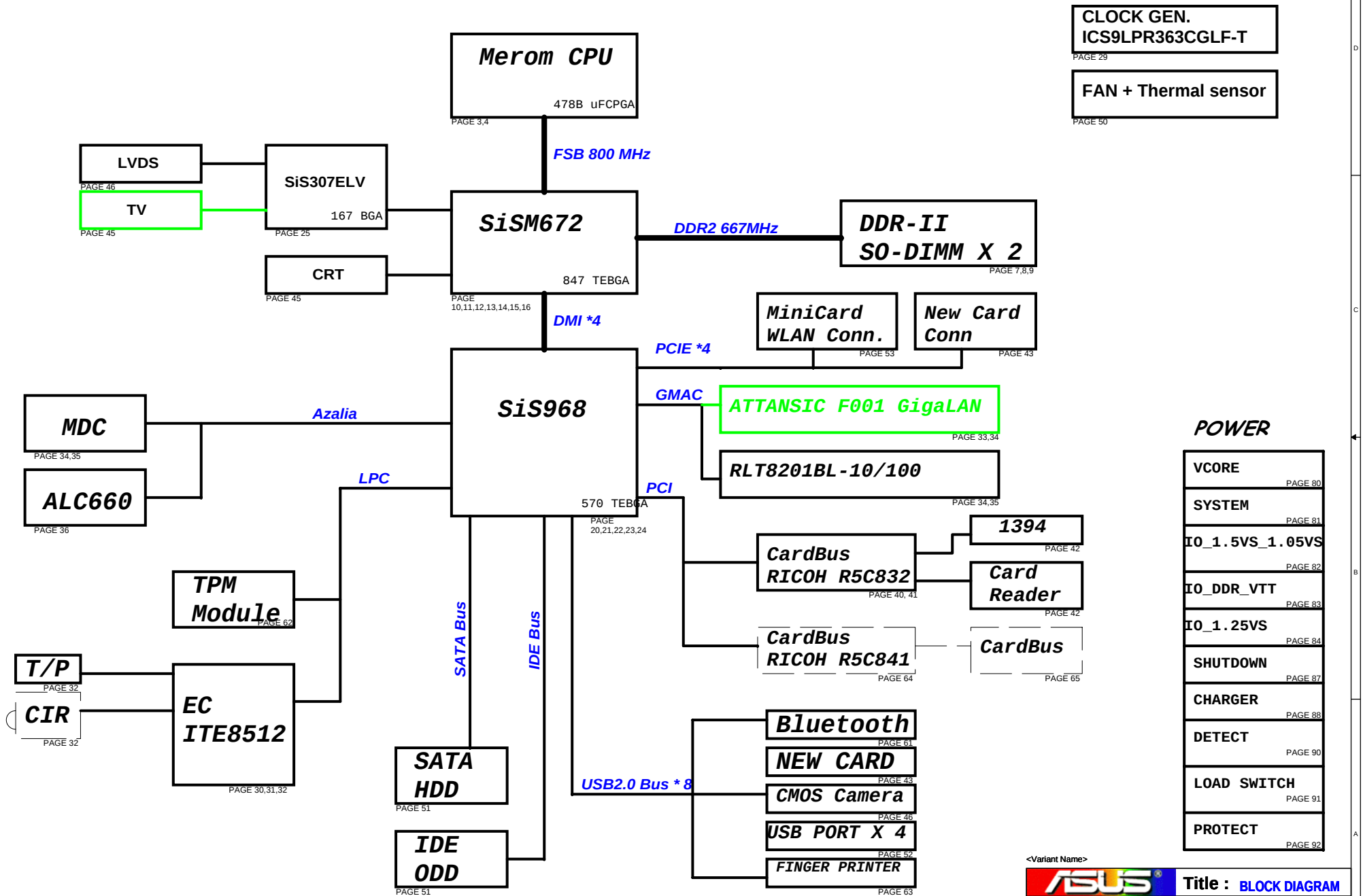
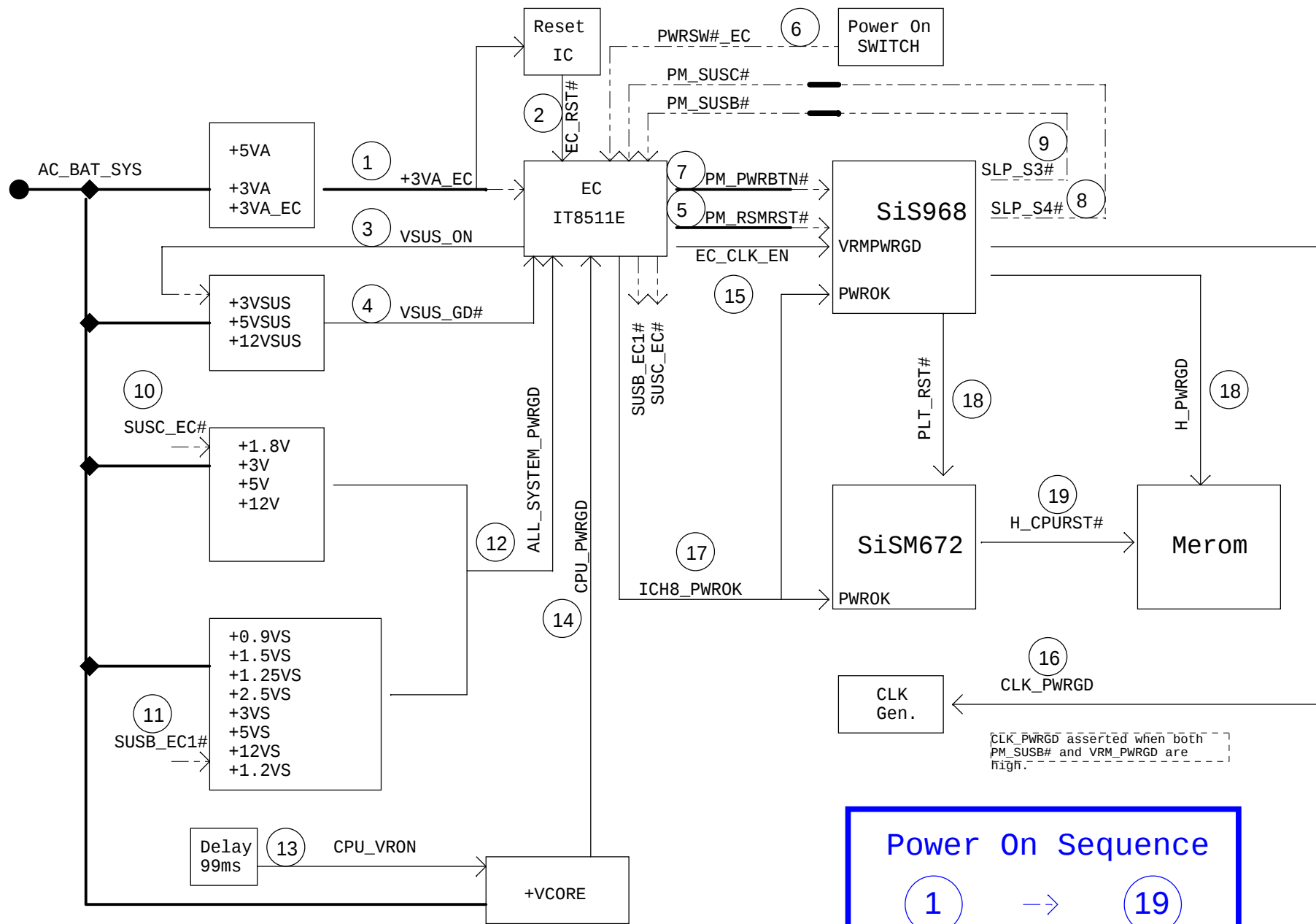


X51C Main BD. R1.0 BLOCK DIAGRAM



<Variant Name>

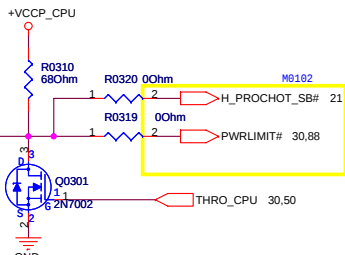
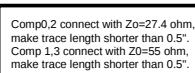
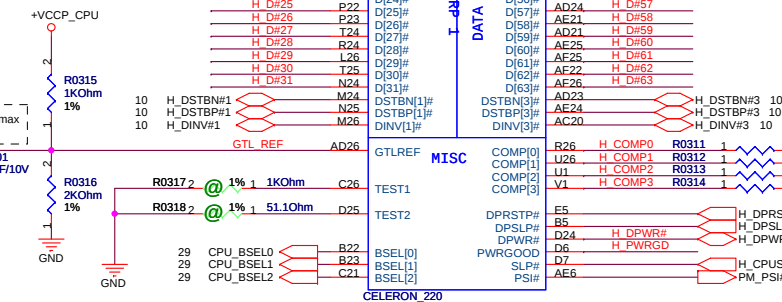
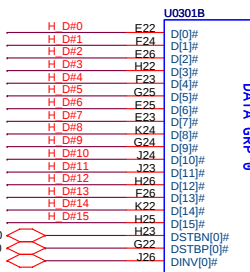
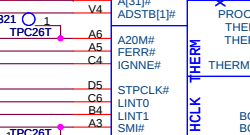
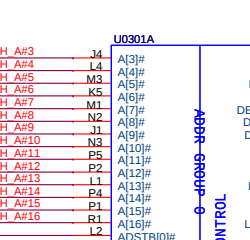
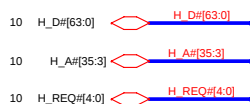


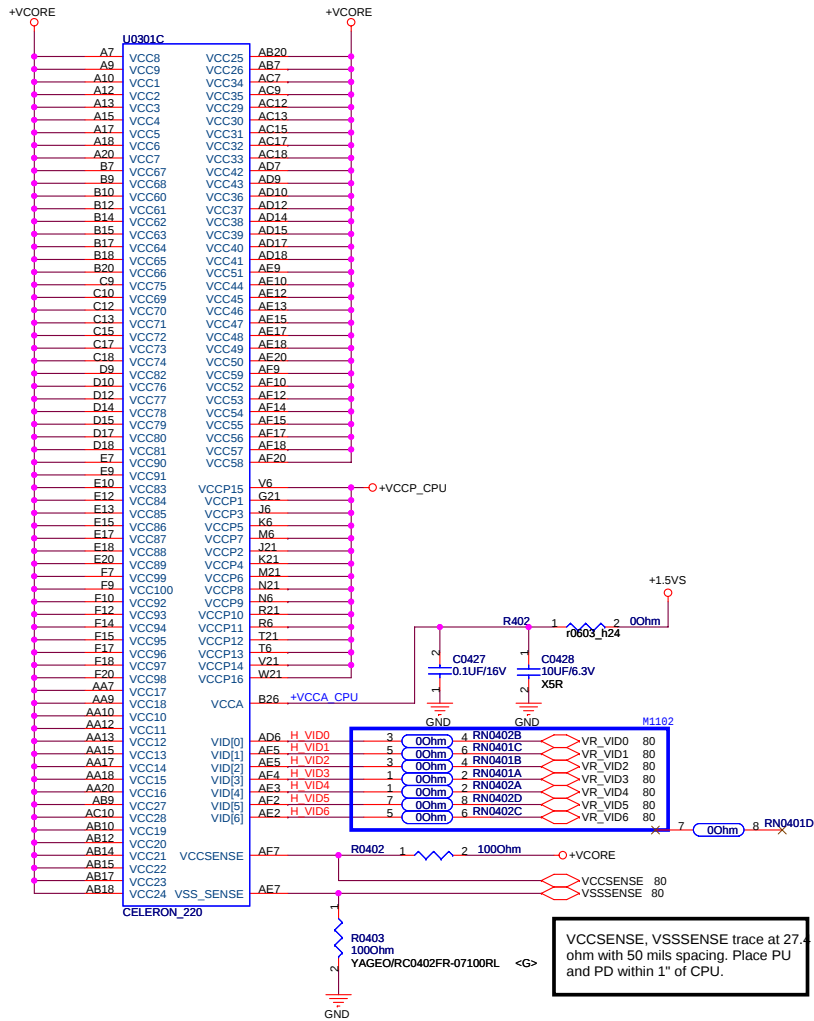
Power On Sequence

1 → 19

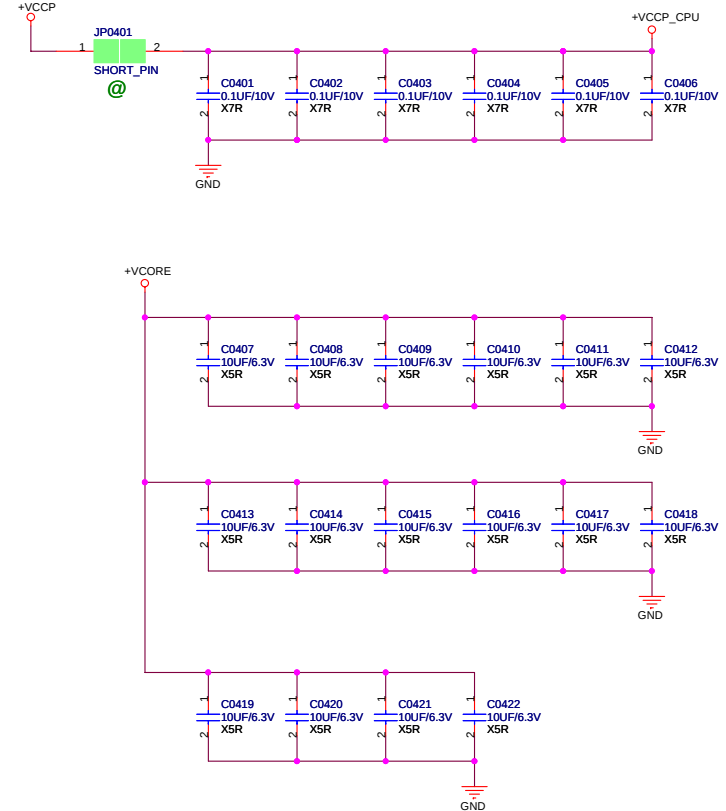
<Variant Name>

ASUS		Title : PowerOn sequence	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Monday, August 13, 2007	Sheet	2 of 94	





+VCCP Decoupling Capacitor (Place near CPU)



5					4					3					2					1																																																																															
D																																																																																																			
C																																																																																																			
B																																																																																																			
A																																																																																																			
															<Variant Name> <table><tr><td colspan="5"></td><td colspan="5">Title : NULL</td></tr><tr><td colspan="5">ASUSTeK COMPUTER INC</td><td colspan="5">Engineer: Hawk / Kaxidy</td></tr><tr><td>Size</td><td colspan="13">Project Name</td><td>Rev</td></tr><tr><td>A</td><td colspan="13">T12C</td><td>1.1</td></tr><tr><td colspan="15">Date: Monday, August 13, 2007</td><td colspan="10">Sheet 5 of 94</td></tr></table>															Title : NULL					ASUSTeK COMPUTER INC					Engineer: Hawk / Kaxidy					Size	Project Name													Rev	A	T12C													1.1	Date: Monday, August 13, 2007															Sheet 5 of 94									
					Title : NULL																																																																																														
ASUSTeK COMPUTER INC					Engineer: Hawk / Kaxidy																																																																																														
Size	Project Name													Rev																																																																																					
A	T12C													1.1																																																																																					
Date: Monday, August 13, 2007															Sheet 5 of 94																																																																																				
5					4					3					2					1																																																																															

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: *Hawk / Kaxidy*

Size
A

Project Name

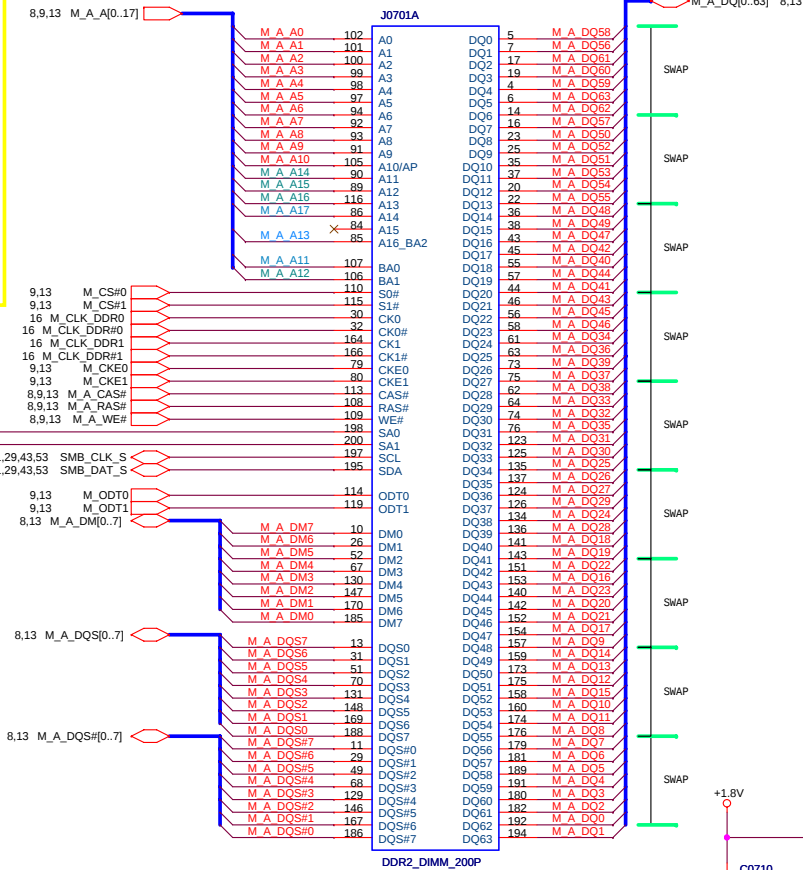
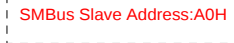
T12C

Rev
1.1

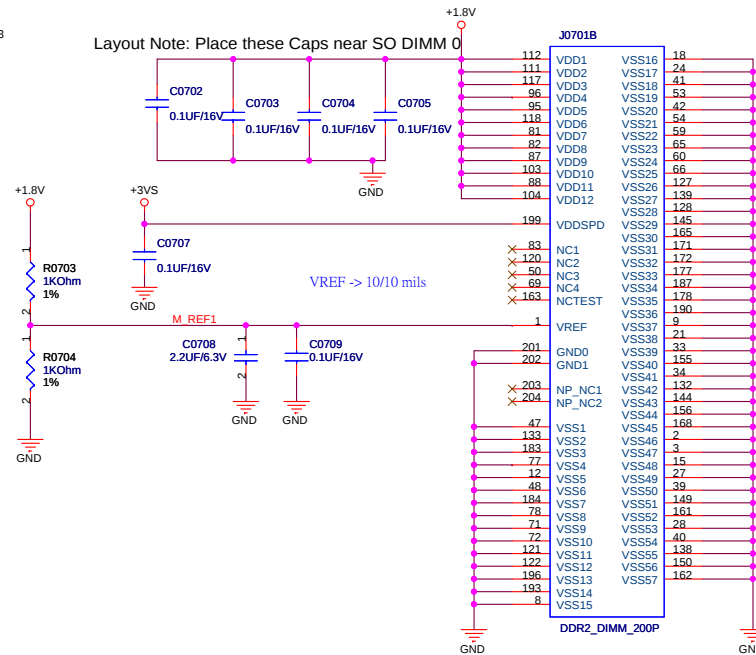
Date: Monday, August 13, 2007

Sheet 6 of 94

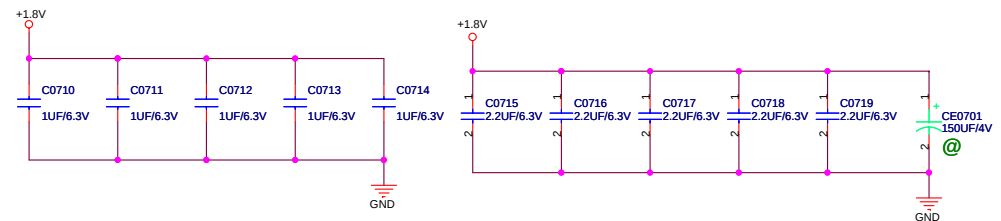
M1227

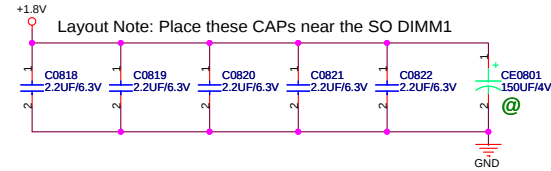
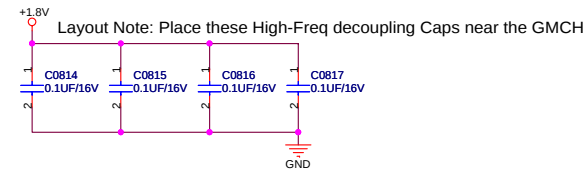
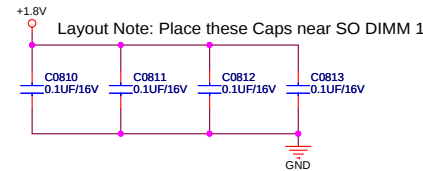
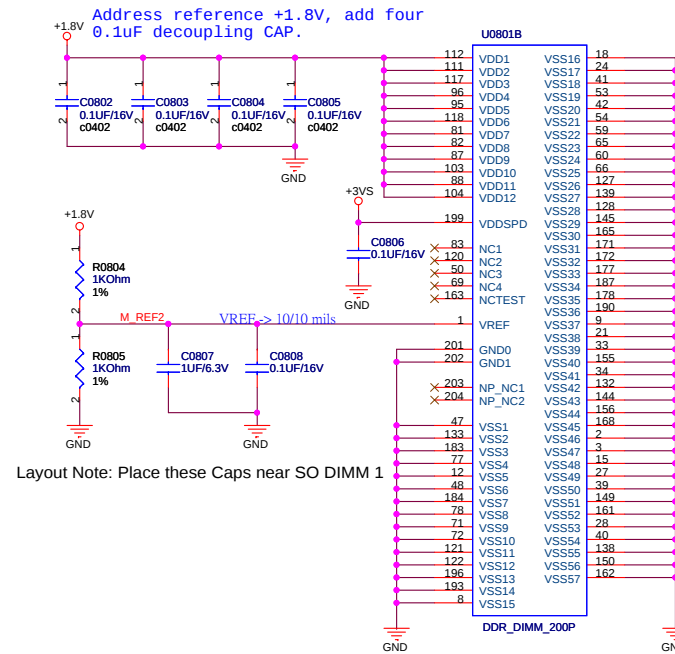
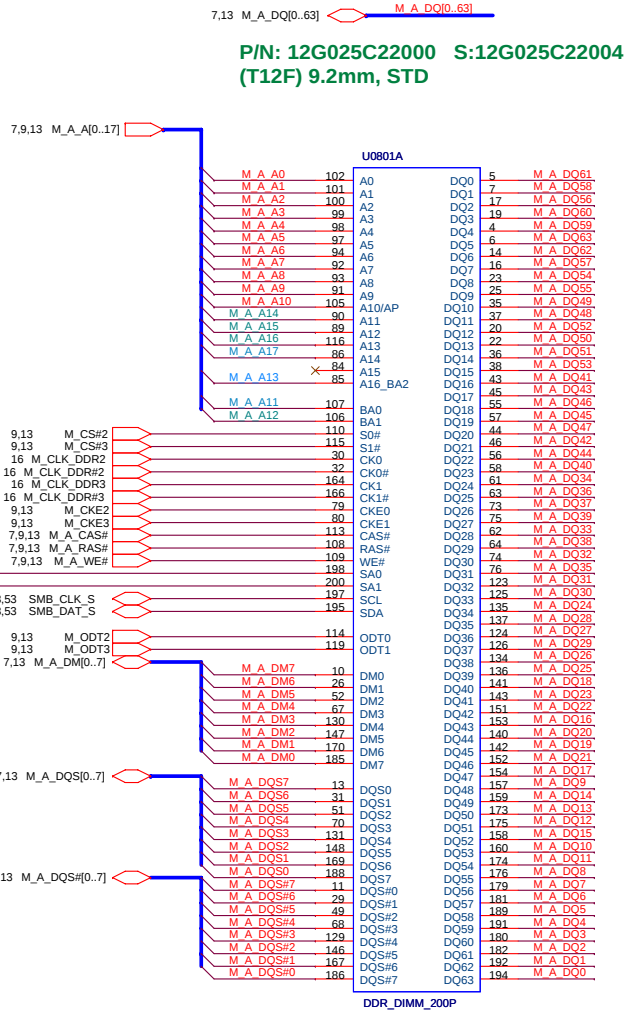
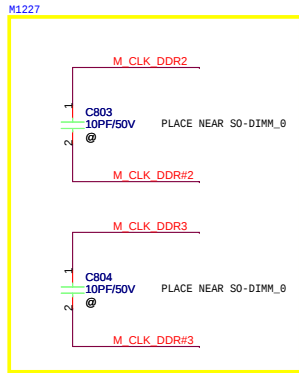


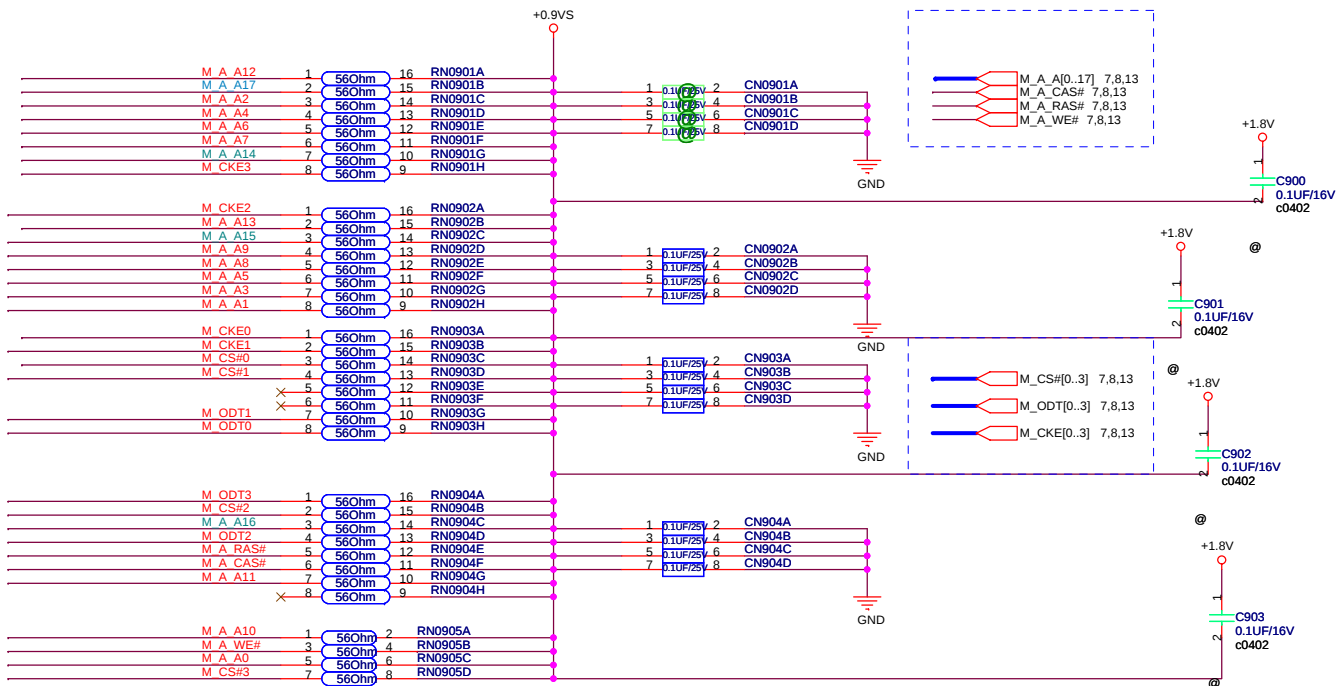
Layout Note: Place these Caps near SO DIMM 0



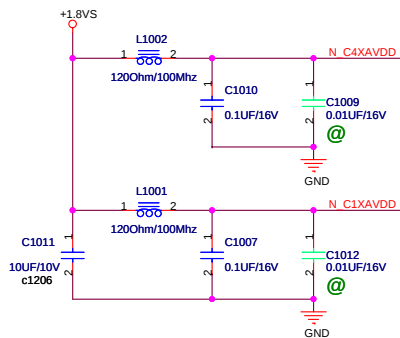
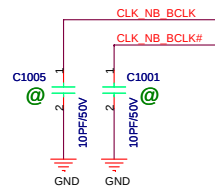
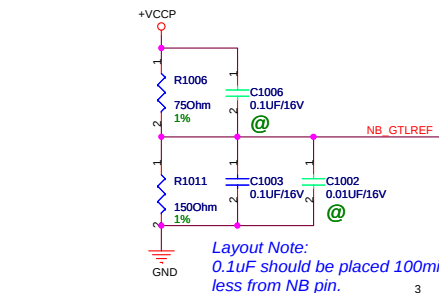
Layout Note: Place these Caps near SO DIMM 0



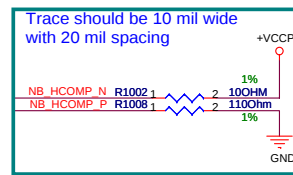
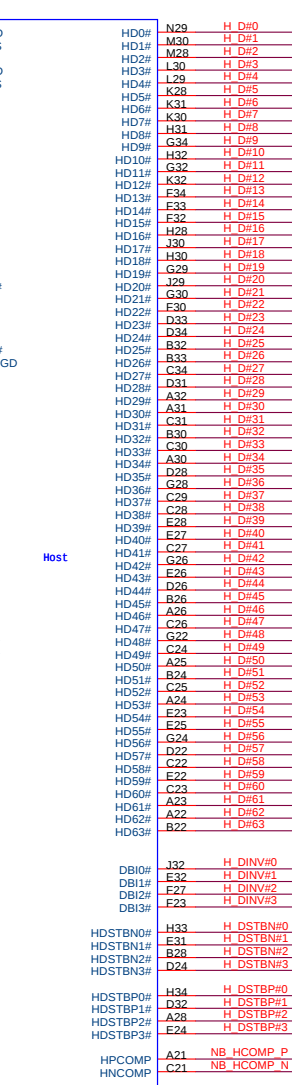
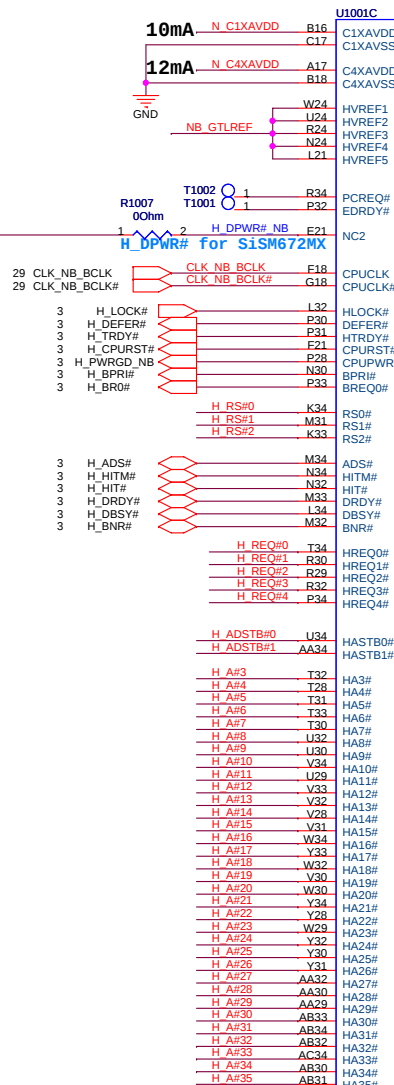




Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS



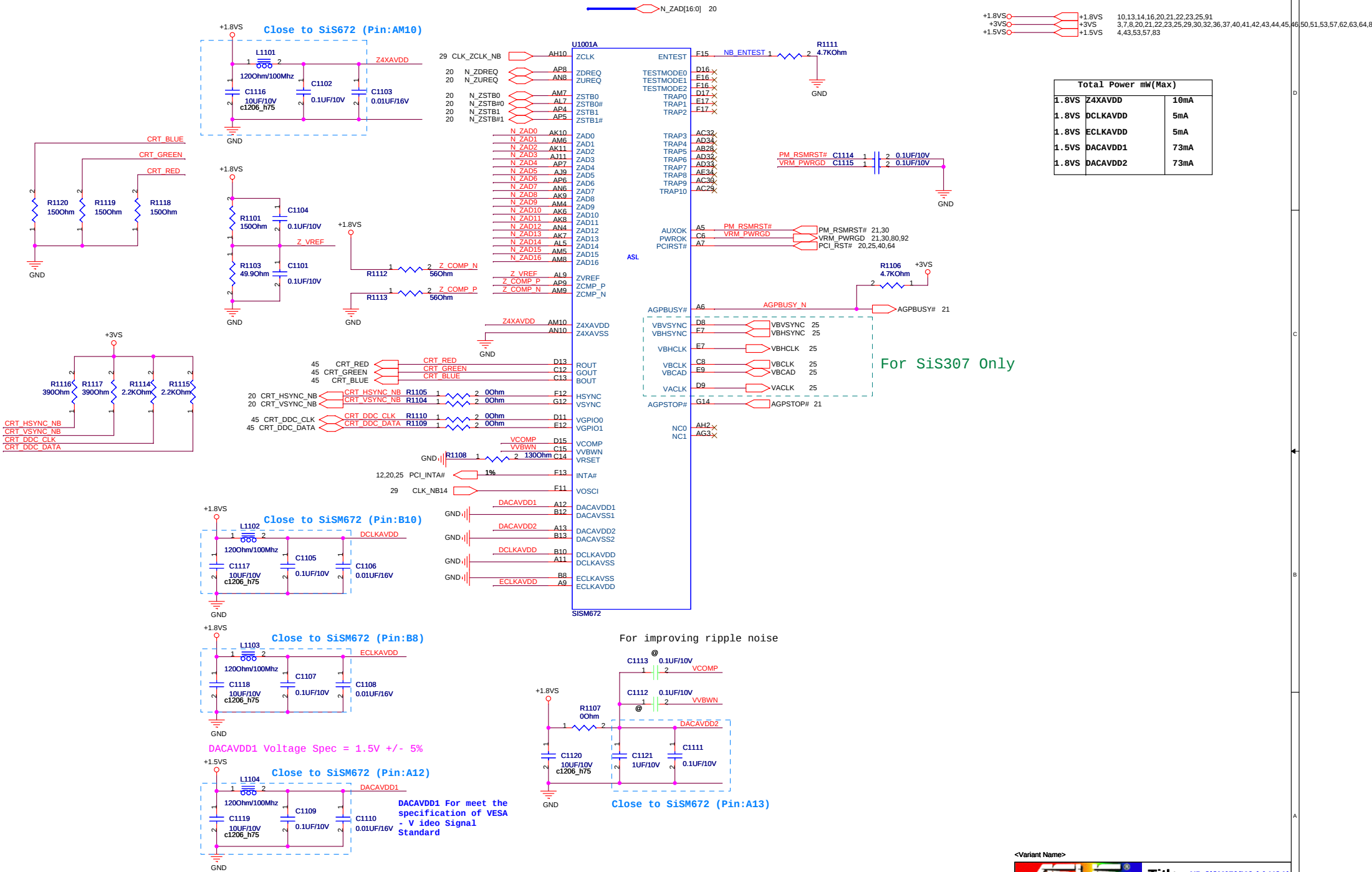
Total Power mW(Max)		
1.8VS	N_C1XAVDD	10mA
	N_C4XAVDD	12mA



+VCCP
+1.8VS

4.14,21,23,29,57,83,92
11,13,14,16,20,21,22,23,25,91

H_D#0[63:0] 3
H_A#0[35:3] 3
H_REQ#0[4:0] 3
H_RS#0[2:0] 3
H_ADSTB#0[1:0] 3
H_DIN#0[3:0] 3
H_DSTBP#0[3:0] 3
H_DSTBN#0[3:0] 3



+1.8VS	+1.8VS	10,13,14,16,20,21,22,23,25,91
+3VS	+3VS	3,7,8,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,
+1.5VS	+1.5VS	4,43,53,57,83

Total Power mw(Max)		
1.8VS	Z4XAVDD	10mA
1.8VS	DCLKAVDD	5mA
1.8VS	ECLKAVDD	5mA
1.5VS	DACAVDD1	73mA
1.8VS	DACAVDD2	73mA

For SiS307 Only

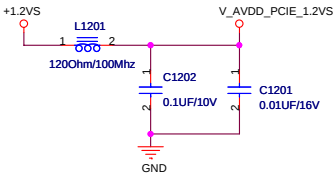
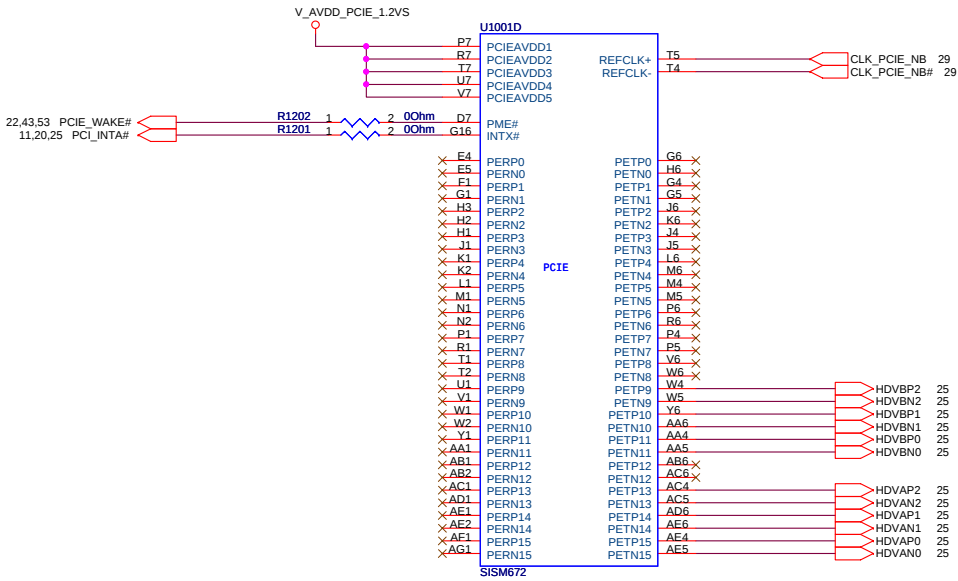
For improving ripple noise

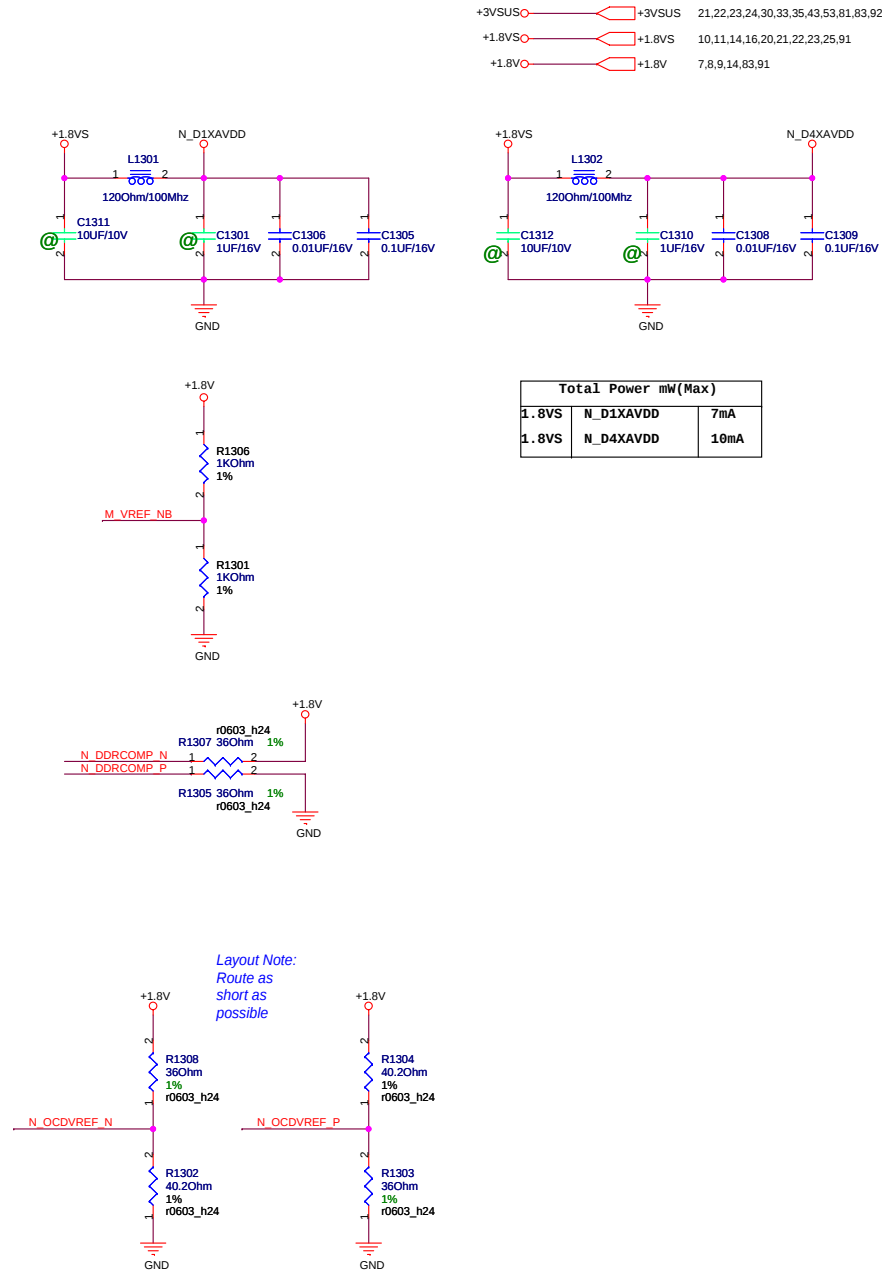
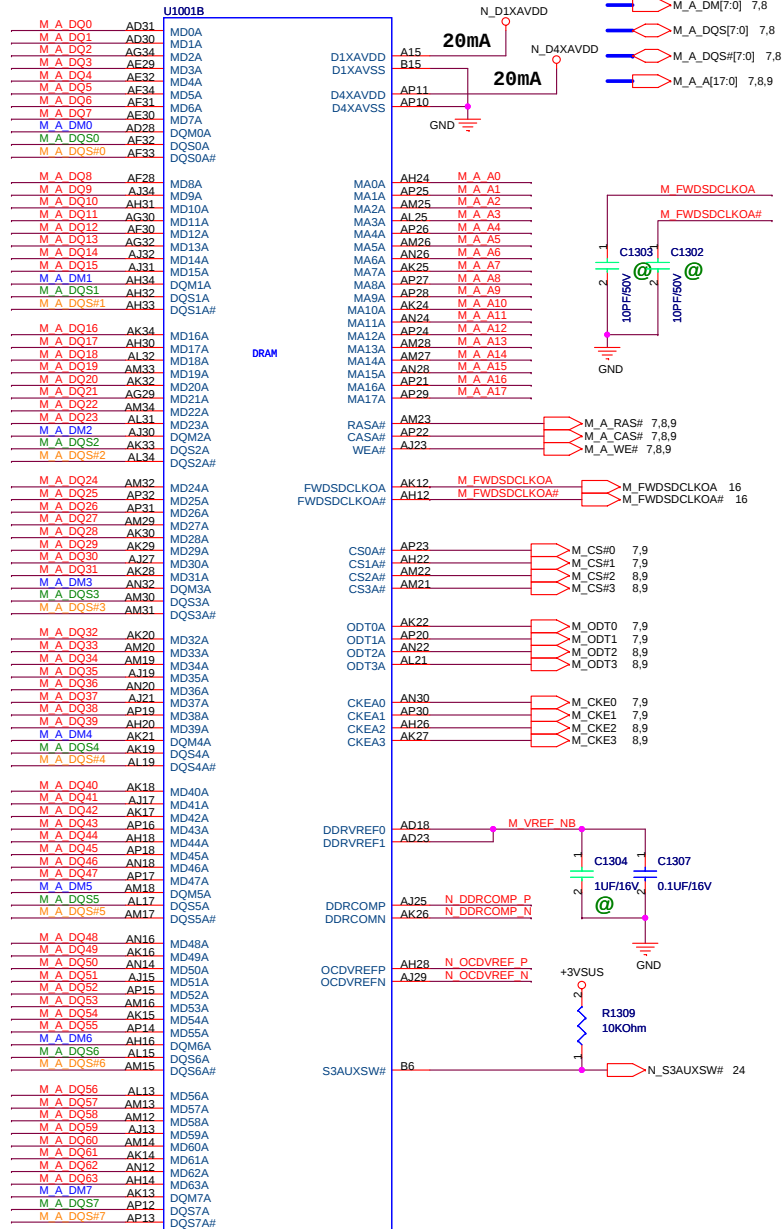
DACAVDD1 Voltage Spec = 1.5V +/- 5%

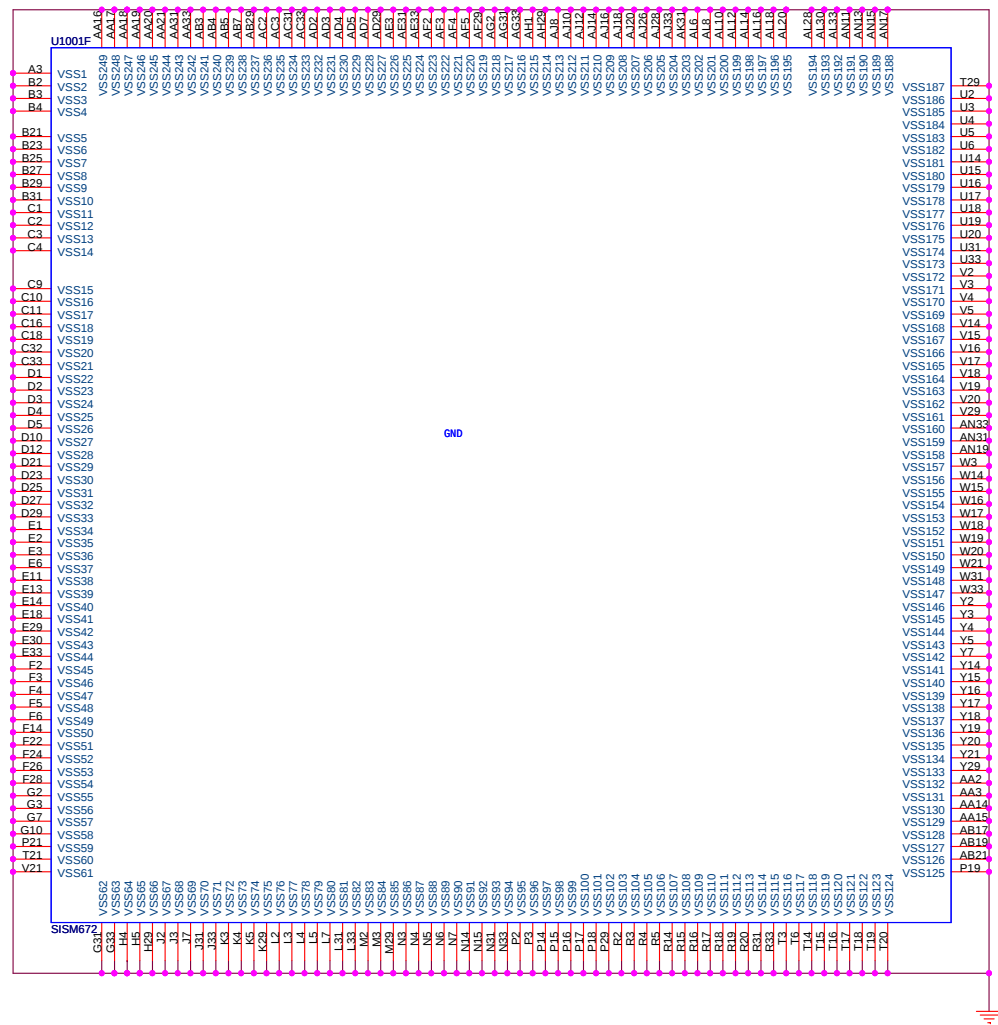
DACAVDD1 For meet the specification of VESA - V ideo Signal Standard

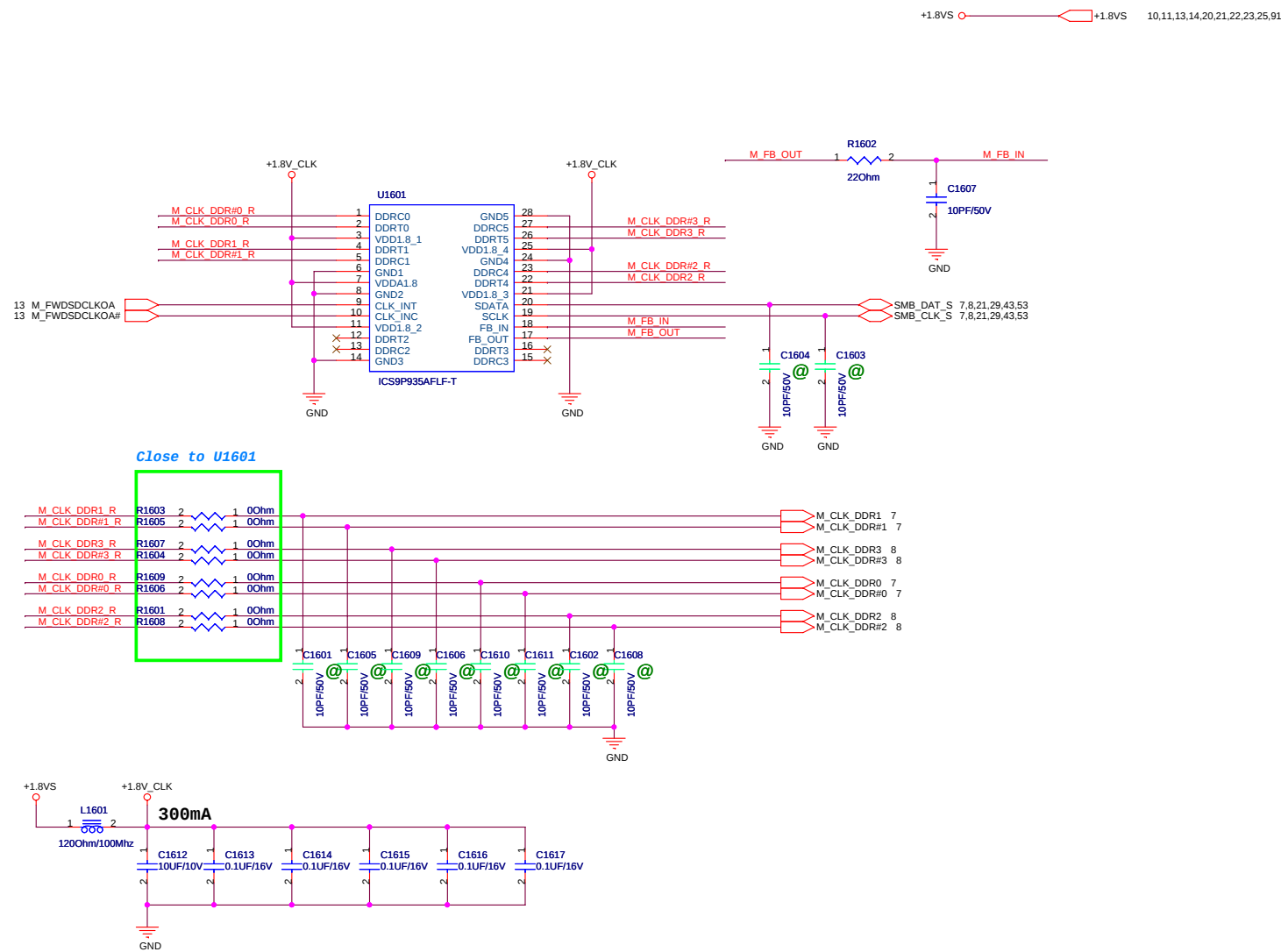
+1.2VS +1.2VS 14.83.91

Total Power mW(Max)		
1.2V	V_AVDD_PCIE_1.2V	190mA









	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

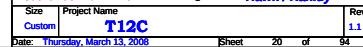
<Variant Name>

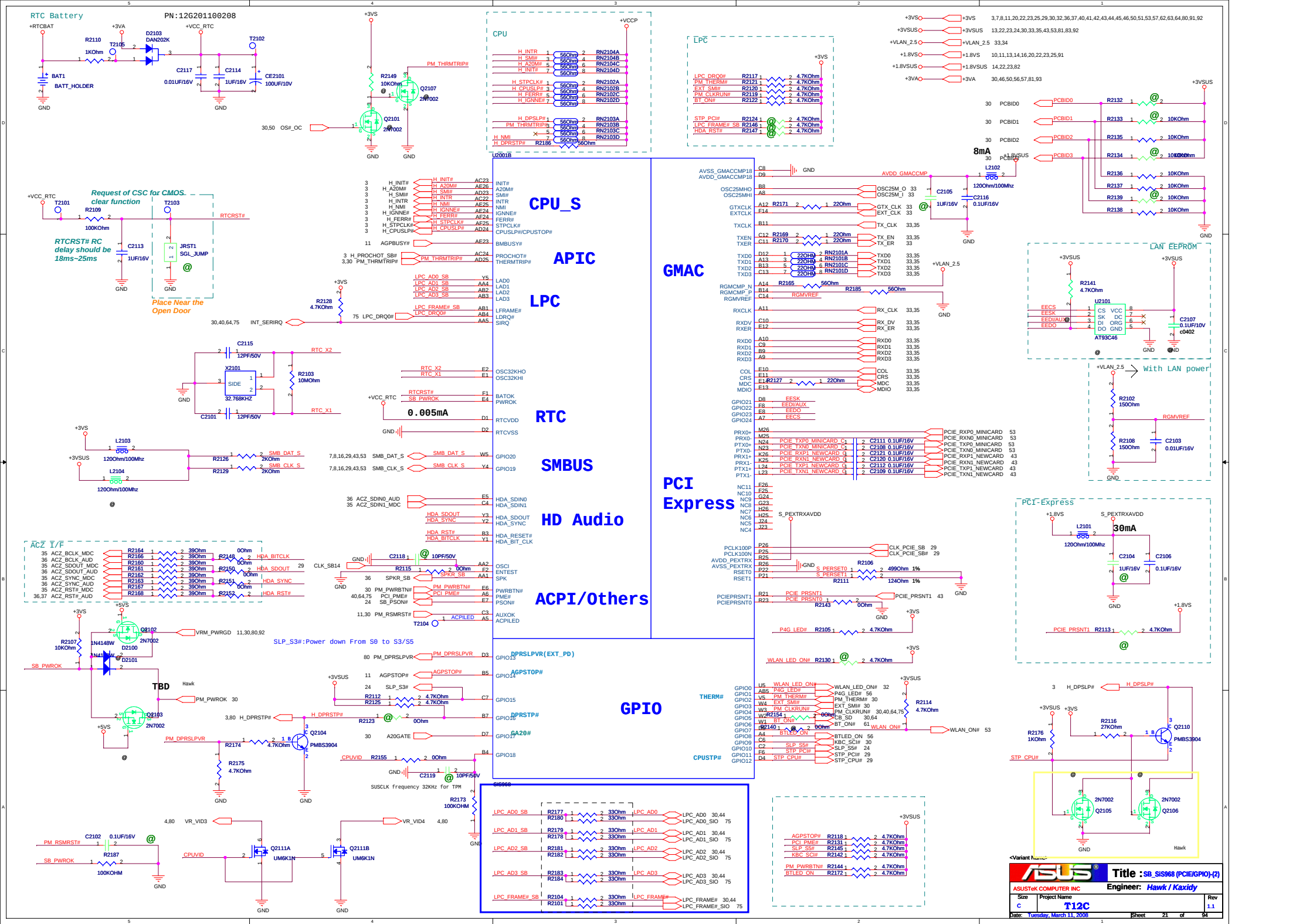
		Title : NULL
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 18 of 94

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

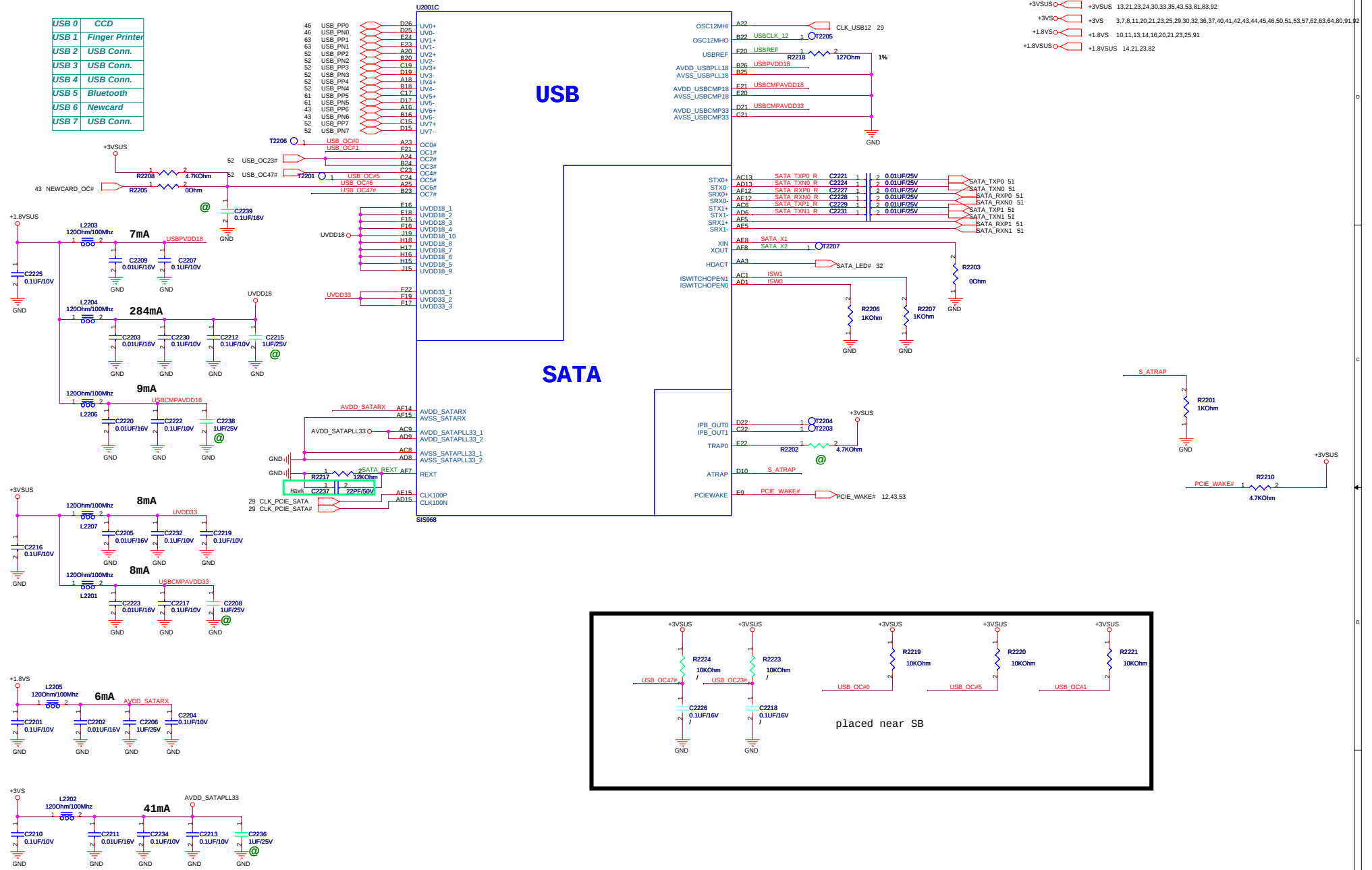
<Variant Name>

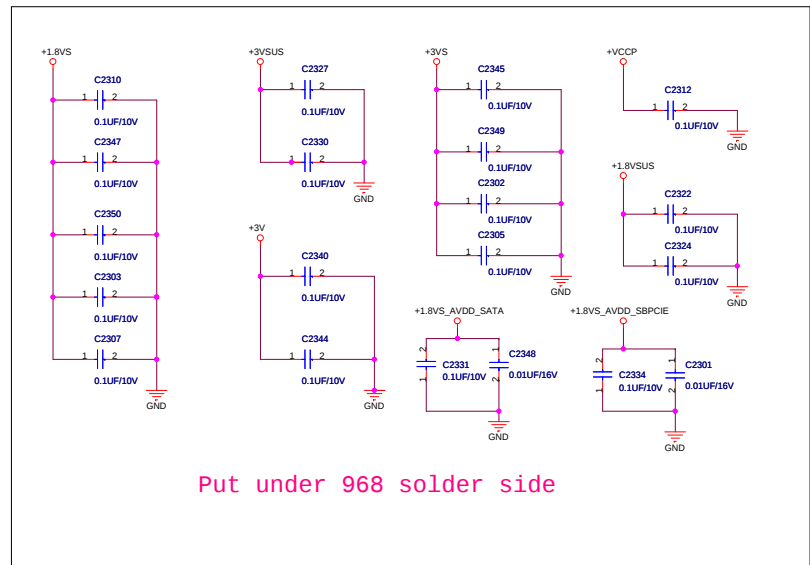
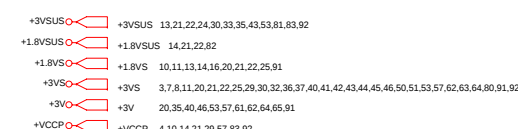
		Title : NULL
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 19 of 94



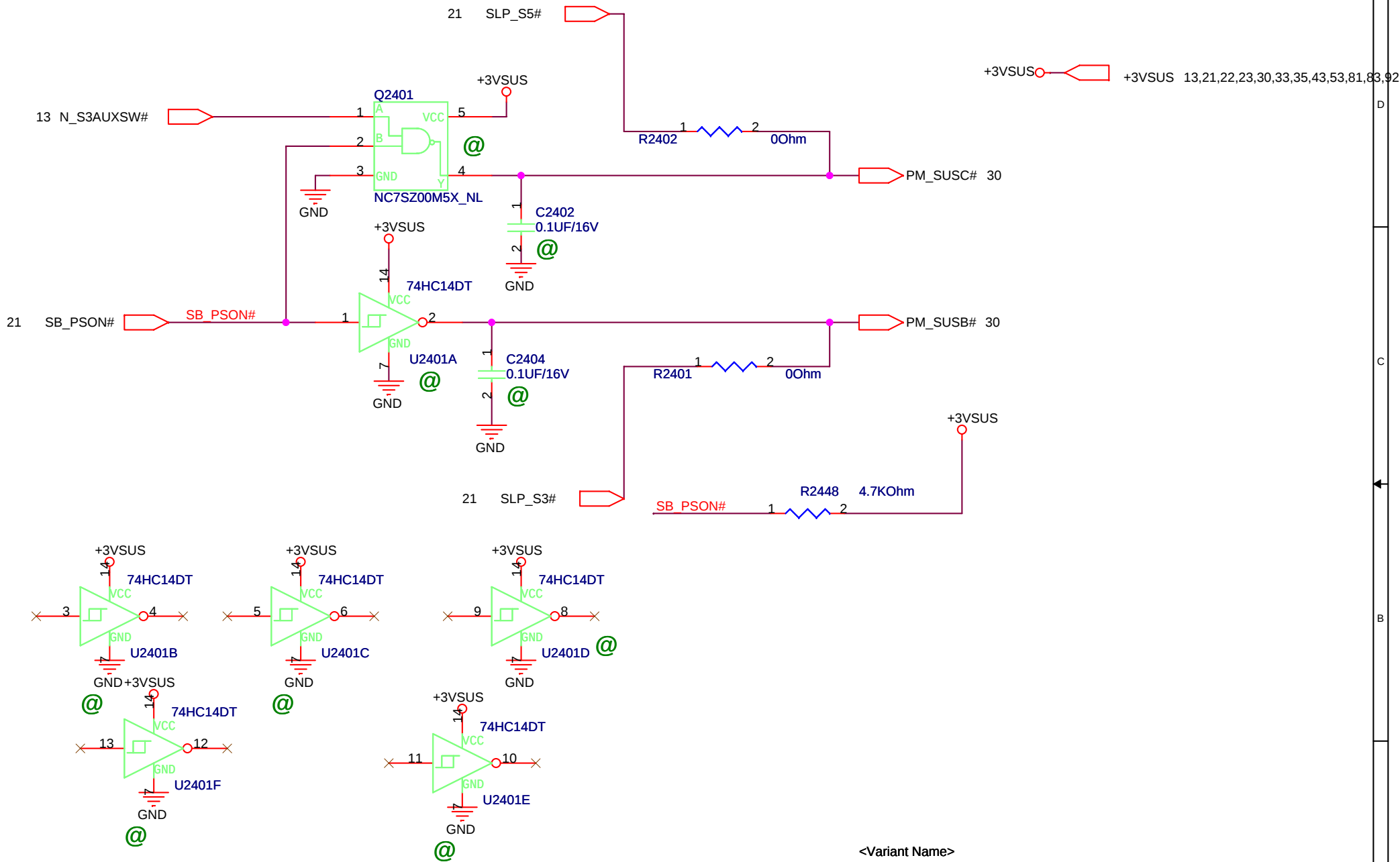


USB 0	CCD
USB 1	Finger Printer
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Bluetooth
USB 6	Newcard
USB 7	USB Conn.



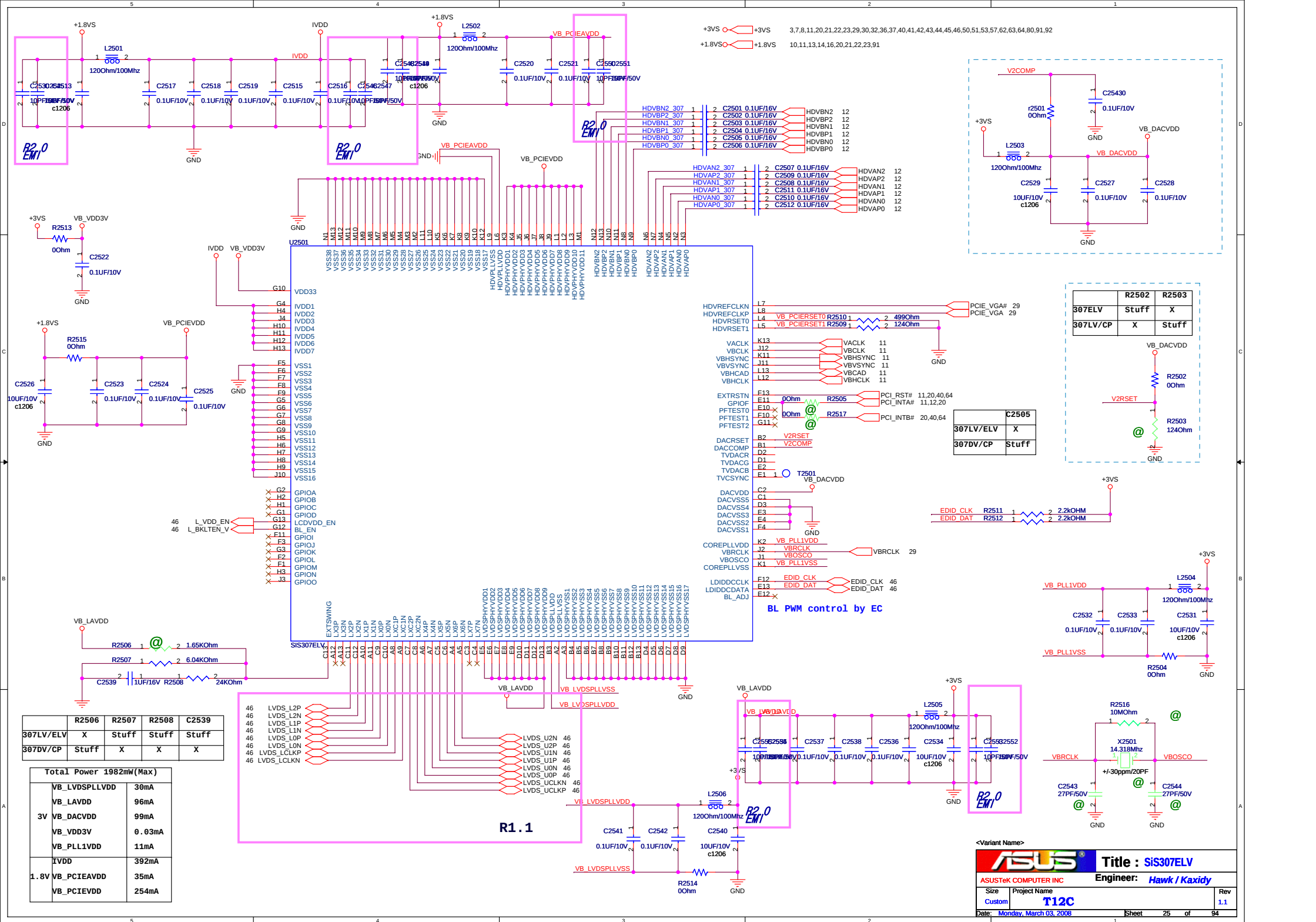


Put under 968 solder side



<Variant Name>

ASUS		Title : SiS968 (STRAPING)	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Friday, August 17, 2007		Sheet	24 of 94



	5	4	3	2	1
D					D
C					C
B					B
A					A

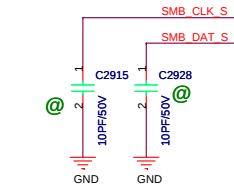
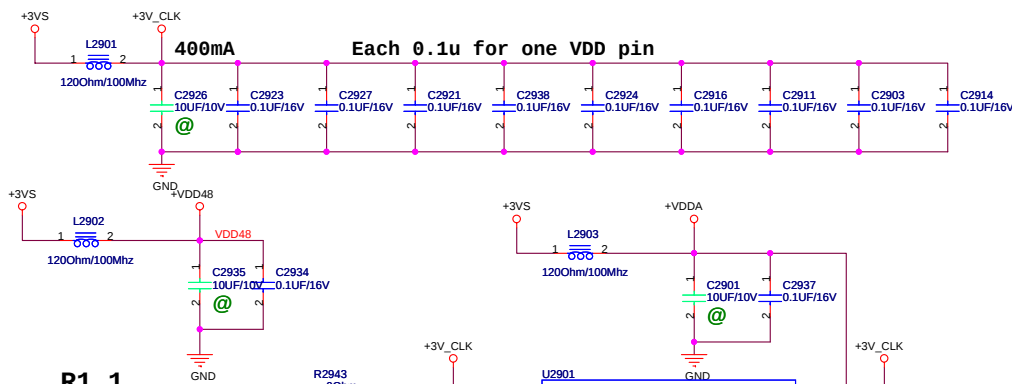
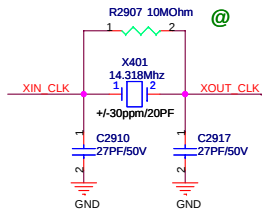
<Variant Name>

		Title : NULL		
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy		
Size A	Project Name T12C			Rev 1.1
Date: Monday, August 13, 2007		Sheet	26	of 94

5	4	3	2	1
D				D
C				C
B				B
A				A

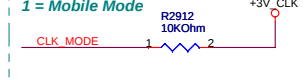
<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Monday, August 13, 2007		Sheet	27 of 94



CLK_MODE

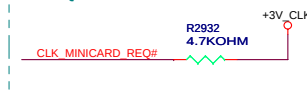
0 = Desktop Mode
1 = Mobile Mode



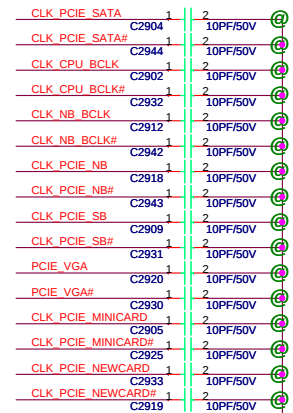
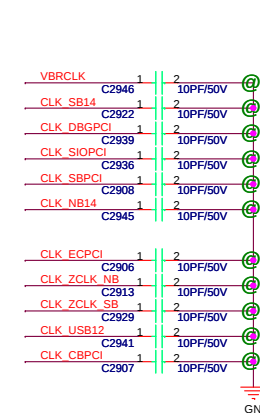
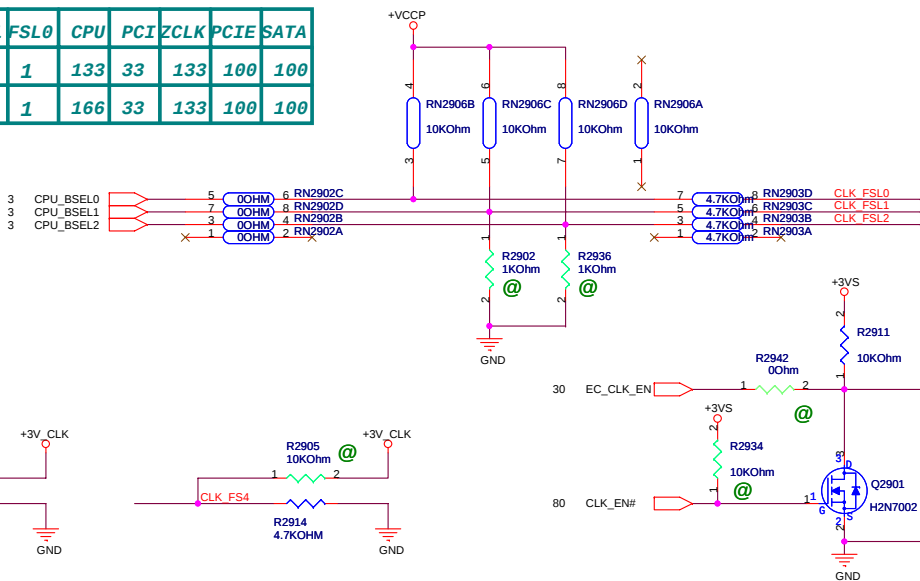
PEREQ0# control PCIE 0



PEREQ1# control PCIE 2

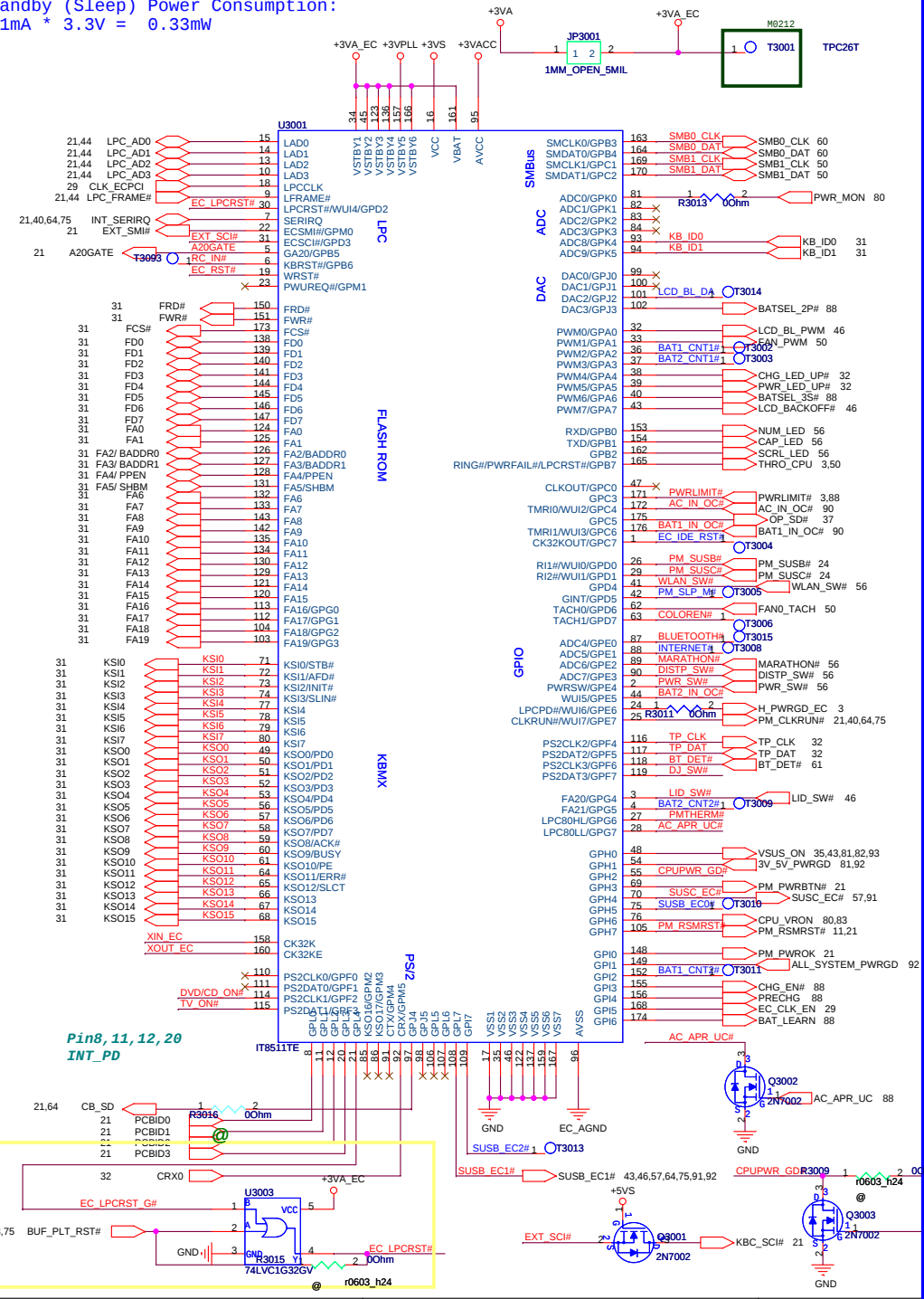


FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



<Variant Name>

andby (Sleep) Power Consumption:
 $1\text{mA} * 3.3\text{V} = 0.33\text{mW}$



+3VA_EC change to +3VS---R1.2

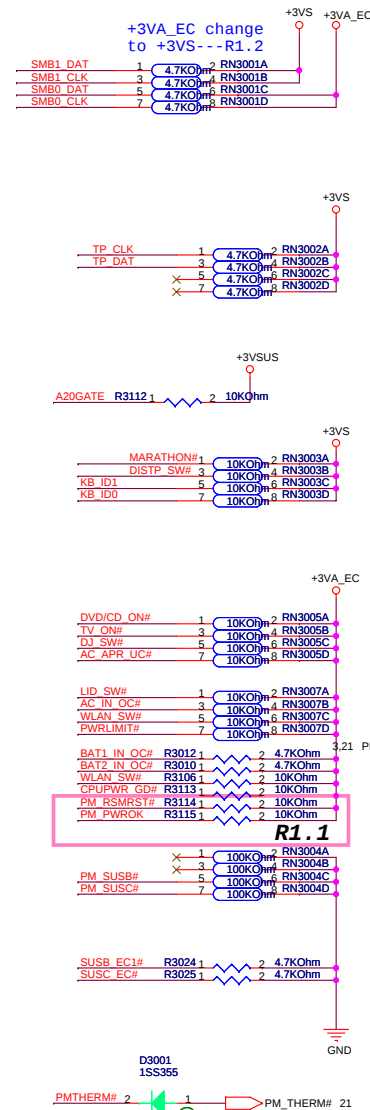
SMB1_DAT 1 4.7kΩ RN3001A

SMB1_CLK 2 4.7kΩ RN3001B

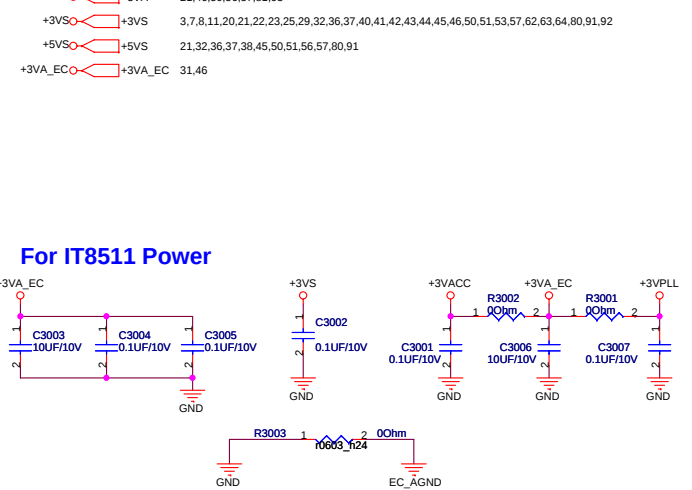
SMB0_DAT 5 4.7kΩ RN3001C

SMB0_CLK 7 4.7kΩ RN3001D

+3VS +3VA_EC



+3VA		+3VA	21,46,50,56,57,81,93
+3VS		+3VS	3,7,8,11,20,21,22,23,25,29,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
+5VS		+5VS	21,32,36,37,38,45,50,51,56,57,80,91
+3VA_EC		+3VA_EC	31,46



THRMTRIP_RST#

Q2109
2N7002

+3V_A_EC

X3001
32.768KHZ

R3007
10M Ohm

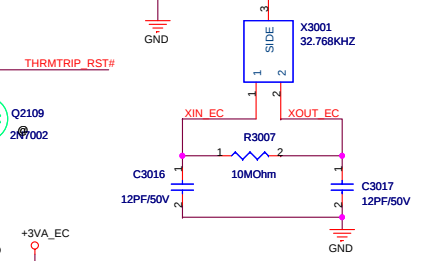
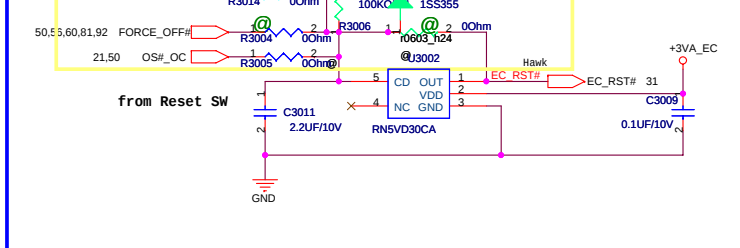
C3016
12PF/50V

C3017
12PF/50V

XIN_EC

XOUT_EC

GND

[illegible]

I/O Base Address	Share Memory	PP Enable
Note: It can be programmable by EC firmware	Note: It can be programmable by EC firmware	Note: Default Internal Pull-Low

<Variant Name>

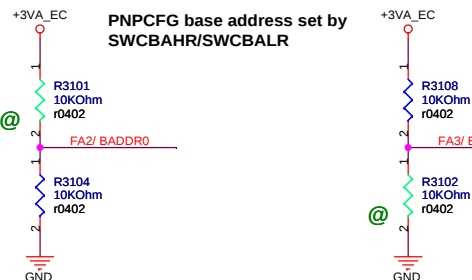
		Title : <i>EC-ITE8511 (2)</i>	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size Custom	Project Name T12C	Rev 1.1	
Date: <i>Friday, March 07, 2008</i>		Sheet	30 of 94

EC Hardware Strap

Strap value sampled after
VSTBY power up reset

+3VA_ECO  +3VA_EC 30,46

PNPCFG base address set by SWCBAHR/SWCBALR



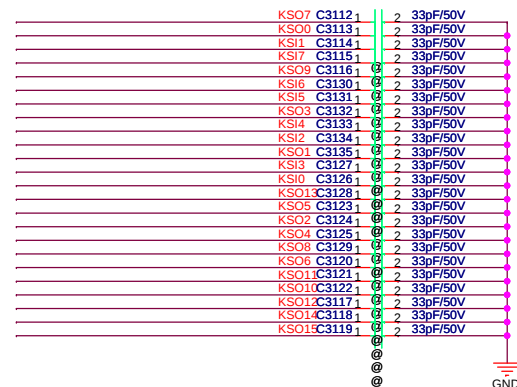
BADDR[1:0]

No pull up:

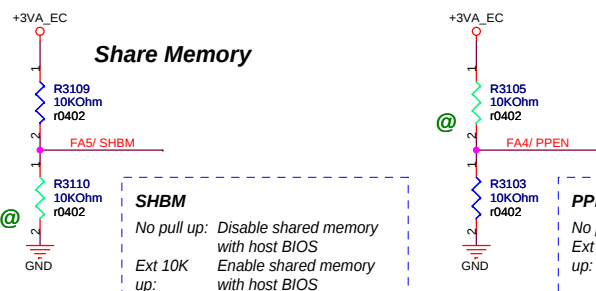
Ext 10K up on BADDR0:

Ext 10K up on BADDR1:

The register pair to access PNPCFG is 002Eh and 002Fh.
The register pair to access PNPCFG is 004Eh and 004Fh.
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.



Share Memory



SHBM

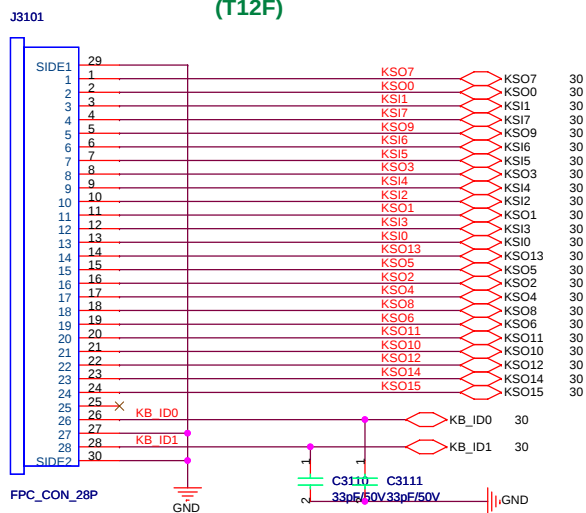
No pull up: Disable shared memory with host BIOS
Ext 10K up: Enable shared memory with host BIOS

PPEN

No pull up: Normal KBS interface pins are switched to parallel port interface for in-system programming.
Ext 10K up:

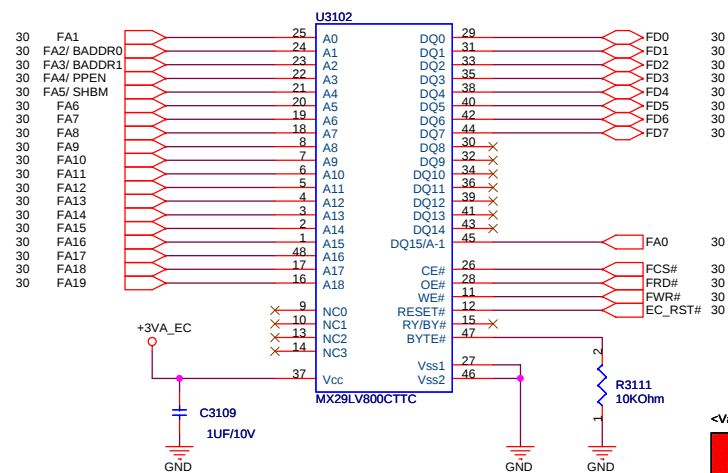
Keyboard Conn.

P/N: 12G182402806
(T12F)



For 8M bits SPI ROM

8M TSOP



<Variant Name>

		Title : EC-ITE8511(2)	
ASUSTek COMPUTER INC.ETD		Engineer: Hawk / Kaxidy	
Size	Project Name	T12C	Rev 1.1
Custom			
Date: Friday, August 17, 2007		Sheet 31	of 94

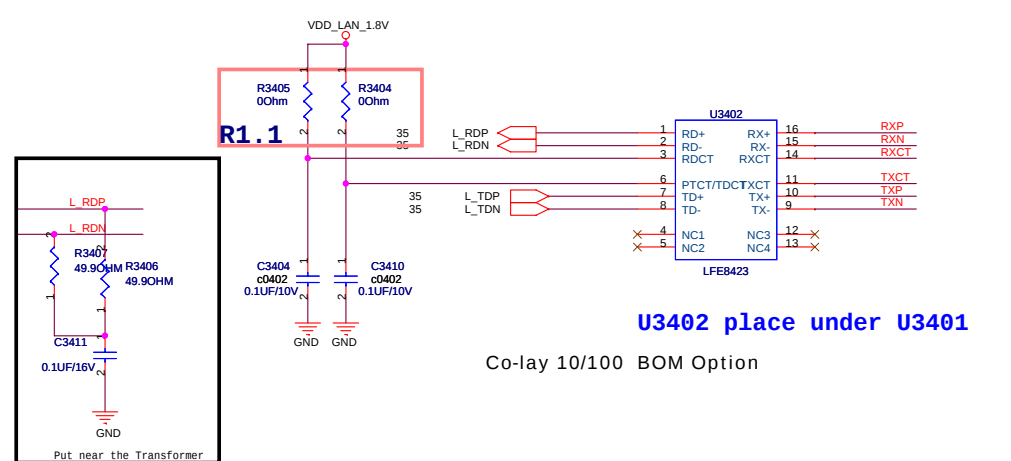
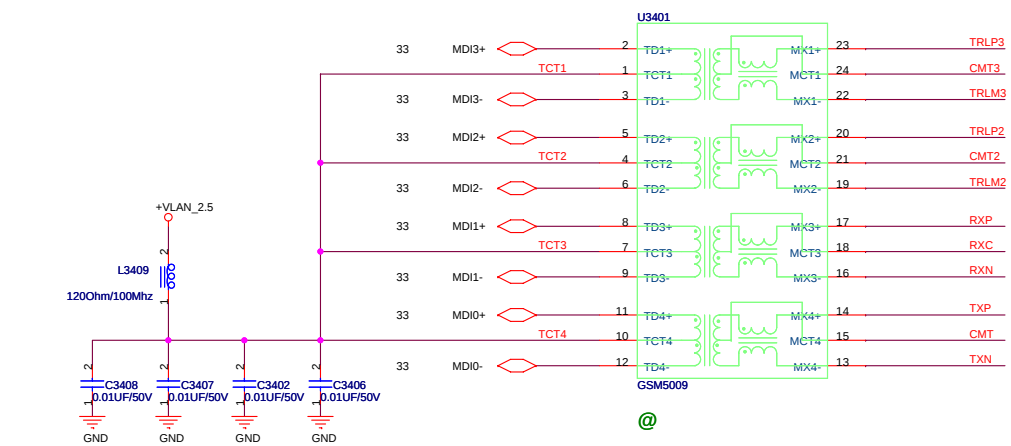
+5VSUS		+5VSUS	33,81
+5VS		+5VS	21,30,36,37,38,45,50,51,56,57,80,91
+3VS		+3VS	3,7,8,11,20,21,22,23,25,29,30,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
+5V		+5V	37,46,52,56,57,65,91

12G183101506

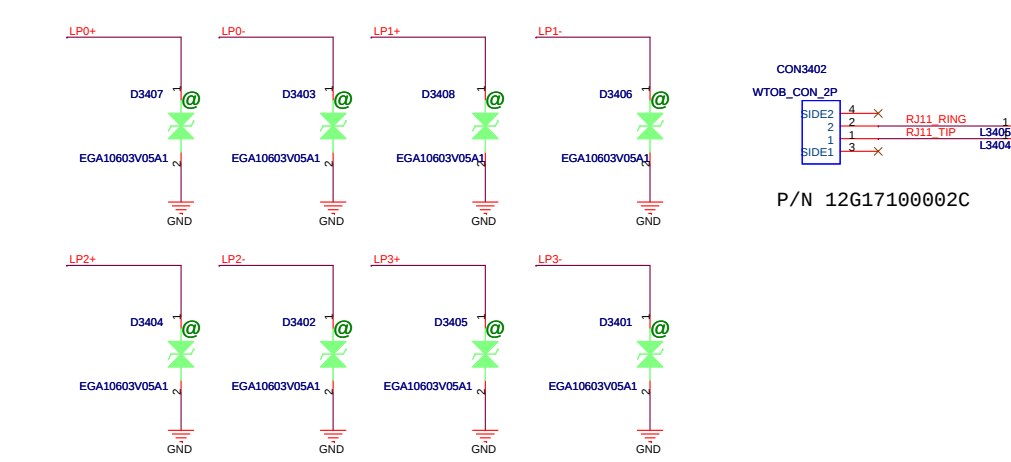
T12







U3402 place under U3401
Co-lay 10/100 BOM Option

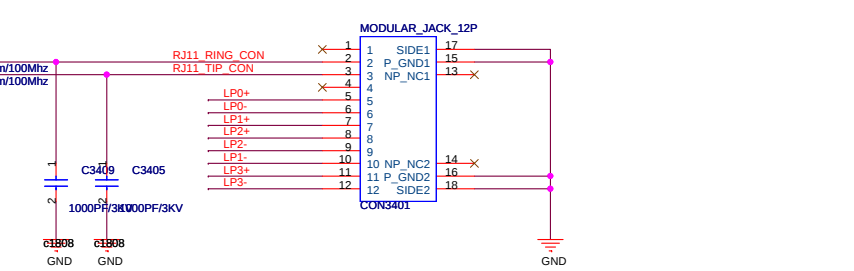
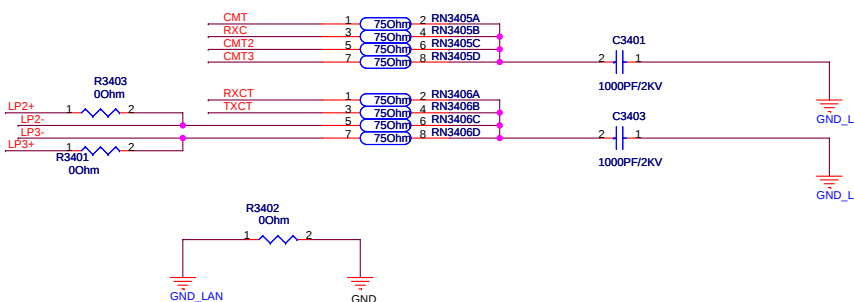


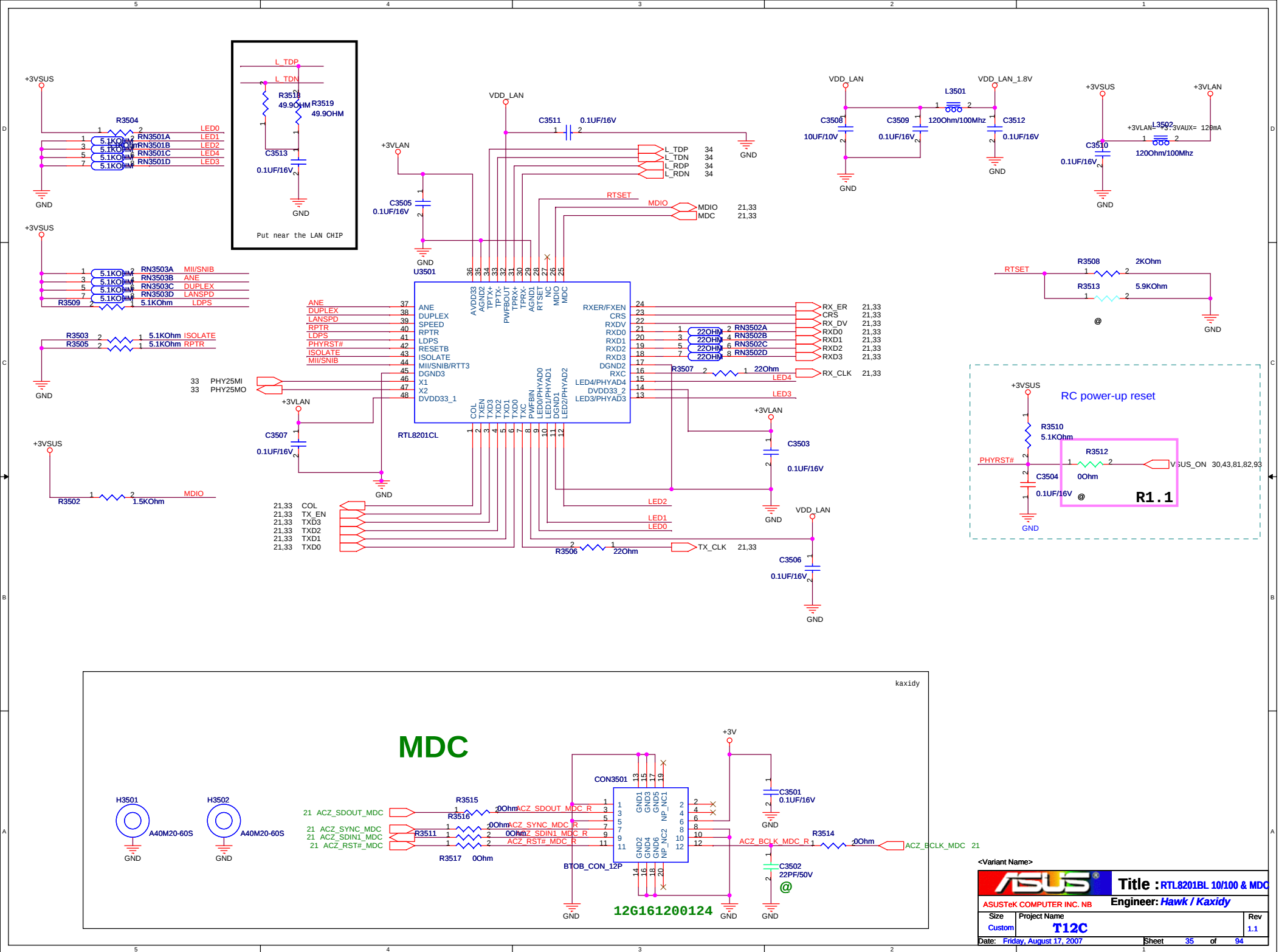
CON3402
WT08_CON_2P
P/N 12G17100002C

VDD_LAN_1.8V VDD_LAN_1.8V 35
+VLAN_2.5 +VLAN_2.5 21,33

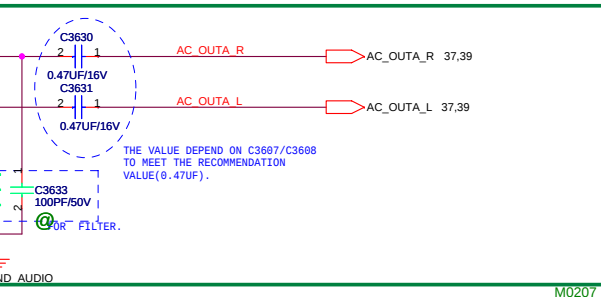


Gigabit LAN Option

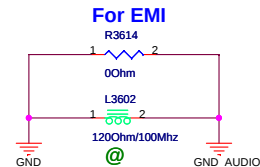
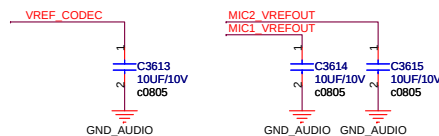
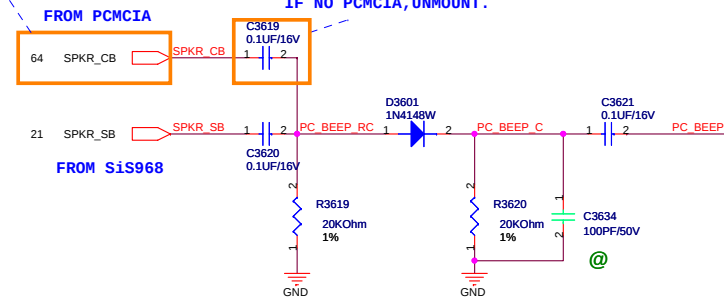




AUDIO POWER



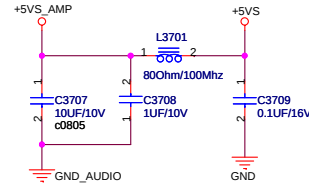
Reserve for Cardbus controller that has PCMCIA function.



Input impedance: 64K ohm(Typical)

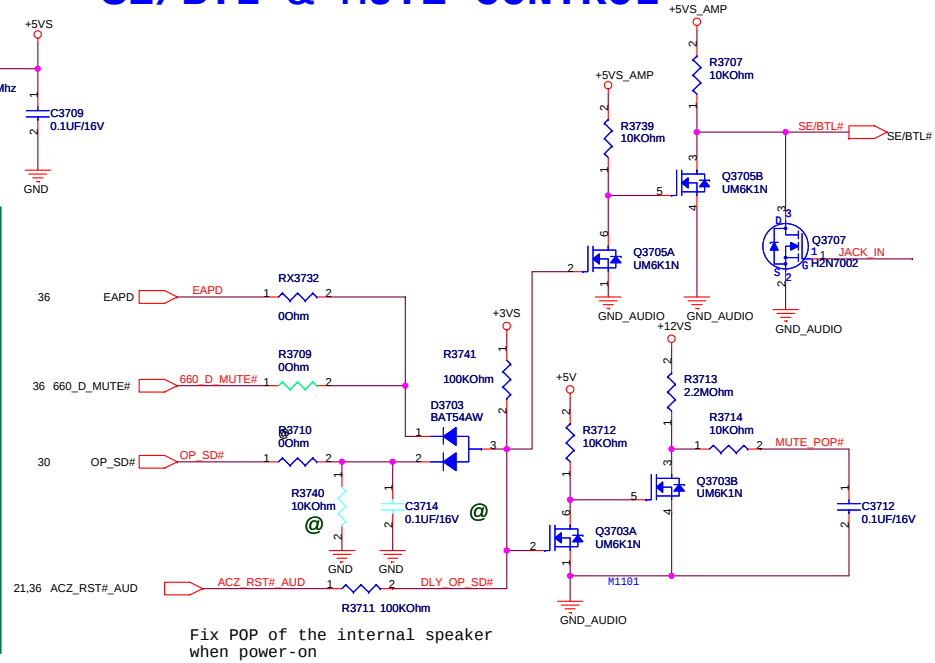
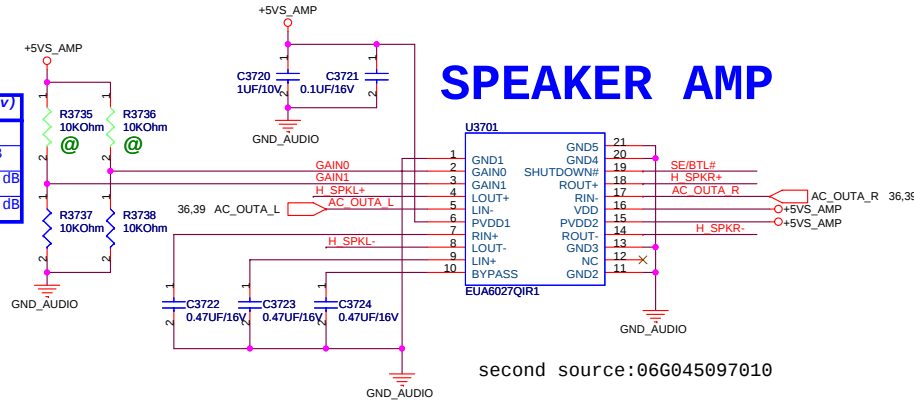
AMP POWER SE/BTL & MUTE CONTROL

+5VS_AMP 39
+5VS 21,30,32,36,38,45,50,51,56,57,80,91



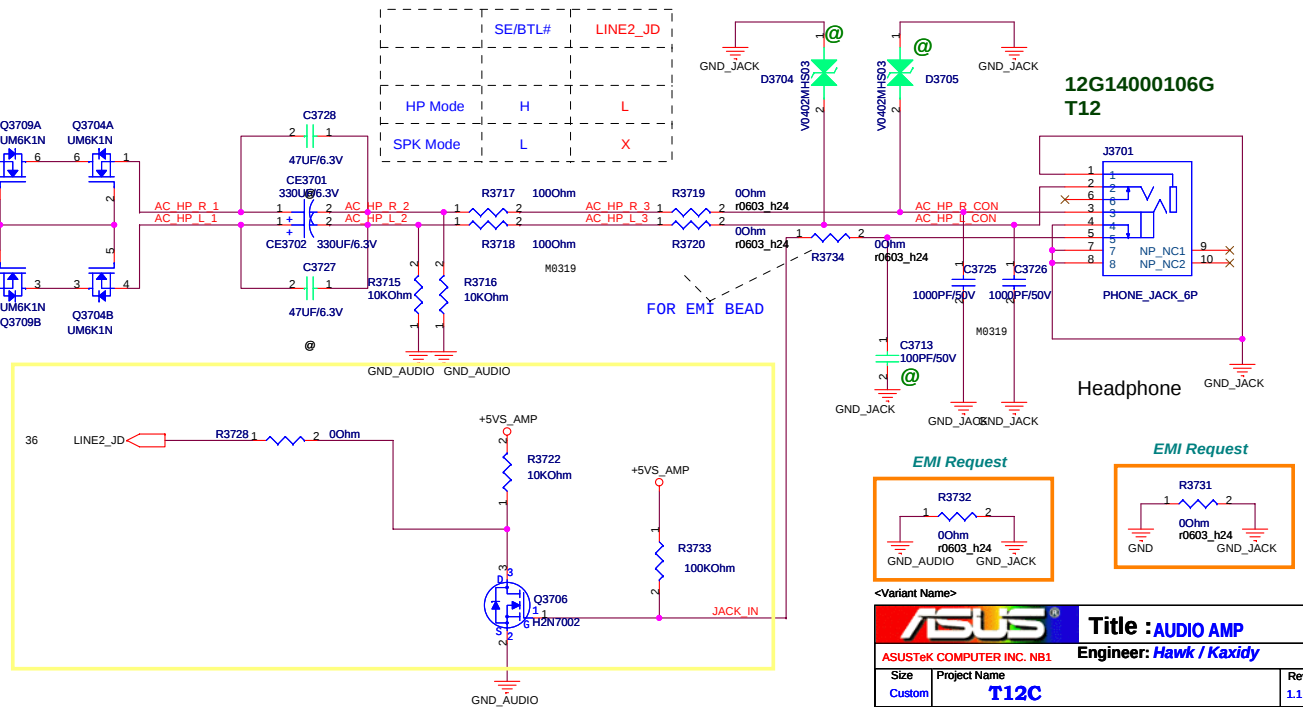
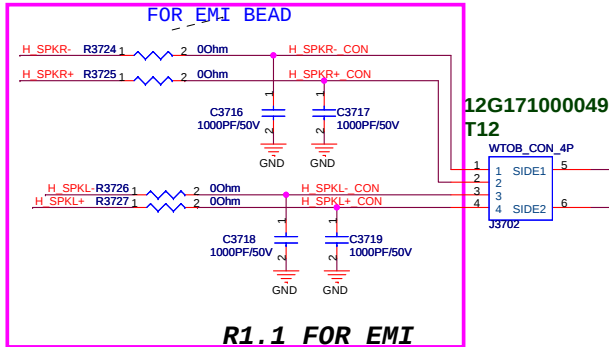
SPEAKER AMP

GAIN0	GAIN1	Av(1mv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



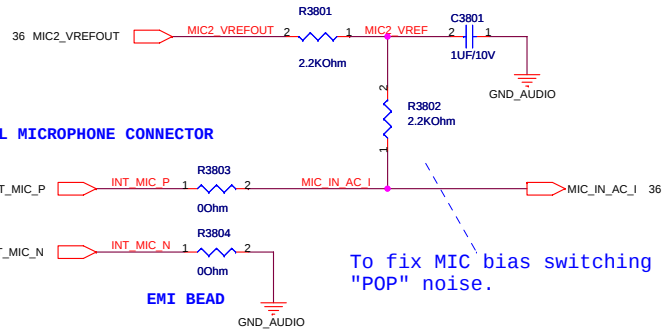
HP CONN

SPEAKER CONNECTOR



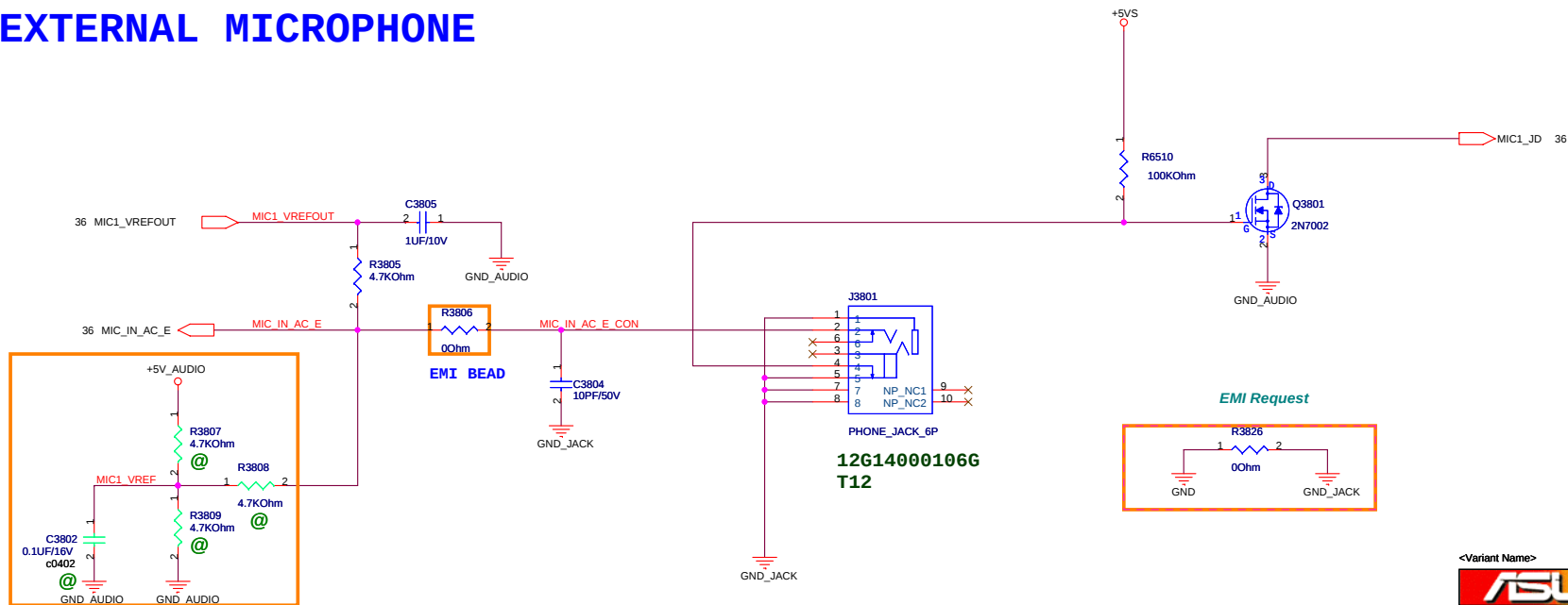
INTERNAL MICROPHONE

+5V_AUDIO 36
+5VS 21,30,32,36,37,45,50,51,56,57,80,91



To fix MIC bias switching
"POP" noise.

EXTERNAL MICROPHONE



Reserved the external MIC
bias(T filter).

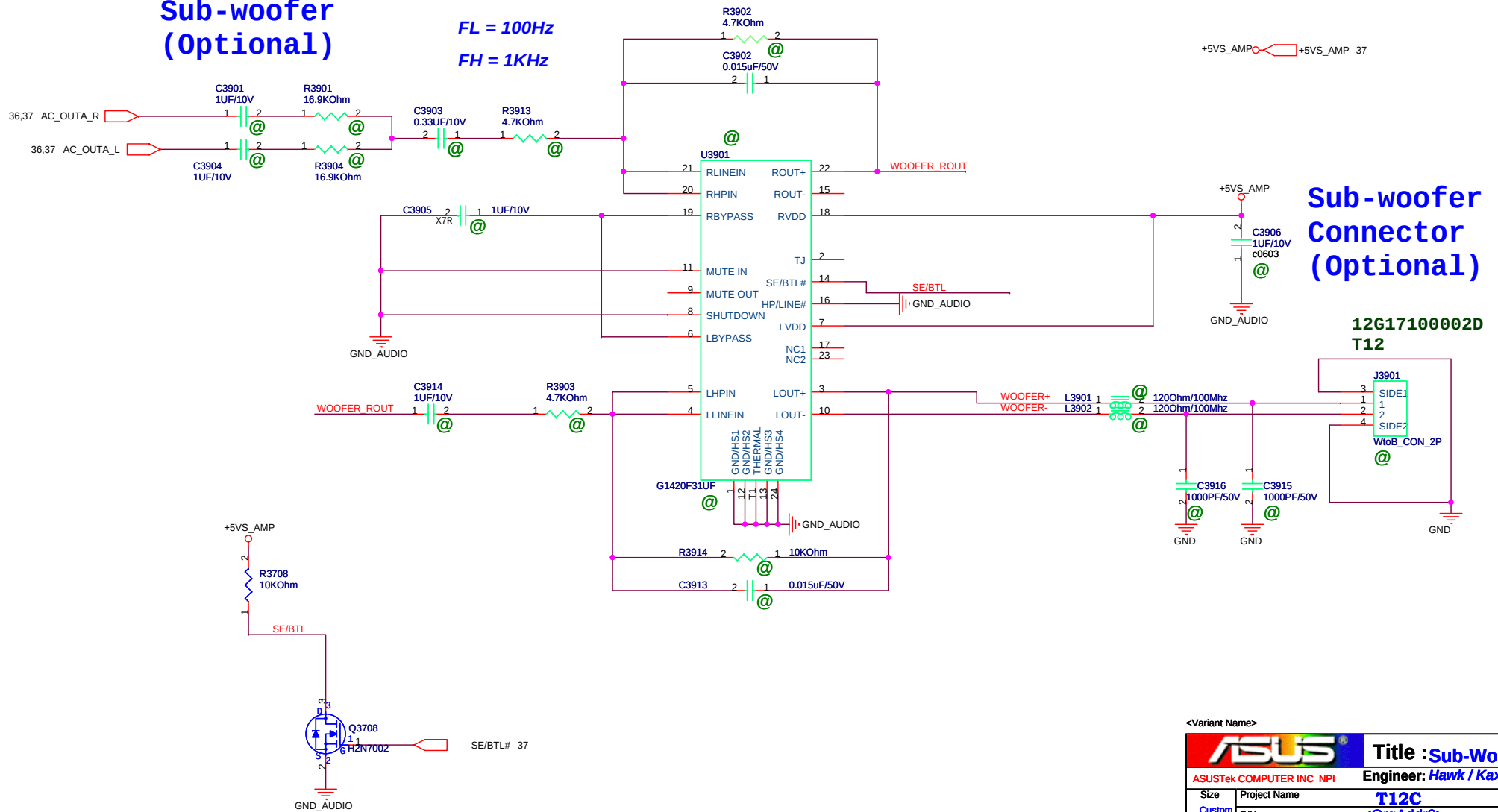
<Variant Name>

ASUS		Title : MICROPHONE	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, August 17, 2007		Sheet 38 of 94	

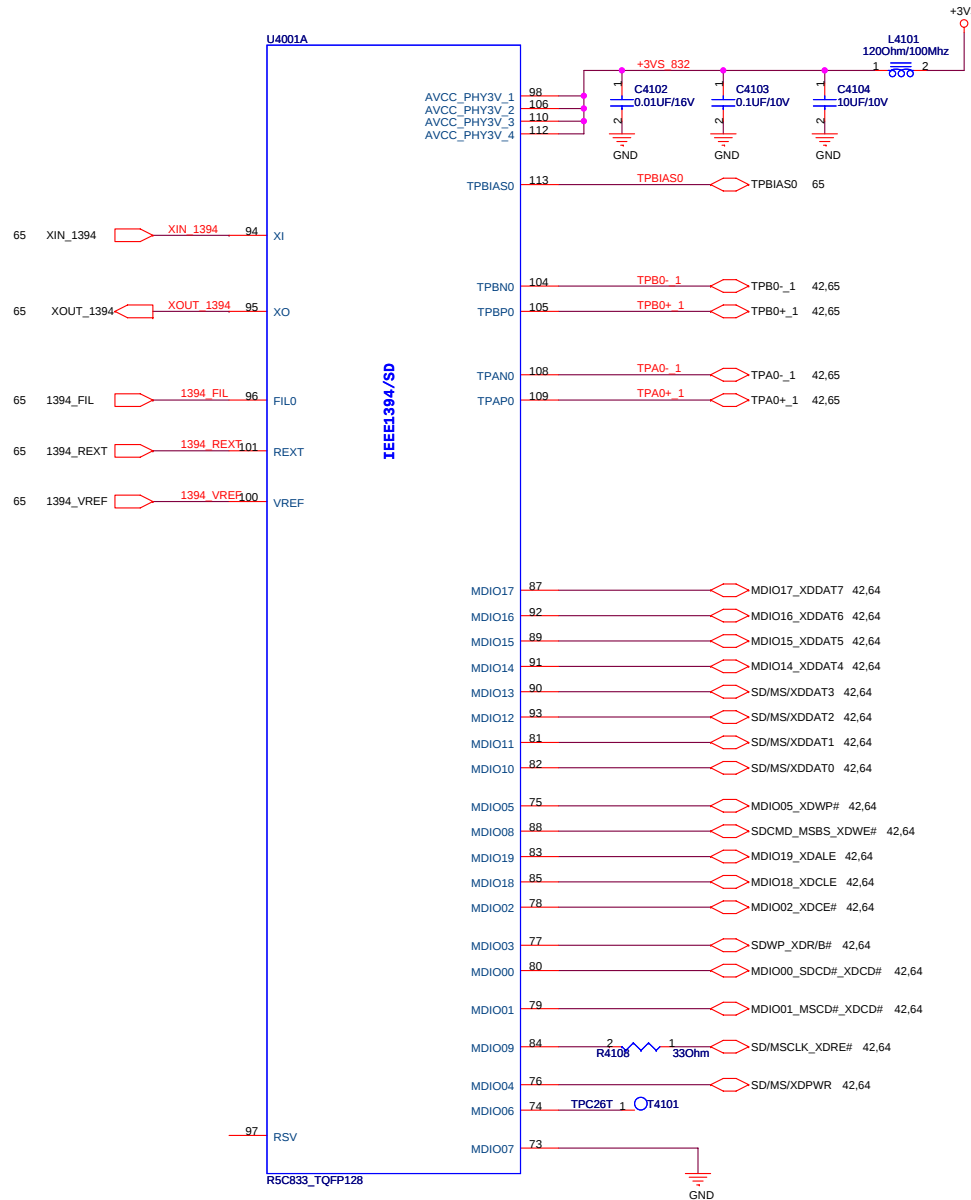
Sub-woofer (Optional)

FL = 100Hz

FH = 1KHz



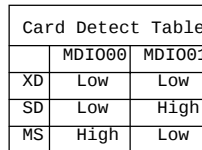
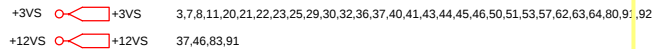
<Variant Name>		Title : Sub-Woofer	
ASUSTek COMPUTER INC. NPI		Engineer: Hawk / Kaxidy	
Size	Project Name	T12C	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Friday, August 17, 2007		Sheet 39 of 94	



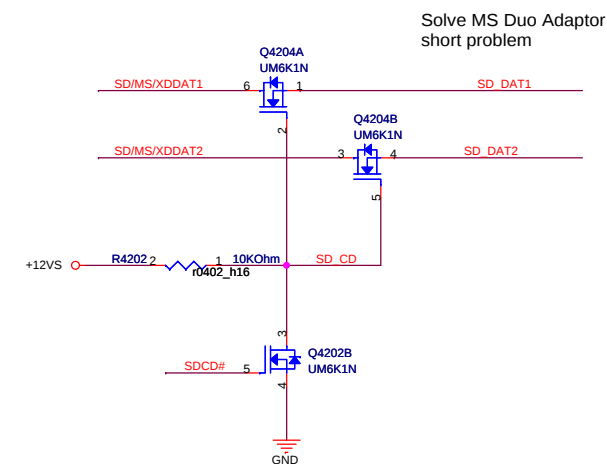
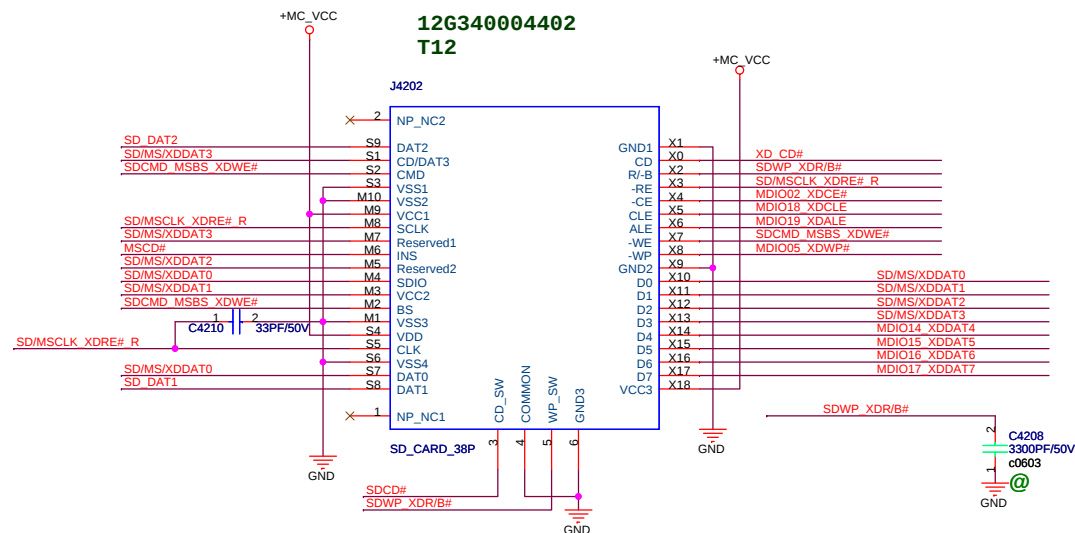
+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

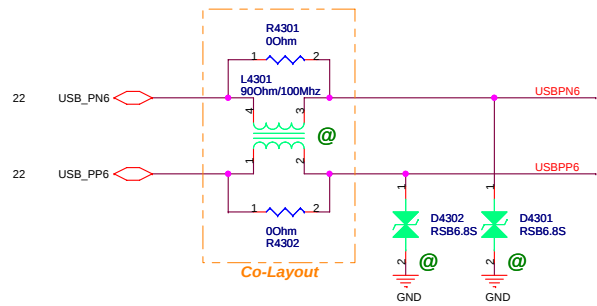
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE



For Memory Stick Duo Adaptor shielding ground issue

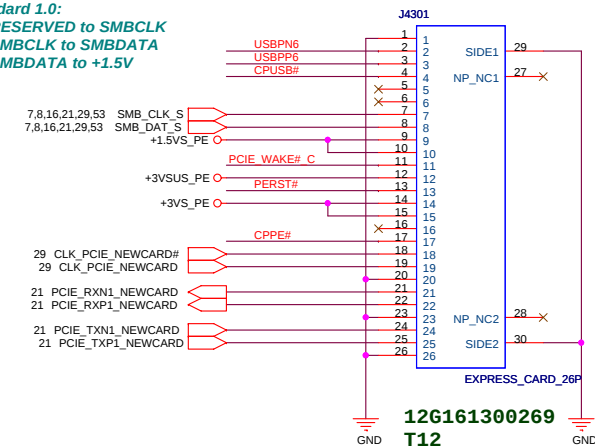


Solve MS Duo Adaptor
short problem



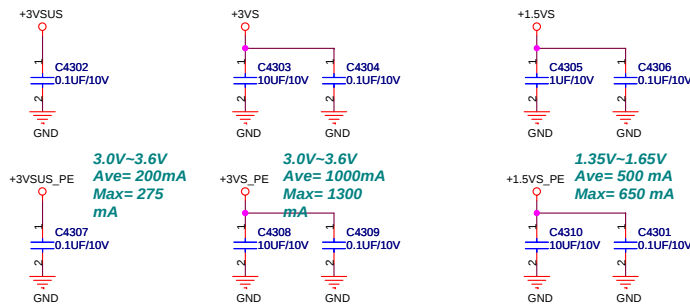
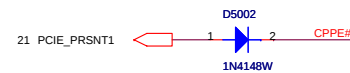
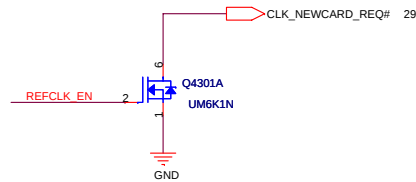
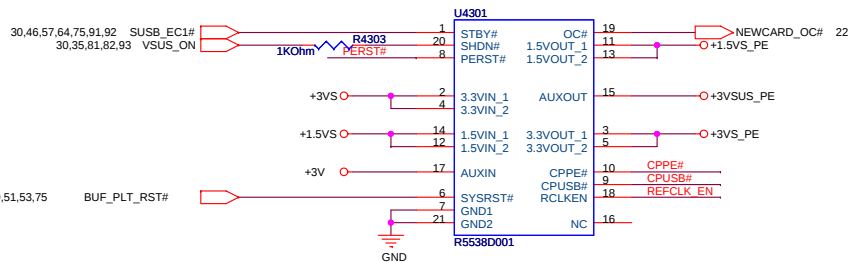
NewCard Header

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

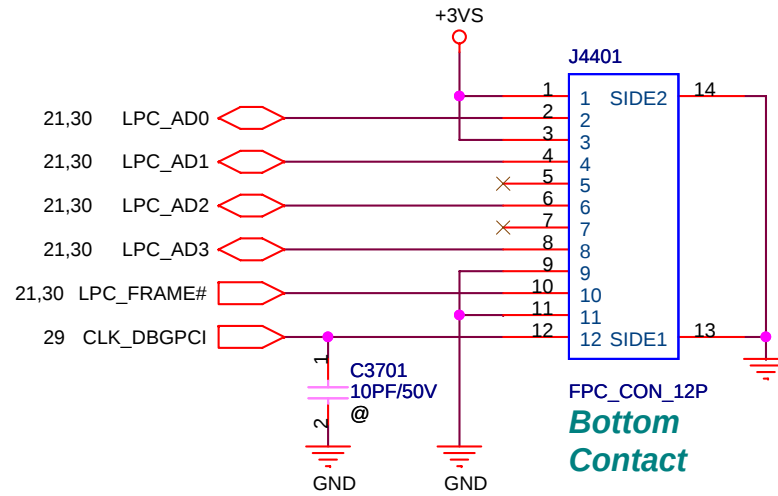


12G161300269
T12

J4302
P_GND1
P_GND2
CARD_EJECTOR_2P
@
12G219100002
T12



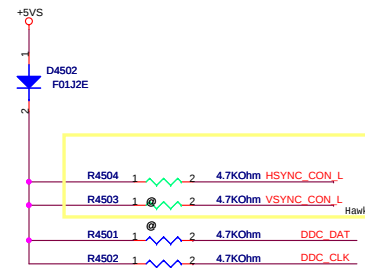
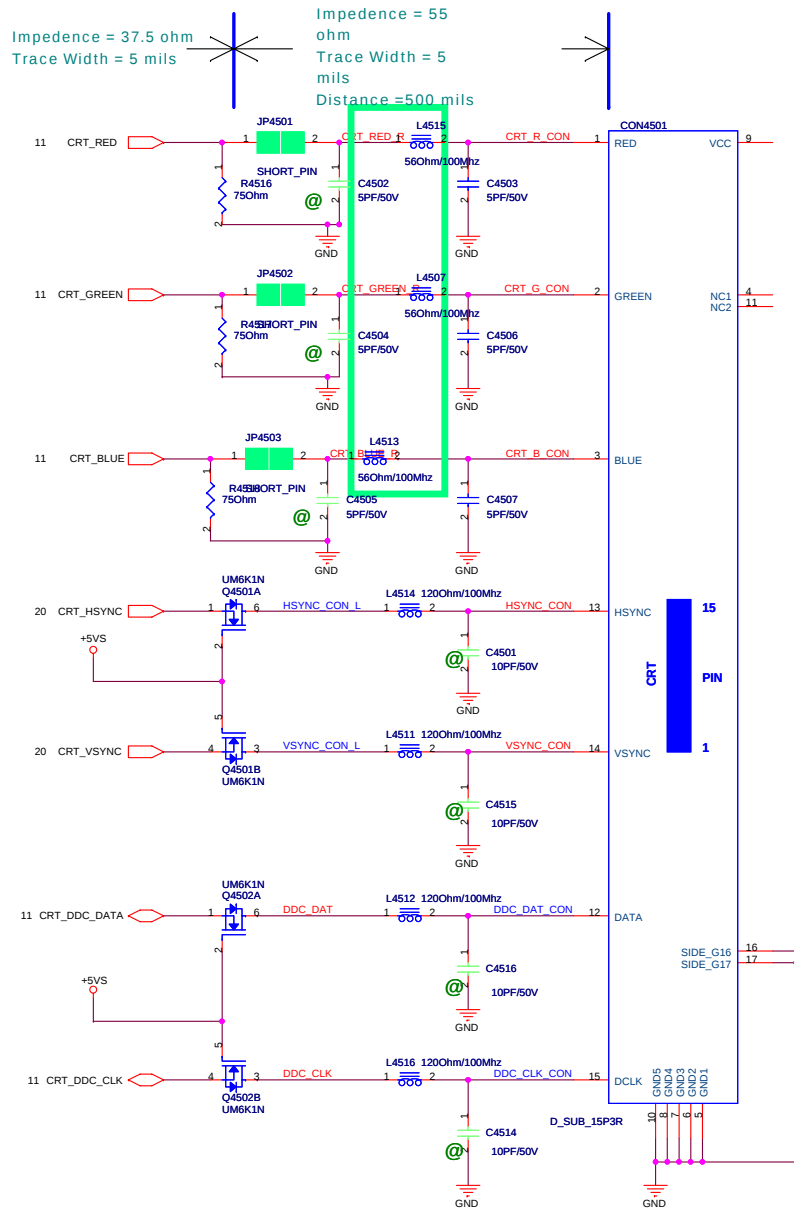
<Variant Name>



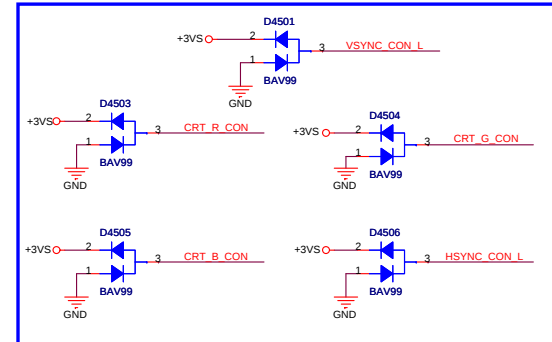
<Variant Name>

		Title : DEBUG	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Tuesday, February 26, 2008		Sheet 44 of 94	

CRT Connector

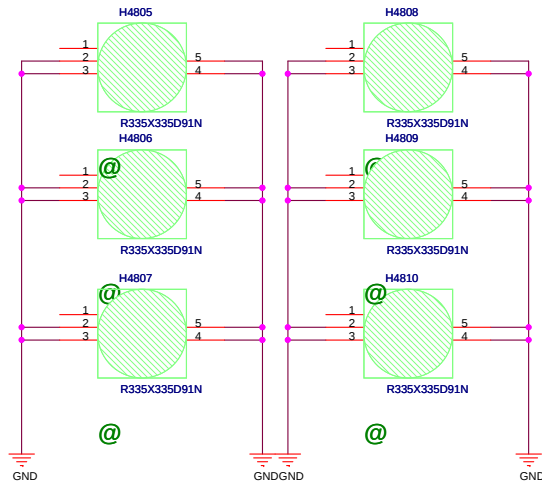


Place near to CRT Port

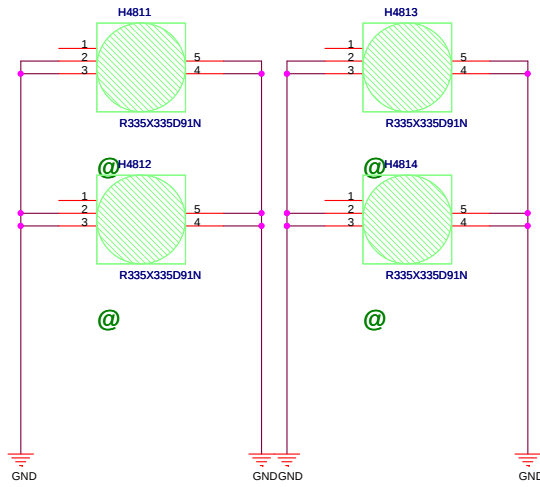


5					4					3					2					1				
D																								
C																								
B																								
A																								
															<Variant Name>									
															 Title : NULL									
															ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy									
Size					Project Name															Rev				
A					T12C															1.1				
Date: Monday, August 13, 2007															Sheet 47 of 94									
5					4					3					2					1				

A Hole / TOP Side



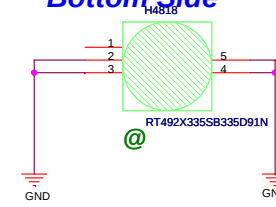
A Hole / Bottom Side



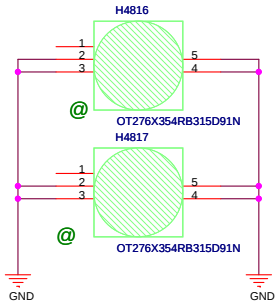
Drill Hole for Fix



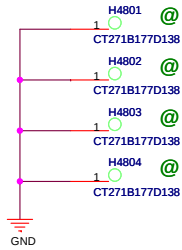
A Hole Special / Bottom Side



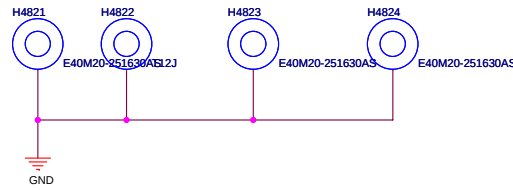
E Hole for Main board fix



F Hole for CPU

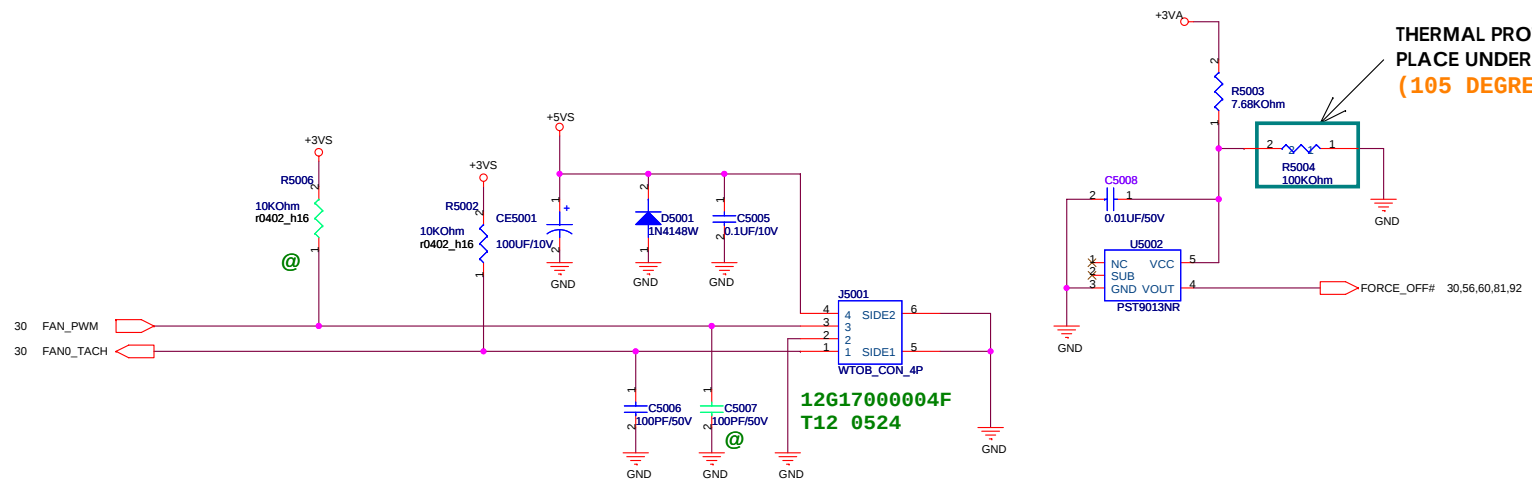


銅柱 Hole for VGA 13GNJ510M170-1



5					4		3		2		1	
D											D	
C											C	
B											B	
A											A	
									</			

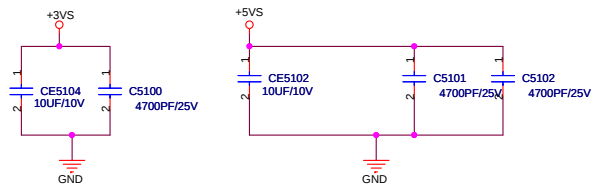
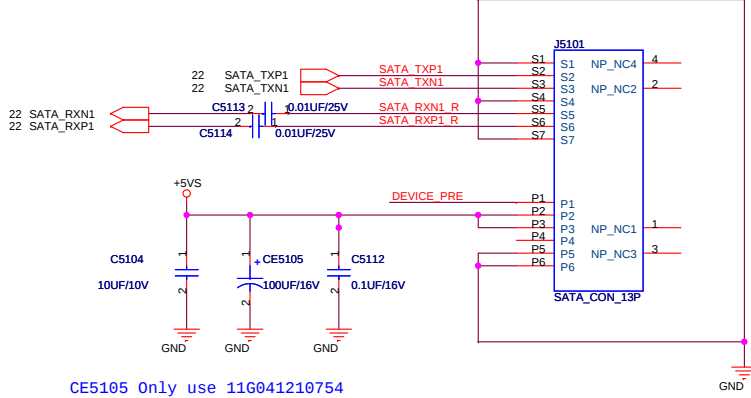
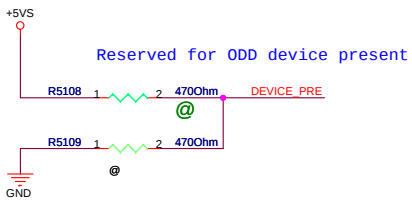
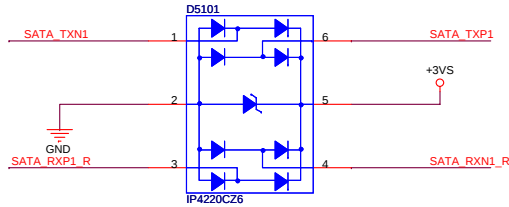
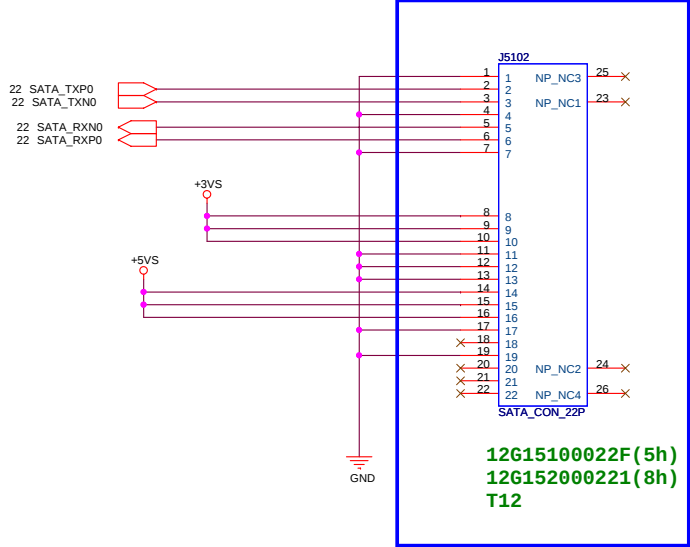
DC
FAN
Control

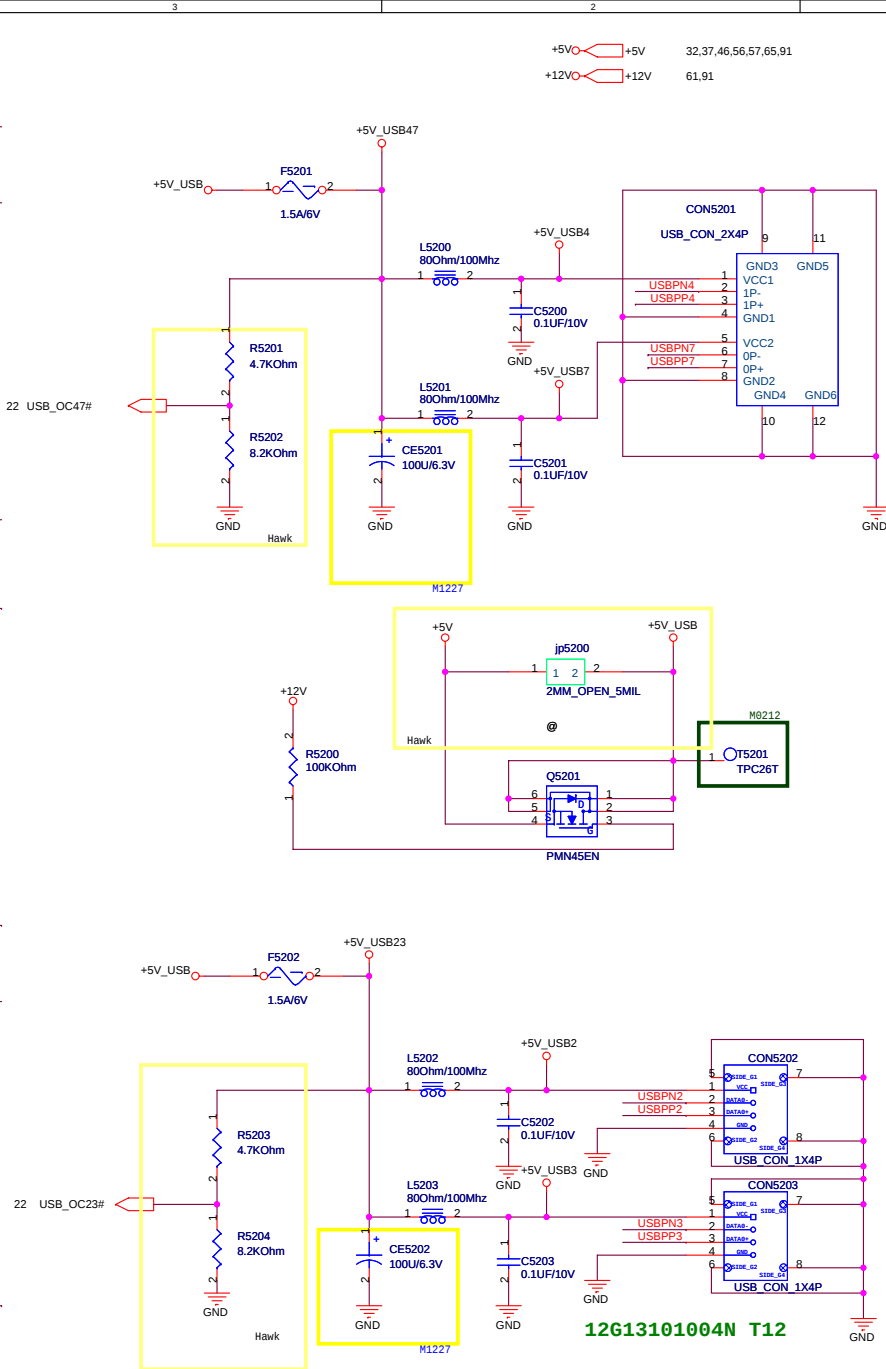
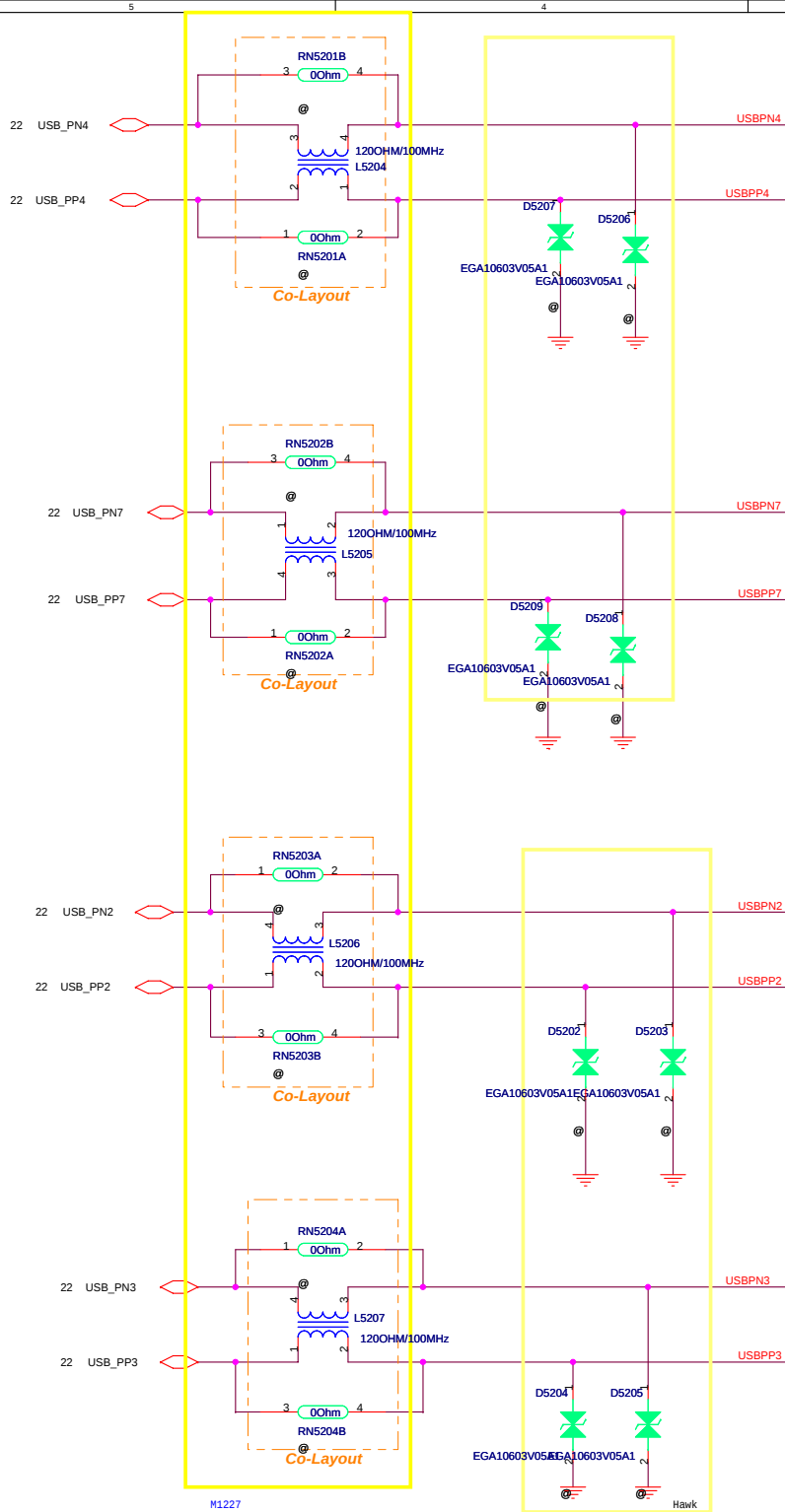


THERMAL PROTECTION
PLACE UNDER CPU
(105 DEGREE C)

SATA HDD

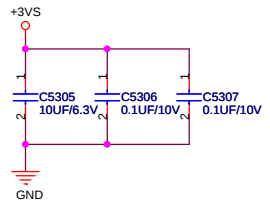
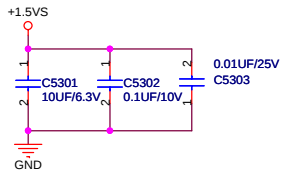
+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,53,57,62,63,64,80,91,92
+5VS 21,30,32,36,37,38,45,50,56,57,80,91



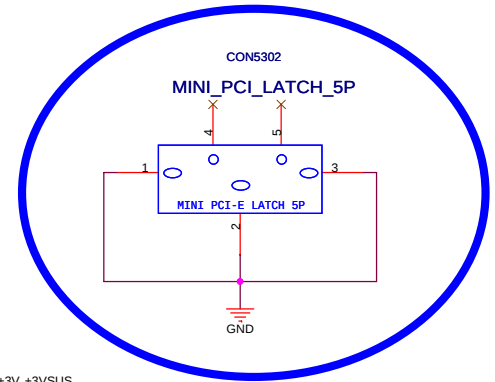


<Variant Name>

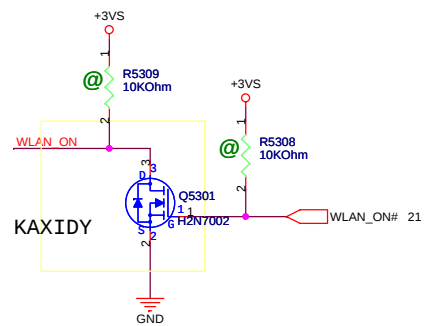
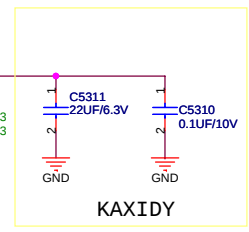
ASUS		Title :USB CONN X 4	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, August 17, 2007	Sheet	52	of 94



+3VS	+3VS	3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,57,62,63,64,80,91,92
+3V	+3V	20,23,35,40,46,57,61,62,64,65,91
+1.5VS	+1.5VS	4,11,43,57,83

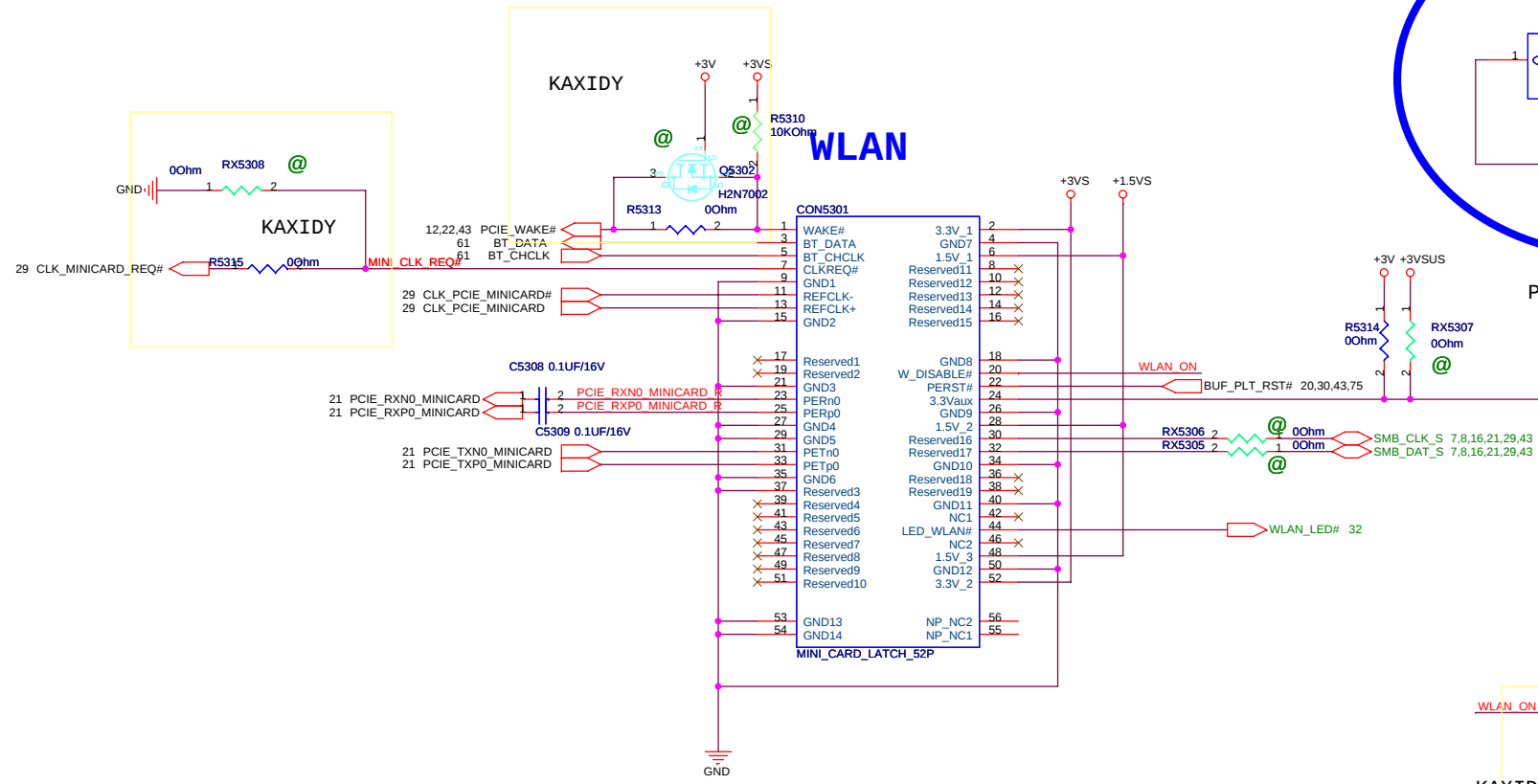


P/N: 12G162210052



<Variant Name>

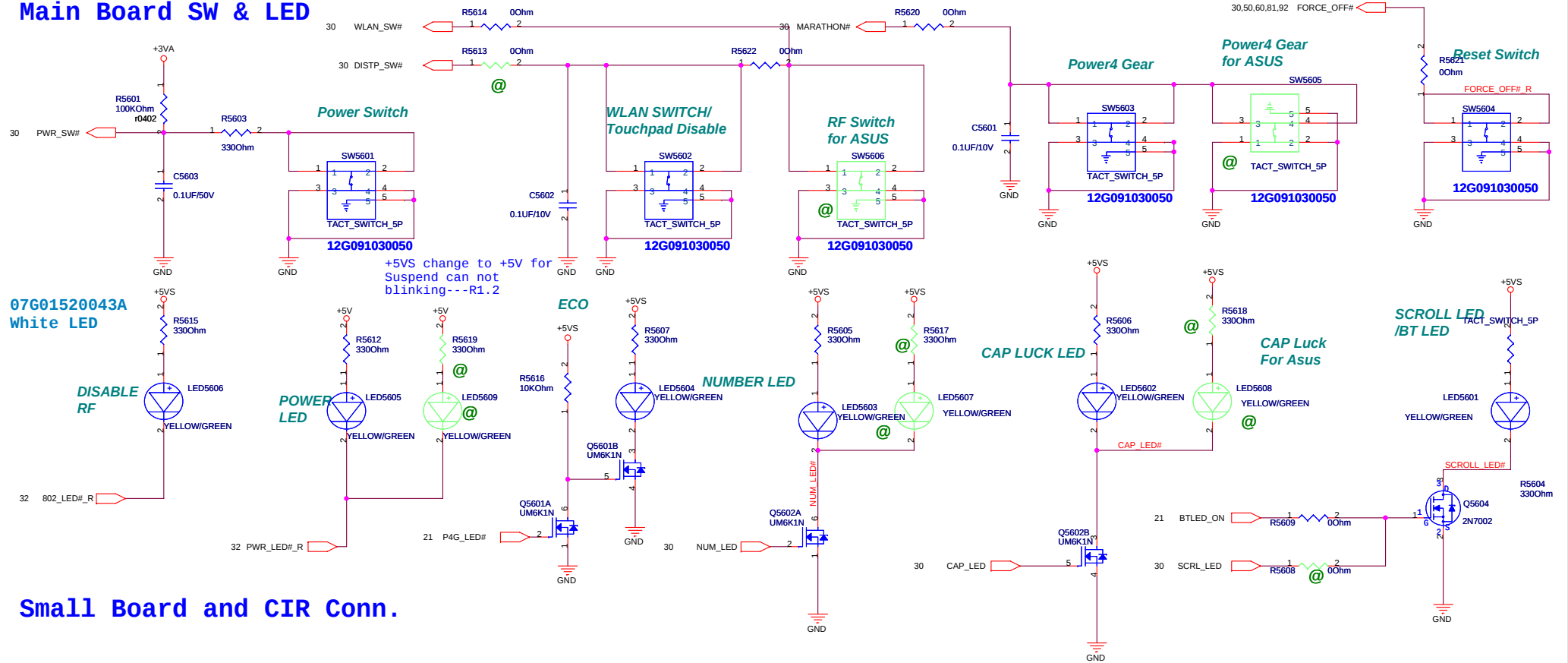
ASUS		Title : MINICARD	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, March 07, 2008	Sheet	53	of 94



5					4					3					2					1					
D																									
C																									
B																									
A																									
<Variant Name>																									
															Title : NULL										
															Engineer: Hawk / Kaxidy										
Size		Project Name																				Rev			
A		T12C																				1.1			
Date: Monday, August 13, 2007															Sheet 54 of 94										
5					4					3					2					1					

	5	4	3	2	1
D					D
C					C
B					B
A				<Variant Name> ASUS® Title : NULL ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy Size Project Name Rev A T12C 1.1 Date: Monday, August 13, 2007 Sheet 55 of 94	A
	5	4	3	2	1

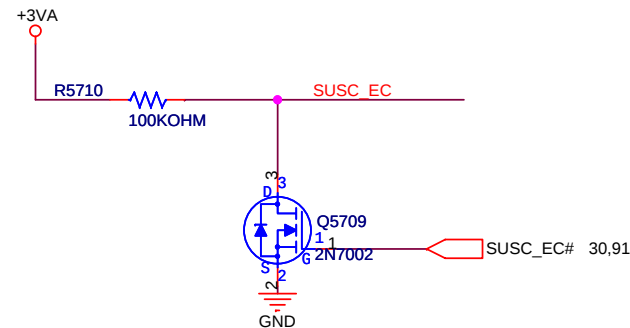
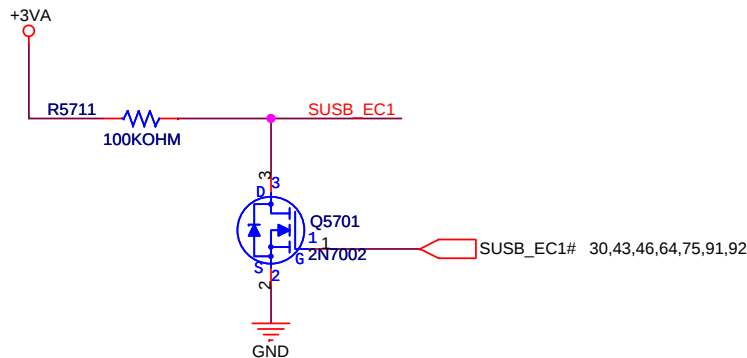
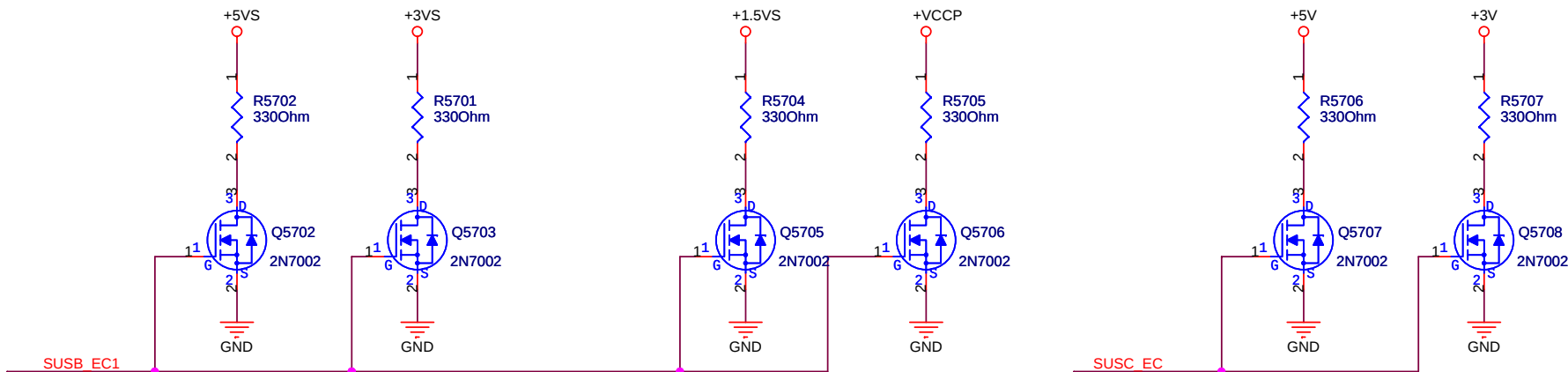
Main Board SW & LED



<Variant Name>

ASUS		Title : LED/SWITCH	
ASUSTek COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, March 07, 2008		Sheet	56 of 94

+3V	20,23,35,40,46,53,61,62,64,65,91
+5V	32,37,46,52,56,65,91
+VCCP	4,10,14,21,23,29,83,92
+1.5VS	4,11,43,53,83
+3VS	3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,62,63,64,80,91,92
+5VS	21,30,32,36,37,38,45,50,51,56,80,91





Title :DISCHARGE

ASUSTeK COMPUTER INC. NBEngineer: Hawk / Kaxidy

Size	Project Name	Rev
Custom	T12C	1.1

Date: Tuesday, March 04, 2008
Sheet 57 of 94

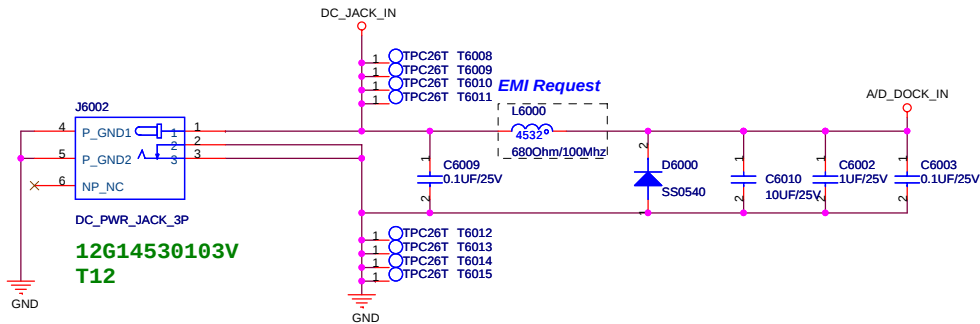
5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
A	T12C		1.1
Date: Monday, August 13, 2007		Sheet	58 of 94

	5	4	3	2	1
D					D
C					C
B					B
A				<Variant Name>  Title : NULL ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy Size Project Name Rev A T12C 1.1 Date: Monday, August 13, 2007 Sheet 59 of 94	A
	5	4	3	2	1

DC- IN



AC_BAT_SYS AC_BAT_SYS 80,81,82,88

BAT_CON BAT_CON 88

A/D_DOCK_IN A/D_DOCK_IN 88,90

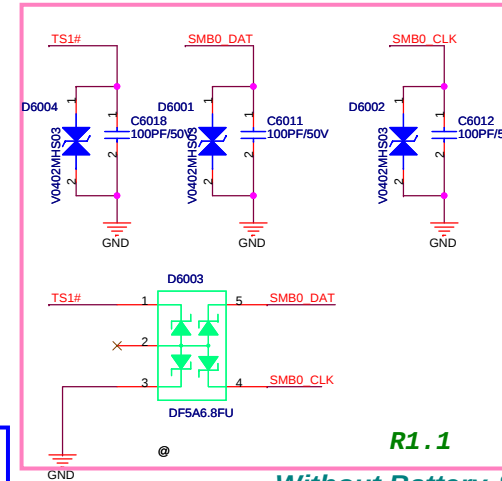
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.



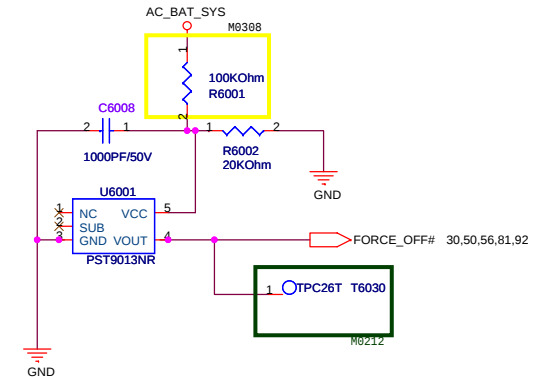
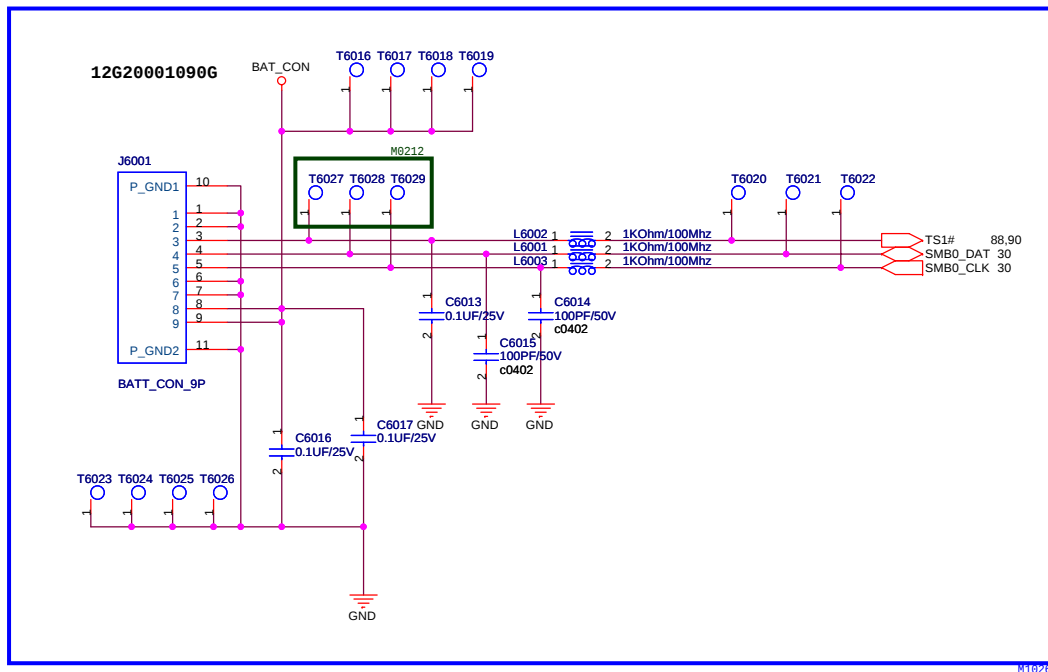
Note:

When we plug in or plug out the
battery, it may cause a spike to
damage the EC and gas gauge. It
needed to add these varistors to
protect those pins.

close to connector

Without Battery & Pull out Adapter

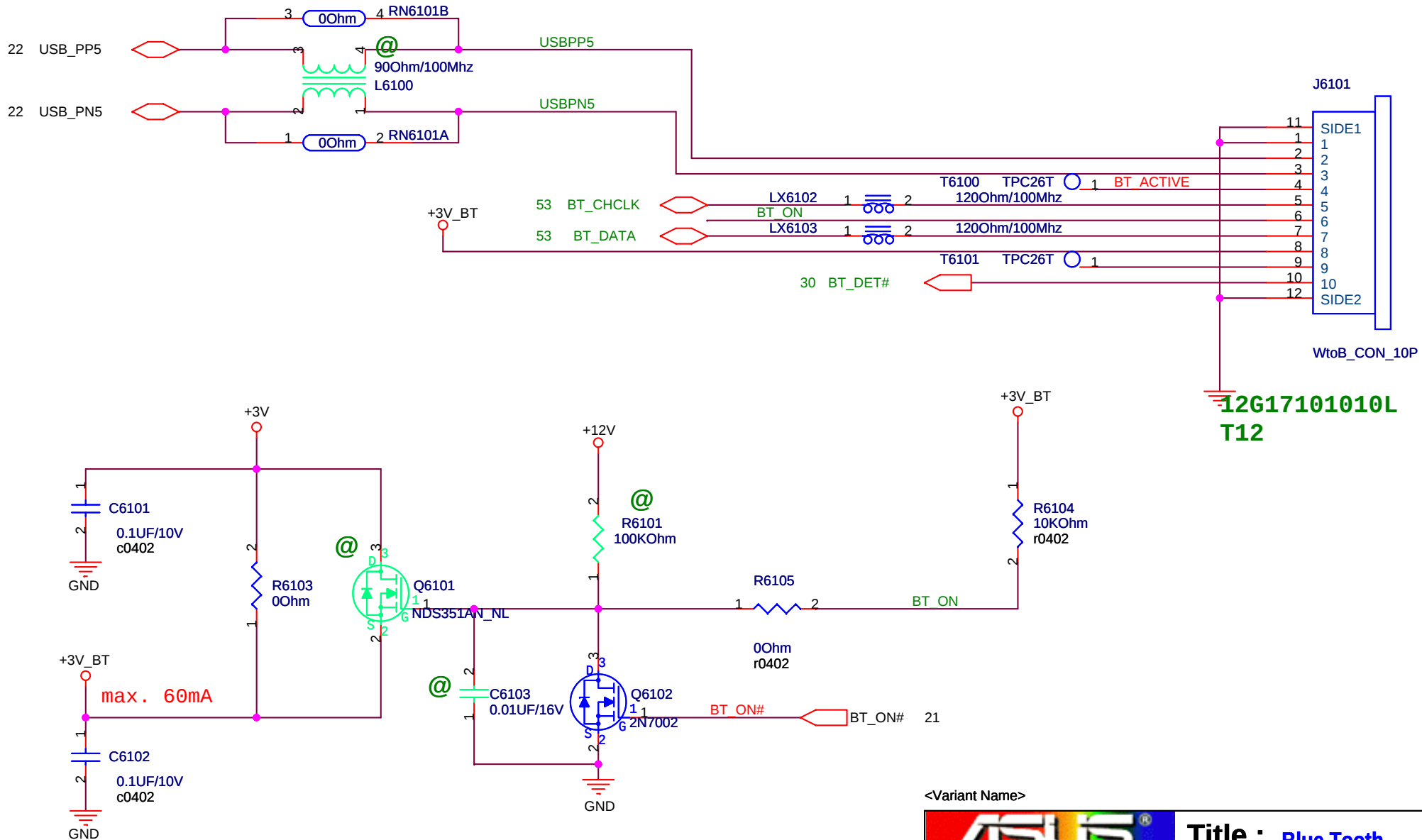
Battery Connector



<Variant Name>

ASUS		Title : DCIN/Batt conn.	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Friday, August 17, 2007	Sheet	60	of 94

BLUETOOTH CONNECTOR



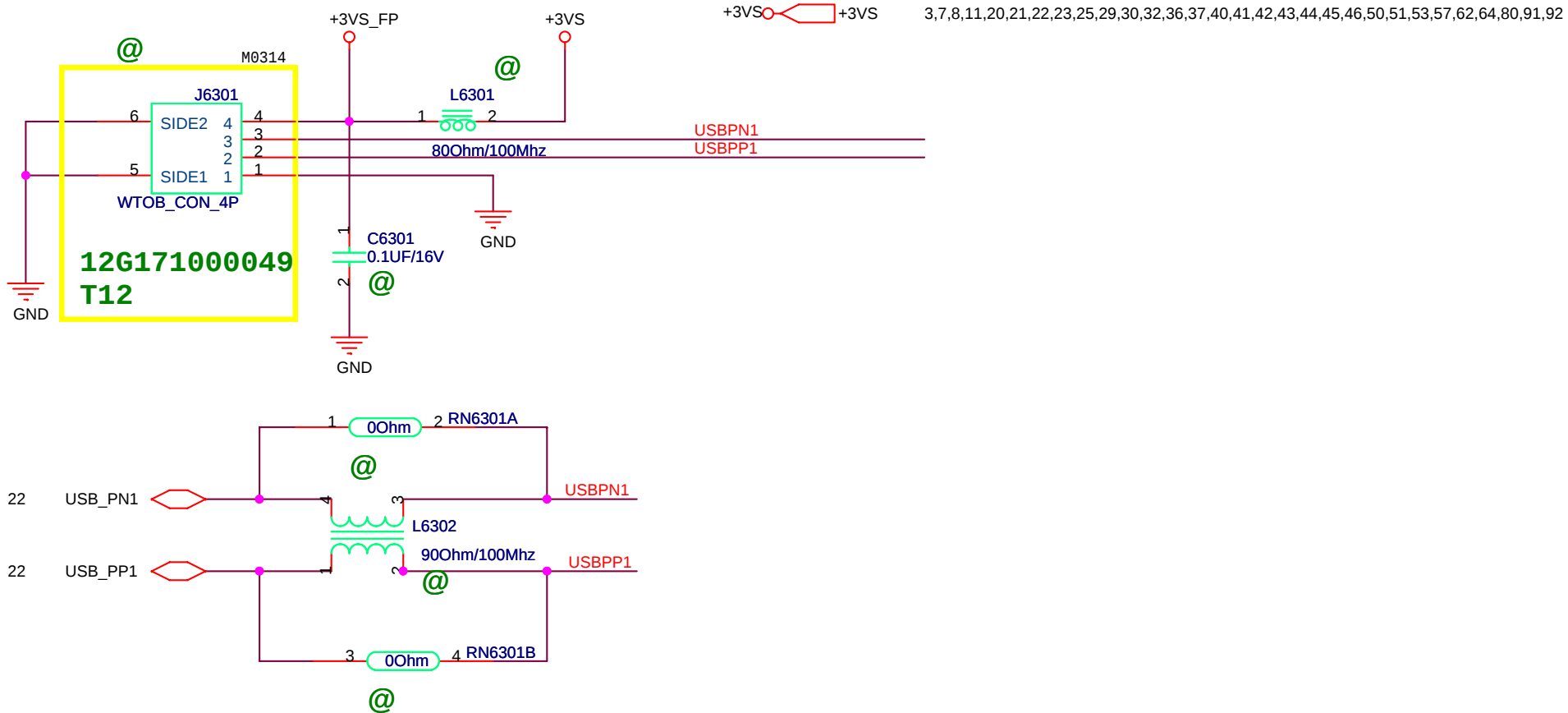
<Variant Name>

ASUS		Title : Blue Tooth	
ASUSTek COMPUTER INC .NB		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Friday, August 17, 2007		Sheet 61 of 94	

TPM Connector

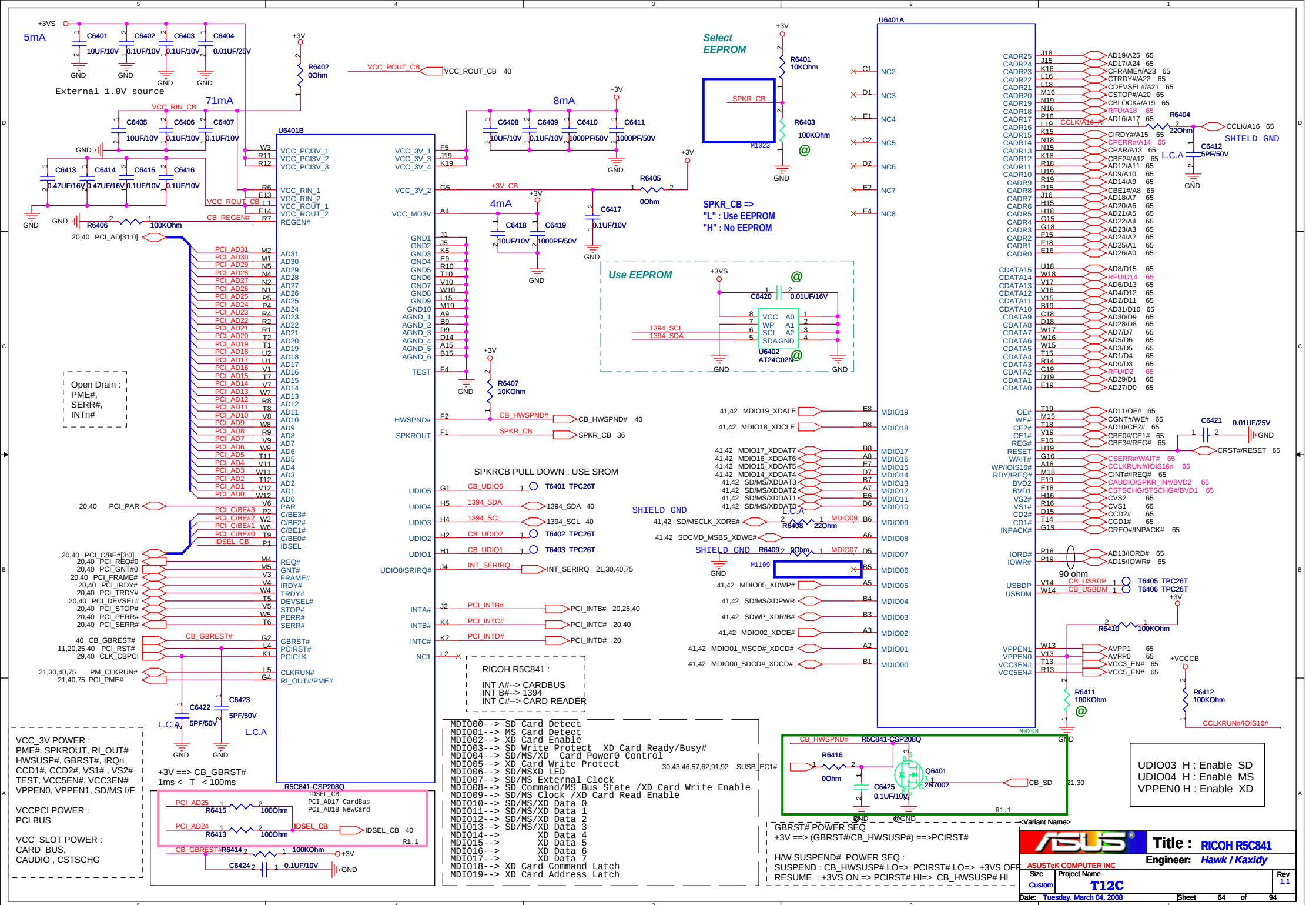
<Variant Name>

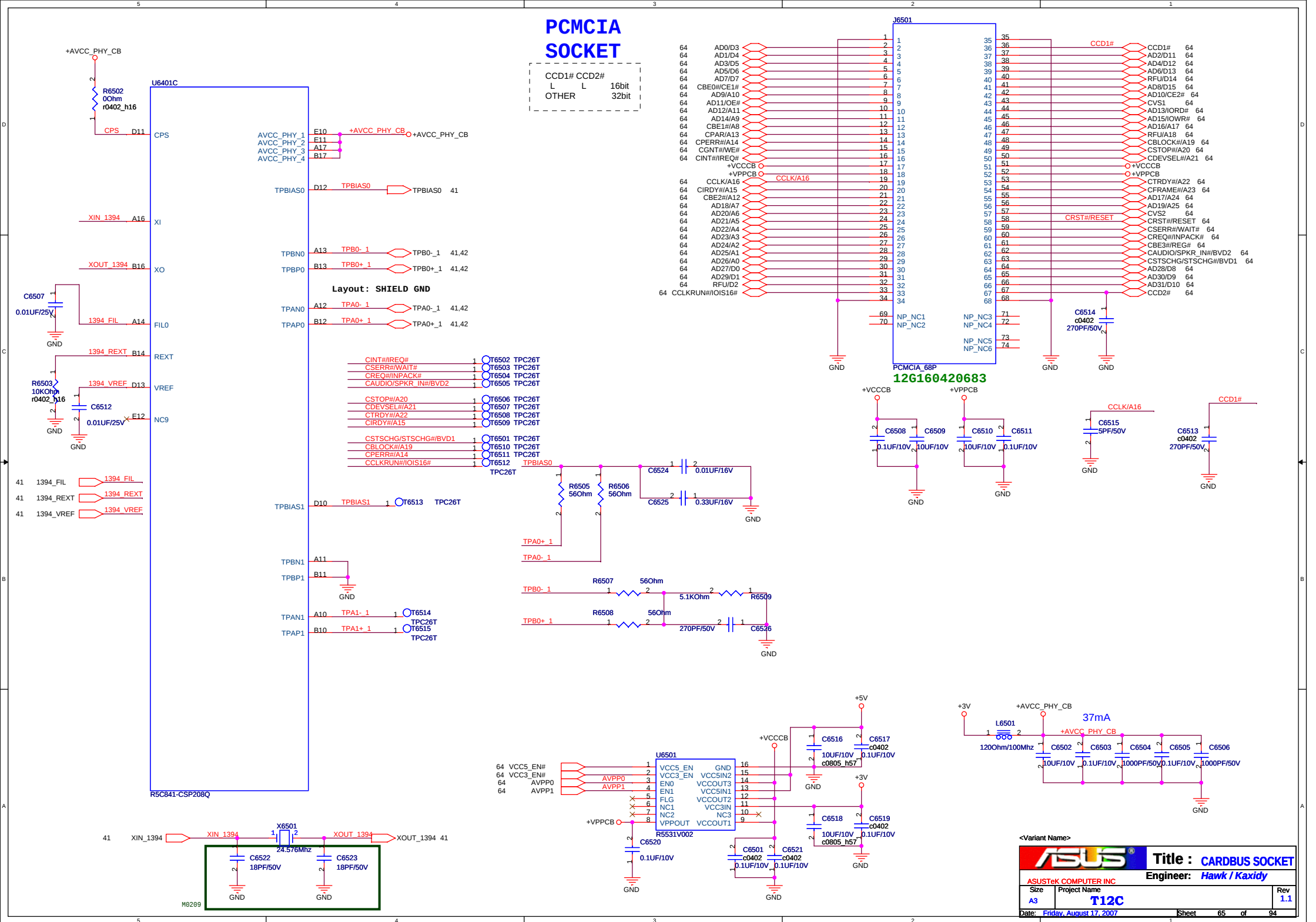
		Title : TPM	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>	
Size A	Project Name T12C		Rev 1.1
Date: <u>Tuesday, March 04, 2008</u>		Sheet	62 of 94



<Variant Name>

ASUS®		Title :Finger Print	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Friday, August 17, 2007		Sheet	63 of 94





D

C

3

A

<Variant Name>



Title : eSATA

ASUSTeK COMPUTER INC

Engineer: *Hawk / Kaxidy*

Size
Custom

Project Name	T12C
--------------	-------------

Rev	
1.1	

Date: Monday, August 13, 2007

Sheet 66 of 94

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD15	2	D
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

D

C

B

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: *Hawk / Kaxidy*

Size

A

Project Name

T12C

Rev

1.1

Date: Monday, August 13, 2007

Sheet	68	of	94
-------	----	----	----

	5	4	3	2	1
D					D
C					C
B					B
A					A

<Variant Name>

		Title : NULL		
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy		
Size A	Project Name T12C			Rev 1.1
Date: Monday, August 13, 2007		Sheet	69	of 94

5					4					3					2					1				
D																								
C																								
B																								
A																								
<Variant Name>															 Title : NULL									
ASUSTeK COMPUTER INC															Engineer: Hawk / Kaxidy									
Size			Project Name												Rev									
A			T12C												1.1									
Date: Monday, August 13, 2007															Sheet 70 of 94									
5					4					3					2					1				

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

		Title : NULL		
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy		
Size A	Project Name T12C			Rev 1.1
Date: Monday, August 13, 2007		Sheet	71	of 94

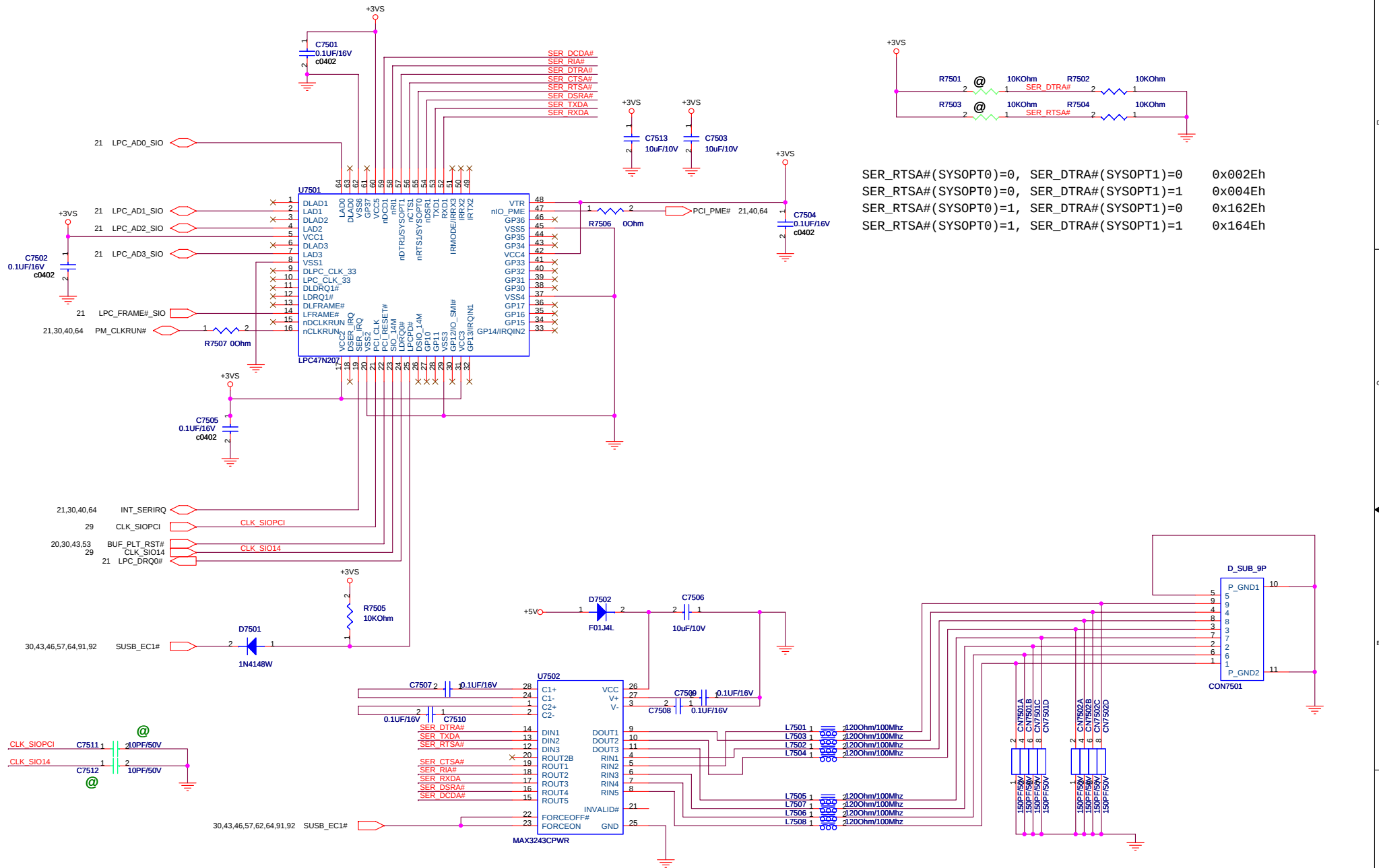
	5	4	3	2	1
D					D
C					C
B					B
A				<Variant Name> ASUS® Title : NULL ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy Size Project Name Rev A T12C 1.1 Date: Monday, August 13, 2007 Sheet 72 of 94	A
	5	4	3	2	1

																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																													</	
--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	----	--

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

		Title : NULL		
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy		
Size A	Project Name T12C			Rev 1.1
Date: Monday, August 13, 2007		Sheet	74	of 94



```

SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=0 0x002Eh
SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=1 0x004Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=0 0x162Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=1 0x164Eh

```

5					4					3					2					1				
D																								
C																								
B																								
A																								
										Title : Null														
ASUSTeK COMPUTER INC										Engineer: Hawk / Kaxidy														
Size Custom		Project Name T12C																		Rev 1.1				
Date: Tuesday, February 26, 2008										Sheet 76 of 94														

	5	4	3	2	1
D					D
C					C
B					B
A					A
				<Variant Name> ASUS® Title : NULL ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy SizeA Project NameT12C Rev1.1 Date: Monday, August 13, 2007 Sheet 77 of 94	
	5	4	3	2	1

5	4	3	2	1
D				D
C				C
B				B
A				A

<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size A	Project Name T12C		Rev 1.1
Date: Monday, August 13, 2007		Sheet	78 of 94

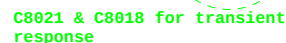
Change Note:

R1.1 :

- 1. Reserve LVDS Up and Low channel of VGA side.
- 2. Change R3404 R3405 to 0ohm for LAN disconnect issue.
- 3. Change U3302 U3303 for new part.
- 4. Add D6004/D6003 for optional
- 5. Add R3114,R3115
- 6. Add Q3301,Q3302,R3341,R3342, C3329,C3330
- 7. Change IDSEL_CB to AD24/AD25. p64
- 8. add R6416 to CB_HWSPND#. P65
- 9. add Q3709 for depop issue. P37
- 9. change Q9203 TO Q3705B for ref error.

R2.0 :

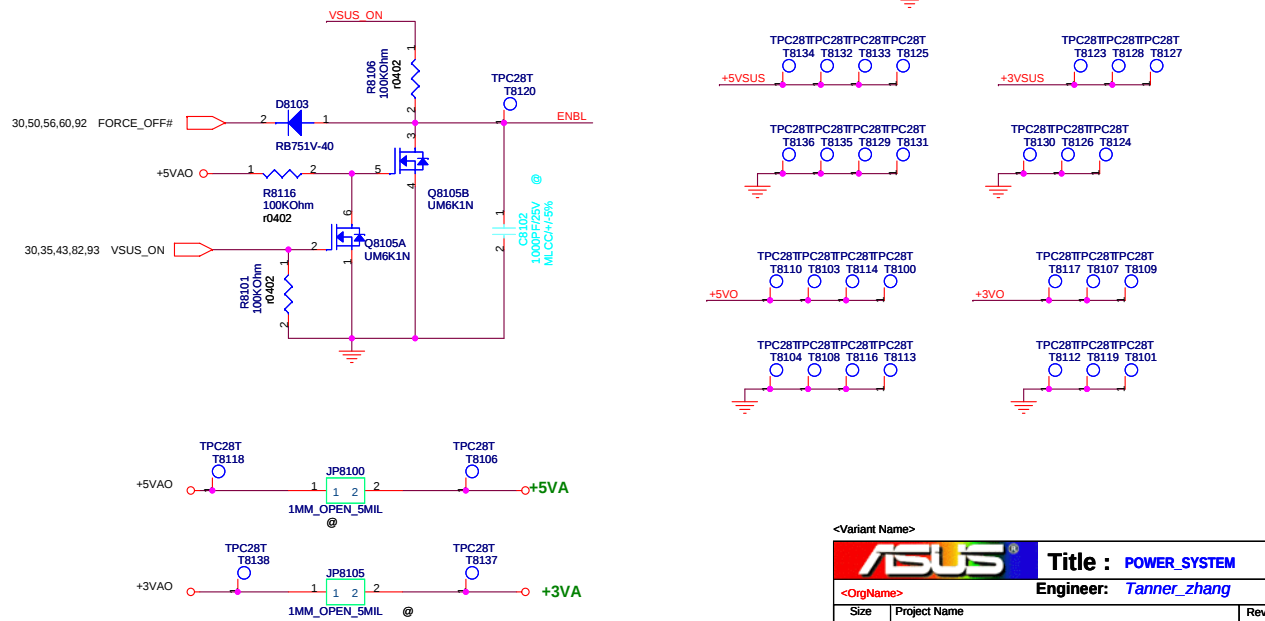
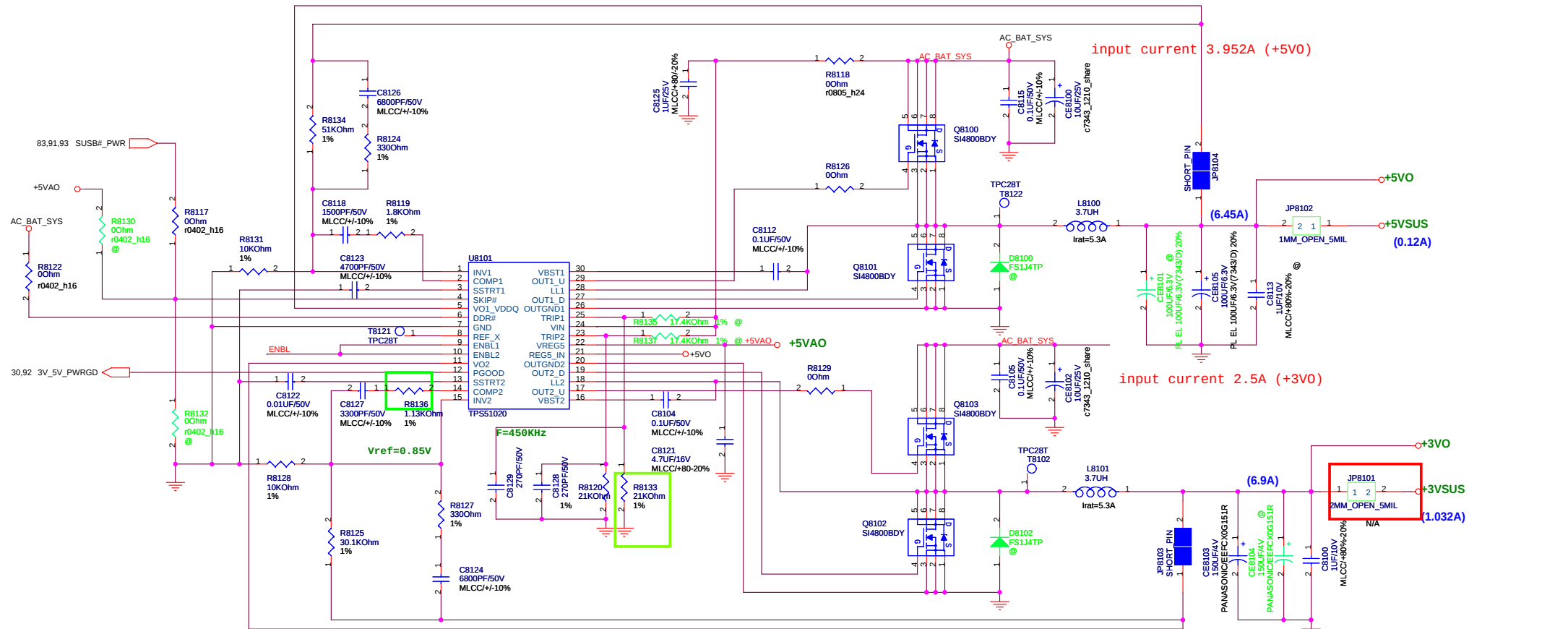
- 1. Add C3202/C4210 /R4216 for EMI
- 2. Add R4607 and change Q4603 for LCD VCC
- 3. Add C2530,C2545,C2546,C2547,C2548,C2549,C2550,C2551,C2552,C2553,C2554,C2555

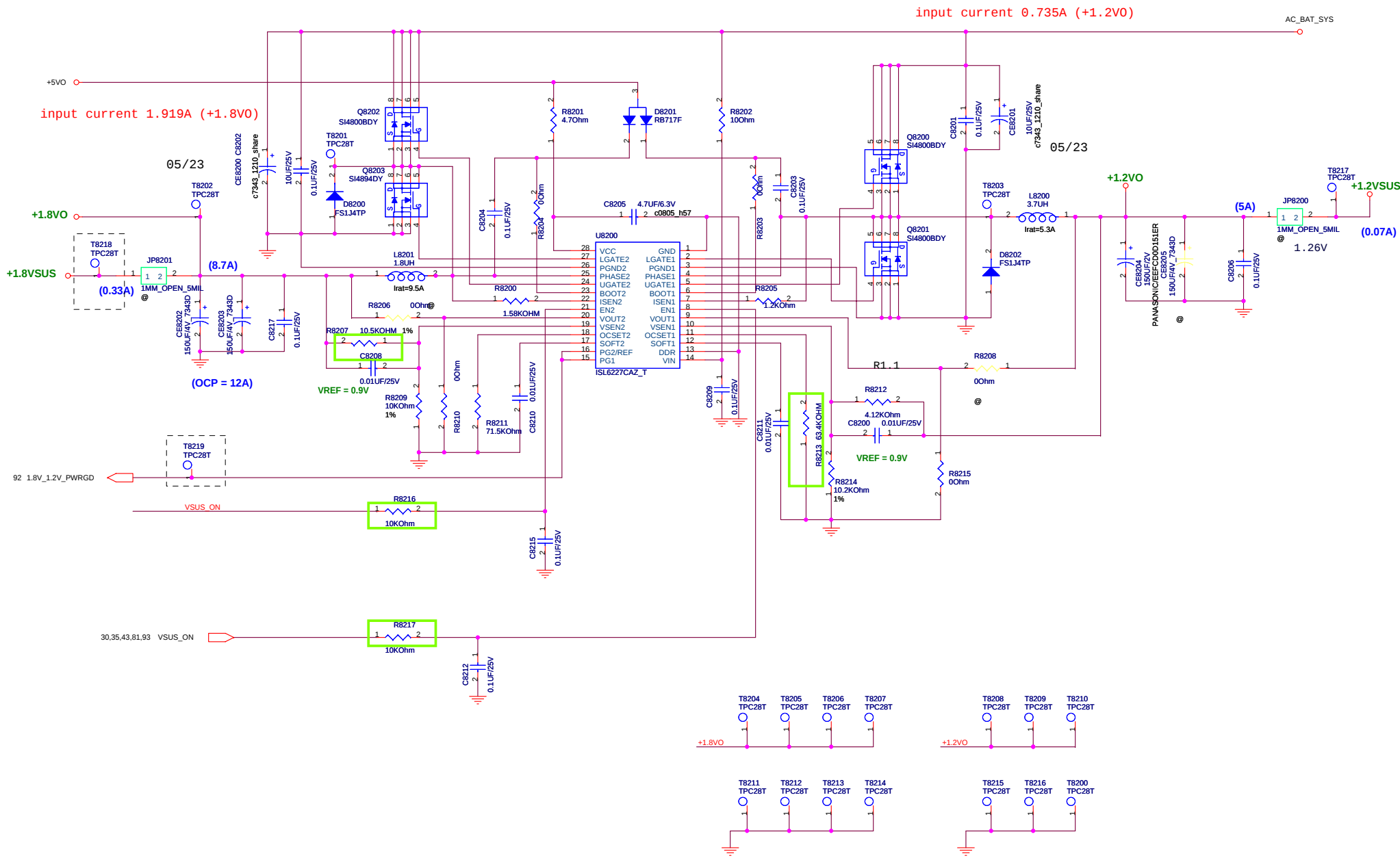


Engineer: *Tanner Zhang*

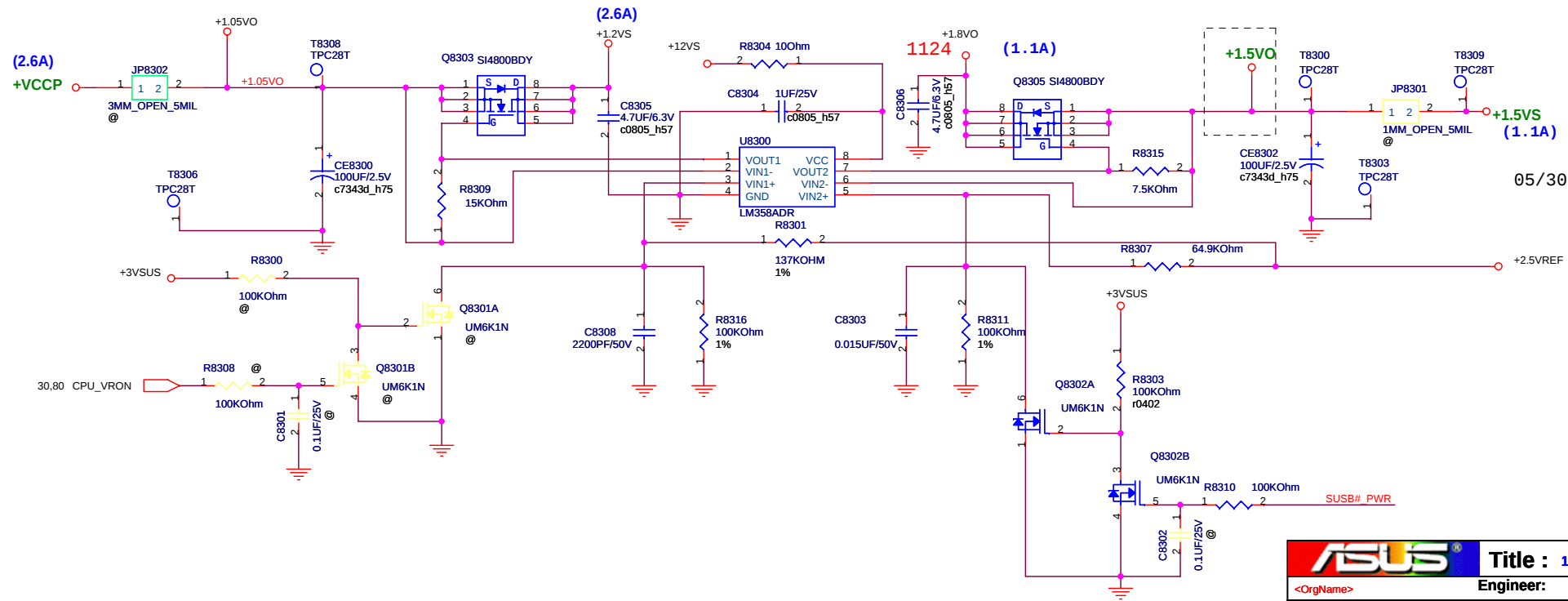
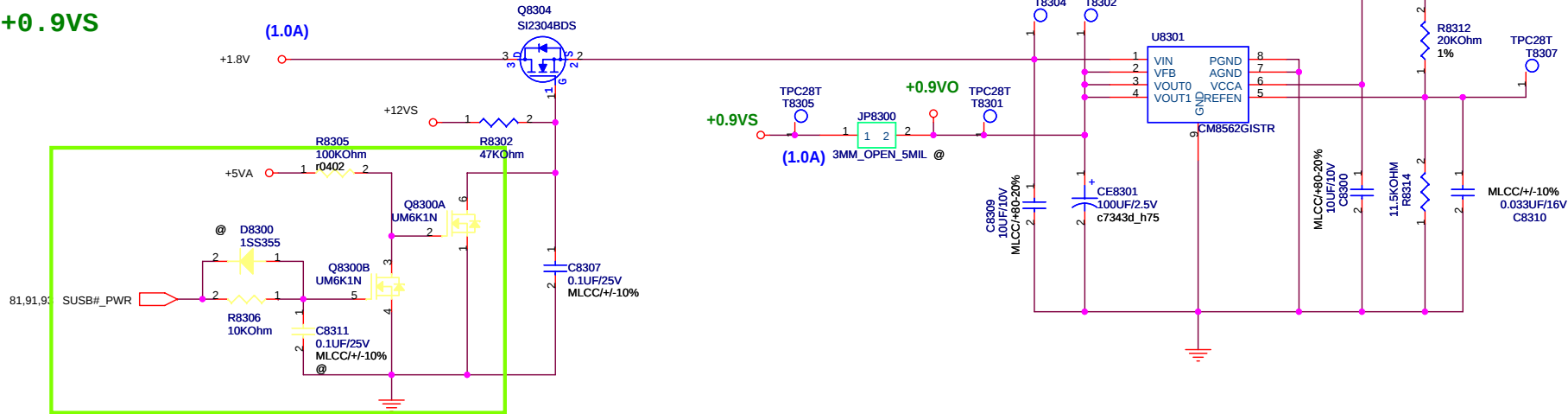
Rev

Sheet 80 of 94



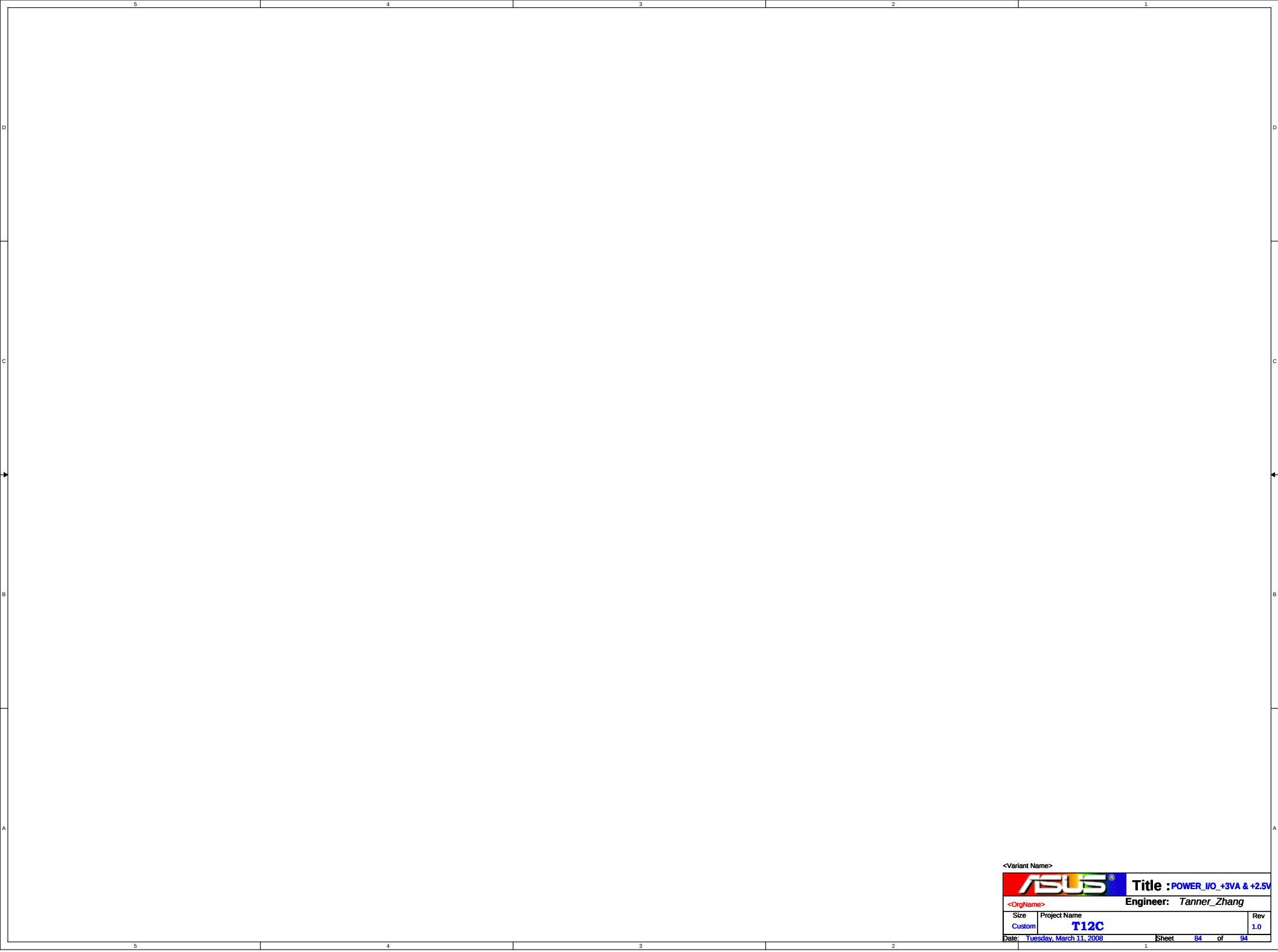


+0.9VS



05/30

ASUS		Title : 1.05V & +0.9VS	
<OrgName>		Engineer: Tanner_zhang	
Size B	Project Name T12C	Rev 1.1	
Date: Tuesday, March 11, 2008		Sheet	83 of 94



<Variant Name>

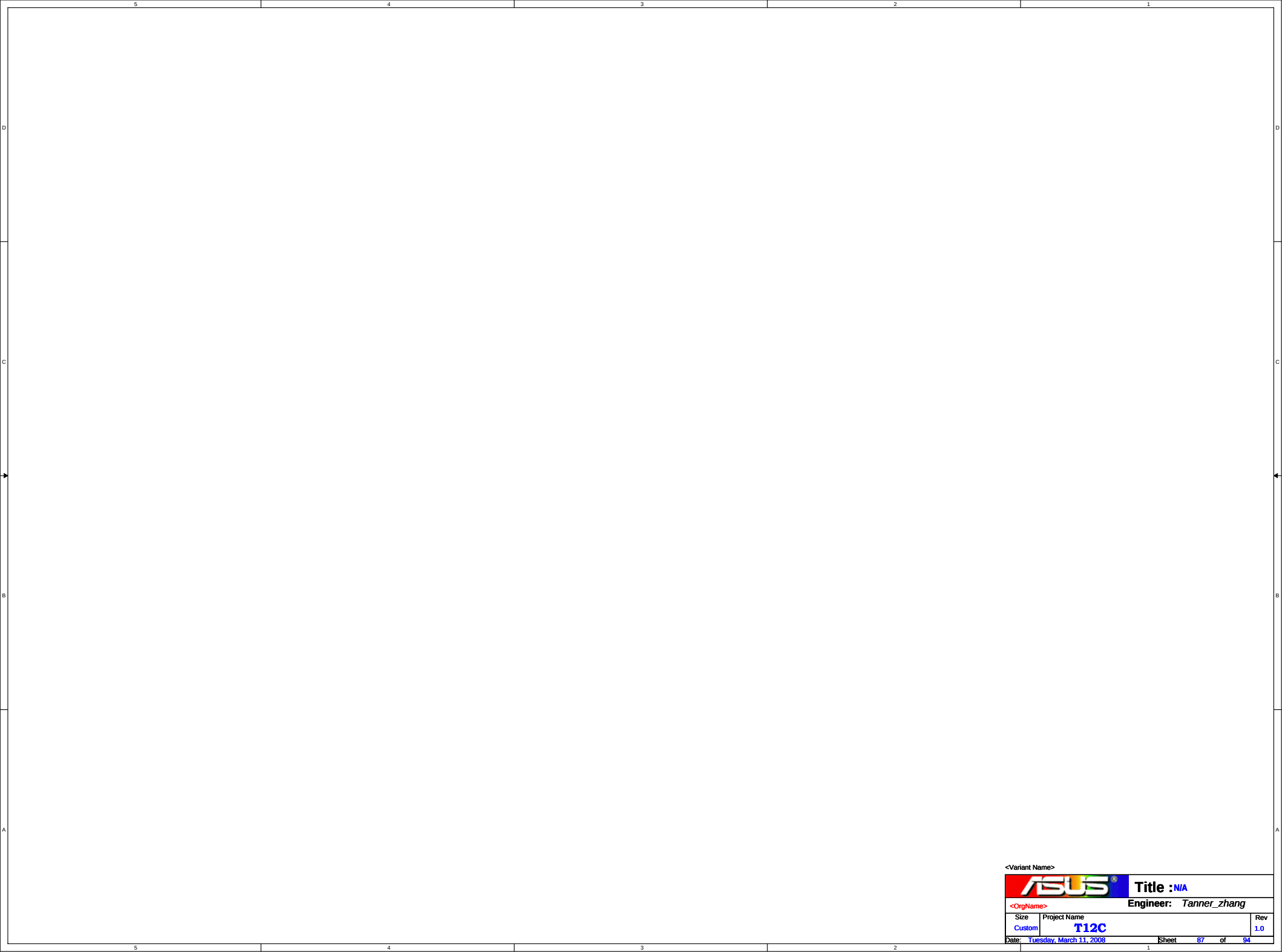


Title :POWER_I/O_+3VA & +2.5V

<OrgName>Engineer: Tanner_Zhang

Size	Project Name	Rev
Custom	T12C	1.0

Date: Tuesday, March 11, 2008Sheet 84 of 94



<Variant Name>



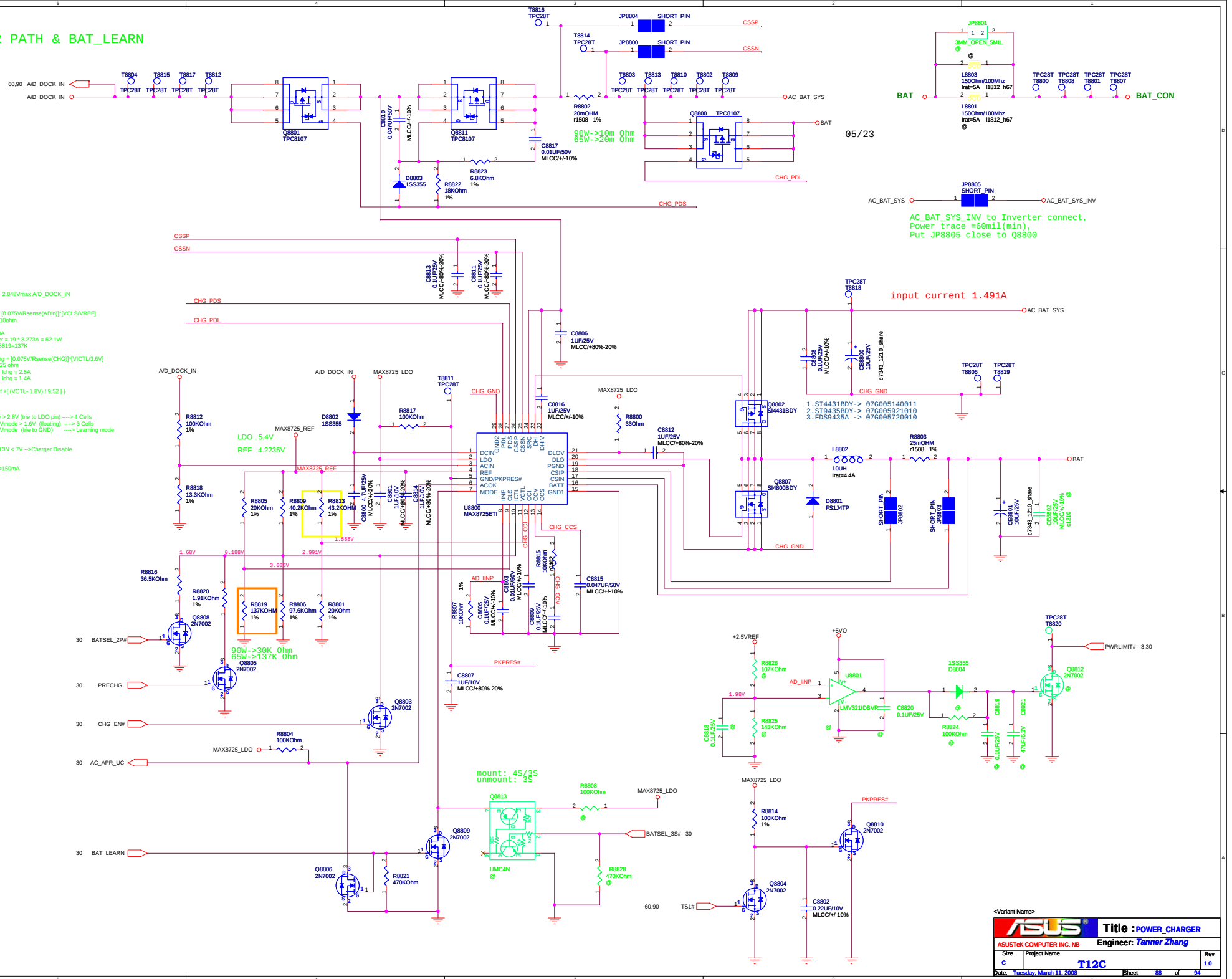
Title :*NIA*

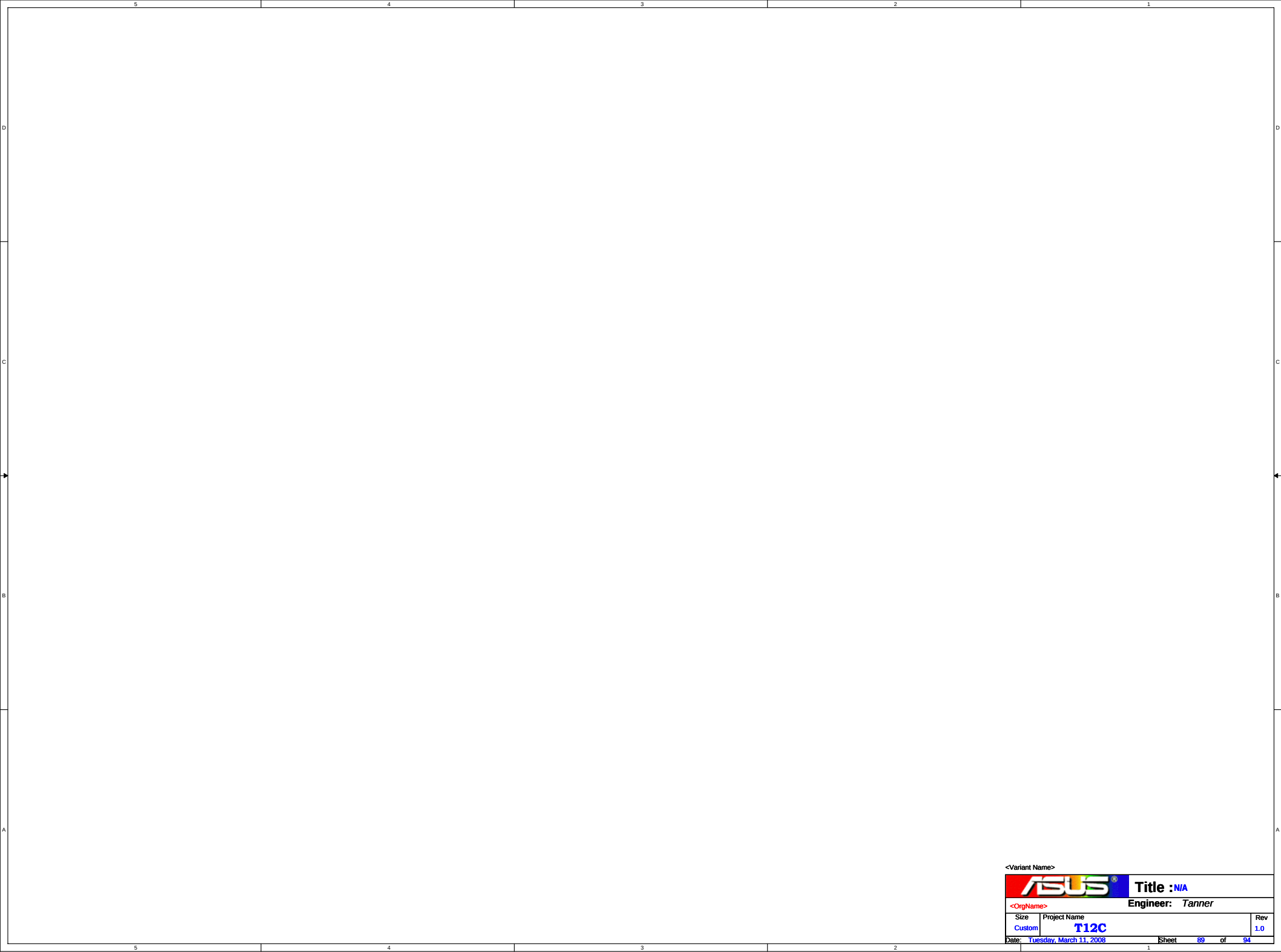
<OrgName>Engineer: *Tanner_zhang*

Size	Project Name	Rev
Custom	T12C	1.0

Date: *Tuesday, March 11, 2008*Sheet *87* of *94*

POWER PATH & BAT_LEARN





<Variant Name>



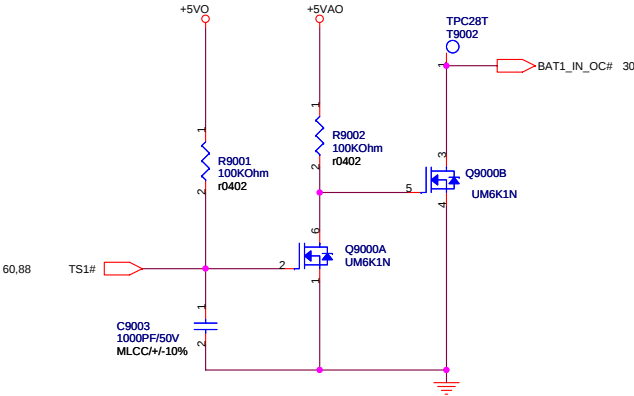
Title :*NIA*

<OrgName>Engineer: *Tanner*

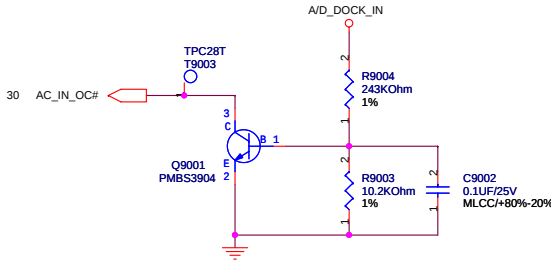
Size	Project Name	Rev
Custom	T12C	1.0

Date: *Tuesday, March 11, 2008*Sheet *89* of *94*

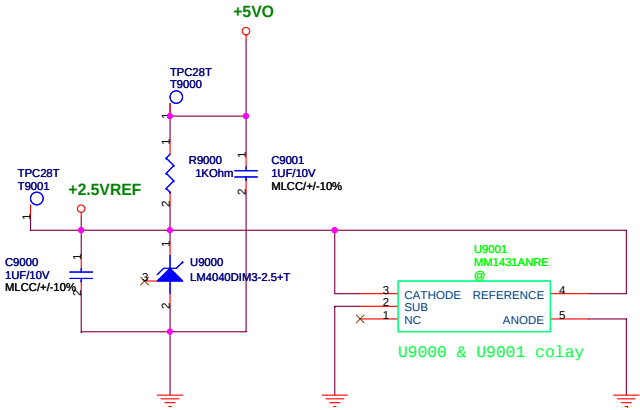
BATTERY IN DETECT



ADAPTER IN DETECT



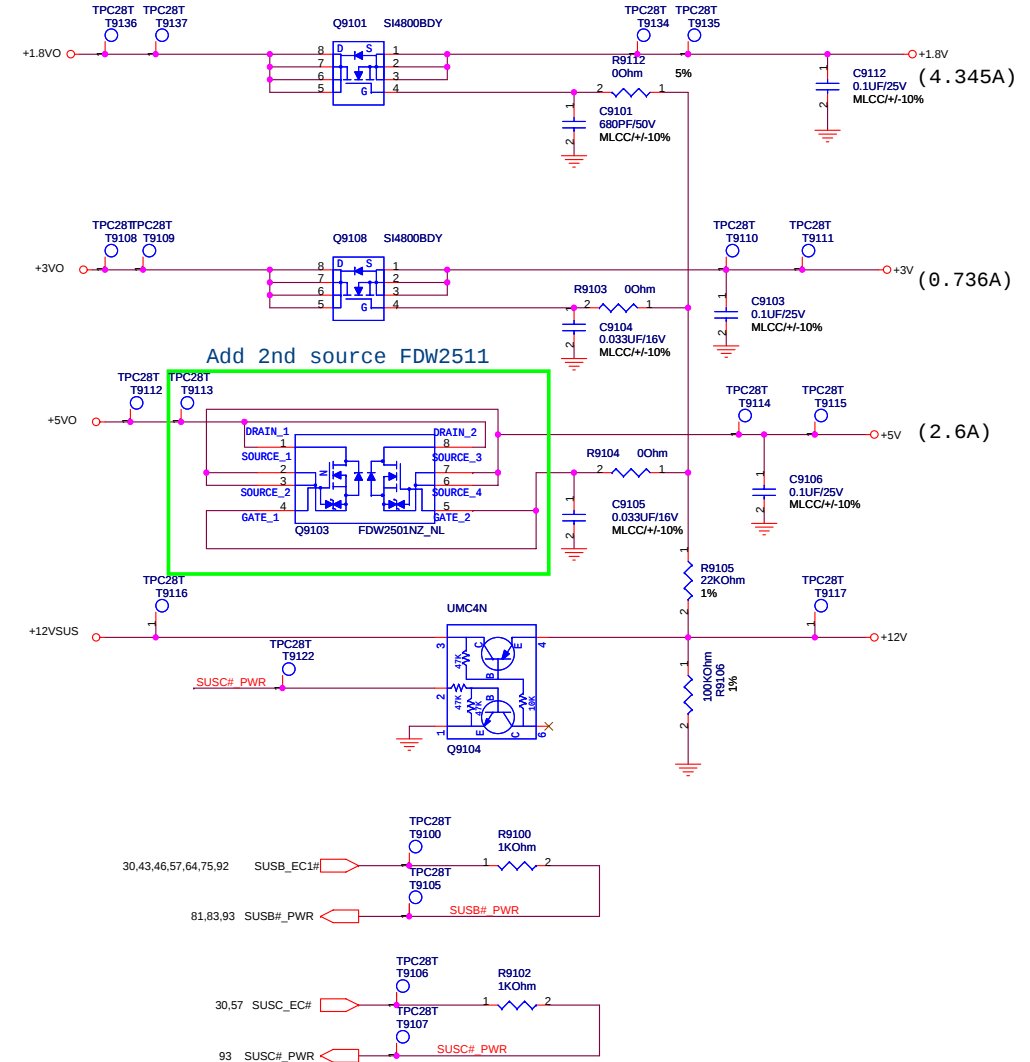
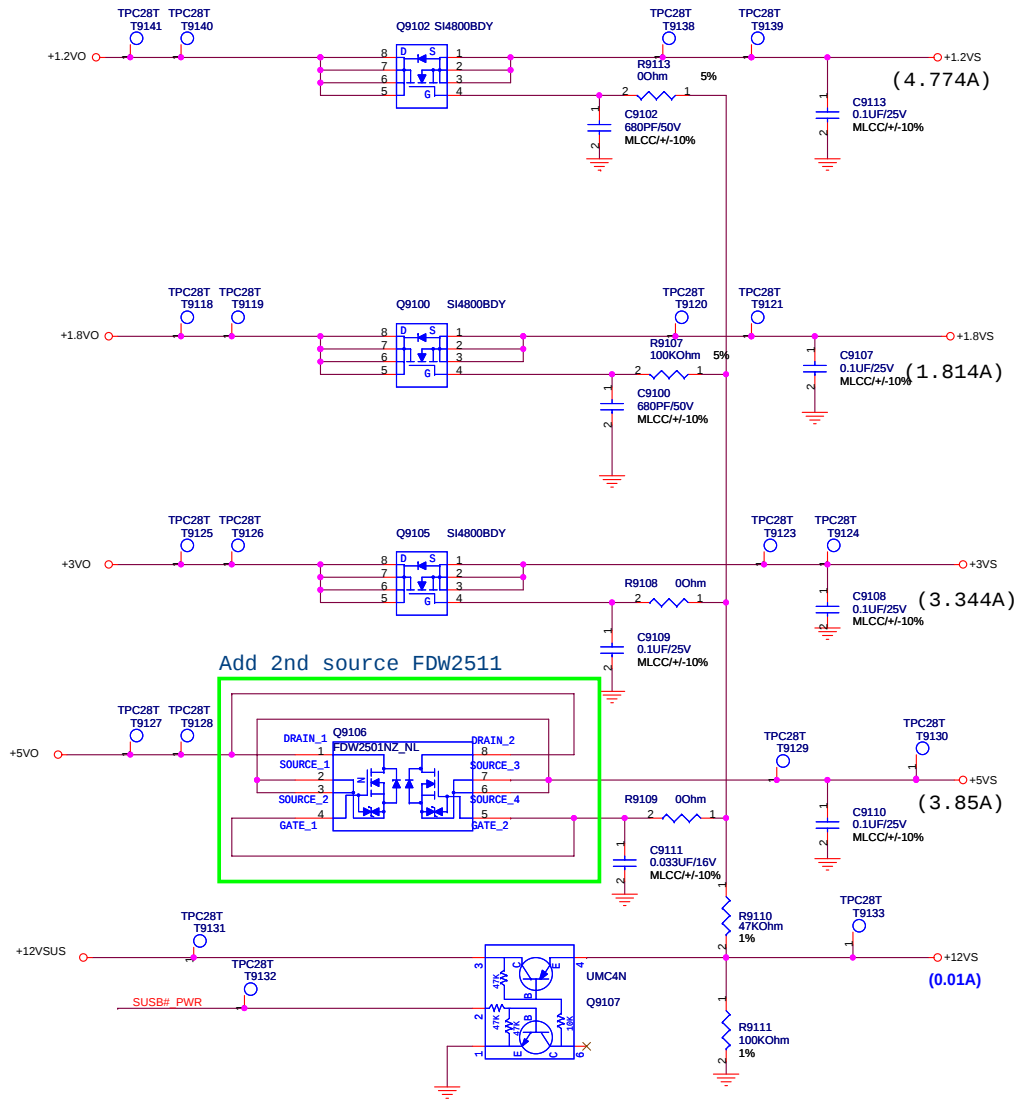
+2.5VREF



U9000 Main source change to 06G006002414(tolerance:1%).
Add second source 06G006002610 (tolerance:1%),
06G006002412 (tolerance:0.2%) and
06G006002020(tolerance:0.2%)

SUSC#_STAGE POWER

SUSB#_STAGE POWER



<Variant Name>

ASUS Title :POWER_LOAD SWITCH

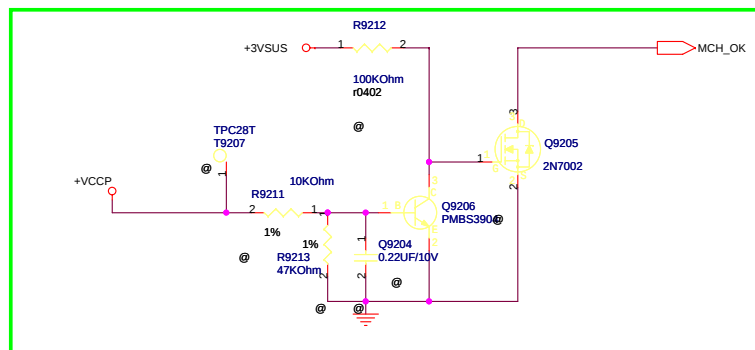
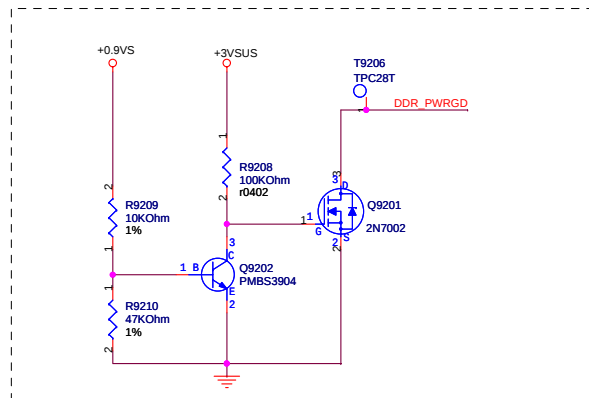
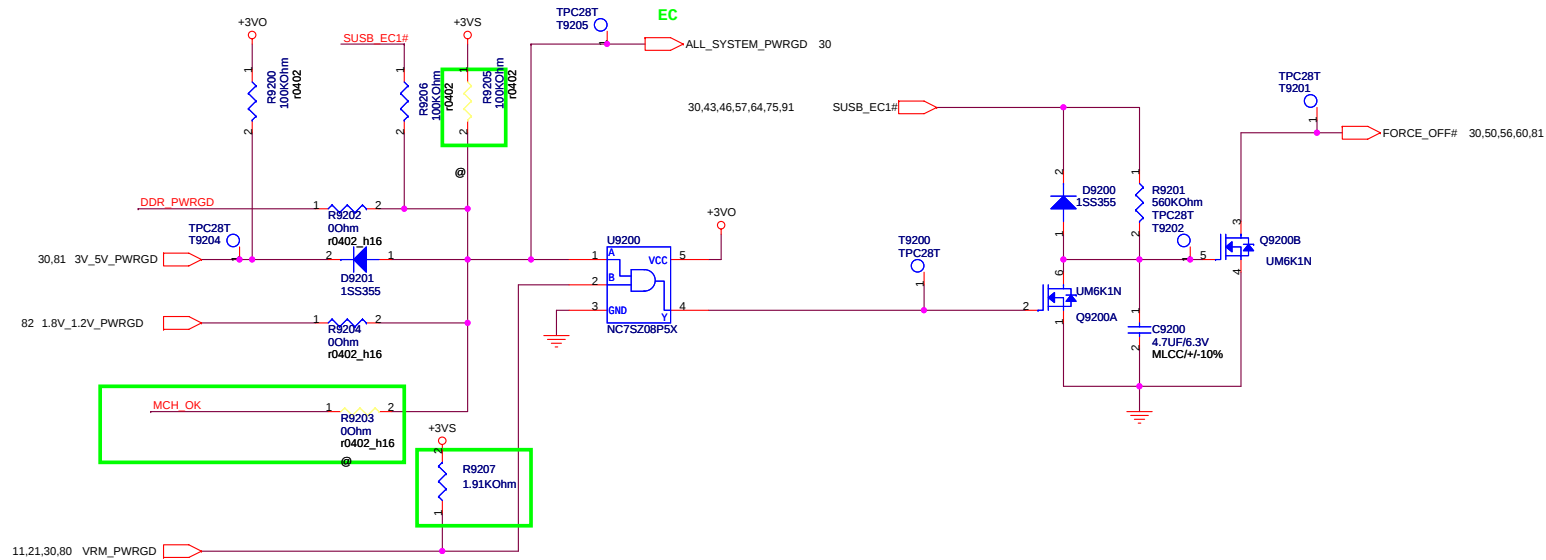
<OrgName> Engineer: Tanner

Size Project Name

Custom T12C Rev 1.0

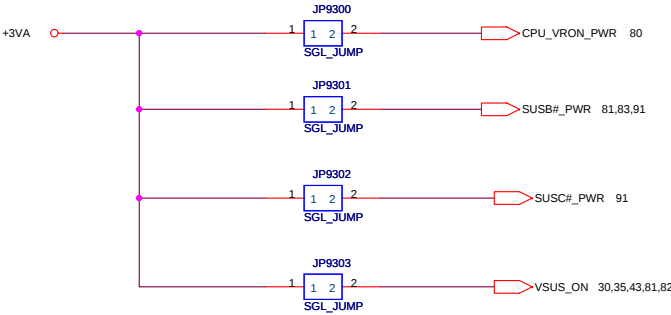
Date: Tuesday, March 11, 2008 Sheet 91 of 94

POWER GOOD DETECTOR





FOR POWER TEST



CHANGE LIST

06/28	SR	change R8133 to 21Kohm, set +5V0 ocp at 8.5A
		Change R8216, R8217 to 10Kohm. VSUS_ON soft start.
		change R8213 to 63.4K. set 1.2V0 OCP.
		delete R8306,Q8300,R8305.
		Add 2P/1P select circuit in charger
		for power squence, change R9207 to 1.91K
		for BOM cost, change the VCore output capcitor
07/13	SR	change R8207 to 10.5K, set 1.8vo up tp 1.845V
		change CE8202 to 100uf/2.5v for layout

