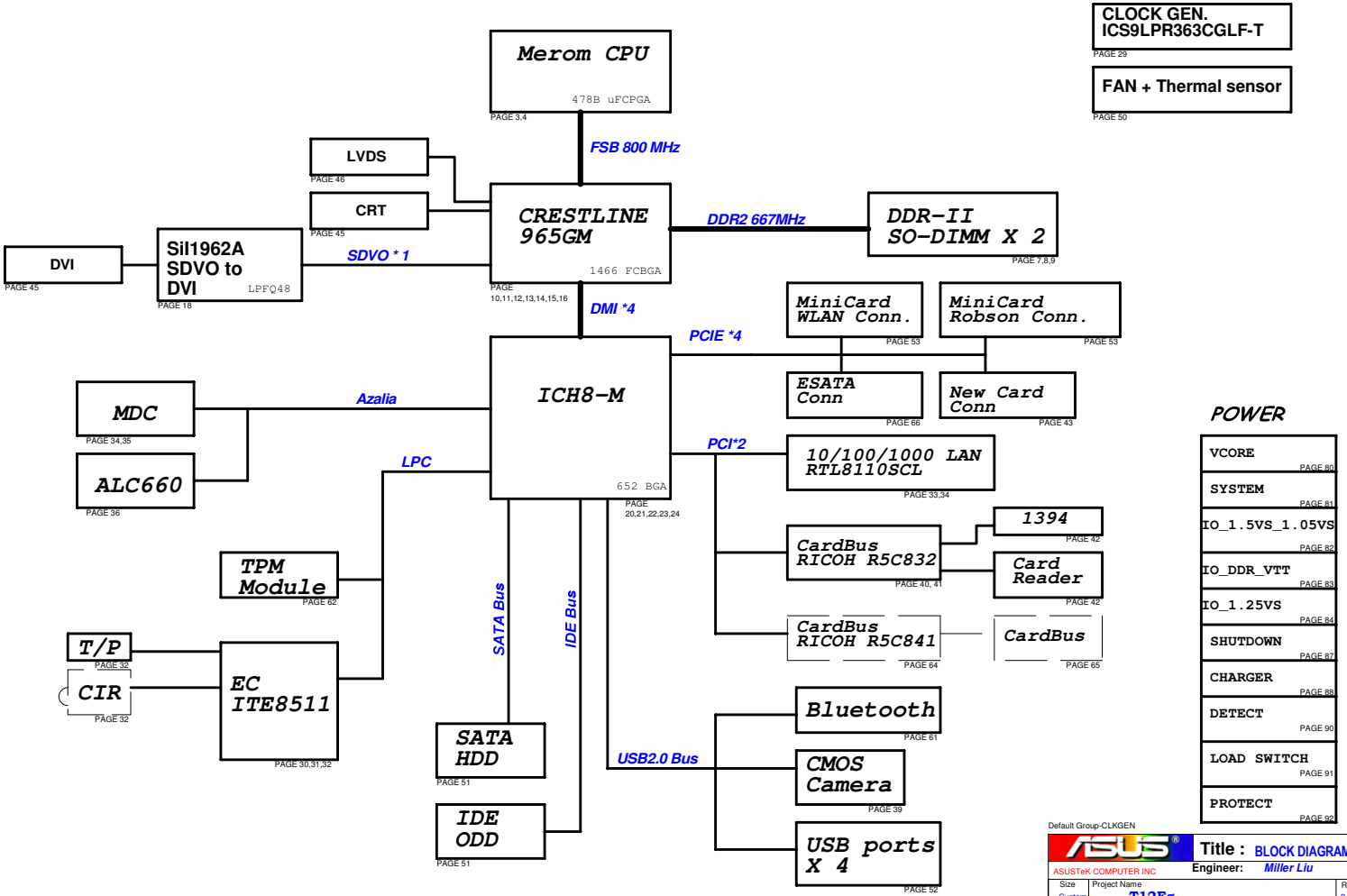
T12Eg Main BD. R2.0 BLOCK DIAGRAM



Default Group-CLKGEN

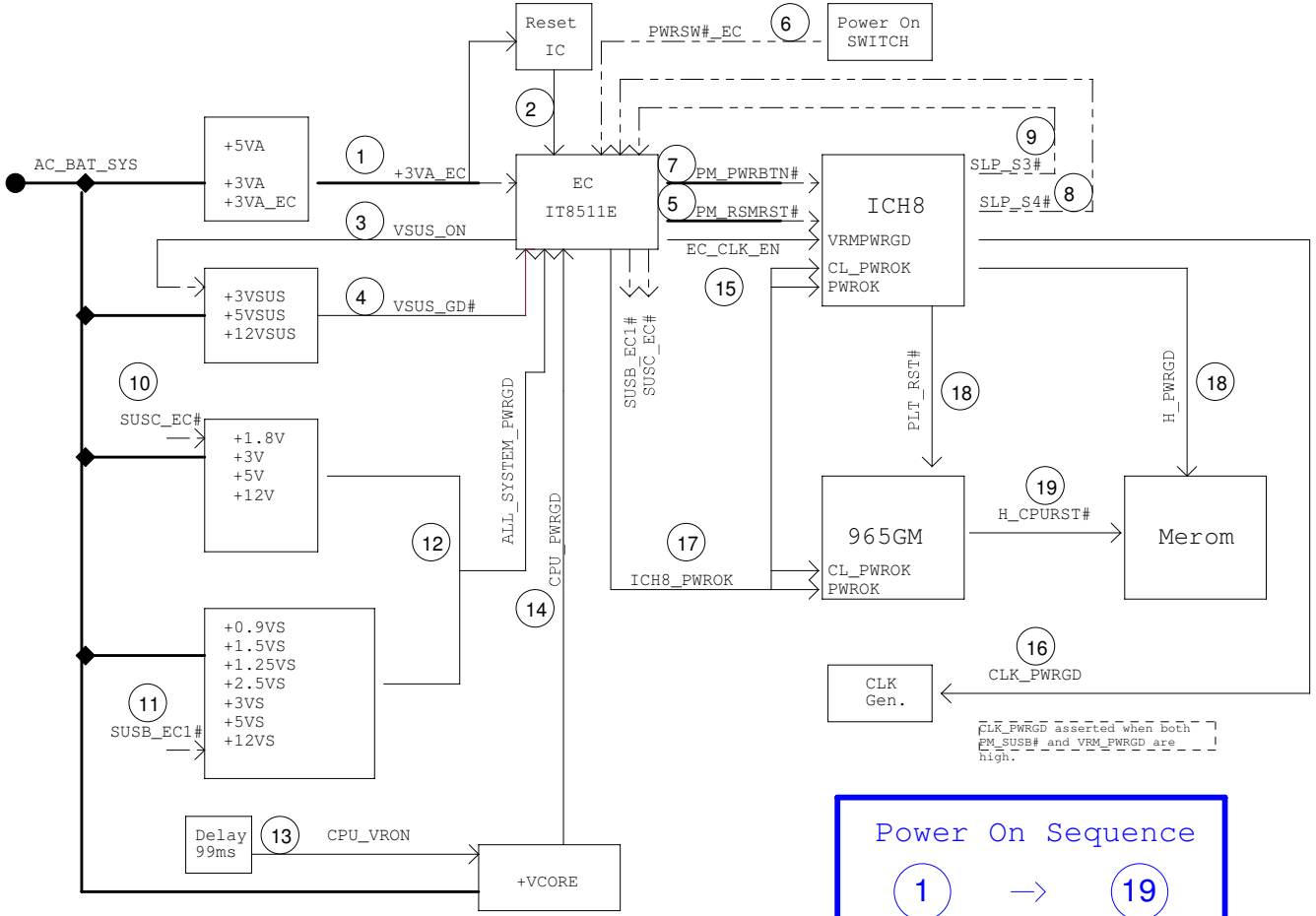
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 1 of 94



Default Group-CLKGEN

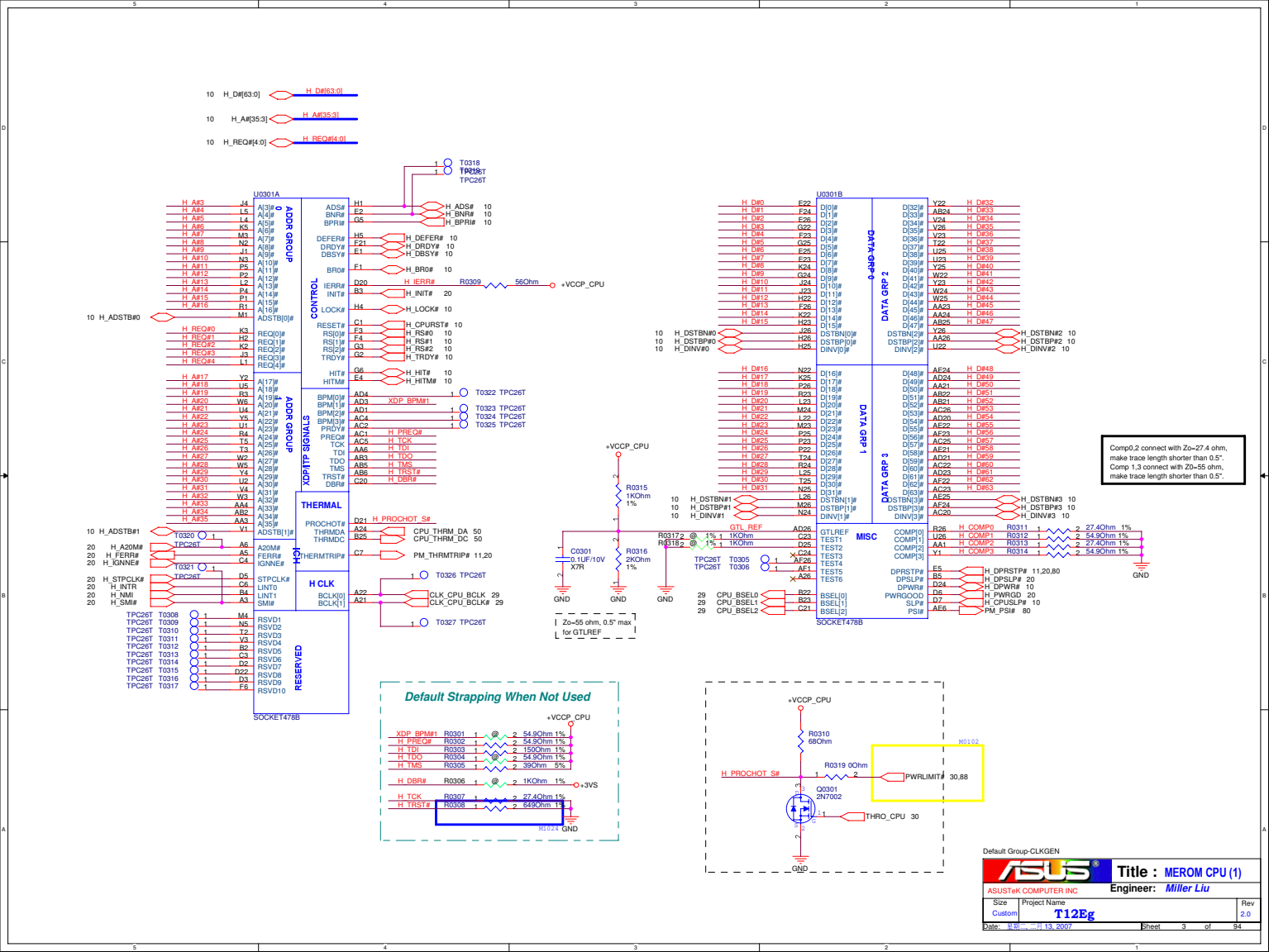
ASUSTeK COMPUTER INC

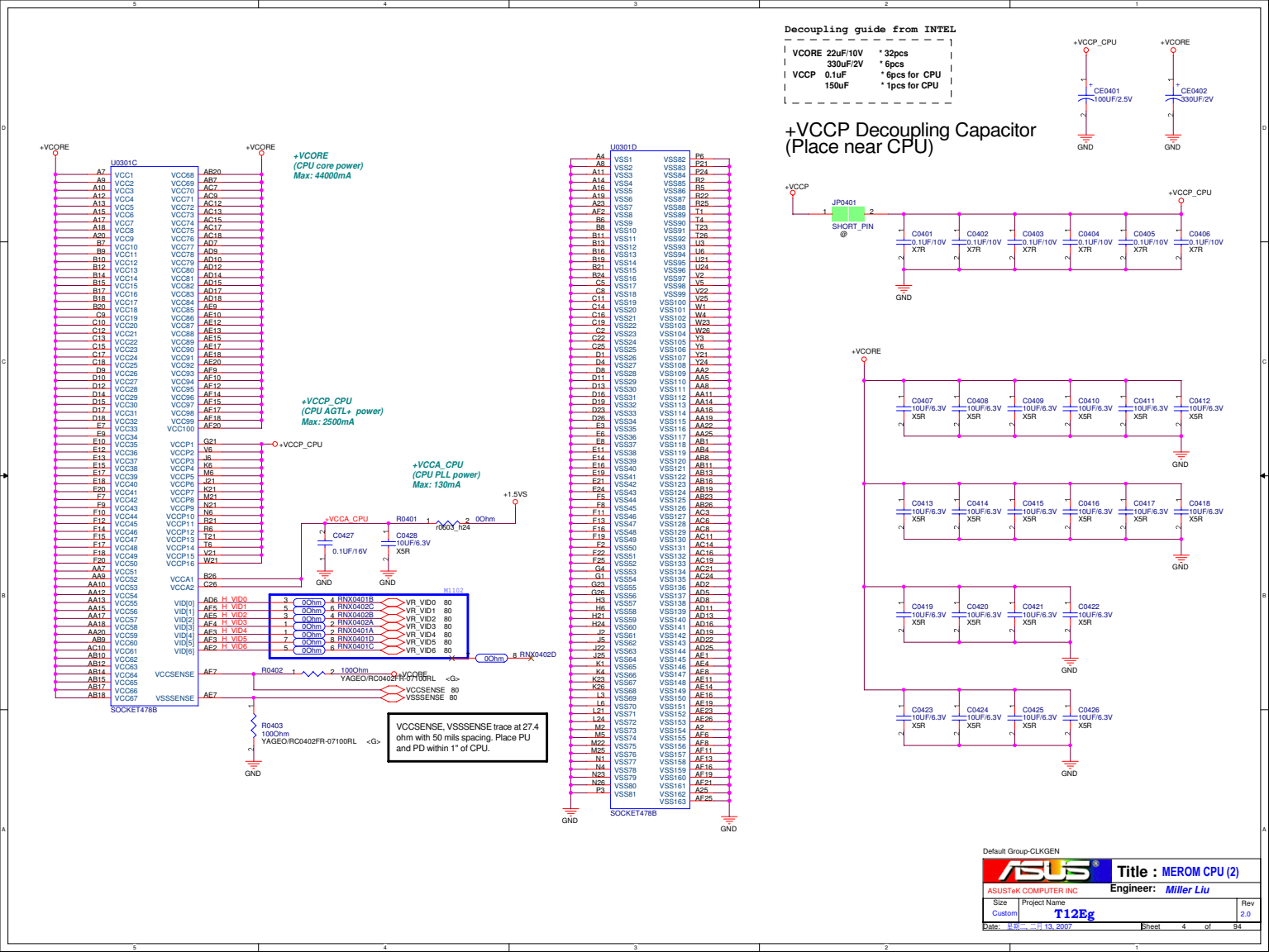
Title : PowerOn sequence

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 2 of 94


U0301A
U0301B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478B
H_D#[63:0]
H_A#[35:3]
H_REQ#[4:0]
H_ADSTB#0
H_ADSTB#1
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
H_PROCHOT_S#
H_IERR#
H_INIT#
H_LOCK#
H_BR0#
H_DEFER#
H_DRDY#
H_DBSY#
H_RS#0
H_RS#1
H_RS#2
H_TRDY#
H_HIT#
H_HITM#
H_BPRI#
H_ADS#
H_BNR#
H_CPURST#
H_PREQ#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
H_DBR#
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
R0309 56Ohm
+VCCP_CPU
R0315 1KOhm 1%
R0316 2KOhm 1%
C0301 0.1UF/10V X7R
GTL_REF
R0317 1KOhm 1%
R0318 1KOhm 1%
Zo=55 ohm, 0.5" max for GTLREF
CPU_THRM_DA 50
CPU_THRM_DC 50
PM_THRMTRIP# 11,20
CLK_CPU_BCLK 29
CLK_CPU_BCLK# 29
CPU_BSEL0 29
CPU_BSEL1 29
CPU_BSEL2 29
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".
Default Strapping When Not Used
XDP_BPM#1 R0301 54.9Ohm 1%
H_PREQ# R0302 54.9Ohm 1%
H_TDI R0303 150Ohm 1%
H_TDO R0304 54.9Ohm 1%
H_TMS R0305 39Ohm 5%
H_DBR# R0306 1KOhm 1%
H_TCK R0307 27.4Ohm 1%
H_TRST# R0308 649Ohm 1%
+3VS
R0310 68Ohm
R0319 0Ohm
PWRLIMIT# 30,88
Q0301 2N7002
THRO_CPU 30
Default Group-CLKGEN
Title : MEROM CPU (1)
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Size: Custom
Project Name: T12Eg
Rev: 2.0
Date: 星期二, 二月 13, 2007
Sheet 3 of 94


Decoupling guide from INTEL
VCORE 22uF/10V * 32pcs
330uF/2V * 6pcs
VCCP 0.1uF * 6pcs for CPU
150uF * 1pcs for CPU
+VCCP Decoupling Capacitor (Place near CPU)
+VCORE
+VCCP_CPU
CE0401 100UF/2.5V
CE0402 330UF/2V
GND
+VCORE
(CPU core power)
Max: 44000mA
+VCCP_CPU
(CPU AGTL+ power)
Max: 2500mA
+VCCA_CPU
(CPU PLL power)
Max: 130mA
+1.5VS
U0301C
SOCKET478B
U0301D
SOCKET478B
JP0401
SHORT_PIN
C0401 0.1UF/10V X7R
C0402 1UF/10V X7R
C0403 0.1UF/10V X7R
C0404 0.1UF/10V X7R
C0405 0.1UF/10V X7R
C0406 0.1UF/10V X7R
C0407 10UF/6.3V X5R
C0408 10UF/6.3V X5R
C0409 10UF/6.3V X5R
C0410 10UF/6.3V X5R
C0411 10UF/6.3V X5R
C0412 10UF/6.3V X5R
C0413 10UF/6.3V X5R
C0414 10UF/6.3V X5R
C0415 10UF/6.3V X5R
C0416 10UF/6.3V X5R
C0417 10UF/6.3V X5R
C0418 10UF/6.3V X5R
C0419 10UF/6.3V X5R
C0420 10UF/6.3V X5R
C0421 10UF/6.3V X5R
C0422 10UF/6.3V X5R
C0423 10UF/6.3V X5R
C0424 10UF/6.3V X5R
C0425 10UF/6.3V X5R
C0426 10UF/6.3V X5R
C0427 0.1UF/16V
C0428 10UF/6.3V X5R
R0401 0Ohm r0603_h24
R0402 100Ohm YAGEO/RC0402FR-07100RL
R0403 100Ohm YAGEO/RC0402FR-07100RL
M1102
RNX0401A
RNX0401B
RNX0401C
RNX0401D
RNX0402A
RNX0402B
RNX0402C
RNX0402D
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
VCCSENSE
VSSSENSE
VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.
Default Group-CLKGEN
ASUSTeK COMPUTER INC
Title : MEROM CPU (2)
Engineer: Miller Liu
Size Custom
Project Name T12Eg
Rev 2.0
Date: 星期二, 二月 13, 2007
Sheet 4 of 94

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: T12Eg	Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 5 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: T12Eg	Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 6 of 94	

P/N: 12G025022004
(T12F) 4.0mm, STD

M122.7

M_CLK_DDR0
R0701 69.8Ohm PLACE NEAR SO-DIMM_1
M_CLK_DDR#0
@
M_CLK_DDR1
R0702 69.8Ohm PLACE NEAR SO-DIMM_1
M_CLK_DDR#1
@

SMBus Slave Address:A0H

9,13 M_A_A[0..13]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13

9,11 M_A_A14
9,13 M_A_BS2
9,13 M_A_BS0
9,13 M_A_BS1
9,11 M_CS#0
9,11 M_CS#1
11 M_CLK_DDR0
11 M_CLK_DDR#0
11 M_CLK_DDR1
11 M_CLK_DDR#1
9,11 M_CKE0
9,11 M_CKE1
9,13 M_A_CAS#
9,13 M_A_RAS#
9,13 M_A_WE#

8,24,29,43,53 SMB_CLK_S
8,24,29,43,53 SMB_DAT_S

9,11 M_ODT0
9,11 M_ODT1

13 M_A_DM[0..7]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7

13 M_A_DQS[0..7]
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

13 M_A_DQS#[0..7]
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7

J0701A

M_A_A0	102	A0	DQ0	5	M_A_DQ4
M_A_A1	101	A1	DQ1	7	M_A_DQ5
M_A_A2	100	A2	DQ2	17	M_A_DQ6
M_A_A3	99	A3	DQ3	19	M_A_DQ7
M_A_A4	98	A4	DQ4	4	M_A_DQ0
M_A_A5	97	A5	DQ5	6	M_A_DQ1
M_A_A6	94	A6	DQ6	14	M_A_DQ2
M_A_A7	92	A7	DQ7	16	M_A_DQ3
M_A_A8	93	A8	DQ8	23	M_A_DQ14
M_A_A9	91	A9	DQ9	25	M_A_DQ9
M_A_A10	105	A10/AP	DQ10	35	M_A_DQ15
M_A_A11	90	A11	DQ11	37	M_A_DQ10
M_A_A12	89	A12	DQ12	20	M_A_DQ13
M_A_A13	116	A13	DQ13	22	M_A_DQ12
	86	A14	DQ14	36	M_A_DQ8
	84	A15	DQ15	38	M_A_DQ11
	85	A16_BA2	DQ16	43	M_A_DQ20
			DQ17	45	M_A_DQ21
	107	BA0	DQ18	55	M_A_DQ23
	106	BA1	DQ19	57	M_A_DQ22
	110	S0#	DQ20	44	M_A_DQ17
	115	S1#	DQ21	46	M_A_DQ16
	30	CK0	DQ22	56	M_A_DQ18
	32	CK0#	DQ23	58	M_A_DQ19
	164	CK1	DQ24	61	M_A_DQ28
	166	CK1#	DQ25	63	M_A_DQ29
	79	CKE0	DQ26	73	M_A_DQ30
	80	CKE1	DQ27	75	M_A_DQ27
	113	CAS#	DQ28	62	M_A_DQ26
	108	RAS#	DQ29	64	M_A_DQ24
	109	WE#	DQ30	74	M_A_DQ25
	198	SA0	DQ31	76	M_A_DQ31
	200	SA1	DQ32	123	M_A_DQ33
	197	SCL	DQ33	125	M_A_DQ36
	195	SDA	DQ34	135	M_A_DQ37
			DQ35	137	M_A_DQ35
	114	ODT0	DQ36	124	M_A_DQ32
	119	ODT1	DQ37	126	M_A_DQ38
			DQ38	134	M_A_DQ34
M_A_DM0	10	DM0	DQ39	136	M_A_DQ39
M_A_DM1	26	DM1	DQ40	141	M_A_DQ44
M_A_DM2	52	DM2	DQ41	143	M_A_DQ42
M_A_DM3	67	DM3	DQ42	141	M_A_DQ41
M_A_DM4	130	DM4	DQ43	153	M_A_DQ43
M_A_DM5	147	DM5	DQ44	140	M_A_DQ40
M_A_DM6	170	DM6	DQ45	142	M_A_DQ45
M_A_DM7	185	DM7	DQ46	152	M_A_DQ46
			DQ47	154	M_A_DQ47
M_A_DQS0	13	DQS0	DQ48	157	M_A_DQS5
M_A_DQS1	31	DQS1	DQ49	159	M_A_DQ49
M_A_DQS2	51	DQS2	DQ50	173	M_A_DQS5
M_A_DQS3	70	DQS3	DQ51	175	M_A_DQ54
M_A_DQS4	131	DQS4	DQ52	158	M_A_DQ48
M_A_DQS5	148	DQS5	DQ53	160	M_A_DQ53
M_A_DQS6	169	DQS6	DQ54	174	M_A_DQ50
M_A_DQS7	188	DQS7	DQ55	176	M_A_DQ51
M_A_DQS#0	11	DQS#0	DQ56	179	M_A_DQ60
M_A_DQS#1	29	DQS#1	DQ57	181	M_A_DQ57
M_A_DQS#2	49	DQS#2	DQ58	189	M_A_DQ58
M_A_DQS#3	68	DQS#3	DQ59	191	M_A_DQ61
M_A_DQS#4	129	DQS#4	DQ60	180	M_A_DQ56
M_A_DQS#5	146	DQS#5	DQ61	182	M_A_DQ59
M_A_DQS#6	167	DQS#6	DQ62	192	M_A_DQ62
M_A_DQS#7	186	DQS#7	DQ63	194	M_A_DQ63

DDR2_DIMM_200P

M_A_DQ[0..63] 13

SWAP SWAP SWAP SWAP SWAP

GND

SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C0702 C0703 C0704 C0705 0.1UF/16V

GND

+3VS

C0707 0.1UF/16V

PM_EXTTS#0

RX0701 0Ohm @

M_VREF_MCH

VREF->.10/10 mils

C0708 2.2UF/6.3V C0709 0.1UF/16V

GND

J0701B

	112	VDD1	VSS16	18	
	111	VDD2	VSS17	24	
	117	VDD3	VSS18	41	
	96	VDD4	VSS19	53	
	95	VDD5	VSS20	42	
	118	VDD6	VSS21	54	
	81	VDD7	VSS22	59	
	82	VDD8	VSS23	65	
	87	VDD9	VSS24	60	
	103	VDD10	VSS25	66	
	88	VDD11	VSS26	127	
	104	VDD12	VSS27	139	
			VSS28	128	
	199	VDDSPD	VSS29	145	
			VSS30	165	
	83	NC1	VSS31	171	
	120	NC2	VSS32	172	
	50	NC3	VSS33	177	
	69	NC4	VSS34	187	
	163	NCTEST	VSS35	178	
			VSS36	190	
	1	VREF	VSS37	9	
			VSS38	21	
	201	GND0	VSS39	33	
	202	GND1	VSS40	155	
			VSS41	34	
	203	NP_NC1	VSS42	132	
	204	NP_NC2	VSS43	144	
			VSS44	156	
	47	VSS1	VSS45	168	
	133	VSS2	VSS46	2	
	183	VSS3	VSS47	3	
	77	VSS4	VSS48	15	
	12	VSS5	VSS49	27	
	48	VSS6	VSS50	39	
	184	VSS7	VSS51	149	
	78	VSS8	VSS52	161	
	71	VSS9	VSS53	28	
	72	VSS10	VSS54	40	
	121	VSS11	VSS55	138	
	122	VSS12	VSS56	150	
	196	VSS13	VSS57	162	
	193	VSS14			
	8	VSS15			

DDR2_DIMM_200P

GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C0710 C0711 C0712 C0713 C0714 1UF/6.3V

GND

+1.8V

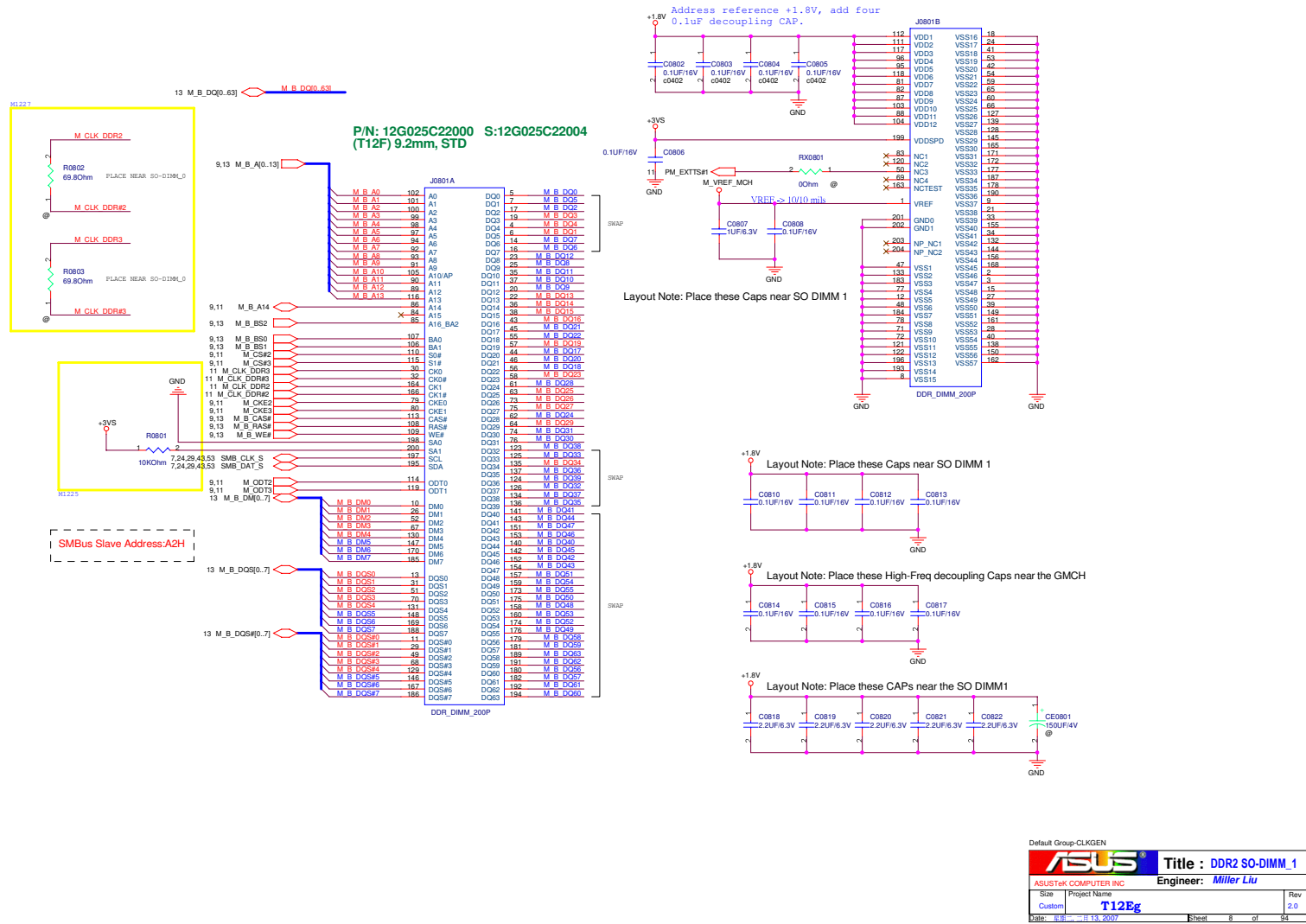
C0715 C0716 C0717 C0718 C0719 2.2UF/6.3V

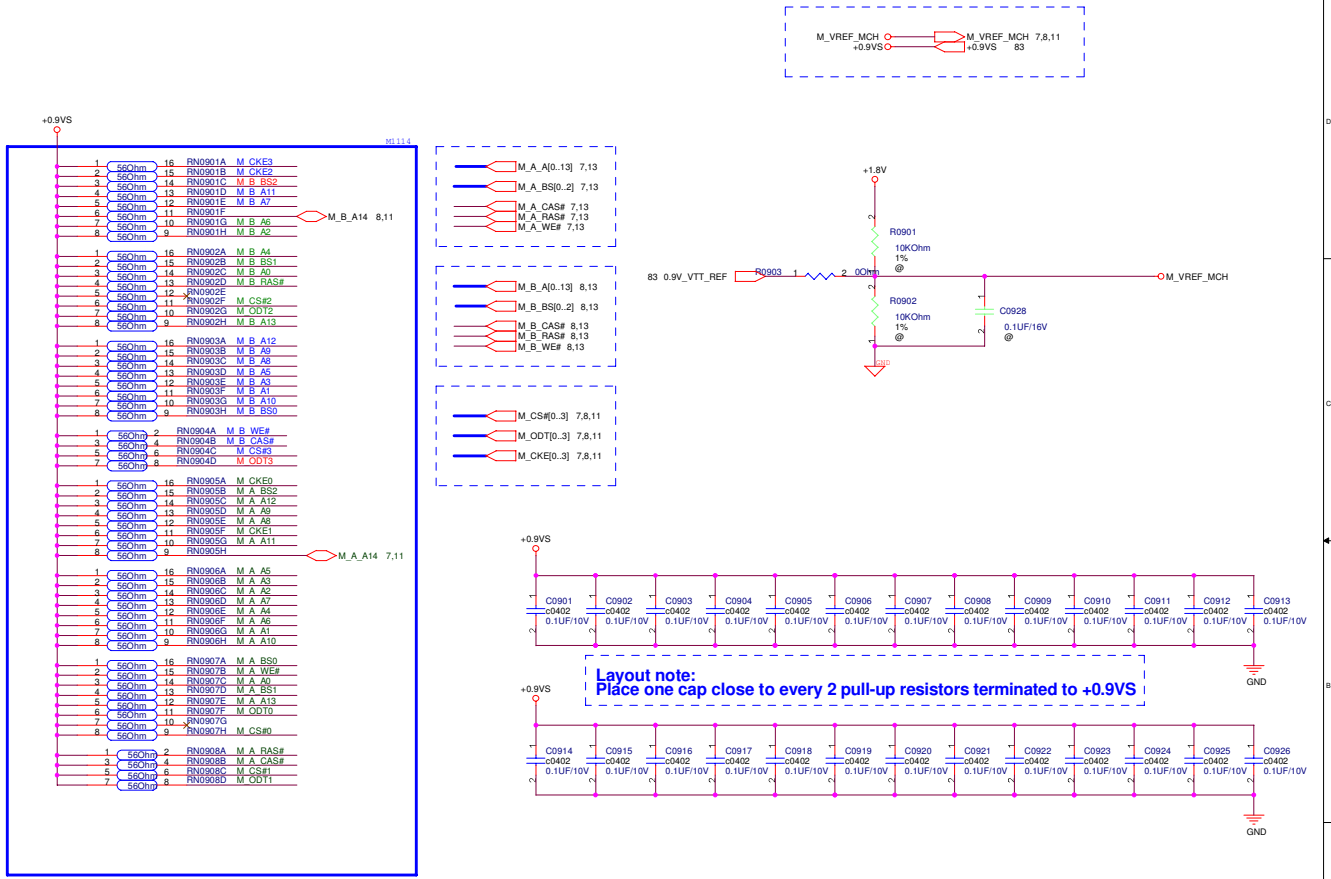
CE0701 150UF/4V @

GND

Default Group-CLKGEN

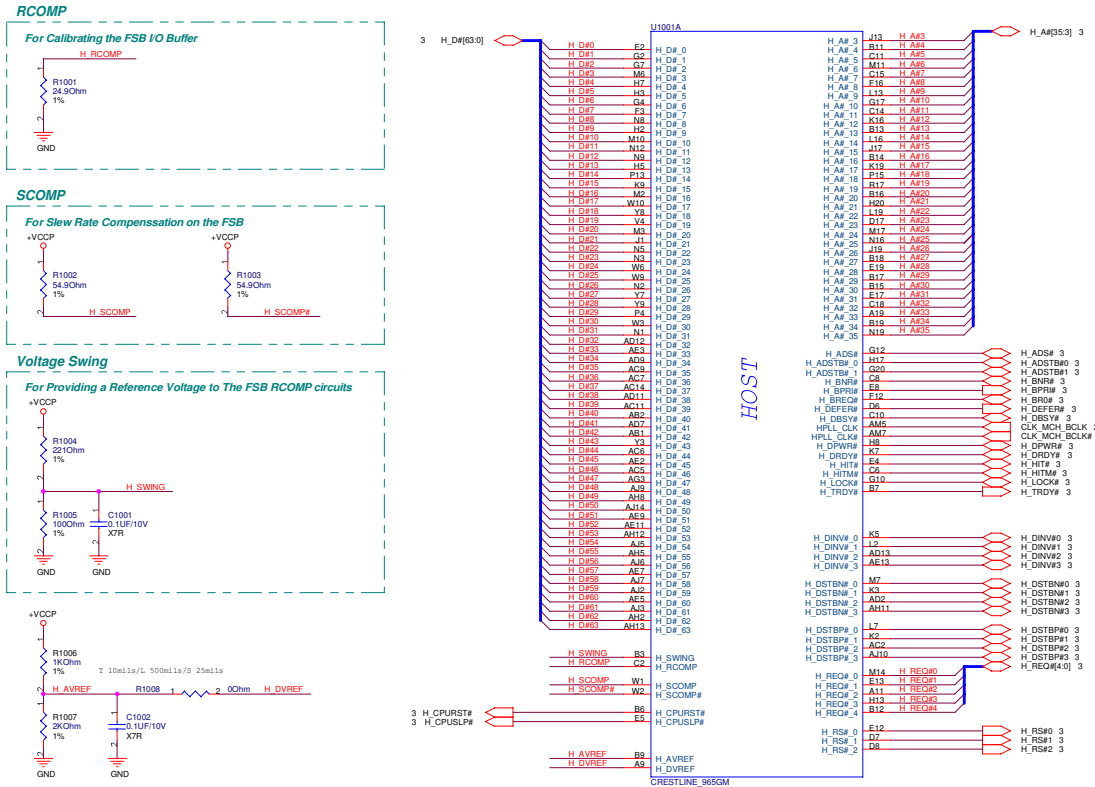
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0		
	Engineer: Miller Liu		
Size: Custom	Project Name: T12Eg		Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 7 of 94		


Address reference +1.8V, add four 0.1uF decoupling CAP.
P/N: 12G025C22000 S:12G025C22004
(T12F) 9.2mm, STD
J0801A
J0801B
DDR_DIMM_200P
Layout Note: Place these Caps near SO DIMM 1
Layout Note: Place these High-Freq decoupling Caps near the GMCH
Layout Note: Place these CAPs near the SO DIMM1
SMBus Slave Address:A2H
VREF -> 10/10 mils
SWAP
Default Group-CLKGEN
Title : DDR2 SO-DIMM_1
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Project Name T12Eg
Rev 2.0
Sheet 8 of 94



Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : DDR2 TERM		
	Engineer: Miller Liu		
Size: Custom	Project Name: T12Eg		Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 9 of 94		



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

Title : NB-965GM (HOST)

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Fg	2.0

Date: 星期一, 二月 13, 2007 Sheet 10 of 94

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — R1101 4.02KOHM @ — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

MCH_CFG_19 — R1102 4.02KOHM @ — +3VS

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

MCH_CFG_12 — R1105 4.02KOHM @ — GND
MCH_CFG_13 — R1106 4.02KOHM @ — GND

CFG8 : Low Power PCI-E

0 = Normal mode
1 = Low Power Mode (D)

MCH_CFG_8 — R1107 4.02KOHM @ — GND

CFG20 : Concurrent SDVO / PCIe

0 = Only one is operational (D)
1 = operate simultaneous

MCH_CFG_20 — R1108 4.02KOHM @ — +3VS

CFG9 : PCIE Graphic Lane

0 = Reverse Lane PCI-E (SDVO)
1 = Normal Operation (D)

MCH_CFG_9 — R1109 4.02KOHM @ — GND

SDVO_CTRL_DATA : SDVO Present

0 = No SDVO (D)
1 = SDVO Present

SDVO_CTRL_DATA — R1110 0Ohm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R1111 4.02KOHM @ — GND

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L

Matanzas 1.301

U1001B

RSVD1 P36
RSVD2 P37
RSVD3 R35
RSVD4 N35
RSVD5 AR12
RSVD6 AR13
RSVD7 AM12
RSVD8 AN13
RSVD9 J12
RSVD10 AR37
RSVD11 AM36
RSVD12 AL36
RSVD13 AM37
RSVD14 D20

C1102 0.1UF/10V X7R — GND

RSVD20 H10
RSVD21 B51
RSVD22 BJ20
RSVD23 BK22
RSVD24 BF19
RSVD25 BH20
RSVD26 BK18
RSVD27 BJ18
RSVD28 BF23
RSVD29 BG23
RSVD30 BC23
RSVD31 BD24
RSVD32 BJ29
RSVD33 BE24
RSVD34 BH34
RSVD35 AW20
RSVD36 BK20
RSVD37 C48
RSVD38 D47
RSVD39 B44
RSVD40 C44
RSVD41 A35
RSVD42 B37
RSVD43 B36
RSVD44 B34
RSVD45 C34

7,9 M_A_A14
8,9 M_B_A14

GMCH DDR MUXING

SM_CK_0 AV29 — M_CLK_DDR0 7
SM_CK_1 BB23 — M_CLK_DDR1 7
SM_CK_3 BA25 — M_CLK_DDR2 8
SM_CK_4 AV23 — M_CLK_DDR3 8

SM_CK#_0 AW30 — M_CLK_DDR#0 7
SM_CK#_1 BA23 — M_CLK_DDR#1 7
SM_CK#_3 AW25 — M_CLK_DDR#2 8
SM_CK#_4 AW23 — M_CLK_DDR#3 8

SM_CKE_0 BE29 — M_CKE0 7,9
SM_CKE_1 AY32 — M_CKE1 7,9
SM_CKE_3 BD39 — M_CKE2 8,9
SM_CKE_4 BG37 — M_CKE3 8,9

SM_CS#_0 BG20 — M_CS#0 7,9
SM_CS#_1 BK16 — M_CS#1 7,9
SM_CS#_2 BG16 — M_CS#2 8,9
SM_CS#_3 BE13 — M_CS#3 8,9

SM_ODT_0 BH18 — M_ODT0 7,9
SM_ODT_1 BJ15 — M_ODT1 7,9
SM_ODT_2 BJ14 — M_ODT2 8,9
SM_ODT_3 BE16 — M_ODT3 8,9

For Calero 20 Ohm
For Crestline 80.6 Ohm

SM_RCOMP BK15 — SM_RCOMP — R1129 2 1% 200hm
SM_RCOMP# BK14 — SM_RCOMP# — R1130 2 1% 200hm — +1.8V

SM_RCOMP_VOH BK31 — SM_RCOMP_VOH
SM_RCOMP_VOL BL31 — SM_RCOMP_VOL

SM_VREF_0 AR49
SM_VREF_1 AW4

M_VREF_MCH — C1108 2.2UF/6.3V — C1109 0.01UF/16V — GND
M1024

GMCH CLK

DPLL_REF_CLK B42 — DPLL_REF_CLK 29
DPLL_REF_CLK# C42 — DPLL_REF_CLK# 29
DPLL_REF_SSCLK J48 — DPLL_REF_SSCLK 29
DPLL_REF_SSCLK# H47 — DPLL_REF_SSCLK# 29

PEG_CLK K44 — CLK_MCH_3GPLL 29
PEG_CLK# K45 — CLK_MCH_3GPLL# 29

GMCH DMI

DMI_RXN_0 AN47 — DMI_TXN0
DMI_RXN_1 AJ38 — DMI_TXN1
DMI_RXN_2 AN42 — DMI_TXN2
DMI_RXN_3 AN46 — DMI_TXN3 — DMI_TXN[3:0] 21

DMI_RXP_0 AM47 — DMI_TXP0
DMI_RXP_1 AJ39 — DMI_TXP1
DMI_RXP_2 AN41 — DMI_TXP2
DMI_RXP_3 AN45 — DMI_TXP3 — DMI_TXP[0..3] 21

DMI_TXN_0 AJ46 — DMI_RXN0
DMI_TXN_1 AJ41 — DMI_RXN1
DMI_TXN_2 AM40 — DMI_RXN2
DMI_TXN_3 AM44 — DMI_RXN3 — DMI_RXN[0..3] 21

DMI_TXP_0 AJ47 — DMI_RXP0
DMI_TXP_1 AJ42 — DMI_RXP1
DMI_TXP_2 AM39 — DMI_RXP2
DMI_TXP_3 AM43 — DMI_RXP3 — DMI_RXP[0..3] 21

29 MCH_BSEL0 — CFG_0 P27
29 MCH_BSEL1 — CFG_1 N27
29 MCH_BSEL2 — CFG_2 N24
CFG_3 C21
CFG_4 C23
MCH_CFG_5 — CFG_5 F23
CFG_6 N23
CFG_7 G23
MCH_CFG_8 — CFG_8 J20
MCH_CFG_9 — CFG_9 C20
CFG_10 R24
MCH_CFG_12 — CFG_11 L23
MCH_CFG_13 — CFG_12 J23
CFG_13 E23
CFG_14 E20
CFG_15 K23
MCH_CFG_16 — CFG_16 M20
CFG_17 M24
CFG_18 L32
MCH_CFG_19 — CFG_19 N33
MCH_CFG_20 — CFG_20 L35

7 PM_EXTTS#0 — PM_EXTTS#0
8 PM_EXTTS#1 — PM_EXTTS#1

GMCH GRAPHICS VID

PM_BM_BUSY# G41
PM_DPRSTP# L39
PM_EXT_TS#_0 L36
PM_EXT_TS#_1 J36
PWROK AW49
RSTIN# AV20
THERMTRIP# N20
DPRSLPVR G36

22 PM_BMBUSY# — RX1101 2 — 1 0Ohm DPRSTP#
3,20,80 H_DPRSTP# — R1114 2 — 1 10KOhm PM_EXTTS#0
+3VS — R1115 2 — 1 10KOhm PM_EXTTS#1
R1138 2 — 1 0Ohm
22,30 ICH8_PWROK — RX1104 1 — 2 100Ohm RST_IN_MCH#
21,30,43,51 PLT_RST#
3,20 PM_THRMTRIP#
22,80 PM_DPRSLPVR — RX1102 1 — 2 0Ohm DPRSLPVR

GFX_VID_0 E35
GFX_VID_1 A39
GFX_VID_2 C38
GFX_VID_3 B38
GFX_VR_EN E36

GMCH MISC

CL_CLK AM49
CL_DATA AK50
CL_PWROK AT43 — CL_PWROK — R1118 0Ohm — ICH8_PWROK
CL_RST# AN49 — CL_RST#0 22
CL_VREF AM50 — MCH_CLVREF

SDVO_CTRL_CLK H35 — SDVO_CTRL_CLK — SDVO_CTRL_CLK 18
SDVO_CTRL_DATA K36 — SDVO_CTRL_DATA — SDVO_CTRL_DATA 18
CLK_REQ# G39 — MCH_CLK_REQ# — MCH_CLK_REQ# 22
ICH_SYNC# G40 — MCH_ICH_SYNC# 22

TEST_1 A37 — R1123 1 — 2 0Ohm
TEST_2 B32 — R1124 1 — 2 22kOhm — GND

BJ51 NC_1
BK51 NC_2
BK50 NC_3
BL50 NC_4
BL49 NC_5
BL3 NC_6
BL2 NC_7
BK1 NC_8
BJ1 NC_9
E1 NC_10
A5 NC_11
C51 NC_12
B50 NC_13
A50 NC_14
A49 NC_15
BK2 NC_16

CRESTLINE_965GM

+1.25VS — R1112 1KOhm 1% — MCH_CLVREF — R1117 392Ohm 1% — C1101 0.1UF/10V — GND GND

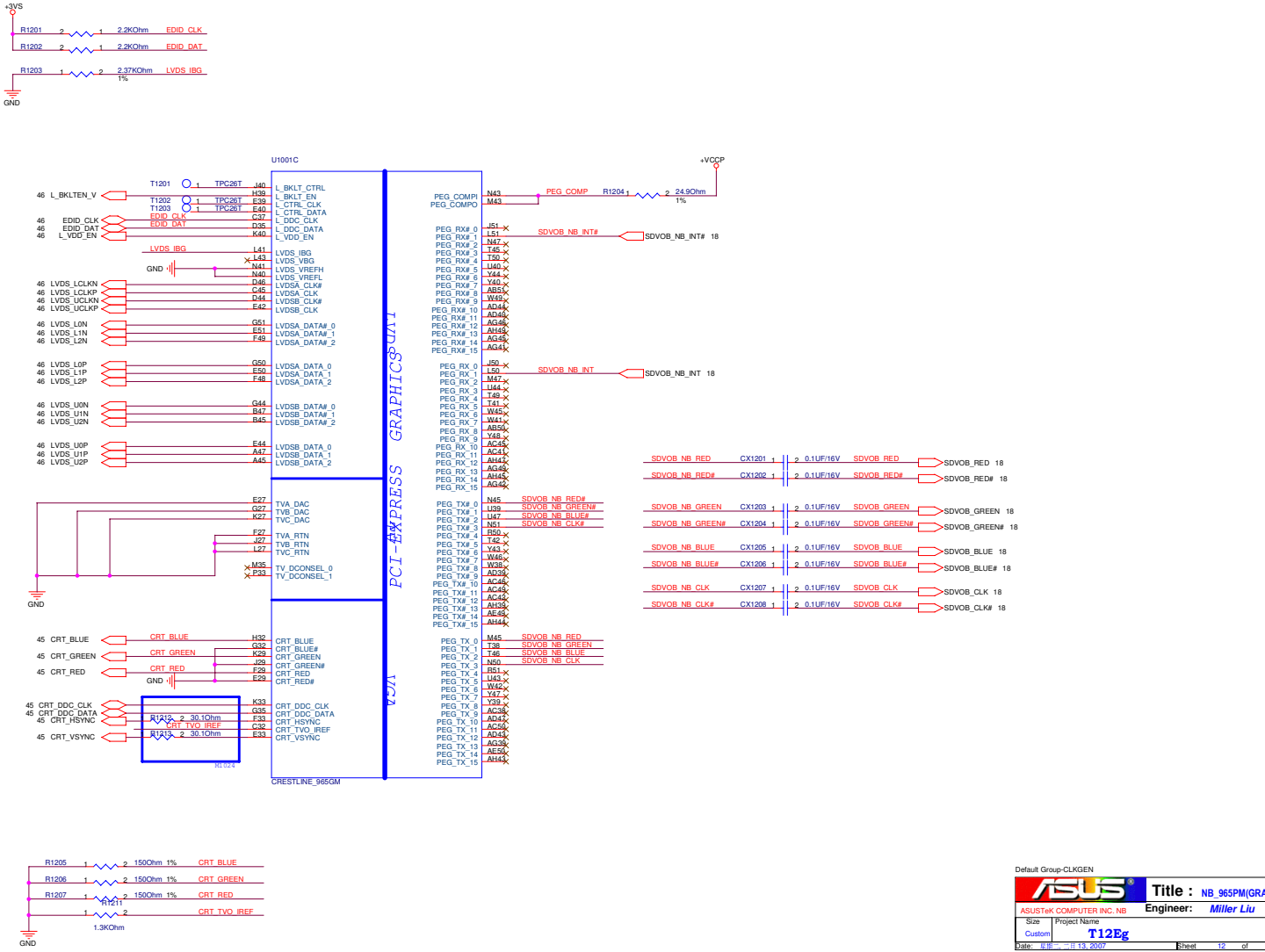
+3VS — R1113 10KOhm r0402 — MCH_CLK_REQ#

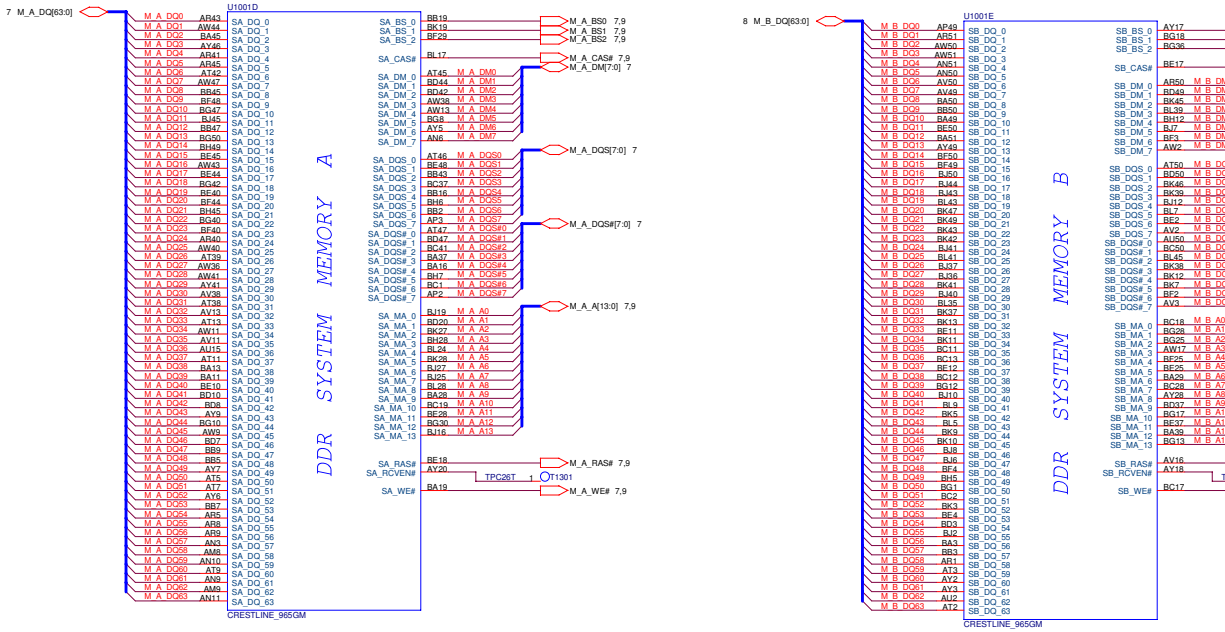
+1.8V — R1119 1KOhm 1%
R1122 3.01KOhm 1% — C1103 1UF/10V — C1104 0.01UF/16V — GND GND — SM_RCOMP_VOH
R1127 1KOhm 1% — C1106 1UF/10V — C1107 0.01UF/16V — GND GND GND — SM_RCOMP_VOL

Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

Title : NB-965GM(DMI & CFG)
Engineer: Miller Liu
Size: Custom
Project Name: T12Fg
Rev: 2.0
Date: 星期一, 二月 13, 2007
Sheet 11 of 94


+3VS
R1201 2 1 2.2KOhm EDID_CLK
R1202 2 1 2.2KOhm EDID_DAT
R1203 1 2 2.37KOhm 1% LVDS_IBG
GND
U1001C
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_965GM
+VCCP
R1204 1 2 24.9Ohm 1%
PEG_COMP
SDVOB_NB_INT#
SDVOB_NB_INT# 18
SDVOB_NB_INT
SDVOB_NB_INT 18
SDVOB_NB_RED
SDVOB_NB_RED#
CX1201 1 2 0.1UF/16V SDVOB_RED
CX1202 1 2 0.1UF/16V SDVOB_RED#
SDVOB_RED 18
SDVOB_RED# 18
SDVOB_NB_GREEN
SDVOB_NB_GREEN#
CX1203 1 2 0.1UF/16V SDVOB_GREEN
CX1204 1 2 0.1UF/16V SDVOB_GREEN#
SDVOB_GREEN 18
SDVOB_GREEN# 18
SDVOB_NB_BLUE
SDVOB_NB_BLUE#
CX1205 1 2 0.1UF/16V SDVOB_BLUE
CX1206 1 2 0.1UF/16V SDVOB_BLUE#
SDVOB_BLUE 18
SDVOB_BLUE# 18
SDVOB_NB_CLK
SDVOB_NB_CLK#
CX1207 1 2 0.1UF/16V SDVOB_CLK
CX1208 1 2 0.1UF/16V SDVOB_CLK#
SDVOB_CLK 18
SDVOB_CLK# 18
T1201 1 TPC26T
T1202 1 TPC26T
T1203 1 TPC26T
46 L_BKLTEN_V
46 EDID_CLK
46 EDID_DAT
46 L_VDD_EN
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
GND
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
46 LVDS_LCLKN
46 LVDS_LCLKP
46 LVDS_UCLKN
46 LVDS_UCLKP
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
46 LVDS_L0N
46 LVDS_L1N
46 LVDS_L2N
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
46 LVDS_L0P
46 LVDS_L1P
46 LVDS_L2P
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
46 LVDS_U0N
46 LVDS_U1N
46 LVDS_U2N
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
46 LVDS_U0P
46 LVDS_U1P
46 LVDS_U2P
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL_0
TV_DCONSEL_1
GND
45 CRT_BLUE
45 CRT_GREEN
45 CRT_RED
CRT_BLUE
CRT_GREEN
CRT_RED
GND
CRT_BLUE
CRT_BLUE#
CRT_GREEN#
CRT_RED
CRT_RED#
45 CRT_DDC_CLK
45 CRT_DDC_DATA
45 CRT_HSYNC
45 CRT_VSYNC
R1212 2 30.1Ohm
CRT_TVO_IREF
R1213 2 30.1Ohm
R1024
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
R1205 1 2 150Ohm 1% CRT_BLUE
R1206 1 2 150Ohm 1% CRT_GREEN
R1207 1 2 150Ohm 1% CRT_RED
R1211
1.3KOhm
CRT_TVO_IREF
GND
Default Group-CLKGEN
Title : NB_965PM(GRAPHIC)
ASUSTeK COMPUTER INC. NB
Engineer: Miller Liu
Size Custom
Project Name T12Eg
Rev 2.0
Date: 星期一, 二月 13, 2007
Sheet 12 of 94



Default Group-CLKGEN

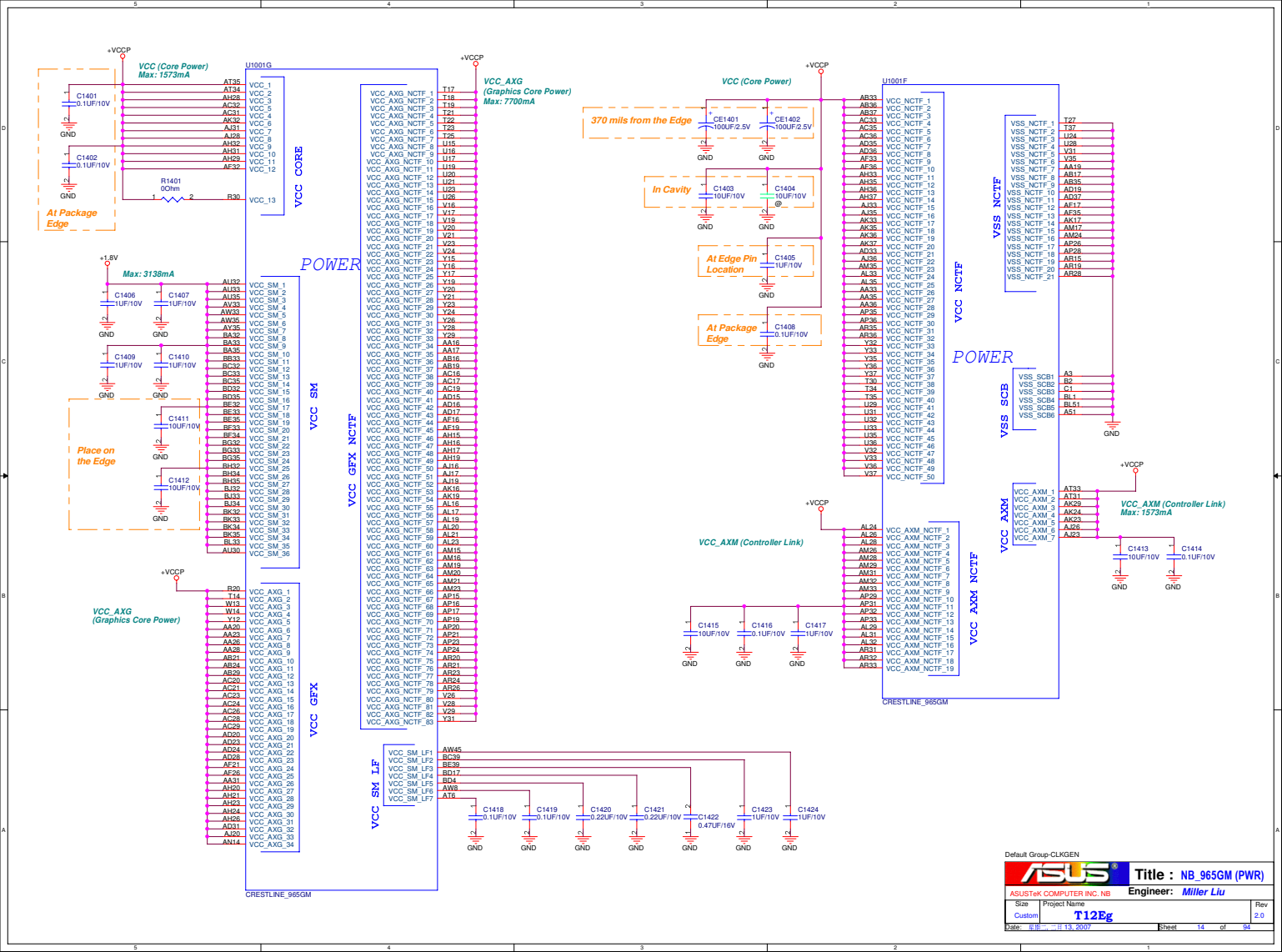
ASUSTeK COMPUTER INC. NB

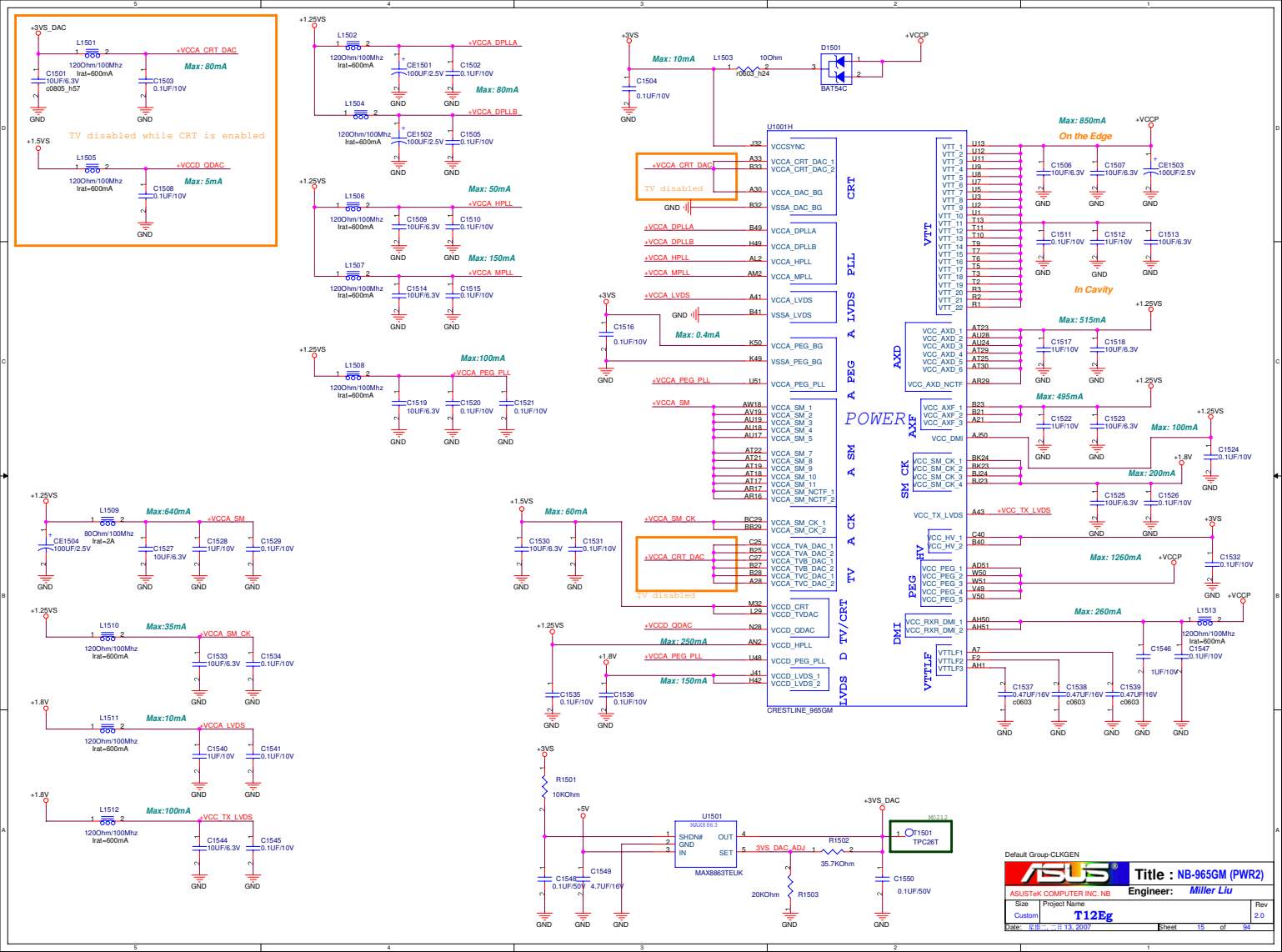
Title : NB-965PM(DDR2)

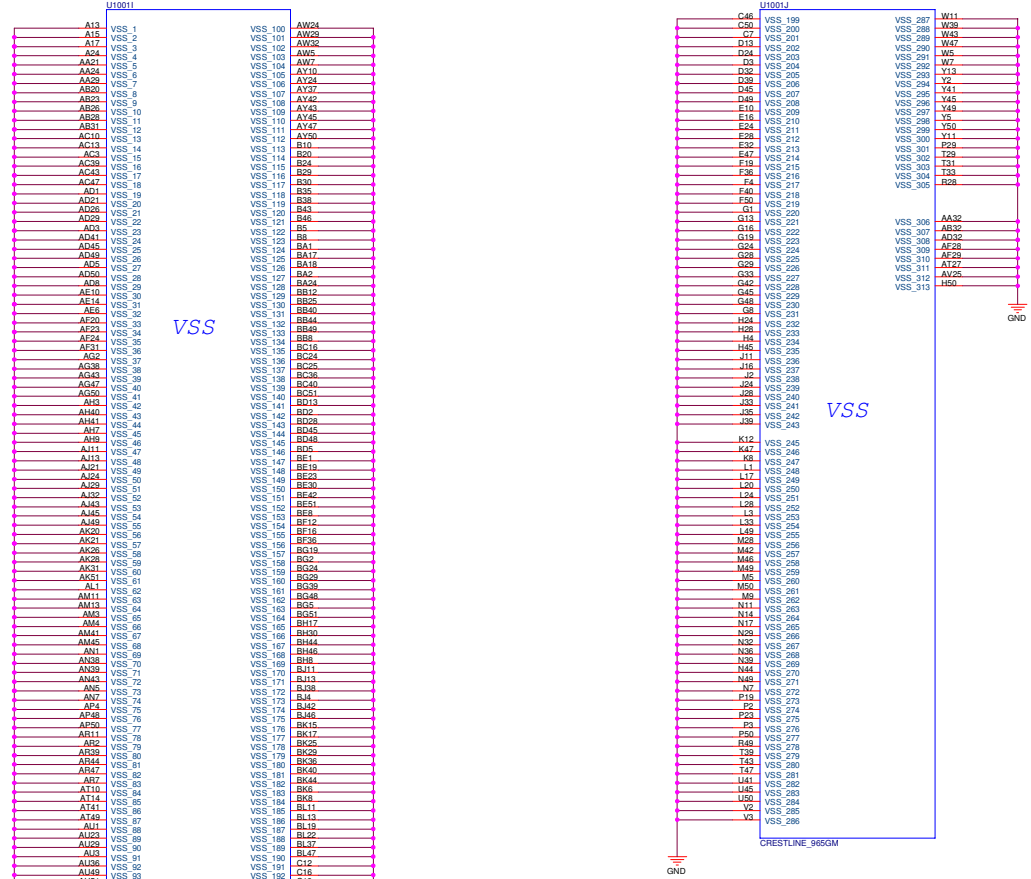
Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期一, 二月 13, 2007 Sheet 13 of 94


VCC (Core Power)
Max: 1573mA
U1001G
VCC CORE
At Package Edge
+1.8V
Max: 3138mA
POWER
VCC SM
VCC GFX NCTF
Place on the Edge
VCC_AXG
(Graphics Core Power)
VCC GFX
VCC_AXG
(Graphics Core Power)
Max: 7700mA
VCC SM LF
CRESTLINE_965GM
370 mils from the Edge
In Cavity
At Edge Pin Location
At Package Edge
U1001F
VCC NCTF
VSS NCTF
VSS SCB
VCC_AXM (Controller Link)
VCC_AXM (Controller Link)
Max: 1573mA
VCC AXM
VCC AXM NCTF
CRESTLINE_965GM
Default Group-CLKGEN
Title : NB_965GM (PWR)
ASUSTeK COMPUTER INC. NB
Engineer: Miller Liu
Size
Custom
Project Name
T12Eg
Rev
2.0
Date: 星期一, 二月 13, 2007
Sheet 14 of 94


+3VS_DAC
L1501
120Ohm/100Mhz
Irat=600mA
+VCCA_CRT_DAC
Max: 80mA
C1501
10UF/6.3V
c0805_h57
C1503
0.1UF/10V
GND
TV disabled while CRT is enabled
+1.5VS
L1505
+VCCD_QDAC
Max: 5mA
C1508
0.1UF/10V
+1.25VS
L1502
+VCCA_DPLLA
CE1501
100UF/2.5V
C1502
0.1UF/10V
L1504
+VCCA_DPLLB
CE1502
C1505
L1506
+VCCA_HPLL
Max: 50mA
C1509
10UF/6.3V
C1510
L1507
+VCCA_MPLL
Max: 150mA
C1514
C1515
L1508
+VCCA_PEG_PLL
Max:100mA
C1519
C1520
C1521
+3VS
Max: 10mA
L1503
10Ohm
r0603_h24
D1501
BAT54C
+VCCP
C1504
0.1UF/10V
U1001H
J32 VCCSYNC
A33 VCCA_CRT_DAC_1
B33 VCCA_CRT_DAC_2
+VCCA_CRT_DAC
TV disabled
A30 VCCA_DAC_BG
B32 VSSA_DAC_BG
CRT
+VCCA_DPLLA
B49 VCCA_DPLLA
+VCCA_DPLLB
H49 VCCA_DPLLB
+VCCA_HPLL
AL2 VCCA_HPLL
+VCCA_MPLL
AM2 VCCA_MPLL
PLL
+VCCA_LVDS
A41 VCCA_LVDS
B41 VSSA_LVDS
LVDS
+3VS
C1516
0.1UF/10V
Max: 0.4mA
K50 VCCA_PEG_BG
K49 VSSA_PEG_BG
+VCCA_PEG_PLL
U51 VCCA_PEG_PLL
PEG
+VCCA_SM
AW18 VCCA_SM_1
AV19 VCCA_SM_2
AU19 VCCA_SM_3
AU18 VCCA_SM_4
AU17 VCCA_SM_5
AT22 VCCA_SM_7
AT21 VCCA_SM_8
AT19 VCCA_SM_9
AT18 VCCA_SM_10
AT17 VCCA_SM_11
AR17 VCCA_SM_NCTF_1
AR16 VCCA_SM_NCTF_2
SM
+VCCA_SM_CK
BC29 VCCA_SM_CK_1
BB29 VCCA_SM_CK_2
SM_CK
+VCCA_CRT_DAC
C25 VCCA_TVA_DAC_1
B25 VCCA_TVA_DAC_2
C27 VCCA_TVB_DAC_1
B27 VCCA_TVB_DAC_2
B28 VCCA_TVC_DAC_1
A28 VCCA_TVC_DAC_2
TV disabled
TV
M32 VCCD_CRT
L29 VCCD_TVDAC
TV/CRT
+VCCD_QDAC
N28 VCCD_QDAC
Max: 250mA
AN2 VCCD_HPLL
+VCCA_PEG_PLL
U48 VCCD_PEG_PLL
Max: 150mA
J41 VCCD_LVDS_1
H42 VCCD_LVDS_2
LVDS
CRESTLINE_965GM
POWER
VTT
U13 VTT_1
U12 VTT_2
U11 VTT_3
U9 VTT_4
U8 VTT_5
U7 VTT_6
U5 VTT_7
U3 VTT_8
U2 VTT_9
U1 VTT_10
T13 VTT_11
T11 VTT_12
T10 VTT_13
T9 VTT_14
T7 VTT_15
T6 VTT_16
T5 VTT_17
T3 VTT_18
T2 VTT_19
R3 VTT_20
R2 VTT_21
R1 VTT_22
Max: 850mA
On the Edge
+VCCP
C1506
10UF/6.3V
C1507
10UF/6.3V
CE1503
100UF/2.5V
C1511
0.1UF/10V
C1512
1UF/10V
C1513
10UF/6.3V
In Cavity
AXD
VCC_AXD_1
VCC_AXD_2
VCC_AXD_3
VCC_AXD_4
VCC_AXD_5
VCC_AXD_6
VCC_AXD_NCTF
AT23
AU28
AU24
AT29
AT25
AT30
AR29
+1.25VS
Max: 515mA
C1517
1UF/10V
C1518
10UF/6.3V
AXF
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
B23
B21
A21
Max: 495mA
VCC_DMI
AJ50
SM_CK
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
BK24
BK23
BJ24
BJ23
C1522
1UF/10V
C1523
10UF/6.3V
+1.25VS
Max: 100mA
C1524
0.1UF/10V
+1.8V
Max: 200mA
C1525
10UF/6.3V
C1526
0.1UF/10V
VCC_TX_LVDS
A43
+VCC_TX_LVDS
HV
VCC_HV_1
VCC_HV_2
C40
B40
+3VS
C1532
0.1UF/10V
PEG
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
AD51
W50
W51
V49
V50
Max: 1260mA
+VCCP
DMI
VCC_RXR_DMI_1
VCC_RXR_DMI_2
AH50
AH51
Max: 260mA
C1513
120Ohm/100Mhz
Irat=600mA
C1546
10UF/10V
C1547
0.1UF/10V
VTTLF
VTTLF1
VTTLF2
VTTLF3
A7
F2
AH1
C1537
0.47UF/16V
c0603
C1538
0.47UF/16V
c0603
C1539
0.47UF/16V
c0603
GND
+1.25VS
L1509
Max:640mA
+VCCA_SM
CE1504
100UF/2.5V
80Ohm/100Mhz
Irat=2A
C1527
10UF/6.3V
C1528
10UF/10V
C1529
0.1UF/10V
+1.25VS
L1510
Max:35mA
+VCCA_SM_CK
C1533
10UF/6.3V
C1534
0.1UF/10V
+1.8V
L1511
Max:10mA
+VCCA_LVDS
C1540
1UF/10V
C1541
0.1UF/10V
+1.8V
L1512
Max:100mA
+VCC_TX_LVDS
C1544
10UF/6.3V
C1545
0.1UF/10V
+1.5VS
Max: 60mA
C1530
10UF/6.3V
C1531
0.1UF/10V
+1.25VS
C1535
0.1UF/10V
+1.8V
C1536
0.1UF/10V
+3VS
R1501
10KOhm
+5V
U1501
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
C1548
0.1UF/50V
4.7UF/16V
C1549
3VS_DAC_ADJ
R1502
35.7KOhm
20KOhm
R1503
+3VS_DAC
MS212
T1501
TPC26T
C1550
0.1UF/50V
Default Group-CLKGEN
Title : NB-965GM (PWR2)
ASUSTeK COMPUTER INC. NB
Engineer: Miller Liu
Size
Custom
Project Name
T12Eg
Rev
2.0
Date: 星期一, 二月 13, 2007
Sheet 15 of 94

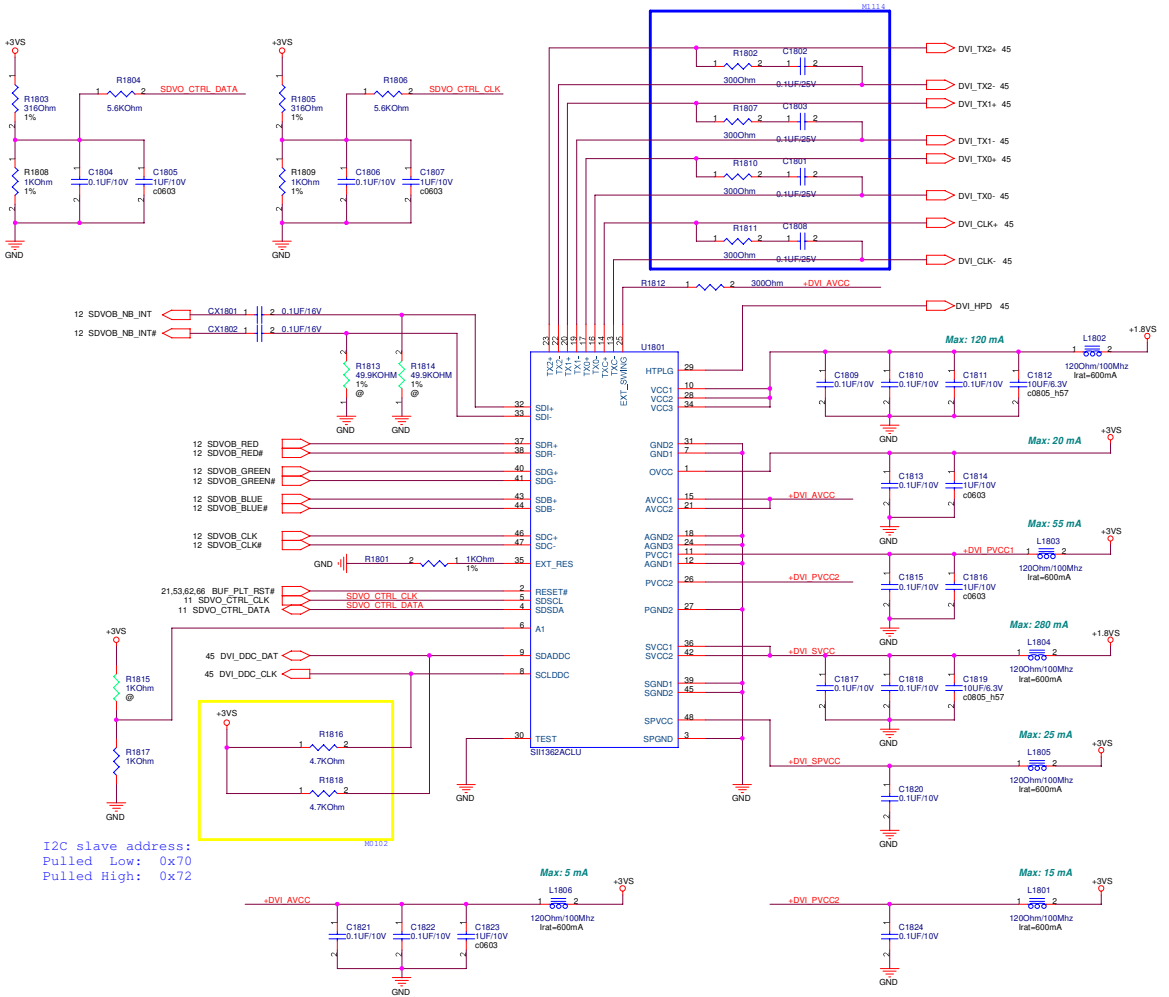


Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : NB_965GM (GND)	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 16 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 17 of 94	



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : Sil362A SDVO-DVI

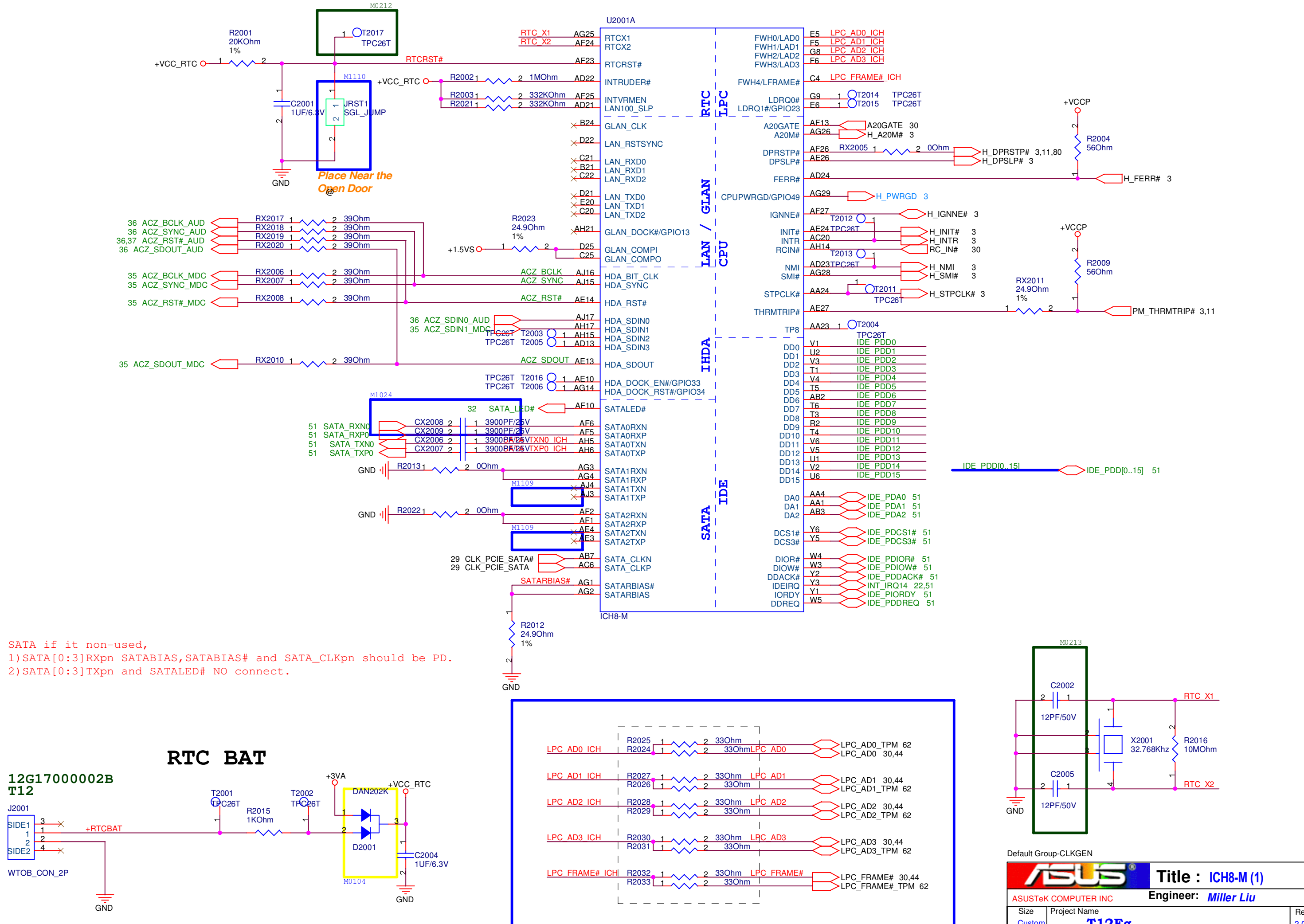
Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 18 of 94

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 19 of 94	


U2001A
ICH8-M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
R2001 20KOhm 1%
+VCC_RTC
RTCRST#
C2001 1UF/6.3V
JRST1 SGL_JUMP
T2017 TPC26T
Place Near the Open Door
R2002 1MOhm
R2003 332KOhm
R2021 332KOhm
R2023 24.9Ohm 1%
+1.5VS
36 ACZ_BCLK_AUD
36 ACZ_SYNC_AUD
36,37 ACZ_RST#_AUD
36 ACZ_SDOUT_AUD
35 ACZ_BCLK_MDC
35 ACZ_SYNC_MDC
35 ACZ_RST#_MDC
35 ACZ_SDOUT_MDC
36 ACZ_SDIN0_AUD
35 ACZ_SDIN1_MDC
RX2017 39Ohm
RX2018 39Ohm
RX2019 39Ohm
RX2020 39Ohm
RX2006 39Ohm
RX2007 39Ohm
RX2008 39Ohm
RX2010 39Ohm
32 SATA_LED#
51 SATA_RXN0
51 SATA_RXP0
51 SATA_TXN0
51 SATA_TXP0
CX2008 3900PF/25V
CX2009 3900PF/25V
CX2006 3900PF/25V
CX2007 3900PF/25V
R2013 0Ohm
R2022 0Ohm
GND
29 CLK_PCIE_SATA#
29 CLK_PCIE_SATA
R2012 24.9Ohm 1%
LPC_AD0_ICH
LPC_AD1_ICH
LPC_AD2_ICH
LPC_AD3_ICH
LPC_FRAME#_ICH
T2014 TPC26T
T2015 TPC26T
A20GATE 30
H_A20M# 3
RX2005 0Ohm
H_DPRSTP# 3,11,80
H_DPSLP# 3
+VCCP
R2004 56Ohm
H_FERR# 3
H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RC_IN# 30
H_NMI 3
H_SMI# 3
H_STPCLK# 3
R2009 56Ohm
RX2011 24.9Ohm 1%
PM_THRMTRIP# 3,11
IDE_PDD[0..15] 51
IDE_PDA0 51
IDE_PDA1 51
IDE_PDA2 51
IDE_PDCS1# 51
IDE_PDCS3# 51
IDE_PDIOR# 51
IDE_PDIOW# 51
IDE_PDDACK# 51
INT_IRQ14 22,51
IDE_PIORDY 51
IDE_PDDREQ 51
C2002 12PF/50V
C2005 12PF/50V
X2001 32.768Khz
R2016 10MOhm
RTC_X1
RTC_X2
R2025 33Ohm
R2024 33Ohm
LPC_AD0_TPM 62
LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD1_TPM 62
LPC_AD2 30,44
LPC_AD2_TPM 62
LPC_AD3 30,44
LPC_AD3_TPM 62
LPC_FRAME# 30,44
LPC_FRAME#_TPM 62
RTC BAT
12G17000002B
T12
J2001
WTOB_CON_2P
+RTCBAT
R2015 1KOhm
+3VA
DAN202K
D2001
C2004 1UF/6.3V
T2001 TPC26T
T2002 TPC26T

SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

Default Group-CLKGEN

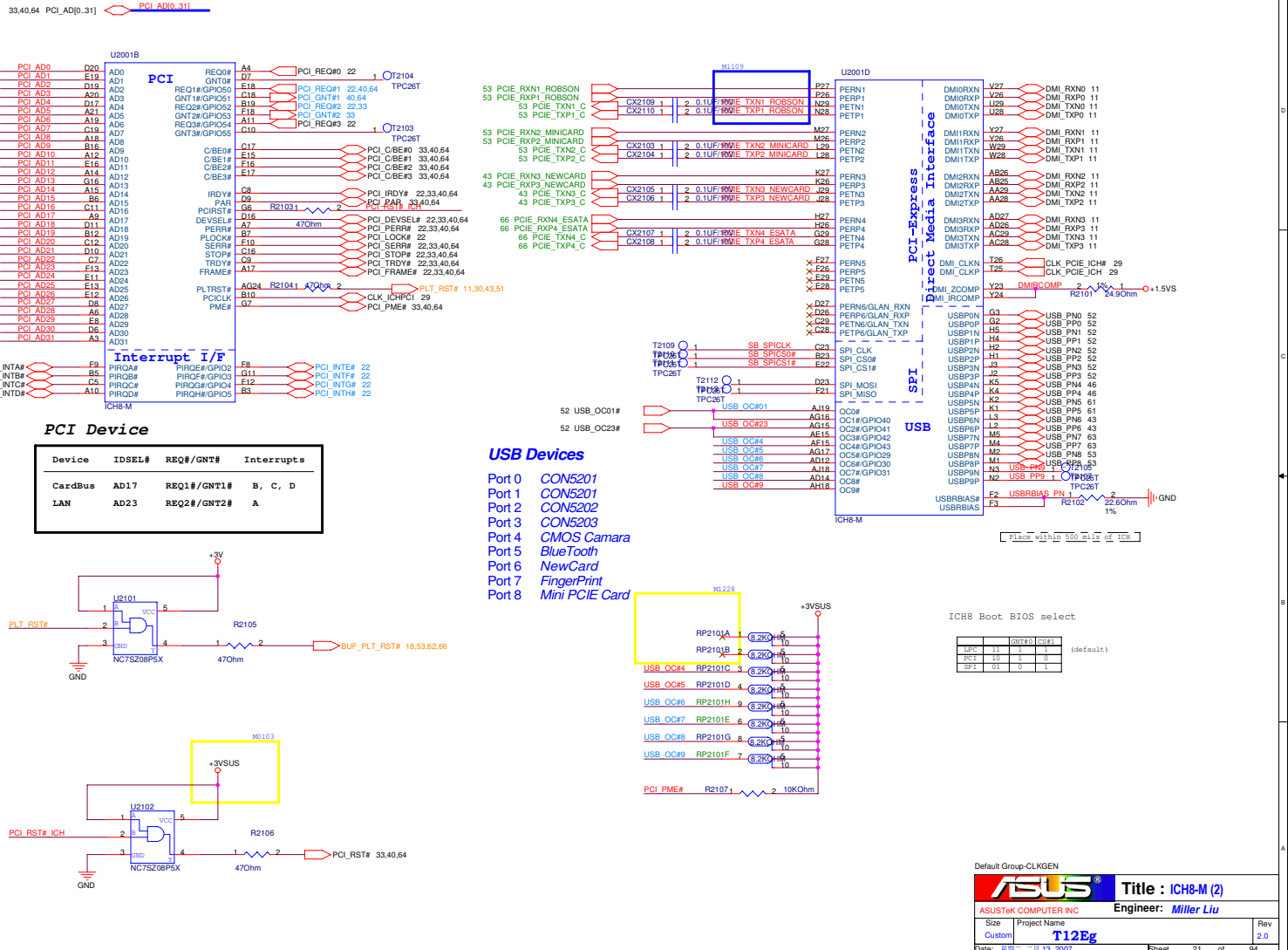
Title : ICH8-M (1)

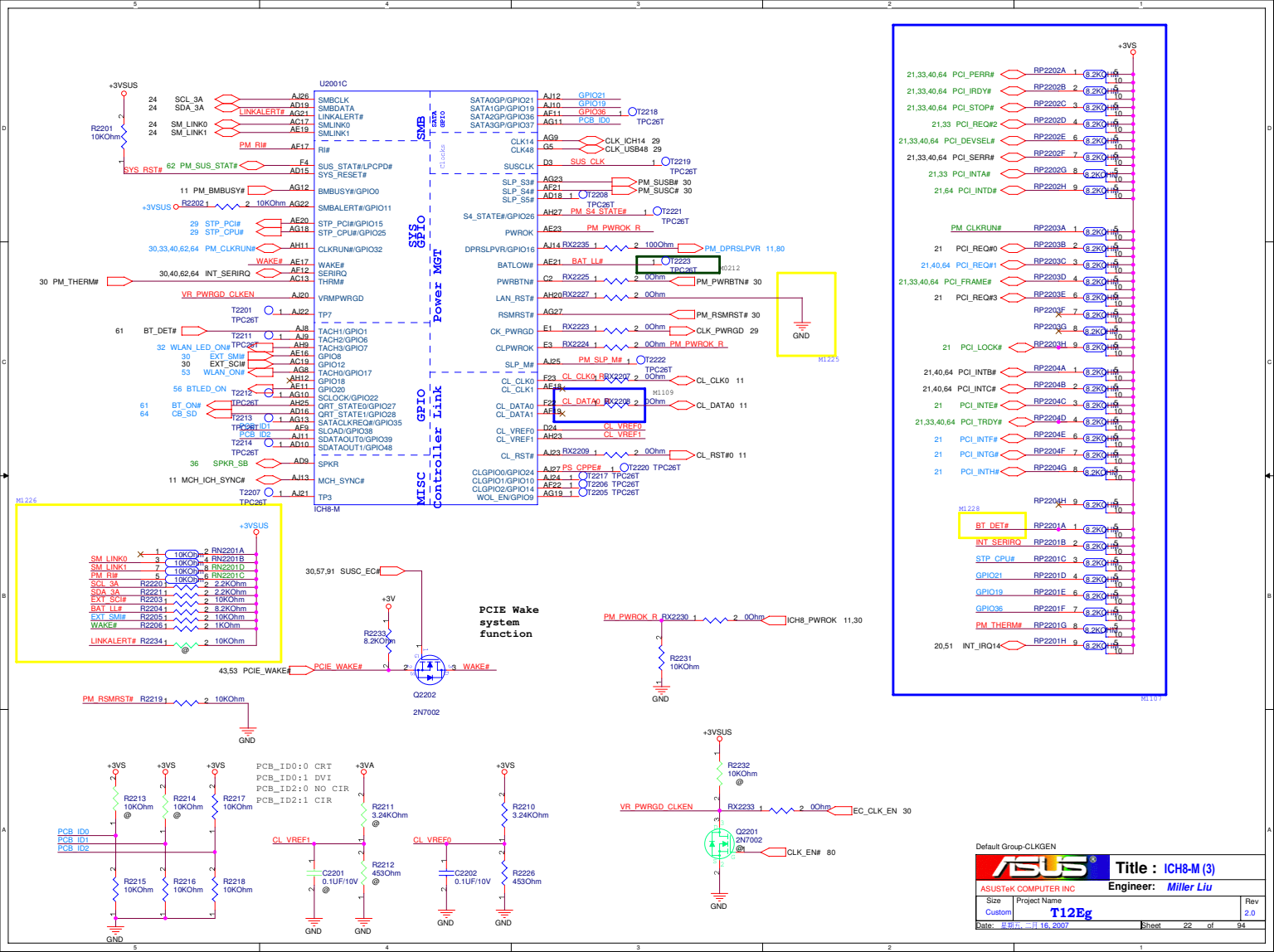
ASUSTeK COMPUTER INC

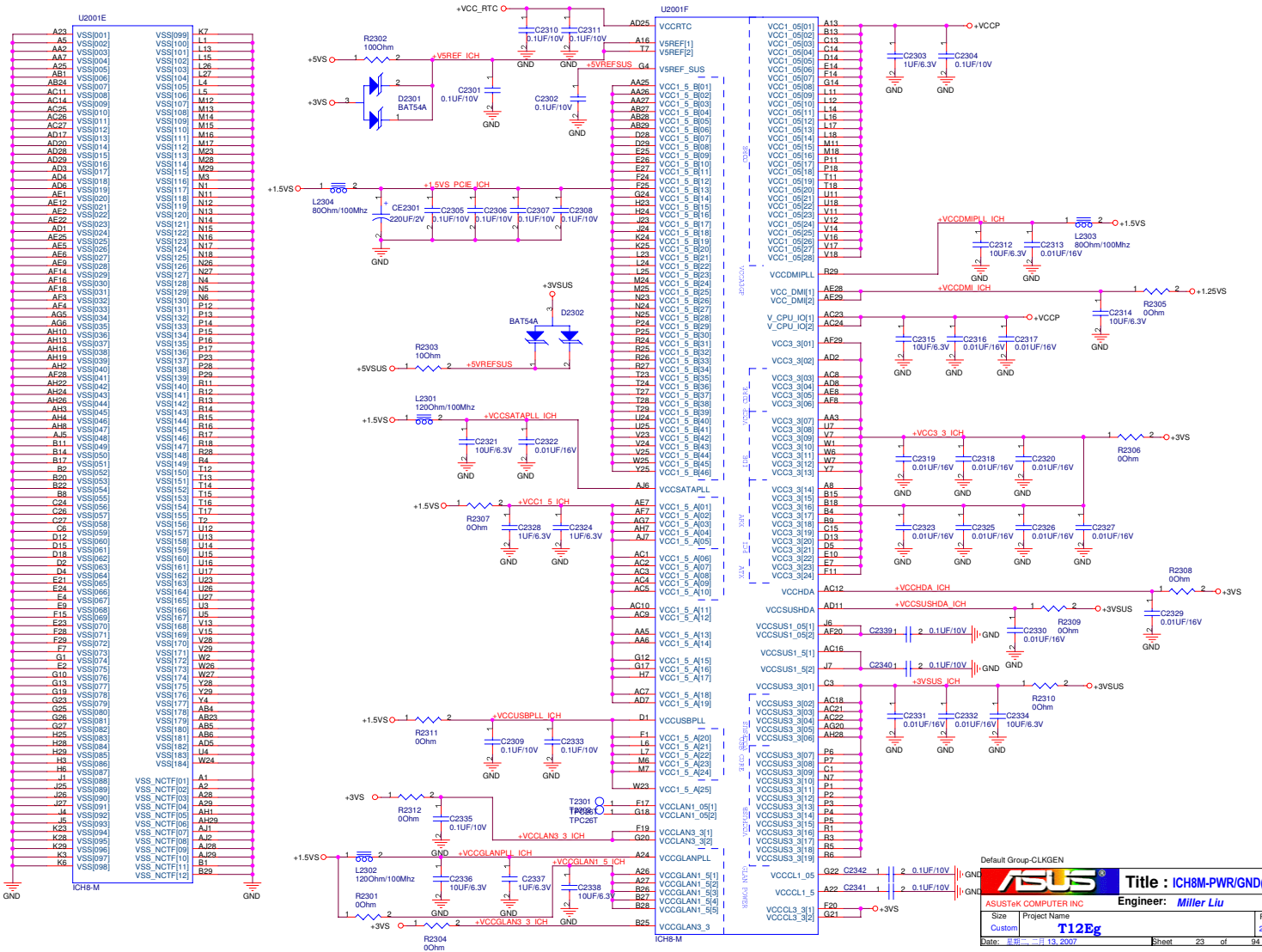
Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

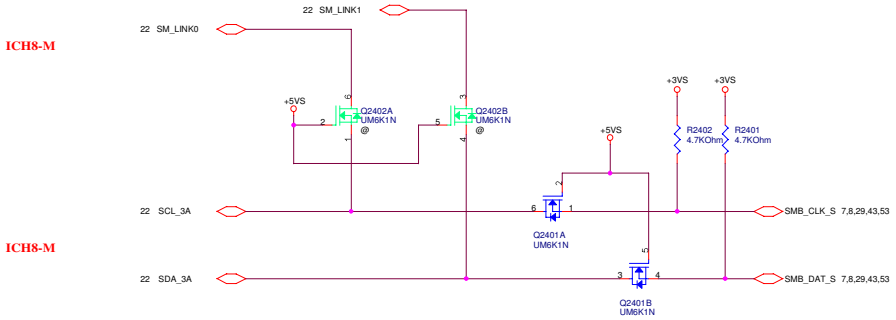
Date: 星期二, 二月 13, 2007 Sheet 20 of 94


33,40,64 PCI_AD[0..31]
PCI_AD[0..31]
U2001B
PCI
PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25 PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31
REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
PCI_REQ#0 22
PCI_GNT#1 22,40,64
PCI_REQ#2 40,64
PCI_GNT#2 22,33
PCI_REQ#3 22
T2104 TPC26T
T2103 TPC26T
C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C/BE#0 33,40,64
PCI_C/BE#1 33,40,64
PCI_C/BE#2 33,40,64
PCI_C/BE#3 33,40,64
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PCI_IRDY# 22,33,40,64
PCI_PAR 33,40,64
PCI_RST# 11,30,43,51
R21031 47Ohm
PCI_DEVSEL# 22,33,40,64
PCI_PERR# 22,33,40,64
PCI_LOCK# 22
PCI_SERR# 22,33,40,64
PCI_STOP# 22,33,40,64
PCI_TRDY# 22,33,40,64
PCI_FRAME# 22,33,40,64
PLTRST# PCICLK PME#
AG24 R21041 47Ohm
B10 CLK_ICHPCI 29
G7 PCI_PME# 33,40,64
Interrupt I/F
PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PCI_INTE# 22
PCI_INTF# 22
PCI_INTG# 22
PCI_INTH# 22
ICH8-M
22,33 PCI_INTA#
22,40,64 PCI_INTB#
22,40,64 PCI_INTC#
22,64 PCI_INTD#
PCI Device
Device IDSEL# REQ#/GNT# Interrupts
CardBus AD17 REQ1#/GNT1# B, C, D
LAN AD23 REQ2#/GNT2# A
M1109
53 PCIE_RXN1_ROBSON
53 PCIE_RXP1_ROBSON
53 PCIE_TXN1_C
53 PCIE_TXP1_C
CX2109 CX2110 0.1UF/10V PCIE_TXN1_ROBSON PCIE_TXP1_ROBSON
53 PCIE_RXN2_MINICARD
53 PCIE_RXP2_MINICARD
53 PCIE_TXN2_C
53 PCIE_TXP2_C
CX2103 CX2104 0.1UF/10V PCIE_TXN2_MINICARD PCIE_TXP2_MINICARD
43 PCIE_RXN3_NEWCARD
43 PCIE_RXP3_NEWCARD
43 PCIE_TXN3_C
43 PCIE_TXP3_C
CX2105 CX2106 0.1UF/10V PCIE_TXN3_NEWCARD PCIE_TXP3_NEWCARD
66 PCIE_RXN4_ESATA
66 PCIE_RXP4_ESATA
66 PCIE_TXN4_C
66 PCIE_TXP4_C
CX2107 CX2108 0.1UF/10V PCIE_TXN4_ESATA PCIE_TXP4_ESATA
U2001D
PCI-Express Direct Media Interface
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_RXN0 11
DMI_RXP0 11
DMI_TXN0 11
DMI_TXP0 11
DMI_RXN1 11
DMI_RXP1 11
DMI_TXN1 11
DMI_TXP1 11
DMI_RXN2 11
DMI_RXP2 11
DMI_TXN2 11
DMI_TXP2 11
DMI_RXN3 11
DMI_RXP3 11
DMI_TXN3 11
DMI_TXP3 11
DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# 29
CLK_PCIE_ICH 29
DMI_ZCOMP DMI_IRCOMP
DMIRCOMP
R2101 24.9Ohm 1%
+1.5VS
SPI
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO
T2109 T2110 T2111 T2112 TPC26T
SB_SPICLK SB_SPICS0# SB_SPICS1#
USB
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P
USB_PN9 USB_PP9 T2105 T2106 TPC26T
USBRBIAS USBRBIAS_PN
R2102 22.6Ohm 1%
GND
ICH8-M
Place within 500 mils of ICH
52 USB_OC01#
52 USB_OC23#
USB_OC#01 USB_OC#23 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
USB Devices
Port 0 CON5201
Port 1 CON5201
Port 2 CON5202
Port 3 CON5203
Port 4 CMOS Camara
Port 5 BlueTooth
Port 6 NewCard
Port 7 FingerPrint
Port 8 Mini PCIE Card
M1228
+3VSUS
RP2101A RP2101B RP2101C RP2101D RP2101H RP2101E RP2101G RP2101F 8.2KOHM
PCI_PME# R2107 10KOhm
ICH8 Boot BIOS select
GNT#0 CS#1
LPC 11 1 1
PCI 10 1 0
SPI 01 0 1
(default)
+3V
U2101
PLT_RST#
R2105
BUF_PLT_RST# 18,53,62,66
NC7SZ08P5X
47Ohm
GND
M0103
+3VSUS
U2102
PCI_RST# ICH
R2106
PCI_RST# 33,40,64
NC7SZ08P5X
47Ohm
GND
Default Group-CLKGEN
Title : ICH8-M (2)
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Size Custom
Project Name T12Eg
Rev 2.0
Date: 星期二, 二月 13, 2007
Sheet 21 of 94


U2001C
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SMB
DATA
GPIO
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
PCB_ID0
TPC26T
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
CLK14
CLK48
CLK_ICH14
CLK_USB48
SUSCLK
SUS_CLK
SLP_S3#
SLP_S4#
SLP_S5#
PM_SUSB#
PM_SUSC#
S4_STATE#/GPIO26
PM_S4_STATE#
PWROK
PM_PWROK_R
DPRSLPVR/GPIO16
PM_DPRSLPVR
BATLOW#
BAT_LL#
PWRBTN#
PM_PWRBTN#
LAN_RST#
RSMRST#
PM_RSMRST#
CK_PWRGD
CLK_PWRGD
CLPWROK
SLP_M#
PM_SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CL_RST#0
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
SMBMUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
ICH8-M
SYS
GPIO
Power MGT
GPIO
Controller Link
MISC
+3VSUS
+3V
+3VS
+3VA
GND
SCL_3A
SDA_3A
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
SYS_RST#
PM_SUS_STAT#
PM_BMBUSY#
PM_CLKRUN#
INT_SERIRQ
PM_THERM#
BT_DET#
WLAN_LED_ON#
EXT_SMI#
EXT_SCI#
WLAN_ON#
BTLED_ON
BT_ON#
CB_SD
PCB_ID1
PCB_ID2
SPKR_SB
MCH_ICH_SYNC#
M1226
SM_LINK0
SM_LINK1
PM_RI#
SCL_3A
SDA_3A
EXT_SCI#
BAT_LL#
EXT_SMI#
WAKE#
LINKALERT#
RN2201A
RN2201B
RN2201D
RN2201C
SUSC_EC#
PCIE_WAKE#
WAKE#
Q2202
2N7002
PCIE Wake
system
function
PM_PWROK_R
ICH8_PWROK
PM_RSMRST#
PCB_ID0:0 CRT
PCB_ID0:1 DVI
PCB_ID2:0 NO CIR
PCB_ID2:1 CIR
CL_VREF1
CL_VREF0
C2201
C2202
0.1UF/10V
VR_PWRGD_CLKEN
EC_CLK_EN
CLK_EN#
Q2201
2N7002
M1225
M1228
M1107
PCI_PERR#
PCI_IRDY#
PCI_STOP#
PCI_REQ#2
PCI_DEVSEL#
PCI_SERR#
PCI_INTA#
PCI_INTD#
PM_CLKRUN#
PCI_REQ#0
PCI_REQ#1
PCI_FRAME#
PCI_REQ#3
PCI_LOCK#
PCI_INTB#
PCI_INTC#
PCI_INTE#
PCI_TRDY#
PCI_INTF#
PCI_INTG#
PCI_INTH#
BT_DET#
INT_SERIRQ
STP_CPU#
GPIO21
GPIO19
GPIO36
PM_THERM#
INT_IRQ14
Default Group-CLKGEN
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Size
Custom
Project Name
T12Eg
Rev
2.0
Date: 星期五, 二月 16, 2007
Sheet 22 of 94


U2001E
ICH8-M
U2001F
ICH8-M
+VCC_RTC
R2302 100Ohm
+5VS
+3VS
D2301 BAT54A
+V5REF_ICH
+5VREFSUS
C2301 0.1UF/10V
C2302 0.1UF/10V
C2310 0.1UF/10V
C2311 0.1UF/10V
+1.5VS
L2304 80Ohm/100Mhz
CE2301 220UF/2V
C2305 0.1UF/10V
C2306 0.1UF/10V
C2307 0.1UF/10V
C2308 0.1UF/10V
+1.5V5_PCIE_ICH
+3VSUS
D2302 BAT54A
R2303 10Ohm
+5VSUS
L2301 120Ohm/100Mhz
+1.5VS
+VCCSATAPLL_ICH
C2321 10UF/6.3V
C2322 0.01UF/16V
R2307 0Ohm
+VCC1_5_ICH
C2328 1UF/6.3V
C2324 1UF/6.3V
R2311 0Ohm
+VCCUSBPLL_ICH
C2309 0.1UF/10V
C2333 0.1UF/10V
R2312 0Ohm
C2335 0.1UF/10V
+VCCLAN3_3_ICH
L2302 120Ohm/100Mhz
+VCCGLANPLL_ICH
C2336 10UF/6.3V
C2337 1UF/6.3V
+VCCGLAN1_5_ICH
C2338 10UF/6.3V
R2301 0Ohm
+3VS
+VCCGLAN3_3_ICH
R2304 0Ohm
T2301 TP26T
+VCCP
C2303 1UF/6.3V
C2304 0.1UF/10V
+VCCDMIPLL_ICH
C2312 10UF/6.3V
C2313 0.01UF/16V
L2303 80Ohm/100Mhz
+VCCDMI_ICH
C2314 10UF/6.3V
R2305 0Ohm
+1.25VS
C2315 10UF/6.3V
C2316 0.01UF/16V
C2317 0.01UF/16V
+VCC3_3_ICH
C2319 0.01UF/16V
C2318 0.01UF/16V
C2320 0.01UF/16V
R2306 0Ohm
C2323 0.01UF/16V
C2325 0.01UF/16V
C2326 0.01UF/16V
C2327 0.01UF/16V
+VCCHDA_ICH
R2308 0Ohm
C2329 0.01UF/16V
+VCCSUSHDA_ICH
R2309 0Ohm
C2330 0.01UF/16V
C23391 0.1UF/10V
C23401 0.1UF/10V
+3VSUS_ICH
R2310 0Ohm
C2331 0.01UF/16V
C2332 0.01UF/16V
C2334 10UF/6.3V
C2342 0.1UF/10V
C2341 0.1UF/10V
GND
Default Group-CLKGEN
Title : ICH8M-PWR/GND(4)
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Size Custom
Project Name T12Eg
Rev 2.0
Date: 星期二, 二月 13, 2007
Sheet 23 of 94

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : ICH8M-Other

Engineer: *Miller Liu*

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 某月二十三月 13, 2007 Sheet 24 of 94

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Jeffrey Lai*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 25 of 94	

Default Group-CLKGEN

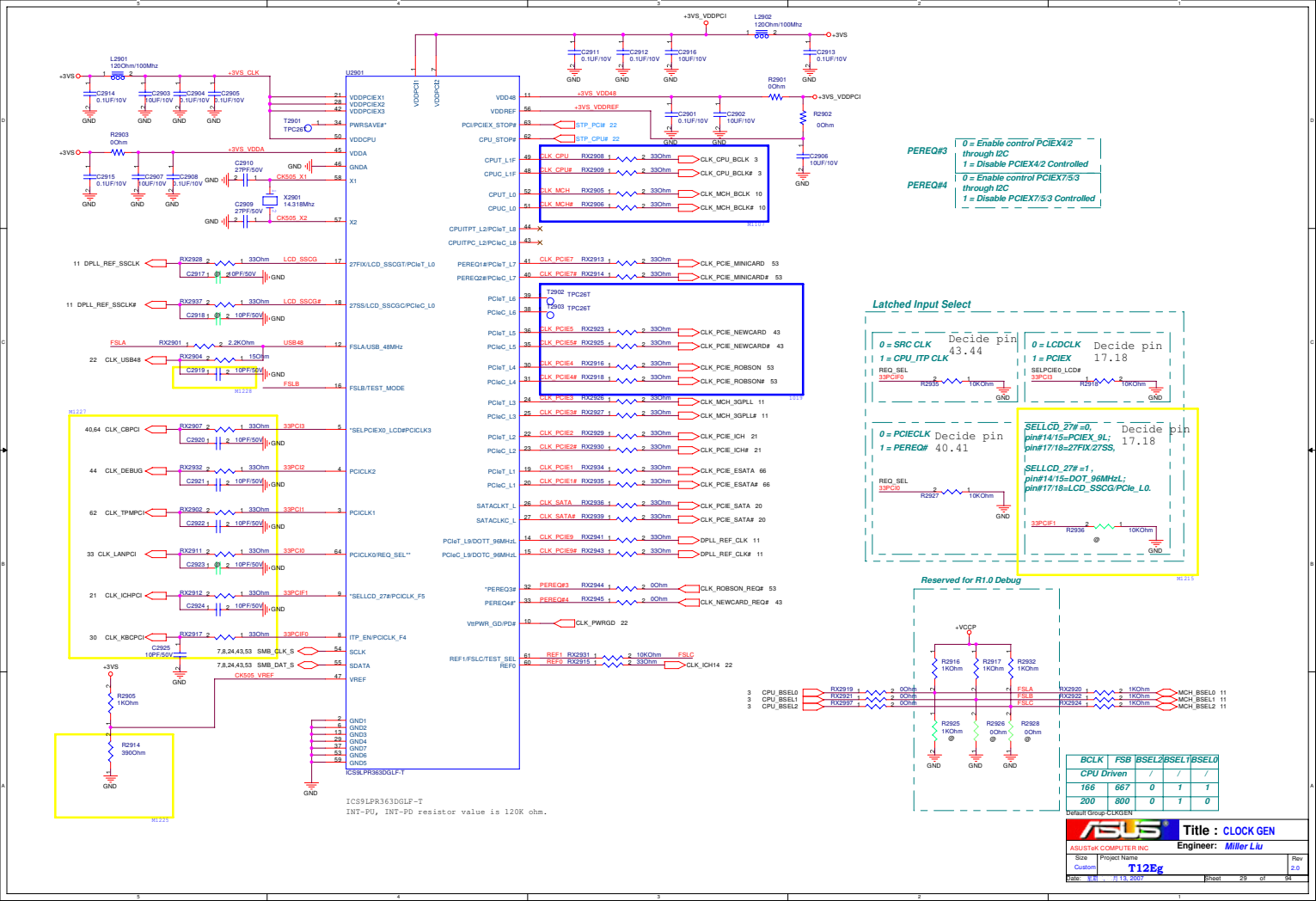
ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 26 of 94	

Default Group-CLKGEN

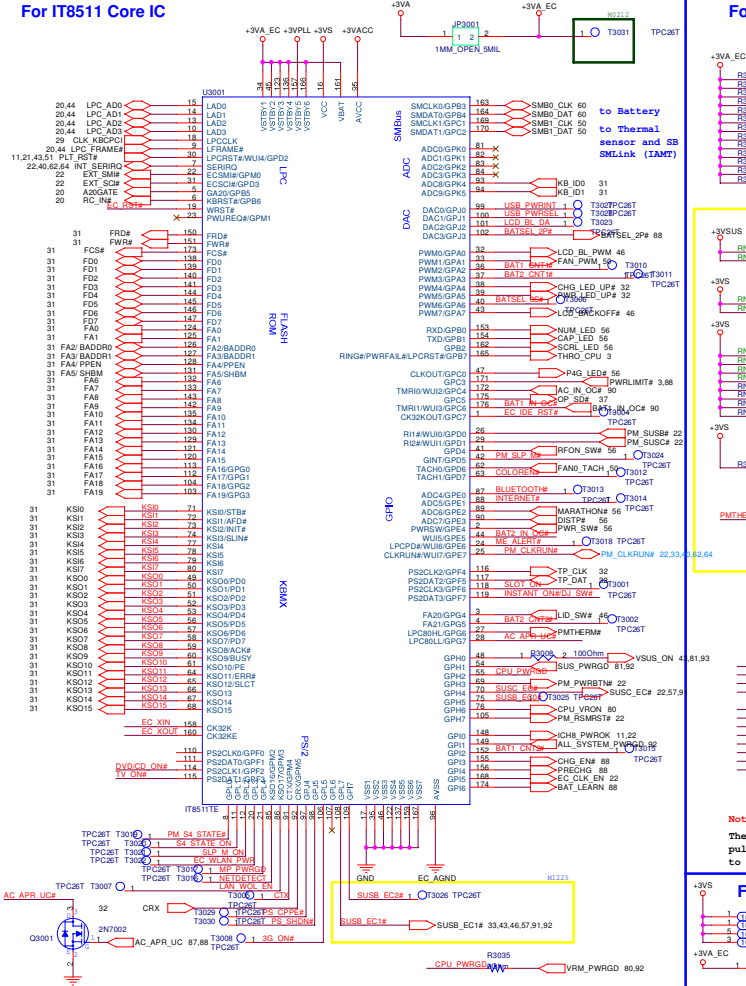
ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 27 of 94	

Default Group-CLKGEN

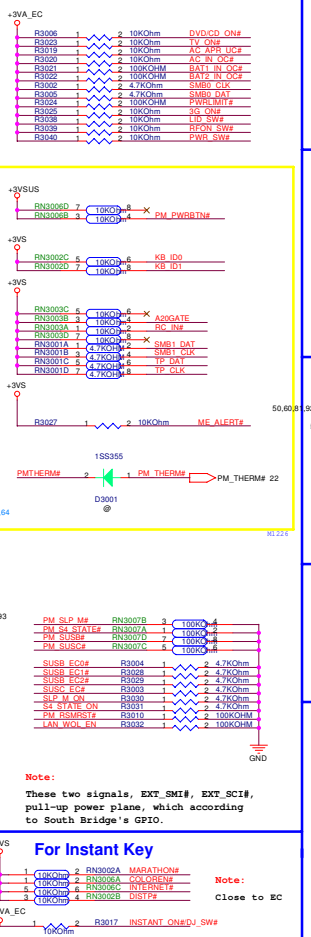
ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 28 of 94	


U2901
ICS9LPR363DGLF-T
INT-PU, INT-PD resistor value is 120K ohm.
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
CPU Driven / / /
166 667 0 1 1
200 800 0 1 0
Default Group-CLKGEN
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Project Name T12Eg
Rev 2.0
Sheet 29 of 94

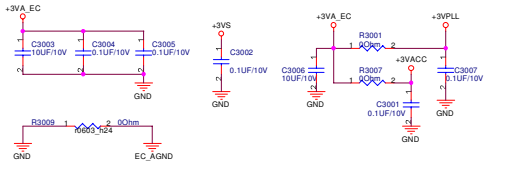
For IT8511 Core IC



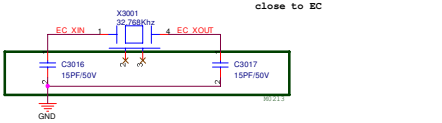
For Pull-up/Pull-down



For IT8511 Power

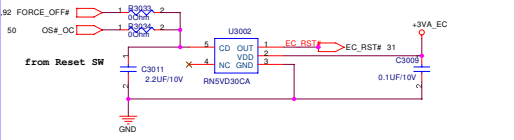


For Xtal



Note:
Cload=12.5PF
close to EC

For EC reset



Note:

For EC Hardware Strap

I/O Base Address	Share Memory	PP Enable
Note: It can be programmable by EC fireware	Note: It can be programmable by EC fireware	Note: Default Internal Pull-Low

For Intel IAMT pin name

ME_ALERT#	EC_WLAN_PWR
PM_S4_STATE#	MP_PWRGD
S4_STATE_ON	NETDETECT
PM_SLP_M#	LAN_WOL_EN
SLP_M_ON	
WLAN_SW#	

For Instant Key

Note:
These two signals, EXT_SMI#, EXT_SCI#, pull-up power plane, which according to South Bridge's GPIO.

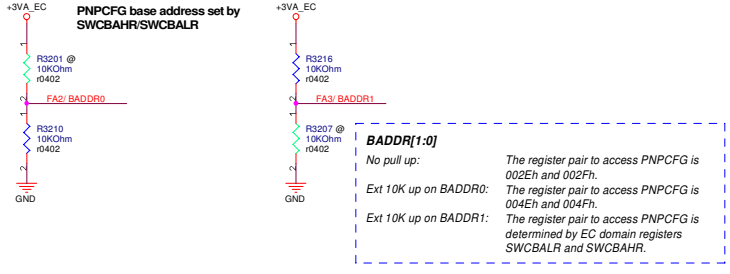
Note:
Close to EC

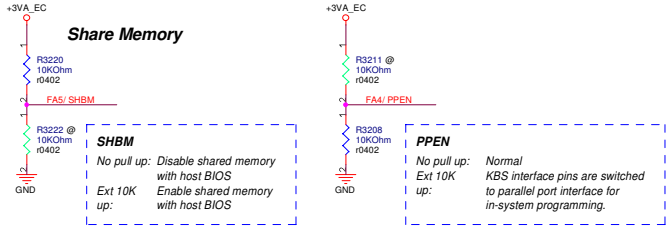
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : EC-ITE8511 (2)	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 星期一, 一月 13, 2007	Sheet 30 of 94	

EC Hardware Strap

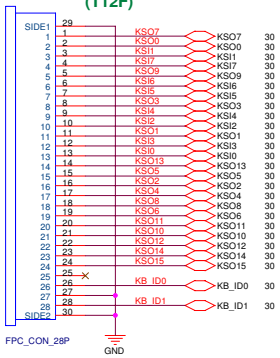
Strap value sampled after VSTBY power up reset





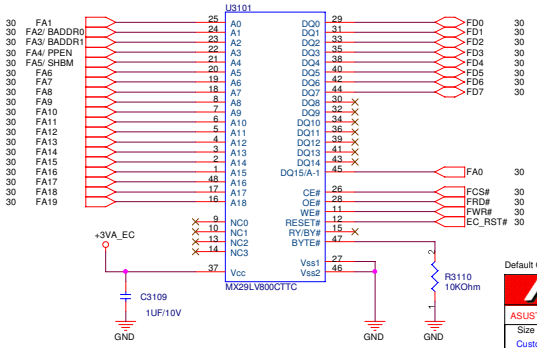
Keyboard Conn.

P/N: 12G182402806 (T12F)



For 8M bits ISA ROM

8M TSOP



Note:

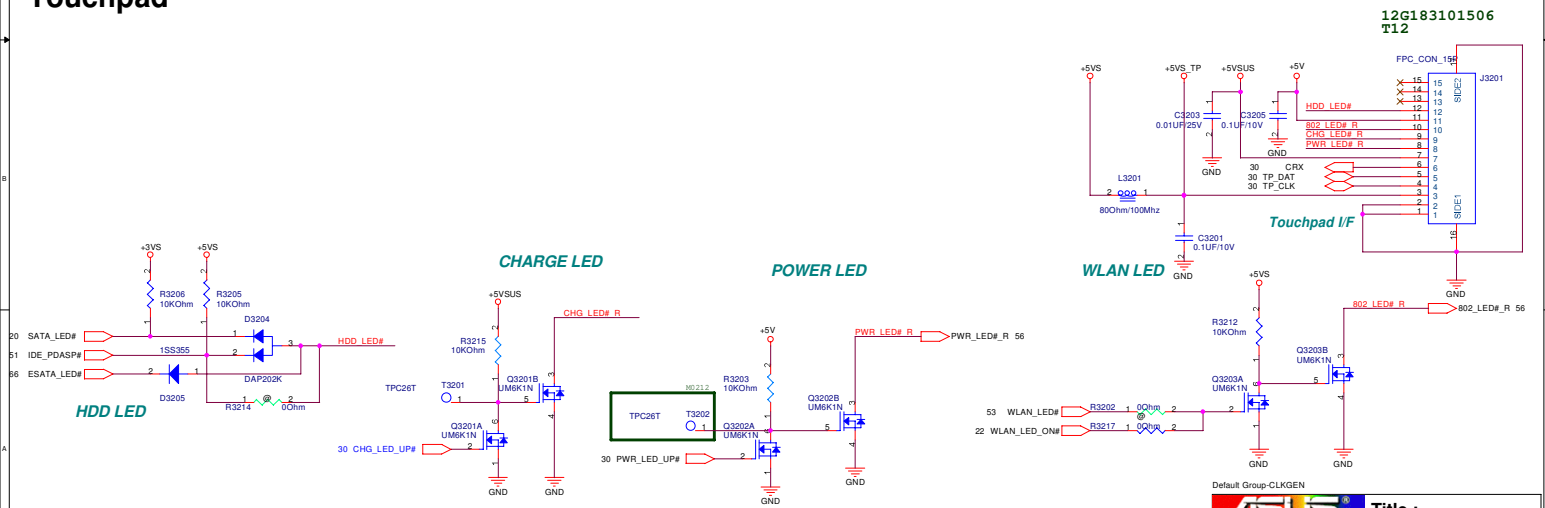
If you use 8M bits ROM, you need to connect FA19 to EC side.

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : EC-ITE8511(2)		
	Engineer: Miller Liu		
Size: Custom	Project Name: T12Eg		Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 31 of 94		

Touchpad

12G183101506
T12



Default Group-CLKGEN

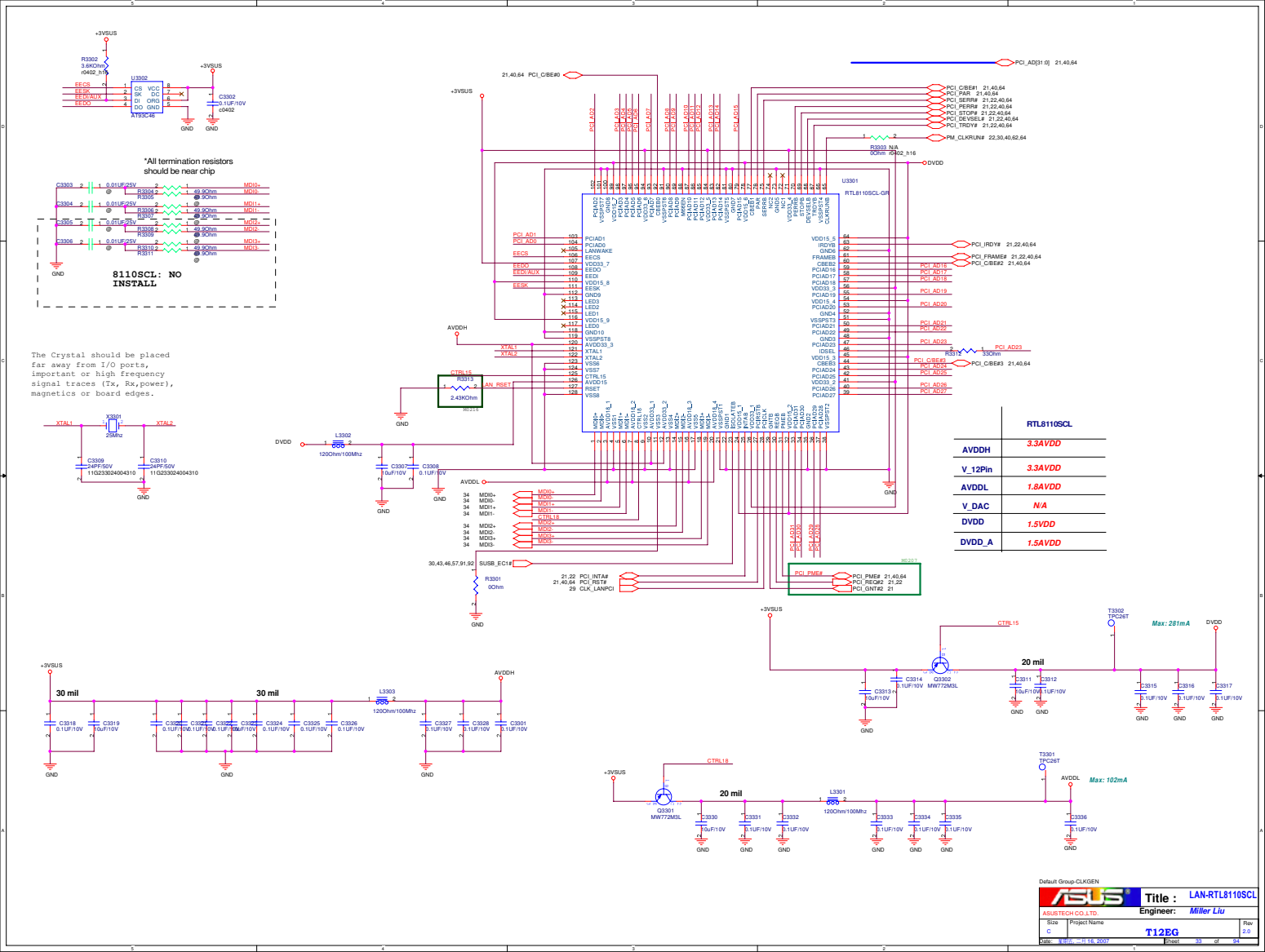
ASUSTeK COMPUTER INC

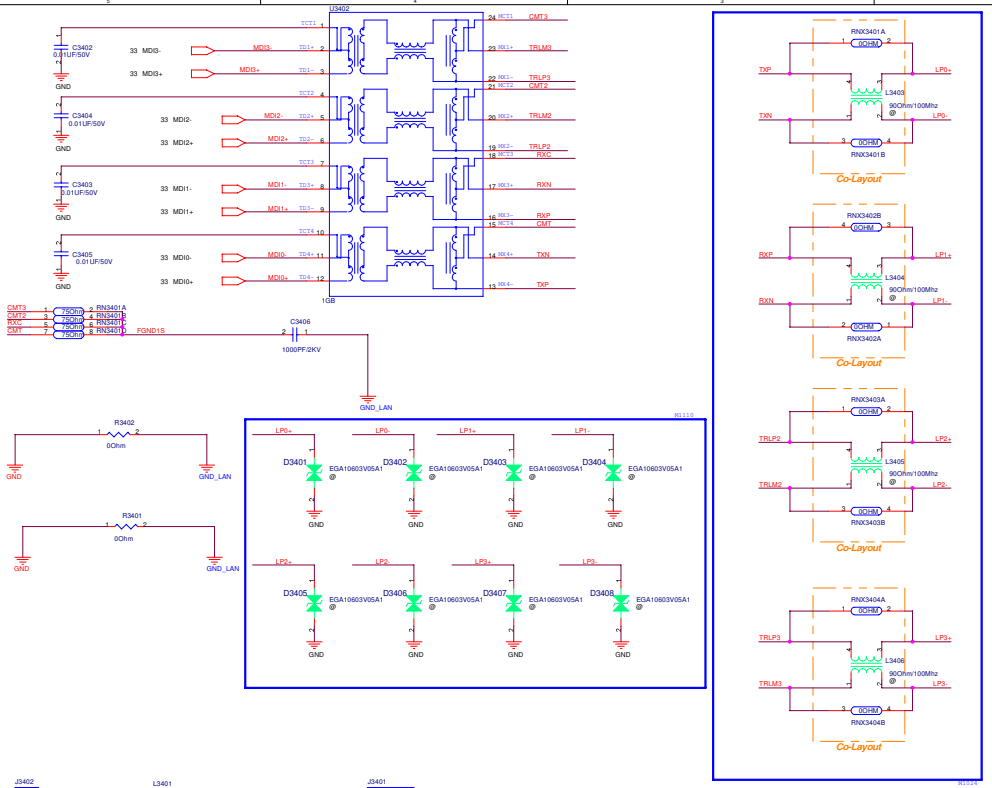
Title : TouchPad

Engineer: Miller Liu

Size	Project Name	Rev
A3	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 32 of 94

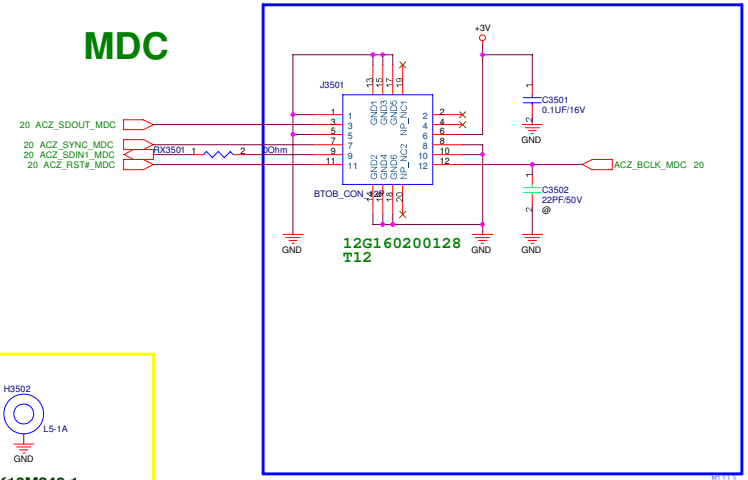

*All termination resistors should be near chip
8110SCL: NO INSTALL
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
RTL8110SCL-GR
RTL8110SCL
3.3AVDD
3.3AVDD
1.8AVDD
N/A
1.5VDD
1.5AVDD
30 mil
20 mil
Max: 281mA
Max: 102mA
Default Group-CLKGEN
Title : LAN-RTL8110SCL
ASUSTeCH CO.,LTD.
Engineer: Miller Liu
Project Name T12EG
Rev 2.0
Sheet 33 of 94

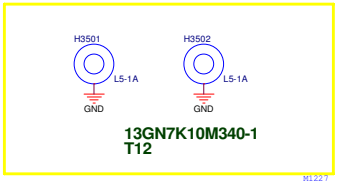


Default Group-CLKGEN

ASUSTECH CO.,LTD.	Title :	RJ11/RJ45	
	Engineer:	Miller Liu	
Size: C	Project Name: T12EG		Rev: 2.0
Date: 星期二, 一月 13, 2007	Sheet 34 of 94		

MDC

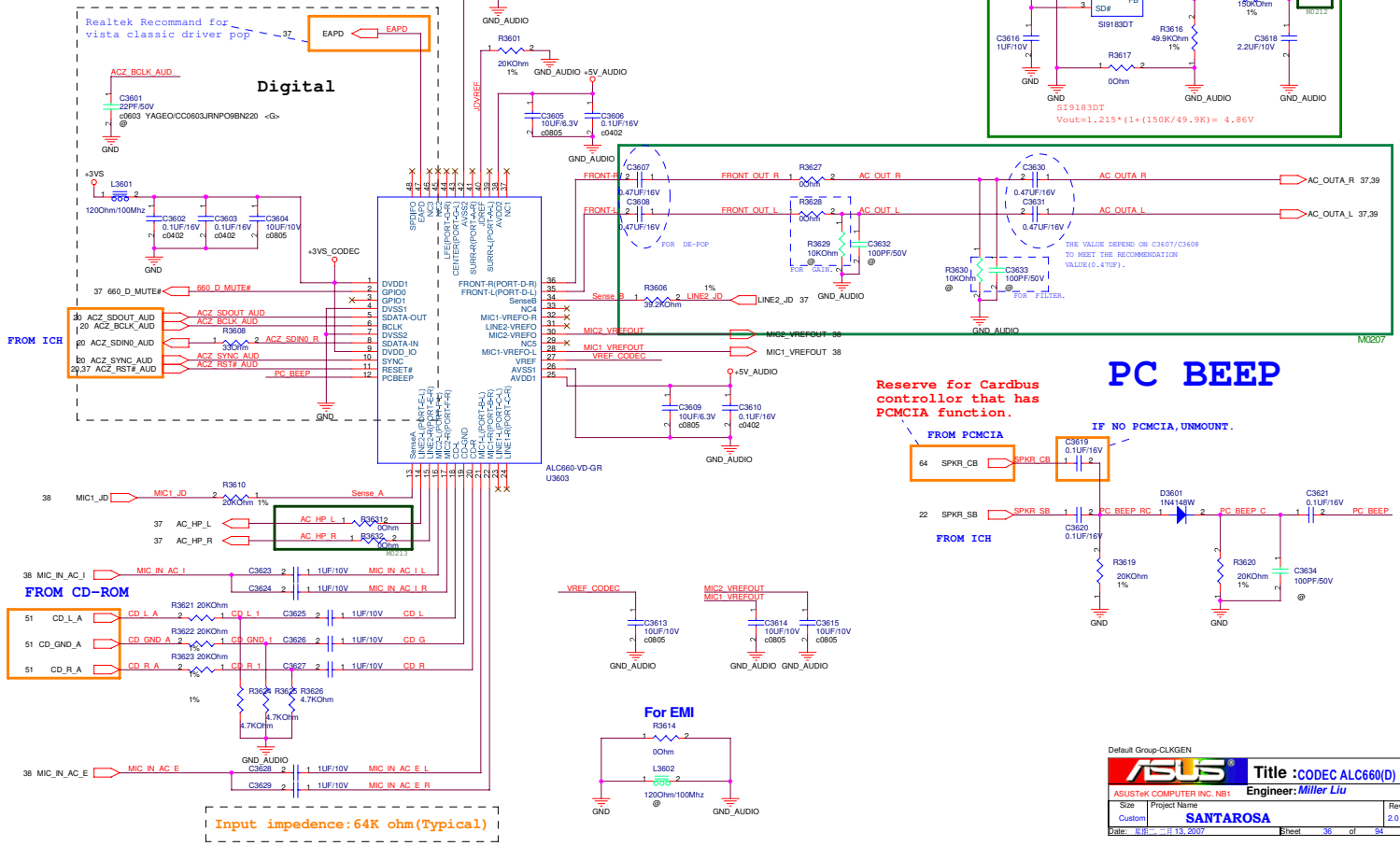




Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : MDC	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 35 of 94	

CODEC ALC660 REV:D



AUDIO POWER

PC BEEP

Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1

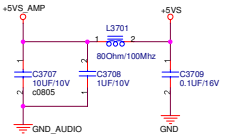
Title : CODEC ALC660(D)

Engineer: Miller Liu

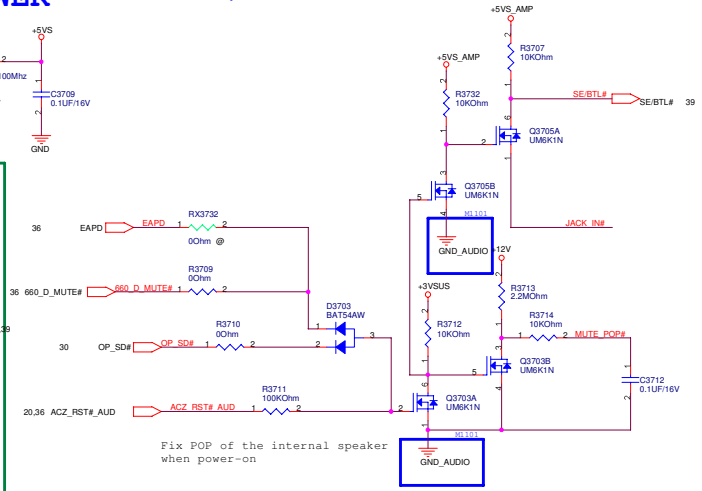
Size	Project Name	Rev
Custom	SANTAROSA	2.0

Date: 星期一, 二月 13, 2007 Sheet 36 of 94

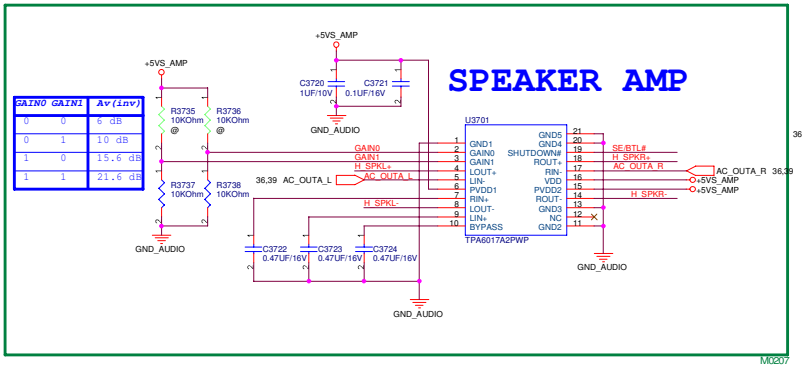
AMP POWER



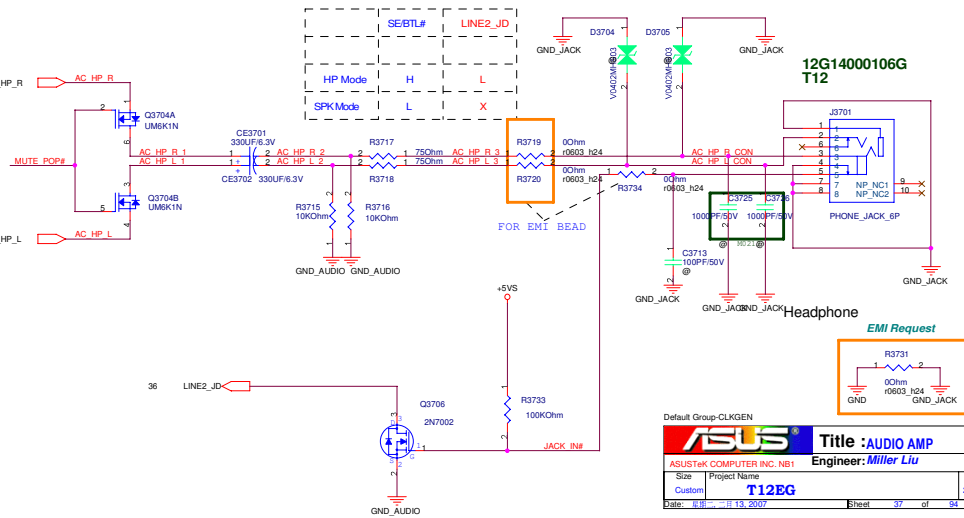
SE/BTL & MUTE CONTROL



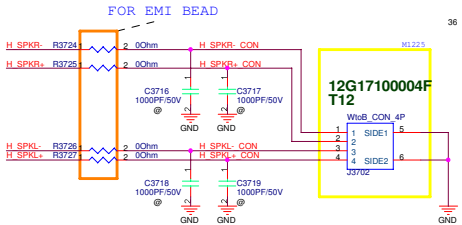
SPEAKER AMP



HP CONN



SPEAKER CONNECTOR



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1

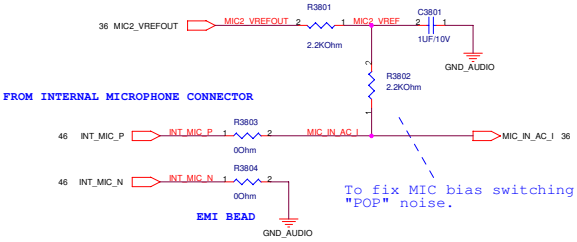
Title : AUDIO AMP

Engineer: Miller Liu

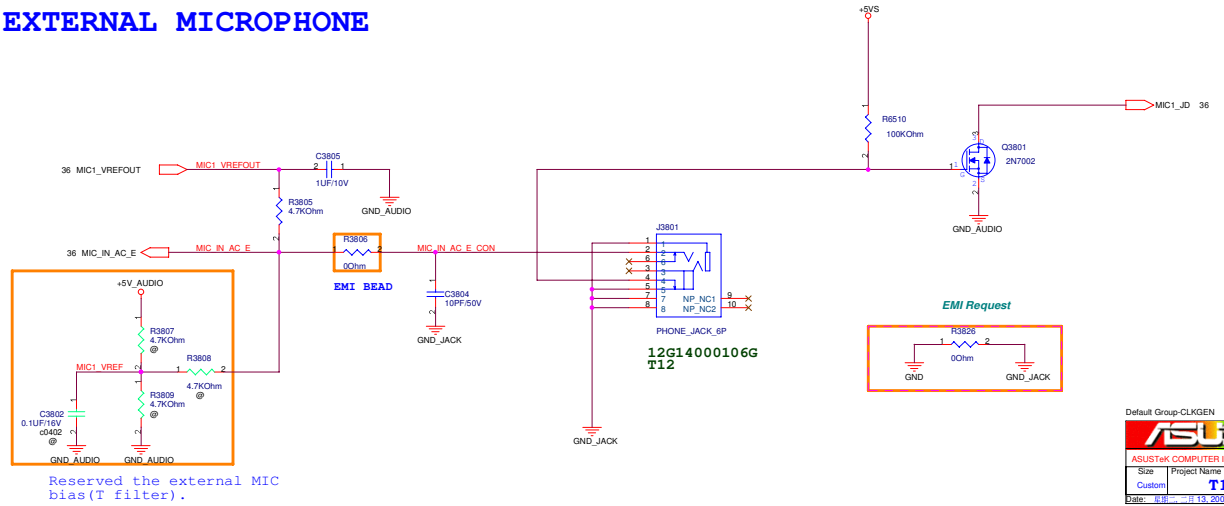
Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期一, 二月 13, 2007 Sheet 37 of 94

INTERNAL MICROPHONE



EXTERNAL MICROPHONE



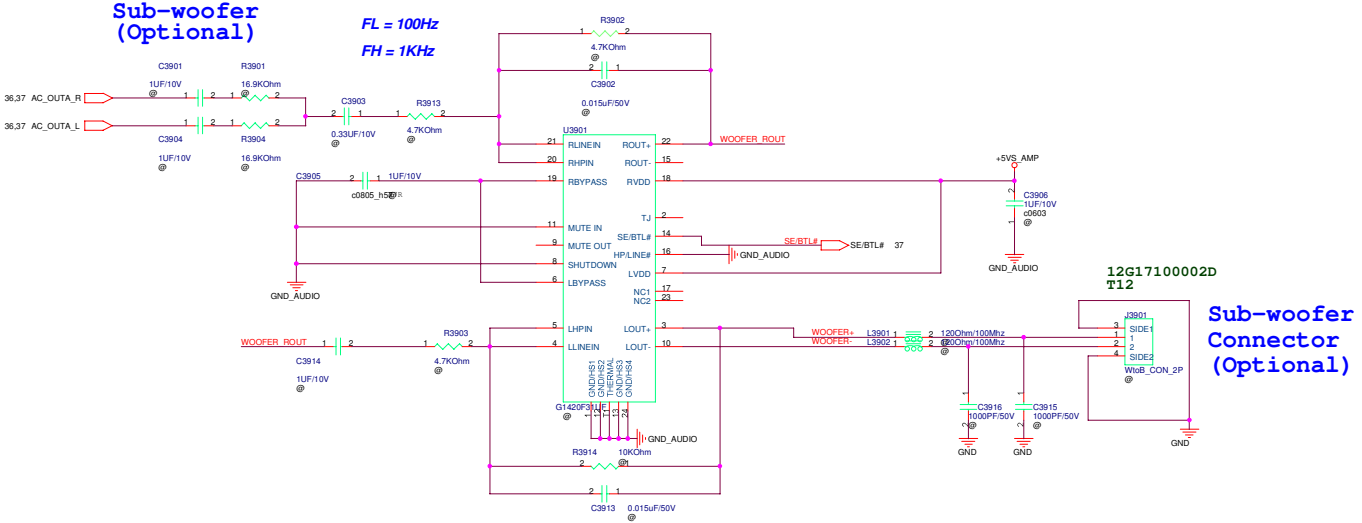
Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1	Title : MIC	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 38 of 94	

Sub-woofer (Optional)

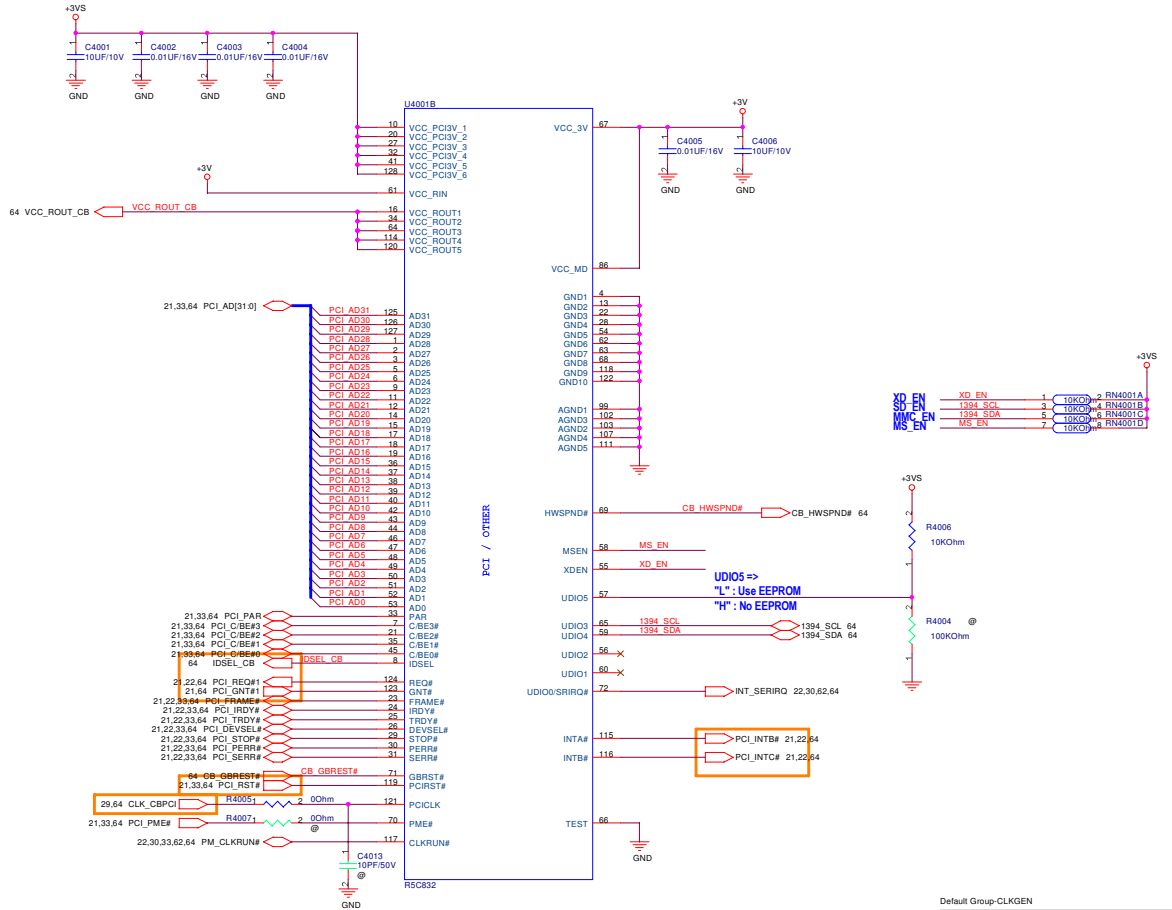
FL = 100Hz

FH = 1KHz



Default Group-CLKGEN

ASUSTek COMPUTER INC NPI		Title : Sub-Woofer	
		Engineer: Miller_Liu	
Size	Project Name	T12EG	Rev
Custom	P/N	<OrgAddr2>	2.0
Date: 星期一, 二月 13, 2007		Sheet 39 of 94	



Default Group-CLKGEN

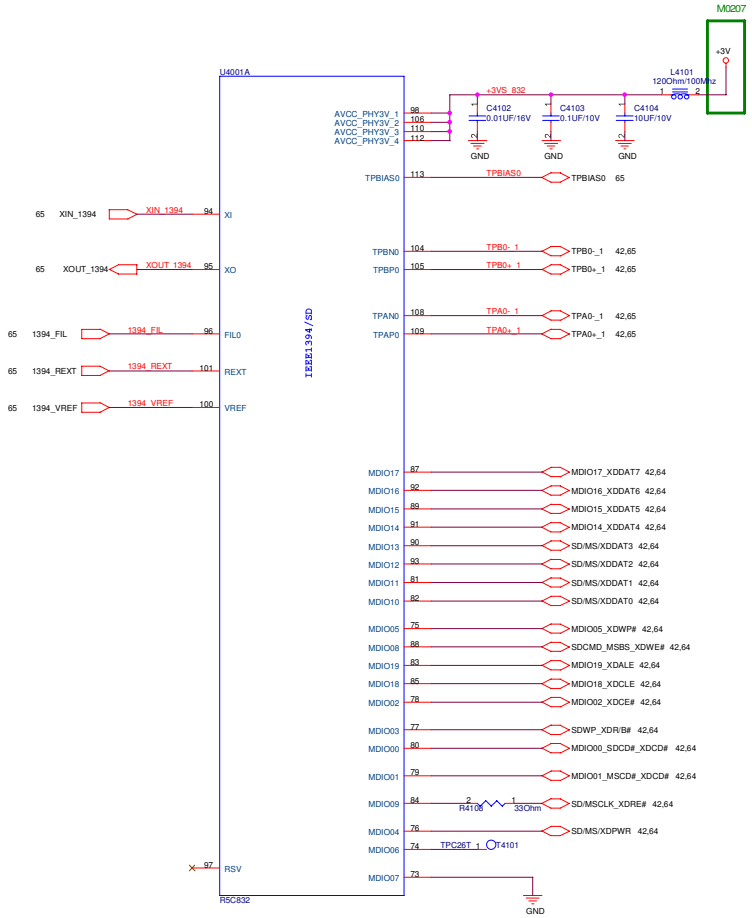
ASUSTeK COMPUTER INC

Title: CARDBUS R5C832 (1)

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期六, 月 16, 2007 Sheet 40 of 94

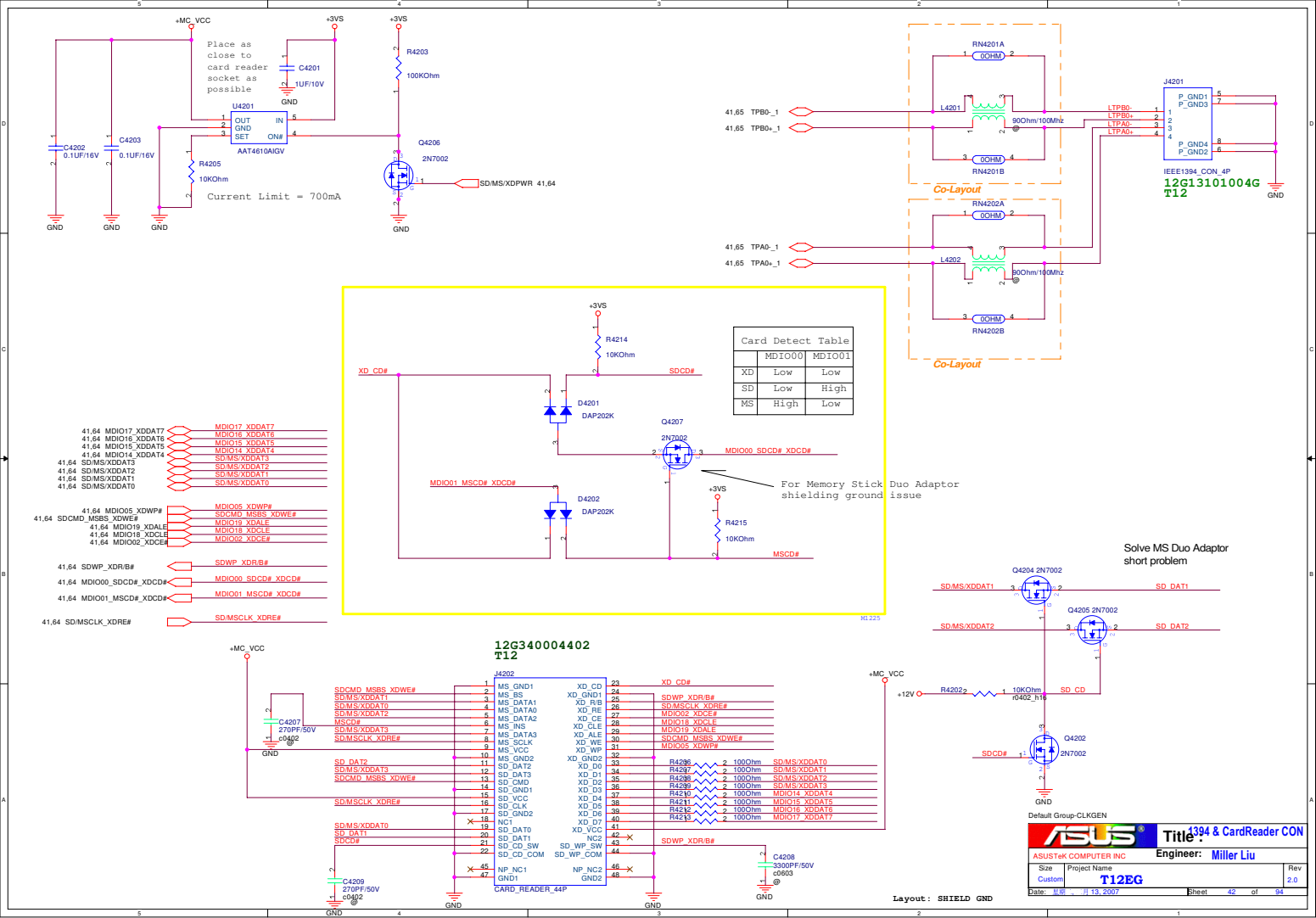


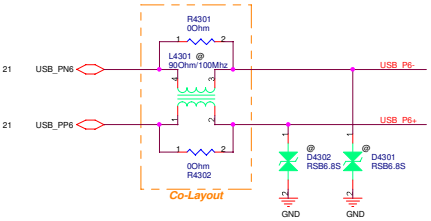

```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

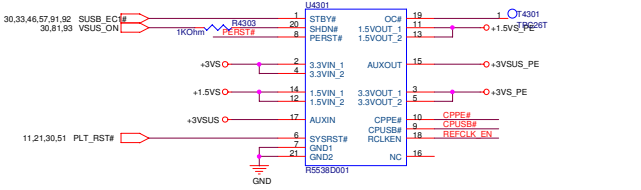
```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

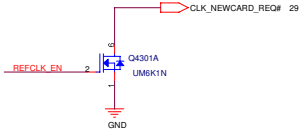
Default Group-CLKGEN

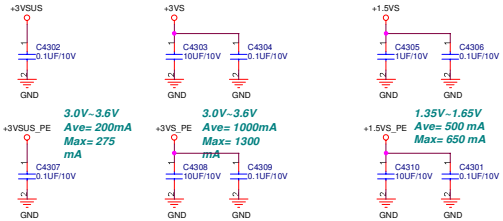
ASUSTeK COMPUTER INC	Title : CARDBUS R5C832 (2)	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 41 of 94	


+MC_VCC
+3VS
Place as close to card reader socket as possible
C4201
1UF/10V
GND
R4203
100KOhm
U4201
OUT
GND
SET
IN
ON#
AAT4610AIGV
C4202
0.1UF/16V
C4203
0.1UF/16V
R4205
10KOhm
Current Limit = 700mA
Q4206
2N7002
SD/MS/XDPWR 41,64
RN4201A
0OHM
L4201
90Ohm/100Mhz
RN4201B
Co-Layout
RN4202A
L4202
RN4202B
41,65 TPB0-_1
41,65 TPB0+_1
41,65 TPA0-_1
41,65 TPA0+_1
LTPB0-
LTPB0+
LTPA0-
LTPA0+
J4201
P_GND1
P_GND3
P_GND4
P_GND2
IEEE1394_CON_4P
12G13101004G
T12
R4214
10KOhm
XD_CD#
SDCD#
D4201
DAP202K
Q4207
2N7002
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D4202
R4215
MSCD#
For Memory Stick Duo Adaptor shielding ground issue
Card Detect Table
MDIO00
MDIO01
XD
Low
SD
MS
High
41,64 MDIO17_XDDAT7
41,64 MDIO16_XDDAT6
41,64 MDIO15_XDDAT5
41,64 MDIO14_XDDAT4
41,64 SD/MS/XDDAT3
41,64 SD/MS/XDDAT2
41,64 SD/MS/XDDAT1
41,64 SD/MS/XDDAT0
41,64 MDIO05_XDWP#
41,64 SDCMD_MSBS_XDWE#
41,64 MDIO19_XDALE
41,64 MDIO18_XDCLE
41,64 MDIO02_XDCE#
41,64 SDWP_XDR/B#
41,64 MDIO00_SDCD#_XDCD#
41,64 MDIO01_MSCD#_XDCD#
41,64 SD/MSCLK_XDRE#
Solve MS Duo Adaptor short problem
Q4204 2N7002
Q4205 2N7002
SD/MS/XDDAT1
SD/MS/XDDAT2
SD_DAT1
SD_DAT2
SD_CD
+12V
R4202
10KOhm
r0402_h16
Q4202
2N7002
12G340004402
T12
J4202
MS_GND1
MS_BS
MS_DATA1
MS_DATA0
MS_DATA2
MS_INS
MS_DATA3
MS_SCLK
MS_VCC
SD_GND2
SD_DAT2
SD_DAT3
SD_CMD
SD_GND1
SD_VCC
SD_CLK
SD_GND2
NC1
SD_DAT0
SD_DAT1
SD_CD_SW
SD_CD_COM
NP_NC1
GND1
XD_CD
XD_GND1
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_GND2
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
XD_VCC
NC2
SD_WP_SW
SD_WP_COM
NP_NC2
GND2
CARD_READER_44P
SDCMD_MSBS_XDWE#
SD/MS/XDDAT1
SD/MS/XDDAT0
SD/MS/XDDAT2
MSCD#
SD/MS/XDDAT3
SD/MSCLK_XDRE#
SD_DAT2
SD/MS/XDDAT3
SDCMD_MSBS_XDWE#
SD/MSCLK_XDRE#
SD/MS/XDDAT0
SD_DAT1
SDCD#
SDWP_XDR/B#
C4207
270PF/50V
c0402
C4209
C4208
3300PF/50V
c0603
R4206
R4207
R4208
R4209
R4210
R4211
R4212
R4213
100Ohm
SD/MS/XDDAT0
SD/MS/XDDAT1
SD/MS/XDDAT2
SD/MS/XDDAT3
MDIO14_XDDAT4
MDIO15_XDDAT5
MDIO16_XDDAT6
MDIO17_XDDAT7
Default Group-CLKGEN
Layout: SHIELD GND
ASUSTeK COMPUTER INC
Title: 1394 & CardReader CON
Engineer: Miller Liu
Size: Custom
Project Name: T12EG
Rev: 2.0
Date: 月 13, 2007
Sheet 42 of 94



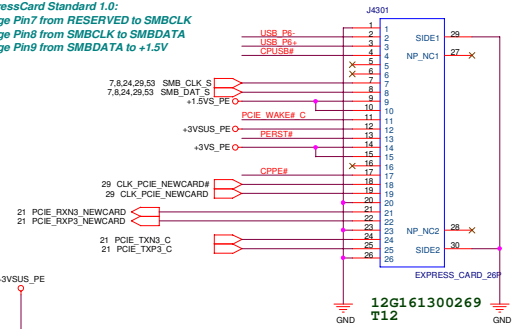


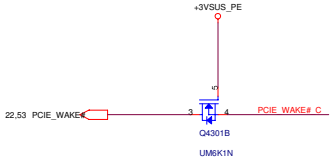


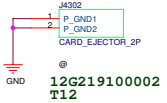


NewCard Header

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

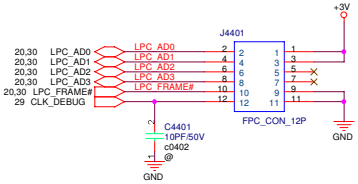






Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12F	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 43 of 94	



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

Title : DEBUG

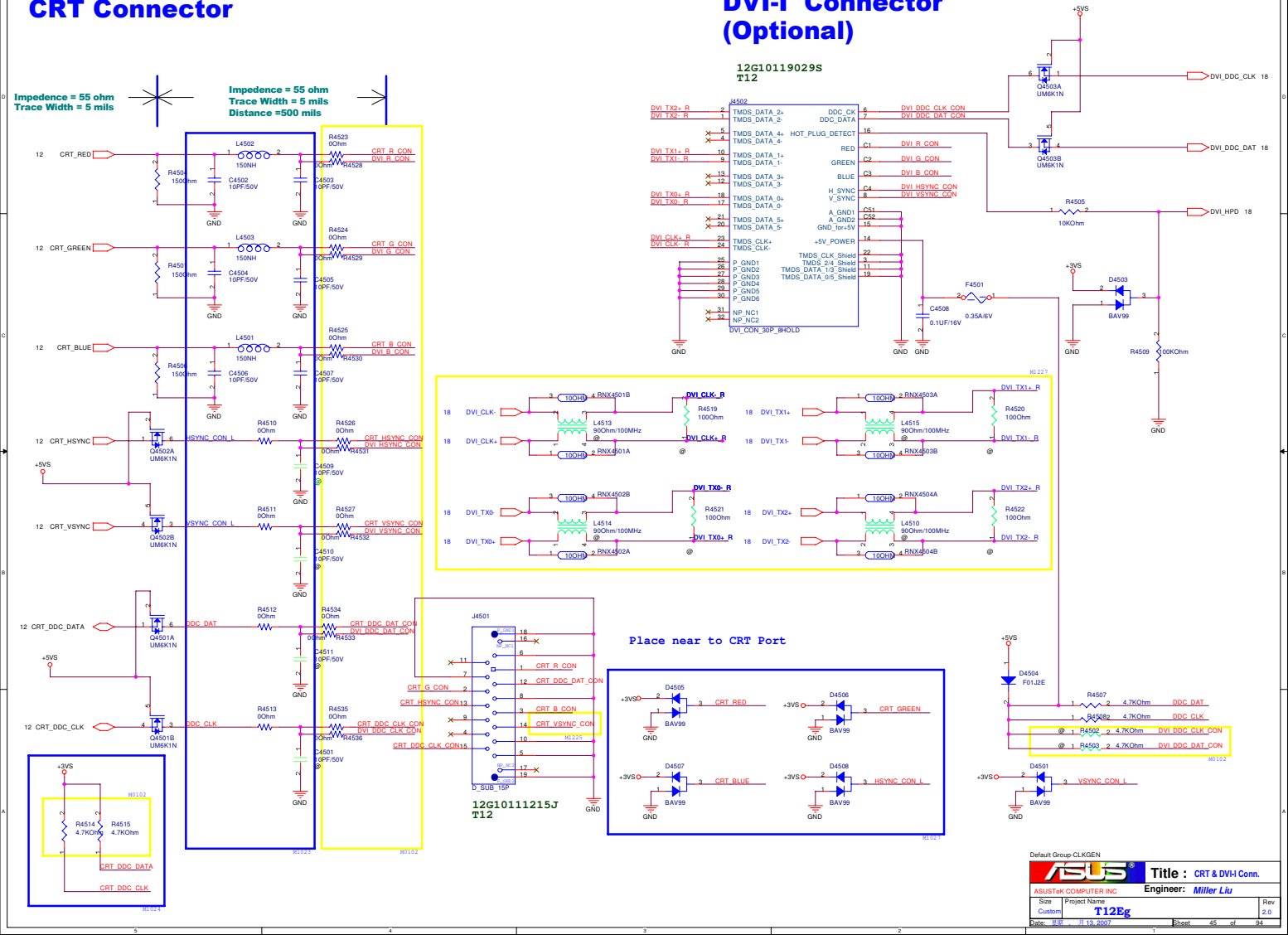
Engineer: *Miller Liu*

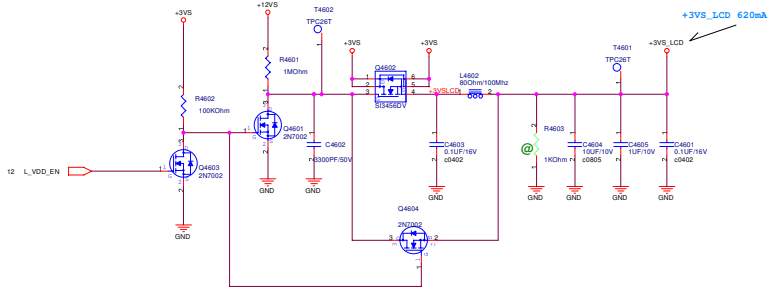
Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 44 of 94

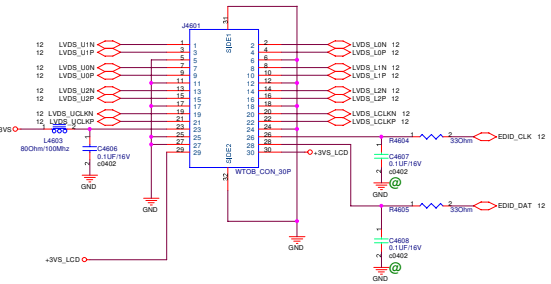
CRT Connector

DVI-I Connector (Optional)



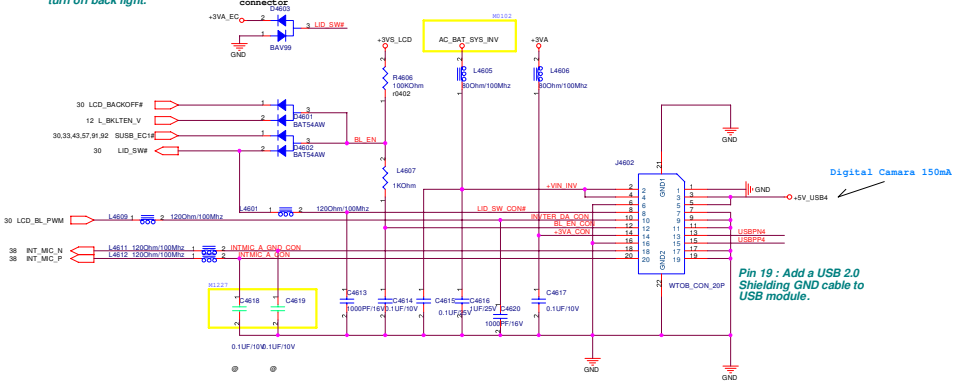


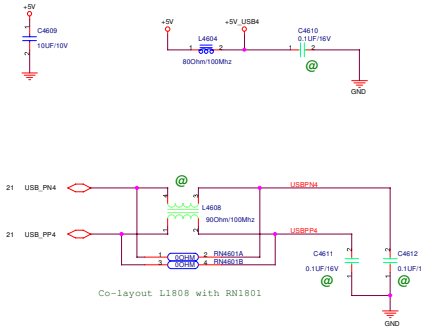
Pin define is the same as A7



LCD LVDS Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.





Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : LVDS & Inverter Conn.

Engineer: Miller Liu

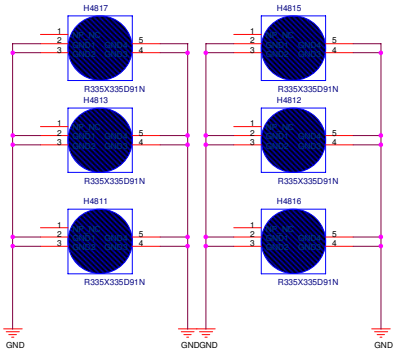
Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 十月 16, 2007 Sheet 46 of 94

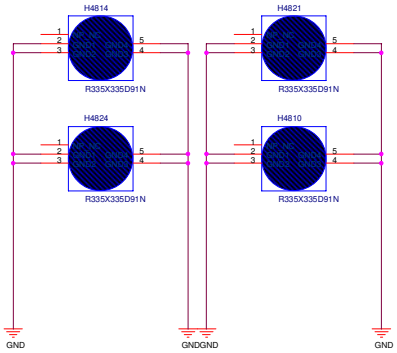
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 47 of 94	

A Hole / TOP Side



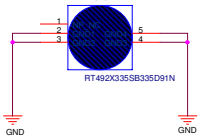
A Hole / Bottom Side



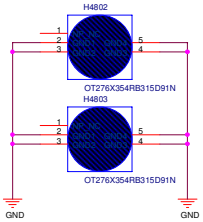
Drill Hole for Fix

圓孔　　橢圓孔　　圓孔New R1.1

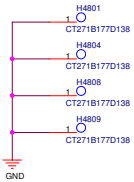
A Hole Special / Bottom Side



E Hole for Main board fix

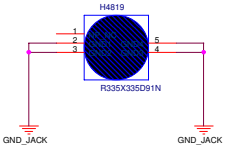


F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1

13GNJ510M170-1
T12



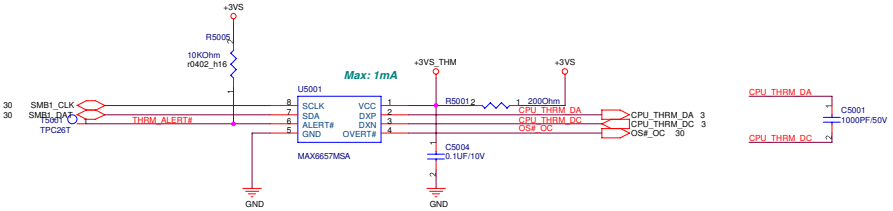
Default Group-CLKGEN

ASUSTek COMPUTER INC NPI	Title : SREW HOLE		
	Engineer: Miller Liu		
Size: Custom	Project Name: T12EG		Rev: 2.0
	P/N: <OrgAddr2>		
Date: 星期二, 二月 13, 2007	Sheet 48 of 94		

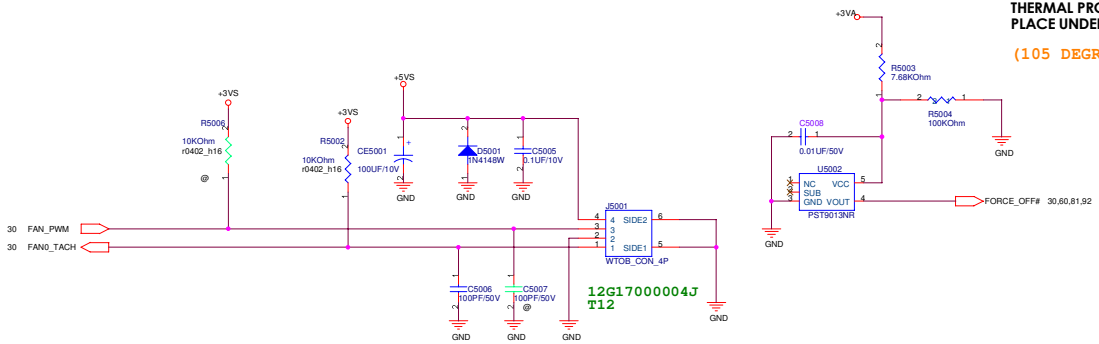
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 49 of 94	

Thermal Sensor



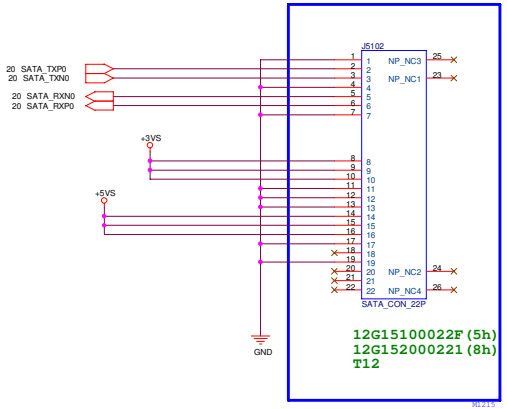
DC FAN Control

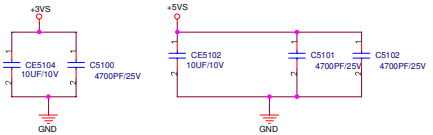


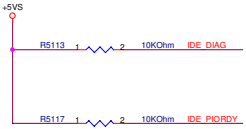
Default Group-CLKGEN

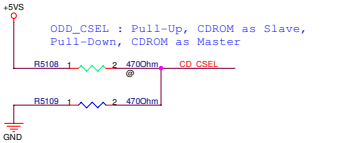
ASUSTeK COMPUTER INC. NB	Title : FAN	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 50 of 94	

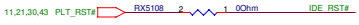
SATA HDD

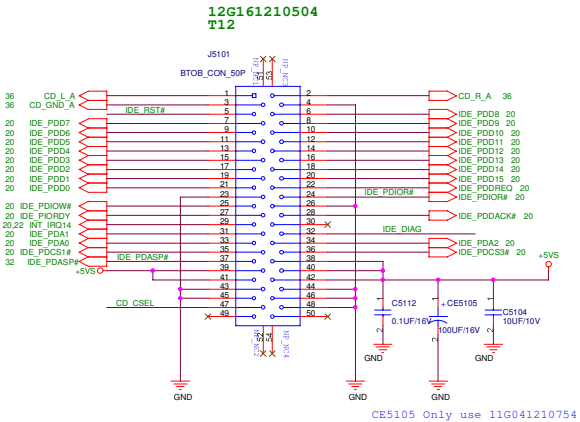








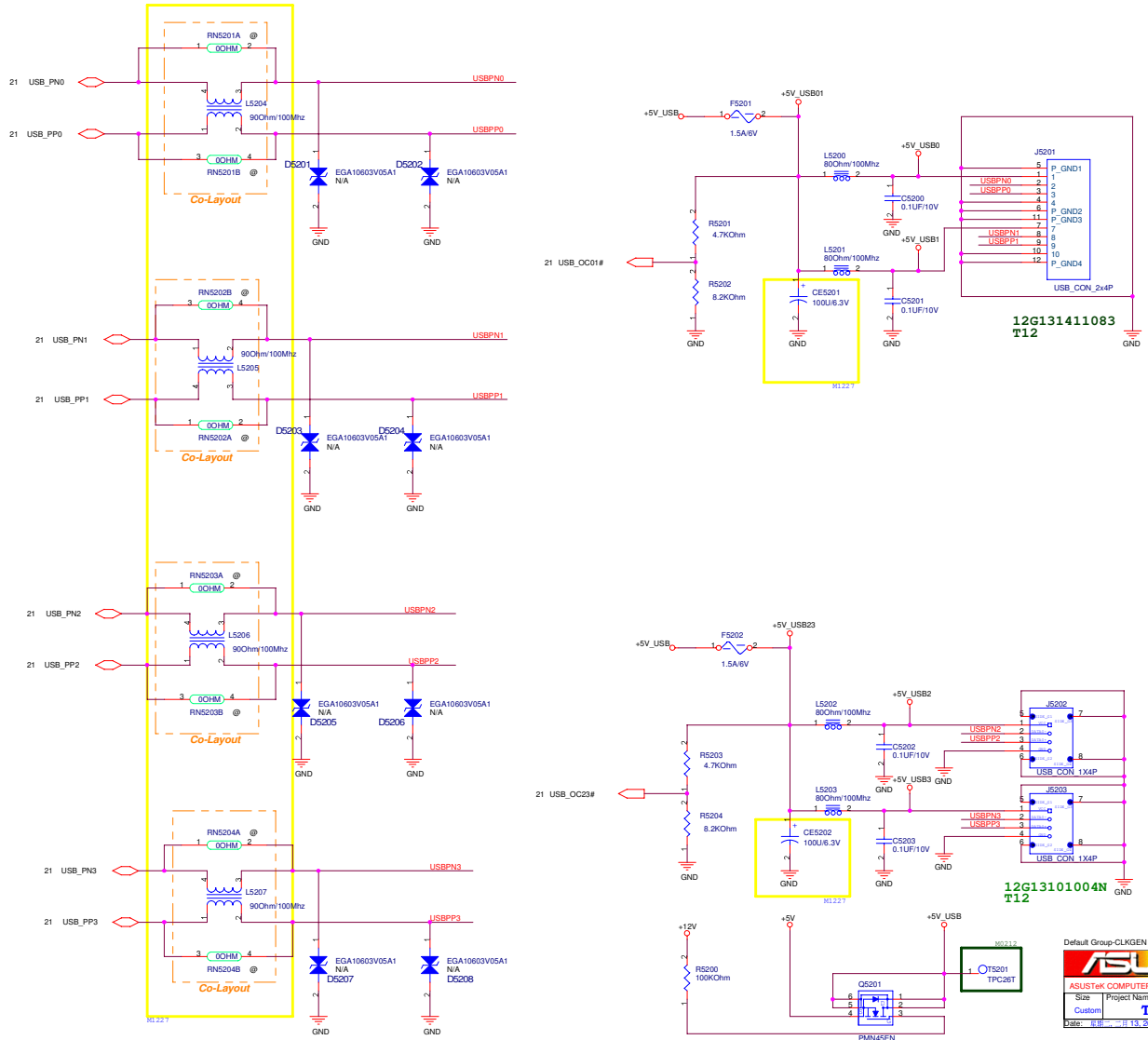




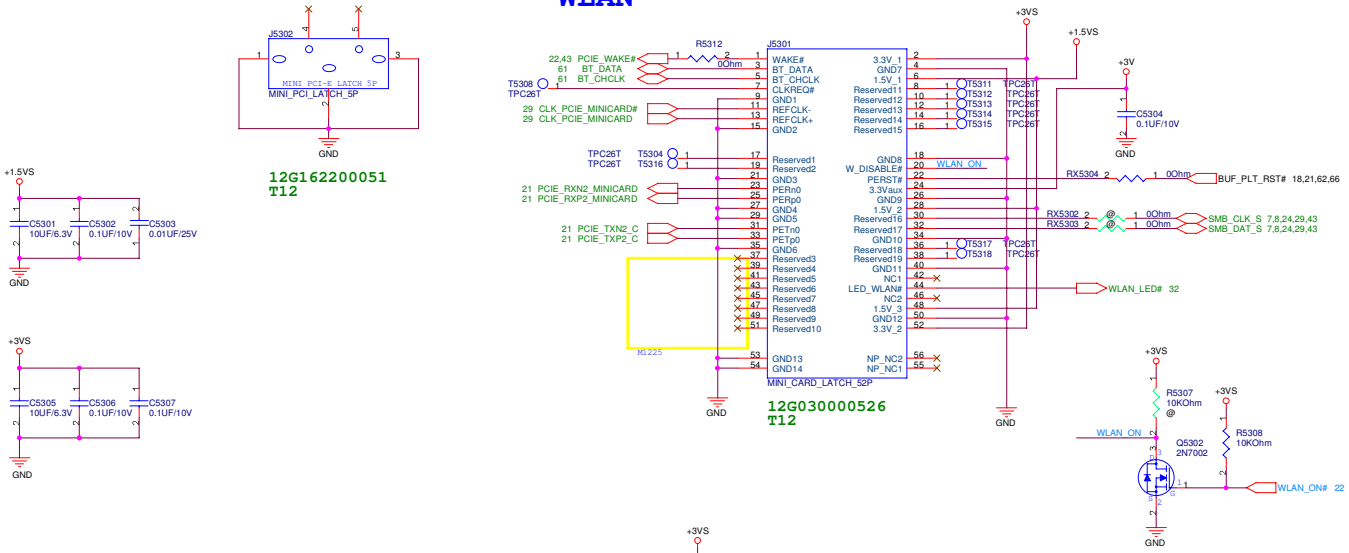
CE5105 Only use 11G041210754

Default Group-CLKGEN

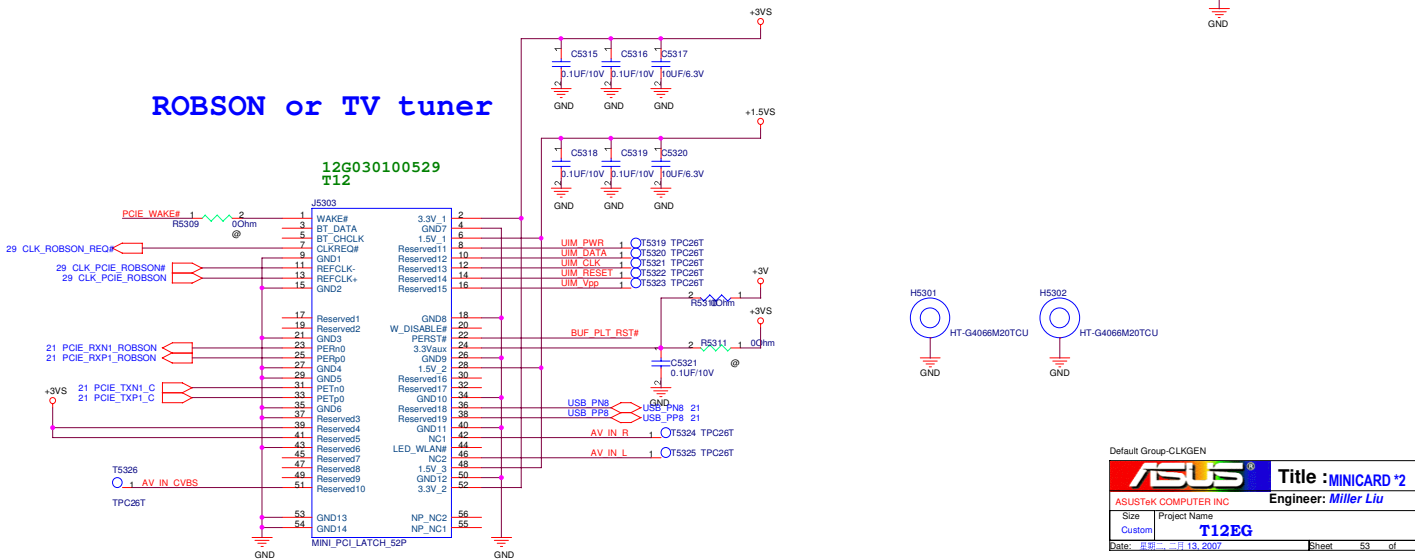
ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 51 of 94	


RN5201A @
0OHM
21 USB_PN0
L5204
90Ohm/100Mhz
21 USB_PP0
0OHM
RN5201B @
Co-Layout
USBPN0
USBPP0
D5201
EGA10603V05A1
N/A
D5202
EGA10603V05A1
N/A
GND
RN5202B @
0OHM
21 USB_PN1
90Ohm/100Mhz
L5205
21 USB_PP1
0OHM
RN5202A @
Co-Layout
USBPN1
USBPP1
D5203
EGA10603V05A1
N/A
D5204
EGA10603V05A1
N/A
GND
RN5203A @
0OHM
21 USB_PN2
L5206
90Ohm/100Mhz
21 USB_PP2
0OHM
RN5203B @
Co-Layout
USBPN2
USBPP2
D5205
EGA10603V05A1
N/A
D5206
EGA10603V05A1
N/A
GND
RN5204A @
0OHM
21 USB_PN3
L5207
90Ohm/100Mhz
21 USB_PP3
0OHM
RN5204B @
Co-Layout
USBPN3
USBPP3
D5207
EGA10603V05A1
N/A
D5208
EGA10603V05A1
N/A
GND
M1227
+5V_USB
F5201
1.5A/6V
+5V_USB01
L5200
80Ohm/100Mhz
+5V_USB0
C5200
0.1UF/10V
R5201
4.7KOhm
21 USB_OC01#
R5202
8.2KOhm
L5201
80Ohm/100Mhz
+5V_USB1
CE5201
100U/6.3V
C5201
0.1UF/10V
J5201
P_GND1
P_GND2
P_GND3
P_GND4
USBPN0
USBPP0
USBPN1
USBPP1
USB_CON_2x4P
12G131411083
T12
M1227
+5V_USB
F5202
1.5A/6V
+5V_USB23
L5202
80Ohm/100Mhz
+5V_USB2
C5202
0.1UF/10V
R5203
4.7KOhm
21 USB_OC23#
R5204
8.2KOhm
L5203
80Ohm/100Mhz
+5V_USB3
CE5202
100U/6.3V
C5203
0.1UF/10V
J5202
J5203
USBPN2
USBPP2
USBPN3
USBPP3
USB_CON_1X4P
12G13101004N
T12
M1227
+12V
+5V
+5V_USB
R5200
100KOhm
Q5201
PMN45EN
M2212
T5201
TPC26T
Default Group-CLKGEN
Title : USB CONN X 4
ASUSTeK COMPUTER INC. NB
Engineer: Miller Liu
Size
Custom
Project Name
T12EG
Rev
2.0
Date: 星期一, 二月 13, 2007
Sheet 52 of 94

WLAN



ROBSON or TV tuner



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : MINICARD *2

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 53 of 94

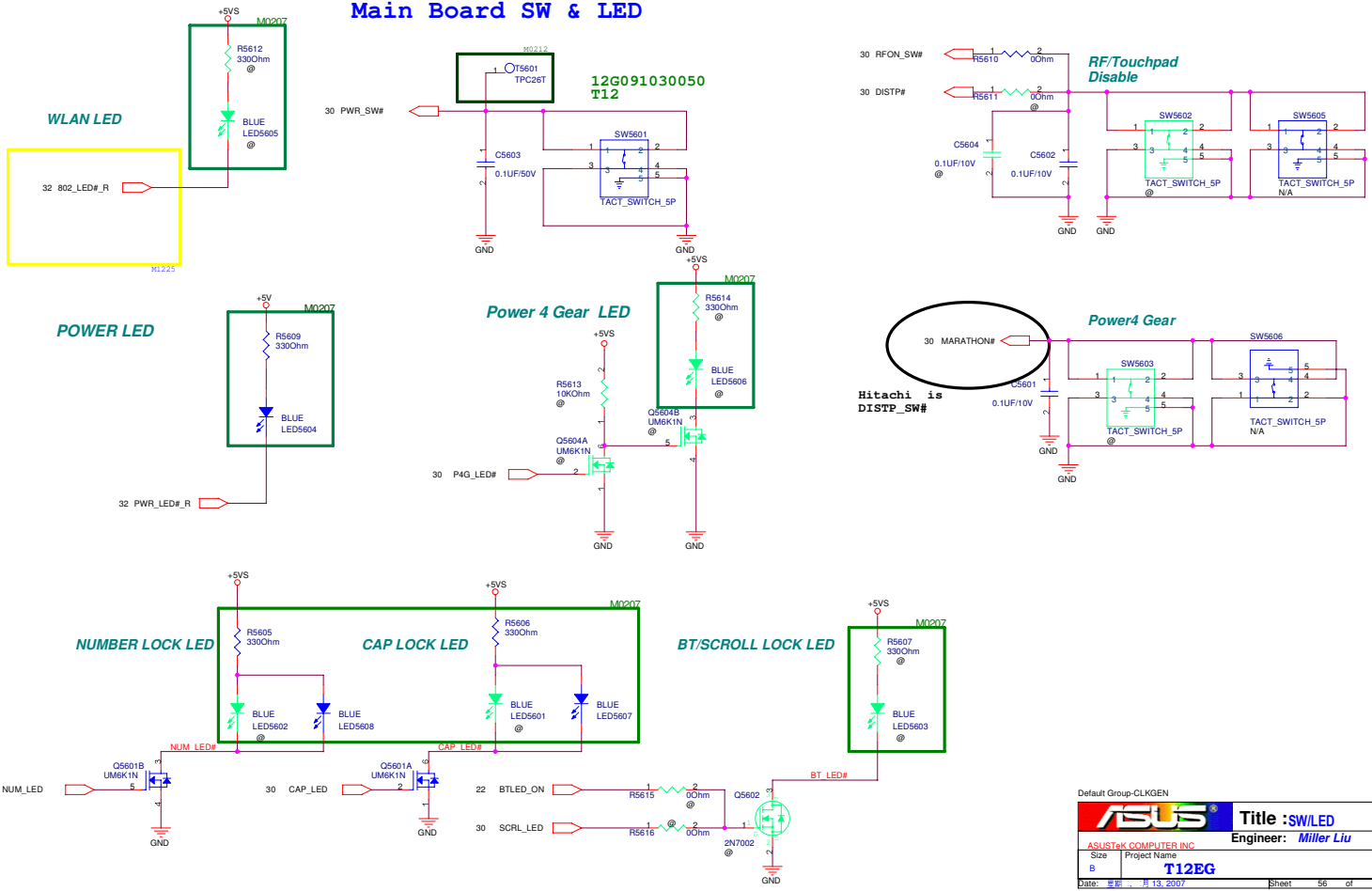
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 54 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 55 of 94	

Main Board SW & LED



Default Group-CLKGEN

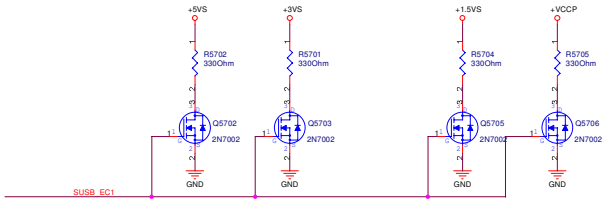
ASUSTeK COMPUTER INC

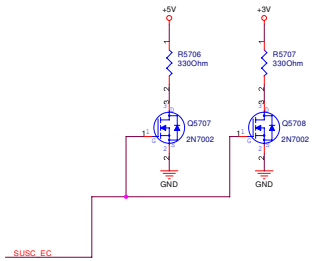
Title : SW/LED

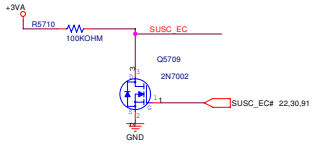
Engineer: Miller Liu

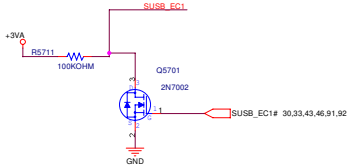
Size	Project Name	Rev
B	T12EG	2.0

Date: 星期 , 月 13, 2007 Sheet 56 of 94









Default Group-CLKGEN

Title :DISCHARGE

ASUSTeK COMPUTER INC. NB

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: M 07 , 11 13, 2007 Sheet 57 of 94

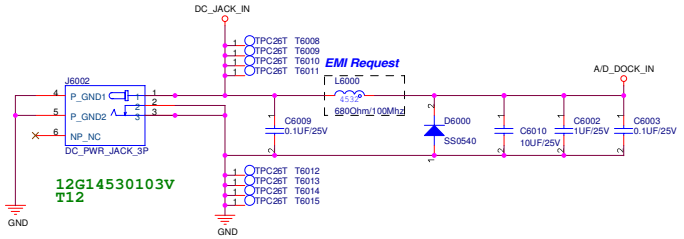
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 58 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 59 of 94	

DC-IN



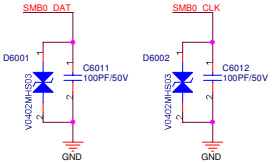
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# don't connect to Battery Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# must connect to Battery Connector.

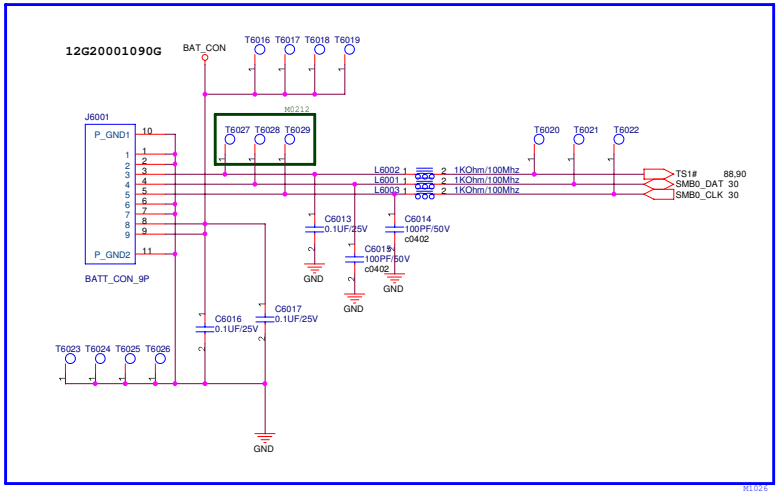


Note:

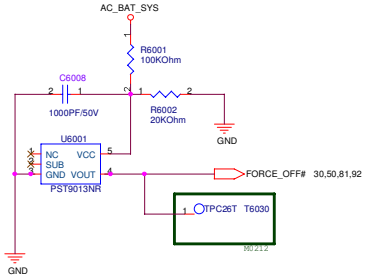
When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

Battery Connector



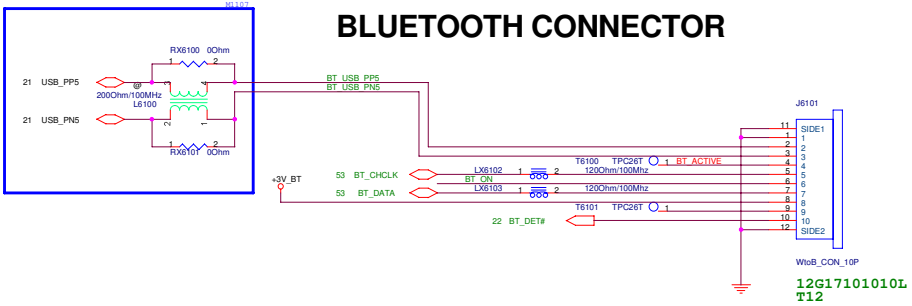
Without Battery & Pull out Adapter

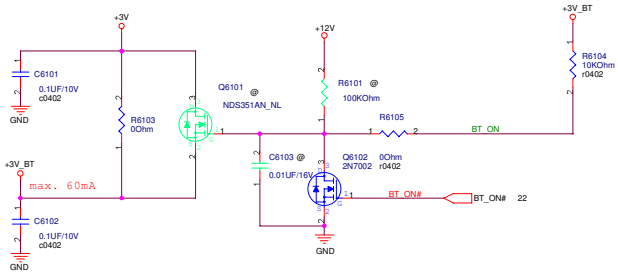


Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : DCIN/Batt conn.	
	Engineer: *Miller Liu*	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 二月 13, 2007	Sheet 60 of 94	

BLUETOOTH CONNECTOR

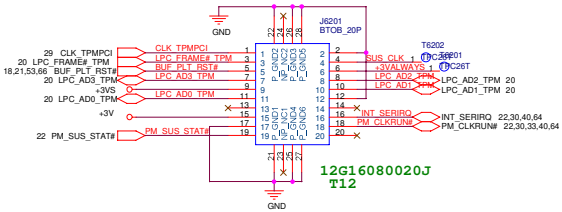


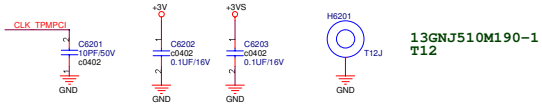


Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 61 of 94	

TPM Connector





Default Group-CLKGEN

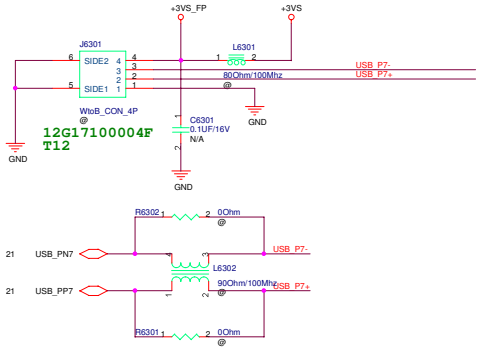
ASUSTeK COMPUTER INC. NB

Title : TPM

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 62 of 94



Default Group-CLKGEN

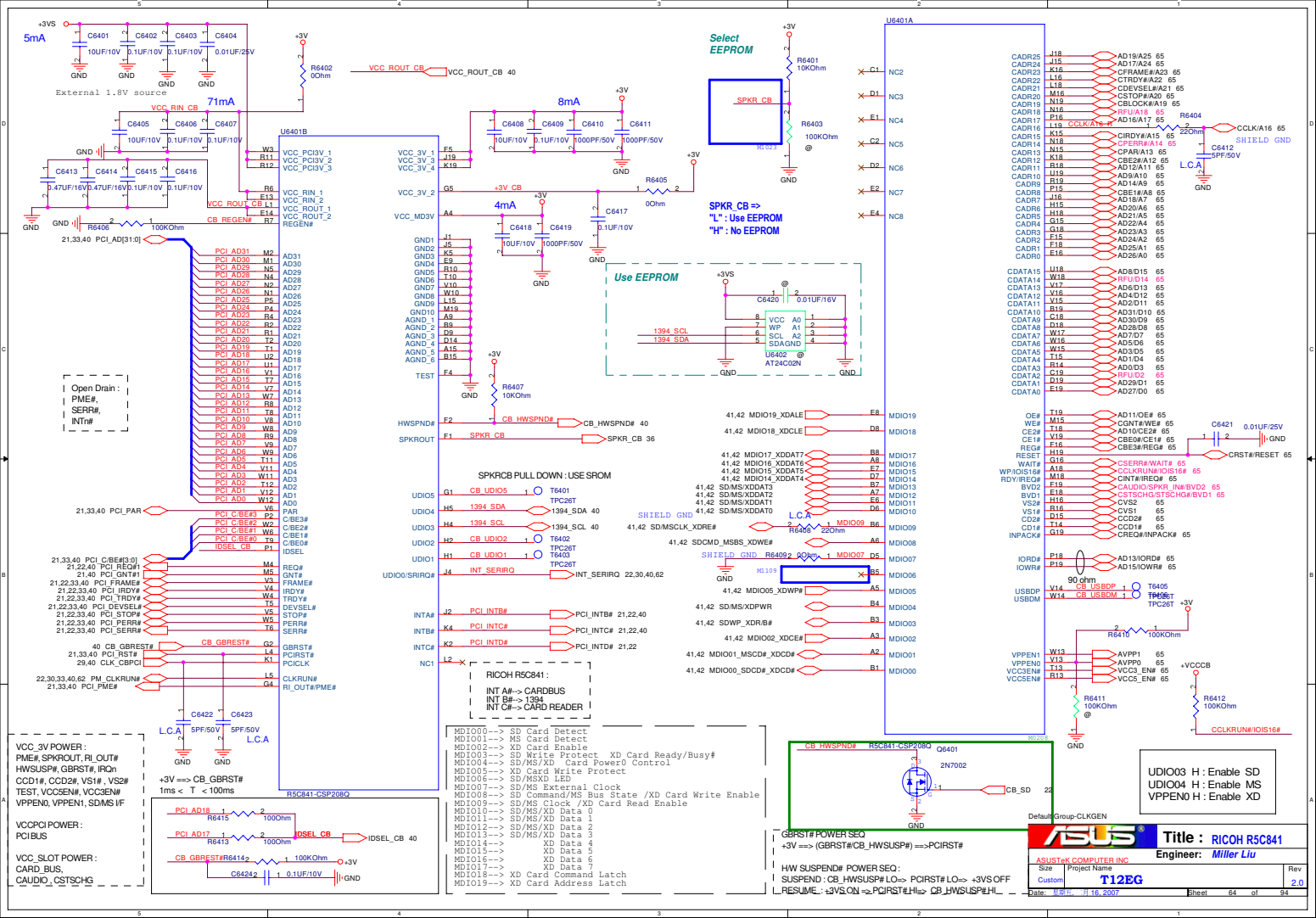
ASUSTeK COMPUTER INC. NB

Title : Finger Print

Engineer: Miller Liu

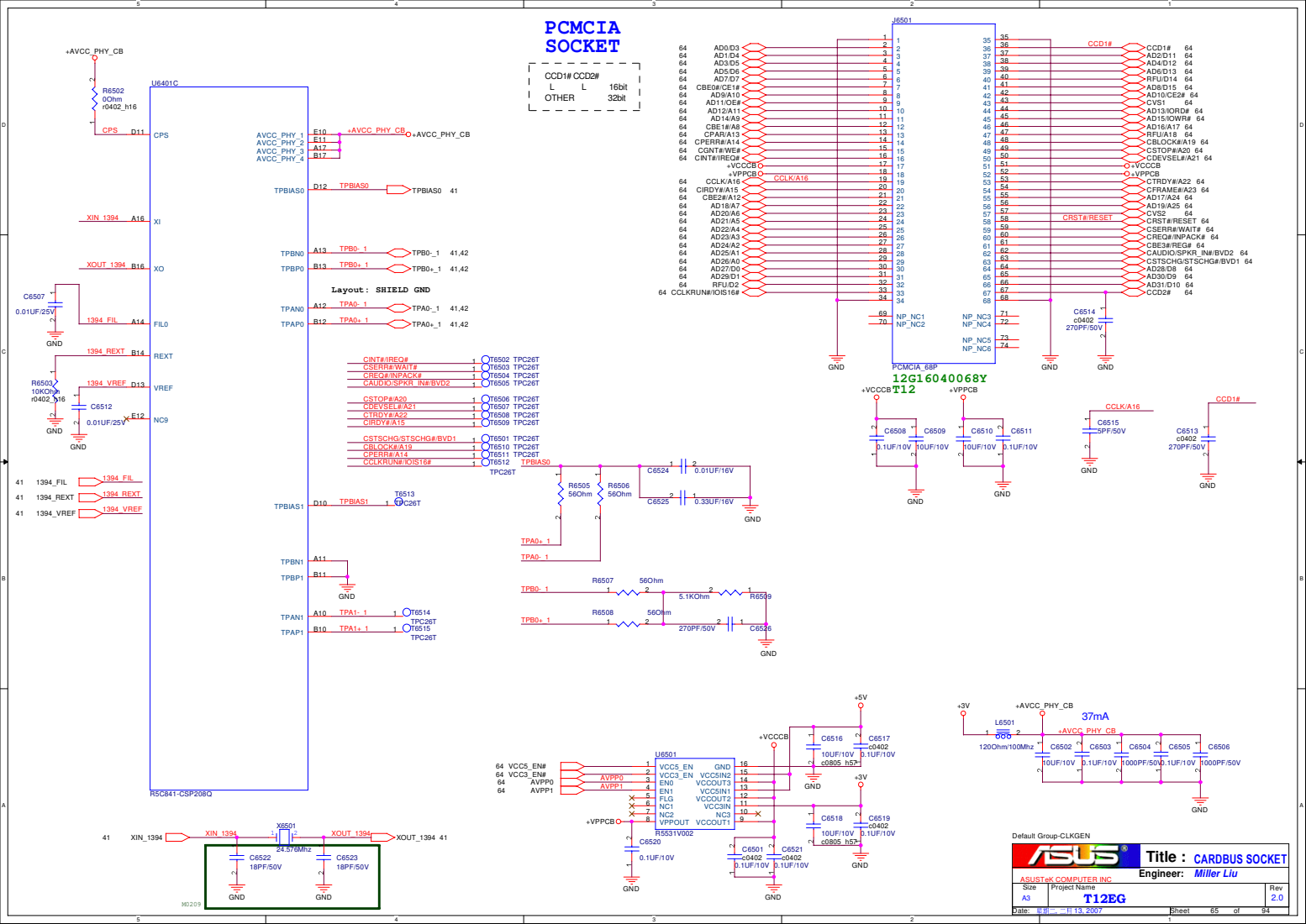
Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期 . 月 13, 2007 Sheet 63 of 94


5mA
71mA
8mA
4mA
External 1.8V source
Select EEPROM
Use EEPROM
SPKR_CB =>
"L" : Use EEPROM
"H" : No EEPROM
Open Drain : PME#, SERR#, INTN#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
R5C841-CSP208Q
U6401A
U6401B
U6420
U6402
R5C841-CSP208Q
Q6401
2N7002
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP#_LO--> PCIRST#_LO--> +3VS OFF
RESUME : +3VS_ON --> PCIRST#_HI--> CB_HWSUSP#_HI
Default Group-CLKGEN
Title : RICOH R5C841
Engineer: Miller Liu
ASUSTeK COMPUTER INC
Project Name T12EG
Rev 2.0
Date: 五月 16, 2007
Sheet 64 of 94

PCMCIA SOCKET

CCD1#	CCD2#	
L	L	16bit
OTHER		32bit



Default Group-CLKGEN

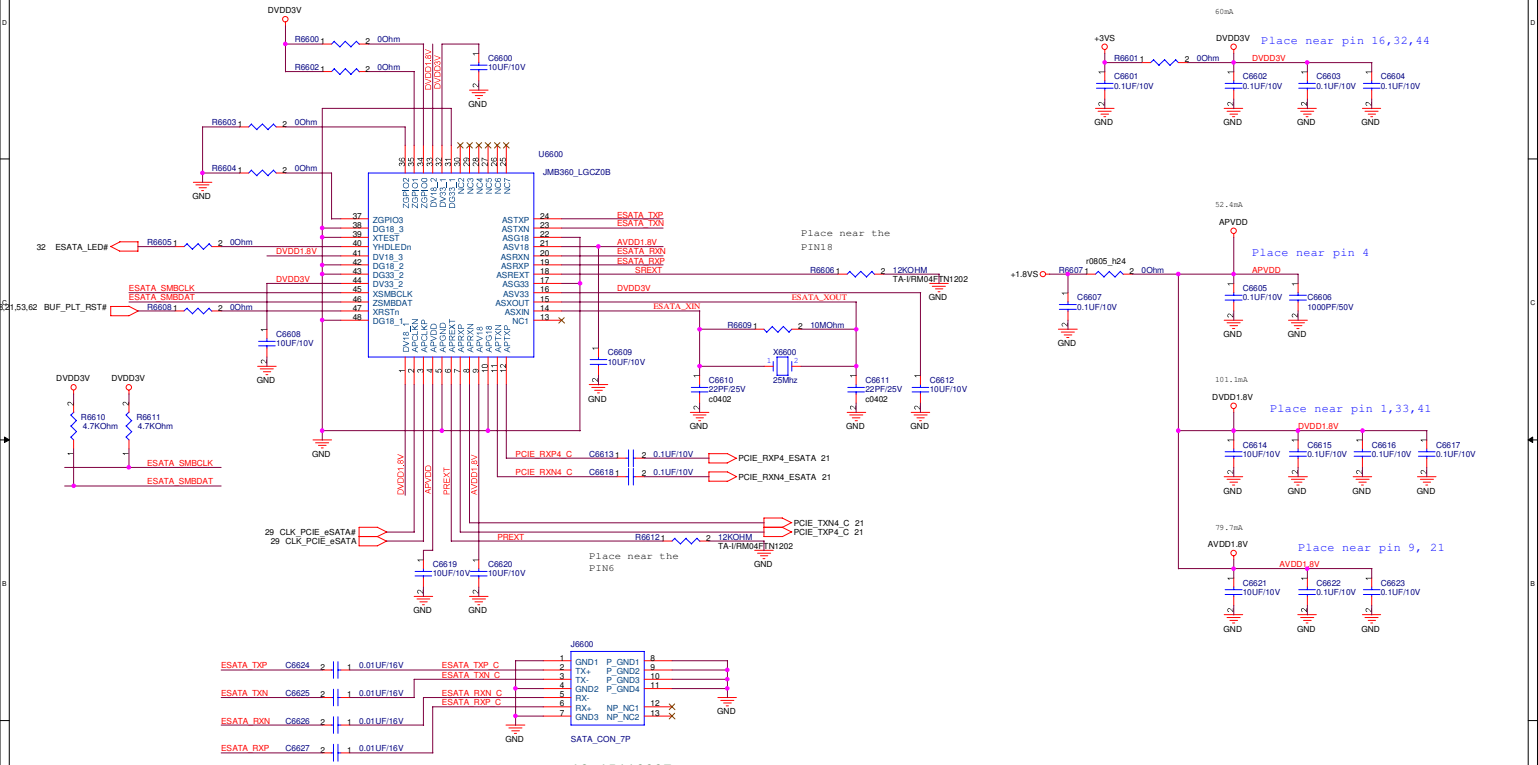
ASUSTeK COMPUTER INC

Title : CARDBUS SOCKET

Engineer: Miller Liu

Size	Project Name	Rev
A3	T12EG	2.0

Date: 星期一, 一月 13, 2007 Sheet 65 of 94



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : eSATA

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期一, 二月 13, 2007 Sheet 66 of 94

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	2	A
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : RESOURCE

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 67 of 94

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 68 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 69 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 70 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 71 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 72 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 73 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 74 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 75 of 94	

Default Group-CLKGEN

Title : Null

ASUSTeK COMPUTER INC

Engineer: *Miller Liu*

Size	Project Name	Rev
Custom	SANTAROSA	2.0

Date: 星期二, 二月 13, 2007 Sheet 76 of 94

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 77 of 94	

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Miller Liu*	
Size: A	Project Name: **T12Eg**	Rev: 2.0
Date: 星期二, 三月 13, 2007	Sheet 78 of 94	

Change Note:

R1.1 :

1. Change CON0801 SM-Bus address to A2.
2. Unmount R2936.(SELLCD_27# =1)
3. RX2227 connect to GND.(Do not use Intel LAN)
4. Add R6415 to connect PCI_AD18(for R5C832).
5. Remove CON5301 Debug Pin.
6. Change CON4501.14 to VSYNC_CON.
7. Change CON3702 pin define(RL SWAP).
8. Change R2914 from 220 ohm to 390 ohm.
9. Mount C2920-22,C2924,C2925,C4618-19,L5204-07, Unmount RN5201-04 for EMI requst.
10. Add R4517,R4517,R4518 to prevent CON4501 short ground issue.
11. Change C0701,C0706,C0801,C0809 to R0701,R0702,R0802,R0803(68.9 ohm).
12. Change RNX4501-04 from 0 to 22ohm, and add R4519-4522(100 ohm).
13. SWAP SUSB_EC1#,SUSB_EC2#.

R2.0 :

1.Change Audio LDO(P36) and Audio AMP(P37).
2.Change CB_SD# to CB_SD (high active) to fix windows progress bar issue(P64).
3.Change LED color from Green to Blue (P56).
4.Change +3VS_832 to connect +3V to fix 1394 S3 issue (P41).
5.Change C6522,C6523 from 20pf to 18pf (ITTI suggestion).(P65).
6.Change C2002,C2005 from 22pf to 12pf (FUJICOM suggestion).(P20).
7.Change C3016,C3017 from 5pf to 15pf (FUJICOM suggestion).(P30).
8.Change R3313 from 2.49K to 2.43K to fix LAN low output peak voltage issue.(P33).

Default Group-CLKGEN

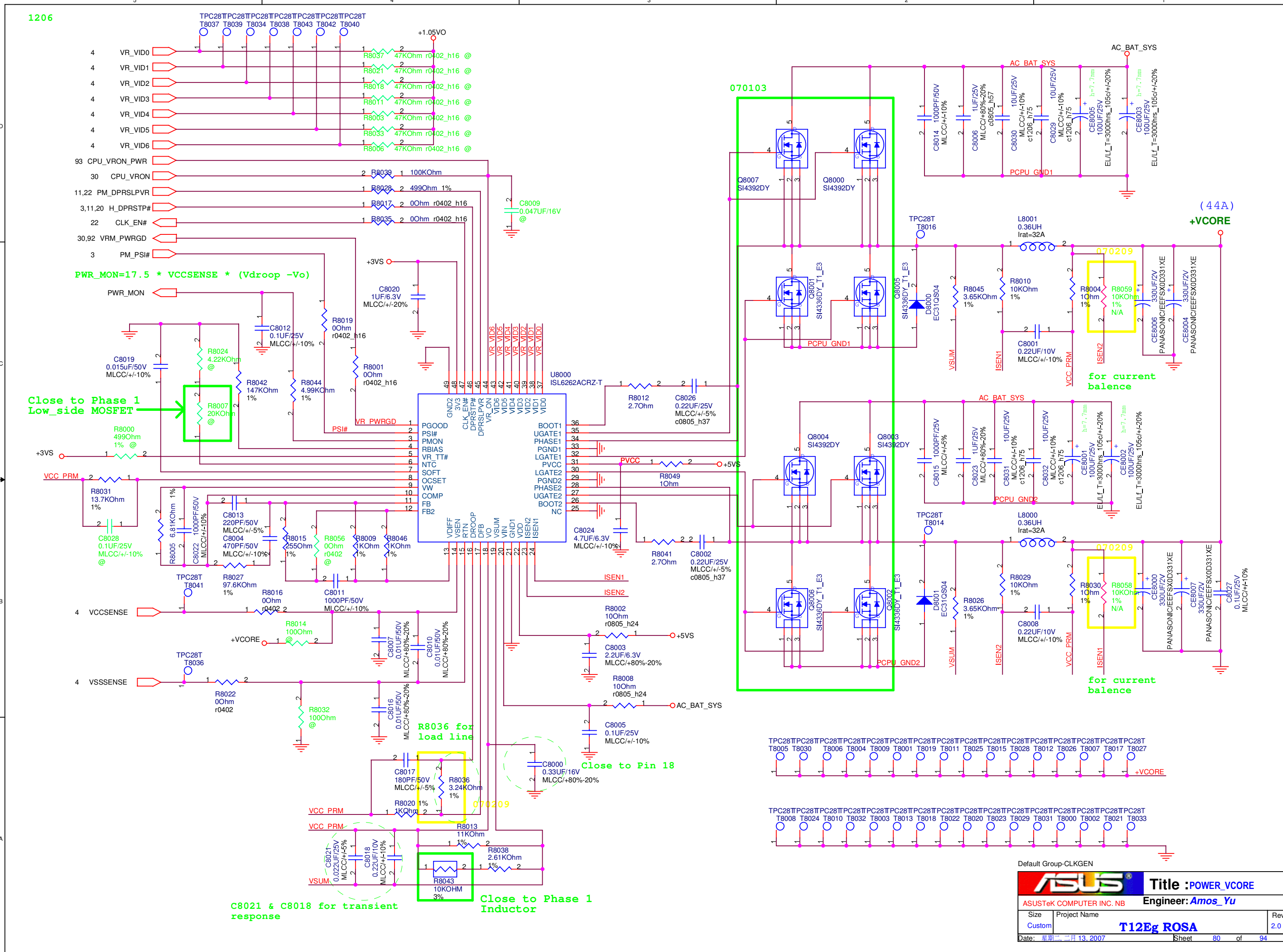
ASUSTeK COMPUTER INC

Title : NULL

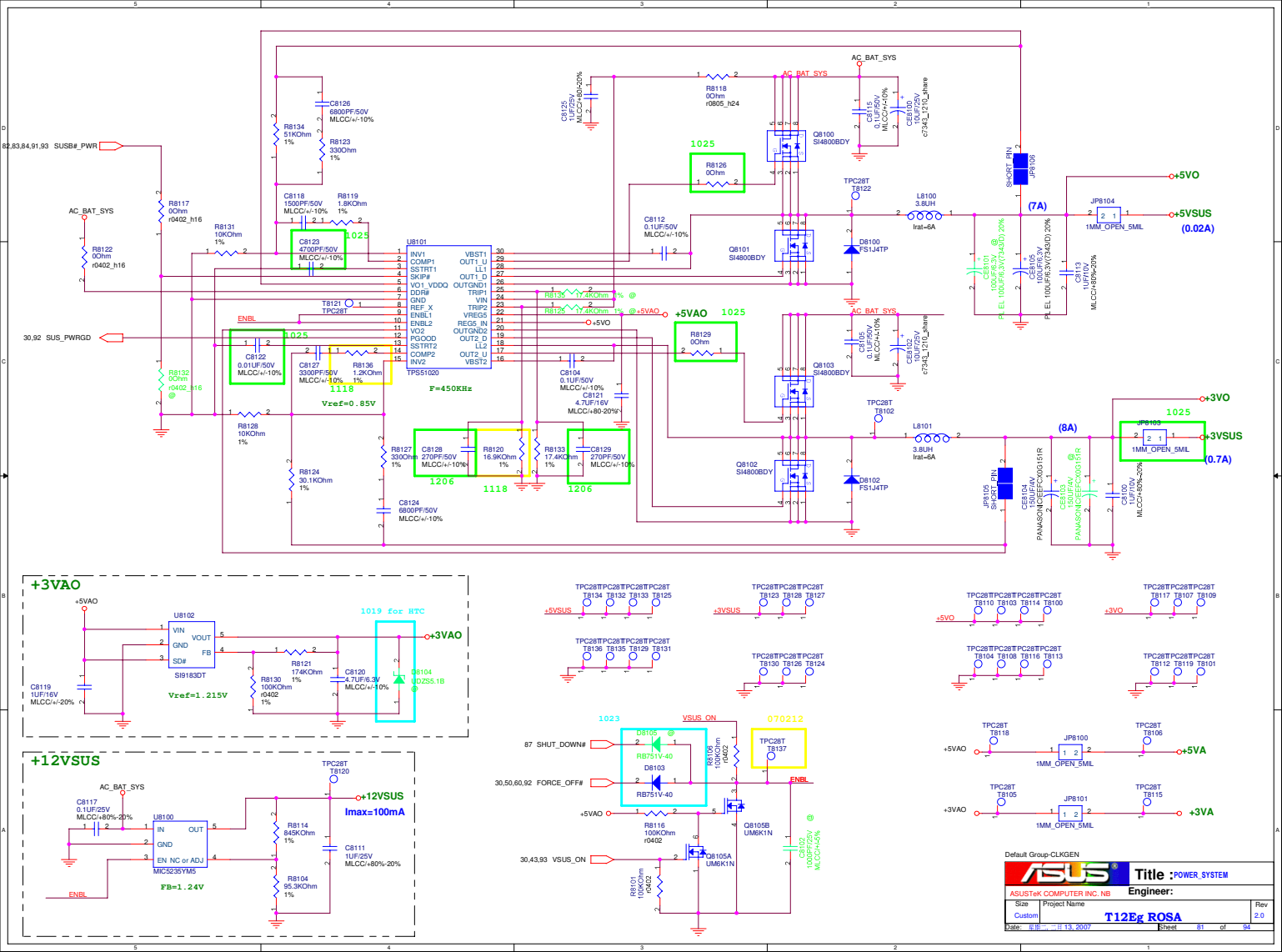
Engineer: Miller Liu

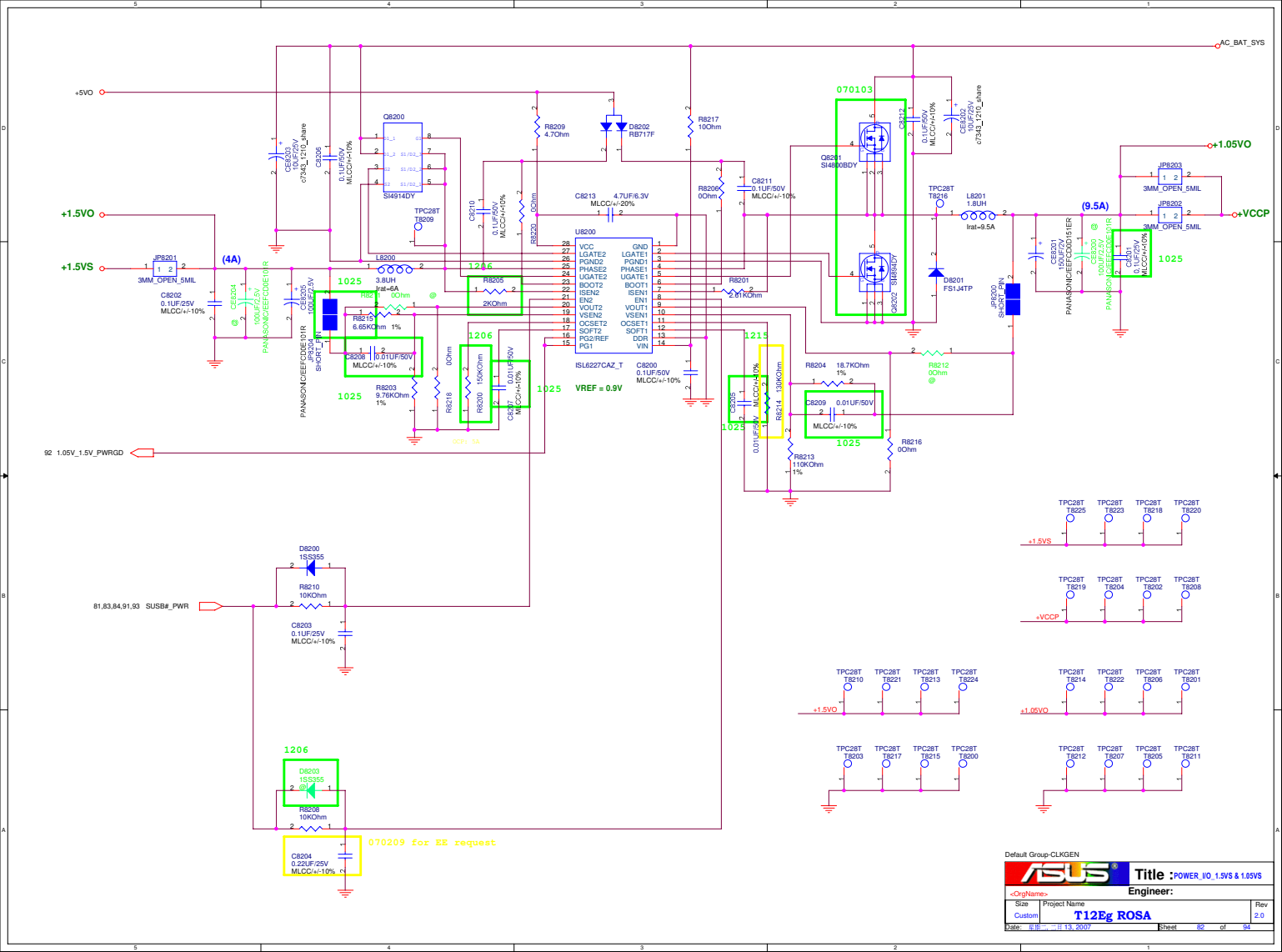
Size	Project Name	Rev
Custom	T12Eg	2.0

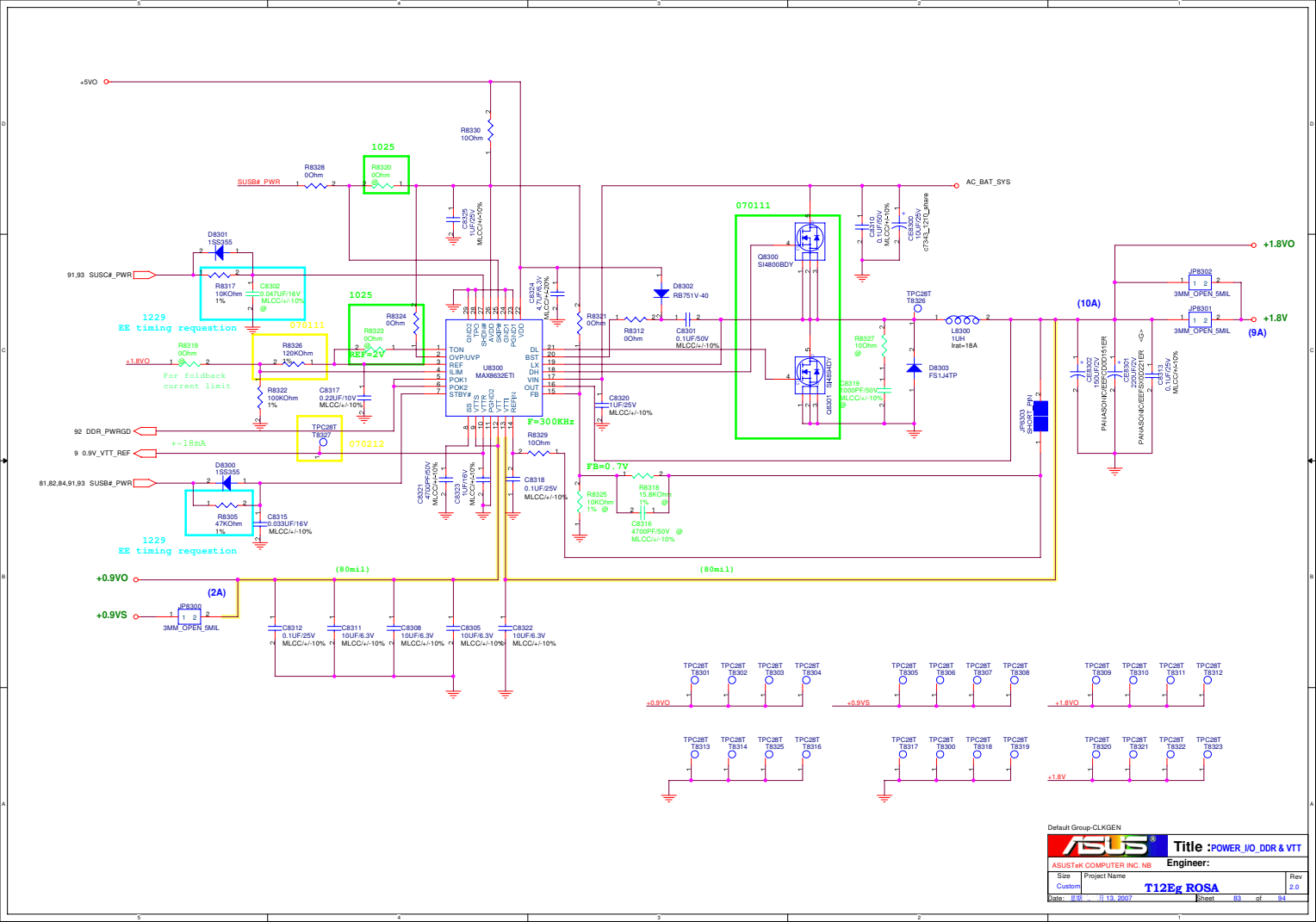
Date: 星期六, 二月 16, 2007 Sheet 79 of 94



1206
070103
(44A)
+VCORE
PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1
Low_side MOSFET
U8000
ISL6262ACRZ-T
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
CPU_VRON_PWR
CPU_VRON
PM_DPRSLPVR
H_DPRSTP#
CLK_EN#
VRM_PWRGD
PM_PSI#
PWR_MON
VCCSENSE
VSSSENSE
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
Q8007 SI4392DY
Q8000 SI4392DY
Q8004 SI4392DY
Q8003 SI4392DY
Q8001 SI4336DY_T1_E3
Q8005 SI4336DY_T1_E3
Q8006 SI4336DY_T1_E3
Q8002 SI4336DY_T1_E3
L8001 0.36UH Irat=32A
L8000 0.36UH Irat=32A
070209
for current balence
R8036 for load line
Close to Pin 18
C8021 & C8018 for transient response
Close to Phase 1 Inductor
R8043 10KOHM 3%
Default Group-CLKGEN
ASUSTeK COMPUTER INC. NB
Title : POWER_VCORE
Engineer: Amos_Yu
Size Custom
Project Name T12Eg ROSA
Rev 2.0
Date: 星期二, 二月 13, 2007
Sheet 80 of 94


AC_BAT_SYS
82,83,84,91,93 SUSB#_PWR
30,92 SUS_PWRGD
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
1118
1025
1206
+5VO
+5VAO
+3VO
+5VSUS
(7A)
(8A)
(0.7A)
(0.02A)
Irat=6A
3.8UH
L8100
L8101
Q8100 SI4800BDY
Q8101 SI4800BDY
Q8103 SI4800BDY
Q8102 SI4800BDY
D8100 FS1J4TP
D8102 FS1J4TP
JP8105 SHORT PIN
JP8103 1MM_OPEN_5MIL
JP8104 1MM_OPEN_5MIL
+3VAO
U8102
SI9183DT
Vref=1.215V
1019 for HTC
D8104 UDZS5.1B
+12VSUS
Imax=100mA
U8100
MIC5235YM5
FB=1.24V
1023
VSUS_ON
070212
87 SHUT_DOWN#
30,50,60,92 FORCE_OFF#
30,43,93 VSUS_ON
Q8105A UM6K1N
Q8105B UM6K1N
+5VA
+3VA
Default Group-CLKGEN
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer:
Size Custom
Project Name T12Eg ROSA
Rev 2.0
Date: 星期一, 二月 13, 2007
Sheet 81 of 94

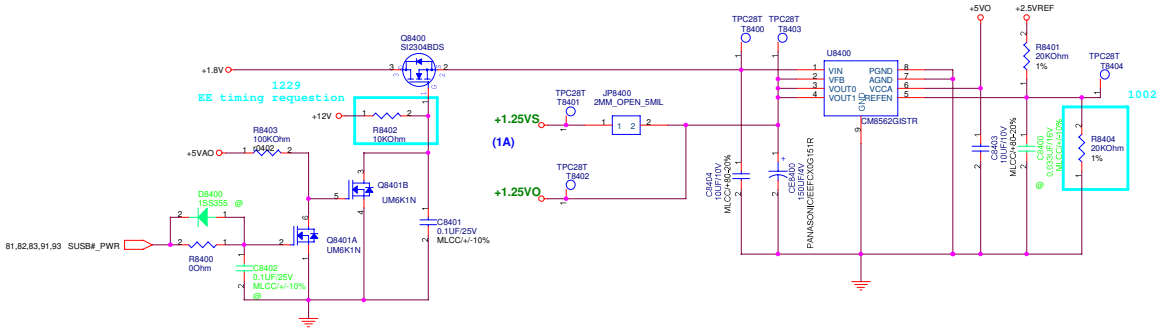

AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
(4A)
(9.5A)
JP8201
3MM_OPEN_5MIL
JP8202
JP8203
Q8200
SI4914DY
Q8201
SI4800BDY
Q8202
SI4840DY
070103
U8200
ISL6227CAZ_T
VREF = 0.9V
L8200
3.8UH
Irat=6A
L8201
1.8UH
Irat=9.5A
D8200
1SS355
D8201
FS1J4TP
D8202
RB717F
D8203
1SS355
92 1.05V_1.5V_PWRGD
81,83,84,91,93 SUSB#_PWR
070209 for EE request
Default Group-CLKGEN
Title : POWER_I/O_1.5VS & 1.05VS
Engineer:
Project Name
T12Eg ROSA
Size
Custom
Rev
2.0
Sheet 82 of 94



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_DDR & VTT	
	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 8 9 , 13, 2007	Sheet 83 of 94	

+1.25VS



Default Group-CLKGEN

ASUS	Title : POWER_I/O_1.25VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 星期二, 九月 13, 2007	Sheet 84 of 94	

Default Group-CLKGEN

Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
C	ROSA	1.1

Date: 6 月 ... H 13, 2007 | Sheet 85 of 94

Default Group-CLKGEN

Title : N/A

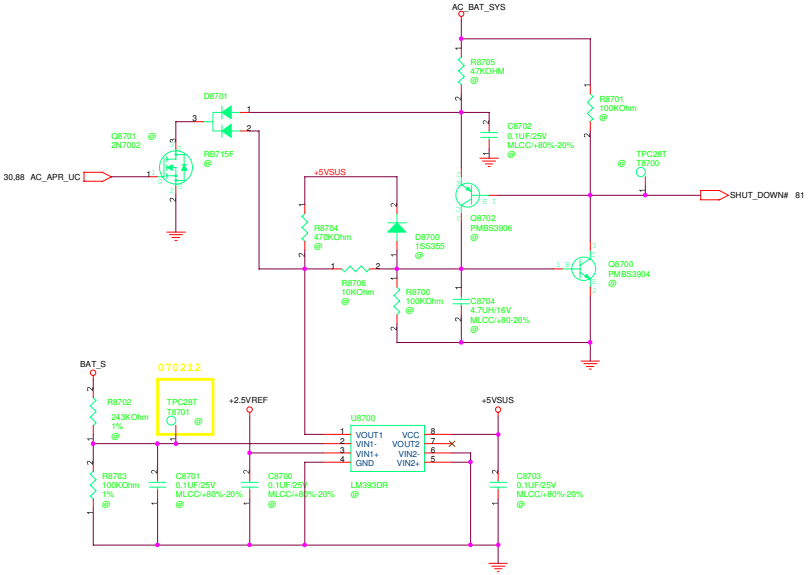
<OrgName>

Engineer:

Size	Project Name	Rev
B	ROSA	1.1

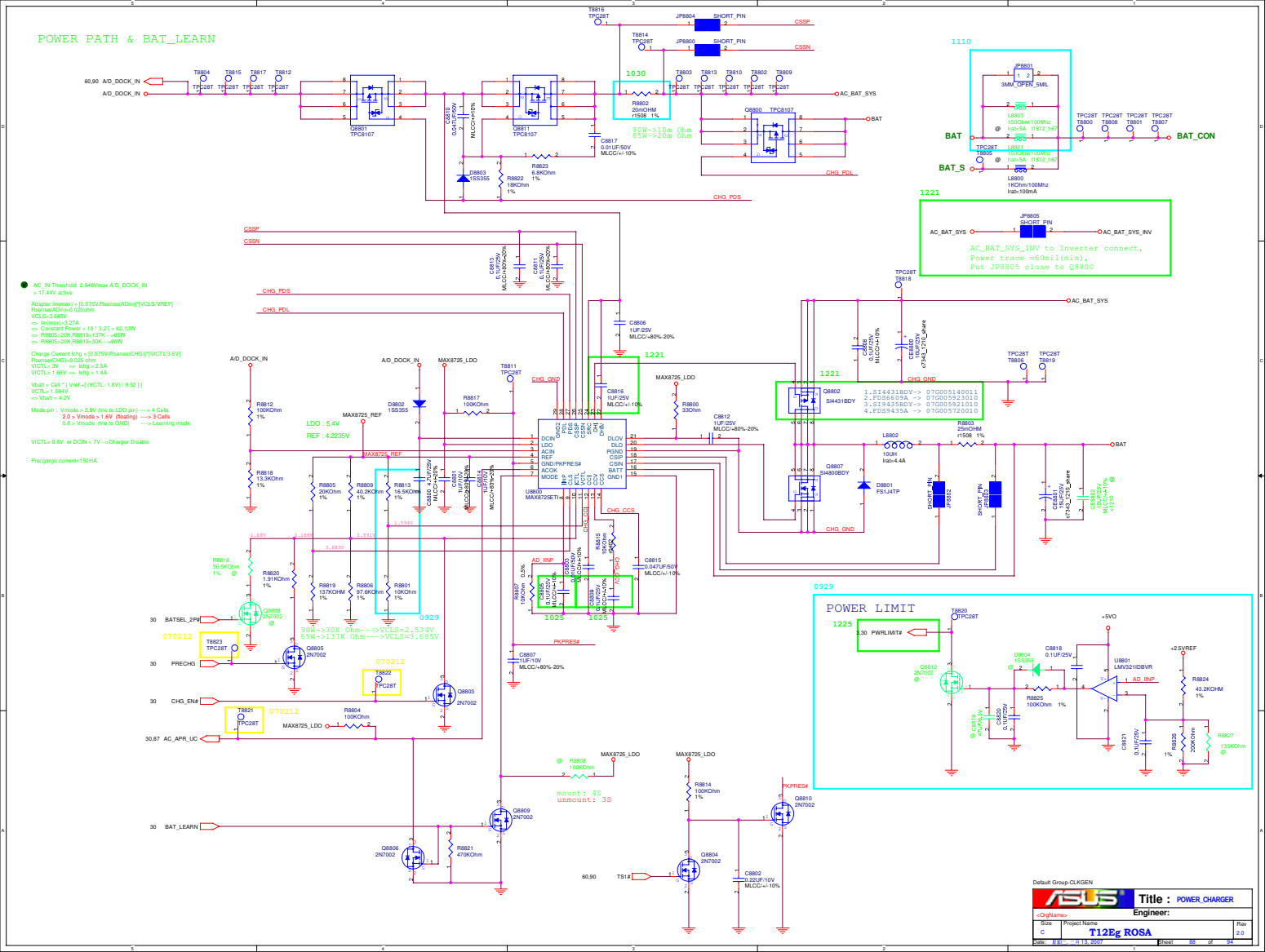
Date: 星期 , 月 13, 2007 Sheet 86 of 94

PIC only



Default Group-CLKGEN

Title : POWER_SHUTDOWN#		
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 87 of 94	


POWER PATH & BAT_LEARN
AC_IN Threshold 2.048V/max A/D_DOCK_IN > 17.44V active
Adapter IIn(max) = [0.075V/Rsense(ADIn)]*[VCLS/VREF]
Rsense(ADIn)=0.020ohm
VCLS=3.685V
=> IIn(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R8805=20K,R8819=137K-->65W
=> R8805=20K,R8819=30K-->20W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.6 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (tria to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
60,90 A/D_DOCK_IN
A/D_DOCK_IN
AC_BAT_SYS
BAT
CHG_PDL
CHG_PDS
CSSP
CSSN
1030
90W->10m Ohm
65W->20m Ohm
1110
BAT
BAT_S
BAT_CON
1221
AC_BAT_SYS
AC_BAT_SYS_INV
AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800
CHG_GND
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
1.68V
2.188V
2.931V
3.685V
1.594V
90W->30K_Ohm--->VCLS=2.534V
65W->137K_Ohm--->VCLS=3.685V
0929
1025
POWER LIMIT
1225
PWRLIMIT#
+5VO
+2.5VREF
AD_IINP
AD_INP
PKPRES#
mount: 4S
unmount: 3S
30 BATSEL_2P#
30 PRECH#
30 CHG_EN#
30,87 AC_APR_UC
30 BAT_LEARN
60,90 TS1#
070212
1. SI4431BDY-> 07G005140011
2. FDD6690A -> 07G005923010
3. SI9435BDY-> 07G005921010
4. FDS9435A -> 07G005720010
1. SI4431BDY-> 07G005140011
2. FDD6690A -> 07G005923010
3. SI9435BDY-> 07G005921010
4. FDS9435A -> 07G005720010
Default Group-CLKGEN
Title : POWER_CHARGER
Engineer:
<OrgName>
Project Name
T12Eg ROSA
Rev 2.0
Sheet 88 of 94

Default Group-CLKGEN

Title : N/A

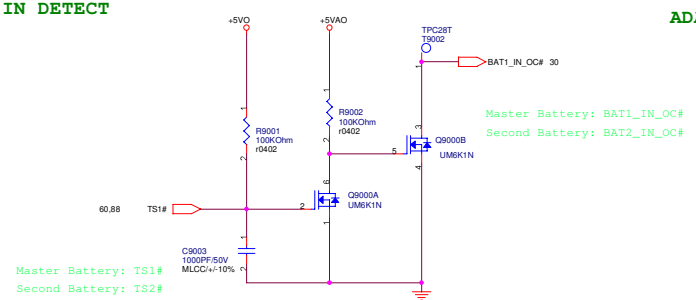
<OrgName>

Engineer:

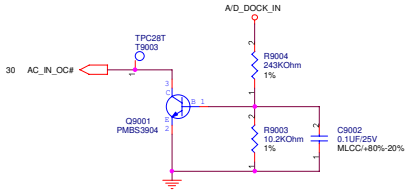
Size	Project Name	Rev
Custom	ROSA	1.1

Date: 星期二, 二月 13, 2007 Sheet 89 of 94

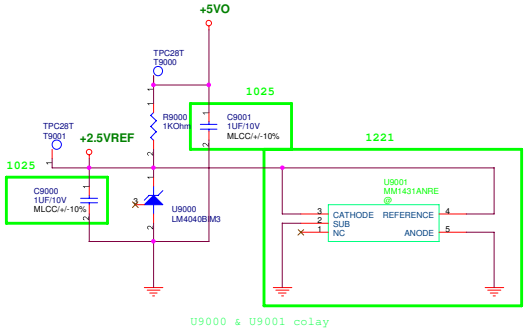
BATTERY IN DETECT



ADAPTER IN DETECT



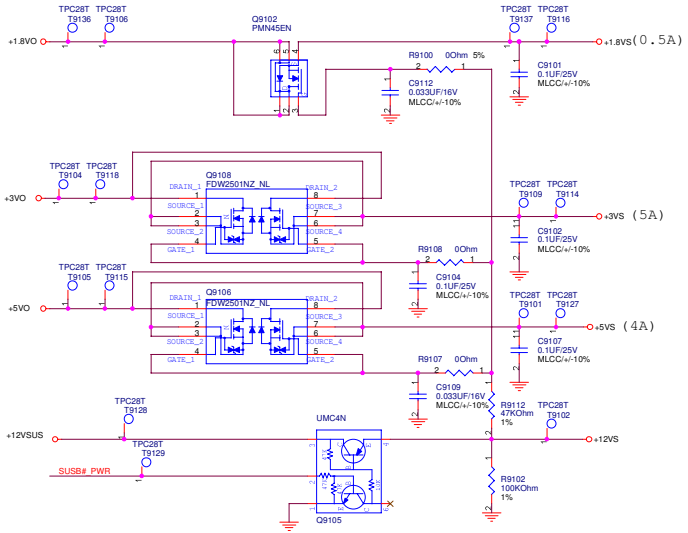
+2.5VREF



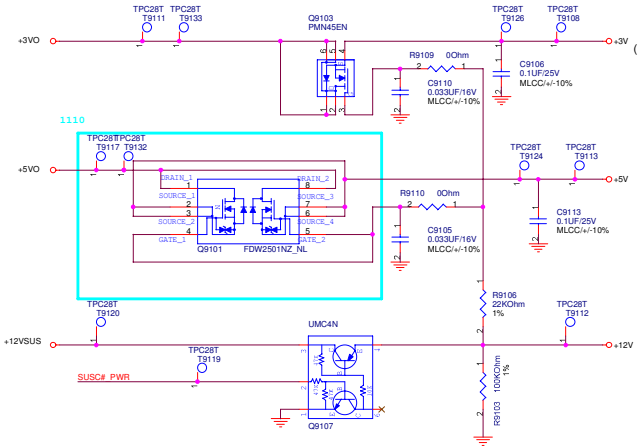
Default Group-CLKGEN

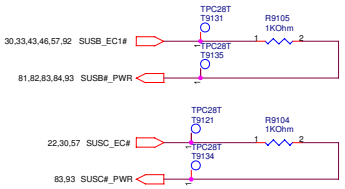
ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 90 of 94	

SUSB#_PWR POWER



SUSC#_PWR POWER





Default Group-CLKGEN

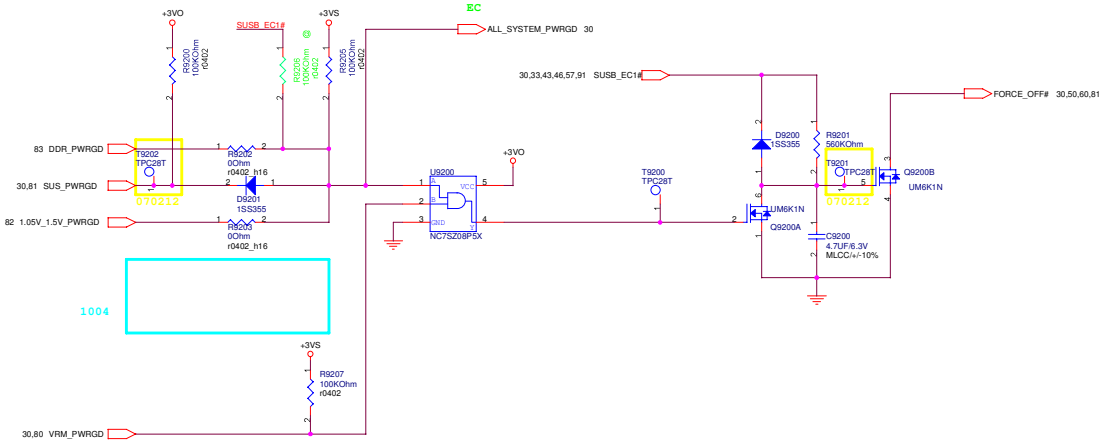
Title : POWER_LOAD SWITCH

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12Eg ROSA	2.0

Date: 星期一, 二月 13, 2007 Sheet 91 of 94

POWER GOOD DETECTER



Default Group-CLKGEN

<OrgName>	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 92 of 94	

AC_BAT_SYS → AC_BAT_SYS 60,80,81,82,83,87,88

BAT → BAT 88

BAT_CON → BAT_CON 60,88

+2.5VREF → +2.5VREF 84,87,88,90

+3VA → +3VA 20,22,30,46,50,57,81

+5VAO → +5VAO 81,84,90

+5VO → +5VO 81,82,83,84,88,90,91

+5VSUS → +5VSUS 23,32,81,87

+5V → +5V 15,32,46,52,56,57,65,91

+5VS → +5VS 23,24,32,36,37,38,45,50,51,56,57,80,91

+3VO → +3VO 81,91,92

+3VSUS → +3VSUS 21,22,23,30,33,37,43,81

+3V → +3V 21,22,35,40,41,44,53,57,61,62,64,65,91

+3VS → +3VS 3,7,8,11,12,15,18,22,23,24,29,30,32,36,40,42,43,45,46,50,51,53,57,62,63,64,66,80,91,92

+12VSUS → +12VSUS 81,91

+12V → +12V 37,42,52,61,84,91

+12VS → +12VS 46,91

+1.8VO → +1.8VO 83,91

+1.8V → +1.8V 7,8,9,11,14,15,83,84

+1.8VS → +1.8VS 18,66,91

+0.9VS → +0.9VS 9,83

+0.9VO → +0.9VO 83

+1.05VO → +1.05VO 80,82

+VCCP → +VCCP 4,10,12,14,15,20,23,29,57,82

+1.5VO → +1.5VO 82

+1.5VS → +1.5VS 4,15,20,21,23,43,53,57,82

+VCORE → +VCORE 4,80

1004

+1.25VS → +1.25VS 11,15,23,84

FOR POWER TEST

070108

+3VA → JP9300 (SGL_JUMP) → CPU_VRON_PWR 80

+3VA → JP9301 (SGL_JUMP) → SUSB#_PWR → SUSB#_PWR 81,82,83,84,91

+3VA → JP9302 (SGL_JUMP) → SUSC#_PWR → SUSC#_PWR 83,91

+3VA → JP9303 (SGL_JUMP) → VSUS_ON → VSUS_ON 30,43,81

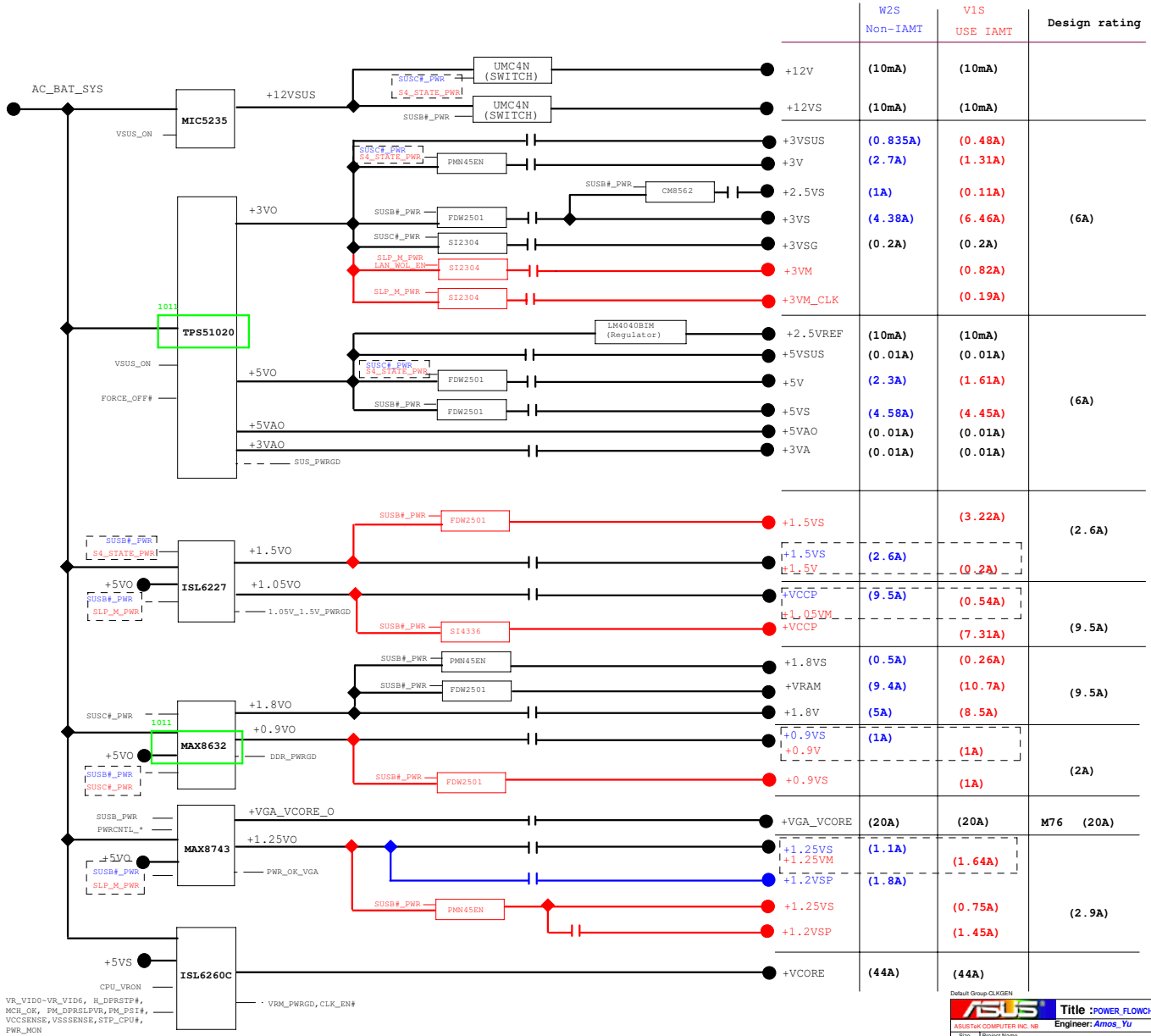
Default Group-CLKGEN

Title : POWER_SIGNAL

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12Eg ROSA	2.0

Date: 星期一, 二月 13, 2007 Sheet 93 of 94


AC_BAT_SYS
MIC5235
VSUS_ON
+12VSUS
UMC4N (SWITCH)
SUSC#_PWR
S4_STATE_PWR
SUSB#_PWR
UMC4N (SWITCH)
TPS51020
1011
VSUS_ON
FORCE_OFF#
+3VO
+5VO
+5VAO
+3VAO
SUS_PWRGD
PMN45EN
CM8562
FDW2501
SI2304
SLP_M_PWR
LAN_WOL_EN
SI2304
SLP_M_PWR
SI2304
LM4040BIM (Regulator)
FDW2501
FDW2501
ISL6227
SUSB#_PWR
S4_STATE_PWR
+5VO
SUSB#_PWR
SLP_M_PWR
+1.5VO
+1.05VO
1.05V_1.5V_PWRGD
FDW2501
SI4336
MAX8632
SUSC#_PWR
1011
+5VO
SUSB#_PWR
SUSC#_PWR
+1.8VO
+0.9VO
DDR_PWRGD
PMN45EN
FDW2501
FDW2501
MAX8743
SUSB_PWR
PWRCNTL_*
+5VO
SUSB#_PWR
SLP_M_PWR
+VGA_VCORE_O
+1.25VO
PWR_OK_VGA
PMN45EN
ISL6260C
+5VS
CPU_VRON
VR_VID0~VR_VID6, H_DPRSTP#, MCH_OK, PM_DPRSLPVR,PM_PSI#, VCCSENSE,VSSSENSE,STP_CPU#, PWR_MON
VRM_PWRGD,CLK_EN#
W2S Non-IAMT
V1S USE IAMT
Design rating
+12V (10mA) (10mA)
+12VS (10mA) (10mA)
+3VSUS (0.835A) (0.48A)
+3V (2.7A) (1.31A)
+2.5VS (1A) (0.11A)
+3VS (4.38A) (6.46A) (6A)
+3VSG (0.2A) (0.2A)
+3VM (0.82A)
+3VM_CLK (0.19A)
+2.5VREF (10mA) (10mA)
+5VSUS (0.01A) (0.01A)
+5V (2.3A) (1.61A)
+5VS (4.58A) (4.45A) (6A)
+5VAO (0.01A) (0.01A)
+3VA (0.01A) (0.01A)
+1.5VS (3.22A) (2.6A)
+1.5VS (2.6A)
+1.5V (0.2A)
+VCCP (9.5A) (0.54A)
+1.05VM
+VCCP (7.31A) (9.5A)
+1.8VS (0.5A) (0.26A)
+VRAM (9.4A) (10.7A) (9.5A)
+1.8V (5A) (8.5A)
+0.9VS (1A)
+0.9V (1A)
+0.9VS (1A) (2A)
+VGA_VCORE (20A) (20A) M76 (20A)
+1.25VS (1.1A)
+1.25VM (1.64A)
+1.2VSP (1.8A)
+1.25VS (0.75A) (2.9A)
+1.2VSP (1.45A)
+VCORE (44A) (44A)
Default Group-CLKGEN
Title :POWER_FLOWCHART
Engineer: Amos_Yu
ASUSTeK COMPUTER INC. NB
Size Custom
Project Name ROSA
Rev 1.0
Date: 9/6/ H 13, 2007
Sheet 94 of 94