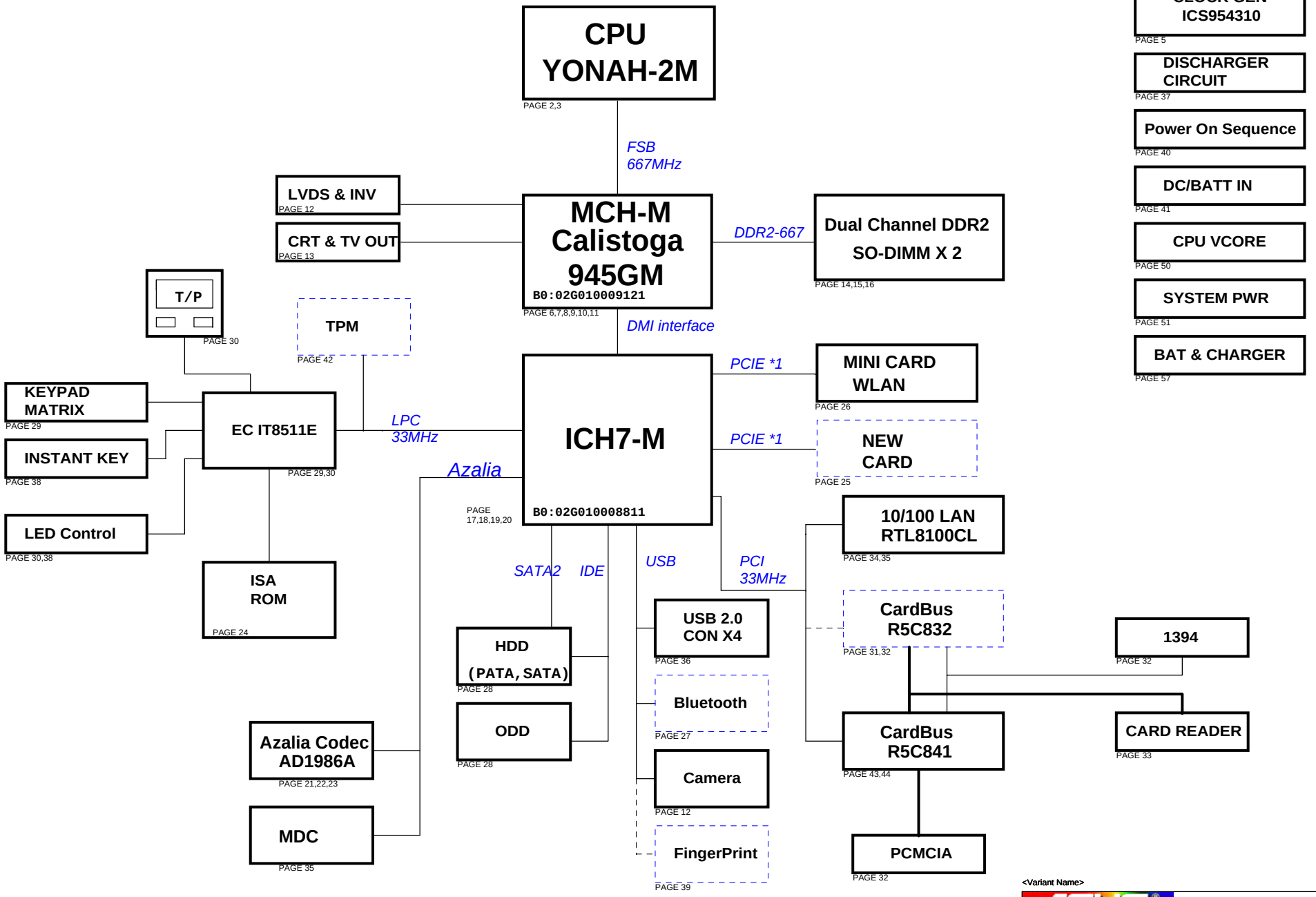
DC/BATT IN

# T12F Block Diagram




<Variant Name>

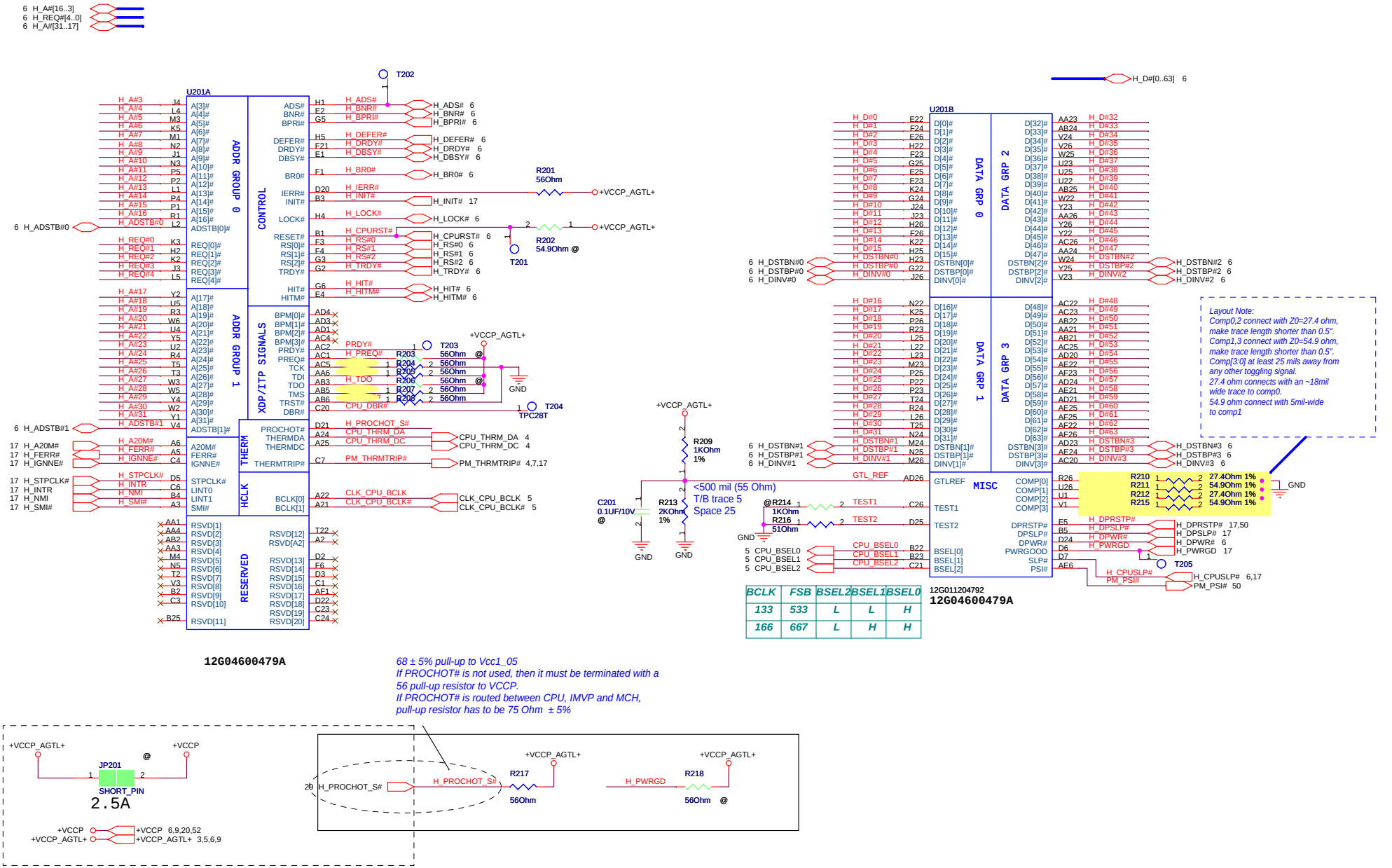
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | 2.3 |

Date: Monday, September 04, 2006 Sheet 1 of 61




| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 133 | 533 | L | L | H |
| 166 | 667 | L | H | H |

12G04600479A

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%




<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 2 of 61

| YUNAH FSB667 | | | |
|---|---|---|---|
| | LFM | TYP | HFM |
| VCC | 1.14V | 1.2V | 1.356V |
| | C4 | C3 | C0 |
| ICC | 0.9A | 7.59A | 27A |

| YUNAH FSB667 | | | |
|---|---|---|---|
| | Min | Typ | Max |
| VCCP | 0.997V | 1.05V | 1.102V |
| | Min | Typ | Max |
| ICCP | | | 2.5A |

+VCCP_AGTL+ → +VCCP_AGTL+ 2,5,6,9

+VCORE → +VCORE 50

+1.5VS → +1.5VS 9,10,20,25,26,37,52

+VCORE

CE301 220UF/4V @ — GND

1215---PWR comp

Place the cap on North of Secondary side

**Vcc Core Decoupling Caps**

**Primary side => Bottom side**

**Secondary side => Top side**

*Place these upper side inside socket cavity on L1*

C302 C303 C304 C305 C306 C307 — 22UF/6.3V — GND

*Place these lower side inside socket cavity on L1*

C308 C309 C310 C311 C312 C313 — 22UF/6.3V @ — GND

*Place these upper side inside socket cavity on L6*

C314 C315 C316 C317 — 22UF/6.3V — GND

C316 N/A, C317 N/A

*Place these lower side inside socket cavity on L6*

C319 C320 C321 C322 — 22UF/6.3V @ — GND

+VCCP_AGTL+

*+1.05V Decoupling Capacitor*

*Place near CPU*

C323 C324 C325 C326 C327 C328 — c0402 — 0.1UF/10V — GND

CE302 100UF/2.5V

U201C

+VCORE

VCC[1] VCC[2] VCC[3] VCC[4] VCC[5] VCC[6] VCC[7] VCC[8] VCC[9] VCC[10] VCC[11] VCC[12] VCC[13] VCC[14] VCC[15] VCC[16] VCC[17] VCC[18] VCC[19] VCC[20] VCC[21] VCC[22] VCC[23] VCC[24] VCC[25] VCC[26] VCC[27] VCC[28] VCC[29] VCC[30] VCC[31] VCC[32] VCC[33] VCC[34] VCC[35] VCC[36] VCC[37] VCC[38] VCC[39] VCC[40] VCC[41] VCC[42] VCC[43] VCC[44] VCC[45] VCC[46] VCC[47] VCC[48] VCC[49] VCC[50] VCC[51] VCC[52] VCC[53] VCC[54] VCC[55] VCC[56] VCC[57] VCC[58] VCC[59] VCC[60] VCC[61] VCC[62] VCC[63] VCC[64] VCC[65] VCC[66] VCC[67]

VCC[68] VCC[69] VCC[70] VCC[71] VCC[72] VCC[73] VCC[74] VCC[75] VCC[76] VCC[77] VCC[78] VCC[79] VCC[80] VCC[81] VCC[82] VCC[83] VCC[84] VCC[85] VCC[86] VCC[87] VCC[88] VCC[89] VCC[90] VCC[91] VCC[92] VCC[93] VCC[94] VCC[95] VCC[96] VCC[97] VCC[98] VCC[99] VCC[100]

VCCP[1] VCCP[2] VCCP[3] VCCP[4] VCCP[5] VCCP[6] VCCP[7] VCCP[8] VCCP[9] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]

VCCA

VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]

VCCSENSE

VSSSENSE

AB20 AB7 AC7 AC9 AC12 AC13 AC15 AC17 AC18 AD7 AD9 AD10 AD12 AD14 AD15 AD17 AD18 AE9 AE10 AE12 AE13 AE15 AE17 AE18 AE20 AF9 AF10 AF12 AF14 AF15 AF17 AF18 AF20

V6 G21 J6 K6 M6 J21 K21 M21 N21 N6 R21 R6 T21 T6 V21 W21 B26

AD6 AE5 AE5 AE4 AE3 AE2 AE2 AF7 AF7

H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6

+VCCP_AGTL+

+VCCA

+1.5VO

JP301 — 1MM_OPEN_5MIL @

RN303D 0Ohm

120mA / 20mil

Close to Pin B26

C301 10UF/10V — C318 0.01UF/25V

checklist suggests 10uF POSCAP

GND

RN302A 0Ohm — VR_VID0 50

RN302B 0Ohm — VR_VID1 50

RN302C 0Ohm — VR_VID2 50

RN302D 0Ohm — VR_VID3 50

RN303A 0Ohm — VR_VID4 50

RN303B 0Ohm — VR_VID5 50

RN303C 0Ohm — VR_VID6 50

R301 100Ohm

R302 100Ohm

**12G04600479A**

U201D

VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25] VSS[26] VSS[27] VSS[28] VSS[29] VSS[30] VSS[31] VSS[32] VSS[33] VSS[34] VSS[35] VSS[36] VSS[37] VSS[38] VSS[39] VSS[40] VSS[41] VSS[42] VSS[43] VSS[44] VSS[45] VSS[46] VSS[47] VSS[48] VSS[49] VSS[50] VSS[51] VSS[52] VSS[53] VSS[54] VSS[55] VSS[56] VSS[57] VSS[58] VSS[59] VSS[60] VSS[61] VSS[62] VSS[63] VSS[64] VSS[65] VSS[66] VSS[67] VSS[68] VSS[69] VSS[70] VSS[71] VSS[72] VSS[73] VSS[74] VSS[75] VSS[76] VSS[77] VSS[78] VSS[79] VSS[80] VSS[81]

VSS[82] VSS[83] VSS[84] VSS[85] VSS[86] VSS[87] VSS[88] VSS[89] VSS[90] VSS[91] VSS[92] VSS[93] VSS[94] VSS[95] VSS[96] VSS[97] VSS[98] VSS[99] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[111] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[129] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[147] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162]

A4 A8 A11 A14 A16 A19 A23 A26 B6 B8 B11 B13 B16 B19 B21 B24 C5 C8 C11 C14 C16 C19 C22 C25 D1 D4 D8 D11 D13 D16 D19 D23 D26 E3 E6 E8 E11 E14 E16 E19 E21 E24 F5 F8 F11 F13 F16 F19 F2 F22 F25 G4 G1 G23 G26 H3 H6 H21 H24 J2 J5 J22 J25 K1 K4 K23 K26 L3 L6 L21 L24 M2 M5 M22 M25 N1 N4 N23 N26 P3

P6 P21 P24 R2 R5 R22 R25 T1 T4 T23 T26 U3 U6 U21 U24 V2 V5 V22 V25 W1 W4 W23 W26 Y3 Y6 Y21 Y24 AA2 AA5 AA8 AA11 AA14 AA16 AA19 AA22 AA25 AB1 AB4 AB8 AB11 AB13 AB16 AB19 AB23 AB26 AC3 AC6 AC8 AC11 AC14 AC16 AC19 AC21 AC24 AD2 AD5 AD8 AD11 AD13 AD16 AD19 AD22 AD25 AE1 AE4 AE8 AE11 AE14 AE16 AE19 AE23 AE26 AF3 AF6 AF8 AF11 AF13 AF16 AF19 AF21 AF24

GND GND

**12G04600479A**

*Layout Note:*
*VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.*
*The VCCSENSE/VSSSENSE should be length matched to within 25 mils.*
*These resistors should be placed within 2 inch of the CPU.*

<Variant Name>

ASUSTeK COMPUTER INC

Title : Yonah CPU (2)

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

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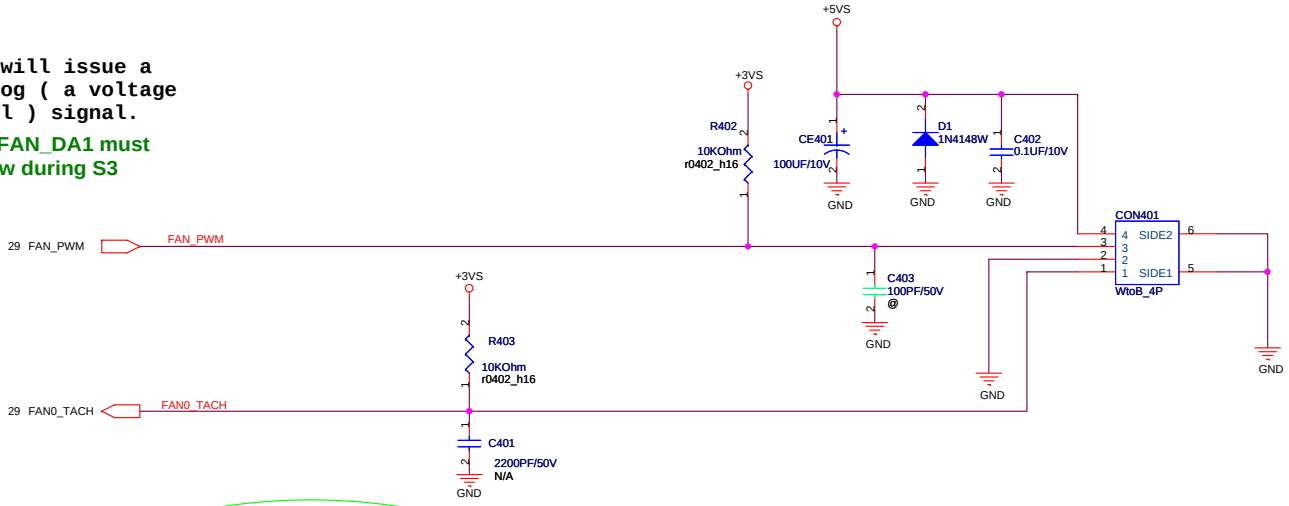
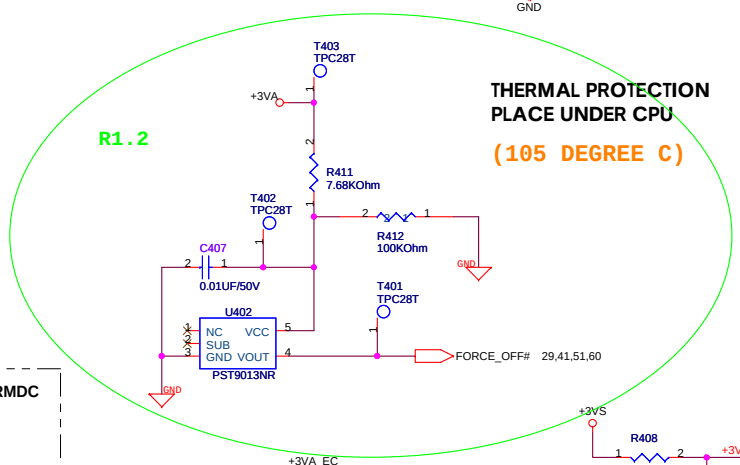
# Fan Speed Control

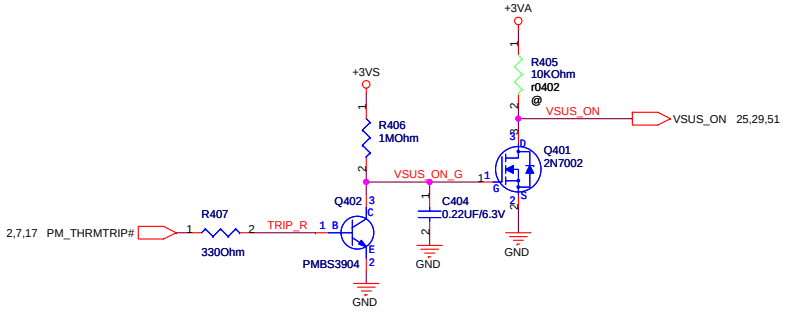
+5VS 13,19,20,21,22,28,29,30,37,38,50,61
+3VS 5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61
+3VA 12,20,22,29,37,38,40,54,59,63

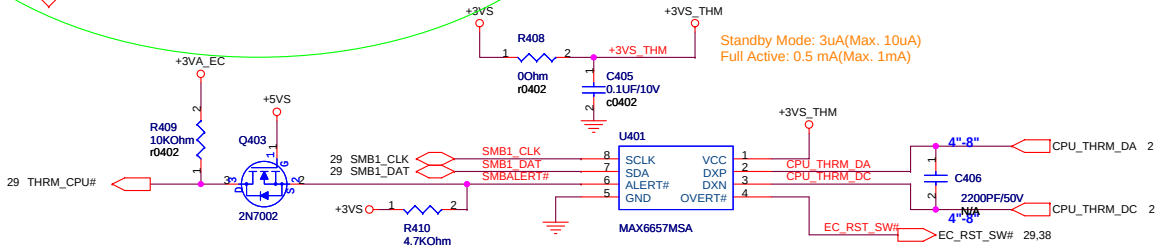
**KBC will issue a analog ( a voltage level ) signal.**

**SW: FAN_DA1 must be low during S3**




**Route H_THERMDA and H_THERMDC on the same layer**

**----------OTHER SIGNALS**
**12 mils**
**==========GND**
**10 mils**
**==========H_THERMDA(10 mils)**
**10 mils**
**==========H_THERMDC(10 mils)**
**10 mils**
**==========GND**
**12 mils**
**----------OTHER SIGNALS**

**Avoid BPSB,Power**

<Variant Name>

ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

Date: Monday, September 04, 2006 Sheet 4 of 61

| Request | Control net | Net name |
|---|---|---|
| PCIE_REQ1# | PCIE0(#),PCIE6(#) | None |
| PCIE_REQ2# | PCIE1(#),PCIE8(#) | None |
| PCIE_REQ3# | PCIE2(#),PCIE4(#) | CLK_PCIE_MINICARD(#) |
| PCIE_REQ4# | PCIE3(#),PCIE5(#),PCIE7(#) | CLK_MCH_3GPLL(#) |

| Bclk | FSB | FSLC BSEL2 | FSLB BSEL1 | FSLA BSEL0 |
|---|---|---|---|---|
| 133 | 533 | L | L | H |
| 166 | 667 | L | H | H |

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

R2.0

U501 ICS954310CGLFT

**PREQ#1**
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

**PREQ#2**
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

**PREQ#3**
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

**PREQ#4**
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

**SELPCIE0_LCD#:**
**0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS**

**SELLCD_27#/PCICLK_F1:**
**1-->pin17,pin18=LCDCLK(96MHz)**

**PCICLK2/REQ_SEL:**
**1-->pin40,pin41=PREQ1#,PREQ2#**

**ITP_EN/PCICLK_F0:**
**1-->CPU_ITP pair**

**Realtek:Mount R519,Remove R550 R534**

Internal Pull-Up Resistor

Internal Pull-Down Resistor

<Variant Name>

ASUSTeK COMPUTER INC

Title : CLOCK GEN

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

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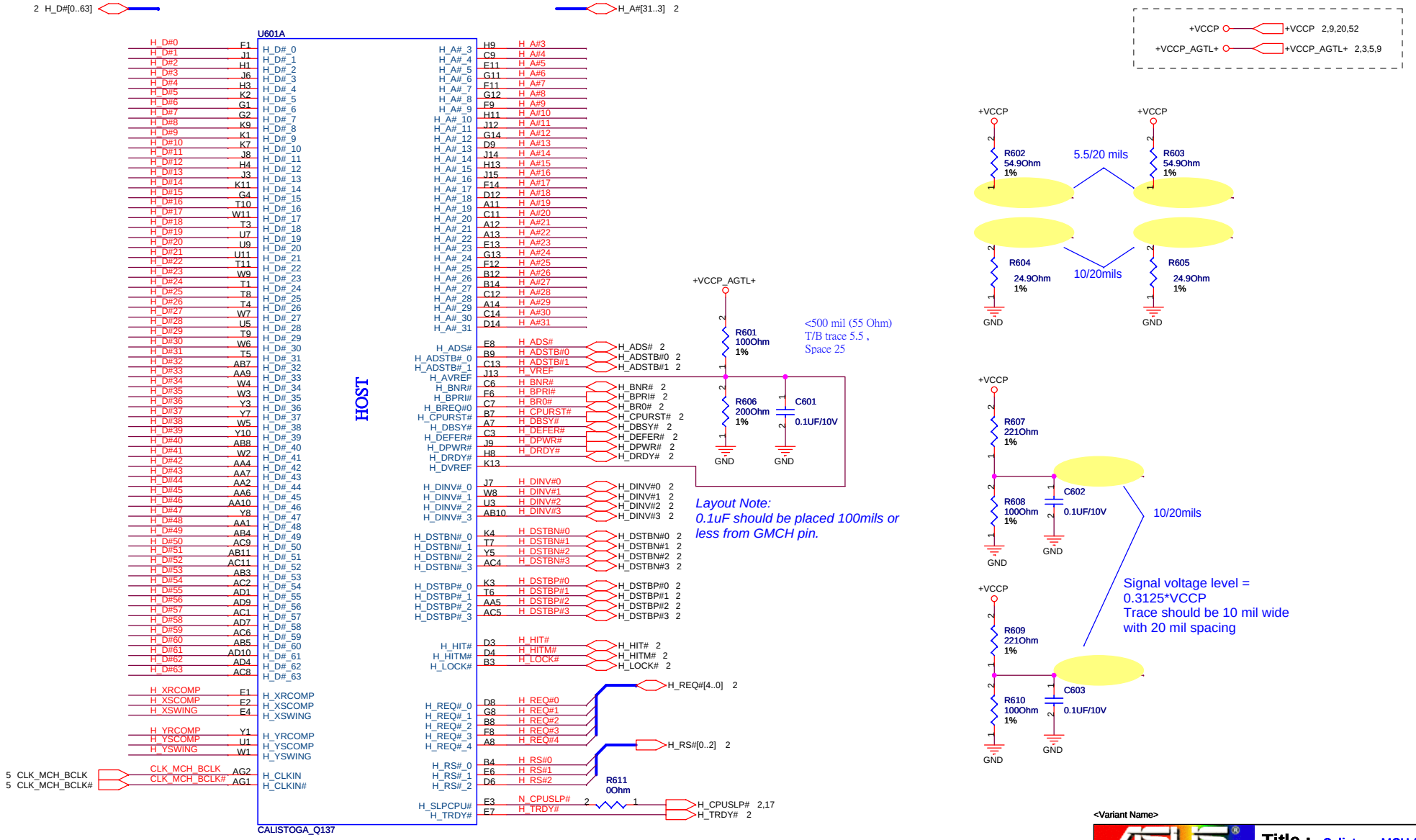
2 H_D#[0..63]
H_A#[31..3] 2
U601A
HOST
CALISTOGA_Q137
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
CLK_MCH_BCLK AG2
CLK_MCH_BCLK# AG1
5 CLK_MCH_BCLK
5 CLK_MCH_BCLK#
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#3
H_A#4
H_A#5
H_A#6
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H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_AVREF J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_DVREF K13
H_ADS# 2
H_ADSTB#0 2
H_ADSTB#1 2
H_BNR# 2
H_BPRI# 2
H_BR0# 2
H_CPURST# 2
H_DBSY# 2
H_DEFER# 2
H_DPWR# 2
H_DRDY# 2
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#0 2
H_DINV#1 2
H_DINV#2 2
H_DINV#3 2
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#0 2
H_DSTBN#1 2
H_DSTBN#2 2
H_DSTBN#3 2
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#0 2
H_DSTBP#1 2
H_DSTBP#2 2
H_DSTBP#3 2
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT#
H_HITM#
H_LOCK#
H_HIT# 2
H_HITM# 2
H_LOCK# 2
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4..0] 2
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[0..2] 2
R611
0Ohm
H_SLPCPU# E3
H_TRDY# E7
N_CPUSLP#
H_TRDY#
H_CPUSLP# 2,17
H_TRDY# 2
+VCCP_AGTL+
R601
100Ohm
1%
R606
200Ohm
1%
C601
0.1UF/10V
GND
<500 mil (55 Ohm)
T/B trace 5.5 ,
Space 25
Layout Note:
0.1uF should be placed 100mils or
less from GMCH pin.
+VCCP
+VCCP_AGTL+
+VCCP 2,9,20,52
+VCCP_AGTL+ 2,3,5,9
R602
54.9Ohm
1%
R603
54.9Ohm
1%
5.5/20 mils
R604
24.9Ohm
1%
R605
24.9Ohm
1%
10/20mils
R607
221Ohm
1%
R608
100Ohm
1%
C602
0.1UF/10V
10/20mils
R609
221Ohm
1%
R610
100Ohm
1%
C603
0.1UF/10V
Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing
<Variant Name>
Title : Calistoga MCH (1)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size B
Project Name T12F
Rev
Date: Monday, September 04, 2006
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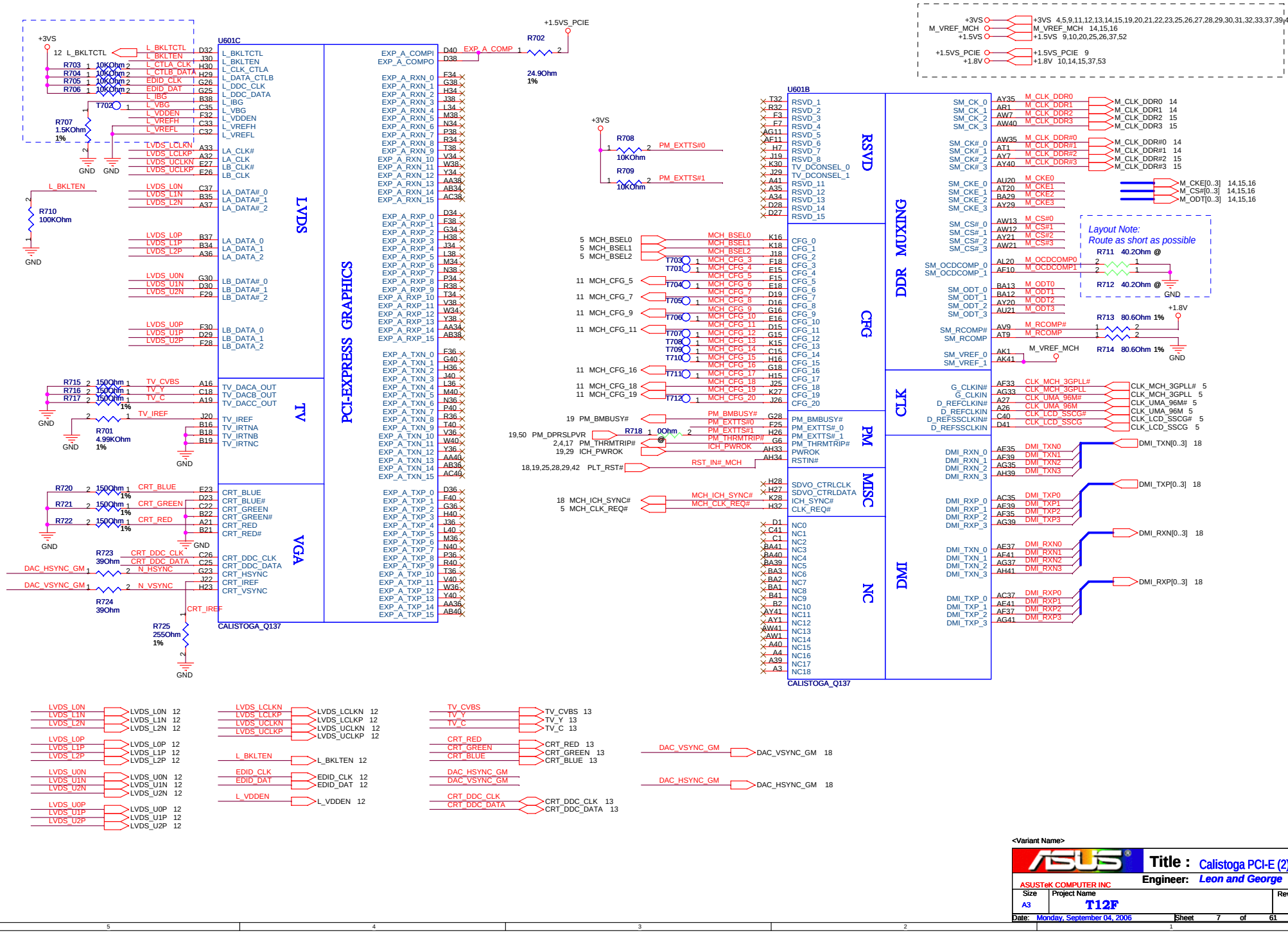
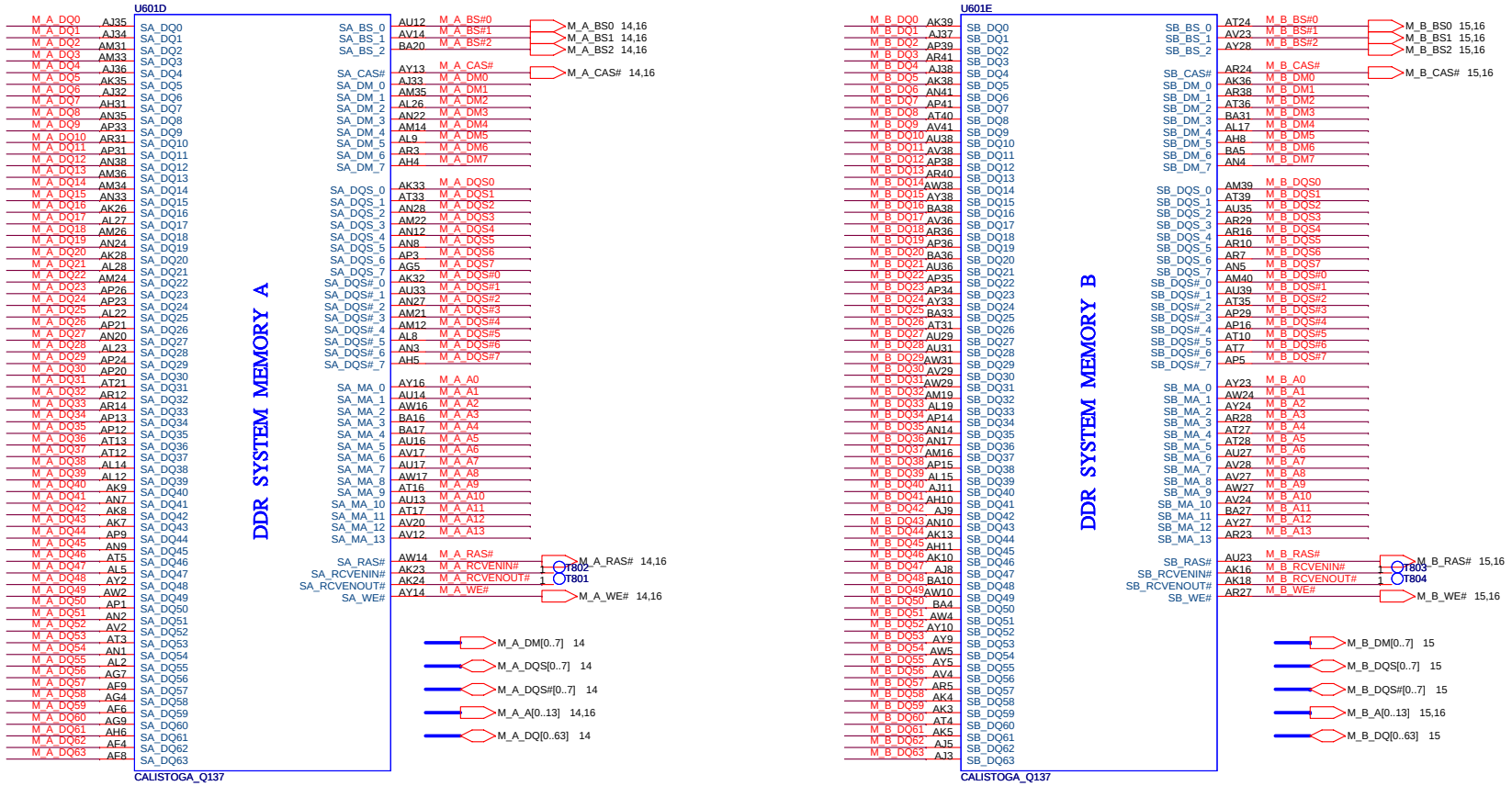

U601C
U601B
CALISTOGA_Q137
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
RSVD
DDR MUXING
CFG
CLK
PM
MISC
DMI
NC
Layout Note:
Route as short as possible
+3VS
+1.5VS_PCIE
+1.8V
M_VREF_MCH
+3VS 4,5,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50
M_VREF_MCH 14,15,16
+1.5VS 9,10,20,25,26,37,52
+1.5VS_PCIE 9
+1.8V 10,14,15,37,53
L_BKLTCTL
L_BKLTEN
L_CTLA_CLK
L_CTLB_DATA
EDID_CLK
EDID_DAT
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LVDS_LCLKN
LVDS_LCLKP
LVDS_UCLKN
LVDS_UCLKP
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LVDS_L0N
LVDS_L1N
LVDS_L2N
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LVDS_L0P
LVDS_L1P
LVDS_L2P
LA_DATA_0
LA_DATA_1
LA_DATA_2
LVDS_U0N
LVDS_U1N
LVDS_U2N
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LVDS_U0P
LVDS_U1P
LVDS_U2P
LB_DATA_0
LB_DATA_1
LB_DATA_2
TV_CVBS
TV_Y
TV_C
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_BLUE#
CRT_GREEN#
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
CRT_IREF
DAC_HSYNC_GM
DAC_VSYNC_GM
N_HSYNC
N_VSYNC
EXP_A_COMPI
EXP_A_COMPO
EXP_A_COMP
EXP_A_RXN_0
EXP_A_RXN_1
EXP_A_RXN_2
EXP_A_RXN_3
EXP_A_RXN_4
EXP_A_RXN_5
EXP_A_RXN_6
EXP_A_RXN_7
EXP_A_RXN_8
EXP_A_RXN_9
EXP_A_RXN_10
EXP_A_RXN_11
EXP_A_RXN_12
EXP_A_RXN_13
EXP_A_RXN_14
EXP_A_RXN_15
EXP_A_RXP_0
EXP_A_RXP_1
EXP_A_RXP_2
EXP_A_RXP_3
EXP_A_RXP_4
EXP_A_RXP_5
EXP_A_RXP_6
EXP_A_RXP_7
EXP_A_RXP_8
EXP_A_RXP_9
EXP_A_RXP_10
EXP_A_RXP_11
EXP_A_RXP_12
EXP_A_RXP_13
EXP_A_RXP_14
EXP_A_RXP_15
EXP_A_TXN_0
EXP_A_TXN_1
EXP_A_TXN_2
EXP_A_TXN_3
EXP_A_TXN_4
EXP_A_TXN_5
EXP_A_TXN_6
EXP_A_TXN_7
EXP_A_TXN_8
EXP_A_TXN_9
EXP_A_TXN_10
EXP_A_TXN_11
EXP_A_TXN_12
EXP_A_TXN_13
EXP_A_TXN_14
EXP_A_TXN_15
EXP_A_TXP_0
EXP_A_TXP_1
EXP_A_TXP_2
EXP_A_TXP_3
EXP_A_TXP_4
EXP_A_TXP_5
EXP_A_TXP_6
EXP_A_TXP_7
EXP_A_TXP_8
EXP_A_TXP_9
EXP_A_TXP_10
EXP_A_TXP_11
EXP_A_TXP_12
EXP_A_TXP_13
EXP_A_TXP_14
EXP_A_TXP_15
PM_EXTTS#0
PM_EXTTS#1
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
MCH_CFG_3
MCH_CFG_4
MCH_CFG_5
MCH_CFG_6
MCH_CFG_7
MCH_CFG_8
MCH_CFG_9
MCH_CFG_10
MCH_CFG_11
MCH_CFG_12
MCH_CFG_13
MCH_CFG_14
MCH_CFG_15
MCH_CFG_16
MCH_CFG_17
MCH_CFG_18
MCH_CFG_19
MCH_CFG_20
PM_BMBUSY#
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP#
ICH_PWROK
RST_IN#_MCH
PLT_RST#
MCH_ICH_SYNC#
MCH_CLK_REQ#
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#2
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS#0
M_CS#1
M_CS#2
M_CS#3
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_OCDCOMP0
M_OCDCOMP1
M_RCOMP
M_RCOMP#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_UMA_96M
CLK_LCD_SSCG
CLK_LCD_SSCG#
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
R702 24.9Ohm 1%
R703 10KOhm
R704 10KOhm
R705 10KOhm
R706 10KOhm
R707 1.5KOhm 1%
R708 10KOhm
R709 10KOhm
R710 100KOhm
R711 40.2Ohm @
R712 40.2Ohm @
R713 80.6Ohm 1%
R714 80.6Ohm 1%
R715 150Ohm 1%
R716 150Ohm 1%
R717 150Ohm 1%
R718 0Ohm @
R720 150Ohm 1%
R721 150Ohm 1%
R722 150Ohm 1%
R723 39Ohm
R724 39Ohm
R725 255Ohm 1%
T701
T702
T703
T704
T705
T706
T707
T708
T709
T710
T711
T712
GND




<Variant Name>

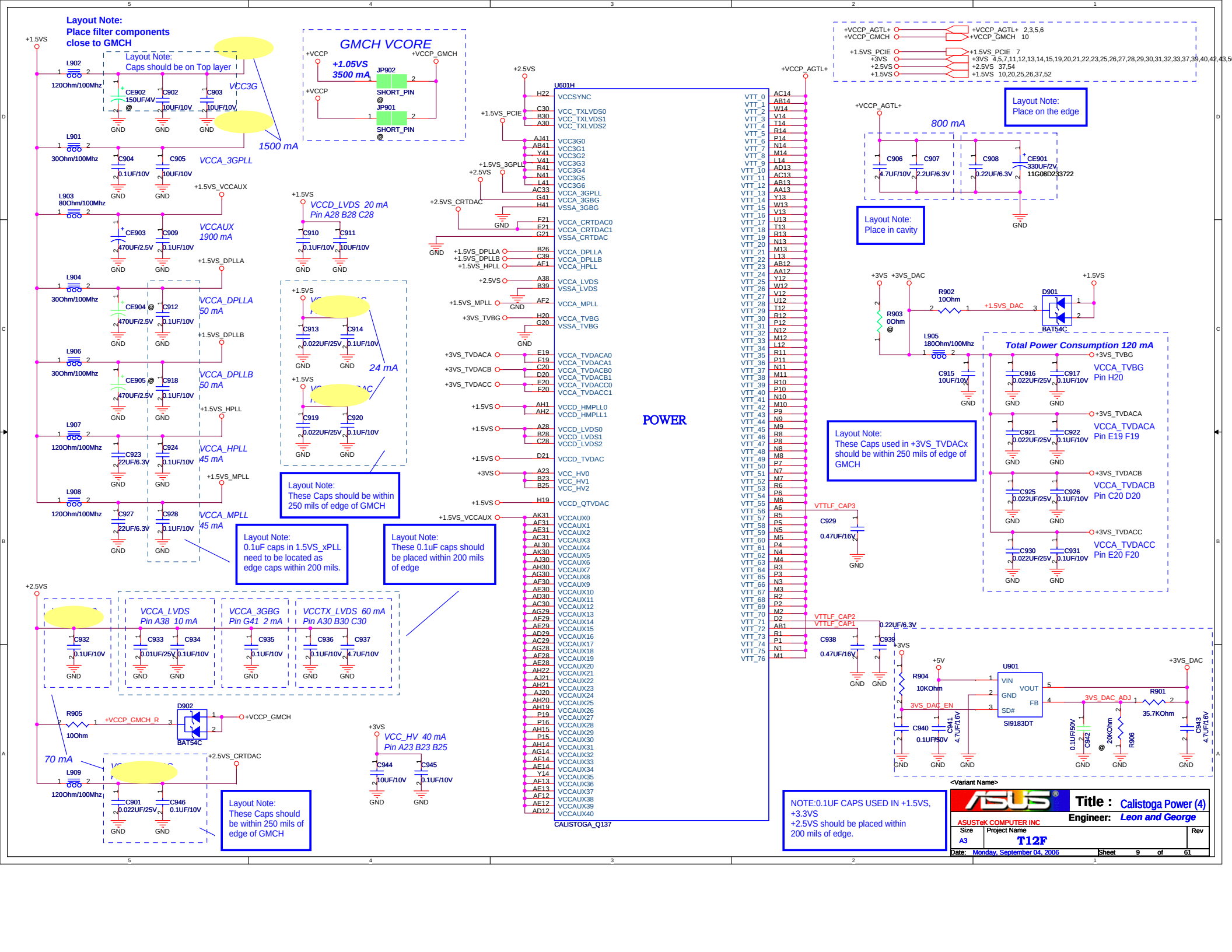
ASUSTeK COMPUTER INC

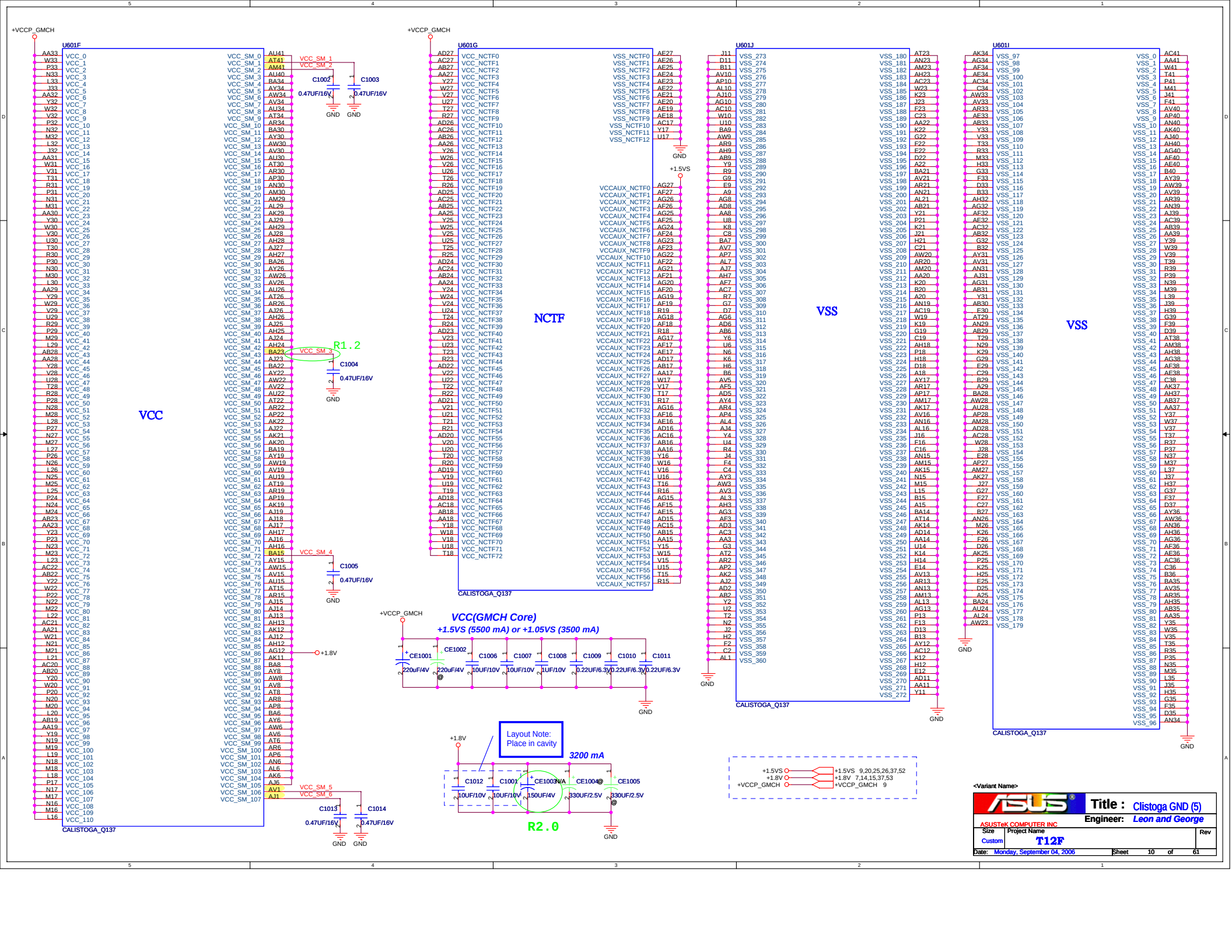
Title : Calistoga DDR2 (3)

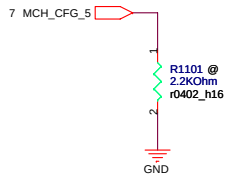
Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

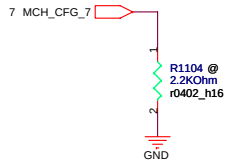
Date: Monday, September 04, 2006 Sheet 8 of 61


Layout Note:
Place filter components
close to GMCH
Layout Note:
Caps should be on Top layer
VCC3G
1500 mA
VCCA_3GPLL
VCCAUX
1900 mA
VCCA_DPLLA
50 mA
VCCA_DPLLB
50 mA
VCCA_HPLL
45 mA
VCCA_MPLL
45 mA
GMCH VCORE
+1.05VS
3500 mA
SHORT_PIN
VCCD_LVDS 20 mA
Pin A28 B28 C28
24 mA
Layout Note:
These Caps should be within
250 mils of edge of GMCH
Layout Note:
0.1uF caps in 1.5VS_xPLL
need to be located as
edge caps within 200 mils.
Layout Note:
These 0.1uF caps should
be placed within 200 mils
of edge
VCCA_LVDS
Pin A38 10 mA
VCCA_3GBG
Pin G41 2 mA
VCCTX_LVDS 60 mA
Pin A30 B30 C30
70 mA
VCC_HV 40 mA
Pin A23 B23 B25
Layout Note:
These Caps should
be within 250 mils of
edge of GMCH
U601H
CALISTOGA_Q137
POWER
Layout Note:
Place on the edge
800 mA
Layout Note:
Place in cavity
Layout Note:
These Caps used in +3VS_TVDACx
should be within 250 mils of edge of
GMCH
Total Power Consumption 120 mA
VCCA_TVBG
Pin H20
VCCA_TVDACA
Pin E19 F19
VCCA_TVDACB
Pin C20 D20
VCCA_TVDACC
Pin E20 F20
NOTE:0.1UF CAPS USED IN +1.5VS,
+3.3VS
+2.5VS should be placed within
200 mils of edge.
Title : Calistoga Power (4)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size A3
Project Name T12F
Rev
Date: Monday, September 04, 2006
Sheet 9 of 61

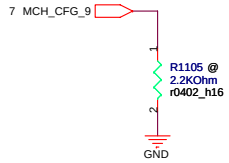

+VCCP_GMCH
U601F
VCC
CALISTOGA_Q137
C1002
C1003
0.47UF/16V
GND
R1.2
VCC_SM_3
C1004
0.47UF/16V
VCC_SM_4
C1005
0.47UF/16V
+1.8V
VCC_SM_5
VCC_SM_6
C1013
C1014
0.47UF/16V
U601G
NCTF
CALISTOGA_Q137
+1.5VS
VCC(GMCH Core)
+1.5VS (5500 mA) or +1.05VS (3500 mA)
CE1001
CE1002
C1006
C1007
C1008
C1009
C1010
C1011
220uF/4V
10UF/10V
1UF/10V
0.22UF/6.3V
Layout Note:
Place in cavity
3200 mA
C1012
C1001
CE1003 N/A
CE1004@
CE1005
150UF/4V
330UF/2.5V
R2.0
U601J
VSS
CALISTOGA_Q137
+1.5VS 9,20,25,26,37,52
+1.8V 7,14,15,37,53
+VCCP_GMCH 9
U601I
VSS
CALISTOGA_Q137
<Variant Name>
ASUSTeK COMPUTER INC
Title : Clistoga GND (5)
Engineer: Leon and George
Size: Custom
Project Name: T12F
Rev
Date: Monday, September 04, 2006
Sheet 10 of 61



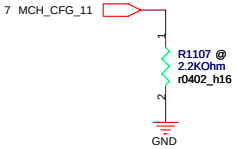

CFG5 : DMI X2 Select
LOW = DMI X 2
***HIGH = DMI X 4 (Default)***



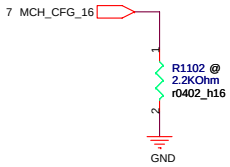

CFG7 : CPU STRAP
LOW = Reserved
***HIGH = Mobility CPU (Default)***



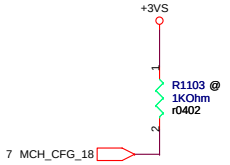

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
***HIGH = NORMAL OPERATION (Default)***



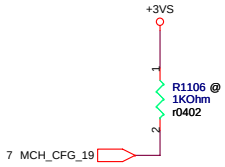

CFG11 : Reserved but need to be pull low




CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
***HIGH = Dynamic ODT Enabled (Default)***



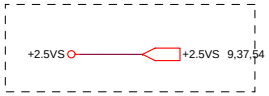

CFG18 : GMCH Core Voltage Level
LOW = 1.05V
***HIGH = 1.5V (default)***




CFG19 : DMI LANE REVERSAL
***LOW = NORMAL***
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

| CFG | All are sampled with respect to the leading edge of the GMCH PWROK | |
|---|---|---|
| 2:0 | FSB Freq select | 001 = FSB533<br>011 = FSB667 |
| 4:3 | | |
| 5 | DMI X 2 Select | 0 = DMI X 2<br>1 = DMI X 4 (Default) |
| 6 | | |
| 7 | CPU Strap | 0 = Reserved<br>1 = Mobile CPU (Default) |
| 8 | | |
| 9 | PCIE Graphics Lane | 0 = Reverse Lanes<br>1 = Normal (Default) |
| 11:10 | Reversal | |
| 13:12 | XOR/ALLZ | 00 = Partial Clock Gating Disable<br>01 = XOR Mode Enabled<br>10 = All-Z Mode Enabled<br>11 = Normal operation (Default) |
| 15:14 | | |
| 16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled<br>1 = Dynamic ODT Enabled (Default) |
| 17 | | |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card Present (Default)<br>1 = SDVO Card Present |
| 18 | VCC select | 0 = 1.05V (Default)<br>1 = 1.5V |
| 19 | DMI Lane Reversal | 0 = Normal (Default)<br>1 = Reverse Lanes |
| 20 | SDVO/PCIE concurrent | 0 = Only SDVO or PCIE x1 is operational(Default)<br>1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |



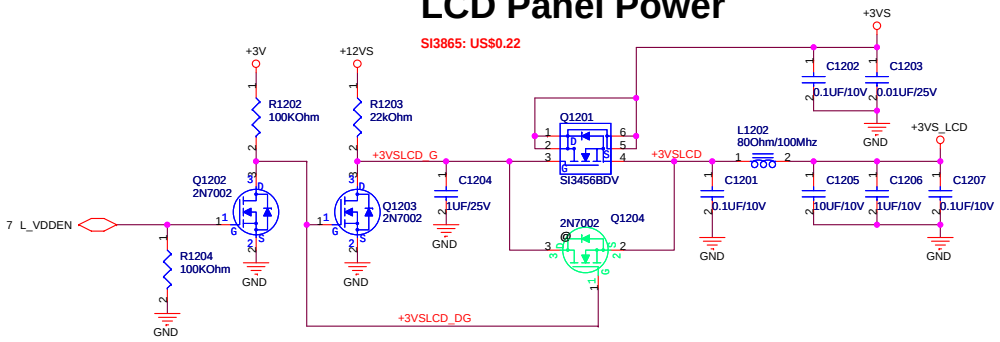

<Variant Name>

Title : Calistoga Strapping
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12F | Rev:
Date: Monday, September 04, 2006 | Sheet 11 of 61

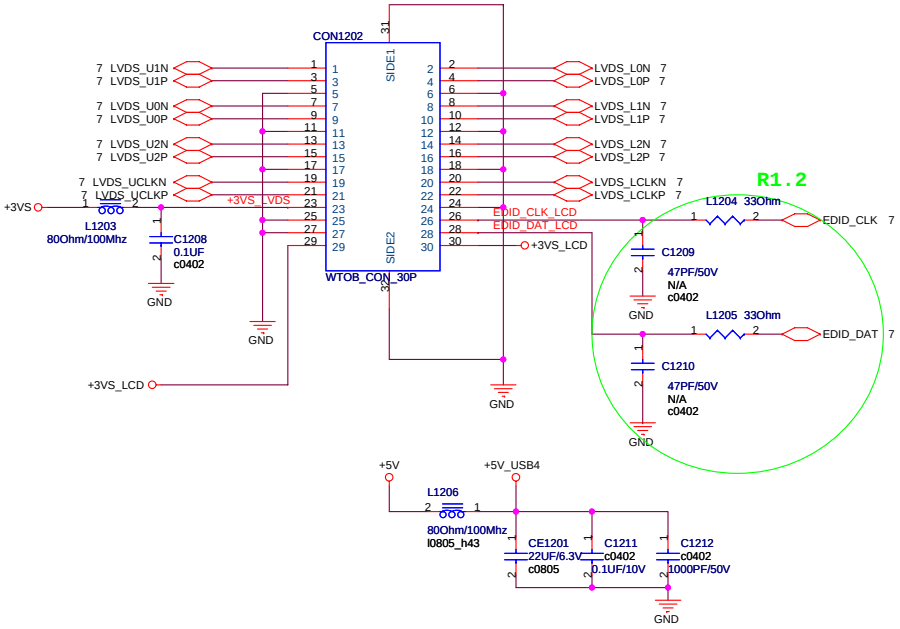
# LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

SI3865: US$0.22




# LCD LVDS Interface







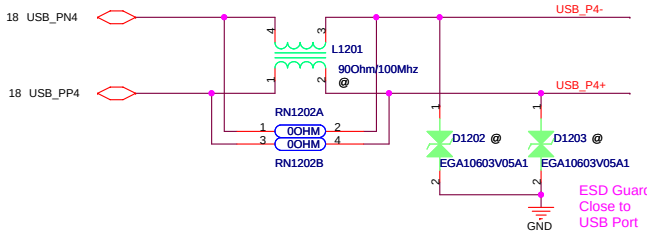
# LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal ( adjust voltage level) to adjust backlight

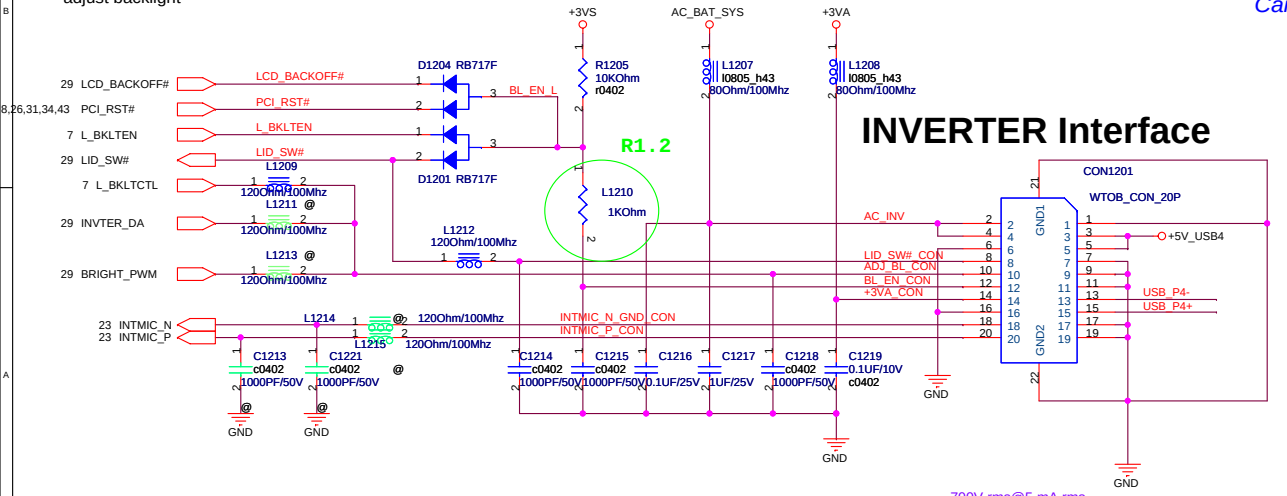
***Inverter Board built in 14.1W LCD Panel***

*USB4 For CMOS Camera*




ESD Guard Close to USB Port

# INVERTER Interface

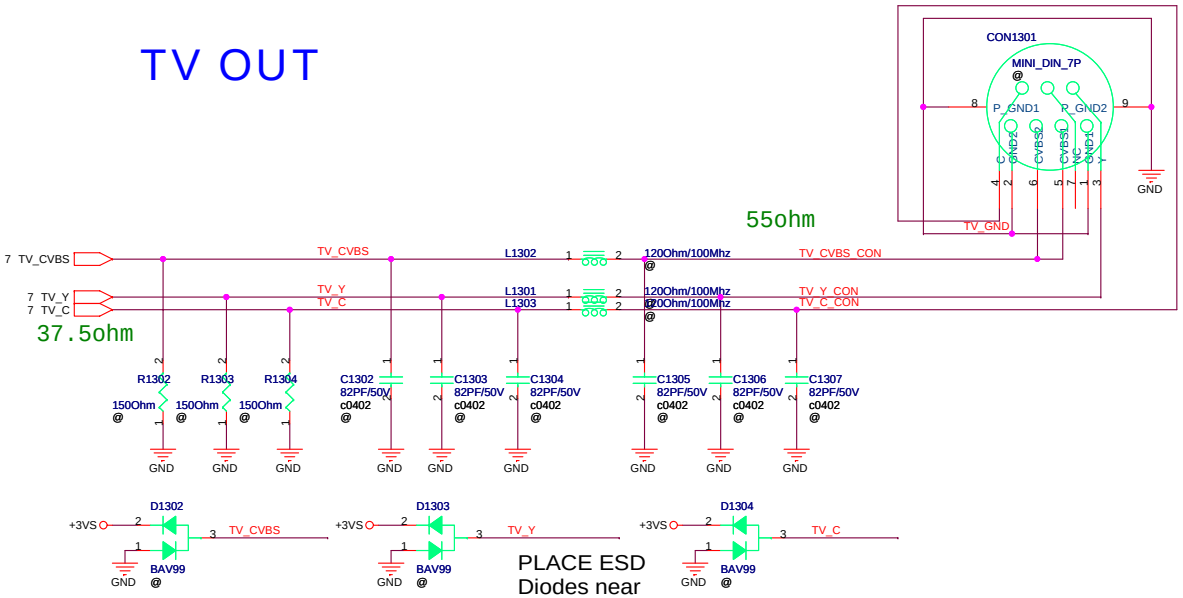



700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

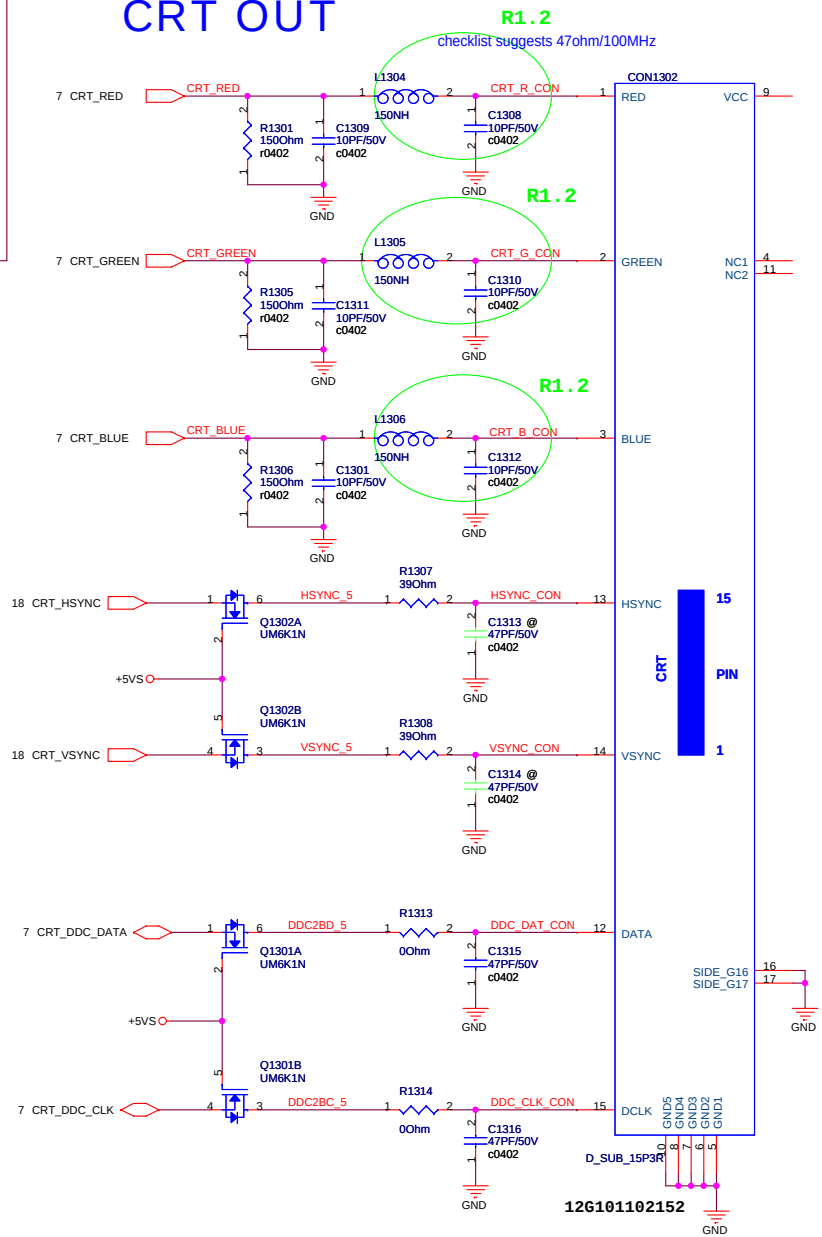
<Variant Name>

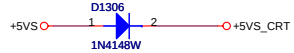
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : LVDS & INVERTER | |
| | Engineer: Leon and George | |
| Size: A3 | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 12 of 61 | |

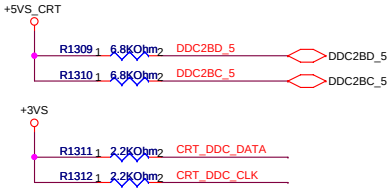
# TV OUT

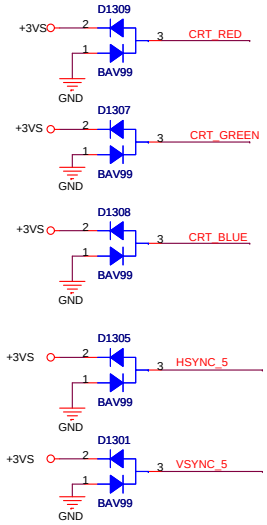



# CRT OUT



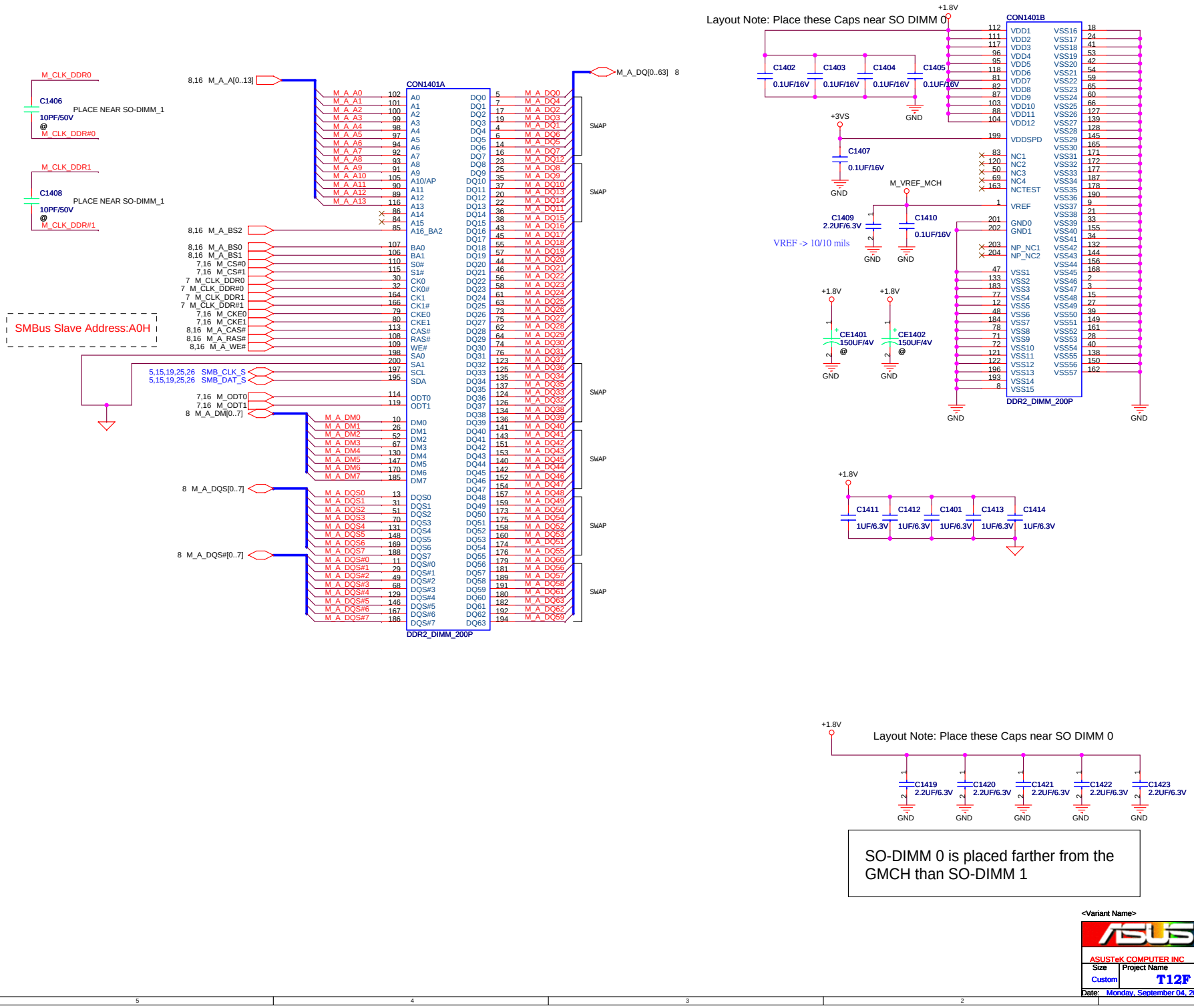




<variant_name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CRT & TV OUT | |
| | Engineer: Leon and George | |
| Size: A3 | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 13 of 61 | |




<variant_name>

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM0

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 14 of 61

SMBus Slave Address:A4H

Address reference +1.8V, add four 0.1uF decoupling CAP.

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these High-Freq decoupling Caps near the GMCH

Layout Note: Place these CAPs near the GMCH

<Variant Name>

Title : DDR2 SO-DIMM1

Engineer: Leon and George

ASUSTeK COMPUTER INC

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

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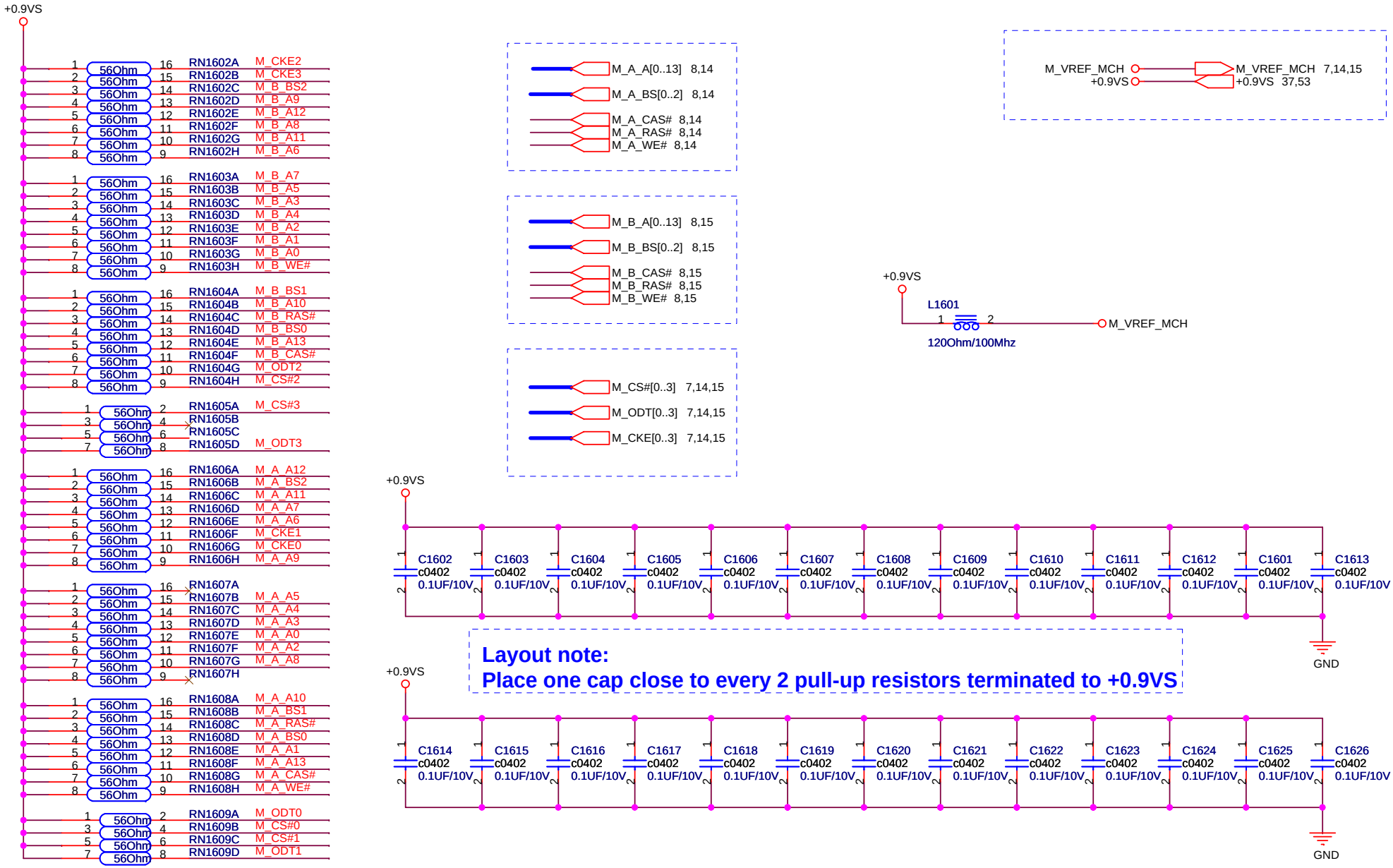



<Variant Name>

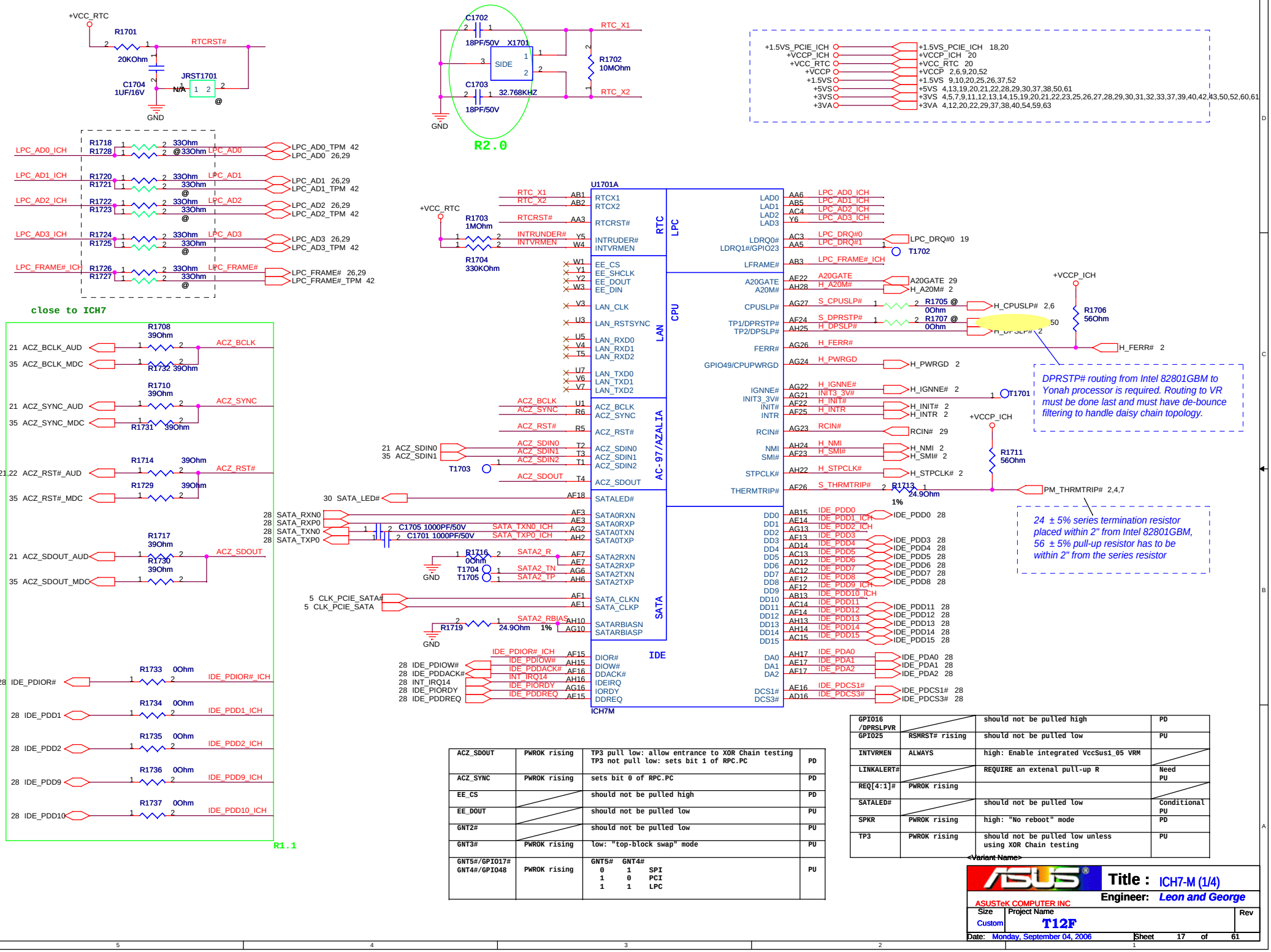
ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 16 of 61




| | | | |
|---|---|---|---|
| ACZ_SDOUT | PWROK rising | TP3 pull low: allow entrance to XOR Chain testing<br>TP3 not pull low: sets bit 1 of RPC.PC | PD |
| ACZ_SYNC | PWROK rising | sets bit 0 of RPC.PC | PD |
| EE_CS | | should not be pulled high | PD |
| EE_DOUT | | should not be pulled low | PU |
| GNT2# | | should not be pulled low | PU |
| GNT3# | PWROK rising | low: "top-block swap" mode | PU |
| GNT5#/GPIO17#<br>GNT4#/GPIO48 | PWROK rising | GNT5# GNT4#<br>0 1 SPI<br>1 0 PCI<br>1 1 LPC | PU |

| | | | |
|---|---|---|---|
| GPIO16<br>/DPRSLPVR | | should not be pulled high | PD |
| GPIO25 | RSMRST# rising | should not be pulled low | PU |
| INTVRMEN | ALWAYS | high: Enable integrated VccSus1_05 VRM | |
| LINKALERT# | | REQUIRE an extenal pull-up R | Need PU |
| REQ[4:1]# | PWROK rising | | |
| SATALED# | | should not be pulled low | Conditional PU |
| SPKR | PWROK rising | high: "No reboot" mode | PD |
| TP3 | PWROK rising | should not be pulled low unless using XOR Chain testing | PU |

<Variant Name>

Title : ICH7-M (1/4)

Engineer: Leon and George

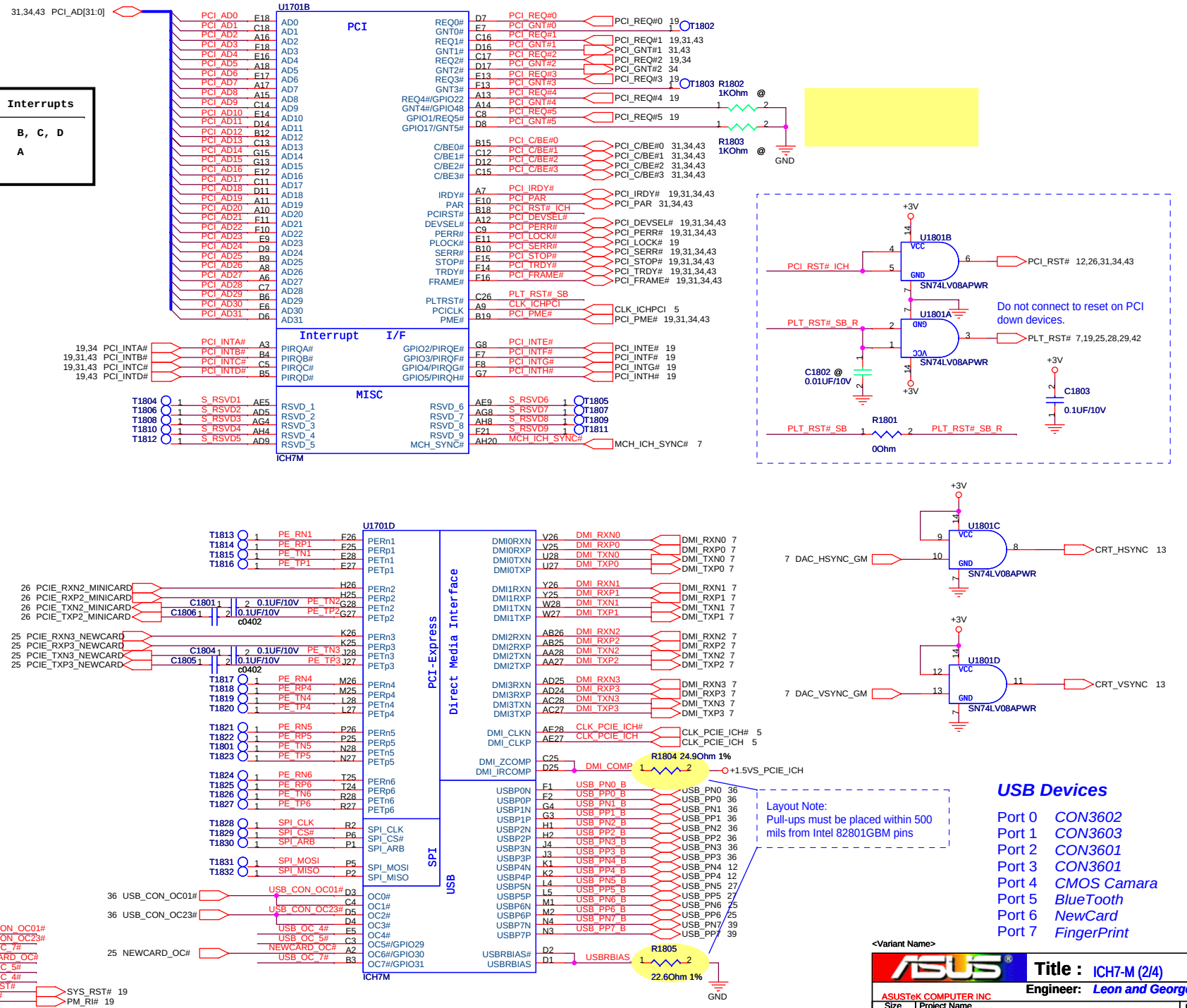
ASUSTeK COMPUTER INC

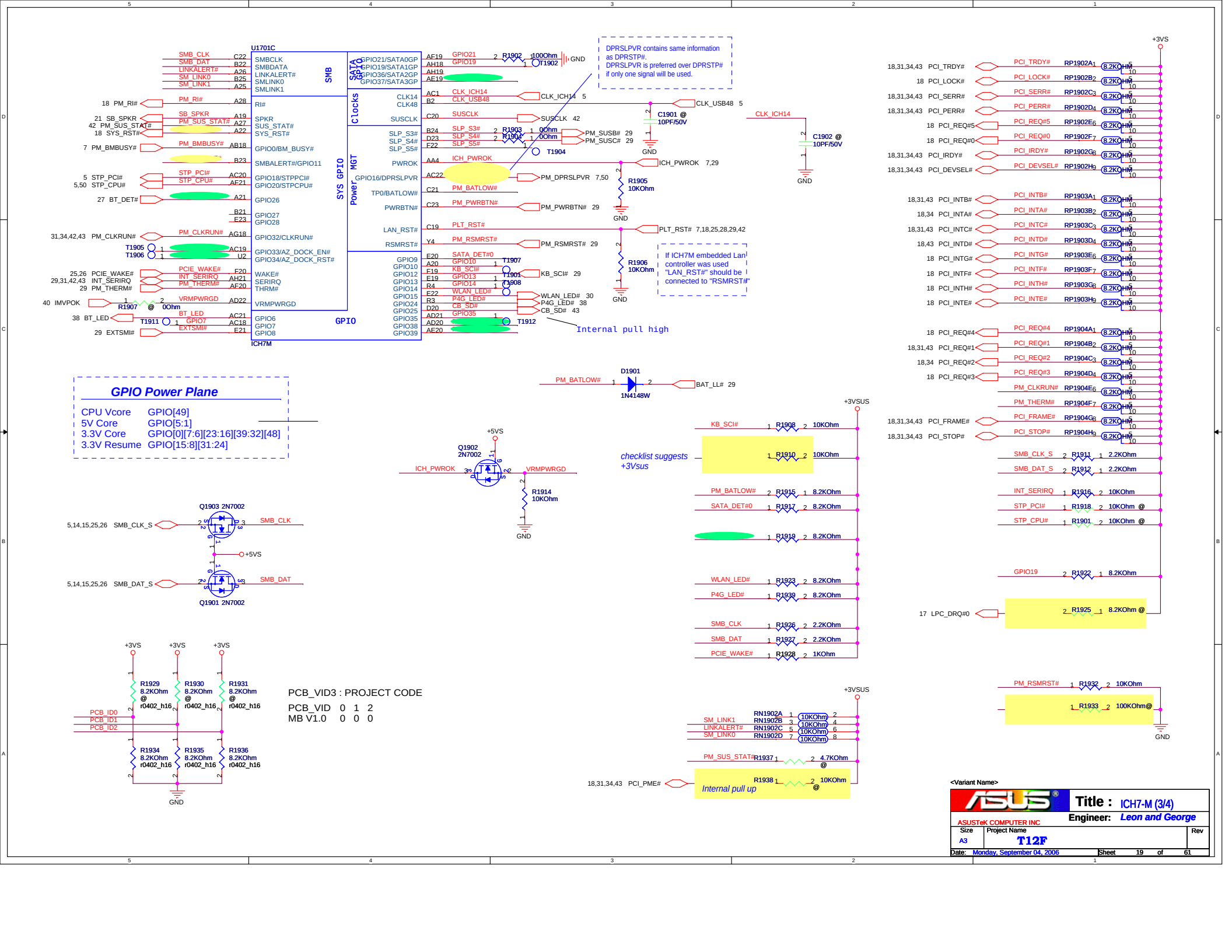
| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

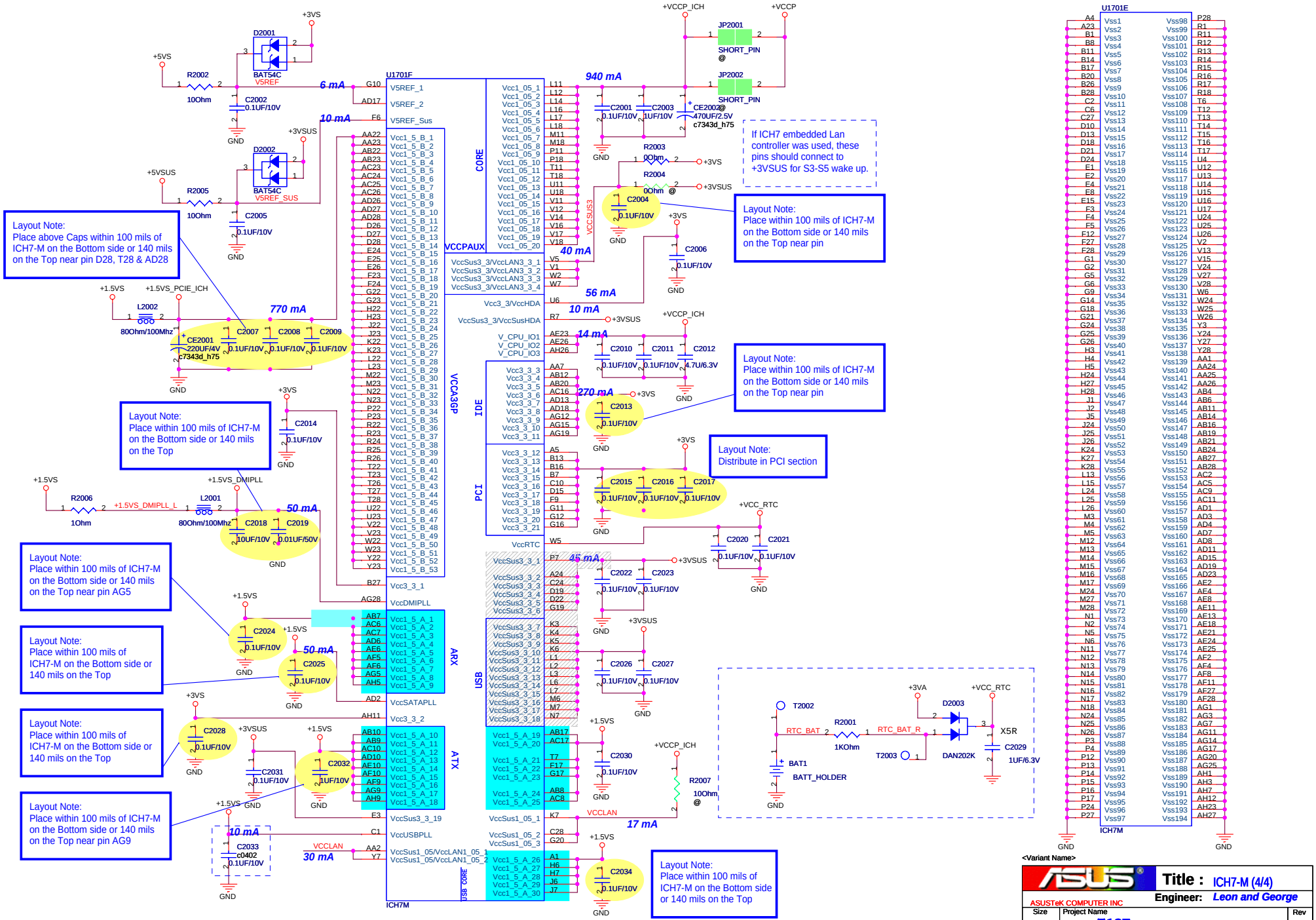
Date: Monday, September 04, 2006 Sheet 17 of 61

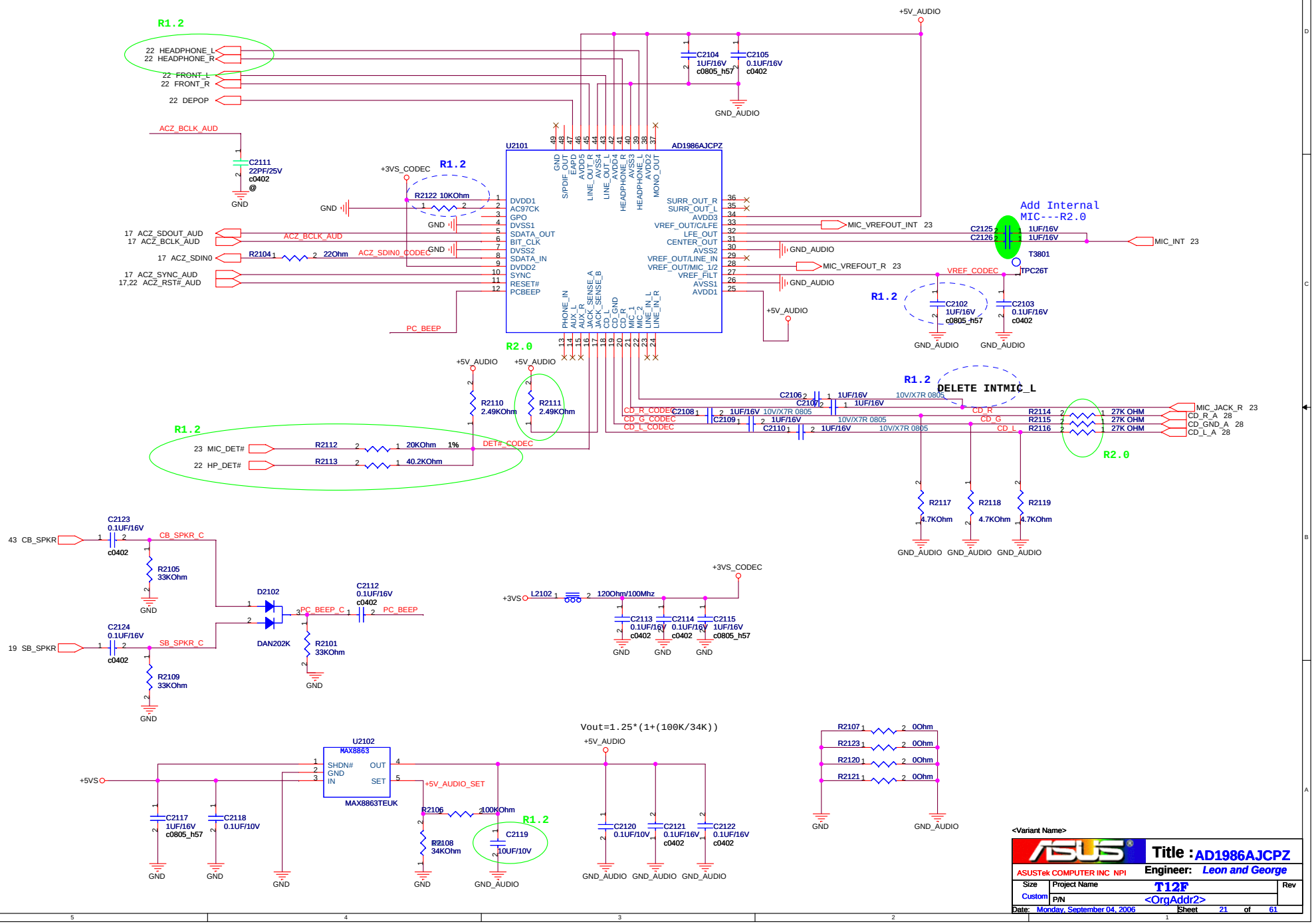
## PCI Device

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|---|---|---|---|
| CardBus | AD17 | REQ1#/GNT1# | B, C, D |
| LAN | AD23 | REQ2#/GNT2# | A |




U1701C
SMB
SATA
Clocks
SYS GPIO
Power MGT
GPIO
ICH7M
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
SB_SPKR
PM_SUS_STAT#
SYS_RST#
PM_BMBUSY#
STP_PCI#
STP_CPU#
BT_DET#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#
IMVPOK
VRMPWRGD
BT_LED
EXTSMI#
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
CLK_ICH14
CLK_USB48
PM_SUSB#
PM_SUSC#
ICH_PWROK
PM_DPRSLPVR
PM_BATLOW#
PM_PWRBTN#
PLT_RST#
PM_RSMRST#
SATA_DET#0
KB_SCI#
WLAN_LED#
P4G_LED#
CB_SD#
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
Internal pull high
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
D1901
1N4148W
PM_BATLOW#
BAT_LL#
Q1902
2N7002
ICH_PWROK
VRMPWRGD
Q1903 2N7002
Q1901 2N7002
SMB_CLK_S
SMB_DAT_S
checklist suggests +3Vsus
PCB_ID0
PCB_ID1
PCB_ID2
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
PCI_PME#
Internal pull up
PCI_TRDY#
PCI_LOCK#
PCI_SERR#
PCI_PERR#
PCI_REQ#5
PCI_REQ#0
PCI_IRDY#
PCI_DEVSEL#
PCI_INTB#
PCI_INTA#
PCI_INTC#
PCI_INTD#
PCI_INTG#
PCI_INTF#
PCI_INTH#
PCI_INTE#
PCI_REQ#4
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PM_CLKRUN#
PM_THERM#
PCI_FRAME#
PCI_STOP#
SMB_CLK_S
SMB_DAT_S
INT_SERIRQ
STP_PCI#
STP_CPU#
GPIO19
LPC_DRQ#0
PM_RSMRST#
Variant Name
Title : ICH7-M (3/4)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size A3
Project Name T12F
Rev
Date: Monday, September 04, 2006
Sheet 19 of 61


U1701F
U1701E
ICH7M
D2001
BAT54C
V5REF
D2002
BAT54C
V5REF_SUS
JP2001
SHORT_PIN
@
JP2002
SHORT_PIN
CE2002@
470UF/2.5V
c7343d_h75
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note: Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Distribute in PCI section
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
Layout Note: Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ARX
ATX
SUS
940 mA
6 mA
10 mA
40 mA
56 mA
14 mA
270 mA
770 mA
50 mA
45 mA
17 mA
30 mA
VCCSUS3
VCCLAN
Title : ICH7-M (4/4)
Engineer: Leon and George
ASUSTeK COMPUTER INC
Size A3
Project Name T12F
Rev
Date: Monday, September 04, 2006
Sheet 20 of 61


R1.2
22 HEADPHONE_L
22 HEADPHONE_R
22 FRONT_L
22 FRONT_R
22 DEPOP
+5V_AUDIO
C2104 1UF/16V c0805_h57
C2105 0.1UF/16V c0402
GND_AUDIO
ACZ_BCLK_AUD
C2111 22PF/25V c0402 @
GND
U2101
AD1986AJCPZ
+3VS_CODEC
R2122 10KOhm
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
17 ACZ_SDIN0
R2104 22Ohm
ACZ_SDIN0_CODEC
17 ACZ_SYNC_AUD
17,22 ACZ_RST#_AUD
PC_BEEP
DVDD1
AC97CK
GPO
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PCBEEP
SURR_OUT_R
SURR_OUT_L
AVDD3
VREF_OUT/C/LFE
LFE_OUT
CENTER_OUT
AVSS2
VREF_OUT/LINE_IN
VREF_OUT/MIC_1/2
VREF_FILT
AVSS1
AVDD1
MIC_VREFOUT_INT 23
MIC_VREFOUT_R 23
GND_AUDIO
Add Internal MIC---R2.0
C2125 1UF/16V
C2126 1UF/16V
MIC_INT 23
T3801
TPC26T
VREF_CODEC
C2102 1UF/16V c0805_h57
C2103 0.1UF/16V c0402
R2.0
R2110 2.49KOhm
R2111 2.49KOhm
23 MIC_DET#
22 HP_DET#
R2112 20KOhm 1%
R2113 40.2KOhm
DET#_CODEC
DELETE INTMIC_L
C2106 1UF/16V 10V/X7R 0805
C2107 1UF/16V
C2108 1UF/16V 10V/X7R 0805
C2109 1UF/16V 10V/X7R 0805
C2110 1UF/16V 10V/X7R 0805
CD_R_CODEC
CD_G_CODEC
CD_L_CODEC
CD_R
CD_G
CD_L
R2114 27K OHM
R2115 27K OHM
R2116 27K OHM
MIC_JACK_R 23
CD_R_A 28
CD_GND_A 28
CD_L_A 28
R2117 4.7KOhm
R2118 4.7KOhm
R2119 4.7KOhm
43 CB_SPKR
19 SB_SPKR
C2123 0.1UF/16V c0402
C2124 0.1UF/16V c0402
CB_SPKR_C
SB_SPKR_C
R2105 33KOhm
R2109 33KOhm
D2102
DAN202K
PC_BEEP_C
C2112 0.1UF/16V c0402
PC_BEEP
R2101 33KOhm
+3VS
L2102 120Ohm/100Mhz
C2113 0.1UF/16V c0402
C2114 0.1UF/16V c0402
C2115 1UF/16V c0805_h57
U2102
MAX8863
MAX8863TEUK
SHDN#
GND
IN
OUT
SET
+5VS
+5V_AUDIO_SET
Vout=1.25*(1+(100K/34K))
R2106 100KOhm
R2108 34KOhm
C2119 10UF/10V
C2117 1UF/16V c0805_h57
C2118 0.1UF/10V
C2120 0.1UF/10V
C2121 0.1UF/16V c0402
C2122 0.1UF/16V c0402
R2107 0Ohm
R2123 0Ohm
R2120 0Ohm
R2121 0Ohm
<Variant Name>
Title : AD1986AJCPZ
ASUSTek COMPUTER INC NPI
Engineer: Leon and George
Size Custom
Project Name T12F
P/N <OrgAddr2>
Rev
Date: Monday, September 04, 2006
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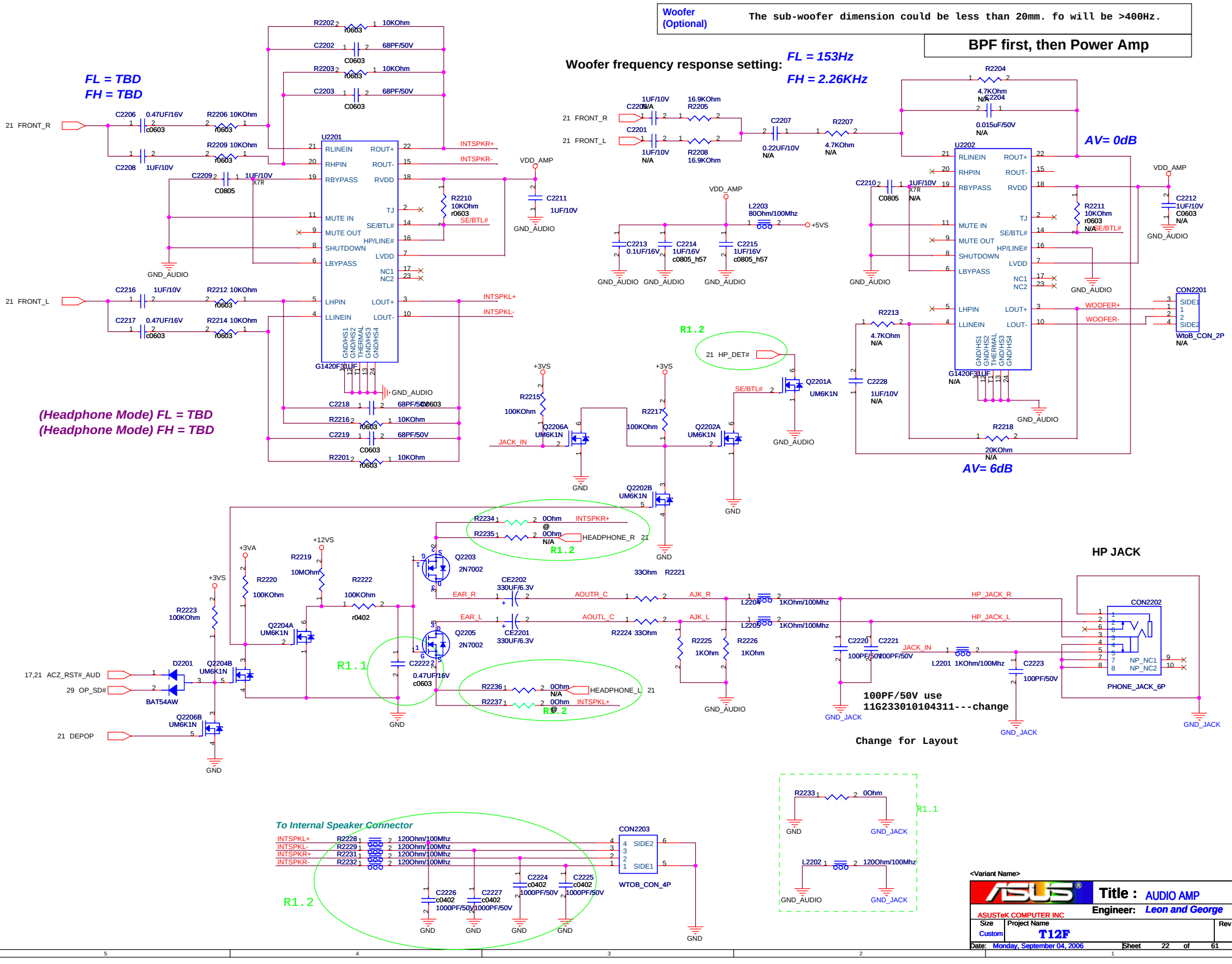
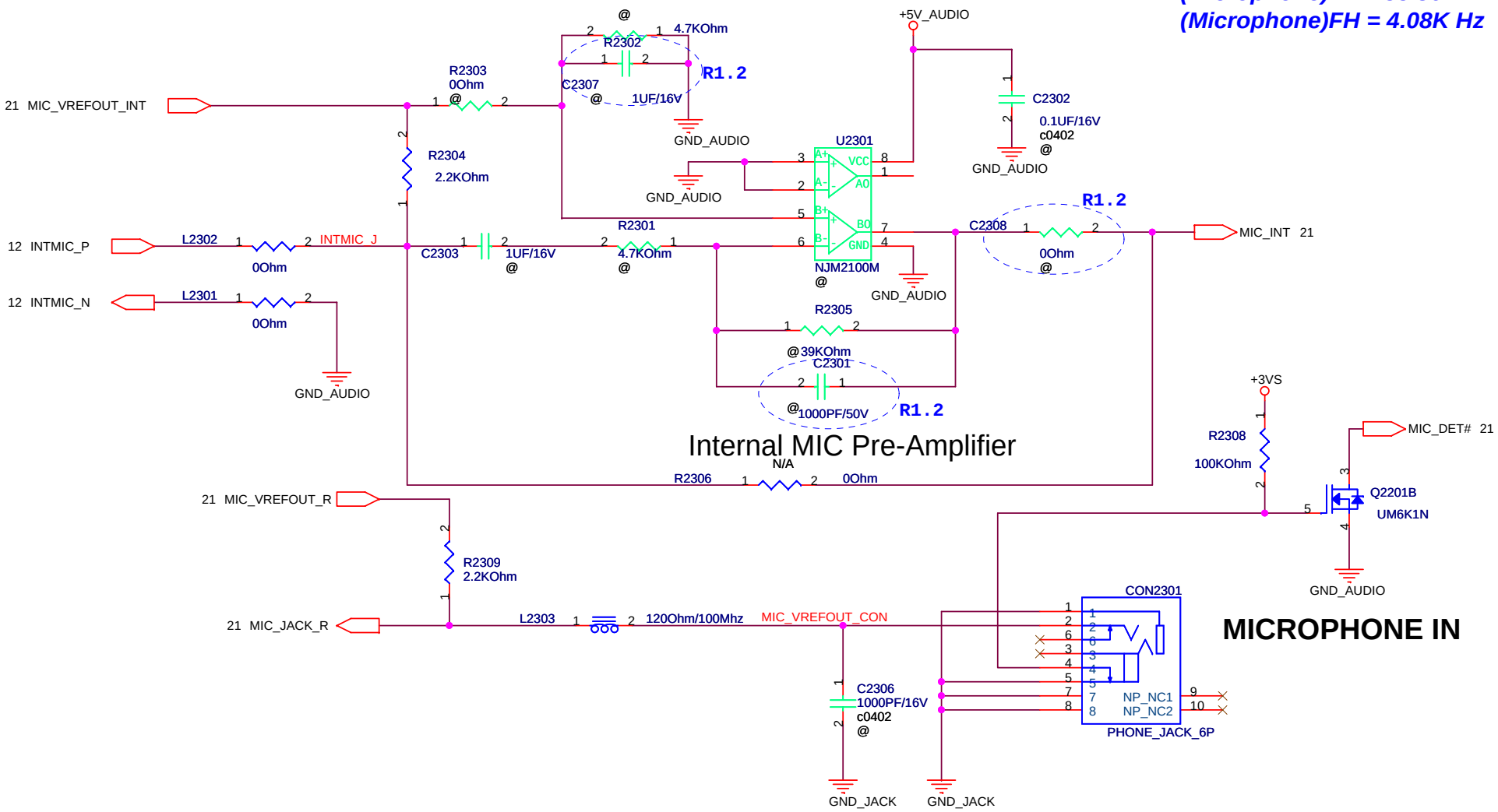

Woofer (Optional)
The sub-woofer dimension could be less than 20mm. fo will be >400Hz.
BPF first, then Power Amp
Woofer frequency response setting:
FL = 153Hz
FH = 2.26KHz
FL = TBD
FH = TBD
(Headphone Mode) FL = TBD
(Headphone Mode) FH = TBD
AV= 0dB
AV= 6dB
HP JACK
100PF/50V use 11G2330101043 11---change
Change for Layout
To Internal Speaker Connector
R1.1
R1.2
U2201
U2202
G1420F31UF
CON2201
CON2202
CON2203
WTOB_CON_4P
PHONE_JACK_6P
Title : AUDIO AMP
Engineer: Leon and George
ASUSTeK COMPUTER INC
Project Name T12F
Size Custom
Rev
Date: Monday, September 04, 2006
Sheet 22 of 61




<Variant Name>

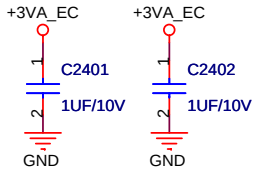
ASUSTeK COMPUTER INC

Title : MIC Pre-AMP

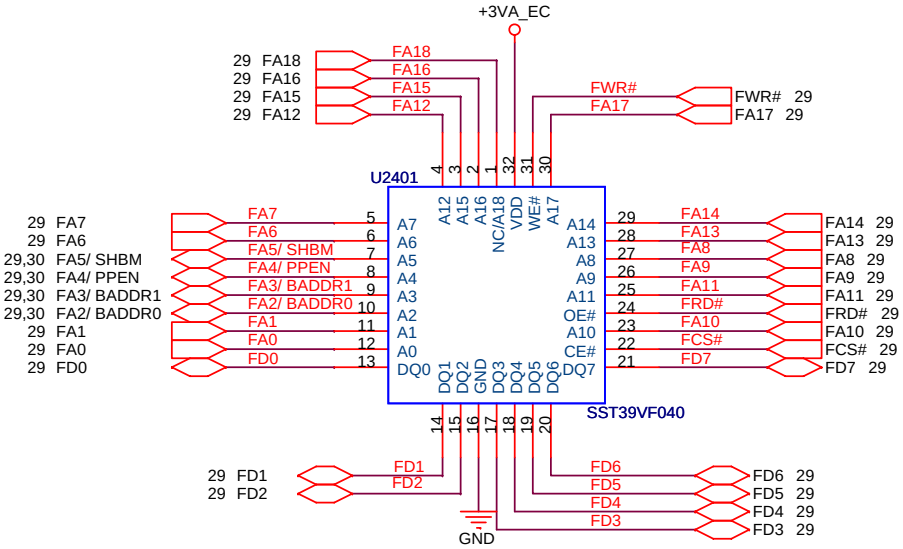
Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 23 of 61




# ISA ROM




<Variant Name>

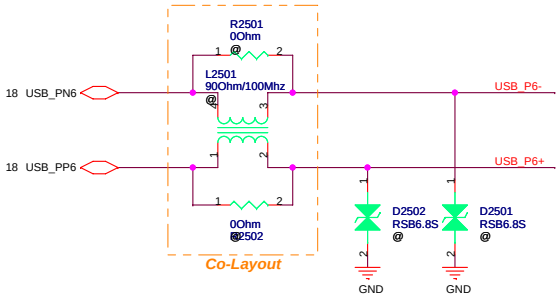
ASUSTeK COMPUTER INC

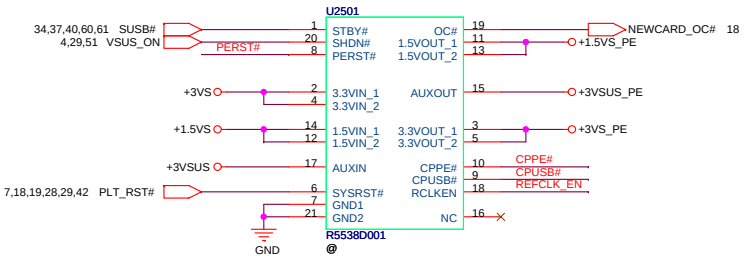
Title : ISA ROM

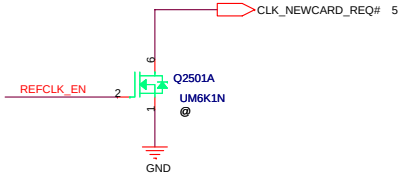
Engineer: Leon and George

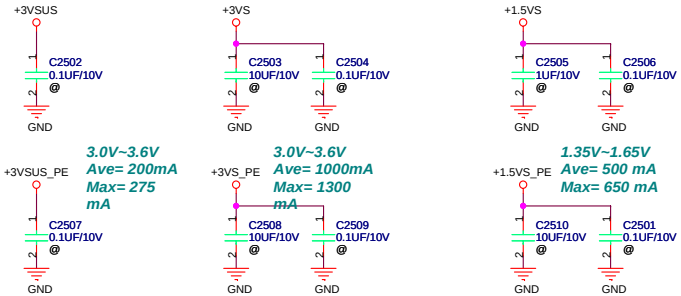
| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 24 of 61



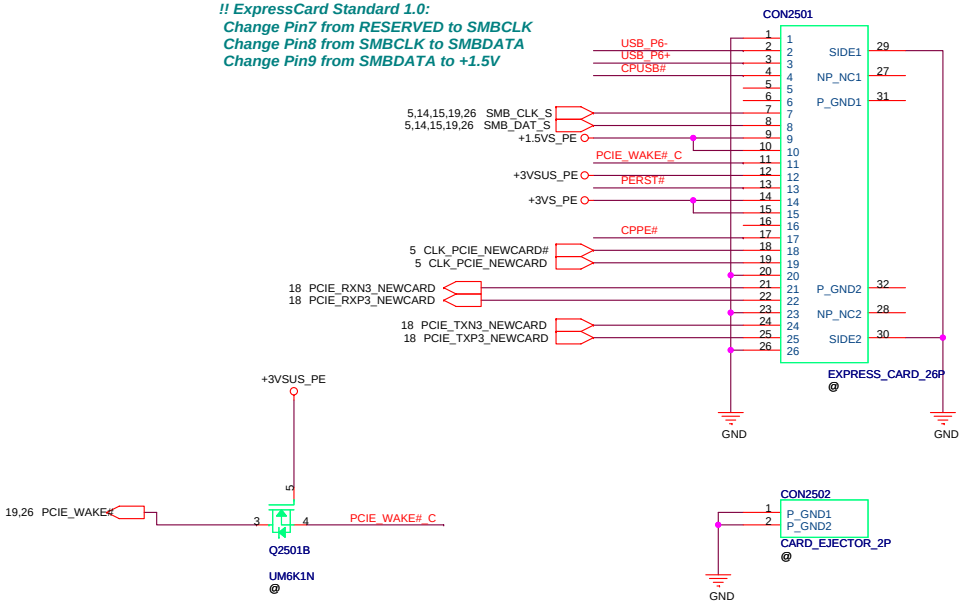




*!! ExpressCard Standard 1.0:*
*Change Pin7 from RESERVED to SMBCLK*
*Change Pin8 from SMBCLK to SMBDATA*
*Change Pin9 from SMBDATA to +1.5V*

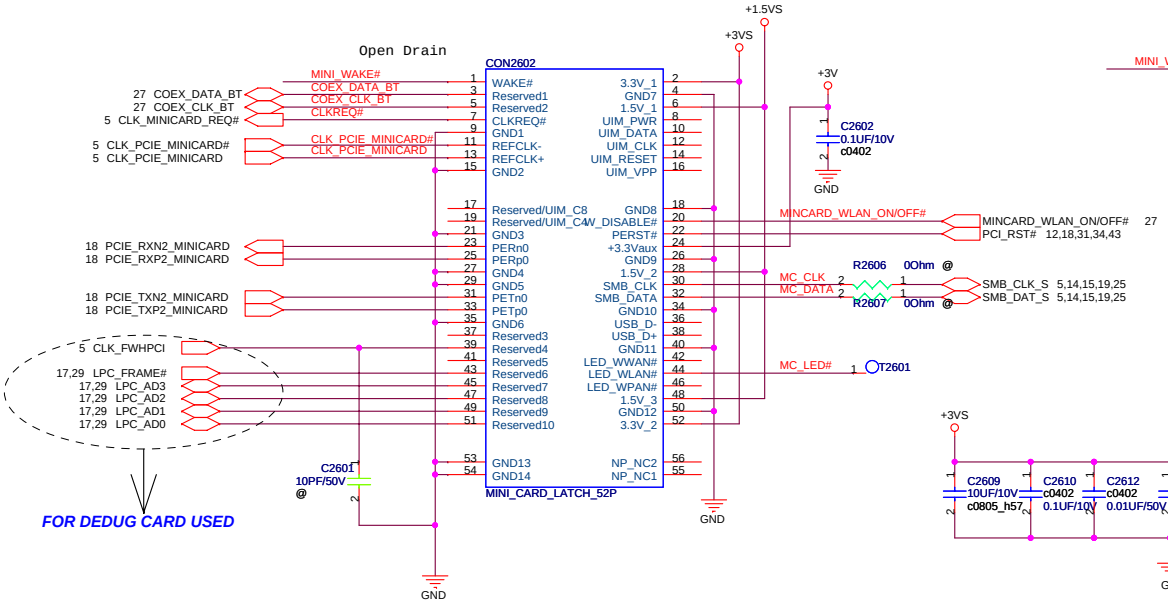
*NewCard Header*

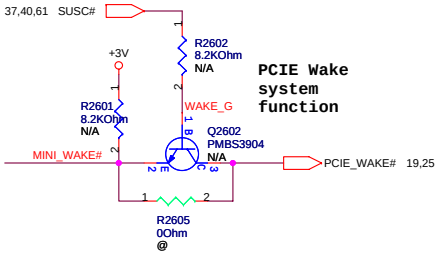


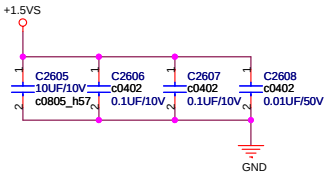

<variant_name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB1 | Title : NEWCARD | |
| | Engineer: Leon and George | |
| Size: Custom | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 25 of 61 | |

# MINI PCIEX CONNECTOR



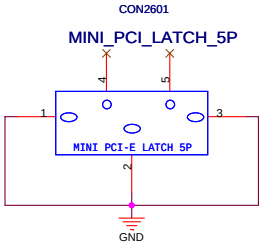



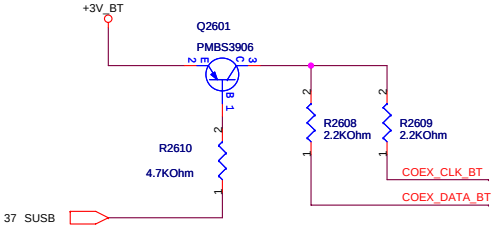


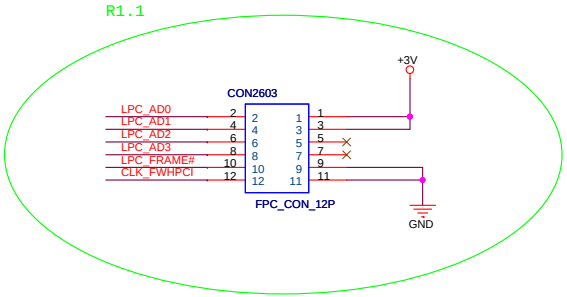


**+3V : 1000 mA(peak)**
**+1.5V: 500mA(peak)**
**+3VSUS: 330mA(peak)**

**Check O/D output or push pull**



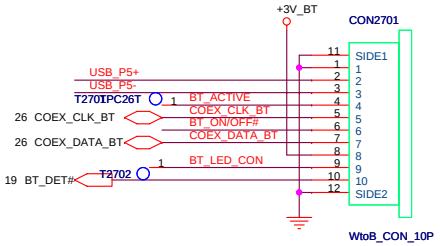



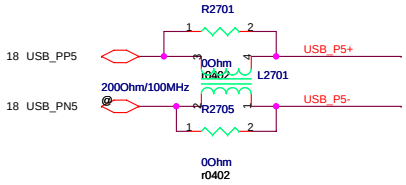




<variant_name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : MINI PCIEX | |
| | Engineer: Leon and George | |
| Size: A3 | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 26 of 61 | |

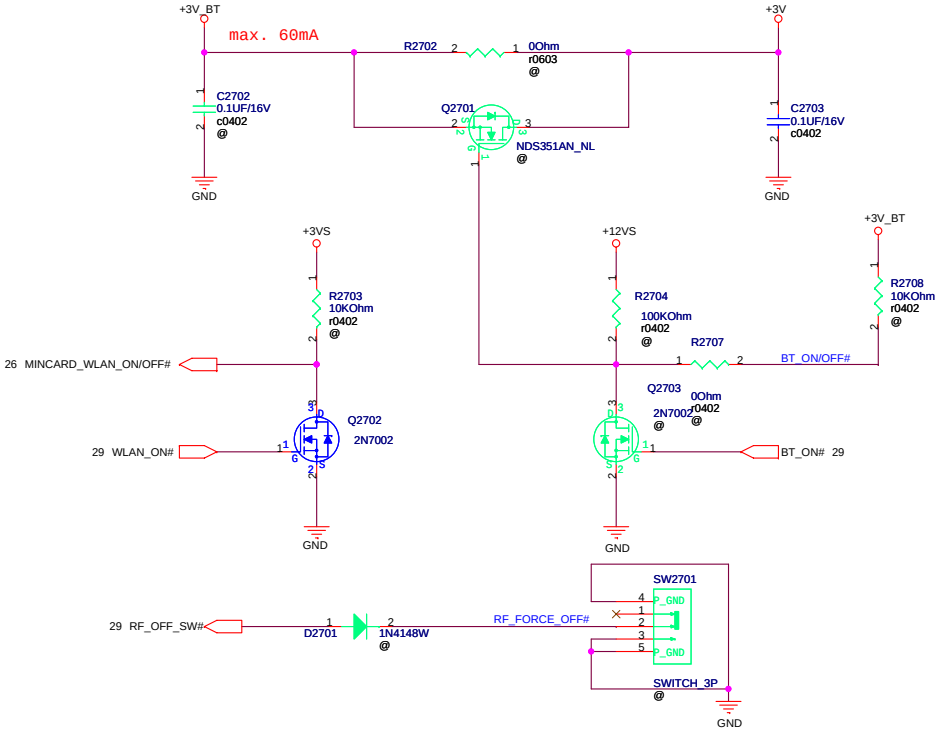
## For Bluetooth



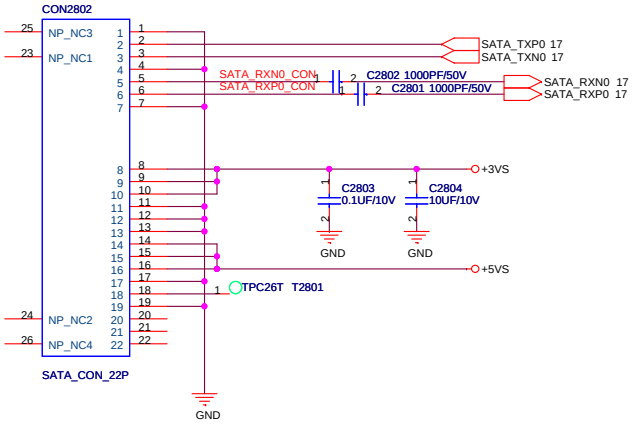

## For Side SW

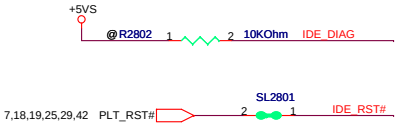
## WLAN/BT ON/OFF Control

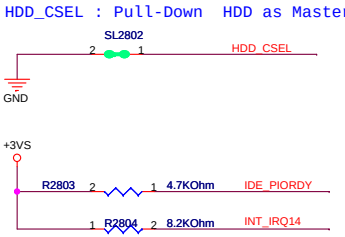


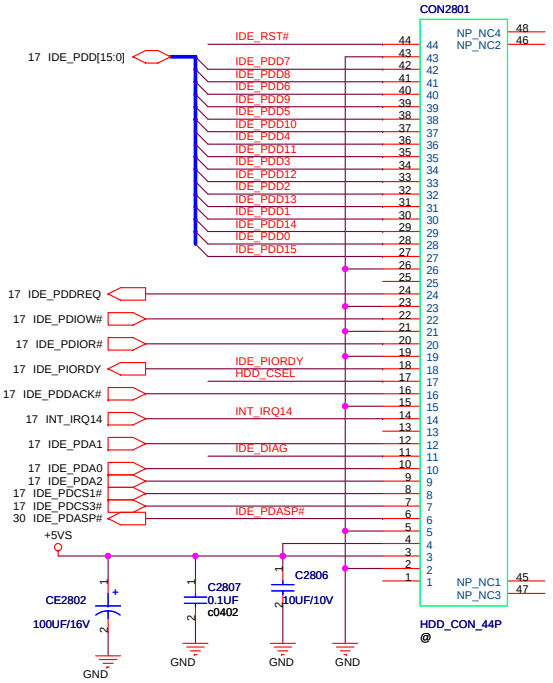

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Blue Tooth | |
| | Engineer: Leon and George | |
| Size: Custom | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 27 of 61 | |



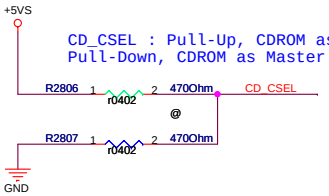



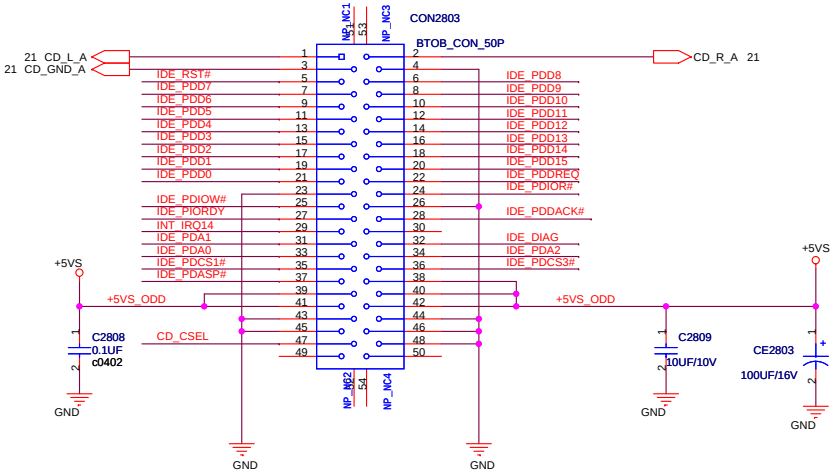




# SATA HDD

# PATA HDD

# CD-ROM




<variant_name>

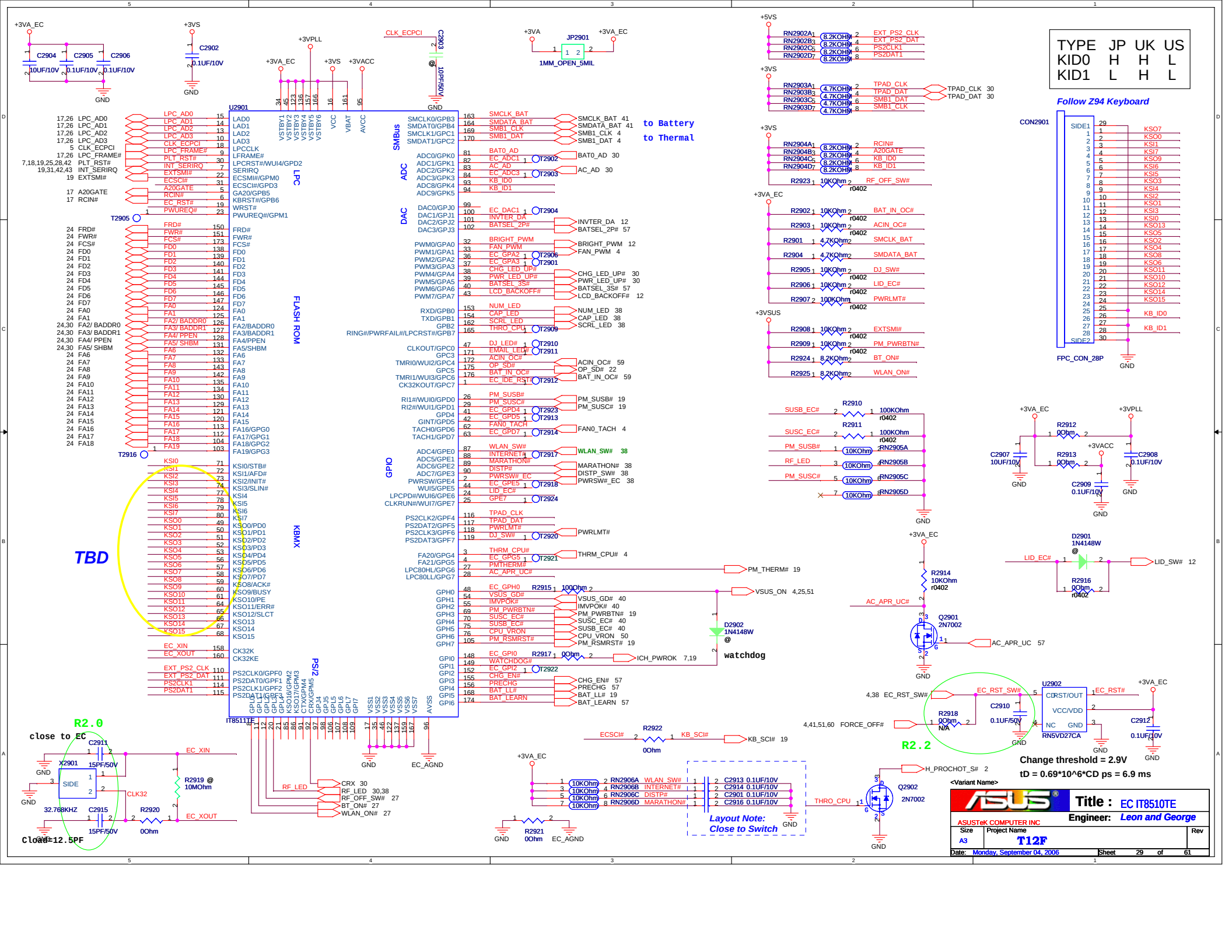
ASUSTeK COMPUTER INC. NB1

Title : PATA-SATA & ODD

Engineer:

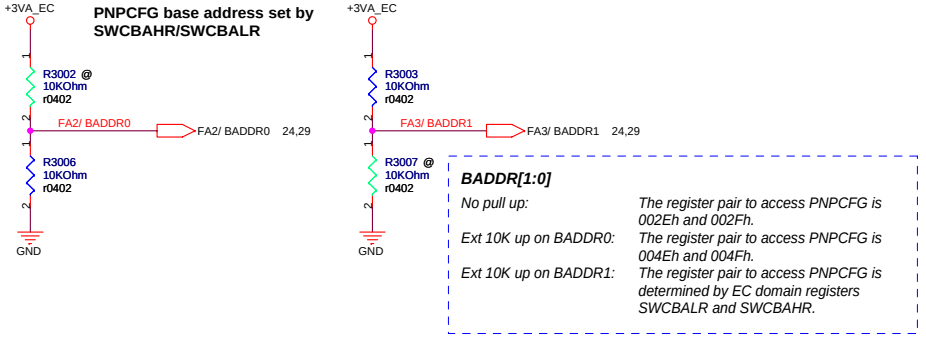
| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 28 of 61


TYPE JP UK US
KID0 H H L
KID1 L H L
Follow Z94 Keyboard
U2901
IT8511TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
TBD
R2.0
close to EC
Cload=12.5PF
R2.2
watchdog
Layout Note:
Close to Switch
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
Title : EC IT8510TE
Engineer: Leon and George
ASUSTeK COMPUTER INC
Project Name T12F
Size A3
Rev
Date: Monday, September 04, 2006
Sheet 29 of 61

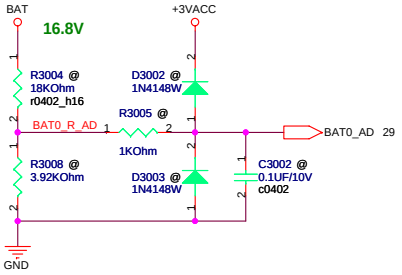
# EC Hardware Strap

*Strap value sampled after VSTBY power up reset*

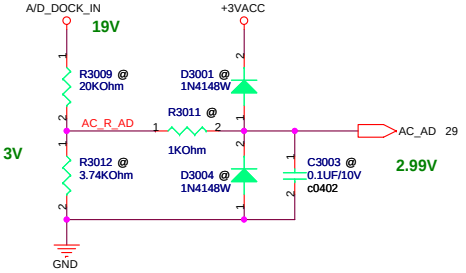



## EC ADC

### Battery



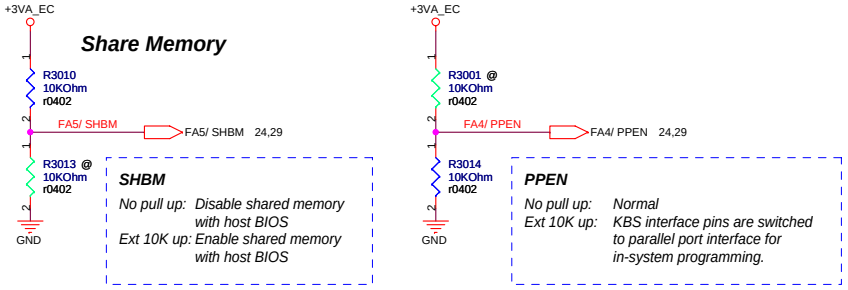

### Adaptor

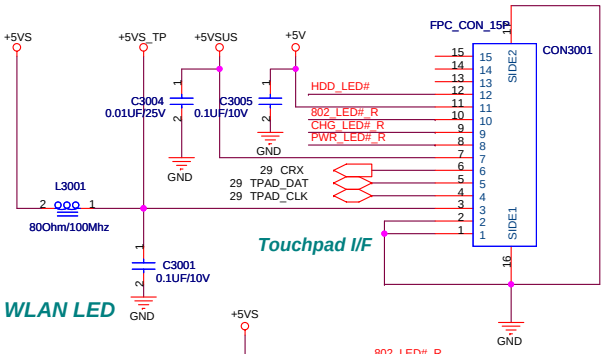



3V

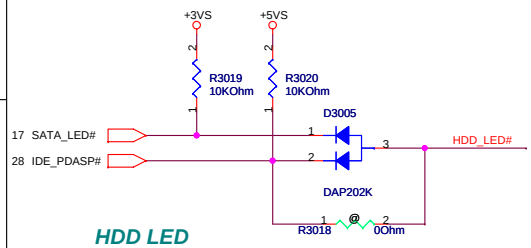
2.99V

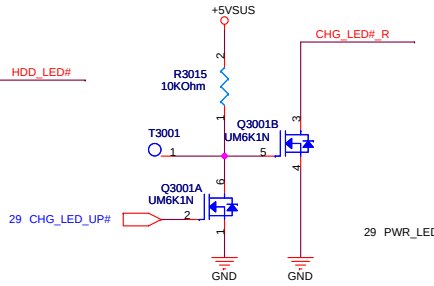
### Share Memory

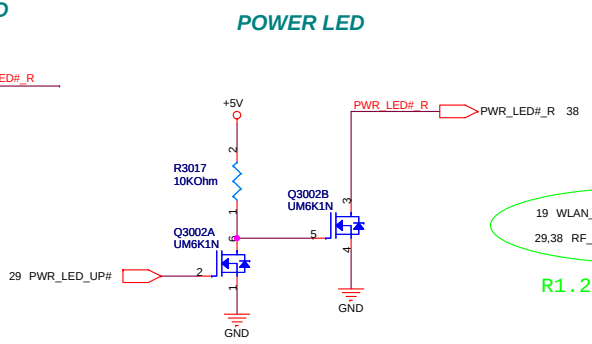



# Touchpad





R1.2




<Variant Name>

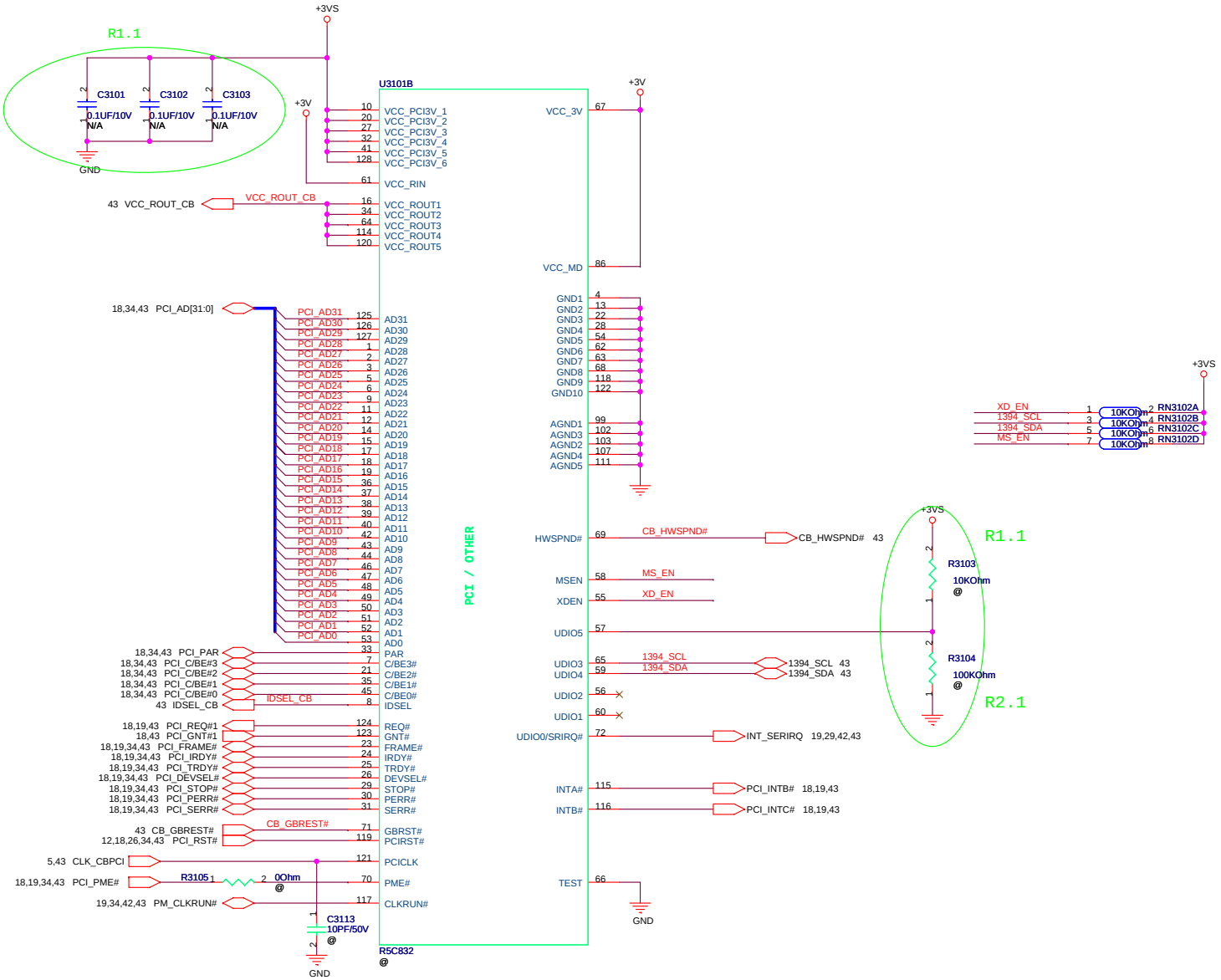
ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

Date: Monday, September 04, 2006 Sheet 30 of 61




<Variant Name>

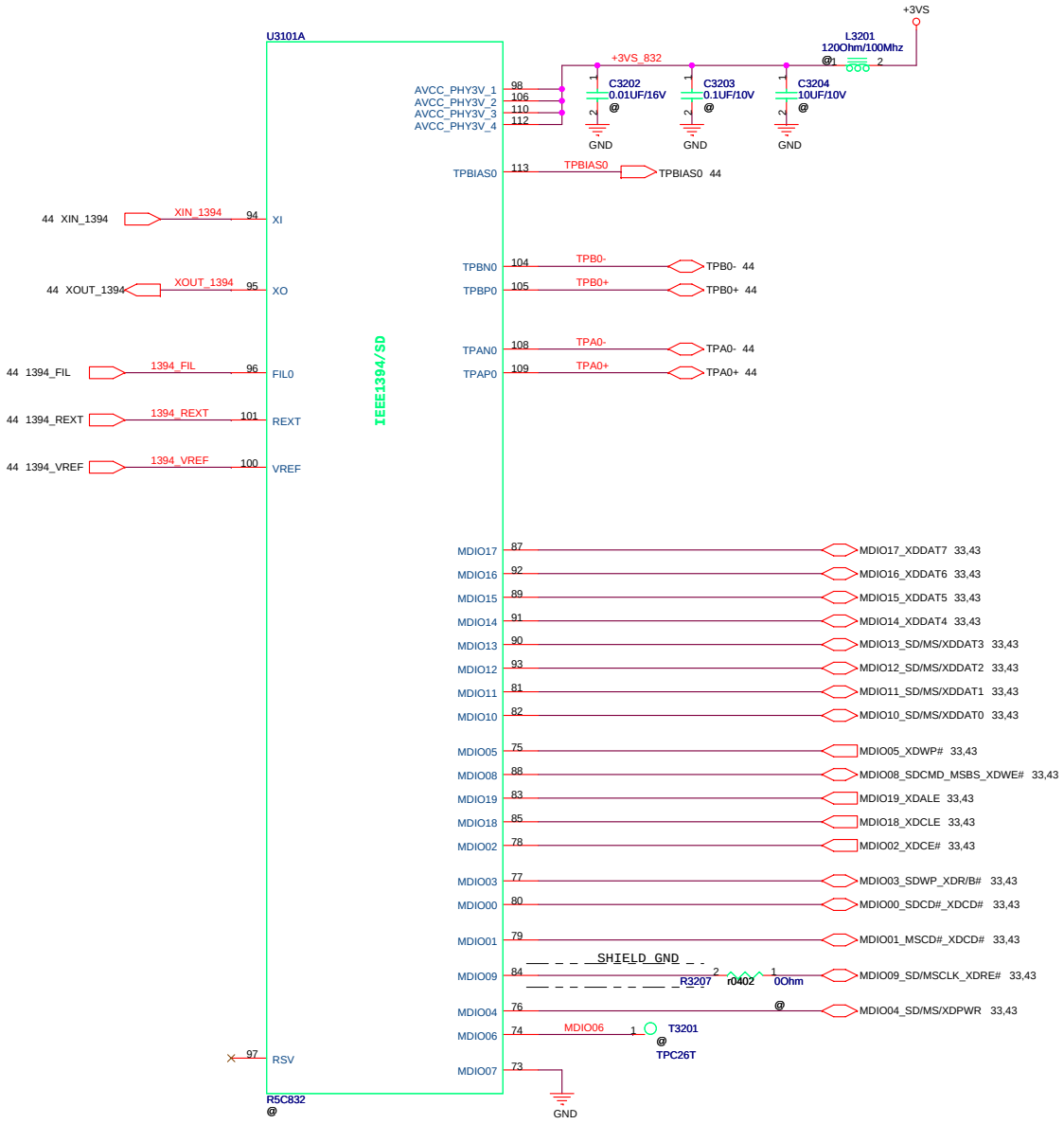
Title : CARD1394-R5C832(1)

ASUSTeK COMPUTER INC. NB1

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 31 of 61




<Variant Name>

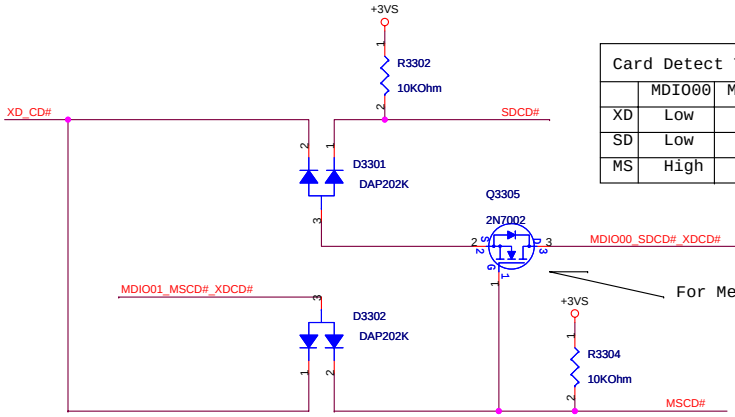
Title : CARD1394-R5C832(2)

ASUSTeK COMPUTER INC. NB1

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

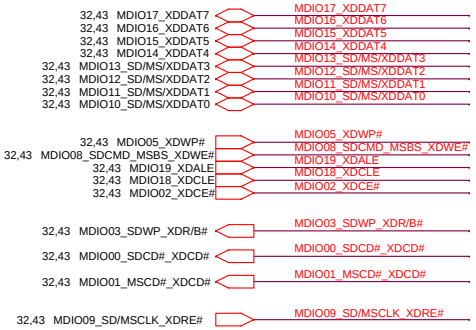
Date: Monday, September 04, 2006 Sheet 32 of 61

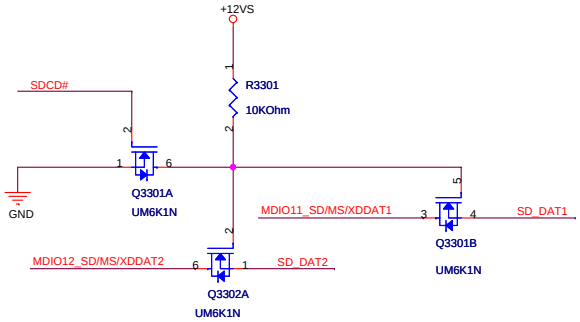



| Card Detect Table | | |
|---|---|---|
| | MDIO00 | MDIO01 |
| XD | Low | Low |
| SD | Low | High |
| MS | High | Low |

For Memory Stick Duo Adaptor shielding ground issue

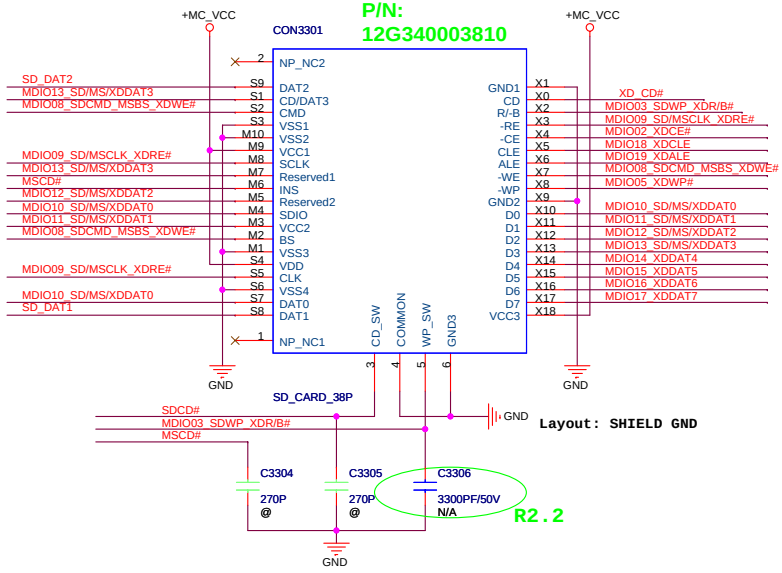
| Name | Drive | Name | Drive |
|---|---|---|---|
| MDIO00 | I - PU | MDIO10 | I/O - PU |
| MDIO01 | I - PU | MDIO11 | I/O - PU |
| MDIO02 | O - PU | MDIO12 | I/O - PU |
| MDIO03 | I - PU | MDIO13 | I/O - PU |
| MDIO04 | O - 3V | MDIO14 | I/O - PU |
| MDIO05 | O - 3V | MDIO15 | I/O - PU |
| MDIO06 | O - 3V | MDIO16 | I/O - PU |
| MDIO07 | I - 3V | MDIO17 | I/O - PU |
| MDIO08 | I/O - PU | MDIO18 | I/O - PU |
| MDIO09 | I/O - PU | MDIO19 | I/O - PU |

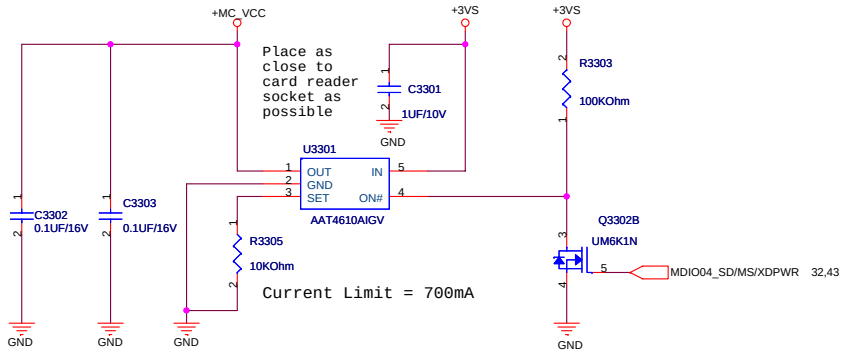



R2.3

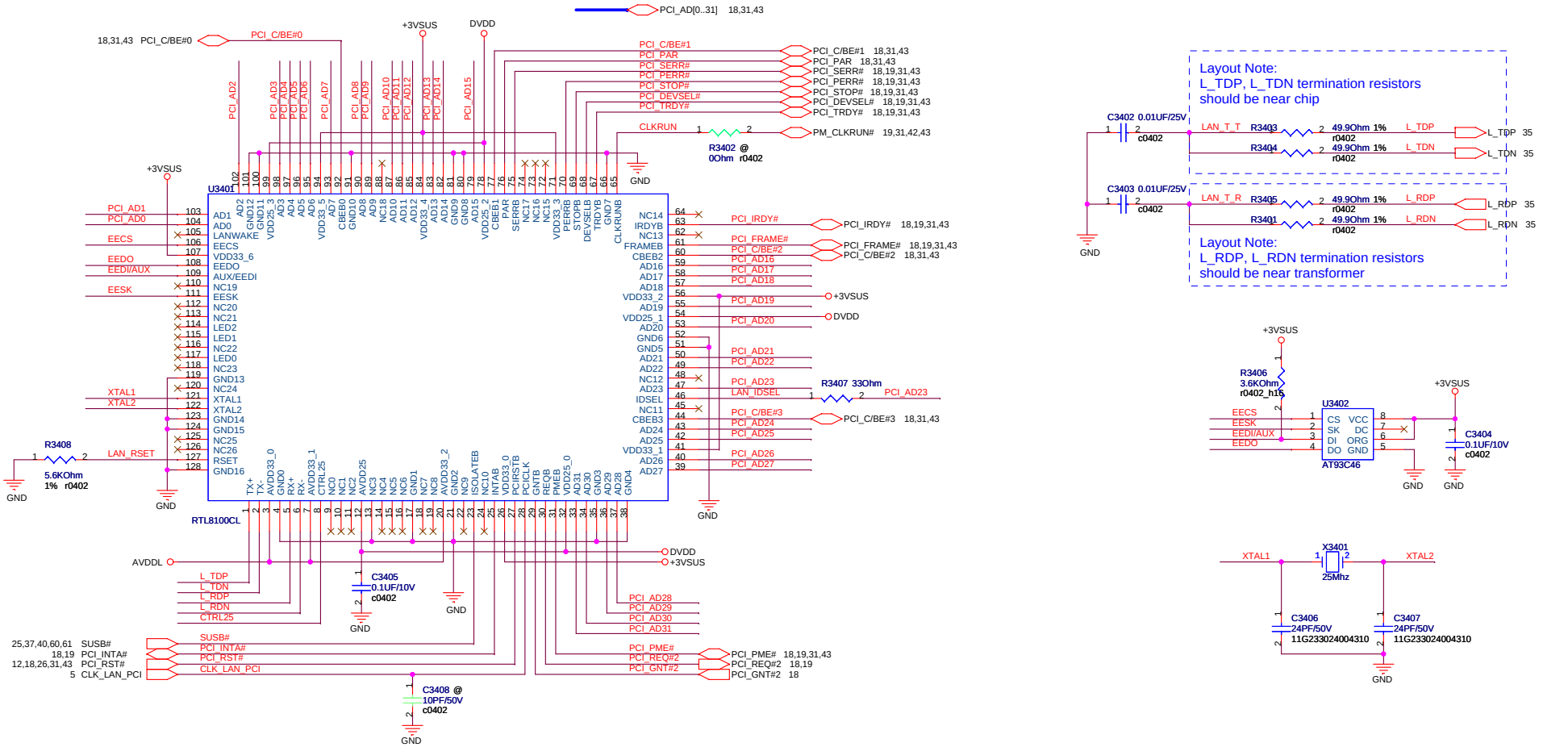
P/N: 12G340003810




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : 4 in 1 CARD READER | |
| | Engineer: Leon and George | |
| Size: A3 | Project Name: T12F | Rev |
| Date: Tuesday, October 17, 2006 | Sheet 33 of 61 | |



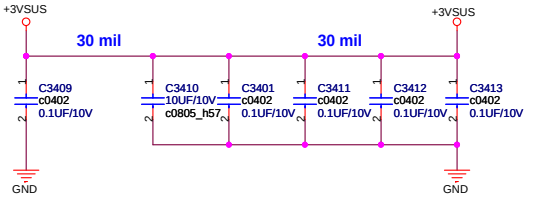


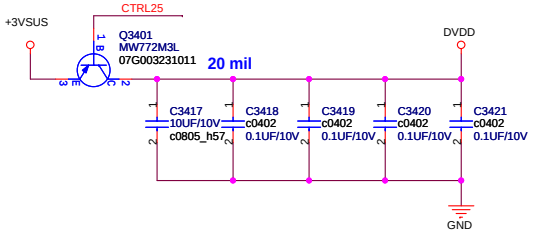


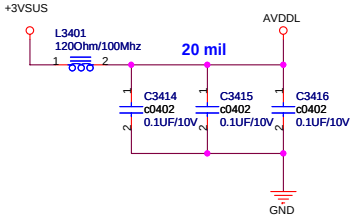








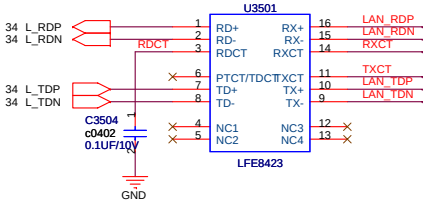



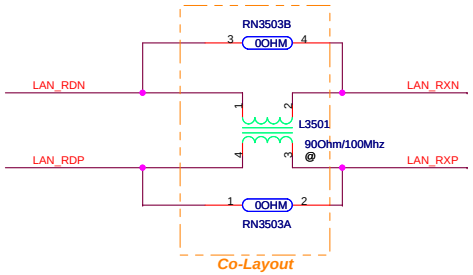



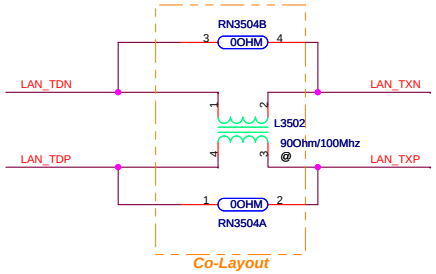

<variant_name>

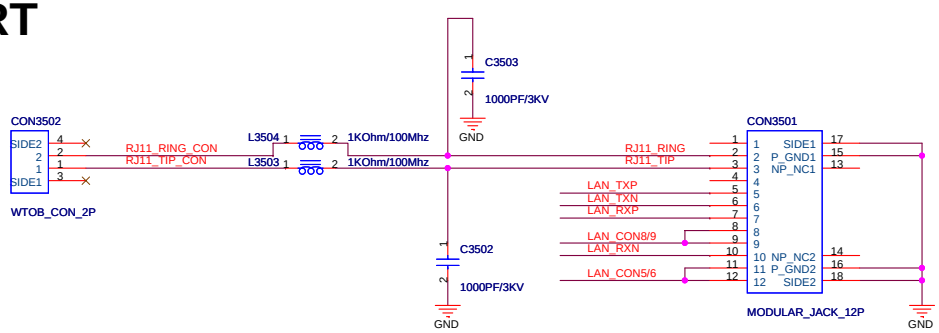
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : LAN_RTL8100CL | |
| | Engineer: Leon and George | |
| Size: A3 | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 34 of 61 | |

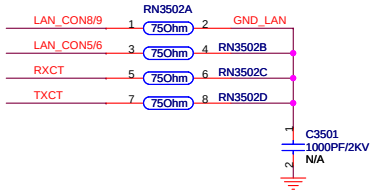
# LAN PORT



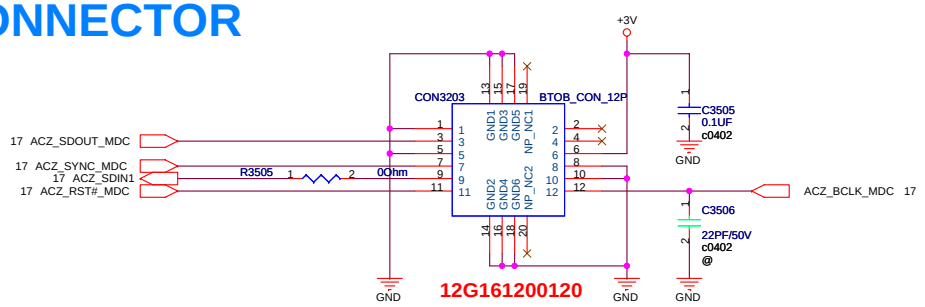



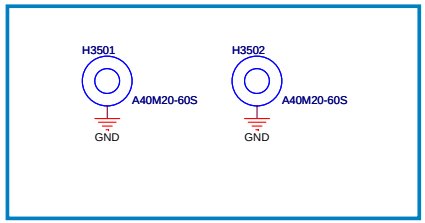




R1.2

# MDC CONNECTOR




<Variant Name>

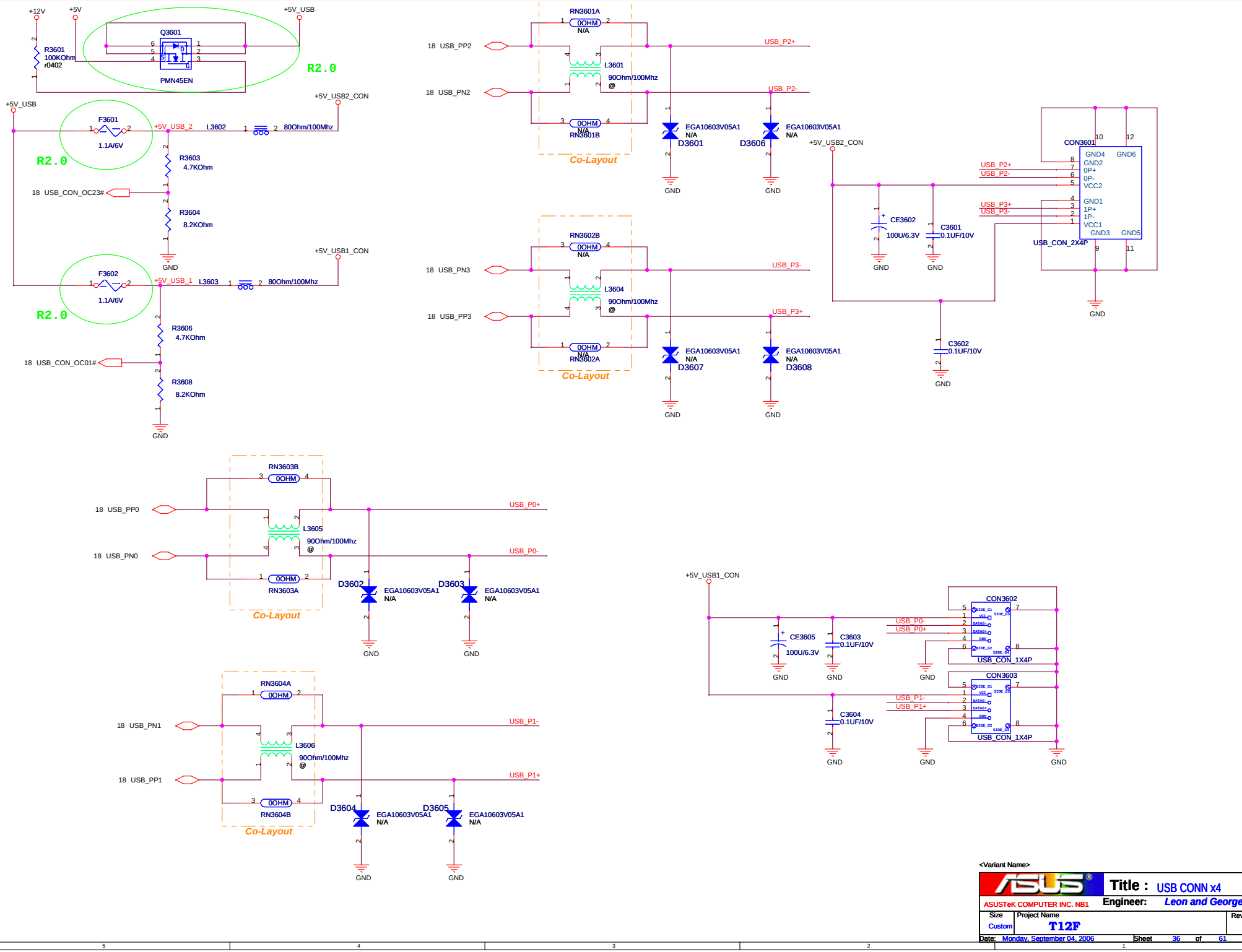
ASUSTeK COMPUTER INC

Title : RJ11/45 & MDC

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 35 of 61




<Variant Name>

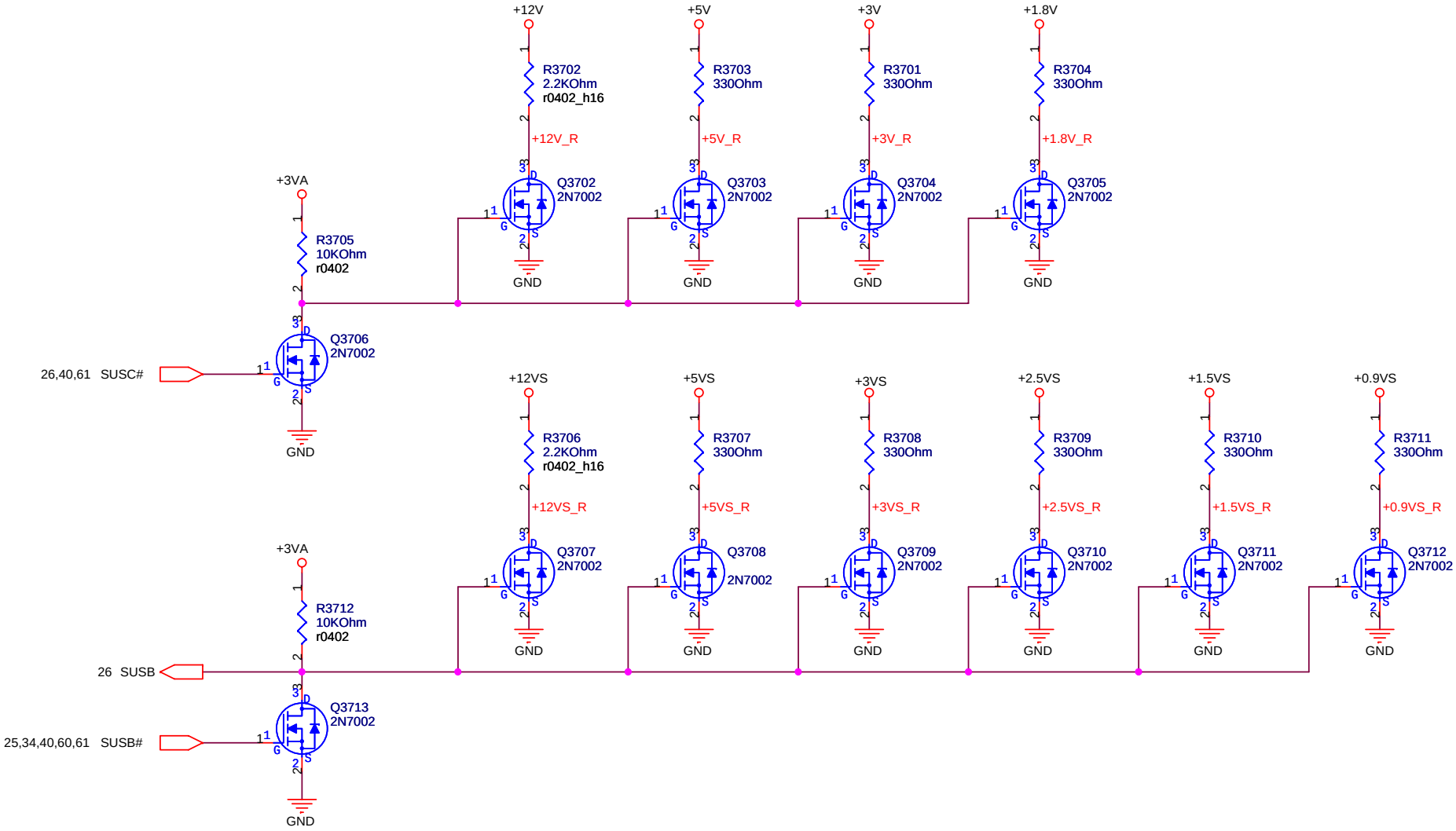
ASUSTeK COMPUTER INC. NB1

Title : USB CONN x4

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 36 of 61




<Variant Name>

ASUSTeK COMPUTER INC

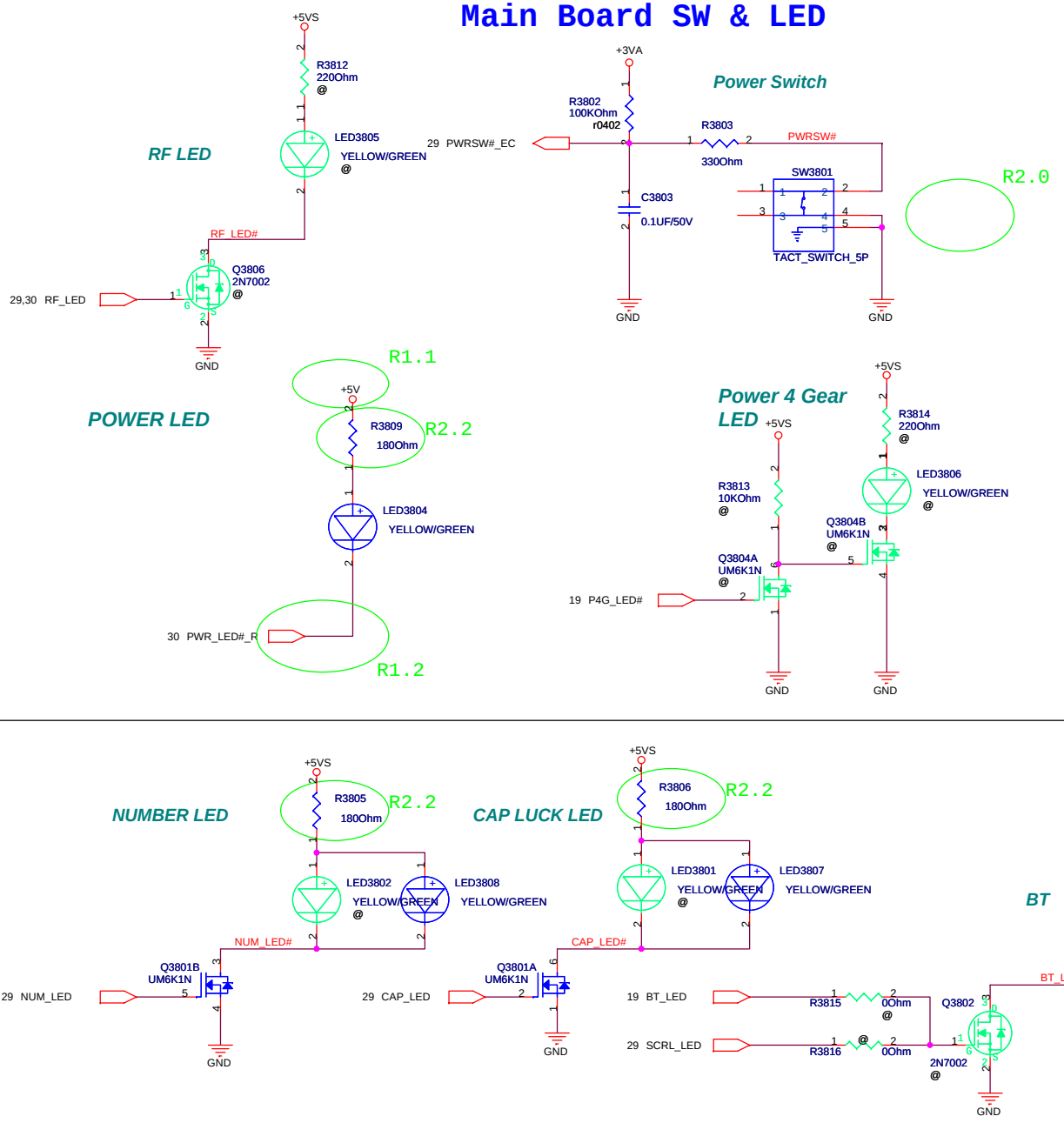
Title : Discharge Circuit

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 37 of 61

# Main Board SW & LED




<Variant Name>

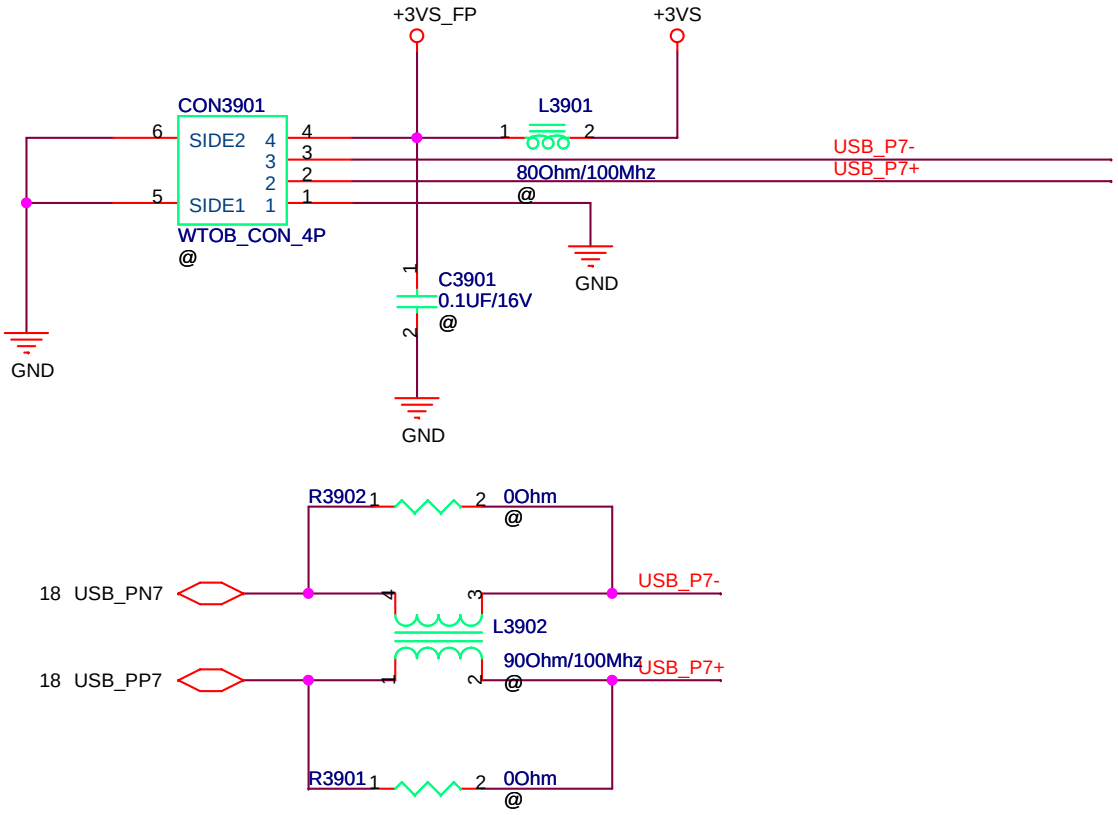
ASUSTeK COMPUTER INC

Title : SW/LED

Engineer: Leon and George

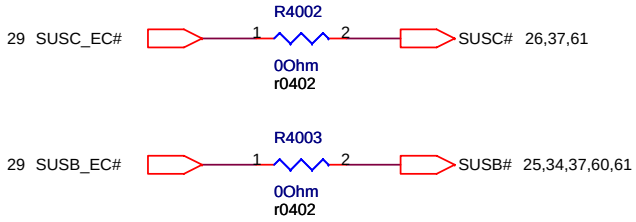
| Size | Project Name | Rev |
|---|---|---|
| B | T12F | |

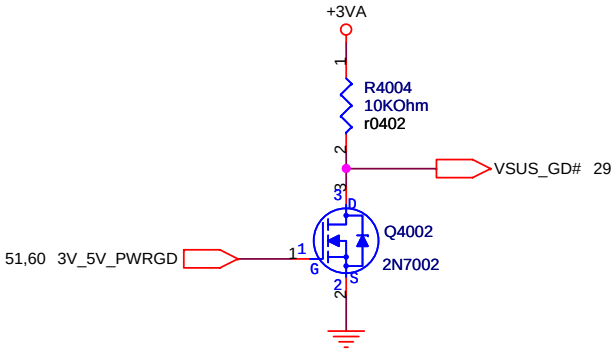
Date: Wednesday, September 06, 2006 Sheet 38 of 61

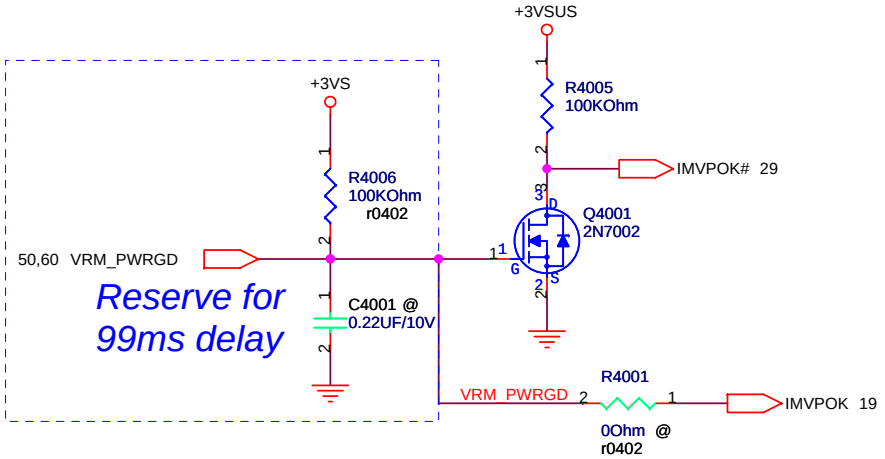



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : FINGER PRINT | |
| | Engineer: Leon and George | |
| Size: A | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 39 of 61 | |




<Variant Name>

ASUSTeK COMPUTER INC

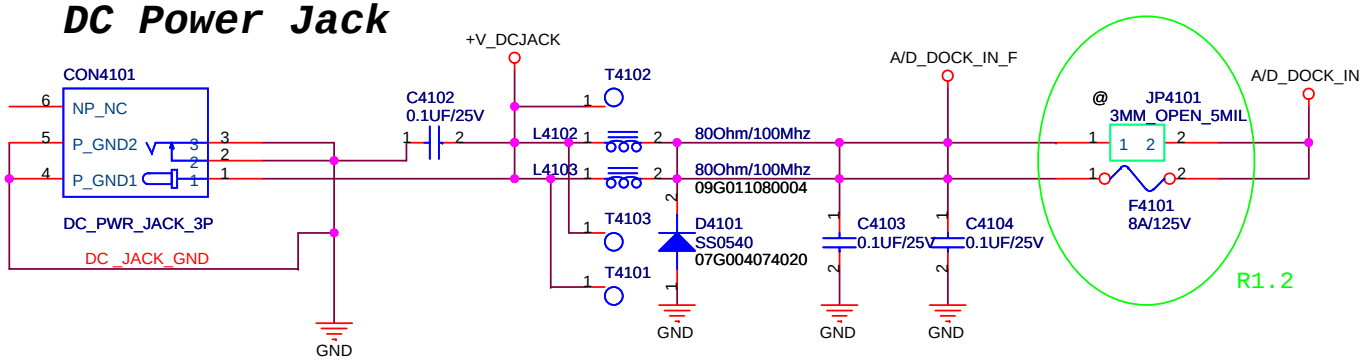
Title : POWER-ON SEQ.

Engineer: Leon and George

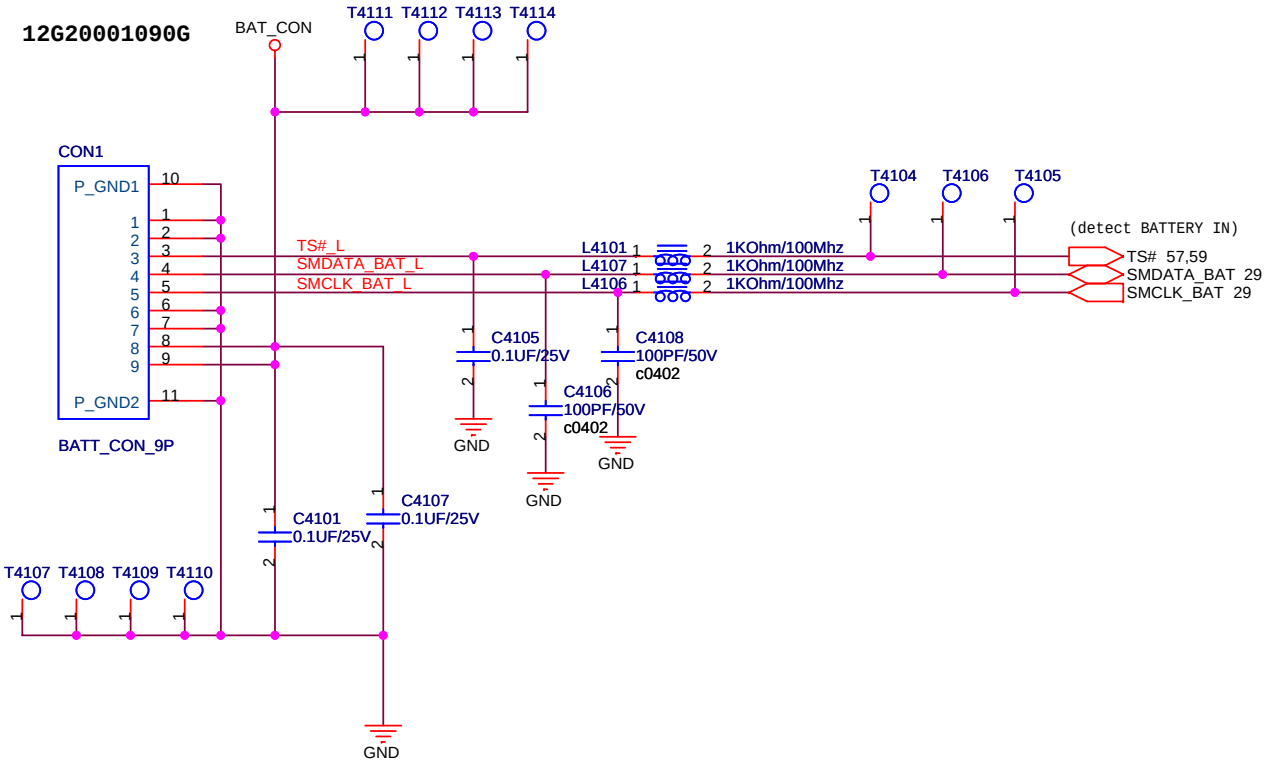
| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 40 of 61

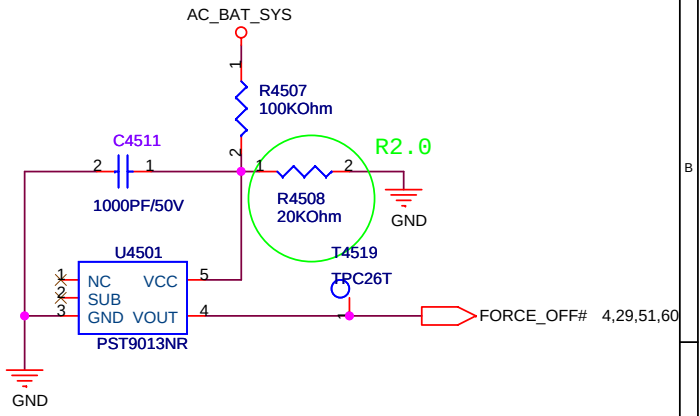
# DC Power Jack




12G200001090G

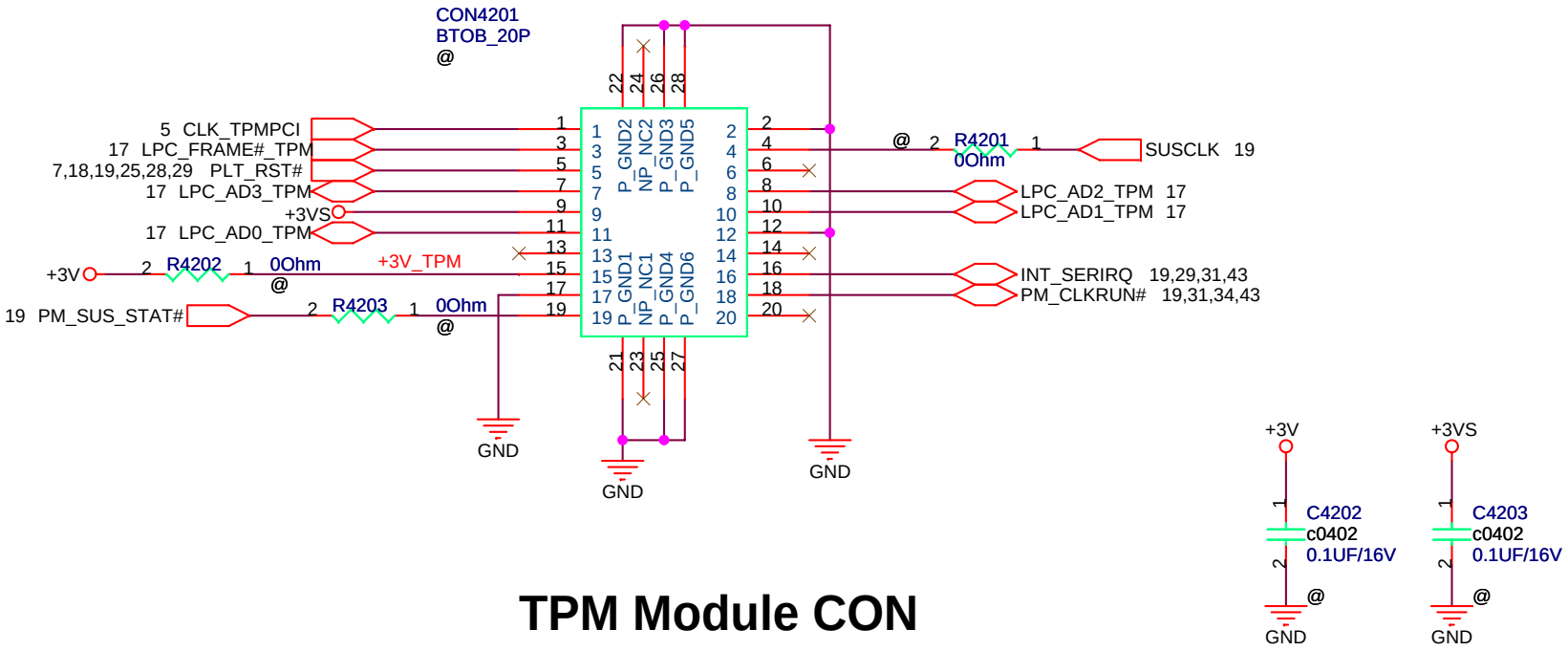



## Without Battery & Pull out Adapter



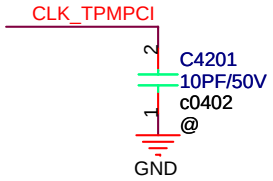

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DC/ BATT IN | |
| | Engineer: Leon and George | |
| Size: A4 | Project Name: T12F | Rev |
| Date: Monday, September 04, 2006 | Sheet 41 of 61 | |




# TPM Module CON




<Variant Name>

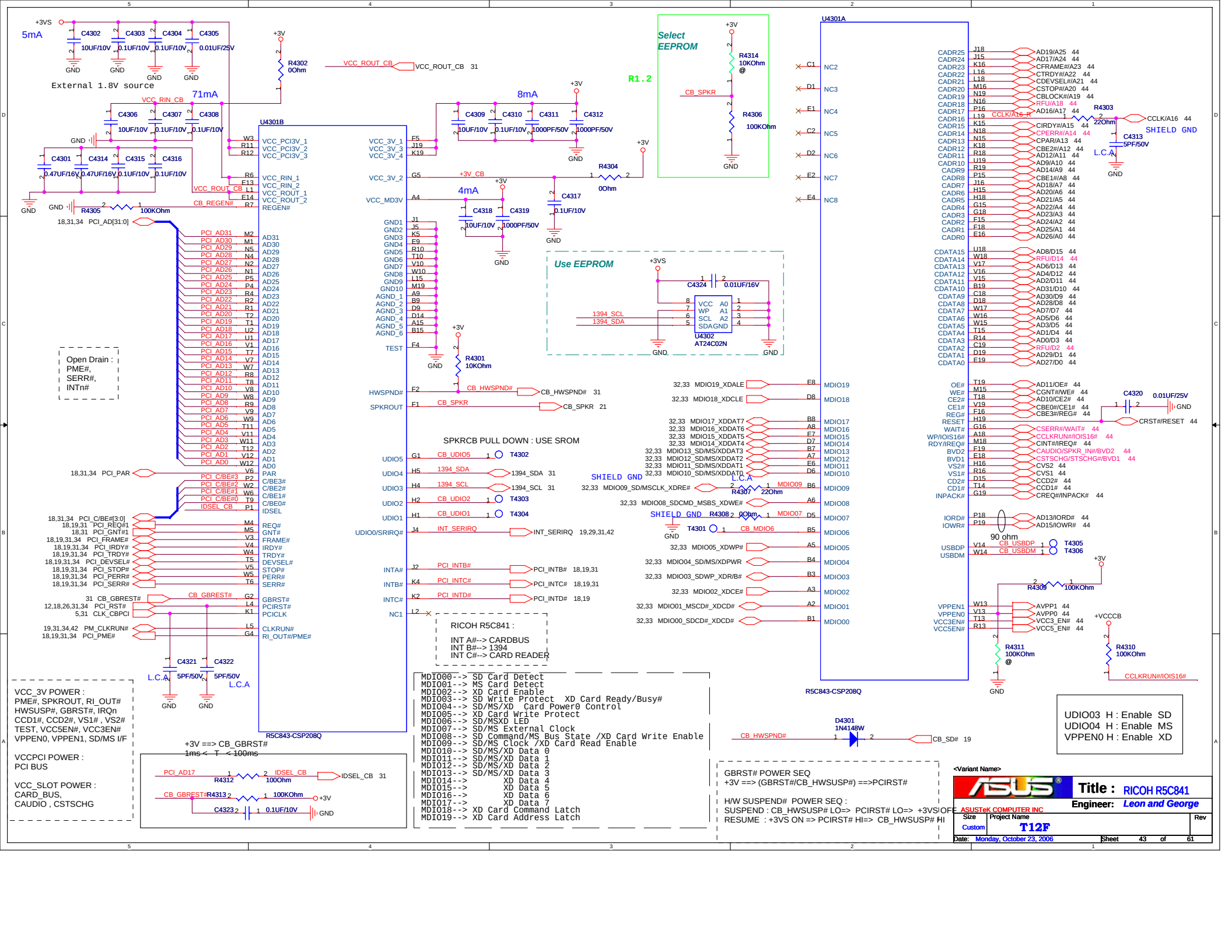
ASUSTeK COMPUTER INC

Title : TPM

Engineer: ~

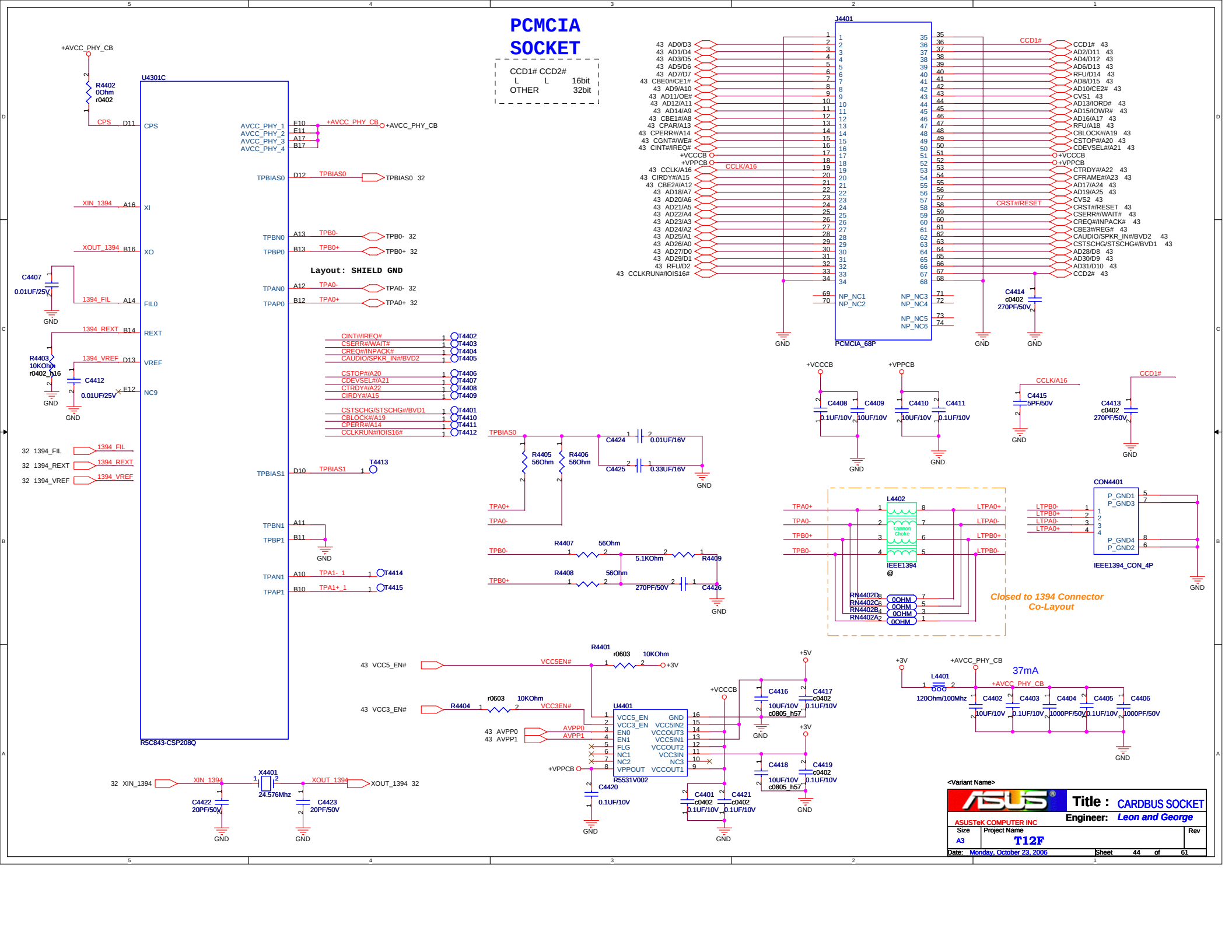
| Size | Project Name | Rev |
|---|---|---|
| A | T12F | |

Date: Monday, September 04, 2006 Sheet 42 of 61


5mA
External 1.8V source
71mA
8mA
4mA
Select EEPROM
R1.2
Use EEPROM
U4301A
U4301B
R5C843-CSP208Q
U4302 AT24C02N
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
GBRST# POWER SEQ +3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ : SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
<Variant Name>
Title : RICOH R5C841
Engineer: Leon and George
ASUSTeK COMPUTER INC
Project Name T12F
Date: Monday, October 23, 2006
Sheet 43 of 61

# PCMCIA SOCKET

| CCD1# | CCD2# | |
|---|---|---|
| L | L | 16bit |
| OTHER | | 32bit |




<Variant Name>

ASUSTeK COMPUTER INC

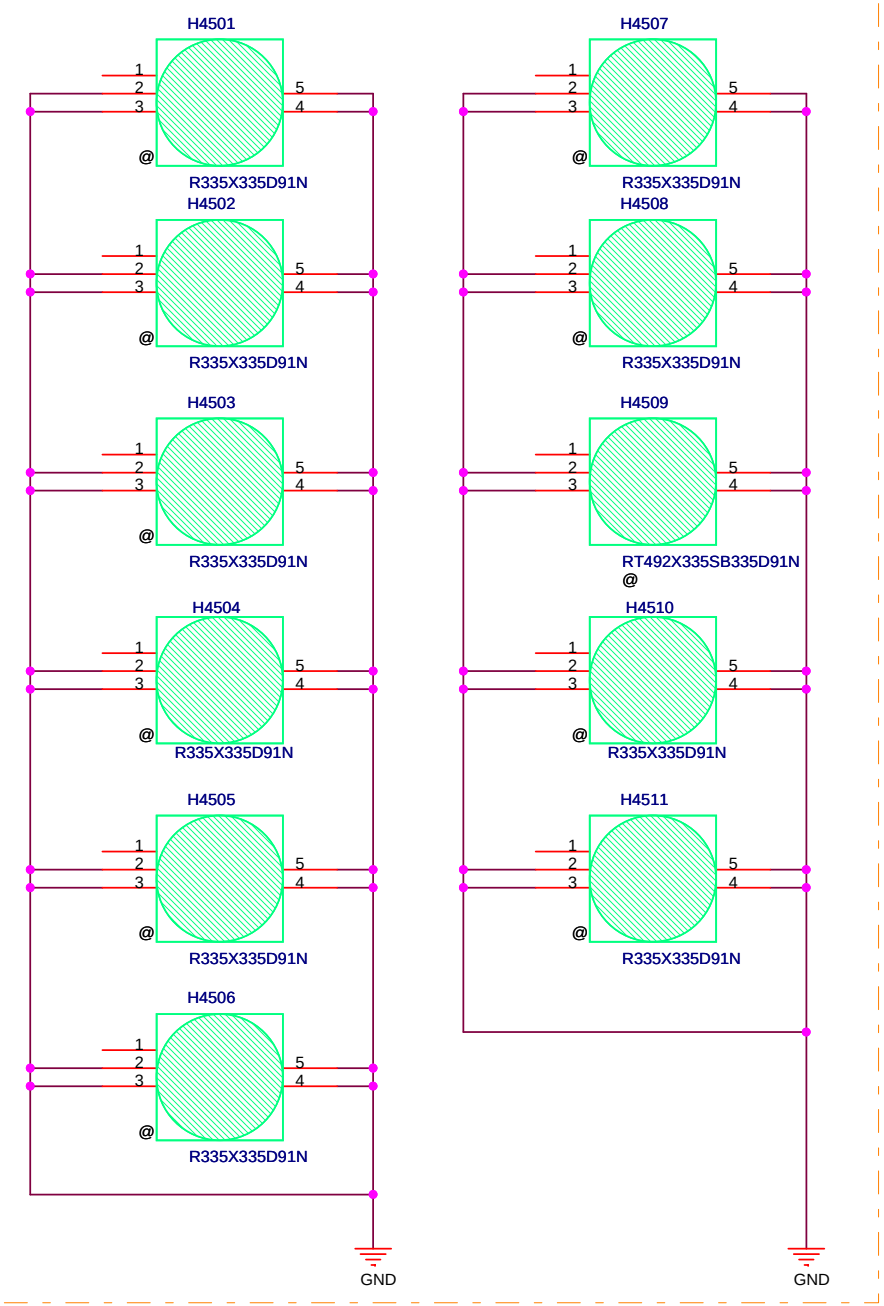
Title : CARDBUS SOCKET

Engineer: Leon and George

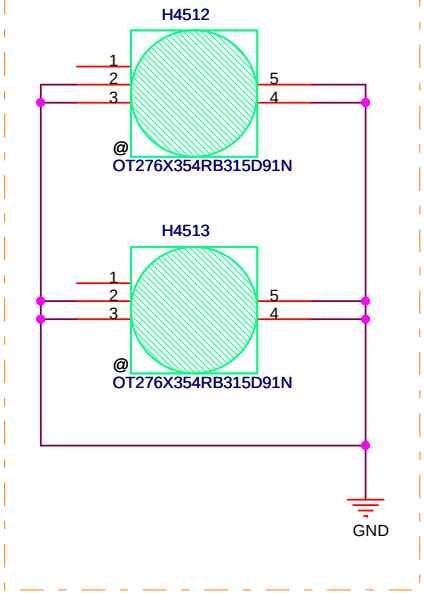
| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

Date: Monday, October 23, 2006 Sheet 44 of 61

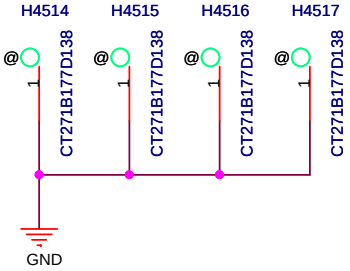
## ABCDH



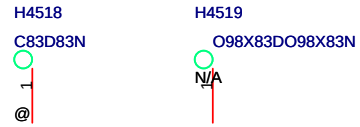

## E



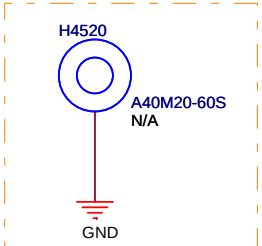

## F



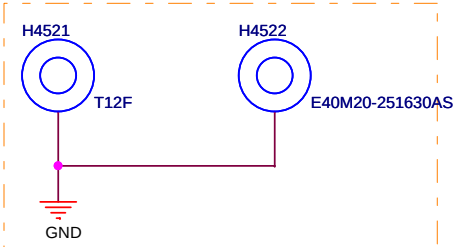

## 固定孔




## I




## G




<Variant Name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| A4 | T12F | |

Date: Monday, September 04, 2006 Sheet 45 of 61

## R1.1

| Page | Action | Reason |
|---|---|---|
| 5 | Add R566,R567,R568,R569 to divide voltage. | Clock GEN output voltage is too high. |
| 17 | Add R1733~R1737 (Reserve) | For EMI request |
| 17 | Add R1729~R1732 | Add MDC feature |
| 22 | Change C2222 from 0.1uF to 0.47uF | Delay the HP turn-on timing to avoid noise at the system power on. |
| 22 | Add R2233 and L2202 to link the different GND | For EMI request |
| 26 | Add CON2603 | Only use for debug, it will be deleted before MP |
| 31 | Add C3101~C3103 | Reduce power rippler of R5C832 |
| 31 | Add R3103 | UDIO5 pull high to disable external EEPROM |
| 35 | Add CON3203 and MDC relative circuit | Add MDC feature |
| 38 | Change power LED power from +5VS to +5V | Slove LED can't flash in S3 |

## R1.2

| Page | Action | Reason |
|---|---|---|
| 4 | Add U402 and relative circuit. | Add hardware thermal protection circuit |
| 12 | Change L1204,L1205,C1209,1210 | For EMI request |
| 12 | Change L1210 to 1k ohm | Reduce leakage current. |
| 13 | Change L1304~L1306 to 150nH and C1308 C1310 C1312 change to 10pF | Improve CRT signal |
| 21 | All R1.2 modification in this page | Follow ADI recommend vlaue to get Vista logo. |
| 22 | All R1.2 modification in this page | Follow ADI recommend vlaue to get Vista logo. |
| 23 | All R1.2 modification in this page | Improve microphone quality |
| 30 | Add R3022 | Reserve RF_LED feature |
| 38 | Del Q3005 and link PWR_LED#_R to LED directly | Cost down |
| 41 | Add F4101 and JP4101 | Reserve, normal use JP4101 |
| 43 | Add R4314 | Reserve, normal no use |

## R2.0

| Page | Action | Reason |
|---|---|---|
| 5 | Change C516,C517 value | Tune up accuracy of 14.318MHz. |
| 17 | Change C1702,C1703 value | Tune up accuracy of 32.768KHz. |
| 21 | Add R2111 to pull high | Avoid input pin NC. |
| 29 | Change C2911,C2915 value | Tune up accuracy of 32.768KHz. |
| 36 | Modify Q3601 circuit | Solve system will auto turn-on when remove USB HDD with external power. |
| 38 | Add C3804 | For ESD request |
| 41 | Change R4508 from 16.9K to 20K ohm | Solve shutdown issue when plug-in AC jack in low battery mode. |
| 10 | Add CE1003 | Reduce power rippler of +1.8V |

## R2.2

| Page | Action | Reason |
|---|---|---|
| 29 | Add R2918 and change C2910 to 0.1uF | Solve CMOS clear issue. |
| 33 | Add C3306 | Solve Type-H XD can't work normally. |
| 38 | Change R3805,R3806,R3809 to 180ohm(1/10W) | Improve Derating |
| | | |
| | | |
| | | |
| | | |

## R2.3

| Page | Action | Reason |
|---|---|---|
| 33 | Change CON3301 to ALPS | Prevent card from being shaved by connector |
| | | |
| | | |

<Variant Name>

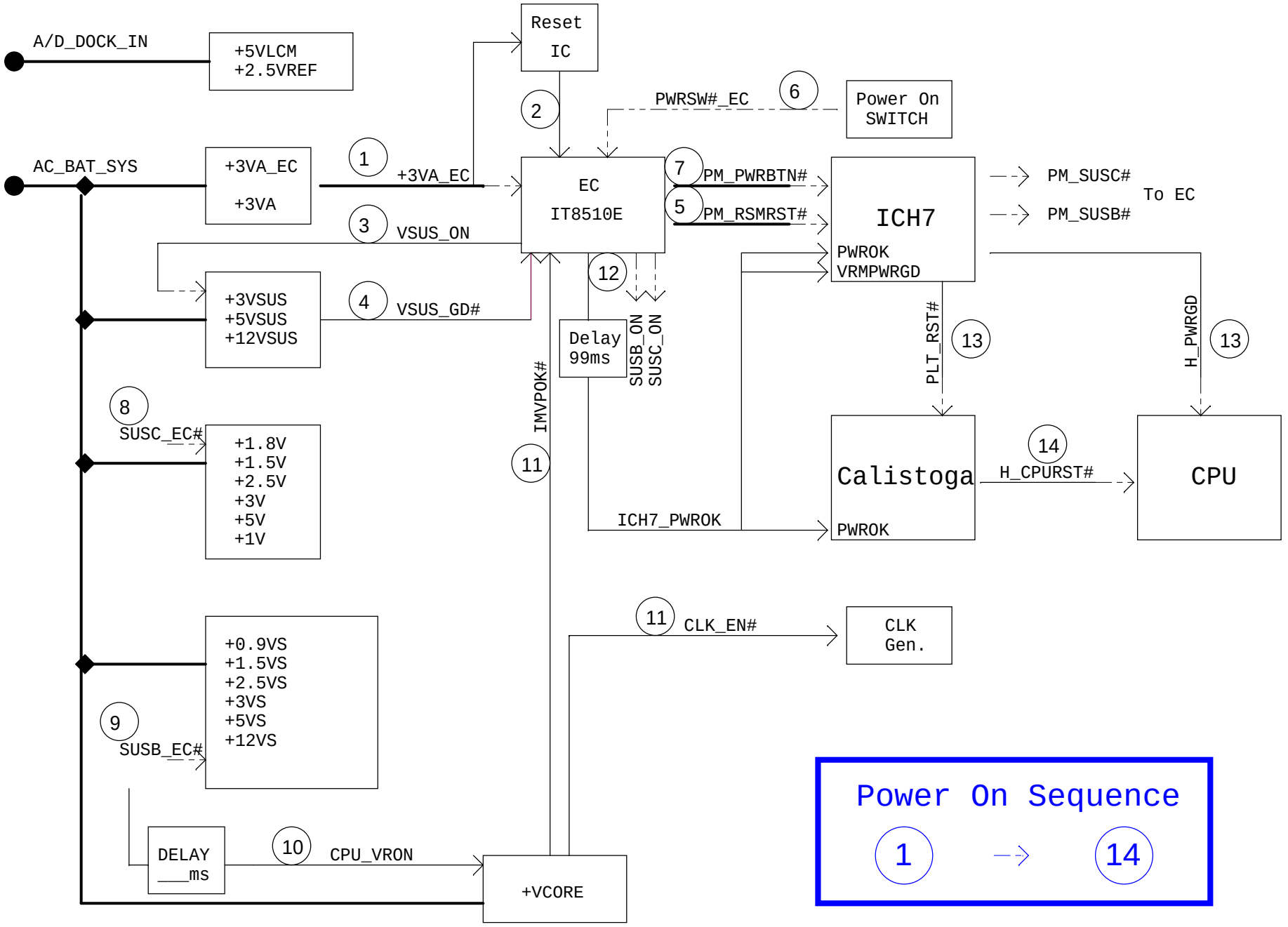
Title : HISTORY

Engineer: Leon and George

ASUSTeK COMPUTER INC

| Size | Project Name | Rev |
|---|---|---|
| A3 | T12F | |

Date: Tuesday, October 17, 2006 Sheet 46 of 61




<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: Leon and George

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 47 of 61

## EC GPIO SETTING

| Pin | Pin Name | Signal Name | Type |
|---|---|---|---|
| 32 | PWM0/GPA0 | BRIGHT_PWM | |
| 33 | PWM1/GPA1 | FAN_PWM | O |
| 36 | PWM2/GPA2 | / | |
| 37 | PWM3/GPA3 | / | |
| 38 | PWM4/GPA4 | CHG_LED_UP# | O |
| 39 | PWM5/GPA5 | PWR_LED_UP# | O |
| 40 | PWM6/GPA6 | BATSEL_3S# | |
| 43 | PWM7/GPA7 | LCD_BACKOFF# | O |
| 153 | RXD/GPB0 | NUM_LED | O |
| 154 | TXD/GPB1 | CAP_LED | O |
| 162 | GPB2 | SCRL_LED | O |
| 163 | SMCLK0/GPB3 | SMCLK_BAT | I/0 |
| 164 | SMDAT0GPB4 | SMDATA_BAT | I/0 |
| 5 | GA20/GPB5 | A20GATE | O |
| 6 | KBRST#/GPB6 | RC_IN# | O |
| 165 | GPB7 | THRO_CPU | O |
| 169 | SMCLK1/GPC1 | SMB1_CLK | I/0 |
| 170 | SMDAT1/GPC2 | SMB1_DAT | I/0 |
| 171 | GPC3 | / | |
| 172 | TMRI0/WUI2/GPC4 | ACIN_OC# | I |
| 175 | GPC5 | OP_SD# | O |
| 176 | TMRI1/WUI3/GPC6 | BAT_IN_OC# | I |
| 1 | CK32KOUT/GPC7 | / | O |
| 26 | RI1#/WUI0/GPD0 | PM_SUSB# | I |
| 29 | RI2#/WUI1/GPD1 | PM_SUSC# | I |
| 30 | LPCRST#/WUI4//GPD2 | PLT_RST# | I |
| 31 | ECSCI#/GPD3 | EXT_SCI# | O |
| 41 | GPD4 | | I |
| 42 | GINT/GPD5 | / | |
| 62 | TACH0/GPD6 | FAN0_TACH | I |
| 63 | TACH1/GPD7 | / | O |
| 87 | ADC4/GPE0 | WLAN_SW# | I |
| 88 | ADC5/GPE1 | / | I |
| 89 | ADC6/GPE2 | MARATHON# | I |
| 90 | ADC7/GPE3 | DISTP_SW# | I |
| 2 | PWRSW/GPE4 | PWRSW#_EC | I |
| 44 | WUI5/GPE5 | / | |
| 24 | LPCPD#/WUI6/GPE6 | LID_EC# | I |
| 25 | CLKRUN#/WUI7/GPE7 | | O |
| 110 | PS2CLK0/GPF0 | / | |
| 111 | PS2DAT0/GPF1 | / | |
| 114 | PS2CLK1/GPF2 | / | I/0 |
| 115 | PS2DAT1/GPF3 | / | I/0 |
| 116 | PS2CLK2/GPF4 | TP_CLK | |
| 117 | PS2DAT2/GPF5 | TP_DAT | |
| 118 | PS2CLK3/GPF6 | PWRLMT# | |
| 119 | PS2DAT3/GPF7 | / | I |
| 113 | FA16/GPG0 | FA16 | |
| 112 | FA17/GPG1 | FA17 | |
| 104 | FA18/GPG2 | FA18 | |
| 103 | FA19/GPG3 | / | |
| 3 | FA20/GPG4 | THRM_CPU# | I |
| 4 | FA21/GPG5 | / | |
| 27 | LPC80HL/GPG6 | PMTHERM# | O |
| 28 | LPC80LL/GPG7 | AC_APR_UC# | I |

| Pin | Pin Name | Signal Name | Type |
|---|---|---|---|
| 48 | GPH0 | VSUS_ON | O |
| 54 | GPH1 | VSUS_GD# | I |
| 55 | GPH2 | IMVPOK# | I |
| 69 | GPH3 | PM_PWRBTN# | O |
| 70 | GPH4 | SUSC_EC# | O |
| 75 | GPH5 | SUSB_EC# | O |
| 76 | GPH6 | CPU_VRON | O |
| 105 | GPH7 | PM_RSMRST# | O |
| 148 | GPI0 | ICH7_PWROK | O |
| 149 | GPI1 | WATCH_DOG# | O |
| 152 | GPI2 | / | |
| 155 | GPI3 | CHG_EN# | O |
| 156 | GPI4 | PRECHG | O |
| 168 | GPI5 | BAT_LL# | O |
| 174 | GPI6 | BAT_LEARN | O |
| 8 | GPL0 | WLAN_ON# | O |
| 11 | GPL1 | BT_ON# | O |
| 12 | GPL2 | RF_OFF_SW# | I |
| 20 | GPL3 | RF_LED | O |
| 92 | CRX | CRX | I/0 |

## ICH7-M GPIO SETTING

| Pin | Pin Name | Signal Name | Type |
|---|---|---|---|
| AB18 | GPIO00/BM_BUSY# | PM_BMBUSY# | I |
| C8 | GPIO01/REQ5# | PCI_REQ#5 | I |
| G8 | GPIO02/PIRQE# | PCI_INTE# | I |
| F7 | GPIO03/PIRQF# | PCI_INTF# | I |
| F8 | GPIO04/PIRQG# | PCI_INTG# | I |
| G7 | GPIO05/PIRQH# | PCI_INTH# | I |
| AC21 | GPIO06 | BT_LED | I/O |
| AC18 | GPIO07 | / | I |
| E21 | GPIO08 | EXTSMI# | I |
| E20 | GPIO09 | SATA_DET#0 | I |
| A20 | GPIO10 | / | O |
| B23 | SMBALERT#/GPIO11 | SMB_ALERT# | I |
| F19 | GPIO12 | KBC_SCI# | I |
| E19 | GPIO13 | / | |
| R4 | GPIO14 | / | |
| E22 | GPIO15 | WLAN_LED# | I/O |
| AC22 | GPIO16 | PM_DPRSLPVR | O |
| D8 | GPIO17/GNT5# | PCI_GNT#5 | O |
| AC20 | GPIO18/STP_PCI# | STP_PCI# | O |
| AH18 | GPIO19/SATA1GP | / | I |
| AF21 | GPIO20/STP_CPU# | STP_CPU# | O |
| AE19 | GPIO21/SATA0GP | / | I |
| A13 | GPIO22/REQ4# | PCI_REQ#4 | I |
| AA5 | LDRQ1#/GPIO23 | LPC_DRQ#1 | I/O |
| R3 | GPIO24 | P4G_LED# | |
| D20 | GPIO25 | CB_SD# | |
| A21 | GPIO26/EL_RSVD | BT_DET# | |
| B21 | GPIO27/EL_STATE0 | | I |
| E23 | GPIO28/EL_STATE1 | | |
| C3 | GPIO29/OC#5 | USB_OC_5# | I |
| A2 | GPIO30/OC#6 | NEWCARD_OC# | I |
| B3 | GPIO31/OC#7 | USB_OC_7# | I |
| AG18 | GPIO32/CLKRUN# | PM_CLKRUN# | O |
| AC19 | GPIO33/AZ_DOCK_EN# | / | O |
| U2 | GPIO34/AZ_DOCK_RST# | / | |
| AD21 | GPIO35 | ICH_GPIO35 | O |
| AH19 | GPIO36/SATA2GP | / | |
| AE19 | GPIO37/SATA3GP | PCB_ID0 | I/O |
| AD20 | GPIO38 | PCB_ID1 | I |
| AE20 | GPIO39 | PCB_ID2 | I |
| A14 | GNT4#/GPIO48 | PCI_GNT#4 | O |
| AG24 | GPIO49/CPUPWRGD | H_PWRGD | O |

| PCI Device | IDSEL# | REQ/GNT# | Interrupts |
|---|---|---|---|
| 10/100 RTL8100CL | AD23 | 2 | A |
| CARDBUS | AD17 | 1 | B |
| 1394 | AD17 | 1 | C |
| CARD READER | AD17 | 1 | D |
| | | | |

| PCIE Device | Bus | | |
|---|---|---|---|
| MINI_CARD | PE(T/R)(p/n)2 | | |
| NEWCARD | PE(T/R)(p/n)3 | | |
| | | | |
| | | | |

| SM-Bus Device | SM-Bus Address |
|---|---|
| Clock Generator | 1101001x ( D2 ) |
| SO-DIMM 0 | 1010000x ( A0 ) |
| SO-DIMM 1 | 1010001x ( A2 ) |
| Thermal Sensor | 1001100x ( 98 ) |
| | |
| | |

<Variant Name>

Title : GPIO Setting

Engineer: Leon and George

ASUSTeK COMPUTER INC

Size: Custom | Project Name: T12F | Rev

Date: Monday, September 04, 2006 | Sheet 48 of 61

<Variant Name>

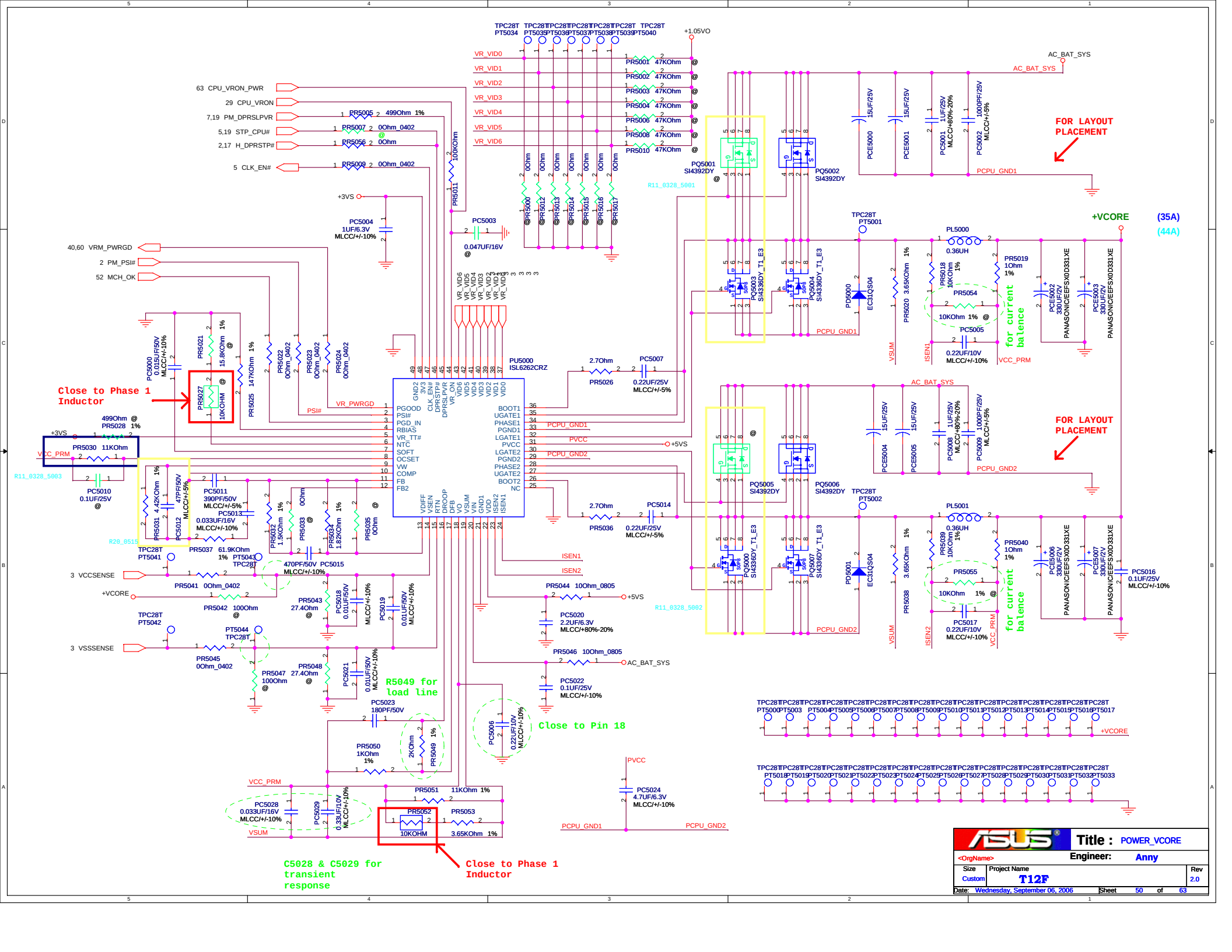
Title : N/A

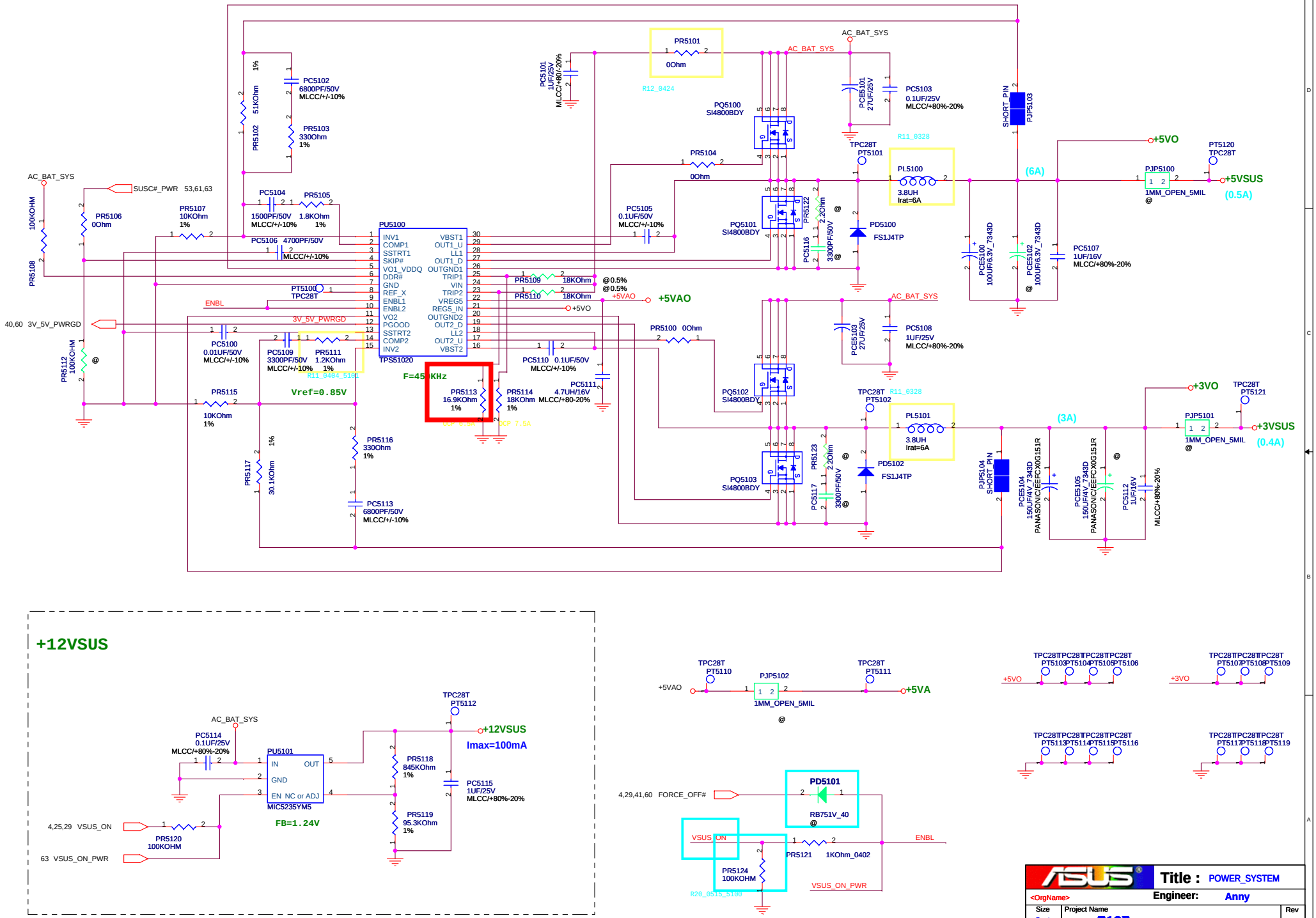
Engineer: Leon and George

ASUSTeK COMPUTER INC

| Size | Project Name | Rev |
|---|---|---|
| Custom | T12F | |

Date: Monday, September 04, 2006 Sheet 49 of 61


PU5000 ISL6262CRZ
PQ5001 SI4392DY
PQ5002 SI4392DY
PQ5005 SI4392DY
PQ5006 SI4392DY
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PQ5000 SI4336DY_T1_E3
PQ5007 SI4336DY_T1_E3
PD5000 EC31QS04
PD5001 EC31QS04
PL5000 0.36UH
PL5001 0.36UH
+1.05VO
+VCORE (35A) (44A)
AC_BAT_SYS
+5VS
+3VS
PCPU_GND1
PCPU_GND2
PVCC
VCC_PRM
VSUM
ISEN1
ISEN2
FOR LAYOUT PLACEMENT
for current balence
Close to Phase 1 Inductor
Close to Pin 18
R5049 for load line
C5028 & C5029 for transient response
Title : POWER_VCORE
Engineer: Anny
Project Name T12F
Size Custom
Rev 2.0
Date: Wednesday, September 06, 2006
Sheet 50 of 63





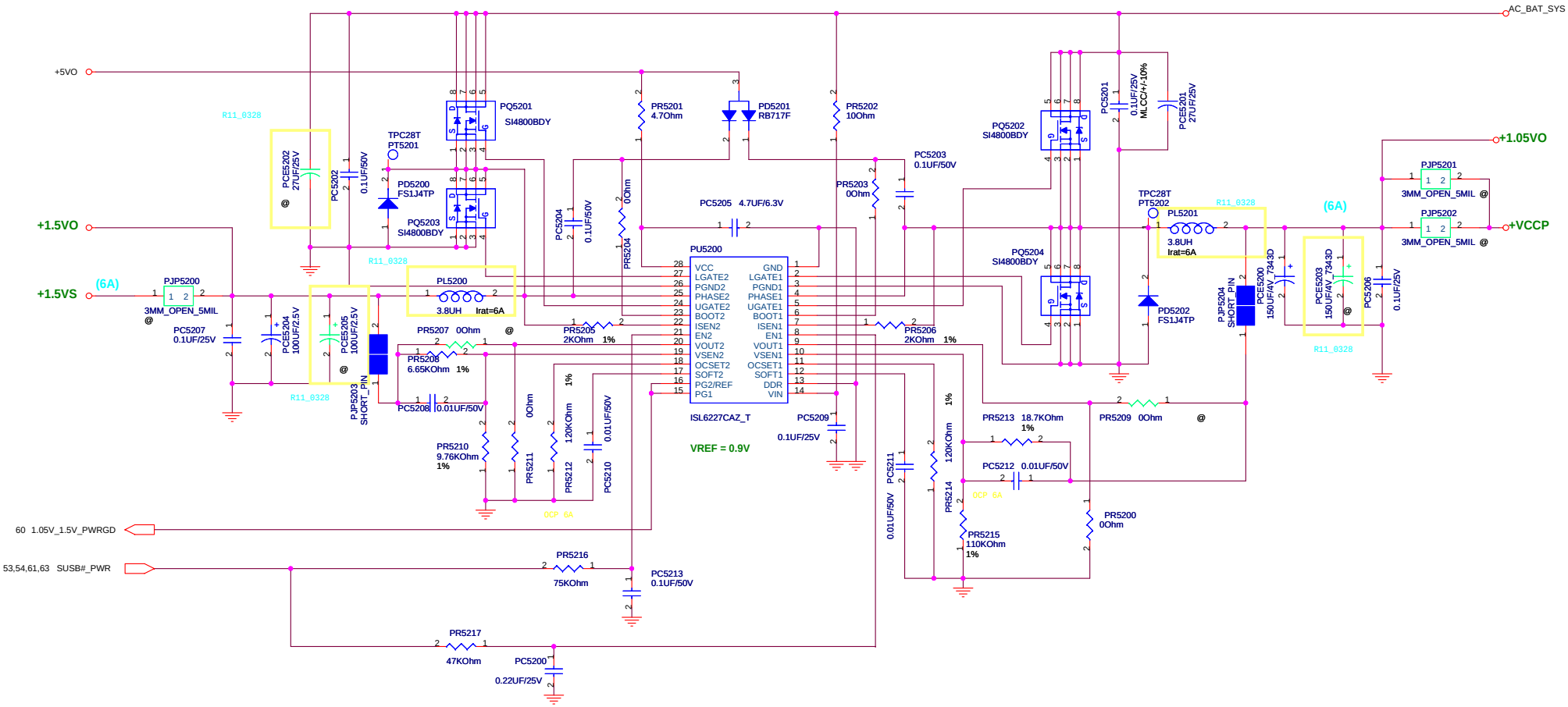




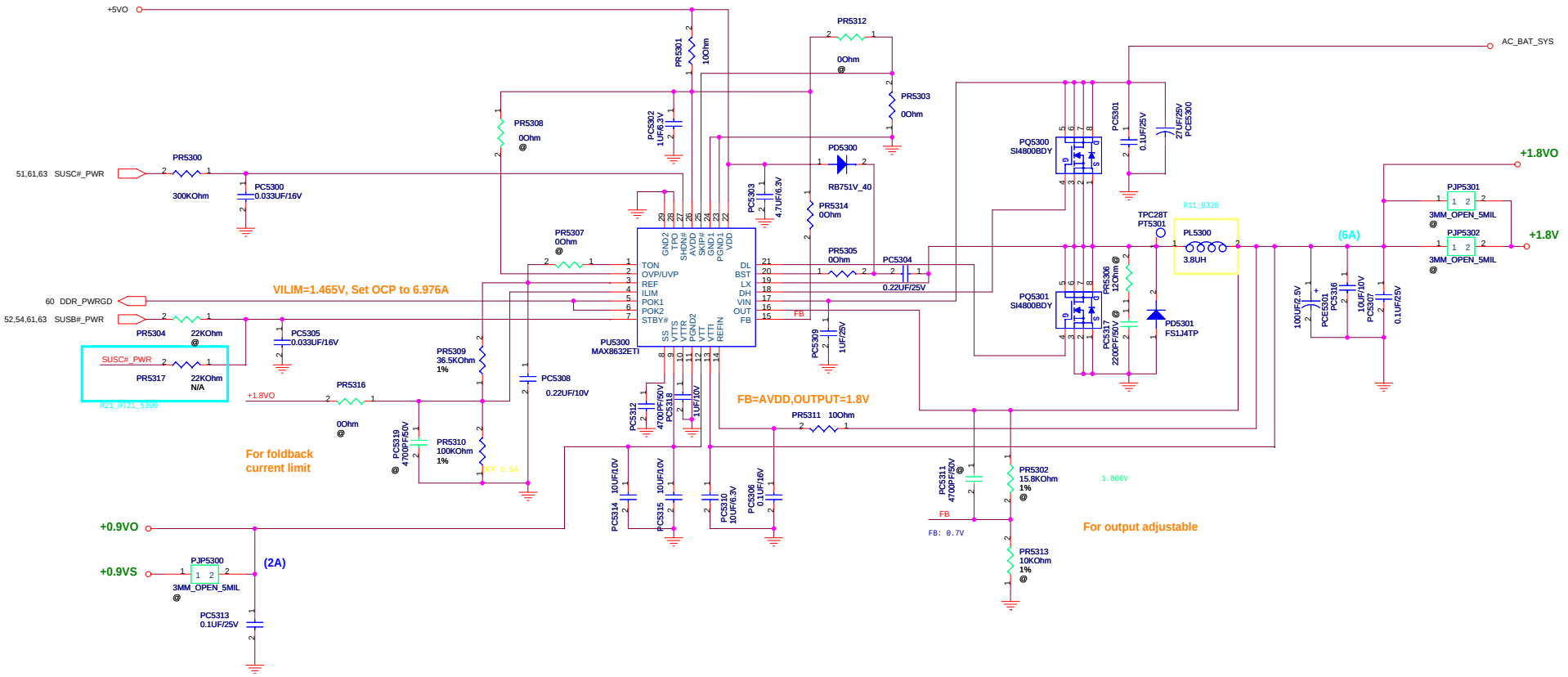




| | | |
|---|---|---|
| ASUS | Title : POWER_SYSTEM | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 51 of 63 | |

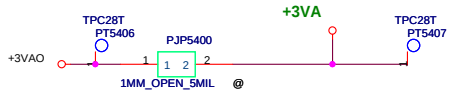


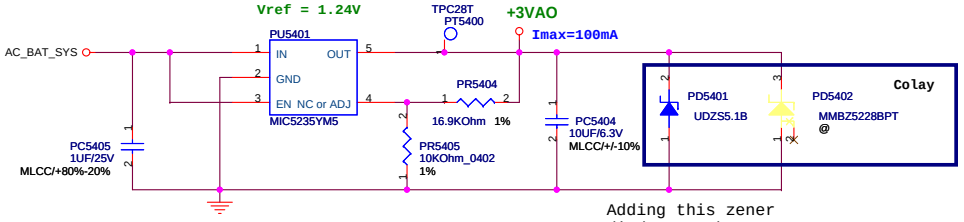

| | | |
|---|---|---|
| Title : POWER_I/O_1.5VS & 1.05VS | | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 52 of 63 | |




| | | |
|---|---|---|
| Title : | POWER_I/O_DDR & VTT | |
| <OrgName> | Engineer: | Anny |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 53 of 63 | |

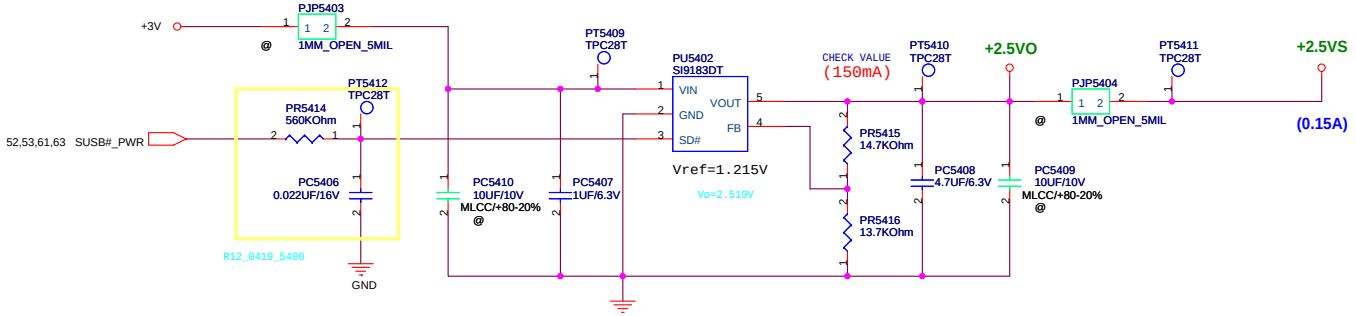
## +3VA0



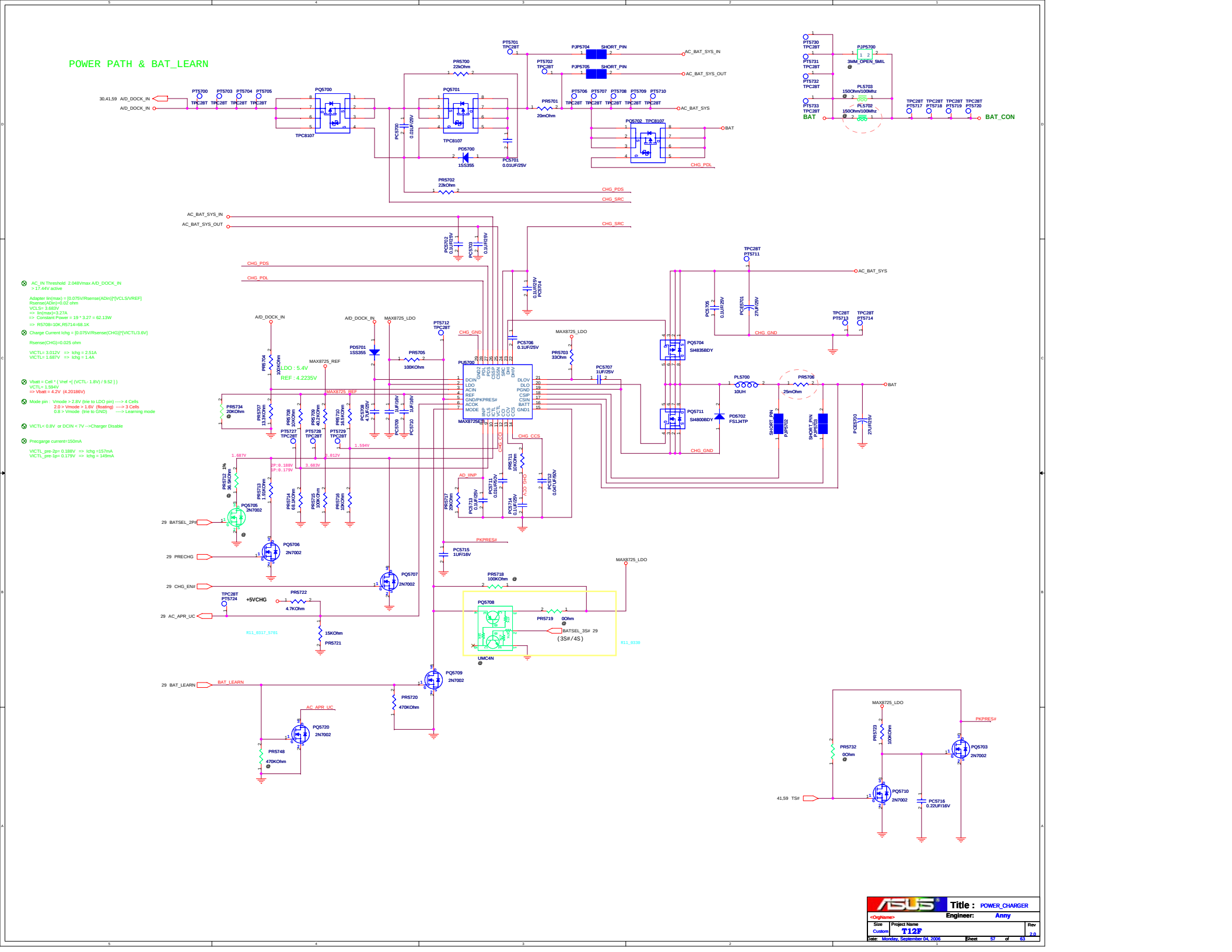

Adding this zener diode to make sure that EC doesn't release smoke when PU5401.1 is short to PU5401.5

## +2.5VS



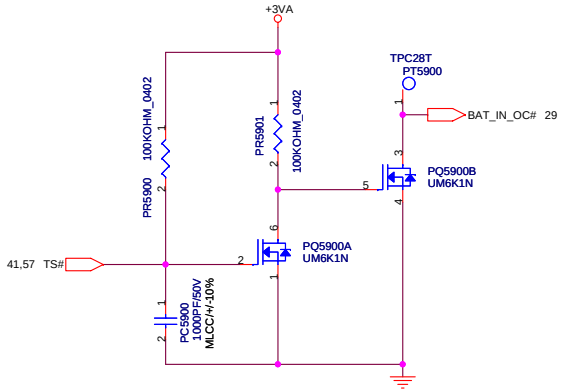

| | | |
|---|---|---|
| ASUS | Title : POWER_I/O_+3VA & +2.5V | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.1 |
| Date: Monday, September 04, 2006 | Sheet 54 of 63 | |

# POWER PATH & BAT_LEARN

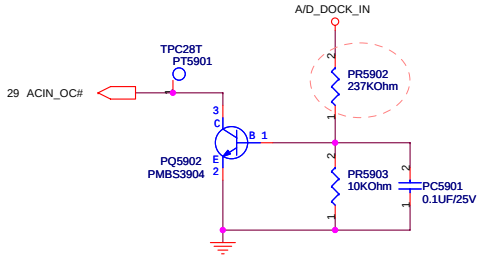



| | | | |
|---|---|---|---|
| ASUS | Title : POWER_CHARGER | | |
| <OrgName> | Engineer: Anny | | |
| Size: Custom | Project Name: T12F | | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 57 of 63 | | |

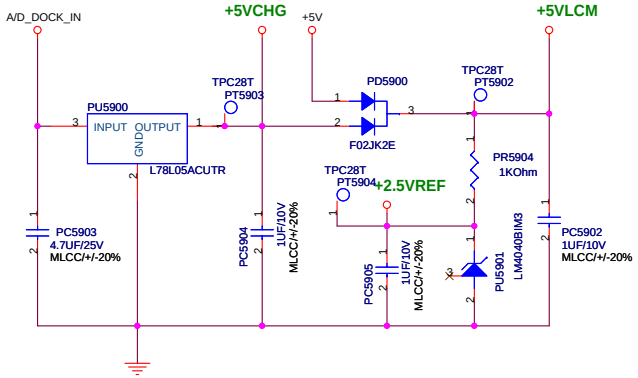
## BATTERY IN DETECT




## ADAPTER IN DETECT

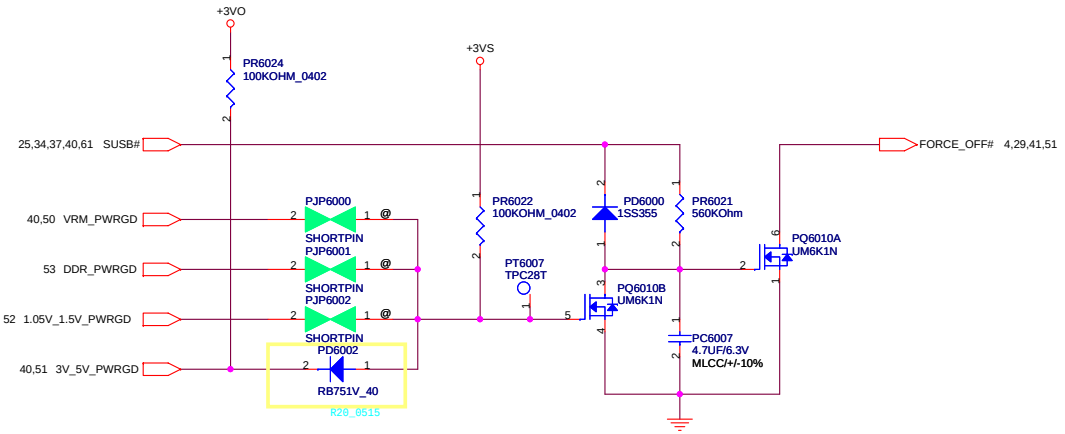



## +5VLCM, +5VCHG & +2.5VREF




| | | |
|---|---|---|
| ASUS | Title : POWER_DETECT | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 59 of 63 | |

## POWER GOOD DETECTER




TPC28T PT6003 1 VRM_PWRGD

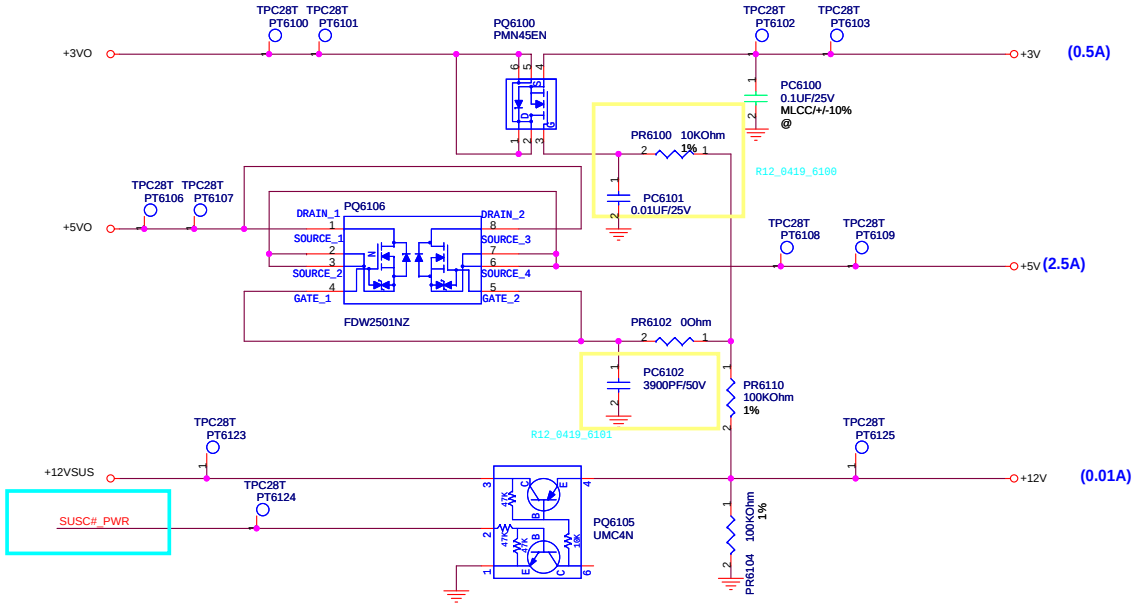
TPC28T PT6004 1 DDR_PWRGD

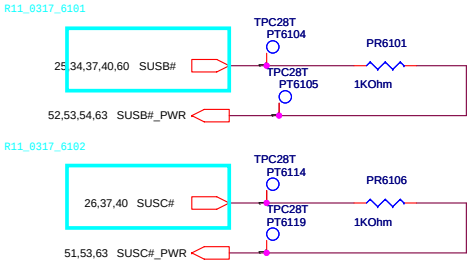
TPC28T PT6005 1 3V_5V_PWRGD

TPC28T PT6006 1 1.05V_1.5V_PWRGD

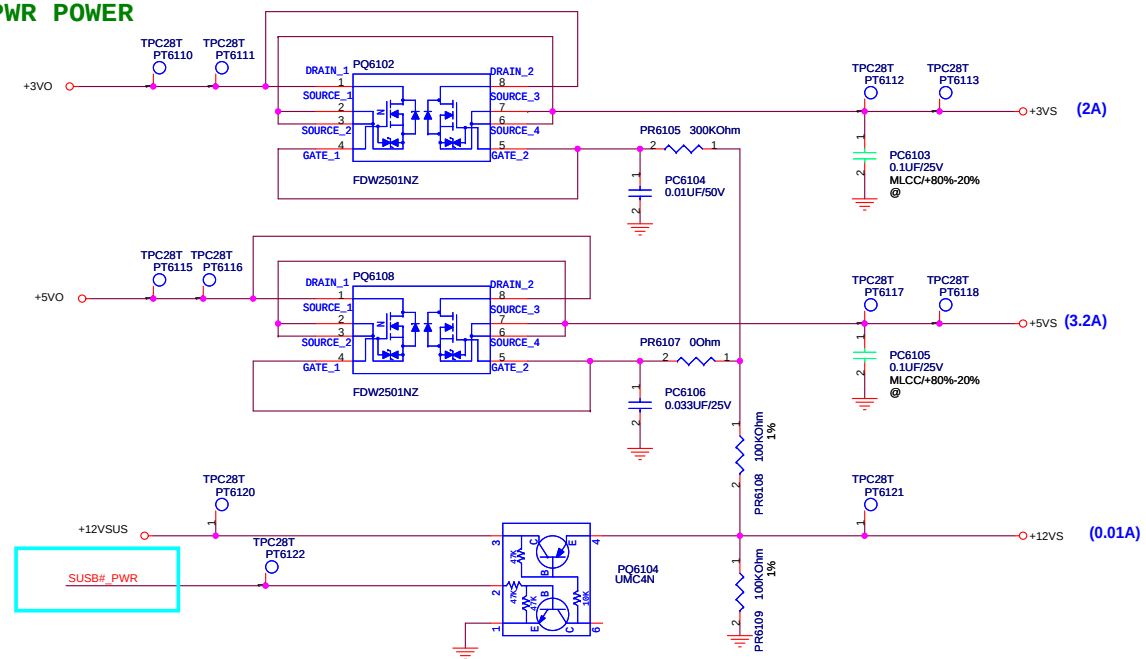
| | | |
|---|---|---|
| Title : POWER_PROTECT | | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 60 of 63 | |

## SUSC#_PWR POWER




## SUSB#_PWR POWER




| | | |
|---|---|---|
| ASUS | Title : POWER_LOAD SWITCH | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 61 of 63 | |

AC_BAT_SYS — AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA — +3VA 4,12,20,22,29,37,38,40,54,59

+5VA — +5VA 51

+5VO — +5VO 51,52,53,61

+3VO — +3VO 51,52,60,61

+3VSUS — +3VSUS 18,19,20,25,29,34,40,51

+5VSUS — +5VSUS 20,30,51

+3V — +3V 12,18,26,27,31,35,37,42,43,44,54,61

+3VS — +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

+12VSUS — +12VSUS 51,61

+12V — +12V 36,37,61

+12VS — +12VS 12,22,27,33,37,61

+5V — +5V 9,12,30,36,37,38,44,59,61

+5VS — +5VS 4,13,19,20,21,22,28,29,30,37,38,50,61

+2.5VO — +2.5VO 54

+2.5VS — +2.5VS 9,37,54

+1.8VO — +1.8VO 53

+1.8V — +1.8V 7,10,14,15,37,53

+VCCP — +VCCP 2,6,9,20,52

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH — +VCCP_GMCH 9,10

+VCCP_ICH — +VCCP_ICH 17,20

+0.9VS — +0.9VS 16,37,53

BAT — BAT 30,57

+5VCHG — +5VCHG 57,59

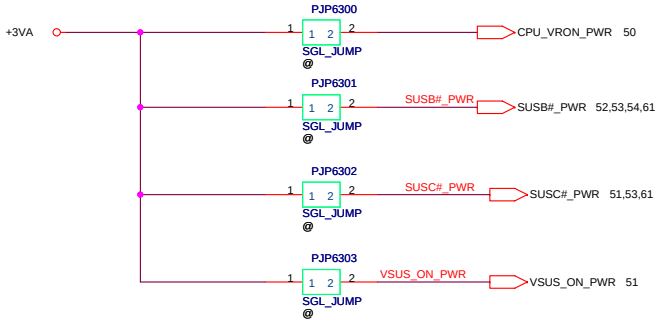
+5VLCM — +5VLCM 59

+2.5VREF — +2.5VREF 59

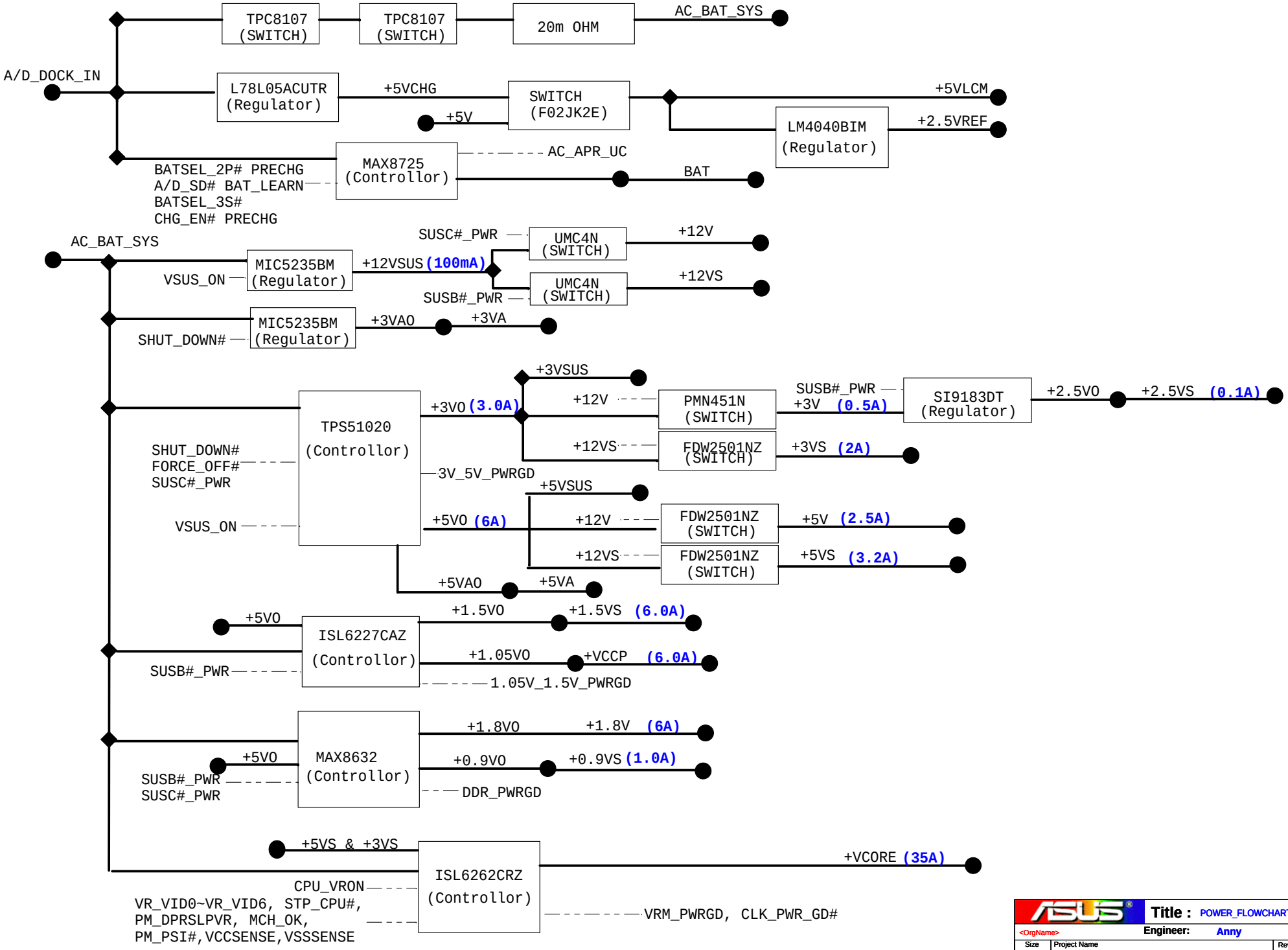
+VCORE — +VCORE 3,50

BAT_CON — BAT_CON 41,57

## FOR POWER TEST




| | | |
|---|---|---|
| ASUS | Title : POWER_SIGNAL | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 63 of 63 | |




| | | |
|---|---|---|
| ASUS | Title : POWER_FLOWCHART | |
| <OrgName> | Engineer: Anny | |
| Size: Custom | Project Name: T12F | Rev: 2.0 |
| Date: Monday, September 04, 2006 | Sheet 87 of 89 | |