T13F SCHEMATIC R1.10

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5	YONAH CPU (2)
6	FAN CTRL&Thernal protection
7	CLK GEN-ICS954310
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9	Calistoga--PCIE
10	Calistoga--DDR2
11	Calistoga--POWER
12	Calistoga--GND
13	Calistoga--Strap
14	DDR2 SO-DIMM_0
15	DDR2 SO-DIMM_1
16	DDR2 ADDRESS TERMINATION
17	LVDS & INVERTER CONN
18	VGA CONN
19	ICH7M--CPU,IDE,AUDIO
20	ICH7M--GPIO
21	ICH7M--PCI,PCI-E,USB
22	ICH7M--VCC,GND
23	HDD & CD-ROM CONN
24	USB PORT
25	B/T & F/P
26	B TO B CONN(M)
27	CARDBUS R5C841
28	PCMCIA SOCKET
29	PCI-E--LAN_RTL8101E
30	AZALIA - ALC660-GR
31	AUDIO_AMPLIFIER
32	MICROPHONE
33	NEWCARD
34	EC-IT8510E
35	ISA ROM & Touch Pad & KB& FP
36	Card Reader GL817E
37	DISCHARGE
38	Instant Key & FFC CONN
39	LEDs
40	EMPTY
41	EMPTY
42	EMPTY
43	EMPTY
44	EMPTY
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46	DC & BAT IN
47	EMPTY
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49	History(2)
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50	POWER_VCORE
51	POWER_SYSTEM
52	POWER_I/O_1.8V & 1.05VS
53	POWER_I/O_DDR & VTT
54	POWER_I/O_VTT & +2.5VS
55	POWER_VGA_CORE(Empty)
56	POWER_VGA_RAM(Empty)
57	POWER_CHARGER
58	POWER_PIC(Empty)
59	POWER_DETECT
60	POWER_PROTECT
61	POWER_LOAD SWITCH
62	POWER_FLOWCHART
63	POWER_SIGNAL

<Variant Name>

ASUSTeK COMPUTER INC

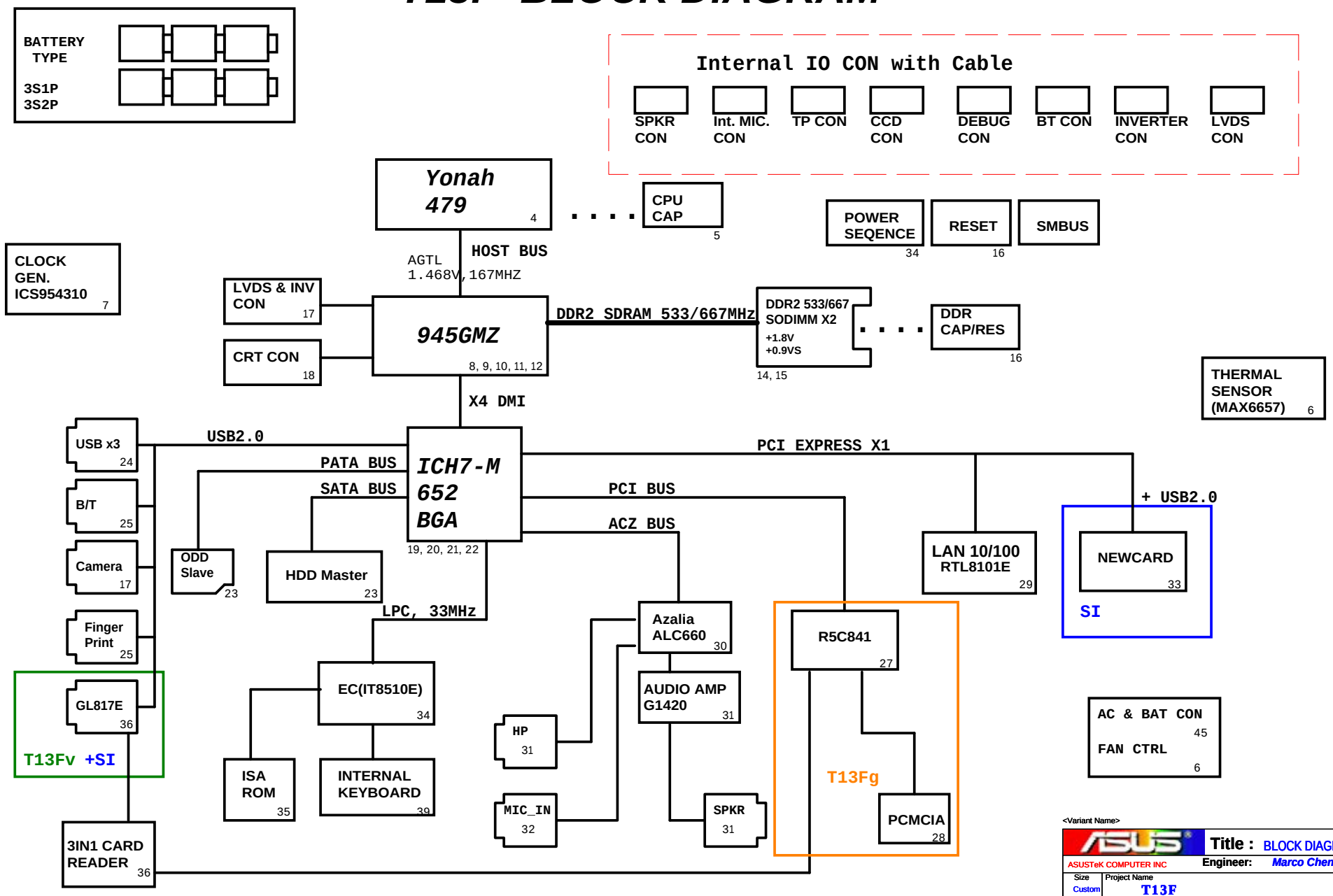
Title : PAGE REF.

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 1 of 63

T13F BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 2 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	CR_DRIVER#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PCI_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	CR_POWER#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	PWRLMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	N/A	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTER_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

ICH7M_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

ICH7M_PCI_DEVICE:

PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

ICH7M_GPIO

Pin			Use As	Signal Name	Power
GPIO 00	i		GPI	PM_BMBUSY#	+3VS
GPIO 01	i		GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i		GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i		GPO	BT_LED_EN	+3VS
GPIO 07	i		GPI	N/A	+3VS
GPIO 08	i		GPI	EXTSMI#	+3VSUS
GPIO 09	i		GPI	N/A	+3VSUS
GPIO 10	i		GPI	N/A	+3VSUS
GPIO 11	i		Native	SMB_ALERT#	+3VSUS
GPIO 12	i		GPI	KBC_SCI#	+3VSUS
GPIO 13	i		GPI	N/A	+3VSUS
GPIO 14	i		GPI	N/A	+3VSUS
GPIO 15	i		GPO	802_LED_EN	+3VSUS
GPIO 16	O	0	GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1	GPO	PCI_GNT#5	+3VS
GPIO 18	O	1	GPO	STP_PCI#	+3VS
GPIO 19	i	1	GPI	N/A	+3VS
GPIO 20	O	1	GPO	STP_CPU#	+3VS
GPIO 21	i	1	GPO	N/A	+3VS
GPIO 22	i	1	Native	PCI_REQ#4	+3VS
GPIO 23	i	1	Native	N/A	+3VS
GPIO 24	O	0	GPO	MSK_PCIRST	+3VSUS
GPIO 25	O	1	GPO	CB_SD#	+3VSUS
GPIO 26	O	0	GPO	BT_ON#	+3VSUS
GPIO 27	O	0	GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0	GPO	MEMROM/YONAH#	+3VSUS
GPIO 29	i	0	Native	USB_OC#5	+3VSUS
GPIO 30	i	0	Native	USB_OC#6	+3VSUS
GPIO 31	i	0	Native	USB_OC#7	+3VSUS
GPIO 32	O	1	GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1	GPO	N/A	+3VS
GPIO 34	O	0	GPO	CPU_Select	+3VS
GPIO 35	O	0	GPO	N/A	+3VS
GPIO 36	i	0	GPO	N/A	+3VS
GPIO 37	i	0	GPI	PCB_ID0	+3VS
GPIO 38	i	0	GPI	PCB_ID1	+3VS
GPIO 39	i	0	GPI	PCB_ID2	+3VS
GPIO [40:47]			NA	NA	NA
GPIO 48			Native	PCI_GNT#4	+3VS
GPIO 49			Native	H_PWRGD	+VCORE

<Variant Name>

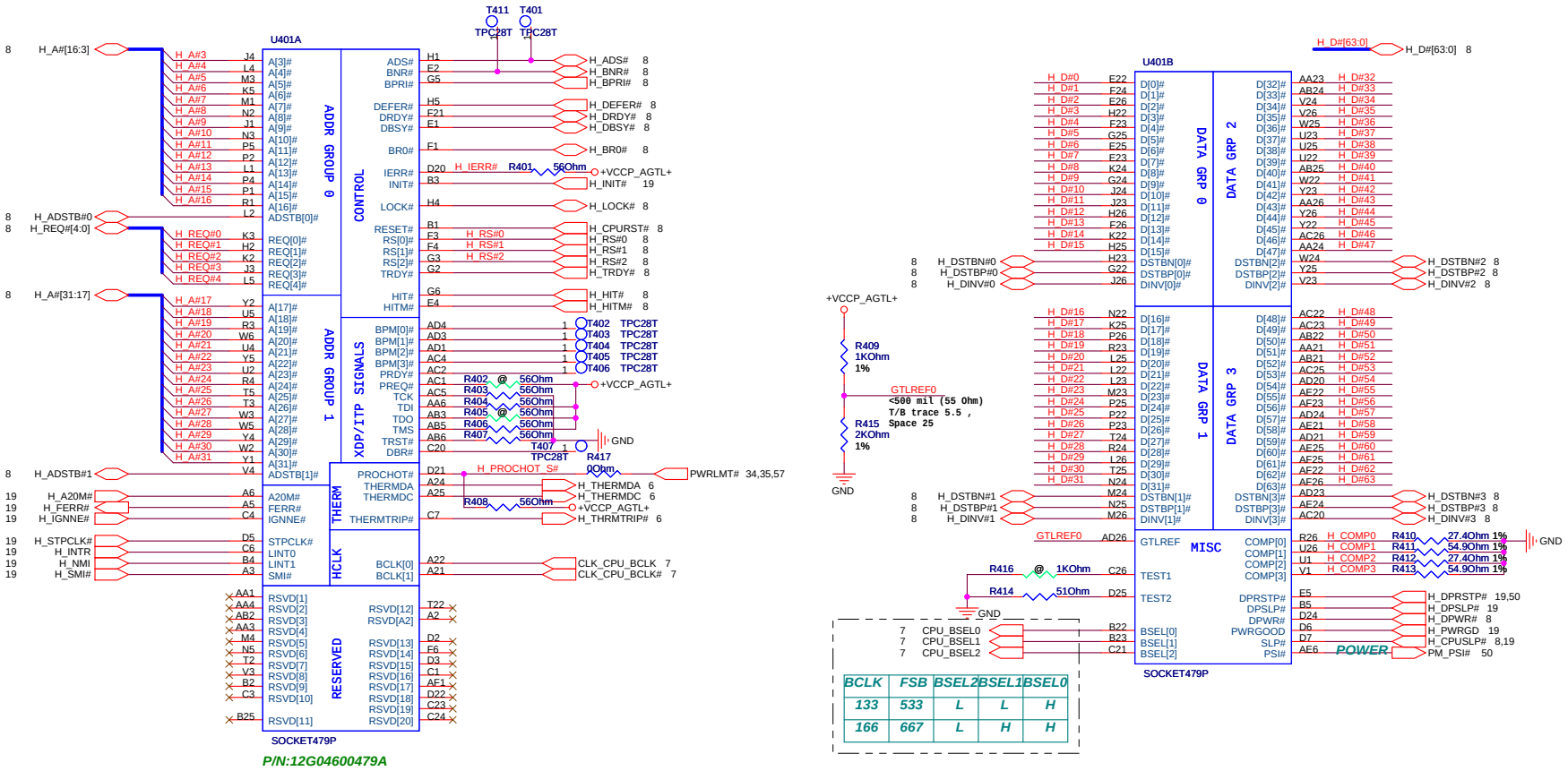
ASUSTeK COMPUTER INC

Title : Schematic data

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 3 of 63


U401A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
SOCKET479P
P/N:12G04600479A
U401B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET479P
POWER
GTLREF0
<500 mil (55 Ohm)
T/B trace 5.5 ,
Space 25
R409 1KOhm 1%
R415 2KOhm 1%
R414 51Ohm
R416 @ 1KOhm
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H

<Variant Name>
Title : YONAH CPU (1)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size: Custom
Project Name: T13F
Rev: 1.11
Date: Tuesday, August 22, 2006
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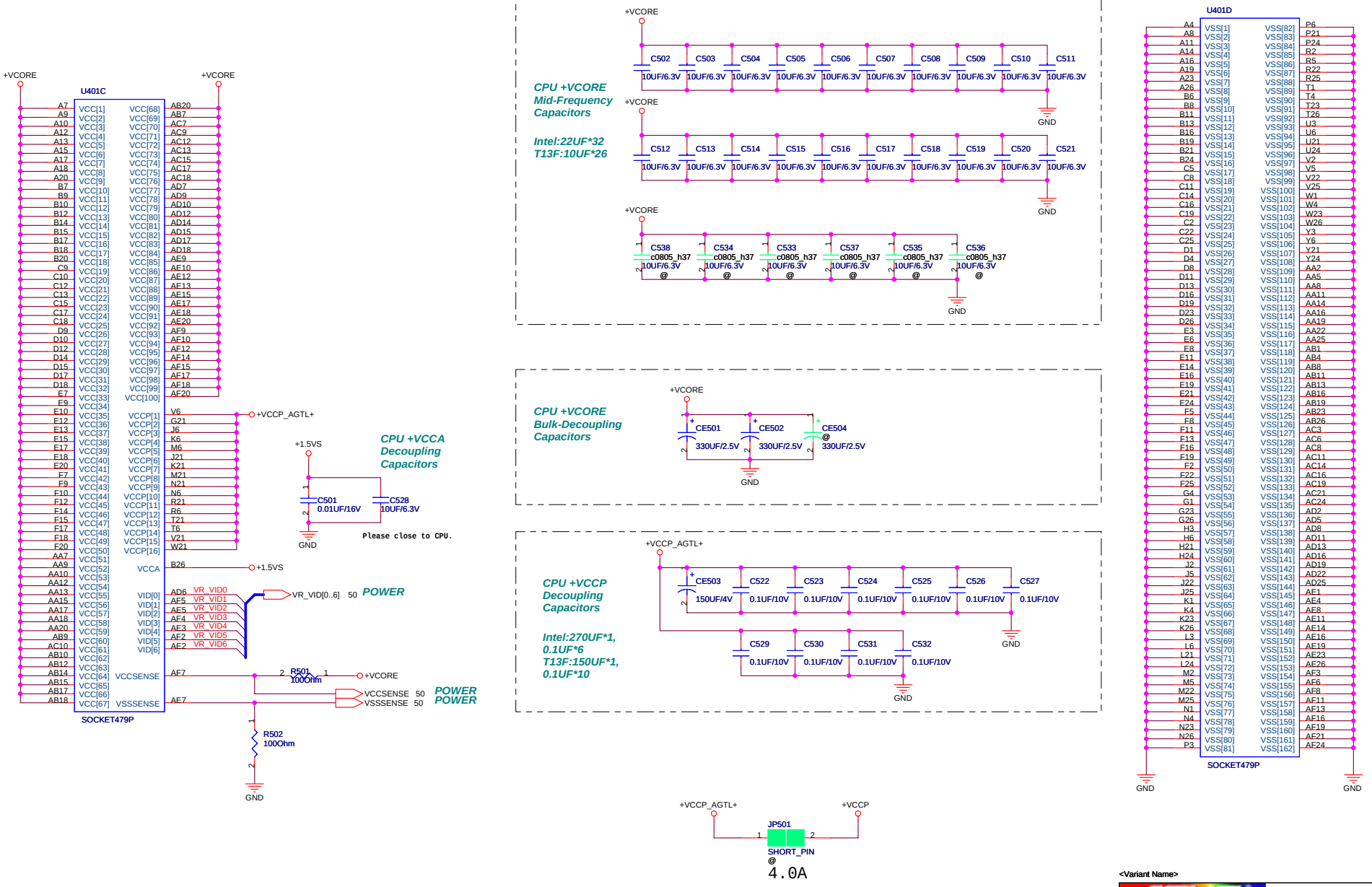
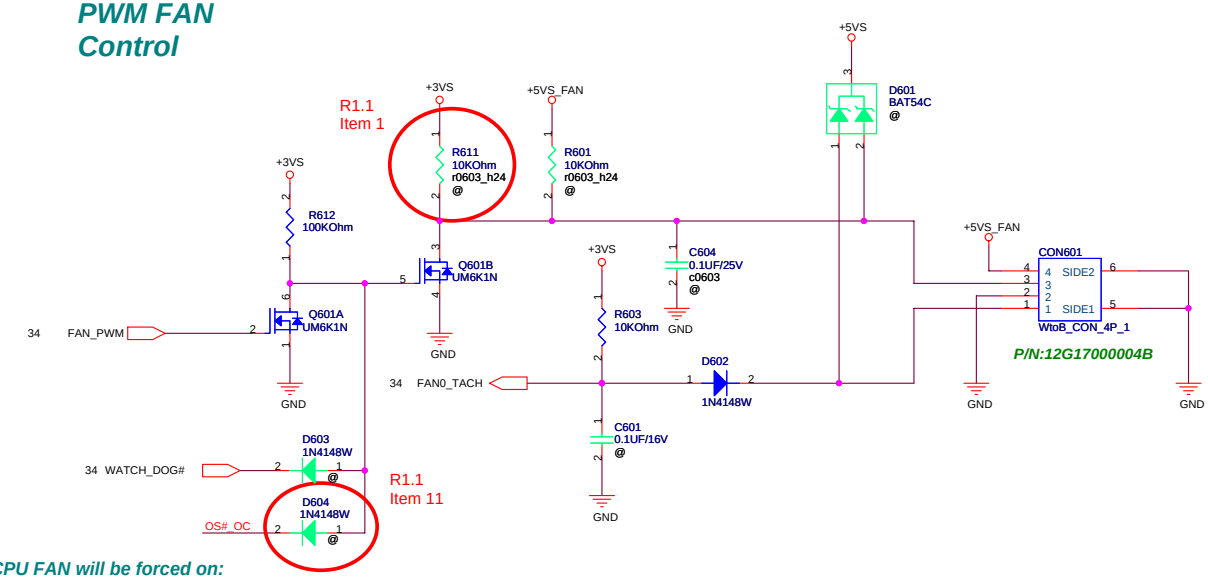
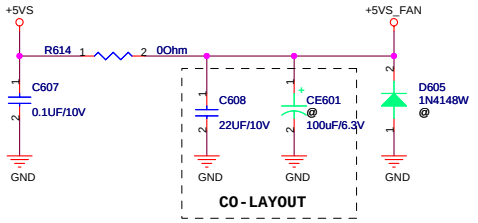


<Variant Name>

ASUSTeK COMPUTER INC	Title : YONAH CPU (2)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 5 of 63	

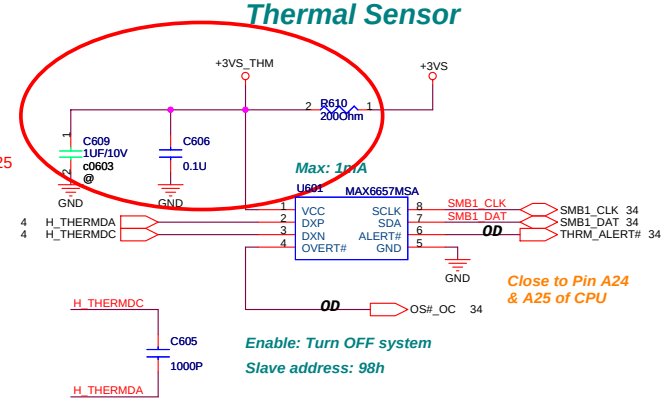
PWM FAN Control

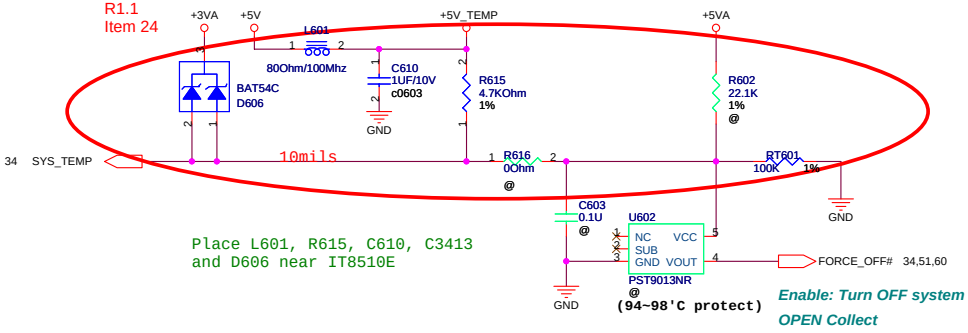


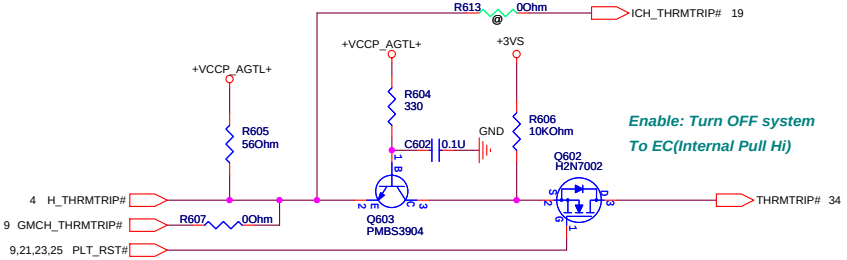


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

Thermal Sensor

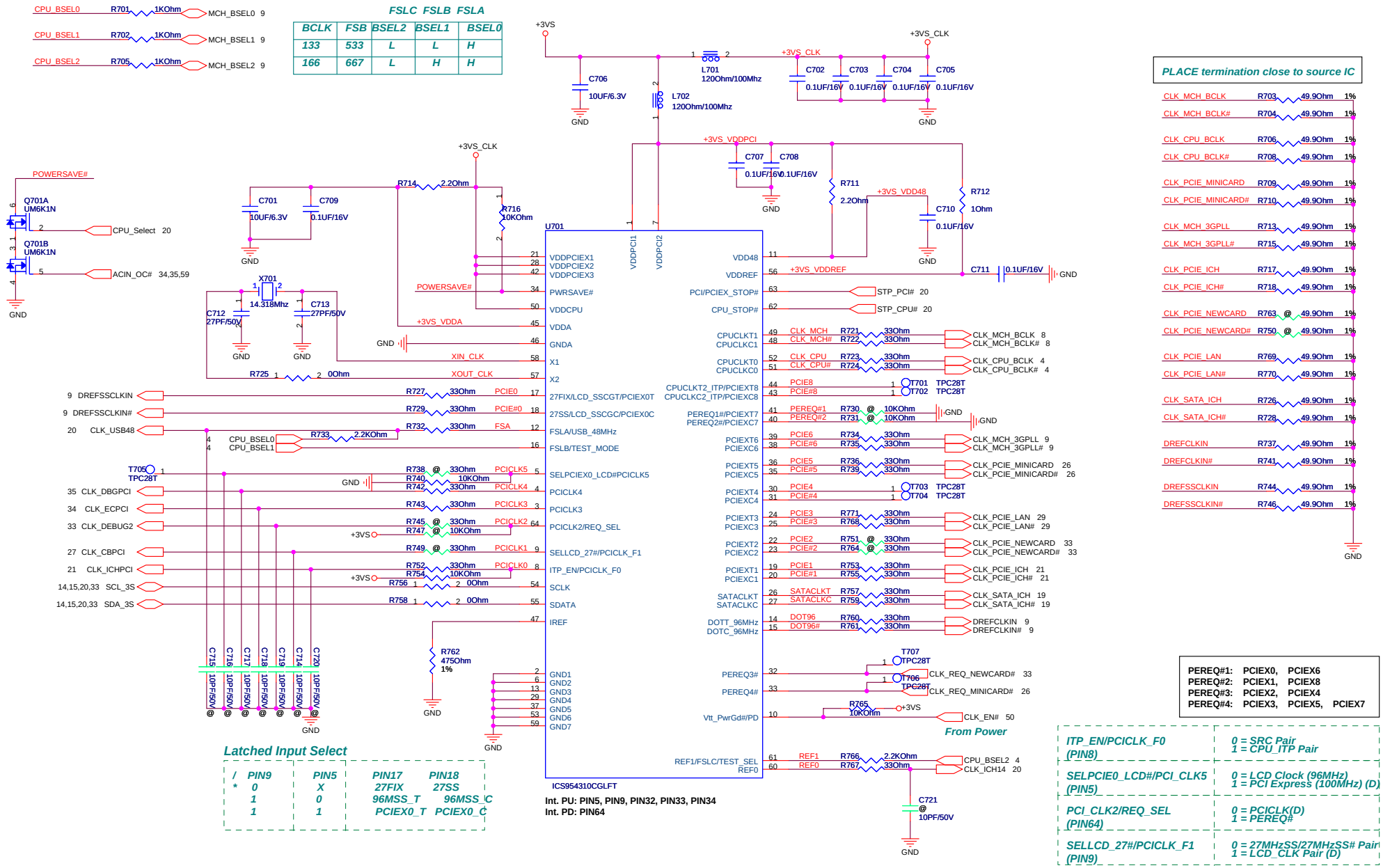






<variant_name>

ASUSTeK COMPUTER INC	Title : FAN_CTRL&Thernal	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 6 of 63	


CPU_BSEL0 R701 1KOhm MCH_BSEL0 9
CPU_BSEL1 R702 1KOhm MCH_BSEL1 9
CPU_BSEL2 R705 1KOhm MCH_BSEL2 9
FSLC FSLB FSLA
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
+3VS
+3VS_CLK
C706 10UF/6.3V
L701 120Ohm/100Mhz
L702 120Ohm/100Mhz
C702 C703 C704 C705 0.1UF/16V
+3VS_VDDPCI
C707 C708 0.1UF/16V
R711 2.2Ohm
+3VS_VDD48
R712 1Ohm
C710 0.1UF/16V
C711 0.1UF/16V
PLACE termination close to source IC
CLK_MCH_BCLK R703 49.9Ohm 1%
CLK_MCH_BCLK# R704 49.9Ohm 1%
CLK_CPU_BCLK R706 49.9Ohm 1%
CLK_CPU_BCLK# R708 49.9Ohm 1%
CLK_PCIE_MINICARD R709 49.9Ohm 1%
CLK_PCIE_MINICARD# R710 49.9Ohm 1%
CLK_MCH_3GPLL R713 49.9Ohm 1%
CLK_MCH_3GPLL# R715 49.9Ohm 1%
CLK_PCIE_ICH R717 49.9Ohm 1%
CLK_PCIE_ICH# R718 49.9Ohm 1%
CLK_PCIE_NEWCARD R763 @ 49.9Ohm 1%
CLK_PCIE_NEWCARD# R750 @ 49.9Ohm 1%
CLK_PCIE_LAN R769 49.9Ohm 1%
CLK_PCIE_LAN# R770 49.9Ohm 1%
CLK_SATA_ICH R726 49.9Ohm 1%
CLK_SATA_ICH# R728 49.9Ohm 1%
DREFCLKIN R737 49.9Ohm 1%
DREFCLKIN# R741 49.9Ohm 1%
DREFSSCLKIN R744 49.9Ohm 1%
DREFSSCLKIN# R746 49.9Ohm 1%
POWERSAVE#
Q701A UM6K1N
Q701B UM6K1N
CPU_Select 20
ACIN_OC# 34,35,59
C701 10UF/6.3V
C709 0.1UF/16V
R714 2.2Ohm
R716 10KOhm
X701 14.318Mhz
C712 27PF/50V
C713 27PF/50V
+3VS_VDDA
XIN_CLK
XOUT_CLK
R725 1 2 0Ohm
U701
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
CPUCLKT2_ITP/PCIEXT8
CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7
PEREQ2#/PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXT1
PCIEXC1
SATACLKT
SATACLKC
DOTT_96MHz
DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
ICS954310CGLFT
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64
From Power
PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7
Latched Input Select
/ PIN9 PIN5 PIN17 PIN18
* 0 X 27FIX 27SS
1 0 96MSS_T 96MSS_C
1 1 PCIEX0_T PCIEX0_C
ITP_EN/PCICLK_F0 (PIN8)
0 = SRC Pair
1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)
0 = PCICLK(D)
1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair (D)
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICS954310
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
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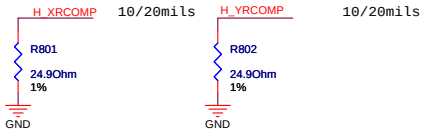
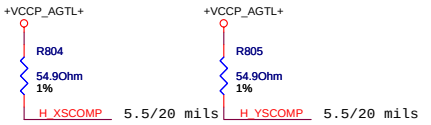
RCOMP

For Calibrating FSB I/O Buffer



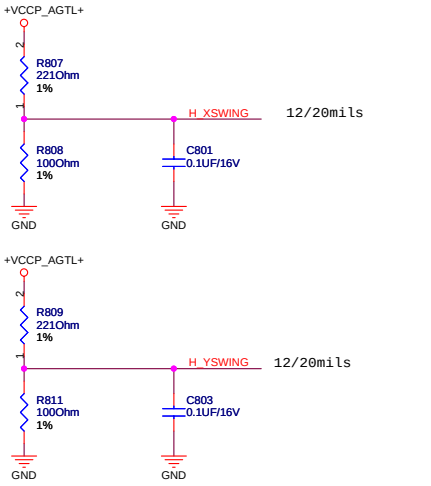
SCOMP

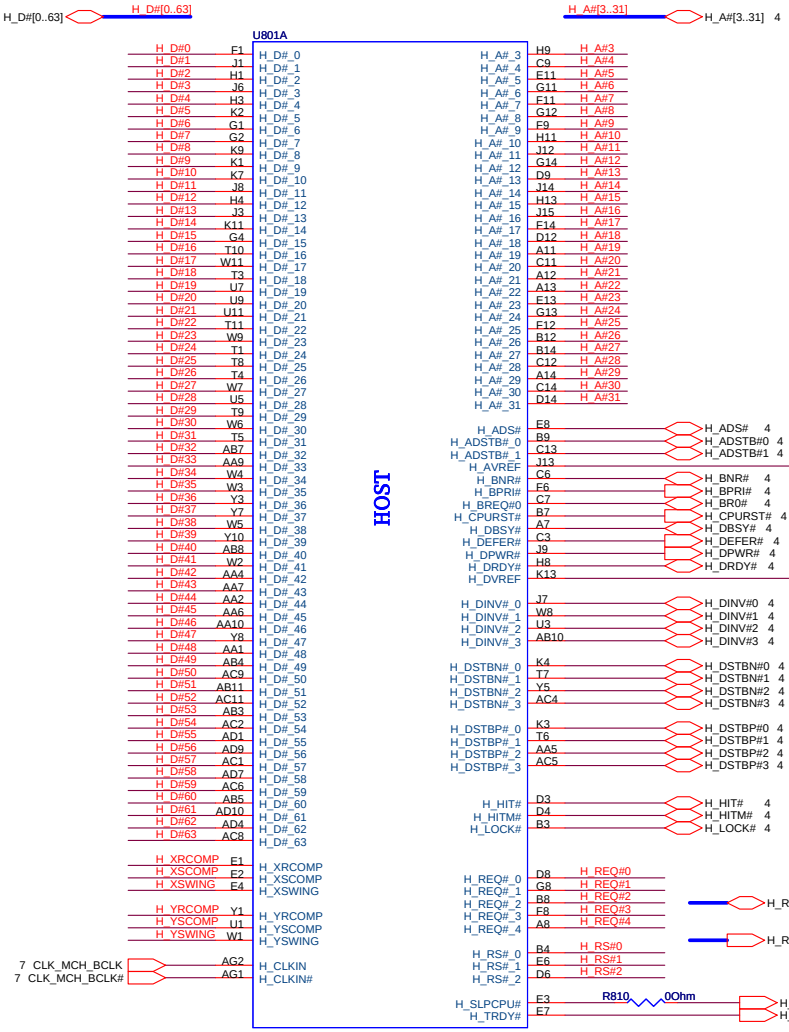
For Slew Rate Compensation on the FSB



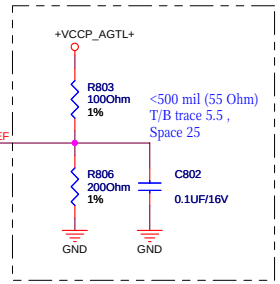
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit





AGTL+ I/O Voltage Reference



<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga--CPU	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
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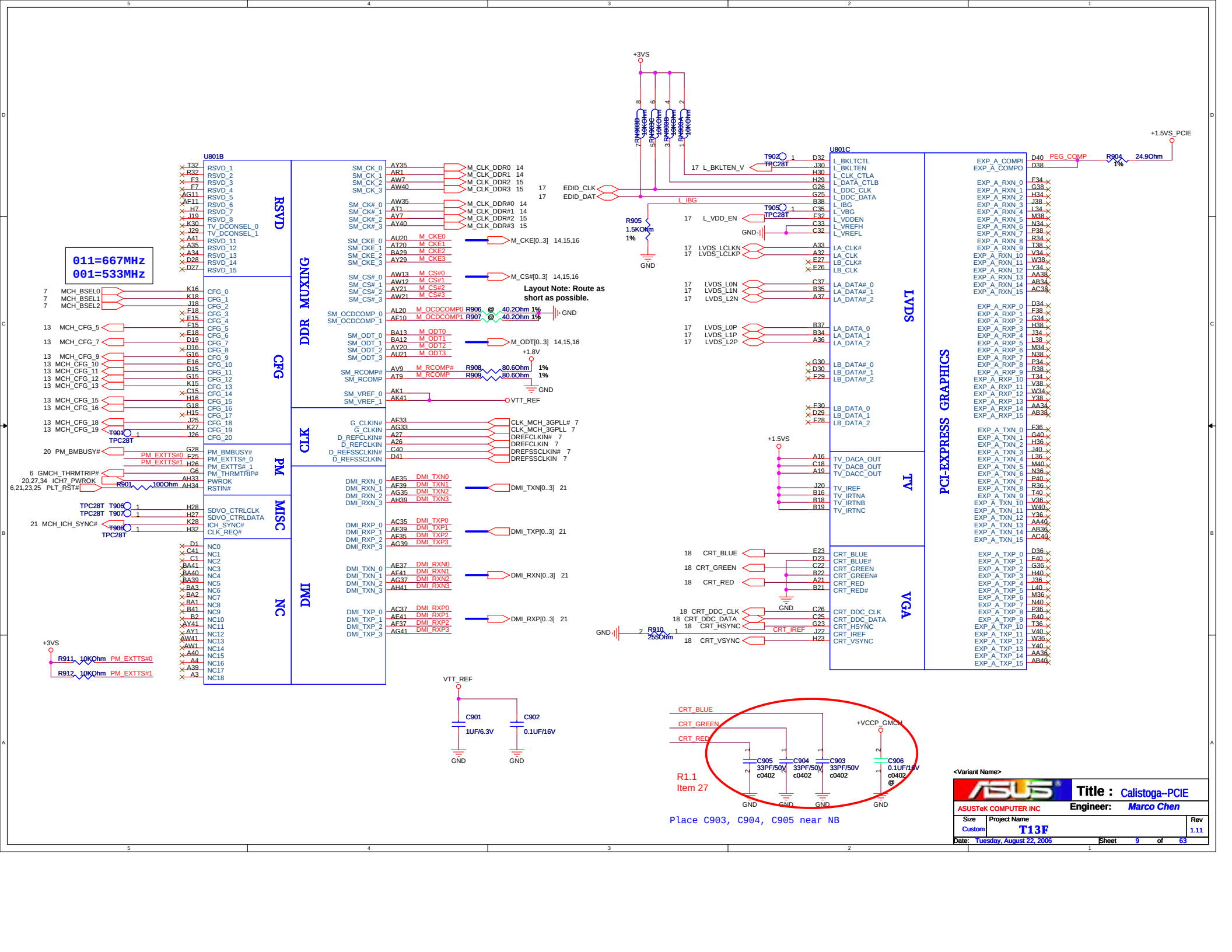
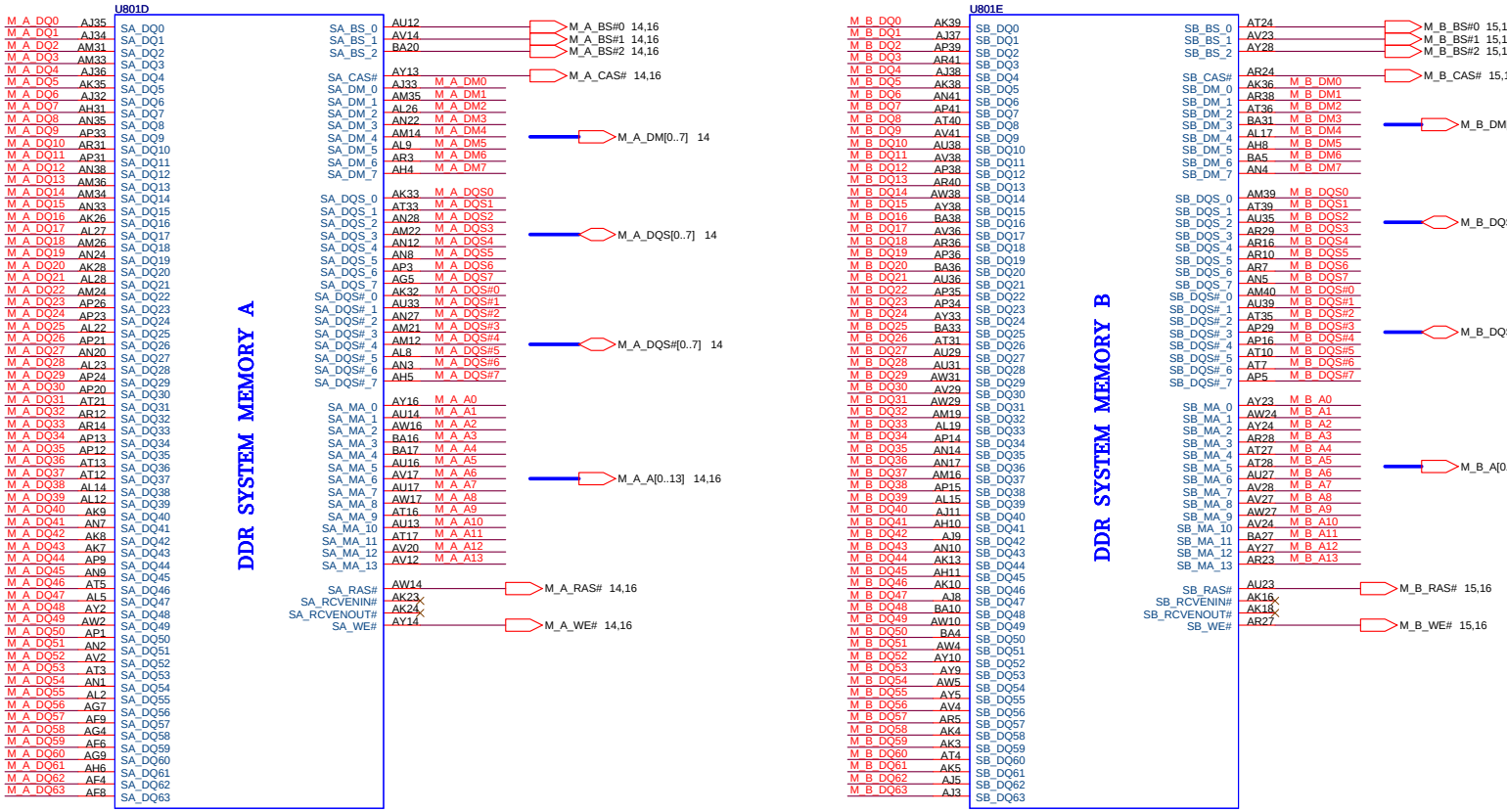

011=667MHz
001=533MHz
U801B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
U801C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
Layout Note: Route as short as possible.
Place C903, C904, C905 near NB
R1.1
Item 27
Title : Calistoga--PCIE
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13F
Date: Tuesday, August 22, 2006
Sheet 9 of 63

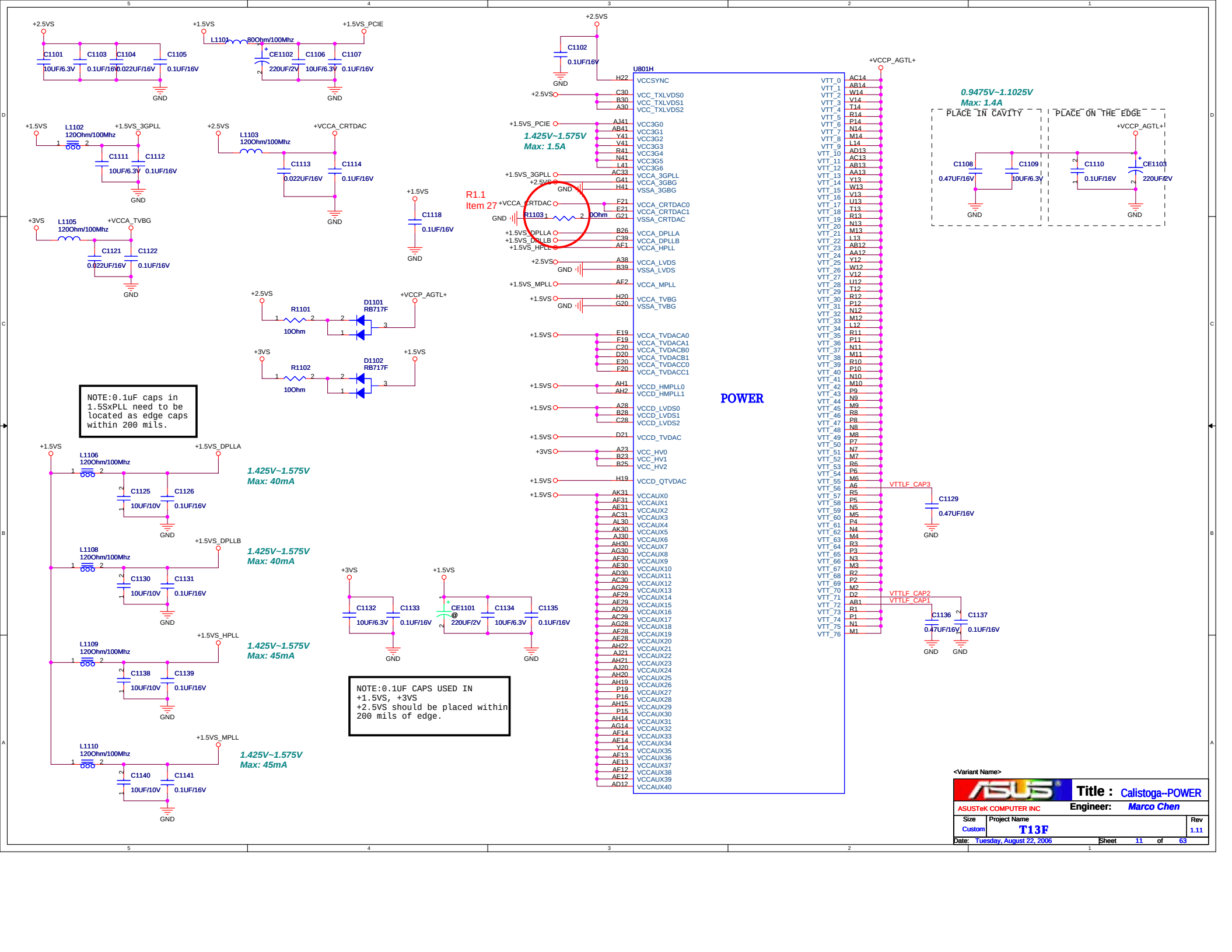
14 M_A_DQ[0..63]

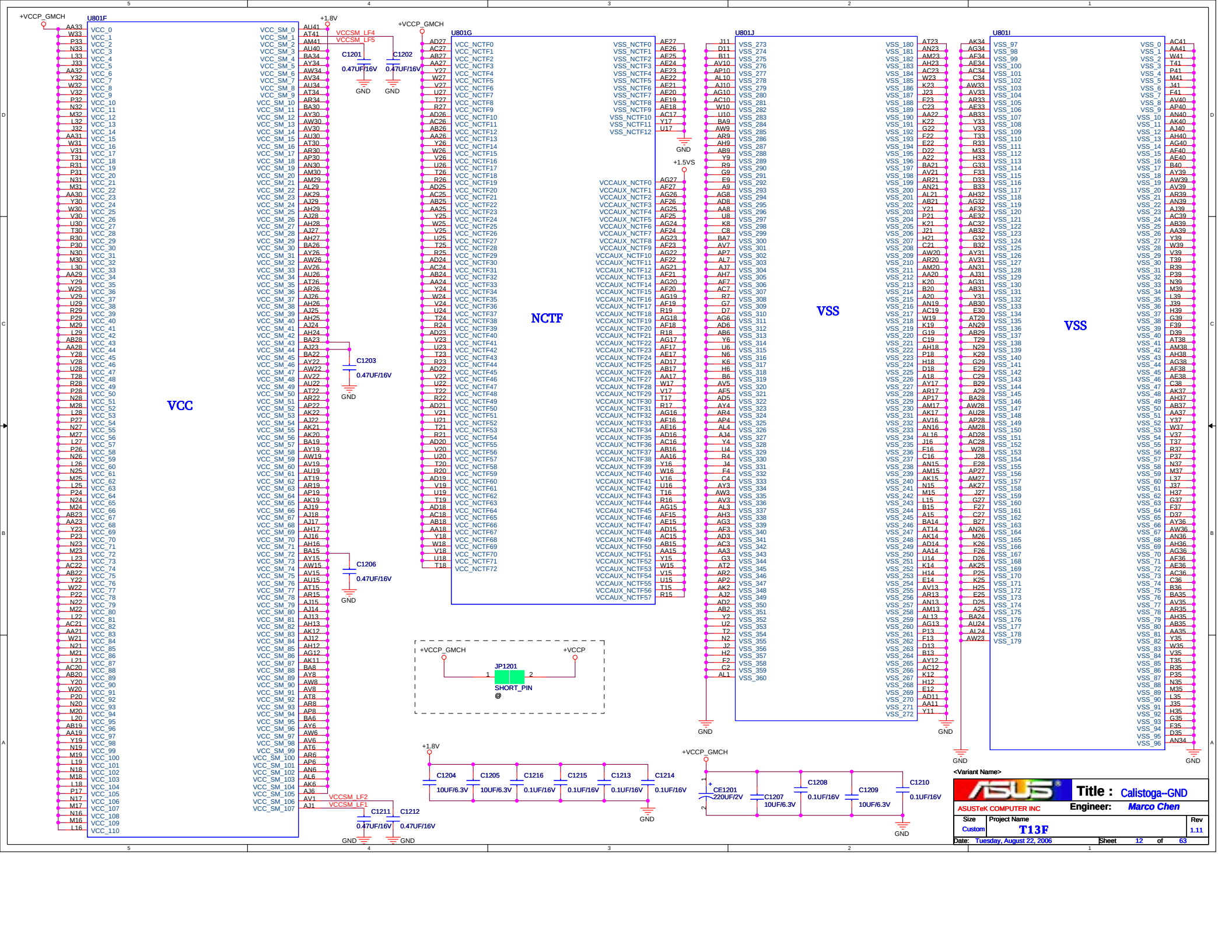
15 M_B_DQ[0..63]

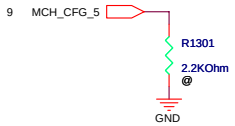


<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga--DDR2	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 10 of 63	

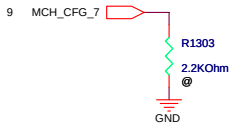

+2.5VS
C1101
10UF/6.3V
C1103
0.1UF/16V
C1104
0.022UF/16V
C1105
0.1UF/16V
GND
+1.5VS
L1101
80Ohm/100Mhz
+1.5VS_PCIE
CE1102
220UF/2V
C1106
10UF/6.3V
C1107
0.1UF/16V
GND
+1.5VS
L1102
120Ohm/100Mhz
+1.5VS_3GPLL
C1111
10UF/6.3V
C1112
0.1UF/16V
GND
+2.5VS
L1103
120Ohm/100Mhz
+VCCA_CRTDAC
C1113
0.022UF/16V
C1114
0.1UF/16V
GND
+1.5VS
C1118
0.1UF/16V
GND
+3VS
L1105
120Ohm/100Mhz
+VCCA_TVBG
C1121
0.022UF/16V
C1122
0.1UF/16V
GND
+2.5VS
R1101
10Ohm
D1101
RB717F
+VCCP_AGTL+
+3VS
R1102
10Ohm
D1102
RB717F
+1.5VS
NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.
+1.5VS
L1106
120Ohm/100Mhz
+1.5VS_DPLLA
C1125
10UF/10V
C1126
0.1UF/16V
GND
1.425V~1.575V
Max: 40mA
+1.5VS
L1108
120Ohm/100Mhz
+1.5VS_DPLLB
C1130
10UF/10V
C1131
0.1UF/16V
GND
1.425V~1.575V
Max: 40mA
+1.5VS
L1109
120Ohm/100Mhz
+1.5VS_HPLL
C1138
10UF/10V
C1139
0.1UF/16V
GND
1.425V~1.575V
Max: 45mA
+1.5VS
L1110
120Ohm/100Mhz
+1.5VS_MPLL
C1140
10UF/10V
C1141
0.1UF/16V
GND
1.425V~1.575V
Max: 45mA
+3VS
C1132
10UF/6.3V
C1133
0.1UF/16V
GND
+1.5VS
CE1101
@
220UF/2V
C1134
10UF/6.3V
C1135
0.1UF/16V
GND
NOTE:0.1UF CAPS USED IN +1.5VS, +3VS +2.5VS should be placed within 200 mils of edge.
+2.5VS
C1102
0.1UF/16V
GND
U801H
H22 VCCSYNC
+2.5VS
C30 VCC_TXLVDS0
B30 VCC_TXLVDS1
A30 VCC_TXLVDS2
+1.5VS_PCIE
AJ41 VCC3G0
AB41 VCC3G1
Y41 VCC3G2
V41 VCC3G3
R41 VCC3G4
N41 VCC3G5
L41 VCC3G6
1.425V~1.575V
Max: 1.5A
+1.5VS_3GPLL
AC33 VCCA_3GPLL
+2.5VS
G41 VCCA_3GBG
GND
H41 VSSA_3GBG
R1.1
Item 27
+VCCA_CRTDAC
F21 VCCA_CRTDAC0
E21 VCCA_CRTDAC1
GND
R1103 10Ohm
G21 VSSA_CRTDAC
+1.5VS_DPLLA
B26 VCCA_DPLLA
+1.5VS_DPLLB
C39 VCCA_DPLLB
+1.5VS_HPLL
AF1 VCCA_HPLL
+2.5VS
A38 VCCA_LVDS
GND
B39 VSSA_LVDS
+1.5VS_MPLL
AF2 VCCA_MPLL
+1.5VS
H20 VCCA_TVBG
GND
G20 VSSA_TVBG
+1.5VS
E19 VCCA_TVDACA0
F19 VCCA_TVDACA1
C20 VCCA_TVDACB0
D20 VCCA_TVDACB1
E20 VCCA_TVDACC0
F20 VCCA_TVDACC1
+1.5VS
AH1 VCCD_HMPLL0
AH2 VCCD_HMPLL1
+1.5VS
A28 VCCD_LVDS0
B28 VCCD_LVDS1
C28 VCCD_LVDS2
+1.5VS
D21 VCCD_TVDAC
+3VS
A23 VCC_HV0
B23 VCC_HV1
B25 VCC_HV2
+1.5VS
H19 VCCD_QTVDAC
+1.5VS
AK31 VCCAUX0
AF31 VCCAUX1
AE31 VCCAUX2
AC31 VCCAUX3
AL30 VCCAUX4
AK30 VCCAUX5
AJ30 VCCAUX6
AH30 VCCAUX7
AG30 VCCAUX8
AF30 VCCAUX9
AE30 VCCAUX10
AD30 VCCAUX11
AC30 VCCAUX12
AG29 VCCAUX13
AF29 VCCAUX14
AE29 VCCAUX15
AD29 VCCAUX16
AC29 VCCAUX17
AG28 VCCAUX18
AE28 VCCAUX19
AE28 VCCAUX20
AH22 VCCAUX21
AJ21 VCCAUX22
AH21 VCCAUX23
AJ20 VCCAUX24
AH20 VCCAUX25
AH19 VCCAUX26
P19 VCCAUX27
P16 VCCAUX28
AH15 VCCAUX29
P15 VCCAUX30
AH14 VCCAUX31
AG14 VCCAUX32
AF14 VCCAUX33
AE14 VCCAUX34
Y14 VCCAUX35
AF13 VCCAUX36
AE13 VCCAUX37
AE12 VCCAUX38
AE12 VCCAUX39
AD12 VCCAUX40
POWER
+VCCP_AGTL+
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 V14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1
VTTLF_CAP3
C1129
0.47UF/16V
GND
VTTLF_CAP2
VTTLF_CAP1
C1136
0.47UF/16V
C1137
0.1UF/16V
GND
GND
0.9475V~1.1025V
Max: 1.4A
PLACE IN CAVITY
C1108
0.47UF/16V
C1109
10UF/6.3V
GND
PLACE ON THE EDGE
+VCCP_AGTL+
C1110
0.1UF/16V
CE1103
220UF/2V
GND
<Variant Name>
Title : Calistoga--POWER
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 11 of 63


U801F
VCC
U801G
NCTF
U801J
VSS
U801I
VSS
+VCCP_GMCH
+1.8V
+1.5VS
VCCSM_LF4
VCCSM_LF5
VCCSM_LF2
VCCSM_LF1
C1201 0.47UF/16V
C1202 0.47UF/16V
C1203 0.47UF/16V
C1206 0.47UF/16V
C1211 0.47UF/16V
C1212 0.47UF/16V
JP1201
SHORT_PIN
+VCCP
C1204 10UF/6.3V
C1205 10UF/6.3V
C1216 0.1UF/16V
C1215 0.1UF/16V
C1213 0.1UF/16V
C1214 0.1UF/16V
CE1201 220UF/2V
C1207 10UF/6.3V
C1208 0.1UF/16V
C1209 10UF/6.3V
C1210 0.1UF/16V
GND
<Variant Name>
Title : Calistoga--GND
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 12 of 63



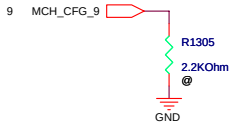
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



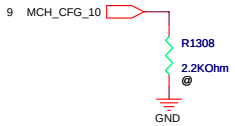
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



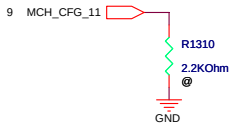
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

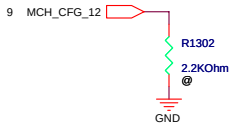
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

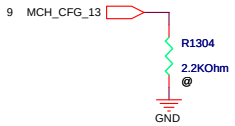
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

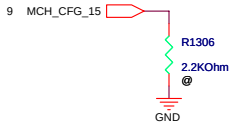
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG[13:12] : GMCH TEST MODE SELECT

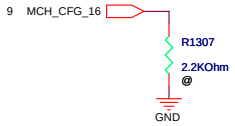
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)





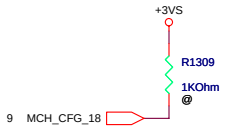
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



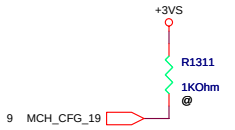
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V



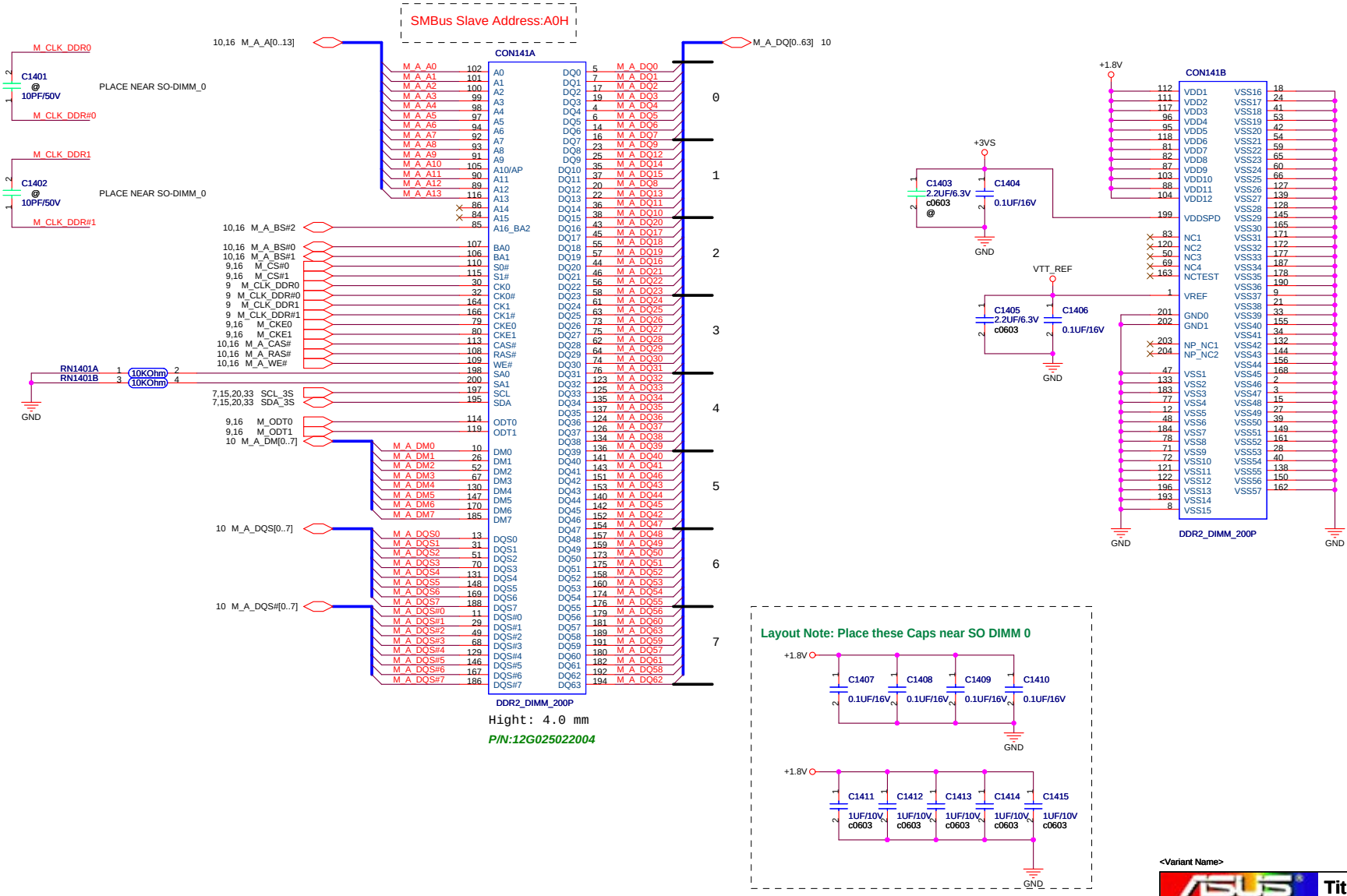
CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga--Strap	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 13 of 63	

DDR2 HAD SWAPED.

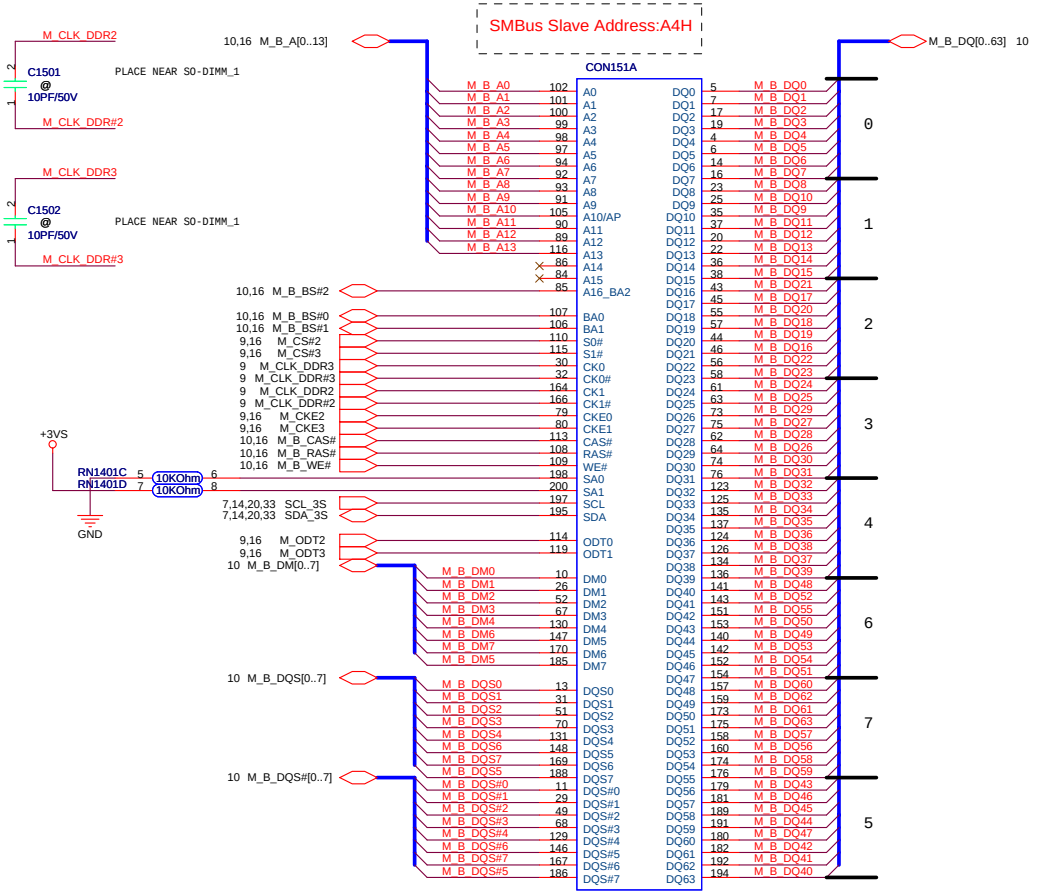


<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_0	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 14 of 63	

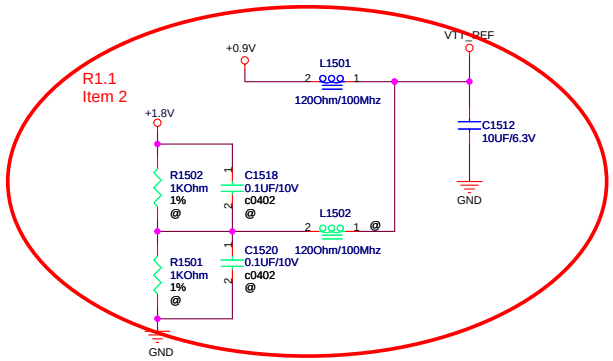
DDR2 HAD SWAPED.

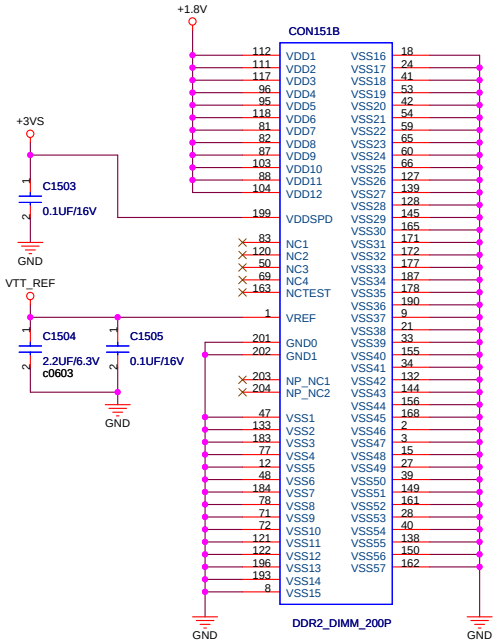
SMBus Slave Address:A4H

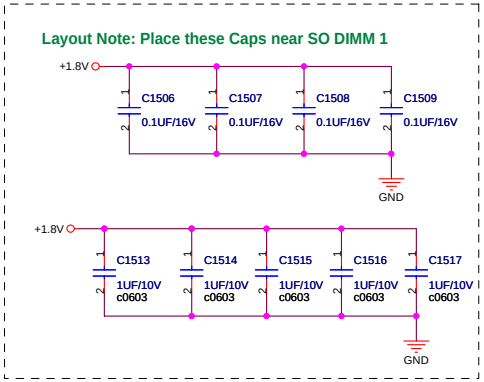


Hight: 9.2 mm

P/N:12G025C22004







<Variant Name>

ASUSTeK COMPUTER INC

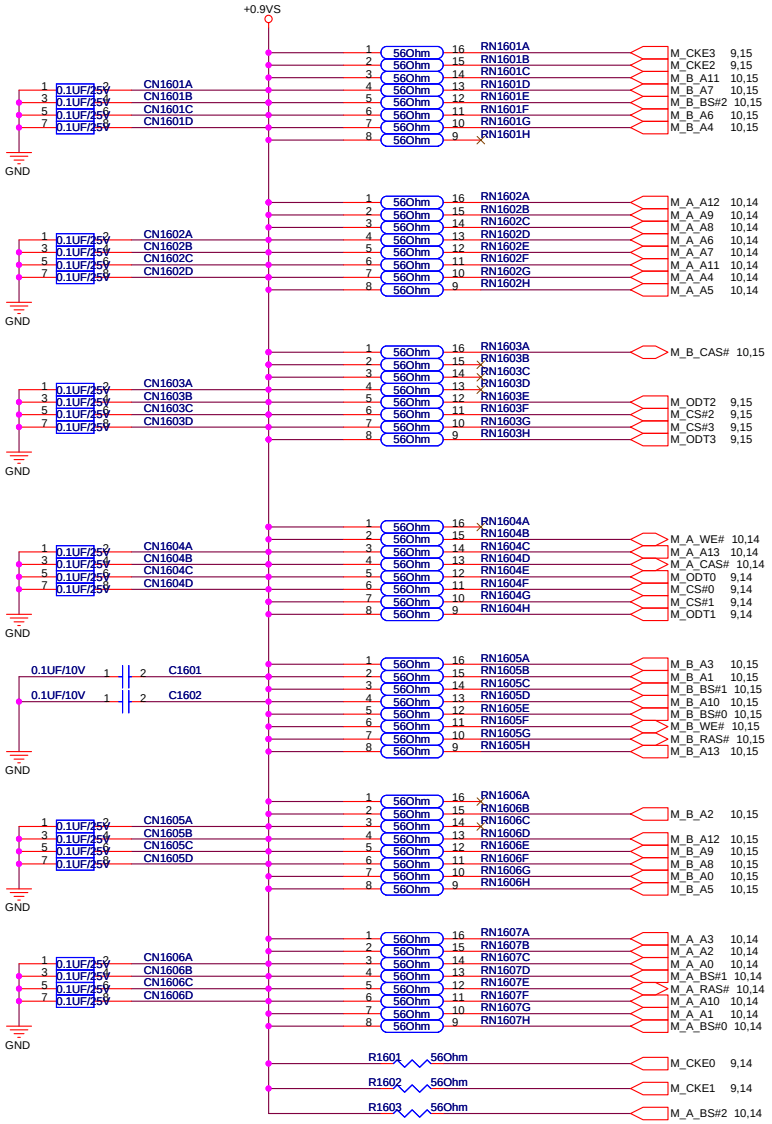
Title : DDR2 SO-DIMM_1

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 15 of 63

DDR2 HAD SWAPED.



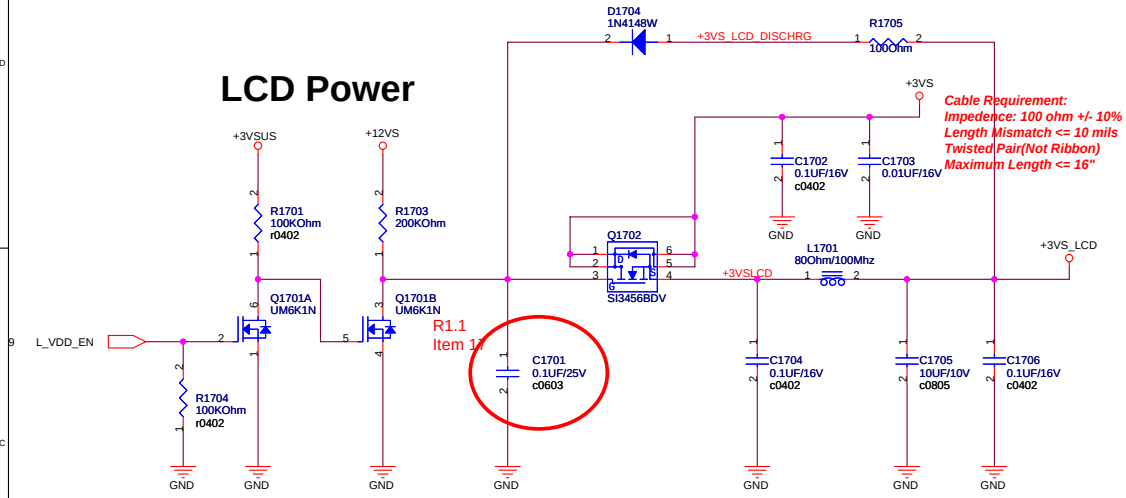
Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 TERMINATION	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 16 of 63	

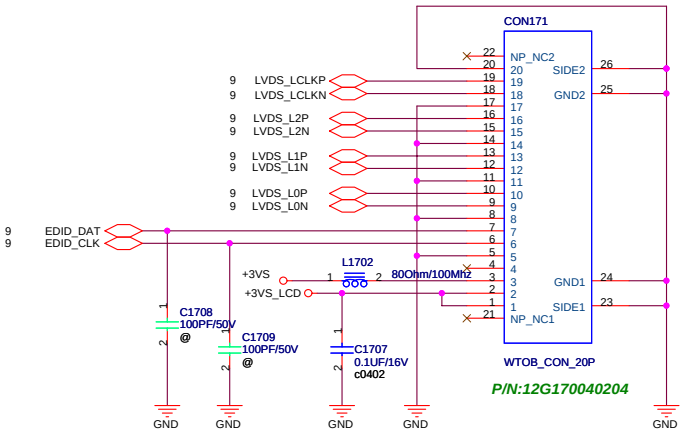
LCD Backlight Control

LCD Power

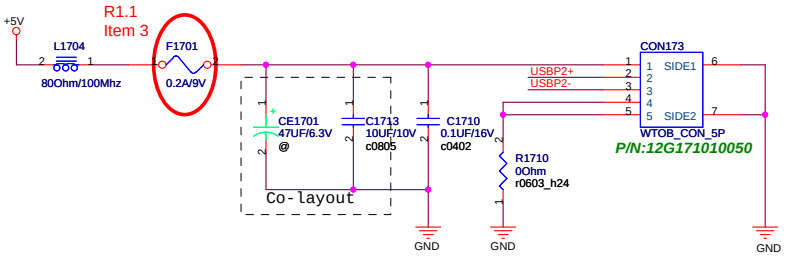


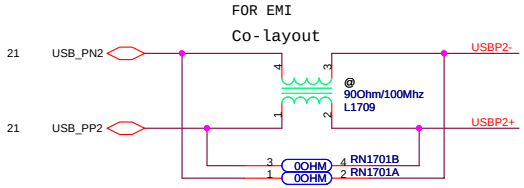
PR_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

LCD LVDS Interface

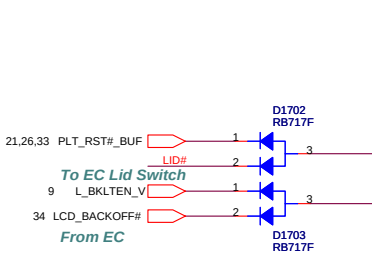


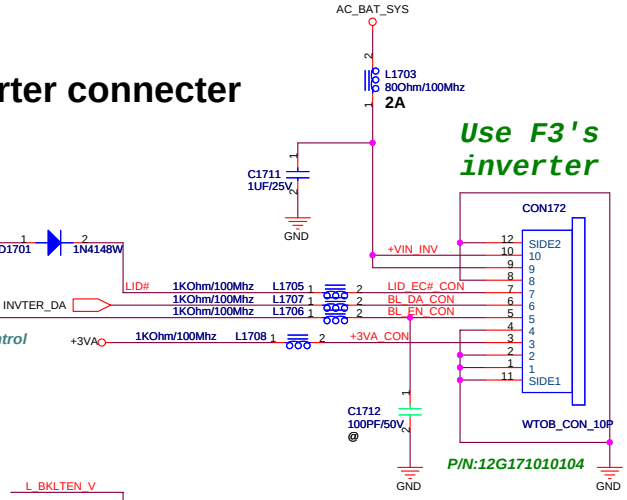
CCD connecter



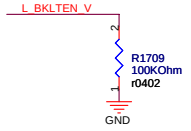


Inverter connecter





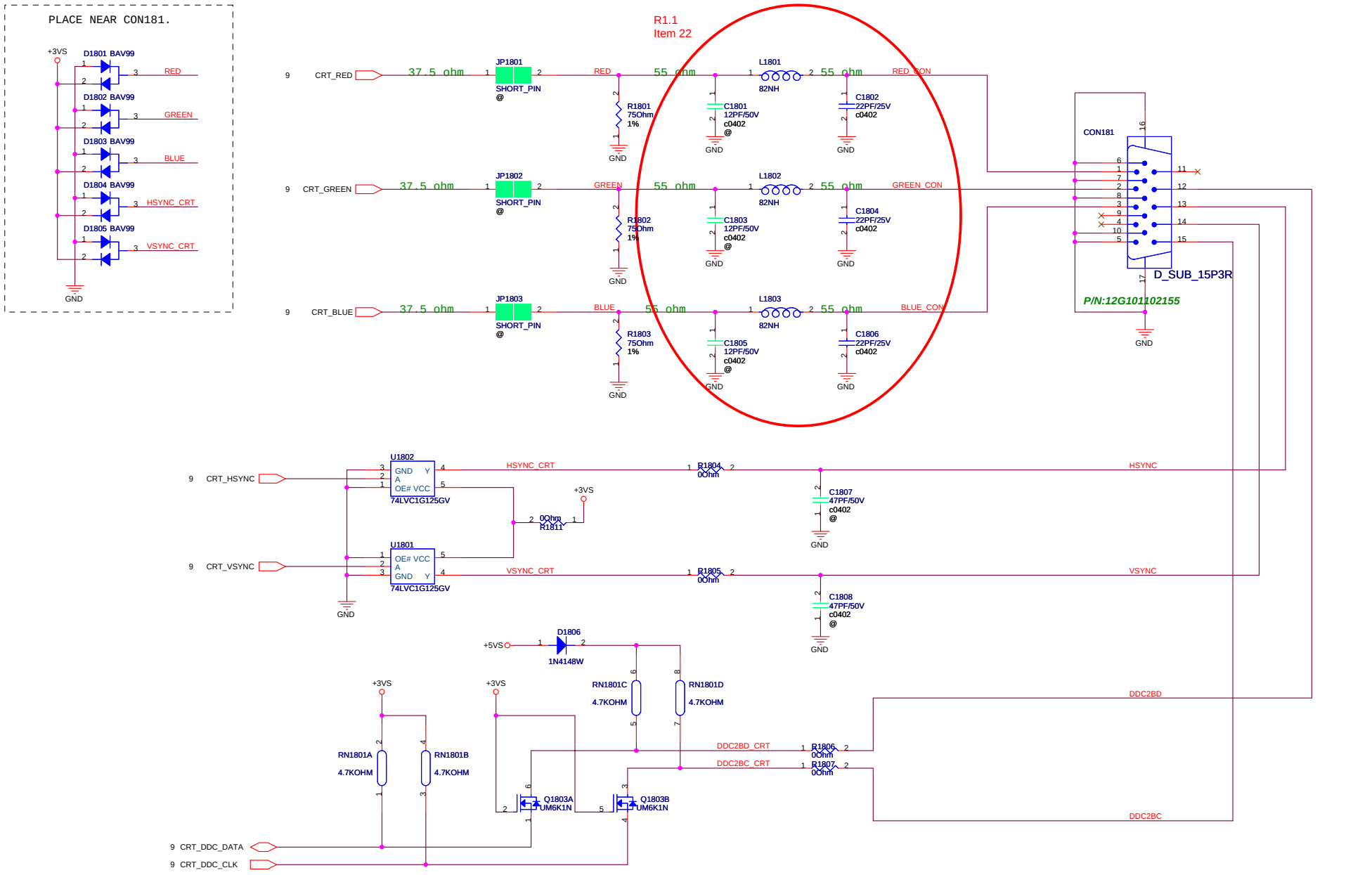
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 17 of 63	

CRT



<Variant Name>

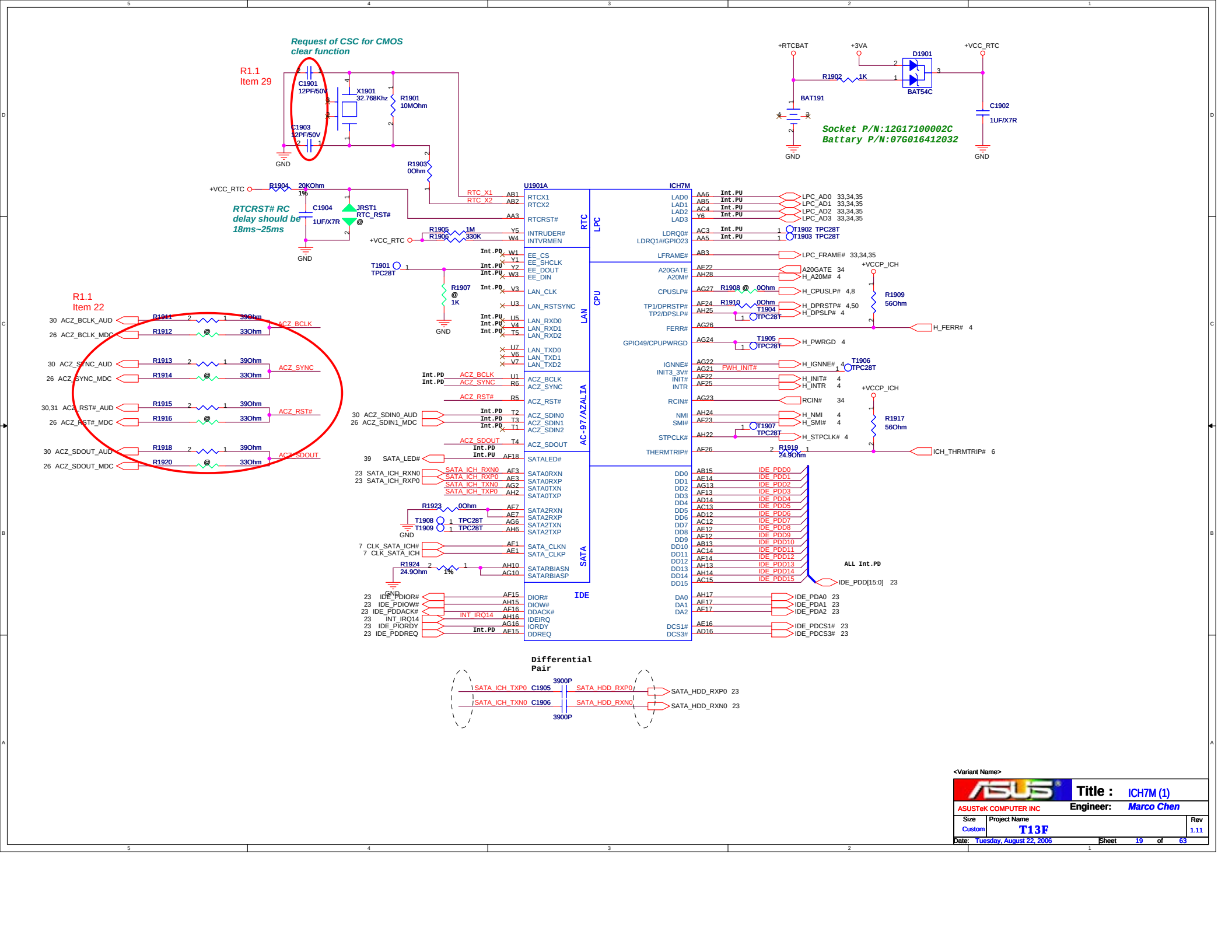
ASUSTeK COMPUTER INC

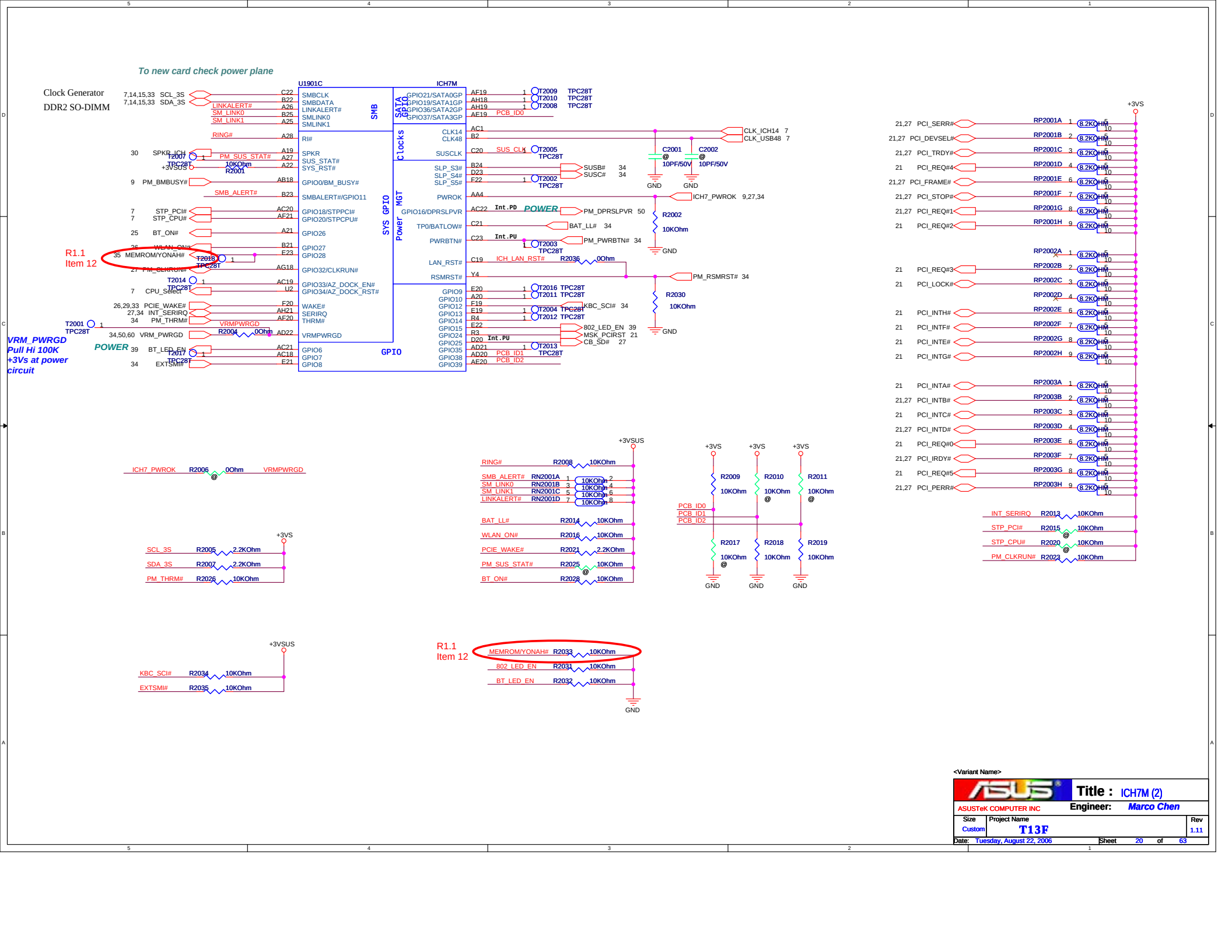
Title : CRT CONN

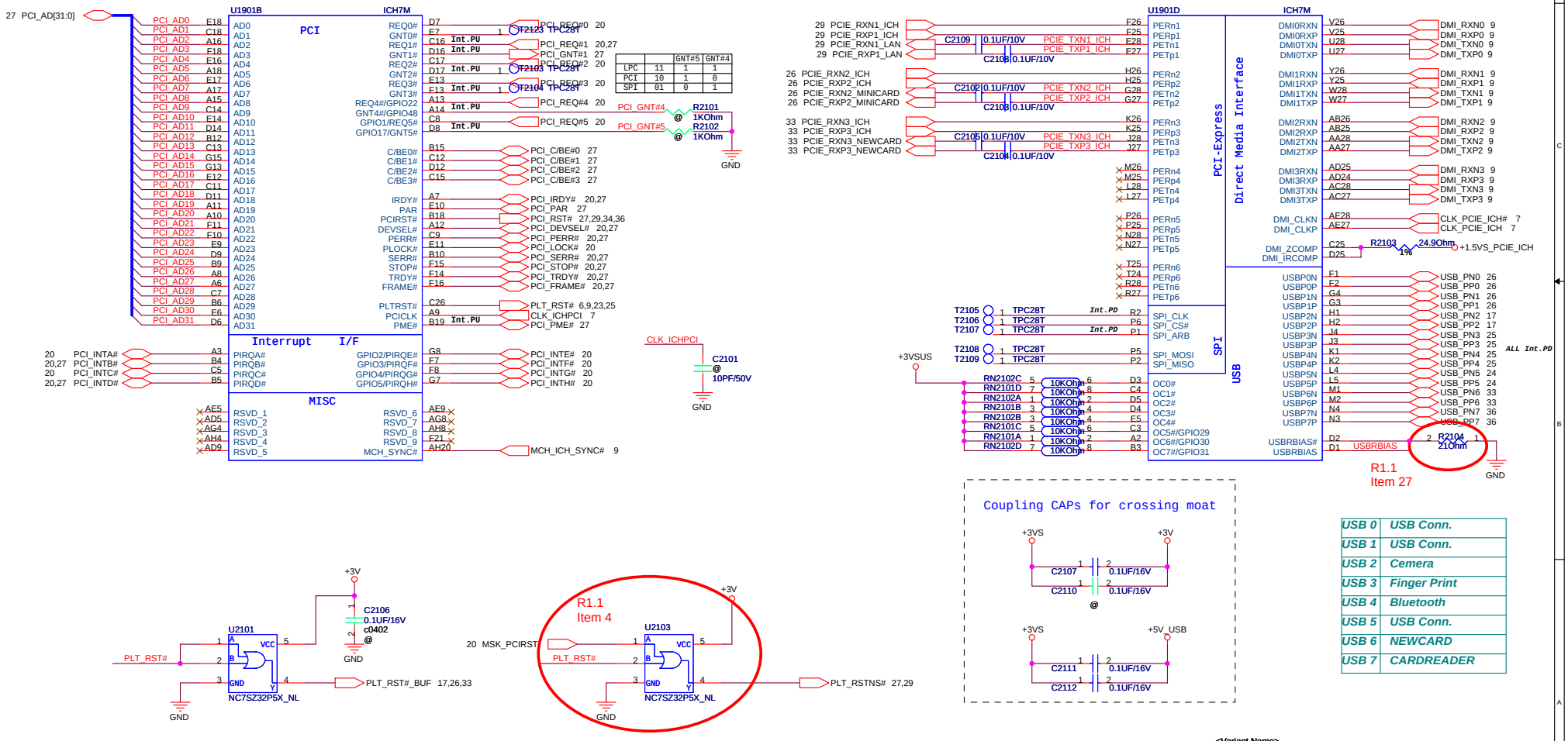
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 18 of 63

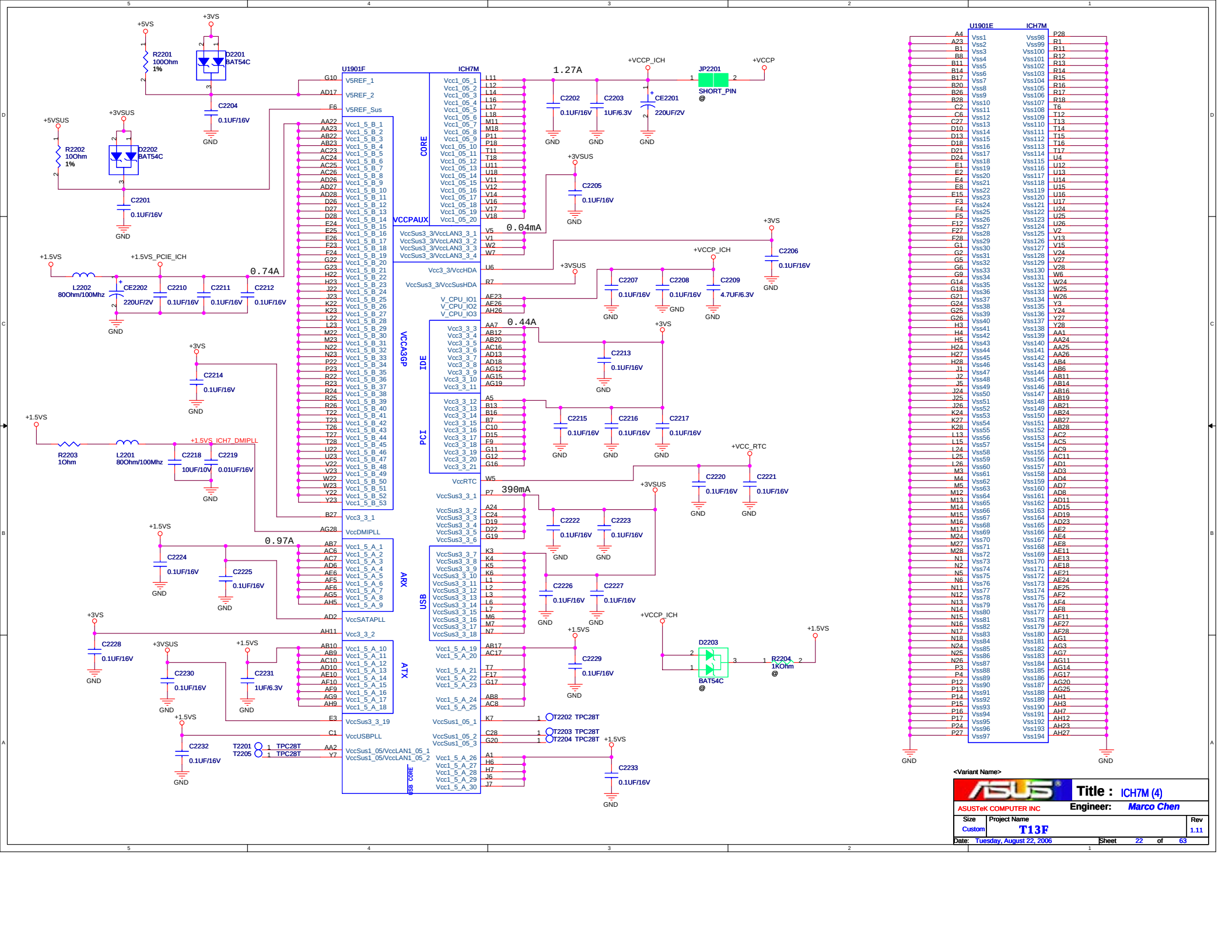

Request of CSC for CMOS clear function
R1.1 Item 29
C1901 12PF/50V
X1901 32.768Khz
R1901 10MOhm
C1903 12PF/50V
GND
R1903 0Ohm
+VCC_RTC
R1904 20KOhm 1%
C1904 1UF/X7R
JRST1
RTC_RST#
RTCRST# RC delay should be 18ms~25ms
R1905 1M
R1906 330K
T1901 TPC28T
R1907 @ 1K
+RTCBAT
+3VA
+VCC_RTC
D1901
BAT54C
R1902 1K
BAT191
C1902 1UF/X7R
Socket P/N:12G17100002C
Battary P/N:07G016412032
U1901A
RTC_X1
RTC_X2
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH7M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
LPC_AD0 33,34,35
LPC_AD1 33,34,35
LPC_AD2 33,34,35
LPC_AD3 33,34,35
LPC_FRAME# 33,34,35
A20GATE 34
H_A20M# 4
H_CPUSLP# 4,8
H_DPRSTP# 4,50
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4
H_IGNNE# 4
H_INIT# 4
H_INTR 4
RCIN# 34
H_NMI 4
H_SMI# 4
H_STPCLK# 4
ICH_THRMTRIP# 6
R1909 56Ohm
R1917 56Ohm
R1919 24.9Ohm
IDE_PDD[15:0] 23
IDE_PDA0 23
IDE_PDA1 23
IDE_PDA2 23
IDE_PDCS1# 23
IDE_PDCS3# 23
R1.1 Item 22
ACZ_BCLK_AUD
ACZ_BCLK_MDC
ACZ_SYNC_AUD
ACZ_SYNC_MDC
ACZ_RST#_AUD
ACZ_RST#_MDC
ACZ_SDOUT_AUD
ACZ_SDOUT_MDC
SATA_LED#
SATA_ICH_RXN0
SATA_ICH_RXP0
SATA_ICH_TXN0
SATA_ICH_TXP0
CLK_SATA_ICH#
CLK_SATA_ICH
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PIORDY
IDE_PDDREQ
Differential Pair
SATA_ICH_TXP0 C1905 3900P SATA_HDD_RXP0 SATA_HDD_RXP0 23
SATA_ICH_TXN0 C1906 3900P SATA_HDD_RXN0 SATA_HDD_RXN0 23
<Variant Name>
Title : ICH7M (1)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 19 of 63


To new card check power plane
Clock Generator
DDR2 SO-DIMM
U1901C
ICH7M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMBALERT#/GPIO11
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
R1.1
Item 12
VRM_PWRGD
Pull Hi 100K
+3Vs at power
circuit
POWER
+3VSUS
+3VS
GND
RP2001A
RP2001B
RP2001C
RP2001D
RP2001E
RP2001F
RP2001G
RP2001H
RP2002A
RP2002B
RP2002C
RP2002D
RP2002E
RP2002F
RP2002G
RP2002H
RP2003A
RP2003B
RP2003C
RP2003D
RP2003E
RP2003F
RP2003G
RP2003H
8.2KOHM
10KOhm
2.2KOhm
0Ohm
Title : ICH7M (2)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size: Custom
Project Name: T13F
Rev: 1.11
Date: Tuesday, August 22, 2006
Sheet 20 of 63



		GNT#5	GNT#4
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Cemera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER



<Variant Name>

ASUSTeK COMPUTER INC

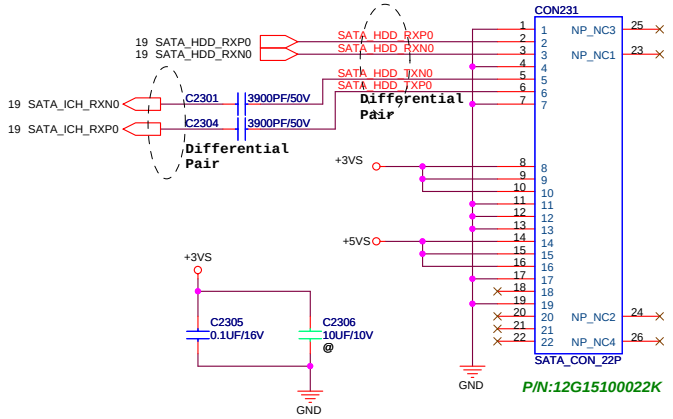
Title : ICH7M (4)

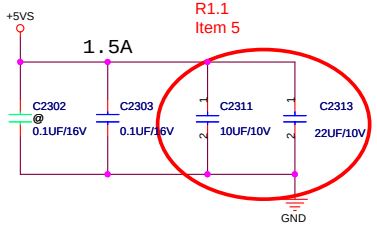
Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

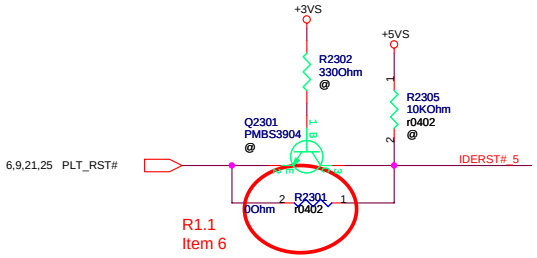
Date: Tuesday, August 22, 2006 Sheet 22 of 63

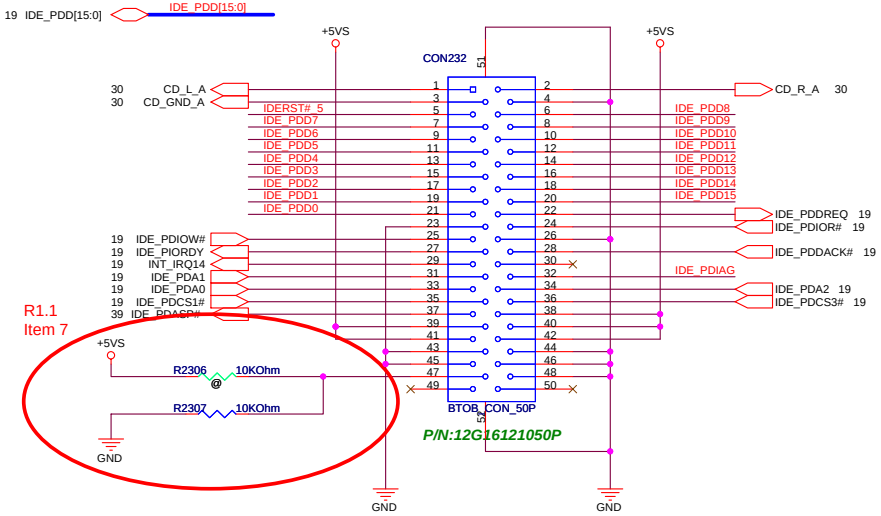
SATA HDD CON

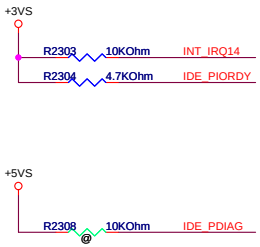




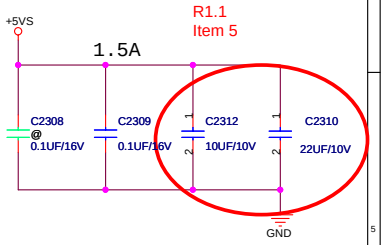
PATA ODD CON





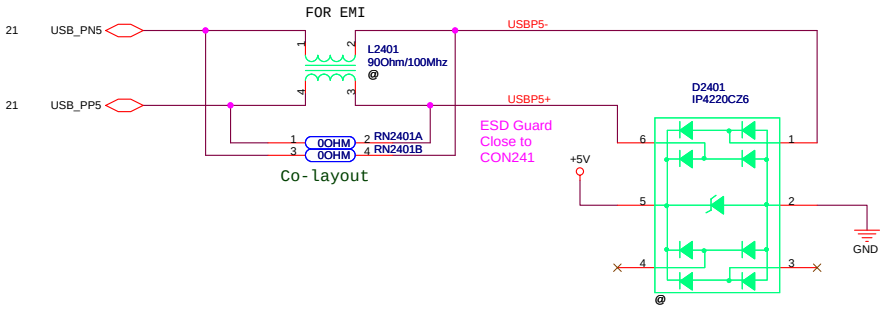


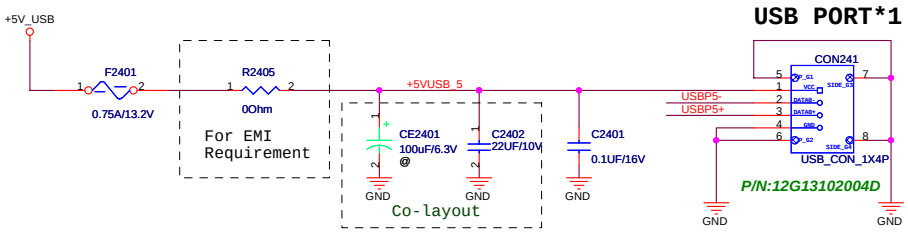
Normal type
High: Slave
Low : Master

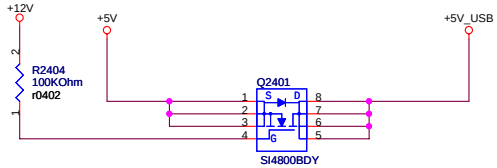


<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & ODD	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 23 of 63	

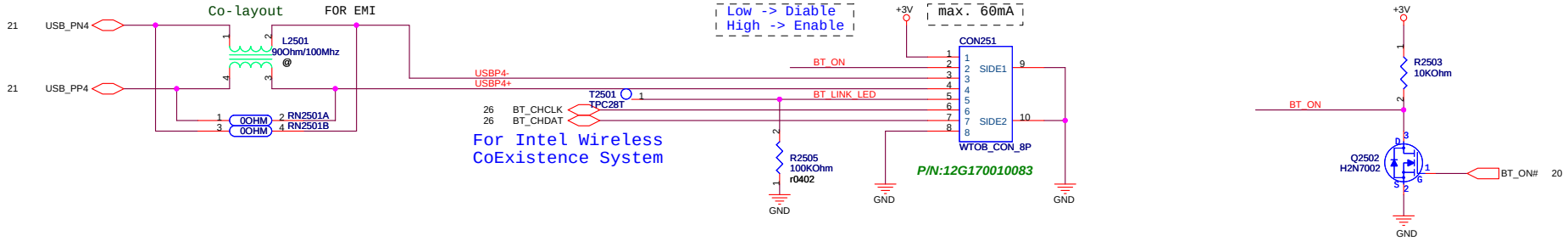




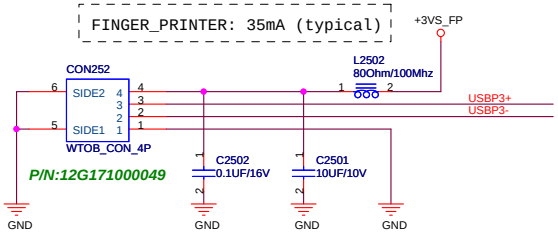


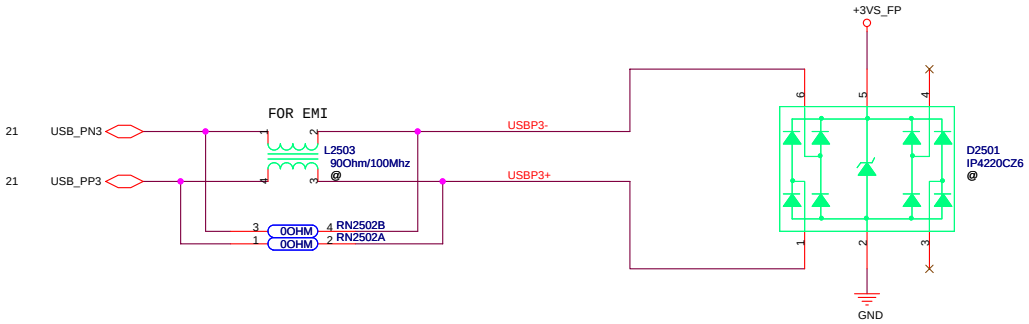
<Variant Name>

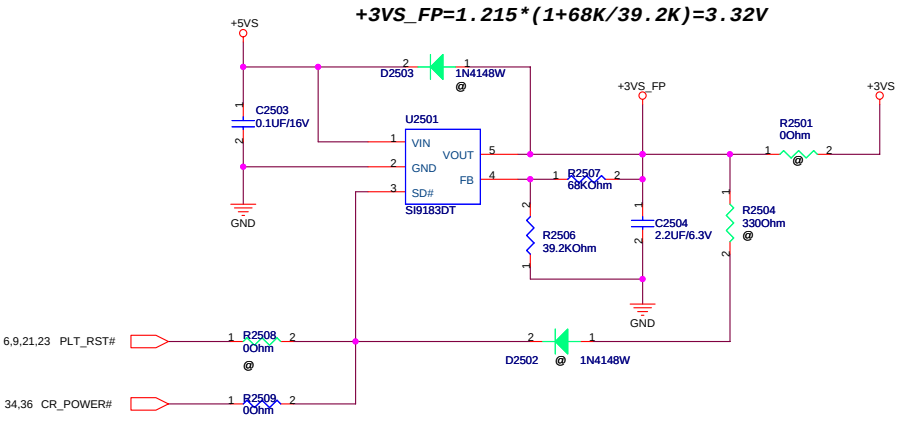
ASUSTeK COMPUTER INC	Title : USB PORT	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 24 of 63	



Finger Printer







<Variant Name>

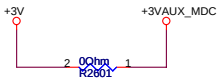
ASUSTeK COMPUTER INC	Title : BT & FP	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 25 of 63	

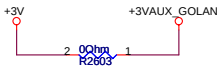
POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

+1.5VS:+1.425V~+1.575V
Max= 375 mA

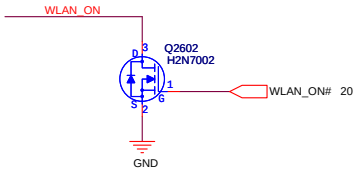
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC:+3.003V~+3.597V
Max= 300 mA





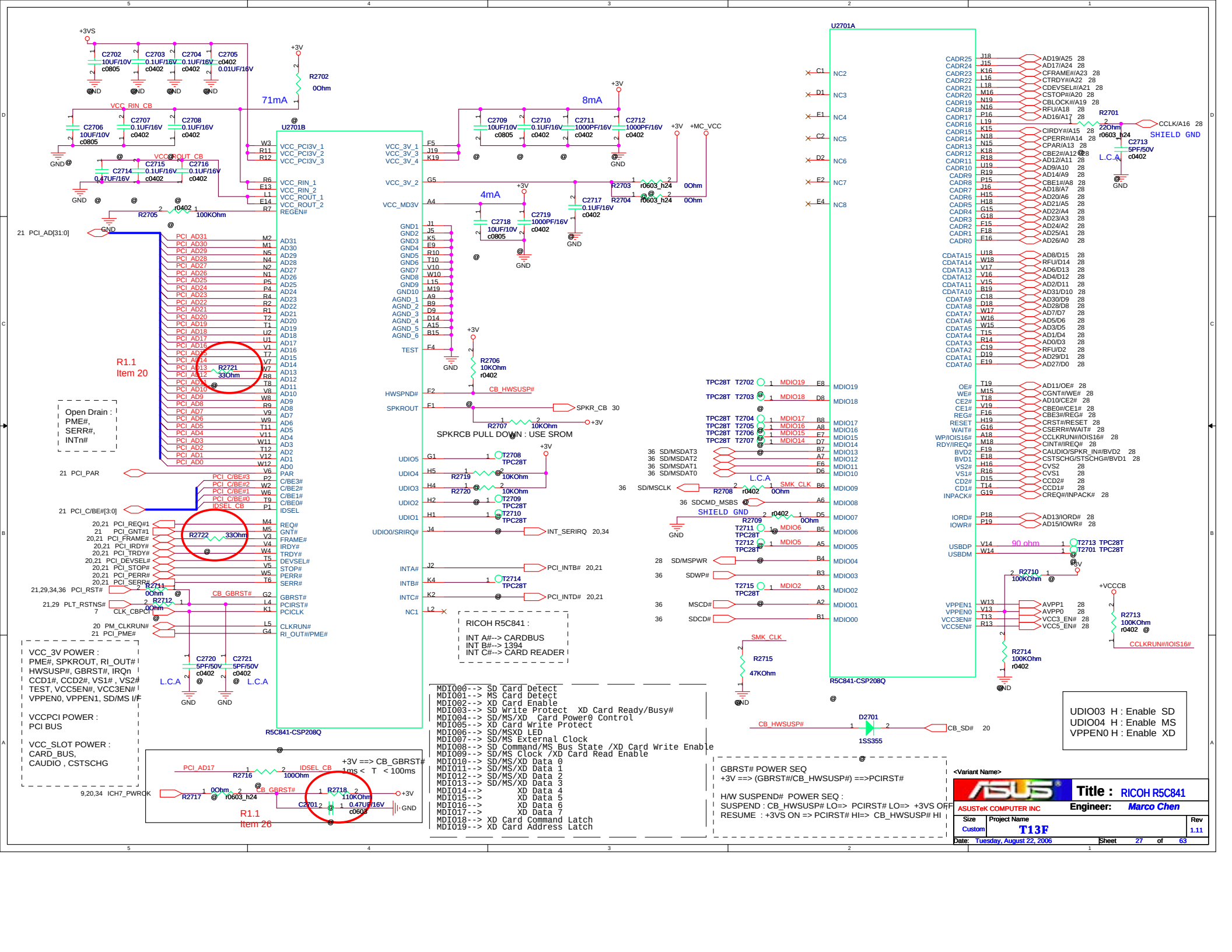
Intel SPEC(18780):Internal
Pull UP 110Kohm

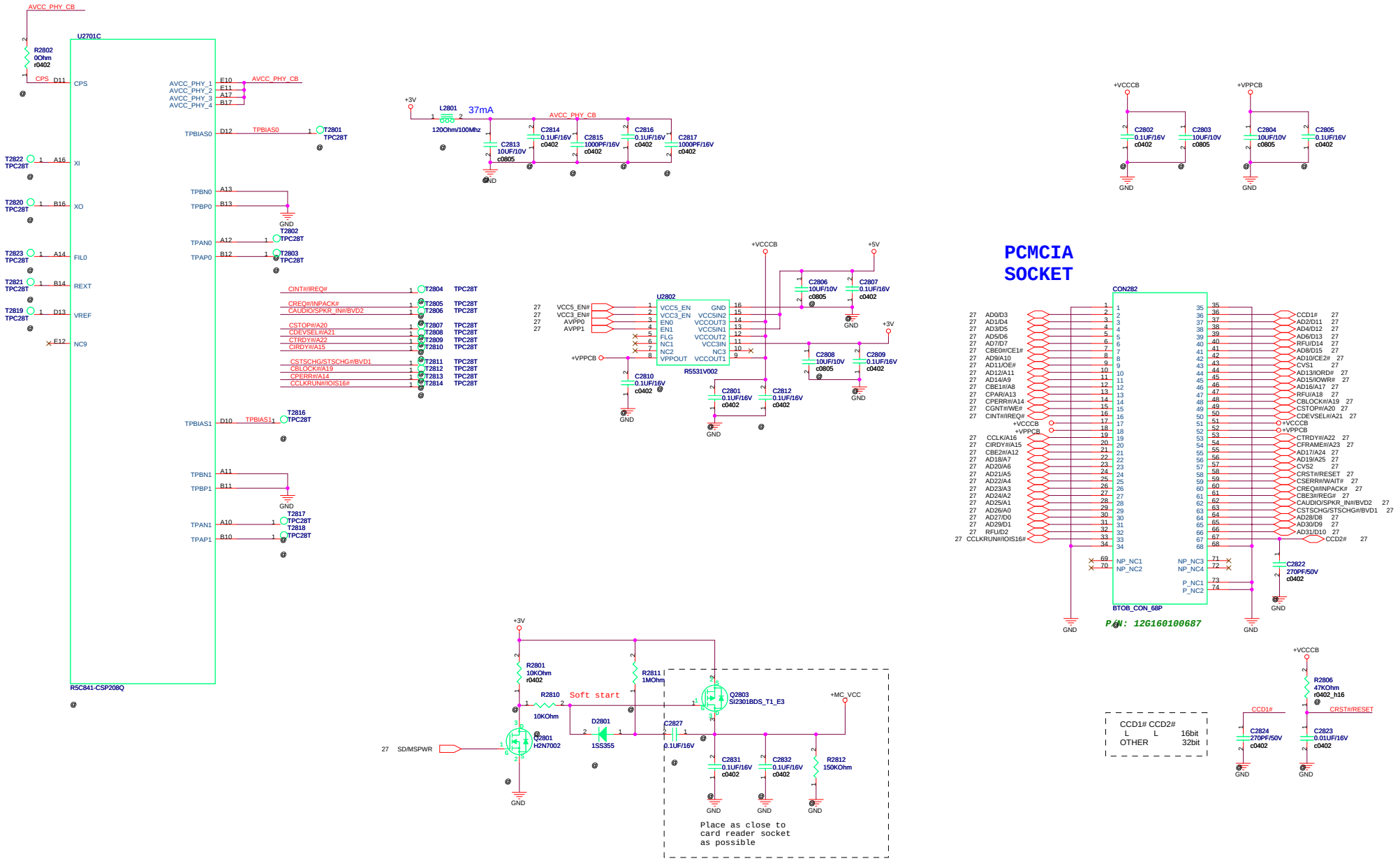


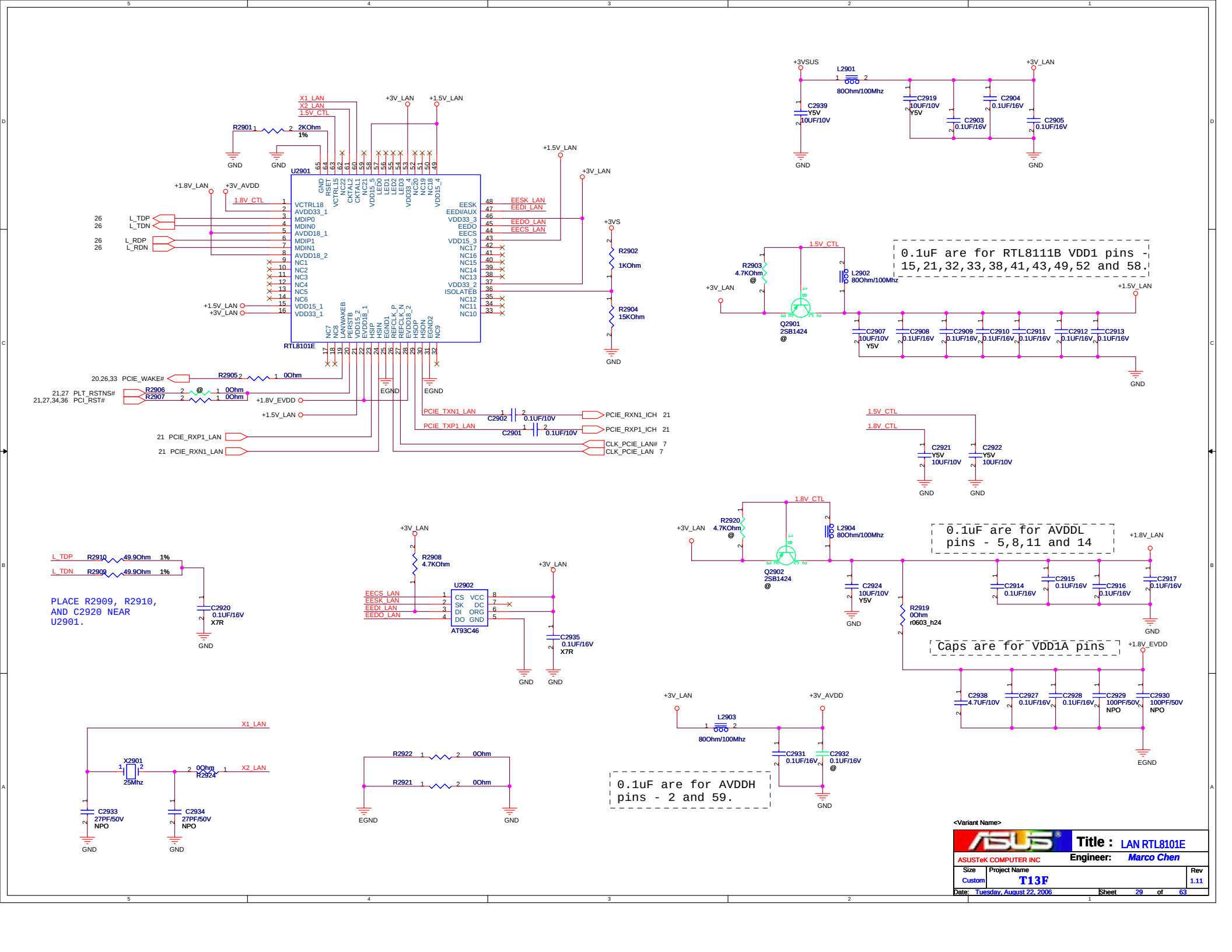
P/N:12G061200504

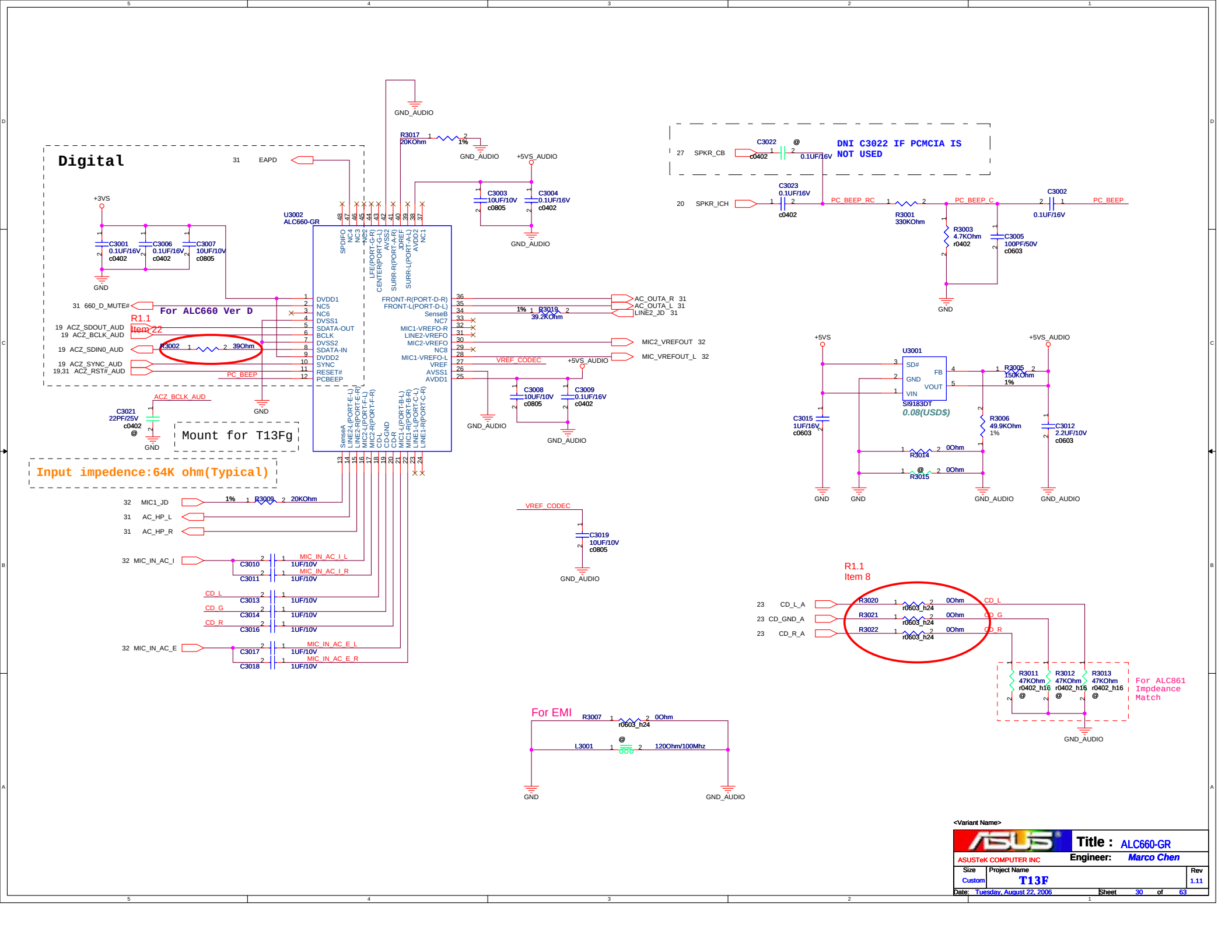
<Variant Name>

ASUSTeK COMPUTER INC	Title : B TO B CONN(M)	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 26 of 63	


U2701B
R5C841-CSP208Q
U2701A
R5C841-CSP208Q
71mA
8mA
4mA
R1.1
Item 20
R1.1
Item 26
Open Drain :
PME#,
SERR#,
INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
+3V ==> CB_GBRST#
1ms < T < 100ms
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Marco Chen
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 27 of 63


PCMCIA SOCKET
U2701C
R5C841-CSP208Q
U2802
R5531V002
CON282
BTOB_CON_68P
P/N: 12G160100687
Soft start
Place as close to card reader socket as possible
CCD1# CCD2#
L L 16bit
OTHER 32bit
<Variant Name>
Title : PCMCIA&3IN1 SOCKET
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size C
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 28 of 63


U2901
RTL8101E
X1_LAN
X2_LAN
1.5V_CTL
R2901 2KOhm 1%
+3V_LAN
+1.5V_LAN
+1.8V_LAN
+3V_AVDD
1.8V_CTL
L_TDP
L_TDN
L_RDP
L_RDN
EESK_LAN
EEDI_LAN
EEDO_LAN
EECS_LAN
+3VS
R2902 1KOhm
R2904 15KOhm
GND
EGND
20,26,33 PCIE_WAKE#
R2905 0Ohm
21,27 PLT_RSTNS#
21,27,34,36 PCI_RST#
R2906 0Ohm
R2907 0Ohm
+1.8V_EVDD
PCIE_TXN1_LAN
PCIE_TXP1_LAN
C2902 0.1UF/10V
C2901 0.1UF/10V
PCIE_RXN1_ICH 21
PCIE_RXP1_ICH 21
21 PCIE_RXP1_LAN
21 PCIE_RXN1_LAN
CLK_PCIE_LAN# 7
CLK_PCIE_LAN 7
+3VSUS
L2901 80Ohm/100Mhz
C2939 Y5V 10UF/10V
C2919 10UF/10V Y5V
C2903 0.1UF/16V
C2904 0.1UF/16V
C2905 0.1UF/16V
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
R2903 4.7KOhm @
L2902 80Ohm/100Mhz
Q2901 2SB1424 @
C2907 10UF/10V Y5V
C2908 0.1UF/16V
C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2912 0.1UF/16V
C2913 0.1UF/16V
C2921 Y5V 10UF/10V
C2922 Y5V 10UF/10V
R2920 4.7KOhm @
L2904 80Ohm/100Mhz
Q2902 2SB1424 @
C2924 10UF/10V Y5V
0.1uF are for AVDDL pins - 5,8,11 and 14
C2914 0.1UF/16V
C2915 0.1UF/16V
C2916 0.1UF/16V
C2917 0.1UF/16V
R2919 0Ohm r0603_h24
Caps are for VDD1A pins
C2938 4.7UF/10V
C2927 0.1UF/16V
C2928 0.1UF/16V
C2929 100PF/50V NPO
C2930 100PF/50V NPO
L_TDP R2910 49.9Ohm 1%
L_TDN R2909 49.9Ohm 1%
PLACE R2909, R2910, AND C2920 NEAR U2901.
C2920 0.1UF/16V X7R
R2908 4.7KOhm
U2902
AT93C46
EECS_LAN
EESK_LAN
EEDI_LAN
EEDO_LAN
C2935 0.1UF/16V X7R
X2901 25Mhz
0Ohm R2924
C2933 27PF/50V NPO
C2934 27PF/50V NPO
R2922 0Ohm
R2921 0Ohm
L2903 80Ohm/100Mhz
C2931 0.1UF/16V
C2932 0.1UF/16V @
0.1uF are for AVDDH pins - 2 and 59.
<Variant Name>
Title : LAN RTL8101E
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 29 of 63



<Variant Name>

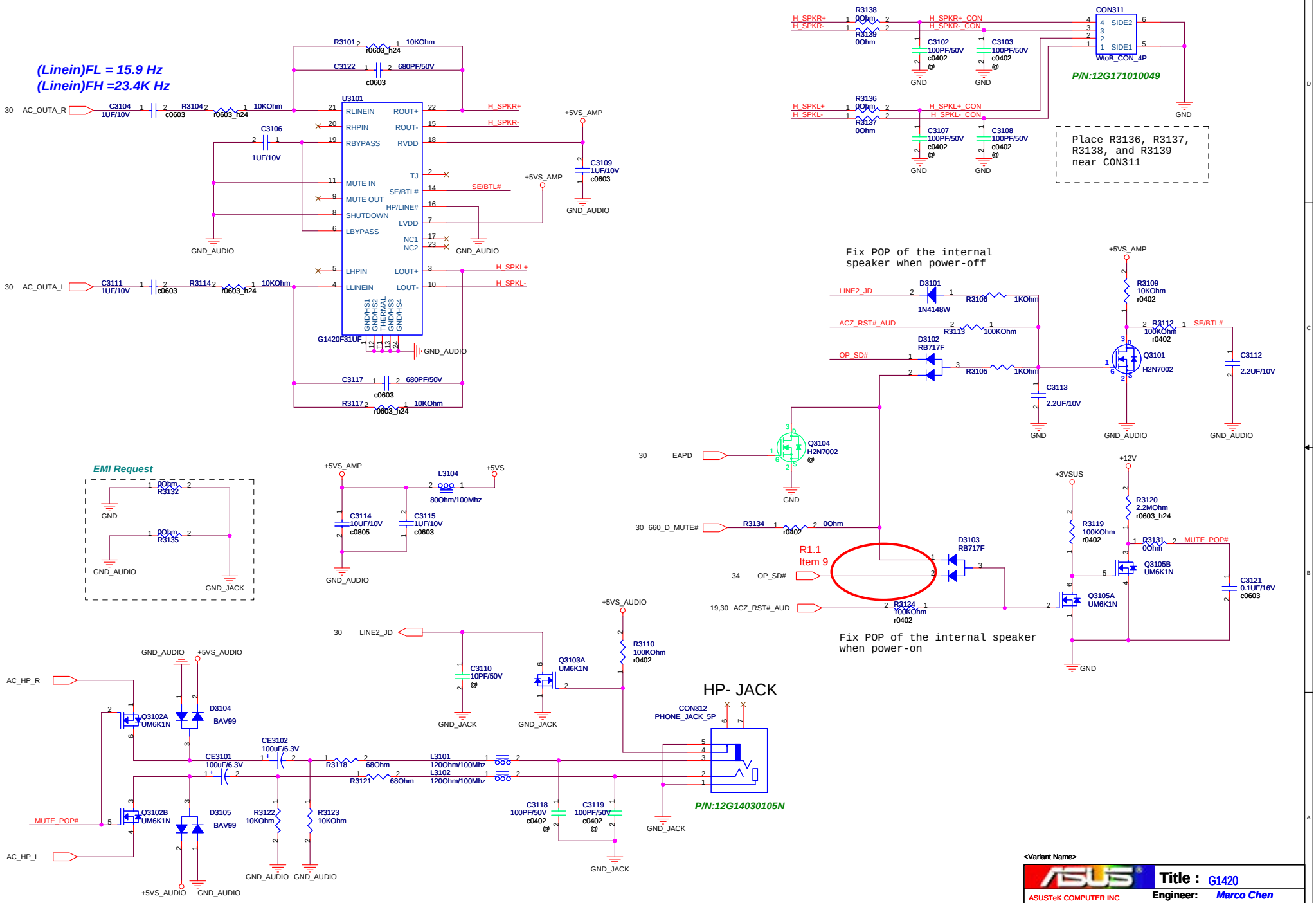
ASUSTeK COMPUTER INC

Title : ALC660-GR

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 30 of 63



<Variant Name>

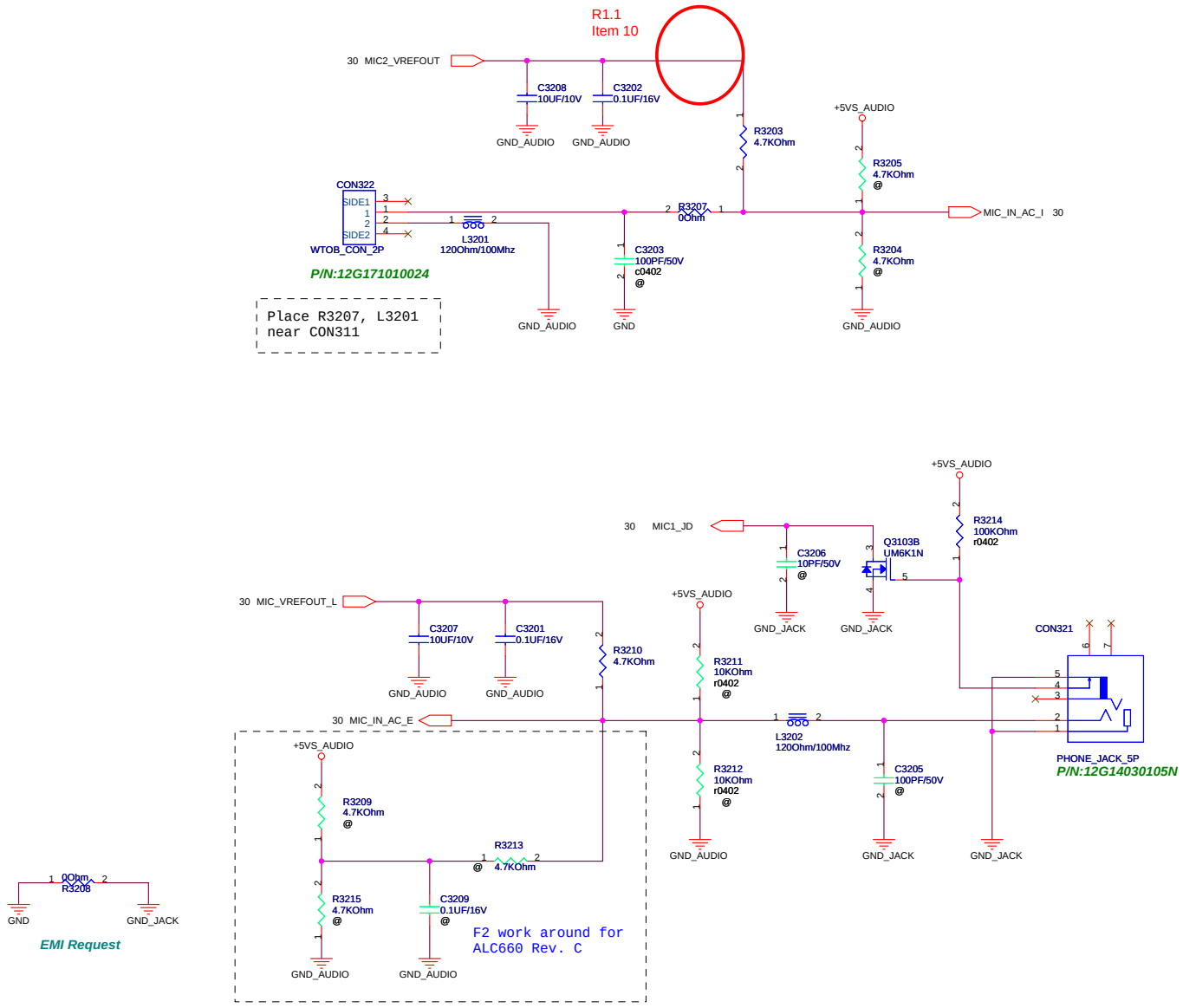
ASUSTeK COMPUTER INC

Title : G1420

Engineer: Marco Chen

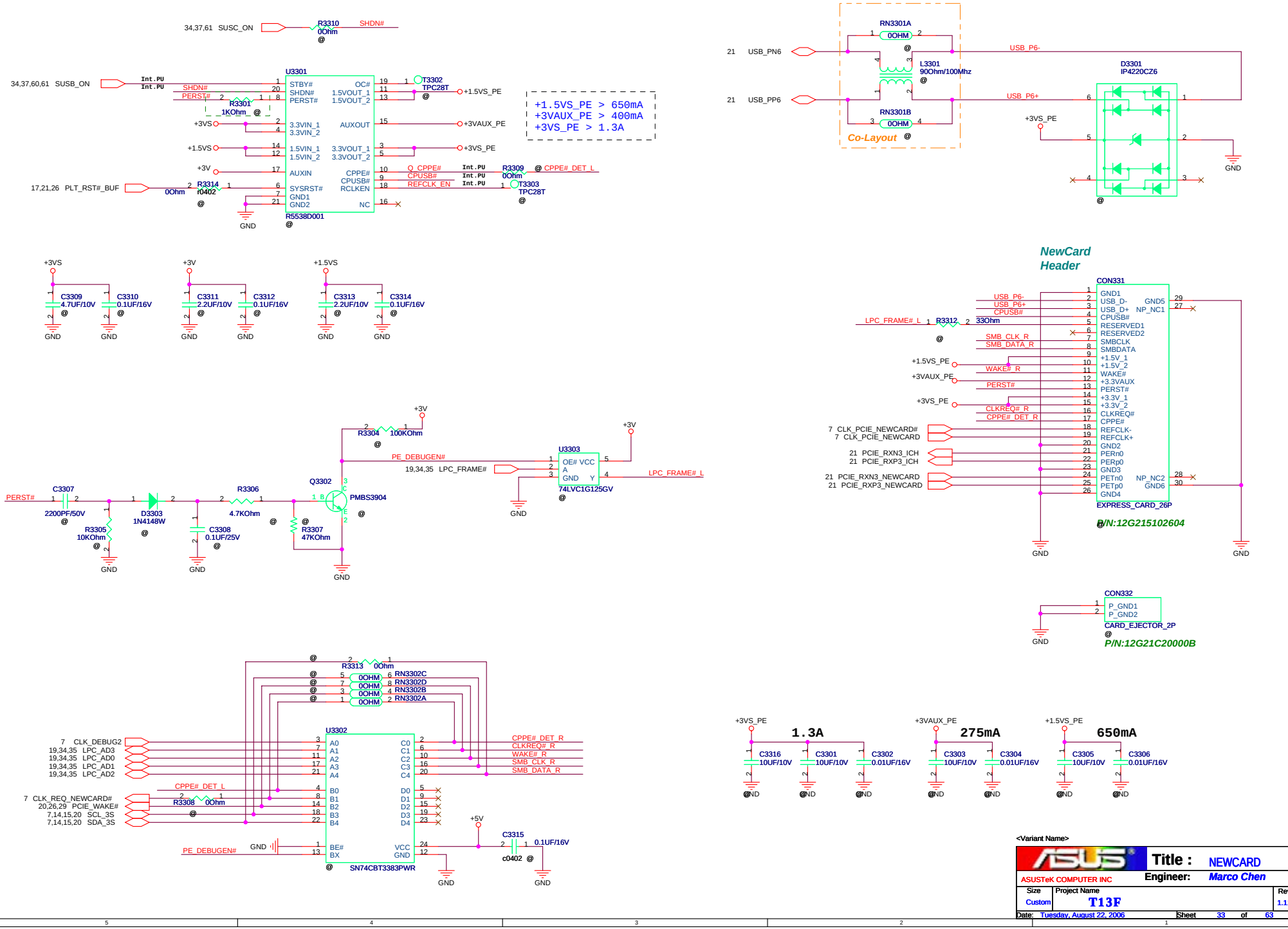
Size	Project Name	Rev
Custom	T13F	1.11

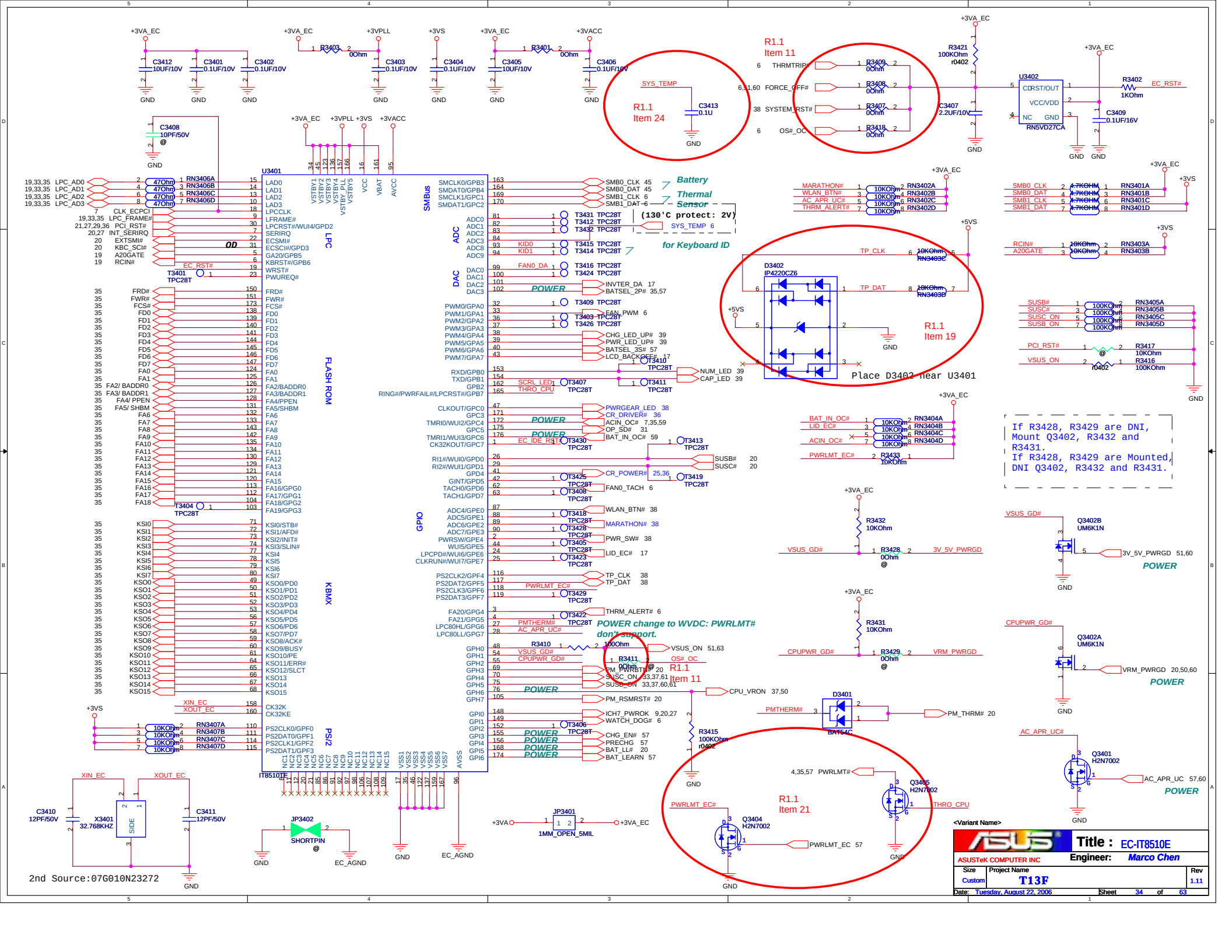
Date: Tuesday, August 22, 2006 Sheet 31 of 63



<Variant Name>

ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 32 of 63	


34,37,61 SUSC_ON
R3310 0Ohm SHDN#
U3301
34,37,60,61 SUSB_ON
SHDN#
PERST#
R3301 1KOhm
+3VS
+1.5VS
+3V
17,21,26 PLT_RST#_BUF
R3314 0Ohm r0402
STBY# SHDN# PERST# SYSRST# GND1 GND2
OC# 1.5VOUT_1 1.5VOUT_2 AUXOUT CPPE# CPUSB# RCLKEN NC
3.3VIN_1 3.3VIN_2 1.5VIN_1 1.5VIN_2 AUXIN
R5538D001
T3302 TPC28T
+1.5VS_PE
+3VAUX_PE
+3VS_PE
O_CPPE#
CPUSB#
REFCLK_EN
R3309 0Ohm @ CPPE# DET L
T3303 TPC28T
+1.5VS_PE > 650mA
+3VAUX_PE > 400mA
+3VS_PE > 1.3A
21 USB_PN6
21 USB_PP6
RN3301A 0OHM
RN3301B 0OHM
L3301 90Ohm/100Mhz
Co-Layout
USB_P6-
USB_P6+
D3301 IP4220CZ6
C3309 4.7UF/10V
C3310 0.1UF/16V
C3311 2.2UF/10V
C3312 0.1UF/16V
C3313 2.2UF/10V
C3314 0.1UF/16V
R3304 100KOhm
PE_DEBUGEN#
19,34,35 LPC_FRAME#
U3303 74LVC1G125GV
LPC_FRAME# L
PERST#
C3307 2200PF/50V
R3305 10KOhm
D3303 1N4148W
R3306 4.7KOhm
C3308 0.1UF/25V
Q3302 PMBS3904
R3307 47KOhm
NewCard Header
CON331 EXPRESS_CARD_26P
LPC_FRAME# L
R3312 33Ohm
SMB_CLK_R
SMB_DATA_R
WAKE# R
CLKREQ# R
CPPE# DET R
7 CLK_PCIE_NEWCARD#
7 CLK_PCIE_NEWCARD
21 PCIE_RXN3_ICH
21 PCIE_RXP3_ICH
21 PCIE_RXN3_NEWCARD
21 PCIE_RXP3_NEWCARD
P/N:12G215102604
CON332 CARD_EJECTOR_2P
P/N:12G21C20000B
R3313 0Ohm
RN3302C RN3302D RN3302B RN3302A
U3302 SN74CBT3383PWR
7 CLK_DEBUG2
19,34,35 LPC_AD3
19,34,35 LPC_AD0
19,34,35 LPC_AD1
19,34,35 LPC_AD2
7 CLK_REQ_NEWCARD#
20,26,29 PCIE_WAKE#
7,14,15,20 SCL_3S
7,14,15,20 SDA_3S
R3308 0Ohm
CPPE# DET L
CPPE# DET R
CLKREQ# R
WAKE# R
SMB_CLK_R
SMB_DATA_R
PE_DEBUGEN#
C3315 0.1UF/16V
+3VS_PE 1.3A
C3316 10UF/10V
C3301 10UF/10V
C3302 0.01UF/16V
+3VAUX_PE 275mA
C3303 10UF/10V
C3304 0.01UF/16V
+1.5VS_PE 650mA
C3305 10UF/10V
C3306 0.01UF/16V
<Variant Name>
Title : NEWCARD
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
Sheet 33 of 63


U3401
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
(130'C protect: 2V)
for Keyboard ID
POWER
R1.1 Item 11
R1.1 Item 24
R1.1 Item 19
R1.1 Item 21
Place D3402 near U3401
If R3428, R3429 are DNI, Mount Q3402, R3432 and R3431.
If R3428, R3429 are Mounted, DNI Q3402, R3432 and R3431.
POWER change to WVDC: PWRLMT# don't support.
2nd Source:07G010N23272
Title : EC-IT8510E
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13F
Date: Tuesday, August 22, 2006
Sheet 34 of 63

EC Hardware Strapping

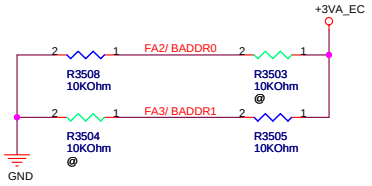
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

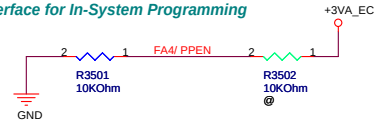


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

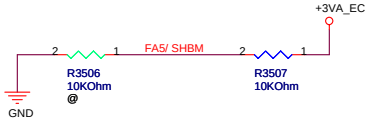
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



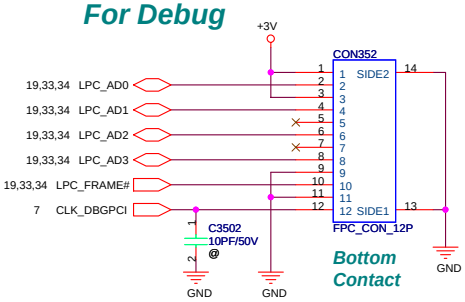
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

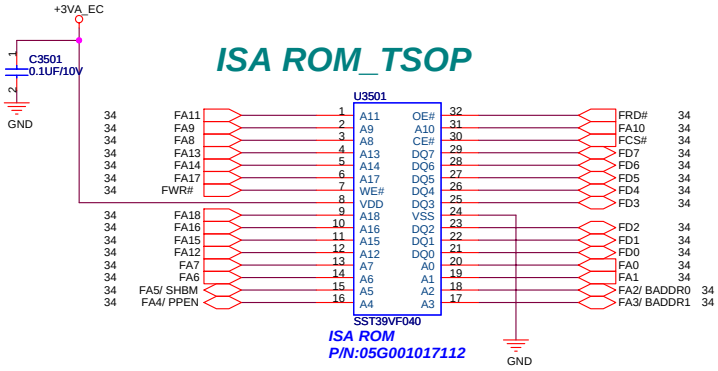


For Debug



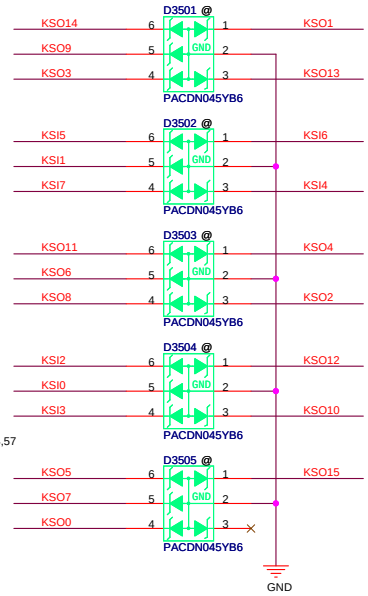
P/N:12G183301208

ISA ROM_TSOP



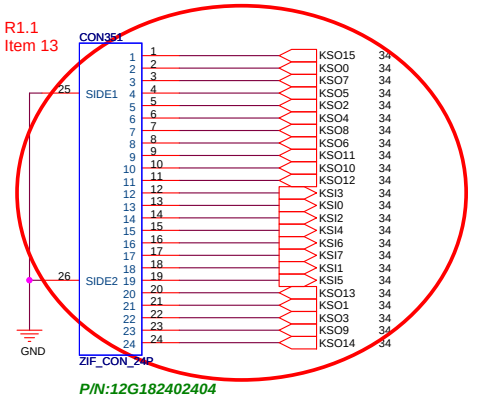
ISA ROM

P/N:05G001017112



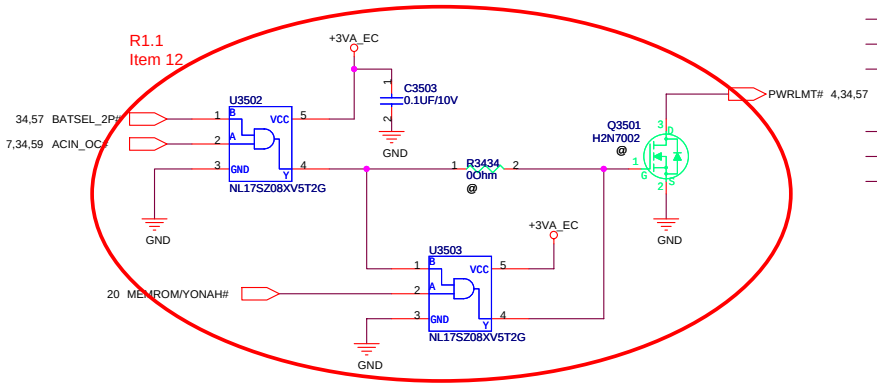
For Keyboard

R1.1
Item 13



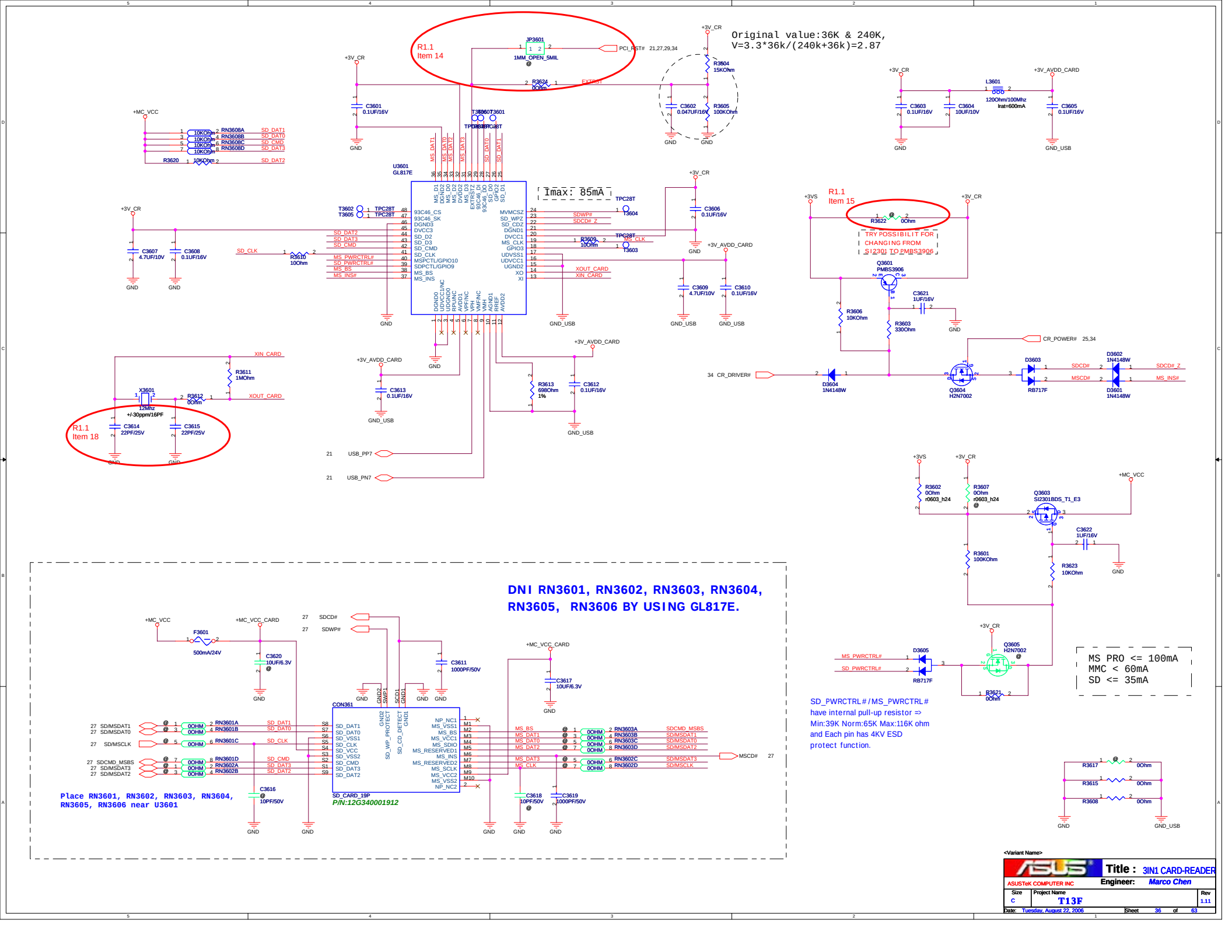
P/N:12G182402404

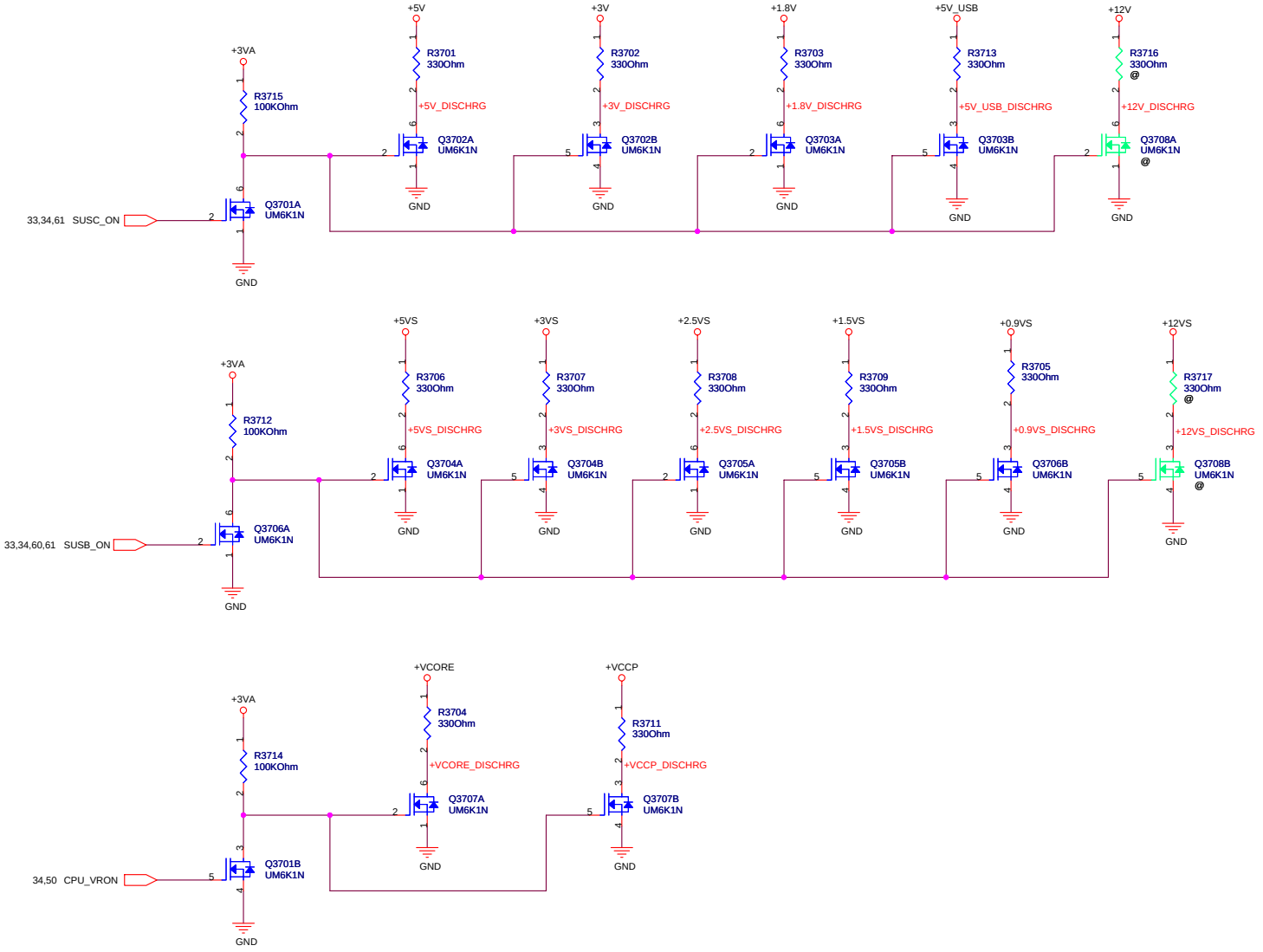
R1.1
Item 12



<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA_ROM&KB conn	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 35 of 63	


R1.1
Item 14
Original value:36K & 240K,
V=3.3*36k/(240k+36k)=2.87
Imax: 85mA
R1.1
Item 15
TRY POSSIBILITY FOR
CHANGING FROM
SI2301 TO PMBS3906
R1.1
Item 18
MS PRO <= 100mA
MMC < 60mA
SD <= 35mA
DNI RN3601, RN3602, RN3603, RN3604,
RN3605, RN3606 BY USING GL817E.
Place RN3601, RN3602, RN3603, RN3604,
RN3605, RN3606 near U3601
SD_PWRCTRL#/MS_PWRCTRL#
have internal pull-up resistor =>
Min:39K Norm:65K Max:116K ohm
and Each pin has 4KV ESD
protect function.
P/N:12G340001912
Title : 3IN1 CARD-READER
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13F
Rev 1.11
Tuesday, August 22, 2006
Sheet 36 of 63



<Variant Name>

Title : DISCHARGE

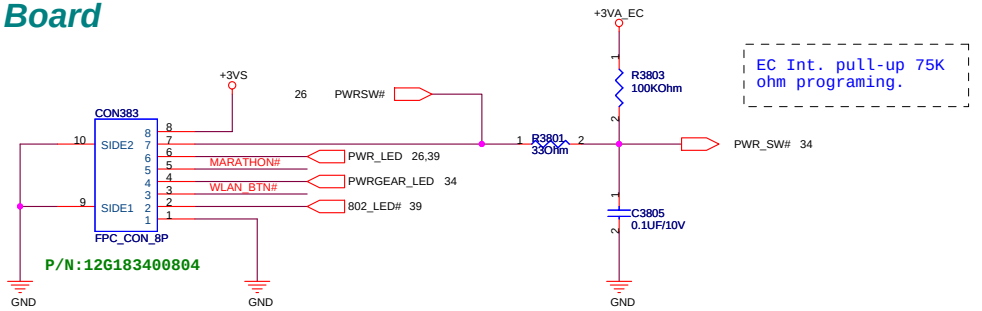
ASUSTeK COMPUTER INC

Engineer: Marco Chen

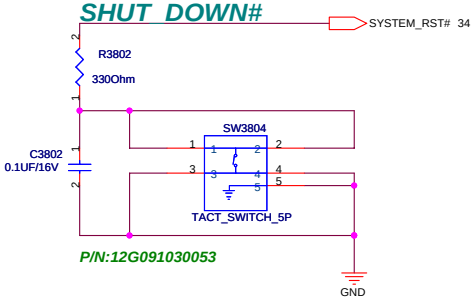
Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 37 of 63

FFC CONNECTER for T13Fv SW Board

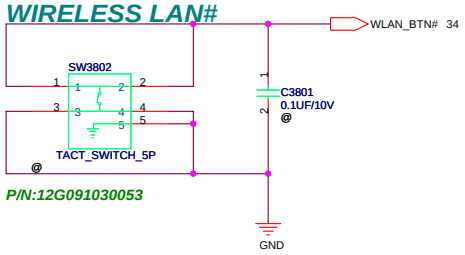


SHUT_DOWN#

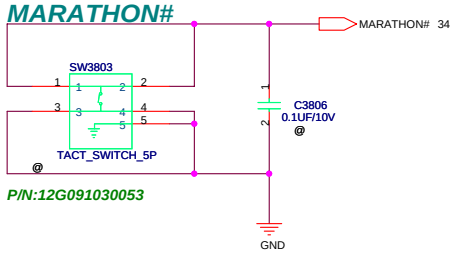


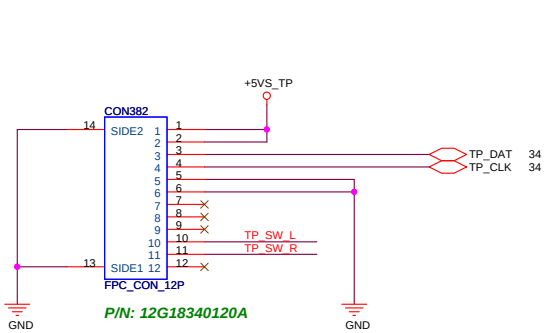
INSTANT KEY for T13Fg

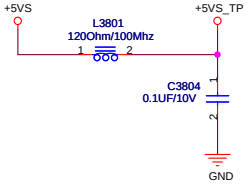
WIRELESS LAN#



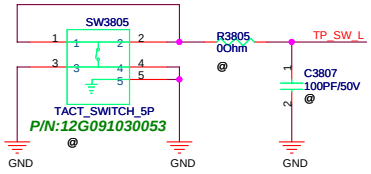
MARATHON#

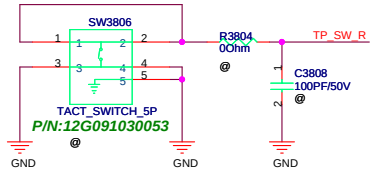






Select Button for T13Fg



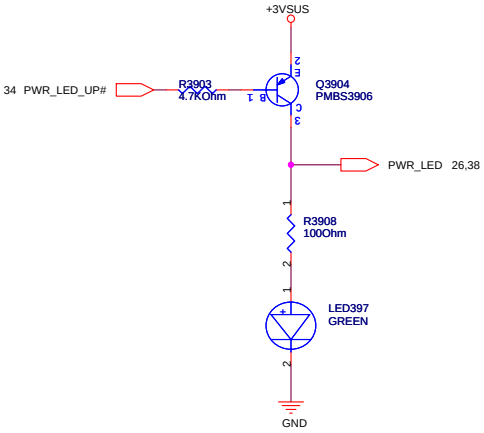


<Variant Name>

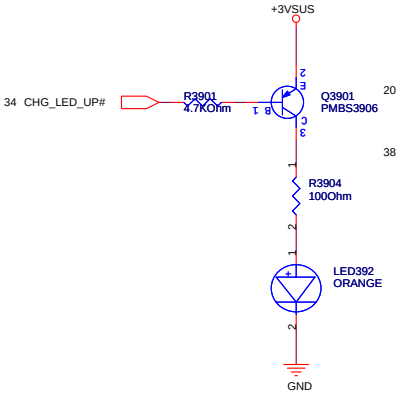
ASUSTeK COMPUTER INC	Title : Key & FFC CONN	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 38 of 63	

PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.

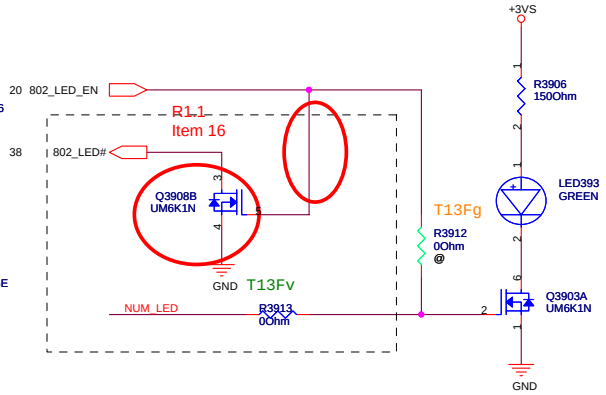
For POWER LED



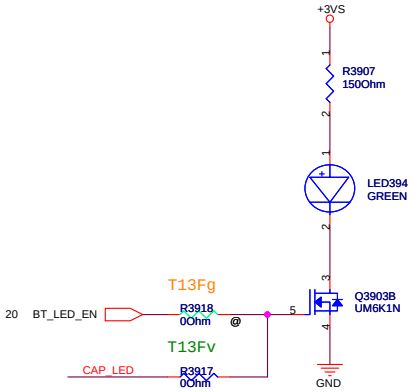
For BATTERY LED



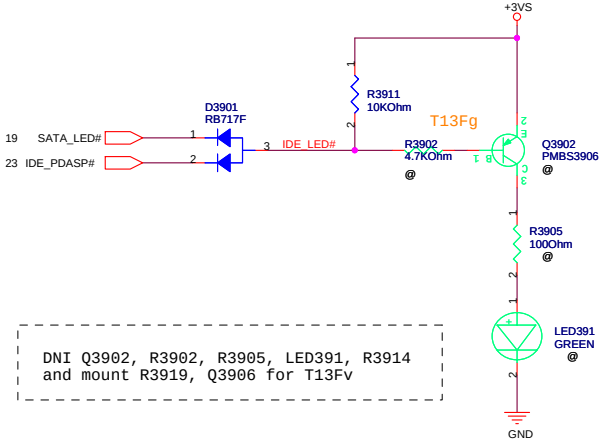
For WireLess LED



For BT LED

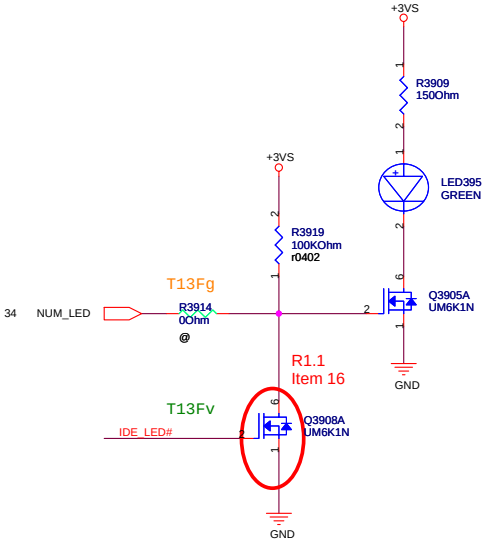


For SATA/IDE LED

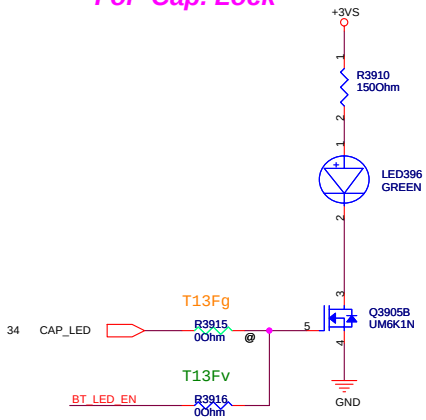


DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3906 for T13Fv

For Num Lock



For Cap. Lock



<Variant Name>

Title : LEDs

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 40 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 41 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 42 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 43 of 63

<Variant Name>

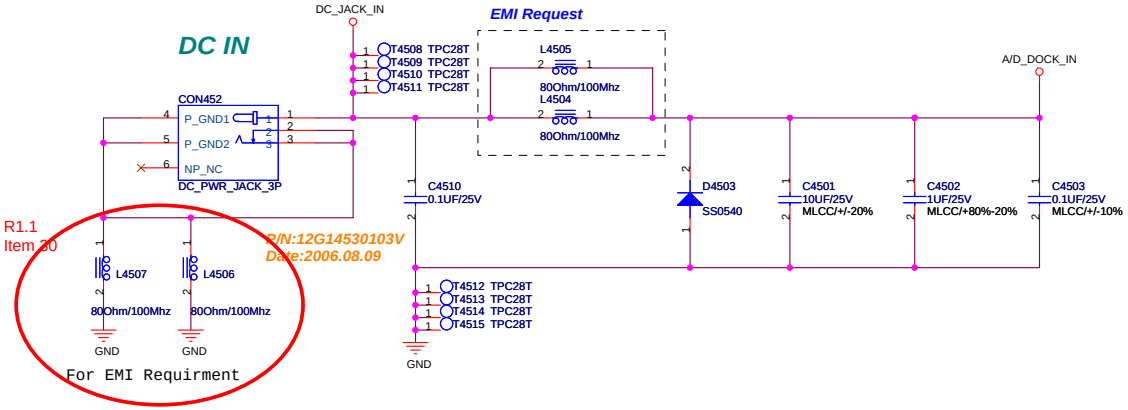
Title : EMPTY

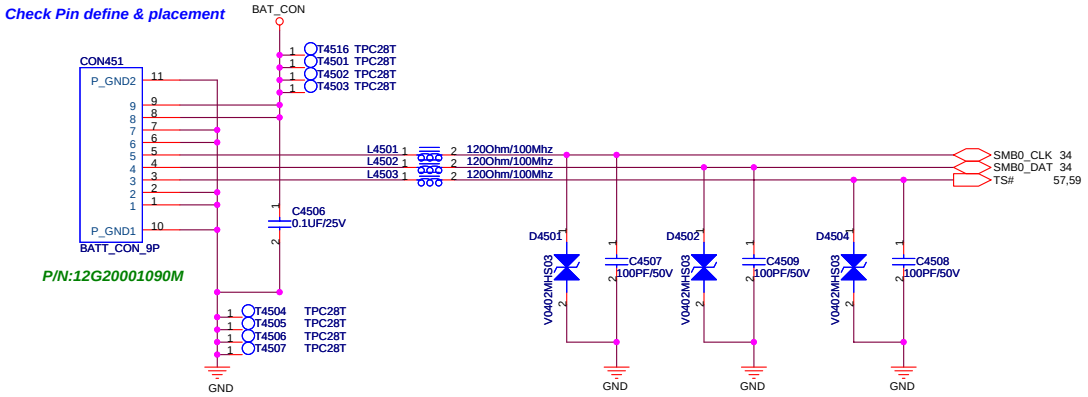
ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

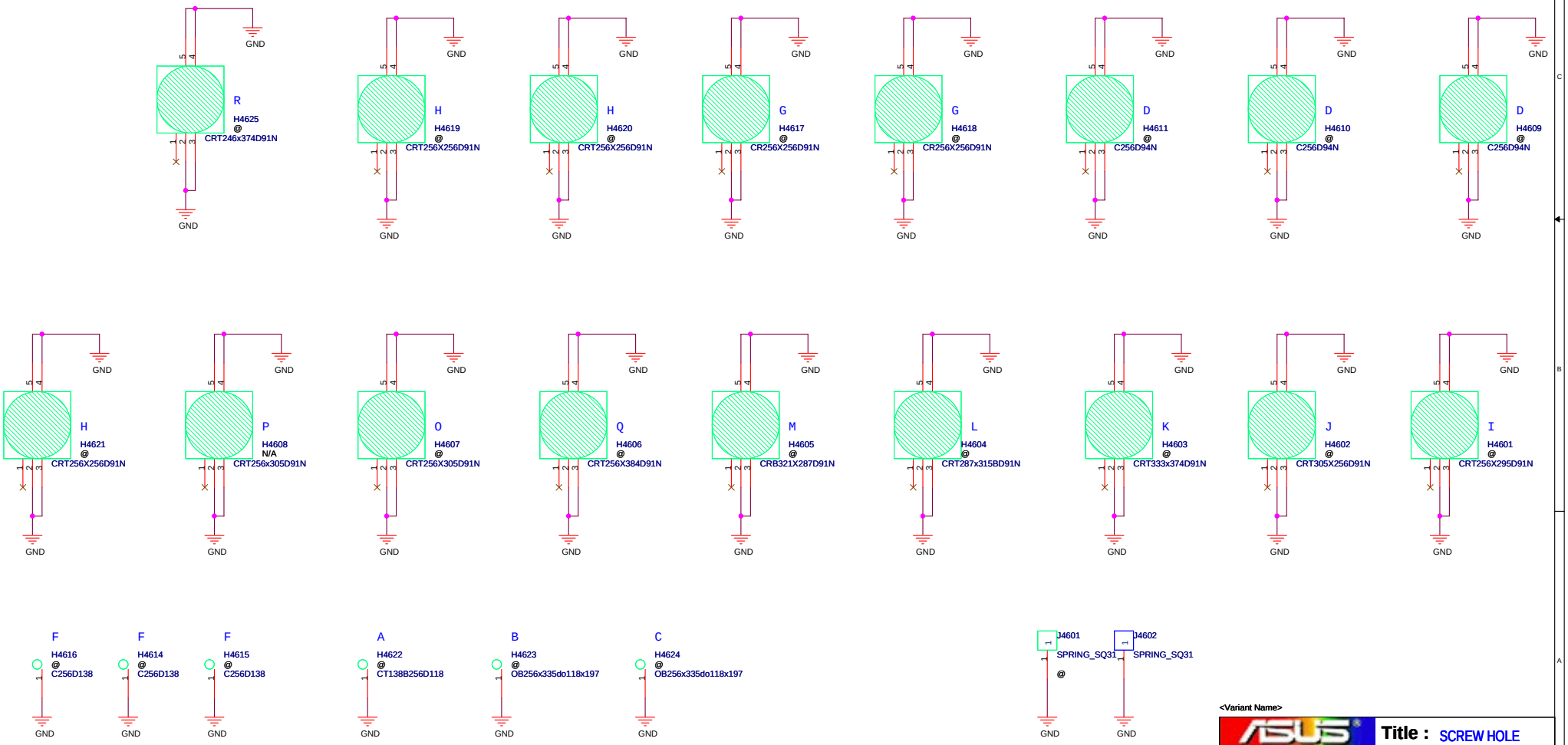
Date: Tuesday, August 22, 2006 Sheet 44 of 63





<Variant Name>

ASUSTeK COMPUTER INC	Title : BAT&Adapter conn	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 45 of 63	



<Variant Name>

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: Marco Chen	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 46 of 63	

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
C	T13F	1.11

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R1.0 -> R1.1

1.)Page 6: DNI R611 because Int. pull-up resister exists in FAN module.

2.)Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

3.)Page 17: Change reference name from F3602 to F1701.

4.)Page 21: DNI U2103.

5.)Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.

6.)Page 23: Change R2301 size from 0603 to 0402.

7.)Page 23: Add pull high resister R2306*DNI and pull down resister R2307*Mount for ODD cable select.

8.)Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.

9.)Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.)Page 32: Delete R3201 and connect MIC2_VREFOUTto R3203.1 directly.

11.)Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.

12.)Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

13.)Page 35: Change keyboard matrix.

14.)Page 36: Change reference name from JP3403 to JP3601

15.)Page 36: Change R3622 size from 0402 to 0603.

16.)Page 39: Delete R3920 and change Q3906 and Q3907*2N7006 to Q3908*UM6K1N.

17.)Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.

18.)Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.

19.)Page 34: Add ESD Protection*D3402 for Touch Pad.

20.)Page 27: Add series resister 33 ohm for PCI_FRAME# and PCI_AD13

21.)Page 34:Change Q3403**UM6K1N to Q3404, Q3405*2N7002.

22.)Page 18: Change L1801, L1802, and L1803 from bead to inductor.

23.)Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

24.)Page 6: Change R615 pull up from +3VS to +5VS_AUDIO.

25.)Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.

26.)Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.

27.)Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.

28.)Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.

29.)Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.

30.)Page 45:Add L4506 and L4507 for EMI requirement.

<Variant Name>

Title : History(1)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

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<Variant Name>

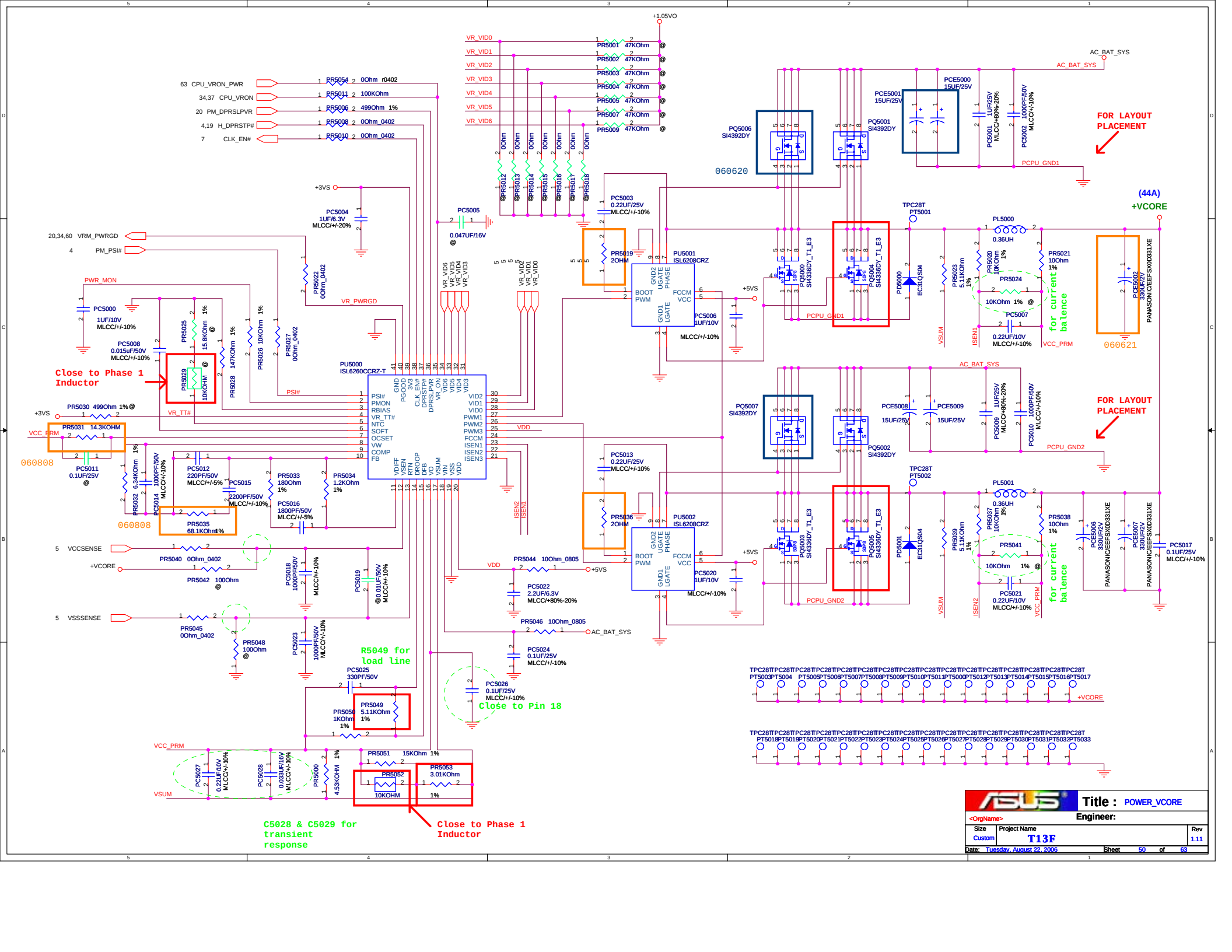
Title : History(2)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

Size	Project Name	Rev
Custom	T13F	1.11

Date: Tuesday, August 22, 2006 Sheet 49 of 63


+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5005 47KOhm
PR5007 47KOhm
PR5009 47KOhm
PR5012 0Ohm
PR5013 0Ohm
PR5014 0Ohm
PR5015 0Ohm
PR5016 0Ohm
PR5017 0Ohm
PR5018 0Ohm
63 CPU_VRON_PWR
34,37 CPU_VRON
20 PM_DPRSLPVR
4,19 H_DPRSTP#
7 CLK_EN#
PR5054 0Ohm r0402
PR5011 100KOhm
PR5006 499Ohm 1%
PR5008 0Ohm_0402
PR5010 0Ohm_0402
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5005 0.047UF/16V @
20,34,60 VRM_PWRGD
4 PM_PSI#
PWR_MON
PC5000 1UF/10V MLCC/+/-10%
PC5008 0.015uF/50V MLCC/+/-10%
PR5025 15.8KOhm 1%
PR5029 @
10KOHM
PR5028 147KOhm 1%
PR5026 10KOhm 1%
PR5027 0Ohm_0402
PR5022 0Ohm_0402
VR_PWRGD
PSI#
VR_TT#
Close to Phase 1 Inductor
PU5000 ISL6260CCRZ-T
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
GND
PGOOD
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
PWM1
PWM2
PWM3
FCCM
ISEN1
ISEN2
ISEN3
VDIFF
VSEN
RTN
DROOP
FB
VO
VSUM
VIN
VSS
VDD
PR5030 499Ohm 1%@
PR5031 14.3KOHM
VCC_PRM
060808
PC5011 0.1UF/25V @
PR5032 6.34KOhm 1%
PC5014 1000PF/50V MLCC/+/-10%
PC5012 220PF/50V MLCC/+/-5%
PC5015 2200PF/50V MLCC/+/-10%
PR5033 180Ohm 1%
PC5016 1800PF/50V MLCC/+/-5%
PR5034 1.2KOhm 1%
PR5035 68.1KOhm 1%
060808
5 VCCSENSE
+VCORE
PR5040 0Ohm_0402
PR5042 100Ohm @
PC5018 1000PF/50V MLCC/+/-10%
PC5019 @0.01UF/50V MLCC/+/-10%
5 VSSSENSE
PR5045 0Ohm_0402
PR5048 100Ohm @
PC5023 1000PF/50V MLCC/+/-10%
R5049 for load line
PC5025 330PF/50V
PR5049 5.11KOhm 1%
PR5050 1KOhm 1%
PC5026 0.1UF/25V MLCC/+/-10%
Close to Pin 18
VCC_PRM
PC5027 0.22UF/10V MLCC/+/-10%
PC5028 0.033UF/16V MLCC/+/-10%
PR5000 4.53KOHM 1%
VSUM
PR5051 15KOhm 1%
PR5052 10KOHM
PR5053 3.01KOhm 1%
C5028 & C5029 for transient response
Close to Phase 1 Inductor
PC5003 0.22UF/25V MLCC/+/-10%
PR5019 2OHM
PU5001 ISL6208CRZ
BOOT
PWM
GND2
UGATE
PHASE
GND1
LGATE
FCCM
VCC
PC5006 1UF/10V MLCC/+/-10%
PC5013 0.22UF/25V MLCC/+/-10%
PR5036 2OHM
PU5002 ISL6208CRZ
PC5020 1UF/10V MLCC/+/-10%
PR5044 10Ohm_0805
PC5022 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
PC5024 0.1UF/25V MLCC/+/-10%
+5VS
VDD
ISEN2
ISEN1
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
PQ5006 SI4392DY
PQ5001 SI4392DY
PQ5007 SI4392DY
PQ5002 SI4392DY
PQ5000 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PQ5003 SI4336DY_T1_E3
PQ5005 SI4336DY_T1_E3
PD5000 EC31QS04
PD5001 EC31QS04
PCE5000 15UF/25V
PCE5001 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/50V MLCC/+/-10%
PCE5008 15UF/25V
PCE5009 15UF/25V
PC5009 1UF/25V MLCC/+80%-20%
PC5010 1000PF/50V MLCC/+/-10%
FOR LAYOUT PLACEMENT
060620
TPC28T PT5001
TPC28T PT5002
PL5000 0.36UH
PL5001 0.36UH
PR5020 10KOhm 1%
PR5021 10Ohm 1%
PR5024 10KOhm 1% @
PC5007 0.22UF/10V MLCC/+/-10%
PR5023 5.11KOhm 1%
PR5037 10KOhm 1%
PR5038 10Ohm 1%
PR5041 10KOhm 1% @
PC5021 0.22UF/10V MLCC/+/-10%
PR5039 5.11KOhm 1%
for current balence
PC5002 330UF/2V PANASONIC/EEFSX0D331XE
PC5006 330UF/2V PANASONIC/EEFSX0D331XE
PC5003 330UF/2V PANASONIC/EEFSX0D331XE
PC5017 0.1UF/25V MLCC/+/-10%
060621
(44A) +VCORE
TPC28T PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5000 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
+VCORE
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
<OrgName>
Engineer:
Size Custom
Project Name T13F
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Date: Tuesday, August 22, 2006
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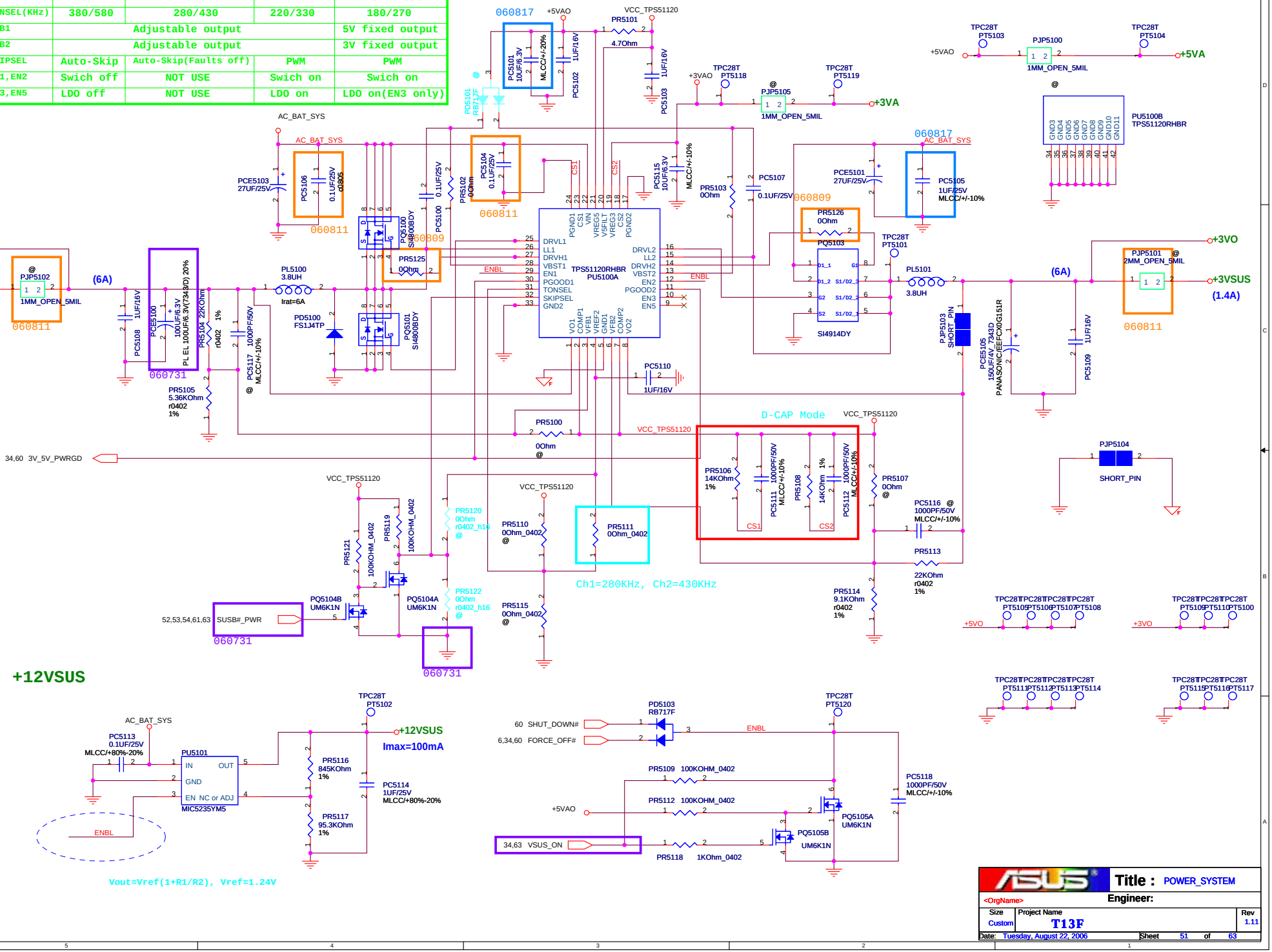
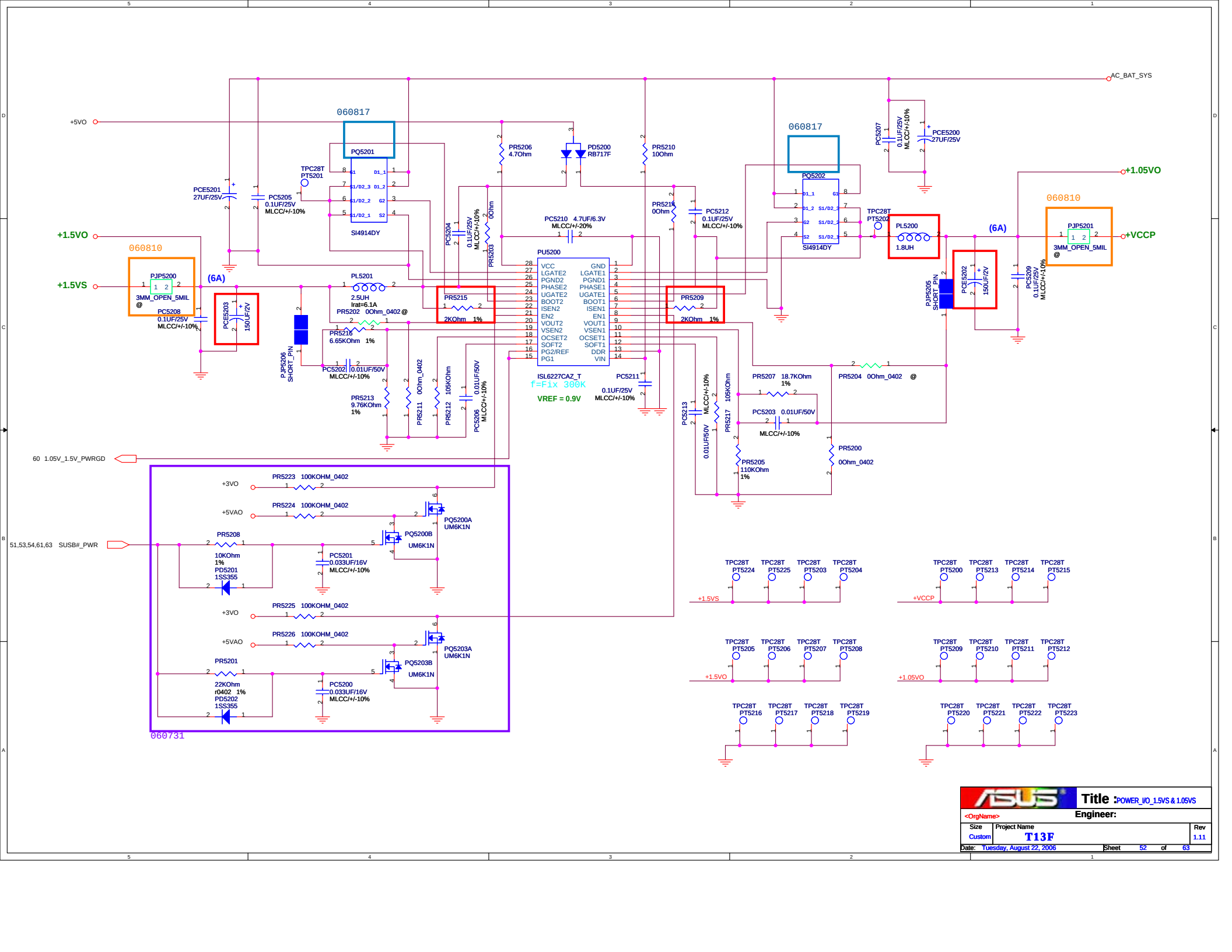
PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFB1	Adjustable output			5V fixed output
VFB2	Adjustable output			3V fixed output
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Swich on	Swich on
EN3,EN5	LDO off	NOT USE	LDO on	LDO on(EN3 only)



ASUS	Title : POWER_SYSTEM		
<OrgName>	Engineer:		
Size: Custom	Project Name: T13F		Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 51 of 63		


AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
060817
060810
060731
PQ5201
SI4914DY
PQ5202
SI4914DY
PU5200
ISL6227CAZ_T
f=Fix 300K
VREF = 0.9V
PL5201
2.5UH
Irat=6.1A
PL5200
1.8UH
PD5200
RB717F
PD5201
1SS355
PD5202
1SS355
PQ5200A
UM6K1N
PQ5200B
UM6K1N
PQ5203A
UM6K1N
PQ5203B
UM6K1N
PJP5200
3MM_OPEN_5MIL
@
PJP5201
3MM_OPEN_5MIL
@
PJP5205
SHORT_PIN
PJP5206
SHORT_PIN
(6A)
(6A)
PR5202 0Ohm_0402 @
PR5204 0Ohm_0402 @
PR5206 4.7Ohm
PR5207 18.7KOhm 1%
PR5208 10KOhm 1%
PR5209 2KOhm 1%
PR5210 10Ohm
PR5211 0Ohm_0402
PR5212 105KOhm
PR5213 9.76KOhm 1%
PR5215 2KOhm 1%
PR5216 6.65KOhm 1%
PR5217 105KOhm
PR5218 0Ohm
PR5219 0Ohm
PR5200 0Ohm_0402
PR5201 22KOhm r0402 1%
PR5205 110KOhm 1%
PR5223 100KOHM_0402
PR5224 100KOHM_0402
PR5225 100KOHM_0402
PR5226 100KOHM_0402
PC5200 0.033UF/16V MLCC/+/-10%
PC5201 0.033UF/16V MLCC/+/-10%
PC5202 0.01UF/50V MLCC/+/-10%
PC5203 0.01UF/50V MLCC/+/-10%
PC5205 0.1UF/25V MLCC/+/-10%
PC5206 0.01UF/50V MLCC/+/-10%
PC5207 0.1UF/25V MLCC/+/-10%
PC5208 0.1UF/25V MLCC/+/-10%
PC5209 0.1UF/25V MLCC/+/-10%
PC5210 4.7UF/6.3V MLCC/+/-20%
PC5211 0.1UF/25V MLCC/+/-10%
PC5212 0.1UF/25V MLCC/+/-10%
PC5213 0.01UF/50V MLCC/+/-10%
PCE5200 27UF/25V
PCE5201 27UF/25V
PC5202 150UF/2V
PC5203 150UF/2V
PC5204 0.1UF/25V MLCC/+/-10%
PC5217 0.01UF/50V MLCC/+/-10%
TPC28T PT5201
TPC28T PT5202
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
+3VO
+5VAO
TPC28T PT5224 PT5225 PT5203 PT5204 +1.5VS
TPC28T PT5200 PT5213 PT5214 PT5215 +VCCP
TPC28T PT5205 PT5206 PT5207 PT5208 +1.5VO
TPC28T PT5209 PT5210 PT5211 PT5212 +1.05VO
TPC28T PT5216 PT5217 PT5218 PT5219
TPC28T PT5220 PT5221 PT5222 PT5223
Title : POWER_I/O_1.5VS & 1.05VS
<OrgName>
Engineer:
Size Custom
Project Name T13F
Rev 1.11
Date: Tuesday, August 22, 2006
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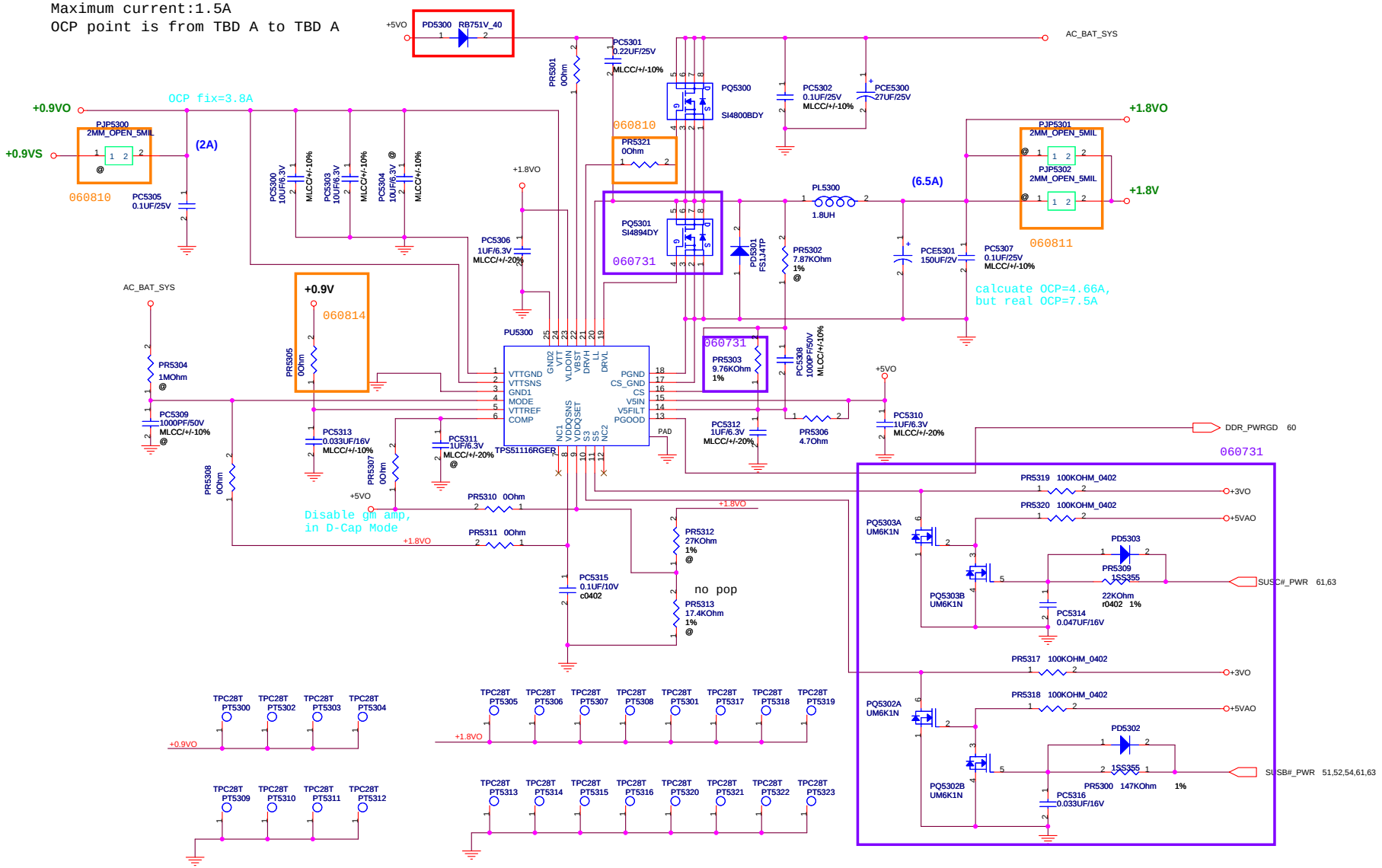
060811

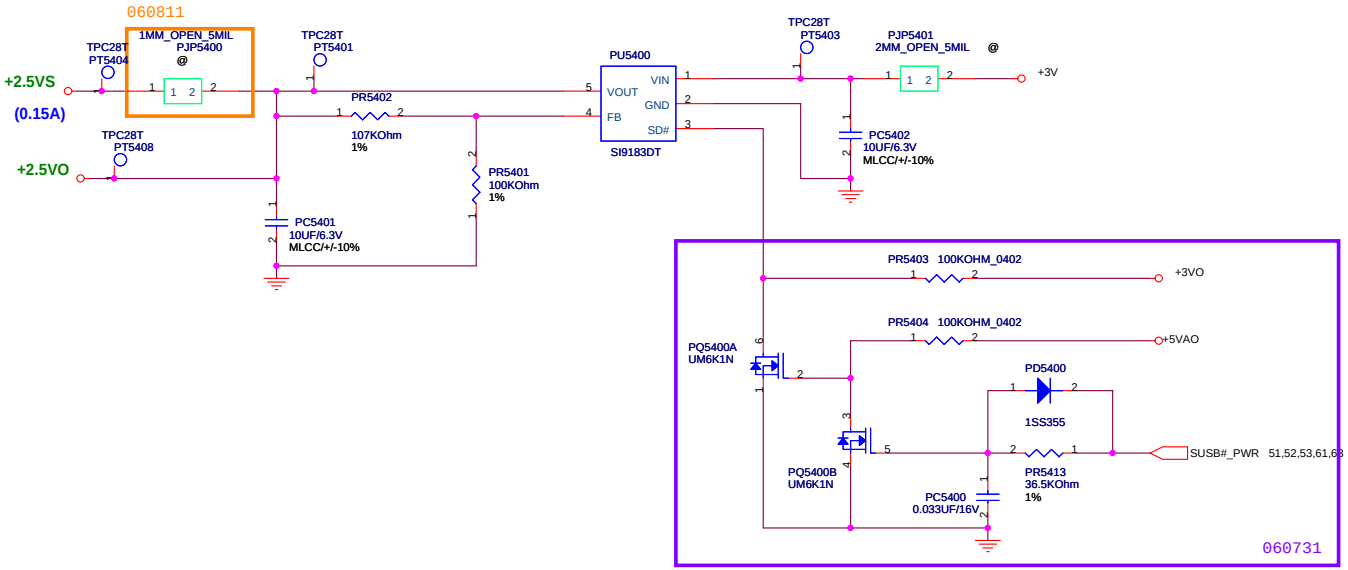
.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A



Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 53 of 14	

+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 54 of 63	

Title : EMPTY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	T13F	1.11

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Title : EMPTY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	T13F	1.11

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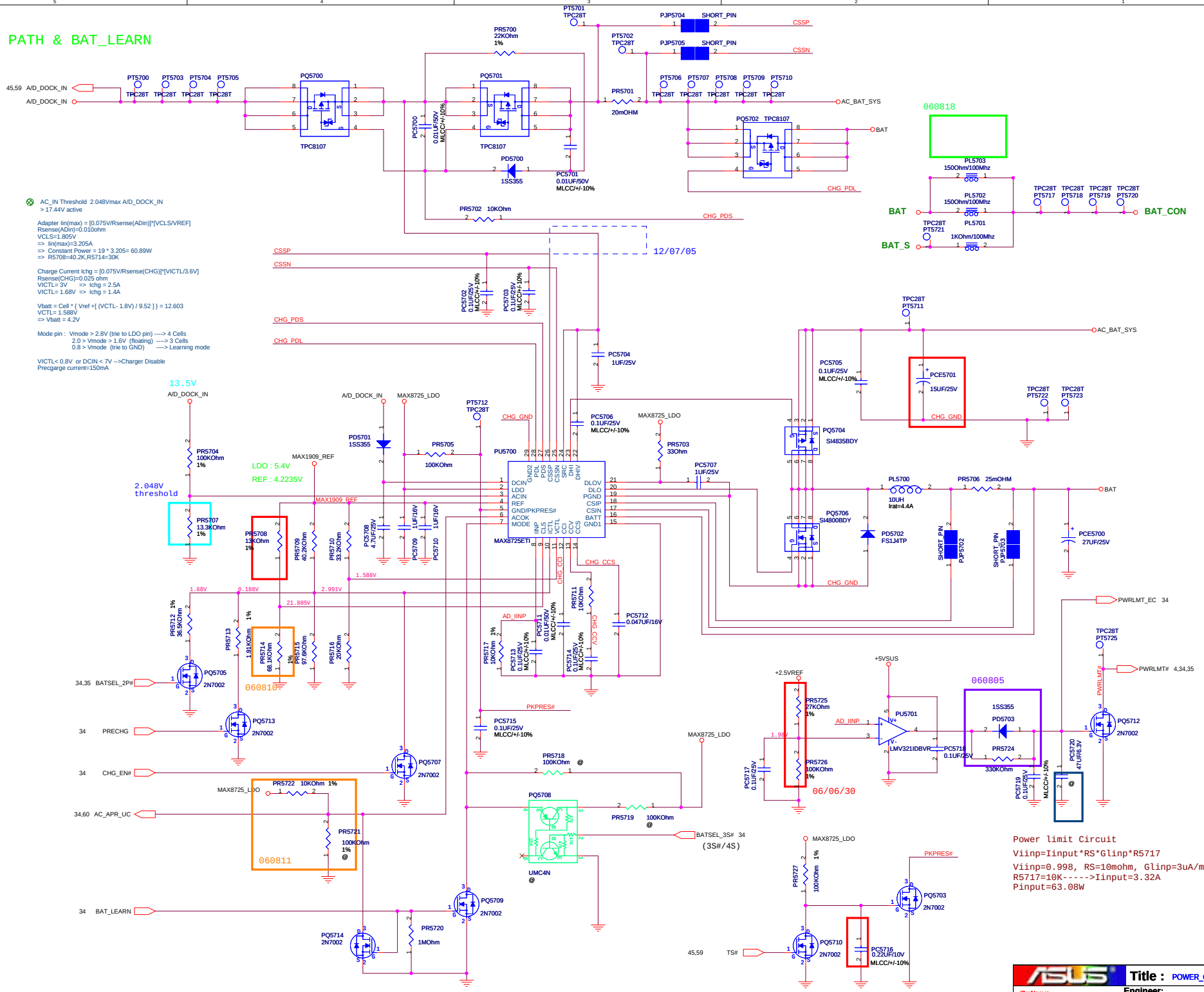
POWER PATH & BAT_LEARN



Title : POWER_PIC

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	T13F	1.11

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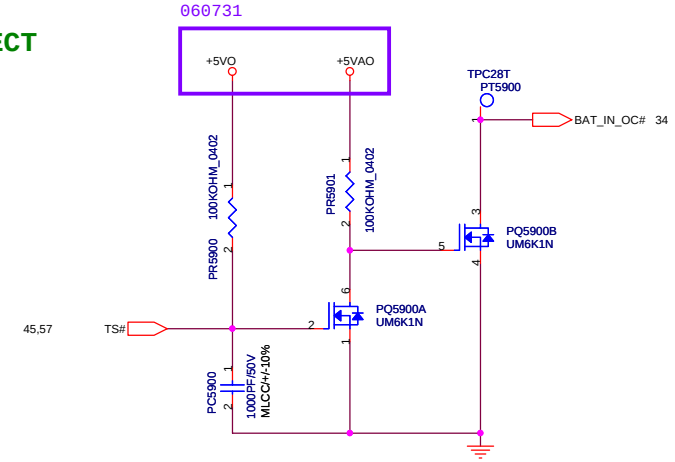
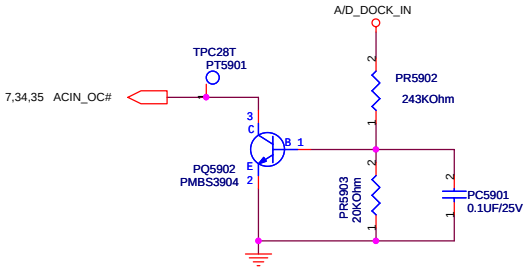
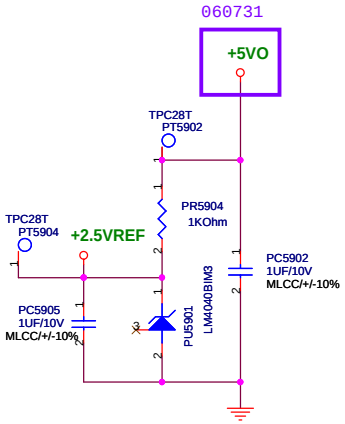
BATTERY IN DETECT



ADAPTER IN DETECT

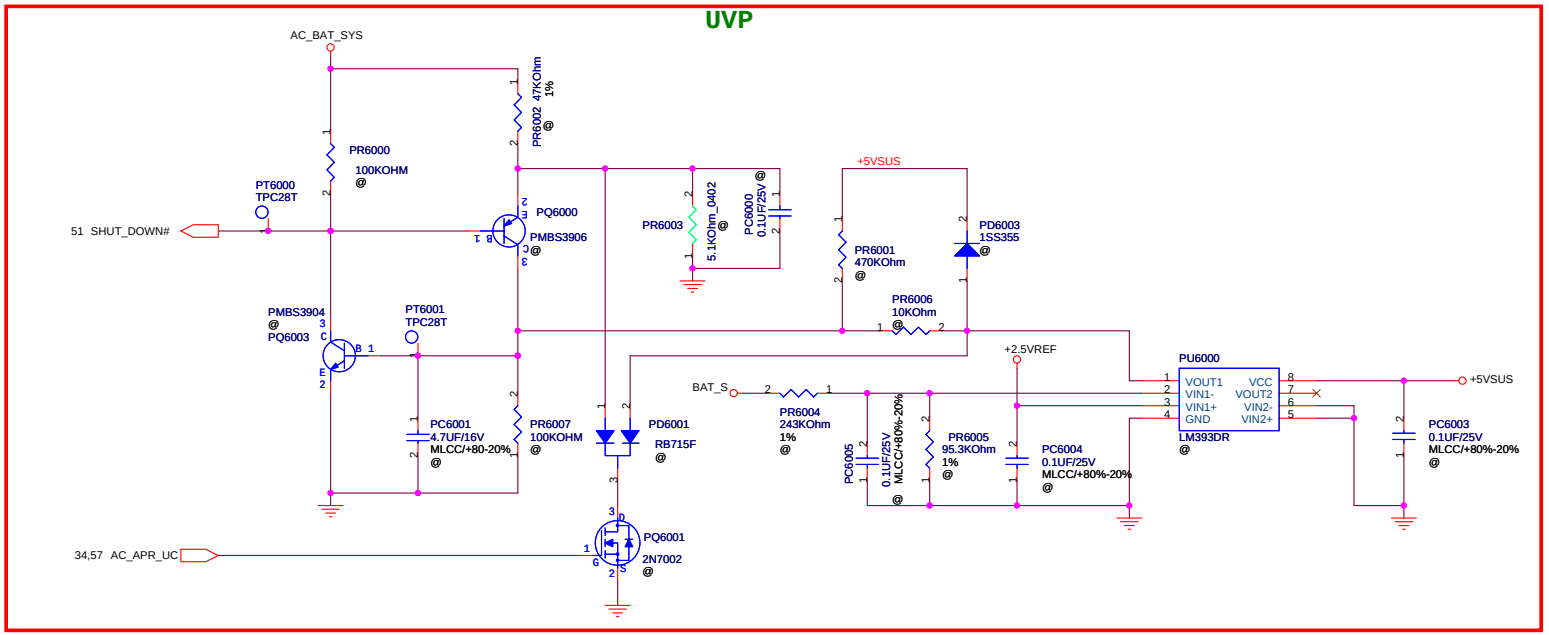


+5VLCM, +5VCHG & +2.5VREF

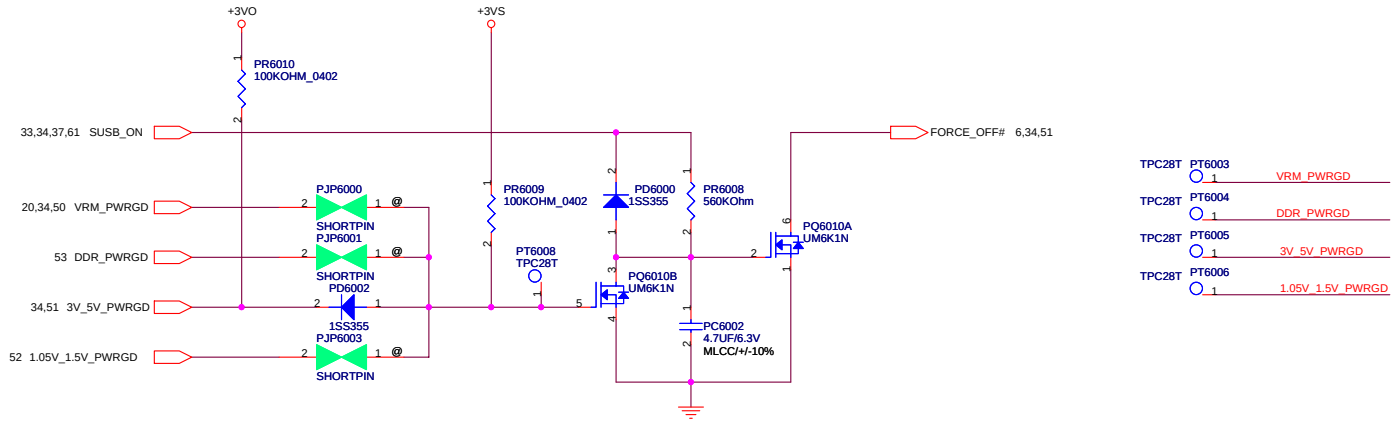


Title : POWER_DETECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 59 of 63	

UVP



POWER GOOD DETECTER



Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
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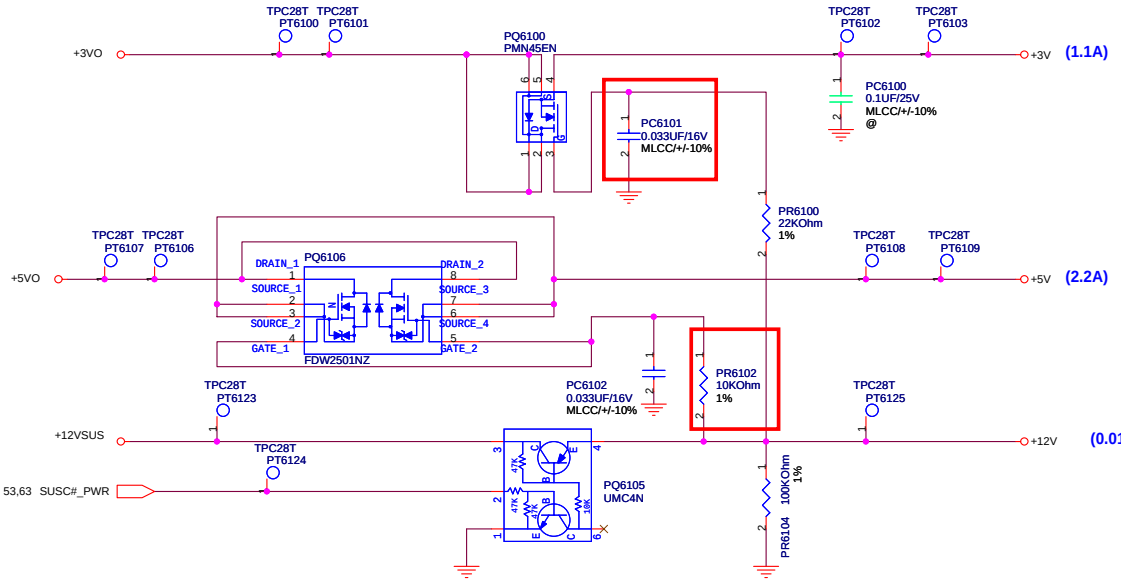
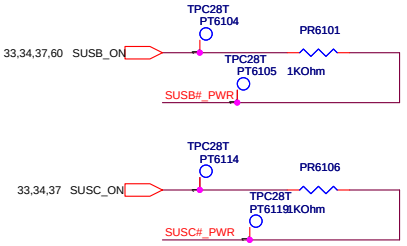
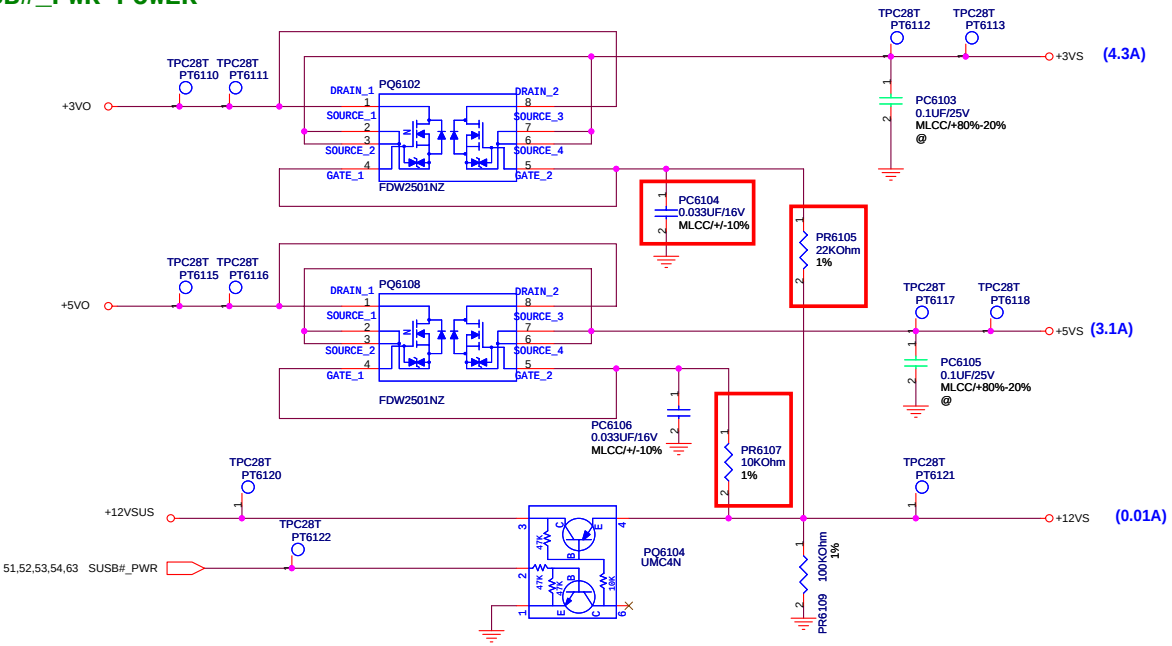
SUSC#_PWR POWER





SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
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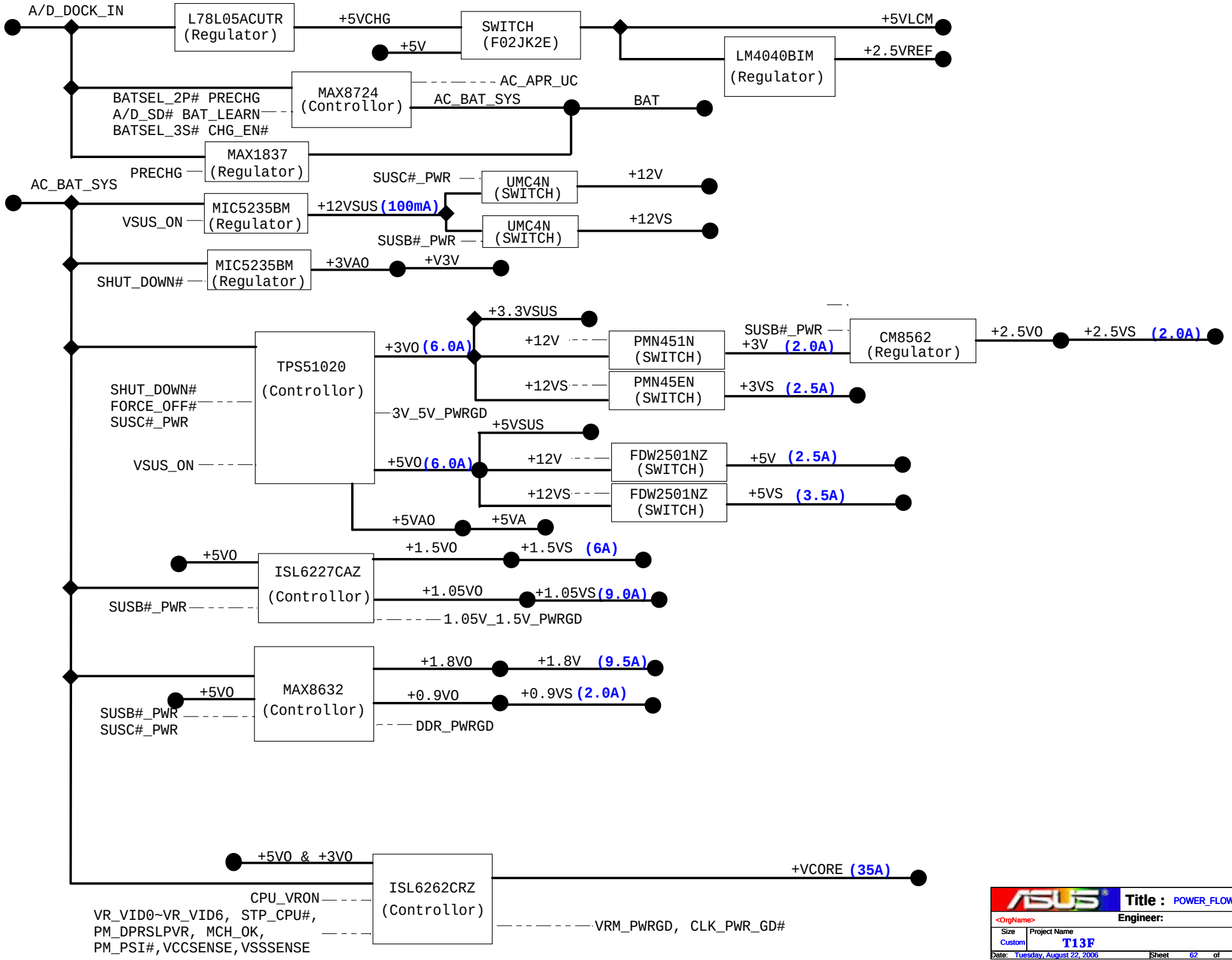

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: T13F	Rev: 1.11
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AC_BAT_SYS → AC_BAT_SYS 17,50,51,52,53,57,60

+3VA → +3VA 6,17,19,34,37,51

+5VA → +5VA 6,51

+5VO → +5VO 51,52,53,59,61

+3VO → +3VO 51,52,53,54,60,61

+3VSUS → +3VSUS 17,20,21,22,29,31,39,51

+5VSUS → +5VSUS 22,51,57,60

+3V → +3V 21,25,26,27,28,33,35,37,54,61

+3VS → +3VS 6,7,9,11,13,14,15,17,18,20,21,22,23,25,26,27,29,30,33,34,36,37,38,39,50,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 24,31,37,61

+12VS → +12VS 17,37,61

+5V → +5V 6,17,24,28,33,37,61

+5VS → +5VS 6,18,22,23,25,30,31,34,37,38,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 11,37,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 9,12,14,15,37,53

+VCCP → +VCCP 5,12,22,37,52

+0.9VS → +0.9VS 16,37,53

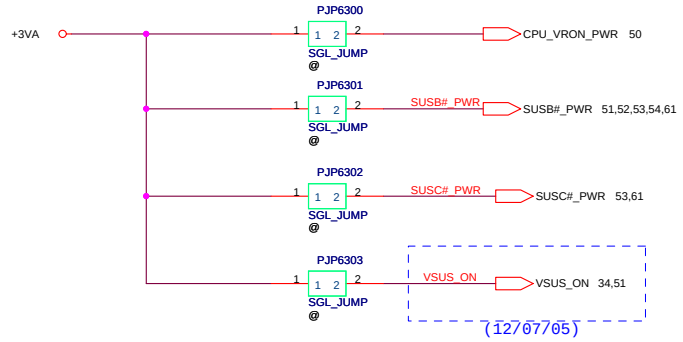
BAT → BAT 57

+2.5VREF → +2.5VREF 57,59,60

+VCORE → +VCORE 5,37,50

BAT_CON → BAT_CON 45,57

FOR POWER TEST



ASUS	Title : POWER_SIGNAL		
<OrgName>	Engineer:		
Size: Custom	Project Name: T13F		Rev: 1.11
Date: Tuesday, August 22, 2006	Sheet 63 of 63		