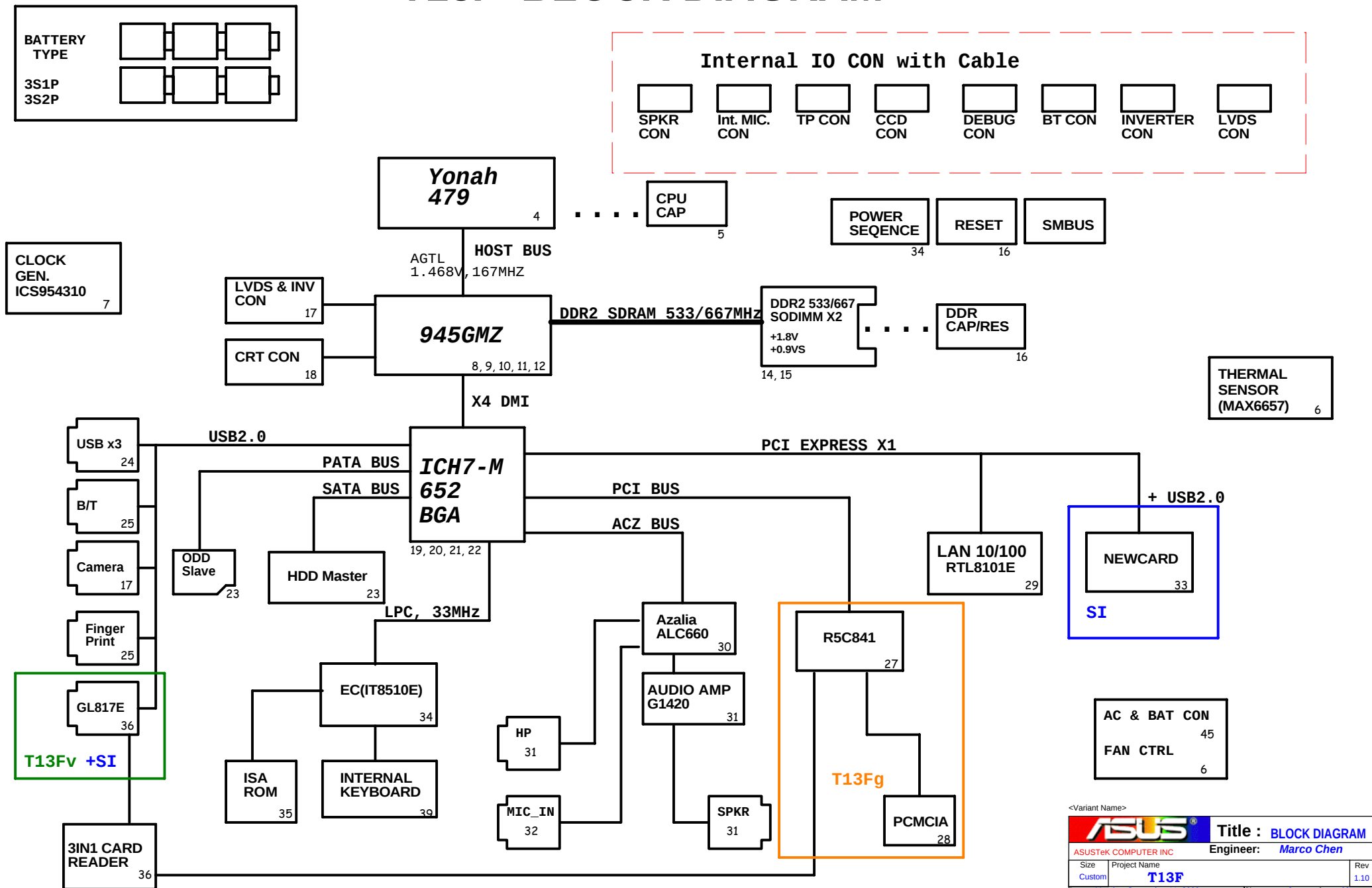


T13FG SCHEMATIC R1.10 FOR NEWCARD

PAGE	Content	PAGE	Content
SYSTEM PAGE REF.		47	EMPTY
4	YONAH CPU (1)	48	History(1)
5	YONAH CPU (2)	49	History(2)
6	FAN CTRL&Thernal protection	POWER PAGE REF.	
7	CLK GEN-ICS954310	50	POWER_VCORE
8	Calistoga--CPU	51	POWER_SYSTEM
9	Calistoga--PCIE	52	POWER_I/O_1.8V & 1.05VS
10	Calistoga--DDR2	53	POWER_I/O_DDR & VTT
11	Calistoga--POWER	54	POWER_I/O_VTT & +2.5VS
12	Calistoga--GND	55	POWER_VGA_CORE(Empty)
13	Calistoga--Strap	56	POWER_VGA_RAM(Empty)
14	DDR2 S0-DIMM_0	57	POWER_CHARGER
15	DDR2 S0-DIMM_1	58	POWER_PIC(Empty)
16	DDR2 ADDRESS TERMINATION	59	POWER_DETECT
17	LVDS & INVERTER CONN	60	POWER_PROTECT
18	VGA CONN	61	POWER_LOAD SWITCH
19	ICH7M--CPU, IDE, AUDIO	62	POWER_FLOWCHART
20	ICH7M--GPIO	63	POWER_SIGNAL
21	ICH7M--PCI, PCI-E, USB		
22	ICH7M--VCC, GND		
23	HDD & CD-ROM CONN		
24	USB PORT		
25	B/T & F/P		
26	B TO B CONN(M)		
27	CARDBUS R5C841		
28	PCMCIA SOCKET		
29	PCI-E--LAN_RTL8101E		
30	AZALIA - ALC660-GR		
31	AUDIO_AMPLIFIER		
32	MICROPHONE		
33	NEWCARD		
34	EC-IT8510E		
35	ISA ROM & Touch Pad & KB& FP		
36	Card Reader GL817E		
37	DISCHARGE		
38	Instant Key & FFC CONN		
39	LEDs		
40	EMPTY		
41	EMPTY		
42	EMPTY		
43	EMPTY		
44	EMPTY		
45	SREW HOLE		
46	DC & BAT IN		

T13F BLOCK DIAGRAM



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	N/A	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	N/A	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	PWRGEAR_LED	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	CR_DRIVER#	O
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PCI_RST#	I
31	ECSC#/#GPD3	EXT_SC#	O
41	GPD4	CR_POWER#	O
42	GIN1/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	WLAN_BTN#	I
88	ADC5/GPE1	N/A	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	N/A	
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/#WUI6/GPE6	LID_EC#	I
25	CLKRUN#/#WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	PWRLMT_EC#	I
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	N/A	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GP10	ICH7_PWROK	O
149	GP11	WATCH_DOG#	O
152	GP12	N/A	
155	GP13	CHG_EN#	O
156	GP14	PRECHG	O
168	GP15	BAT_LL#	O
174	GP16	BAT_LEARN	O
81	ADC0	N/A	
82	ADC1	N/A	
83	ADC2	N/A	
84	ADC3	SYS_TEMP	I
93	ADC8	KID0	
94	ADC9	KID1	
99	DAC0	N/A	
100	DAC1	N/A	
101	DAC2	INVTERR_DA	O
102	DAC3	BATSEL_2P#	O

ICH7M_PCI EXPRESS:

PCI-E Device	PAIR
RTL8101E	1
GOLAN	2
NEWCARD	3

ICH7M_SMBUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A4)
Thermal Sensor(MAX6657)	1001100x (98)

ICH7M_PCI_DEVICE:

PCI Device	IDSEL#	REQ/GNT#	Interrupts
R5C841	AD17	1	B, D

ICH7M_GPIO

Pin	Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#
GPIO 01	i	GPI	PCI_REQ#5
GPIO [5:2]	i	GPI	PCI_INT[E:H]#
GPIO 06	i	GPO	BT_LED_EN
GPIO 07	i	GPI	N/A
GPIO 08	i	GPI	EXTSMI#
GPIO 09	i	GPI	N/A
GPIO 10	i	GPI	N/A
GPIO 11	i	Native	SMB_ALERT#
GPIO 12	i	GPI	KBC_SCI#
GPIO 13	i	GPI	N/A
GPIO 14	i	GPI	N/A
GPIO 15	i	GPO	802_LED_EN
GPIO 16	O 0	GPO	PM DPRSLPVR
GPIO 17	O 1	GPO	PCI_GNT#5
GPIO 18	O 1	GPO	STP_PCI#
GPIO 19	i 1	GPI	N/A
GPIO 20	O 1	GPO	STP_CPU#
GPIO 21	i 1	GPO	N/A
GPIO 22	i 1	Native	PCI_REQ#4
GPIO 23	i 1	Native	N/A
GPIO 24	O 0	GPO	MSK_PCIRST
GPIO 25	O 1	GPO	CB_SD#
GPIO 26	O 0	GPO	BT_ON#
GPIO 27	O 0	GPO	WLAN_ON#
GPIO 28	O 0	GPO	MEMROM/YONAH#
GPIO 29	i 0	Native	USB_OC#5
GPIO 30	i 0	Native	USB_OC#6
GPIO 31	i 0	Native	USB_OC#7
GPIO 32	O 1	GPO	PM_CLKRUN#
GPIO 33	O 1	GPO	N/A
GPIO 34	O 0	GPO	CPU_Select
GPIO 35	O 0	GPO	N/A
GPIO 36	i 0	GPO	N/A
GPIO 37	i 0	GPI	PCB_ID0
GPIO 38	i 0	GPI	PCB_ID1
GPIO 39	i 0	GPI	PCB_ID2
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

<Variant Name>



Title : Schematic data

ASUSTek COMPUTER INC

Engineer: Marco Chen

Size

Project Name

Rev

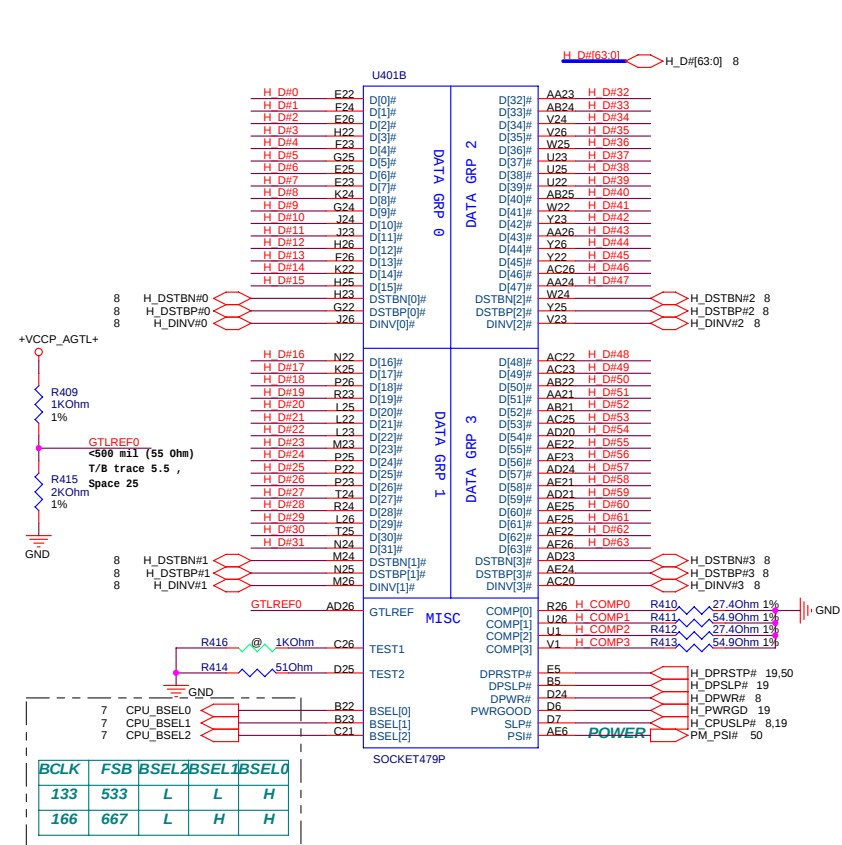
Custom

T13F

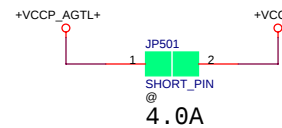
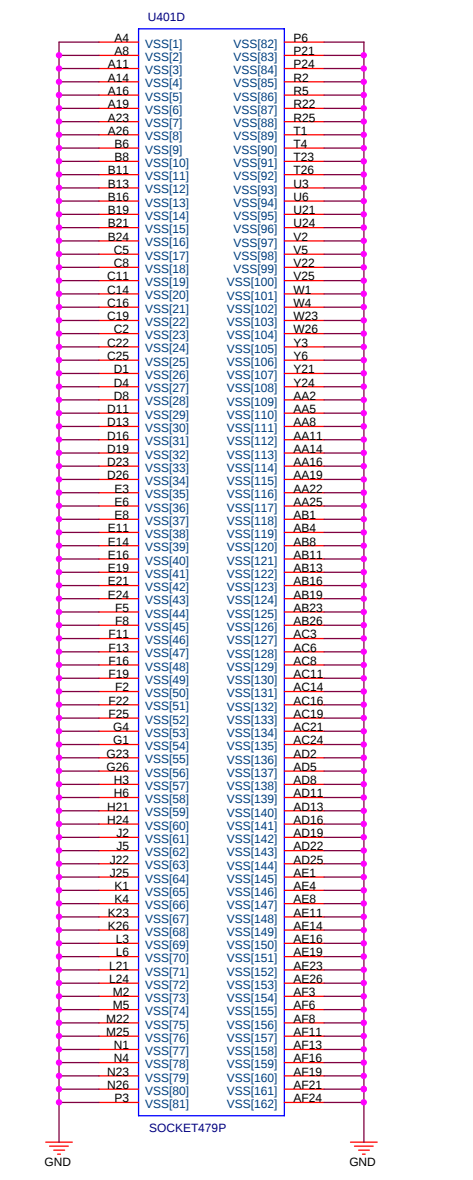
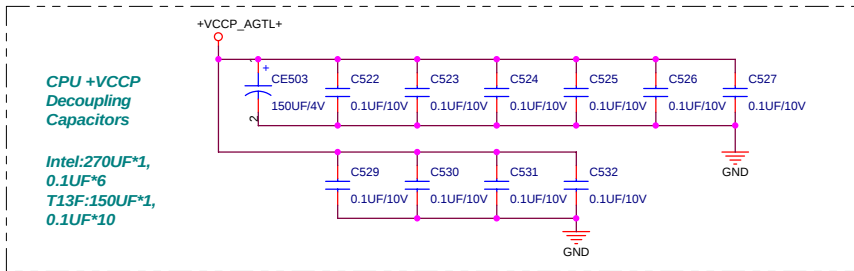
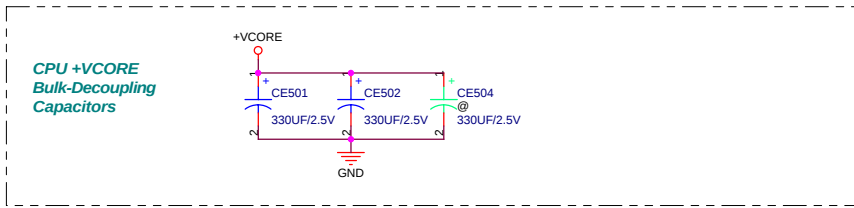
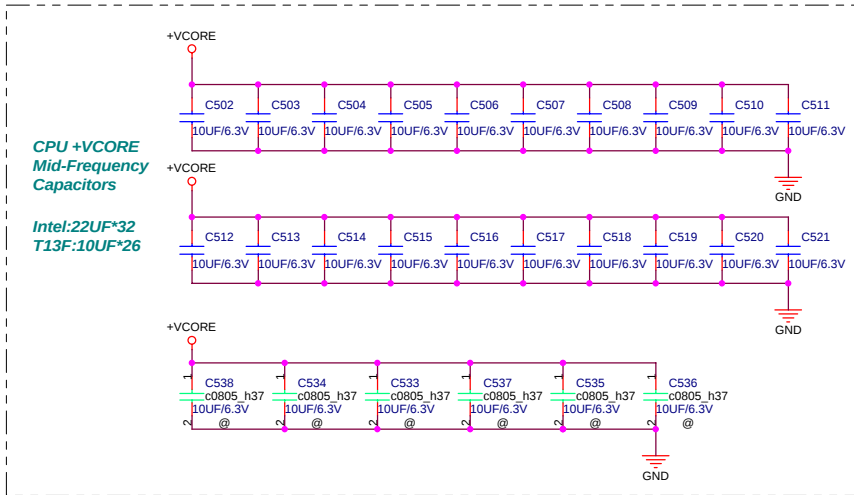
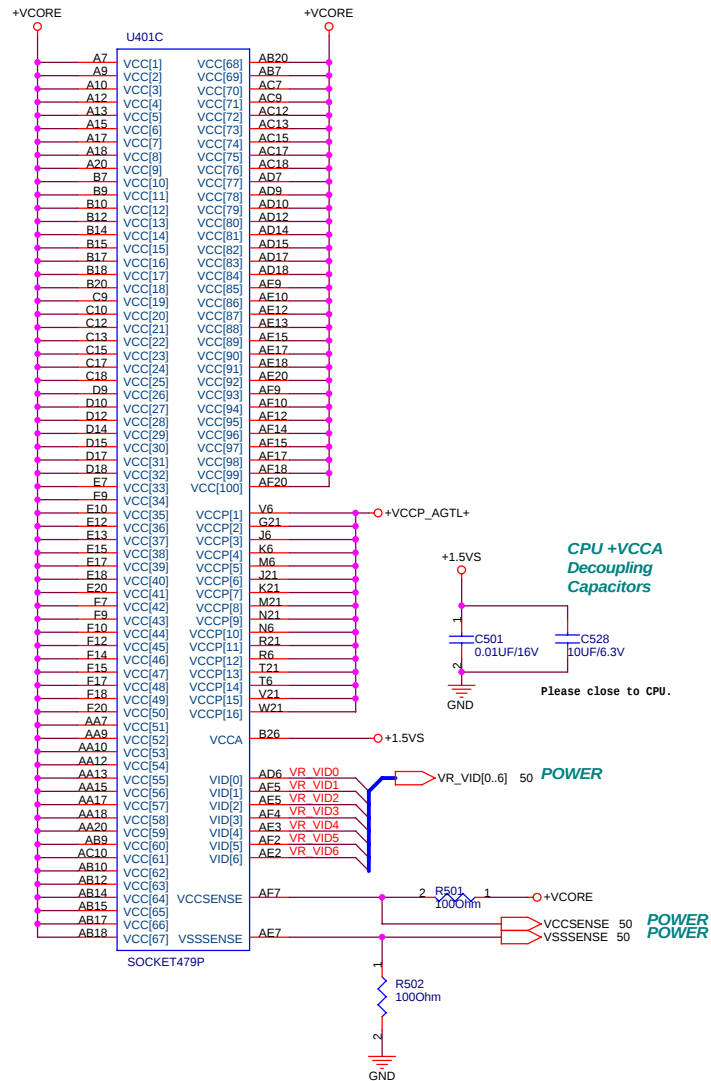
1.10

Date: Monday, September 11, 2006

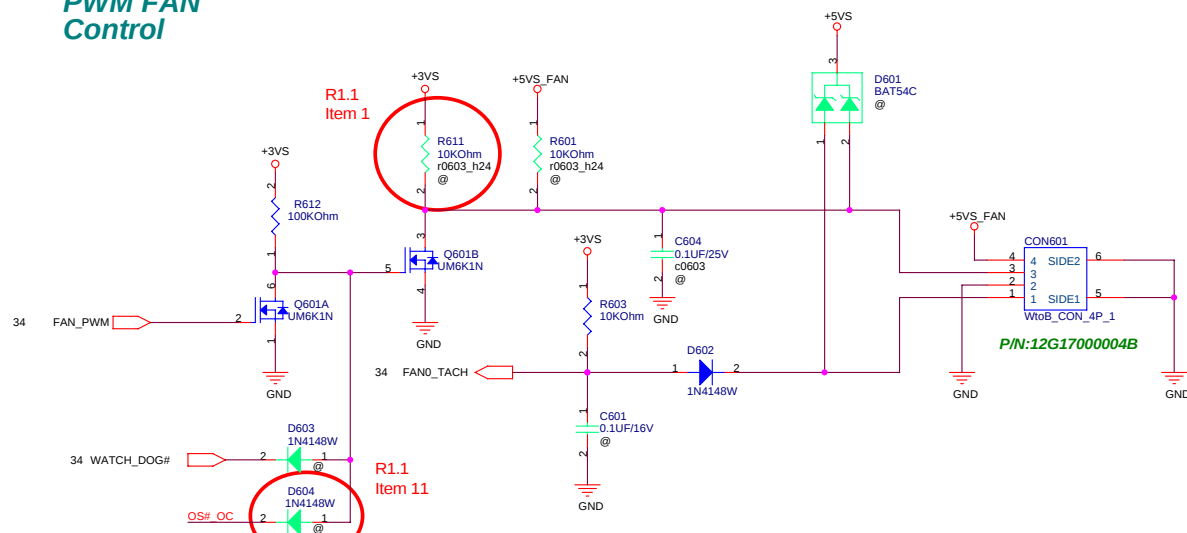
Sheet 3 of 63



		Title : YONAH CPU (1)	
ASUSTeK COMPUTER INC.		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006		Sheet 4	of 63

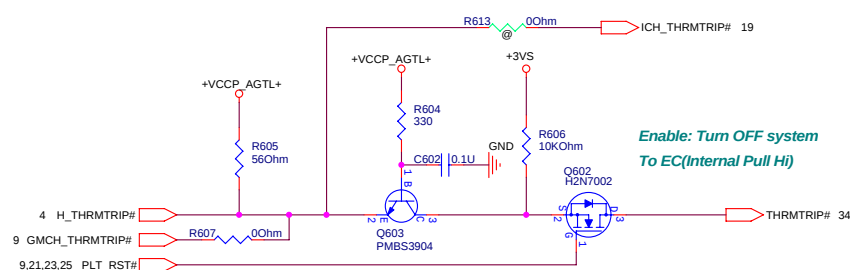
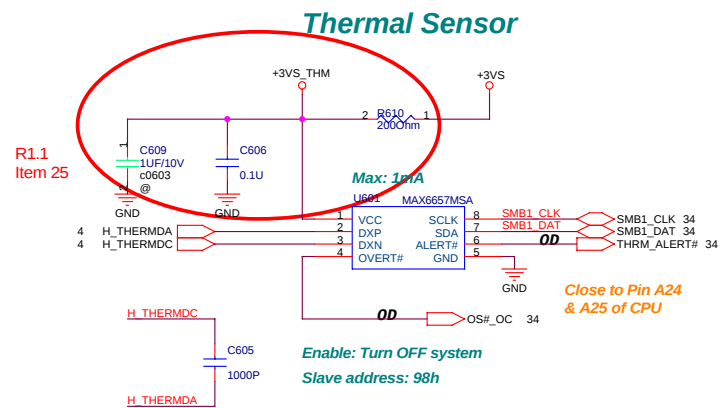
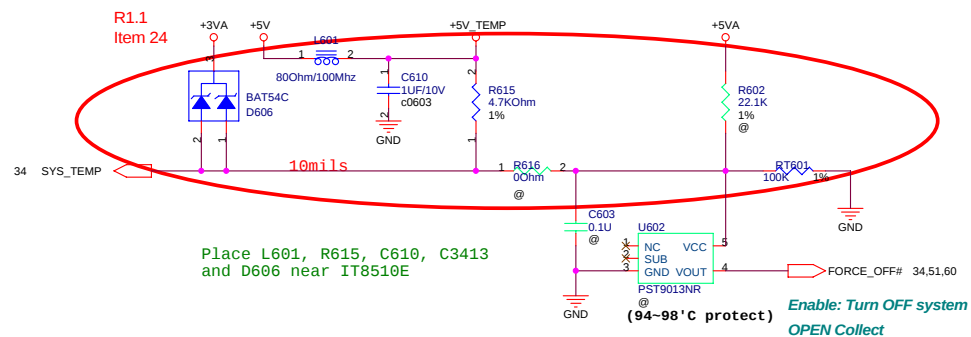


PWM FAN Control



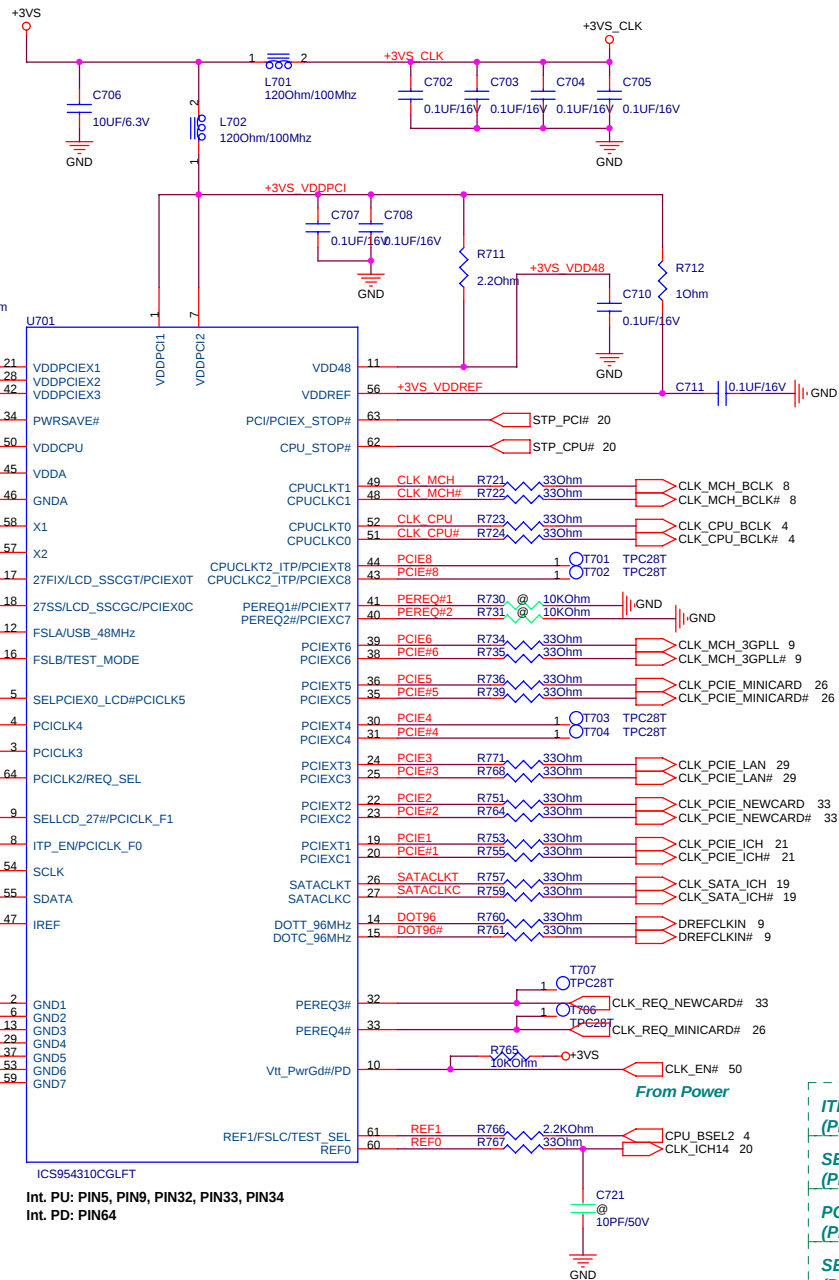
CPU FAN will be forced on:

- 1) Thermal Sensor Over-temperature
- 2) WATCHDOG asserted by EC



CPU_BSEL0 R701 1KOhm MCH_BSEL0 9
CPU_BSEL1 R702 1KOhm MCH_BSEL1 9
CPU_BSEL2 R705 1KOhm MCH_BSEL2 9

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



PLACE termination close to source IC

CLK_MCH_BCLK R703 49.9Ohm 1%
CLK_MCH_BCLK# R704 49.9Ohm 1%
CLK_CPU_BCLK R706 49.9Ohm 1%
CLK_CPU_BCLK# R708 49.9Ohm 1%
CLK_PCIE_MINICARD R709 49.9Ohm 1%
CLK_PCIE_MINICARD# R710 49.9Ohm 1%
CLK_MCH_3GPLL R713 49.9Ohm 1%
CLK_MCH_3GPLL# R715 49.9Ohm 1%
CLK_PCIE_ICH R717 49.9Ohm 1%
CLK_PCIE_ICH# R718 49.9Ohm 1%
CLK_PCIE_NEWCARD R763 49.9Ohm 1%
CLK_PCIE_NEWCARD# R750 49.9Ohm 1%
CLK_PCIE_LAN R769 49.9Ohm 1%
CLK_PCIE_LAN# R770 49.9Ohm 1%
CLK_SATA_ICH R726 49.9Ohm 1%
CLK_SATA_ICH# R728 49.9Ohm 1%
DREFCLKIN R737 49.9Ohm 1%
DREFCLKIN# R741 49.9Ohm 1%
DREFSSCLKIN R744 49.9Ohm 1%
DREFSSCLKIN# R746 49.9Ohm 1%

PEREQ#1: PCIE0, PCIE6
PEREQ#2: PCIE1, PCIE8
PEREQ#3: PCIE2, PCIE4
PEREQ#4: PCIE3, PCIE5, PCIE7

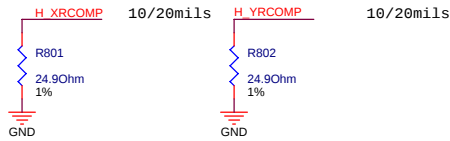
Latched Input Select

/ PIN9	PIN5	PIN17	PIN18
* 0	X	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIE0_T	PCIE0_C

ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELCED_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

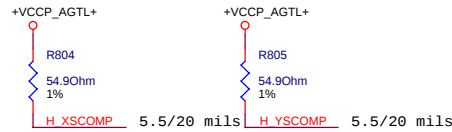
RCOMP

For Calibrating FSB I/O Buffer



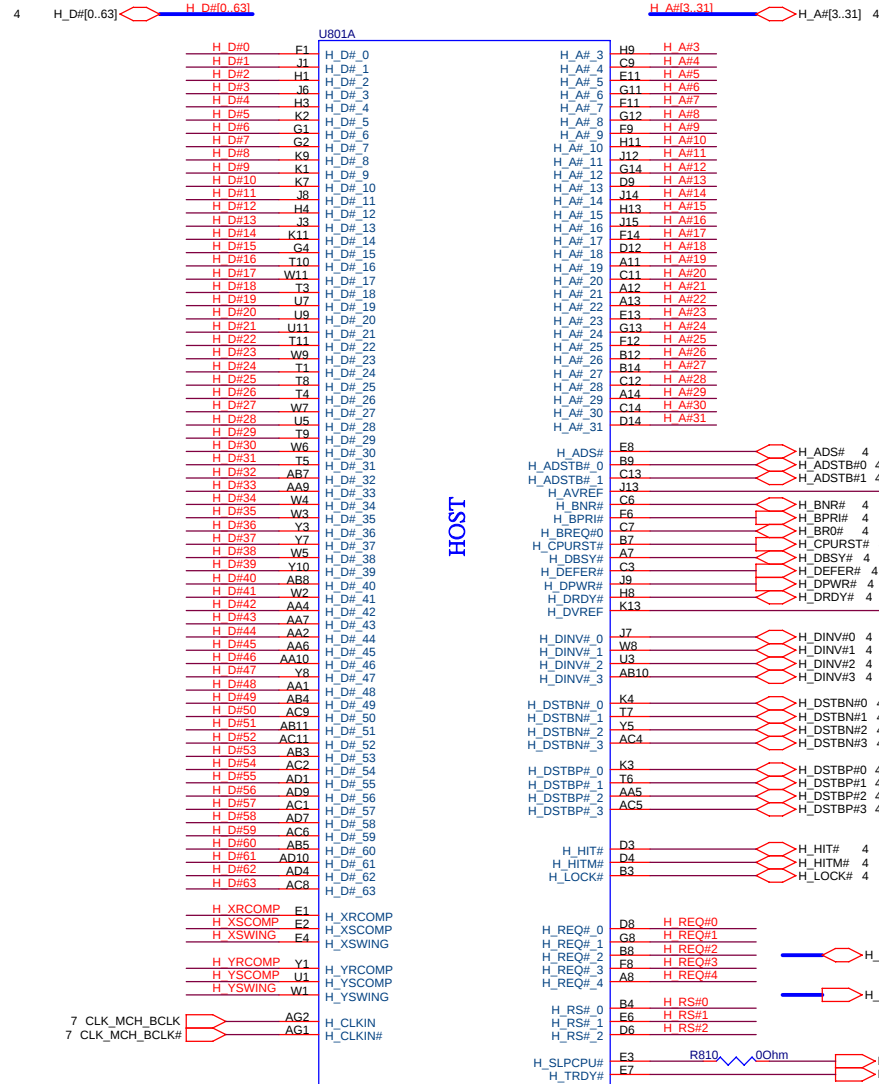
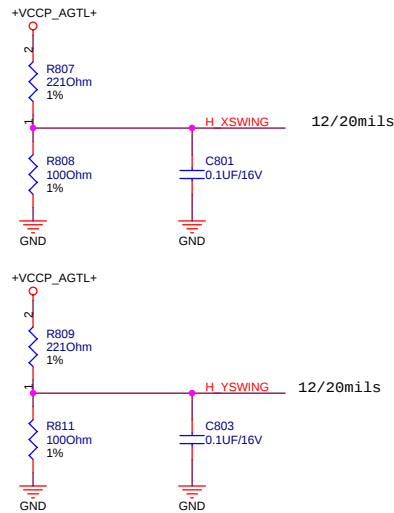
SCOMP

For Slew Rate Compensation on the FSB

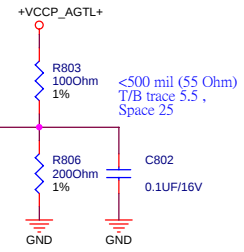


Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit



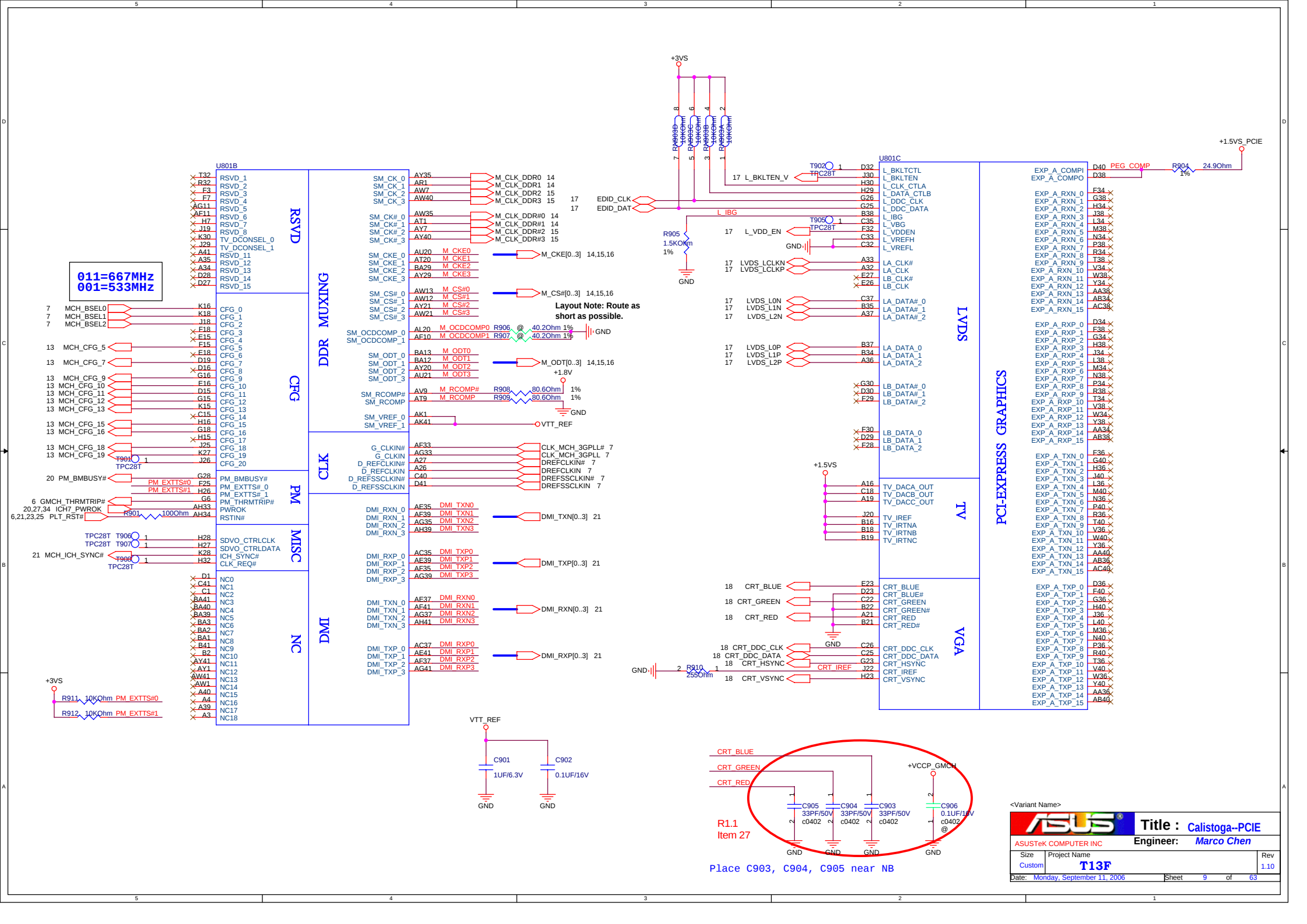
AGTL+ I/O Voltage Reference



H_CPURST# 1

T801 TPC28T

<Variant Name>



14 M_A_DQ[0..63]

U801D

M_A_DQ0	A135	SA_DQ0
M_A_DQ1	A134	SA_DQ1
M_A_DQ2	AM31	SA_DQ2
M_A_DQ3	AM33	SA_DQ3
M_A_DQ4	A136	SA_DQ4
M_A_DQ5	AK35	SA_DQ5
M_A_DQ6	A132	SA_DQ6
M_A_DQ7	AH31	SA_DQ7
M_A_DQ8	AN35	SA_DQ8
M_A_DQ9	AP33	SA_DQ9
M_A_DQ10	AB31	SA_DQ10
M_A_DQ11	AP31	SA_DQ11
M_A_DQ12	AN38	SA_DQ12
M_A_DQ13	AM36	SA_DQ13
M_A_DQ14	AM34	SA_DQ14
M_A_DQ15	AN33	SA_DQ15
M_A_DQ16	AK26	SA_DQ16
M_A_DQ17	AL27	SA_DQ17
M_A_DQ18	AM26	SA_DQ18
M_A_DQ19	AN24	SA_DQ19
M_A_DQ20	AK28	SA_DQ20
M_A_DQ21	AL28	SA_DQ21
M_A_DQ22	AM24	SA_DQ22
M_A_DQ23	AP28	SA_DQ23
M_A_DQ24	AP23	SA_DQ24
M_A_DQ25	AL22	SA_DQ25
M_A_DQ26	AP21	SA_DQ26
M_A_DQ27	AN20	SA_DQ27
M_A_DQ28	AL23	SA_DQ28
M_A_DQ29	AP24	SA_DQ29
M_A_DQ30	AP20	SA_DQ30
M_A_DQ31	AT21	SA_DQ31
M_A_DQ32	AR12	SA_DQ32
M_A_DQ33	AR14	SA_DQ33
M_A_DQ34	AP13	SA_DQ34
M_A_DQ35	AP12	SA_DQ35
M_A_DQ36	AT13	SA_DQ36
M_A_DQ37	AT12	SA_DQ37
M_A_DQ38	AL14	SA_DQ38
M_A_DQ39	AL12	SA_DQ39
M_A_DQ40	AK9	SA_DQ40
M_A_DQ41	AN7	SA_DQ41
M_A_DQ42	AK8	SA_DQ42
M_A_DQ43	AK7	SA_DQ43
M_A_DQ44	AP9	SA_DQ44
M_A_DQ45	AN9	SA_DQ45
M_A_DQ46	AT5	SA_DQ46
M_A_DQ47	AL5	SA_DQ47
M_A_DQ48	AY2	SA_DQ48
M_A_DQ49	AW2	SA_DQ49
M_A_DQ50	AP1	SA_DQ50
M_A_DQ51	AN2	SA_DQ51
M_A_DQ52	AV2	SA_DQ52
M_A_DQ53	AT3	SA_DQ53
M_A_DQ54	AN1	SA_DQ54
M_A_DQ55	AL2	SA_DQ55
M_A_DQ56	AG7	SA_DQ56
M_A_DQ57	AF9	SA_DQ57
M_A_DQ58	AG4	SA_DQ58
M_A_DQ59	AF6	SA_DQ59
M_A_DQ60	AG9	SA_DQ60
M_A_DQ61	AH6	SA_DQ61
M_A_DQ62	AF4	SA_DQ62
M_A_DQ63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M_A_BS#0 14,16
SA_BS_1	AV14	M_A_BS#1 14,16
SA_BS_2	BA20	M_A_BS#2 14,16
SA_CAS#	AY13	M_A_CAS# 14,16
SA_DM_0	AJ33	M_A_DM0
SA_DM_1	AM35	M_A_DM1
SA_DM_2	AL26	M_A_DM2
SA_DM_3	AN22	M_A_DM3
SA_DM_4	AM14	M_A_DM4
SA_DM_5	AL9	M_A_DM5
SA_DM_6	AR3	M_A_DM6
SA_DM_7	AH4	M_A_DM7
SA_DQS_0	AK33	M_A_DQS0
SA_DQS_1	AT33	M_A_DQS1
SA_DQS_2	AN28	M_A_DQS2
SA_DQS_3	AM22	M_A_DQS3
SA_DQS_4	AN12	M_A_DQS4
SA_DQS_5	AN8	M_A_DQS5
SA_DQS_6	AP3	M_A_DQS6
SA_DQS_7	AG5	M_A_DQS7
SA_DQS#_0	AK32	M_A_DQS#0
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SA_DQS#_2	AM21	M_A_DQS#2
SA_DQS#_3	AM12	M_A_DQS#3
SA_DQS#_4	AL8	M_A_DQS#4
SA_DQS#_5	AN3	M_A_DQS#5
SA_DQS#_6	AH5	M_A_DQS#6
SA_DQS#_7	AY16	M_A_A0
SA_MA_0	AU14	M_A_A1
SA_MA_1	AW16	M_A_A2
SA_MA_2	BA16	M_A_A3
SA_MA_3	BA17	M_A_A4
SA_MA_4	AU16	M_A_A5
SA_MA_5	AV17	M_A_A6
SA_MA_6	AU17	M_A_A7
SA_MA_7	AW17	M_A_A8
SA_MA_8	AT16	M_A_A9
SA_MA_9	AU13	M_A_A10
SA_MA_10	AT17	M_A_A11
SA_MA_11	AV20	M_A_A12
SA_MA_12	AV12	M_A_A13
SA_MA_13		
SA_RAS#	AW14	M_A_RAS# 14,16
SA_RCVENIN#	AK23	
SA_RCVENOUT#	AK24	
SA_WE#	AY14	M_A_WE# 14,16

15 M_B_DQ[0..63]

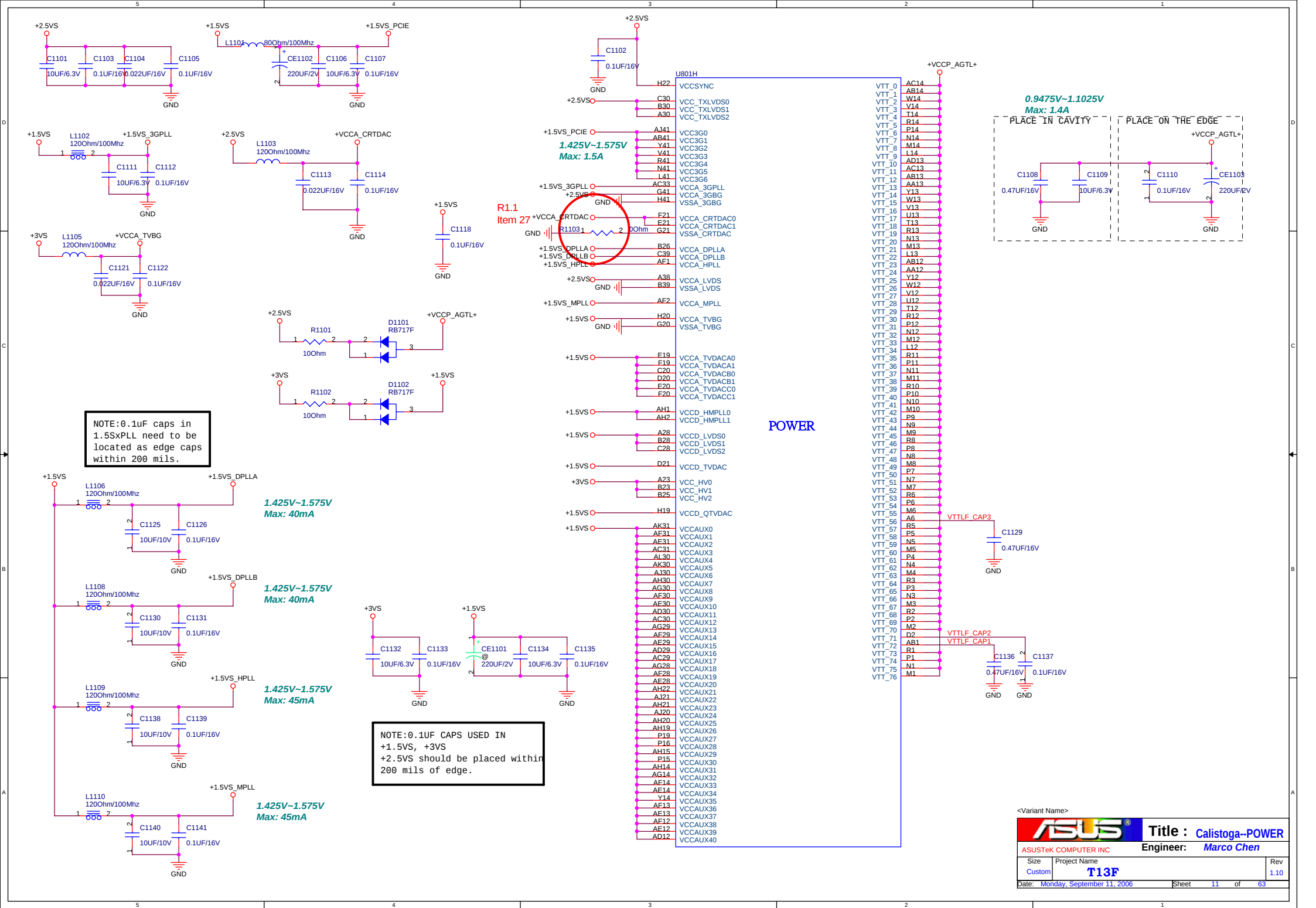
U801E

M_B_DQ0	AK39	SB_DQ0
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M_B_DQ4	AK38	SB_DQ4
M_B_DQ5	AJ38	SB_DQ5
M_B_DQ6	AN41	SB_DQ6
M_B_DQ7	AP41	SB_DQ7
M_B_DQ8	AT40	SB_DQ8
M_B_DQ9	AV41	SB_DQ9
M_B_DQ10	AU38	SB_DQ10
M_B_DQ11	AV38	SB_DQ11
M_B_DQ12	AP38	SB_DQ12
M_B_DQ13	AR40	SB_DQ13
M_B_DQ14	AW38	SB_DQ14
M_B_DQ15	AY38	SB_DQ15
M_B_DQ16	BA38	SB_DQ16
M_B_DQ17	AV36	SB_DQ17
M_B_DQ18	AR36	SB_DQ18
M_B_DQ19	AP36	SB_DQ19
M_B_DQ20	BA36	SB_DQ20
M_B_DQ21	AU36	SB_DQ21
M_B_DQ22	AP35	SB_DQ22
M_B_DQ23	AP34	SB_DQ23
M_B_DQ24	AY33	SB_DQ24
M_B_DQ25	BA33	SB_DQ25
M_B_DQ26	AT31	SB_DQ26
M_B_DQ27	AU29	SB_DQ27
M_B_DQ28	AU31	SB_DQ28
M_B_DQ29	AW31	SB_DQ29
M_B_DQ30	AV29	SB_DQ30
M_B_DQ31	AW29	SB_DQ31
M_B_DQ32	AM19	SB_DQ32
M_B_DQ33	AL19	SB_DQ33
M_B_DQ34	AP14	SB_DQ34
M_B_DQ35	AP14	SB_DQ35
M_B_DQ36	AM17	SB_DQ36
M_B_DQ37	AM16	SB_DQ37
M_B_DQ38	AP15	SB_DQ38
M_B_DQ39	AL15	SB_DQ39
M_B_DQ40	AJ11	SB_DQ40
M_B_DQ41	AH10	SB_DQ41
M_B_DQ42	AJ9	SB_DQ42
M_B_DQ43	AN10	SB_DQ43
M_B_DQ44	AK13	SB_DQ44
M_B_DQ45	AH11	SB_DQ45
M_B_DQ46	AK10	SB_DQ46
M_B_DQ47	AJ8	SB_DQ47
M_B_DQ48	BA10	SB_DQ48
M_B_DQ49	AW10	SB_DQ49
M_B_DQ50	BA4	SB_DQ50
M_B_DQ51	AW4	SB_DQ51
M_B_DQ52	AY10	SB_DQ52
M_B_DQ53	AY9	SB_DQ53
M_B_DQ54	AW5	SB_DQ54
M_B_DQ55	AY5	SB_DQ55
M_B_DQ56	AV4	SB_DQ56
M_B_DQ57	AR5	SB_DQ57
M_B_DQ58	AK4	SB_DQ58
M_B_DQ59	AK3	SB_DQ59
M_B_DQ60	AT4	SB_DQ60
M_B_DQ61	AK5	SB_DQ61
M_B_DQ62	AJ5	SB_DQ62
M_B_DQ63	AJ3	SB_DQ63

DDR SYSTEM MEMORY B

SB_BS_0	AT24	M_B_BS#0 15,16
SB_BS_1	AV23	M_B_BS#1 15,16
SB_BS_2	AY28	M_B_BS#2 15,16
SB_CAS#	AR24	M_B_CAS# 15,16
SB_DM_0	AK36	M_B_DM0
SB_DM_1	AR38	M_B_DM1
SB_DM_2	AT36	M_B_DM2
SB_DM_3	BA31	M_B_DM3
SB_DM_4	AL17	M_B_DM4
SB_DM_5	AH9	M_B_DM5
SB_DM_6	BA5	M_B_DM6
SB_DM_7	AN4	M_B_DM7
SB_DQS_0	AM39	M_B_DQS0
SB_DQS_1	AT39	M_B_DQS1
SB_DQS_2	AU35	M_B_DQS2
SB_DQS_3	AR29	M_B_DQS3
SB_DQS_4	AR16	M_B_DQS4
SB_DQS_5	AR10	M_B_DQS5
SB_DQS_6	AR7	M_B_DQS6
SB_DQS_7	AN5	M_B_DQS7
SB_DQS#_0	AM40	M_B_DQS#0
SB_DQS#_1	AU39	M_B_DQS#1
SB_DQS#_2	AT35	M_B_DQS#2
SB_DQS#_3	AP29	M_B_DQS#3
SB_DQS#_4	AP16	M_B_DQS#4
SB_DQS#_5	AT10	M_B_DQS#5
SB_DQS#_6	AT7	M_B_DQS#6
SB_DQS#_7	AP5	M_B_DQS#7
SB_MA_0	AY23	M_B_A0
SB_MA_1	AW24	M_B_A1
SB_MA_2	AY24	M_B_A2
SB_MA_3	AR28	M_B_A3
SB_MA_4	AT27	M_B_A4
SB_MA_5	AT28	M_B_A5
SB_MA_6	AU27	M_B_A6
SB_MA_7	AV28	M_B_A7
SB_MA_8	AV27	M_B_A8
SB_MA_9	AW27	M_B_A9
SB_MA_10	AY24	M_B_A10
SB_MA_11	BA27	M_B_A11
SB_MA_12	AY27	M_B_A12
SB_MA_13	AR23	M_B_A13
SB_RAS#	AU23	M_B_RAS# 15,16
SB_RCVENIN#	AK18	
SB_RCVENOUT#	AK18	
SB_WE#	AR27	M_B_WE# 15,16

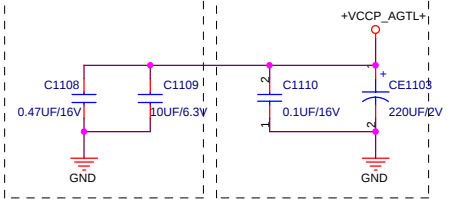
<Variant Name>



0.9475V~1.1025V
Max: 1.4A

PLACE IN CAVITY

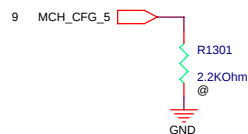
PLACE ON THE EDGE



POWER

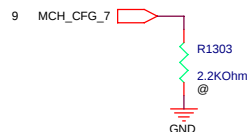
<Variant Name>

ASUS®		Title : Calistoga-POWER	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Monday, September 11, 2006		Sheet 11 of 63	



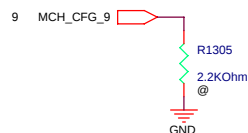
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



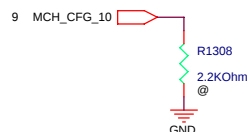
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



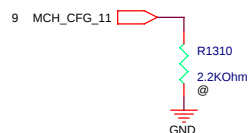
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
 HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

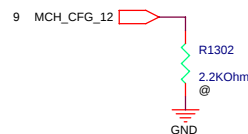
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

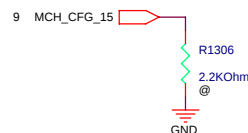
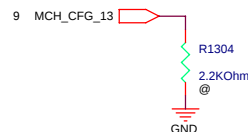
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.



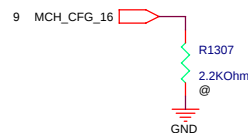
CFG[13:12] : GMCH TEST MODE SELECT

00 = Partial CLK gating disable
 01 = XOR Mode Enable
 10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)



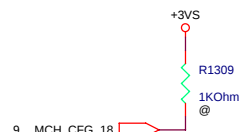
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



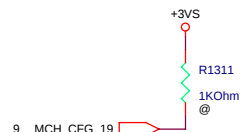
CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
 HIGH = 1.5V



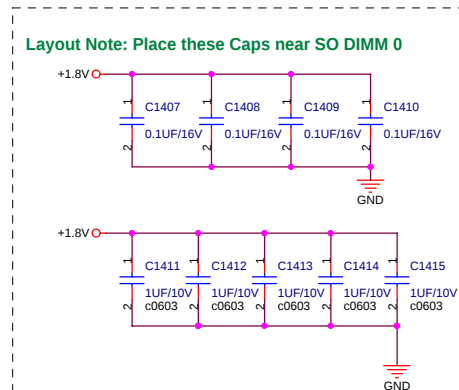
CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
 HIGH = LANES REVERSED

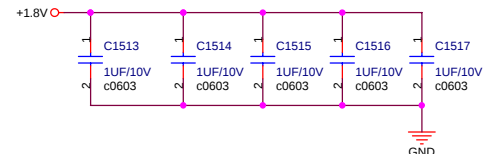
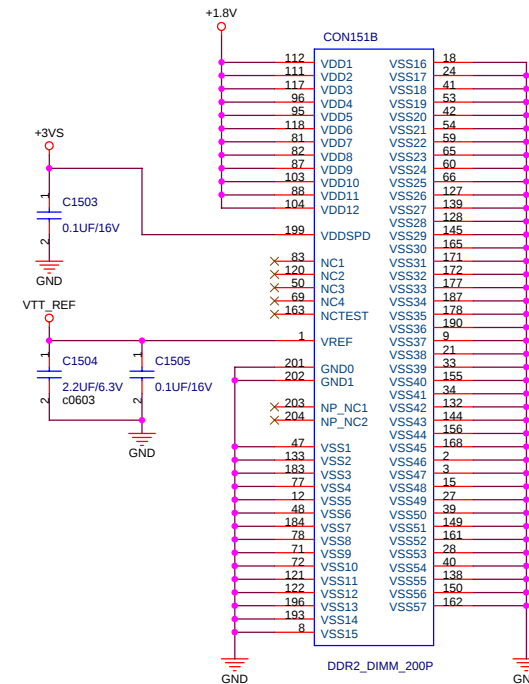
<Variant Name>

ASUS		Title : Calistoga-Strap	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F	Rev 1.10	
Date: Monday, September 11, 2006	Sheet 13	of 63	

SMBus Slave Address:A0H

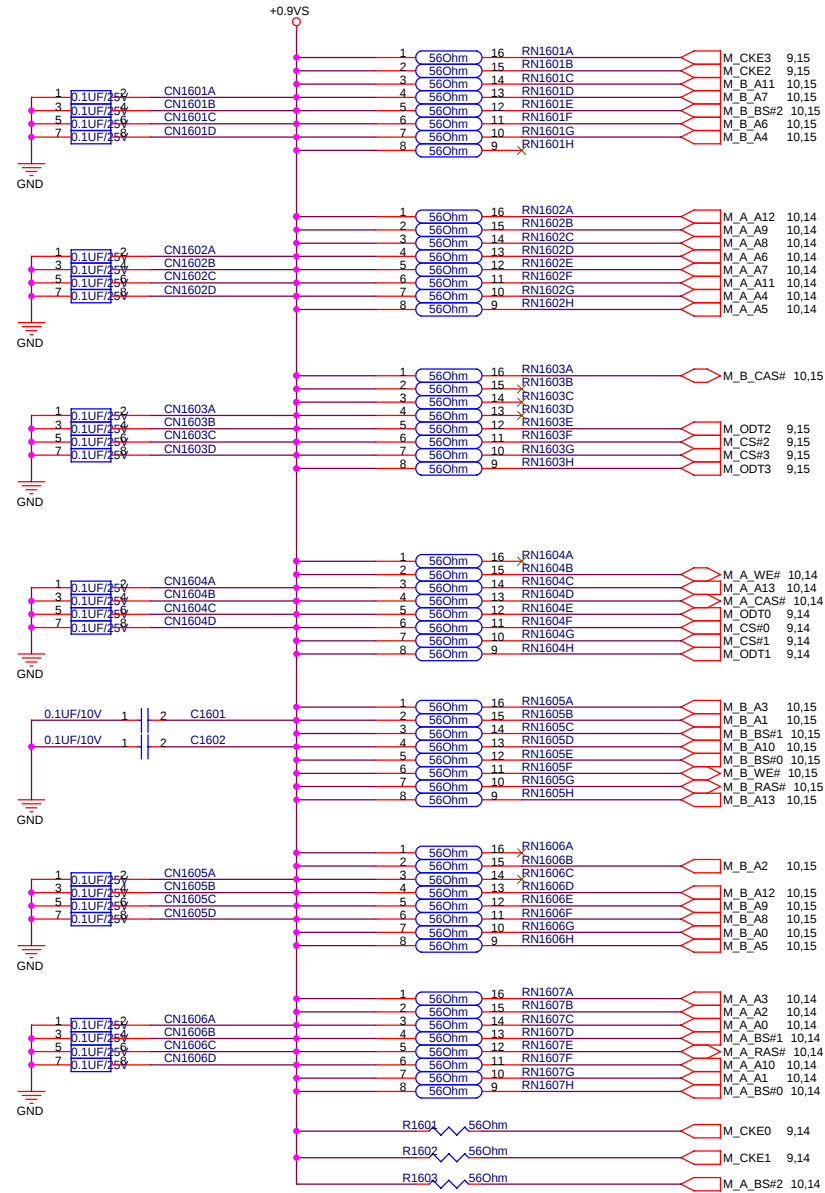


SMBus Slave Address:A4H



		Title : <u>DDR2 SO-DIMM 1</u>	
ASUSTeK COMPUTER INC		Engineer: <u>Marco Chen</u>	
Size Custom	Project Name T13F	Rev <u>1.10</u>	
Date: <u>Monday, September 11, 2006</u>		Sheet <u>15</u>	of <u>63</u>

DDR2 HAD SWAPED.

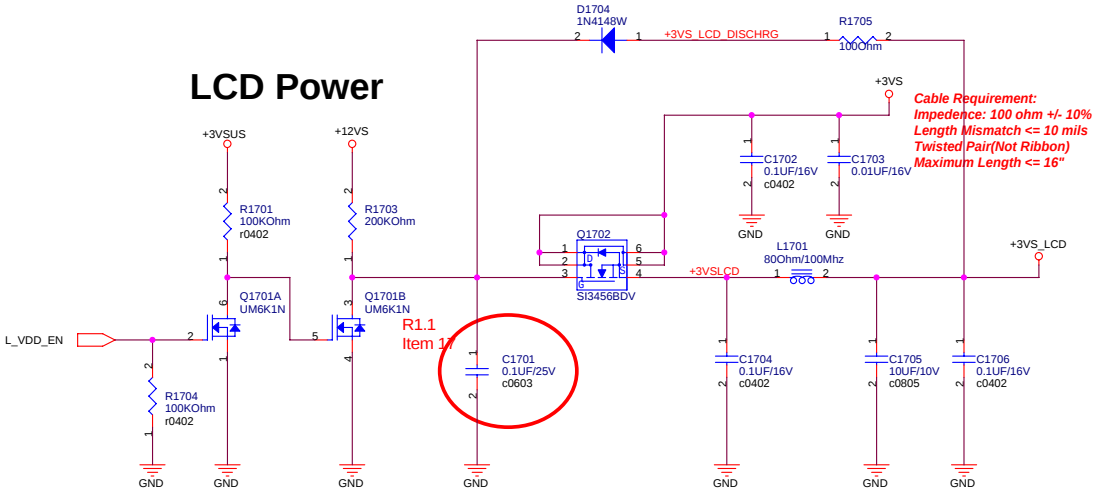


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

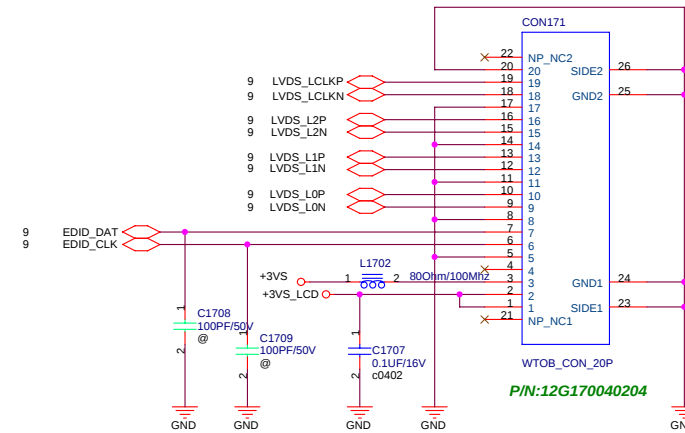
LCD Backlight Control

LCD Power

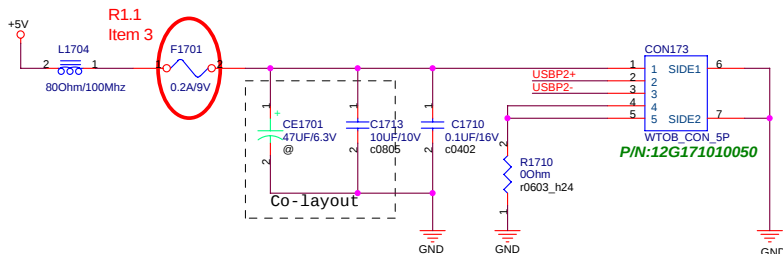


PR_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

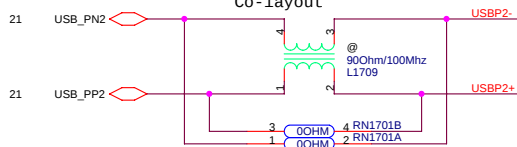
LCD LVDS Interface



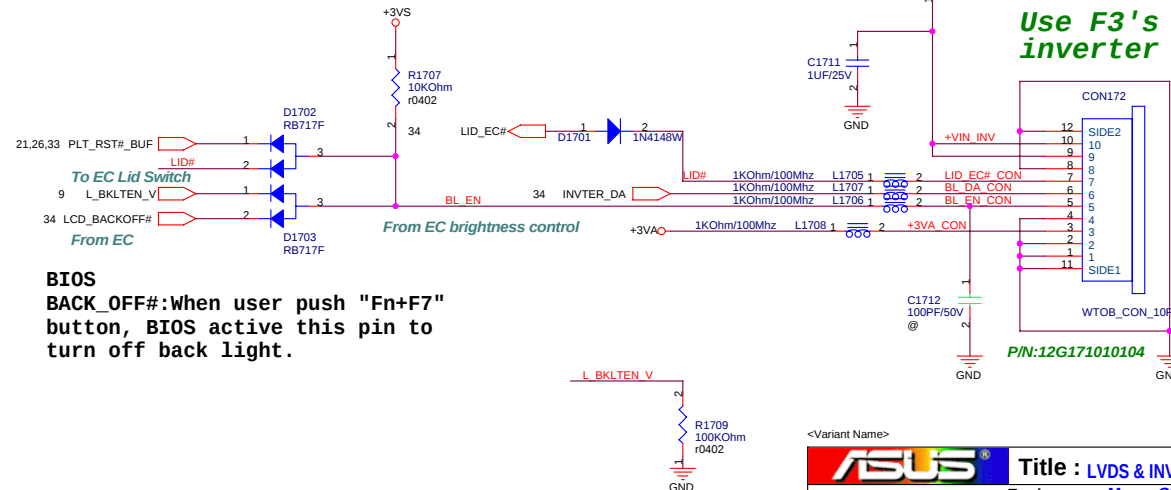
CCD connector



FOR EMI
Co-layout



Inverter connector



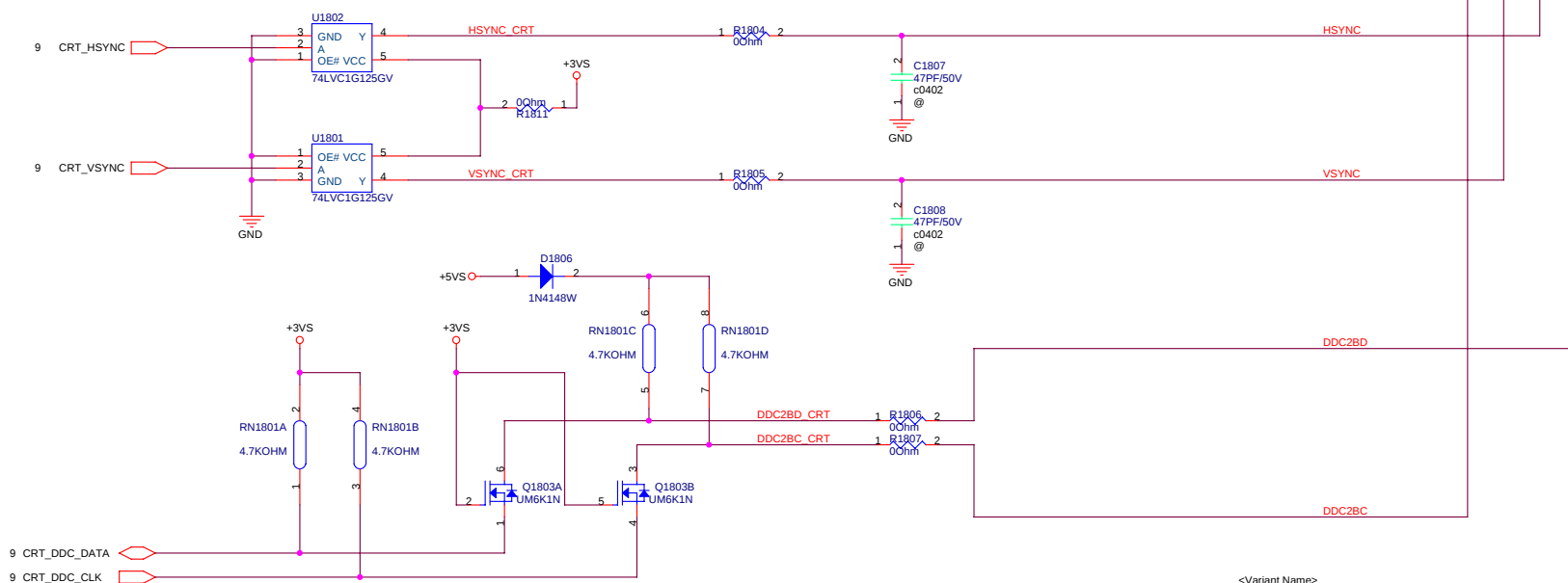
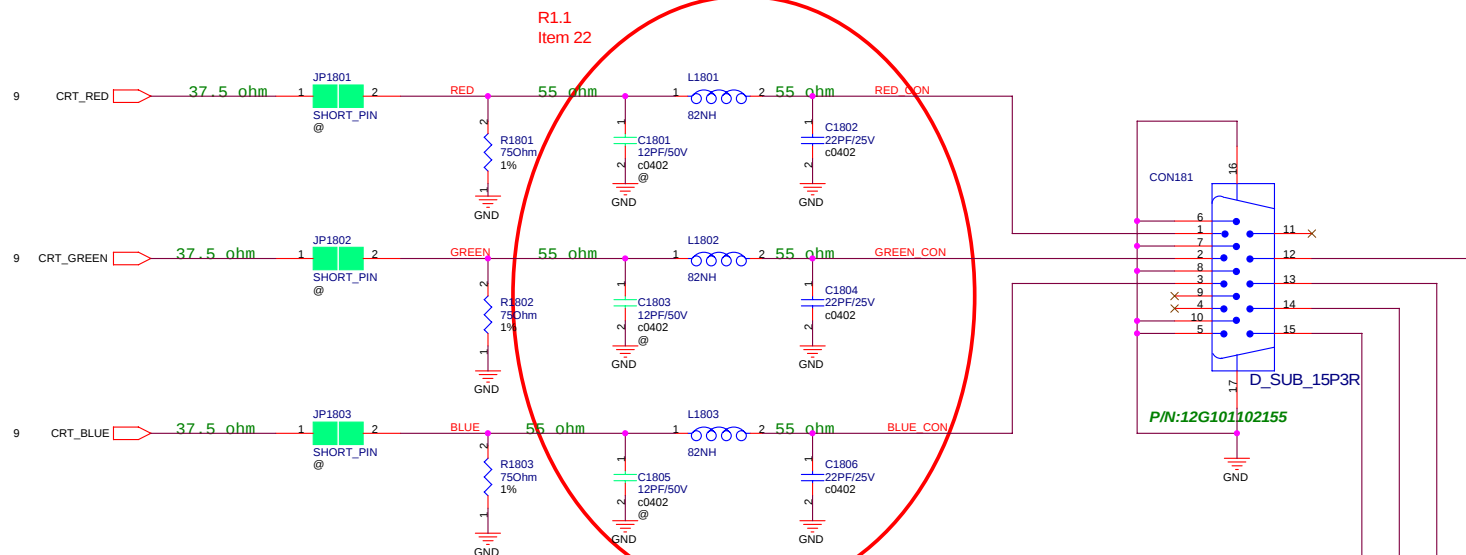
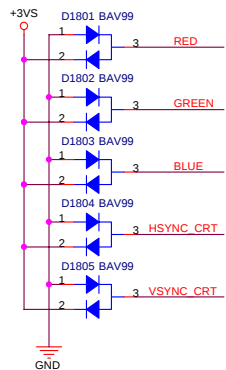
BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

<Variant Name>

		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: <i>Marco Chen</i>	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006		Sheet 17 of 63	

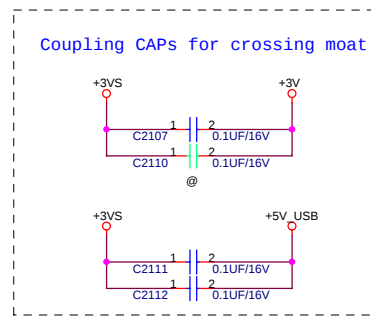
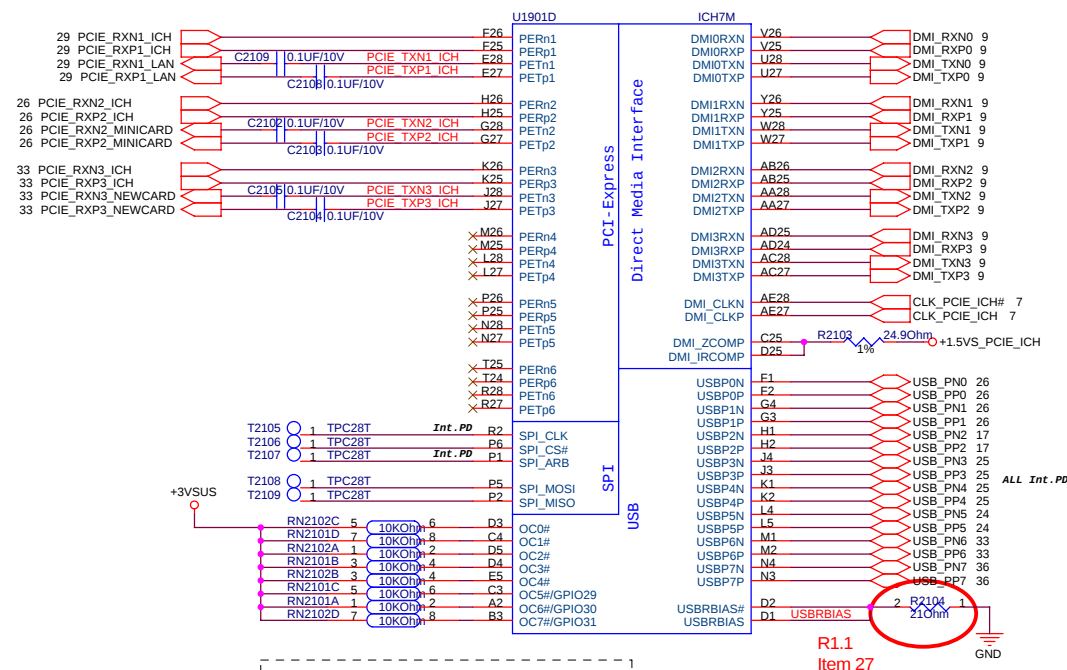
CRT

PLACE NEAR CON181.

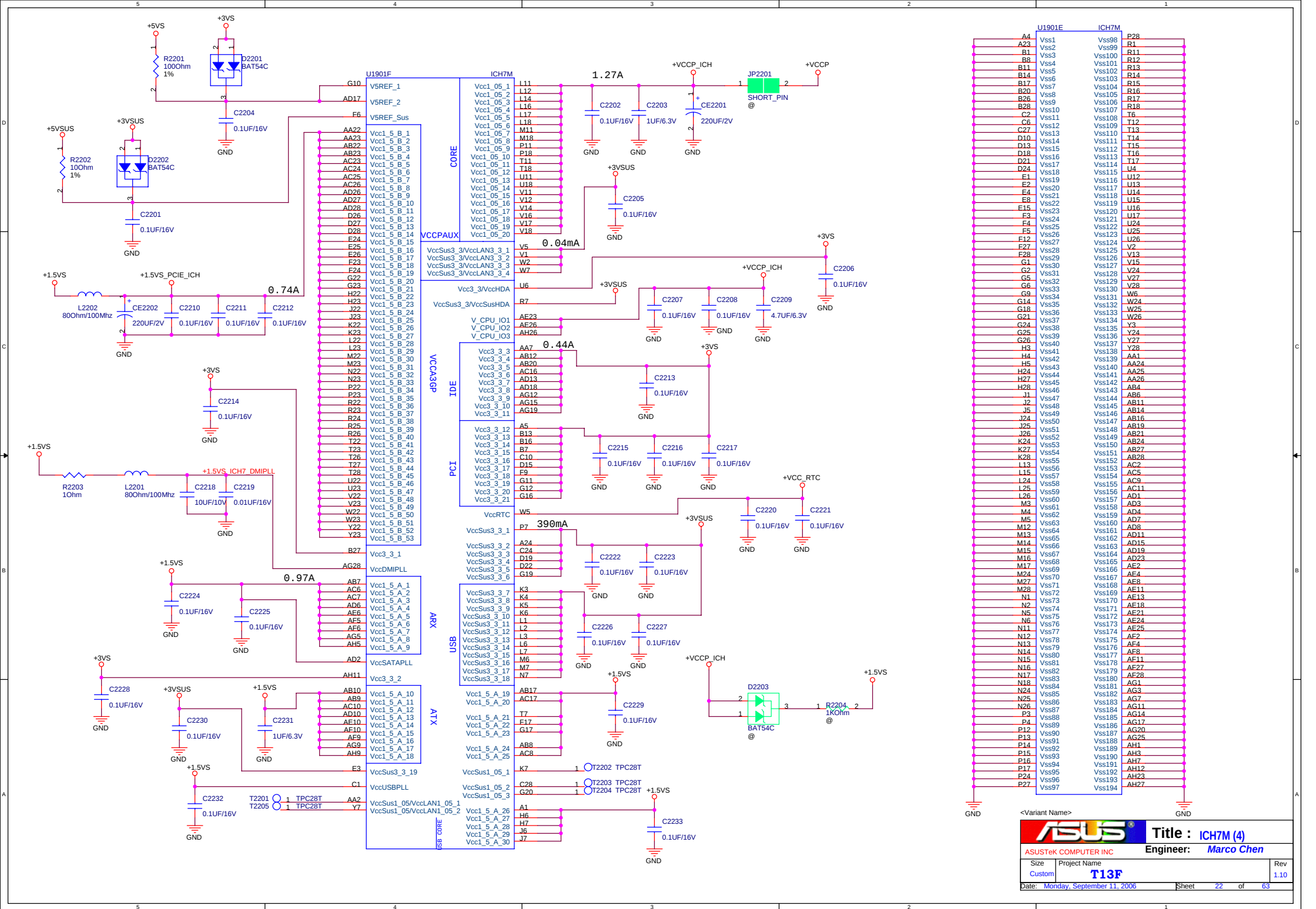


<Variant Name>

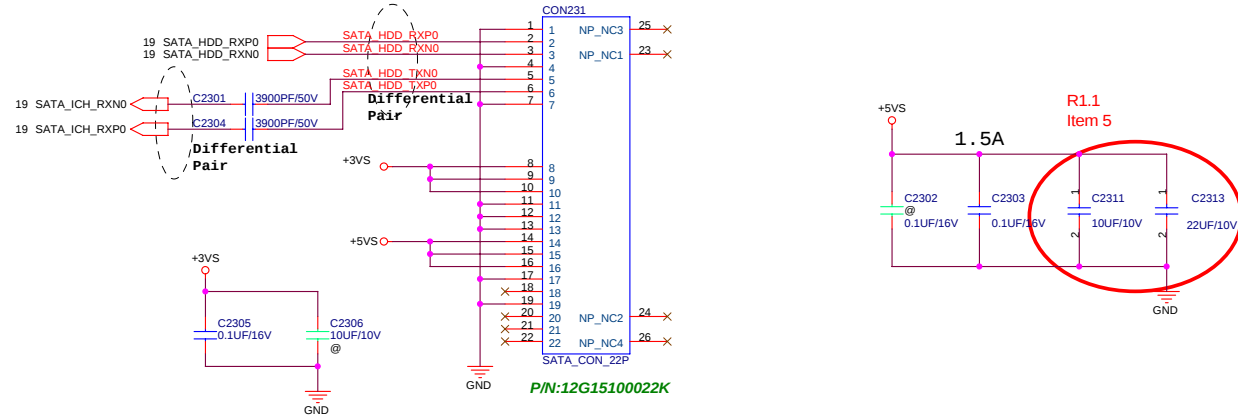
ASUS		Title : CRT CONN	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Monday, September 11, 2006		Sheet 18 of 63	



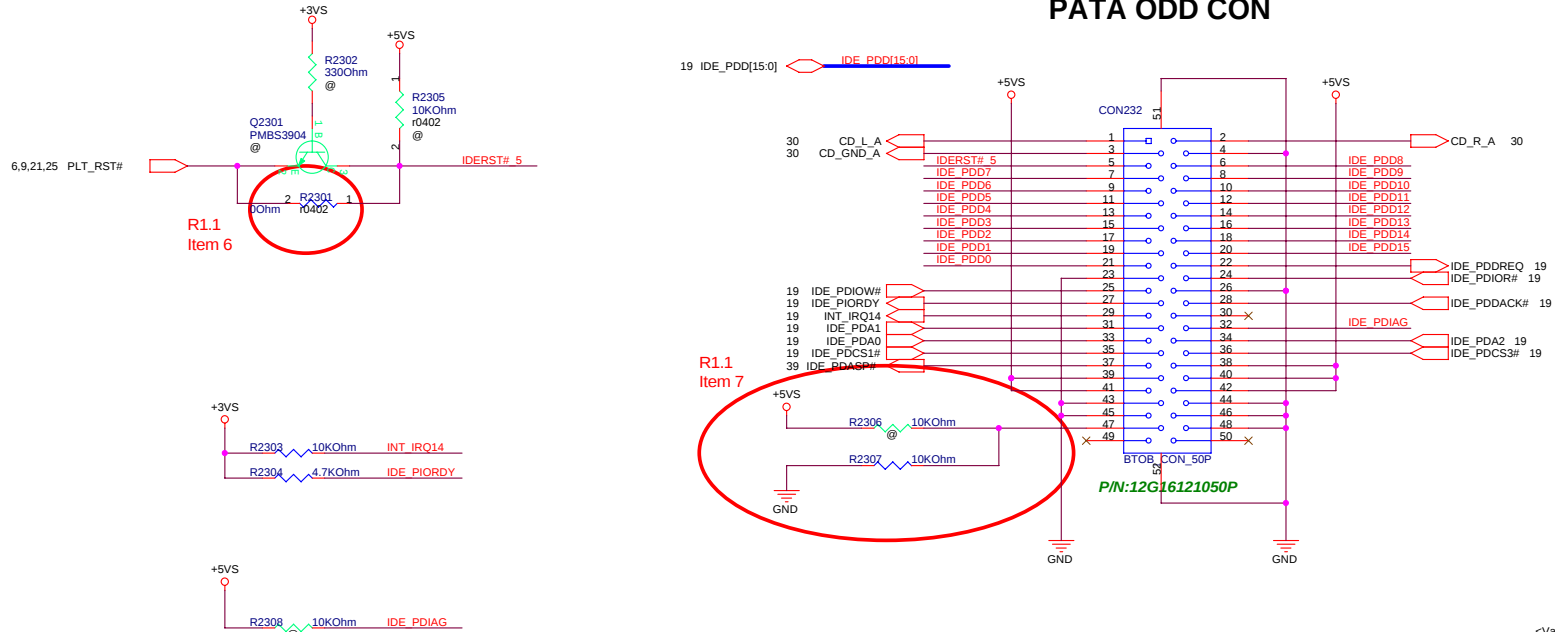
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Camera
USB 3	Finger Print
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	NEWCARD
USB 7	CARDREADER



SATA HDD CON



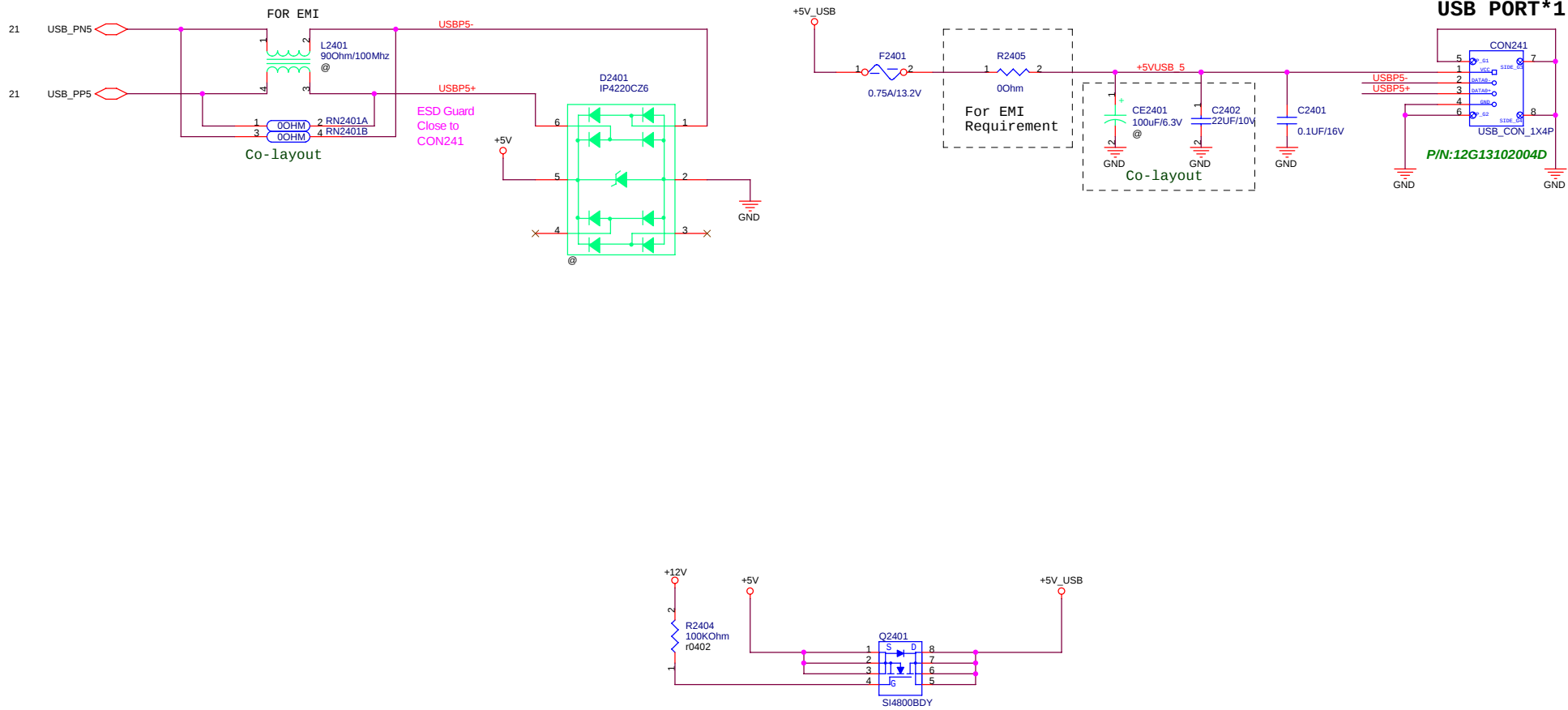
PATA ODD CON



Normal type
High: Slave
Low: Master

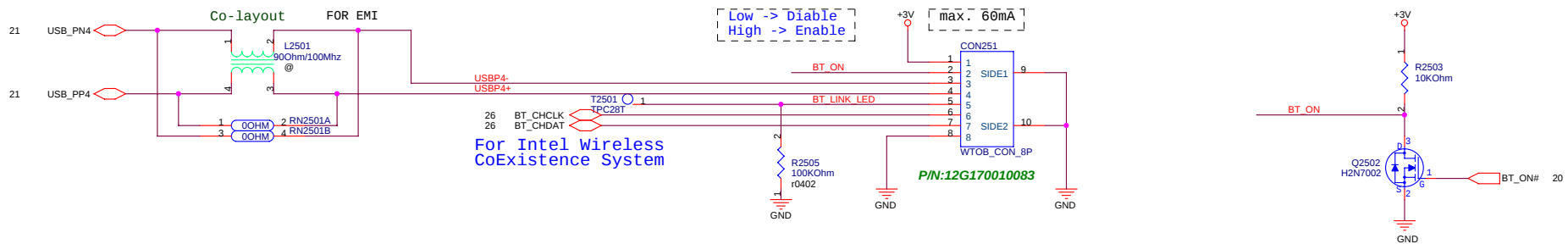
<Variant Name>

		Title : HDD & ODD	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006		Sheet 23 of 63	



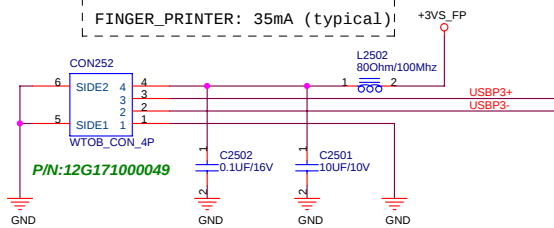
<Variant Name>

		Title : USB PORT	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006	Sheet	24 of 63	

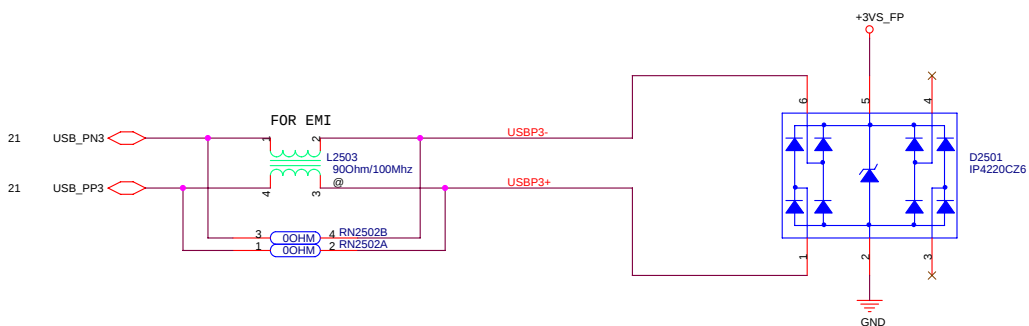


Finger Printer

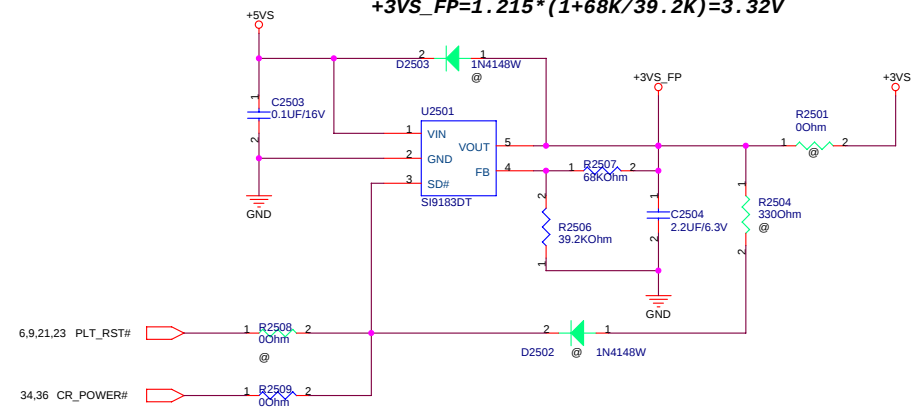
FINGER_PRINTER: 35mA (typical)



FOR EMI



$$+3VS_FP = 1.215 * (1 + 68K / 39.2K) = 3.32V$$



<Variant Name>

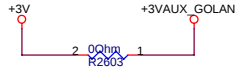
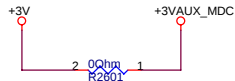
ASUS		Title : BT & FP	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Monday, September 11, 2006		Sheet	25 of 63

POWER CONSUMPTION:
+3VS: +3.003V~+3.597V
Max= 750 mA

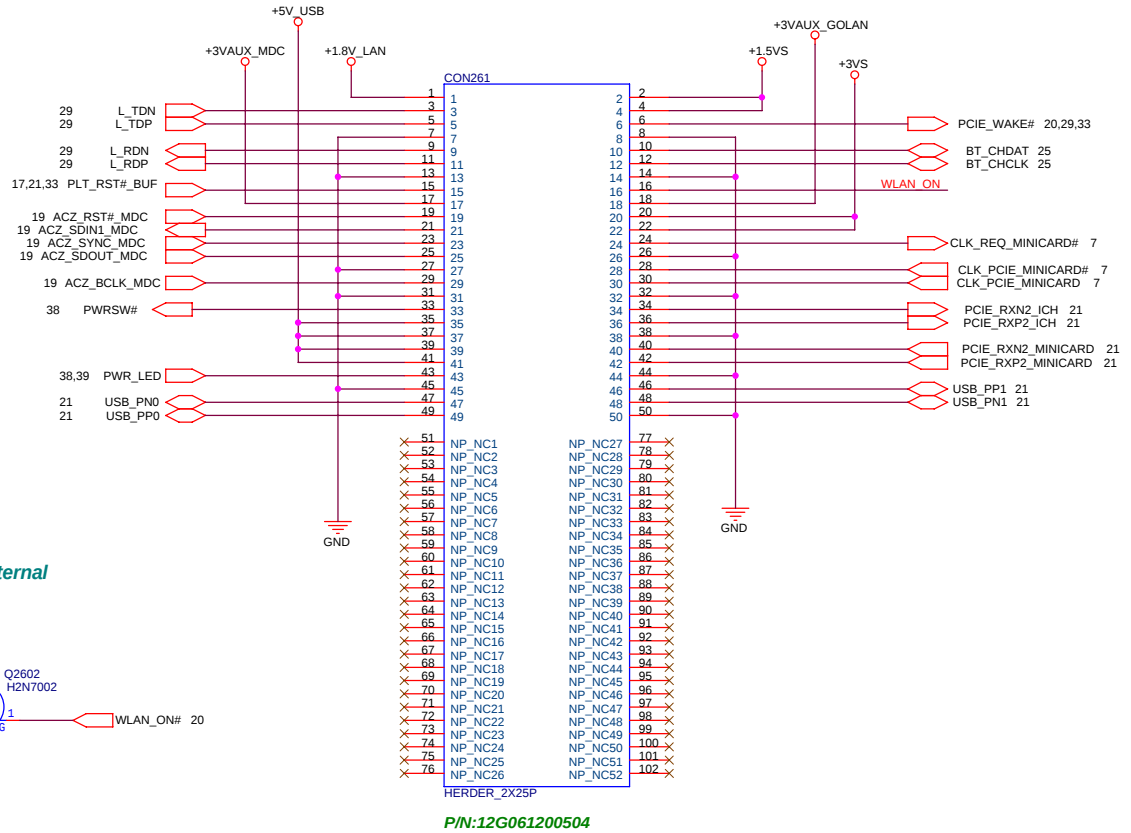
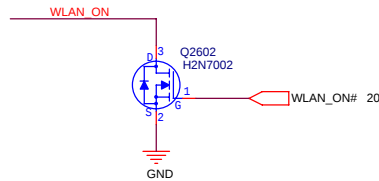
+1.5VS: +1.425V~+1.575V
Max= 375 mA

+3VAUX_GOLAN: +3.003V~+3.597V
Max= 250 mA

+3VAUX_MDC: +3.003V~+3.597V
Max= 300 mA

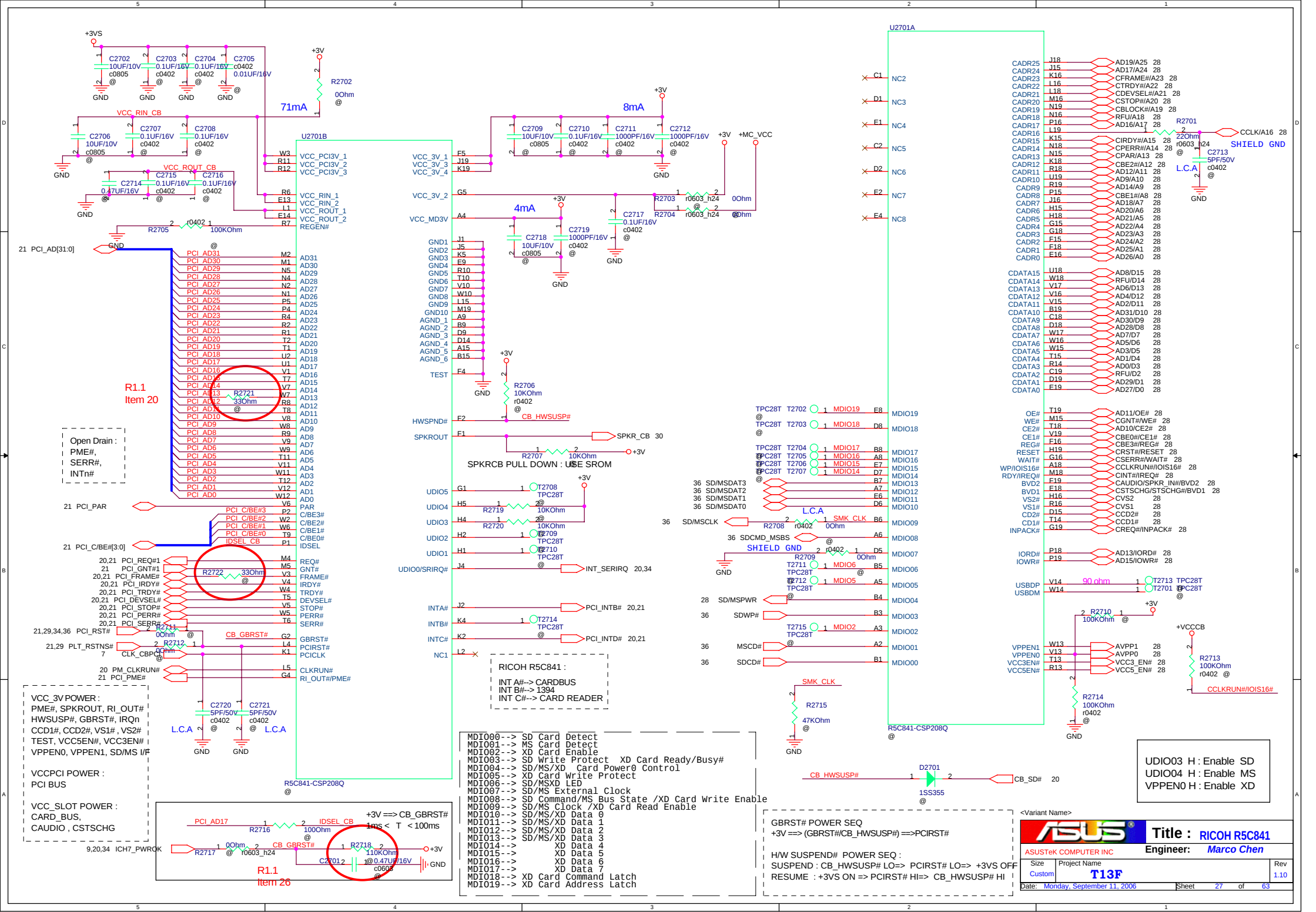


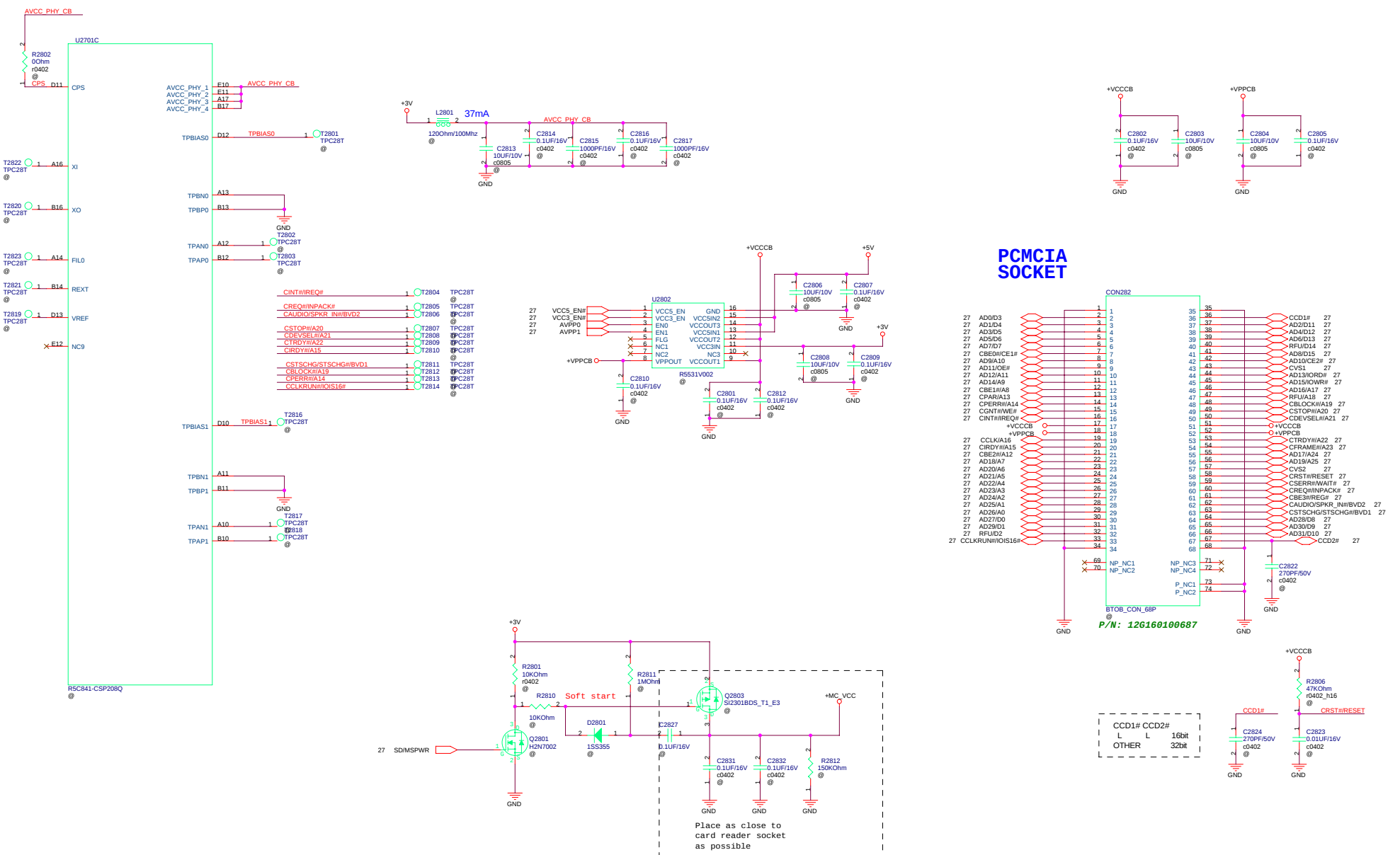
**Intel SPEC(18780):Internal
Pull UP 110Kohm**

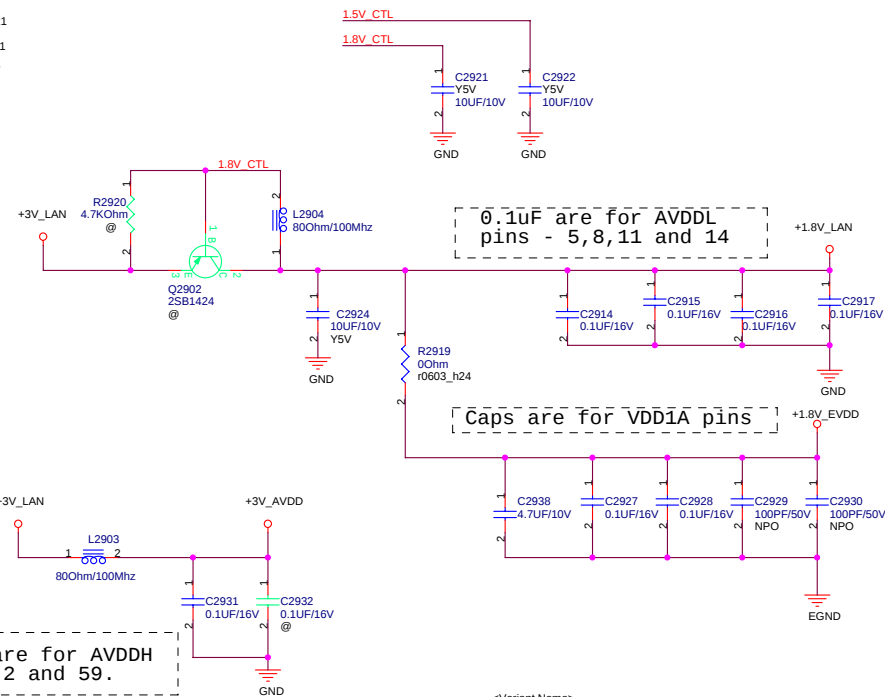
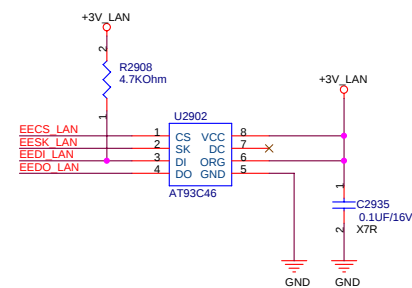
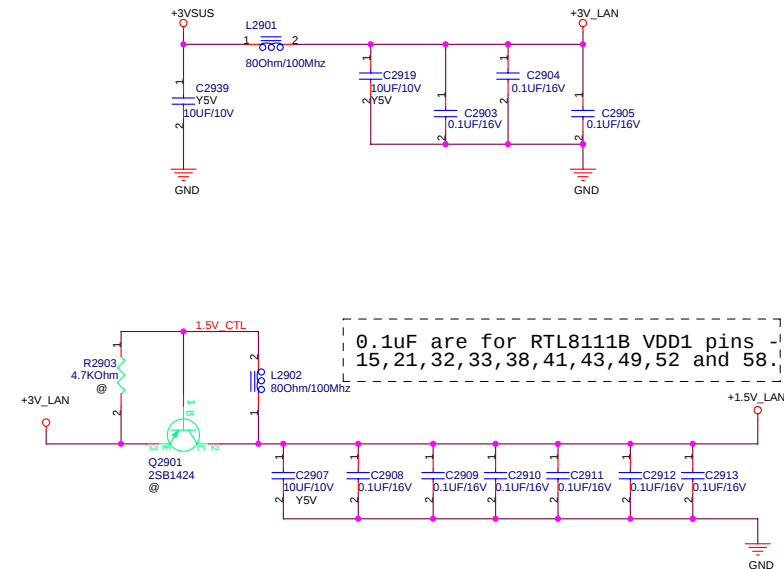


<Variant Name>

ASUS ASUSTeK COMPUTER INC		Title : B TO B CONN(M) Engineer: Marco Chen	
Size Custom	Project Name T13F	Rev 1.10	
Date: Monday, September 11, 2006		Sheet 26 of 63	

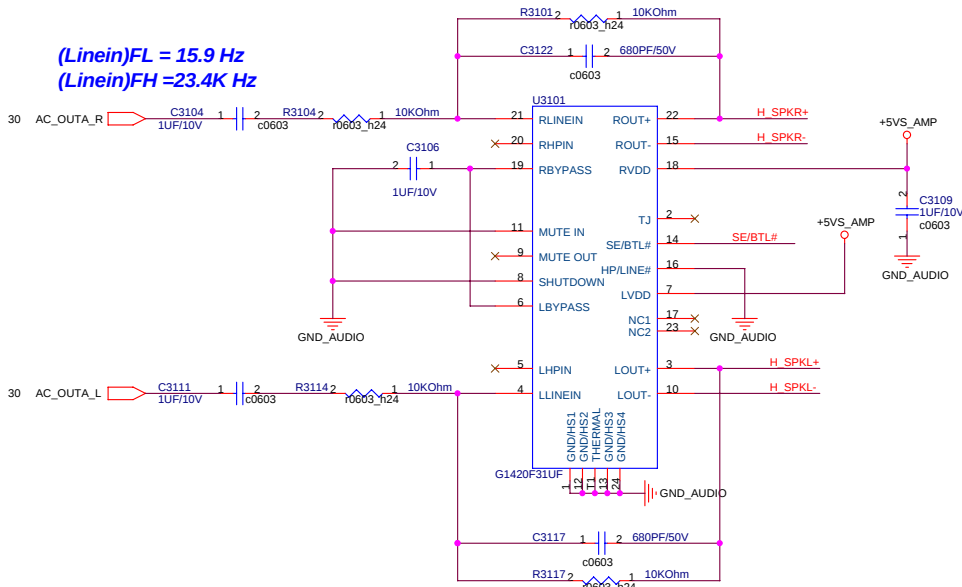




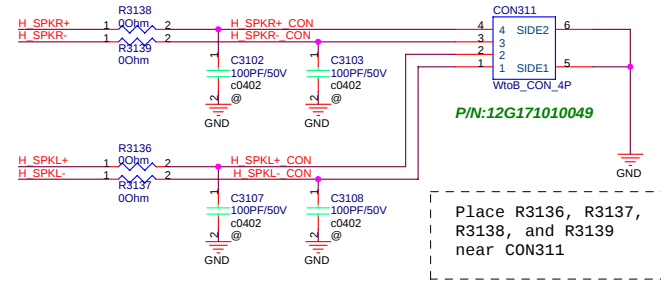
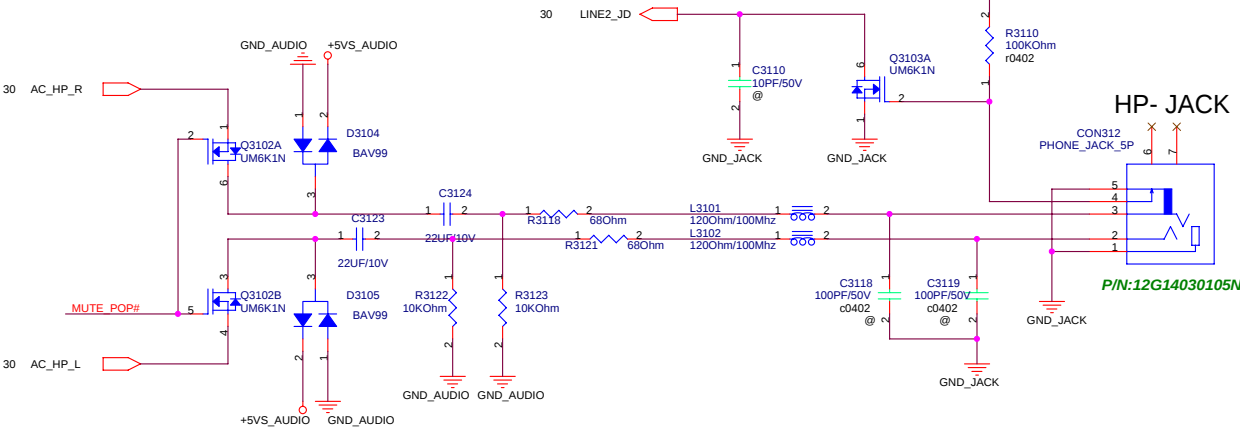
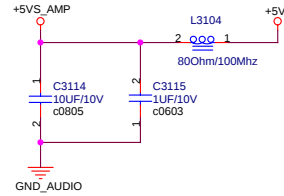
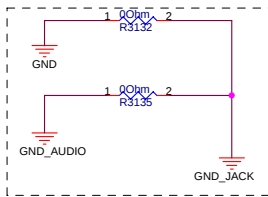


		Title : LAN RTL8101E	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006		Sheet 29	of 63

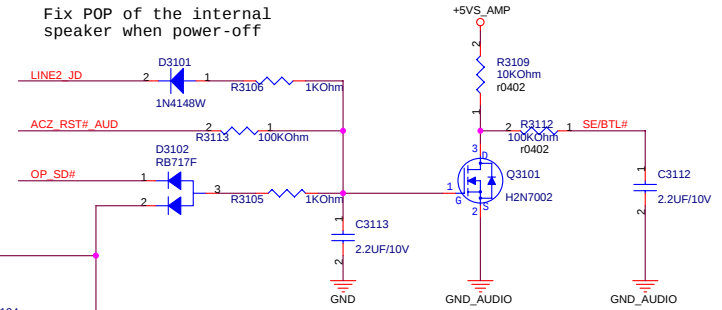
(Linein)FL = 15.9 Hz
(Linein)FH = 23.4K Hz



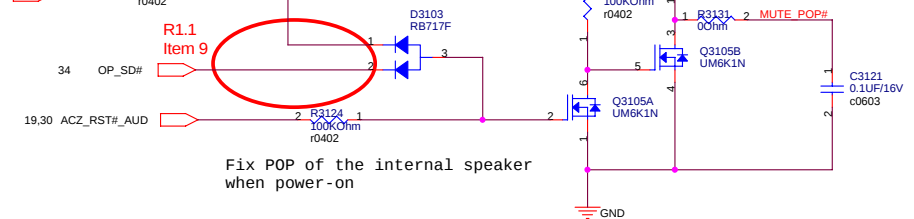
EMI Request



Fix POP of the internal speaker when power-off

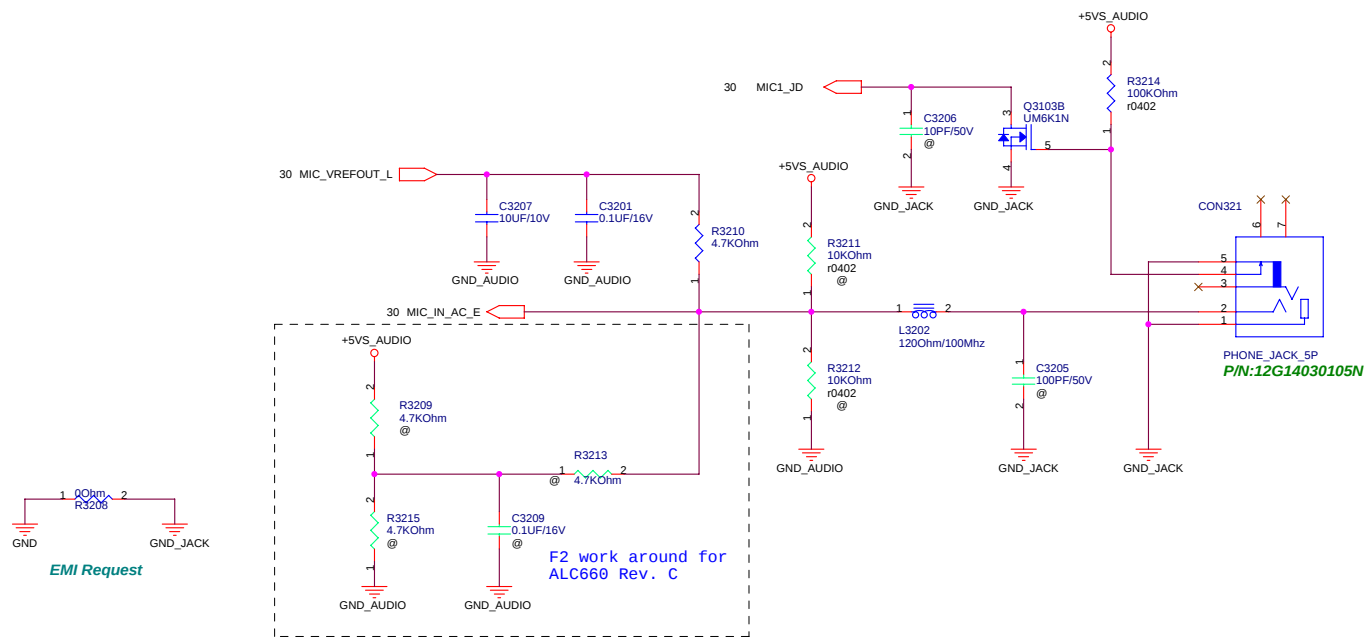
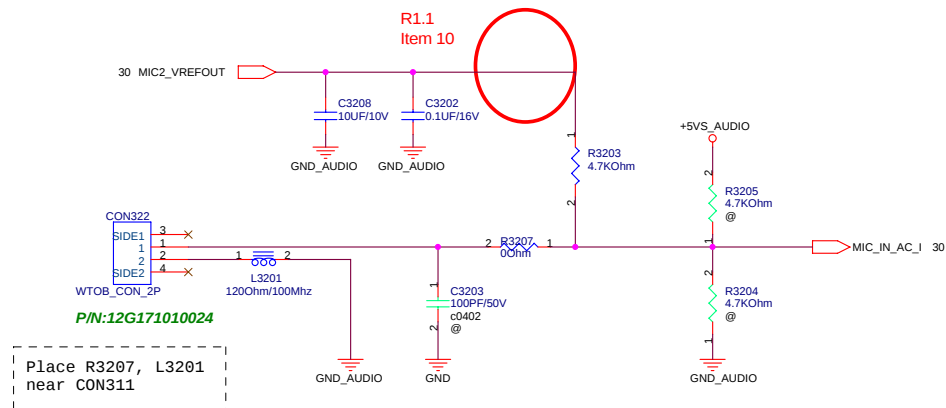


Fix POP of the internal speaker when power-on



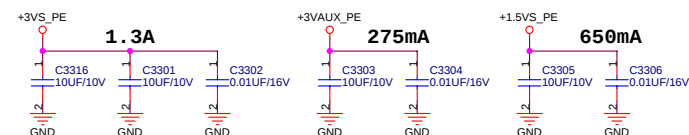
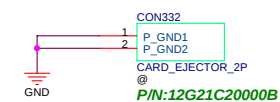
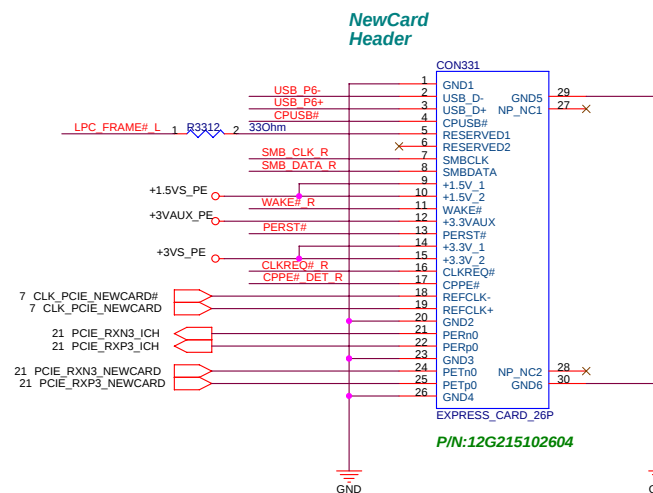
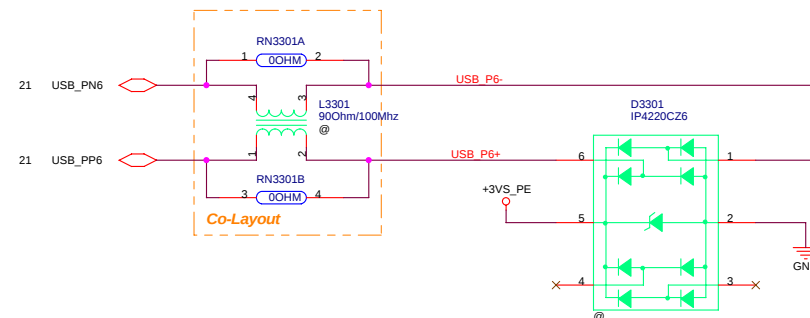
<Variant Name>

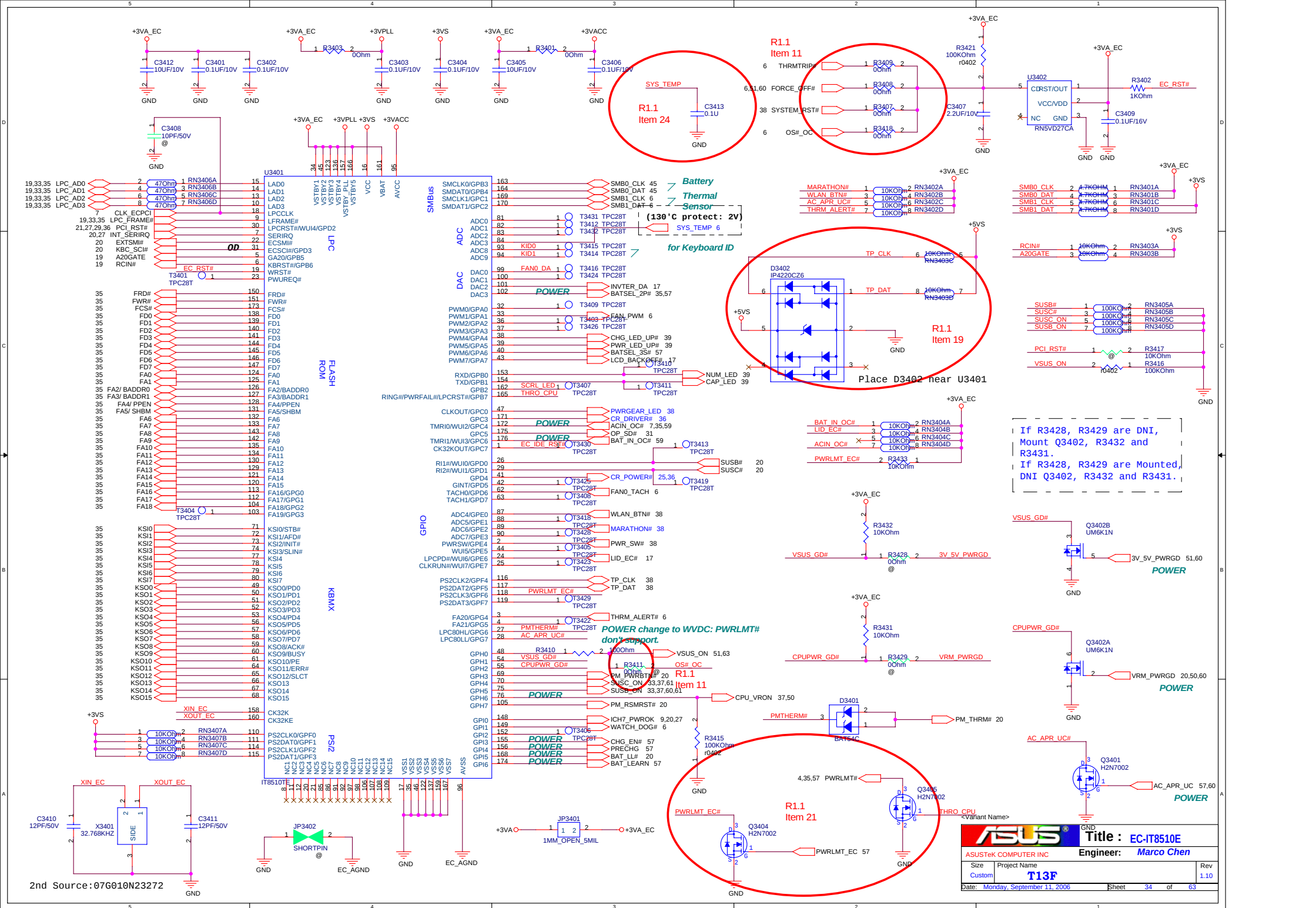
		Title : G1420	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F		Rev 1.10
Date: Monday, September 11, 2006		Sheet 31	of 63



<Variant Name>

		Title : MICROPHONE	
ASUSTek COMPUTER INC		Engineer: <i>Marco Chen</i>	
Size Custom	Project Name T13F	Date: Monday, September 11, 2006	Sheet 32 of 63
		Rev 1.10	

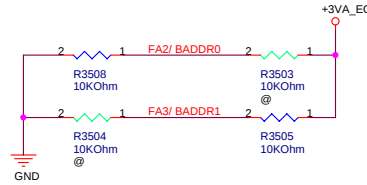




EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
 10: PNPCNG Access Register Pair Are 004Eh and 004Fh
 01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
 11: Reserved



Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

- 0: Normal

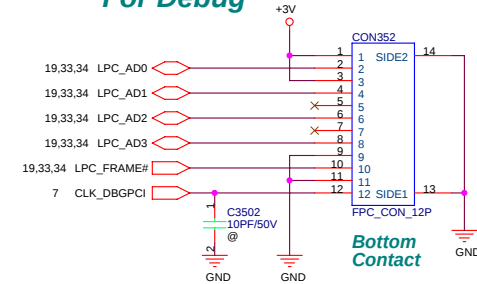
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS

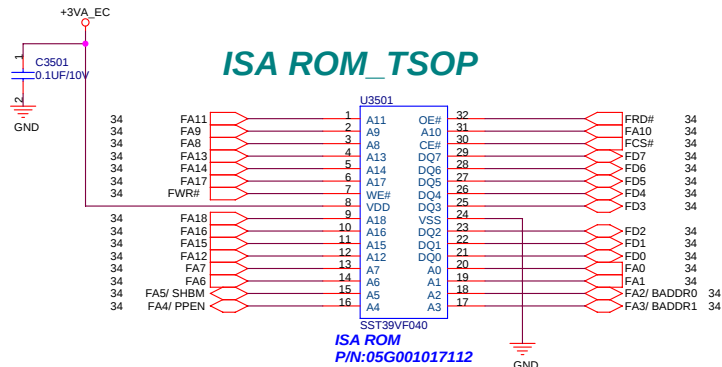
1: Enable Shared Memory with Host BIOS

For Debug

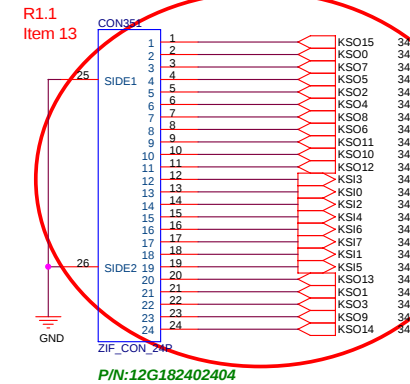


P/N:12G183301208

ISA ROM_TSOP

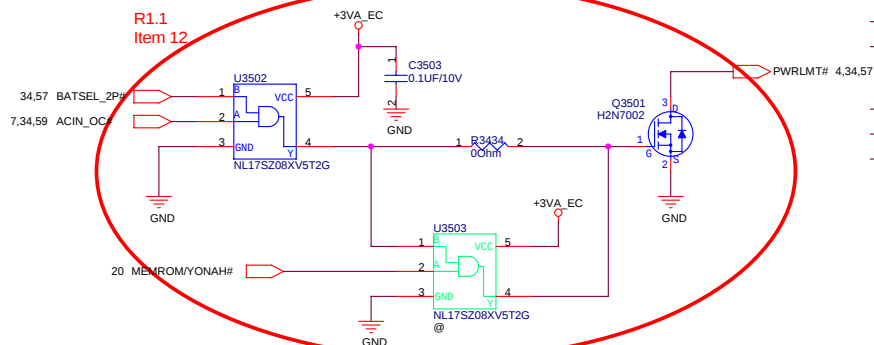


For Keyboard



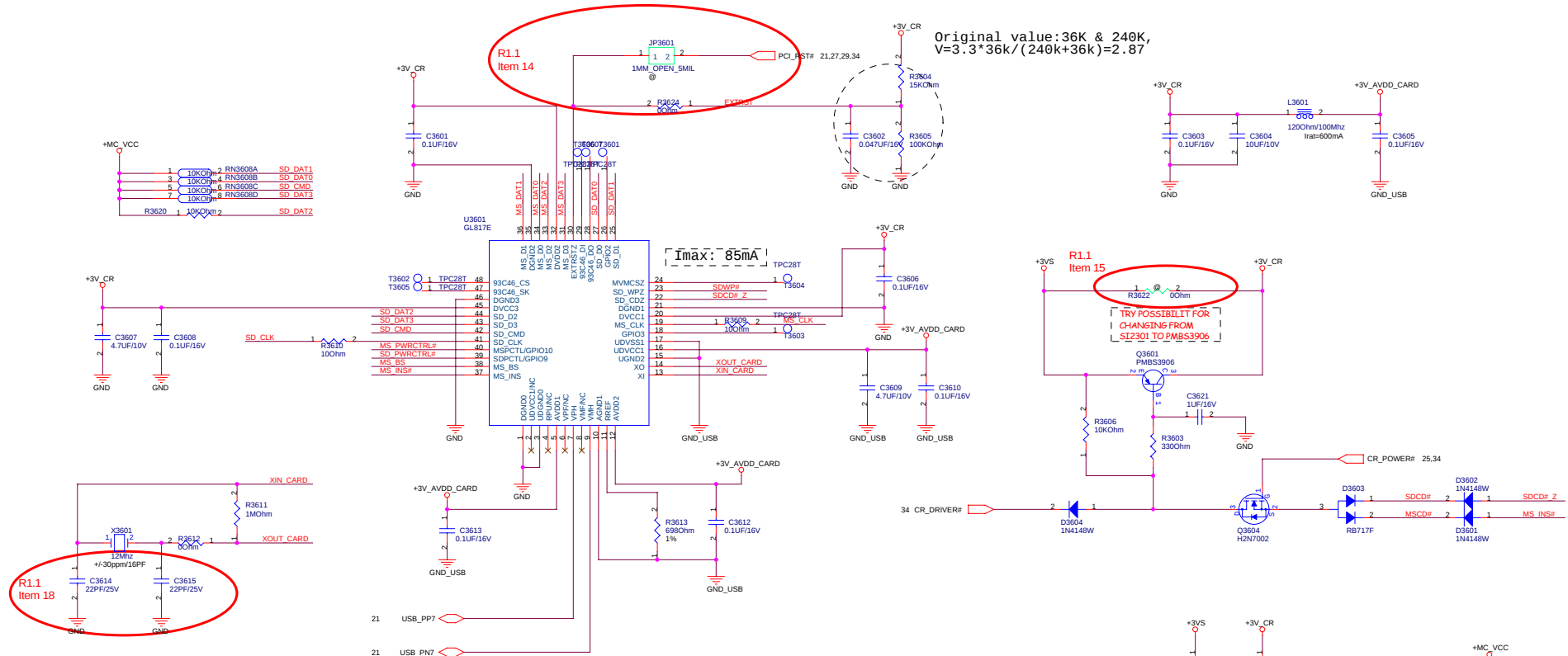
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R1.1
Item 12

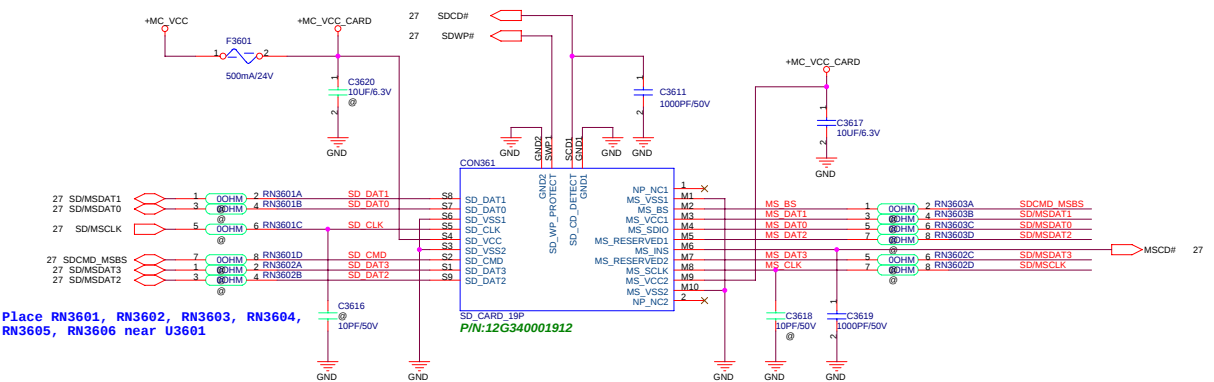


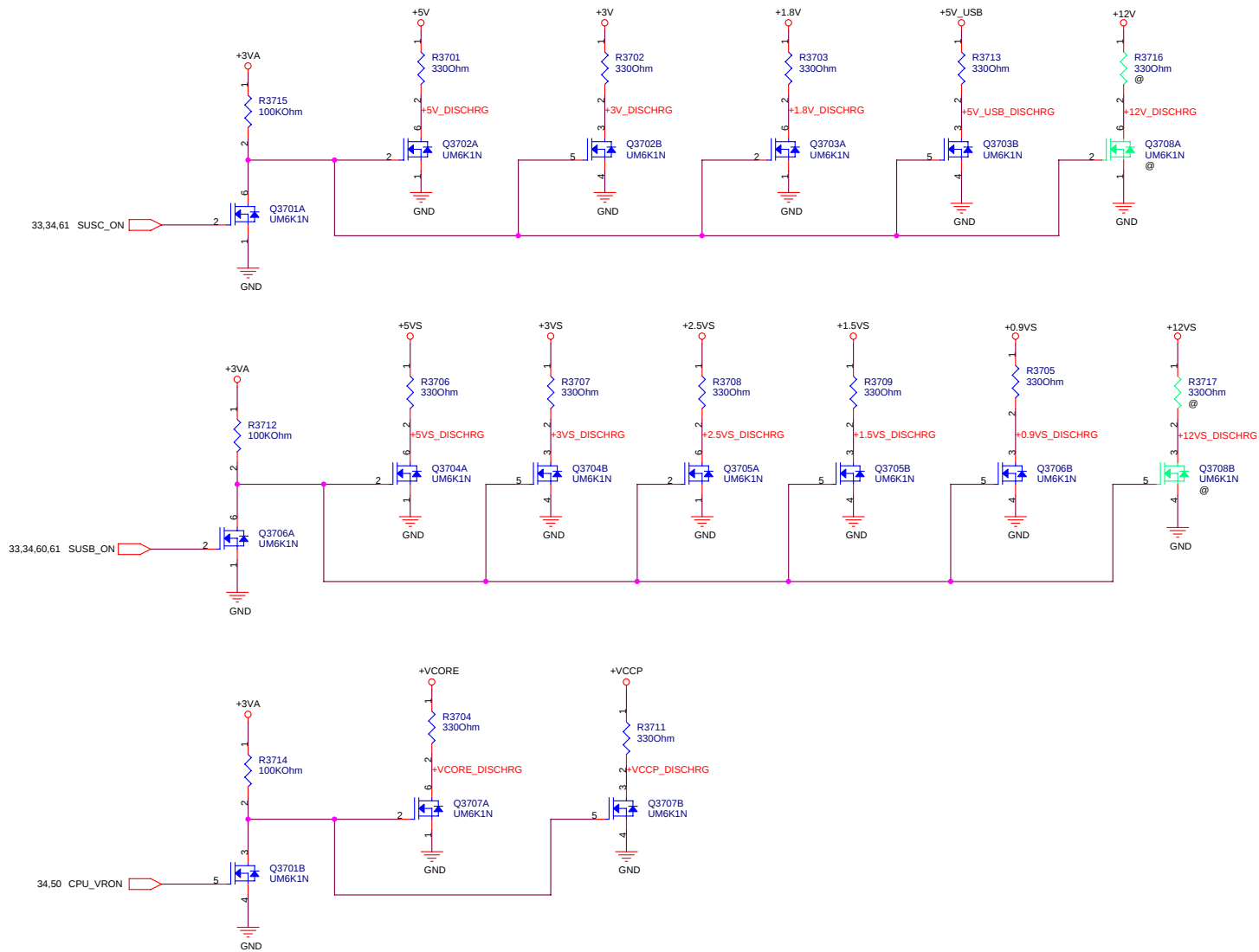
<Variant Name>

ASUS		Title :ISA_ROM&KB conn	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Monday, September 11, 2006		Sheet 35 of 63	



DNI RN3601, RN3602, RN3603 BY USING GL817E.

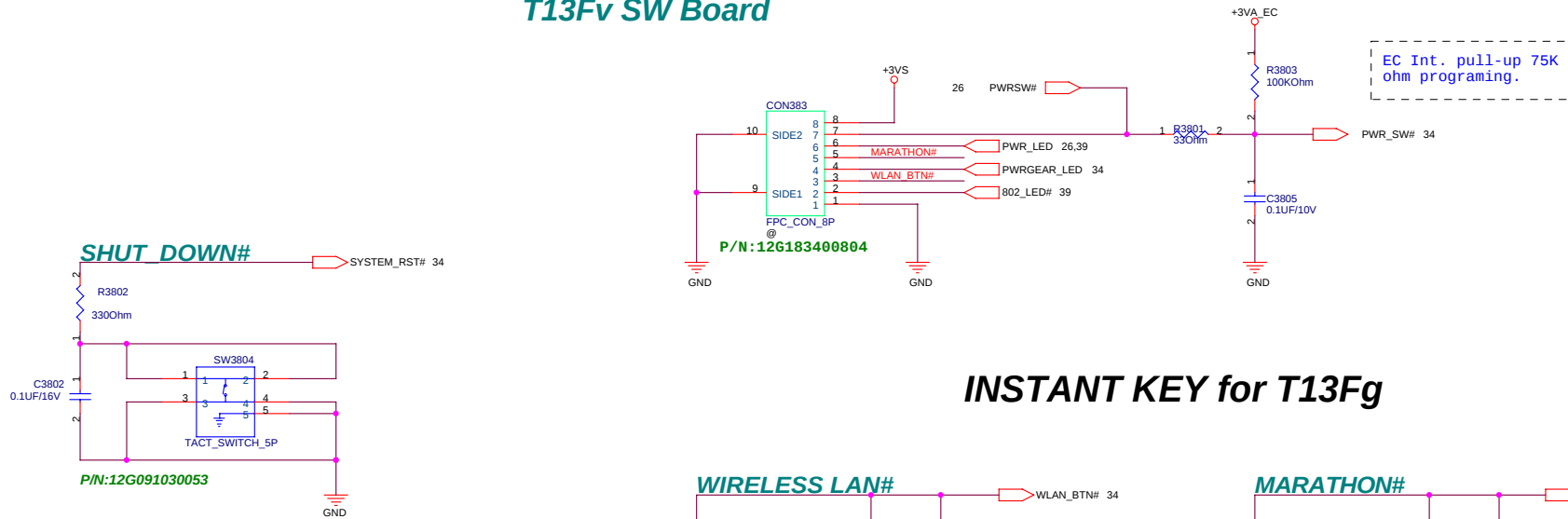




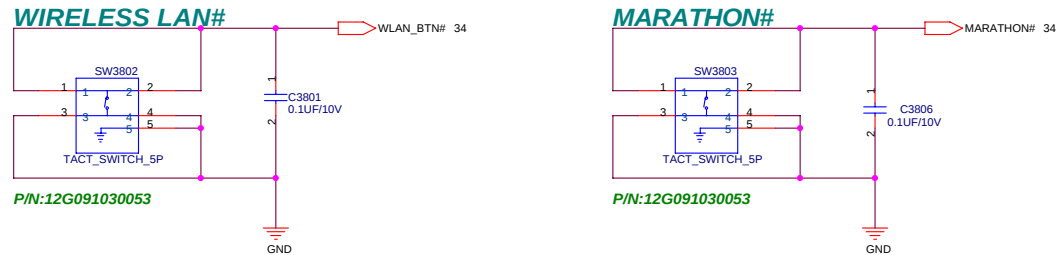
<Variant Name>

ASUS		Title : DISCHARGE	
ASUSTeK COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	T13F	Rev
Custom			1.10
Date: Monday, September 11, 2006		Sheet 37 of 63	

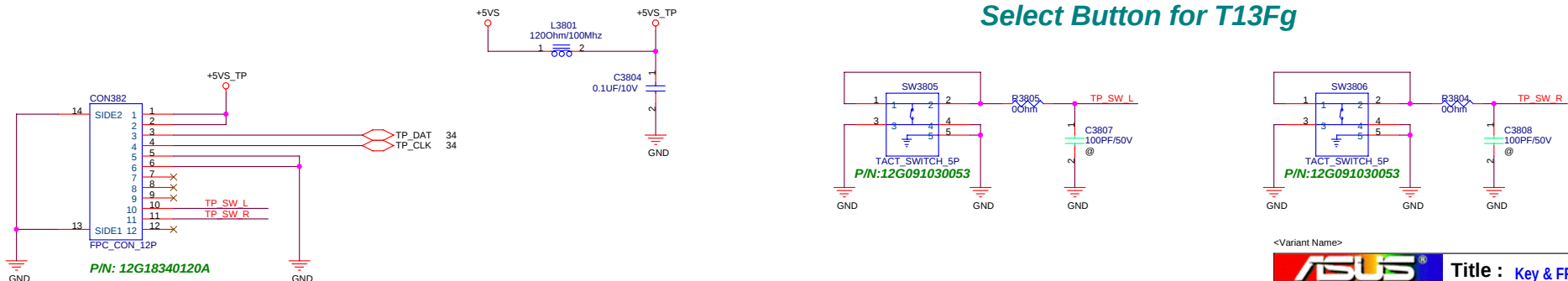
FFC CONNECTER for T13Fv SW Board



INSTANT KEY for T13Fg



Select Button for T13Fg

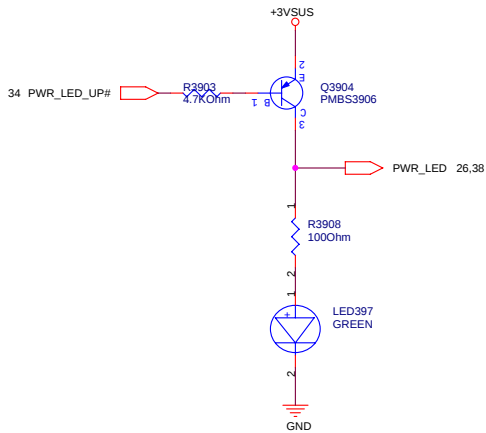


<Variant Name>

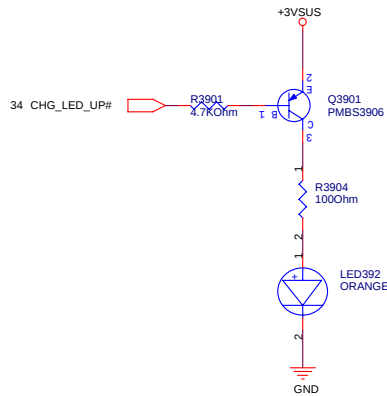
ASUS		Title : Key & FFC CONN	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size	Project Name	Rev	
Custom	T13F	1.10	
Date: Monday, September 11, 2006		Sheet 38 of 63	

```
PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.
```

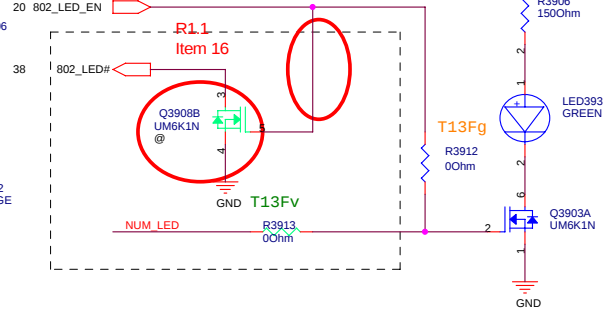
For POWER LED



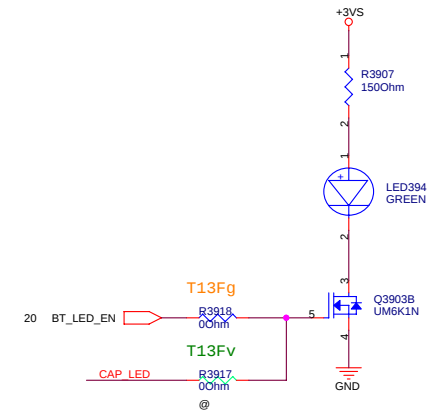
For BATTERY LED



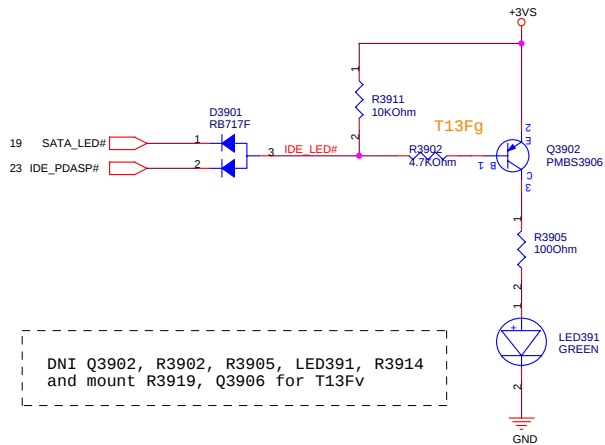
For WireLess LED



For BT LED

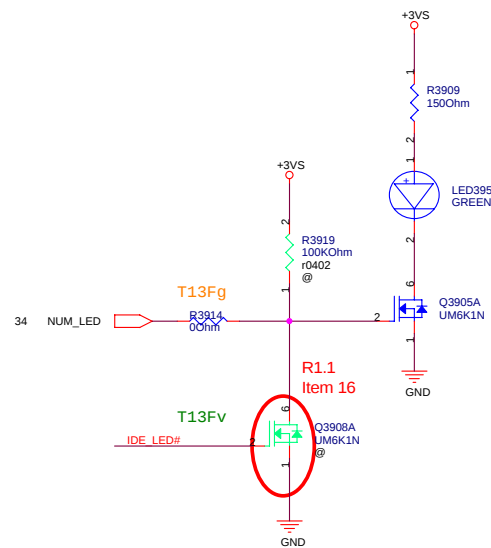


For SATA/IDE LED

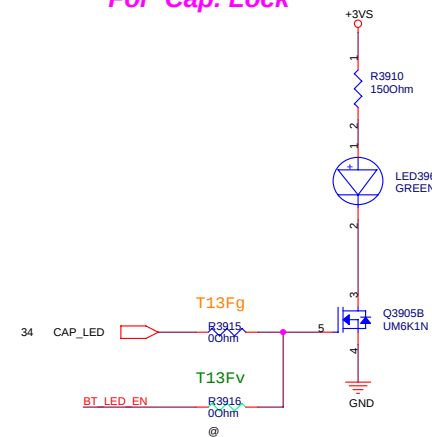


DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3906 for T13Fv

For Num Lock



For Cap. Lock



<Variant Name>



Title : LEDs

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size
Custom

Project Name	T13F
--------------	-------------

T13F

Rev	
1.10	

Date: Monday, September 11, 2006

Sheet 39 of 63

D

3

C

6

B

3

A

A

<Variant Name>



Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size
Custom

Project Name	T13F
--------------	-------------

Rev	
1.10	

Date: Monday, September 11, 2006

Sheet 40 of 63

D

3

C

6

B

3

A

A

<Variant Name>



Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

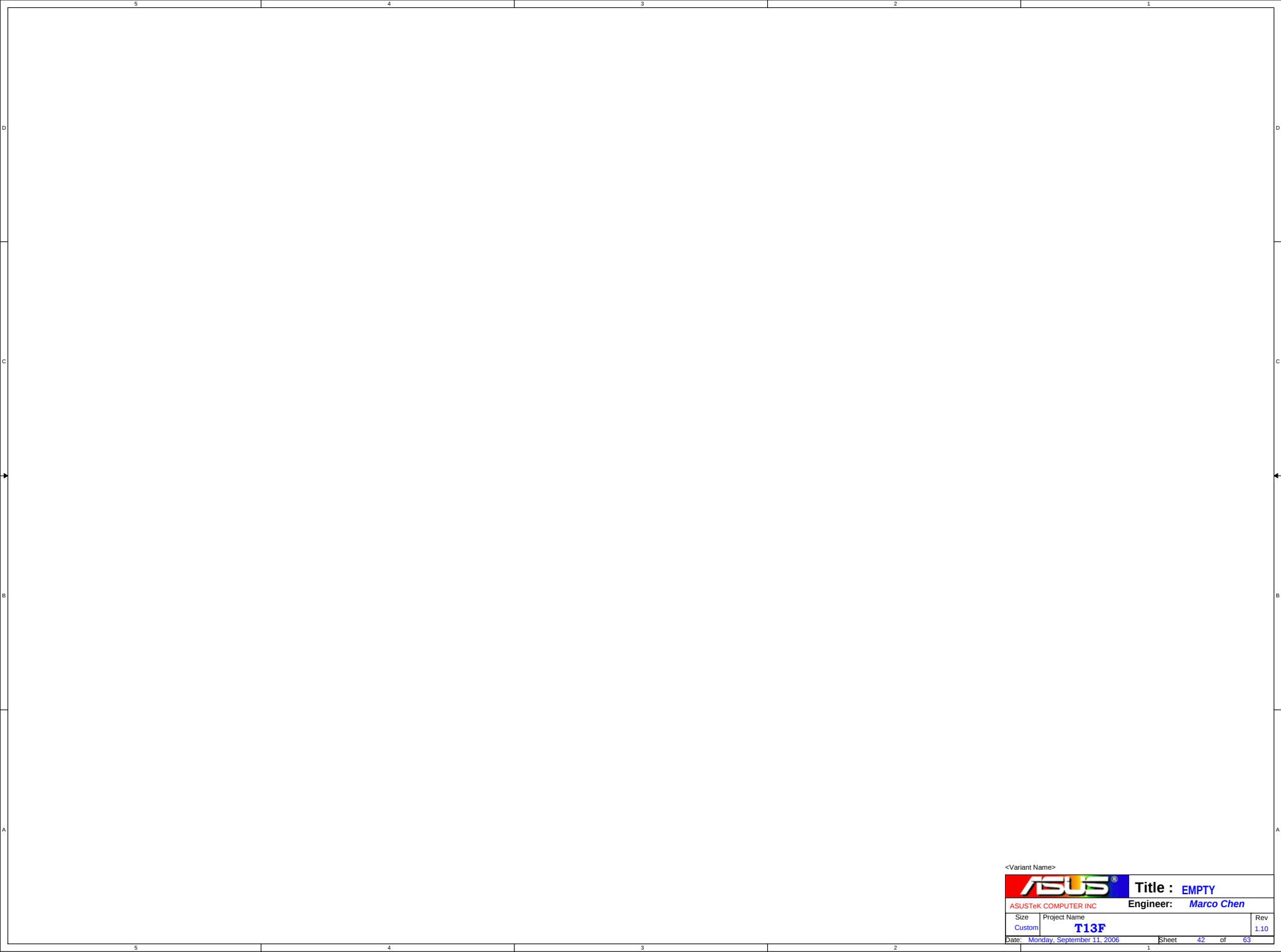
Size
Custom

Project Name	T13F
--------------	-------------

Rev	
1.10	

Date: Monday, September 11, 2006

Sheet 41 of 63



<Variant Name>					Title : EMPTY	
ASUSTek COMPUTER INC			Engineer: Marco Chen			
Size	Project Name				Rev	
Custom	T13F				1.10	
Date: Monday, September 11, 2006			Sheet	42	of	63

D

3

C

6

B

3

A

A

<Variant Name>



Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

Size
Custom

Project Name	T13F
--------------	-------------

Rev	
1.10	

Date: Monday, September 11, 2006

Sheet 43 of 63

D

3

C

6

B

3

A

A

<Variant Name>



Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: *Marco Chen*

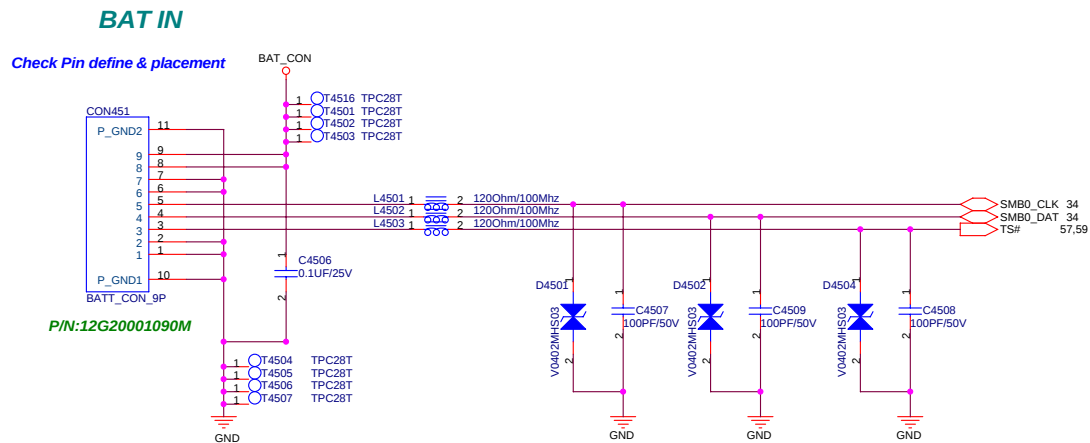
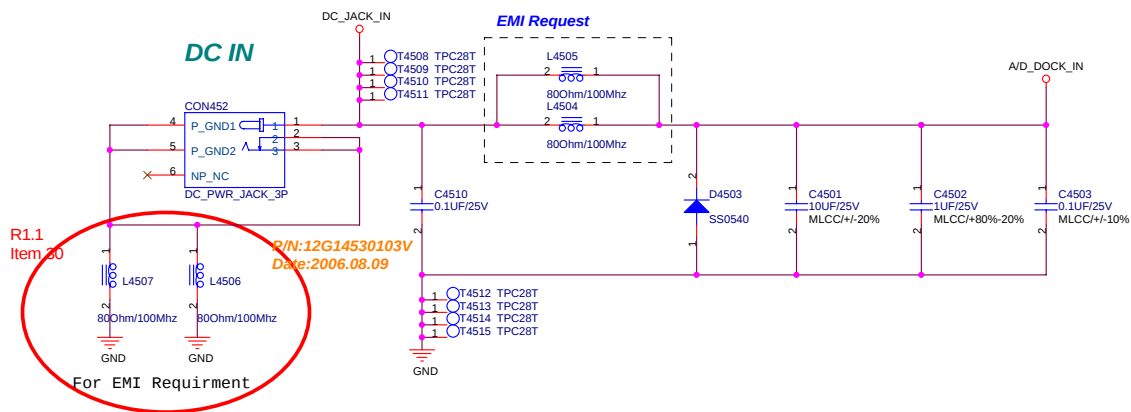
Size
Custom

Project Name	T13F
--------------	-------------

Rev	
1.10	

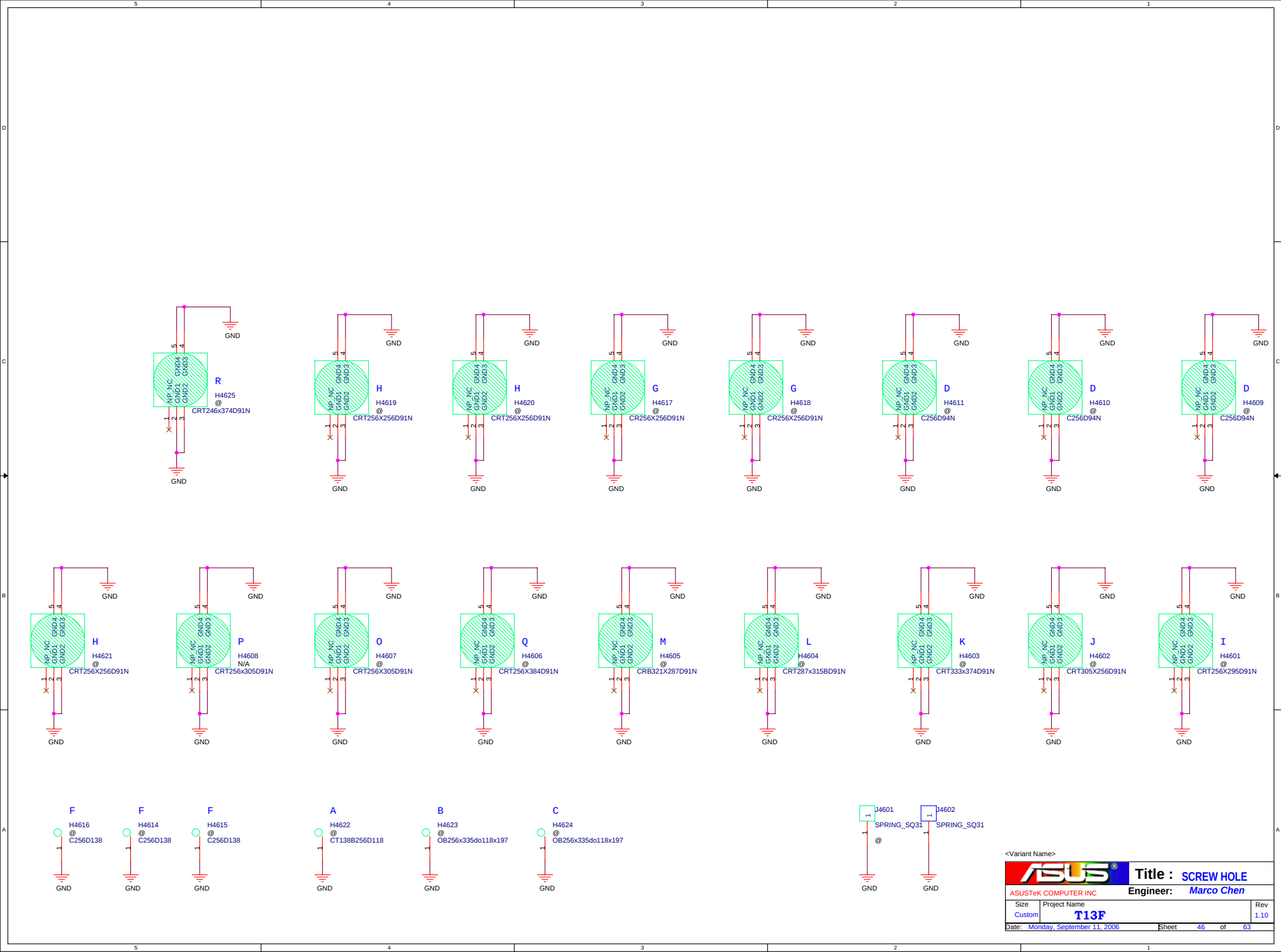
Date: Monday, September 11, 2006

Sheet 44 of 63



<Variant Name>

		Title :BAT&Adapter conn	
ASUSTek COMPUTER INC		Engineer: Marco Chen	
Size Custom	Project Name T13F	Rev 1.10	
Date: Monday, September 11, 2006			
		Sheet 45	of 63



- R1.0 -> R1.1
- 1.Page 6: DNI R611 because Int. pull-up resister exists in FAN module.

2.Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

3.Page 17: Change reference name from F3602 to F1701.

4.Page 21: DNI U2103.

5.Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.

6.Page 23: Change R2301 size from 0603 to 0402.

7.Page 23: Add pull high resister R2306*DNI and pull down resister R2307*Mount for ODD cable select.

8.Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.

9.Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.Page 32: Delete R3201 and connect MIC2_VREFOUTto R3203.1 directly.

11.Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.

12.Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

13.Page 35: Change keyboard matrix.

14.Page 36: Change reference name from JP3403 to JP3601

15.Page 36: Change R3622 size from 0402 to 0603.

16.Page 39: Delete R3920 and change Q3906 and Q3907*2N7006 to Q3908*UM6K1N.

17.Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.

18.Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.

19.Page 34: Add ESD Protection*D3402 for Touch Pad.

20.Page 27: Add series resister 33 ohm for PCI_FRAME# and PCI_AD13

21.Page 34:Change Q3403**UM6K1N to Q3404, Q3405*2N7002.

22.Page 18: Change L1801, L1802, and L1803 from bead to inductor.

23.Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

24.Page 6: Change R615 pull up from +3VS to +5VS_AUDIO0.

25.Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.

26.Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.

27.Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.

28.Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.

29.Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.

30.Page 45:Add L4506 and L4507 for EMI requirement.
- <Variant Name>

Title : [History\(1\)](#)

ASUSTeK COMPUTER INCEngineer: [Marco Chen](#)

SizeProject Name

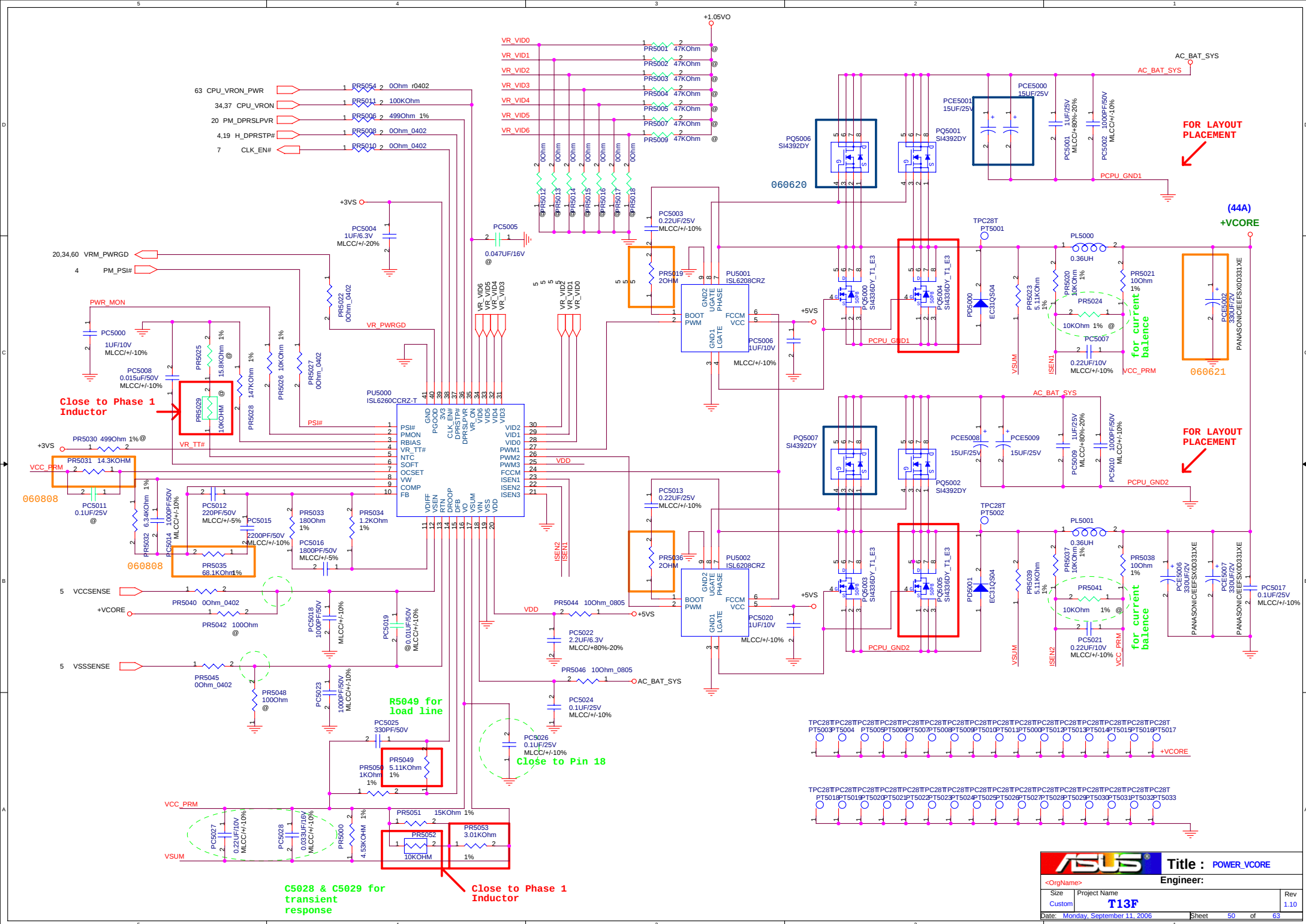
CustomT13F

Date: [Monday, September 11, 2006](#)Sheet 48 of 63

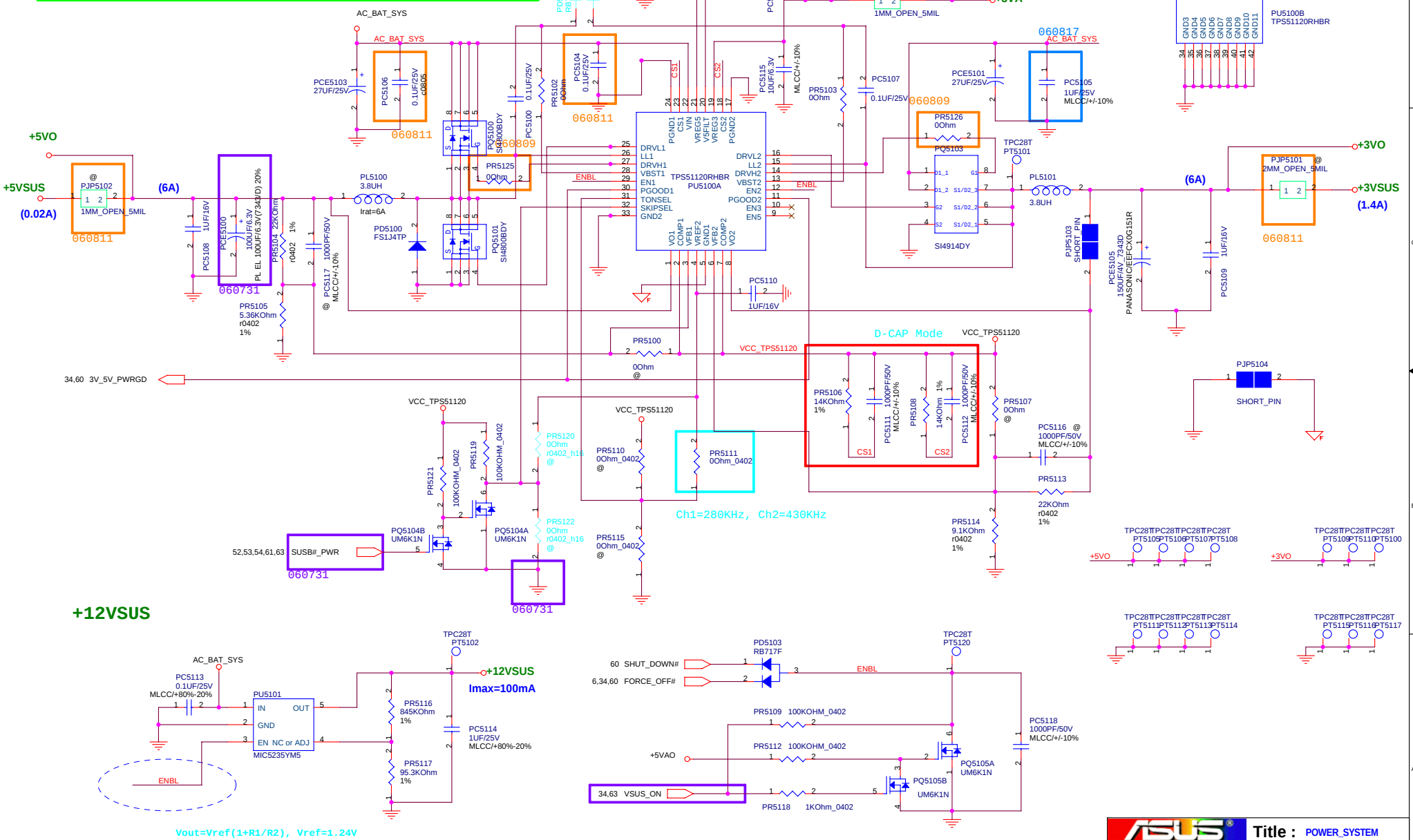
Rev1.10

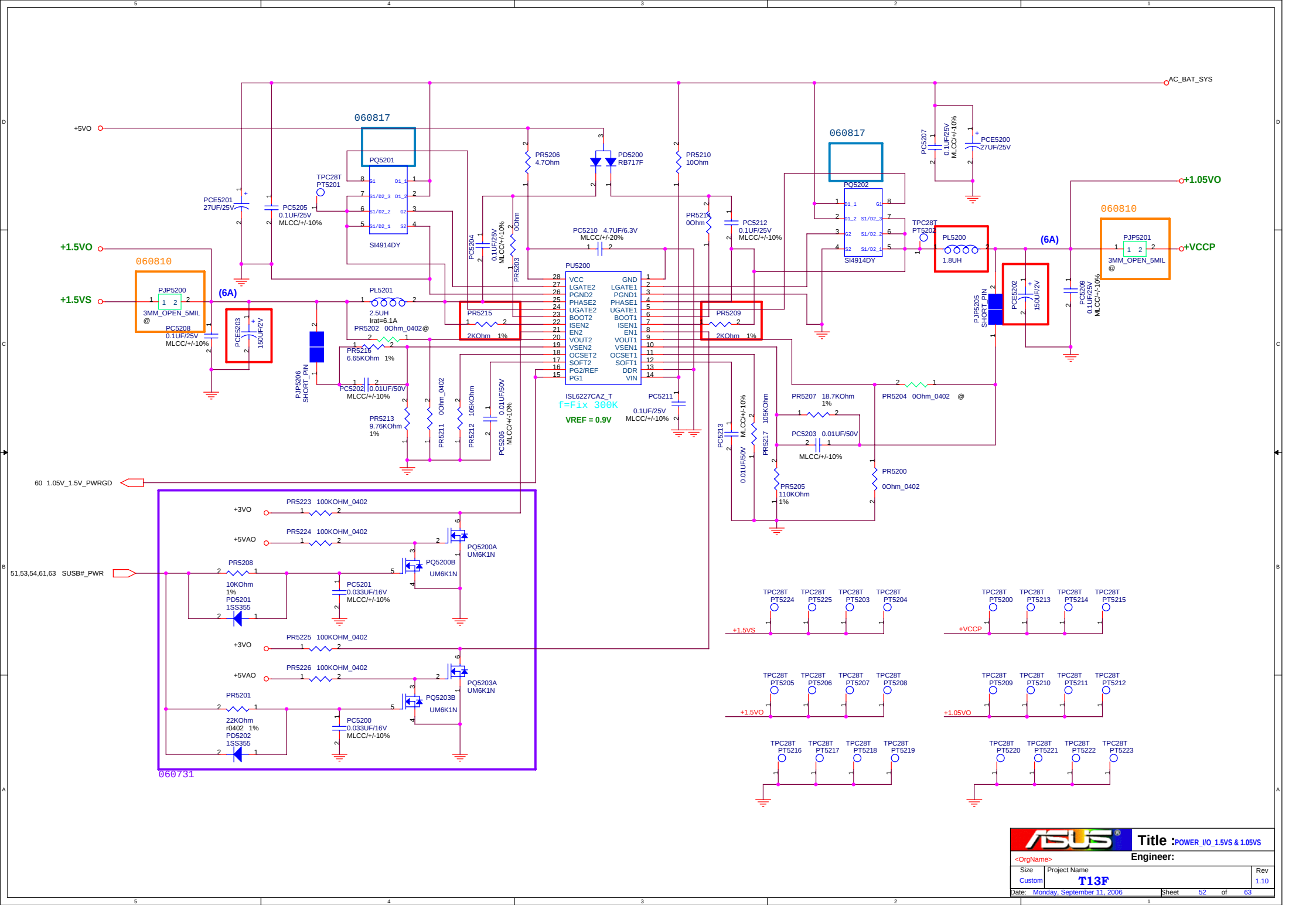
T13FG R100 (Modify from T13F_MBX_R100_0707)

- 1.DNI R749
- 2.Mount D2501
- 3.Mark page27 28 empty
- 4.DNI C3022 Mount C3021
- 5.Change CE3101, CE3102 to C3123, C3124 from 100uF to 22uF
- 6.Mount R3434, Q3501;DNI U3503
- 7.DNI RN3601, RN3602, RN3603
- 8.DNI CON3803
- 9.DNI Q3908



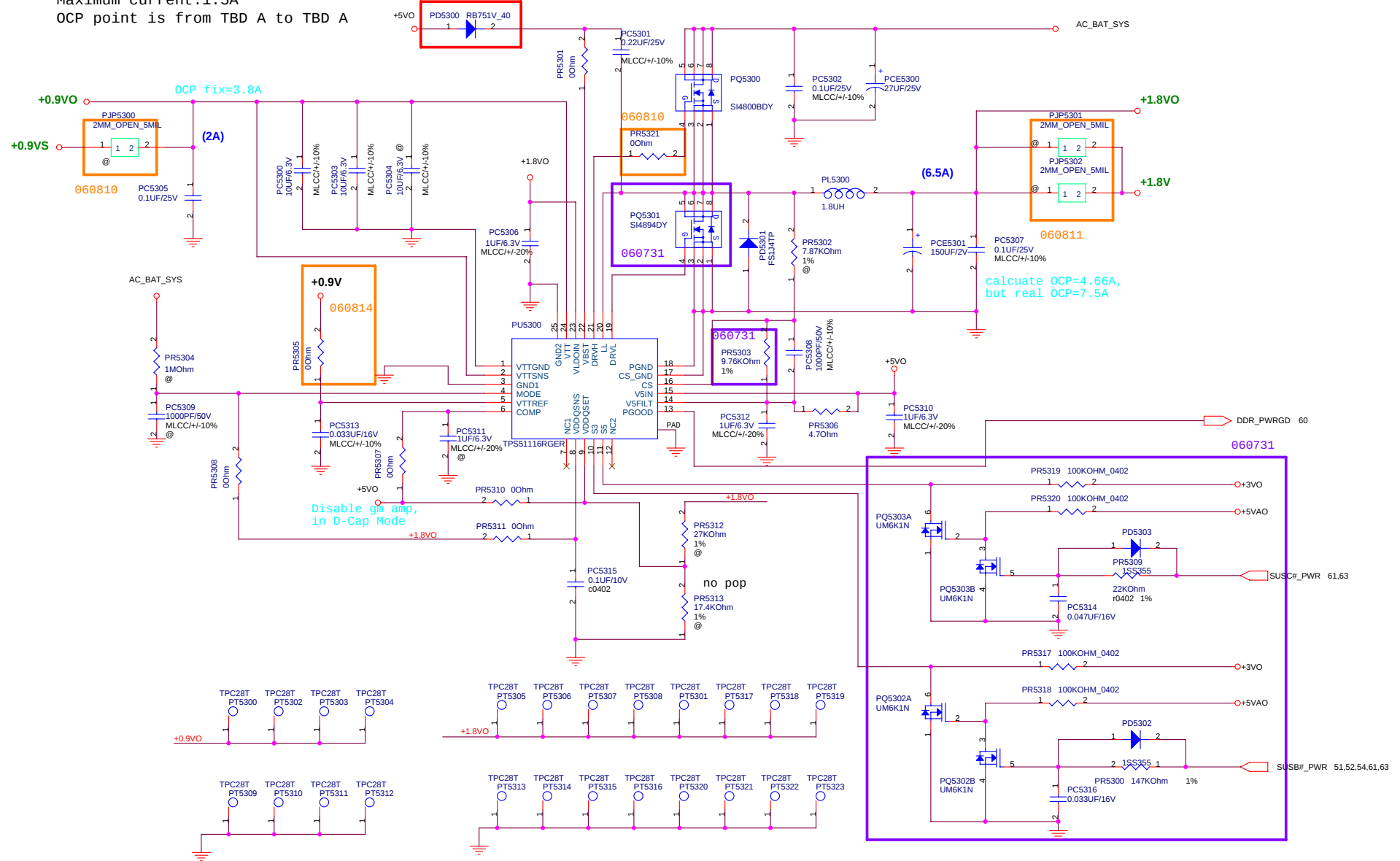
PIN	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current mode	D-CAP mode
TONSEL(KHz)	380/580	280/430	220/330	180/270
VFBI	Adjustable output		5V fixed output	
VFBI	Adjustable output		3V fixed output	
SKIPSEL	Auto-Skip	Auto-Skip(Faults off)	PWM	PWM
EN1,EN2	Swich off	NOT USE	Switch on	Switch on
EN3,EN5	LD0 off	NOT USE	LD0 on	LD0 on(EN3 only)



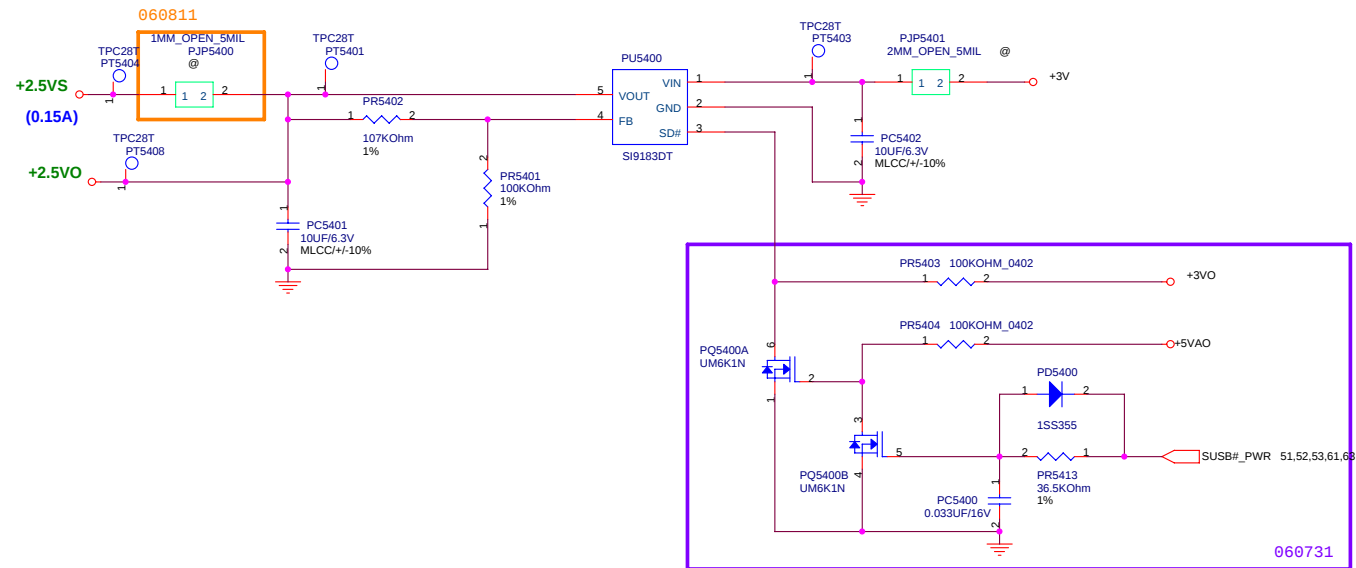


.9 Volt +/-5%
 Design Current:1.05A
 Maximum current:1.5A
 OCP point is from TBD A to TBD A

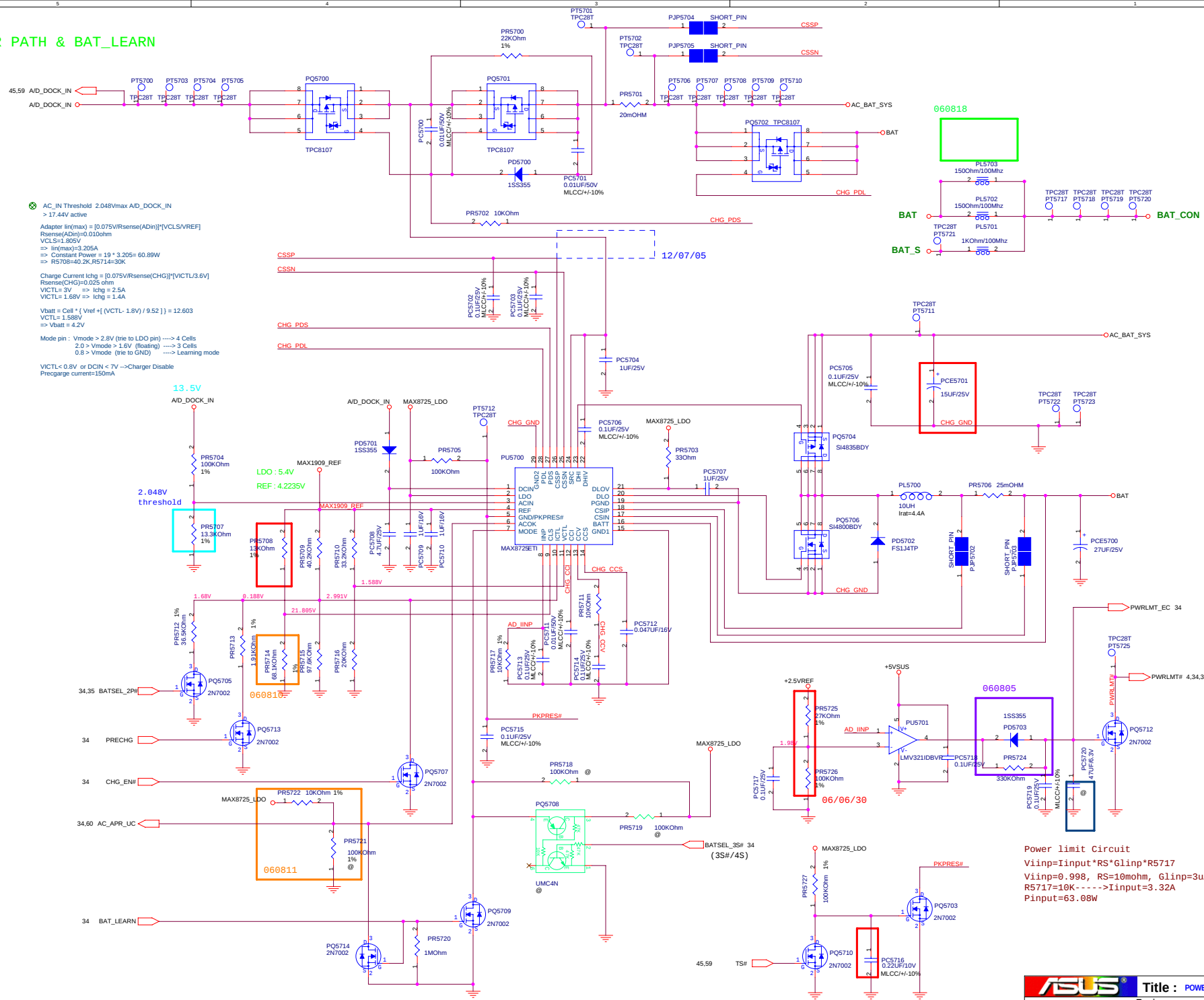
1.8Volt +/-5%
 Design Current:7.3A
 Maximum current:10.5A
 OCP point is from TBD A to TBD A



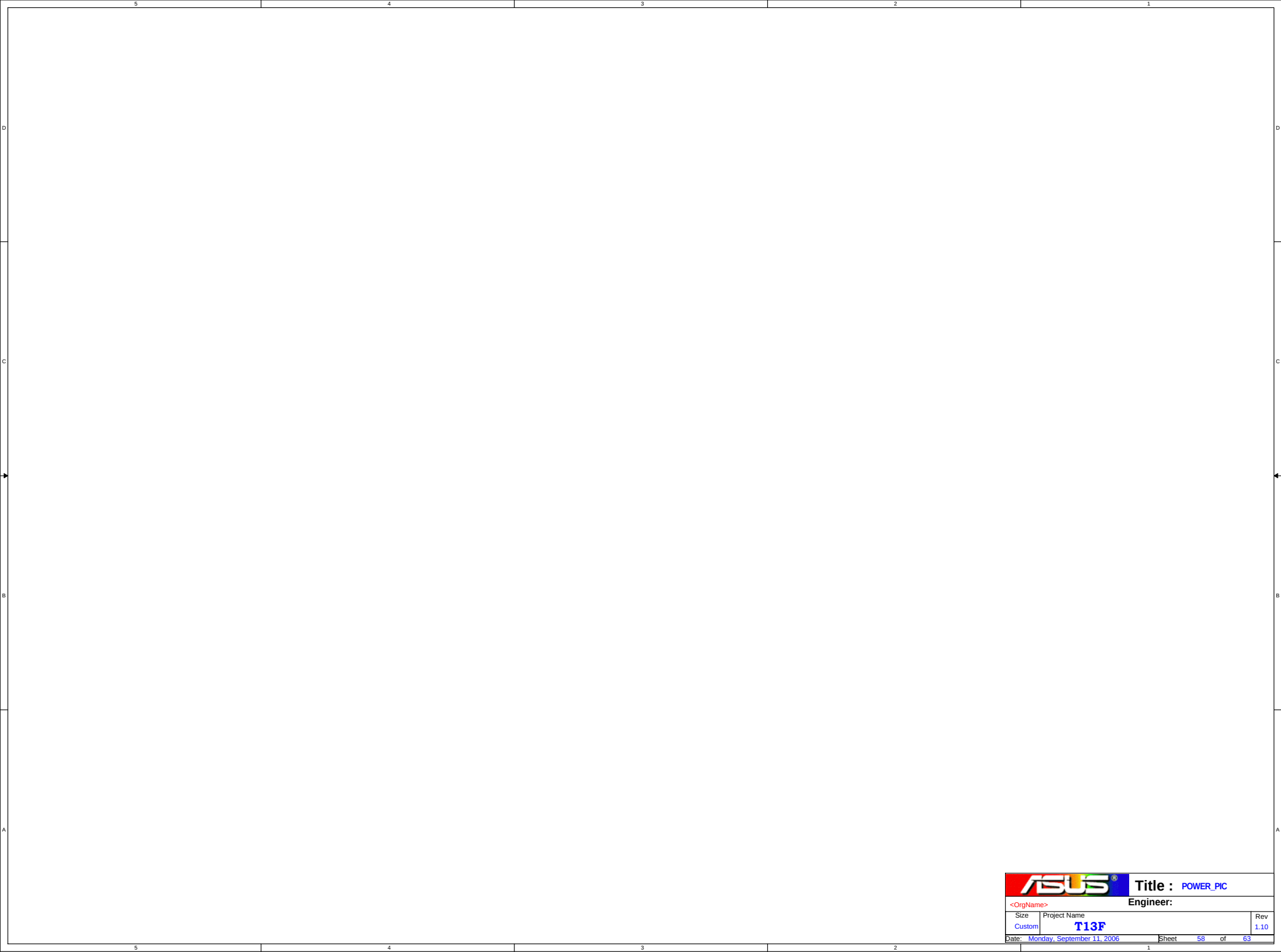
+2.5VS



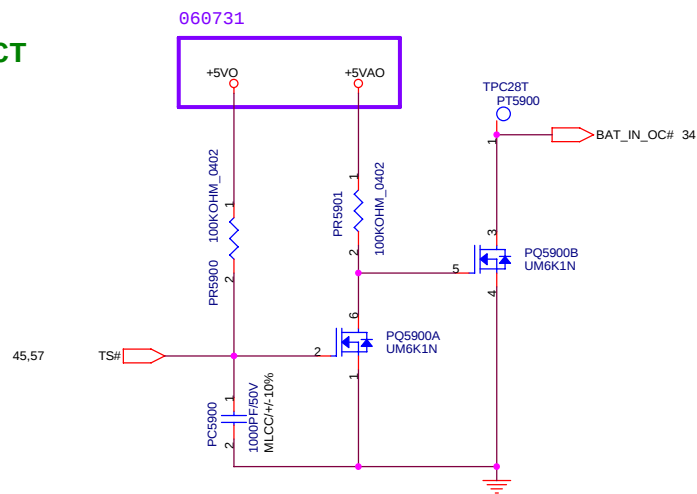
POWER PATH & BAT_LEARN



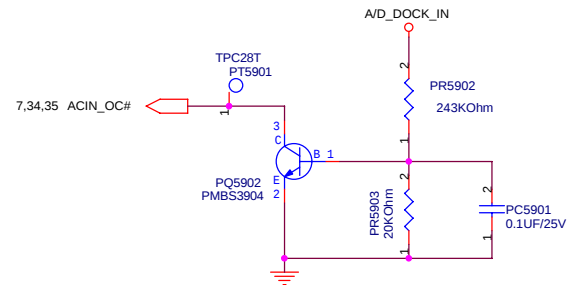
Power limit Circuit
 $V_{inp} = I_{input} \cdot R_S \cdot G_{linp} \cdot R_{5717}$
 $V_{inp} = 0.998$, $R_S = 10\text{mohm}$, $G_{linp} = 3\text{uA/mV}$,
 $R_{5717} = 10\text{K}$ -----> $I_{input} = 3.32\text{A}$
 $P_{input} = 63.08\text{W}$



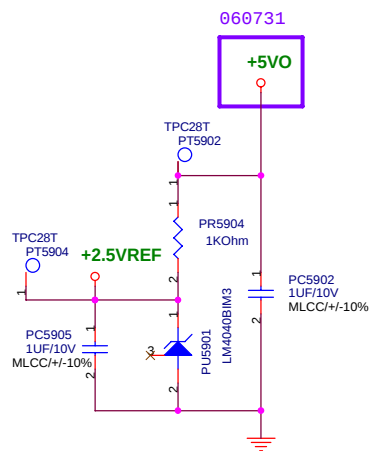
BATTERY IN DETECT

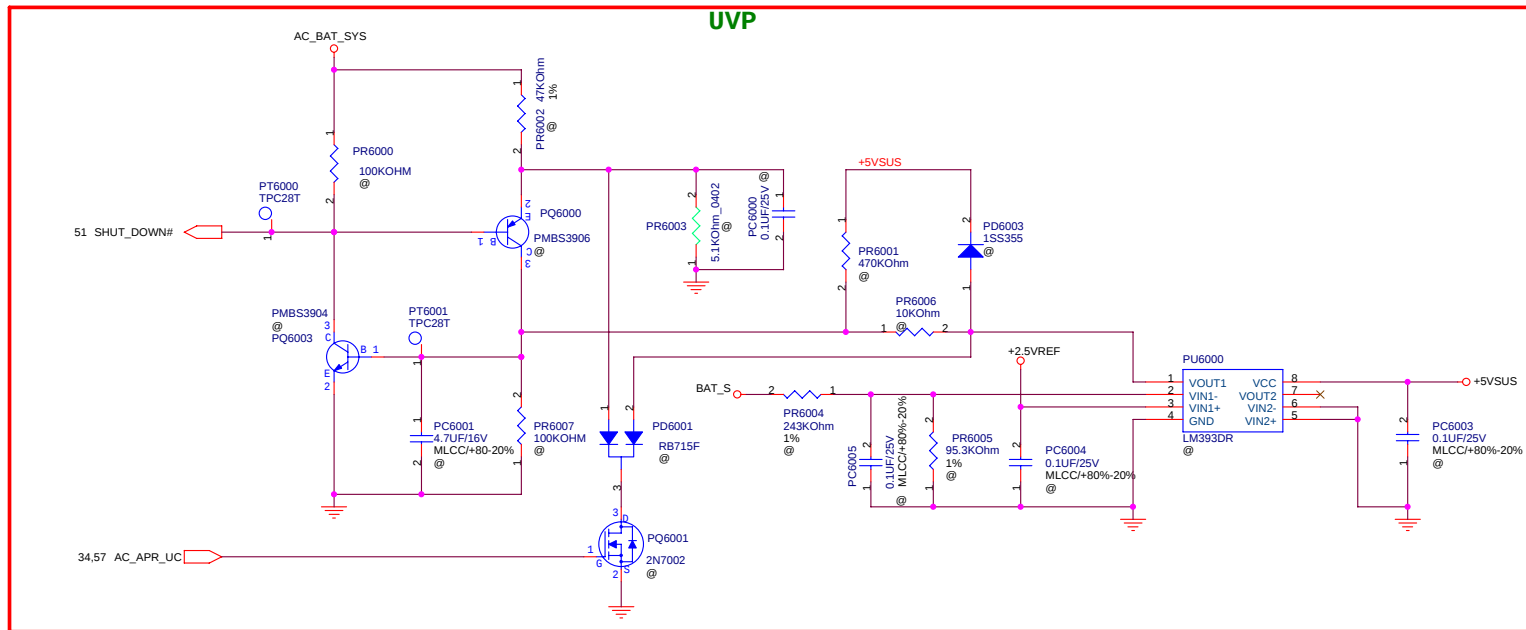


ADAPTER IN DETECT

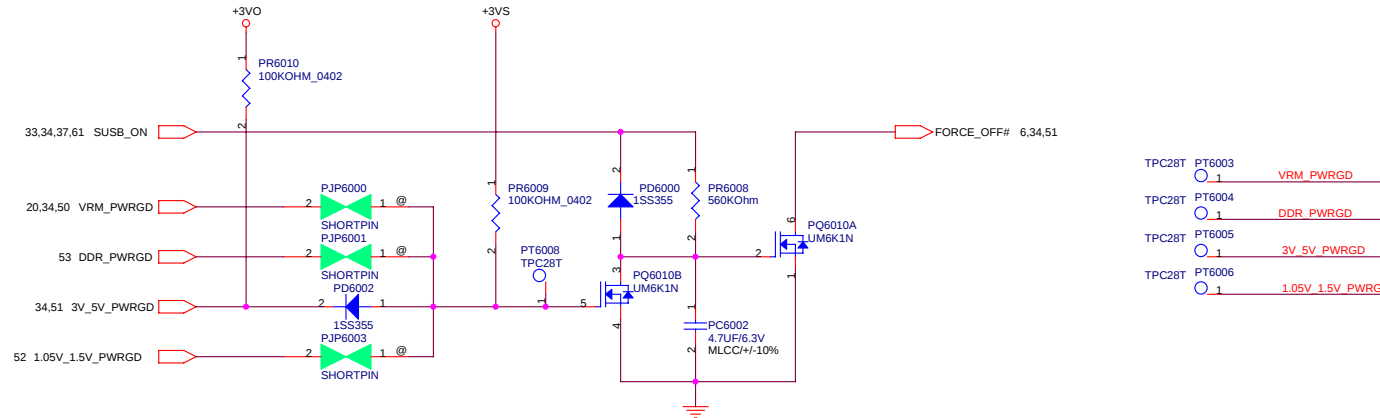


+5VLCM, +5VCHG & +2.5VREF



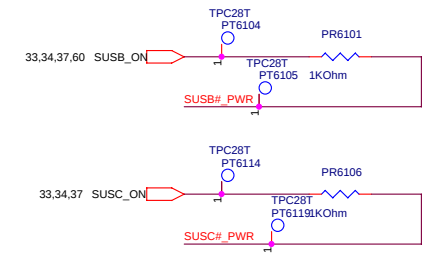
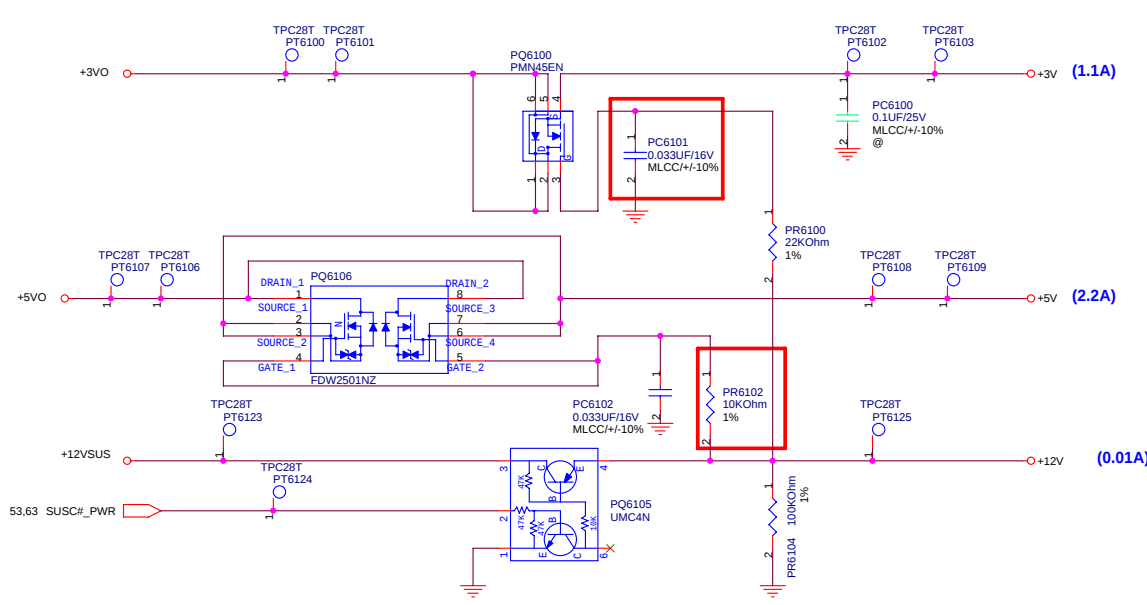


POWER GOOD DETECTOR

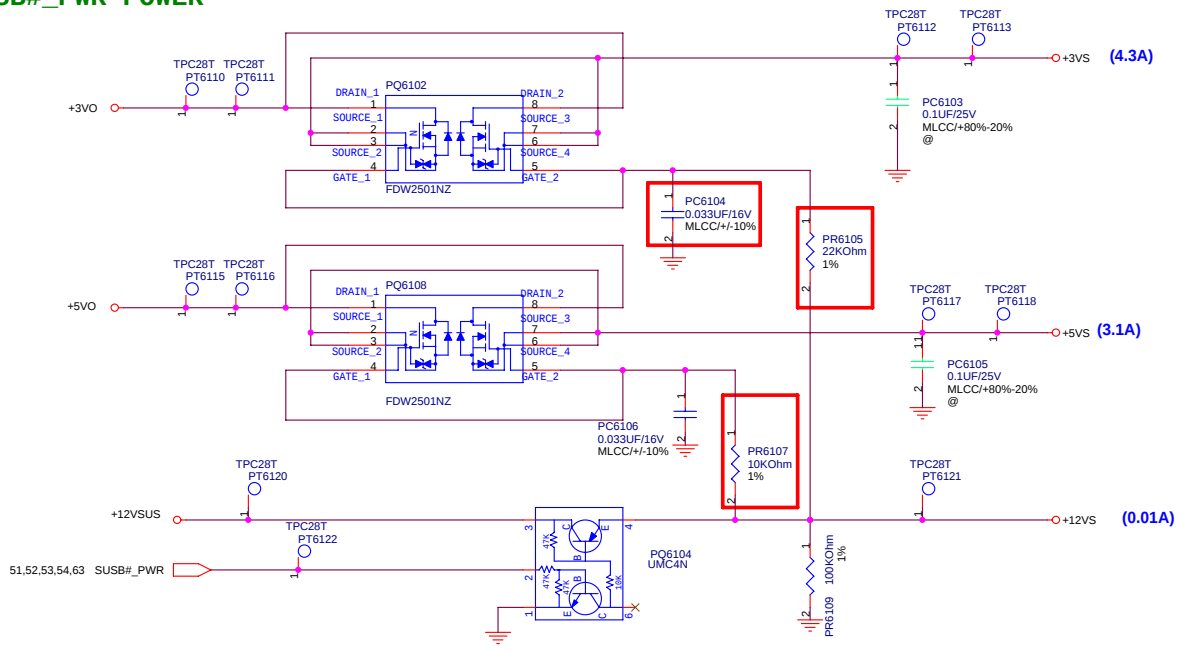


TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.5V_PWRGD

SUSC#_PWR POWER



SUSB#_PWR POWER





FOR POWER TEST

