# T13Fv SCHEMATIC R1.11

## SYSTEM PAGE REF.



## POWER PAGE REF.



<Variant Name>

ASUSTeK COMPUTER INC

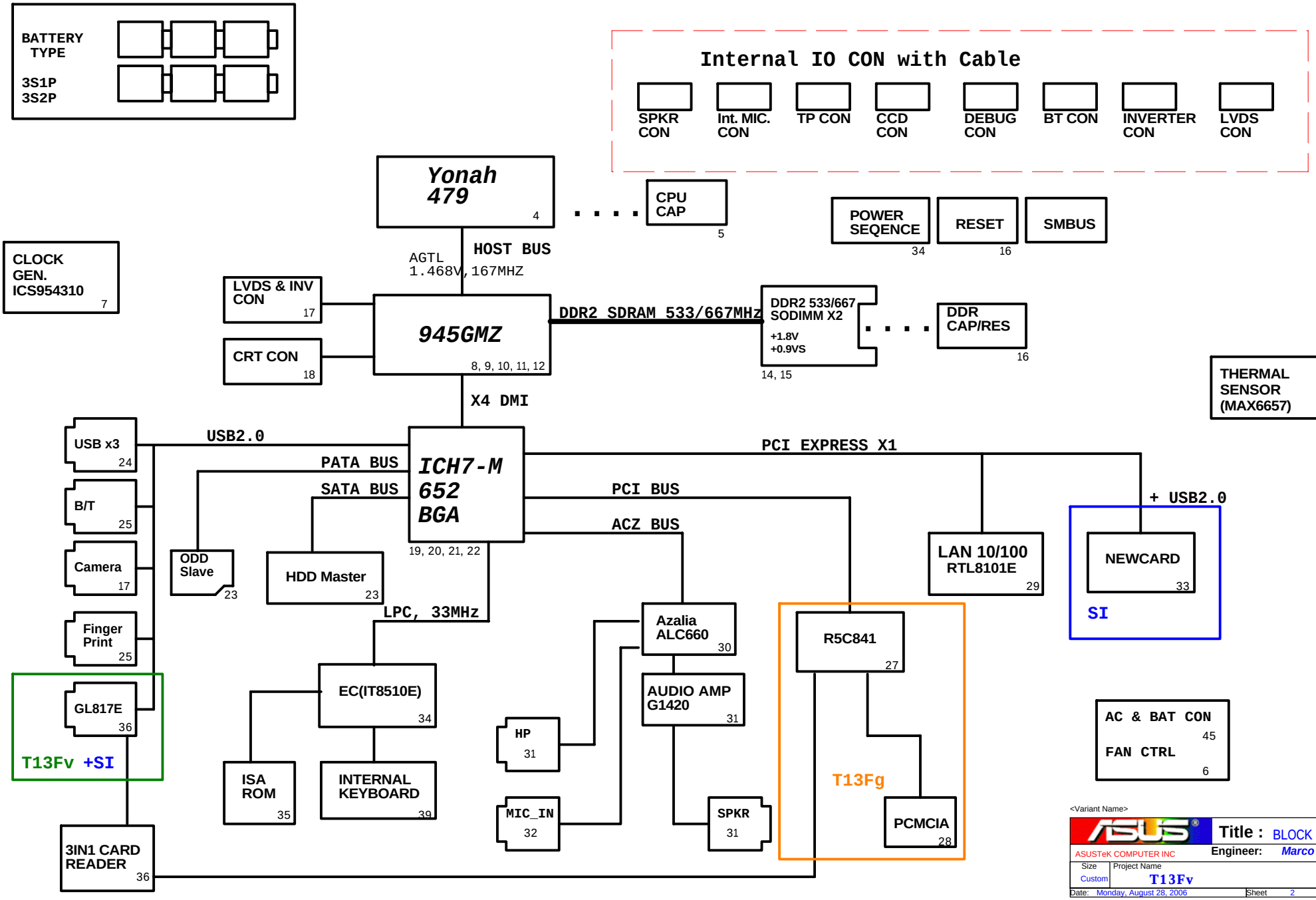
Title : PAGE REF.

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 1 of 63

# T13F BLOCK DIAGRAM




<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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## EC GPIO SETTING

| Pin | Pin Name | Signal Name | Type |
|---|---|---|---|
| 32 | PWM0/GPA0 | N/A | |
| 33 | PWM1/GPA1 | FAN_PWM | |
| 36 | PWM2/GPA2 | N/A | |
| 37 | PWM3/GPA3 | N/A | |
| 38 | PWM4/GPA4 | CHG_LED_UP# | O |
| 39 | PWM5/GPA5 | PWR_LED_UP# | O |
| 40 | PWM6/GPA6 | BATSEL_3S# | O |
| 43 | PWM7/GPA7 | LCD_BACKOFF# | O |
| 153 | RXD/GPB0 | NUM_LED | O |
| 154 | TXD/GPB1 | CAP_LED | O |
| 162 | GPB2 | N/A | O |
| 163 | SMCLK0/GPB3 | SMB0_CLK | I/0 |
| 164 | SMDAT0GPB4 | SMB0_DAT | I/0 |
| 5 | GA20/GPB5 | A20GATE | O |
| 6 | KBRST#/GPB6 | RCIN# | O |
| 165 | GPB7 | THRO_CPU | O |
| 47 | CLKOUT/GPC0 | PWRGEAR_LED | O |
| 169 | SMCLK1/GPC1 | SMB1_CLK | I/0 |
| 170 | SMDAT1/GPC2 | SMB1_DAT | I/0 |
| 171 | GPC3 | CR_DRIVER# | O |
| 172 | TMRI0/WUI2/GPC4 | ACIN_OC# | I |
| 175 | GPC5 | OP_SD# | O |
| 176 | TMRI1/WUI3/GPC6 | BAT_IN_OC# | I |
| 1 | CK32KOUT/GPC7 | EC_IDE_RST# | O |
| 26 | RI1#/WUI0/GPD0 | SUSB# | I |
| 29 | RI2#/WUI1/GPD1 | SUSC# | I |
| 30 | LPCRST#/WUI4//GPD2 | PCI_RST# | I |
| 31 | ECSCI#/GPD3 | EXT_SCI# | O |
| 41 | GPD4 | CR_POWER# | O |
| 42 | GINT/GPD5 | N/A | |
| 62 | TACH0/GPD6 | FAN0_TACH | I |
| 63 | TACH1/GPD7 | N/A | |
| 87 | ADC4/GPE0 | WLAN_BTN# | I |
| 88 | ADC5/GPE1 | N/A | I |
| 89 | ADC6/GPE2 | MARATHON# | I |
| 90 | ADC7/GPE3 | N/A | |
| 2 | PWRSW/GPE4 | PWR_SW# | I |
| 44 | WUI5/GPE5 | N/A | |
| 24 | LPCPD#/WUI6/GPE6 | LID_EC# | I |
| 25 | CLKRUN#/WUI7/GPE7 | N/A | |
| 110 | PS2CLK0/GPF0 | / | |
| 111 | PS2DAT0/GPF1 | / | |
| 114 | PS2CLK1/GPF2 | / | |
| 115 | PS2DAT1/GPF3 | / | |
| 116 | PS2CLK2/GPF4 | TP_CLK | I/0 |
| 117 | PS2DAT2/GPF5 | TP_DAT | I/0 |
| 118 | PS2CLK3/GPF6 | PWRLMT_EC# | I |
| 119 | PS2DAT3/GPF7 | / | I |
| 113 | FA16/GPG0 | FA16 | |
| 112 | FA17/GPG1 | FA17 | |
| 104 | FA18/GPG2 | FA18 | |
| 103 | FA19/GPG3 | / | |
| 3 | FA20/GPG4 | THRM_CPU# | I |
| 4 | FA21/GPG5 | N/A | |
| 27 | LPC80HL/GPG6 | PMTHERM# | O |
| 28 | LPC80LL/GPG7 | AC_APR_UC# | I |

| Pin | Pin Name | Signal Name | Type |
|---|---|---|---|
| 48 | GPH0 | VSUS_ON | O |
| 54 | GPH1 | VSUS_GD# | O |
| 55 | GPH2 | CPUPWR_GD# | O |
| 69 | GPH3 | PM_PWRBTN# | O |
| 70 | GPH4 | SUSC_ON | O |
| 75 | GPH5 | SUSB_ON | O |
| 76 | GPH6 | CPU_VRON | O |
| 105 | GPH7 | PM_RSMRST# | O |
| 148 | GPI0 | ICH7_PWROK | O |
| 149 | GPI1 | WATCH_DOG# | O |
| 152 | GPI2 | N/A | |
| 155 | GPI3 | CHG_EN# | O |
| 156 | GPI4 | PRECHG | O |
| 168 | GPI5 | BAT_LL# | O |
| 174 | GPI6 | BAT_LEARN | O |
| 81 | ADC0 | N/A | |
| 82 | ADC1 | N/A | |
| 83 | ADC2 | N/A | |
| 84 | ADC3 | SYS_TEMP | I |
| 93 | ADC8 | KID0 | |
| 94 | ADC9 | KID1 | |
| 99 | DAC0 | N/A | |
| 100 | DAC1 | N/A | |
| 101 | DAC2 | INVTER_DA | O |
| 102 | DAC3 | BATSEL_2P# | O |

## ICH7M_PCI EXPRESS:

| PCI-E Device | PAIR |
|---|---|
| RTL8101E | 1 |
| GOLAN | 2 |
| NEWCARD | 3 |

## ICH7M_SMBUS ADDRESS :

| SM-Bus Device | SM-Bus Address |
|---|---|
| Clock Generator | 1101001x ( D2 ) |
| SO-DIMM 0 | 1010000x ( A0 ) |
| SO-DIMM 1 | 1010001x ( A4 ) |
| Thermal Sensor( MAX6657) | 1001100x ( 98 ) |

## ICH7M_PCI_DEVICE:

| PCI Device | IDSEL# | REQ/GNT# | Interrupts |
|---|---|---|---|
| R5C841 | AD17 | 1 | B, D |

## ICH7M_GPIO

| Pin | | | Use As | Signal Name | Power |
|---|---|---|---|---|---|
| GPIO 00 | i | | GPI | PM_BMBUSY# | +3VS |
| GPIO 01 | i | | GPI | PCI_REQ#5 | +3VS |
| GPIO [5:2] | i | | GPI | PCI_INT[E:H]# | +3VS |
| GPIO 06 | i | | GPO | BT_LED_EN | +3VS |
| GPIO 07 | i | | GPI | N/A | +3VS |
| GPIO 08 | i | | GPI | EXTSMI# | +3VSUS |
| GPIO 09 | i | | GPI | N/A | +3VSUS |
| GPIO 10 | i | | GPI | N/A | +3VSUS |
| GPIO 11 | i | | Native | SMB_ALERT# | +3VSUS |
| GPIO 12 | i | | GPI | KBC_SCI# | +3VSUS |
| GPIO 13 | i | | GPI | N/A | +3VSUS |
| GPIO 14 | i | | GPI | N/A | +3VSUS |
| GPIO 15 | i | | GPO | 802_LED_EN | +3VSUS |
| GPIO 16 | O | 0 | GPO | PM_DPRSLPVR | +3VS |
| GPIO 17 | O | 1 | GPO | PCI_GNT#5 | +3VS |
| GPIO 18 | O | 1 | GPO | STP_PCI# | +3VS |
| GPIO 19 | i | 1 | GPI | N/A | +3VS |
| GPIO 20 | O | 1 | GPO | STP_CPU# | +3VS |
| GPIO 21 | i | 1 | GPO | N/A | +3VS |
| GPIO 22 | i | 1 | Native | PCI_REQ#4 | +3VS |
| GPIO 23 | i | 1 | Native | N/A | +3VS |
| GPIO 24 | O | 0 | GPO | MSK_PCIRST | +3VSUS |
| GPIO 25 | O | 1 | GPO | CB_SD# | +3VSUS |
| GPIO 26 | O | 0 | GPO | BT_ON# | +3VSUS |
| GPIO 27 | O | 0 | GPO | WLAN_ON# | +3VSUS |
| GPIO 28 | O | 0 | GPO | MEMROM/YONAH# | +3VSUS |
| GPIO 29 | i | 0 | Native | USB_OC#5 | +3VSUS |
| GPIO 30 | i | 0 | Native | USB_OC#6 | +3VSUS |
| GPIO 31 | i | 0 | Native | USB_OC#7 | +3VSUS |
| GPIO 32 | O | 1 | GPO | PM_CLKRUN# | +3VS |
| GPIO 33 | O | 1 | GPO | N/A | +3VS |
| GPIO 34 | O | 0 | GPO | CPU_Select | +3VS |
| GPIO 35 | O | 0 | GPO | N/A | +3VS |
| GPIO 36 | i | 0 | GPO | N/A | +3VS |
| GPIO 37 | i | 0 | GPI | PCB_ID0 | +3VS |
| GPIO 38 | i | 0 | GPI | PCB_ID1 | +3VS |
| GPIO 39 | i | 0 | GPI | PCB_ID2 | +3VS |
| GPIO [40:47] | | | NA | NA | NA |
| GPIO 48 | | | Native | PCI_GNT#4 | +3VS |
| GPIO 49 | | | Native | H_PWRGD | +VCORE |

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic data

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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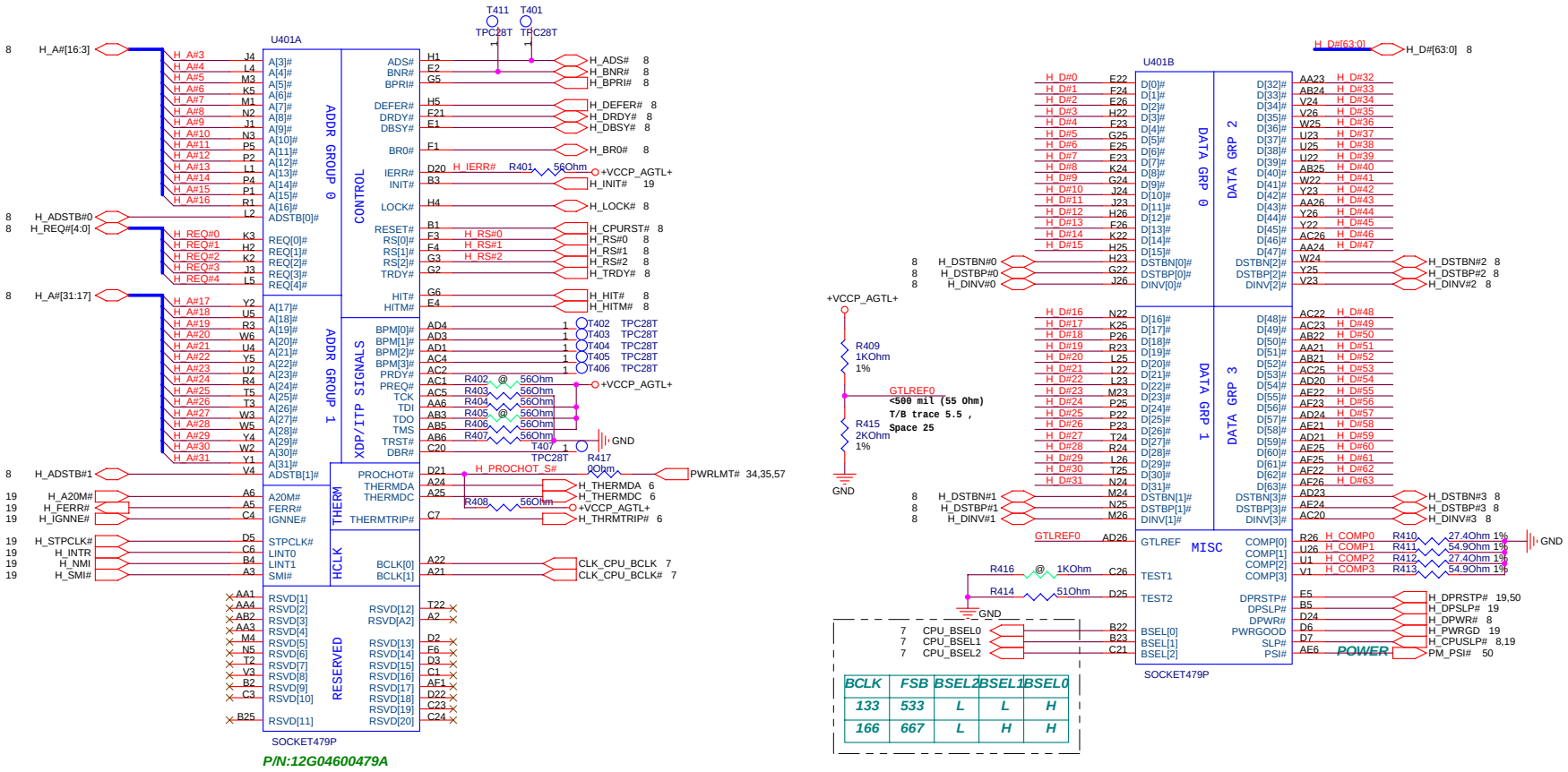


P/N:12G04600479A

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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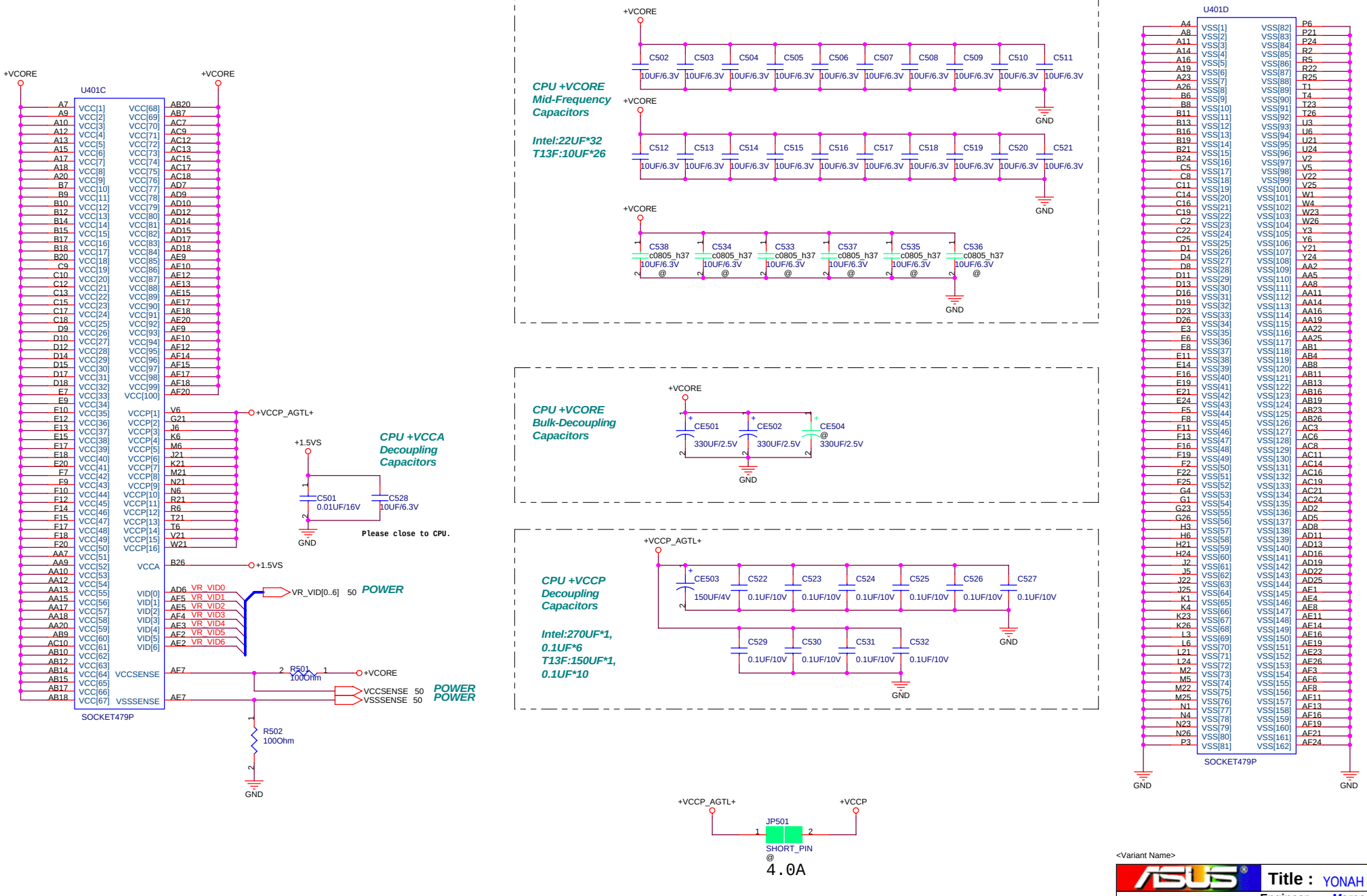
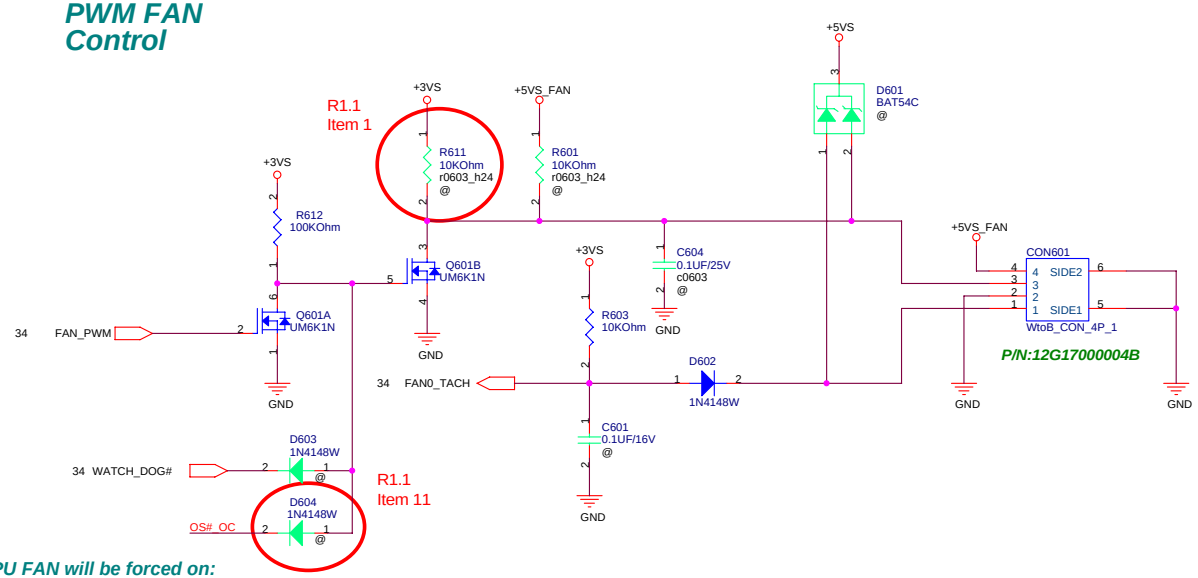
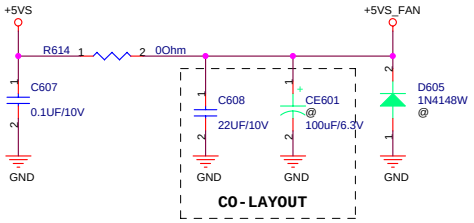



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : YONAH CPU (2) | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 5 of 63 | |

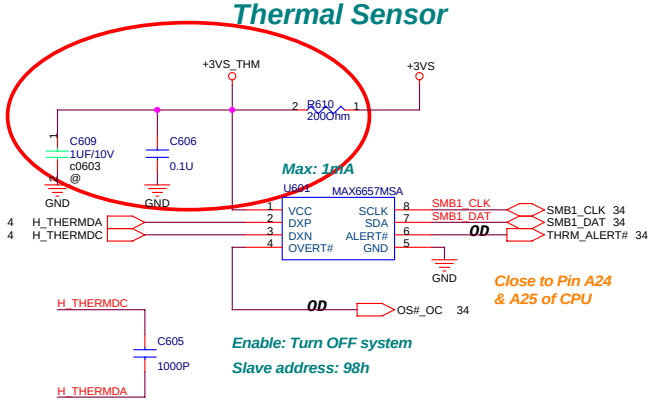
# PWM FAN Control

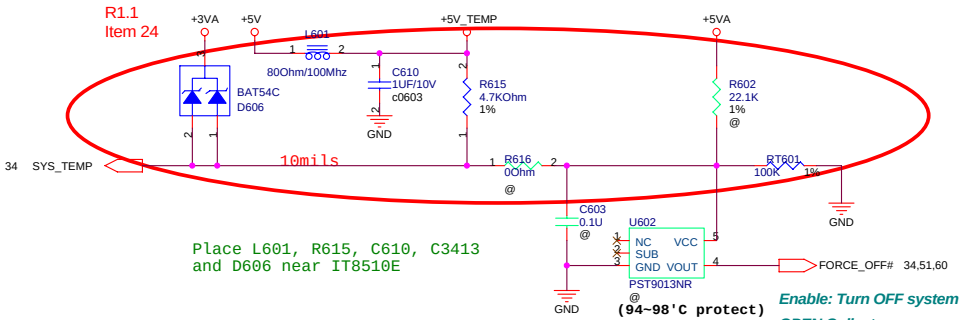


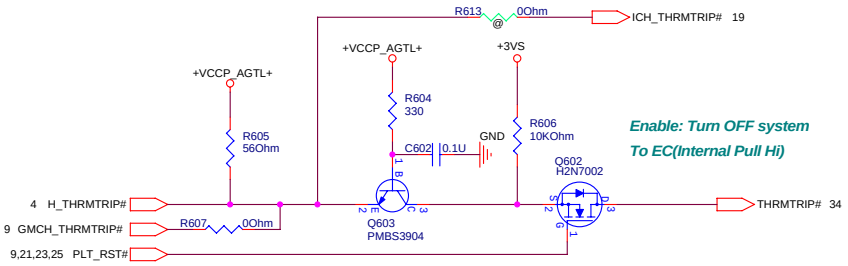




**CPU FAN will be forced on:**
**1) Thermal Sensor Over-temperture**
**2) WATCHDOG asserted by EC**

# Thermal Sensor

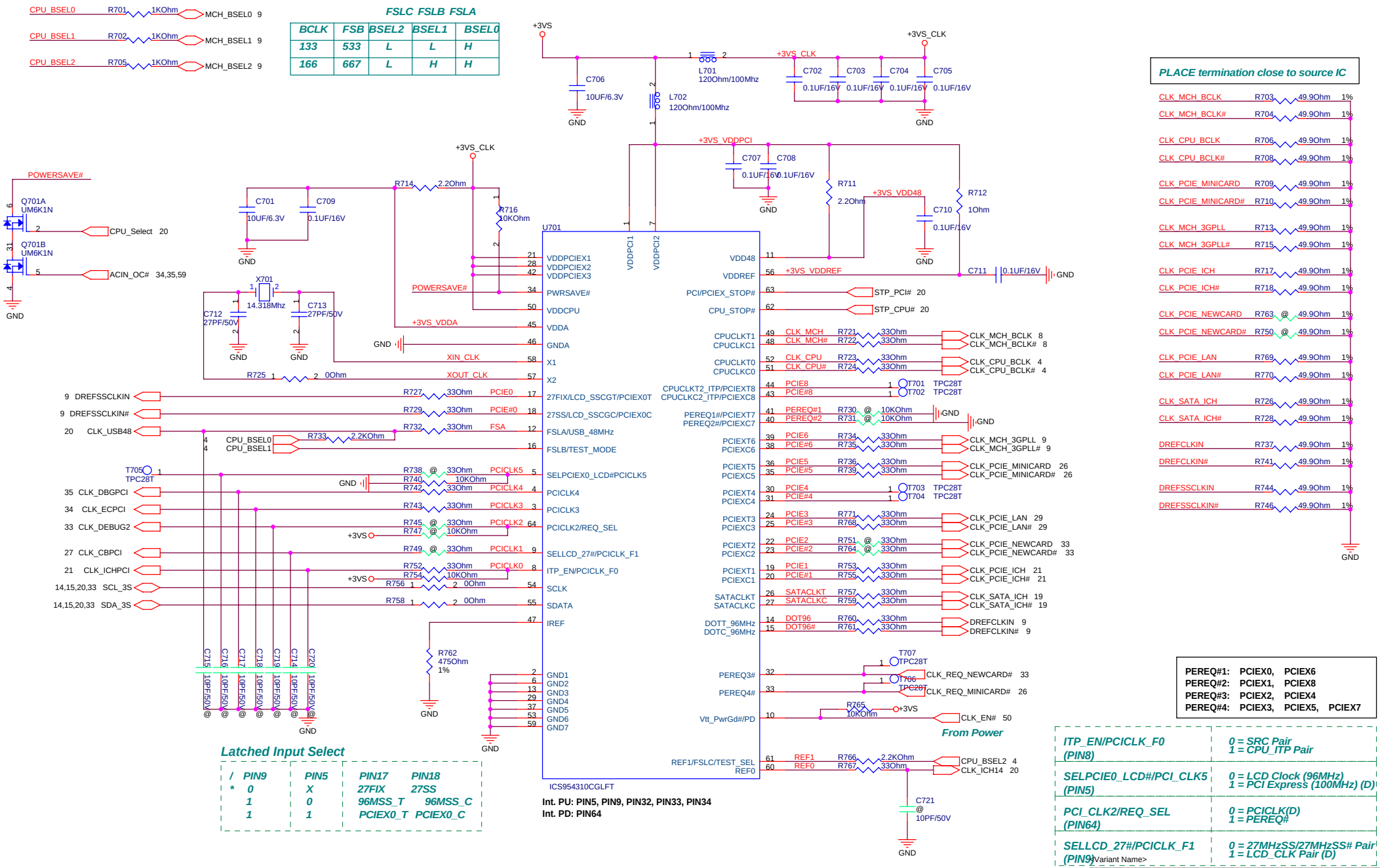



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : FAN_CTRL&Thernal | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 6 of 63 | |


CPU_BSEL0 R701 1KOhm MCH_BSEL0 9
CPU_BSEL1 R702 1KOhm MCH_BSEL1 9
CPU_BSEL2 R705 1KOhm MCH_BSEL2 9
FSLC FSLB FSLA
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
PLACE termination close to source IC
CLK_MCH_BCLK R703 49.9Ohm 1%
CLK_MCH_BCLK# R704 49.9Ohm 1%
CLK_CPU_BCLK R706 49.9Ohm 1%
CLK_CPU_BCLK# R708 49.9Ohm 1%
CLK_PCIE_MINICARD R709 49.9Ohm 1%
CLK_PCIE_MINICARD# R710 49.9Ohm 1%
CLK_MCH_3GPLL R713 49.9Ohm 1%
CLK_MCH_3GPLL# R715 49.9Ohm 1%
CLK_PCIE_ICH R717 49.9Ohm 1%
CLK_PCIE_ICH# R718 49.9Ohm 1%
CLK_PCIE_NEWCARD R763 @ 49.9Ohm 1%
CLK_PCIE_NEWCARD# R750 @ 49.9Ohm 1%
CLK_PCIE_LAN R769 49.9Ohm 1%
CLK_PCIE_LAN# R770 49.9Ohm 1%
CLK_SATA_ICH R726 49.9Ohm 1%
CLK_SATA_ICH# R728 49.9Ohm 1%
DREFCLKIN R737 49.9Ohm 1%
DREFCLKIN# R741 49.9Ohm 1%
DREFSSCLKIN R744 49.9Ohm 1%
DREFSSCLKIN# R746 49.9Ohm 1%
GND
+3VS
+3VS_CLK
C706 10UF/6.3V
L701 120Ohm/100Mhz
L702 120Ohm/100Mhz
C702 C703 C704 C705 0.1UF/16V
+3VS_VDDPCI
C707 C708 0.1UF/16V
R711 2.2Ohm
+3VS_VDD48
R712 1Ohm
C710 0.1UF/16V
C711 0.1UF/16V
POWERSAVE#
Q701A UM6K1N
Q701B UM6K1N
CPU_Select 20
ACIN_OC# 34,35,59
C701 10UF/6.3V
C709 0.1UF/16V
R714 2.2Ohm
R716 10KOhm
X701 14.318Mhz
C712 27PF/50V
C713 27PF/50V
+3VS_VDDA
XIN_CLK
XOUT_CLK
R725 0Ohm
U701
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
CPUCLKT2_ITP/PCIEXT8
CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7
PEREQ2#/PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXT1
PCIEXC1
SATACLKT
SATACLKC
DOTT_96MHz
DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
ICS954310CGLFT
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64
STP_PCI# 20
STP_CPU# 20
CLK_MCH_BCLK 8
CLK_MCH_BCLK# 8
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_3GPLL 9
CLK_MCH_3GPLL# 9
CLK_PCIE_MINICARD 26
CLK_PCIE_MINICARD# 26
CLK_PCIE_LAN 29
CLK_PCIE_LAN# 29
CLK_PCIE_NEWCARD 33
CLK_PCIE_NEWCARD# 33
CLK_PCIE_ICH 21
CLK_PCIE_ICH# 21
CLK_SATA_ICH 19
CLK_SATA_ICH# 19
DREFCLKIN 9
DREFCLKIN# 9
CLK_REQ_NEWCARD# 33
CLK_REQ_MINICARD# 26
CLK_EN# 50
From Power
CPU_BSEL2 4
CLK_ICH14 20
T701 TPC28T
T702 TPC28T
T703 TPC28T
T704 TPC28T
T705 TPC28T
T706 TPC28T
T707 TPC28T
R762 475Ohm 1%
C721 @ 10PF/50V
PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7
Latched Input Select
/ PIN9 PIN5 PIN17 PIN18
* 0 X 27FIX 27SS
1 0 96MSS_T 96MSS_C
1 1 PCIEX0_T PCIEX0_C
ITP_EN/PCICLK_F0 (PIN8)
0 = SRC Pair
1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)
0 = PCICLK(D)
1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair (D)
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICS954310
Engineer: Marco Chen
Size Custom
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
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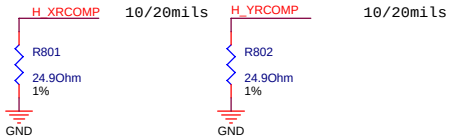
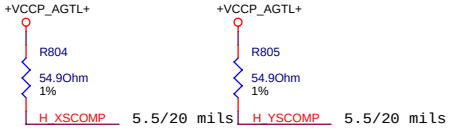
## RCOMP

*For Calibrating FSB I/O Buffer*



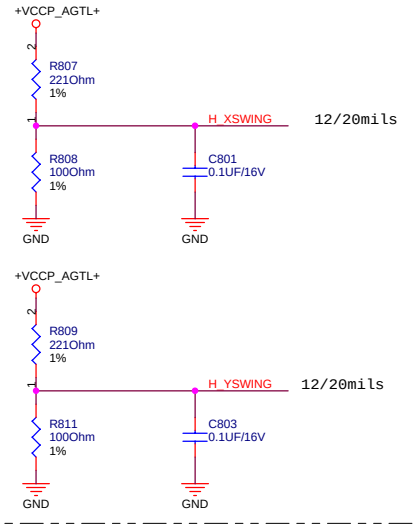

## SCOMP

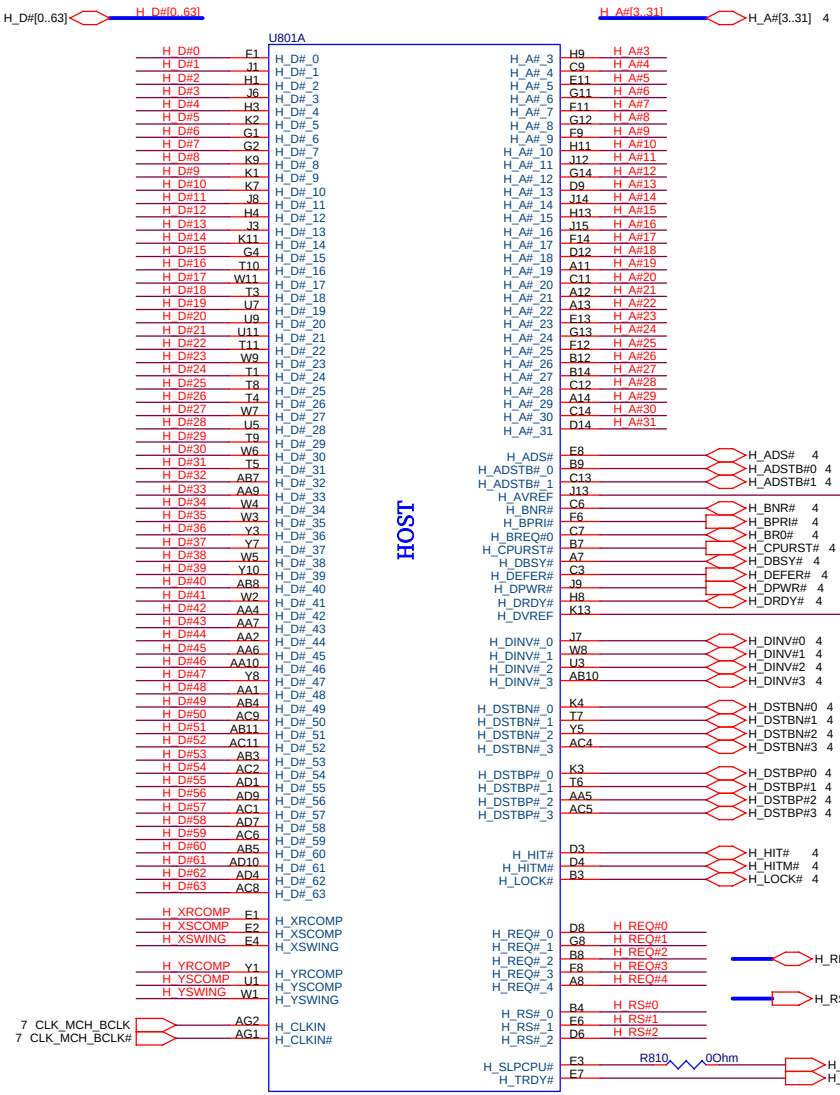
*For Slew Rate Compensation on the FSB*



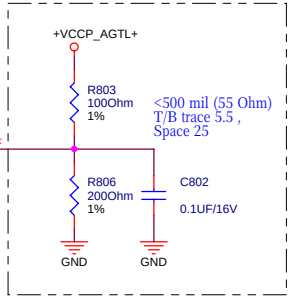

## Voltage Swing

*For Providing a Reference Voltage to The FSB RCOMP Circuit*




## AGTL+ I/O Voltage Reference




<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--CPU

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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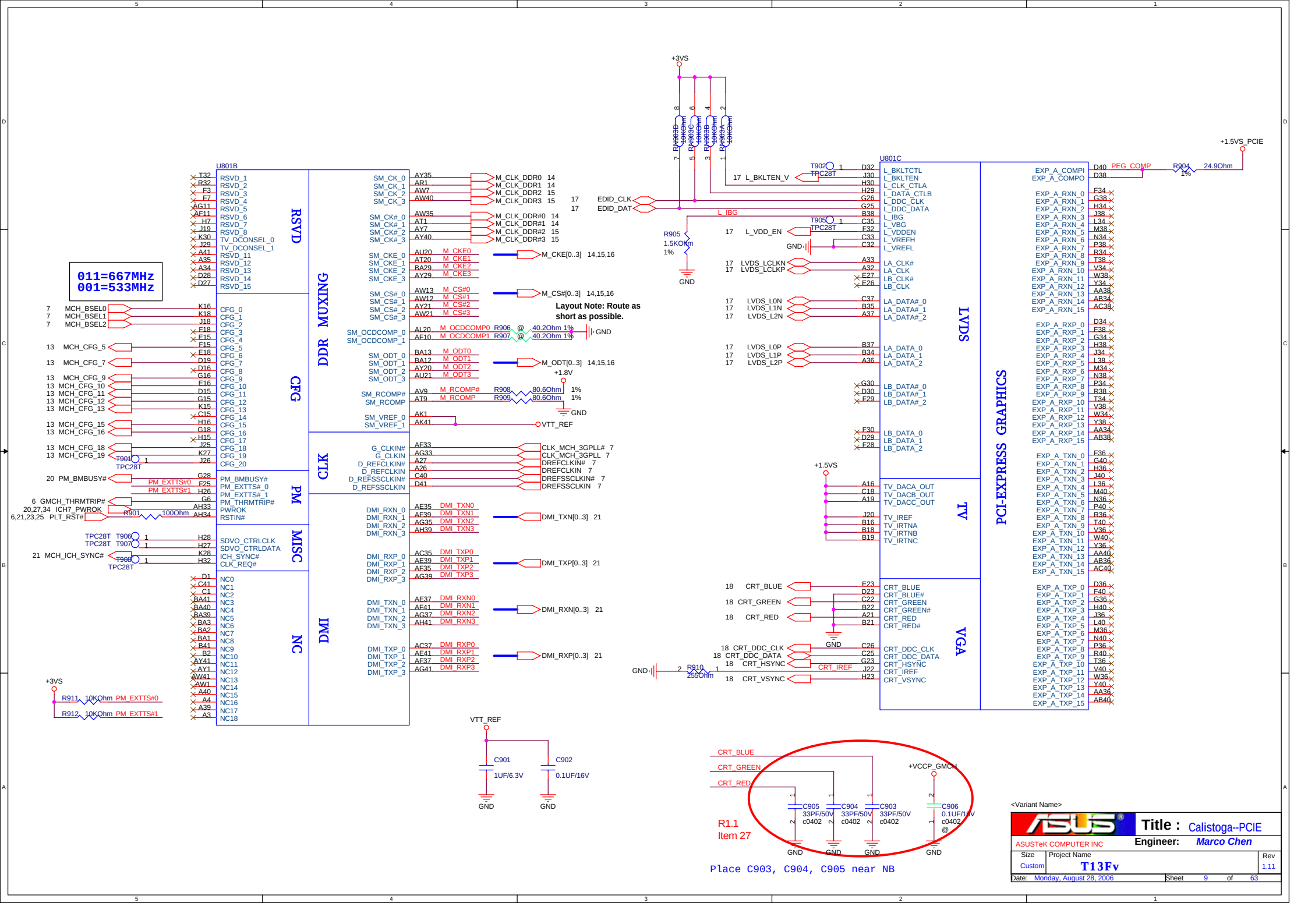
011=667MHz
001=533MHz
U801B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
U801C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
+3VS
+1.5VS
+1.5VS_PCIE
+1.8V
VTT_REF
GND
EDID_CLK
EDID_DAT
L_IBG
L_BKLTEN_V
L_VDD_EN
R905 1.5KOhm 1%
R904 24.9Ohm 1%
PEG_COMP
R906 @ 40.2Ohm 1%
R907 @ 40.2Ohm 1%
R908 80.6Ohm 1%
R909 80.6Ohm 1%
R910 255Ohm
R901 100Ohm
R911 10KOhm PM_EXTTS#0
R912 10KOhm PM_EXTTS#1
M_CLK_DDR0 14
M_CLK_DDR1 14
M_CLK_DDR2 15
M_CLK_DDR3 15
M_CKE[0..3] 14,15,16
M_CS#[0..3] 14,15,16
M_ODT[0..3] 14,15,16
Layout Note: Route as short as possible.
CLK_MCH_3GPLL# 7
CLK_MCH_3GPLL 7
DREFCLKIN# 7
DREFCLKIN 7
DREFSSCLKIN# 7
DREFSSCLKIN 7
DMI_TXN[0..3] 21
DMI_TXP[0..3] 21
DMI_RXN[0..3] 21
DMI_RXP[0..3] 21
C901 1UF/6.3V
C902 0.1UF/16V
C903 33PF/50V c0402
C904 33PF/50V c0402
C905 33PF/50V c0402
C906 0.1UF/16V c0402 @
+VCCP_GMCH
R1.1
Item 27
Place C903, C904, C905 near NB
<Variant Name>
Title : Calistoga--PCIE
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13Fv
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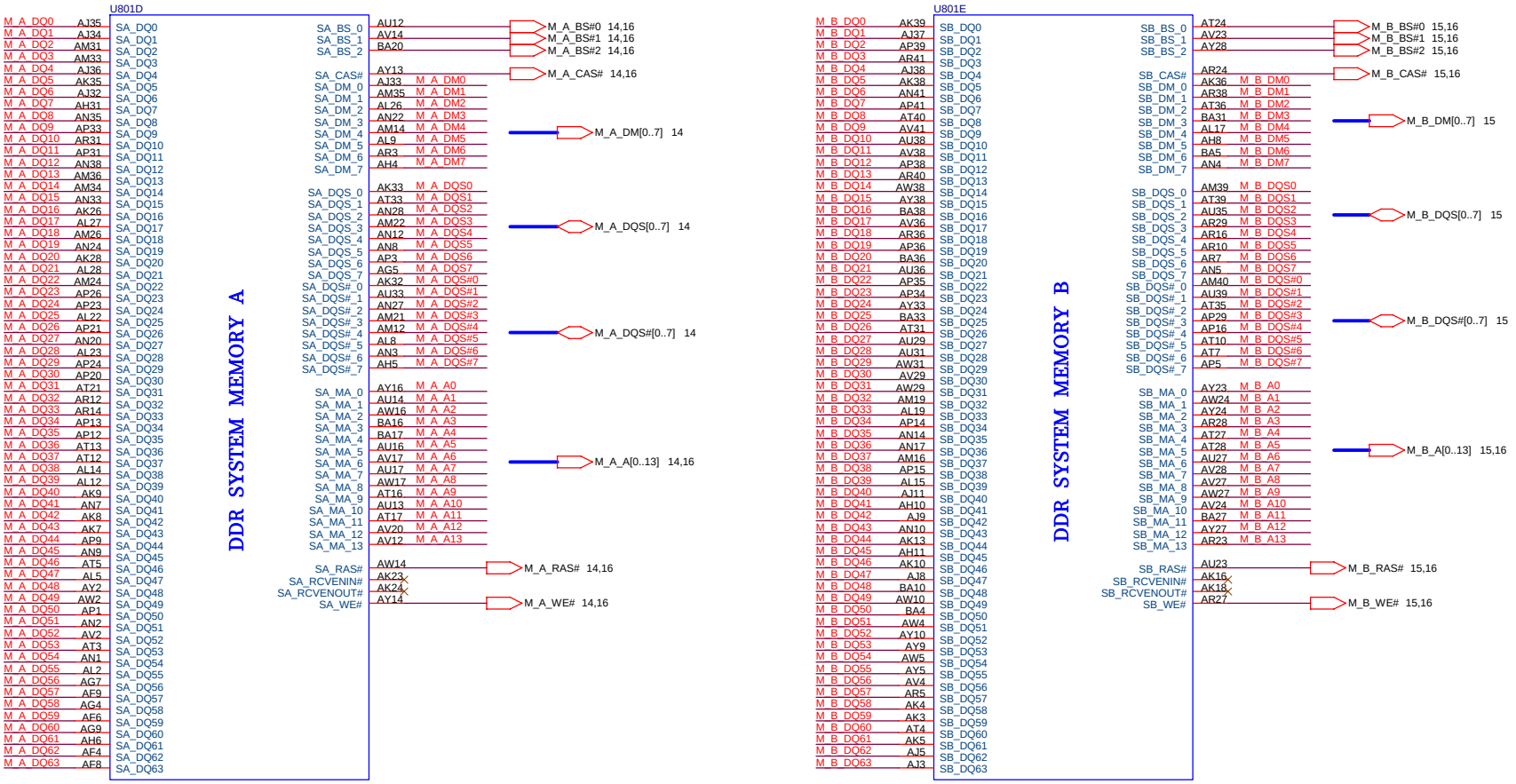
14 M_A_DQ[0..63]

15 M_B_DQ[0..63]




<Variant Name>

ASUSTeK COMPUTER INC

Title : Calistoga--DDR2

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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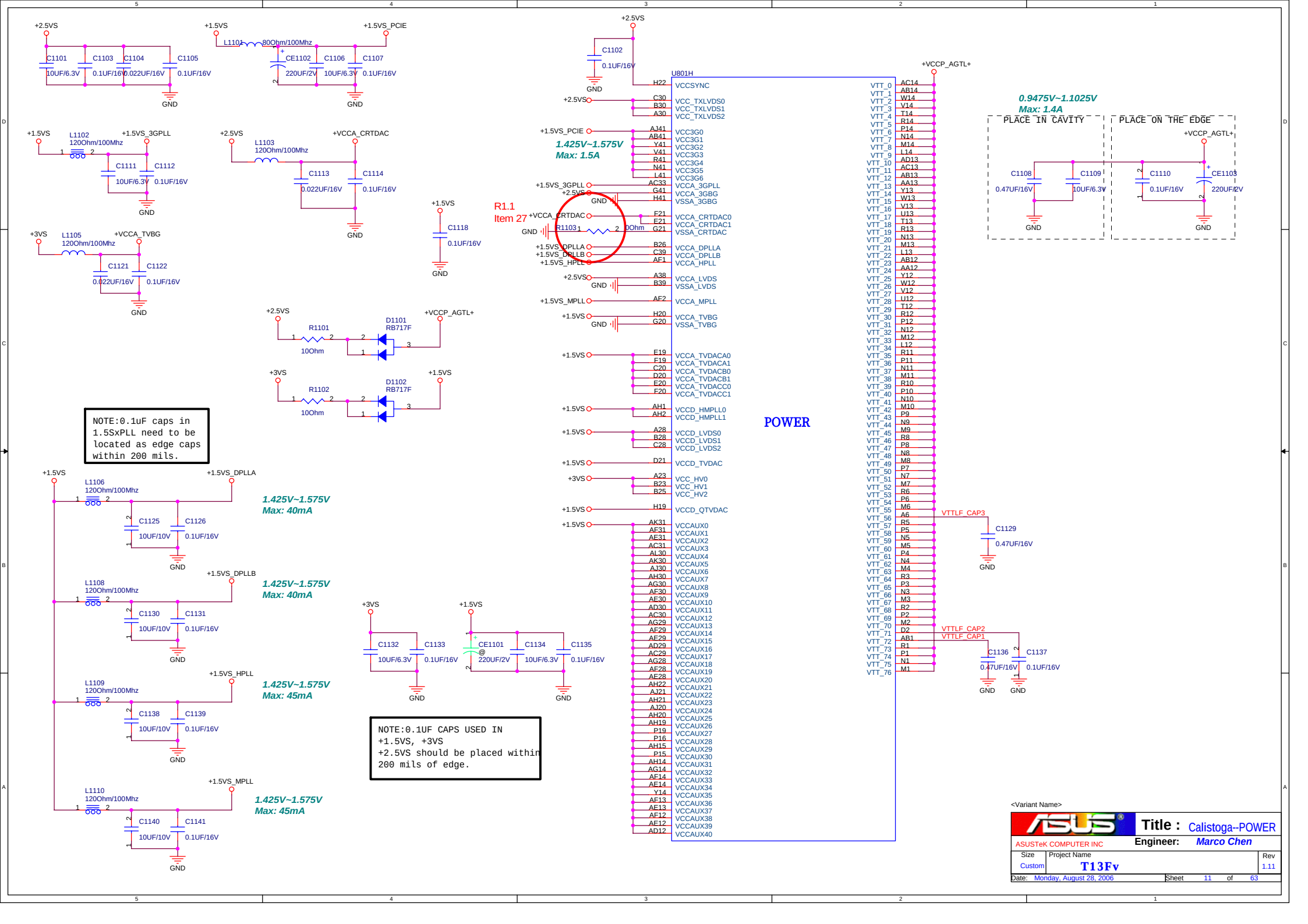



<Variant Name>

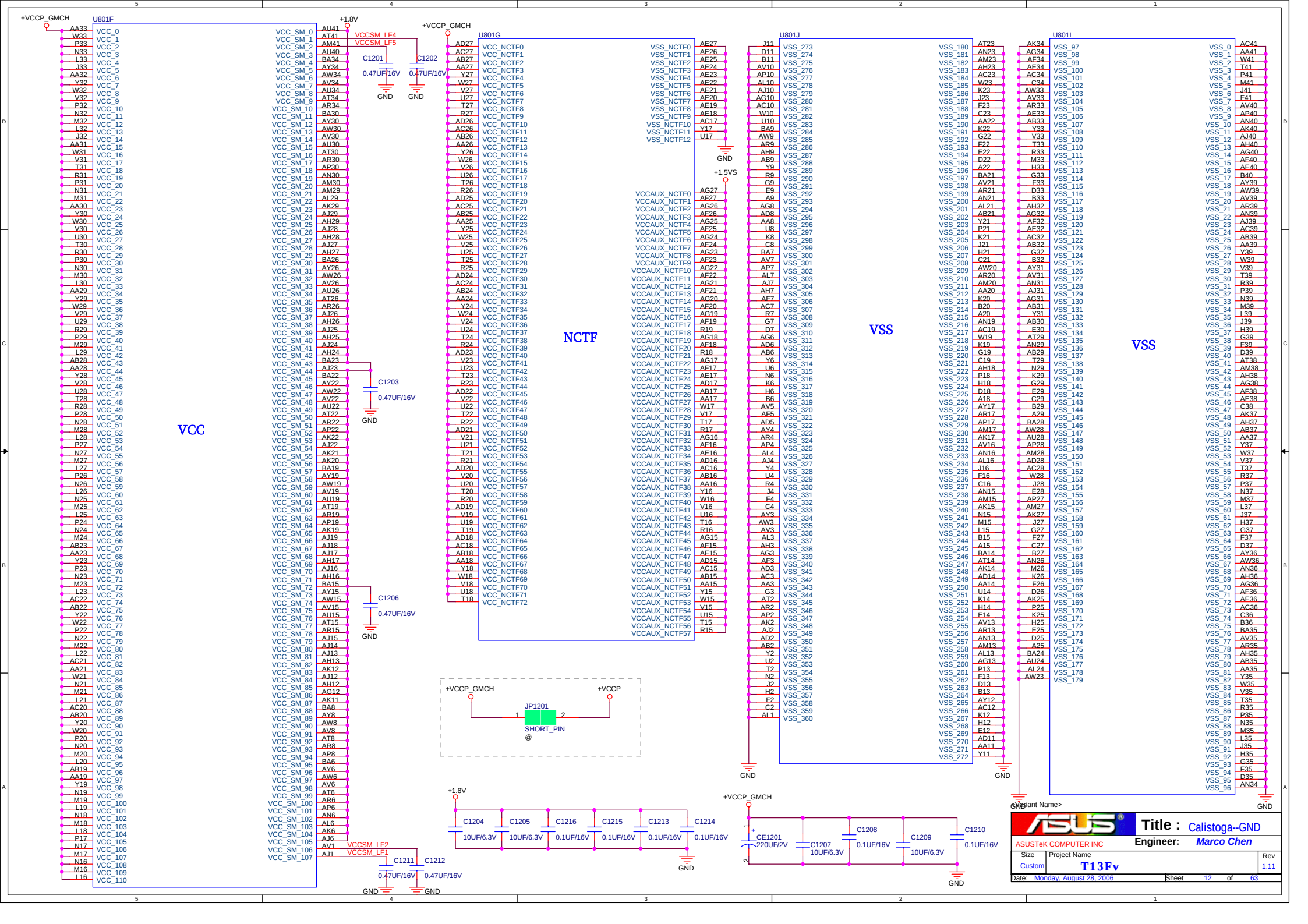
ASUSTeK COMPUTER INC

Title : Calistoga--POWER

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 11 of 63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VCC_4
VCC_5
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VCC_9
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VCCSM_LF5
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C1202
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GND
C1203
0.47UF/16V
C1206
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VCCSM_LF1
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C1212
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C1205
10UF/6.3V
C1216
0.1UF/16V
C1215
0.1UF/16V
C1213
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C1214
0.1UF/16V
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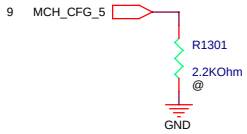
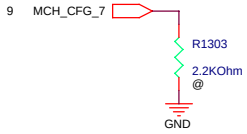
<Variant Name>
Title : Calistoga--GND
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size
Custom
Project Name
T13Fv
Rev
1.11
Date: Monday, August 28, 2006
Sheet 12 of 63



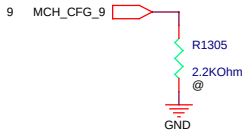

CFG5 : DMI STRAP

LOW = DMI X 2
***HIGH = DMI X 4 (Default)***



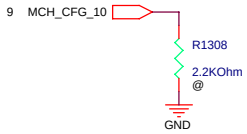

CFG7 : CPU STRAP

LOW = RESERVED
***HIGH = Mobile Yonah CPU (Default)***



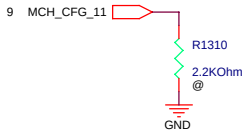

CFG9 : PCIE GRAPHIC LANE

**LOW = REVERSE LANE**
HIGH = NORMAL OPERATION (Default)




CFG10 : HOST PLL VCO SELECT

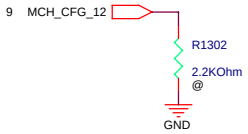
LOW = RESERVED
***HIGH = MOBILITY (Default)***




CFG11 : PSB 4x CLK ENABLE

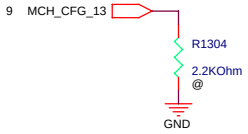
LOW = 4X ENABLED
***HIGH = 8X ENABLED (Default)***

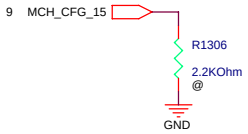
**CFG[17..3] have internal pullup resistors.**
**CFG[19..18] have internal pulldown resistors.**
**SDVOCRTL_DATA has internal pulldown resistors.**




CFG[13:12] : GMCH TEST MODE SELECT

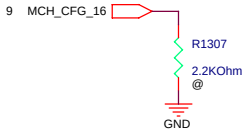
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
***11 = NORMAL OPERATION (Default)***



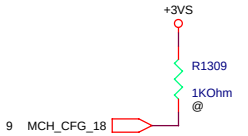

CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
***HIGH = Normal Operation (Default)***



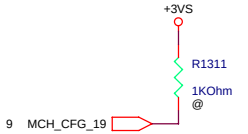

CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
***HIGH = Dynamic ODT Enabled (Default)***




CFG18 : GMCH Core Voltage Level

***LOW = 1.05V (Default)***
HIGH = 1.5V




CFG19 : DMI LANE REVERSAL

***LOW = NORMAL (Default)***
HIGH = LANES REVERSED

<Variant Name>

ASUSTeK COMPUTER INC

**Title :** Calistoga--Strap

**Engineer:** ***Marco Chen***

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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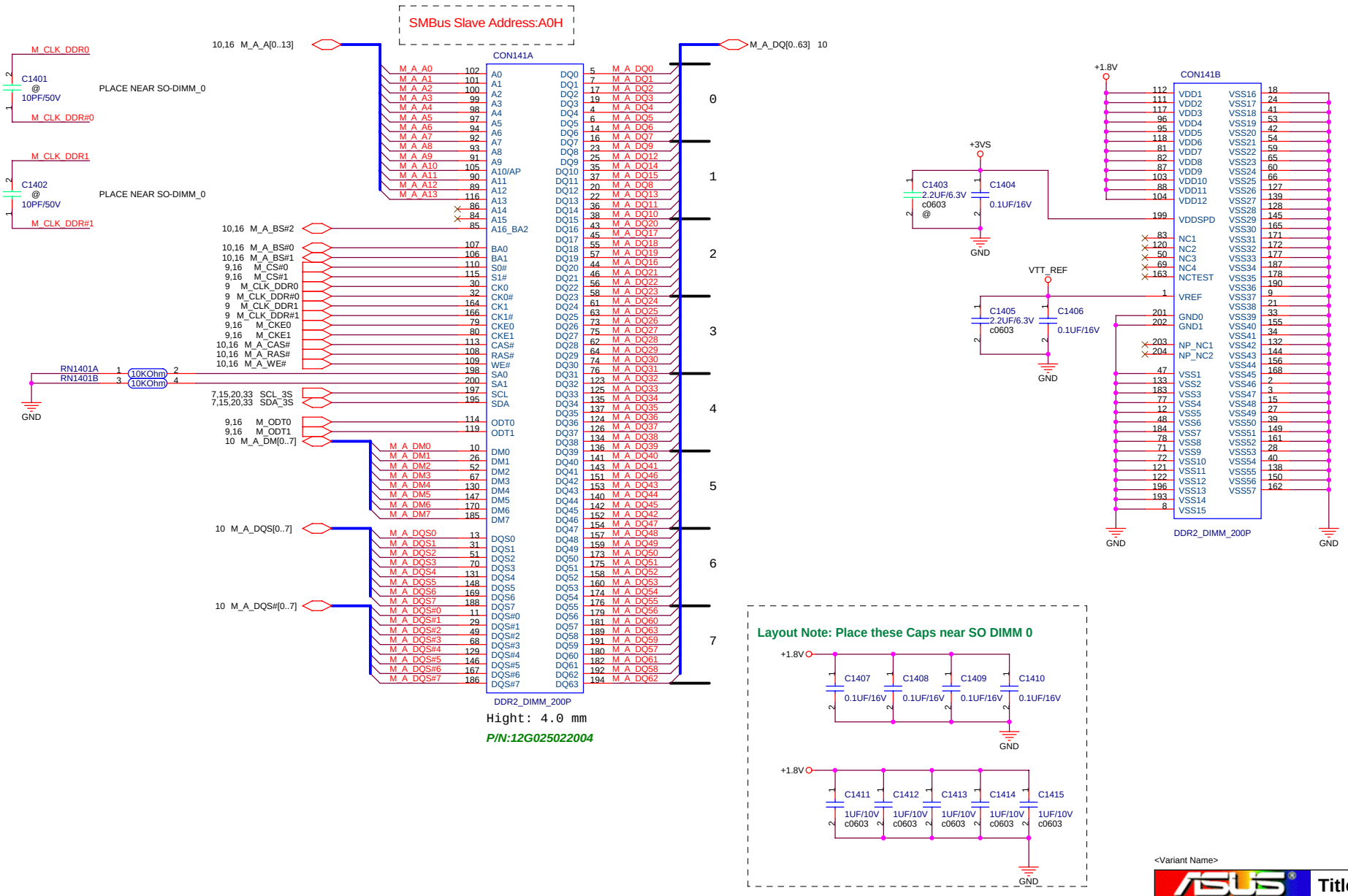
**DDR2 HAD SWAPED.**





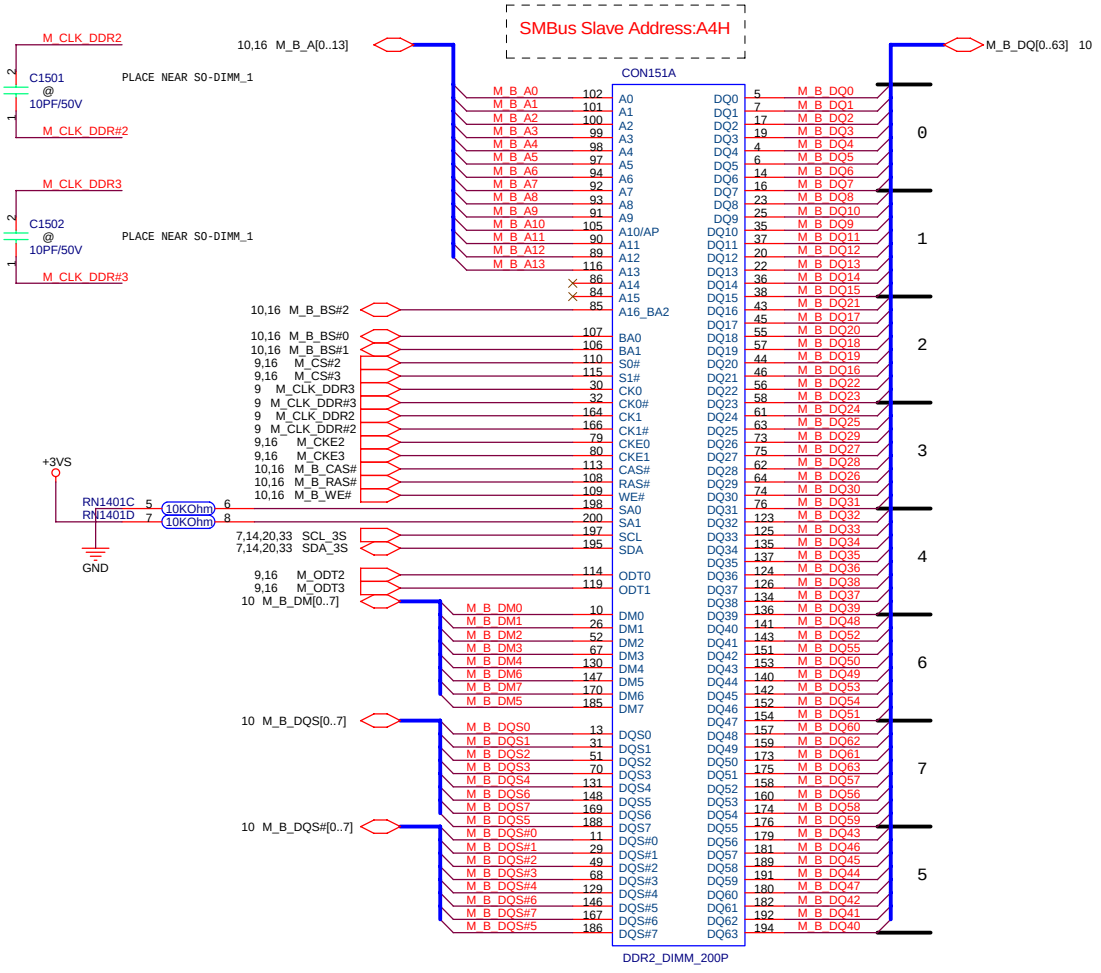





<Variant Name>

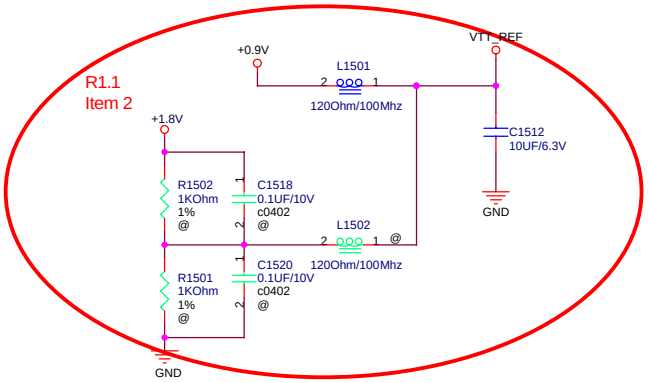
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DDR2 SO-DIMM_0 | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 14 of 63 | |

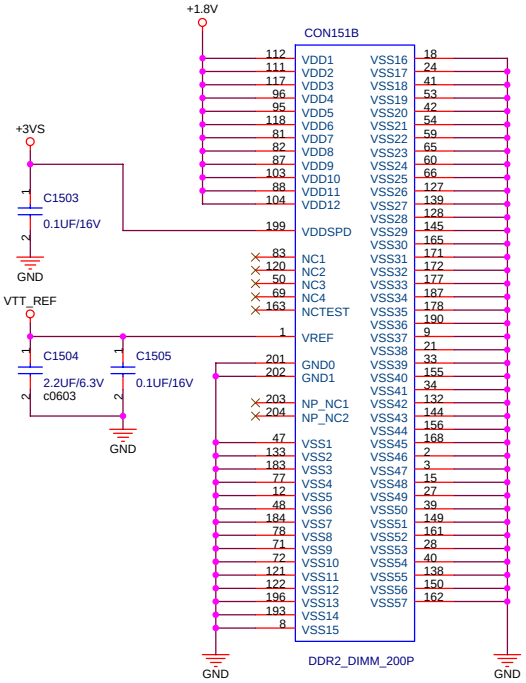
# DDR2 HAD SWAPED.

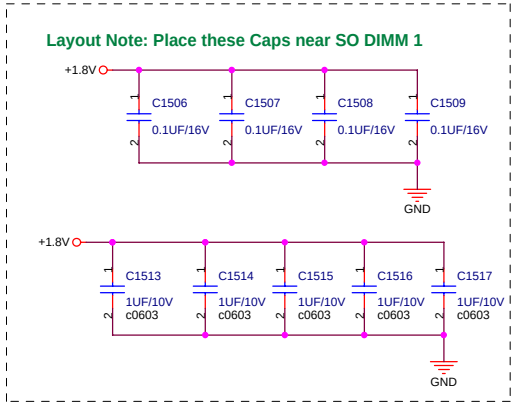



Hight: 9.2 mm

***P/N:12G025C22004***




<Variant Name>

ASUSTeK COMPUTER INC

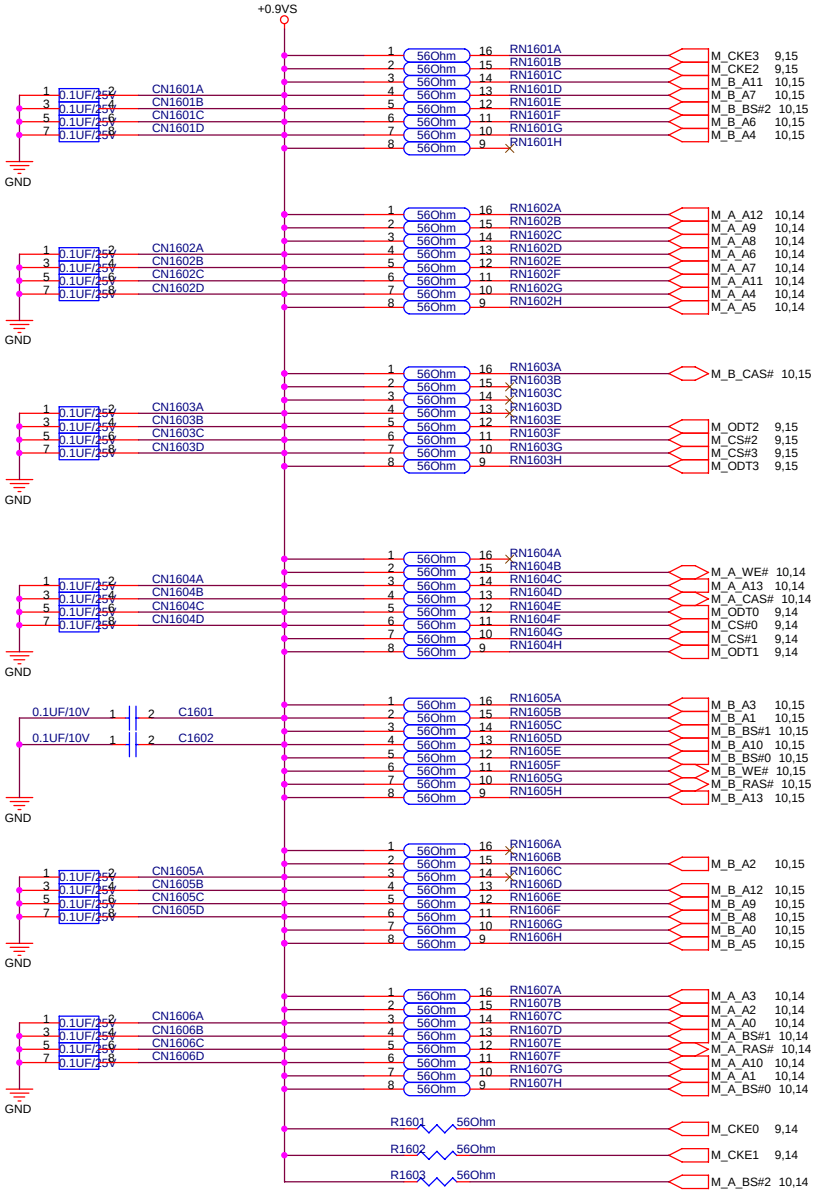
Title : DDR2 SO-DIMM_1

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 15 of 63

# DDR2 HAD SWAPED.



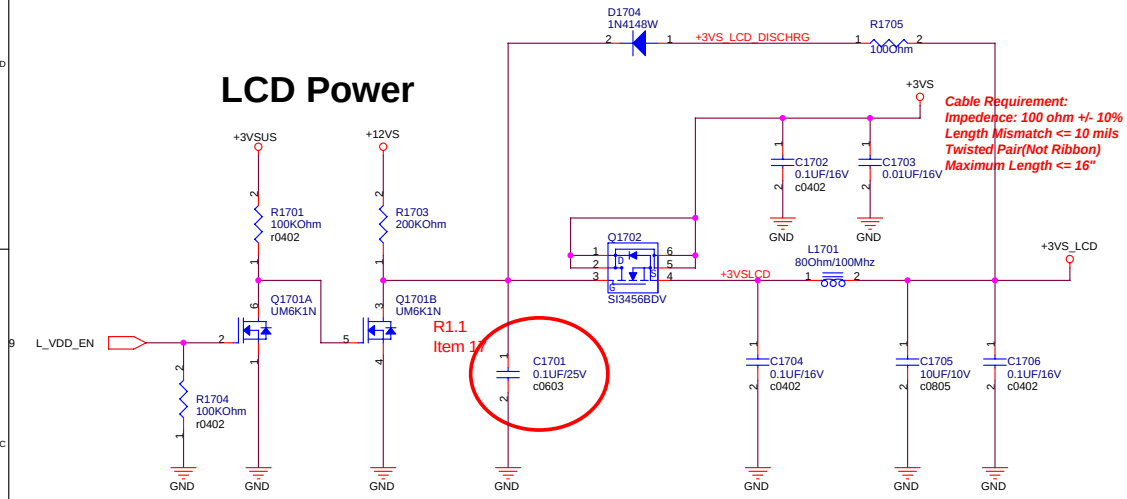

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DDR2 TERMINATION | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 16 of 63 | |

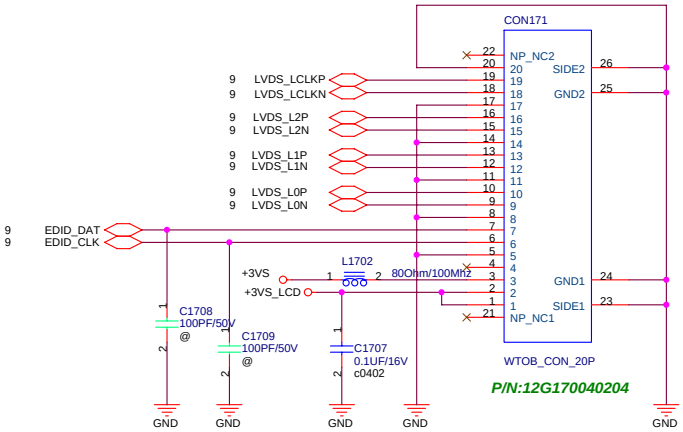
# LCD Backlight Control

## LCD Power

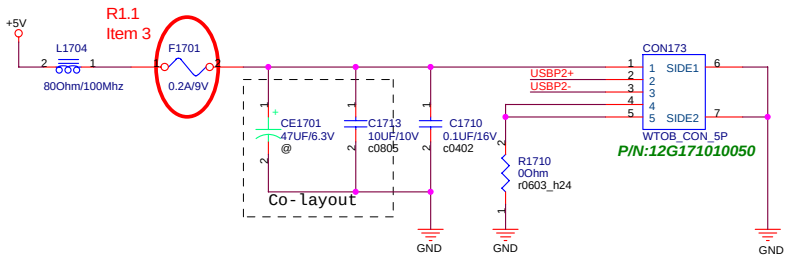


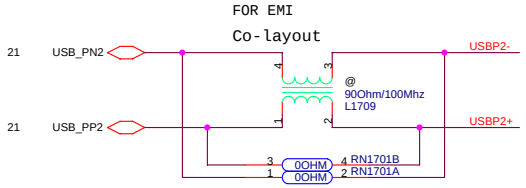

PR_NOTE: Change R1703 to 200K ohm, C1701 to 0.1uF/25V, D1704 to BAT54C and R1705 to 100ohm

# LCD LVDS Interface

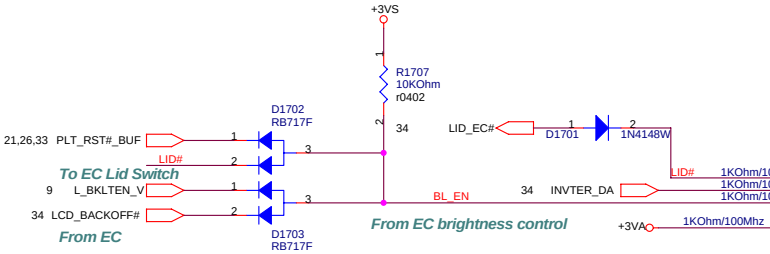


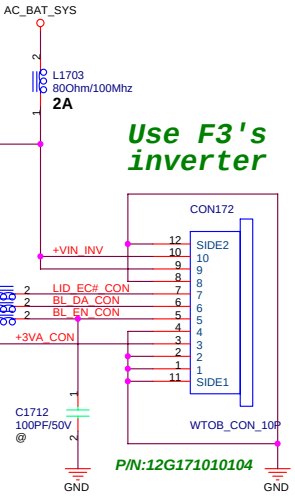

# CCD connecter



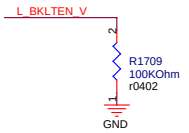




# Inverter connecter



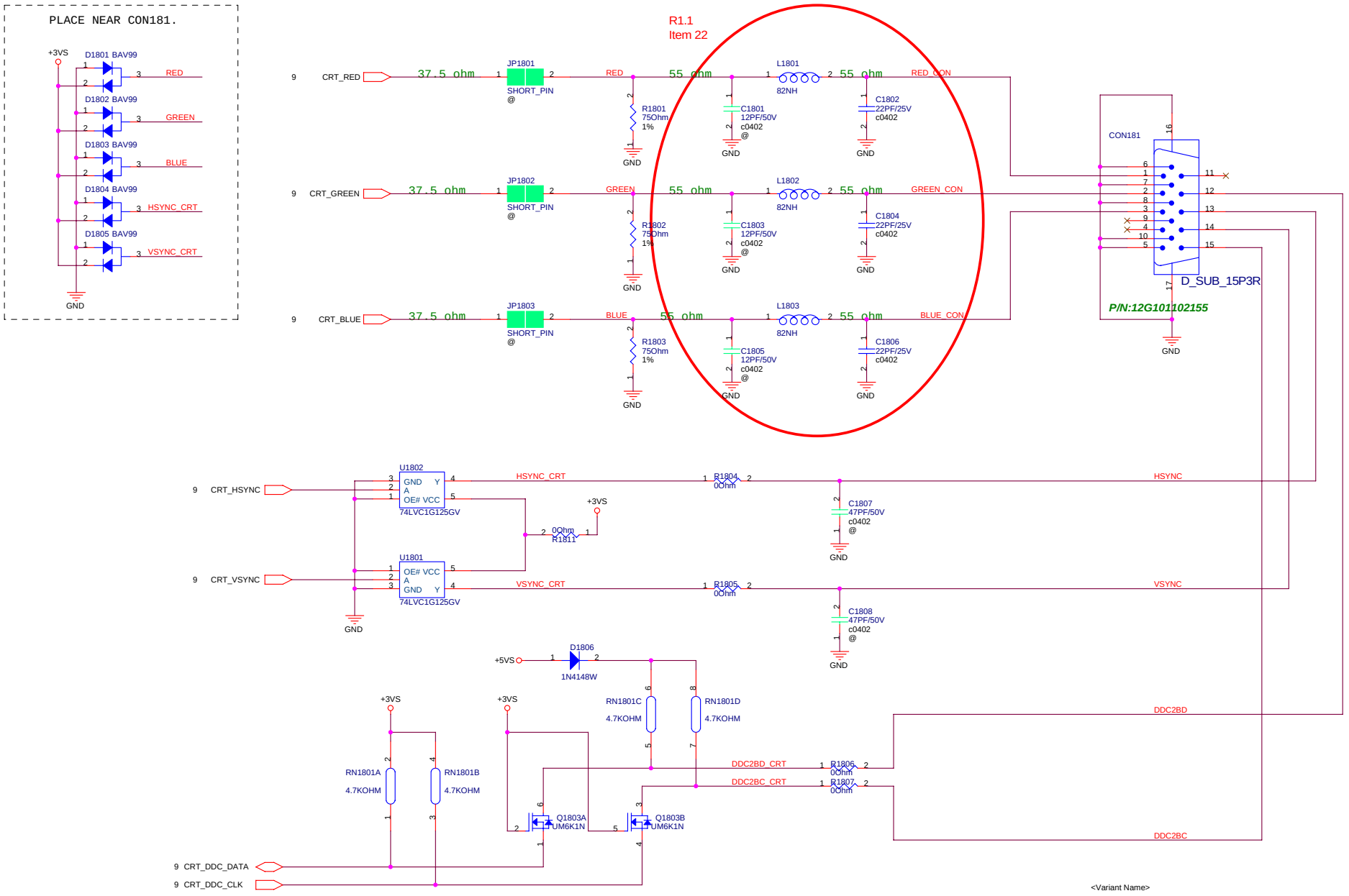

**BIOS**
**BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.**




<Variant Name>

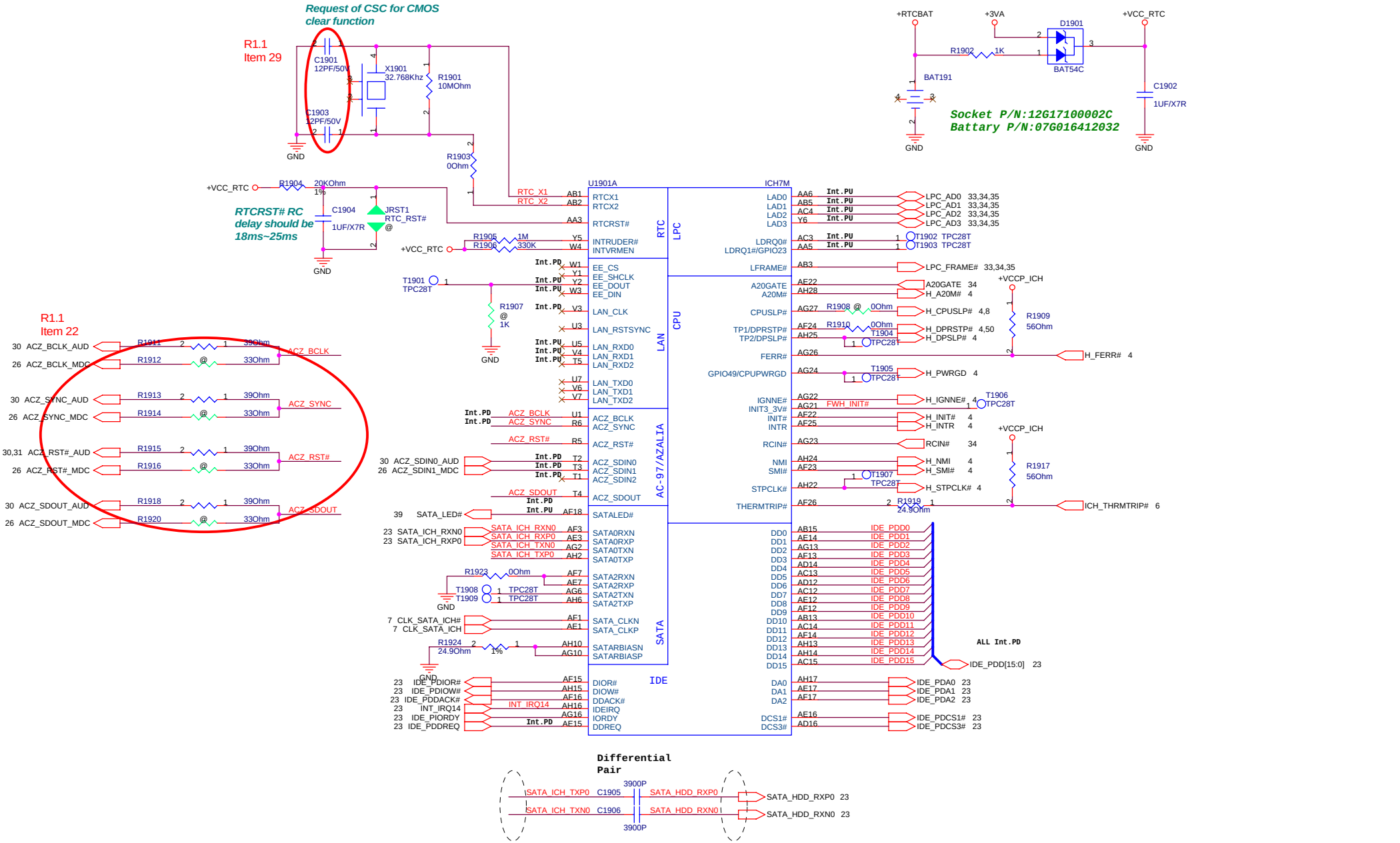
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : LVDS & INVERTER | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 17 of 63 | |

# CRT




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CRT CONN | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 18 of 63 | |




<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7M (1)

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 19 of 63

*To new card check power plane*

Clock Generator
DDR2 SO-DIMM

U1901C

7,14,15,33 SCL_3S
7,14,15,33 SDA_3S
LINKALERT#
SM_LINK0
SM_LINK1
RING#
30 SPKR_ICH
PM_SUS_STAT#
+3VSUS
9 PM_BMBUSY#
SMB_ALERT#
7 STP_PCI#
7 STP_CPU#
25 BT_ON#
26 WLAN_ON#
35 MEMROM/YONAH#
27 PM_CLKRUN#
7 CPU_Select
26,29,33 PCIE_WAKE#
27,34 INT_SERIRQ
34 PM_THRM#
VRMPWRGD
34,50,60 VRM_PWRGD
39 BT_LED_EN
34 EXTSMI#

C22 SMBCLK
B22 SMBDATA
A26 LINKALERT#
B25 SMLINK0
A25 SMLINK1
SMB

A28 RI#
A19 SPKR
A27 SUS_STAT#
A22 SYS_RST#
AB18 GPIO0/BM_BUSY#
B23 SMBALERT#/GPIO11
AC20 GPIO18/STPPCI#
AF21 GPIO20/STPCPU#
A21 GPIO26
B21 GPIO27
E23 GPIO28
AG18 GPIO32/CLKRUN#
AC19 GPIO33/AZ_DOCK_EN#
U2 GPIO34/AZ_DOCK_RST#
F20 WAKE#
AH21 SERIRQ
AE20 THRM#
AD22 VRMPWRGD
AC21 GPIO6
AC18 GPIO7
E21 GPIO8
SYS GPIO
GPIO

ICH7M

GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
SATA GPIO

AE19 T2009 TPC28T
AH18 T2010 TPC28T
AH19 T2008 TPC28T
AE19 PCB_ID0

CLK14
CLK48
SUSCLK
Clocks

AC1
B2
C20 SUS_CLK T2005 TPC28T
CLK_ICH14 7
CLK_USB48 7

C2001 @ 10PF/50V
C2002 @ 10PF/50V
GND GND

SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
MGT Power

B24 SUSB# 34
D23 SUSC# 34
F22 T2002 TPC28T
AA4 ICH7_PWROK 9,27,34
AC22 Int.PD POWER PM_DPRSLPVR 50
C21 BAT_LL# 34
C23 Int.PU T2003 TPC28T PM_PWRBTN# 34
C19 ICH_LAN_RST# R2036 0Ohm
Y4 PM_RSMRST# 34

R2002 10KOhm GND
R2030 10KOhm GND

GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39

E20 T2016 TPC28T
A20 T2011 TPC28T
F19 KBC_SCI# 34
E19 T2004 TPC28T
R4 T2012 TPC28T
E22 802_LED_EN 39
R3 MSK_PCIRST 21
D20 Int.PU CB_SD# 27
AD21 T2013 TPC28T
AD20 PCB_ID1
AE20 PCB_ID2

R1.1
Item 12

T2018 TPC28T
T2014 TPC28T
T2001 TPC28T
T2017 TPC28T

VRM_PWRGD
Pull Hi 100K
+3Vs at power
circuit

POWER

+3VS

RP2001A 21,27 PCI_SERR#
RP2001B 21,27 PCI_DEVSEL#
RP2001C 21,27 PCI_TRDY#
RP2001D 21 PCI_REQ#4
RP2001E 21,27 PCI_FRAME#
RP2001F 21,27 PCI_STOP#
RP2001G 21,27 PCI_REQ#1
RP2001H 21 PCI_REQ#2

RP2002A
RP2002B 21 PCI_REQ#3
RP2002C 21 PCI_LOCK#
RP2002D
RP2002E 21 PCI_INTH#
RP2002F 21 PCI_INTF#
RP2002G 21 PCI_INTE#
RP2002H 21 PCI_INTG#

RP2003A 21 PCI_INTA#
RP2003B 21,27 PCI_INTB#
RP2003C 21 PCI_INTC#
RP2003D 21,27 PCI_INTD#
RP2003E 21 PCI_REQ#0
RP2003F 21,27 PCI_IRDY#
RP2003G 21 PCI_REQ#5
RP2003H 21,27 PCI_PERR#

8.2KOhm 5 10

ICH7_PWROK R2006 @ 0Ohm VRMPWRGD

+3VSUS

RING# R2008 10KOhm
SMB_ALERT# RN2001A 1 2 10KOhm
SM_LINK0 RN2001B 3 4 10KOhm
SM_LINK1 RN2001C 5 6 10KOhm
LINKALERT# RN2001D 7 8 10KOhm
BAT_LL# R2014 10KOhm
WLAN_ON# R2016 10KOhm
PCIE_WAKE# R2021 2.2KOhm
PM_SUS_STAT# R2025 @ 10KOhm
BT_ON# R2028 10KOhm

+3VS

R2009 10KOhm
R2010 10KOhm @
R2011 10KOhm @
PCB_ID0
PCB_ID1
PCB_ID2
R2017 10KOhm @
R2018 10KOhm
R2019 10KOhm
GND GND GND

INT_SERIRQ R2013 10KOhm
STP_PCI# R2015 @ 10KOhm
STP_CPU# R2020 @ 10KOhm
PM_CLKRUN# R2023 10KOhm

+3VS

SCL_3S R2005 2.2KOhm
SDA_3S R2007 2.2KOhm
PM_THRM# R2026 10KOhm

+3VSUS

KBC_SCI# R2034 10KOhm
EXTSMI# R2035 10KOhm

R1.1
Item 12

MEMROM/YONAH# R2033 10KOhm
802_LED_EN R2031 10KOhm
BT_LED_EN R2032 10KOhm
GND

<Variant Name>

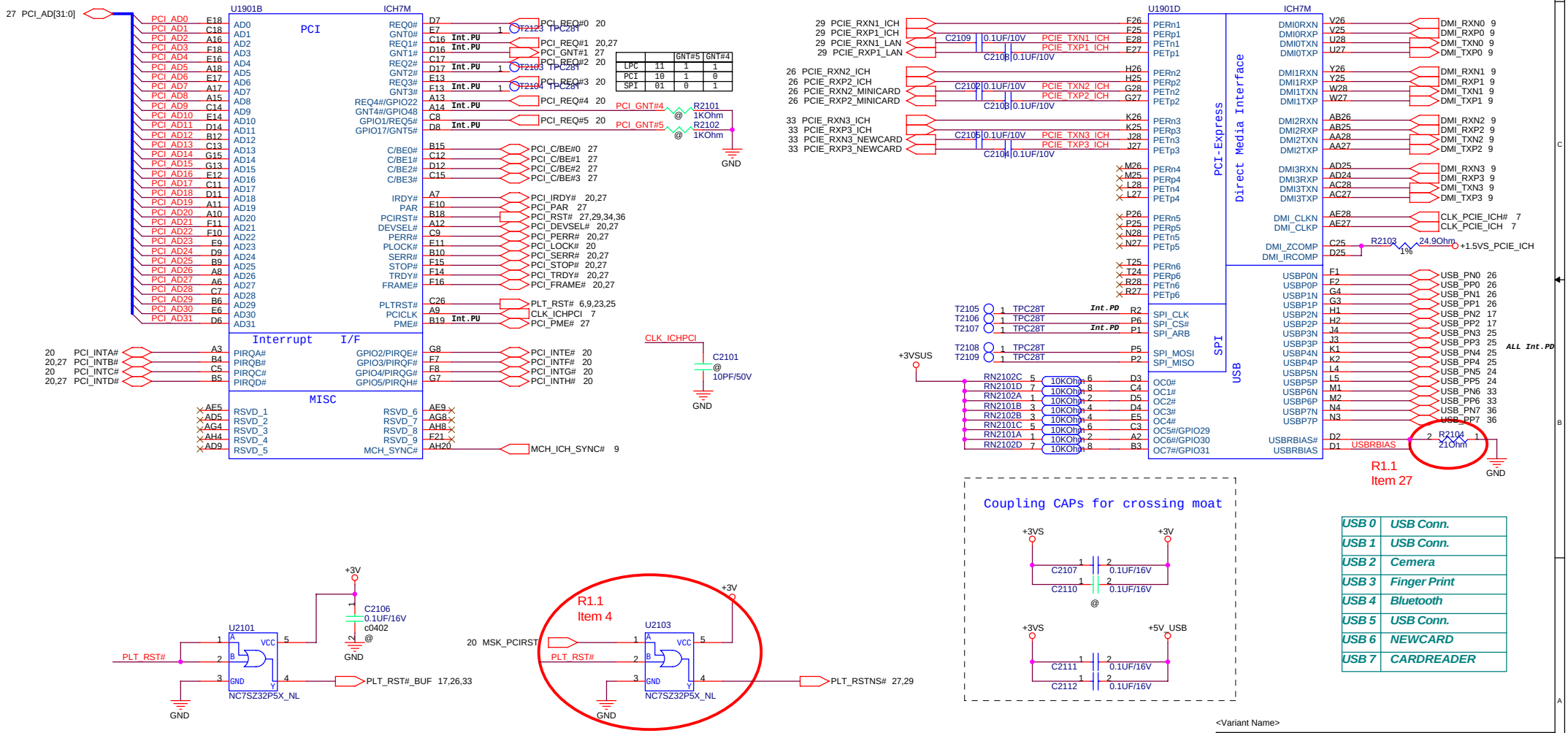
ASUSTeK COMPUTER INC

Title : ICH7M (2)

Engineer: Marco Chen

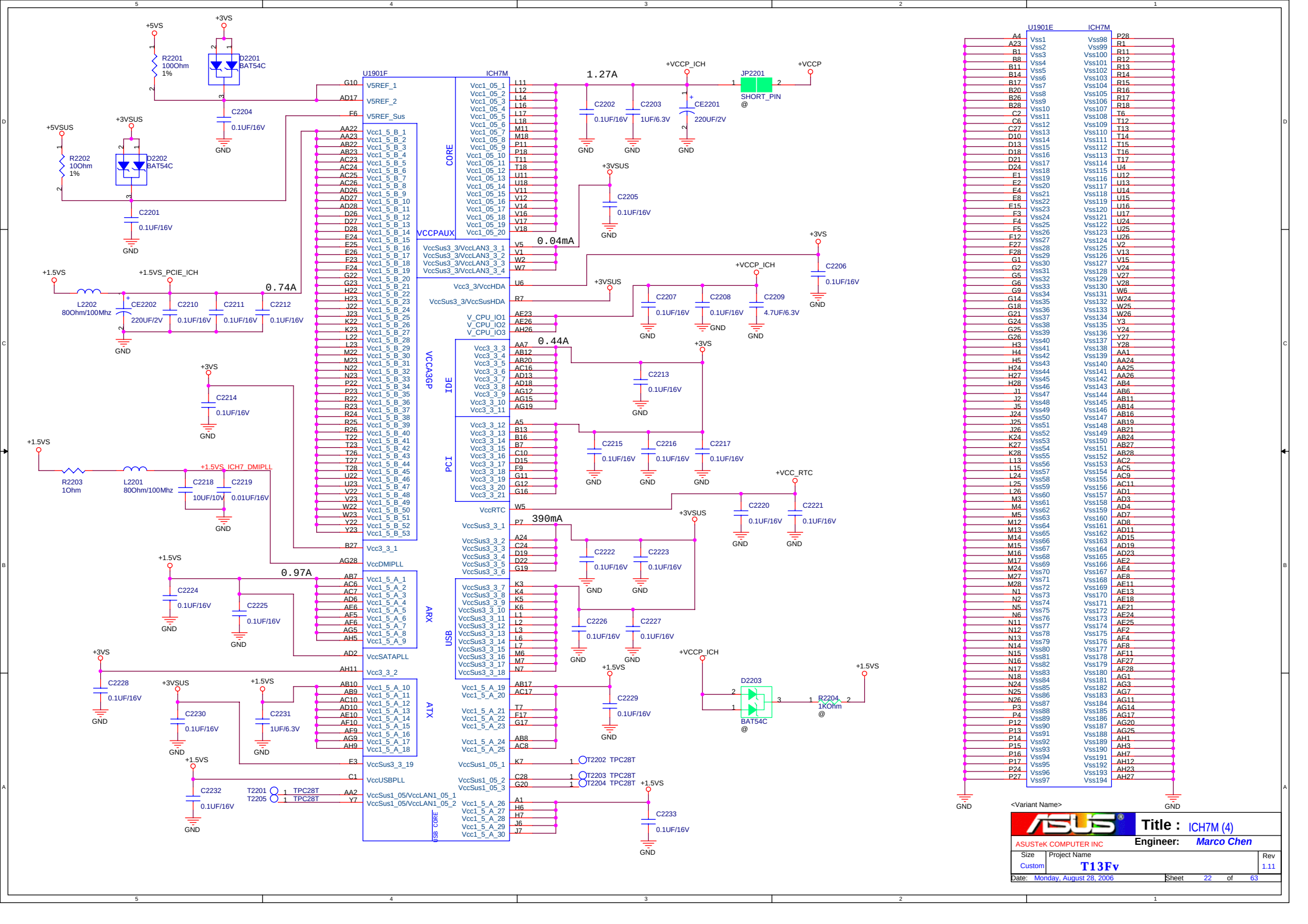
| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 20 of 63

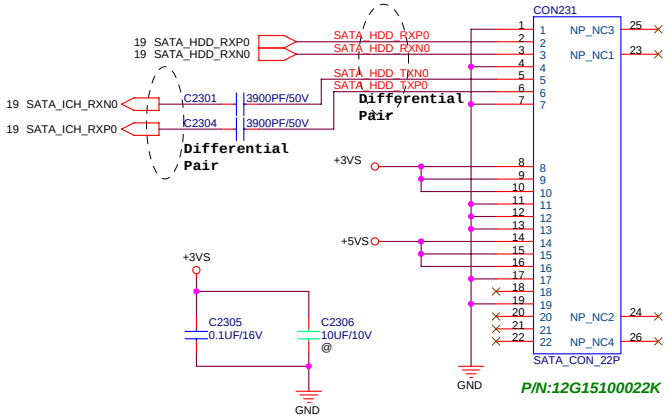


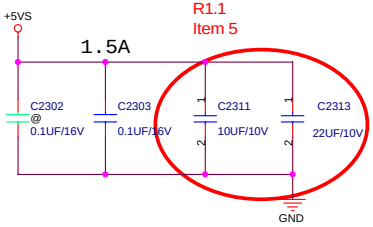

| | | GNT#5 | GNT#4 |
|---|---|---|---|
| LPC | 11 | 1 | 1 |
| PCI | 10 | 1 | 0 |
| SPI | 01 | 0 | 1 |

| | |
|---|---|
| USB 0 | USB Conn. |
| USB 1 | USB Conn. |
| USB 2 | Camera |
| USB 3 | Finger Print |
| USB 4 | Bluetooth |
| USB 5 | USB Conn. |
| USB 6 | NEWCARD |
| USB 7 | CARDREADER |

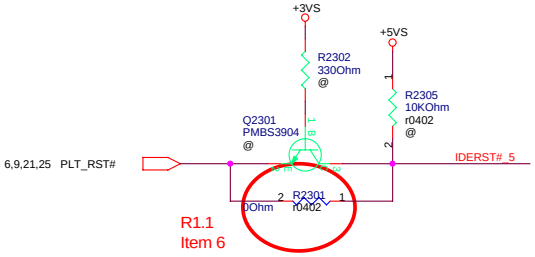

U1901F
ICH7M
U1901E
R2201 100Ohm 1%
D2201 BAT54C
C2204 0.1UF/16V
R2202 10Ohm 1%
D2202 BAT54C
C2201 0.1UF/16V
L2202 80Ohm/100Mhz
CE2202 220UF/2V
C2210 0.1UF/16V
C2211 0.1UF/16V
C2212 0.1UF/16V
0.74A
C2214 0.1UF/16V
R2203 1Ohm
L2201 80Ohm/100Mhz
C2218 10UF/10V
C2219 0.01UF/16V
C2224 0.1UF/16V
C2225 0.1UF/16V
0.97A
C2228 0.1UF/16V
C2230 0.1UF/16V
C2231 1UF/6.3V
C2232 0.1UF/16V
T2201 TPC28T
T2205 TPC28T
1.27A
C2202 0.1UF/16V
C2203 1UF/6.3V
CE2201 220UF/2V
JP2201 SHORT_PIN
C2205 0.1UF/16V
0.04mA
C2206 0.1UF/16V
C2207 0.1UF/16V
C2208 0.1UF/16V
C2209 4.7UF/6.3V
0.44A
C2213 0.1UF/16V
C2215 0.1UF/16V
C2216 0.1UF/16V
C2217 0.1UF/16V
390mA
C2220 0.1UF/16V
C2221 0.1UF/16V
C2222 0.1UF/16V
C2223 0.1UF/16V
C2226 0.1UF/16V
C2227 0.1UF/16V
C2229 0.1UF/16V
C2233 0.1UF/16V
D2203 BAT54C
R2204 1KOhm
T2202 TPC28T
T2203 TPC28T
T2204 TPC28T
+5VS
+3VS
+5VSUS
+3VSUS
+1.5VS
+1.5VS_PCIE_ICH
+1.5VS_ICH7_DMIPLL
+VCCP_ICH
+VCCP
+VCC_RTC
GND
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
USB
ATX
USB CORE
<Variant Name>
Title : ICH7M (4)
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 22 of 63

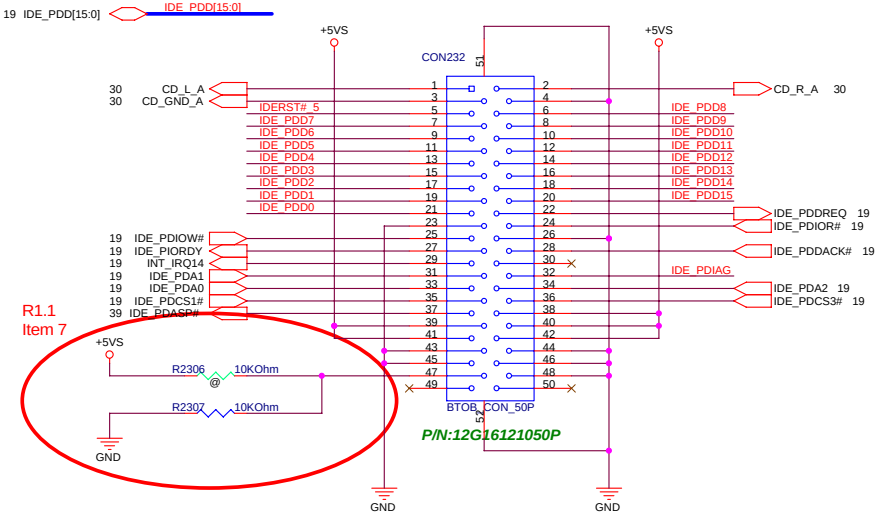
# SATA HDD CON

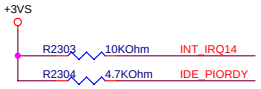


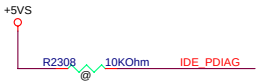




# PATA ODD CON

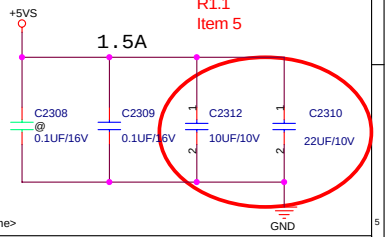



*Normal type*
*High: Slave*
*Low : Master*




<Variant Name>

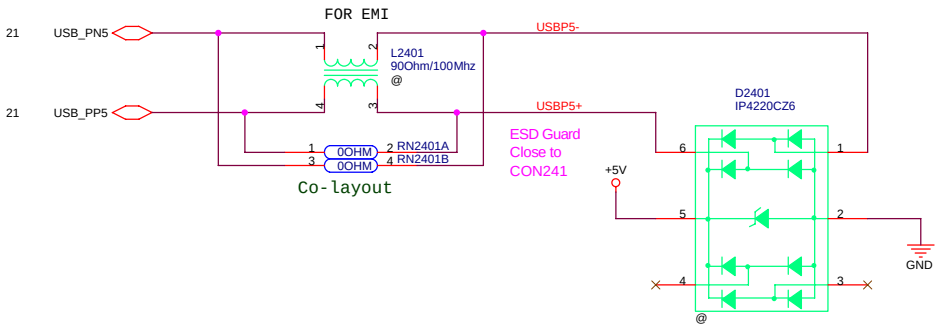
Title : HDD & ODD

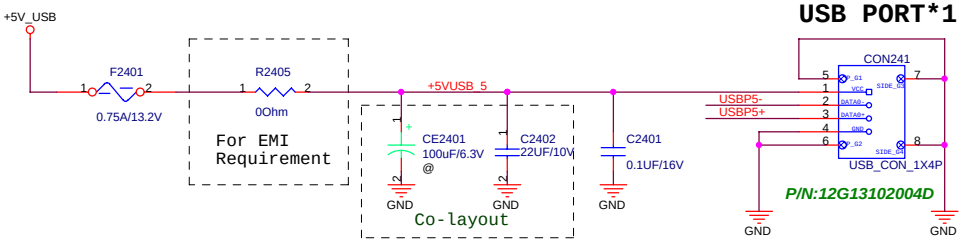
ASUSTeK COMPUTER INC

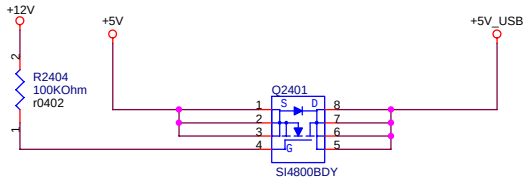
Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 23 of 63




<Variant Name>

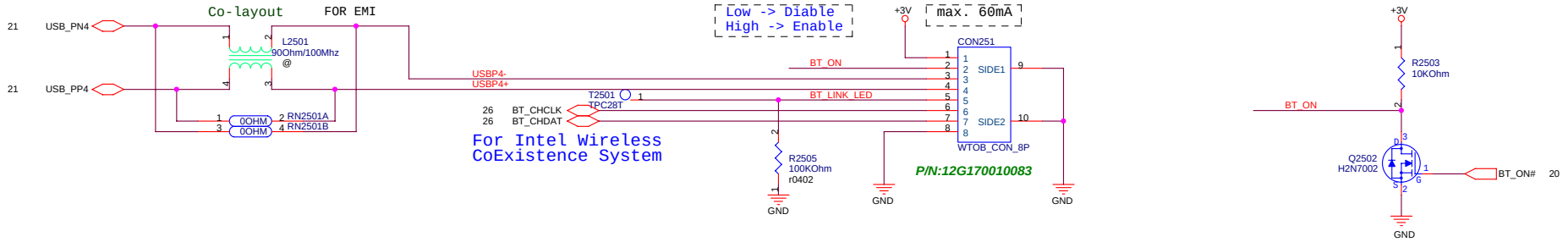
ASUSTeK COMPUTER INC

Title : USB PORT

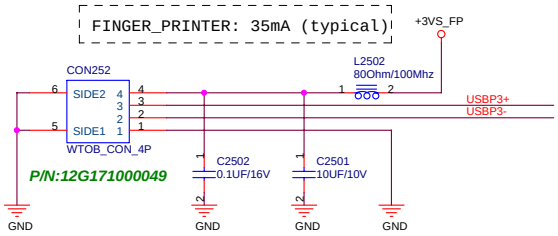
Engineer: Marco Chen

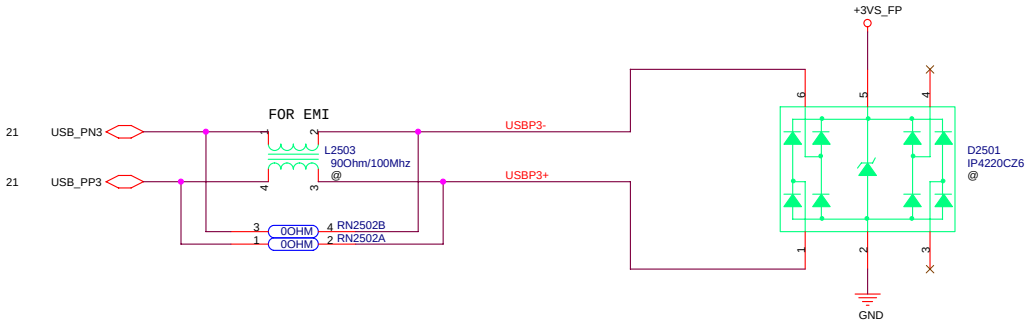
| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

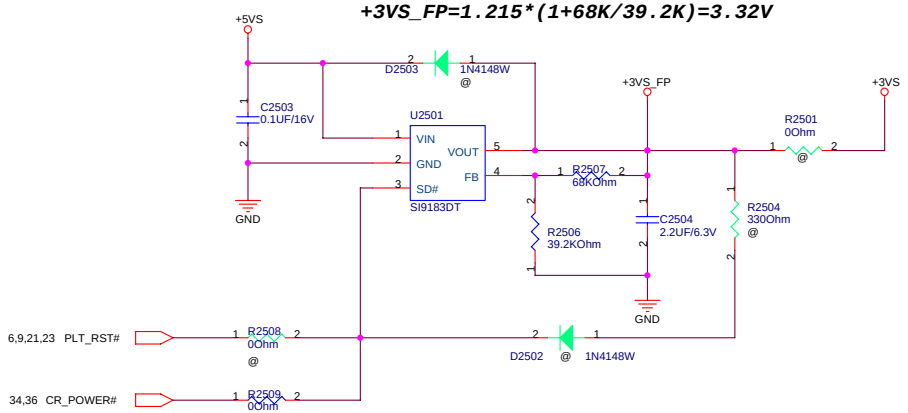
Date: Monday, August 28, 2006 Sheet 24 of 63




## Finger Printer




<Variant Name>

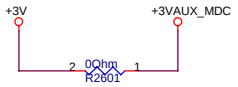
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : BT & FP | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 25 of 63 | |

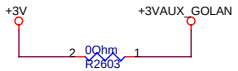
**POWER CONSUMPTION:**
**+3VS: +3.003V~+3.597V**
**Max= 750 mA**

**+1.5VS:+1.425V~+1.575V**
**Max= 375 mA**

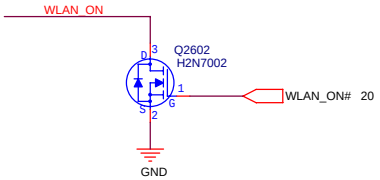
**+3VAUX_GOLAN:+3.003V~+3.597V**
**Max= 250 mA**

**+3VAUX_MDC:+3.003V~+3.597V**
**Max= 300 mA**




**Intel SPEC(18780):Internal**
**Pull UP 110Kohm**



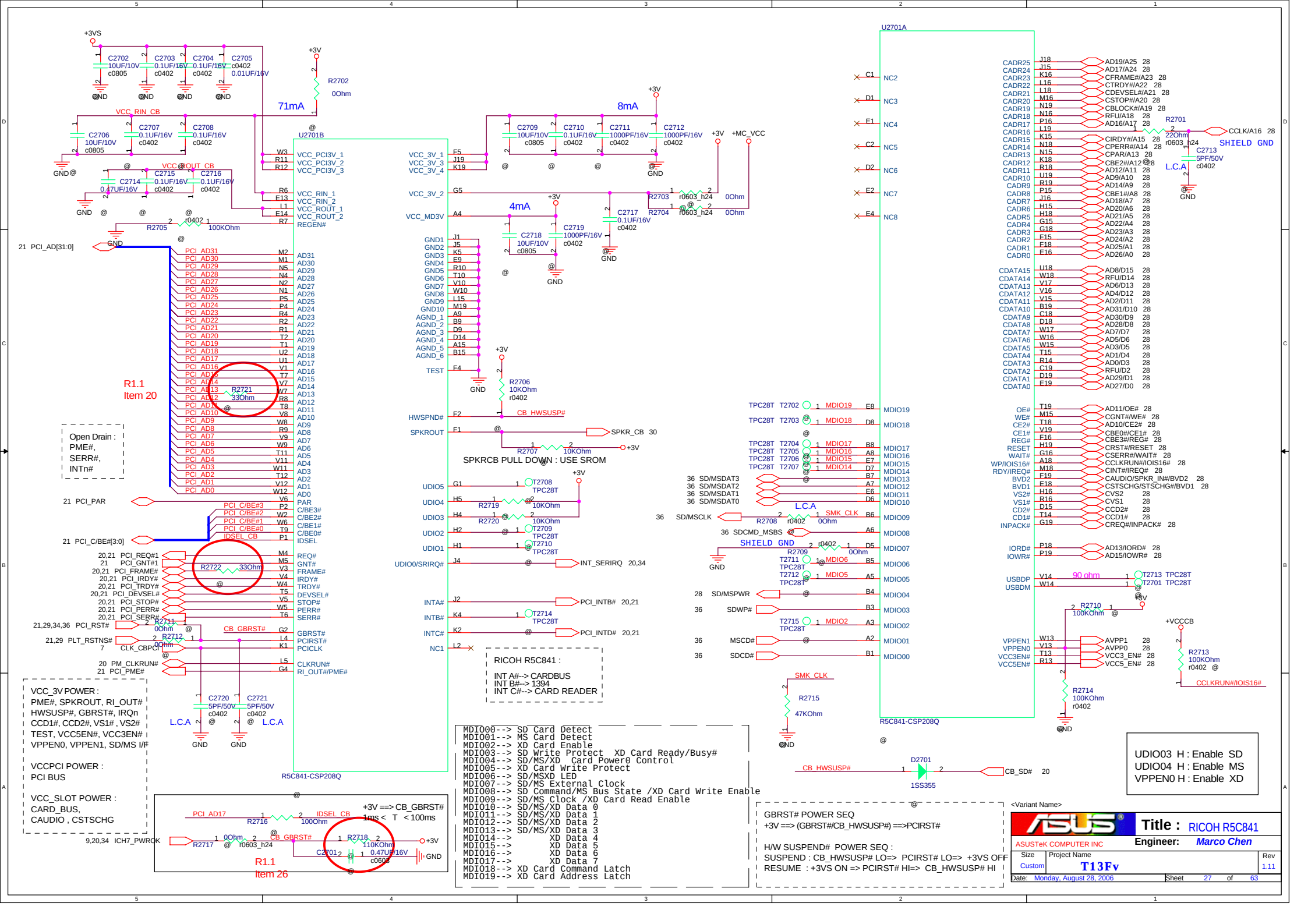


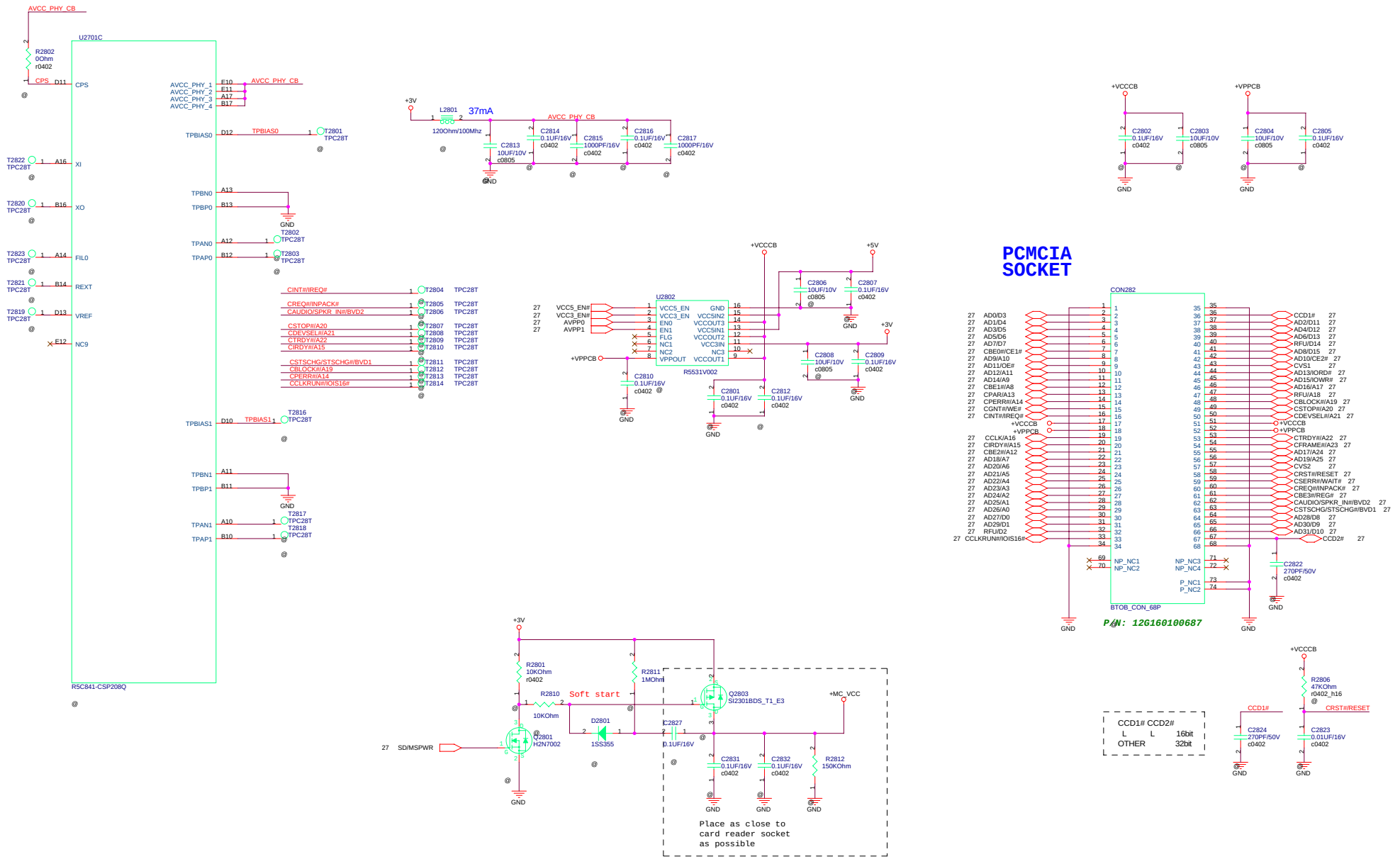


***P/N:12G061200504***

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : B TO B CONN(M) | |
| | Engineer: *Marco Chen* | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 26 of 63 | |


U2701A
U2701B
R5C841-CSP208Q
71mA
8mA
4mA
R1.1
Item 20
R1.1
Item 26
Open Drain :
PME#,
SERR#,
INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
+3V ==> CB_GBRST#
1ms < T < 100ms
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Marco Chen
Project Name T13Fv
Size Custom
Rev 1.11
Date: Monday, August 28, 2006
Sheet 27 of 63




<Variant Name>

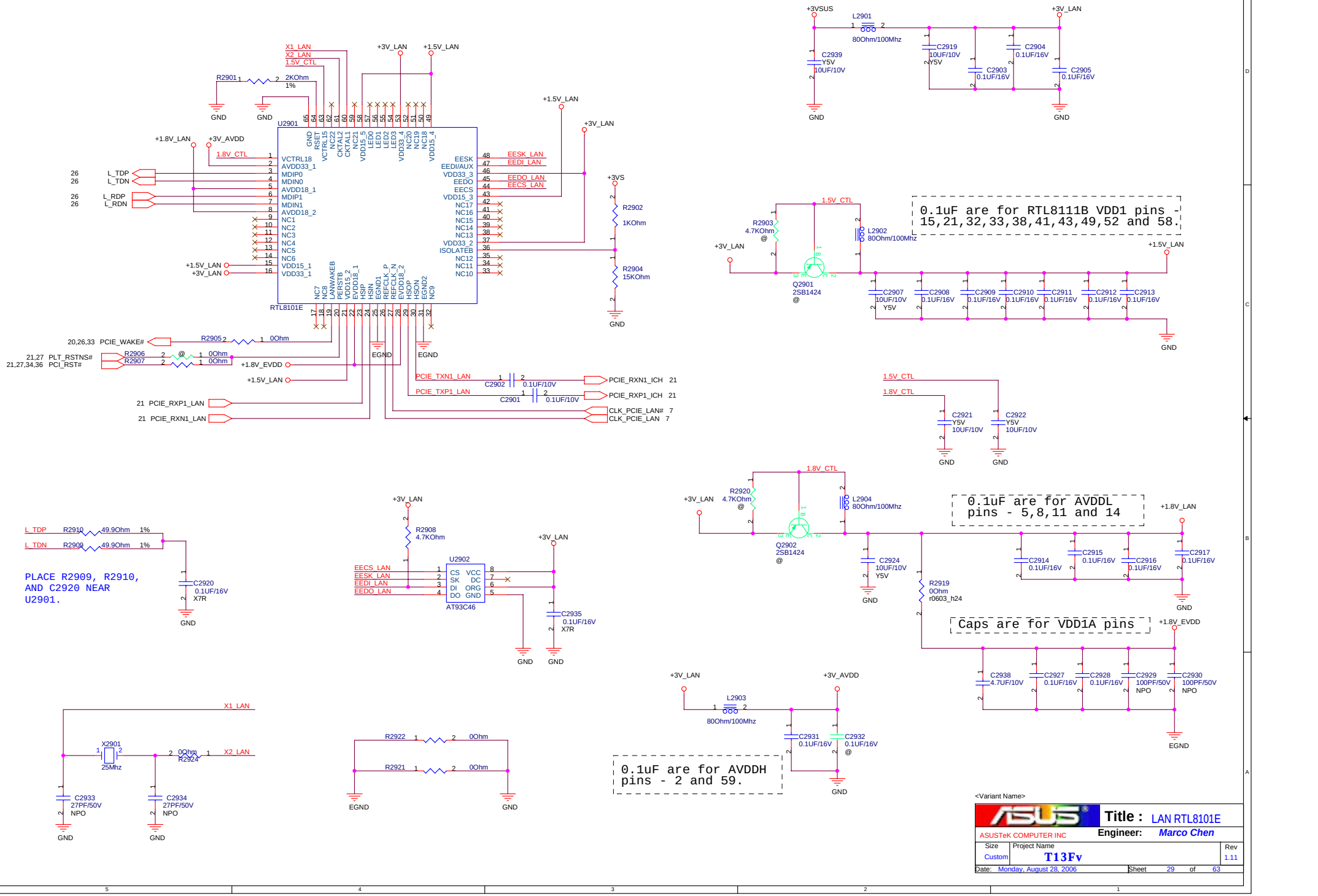
ASUSTeK COMPUTER INC

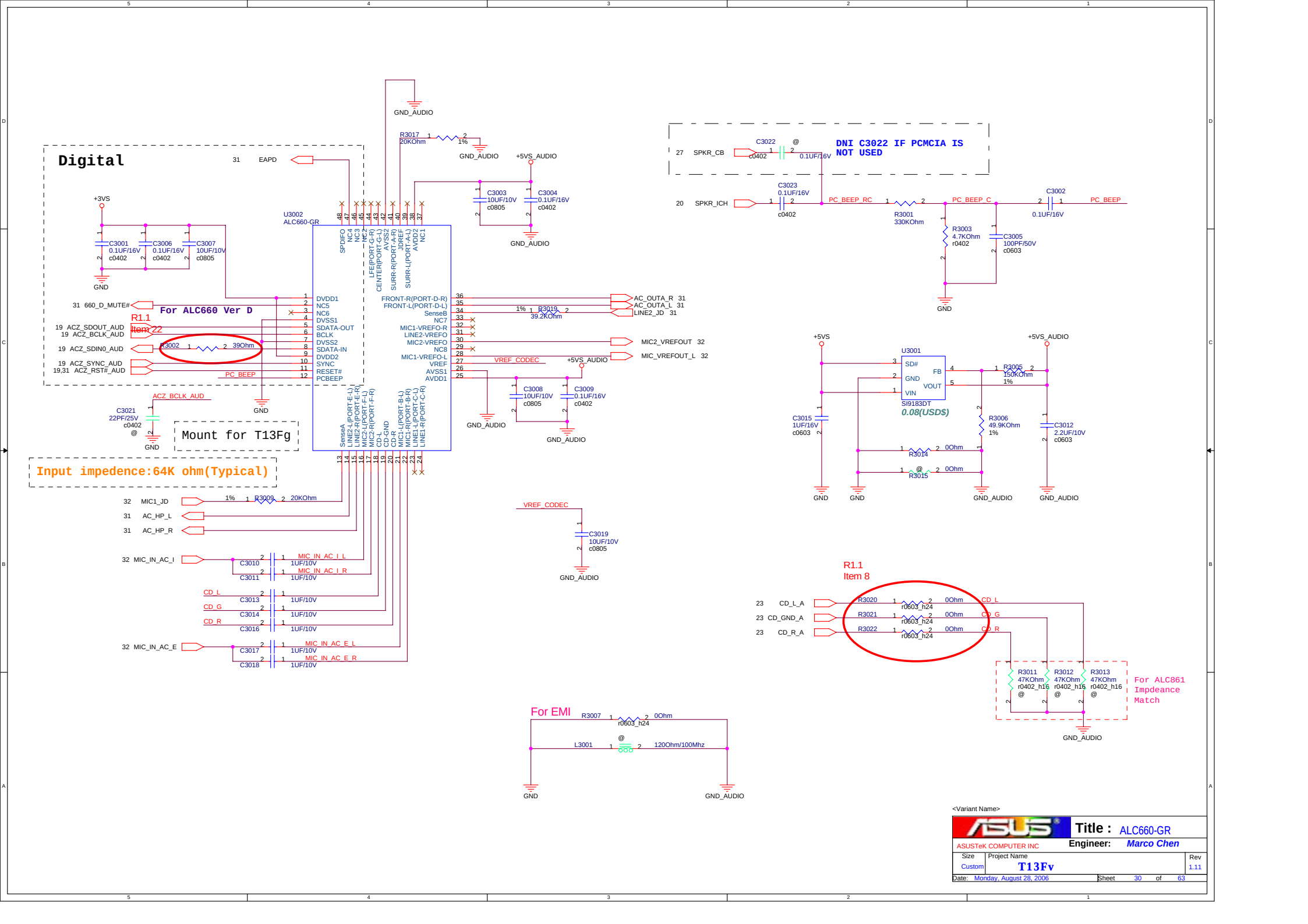
Title : PCMCIA&3IN1 SOCKET

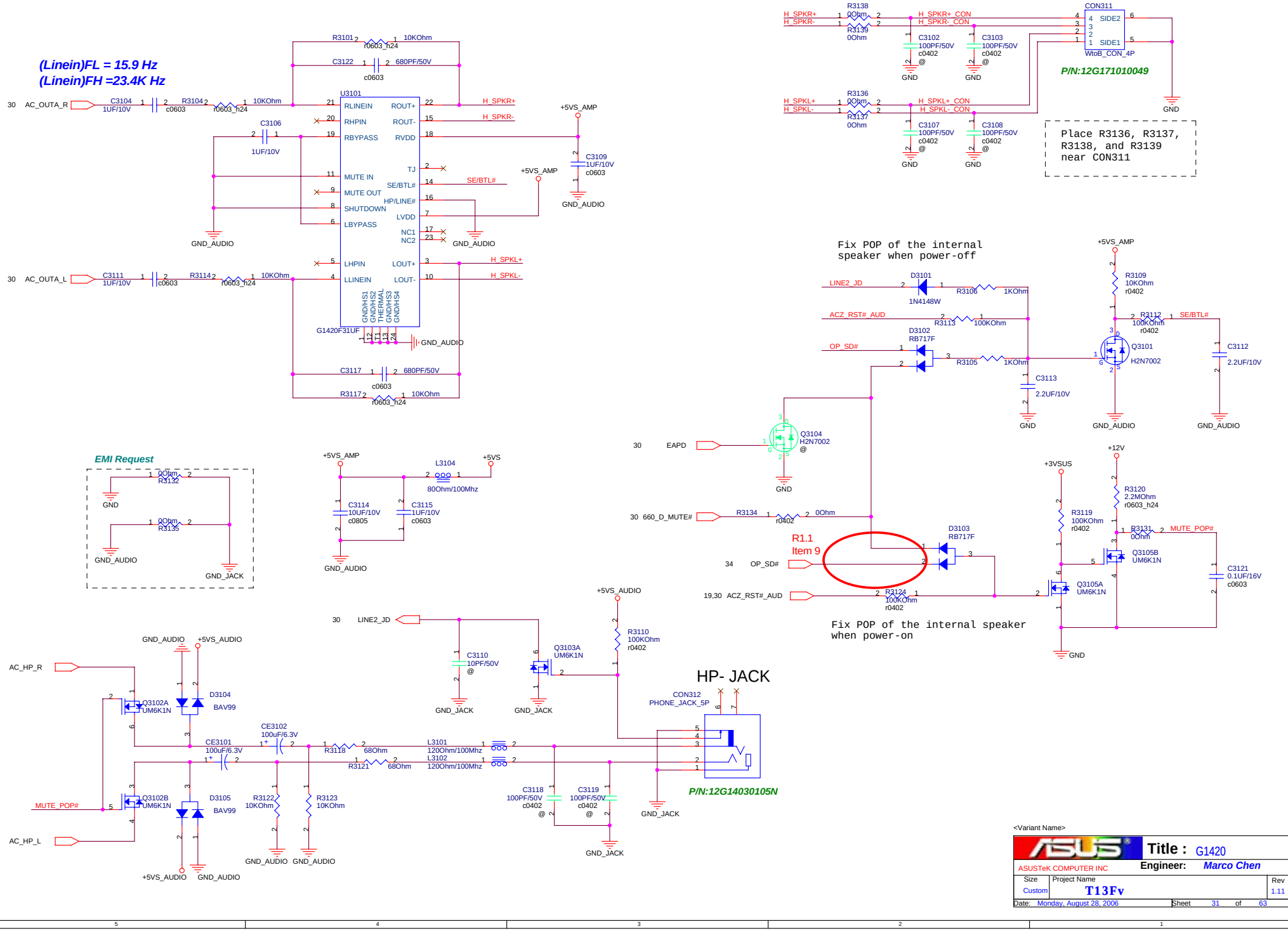
Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| C | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 28 of 63


X1_LAN
X2_LAN
1.5V_CTL
+3V_LAN
+1.5V_LAN
R2901 2KOhm 1%
GND
U2901
RTL8101E
+1.8V_LAN
+3V_AVDD
1.8V_CTL
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
NC1
NC2
NC3
NC4
NC5
NC6
VDD15_1
VDD33_1
L_TDP
L_TDN
L_RDP
L_RDN
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
VDD15_3
NC17
NC16
NC15
NC14
NC13
VDD33_2
ISOLATEB
NC12
NC11
NC10
EESK_LAN
EEDI_LAN
EEDO_LAN
EECS_LAN
+3VS
R2902 1KOhm
R2904 15KOhm
20,26,33 PCIE_WAKE#
R2905 0Ohm
21,27 PLT_RSTNS#
21,27,34,36 PCI_RST#
R2906 0Ohm
R2907 0Ohm
+1.8V_EVDD
EGND
PCIE_TXN1_LAN
PCIE_TXP1_LAN
C2902 0.1UF/10V
C2901 0.1UF/10V
PCIE_RXN1_ICH 21
PCIE_RXP1_ICH 21
21 PCIE_RXP1_LAN
21 PCIE_RXN1_LAN
CLK_PCIE_LAN# 7
CLK_PCIE_LAN 7
+3VSUS
L2901 80Ohm/100Mhz
C2939 Y5V 10UF/10V
C2919 10UF/10V Y5V
C2903 0.1UF/16V
C2904 0.1UF/16V
C2905 0.1UF/16V
1.5V_CTL
R2903 4.7KOhm @
L2902 80Ohm/100Mhz
Q2901 2SB1424 @
0.1uF are for RTL8111B VDD1 pins 15,21,32,33,38,41,43,49,52 and 58.
C2907 10UF/10V Y5V
C2908 0.1UF/16V
C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2912 0.1UF/16V
C2913 0.1UF/16V
1.8V_CTL
C2921 Y5V 10UF/10V
C2922 Y5V 10UF/10V
R2920 4.7KOhm @
L2904 80Ohm/100Mhz
Q2902 2SB1424 @
0.1uF are for AVDDL pins - 5,8,11 and 14
C2924 10UF/10V Y5V
R2919 0Ohm r0603_h24
C2914 0.1UF/16V
C2915 0.1UF/16V
C2916 0.1UF/16V
C2917 0.1UF/16V
Caps are for VDD1A pins
C2938 4.7UF/10V
C2927 0.1UF/16V
C2928 0.1UF/16V
C2929 100PF/50V NPO
C2930 100PF/50V NPO
L_TDP R2910 49.9Ohm 1%
L_TDN R2909 49.9Ohm 1%
PLACE R2909, R2910, AND C2920 NEAR U2901.
C2920 0.1UF/16V X7R
R2908 4.7KOhm
U2902
AT93C46
EECS_LAN
EESK_LAN
EEDI_LAN
EEDO_LAN
C2935 0.1UF/16V X7R
X1_LAN
X2_LAN
X2901 25Mhz
R2924 0Ohm
C2933 27PF/50V NPO
C2934 27PF/50V NPO
R2922 0Ohm
R2921 0Ohm
L2903 80Ohm/100Mhz
C2931 0.1UF/16V
C2932 0.1UF/16V @
0.1uF are for AVDDH pins - 2 and 59.
<Variant Name>
Title : LAN RTL8101E
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Size Custom
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 29 of 63


Digital
U3002
ALC660-GR
For ALC660 Ver D
R1.1
Item 22
Mount for T13Fg
Input impedence:64K ohm(Typical)
DNI C3022 IF PCMCIA IS NOT USED
U3001
SI9183DT
0.08(USD$)
R1.1
Item 8
For EMI
For ALC861 Impdeance Match
Title : ALC660-GR
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 30 of 63




<Variant Name>

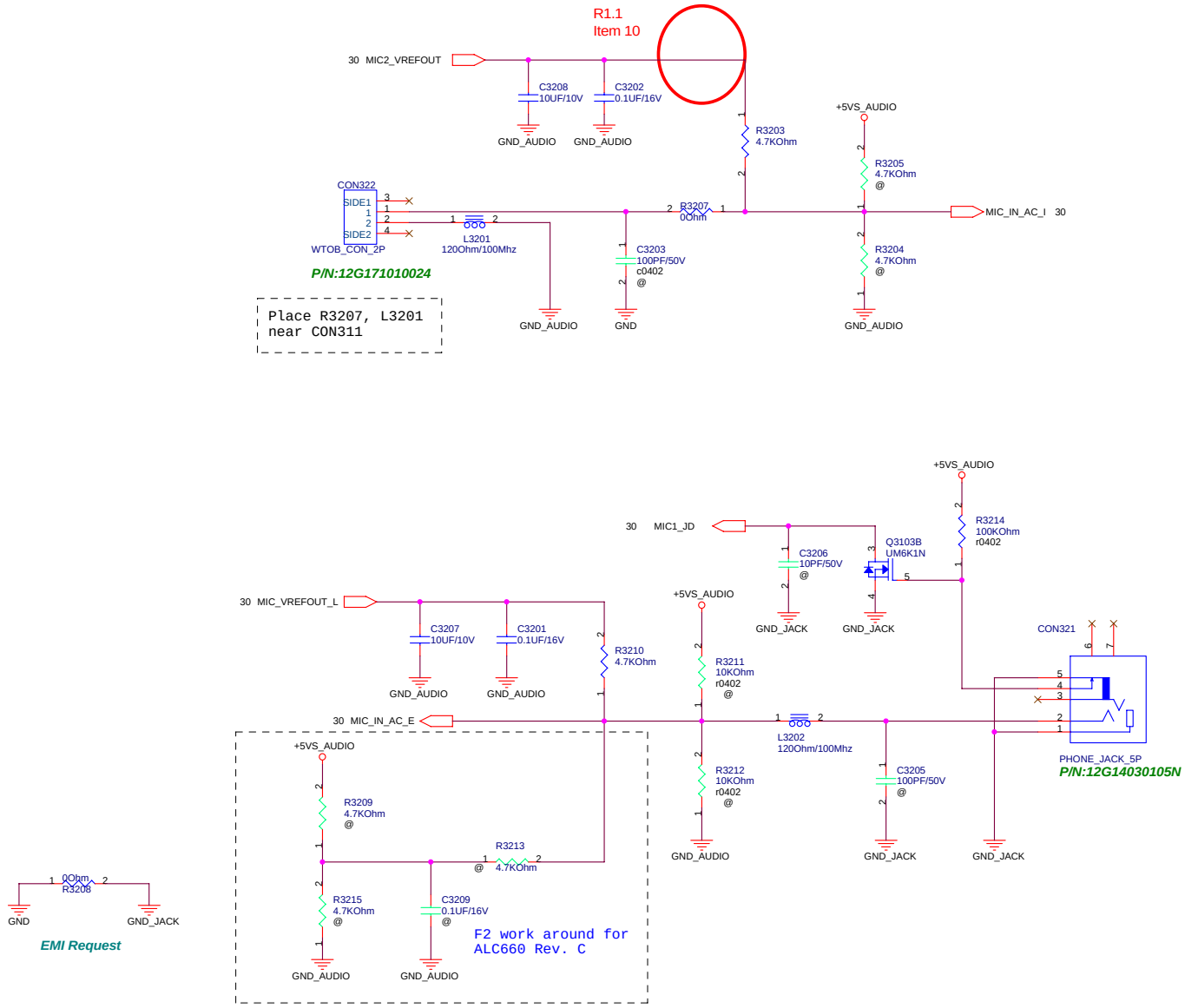
ASUSTeK COMPUTER INC

Title : G1420

Engineer: Marco Chen

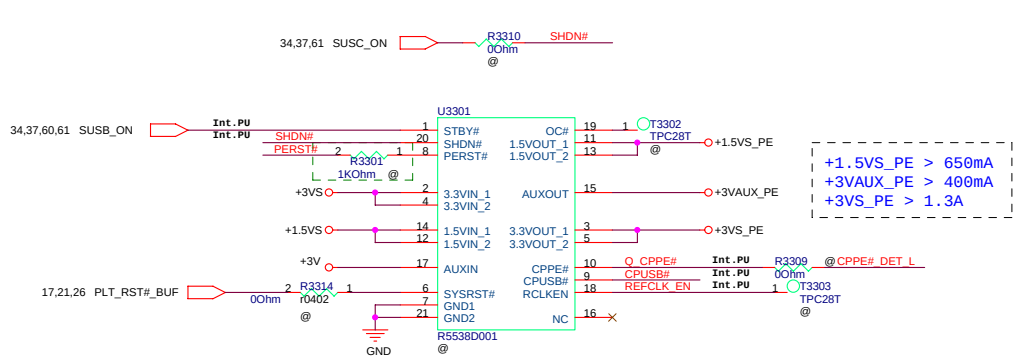
| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

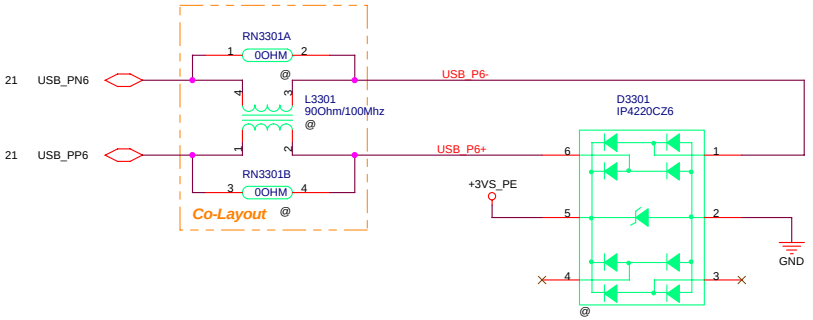
Date: Monday, August 28, 2006 Sheet 31 of 63

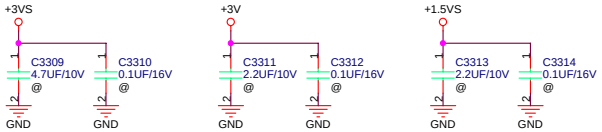


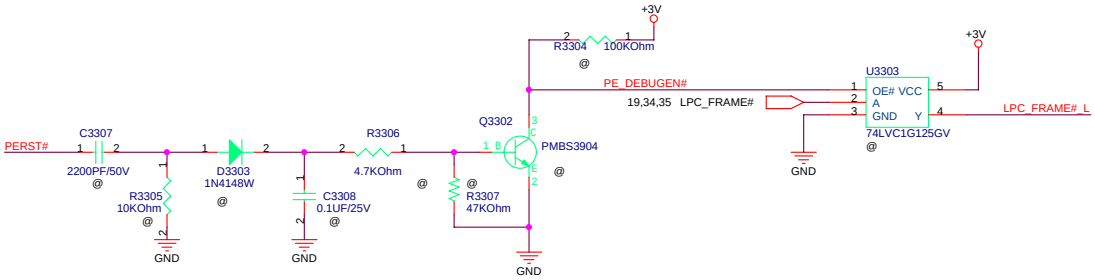

<Variant Name>

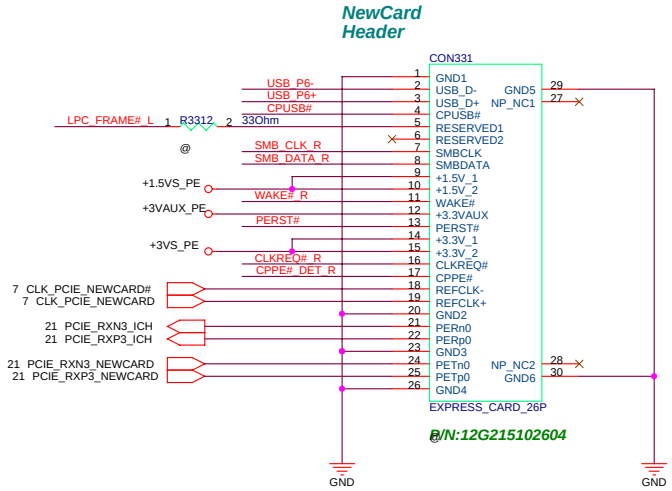
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : MICROPHONE | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 32 of 63 | |

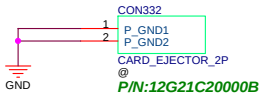


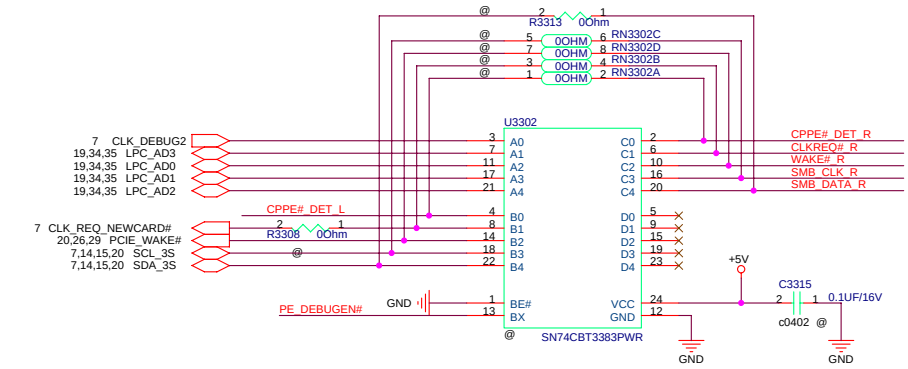



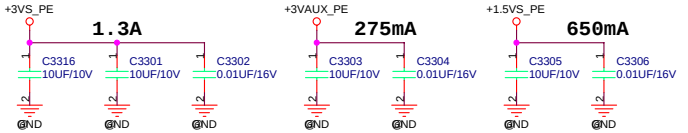



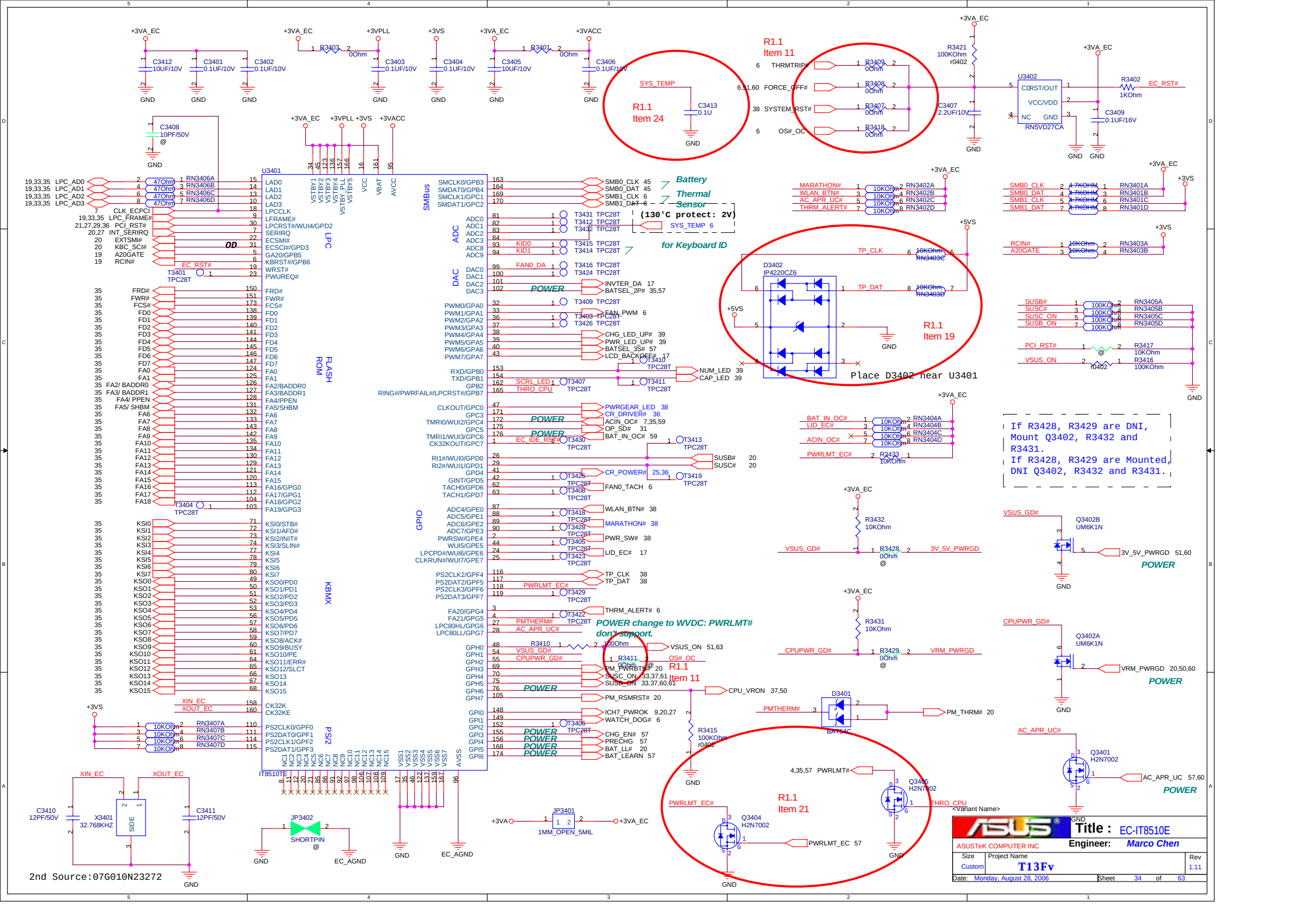




<variant_name>

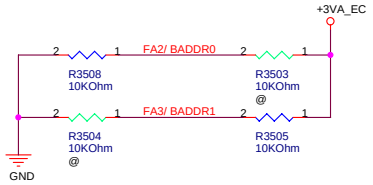
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : NEWCARD | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 33 of 63 | |


U3401
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
SMBus
ADC
DAC
Battery
Thermal Sensor
for Keyboard ID
POWER
OD
(130'C protect: 2V)
R1.1 Item 11
R1.1 Item 24
R1.1 Item 19
R1.1 Item 21
Place D3402 near U3401
If R3428, R3429 are DNI, Mount Q3402, R3432 and R3431.
If R3428, R3429 are Mounted, DNI Q3402, R3432 and R3431.
POWER change to WVDC: PWRLMT# don't support.
2nd Source:07G010N23272
Title : EC-IT8510E
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 34 of 63

## EC Hardware Strapping

**FA2/ BADDR0 & FA3/ BADDR1**

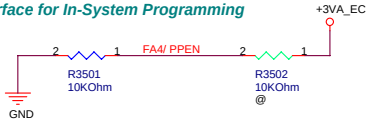
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved




Note: Sampled at VSTBY Power Up Reset

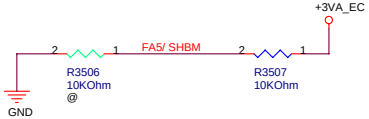
**FA4/ PPEN**

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

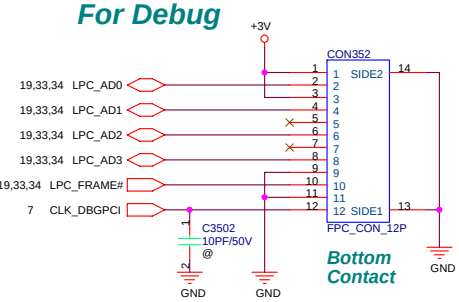



**FA5/ SHBM**

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

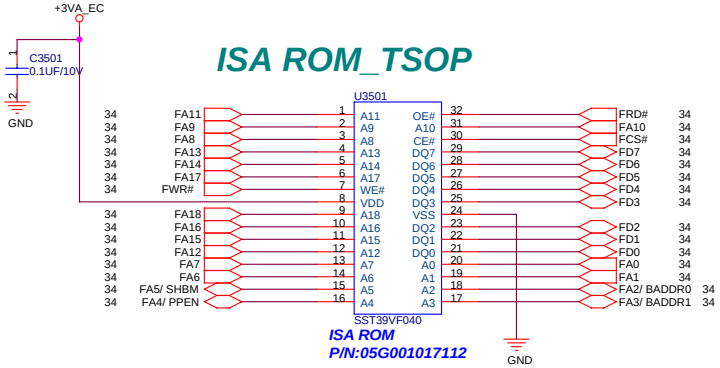



## For Debug

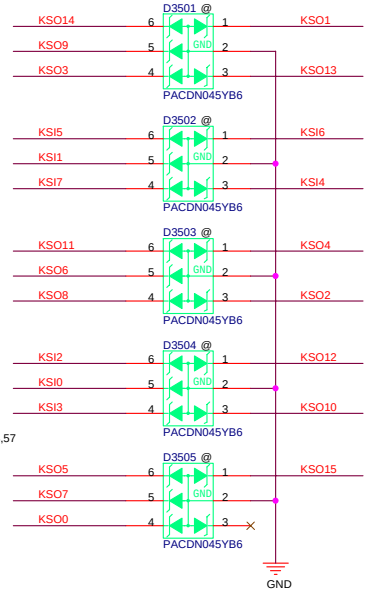



P/N:12G183301208

## ISA ROM_TSOP

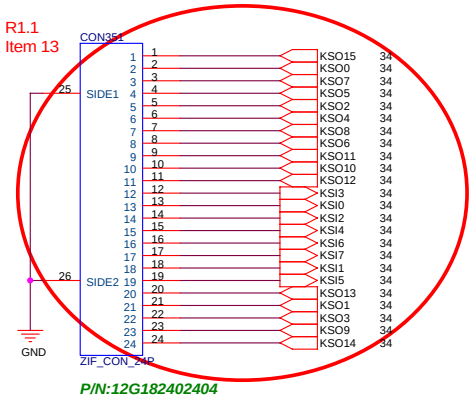



ISA ROM
P/N:05G001017112



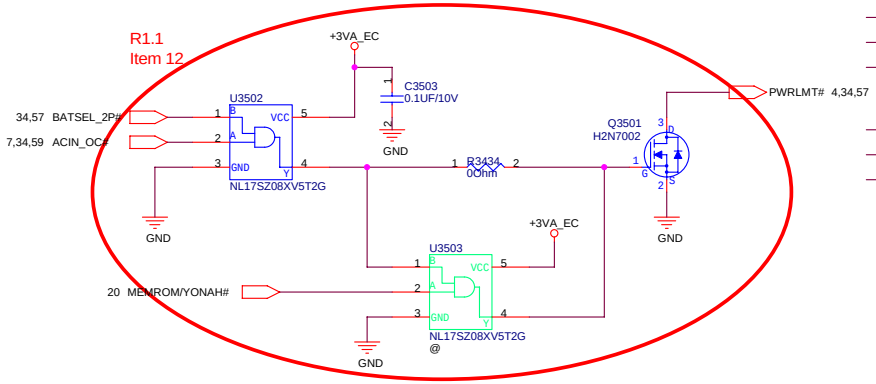

## For Keyboard

R1.1
Item 13



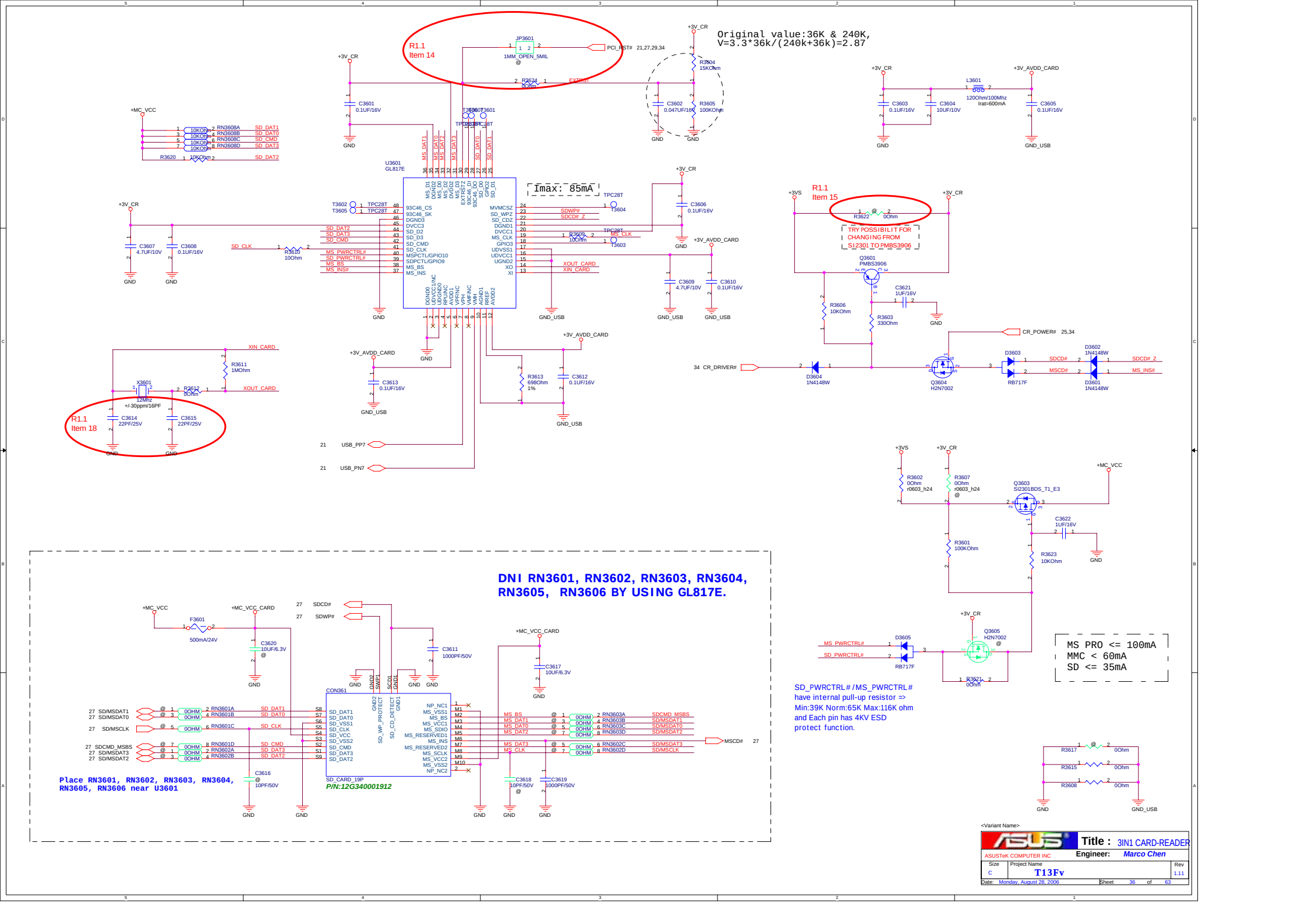

P/N:12G182402404

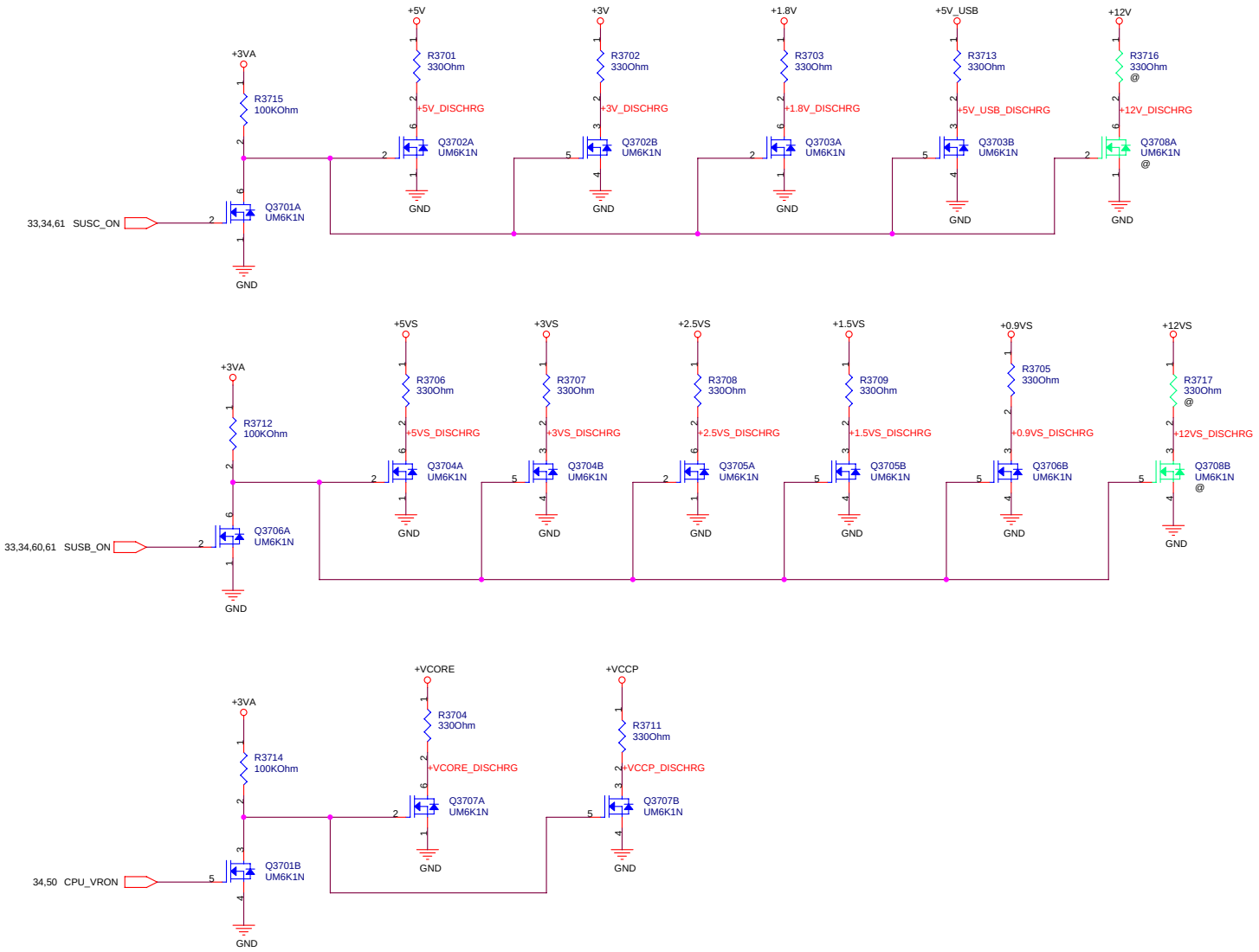
R1.1
Item 12




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : ISA_ROM&KB conn | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 35 of 63 | |

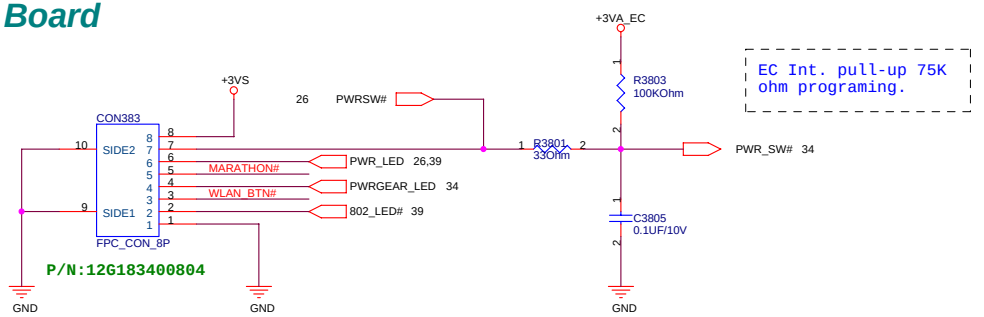

R1.1
Item 14
Original value:36K & 240K,
V=3.3*36k/(240k+36k)=2.87
Imax: 85mA
R1.1
Item 15
TRY POSSIBILITY FOR
CHANGING FROM
SI2301 TO PMBS3906
R1.1
Item 18
DNI RN3601, RN3602, RN3603, RN3604,
RN3605, RN3606 BY USING GL817E.
Place RN3601, RN3602, RN3603, RN3604,
RN3605, RN3606 near U3601
P/N:12G340001912
SD_PWRCTRL# / MS_PWRCTRL#
have internal pull-up resistor =>
Min:39K Norm:65K Max:116K ohm
and Each pin has 4KV ESD
protect function.
MS PRO <= 100mA
MMC < 60mA
SD <= 35mA
Title : 3IN1 CARD-READER
ASUSTeK COMPUTER INC
Engineer: Marco Chen
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
Sheet 36 of 63



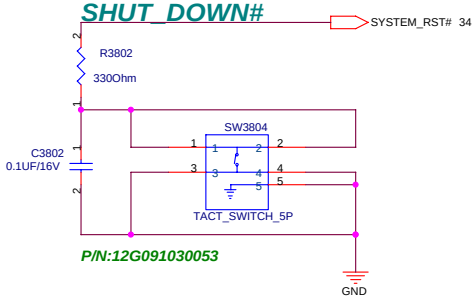

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DISCHARGE | |
| | Engineer: *Marco Chen* | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 37 of 63 | |

# FFC CONNECTER for T13Fv SW Board

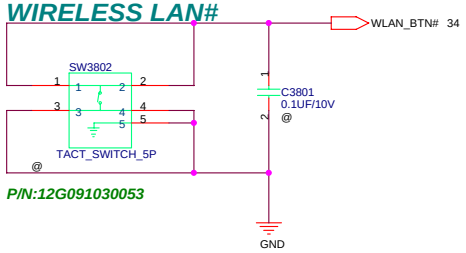



## SHUT_DOWN#

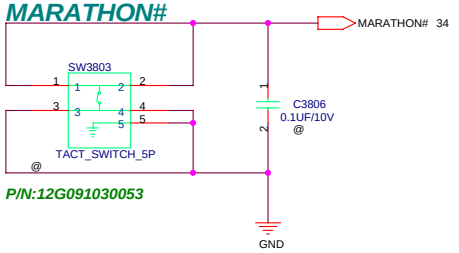


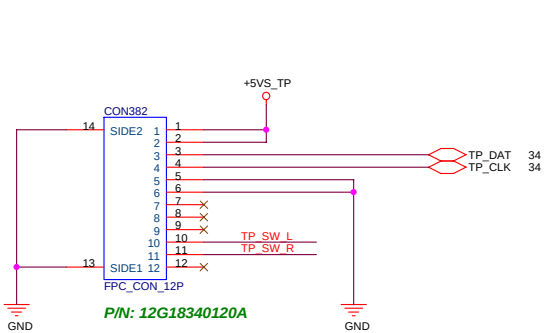

# INSTANT KEY for T13Fg

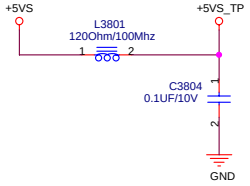
## WIRELESS LAN#



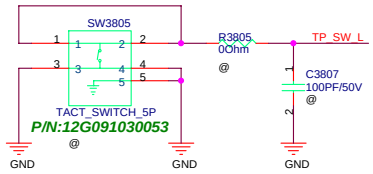

## MARATHON#

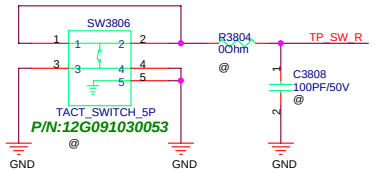



## Select Button for T13Fg



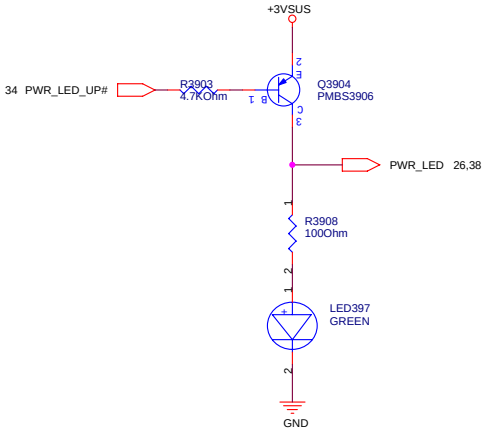




<Variant Name>

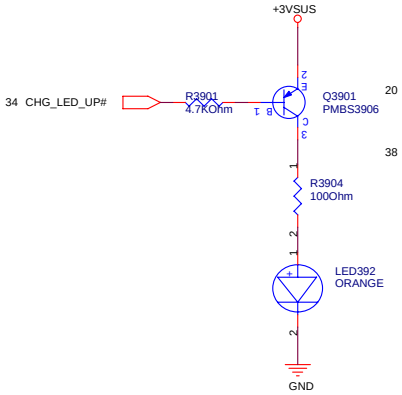
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : Key & FFC CONN | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 38 of 63 | |

PR_NOTE: Change all LED series resisters from 0402 to 0603 type
and change color from green to blue.

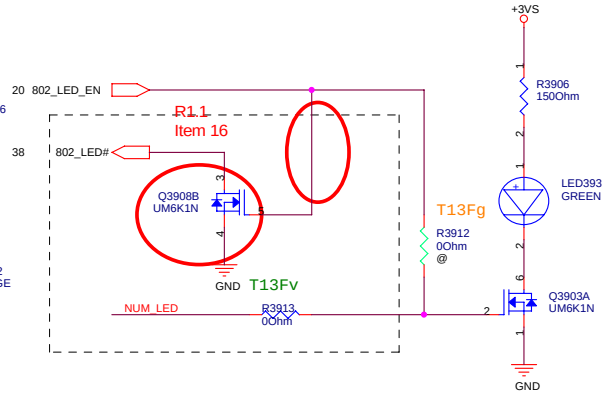
## For POWER LED



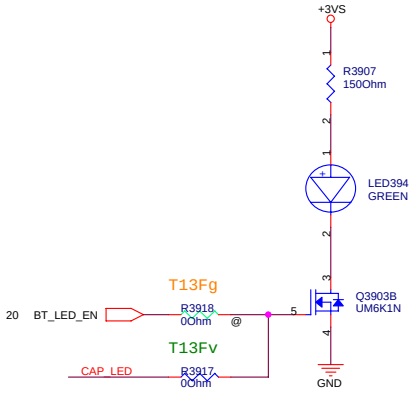

## For BATTERY LED



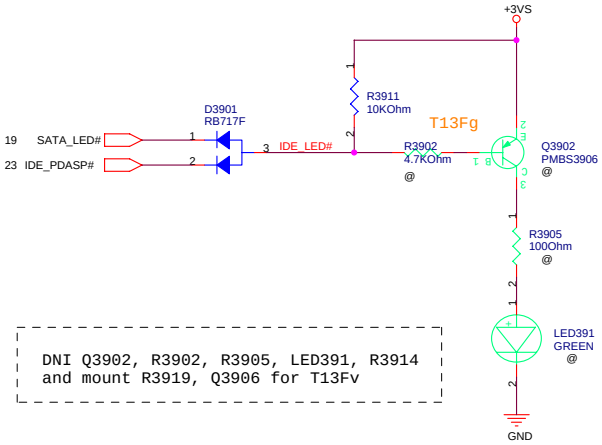

## For WireLess LED




## For BT LED

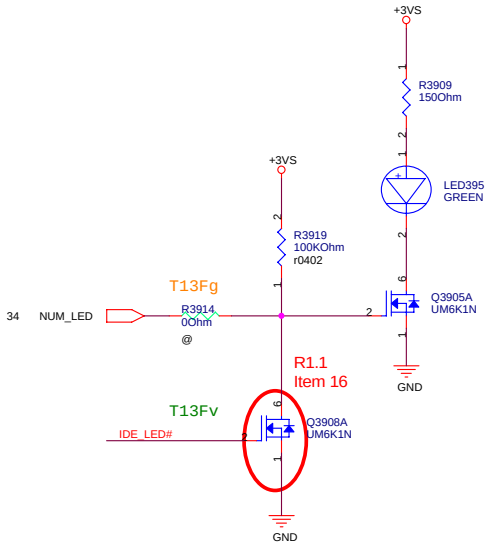



## For SATA/IDE LED

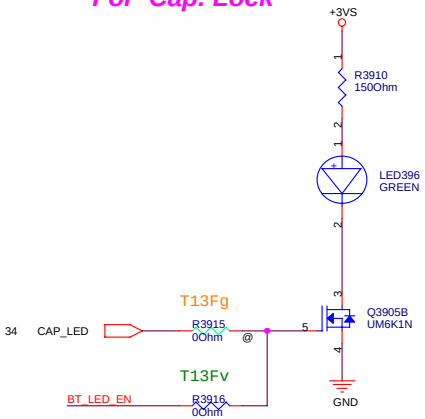



DNI Q3902, R3902, R3905, LED391, R3914
and mount R3919, Q3906 for T13Fv

## For Num Lock




## For Cap. Lock




<Variant Name>

Title : LEDs

ASUSTeK COMPUTER INC Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 40 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 41 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 42 of 63

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 43 of 63

<Variant Name>

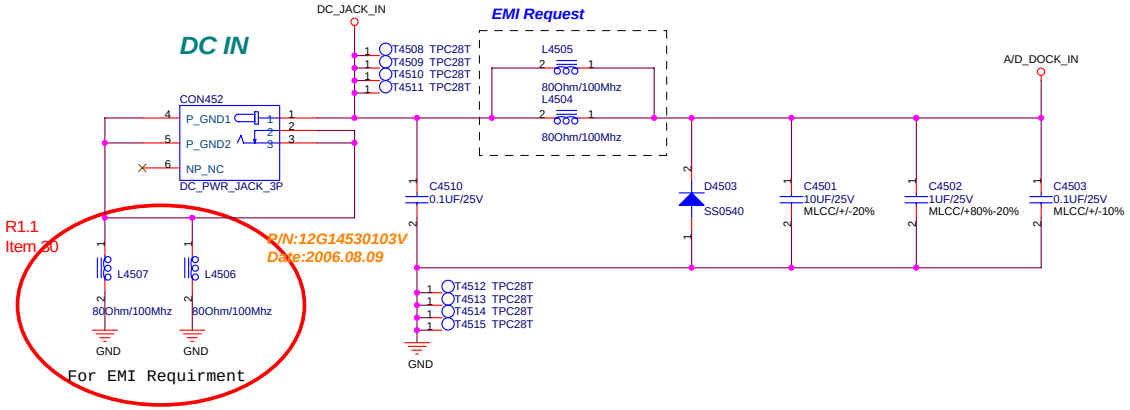
Title : EMPTY

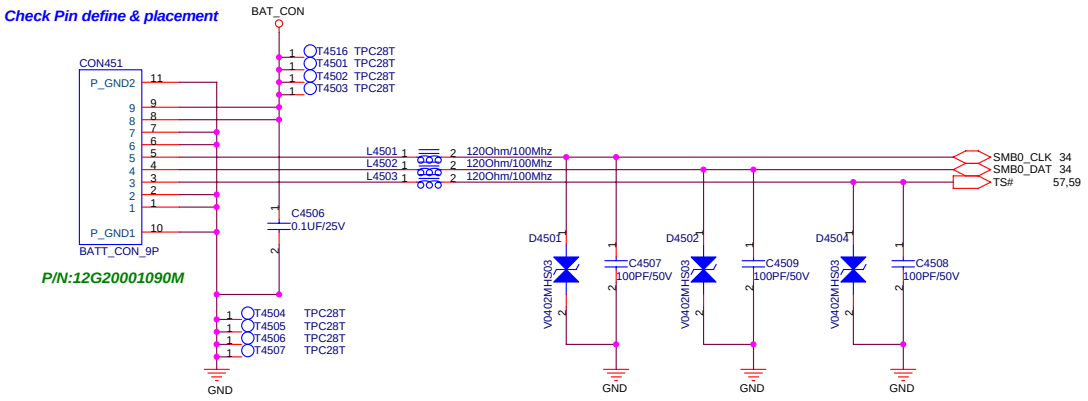
ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 44 of 63




<Variant Name>

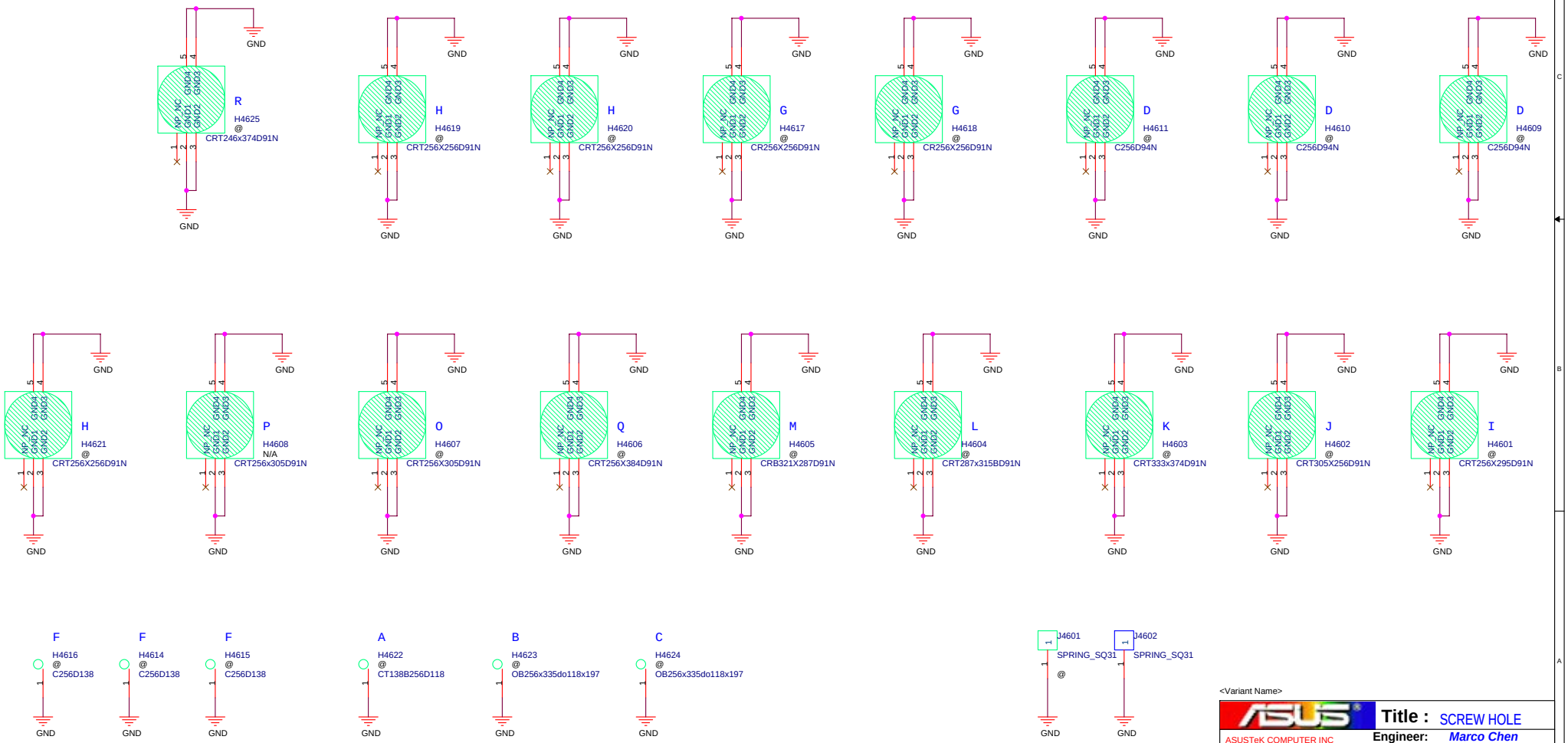
ASUSTeK COMPUTER INC

Title : BAT&Adapter conn

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 45 of 63




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : SCREW HOLE | |
| | Engineer: Marco Chen | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 46 of 63 | |

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| C | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 47 of 63

R1.0 -> R1.1

1.Page 6: DNI R611 because Int. pull-up resister exists in FAN module.

2.Page 15: Add circuits to change DDR2 Vref from +0.9VS to +0.9V.

3.Page 17: Change reference name from F3602 to F1701.

4.Page 21: DNI U2103.

5.Page 23: Change reference name C4511 -> C2311, C4513 -> C2313, C4512 -> C2312, C4514 -> C2310.

6.Page 23: Change R2301 size from 0603 to 0402.

7.Page 23: Add pull high resister R2306*DNI and pull down resister R2307*Mount for ODD cable select.

8.Page 30: Change reference name L3008 -> R3020, L3009 -> R3021, L3010 -> R3022.

9.Page 31: Delete R3133 and connect OP_SD# to D3103.2 directly.

10.Page 32: Delete R3201 and connect MIC2_VREFOUTto R3203.1 directly.

11.Page 34:DNI D604, R3411 and mount R3408, R3418 for thermal protection.

12.Page 35: Add circuits to throttle CPU speed 50% when un-plug adapter and battery is 3S1P type.

13.Page 35: Change keyboard matrix.

14.Page 36: Change reference name from JP3403 to JP3601

15.Page 36: Change R3622 size from 0402 to 0603.

16.Page 39: Delete R3920 and change Q3906 and Q3907*2N7006 to Q3908*UM6K1N.

17.Page 17: C1701 from 0.1uF/25V to 0.22Uf/25V to meet LCD power sequence.

18.Page 36: Change C3614 and C3614 form 15pF to 20pF for ITTI recommendation.

19.Page 34: Add ESD Protection*D3402 for Touch Pad.

20.Page 27: Add series resister 33 ohm for PCI_FRAME# and PCI_AD13

21.Page 34:Change Q3403**UM6K1N to Q3404, Q3405*2N7002.

22.Page 18: Change L1801, L1802, and L1803 from bead to inductor.

23.Page 19, 30: Change R1911, R1913, R1915, R1918 and R3002 from 33ohm to 39ohm.

24.Page 6: Change R615 pull up from +3VS to +5VS_AUDIO.

25.Page 6: Change R610 from 100ohm to 200ohm and reserve 1uF decoupling CAP.

26.Page 27: Change R2718 from 510Kohm to 110Kohm and C2701 from 0.1uF to 0.47uF.

27.Page 9, 11: Reserve C903, C904, C905, C906 and R1103 for EMI requirement.

28.Page 21: Change R2104 from 22.6ohm to 21ohm to enhance USB driven strength.

29.Page 19: Change C1901, and C1903 from 15p F to 12p F for ITTI recommendation.

30.Page 45:Add L4506 and L4507 for EMI requirement.

<Variant Name>

Title : History(1)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 48 of 63

<Variant Name>

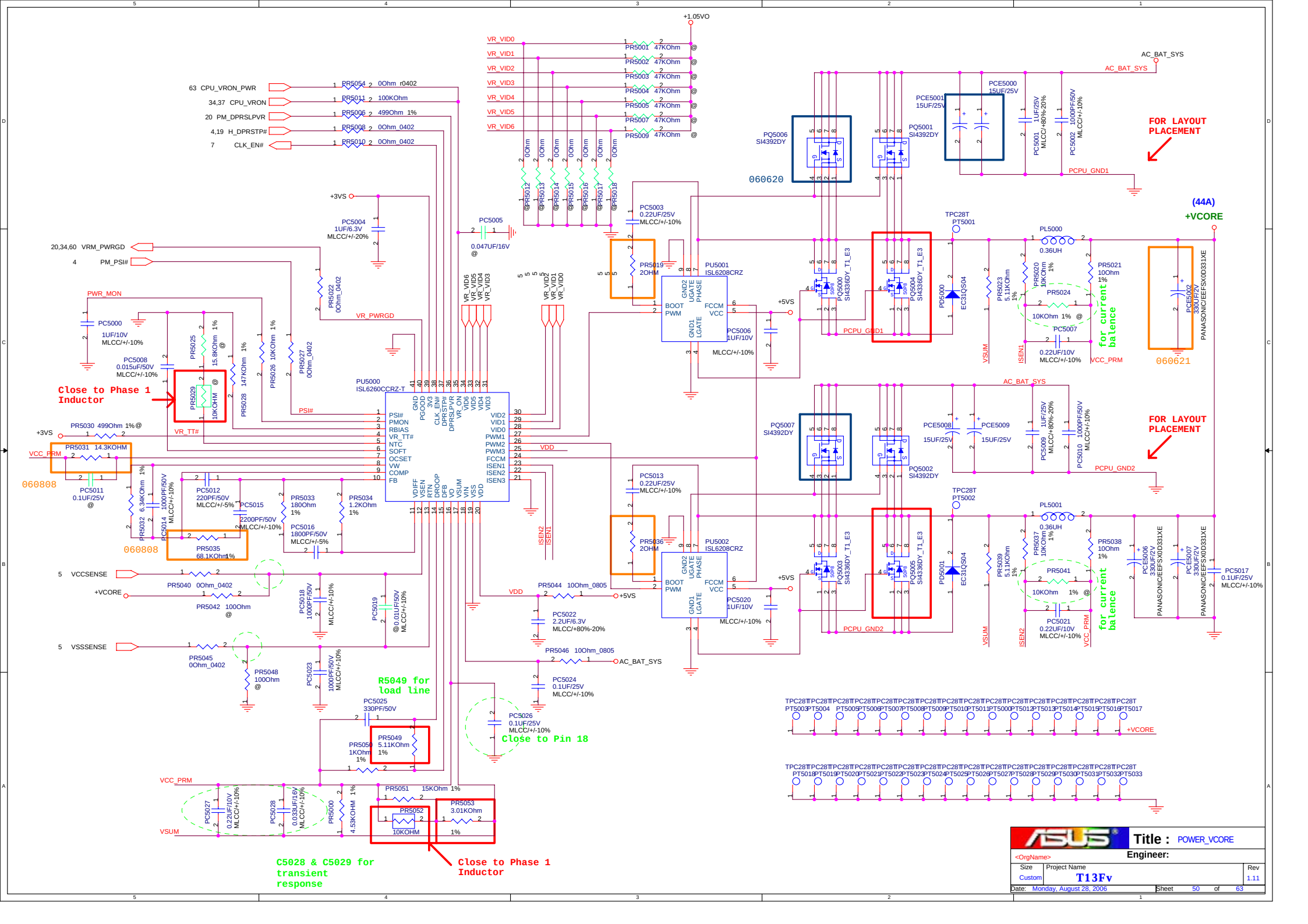
Title : History(2)

ASUSTeK COMPUTER INC

Engineer: Marco Chen

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 49 of 63


+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm @
PR5002 47KOhm @
PR5003 47KOhm @
PR5004 47KOhm @
PR5005 47KOhm @
PR5007 47KOhm @
PR5009 47KOhm @
0Ohm
PR5012 PR5013 PR5014 PR5015 PR5016 PR5017 PR5018
63 CPU_VRON_PWR
34,37 CPU_VRON
20 PM_DPRSLPVR
4,19 H_DPRSTP#
7 CLK_EN#
PR5054 0Ohm r0402
PR5011 100KOhm
PR5006 499Ohm 1%
PR5008 0Ohm_0402
PR5010 0Ohm_0402
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5005 0.047UF/16V @
20,34,60 VRM_PWRGD
4 PM_PSI#
PR5022 0Ohm_0402
VR_PWRGD
PWR_MON
PC5000 1UF/10V MLCC/+/-10%
PR5025 15.8KOhm 1% @
PR5026 10KOhm 1%
PR5027 0Ohm_0402
PC5008 0.015uF/50V MLCC/+/-10%
PR5029 10KOHM 1% @
PR5028 147KOhm 1%
Close to Phase 1 Inductor
PU5000 ISL6260CCRZ-T
PSI#
VR_TT#
VDD
ISEN2
ISEN1
PR5030 499Ohm 1% @
PR5031 14.3KOHM
VCC_PRM
060808
PC5011 0.1UF/25V @
PR5032 6.34KOhm 1%
PC5014 1000PF/50V MLCC/+/-10%
PC5012 220PF/50V MLCC/+/-5%
PC5015 2200PF/50V MLCC/+/-10%
PR5033 180Ohm 1%
PC5016 1800PF/50V MLCC/+/-5%
PR5034 1.2KOhm 1%
PR5035 68.1KOhm 1%
5 VCCSENSE
+VCORE
PR5040 0Ohm_0402
PR5042 100Ohm @
PC5018 1000PF/50V MLCC/+/-10%
PC5019 @ 0.01UF/50V MLCC/+/-10%
5 VSSSENSE
PR5045 0Ohm_0402
PR5048 100Ohm @
PC5023 1000PF/50V MLCC/+/-10%
R5049 for load line
PC5025 330PF/50V
PR5049 5.11KOhm 1%
PR5050 1KOhm 1%
PC5026 0.1UF/25V MLCC/+/-10%
Close to Pin 18
VCC_PRM
PC5027 0.22UF/10V MLCC/+/-10%
PC5028 0.033UF/16V MLCC/+/-10%
PR5000 4.53KOHM 1%
PR5051 15KOhm 1%
PR5052 10KOHM
PR5053 3.01KOhm 1%
VSUM
C5028 & C5029 for transient response
Close to Phase 1 Inductor
PC5003 0.22UF/25V MLCC/+/-10%
PR5019 2OHM
PU5001 ISL6208CRZ
BOOT PWM GND2 UGATE PHASE FCCM VCC GND1 LGATE
PC5006 1UF/10V MLCC/+/-10%
+5VS
PC5013 0.22UF/25V MLCC/+/-10%
PR5036 2OHM
PU5002 ISL6208CRZ
PC5020 1UF/10V MLCC/+/-10%
PR5044 10Ohm_0805
PC5022 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
AC_BAT_SYS
PC5024 0.1UF/25V MLCC/+/-10%
PQ5006 SI4392DY
PQ5001 SI4392DY
060620
PCE5001 15UF/25V
PCE5000 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/50V MLCC/+/-10%
PCPU_GND1
FOR LAYOUT PLACEMENT
(44A)
+VCORE
TPC28T PT5001
PL5000 0.36UH
PD5000 EC31QS04
PR5023 5.11KOhm 1%
PR5020 10KOhm 1%
PR5024 10KOhm 1% @
PR5021 10Ohm 1%
PC5007 0.22UF/10V MLCC/+/-10%
VCC_PRM
for current balence
PCE5002 330UF/2V PANASONIC/EEFSX0D331XE
060621
PQ5007 SI4392DY
PQ5002 SI4392DY
PCE5008 15UF/25V
PCE5009 15UF/25V
PC5009 1UF/25V MLCC/+80%-20%
PC5010 1000PF/50V MLCC/+/-10%
PCPU_GND2
TPC28T PT5002
PL5001 0.36UH
PD5001 EC31QS04
PR5039 5.11KOhm 1%
PR5037 10KOhm 1%
PR5041 10KOhm 1% @
PR5038 10Ohm 1%
PC5021 0.22UF/10V MLCC/+/-10%
PCE5006 330UF/2V PANASONIC/EEFSX0D331XE
PC5007 330UF/2V PANASONIC/EEFSX0D331XE
PC5017 0.1UF/25V MLCC/+/-10%
TPC28T PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5000 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
+VCORE
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
Engineer:
<OrgName>
Size Custom
Project Name T13Fv
Rev 1.11
Date: Monday, August 28, 2006
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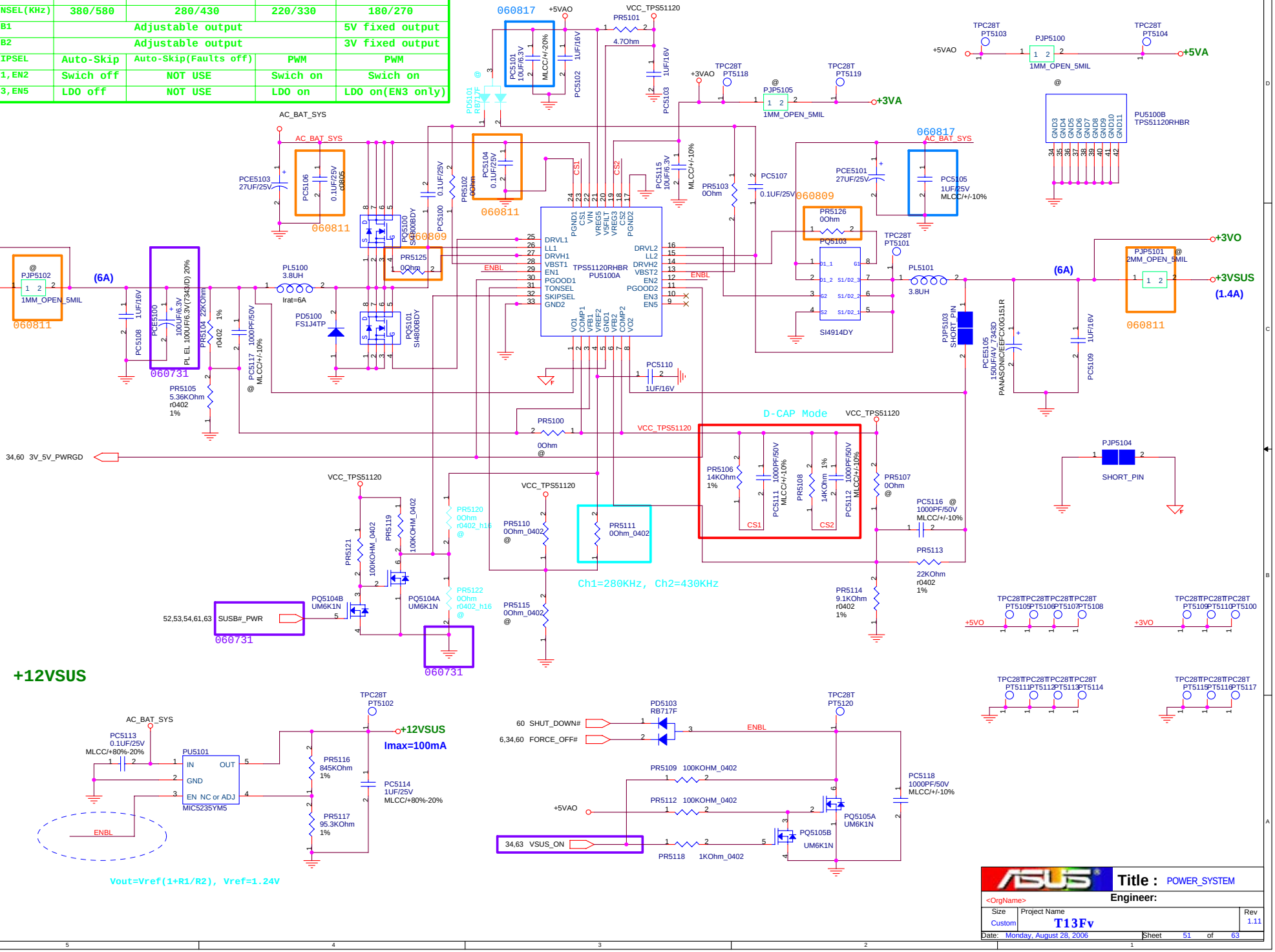
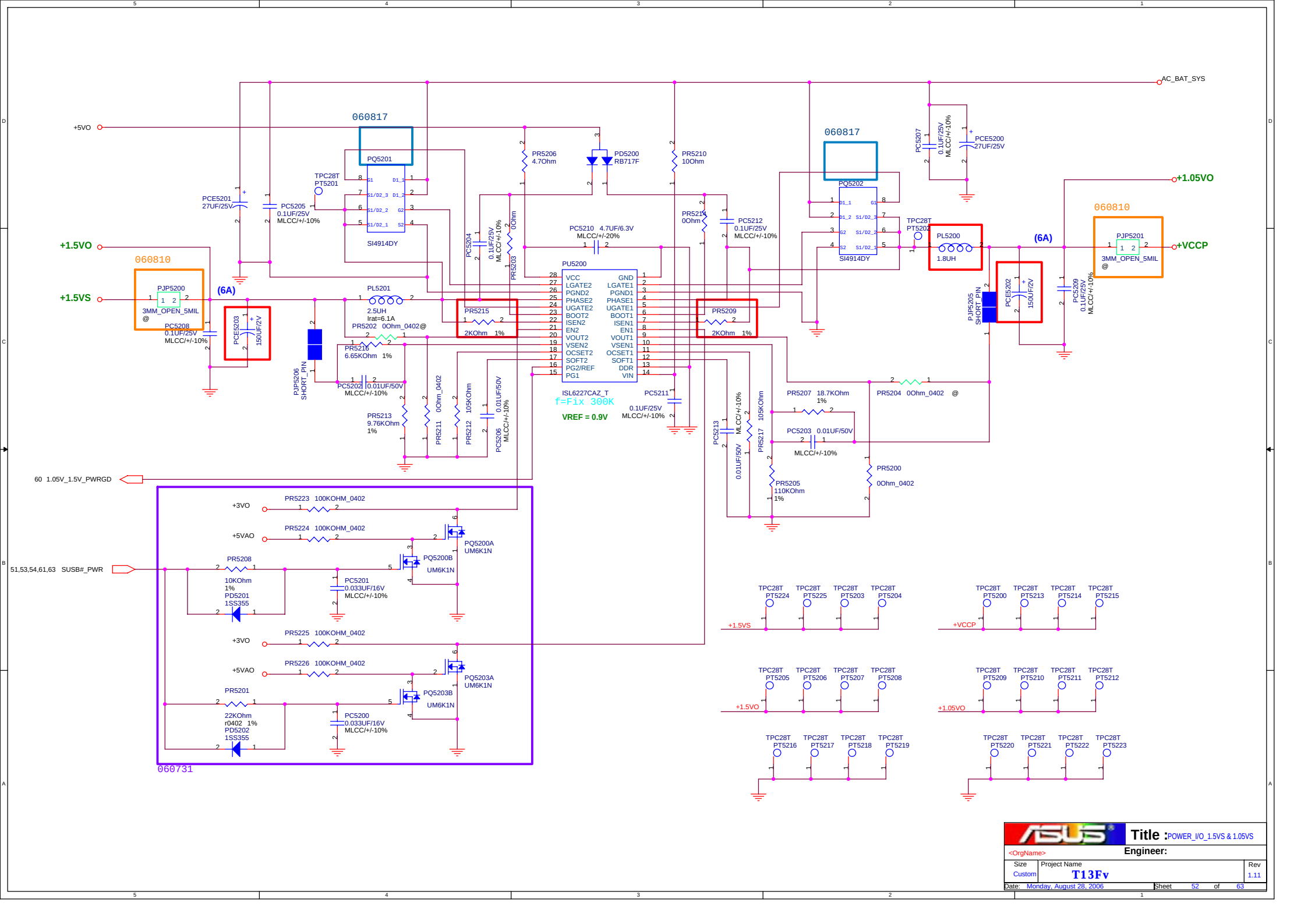
| PIN | GND | VREF2 | FLOAT | V5FILT |
|---|---|---|---|---|
| COMP | N/A | N/A | Current mode | D-CAP mode |
| TONSEL(KHz) | 380/580 | 280/430 | 220/330 | 180/270 |
| VFB1 | Adjustable output | | | 5V fixed output |
| VFB2 | Adjustable output | | | 3V fixed output |
| SKIPSEL | Auto-Skip | Auto-Skip(Faults off) | PWM | PWM |
| EN1,EN2 | Swich off | NOT USE | Swich on | Swich on |
| EN3,EN5 | LDO off | NOT USE | LDO on | LDO on(EN3 only) |




AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
060817
060810
060731
PQ5201
SI4914DY
PQ5202
SI4914DY
PU5200
ISL6227CAZ_T
f=Fix 300K
VREF = 0.9V
PJP5200
PJP5201
PL5200
1.8UH
PL5201
2.5UH
Irat=6.1A
PR5202 0Ohm_0402@
PR5215
2KOhm 1%
PR5209
2KOhm 1%
PR5216
6.65KOhm 1%
PR5213
9.76KOhm
1%
PR5207 18.7KOhm
1%
PR5204 0Ohm_0402 @
PR5205
110KOhm
1%
PR5200
0Ohm_0402
PR5206
4.7Ohm
PD5200
RB717F
PR5210
10Ohm
PR5208
10KOhm
1%
PD5201
1SS355
PR5201
22KOhm
r0402 1%
PD5202
1SS355
PQ5200A
UM6K1N
PQ5200B
UM6K1N
PQ5203A
UM6K1N
PQ5203B
UM6K1N
PR5223 100KOHM_0402
PR5224 100KOHM_0402
PR5225 100KOHM_0402
PR5226 100KOHM_0402
PJP5206
SHORT_PIN
PJP5205
SHORT_PIN
(6A)
(6A)
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
+3VO
+5VAO
+3VO
+5VAO
3MM_OPEN_5MIL
@
3MM_OPEN_5MIL
@
Title : POWER_I/O_1.5VS & 1.05VS
Engineer:
<OrgName>
Size
Custom
Project Name
T13Fv
Rev
1.11
Date: Monday, August 28, 2006
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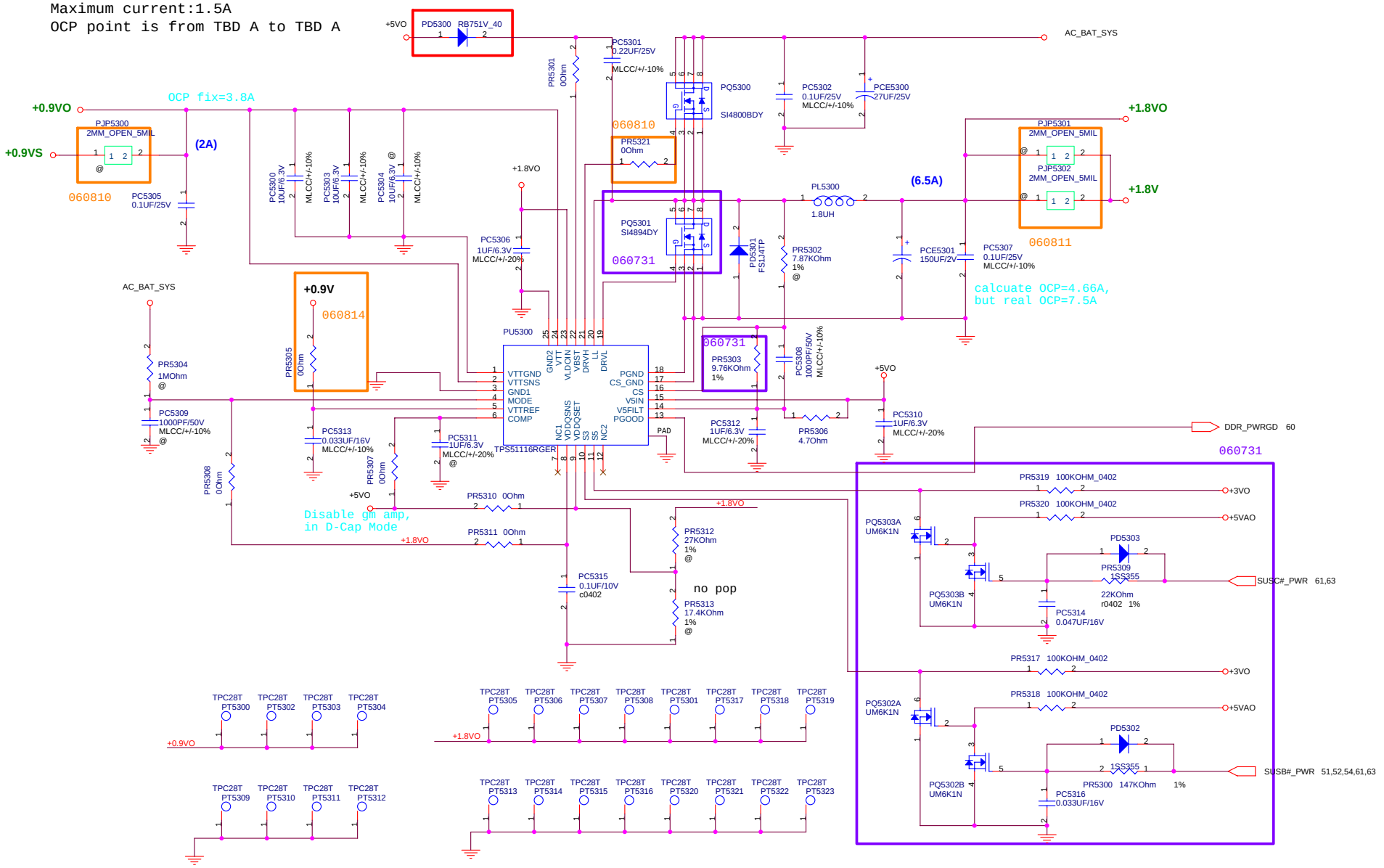
060811

.9 Volt +/-5%.9 Volt +/-5%
Design Current:1.05A
Maximum current:1.5A
OCP point is from TBD A to TBD A

1.8Volt +/-5%
Design Current:7.3A
Maximum current:10.5A
OCP point is from TBD A to TBD A




ASUS

Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

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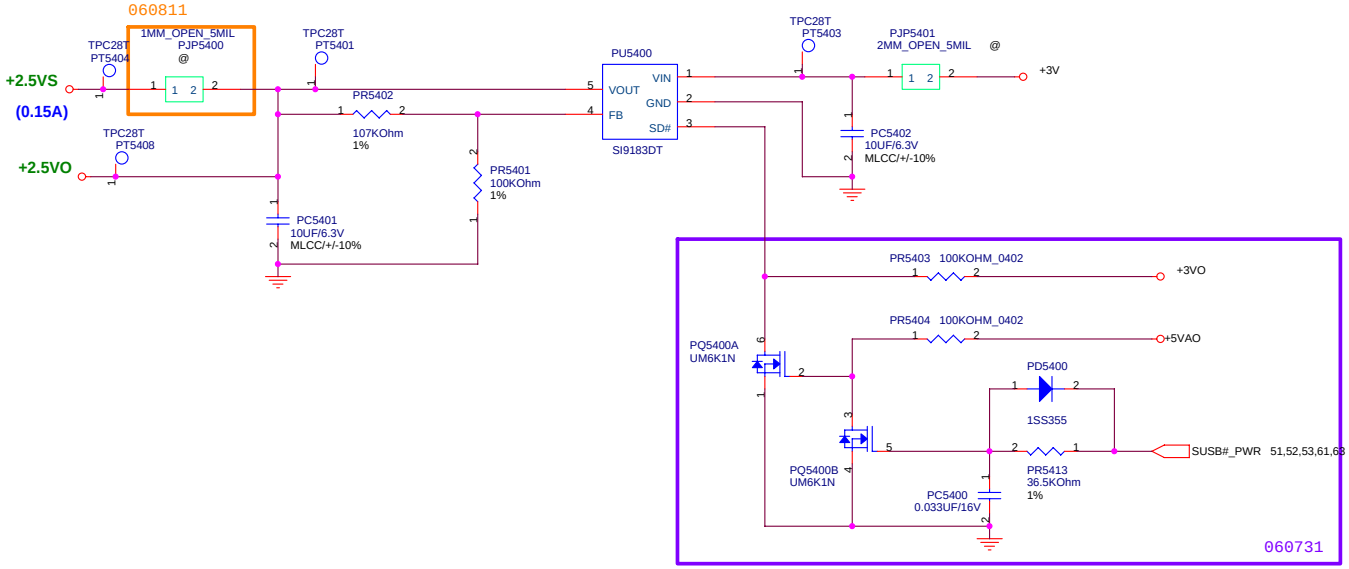
## +2.5VS




| | | |
|---|---|---|
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 54 of 63 | |

Title : POWER_I/O_+3VA & +2.5V

Title : EMPTY

<OrgName>

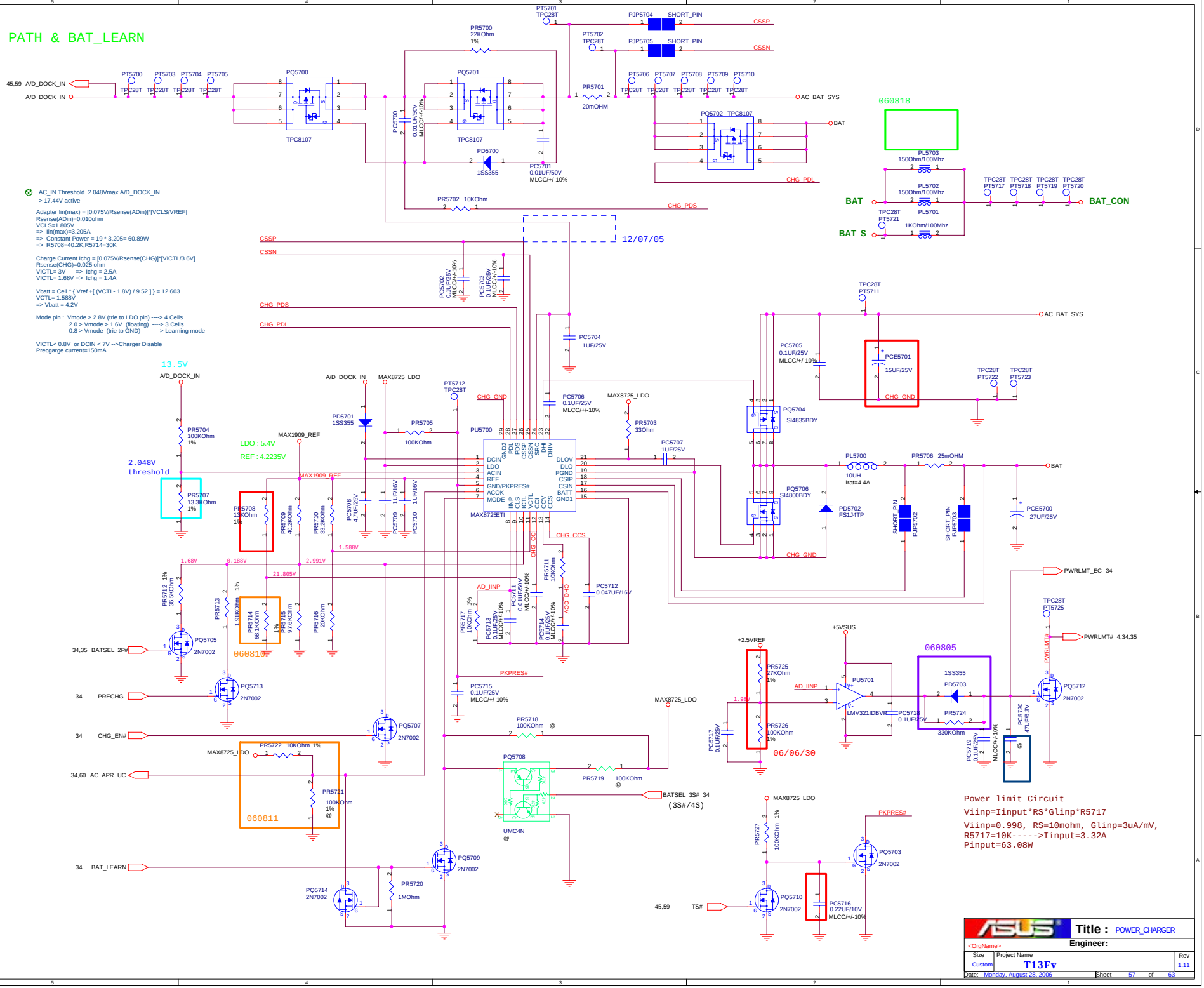
Engineer:

| Size | Project Name | Rev |
|---|---|---|
| Custom | T13Fv | 1.11 |

Date: Monday, August 28, 2006 Sheet 55 of 63

| | |
|---|---|
| Title : | EMPTY |
| <OrgName> | Engineer: |
| Size: Custom | Project Name: T13Fv |
| Rev: 1.11 | |
| Date: Monday, August 28, 2006 | Sheet 56 of 63 |

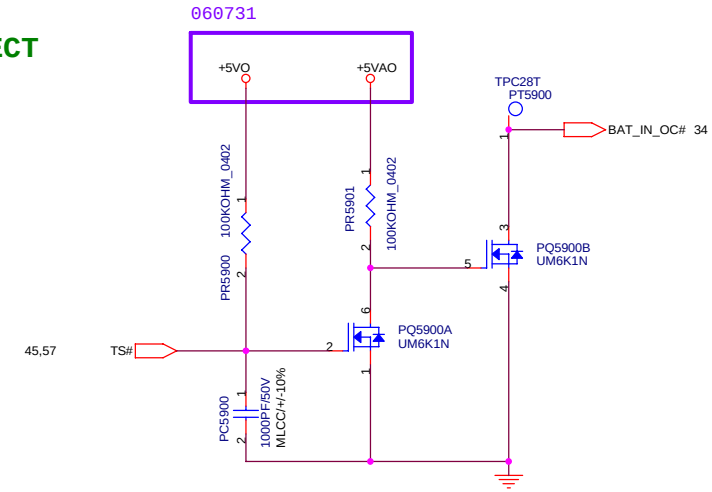
# POWER PATH & BAT_LEARN



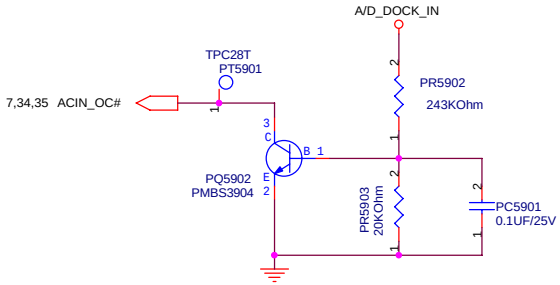

| | | |
|---|---|---|
| ASUS | Title : POWER_CHARGER | |
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 57 of 63 | |

| | |
|---|---|
| Title : | POWER_PIC |
| <OrgName> | Engineer: |
| Size: Custom | Project Name: T13Fv |
| Rev: 1.11 | |
| Date: Monday, August 28, 2006 | Sheet 58 of 63 |

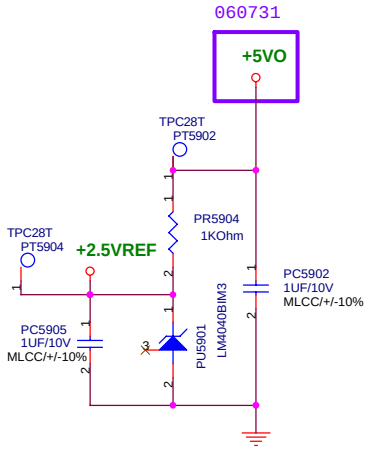
## BATTERY IN DETECT




## ADAPTER IN DETECT

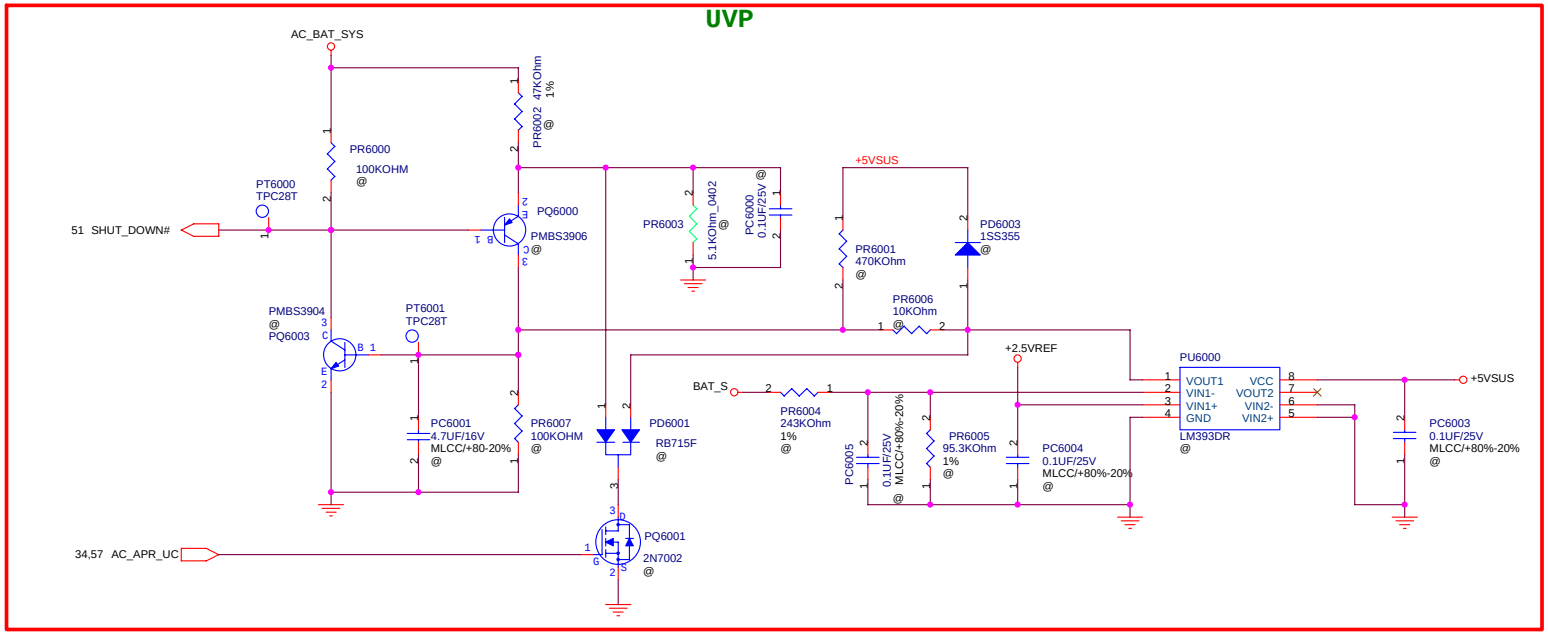



## +5VLCM, +5VCHG & +2.5VREF

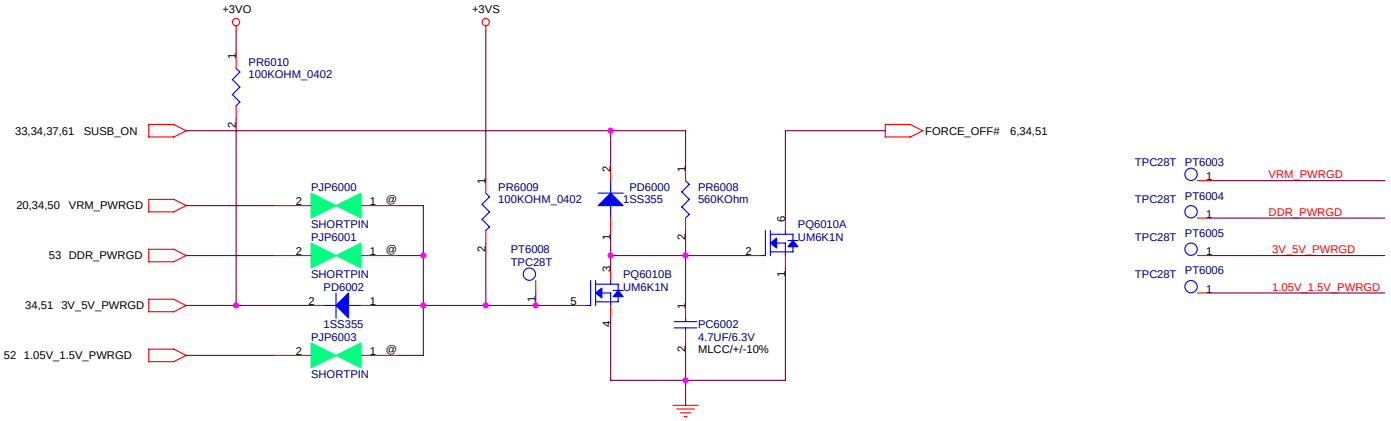



| | | |
|---|---|---|
| ASUS | Title : POWER_DETECT | |
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 59 of 63 | |

## UVP

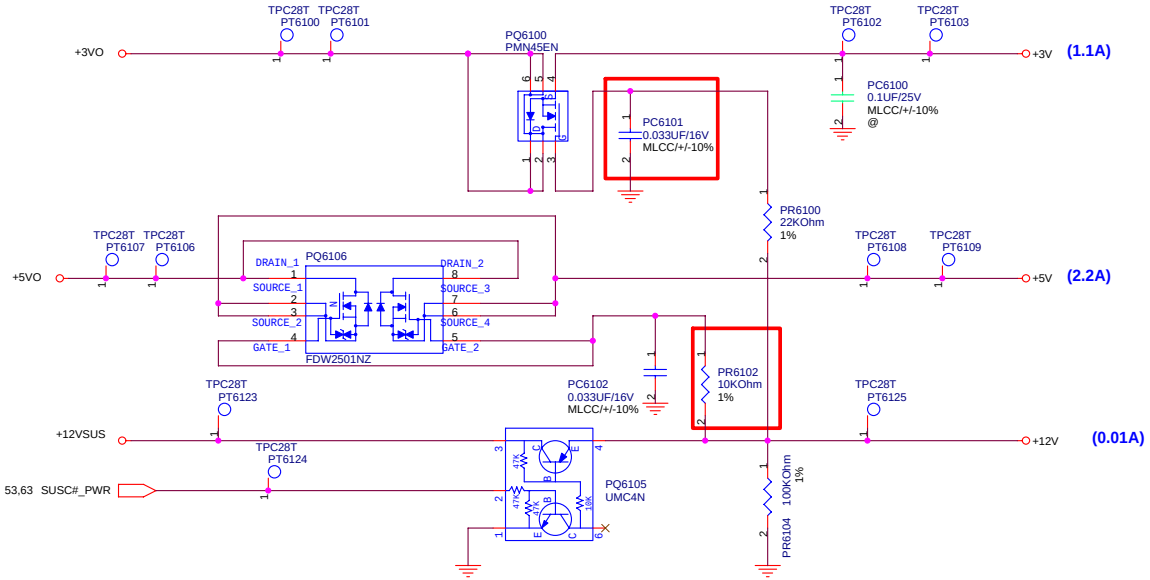


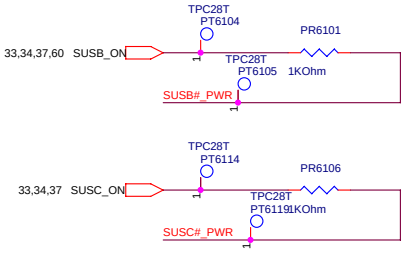

## POWER GOOD DETECTER



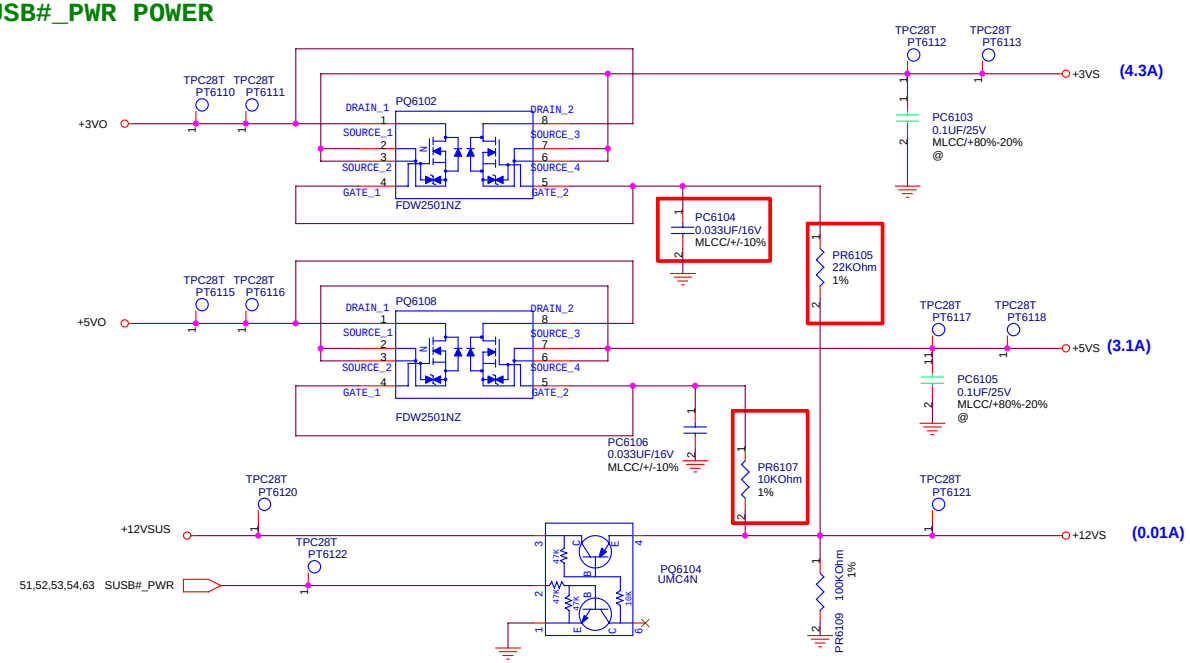

| | | |
|---|---|---|
| Title : POWER_PROTECT | | |
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 60 of 63 | |

## SUSC#_PWR POWER

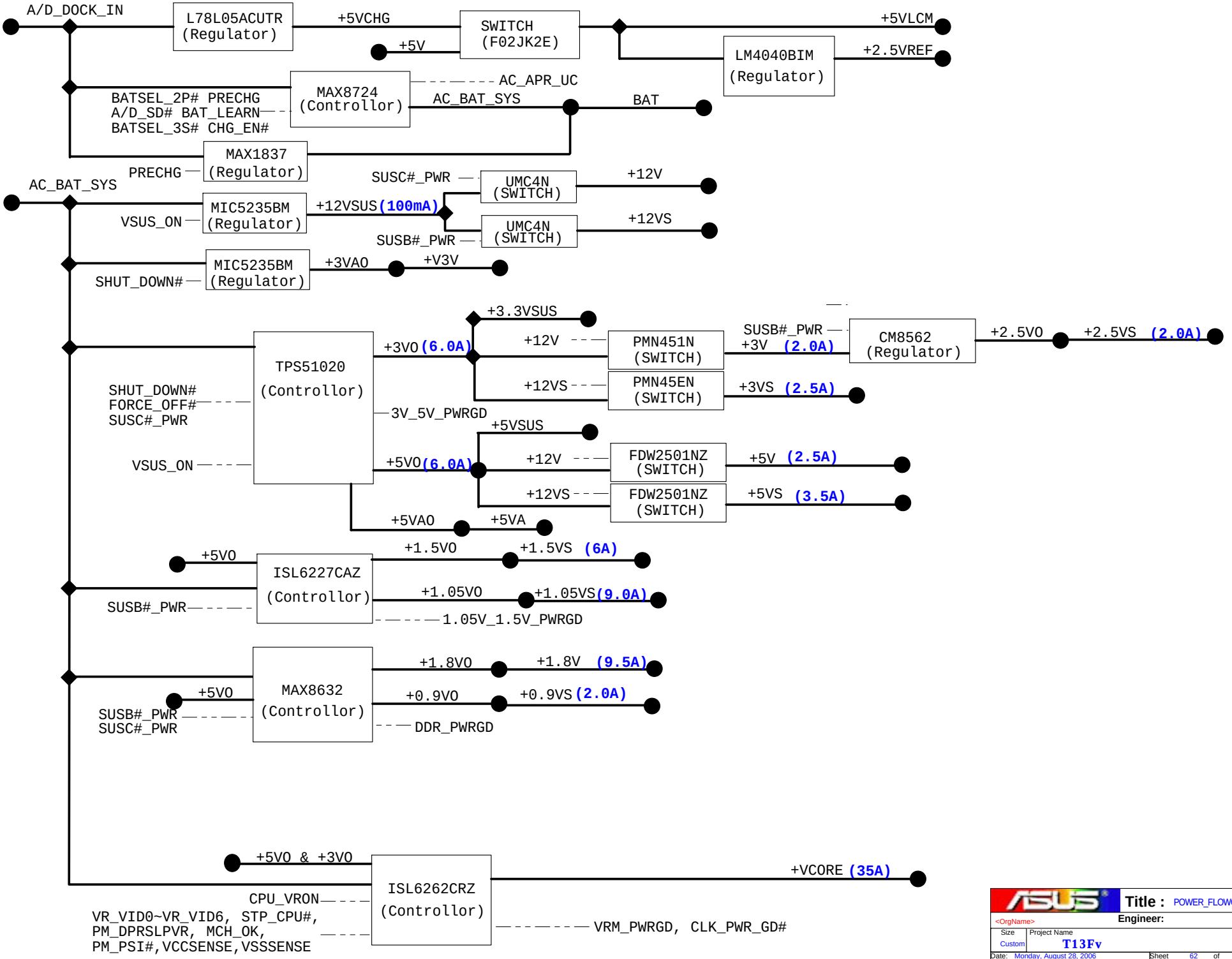



## SUSB#_PWR POWER

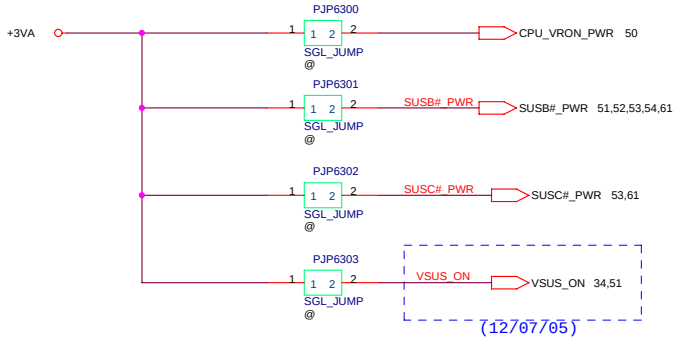



| | | |
|---|---|---|
| ASUS | Title : POWER_LOAD SWITCH | |
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 61 of 63 | |




| | | |
|---|---|---|
| Title : POWER_FLOWCHART | | |
| <OrgName> | Engineer: | |
| Size: Custom | Project Name: T13Fv | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 62 of 63 | |


## FOR POWER TEST




| | | | |
|---|---|---|---|
| ASUS | Title : POWER_SIGNAL | | |
| <OrgName> | Engineer: | | |
| Size: Custom | Project Name: T13Fv | | Rev: 1.11 |
| Date: Monday, August 28, 2006 | Sheet 63 of 63 | | |