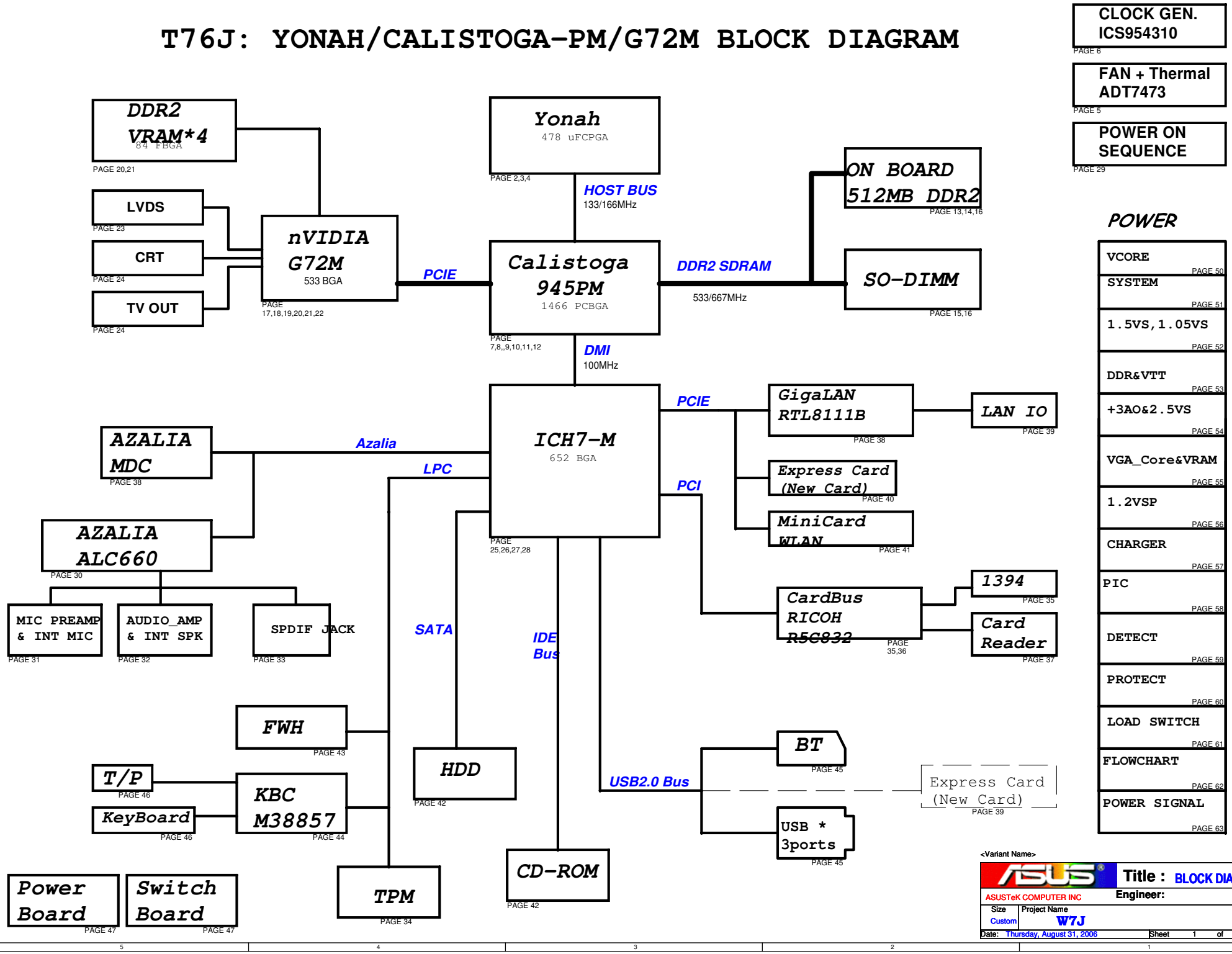
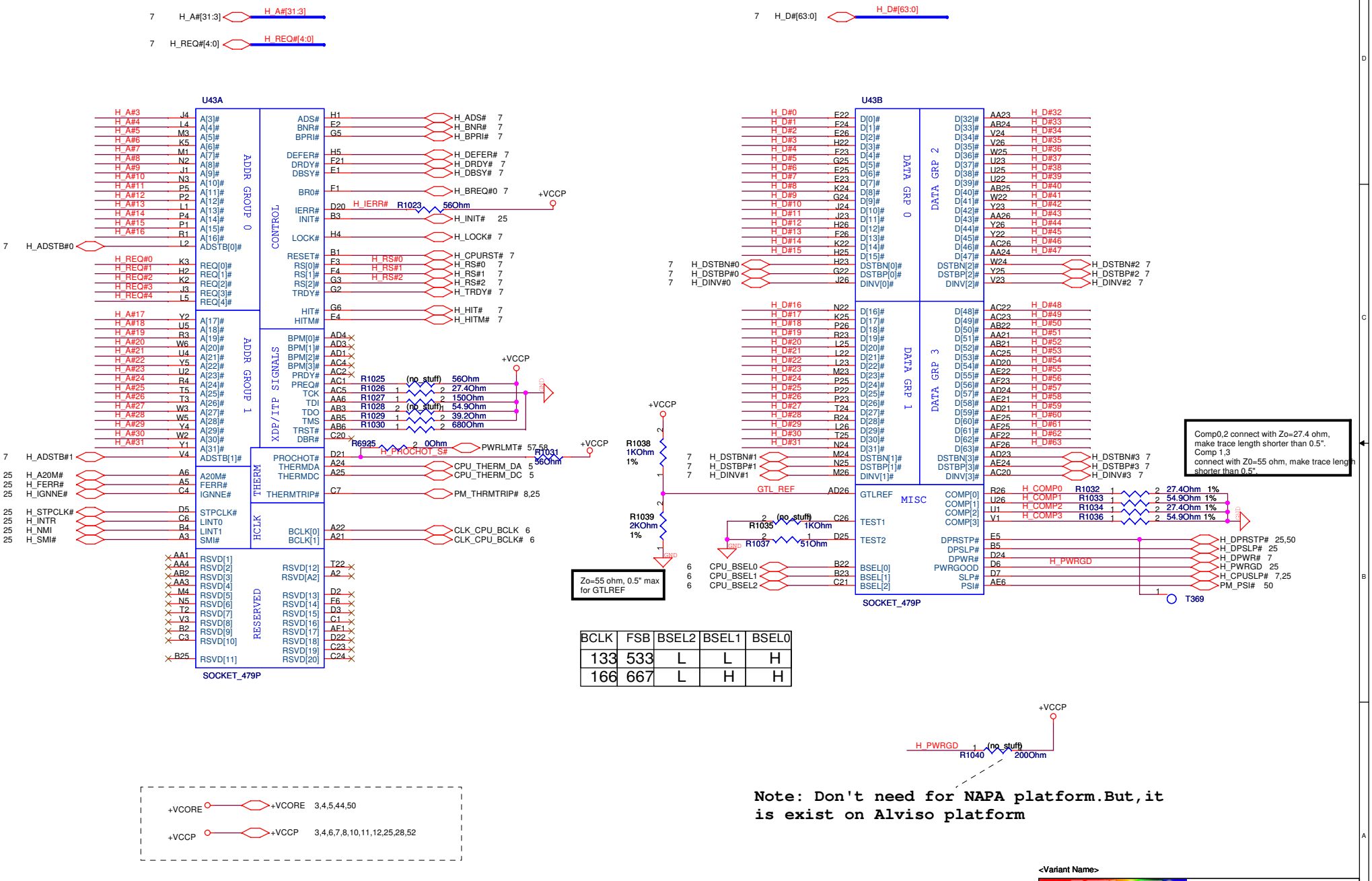
T76J: YONAH/CALISTOGA-PM/G72M BLOCK DIAGRAM





BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Note: Don't need for NAPA platform.But,it is exist on Alviso platform

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

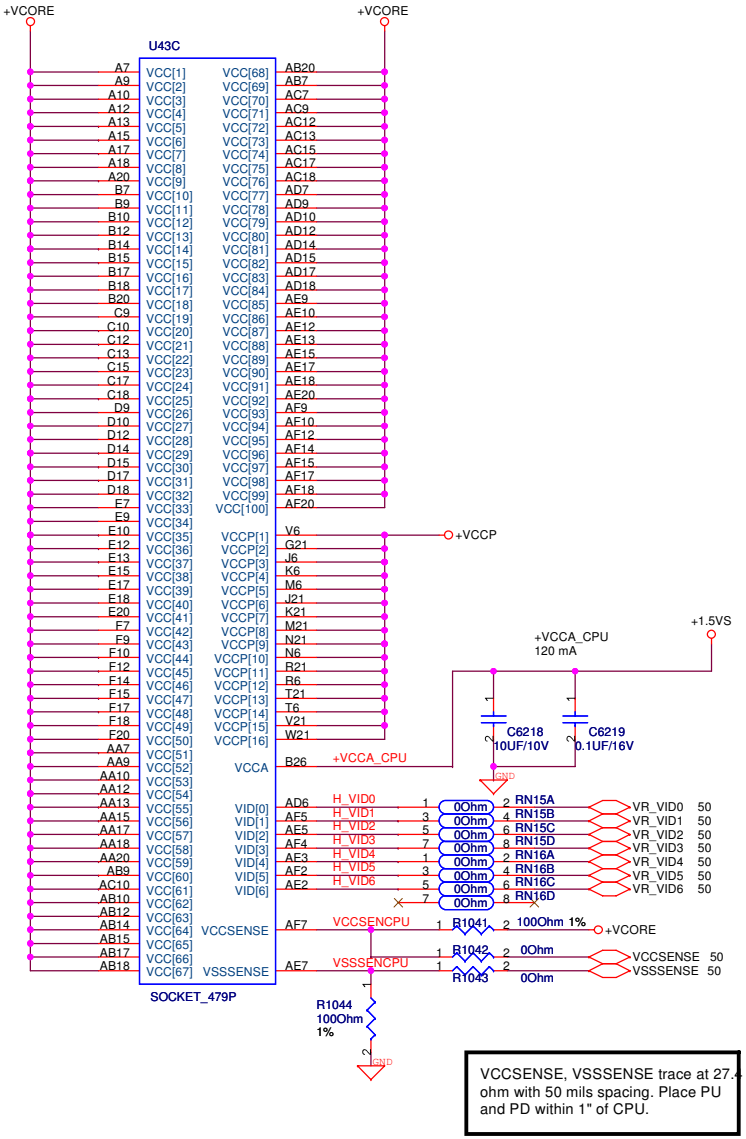
Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

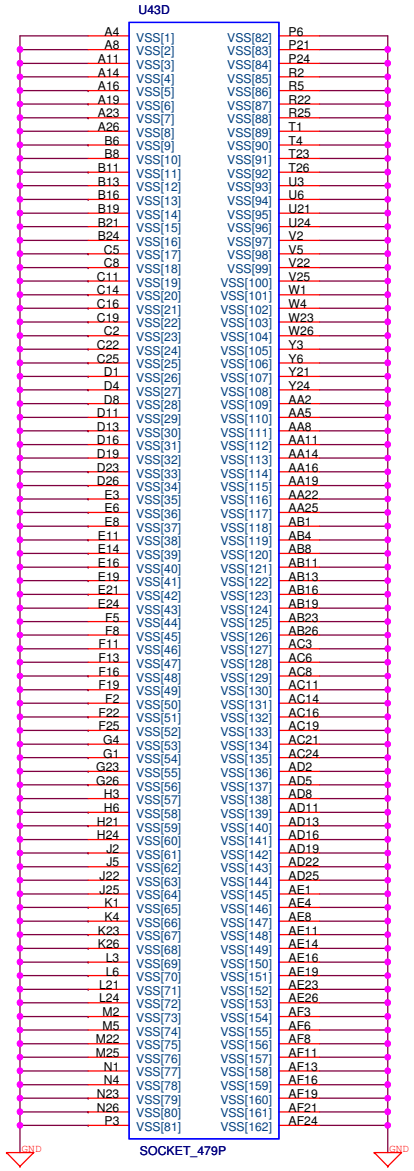
Date: Thursday, August 31, 2006 Sheet 2 of 64

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



<Variant Name>

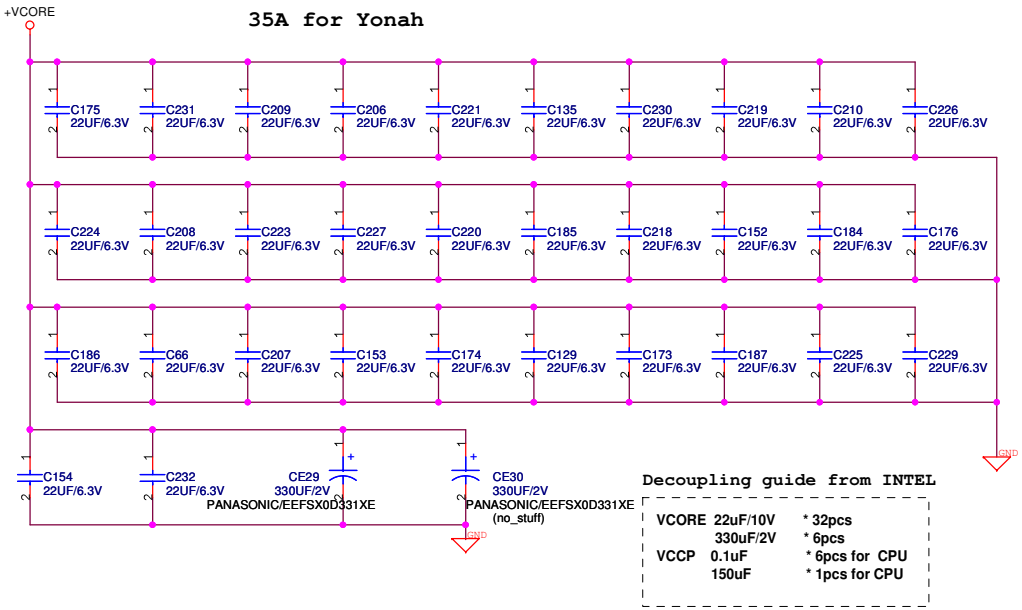
ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

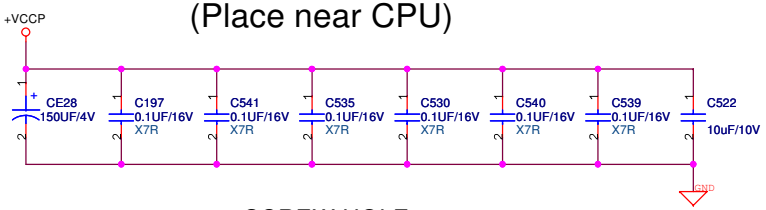
Date: Thursday, August 31, 2006 Sheet 3 of 64



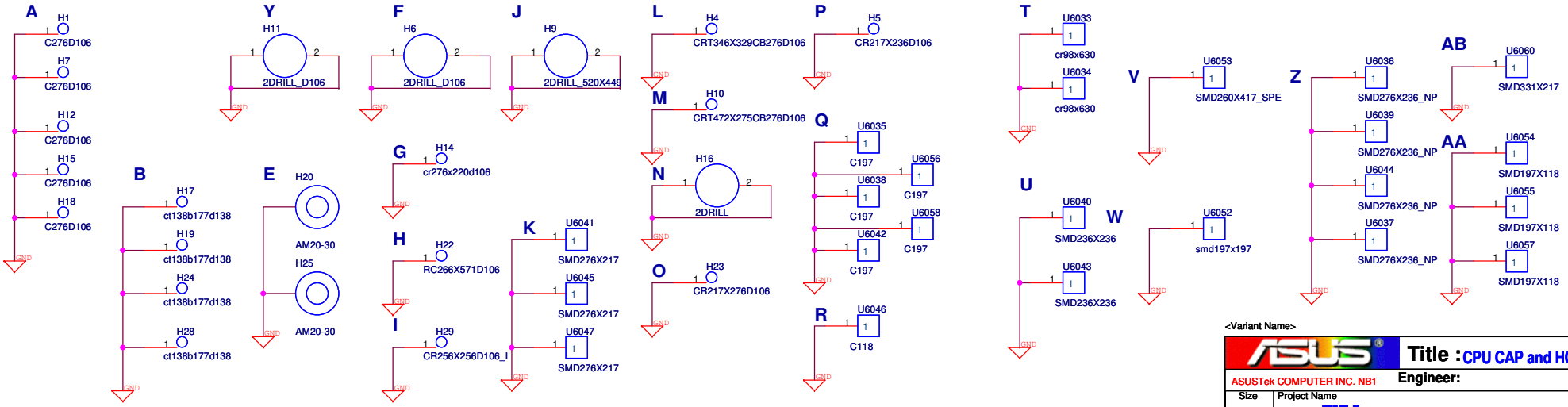
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



SCREW HOLE



<Variant Name>

ASUSTek COMPUTER INC. NB1

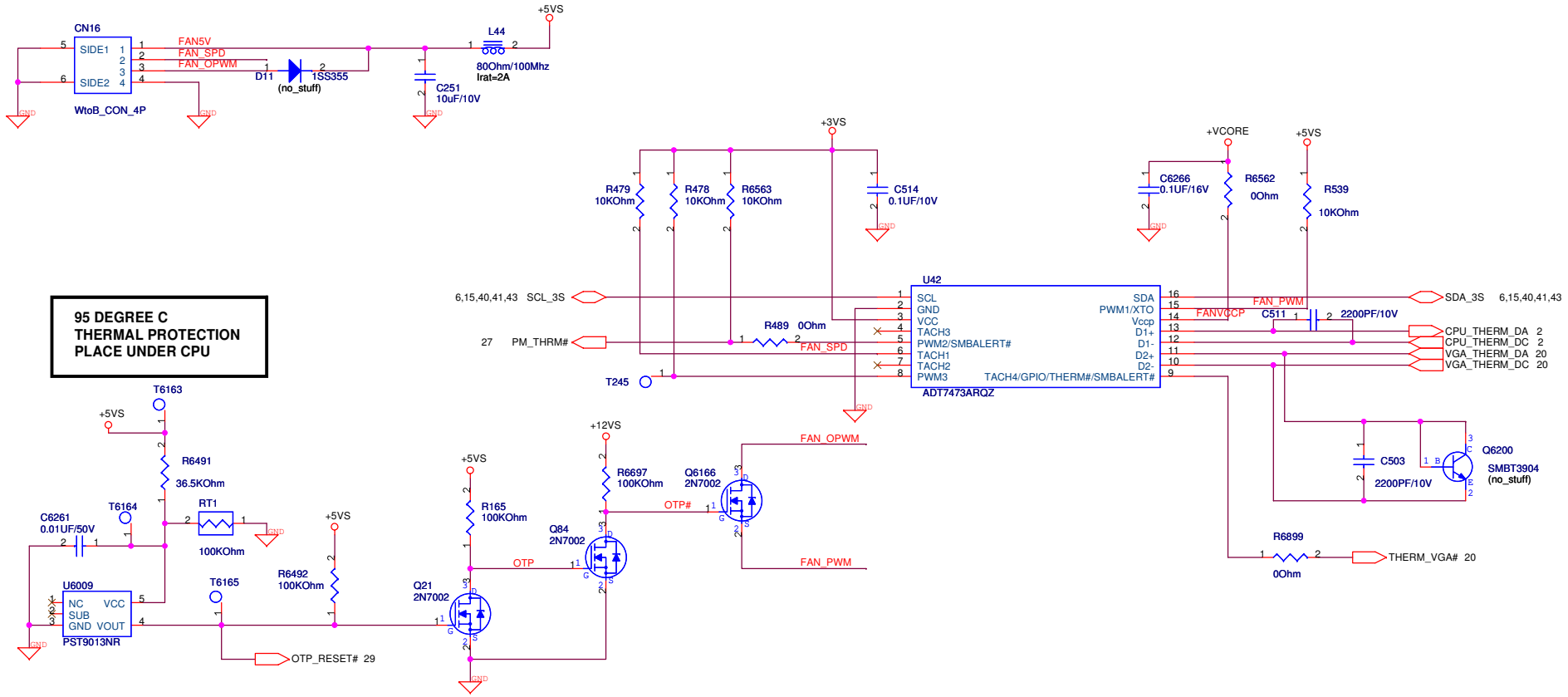
Title : CPU CAP and HOLES

Engineer:

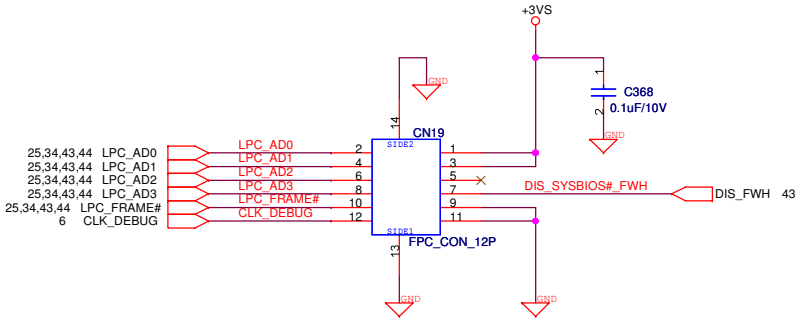
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 4 of 64

FAN & THERMAL CONTROLLER



LPC DEBUG PORT



<Variant Name>

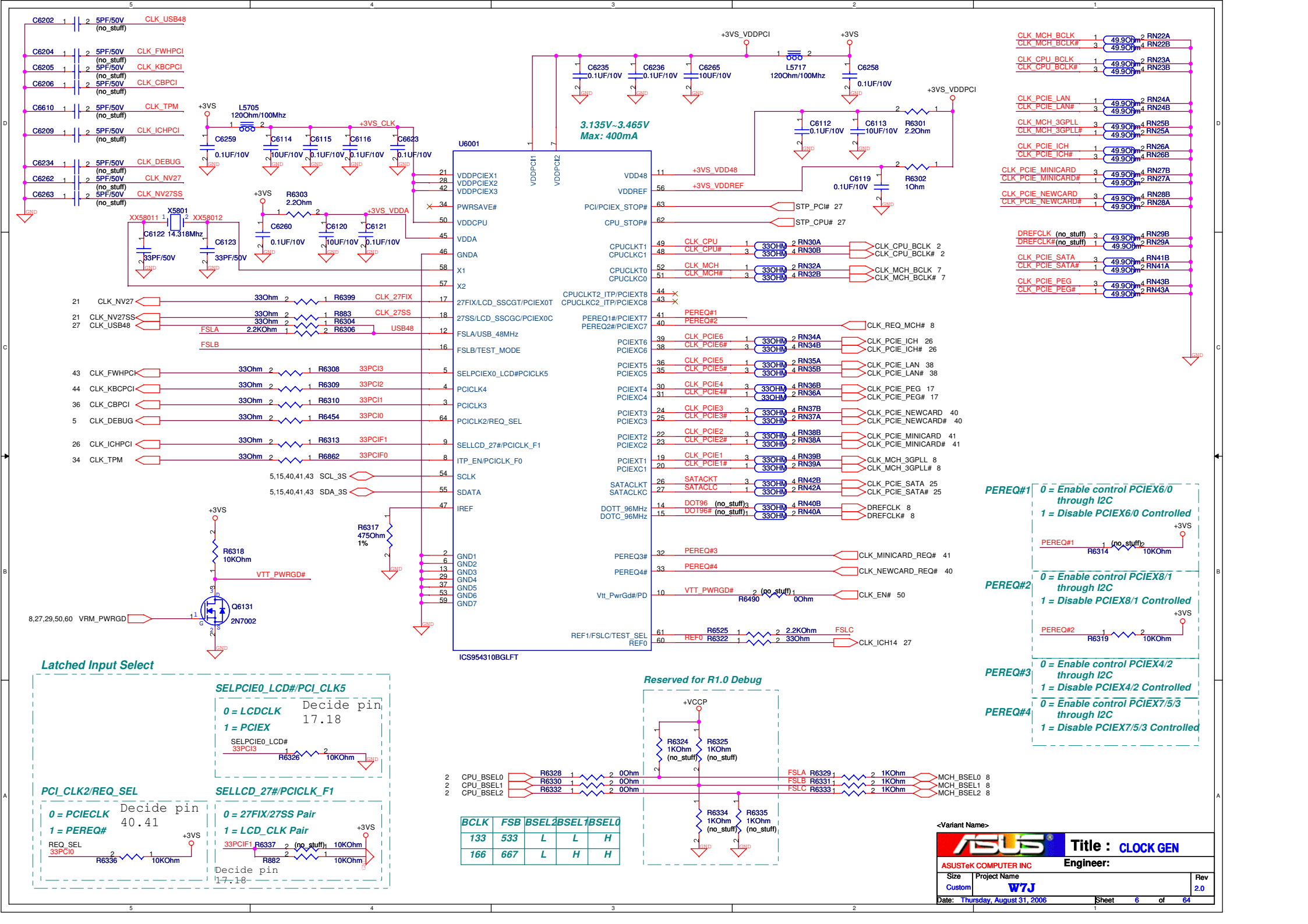
ASUSTeK COMPUTER INC

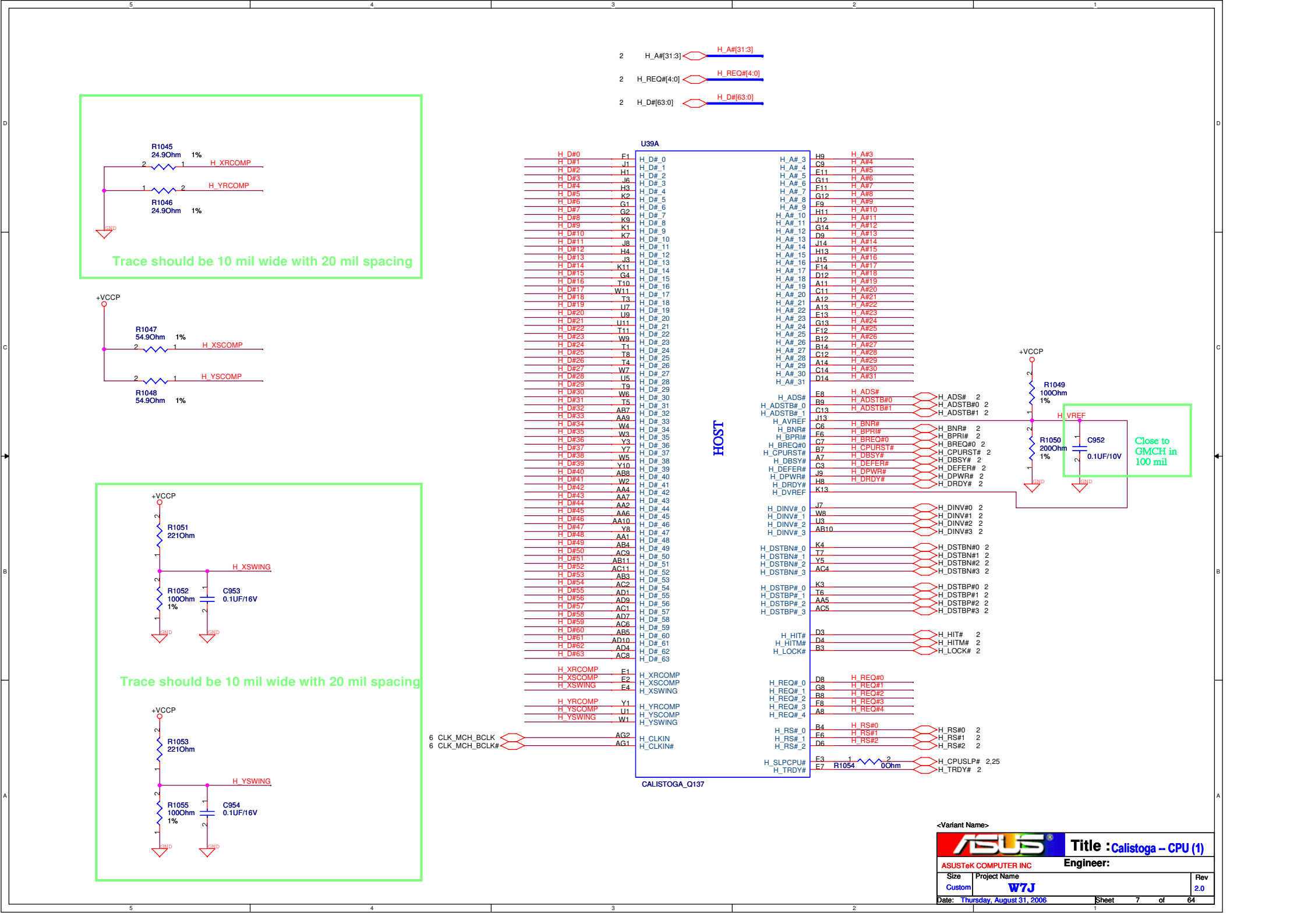
Title : FAN & debug port

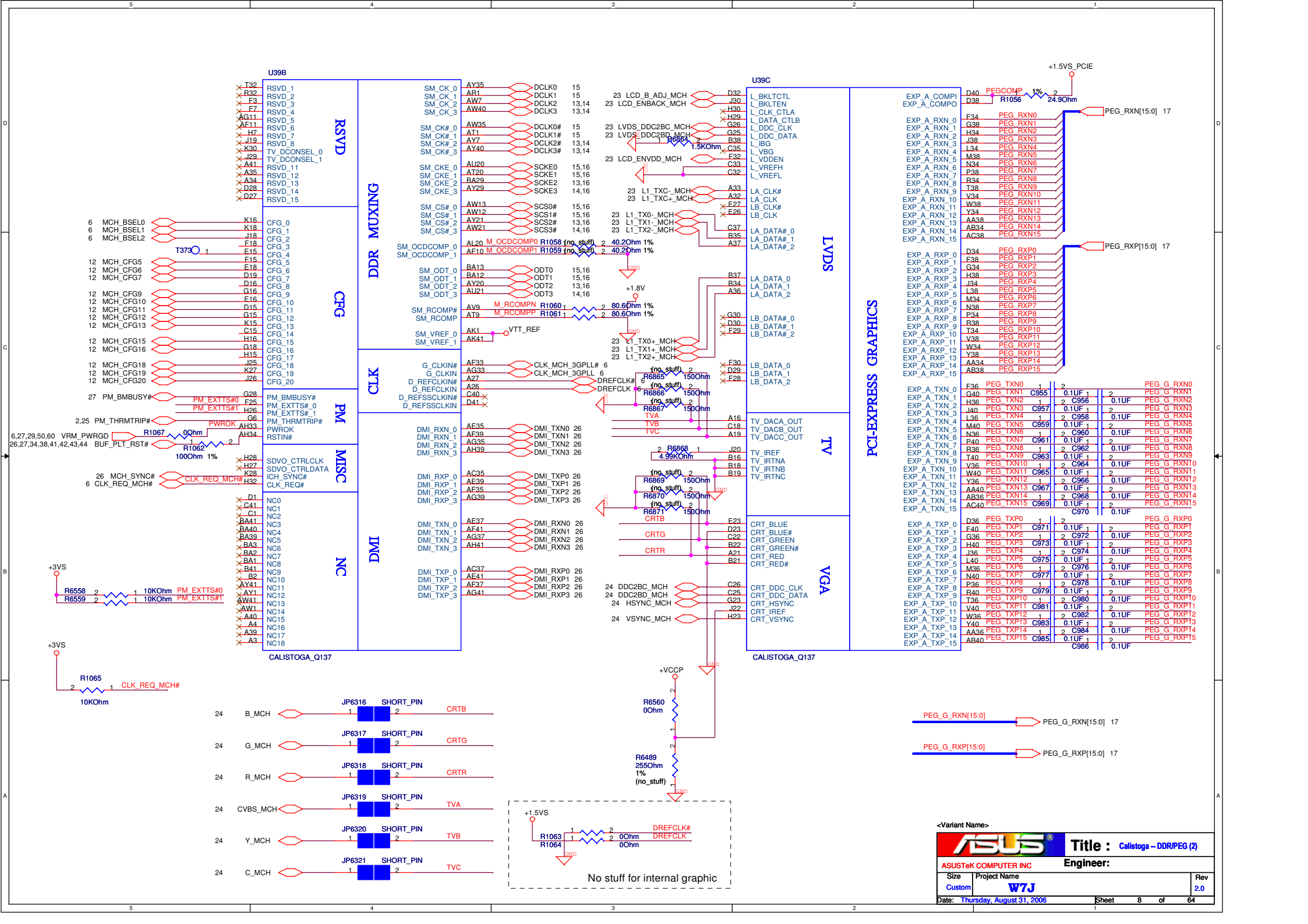
Engineer:

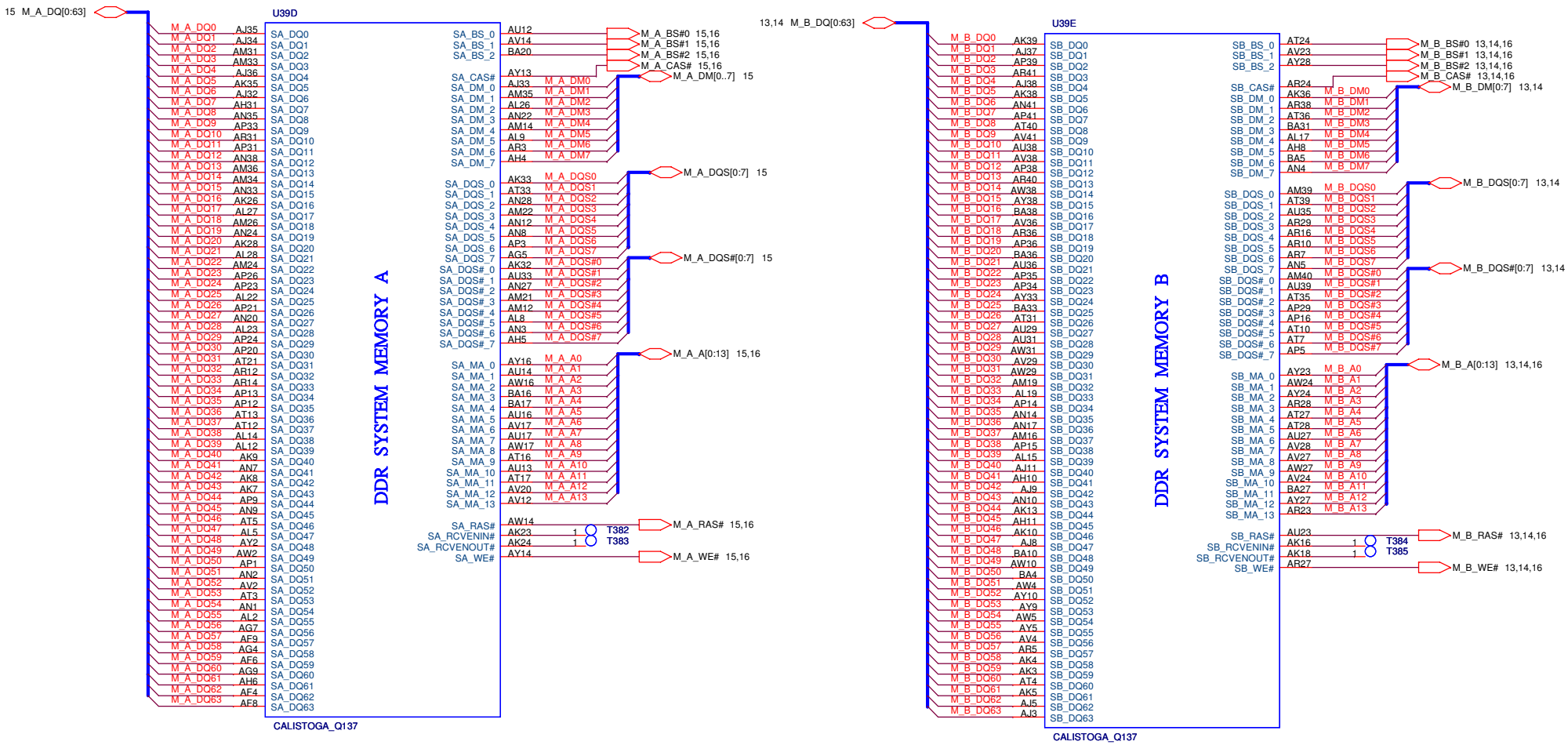
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 5 of 64


U6001
ICS954310BGLFT
3.135V~3.465V
Max: 400mA
Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
PCI_CLK2/REQ_SEL
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27#/PCICLK_F1
0 = 27FIX/27SS Pair
1 = LCD_CLK Pair
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#1
0 = Enable control PCIEX6/0 through I2C
1 = Disable PCIEX6/0 Controlled
PEREQ#2
0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer:
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 6 of 64


R1045
24.9Ohm 1%
H_XRCOMP
H_YRCOMP
R1046
24.9Ohm 1%
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1047
54.9Ohm 1%
H_XSCOMP
H_YSCOMP
R1048
54.9Ohm 1%
+VCCP
R1051
221Ohm
H_XSWING
R1052
100Ohm
1%
C953
0.1UF/16V
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1053
221Ohm
H_YSWING
R1055
100Ohm
1%
C954
0.1UF/16V
GND
2 H_A#[31:3]
H_A#[31:3]
2 H_REQ#[4:0]
H_REQ#[4:0]
2 H_D#[63:0]
H_D#[63:0]
U39A
HOST
CALISTOGA_Q137
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
6 CLK_MCH_BCLK AG2
6 CLK_MCH_BCLK# AG1
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 E9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_AVREF J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_DVREF K13
H_ADS# H_ADS# 2
H_ADSTB#0 H_ADSTB#0 2
H_ADSTB#1 H_ADSTB#1 2
H_BNR# H_BNR# 2
H_BPRI# H_BPRI# 2
H_BREQ#0 H_BREQ#0 2
H_CPURST# H_CPURST# 2
H_DBSY# H_DBSY# 2
H_DEFER# H_DEFER# 2
H_DPWR# H_DPWR# 2
H_DRDY# H_DRDY# 2
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0 2
H_DINV#1 2
H_DINV#2 2
H_DINV#3 2
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0 2
H_DSTBN#1 2
H_DSTBN#2 2
H_DSTBN#3 2
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0 2
H_DSTBP#1 2
H_DSTBP#2 2
H_DSTBP#3 2
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# 2
H_HITM# 2
H_LOCK# 2
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#0 2
H_RS#1 2
H_RS#2 2
H_SLPCPU# E3
H_TRDY# E7
R1054 1 2 0Ohm
H_CPUSLP# 2,25
H_TRDY# 2
+VCCP
R1049
100Ohm
1%
H_VREF
R1050
200Ohm
1%
C952
0.1UF/10V
GND
Close to GMCH in 100 mil
<Variant Name>
Title : Calistoga -- CPU (1)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 7 of 64


U39B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
CALISTOGA_Q137
U39C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
+1.5VS_PCIE
PEG_RXN[15:0] 17
PEG_RXP[15:0] 17
PEG_G_RXN[15:0] 17
PEG_G_RXP[15:0] 17
+3VS
+VCCP
+1.8V
+1.5VS
No stuff for internal graphic
<Variant Name>
Title : Calistoga -- DDR/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 8 of 64



<Variant Name>

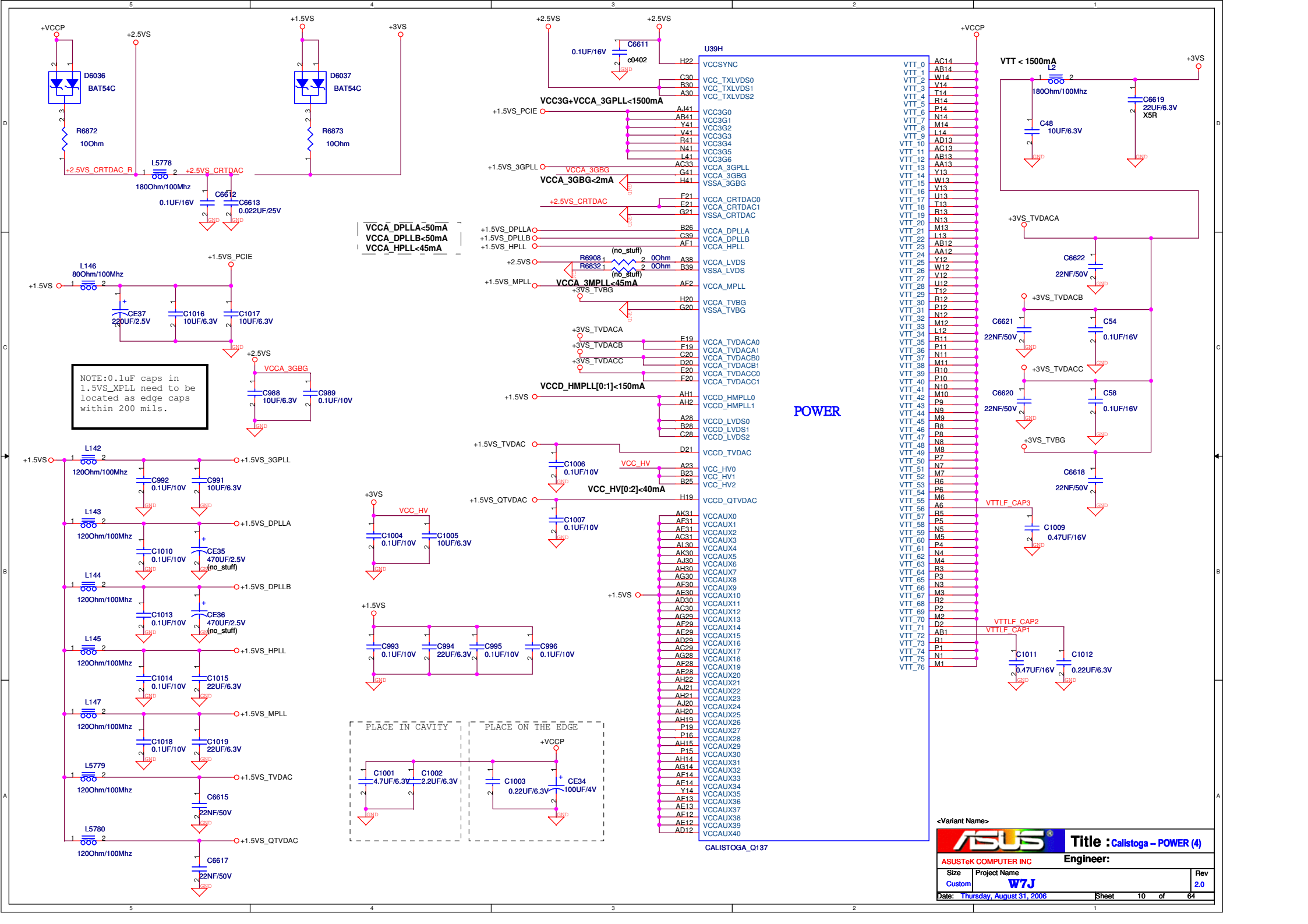
ASUSTeK COMPUTER INC

Title : Calistoga – DDR bus (3)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 9 of 64


+VCCP
+2.5VS
+1.5VS
+3VS
D6036
BAT54C
D6037
BAT54C
R6872
10Ohm
R6873
10Ohm
+2.5VS_CRTDAC_R
L5778
180Ohm/100Mhz
+2.5VS_CRTDAC
C6612
0.1UF/16V
C6613
0.022UF/25V
VCCA_DPLLA<50mA
VCCA_DPLLB<50mA
VCCA_HPLL<45mA
L146
80Ohm/100Mhz
+1.5VS_PCIE
CE37
220UF/2.5V
C1016
10UF/6.3V
C1017
10UF/6.3V
NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
VCCA_3GBG
C988
10UF/6.3V
C989
0.1UF/10V
L142
120Ohm/100Mhz
+1.5VS_3GPLL
C992
0.1UF/10V
C991
10UF/6.3V
L143
+1.5VS_DPLLA
C1010
0.1UF/10V
CE35
470UF/2.5V
(no_stuff)
L144
+1.5VS_DPLLB
C1013
0.1UF/10V
CE36
470UF/2.5V
(no_stuff)
L145
+1.5VS_HPLL
C1014
0.1UF/10V
C1015
22UF/6.3V
L147
+1.5VS_MPLL
C1018
0.1UF/10V
C1019
22UF/6.3V
L5779
+1.5VS_TVDAC
C6615
22NF/50V
L5780
+1.5VS_QTVDAC
C6617
22NF/50V
C6611
0.1UF/16V
c0402
U39H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G+VCCA_3GPLL<1500mA
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_3GBG<2mA
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
R6908
R6832
0Ohm
(no_stuff)
VCCA_LVDS
VSSA_LVDS
VCCA_3MPLL<45mA
VCCA_MPLL
+3VS_TVBG
VCCA_TVBG
VSSA_TVBG
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL[0:1]<150mA
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
C1006
0.1UF/10V
VCC_HV
VCC_HV0
VCC_HV1
VCC_HV2
VCC_HV[0:2]<40mA
VCCD_QTVDAC
C1007
0.1UF/10V
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
CALISTOGA_Q137
POWER
C1004
0.1UF/10V
C1005
10UF/6.3V
C993
0.1UF/10V
C994
22UF/6.3V
C995
0.1UF/10V
C996
0.1UF/10V
PLACE IN CAVITY
C1001
4.7UF/6.3V
C1002
2.2UF/6.3V
PLACE ON THE EDGE
C1003
0.22UF/6.3V
CE34
100UF/4V
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VTT_26
VTT_27
VTT_28
VTT_29
VTT_30
VTT_31
VTT_32
VTT_33
VTT_34
VTT_35
VTT_36
VTT_37
VTT_38
VTT_39
VTT_40
VTT_41
VTT_42
VTT_43
VTT_44
VTT_45
VTT_46
VTT_47
VTT_48
VTT_49
VTT_50
VTT_51
VTT_52
VTT_53
VTT_54
VTT_55
VTT_56
VTT_57
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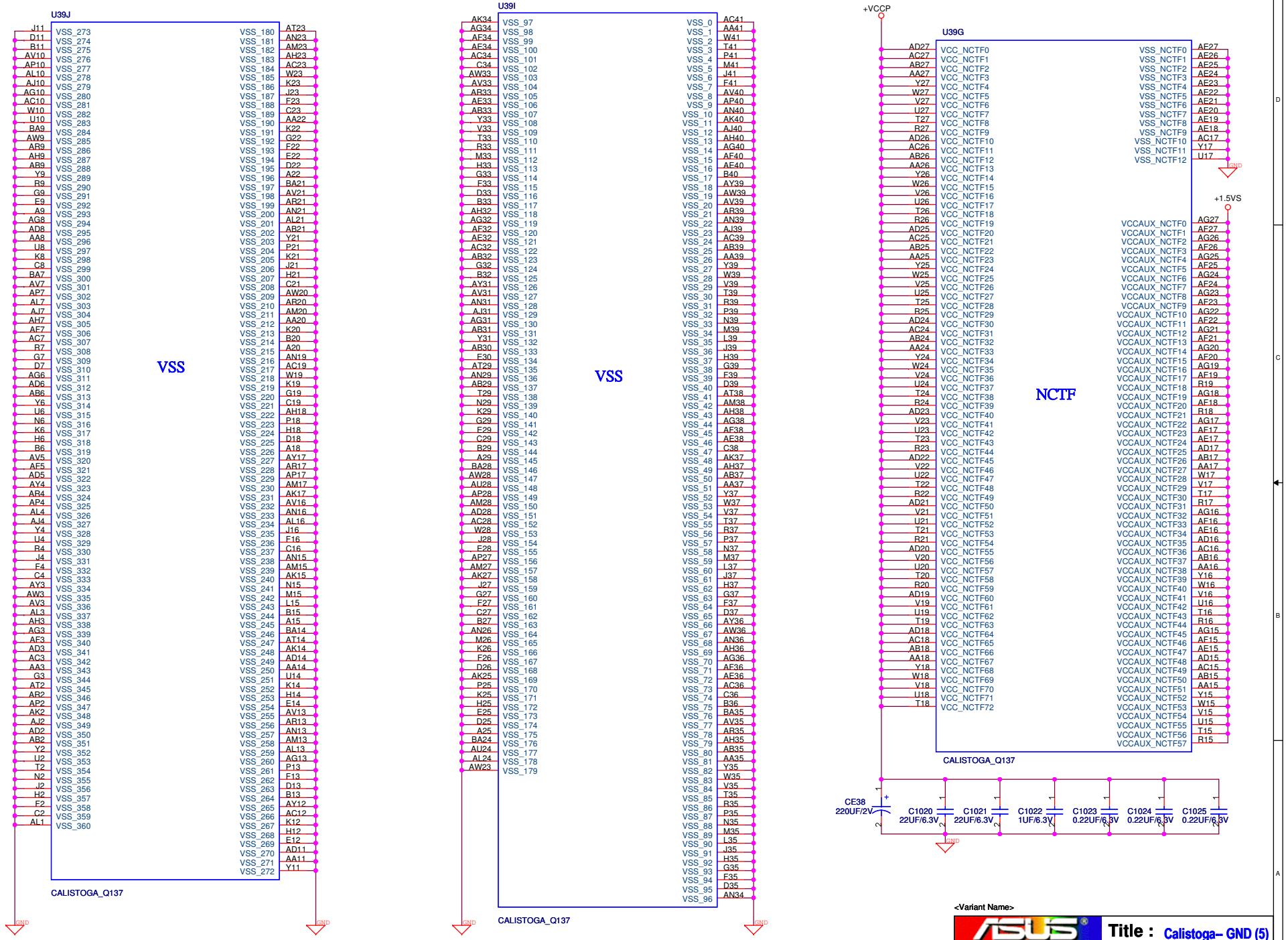
VTT_59
VTT_60
VTT_61
VTT_62
VTT_63
VTT_64
VTT_65
VTT_66
VTT_67
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VTT < 1500mA
L2
180Ohm/100Mhz
C48
10UF/6.3V
C6619
22UF/6.3V
X5R
C6622
22NF/50V
C6621
22NF/50V
C54
0.1UF/16V
C6620
22NF/50V
C58
0.1UF/16V
C6618
22NF/50V
VTTLF_CAP3
C1009
0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C1011
0.47UF/16V
C1012
0.22UF/6.3V
<Variant Name>
Title : Calistoga – POWER (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
2.0
Date: Thursday, August 31, 2006
Sheet 10 of 64



<Variant Name>

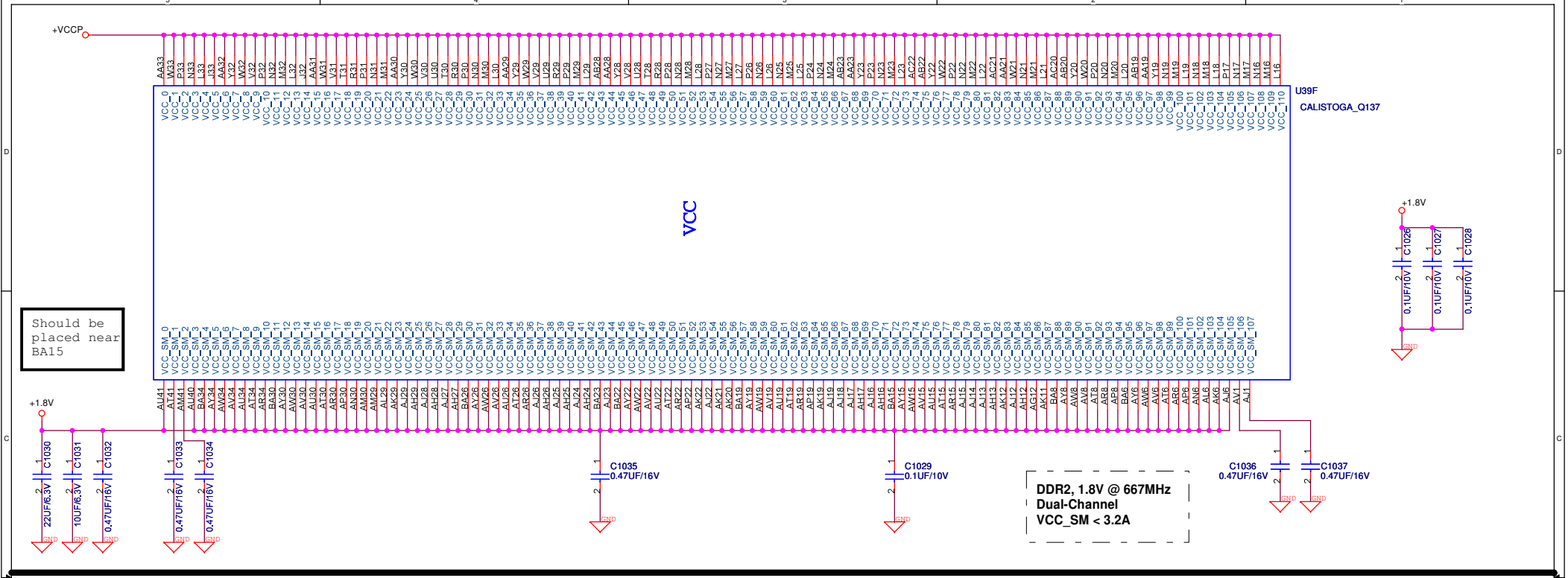
ASUSTeK COMPUTER INC

Title : Calistoga– GND (5)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 11 of 64



8 MCH_CFG5

R1069 2.2KOhm (no_stuff)

CFG5 : DMI STRAP

LOW = DMI X 2

HIGH = DMI X 4 (Default)

8 MCH_CFG9

R1077 2.2KOhm

CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

HIGH = NORMAL OPERATION (Default)

8 MCH_CFG15

R1078 2.2KOhm (no_stuff)

CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE

HIGH = NORMAL OPERATION

8 MCH_CFG12

8 MCH_CFG13

R1076 2.2KOhm (no_stuff)

R1072 2.2KOhm (no_stuff)

8 MCH_CFG6

R6479 2.2KOhm (no_stuff)

CFG6 : DDR STRAP

LOW = Moby Dick

HIGH = Calistoga (Default)

8 MCH_CFG10

R1070 2.2KOhm (no_stuff)

CFG10: HOST PLL VCO SELECT

LOW = RESERVED

HIGH = MOBILITY

8 MCH_CFG16

R1071 2.2KOhm (no_stuff)

CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled

HIGH = Dynamic ODT Enabled (Default)

+3VS

R1079 1KOhm (no_stuff)

CFG19 : DMI LANE REVERSAL

LOW = NORMAL

HIGH = LANES REVERSED

8 MCH_CFG19

8 MCH_CFG7

R1075 2.2KOhm (no_stuff)

CFG7 : CPU STRAP

LOW = RSVD

HIGH = Mobile CPU (Default)

8 MCH_CFG11

R1073 2.2KOhm (no_stuff)

CFG11 : PSB 4X CLK ENABLE

LOW = Reserved

HIGH = Calistoga (Default)

CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)

HIGH = 1.5V

+3VS

R1074 1KOhm (no_stuff)

8 MCH_CFG18

CFG20 : PCIE Backward Interpoerability mode

LOW = only SDVO or PCIE*1 isoperational (default)

HIGH = SDVO and PCIE*1 are operating simulaneously via the PEG port

+3VS

R6480 1KOhm (no_stuff)

8 MCH_CFG20

<Variant Name>

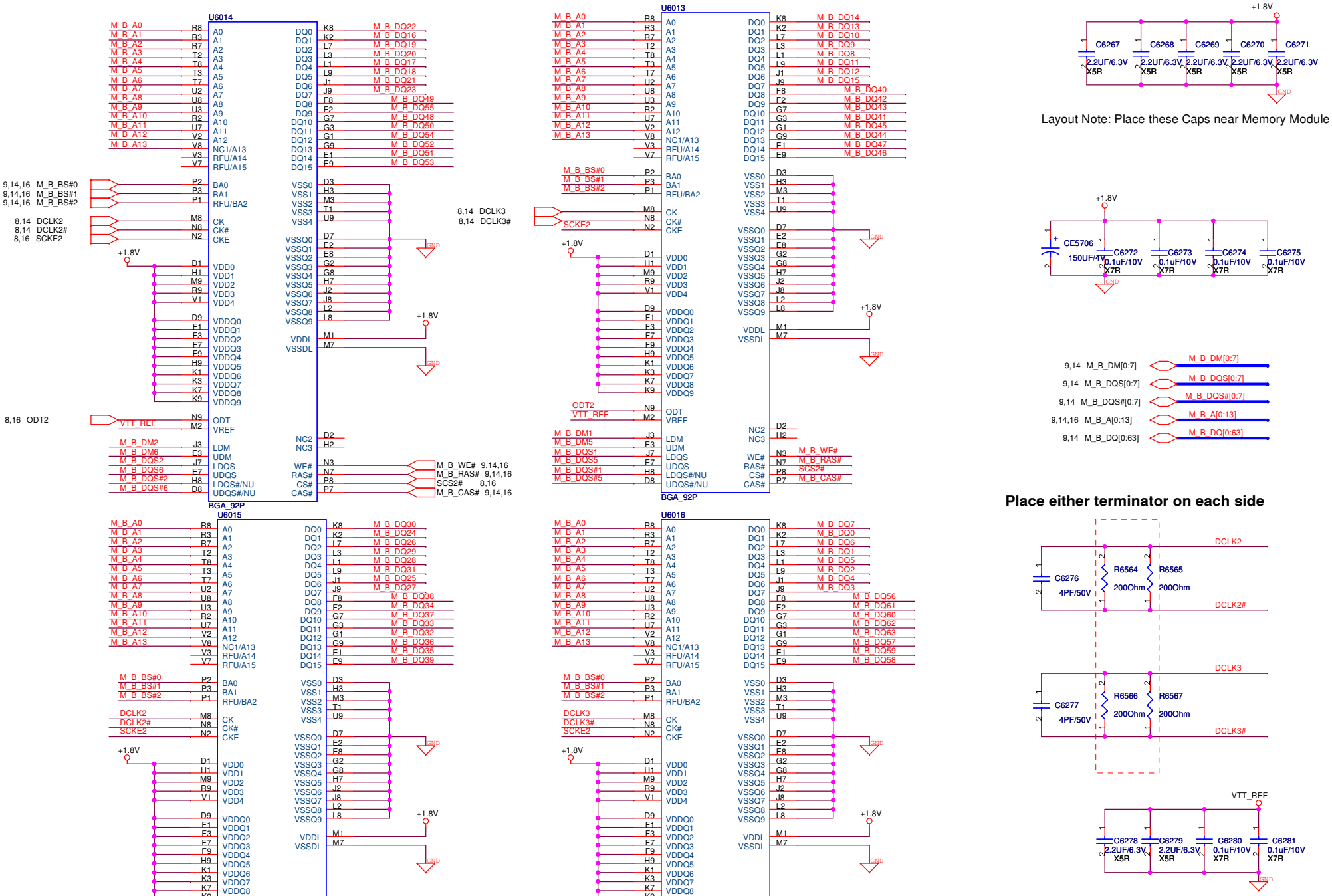
ASUSTeK COMPUTER INC

Title : Calistoga– GND (6)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 12 of 64



<Variant Name>

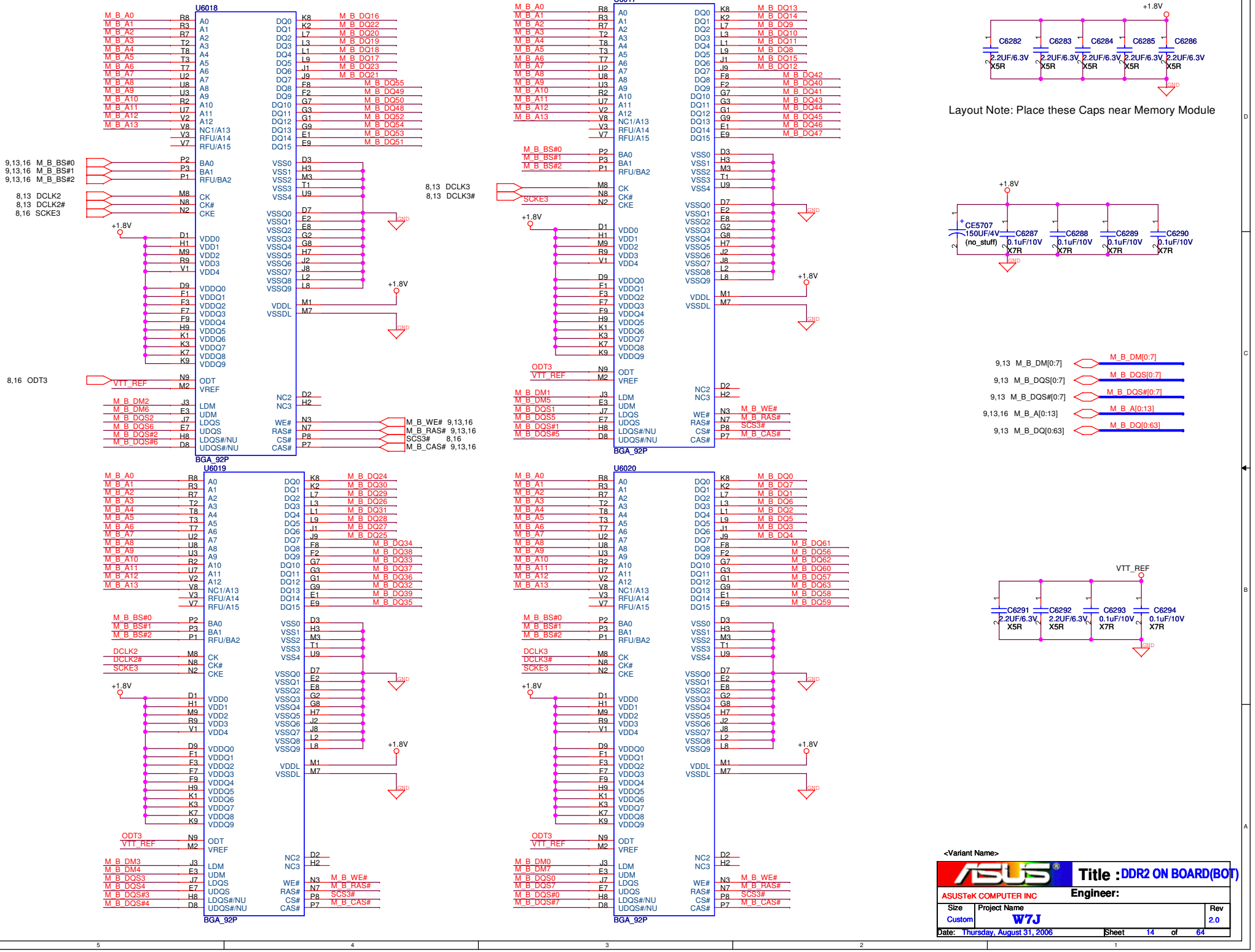
ASUSTeK COMPUTER INC

Title : DDRON BOARD(TOP)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 13 of 64


U6018
U6017
U6019
U6020
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
DCLK3
DCLK3#
SCKE3
ODT3
VTT_REF
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7
M_B_DQ16
M_B_DQ17
M_B_DQ18
M_B_DQ19
M_B_DQ20
M_B_DQ21
M_B_DQ22
M_B_DQ23
M_B_DQ24
M_B_DQ25
M_B_DQ26
M_B_DQ27
M_B_DQ28
M_B_DQ29
M_B_DQ30
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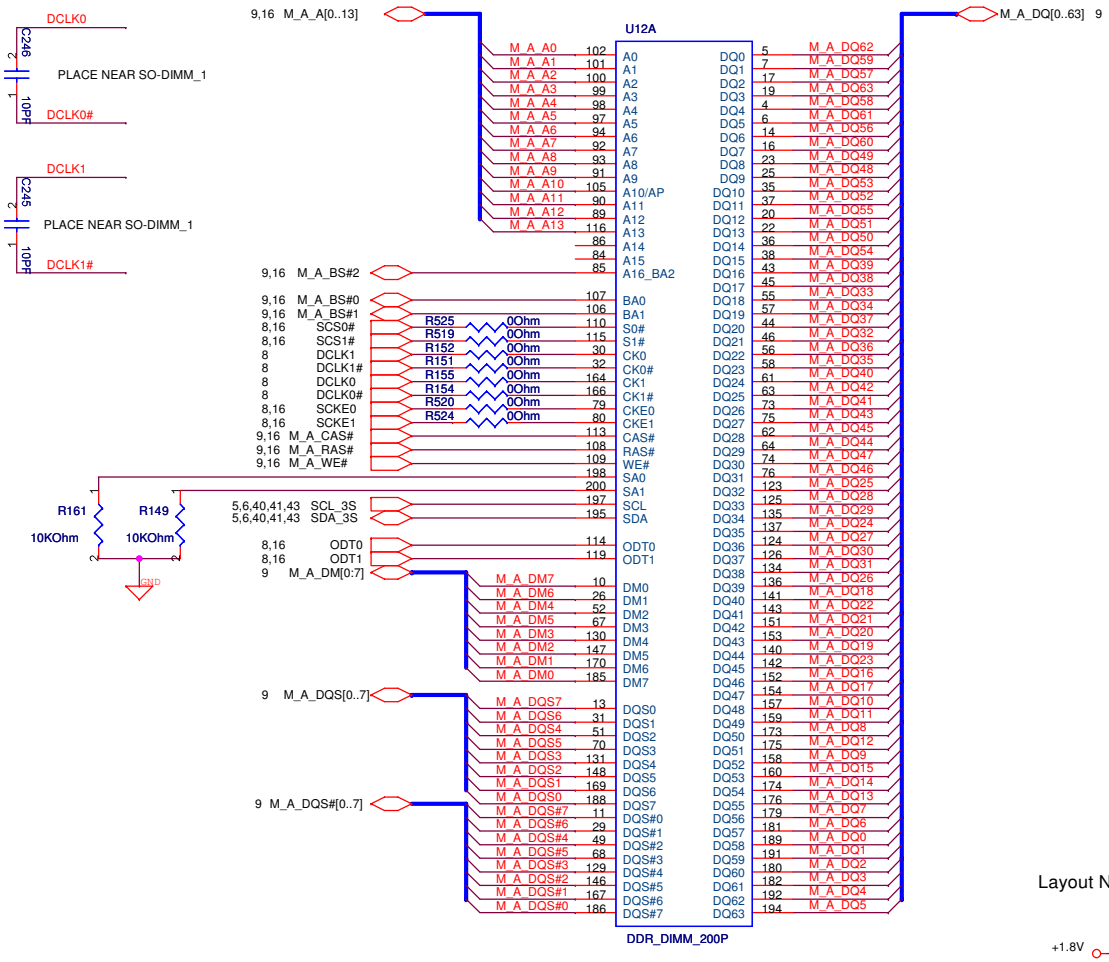
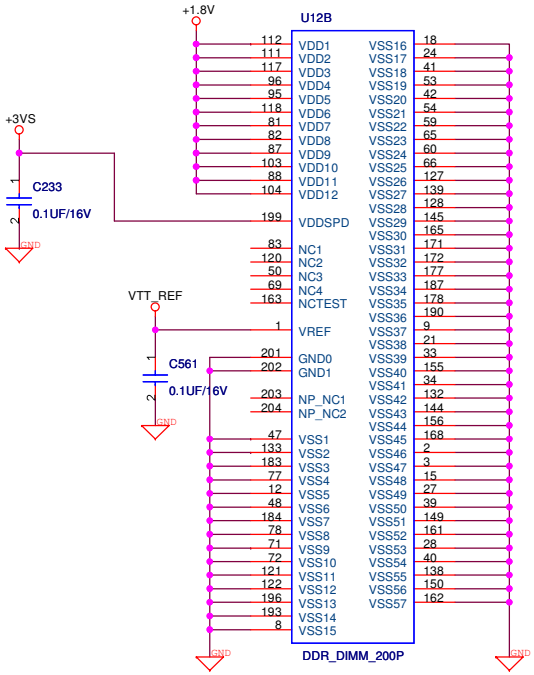
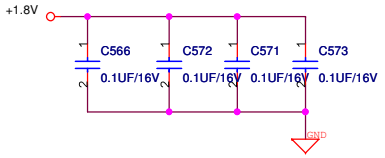
M_B_DQ59
M_B_DQ60
M_B_DQ61
M_B_DQ62
M_B_DQ63
M_B_DQ0
M_B_DQ1
M_B_DQ2
M_B_DQ3
M_B_DQ4
M_B_DQ5
M_B_DQ6
M_B_DQ7
M_B_DQ8
M_B_DQ9
M_B_DQ10
M_B_DQ11
M_B_DQ12
M_B_DQ13
M_B_DQ14
M_B_DQ15
M_B_WE#
M_B_RAS#
M_B_CAS#
SCS3#
+1.8V
GND
C6282
C6283
C6284
C6285
C6286
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5707
150UF/4V
(no_stuff)
C6287
C6288
C6289
C6290
0.1uF/10V
X7R
M_B_DM[0:7]
M_B_DQS[0:7]
M_B_DQS#[0:7]
M_B_A[0:13]
M_B_DQ[0:63]
C6291
C6292
C6293
C6294
<Variant Name>
Title : DDR2 ON BOARD(BOT)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
2.0
Date: Thursday, August 31, 2006
Sheet 14 of 64



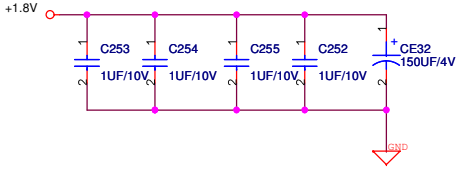
Top SO-DIMM:
12-025122005



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1



TOP SIDE:
Channel A

<Variant Name>

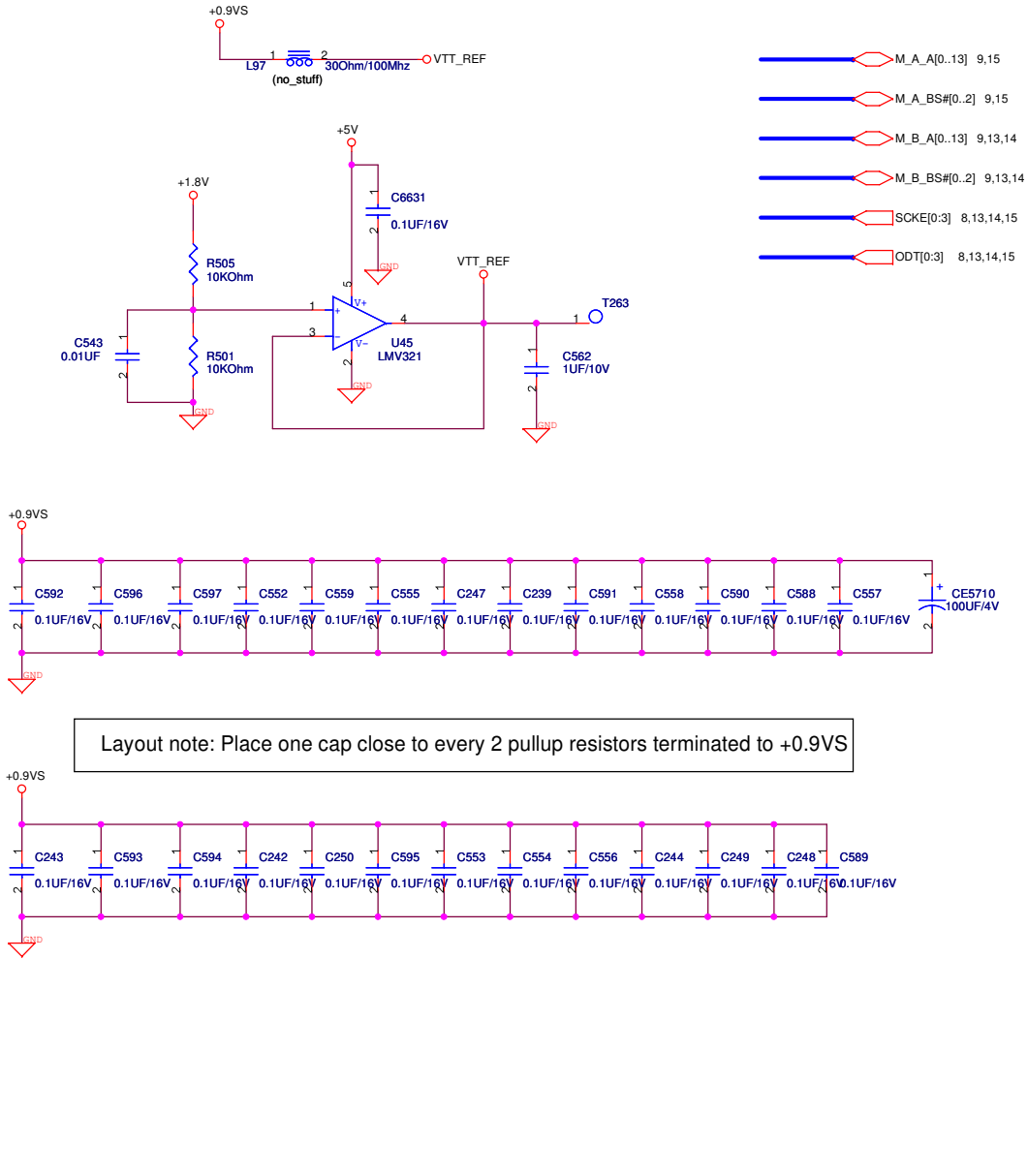
Title : DDR2 SO-DIMM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 15 of 64



<Variant Name>

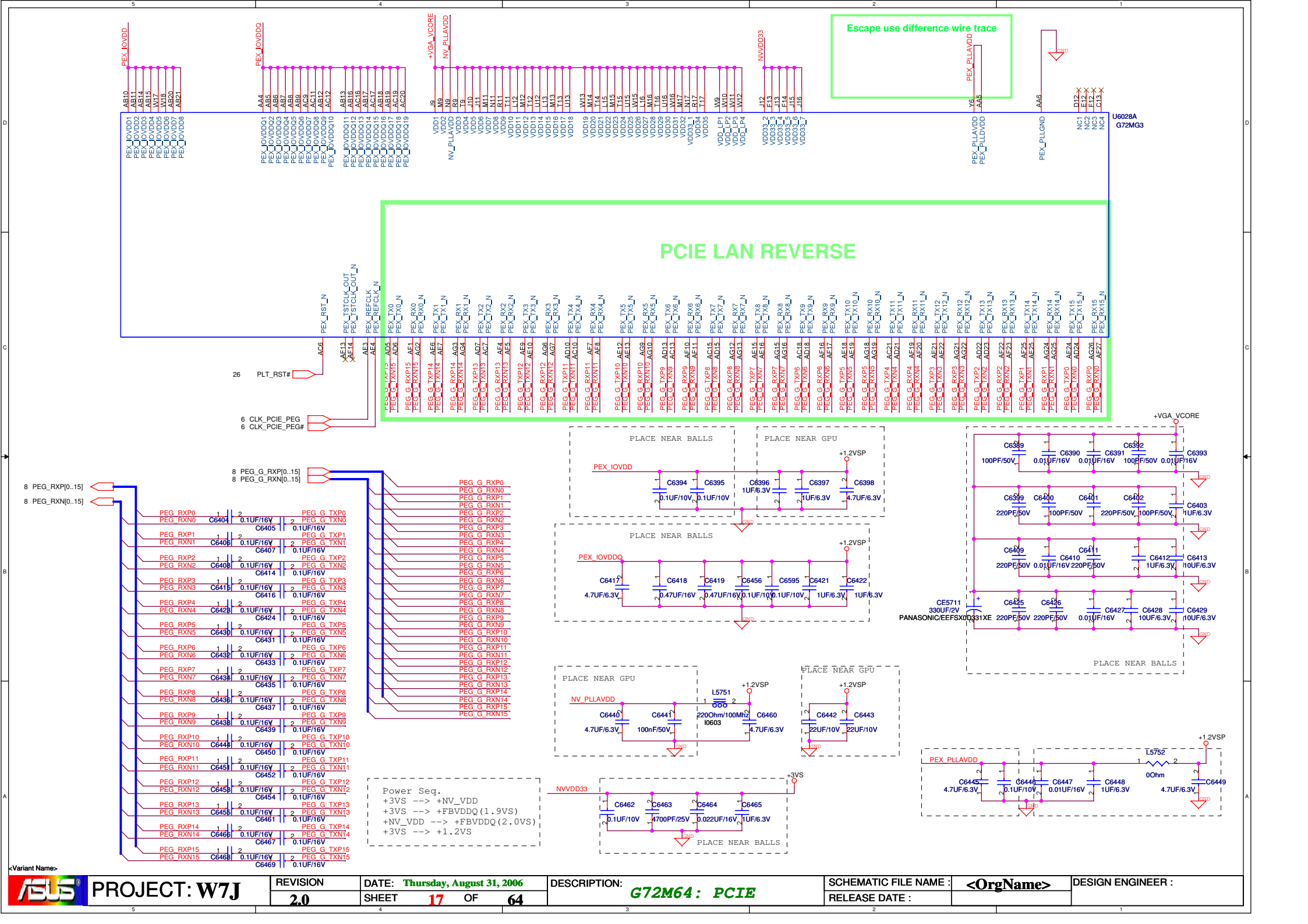
ASUSTeK COMPUTER INC

Title : DDR2 ADDR TERM

Engineer:

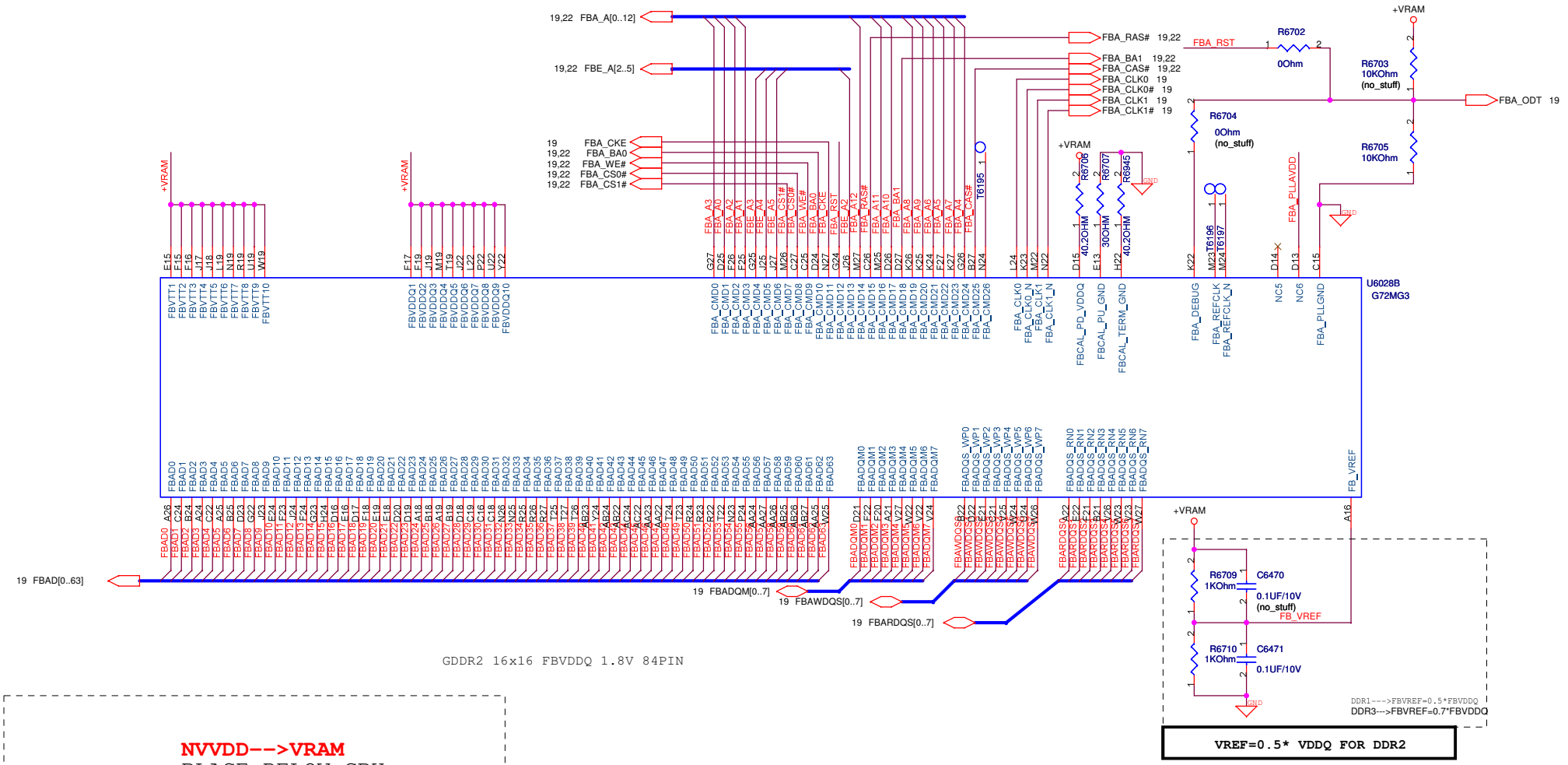
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 16 of 64



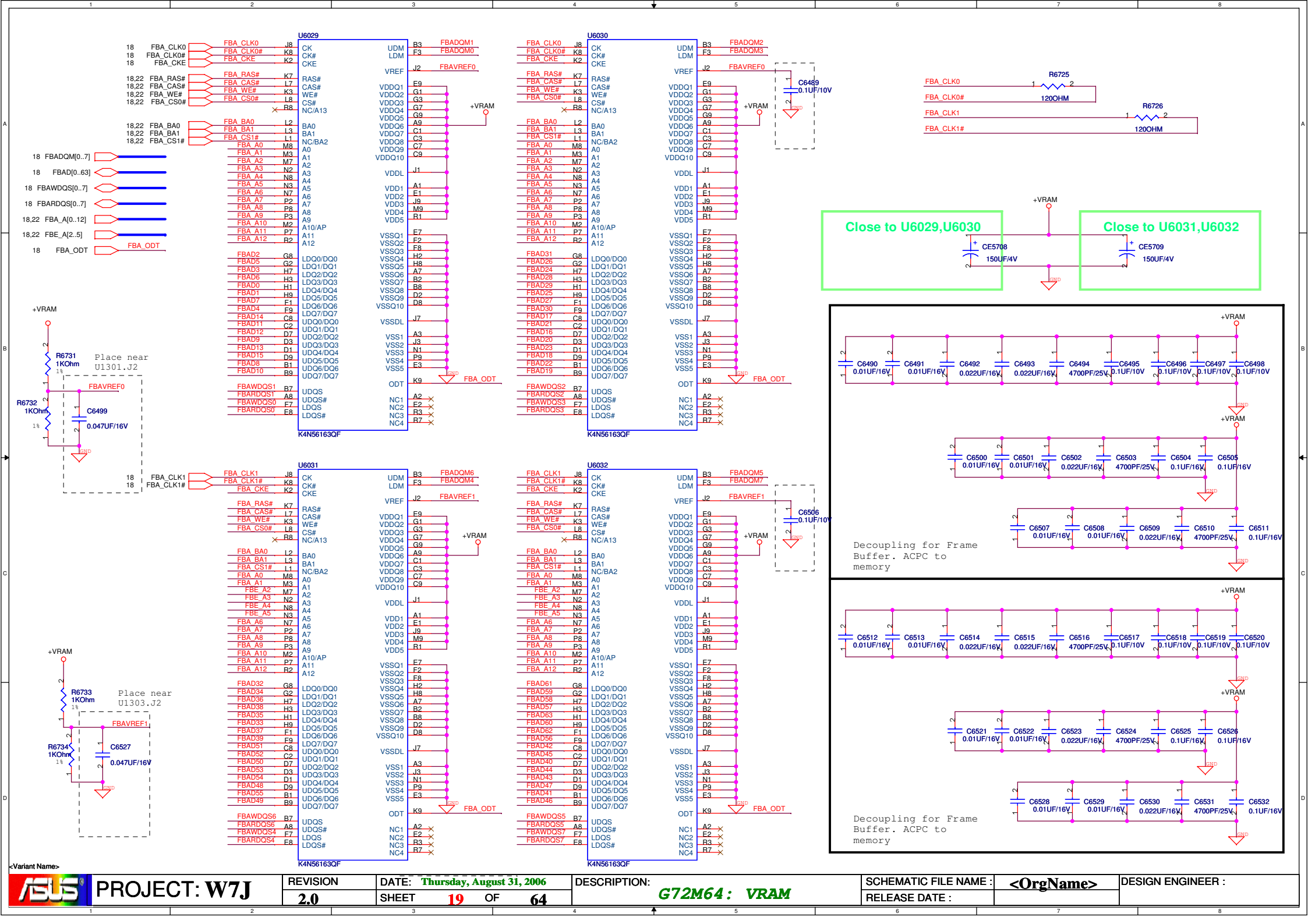
<Variant Name>

PROJECT: W7J	REVISION	DATE: Thursday, August 31, 2006	DESCRIPTION: G72M64 : PCIE	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	2.0	SHEET 17 OF 64		RELEASE DATE :	



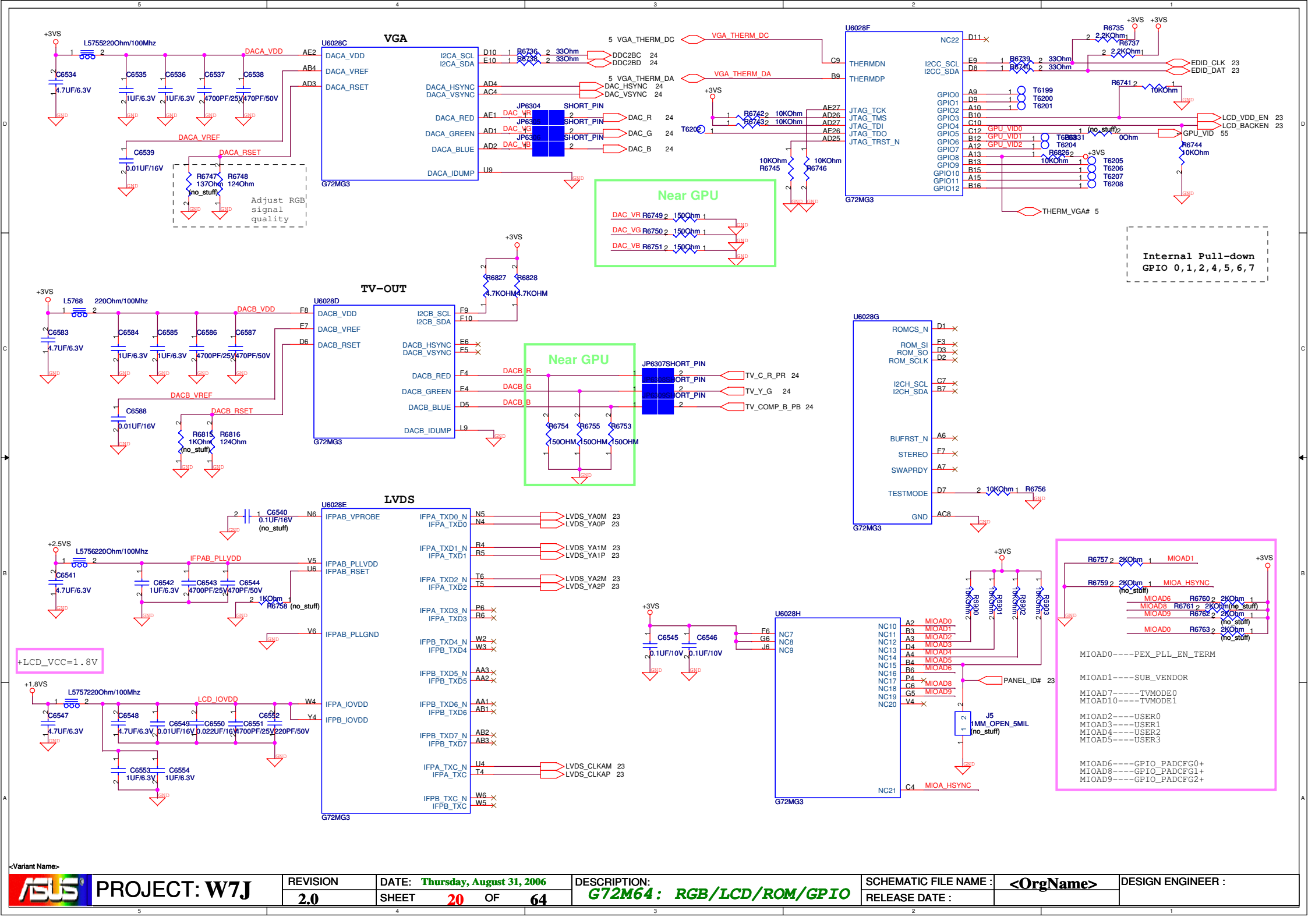
<Variant Name>

PROJECT: W7J	REVISION	DATE: Thursday, August 31, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.0	SHEET 18 OF 64	G72M64 : FB	RELEASE DATE :	<OrgName>



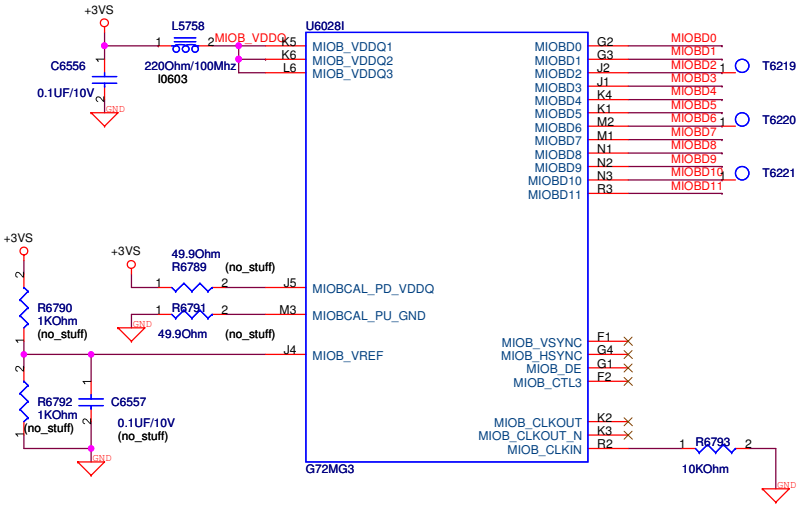
<Variant Name>

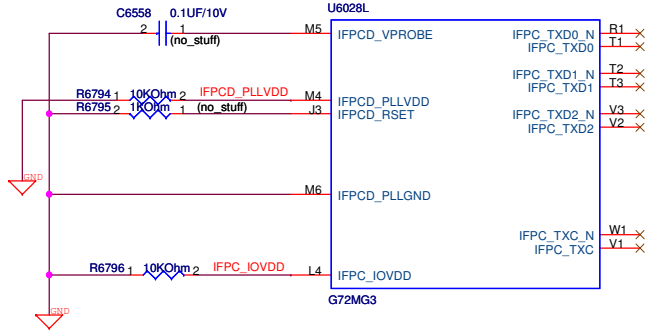
PROJECT: W7J	REVISION 2.0	DATE: Thursday, August 31, 2006	DESCRIPTION: G72M64 : VRAM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 19 OF 64		RELEASE DATE :	

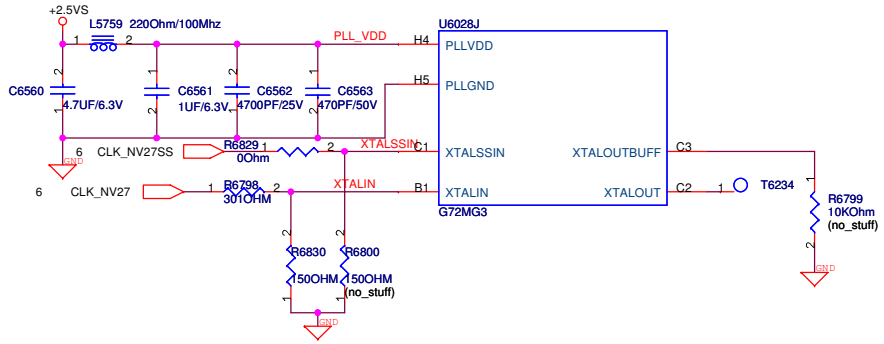


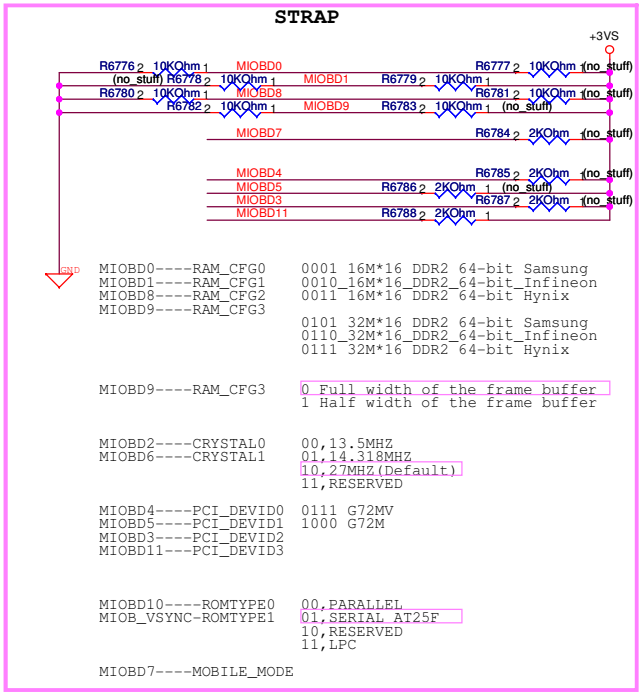
<Variant Name>

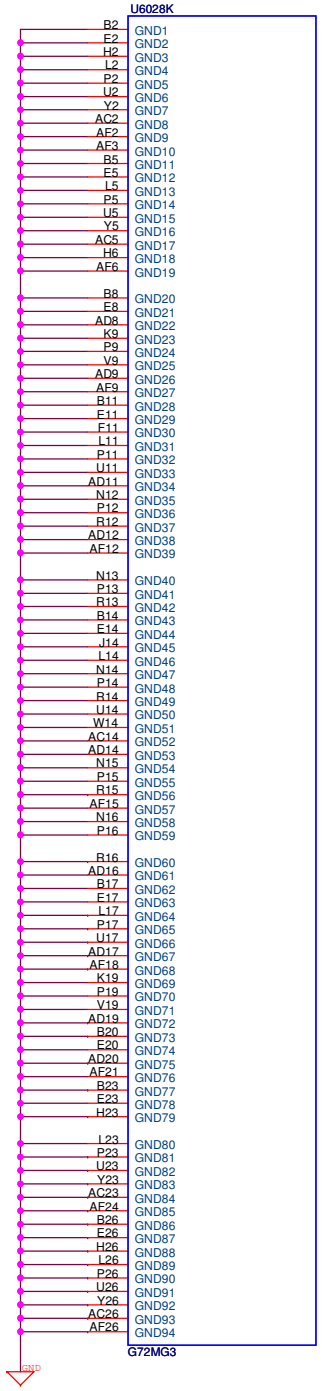
PROJECT: W7J	REVISION	DATE: Thursday, August 31, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.0	SHEET 20 OF 64	G72M64: RGB/LCD/ROM/GPIO	RELEASE DATE :	<OrgName>







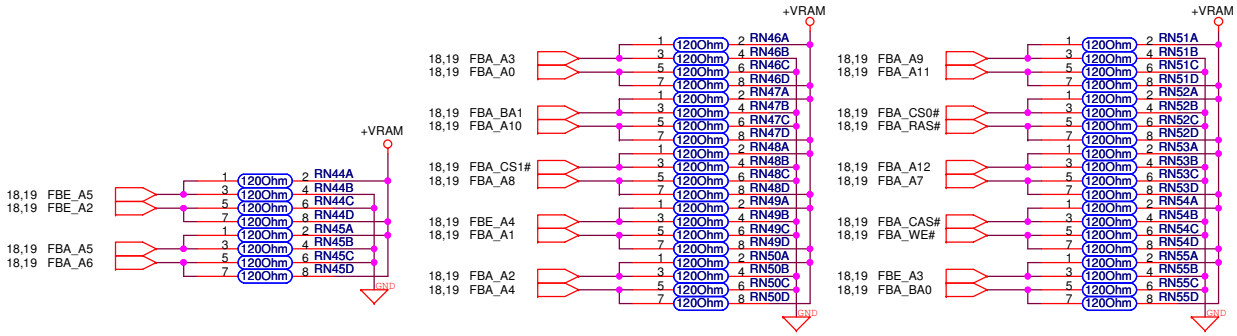




<Variant Name>

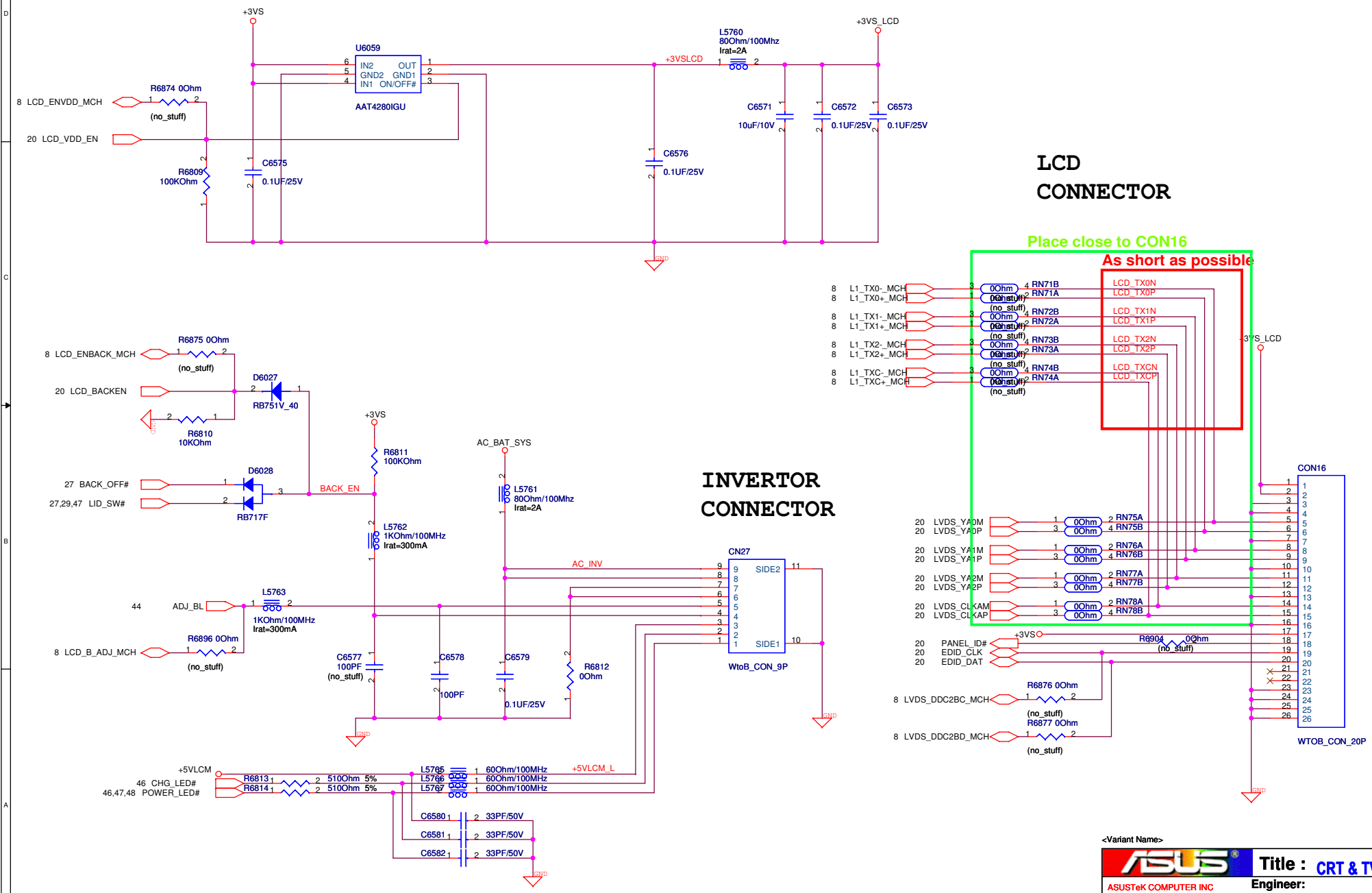
PROJECT: W7J	REVISION 2.0	DATE: Thursday, August 31, 2006	SHEET 21 OF 64	DESCRIPTION: G72M64 : MIOB/CRYSTAL/TMDS	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER :

FBA CMD/ADDR Termination



<Variant Name>

ASUSTeK COMPUTER INC	Title : G72M-Terminator	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 22 of 64	



<Variant Name>

ASUSTeK COMPUTER INC

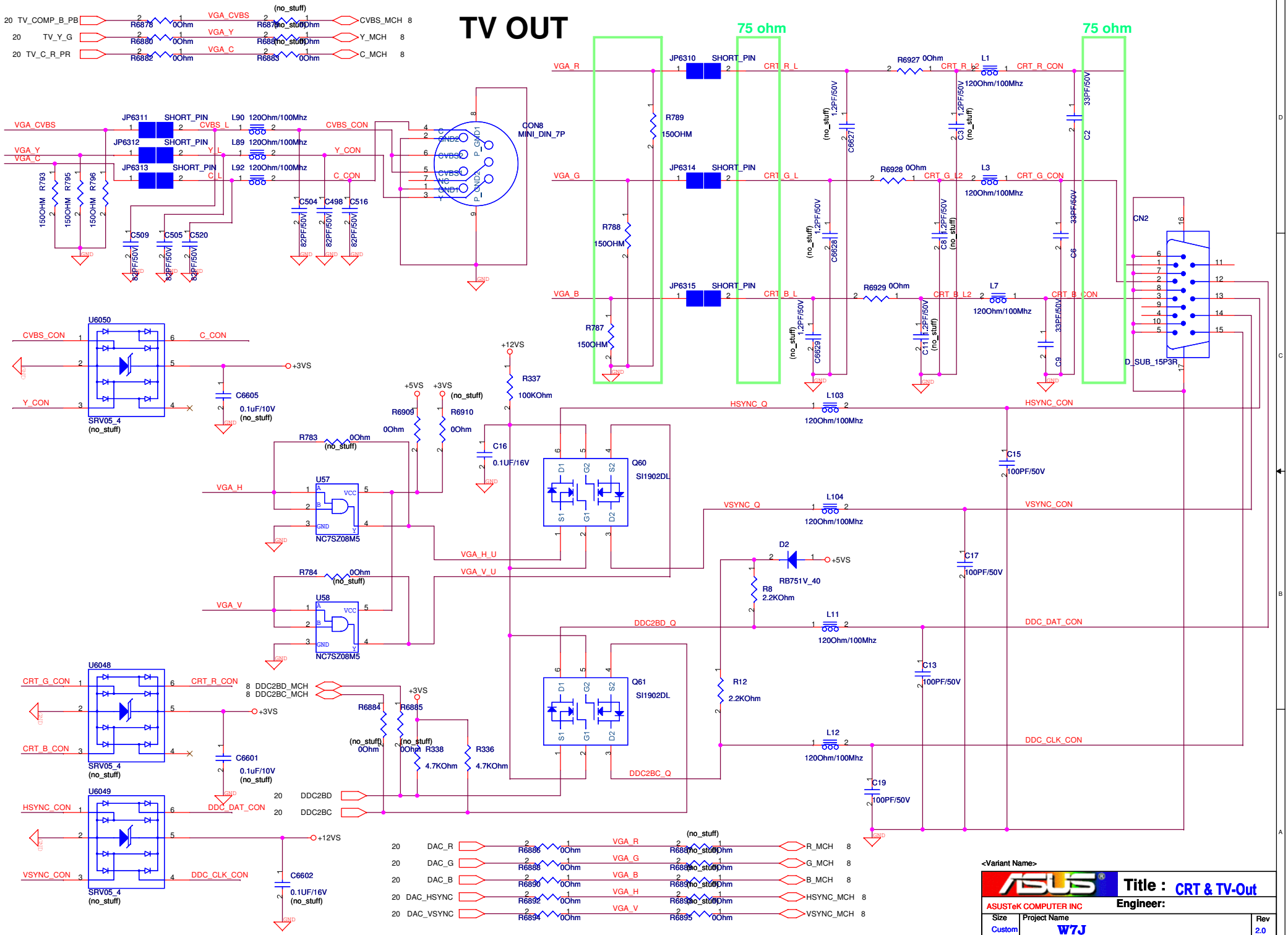
Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 23 of 64

TV OUT



<Variant Name>

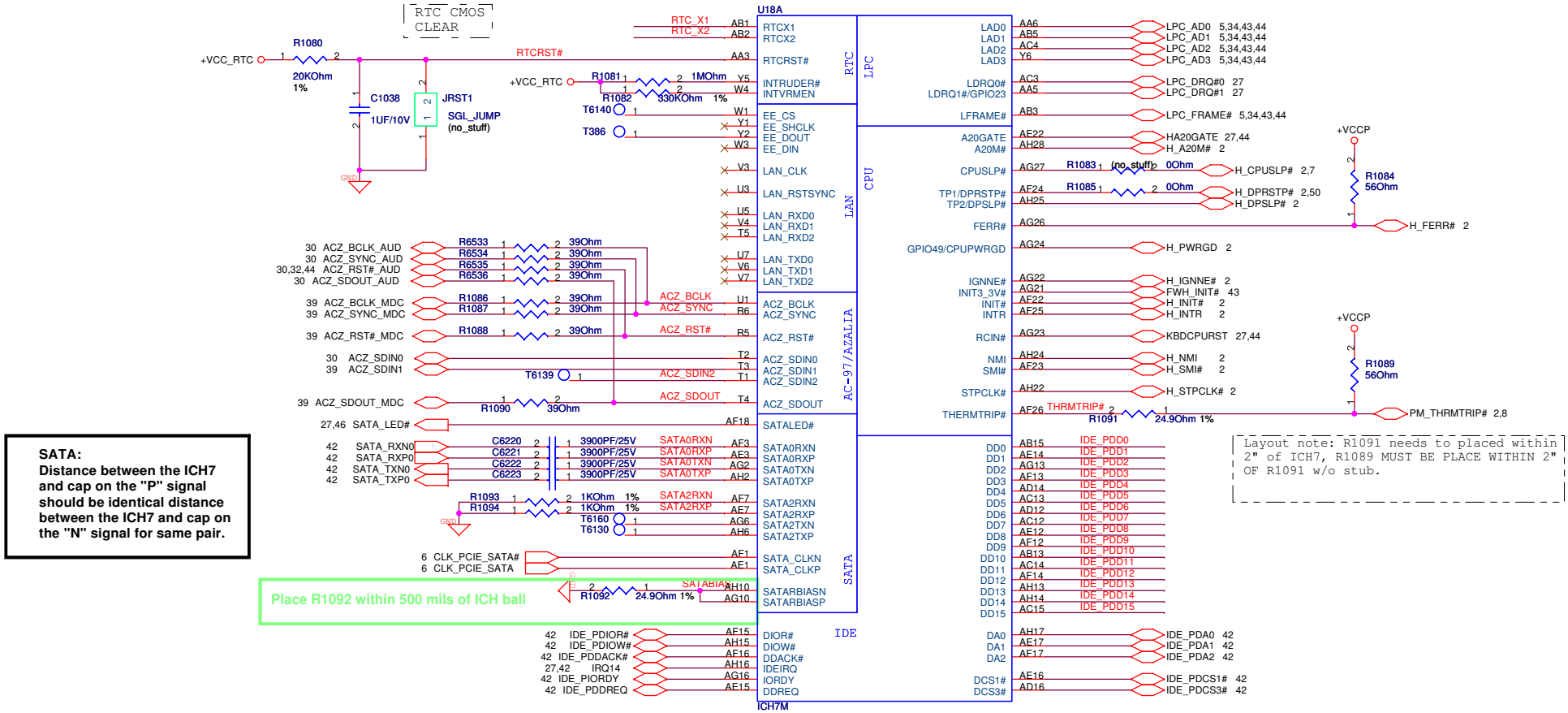
ASUSTeK COMPUTER INC

Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 24 of 64

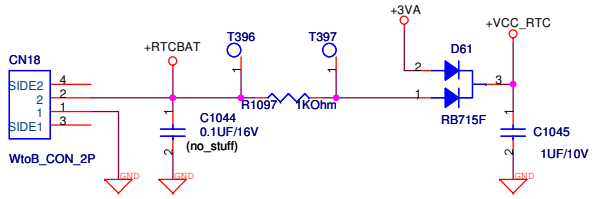


SATA:
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

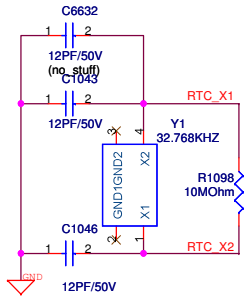
SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

IDE_PDD[0..15] — IDE_PDD[0..15] 42

RTC BAT



RTC Battery
P/N=07-016322032



<Variant Name>

ASUSTeK COMPUTER INC	Title : ICH7-M (1)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 25 of 64	

36 PCI_AD[0..31] — PCI_AD[0..31]

ICH7 Boot BIOS select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

GNT#3 without PD, if NOT top-block swap(inter high)

U18B — ICH7M

PCI: PCI_AD0–PCI_AD31 (E18, C18, A16, E16, A18, E17, A17, A15, C14, E14, D14, B12, C13, G15, G13, E12, C11, D11, A11, A10, F11, F10, E9, D9, B9, A8, A6, C7, B6, E6, D6)

PCI signals: REQ#0 D7, GNT0# E7, REQ#1 C16, GNT1# D16, REQ#2 C17, GNT2# D17, REQ#3 E13, GNT3# F13, REQ4#/GPIO22 A13, GNT4#/GPIO48 A14, GPIO1/REQ5# C8, GPIO17/GNT5# D8

PCI_REQ#0 27,36 — PCI_GNT#0 36 — PCI_REQ#1 27 — T6133 — T6170 — PCI_REQ#2 27 — R6403 1KOhm (no_stuff) — PCI_REQ#3 27 — PCI_REQ#4 27 — T6135 — PCI_REQ#5 27 — T6136

C/BE0# B15, C/BE1# C12, C/BE2# D12, C/BE3# C15

PCI_C/BE#0 36 — PCI_C/BE#1 36 — PCI_C/BE#2 36 — PCI_C/BE#3 36

IRDY# A7 — PCI_IRDY# 27,36

PAR E10 — PCI_PAR 36

PCIRST# B18 — PCI_RST#_ICH

DEVSEL# A12 — PCI_DEVSEL# 27,36

PERR# C9 — PCI_PERR# 27,36

PLOCK# E11 — PCI_LOCK# 27

SERR# B10 — PCI_SERR# 27,36

STOP# F15 — PCI_STOP# 27,36

TRDY# F14 — PCI_TRDY# 27,36

FRAME# F16 — PCI_FRAME# 27,36

PLTRST# C26 — PLT_RST#_SB

PCICLK A9 — CLK_ICHPCI 6

PME# B19

+3VSUS — R6568 10KOhm

Interrupt I/F

PIRQA# A3 — PCI_INTA# 27

PIRQB# B4 — PCI_INTB# 27

PIRQC# C5 — PCI_INTC# 27

PIRQD# B5 — PCI_INTD# 27

GPIO2/PIRQE# G8 — PCI_INTE# 27,36

GPIO3/PIRQF# F7 — PCI_INTF# 27,36

GPIO4/PIRQG# F8 — PCI_INTG# 27

GPIO5/PIRQH# G7 — PCI_INTH# 27

MISC

RSVD_1 AE5 — T400

RSVD_2 AD5 — T403

RSVD_3 AG4 — T406

RSVD_4 AH4 — T409

RSVD_5 AD9 — T411

RSVD_6 AE9 — T401

RSVD_7 AG8 — T404

RSVD_8 AH8 — T407

RSVD_9 F21 — T410

MCH_SYNC# AH20 — MCH_SYNC# 8

pull up to +3VS by internal pull-up resistor

U18D — ICH7M

PCI-Express / Direct Media Interface

PERn1 F26, PERp1 F25, PETn1 E28, PETp1 E27

PCIE_RXN1 40 — PCIE_RXP1 40 — PCIE_TXN1 40 — PCIE_TXP1 40

0.1UF/10V — C1047 — C1048 — PETN1 — PETP1

PERn2 H26, PERp2 H25, PETn2 G28, PETp2 G27

PCIE_RXN2 38 — PCIE_RXP2 38 — PCIE_TXN2 38 — PCIE_TXP2 38

C1049 — C1050 — PETN2 — PETP2

PERn3 K26, PERp3 K25, PETn3 J28, PETp3 J27

PCIE_RXN3 41 — PCIE_RXP3 41 — PCIE_TXN3 41 — PCIE_TXP3 41

C1051 — C1052 — PETN3 — PETP3

PERn4 M26, PERp4 M25, PETn4 L28, PETp4 L27

PERn5 P26, PERp5 P25, PETn5 N28, PETp5 N27

PERn6 T25, PERp6 T24, PETn6 R28, PETp6 R27

DMI0RXN V26 — DMI_RXN0 8

DMI0RXP V25 — DMI_RXP0 8

DMI0TXN U28 — DMI_TXN0 8

DMI0TXP U27 — DMI_TXP0 8

DMI1RXN Y26 — DMI_RXN1 8

DMI1RXP Y25 — DMI_RXP1 8

DMI1TXN W28 — DMI_TXN1 8

DMI1TXP W27 — DMI_TXP1 8

DMI2RXN AB26 — DMI_RXN2 8

DMI2RXP AB25 — DMI_RXP2 8

DMI2TXN AA28 — DMI_TXN2 8

DMI2TXP AA27 — DMI_TXP2 8

DMI3RXN AD25 — DMI_RXN3 8

DMI3RXP AD24 — DMI_RXP3 8

DMI3TXN AC28 — DMI_TXN3 8

DMI3TXP AC27 — DMI_TXP3 8

DMI_CLKN AE28 — CLK_PCIE_ICH# 6

DMI_CLKP AE27 — CLK_PCIE_ICH 6

DMI_ZCOMP C25 — DMICOMP

DMI_IRCOMP D25 — R1099 24.9Ohm 1% — +1.5VS

Place within 500 mils of ICH

SPI_CLK P6, SPI_CS# P1, SPI_ARB R2, SPI_MOSI P5, SPI_MISO P2

USBP0N F1 — USB_PN0 45

USBP0P F2 — USB_PP0 45

USBP1N G4 — USB_PN1 45

USBP1P G3 — USB_PP1 45

USBP2N H1 — USB_PN2 47

USBP2P H2 — USB_PP2 47

USBP3N J4 — USB_PN3 45

USBP3P J3 — USB_PP3 45

USBP4N K1 — USB_PN4 45

USBP4P K2 — USB_PP4 45

USBP5N L4 — USB_PN5 45

USBP5P L5 — USB_PP5 45

USBP6N M1, USBP6P M2

USBP7N N4 — T405

USBP7P N3 — T408

USBRBIAS# D2 — USBBIAS

USBRBIAS D1 — R1100 22.6Ohm 1% — GND

Place within 500 mils of ICH

+3V — RN18A 10KOhm (no_stuff) — RN18B 10KOhm (no_stuff) — RN18C 10KOhm (no_stuff) — RN18D 10KOhm (no_stuff)

27,40 USB_OC#0 — D3

27 USB_OC#2 — C4

27,45 USB_OC#13 — D5

27,45 USB_OC#4 — D4

27 USB_OC#5 — E5

27 USB_OC#6 — C3

27 USB_OC#7 — A2

OC0# B3, OC1#, OC2#, OC3#, OC4#, OC5#/GPIO29, OC6#/GPIO30, OC7#/GPIO31

U68D 74HC08

8,27,34,38,41,42,43,44 BUF_PLT_RST# — PLT_RST#_SB — +3V — C1056 0.01UF (no_stuff)

U68A 74HC08

36,40,42 PCI_RST# — PCI_RST#_ICH — +3V — C1053 0.1UF/16V

+3V — R1102 10KOhm — C1054 0.1UF/16V

U68C 74HC08

17 PLT_RST# — R6408 0Ohm (no_stuff) — PLT_RST#_SB — R1104 0Ohm (no_stuff) — SW_RST# 27

R1106 0Ohm

+3V — C1055 0.1UF/16V

U69 74LVC1G32GV

PCI_RST# — 44 SET_PCIRSTNS# — R1108 10KOhm — R1109 47KOhm — C1057 0.01UF — PCI_RSTNS# 36,44

Can be issue SCI or SMI List: GPIO0~GPIO15

Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28

Only GPI Pin: GPIO~8,11~15,26,29,30,31,40(5V),41

Only GPO Pin: GPIO16~17,19,21,23,48

Can be GPIO: GPIO24,25,27,28,33,34

Resume Power Input Pin List:

BATLOW#,AC_SDIN[0:1],LAN_RST#,

OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#

<Variant Name>

ASUSTeK COMPUTER INC

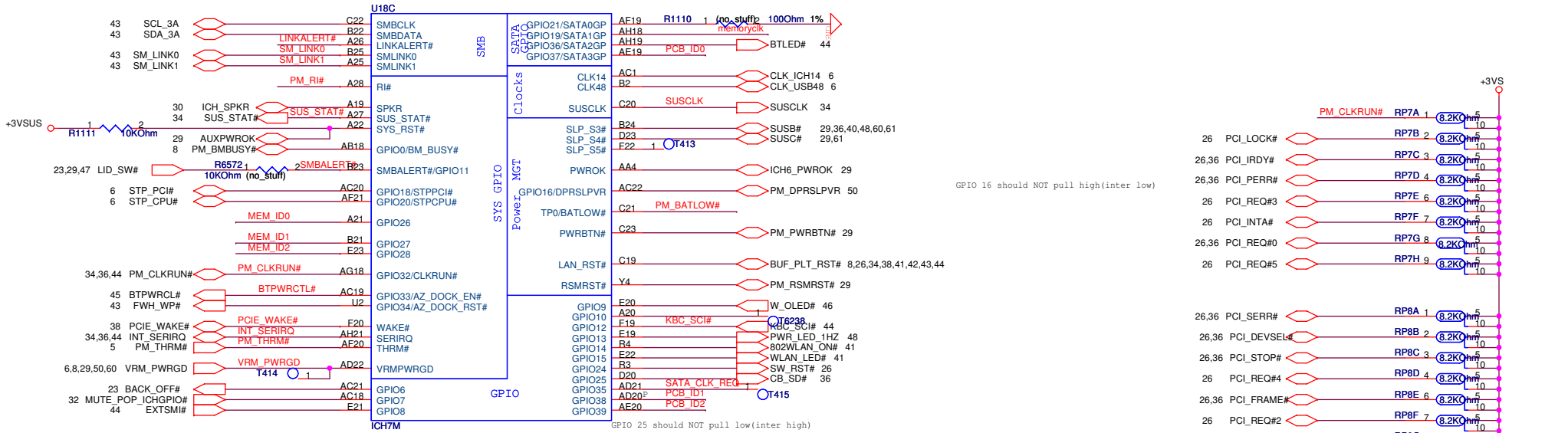
Title : ICH7-M (2)

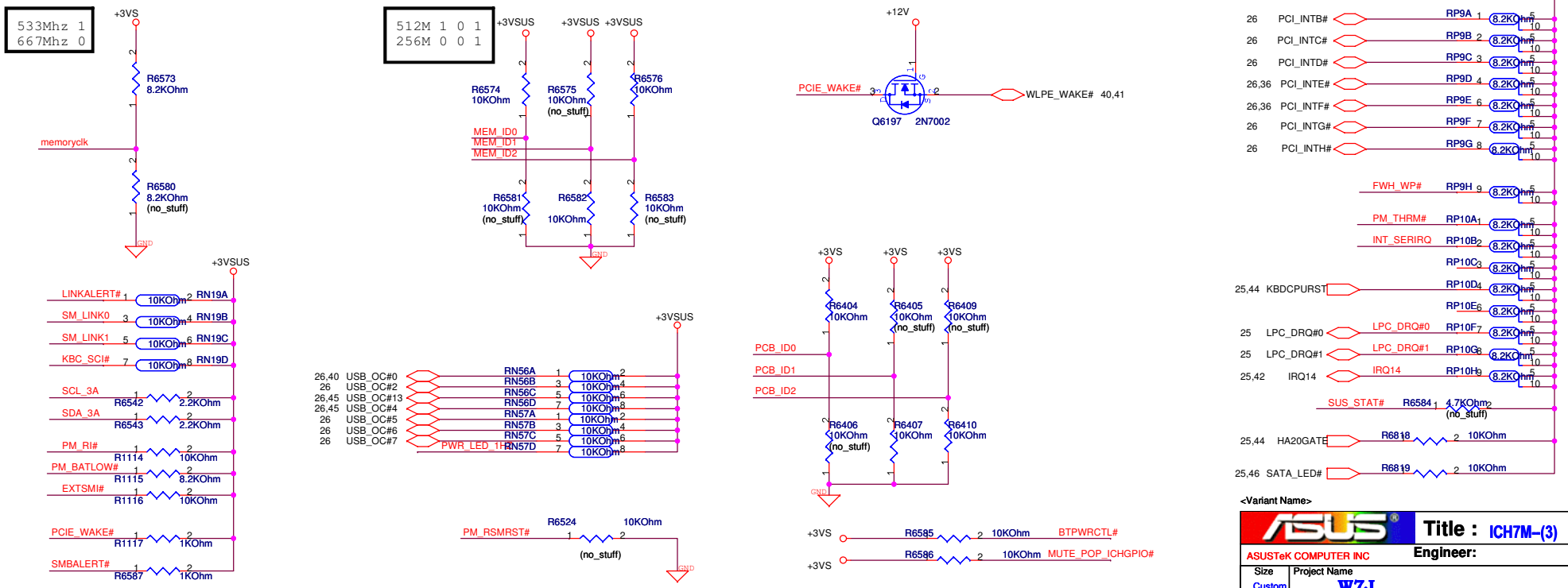
Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 26 of 64

The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.





<Variant Name>

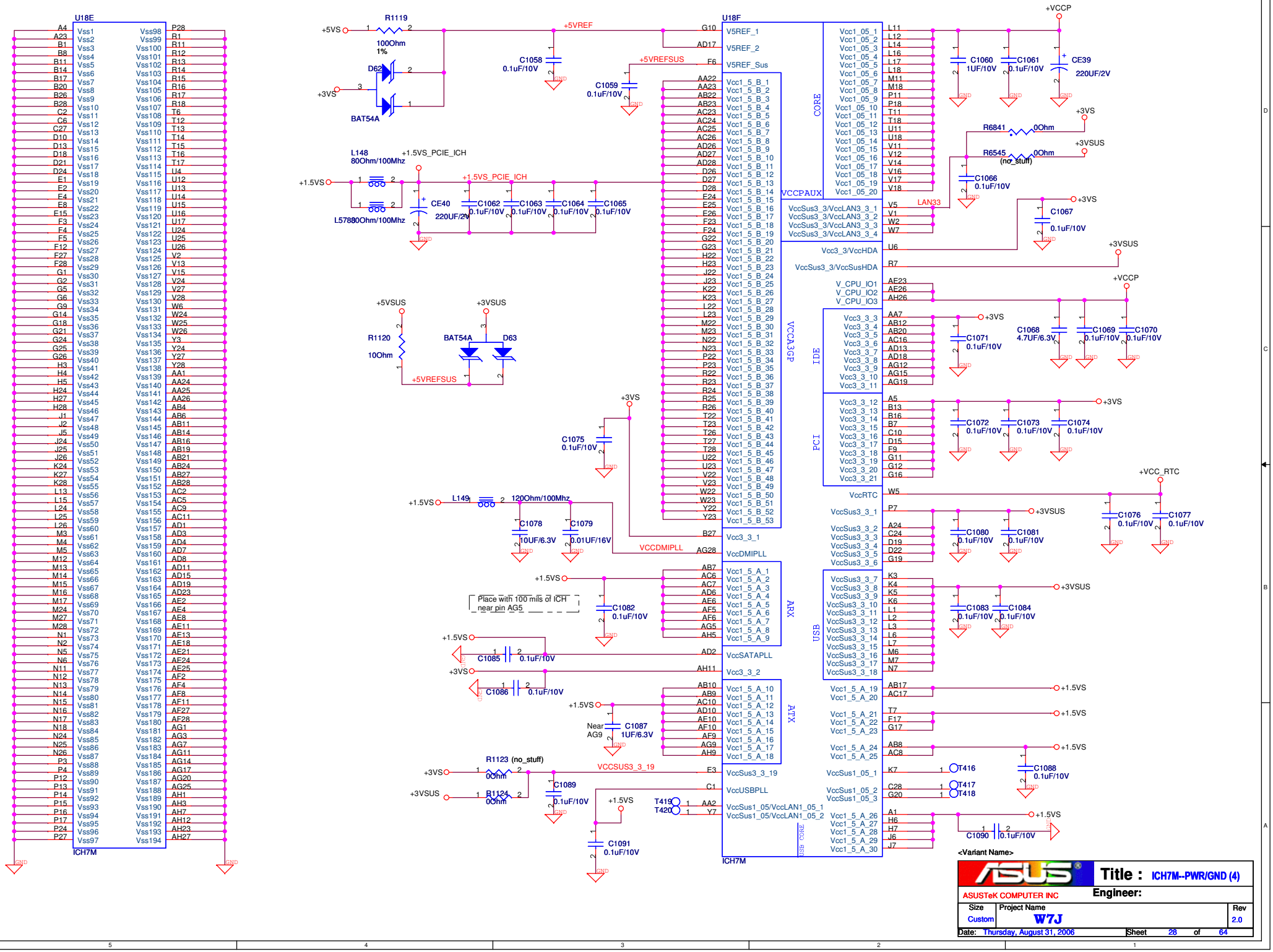
ASUSTeK COMPUTER INC

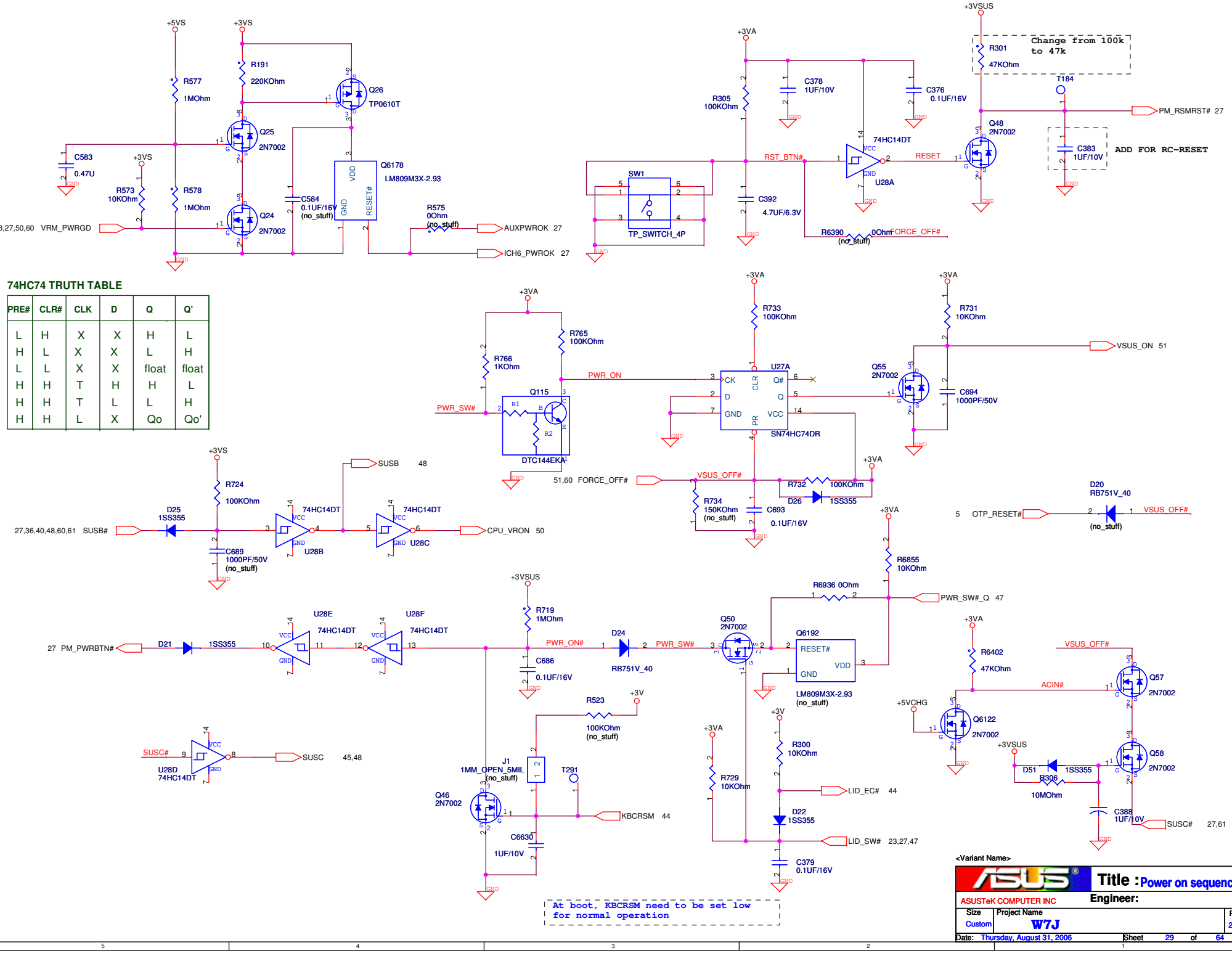
Title : ICH7M-(3)

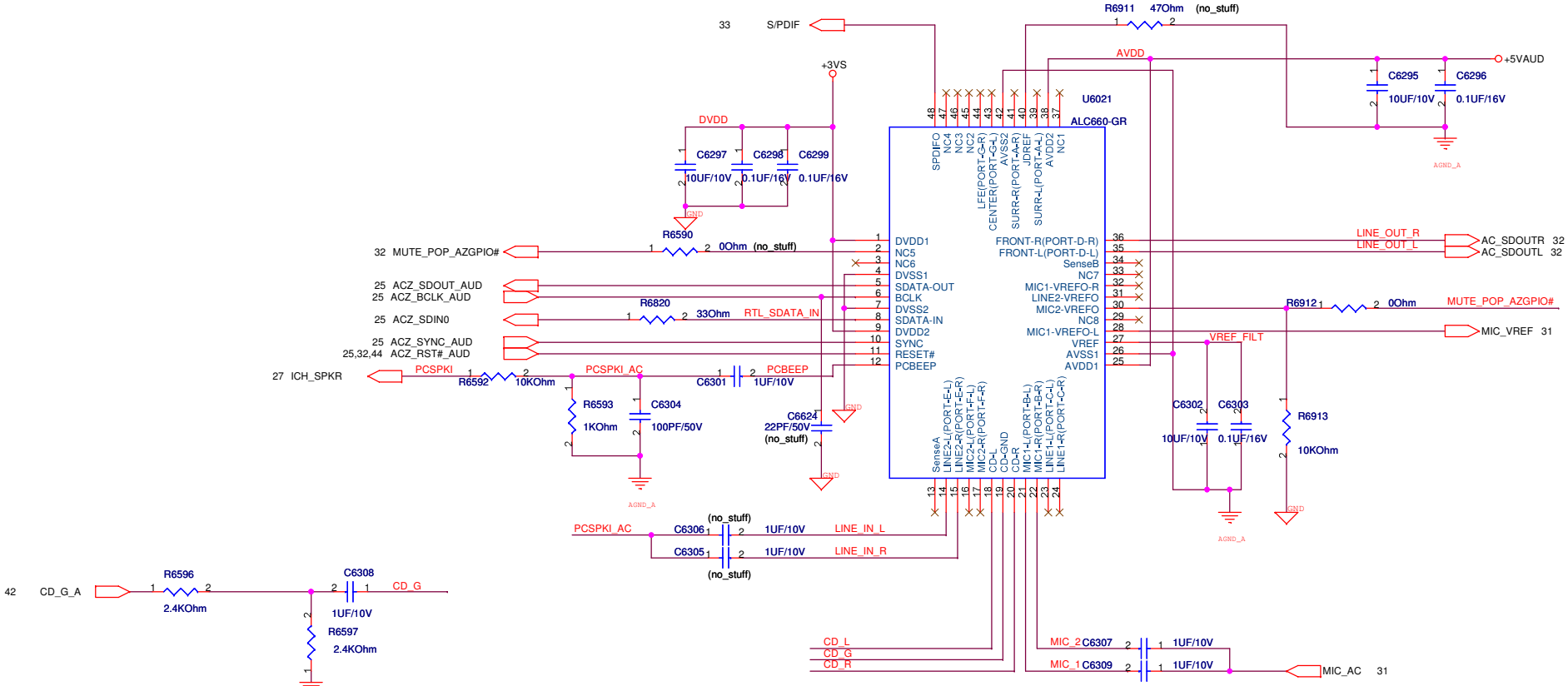
Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

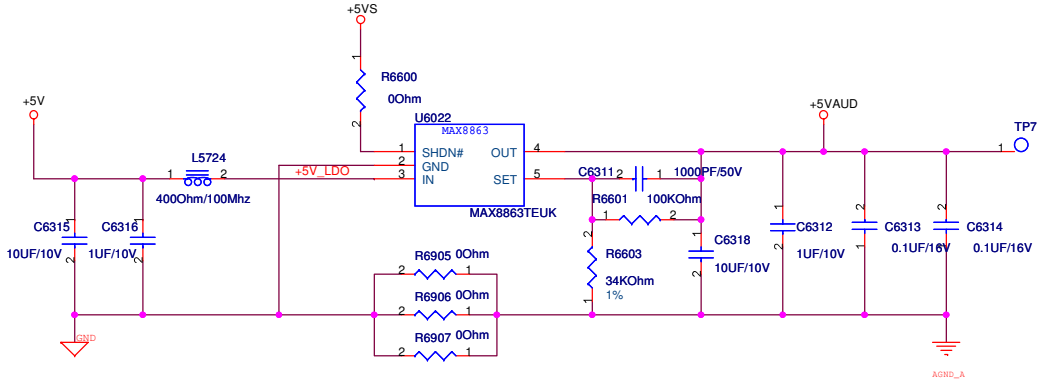
Date: Thursday, August 31, 2006 Sheet 27 of 64


U18E
ICH7M
R1119
100Ohm
1%
BAT54A
+5VS
+3VS
+5VREF
C1058
0.1uF/10V
C1059
0.1uF/10V
+5VREFSUS
L148
80Ohm/100Mhz
L57880Ohm/100Mhz
+1.5VS_PCIE_ICH
CE40
220UF/2V
C1062
C1063
C1064
C1065
0.1uF/10V
R1120
10Ohm
+5VSUS
+3VSUS
D63
L149
120Ohm/100Mhz
C1078
10UF/6.3V
C1079
0.01UF/16V
VCCDMIPLL
C1075
C1082
0.1uF/10V
Place with 100 mils of ICH
near pin AG5
C1085
C1086
C1087
1UF/6.3V
Near
AG9
R1123 (no_stuff)
R1124
0Ohm
VCCSUS3_3_19
C1089
C1091
T419
T420
U18F
V5REF_1
V5REF_2
V5REF_Sus
VccDMIPLL
VccSATAPLL
VccUSBPLL
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
USB
ATX
USB_CORE
C1060
1UF/10V
C1061
0.1uF/10V
CE39
220UF/2V
R6841
0Ohm
R6545
0Ohm
(no_stuff)
C1066
0.1uF/10V
C1067
0.1uF/10V
LAN33
U6
R7
C1068
4.7UF/6.3V
C1069
C1070
C1071
C1072
C1073
C1074
C1076
C1077
C1080
C1081
C1083
C1084
C1088
C1090
+VCCP
+VCC_RTC
T416
T417
T418
<Variant Name>
Title : ICH7M--PWR/GND (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
2.0
Date: Thursday, August 31, 2006
Sheet 28 of 64


+5VS
+3VS
R577
1MOhm
R191
220KOhm
Q26
TP0610T
Q25
2N7002
C583
0.47U
R573
10KOhm
R578
1MOhm
Q24
2N7002
C584
0.1UF/16V
(no_stuff)
Q6178
LM809M3X-2.93
VDD
GND
RESET#
R575
0Ohm
(no_stuff)
6,8,27,50,60 VRM_PWRGD
AUXPWROK 27
ICH6_PWROK 27
+3VA
R305
100KOhm
C378
1UF/10V
C376
0.1UF/16V
74HC14DT
U28A
RST_BTN#
RESET
C392
4.7UF/6.3V
SW1
TP_SWITCH_4P
R6390
0Ohm
(no_stuff)
FORCE_OFF#
+3VSUS
R301
47KOhm
Change from 100k
to 47k
T184
PM_RSMRST# 27
Q48
2N7002
C383
1UF/10V
ADD FOR RC-RESET
74HC74 TRUTH TABLE
PRE# CLR# CLK D Q Q'
L H X X H L
H L X X L H
L L X X float float
H H T H H L
H H T L L H
H H L X Qo Qo'
+3VA
R765
100KOhm
R766
1KOhm
PWR_ON
PWR_SW#
Q115
DTC144EKA
R733
100KOhm
U27A
SN74HC74DR
CK
D
GND
CLR
PR
Q#
Q
VCC
R731
10KOhm
VSUS_ON 51
Q55
2N7002
C694
1000PF/50V
51,60 FORCE_OFF#
VSUS_OFF#
R732
100KOhm
D26
1SS355
R734
150KOhm
(no_stuff)
C693
0.1UF/16V
+3VS
R724
100KOhm
SUSB 48
D25
1SS355
27,36,40,48,60,61 SUSB#
74HC14DT
U28B
U28C
CPU_VRON 50
C689
1000PF/50V
(no_stuff)
D20
RB751V_40
5 OTP_RESET#
VSUS_OFF#
(no_stuff)
R6855
10KOhm
R6936 0Ohm
PWR_SW#_Q 47
+3VSUS
R719
1MOhm
PWR_ON#
D24
RB751V_40
PWR_SW#
C686
0.1UF/16V
Q50
2N7002
Q6192
RESET#
VDD
GND
LM809M3X-2.93
(no_stuff)
U28E
U28F
74HC14DT
27 PM_PWRBTN#
D21
1SS355
+3V
R523
100KOhm
(no_stuff)
SUSC# 9
U28D
74HC14DT
8 SUSC 45,48
J1
1MM_OPEN_5MIL
(no_stuff)
T291
KBCRSM 44
Q46
2N7002
C6630
1UF/10V
+3VA
R729
10KOhm
+3V
R300
10KOhm
LID_EC# 44
D22
1SS355
LID_SW# 23,27,47
C379
0.1UF/16V
R6402
47KOhm
ACIN#
Q57
2N7002
+5VCHG
Q6122
2N7002
+3VSUS
D51
1SS355
R306
10MOhm
Q58
2N7002
C388
1UF/10V
SUSC# 27,61
At boot, KBCRSM need to be set low
for normal operation
<Variant Name>
ASUSTeK COMPUTER INC
Title : Power on sequence
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 29 of 64



AUDIO_LDO



<Variant Name>

ASUSTeK COMPUTER INC

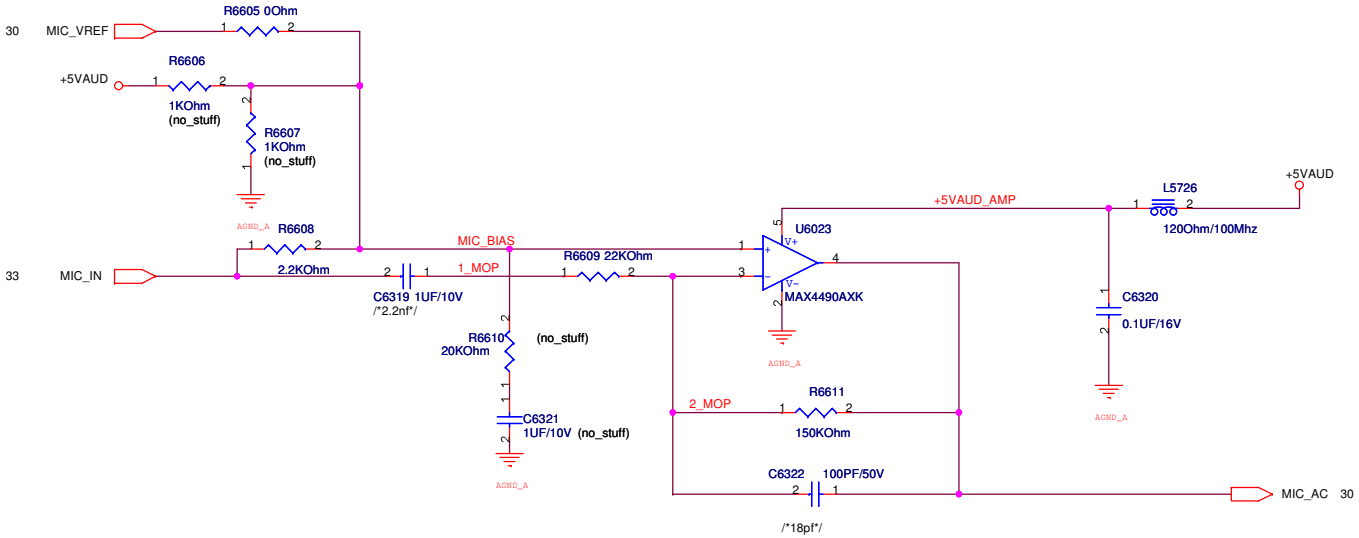
Title : AZALIA_ALC660

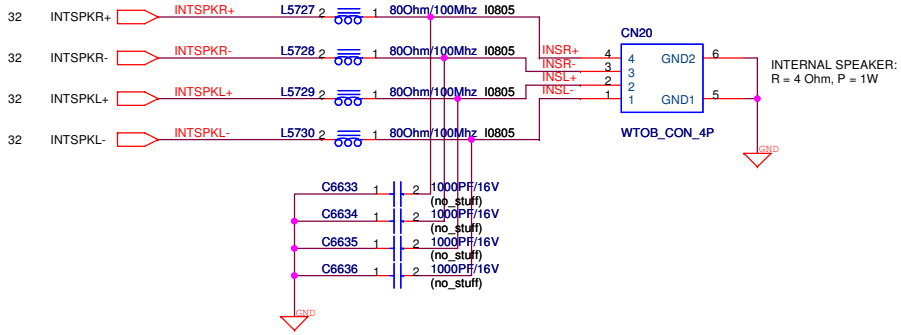
Engineer:

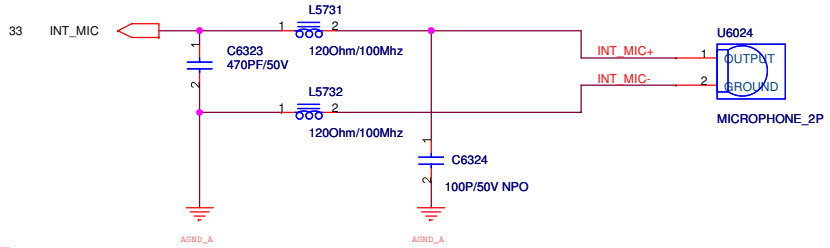
Size	Project Name	Rev
Custom	W7J	2.0

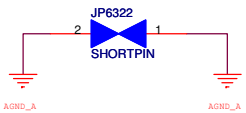
Date: Thursday, August 31, 2006 Sheet 30 of 64

MIC PreAmp & Mic Jack



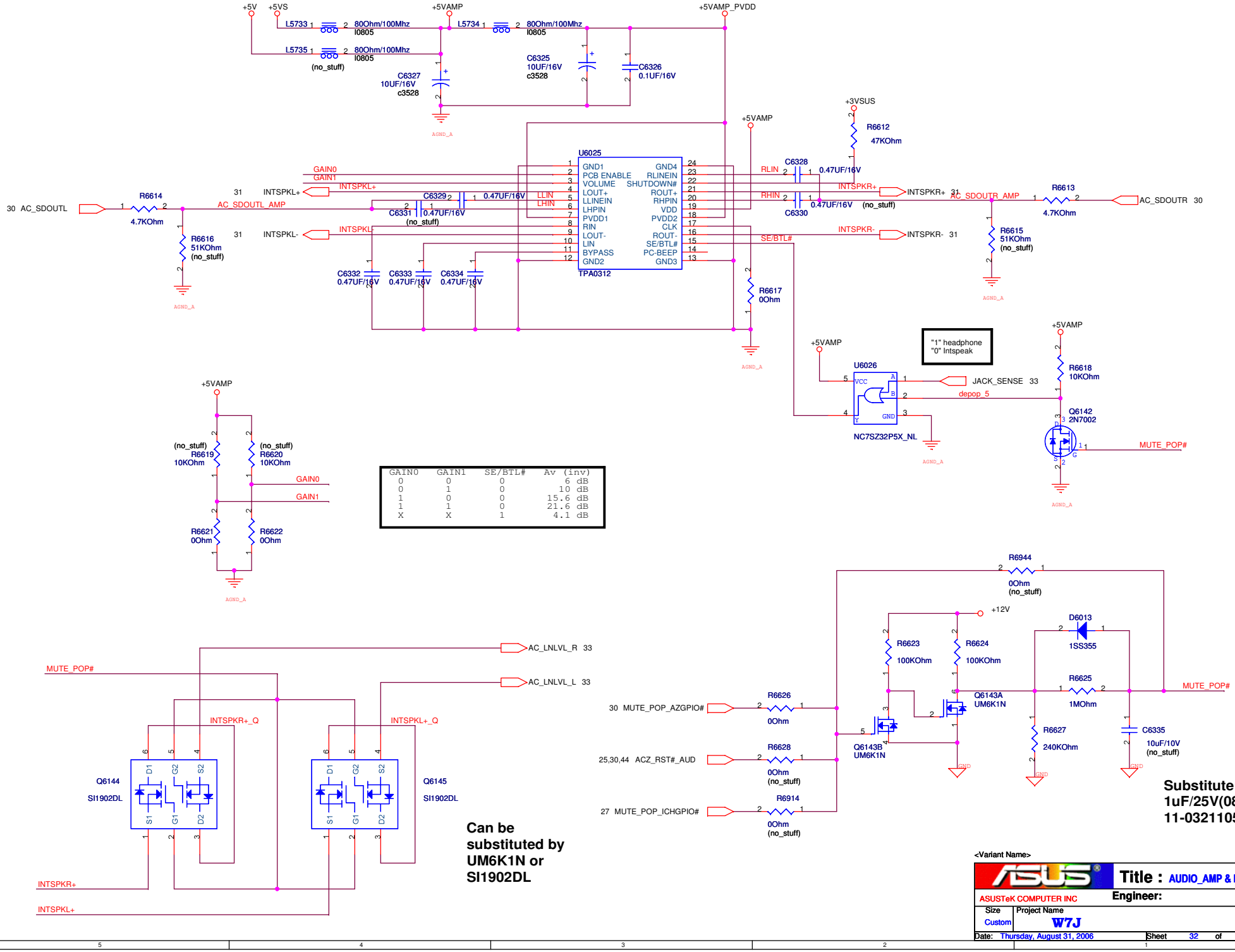






<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC PREAMP & INT MIC	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 31 of 64	



<Variant Name>

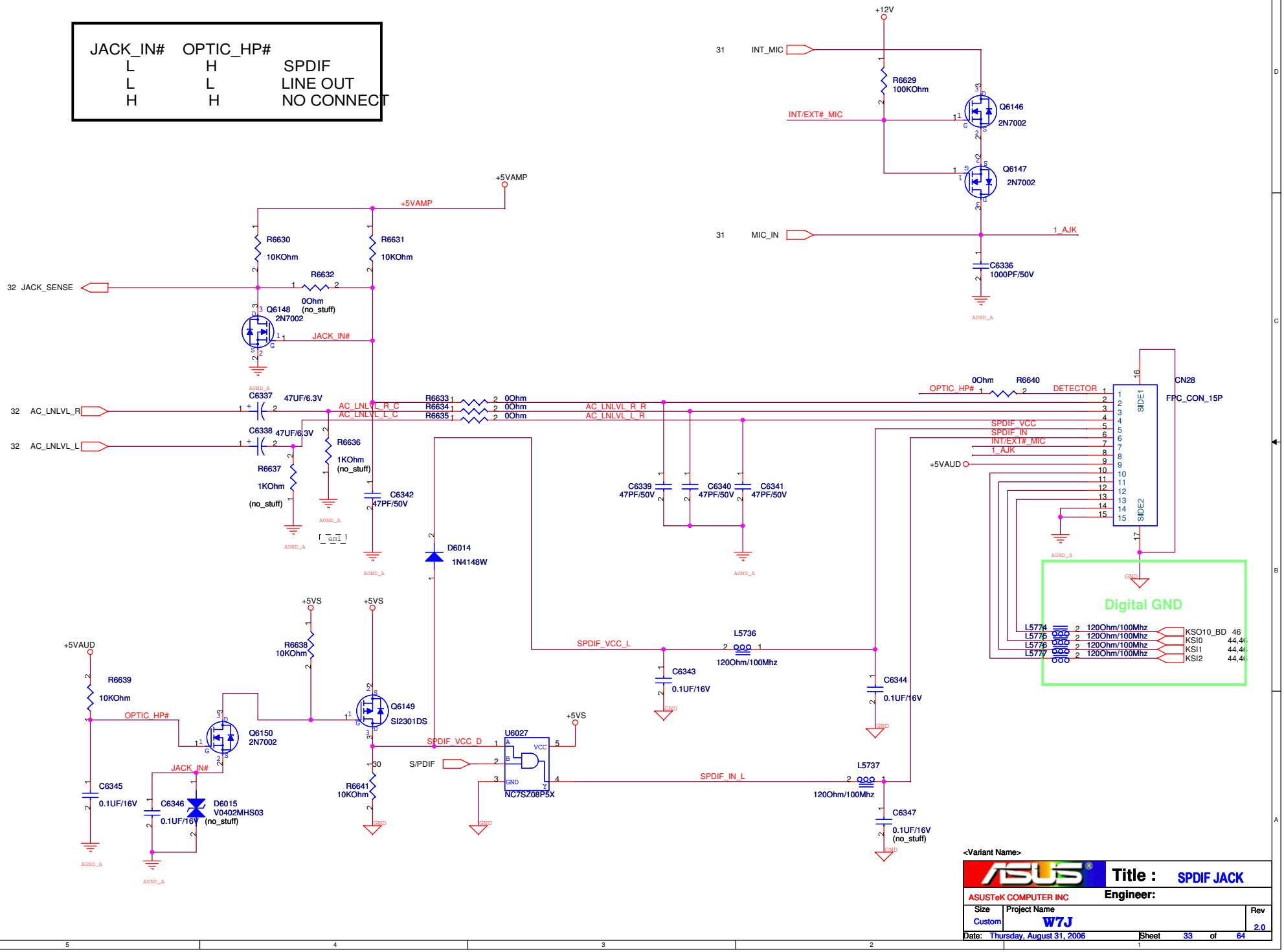
ASUSTeK COMPUTER INC

Title : AUDIO_AMP & INT SPK

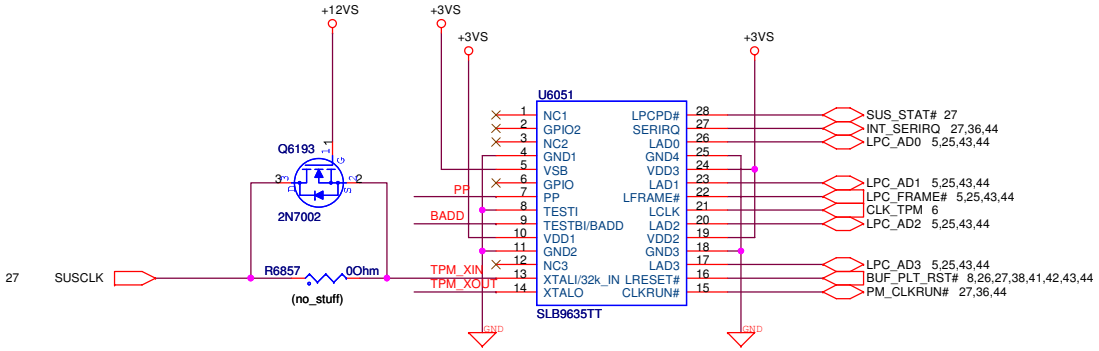
Engineer:

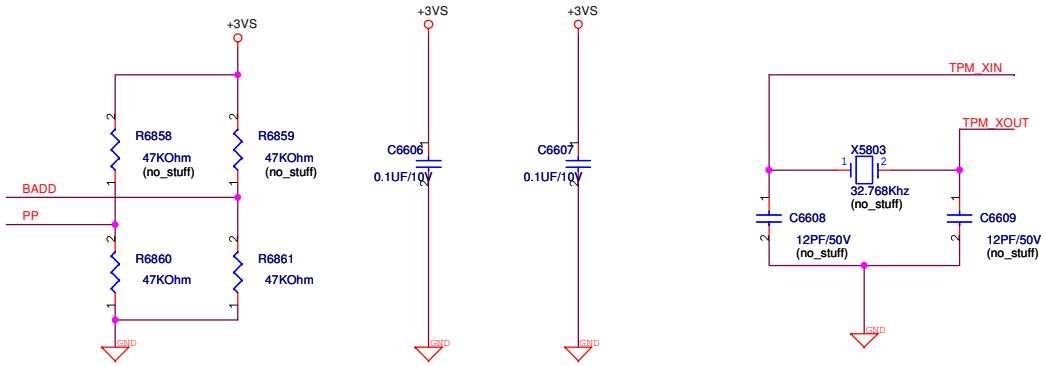
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 32 of 64


JACK_IN# OPTIC_HP#
L H SPDIF
L L LINE OUT
H H NO CONNECT
+12V
31 INT_MIC
R6629 100KOhm
INT/EXT#_MIC
Q6146 2N7002
Q6147 2N7002
31 MIC_IN
1_AJK
C6336 1000PF/50V
+5VAMP
R6630 10KOhm
R6631 10KOhm
32 JACK_SENSE
R6632 0Ohm (no_stuff)
Q6148 2N7002
JACK_IN#
32 AC_LNLVL_R
32 AC_LNLVL_L
C6337 47UF/6.3V
C6338 47UF/6.3V
R6633 0Ohm
R6634 0Ohm
R6635 0Ohm
AC_LNLVL_R_C
AC_LNLVL_L_C
AC_LNLVL_R_R
AC_LNLVL_L_R
R6636 1KOhm (no_stuff)
R6637 1KOhm (no_stuff)
C6342 47PF/50V
C6339 47PF/50V
C6340 47PF/50V
C6341 47PF/50V
D6014 1N4148W
OPTIC_HP#
R6640 0Ohm
DETECTOR
CN28
FPC_CON_15P
SIDE1
SIDE2
SPDIF_VCC
SPDIF_IN
INT/EXT#_MIC
1_AJK
+5VAUD
Digital GND
L5774 120Ohm/100Mhz
L5775 120Ohm/100Mhz
L5776 120Ohm/100Mhz
L5777 120Ohm/100Mhz
KSO10_BD 46
KSI0 44,46
KSI1 44,46
KSI2 44,46
+5VS
R6638 10KOhm
R6639 10KOhm
Q6149 SI2301DS
Q6150 2N7002
SPDIF_VCC_D
S/PDIF
U6027 NC7SZ08P5X
SPDIF_IN_L
L5736 120Ohm/100Mhz
L5737 120Ohm/100Mhz
C6343 0.1UF/16V
C6344 0.1UF/16V
C6345 0.1UF/16V
C6346 0.1UF/16V
C6347 0.1UF/16V (no_stuff)
D6015 V0402MHS03 (no_stuff)
R6641 10KOhm
AGND_A
GND
<Variant Name>
Title : SPDIF JACK
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 33 of 64

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.





<Variant Name>

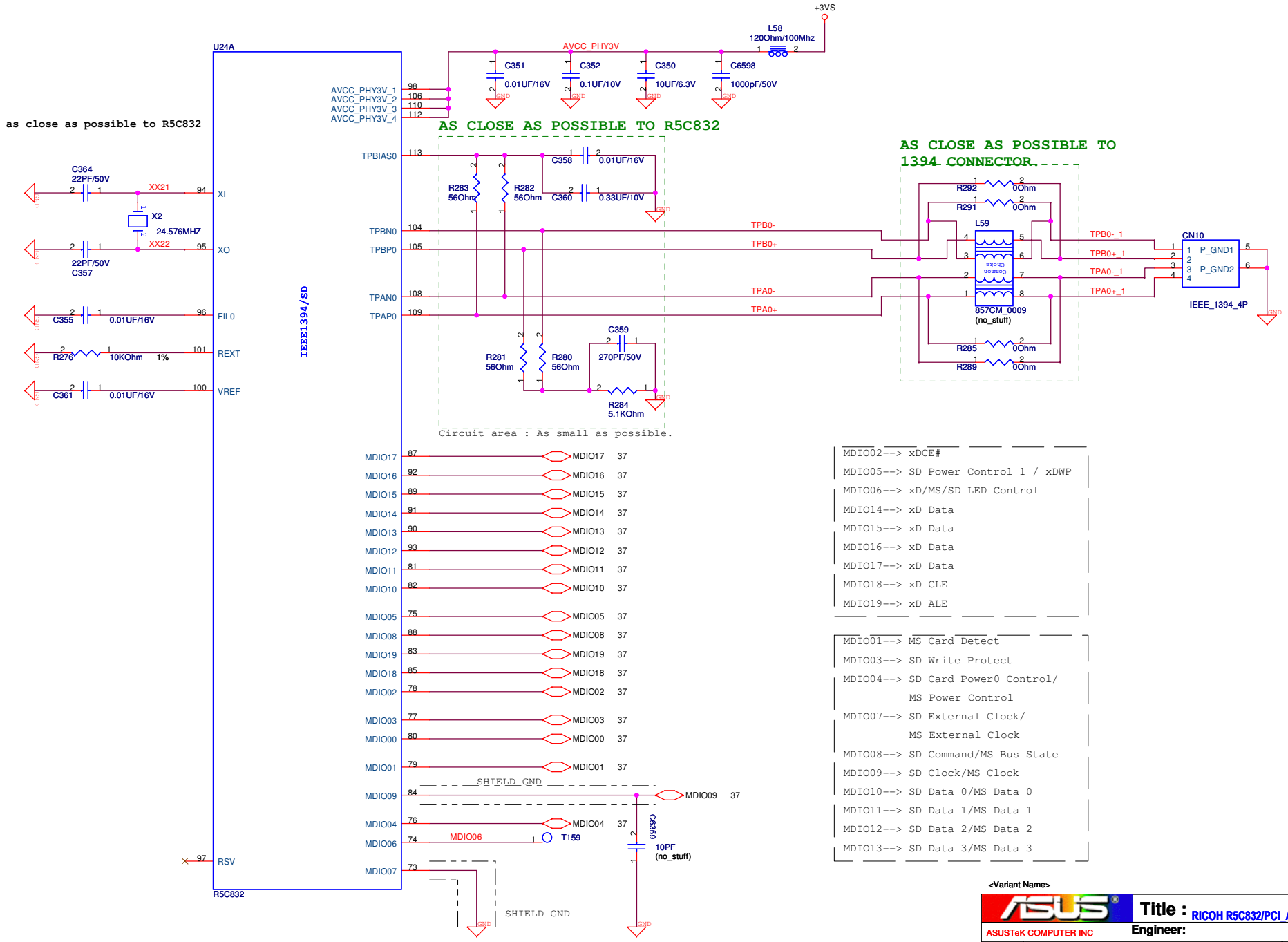
ASUSTeK COMPUTER INC

Title : TPM 1.2

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 34 of 64



<Variant Name>

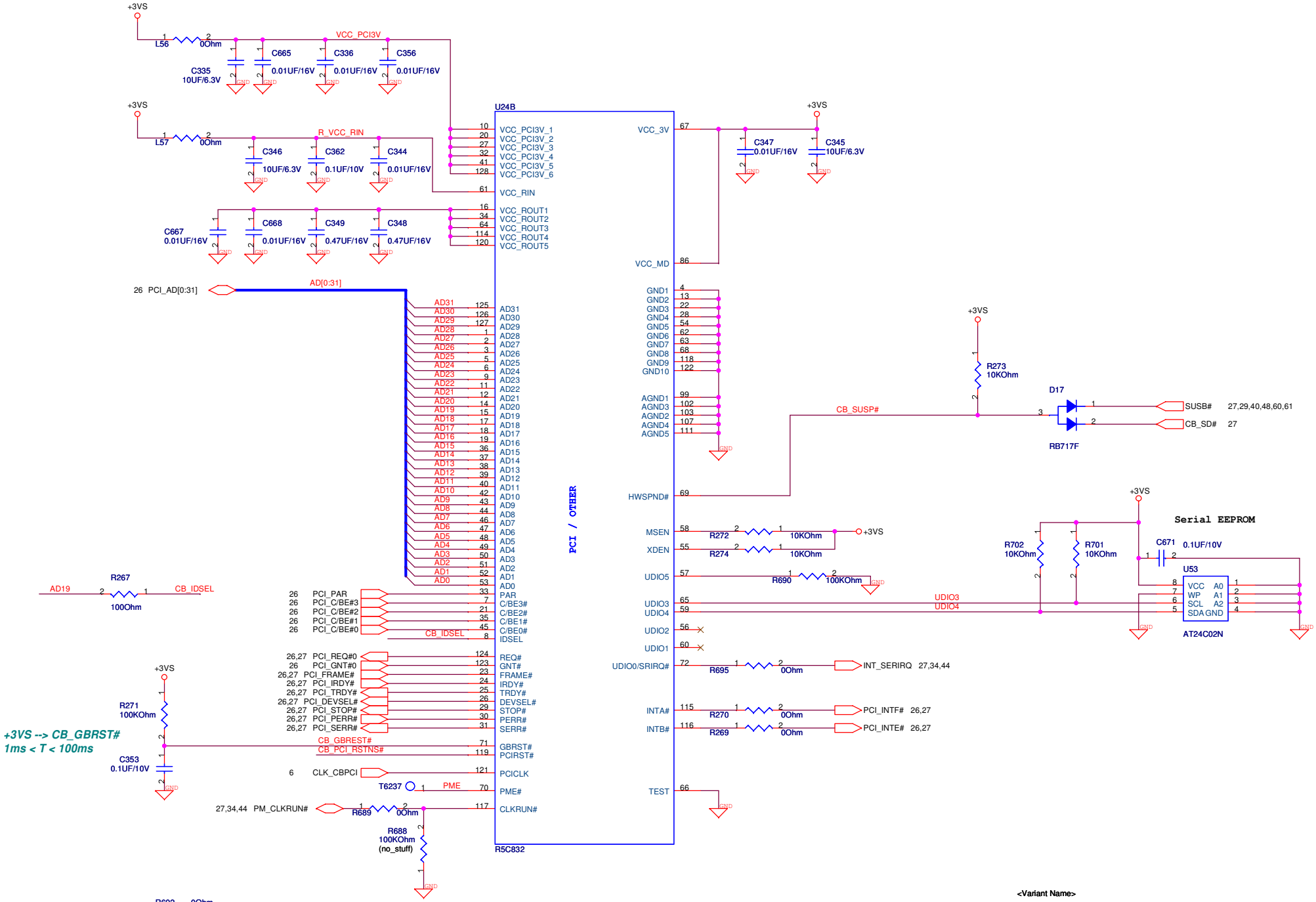
ASUSTeK COMPUTER INC

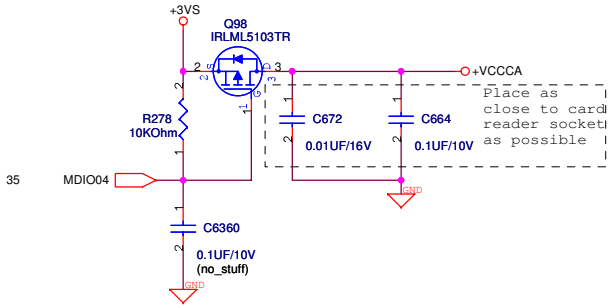
Title : RICOH R5C832/PCI_A

Engineer:

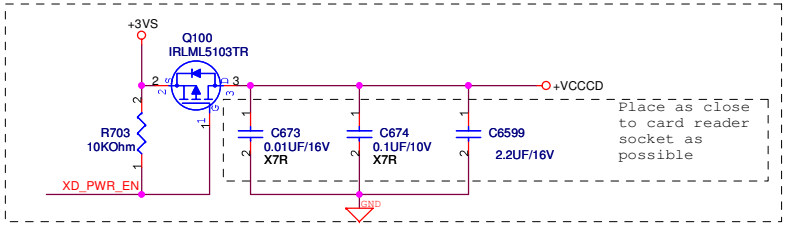
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 35 of 64

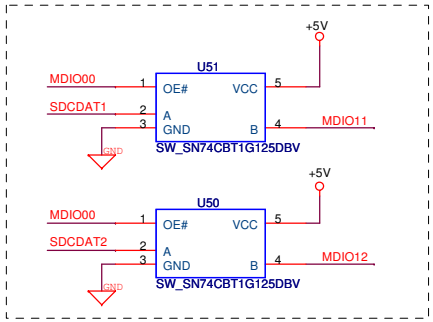

+3VS
L56 0Ohm
VCC_PCI3V
C335 10UF/6.3V
C665 0.01UF/16V
C336 0.01UF/16V
C356 0.01UF/16V
L57 0Ohm
R_VCC_RIN
C346 10UF/6.3V
C362 0.1UF/10V
C344 0.01UF/16V
C667 0.01UF/16V
C668 0.01UF/16V
C349 0.47UF/16V
C348 0.47UF/16V
U24B
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
C347 0.01UF/16V
C345 10UF/6.3V
VCC_MD
26 PCI_AD[0:31]
AD[0:31]
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R273 10KOhm
D17
RB717F
SUSB# 27,29,40,48,60,61
CB_SD# 27
CB_SUSP#
HWSPND#
MSEN
XDEN
R272 10KOhm
R274 10KOhm
UDIO5
R690 100KOhm
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
R695 0Ohm
INT_SERIRQ 27,34,44
INTA#
INTB#
R270 0Ohm
R269 0Ohm
PCI_INTF# 26,27
PCI_INTE# 26,27
TEST
Serial EEPROM
R702 10KOhm
R701 10KOhm
C671 0.1UF/10V
U53
VCC A0
WP A1
SCL A2
SDA GND
AT24C02N
AD19
R267 100Ohm
CB_IDSEL
26 PCI_PAR
26 PCI_C/BE#3
26 PCI_C/BE#2
26 PCI_C/BE#1
26 PCI_C/BE#0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
26,27 PCI_REQ#0
26 PCI_GNT#0
26,27 PCI_FRAME#
26,27 PCI_IRDY#
26,27 PCI_TRDY#
26,27 PCI_DEVSEL#
26,27 PCI_STOP#
26,27 PCI_PERR#
26,27 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
R271 100KOhm
+3VS --> CB_GBRST#
1ms < T < 100ms
C353 0.1UF/10V
CB_GBREST#
CB_PCI_RSTNS#
GBRST#
PCIRST#
6 CLK_CBPCI
PCICLK
T6237
PME
PME#
27,34,44 PM_CLKRUN#
R689 0Ohm
CLKRUN#
R688 100KOhm (no_stuff)
R5C832
PCI / OTHER
R692 0Ohm
26,40,42 PCI_RST#
CB_PCI_RSTNS#
R693 0Ohm
26,44 PCI_RSTNS#
(no_stuff)
<Variant Name>
Title : RICOH R5C832/PCI_B
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 36 of 64



To correct the problem when MS Duo adaptor is in use.

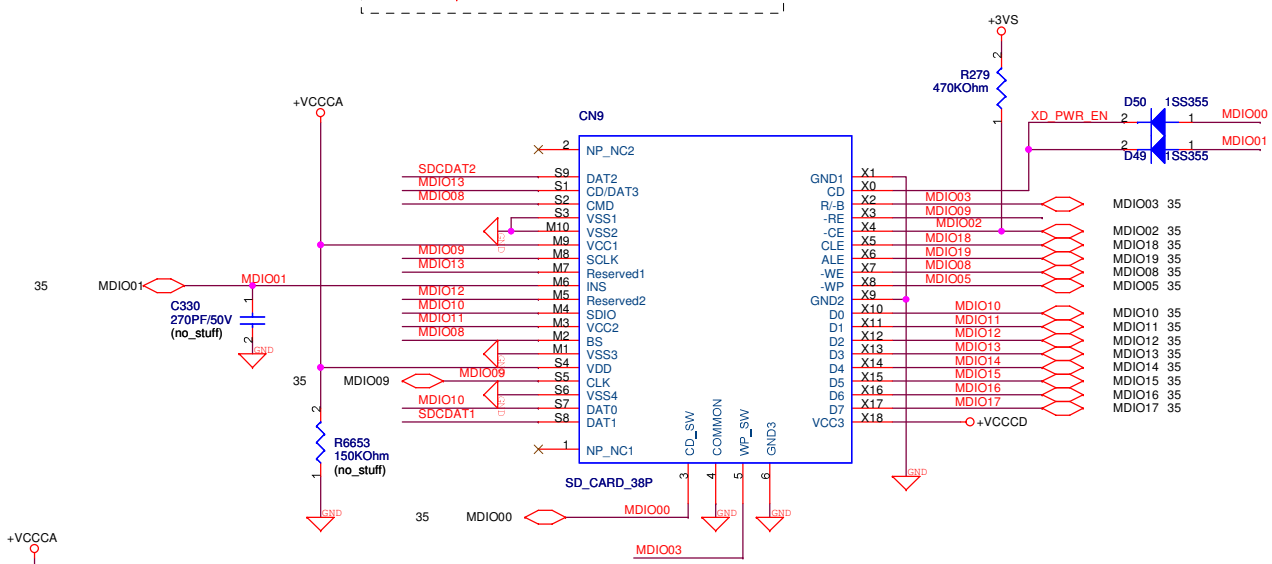


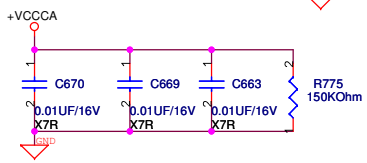
SD/MMC/MS/MS-PRO Card Reader Socket



MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

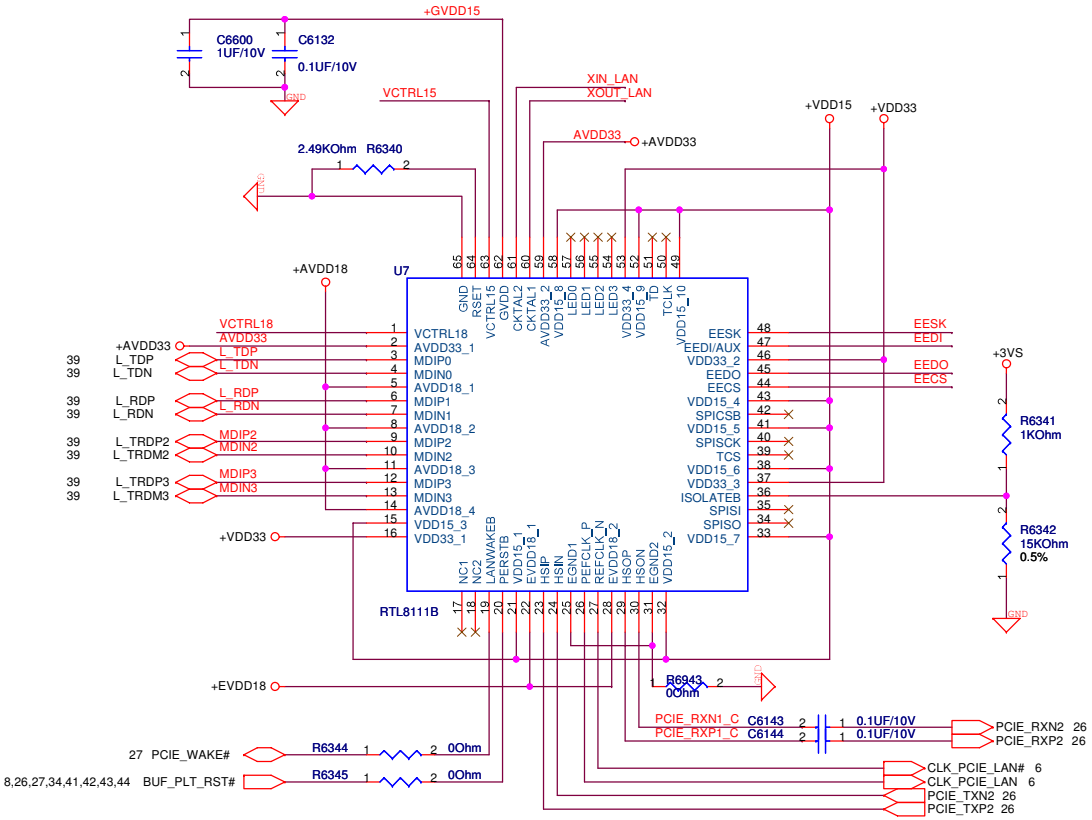


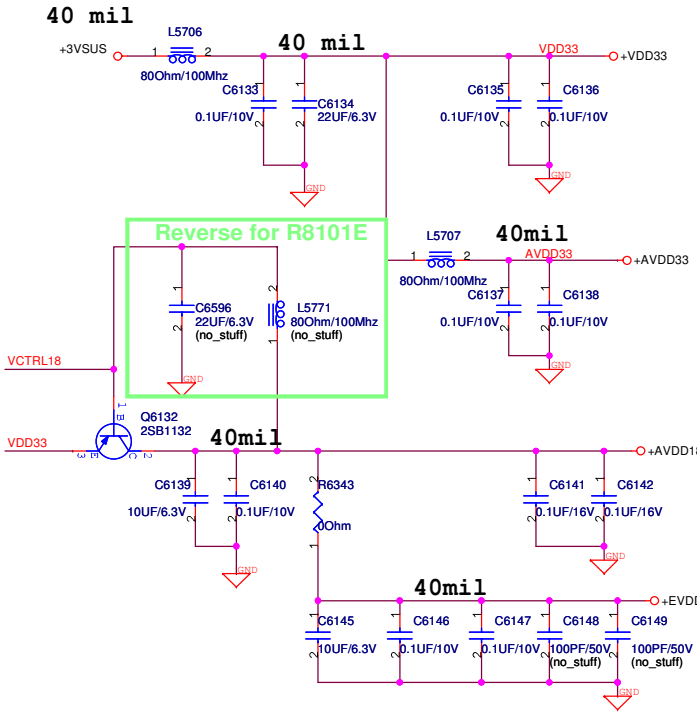


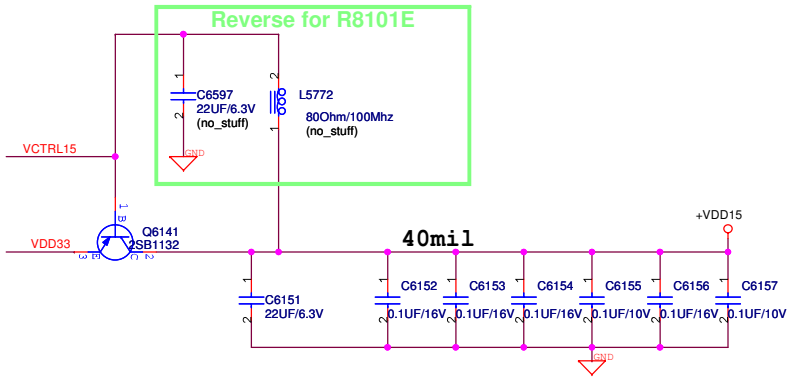
<Variant Name>

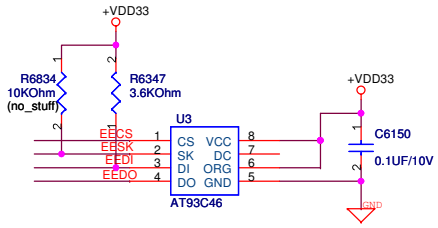
ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 37 of 64	

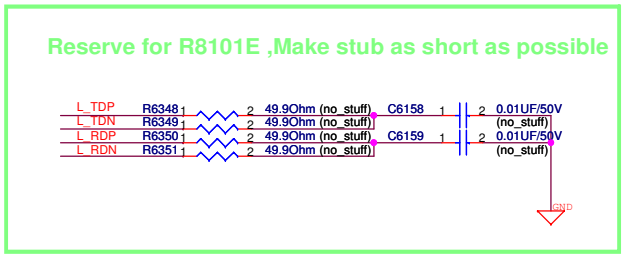
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

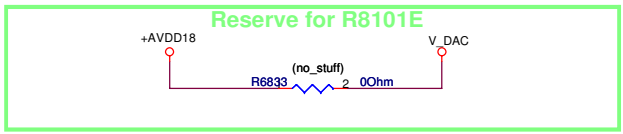


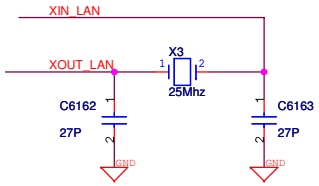






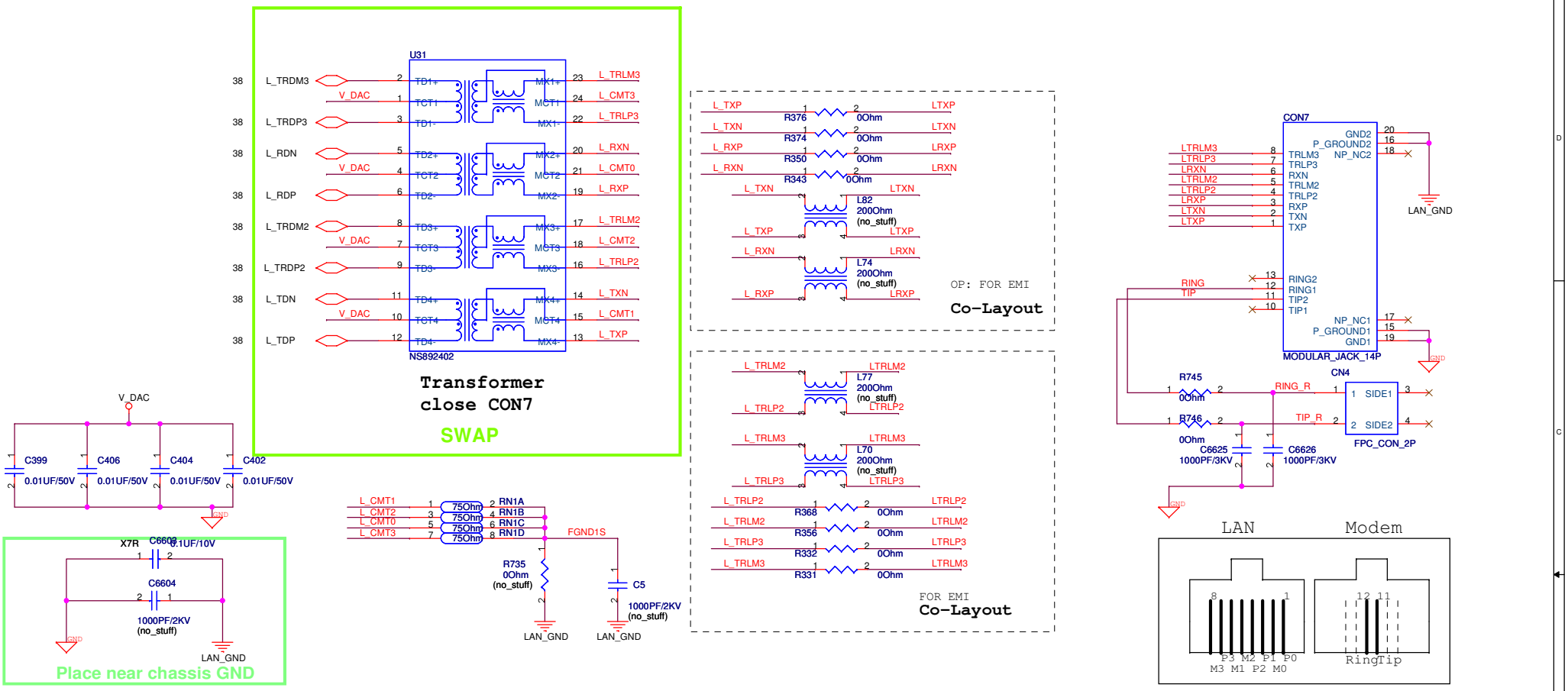




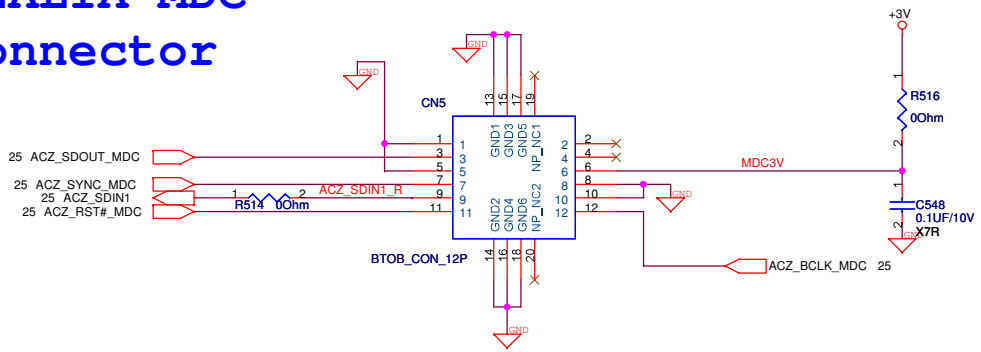


<Variant Name>

Title : GigaLAN
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: W7J
Rev: 2.0
Date: Thursday, August 31, 2006
Sheet 38 of 64



AZALIA MDC Connector



<Variant Name>

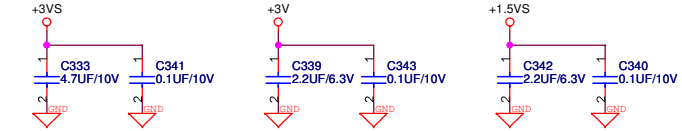
ASUSTeK COMPUTER INC

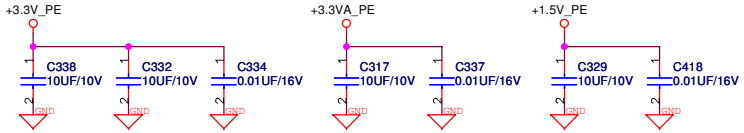
Title : RJ11+45 , MDC

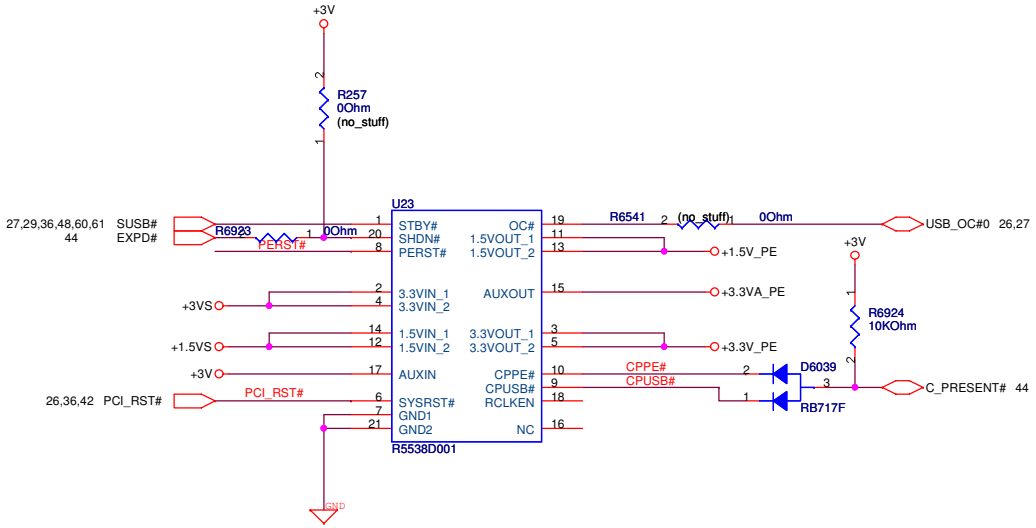
Engineer:

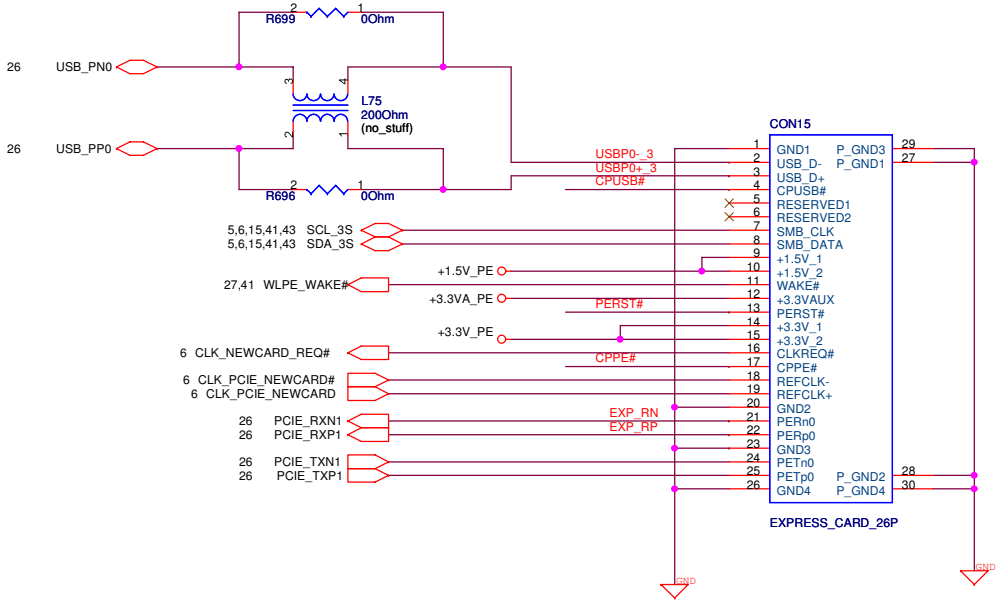
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 39 of 64









<Variant Name>

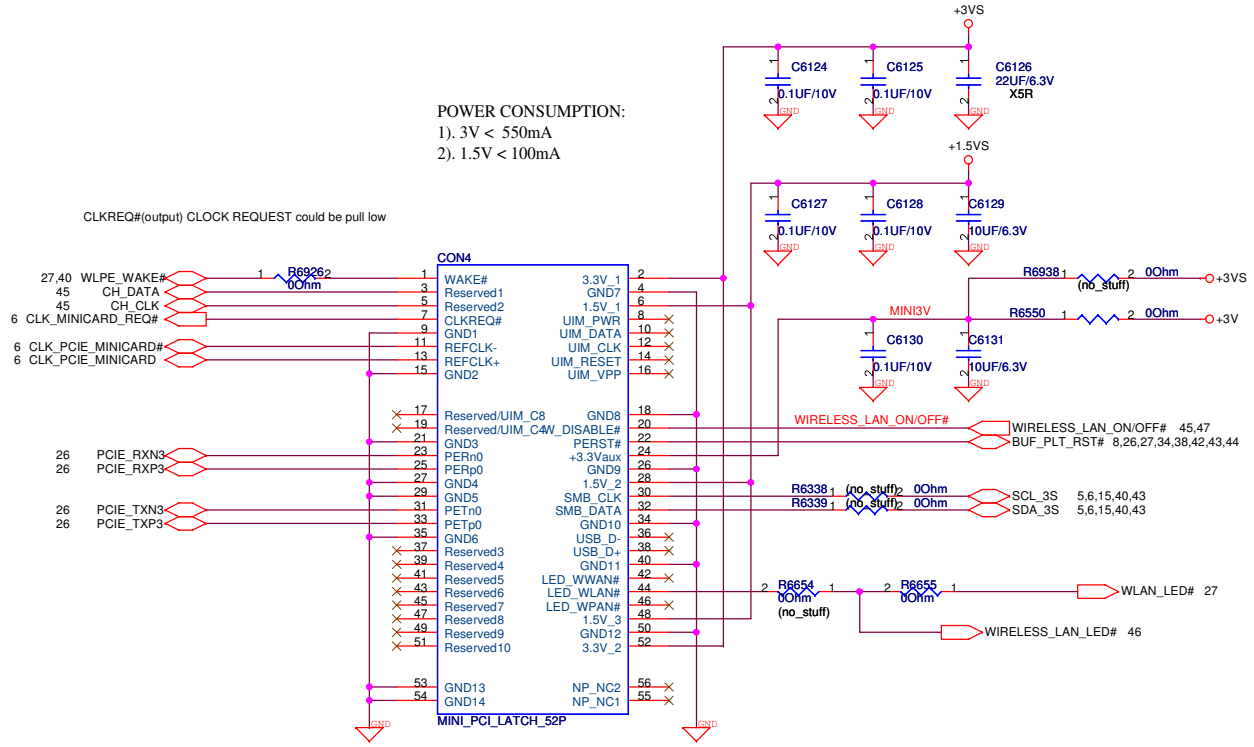
ASUSTeK COMPUTER INC

Title : Express Card

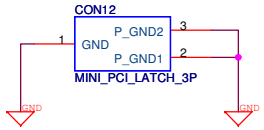
Engineer:

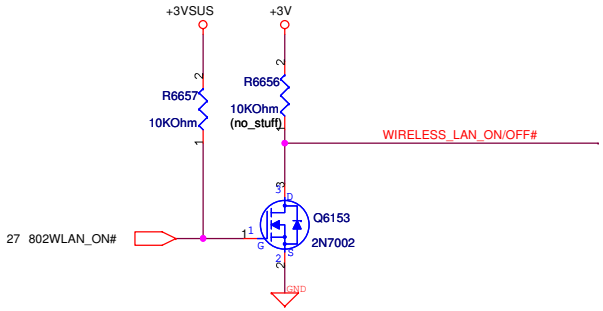
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 40 of 64



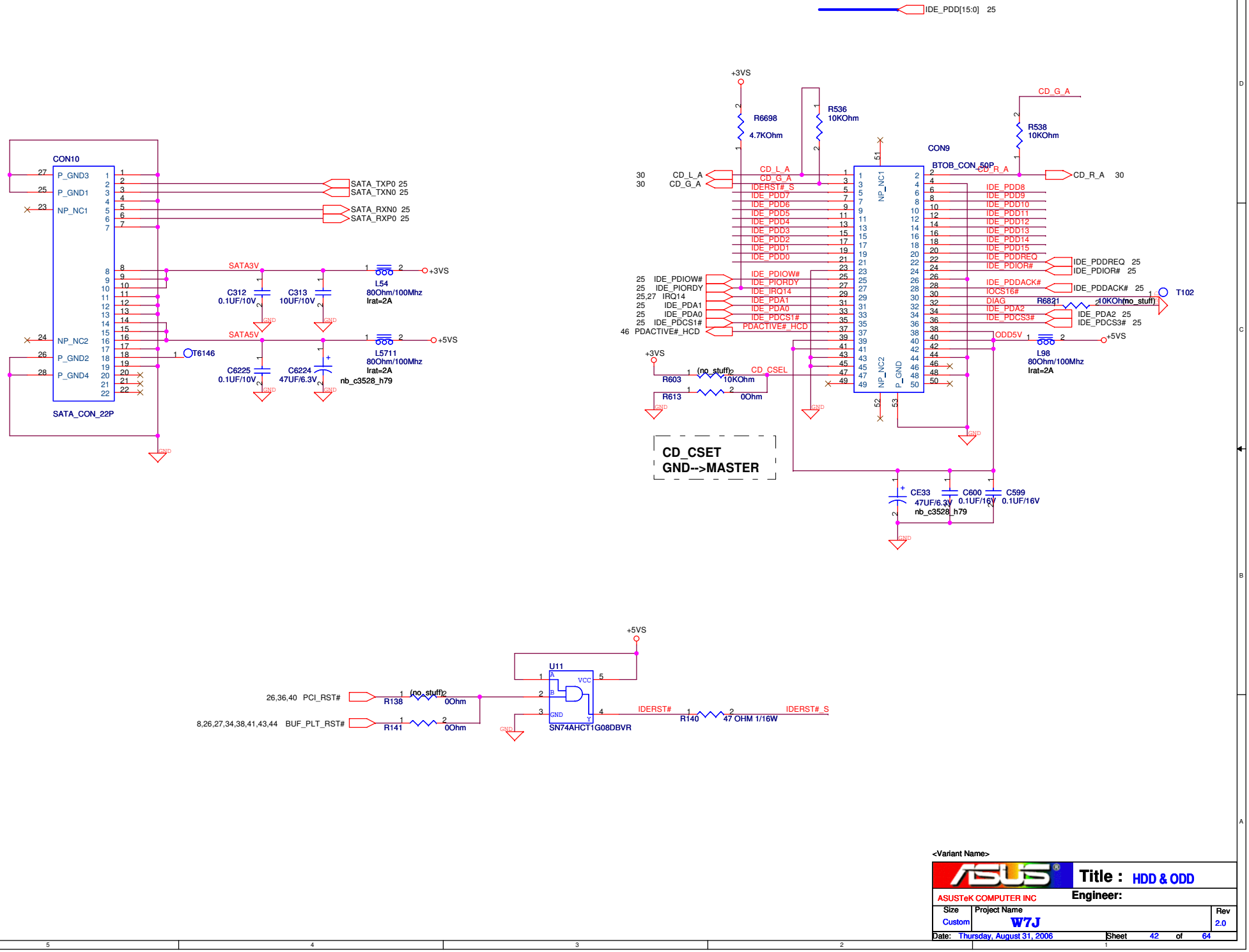
Mini Card Latch





<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD (802.11)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 41 of 64	



<Variant Name>

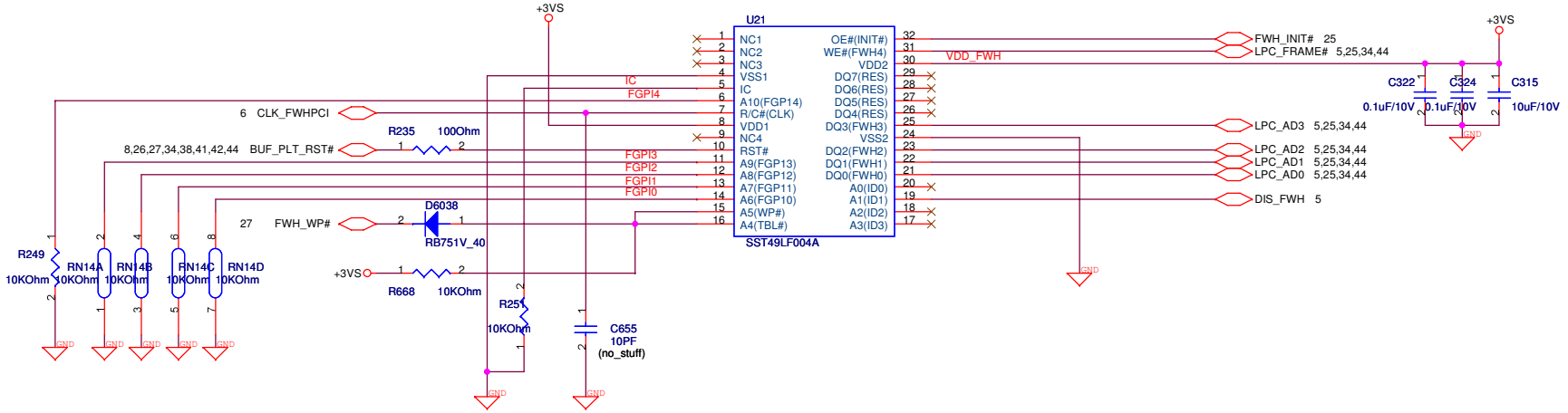
ASUSTeK COMPUTER INC

Title : HDD & ODD

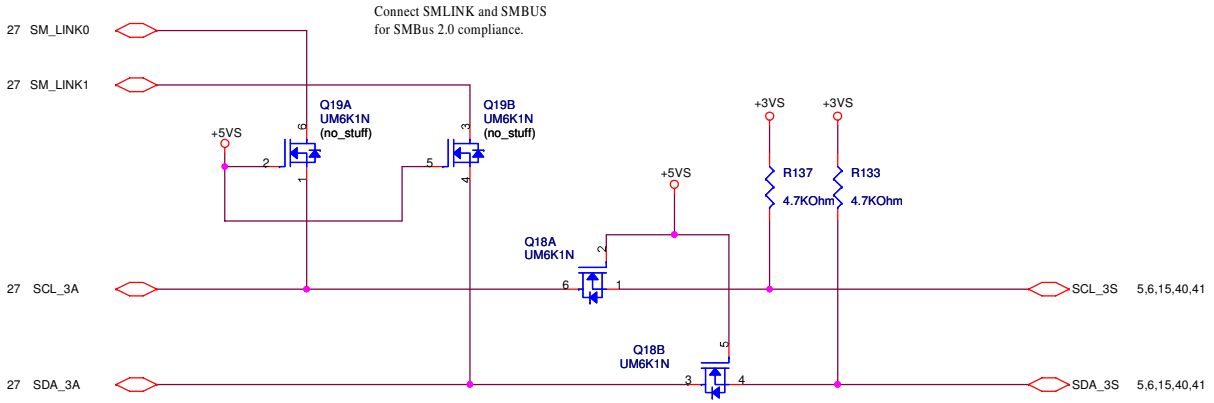
Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 42 of 64



ICH7-M



ICH7-M

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
EXPRESS CARD
MINI-CARD

<Variant Name>

ASUSTeK COMPUTER INC

Title : FWH , SM BUS

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 43 of 64

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

U46

M38857

80mA

KID1	KID0	Matrix
0	0	US
1	1	UK
0	1	JP

<Variant Name>

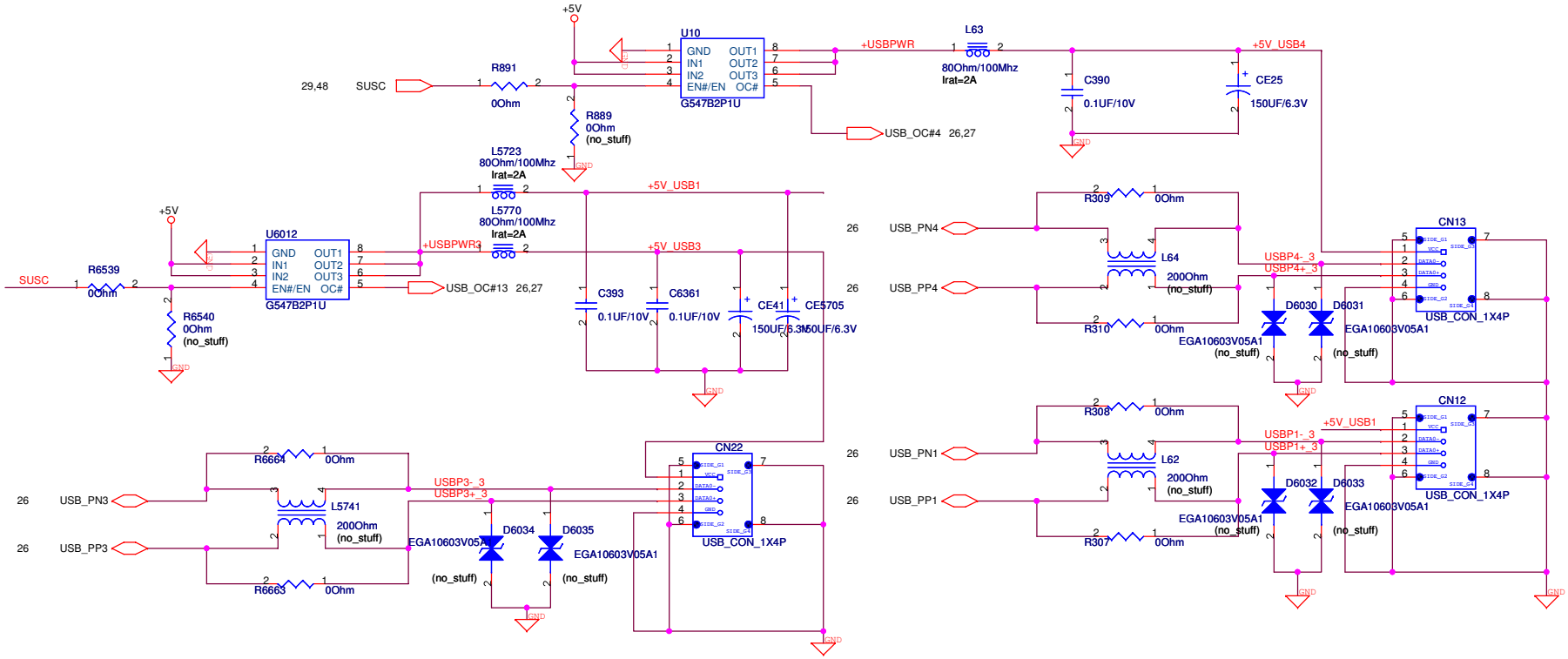
ASUSTeK COMPUTER INC

Title : KBC M38857

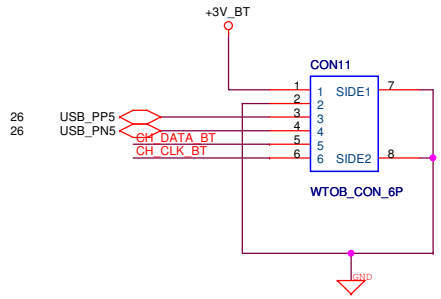
Engineer:

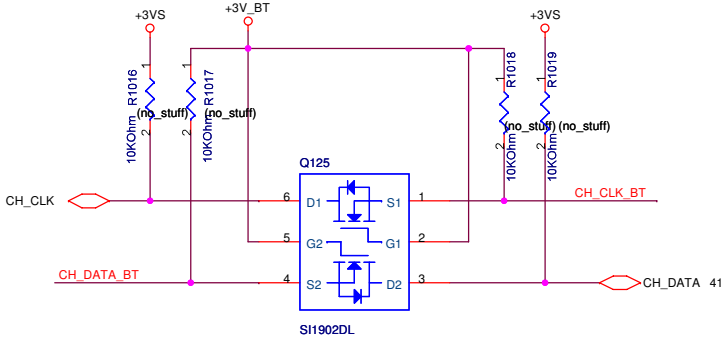
Size	Project Name	Rev
Custom	W7J	2.0

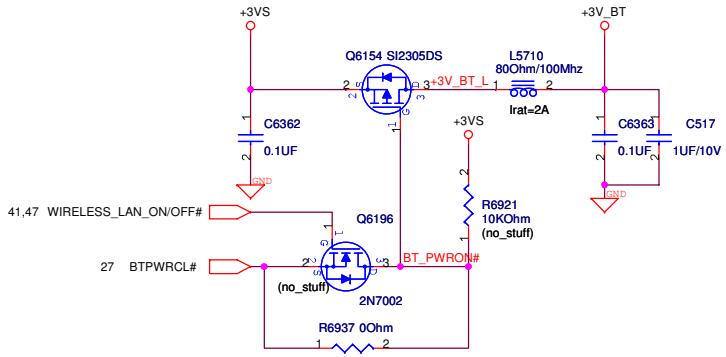
Date: Thursday, August 31, 2006 Sheet 44 of 64



Bluetooth Module Connector







<Variant Name>

ASUSTeK COMPUTER INC

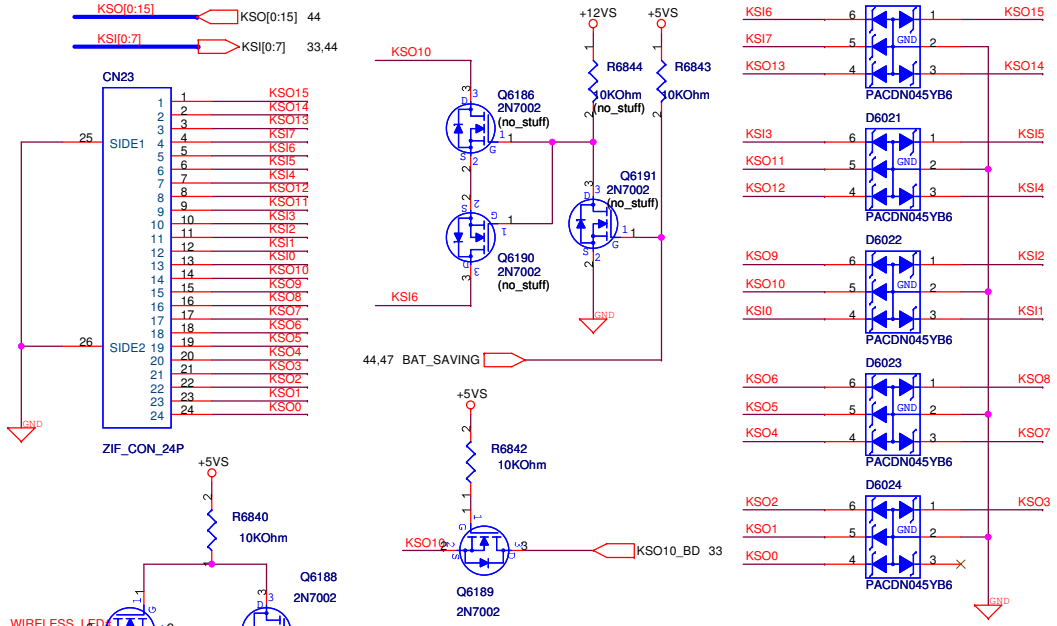
Title : USB * 3ports & BT

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

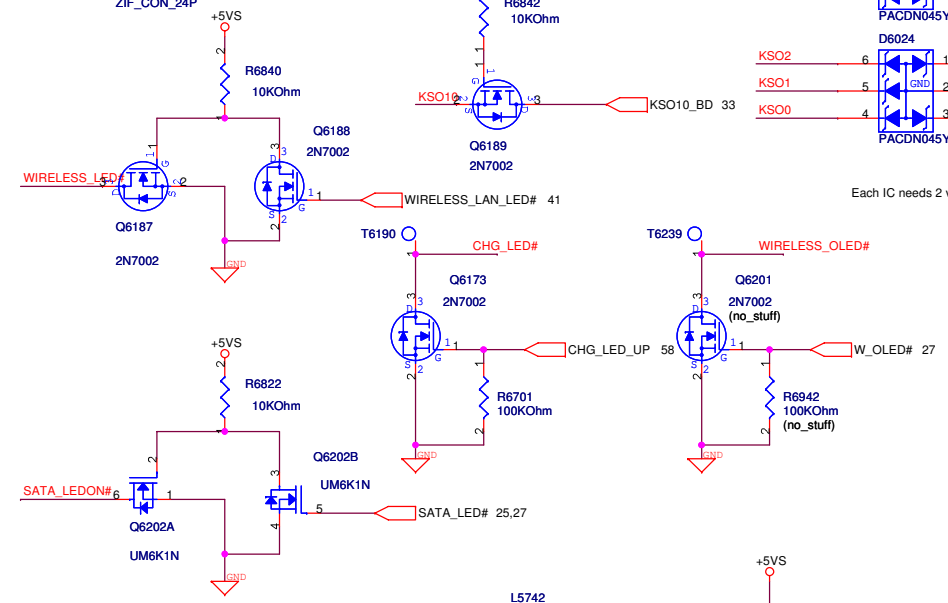
Date: Thursday, August 31, 2006 Sheet 45 of 64

Internal Keyboard Connector

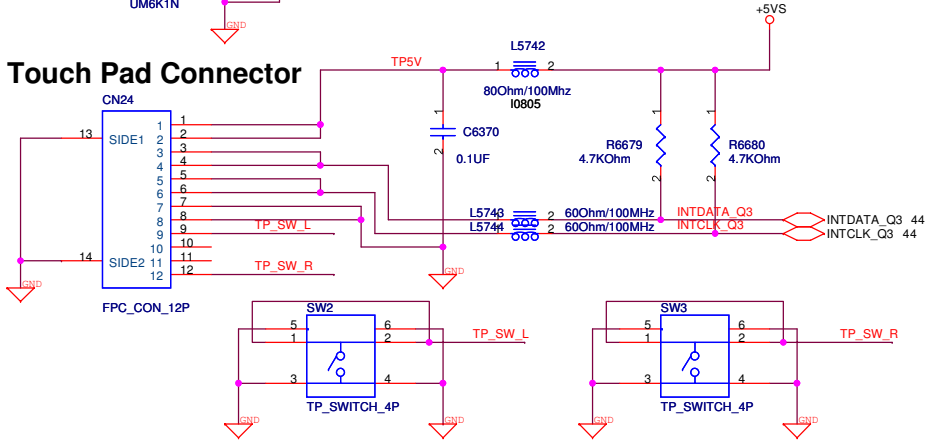


EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.

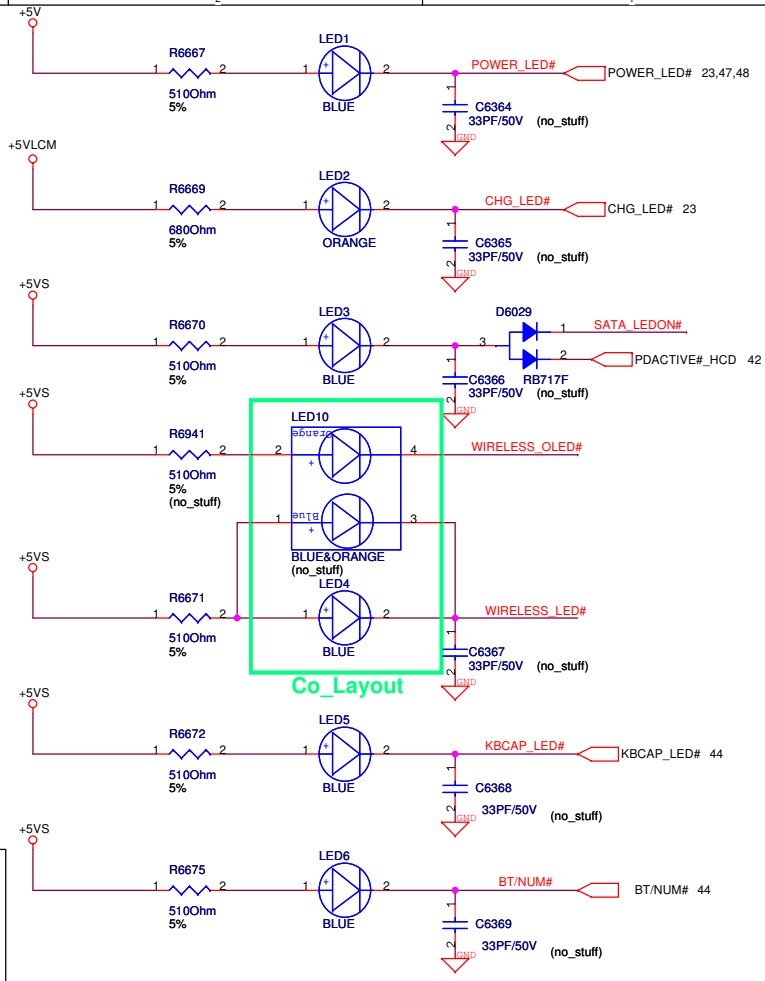
Each IC needs 2 vias to ground.



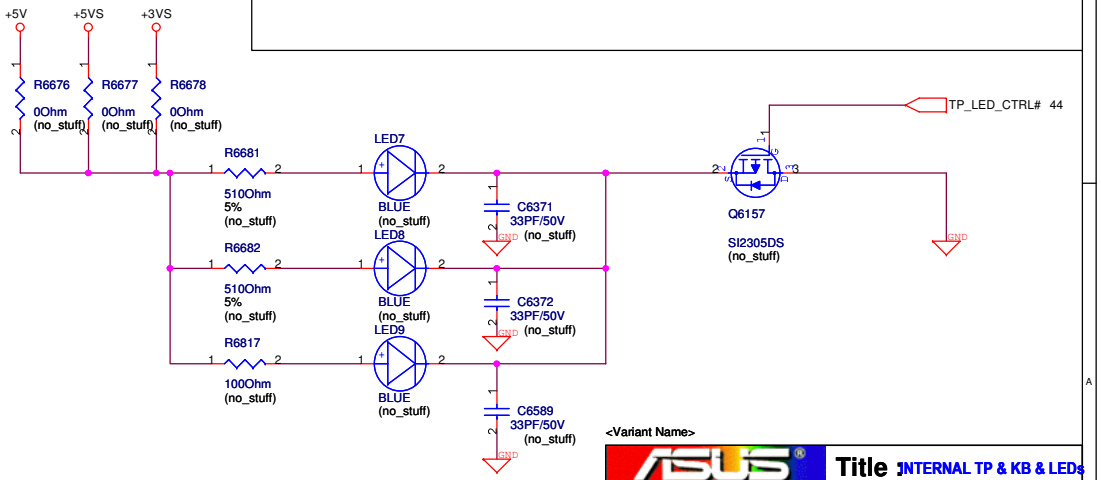
Touch Pad Connector



LEDs



Touch Pad LED



<Variant Name>

ASUSTeK COMPUTER INC

Title :INTERNAL TP & KB & LEDs

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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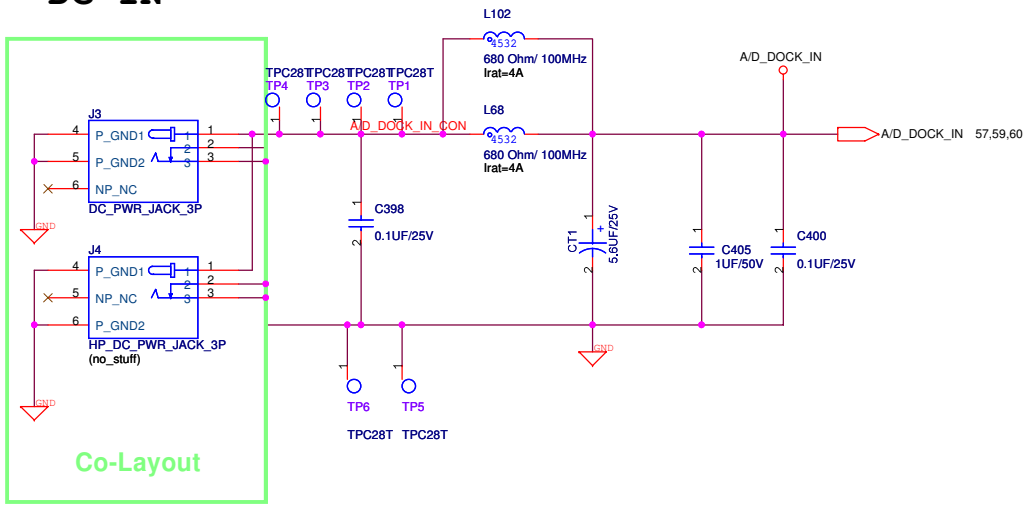
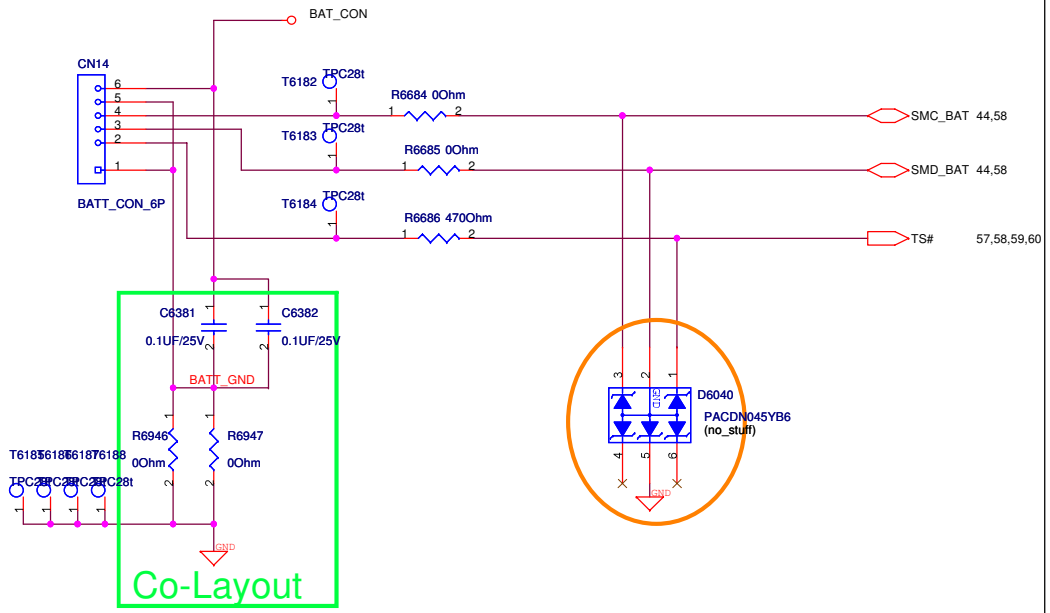
DC-IN

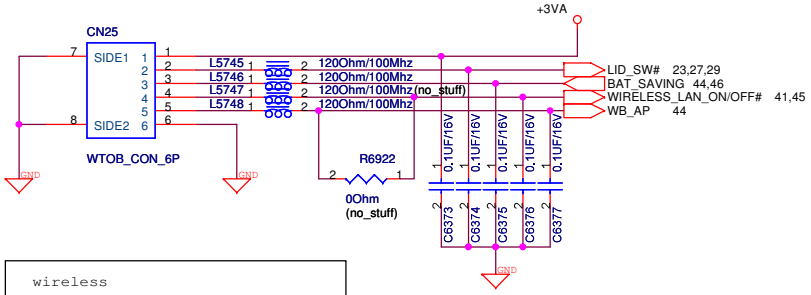


Battery Connector



EXT BOARD

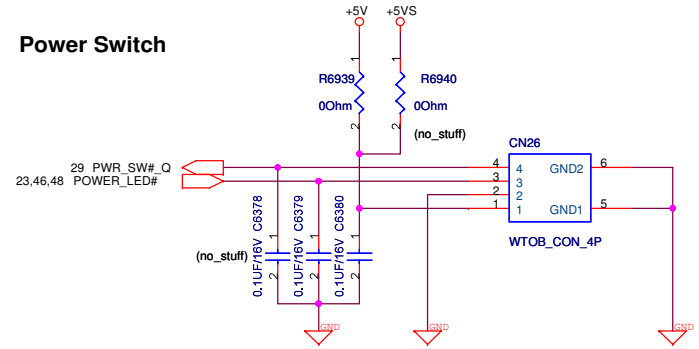
LID_SW_BD CN



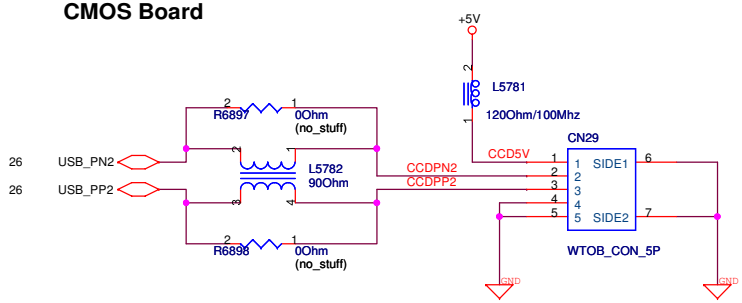

```
wireless
------------------------------
right on ---> active high
left off ---> active low


WB_AP
------------------------------
right off ---> active high
left  on  ---> active low
```

Power Switch



CMOS Board



<Variant Name>

ASUSTeK COMPUTER INC

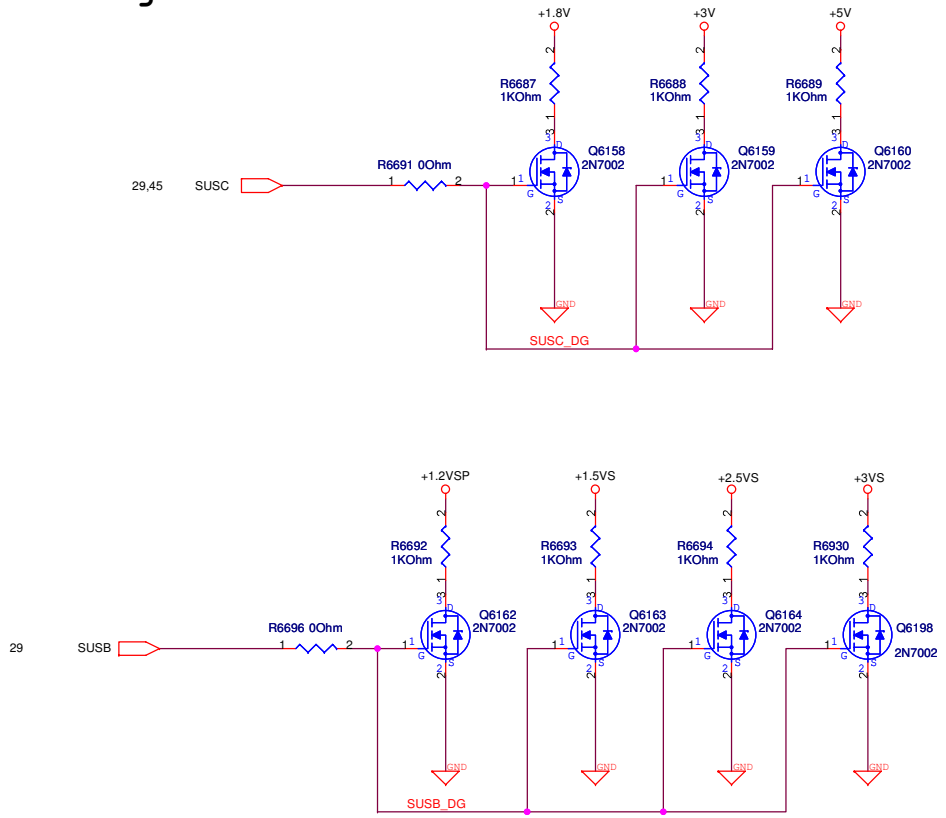
Title : DCIN,BATT CON,EXT BOARD

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 47 of 64

Discharge

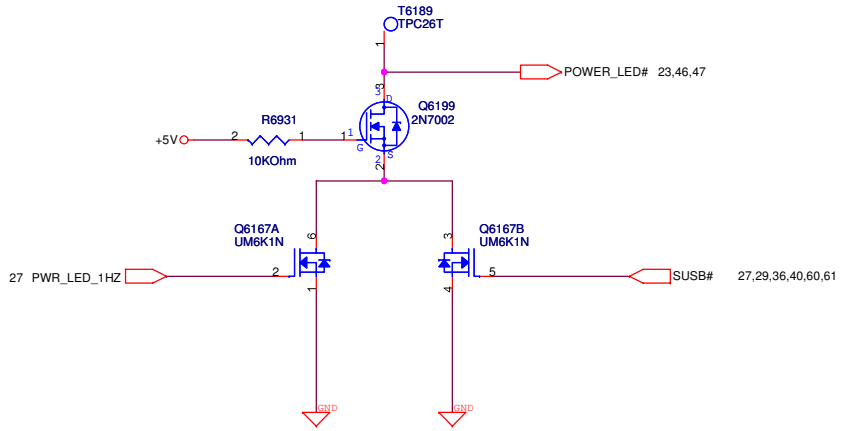


Poewr List

+3VA	+3VA	25,29,47,54,63
+3VSUS	+3VSUS	26,27,28,29,32,38,41,51
+5VA	+5VA	51,54,60
+5VSUS	+5VSUS	28,51,60
+3V	+3V	26,29,39,40,41,44,54,61
+5V	+5V	16,30,32,37,44,45,46,47,59,61
+12V	+12V	27,32,33,61
+3VS	+3VS	5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,50,52,60,61
+5VS	+5VS	5,24,28,29,30,32,33,42,43,44,46,47,50,61
+12VS	+12VS	5,24,34,46,61
+VCORE	+VCORE	3,4,5,44,50
+VCCP	+VCCP	2,3,4,6,7,8,10,11,12,25,28,52
+1.2VSP	+1.2VSP	17,18,56
+2.5VS	+2.5VS	10,20,21,54
+1.8VS	+1.8VS	20,61
+0.9VS	+0.9VS	16,53
+1.5VS	+1.5VS	3,8,10,11,26,28,40,41,52
+VCC_RTC	+VCC_RTC	25,28
+1.8V	+1.8V	8,12,13,14,15,16,53
VTT_REF	VTT_REF	8,13,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	47,57,59,60
+VGA_VCORE	+VGA_VCORE	17,55

GND

Power LED On



<Variant Name>

Discharge,Power Rail & Power LED On

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 48 of 64

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARD READER	AD19	0	E
1394	AD19	0	F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor	0101110x (2E)
PIC	1001001x (92)
Express Card	TBD
Mini Card	TBD

ICH7-M GPIO	W7J
GPIO 0	PM_BMBUSY#
GPIO 1	PCI_REQ#5
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 6	BACK_OFF#
GPIO 7	MUTE_POP_ICHGPIO#
GPIO 8	EXTSMI#
GPIO 9	W_OLED#
GPIO 10	(PWRLMT#)
GPIO 11	SMBALERT#
GPIO 12	KBC_SCI#
GPIO 13	PWR_LED_1HZ
GPIO 14	WLAN_ON#
GPIO 15	802_LED_EN#
GPIO 16	DPRSLPVR
GPIO 17	GNT5#
GPIO 18	STP_PCI#
GPIO 19	Memoryclk
GPIO 20	STP_CPU#
GPIO 21	
GPIO 22	PCI_REQ#4
GPIO 23	LPC_DRQ#1
GPIO 24	SW_RST#
GPIO 25	CB_SD#
GPIO 26	MEM ID0
GPIO 27	MEM ID1
GPIO 28	MEM ID2
GPIO 29	USB_OC#5
GPIO 30	USB_OC#6
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 33	BT_ON#
GPIO 34	FWH_WP#
GPIO 35	SATACLKREQ#
GPIO 36	BT_LED_EN#
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 48	GNT4#
GPIO 49	CPUPWRGD

KBC GPIO	W7J
P23	
P22	BAT_LEARN
P21	
P20	KBCRSM
P42	WATCHDOG
P43	
P44	xKBRC
P45	GA20
P46	KBDSCI
P47	CLKRUN#
P50	BAT_LLOW#
P51	TP_LED_CTRL#
P52	
P53	EXPD#
P54	LID_EC#
P55	BAT_IN#
P56	CPU_FAN_PWM
P57	ADJ_BL
P67	WB_AP
P66	M_MODE#
P65	
P64	ACIN#
P63	EOC#_LED
P62	C_PRESENT#
P61	ACZ_RST#_AUD
P60	
P75	KBDCLK_5S
P74	MOUSECLK_5S
P73	INTCLK_Q3
P72	KBDDATA_5S
P71	MOUSEDATA_5S
P70	INTDATA_Q3
P77	SMC_KBC
P76	SMD_KBC
P27	SCROLL_LED#
P26	NUM_LED#
P25	CAP_LED#
P24	SET_RSTNS#
P40	EXT_SMI#
P41	

<Variant Name>

ASUSTeK COMPUTER INC

Title : System Resource

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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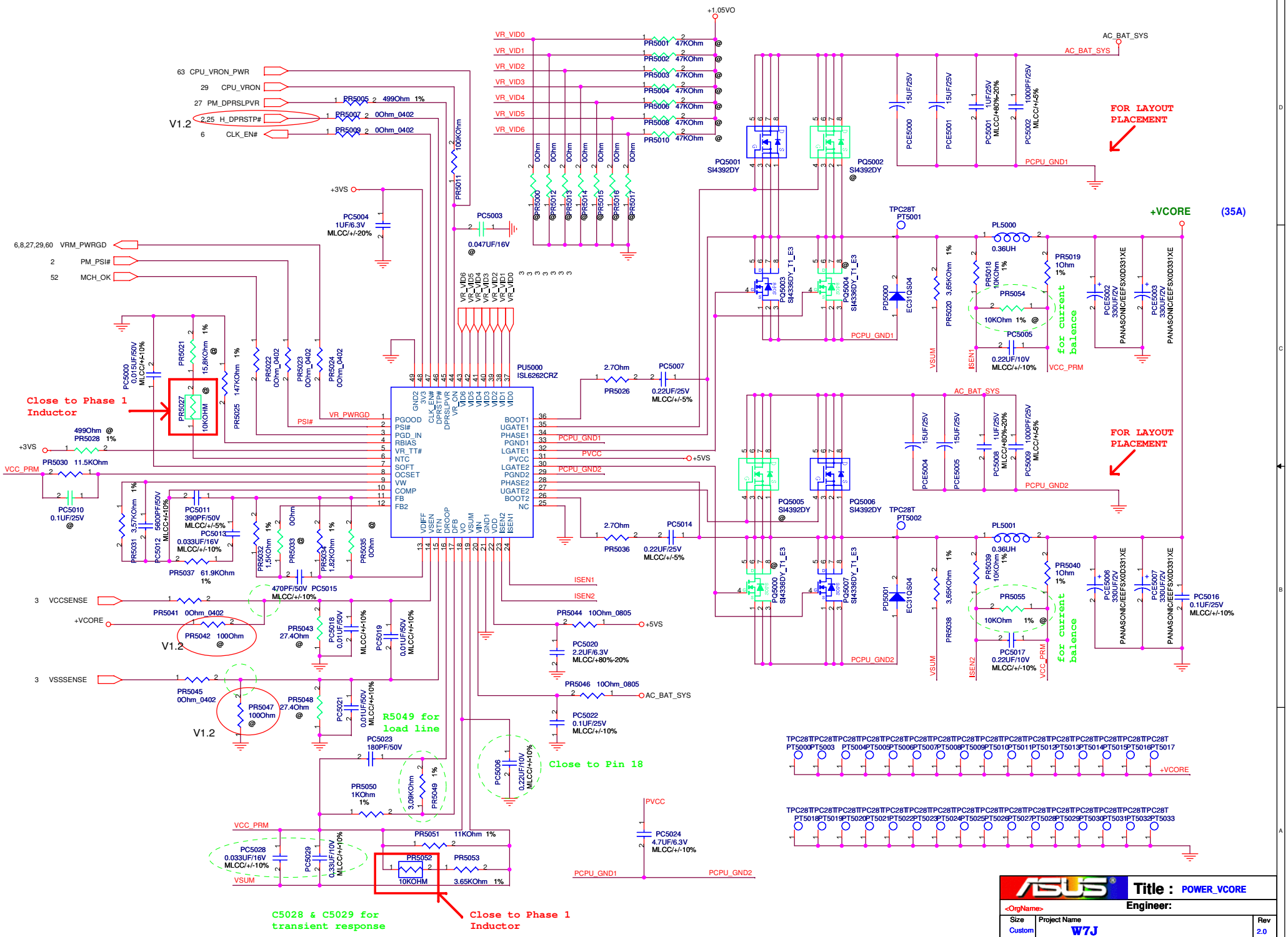
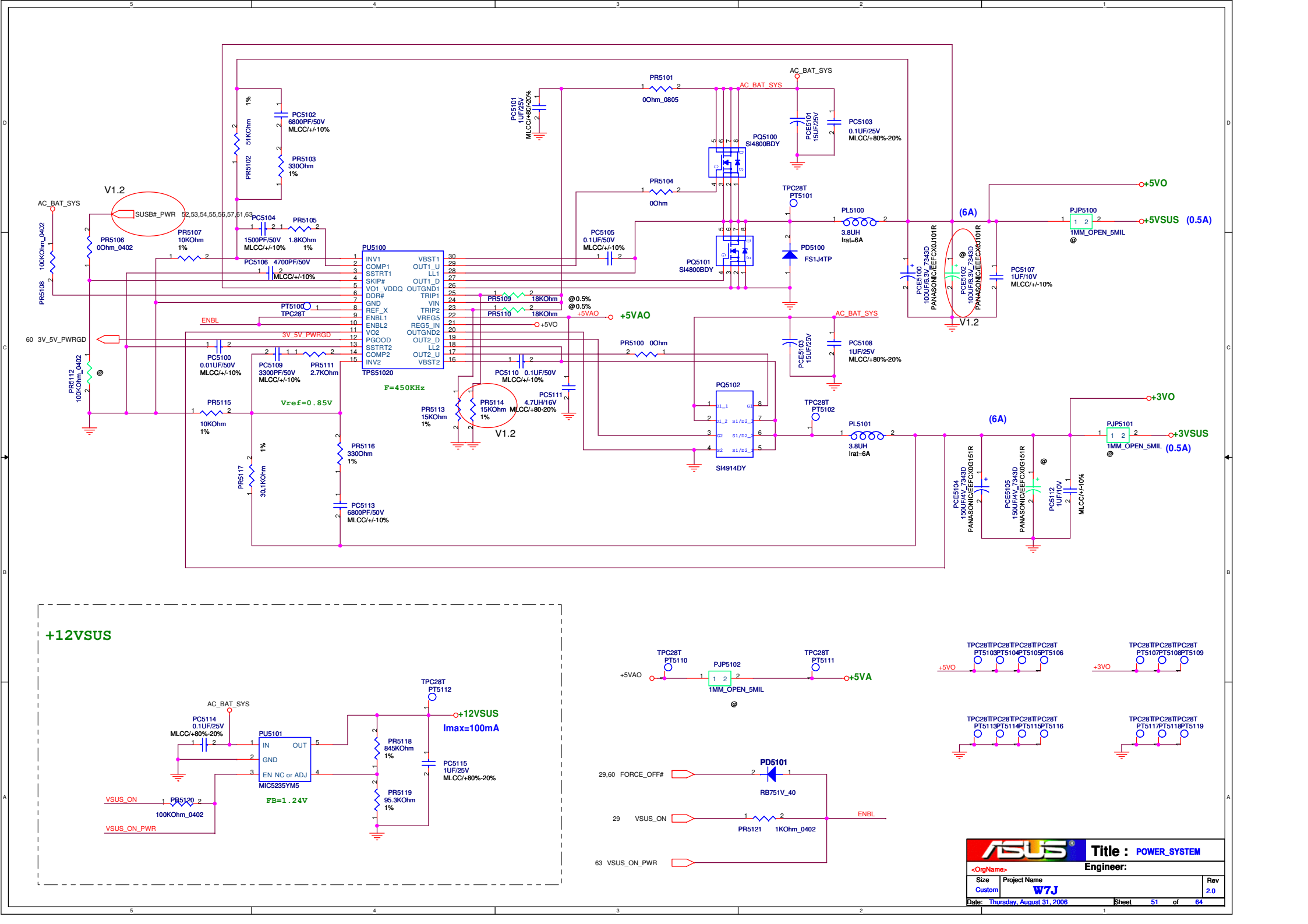
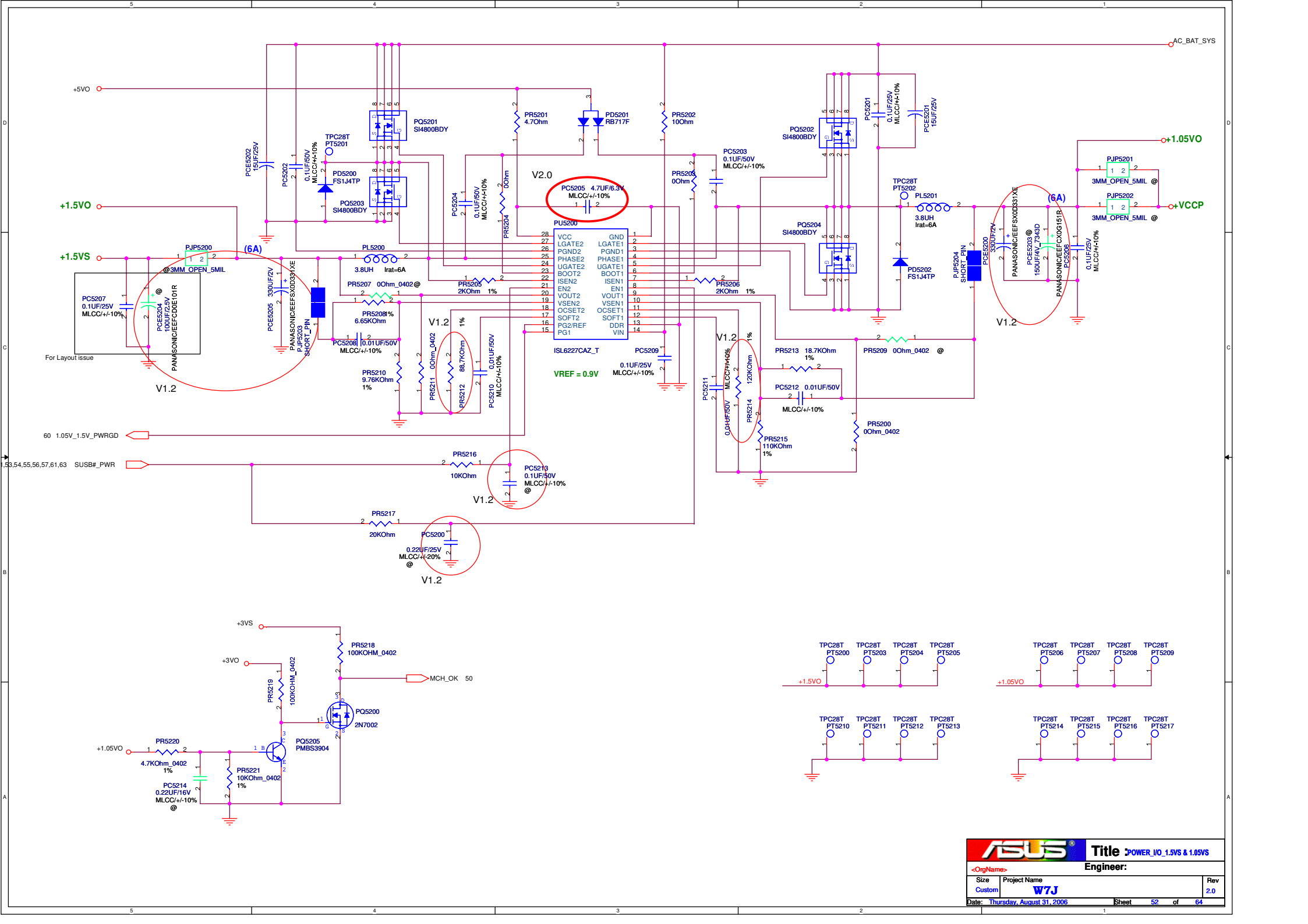
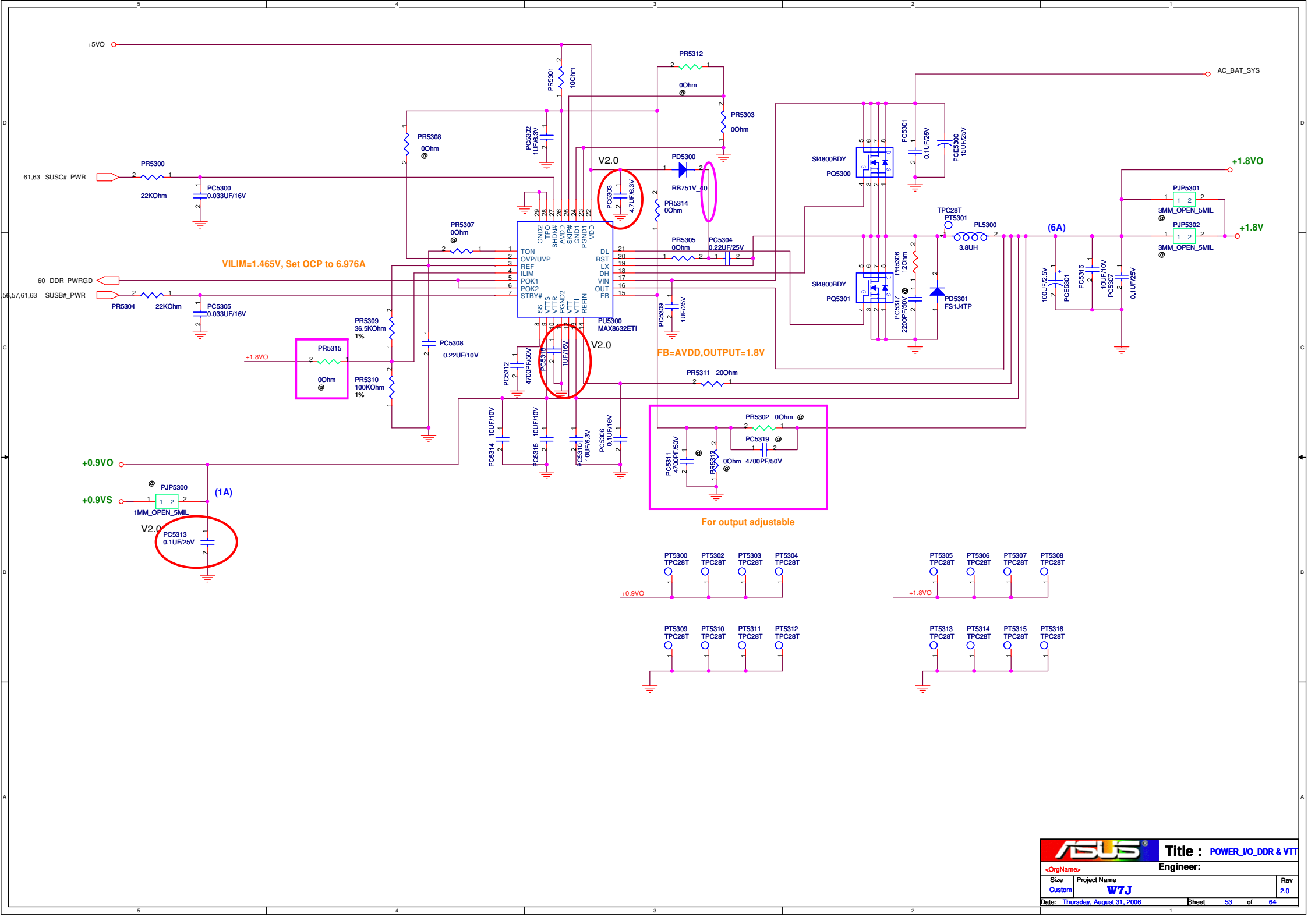

+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5006 47KOhm
PR5008 47KOhm
PR5010 47KOhm
AC_BAT_SYS
FOR LAYOUT PLACEMENT
PCPU_GND1
PQ5001 SI4392DY
PQ5002 SI4392DY
PCE5000 15UF/25V
PCE5001 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/25V MLCC/+/-5%
+VCORE (35A)
TPC28T PT5001
PL5000 0.36UH
PR5019 1Ohm 1%
PR5018 10KOhm 1%
PR5054 10KOhm 1% @
PC5005 0.22UF/10V MLCC/+/-10%
for current balence
PCE5002 330UF/2V PANASONIC/EEFSXOD331XE
PCE5003 330UF/2V PANASONIC/EEFSXOD331XE
PD5000 EC31QS04
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PR5020 3.65KOhm 1%
VSUM
ISEN1
VCC_PRM
PU5000 ISL6262CRZ
PR5026 2.7Ohm
PC5007 0.22UF/25V MLCC/+/-5%
PCPU_GND2
PVCC
+5VS
PQ5005 SI4392DY @
PQ5006 SI4392DY
PCE5004 15UF/25V
PCE5005 15UF/25V
PC5008 1UF/25V MLCC/+80%-20%
PC5009 1000PF/25V MLCC/+/-5%
TPC28T PT5002
PL5001 0.36UH
PR5040 1Ohm 1%
PR5039 10KOhm 1%
PR5055 10KOhm 1% @
PC5017 0.22UF/10V MLCC/+/-10%
PC5006 330UF/2V PANASONIC/EEFSXOD331XE
PCE5007 330UF/2V PANASONIC/EEFSXOD331XE
PC5016 0.1UF/25V MLCC/+/-10%
PD5001 EC31QS04
PQ5007 SI4336DY_T1_E3
PQ5008 SI4336DY_T1_E3
PR5038 3.65KOhm 1%
PR5026 2.7Ohm
PC5014 0.22UF/25V MLCC/+/-5%
PR5036 2.7Ohm
63 CPU_VRON_PWR
29 CPU_VRON
27 PM_DPRSLPVR
2,25 H_DPRSTP#
6 CLK_EN#
V1.2
PR5005 499Ohm 1%
PR5007 0Ohm_0402
PR5009 0Ohm_0402
PR5011 100KOhm
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5003 0.047UF/16V @
PR5000 0Ohm
PR5012 0Ohm
PR5013 0Ohm
PR5014 0Ohm
PR5015 0Ohm
PR5016 0Ohm
PR5017 0Ohm
6,8,27,29,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
PC5000 0.015UF/50V MLCC/+/-10%
PR5021 15.8KOhm 1%
PR5027 10KOHM 1%
PR5022 0Ohm_0402
PR5023 0Ohm_0402
PR5024 0Ohm_0402
PR5025 147KOhm 1%
Close to Phase 1 Inductor
PSI#
VR_PWRGD
499Ohm @ PR5028 1%
PR5030 11.5KOhm
PC5010 0.1UF/25V @
PR5031 3.57KOhm 1%
PC5012 560PF/50V MLCC/+/-10%
PC5011 390PF/50V MLCC/+/-5%
PC5013 0.033UF/16V MLCC/+/-10%
PR5037 61.9KOhm 1%
PR5032 1.5KOhm 1%
PR5033 0Ohm @
PR5034 1.82KOhm 1%
PR5035 0Ohm @
470PF/50V PC5015 MLCC/+/-10%
3 VCCSENSE
+VCORE
PR5041 0Ohm_0402
PR5042 100Ohm @
PR5043 27.4Ohm @
PC5018 0.01UF/50V MLCC/+/-10%
PC5019 0.01UF/50V MLCC/+/-10%
3 VSSSENSE
PR5045 0Ohm_0402
PR5047 100Ohm @
PR5048 27.4Ohm @
PC5021 0.01UF/50V MLCC/+/-10%
R5049 for load line
PC5023 180PF/50V
PR5050 1KOhm 1%
PR5049 3.09KOhm 1%
PC5006 0.22UF/10V MLCC/+/-10%
Close to Pin 18
PR5044 10Ohm_0805
PC5020 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
PC5022 0.1UF/25V MLCC/+/-10%
AC_BAT_SYS
PC5024 4.7UF/6.3V MLCC/+/-10%
PR5051 11KOhm 1%
PR5052 10KOHM
PR5053 3.65KOhm 1%
PC5028 0.033UF/16V MLCC/+/-10%
PC5029 0.33UF/10V MLCC/+/-10%
C5028 & C5029 for transient response
Close to Phase 1 Inductor
TPC28T PT5000 PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
Engineer:
<OrgName>
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 50 of 64



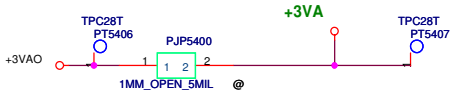
ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 51 of 64	

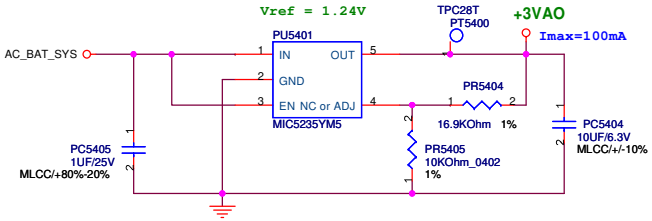

AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
PU5200
ISL6227CAZ_T
VREF = 0.9V
V2.0
V1.2
PQ5201 SI4800BDY
PQ5202 SI4800BDY
PQ5203 SI4800BDY
PQ5204 SI4800BDY
PD5200 FS1J4TP
PD5201 RB717F
PD5202 FS1J4TP
PL5200 3.8UH Irat=6A
PL5201 3.8UH Irat=6A
PJP5200
PJP5201 3MM_OPEN_5MIL @
PJP5202 3MM_OPEN_5MIL @
PJP5203 SHORT_PIN
PJP5204 SHORT_PIN
PR5201 4.7Ohm
PR5202 10Ohm
PR5203 0Ohm
PR5204 0Ohm
PR5205 2KOhm 1%
PR5206 2KOhm 1%
PR5207 0Ohm_0402 @
PR5208 6.65KOhm 1%
PR5209 0Ohm_0402 @
PR5210 9.76KOhm 1%
PR5211 0Ohm_0402
PR5212 88.7KOhm 1%
PR5213 18.7KOhm 1%
PR5214 120KOhm 1%
PR5215 110KOhm 1%
PR5216 10KOhm
PR5217 20KOhm
PR5218 100KOHM_0402
PR5219 100KOHM_0402
PR5220 4.7KOhm_0402 1%
PR5221 10KOhm_0402 1%
PR5200 0Ohm_0402
PC5201 0.1UF/25V MLCC/+/-10%
PC5202 0.1UF/50V MLCC/+/-10%
PC5203 0.1UF/50V MLCC/+/-10%
PC5204 0.1UF/50V MLCC/+/-10%
PC5205 4.7UF/6.3V MLCC/+/-10%
PC5206 0.1UF/25V MLCC/+/-10%
PC5207 0.1UF/25V MLCC/+/-10%
PC5208 0.01UF/50V MLCC/+/-10%
PC5209 0.1UF/25V MLCC/+/-10%
PC5210 0.01UF/50V MLCC/+/-10%
PC5211 0.01UF/50V MLCC/+/-10%
PC5212 0.01UF/50V MLCC/+/-10%
PC5213 0.1UF/50V MLCC/+/-10% @
PC5214 0.22UF/16V MLCC/+/-10% @
PC5200 0.22UF/25V MLCC/+/-20% @
PCE5202 15UF/25V
PCE5201 15UF/25V
PCE5200 330UF/2V
PCE5205 330UF/2V
PCE5204 100UF/2.5V
PANASONIC/EEFCD0E101R
PANASONIC/EEFSXOD331XE
PANASONIC/EEFCX0G151R
PCE5203 @ 150UF/4V_7343D
PC5207 0.1UF/25V MLCC/+/-10%
For Layout issue
(6A)
V1.2
TPC28T PT5201
TPC28T PT5202
TPC28T PT5200
TPC28T PT5203
TPC28T PT5204
TPC28T PT5205
TPC28T PT5206
TPC28T PT5207
TPC28T PT5208
TPC28T PT5209
TPC28T PT5210
TPC28T PT5211
TPC28T PT5212
TPC28T PT5213
TPC28T PT5214
TPC28T PT5215
TPC28T PT5216
TPC28T PT5217
PQ5205 PMBS3904
PQ5200 2N7002
60 1.05V_1.5V_PWRGD
53,54,55,56,57,61,63 SUSB#_PWR
MCH_OK 50
+3VS
+3VO
Title :POWER_I/O_1.5VS & 1.05VS
Engineer:
<OrgName>
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 52 of 64



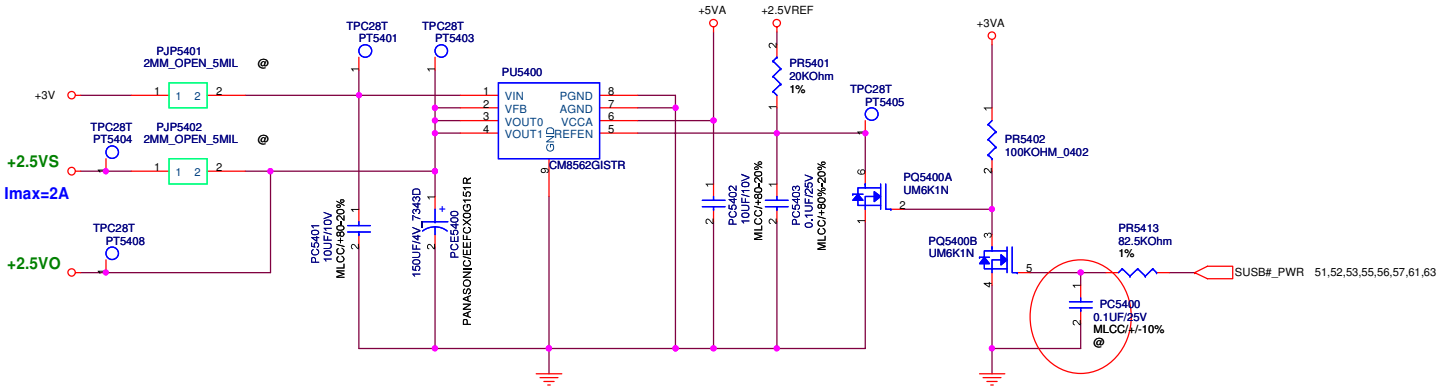
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 53 of 64	

+3VAO

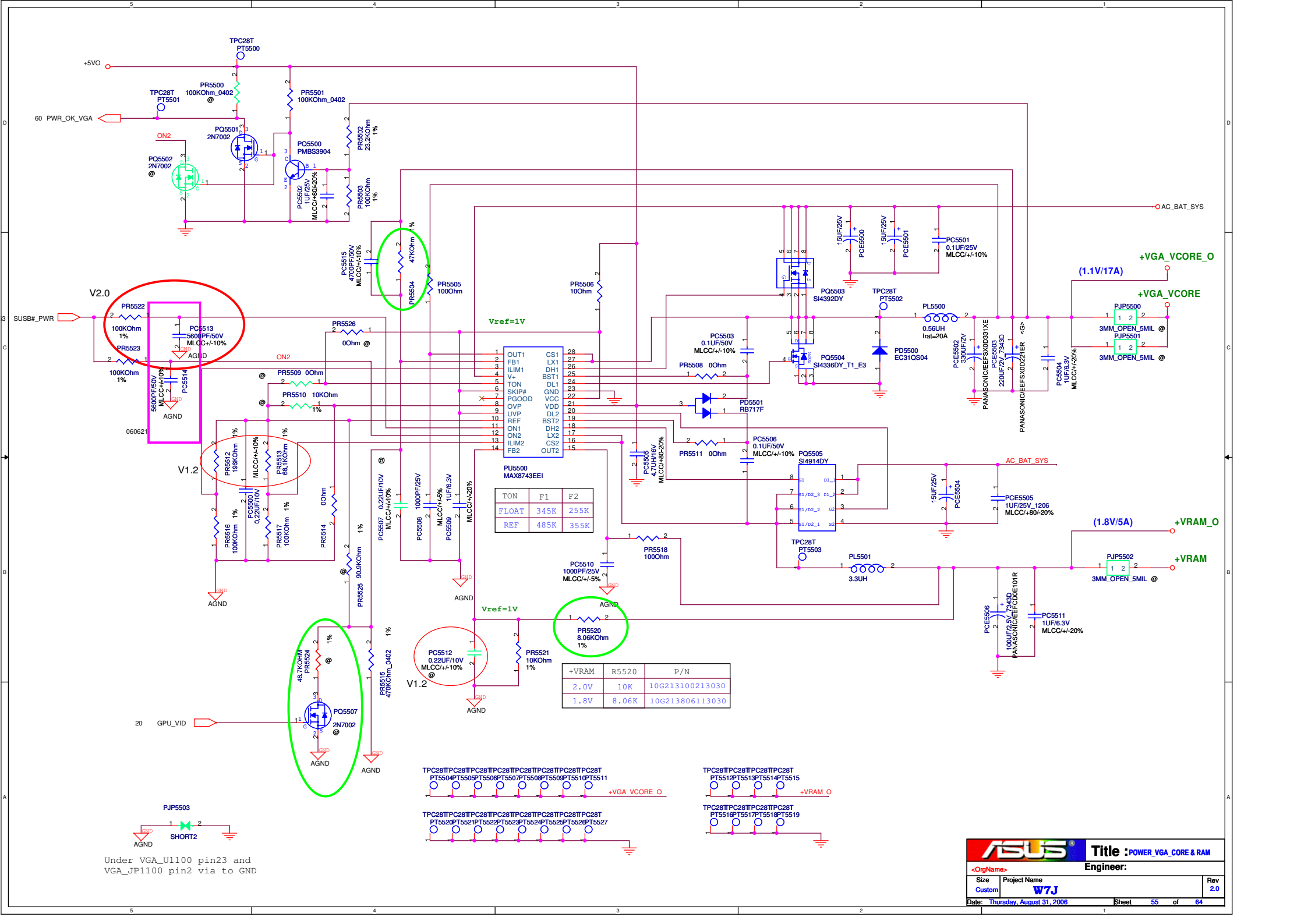




+2.5VS



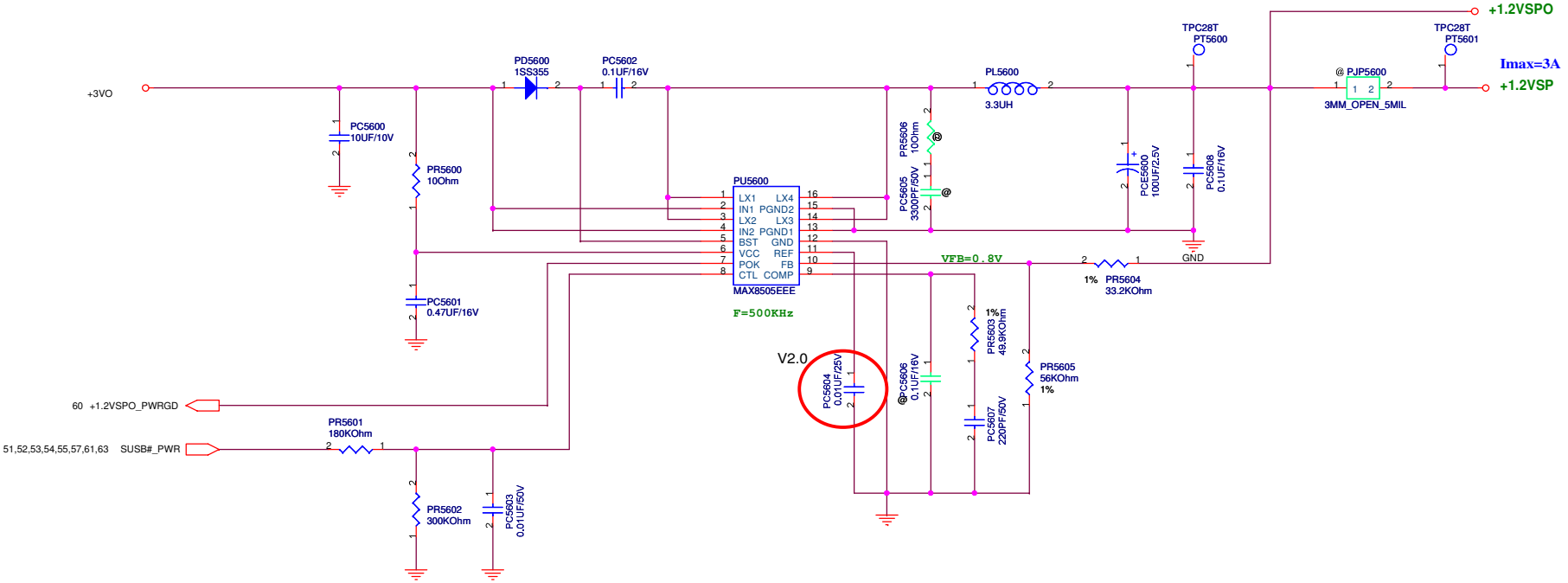
Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 54 of 64	



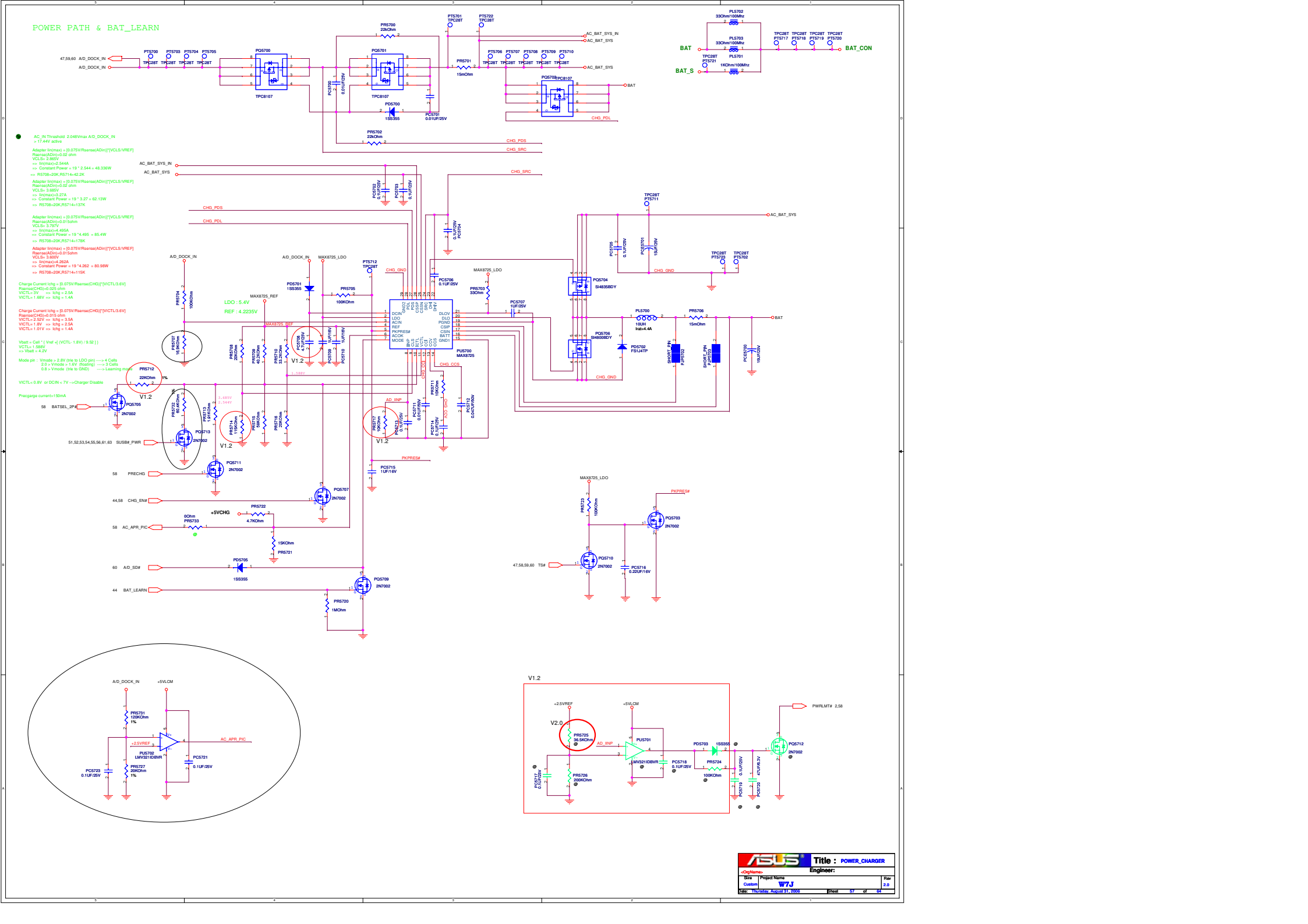
TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

+1.2VSP

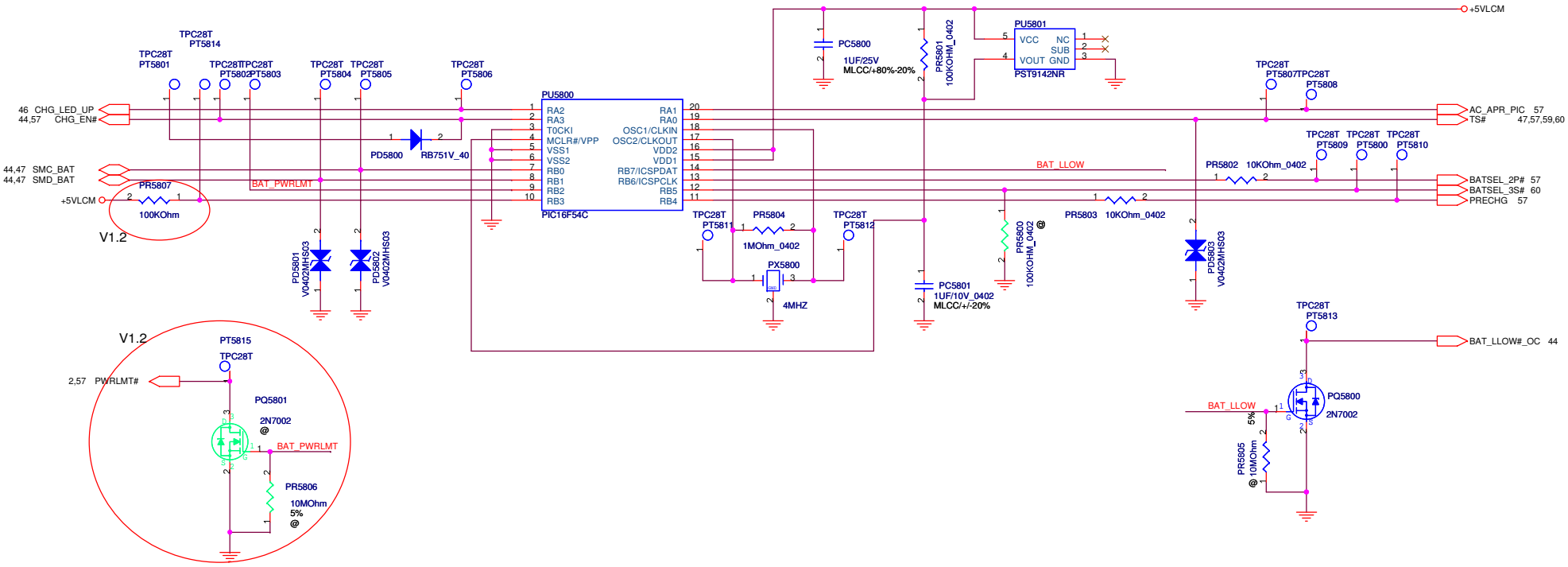


ASUS	Title : POWER_VGA_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 56 of 64	



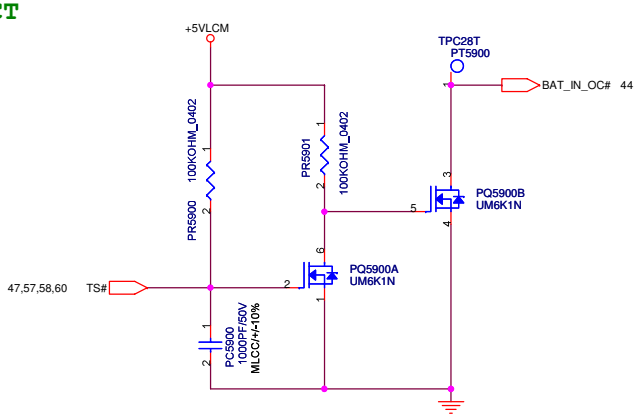
Title :	POWER_CHARGER
Engineer:	
<OrgName>	
Size: Custom	Project Name: W7J
Rev:	2.0
Date:	Thursday, August 31, 2006
Sheet	57 of 64

PIC16F54C

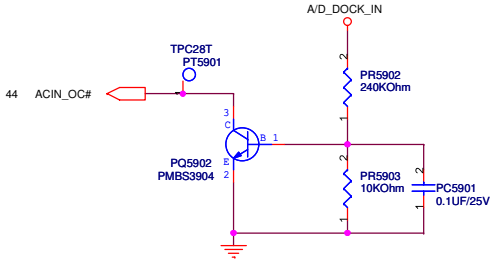


ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 58 of 64	

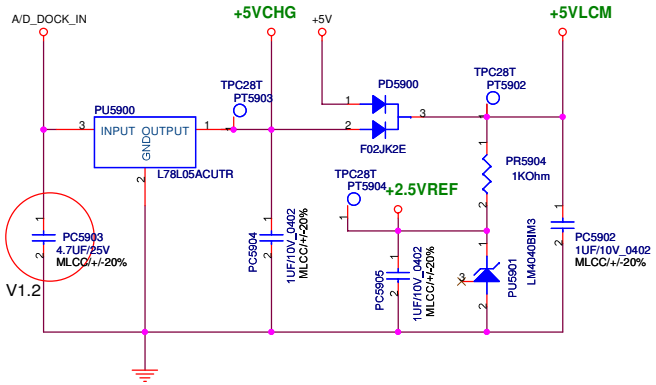
BATTERY IN DETECT



ADAPTER IN DETECT

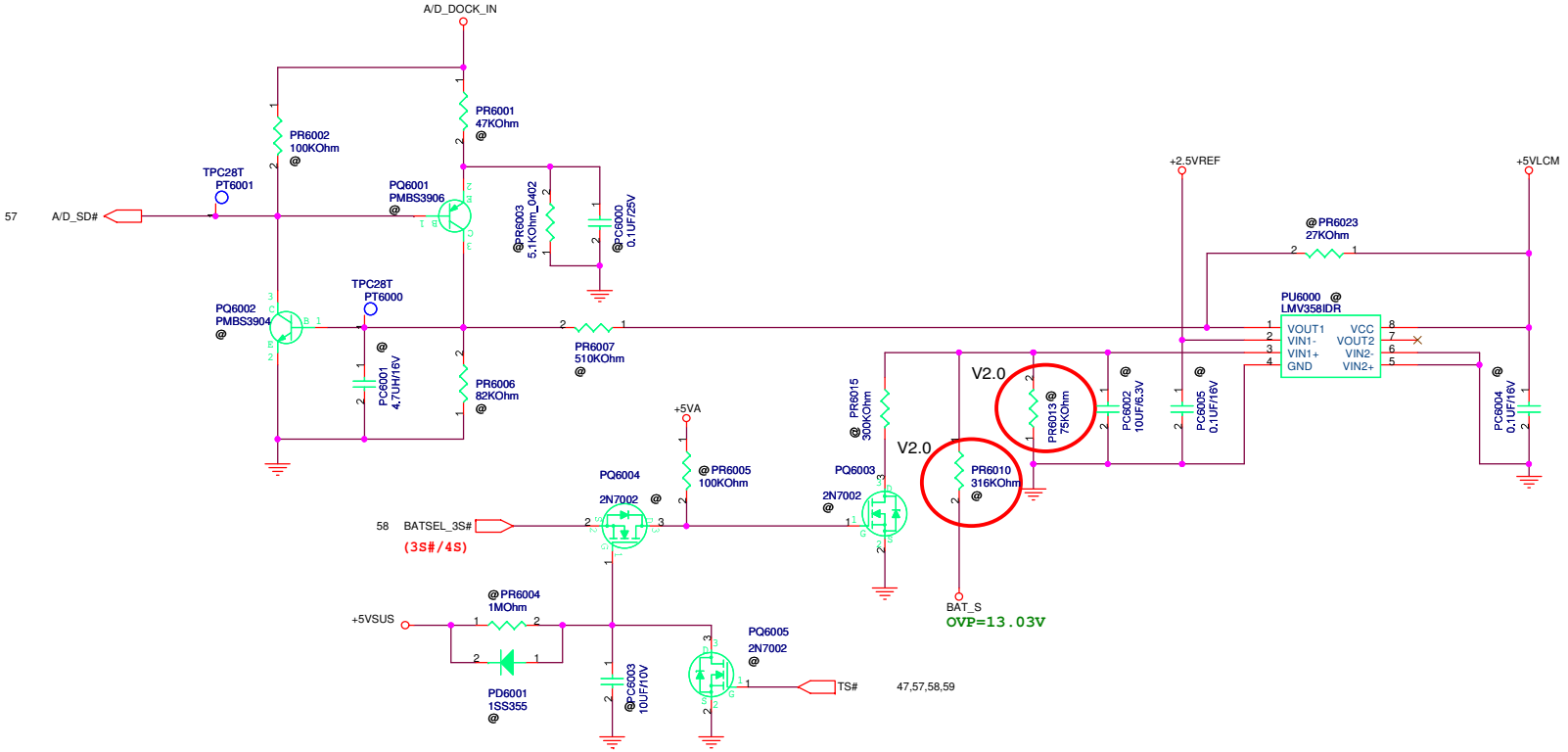


+5VLCM, +5VCHG & +2.5VREF

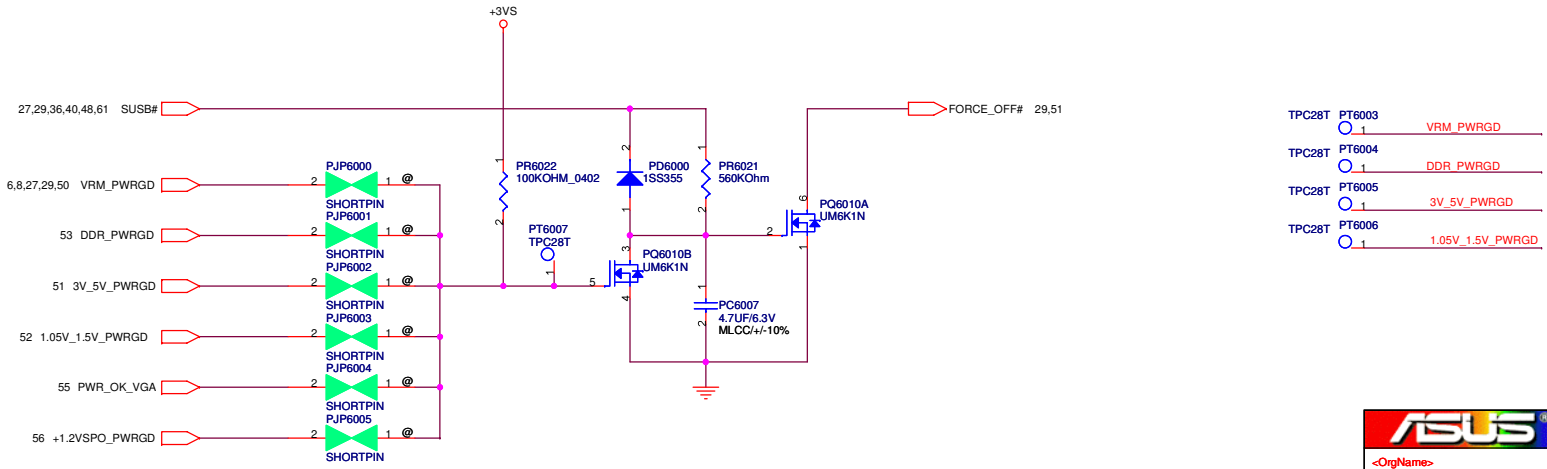


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 59 of 64	

BATTERY A/D_SD# (OVP)

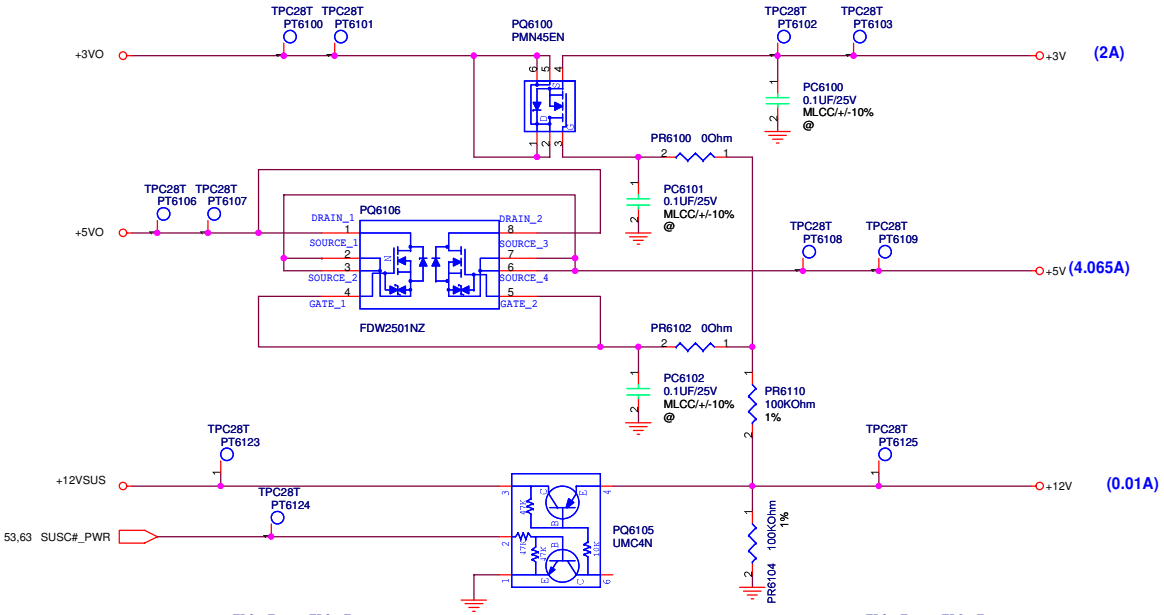


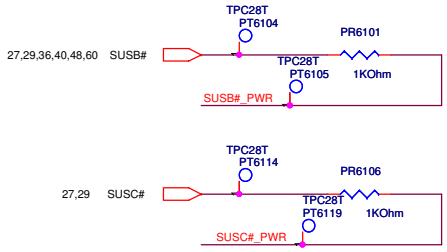
POWER GOOD DETECTER

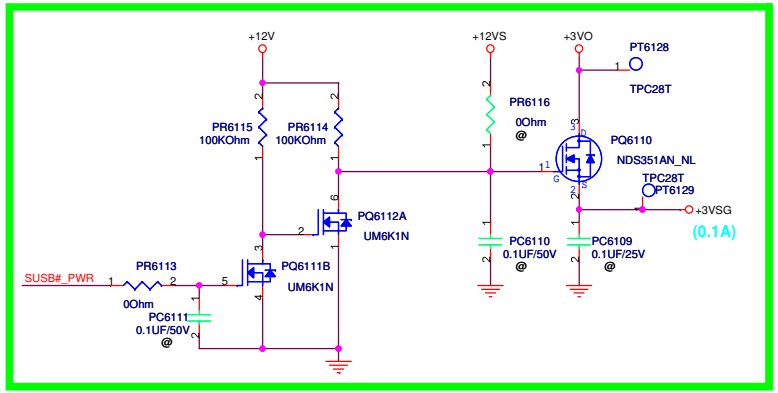


ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 60 of 64	

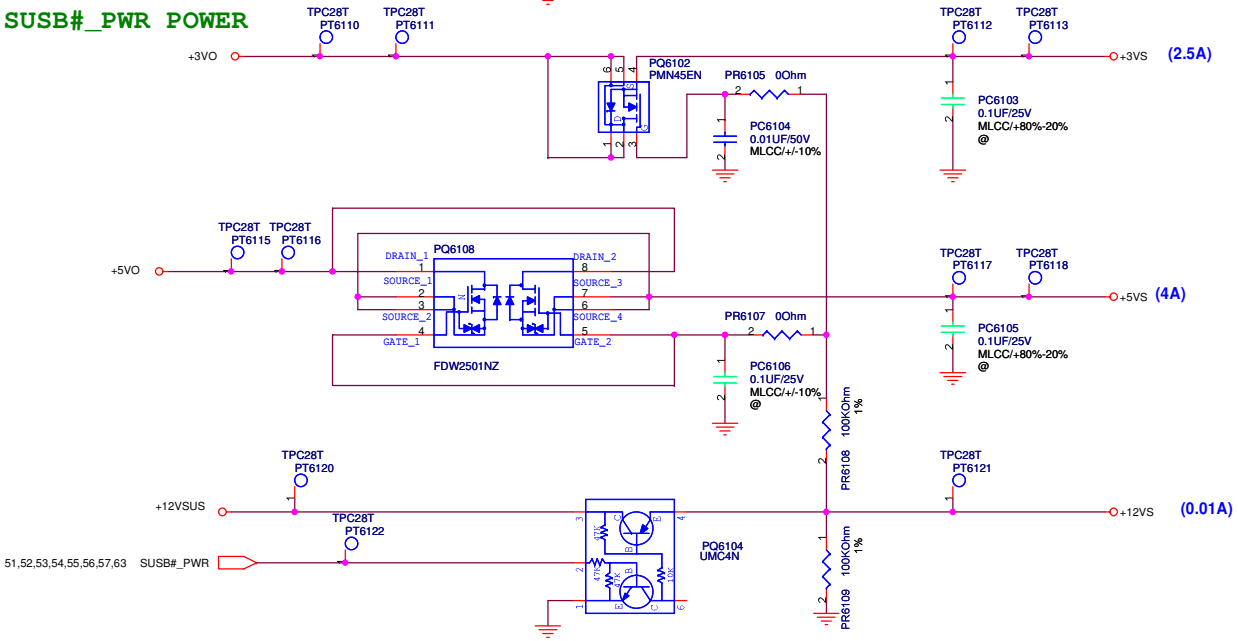
SUSC#_PWR POWER

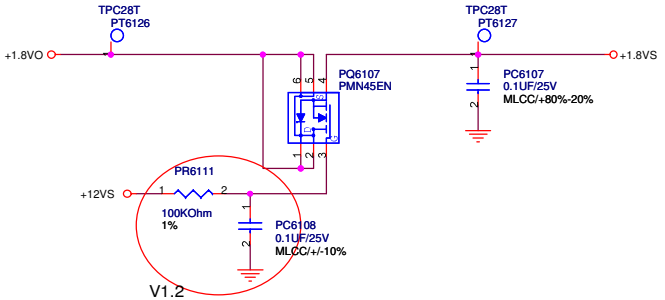






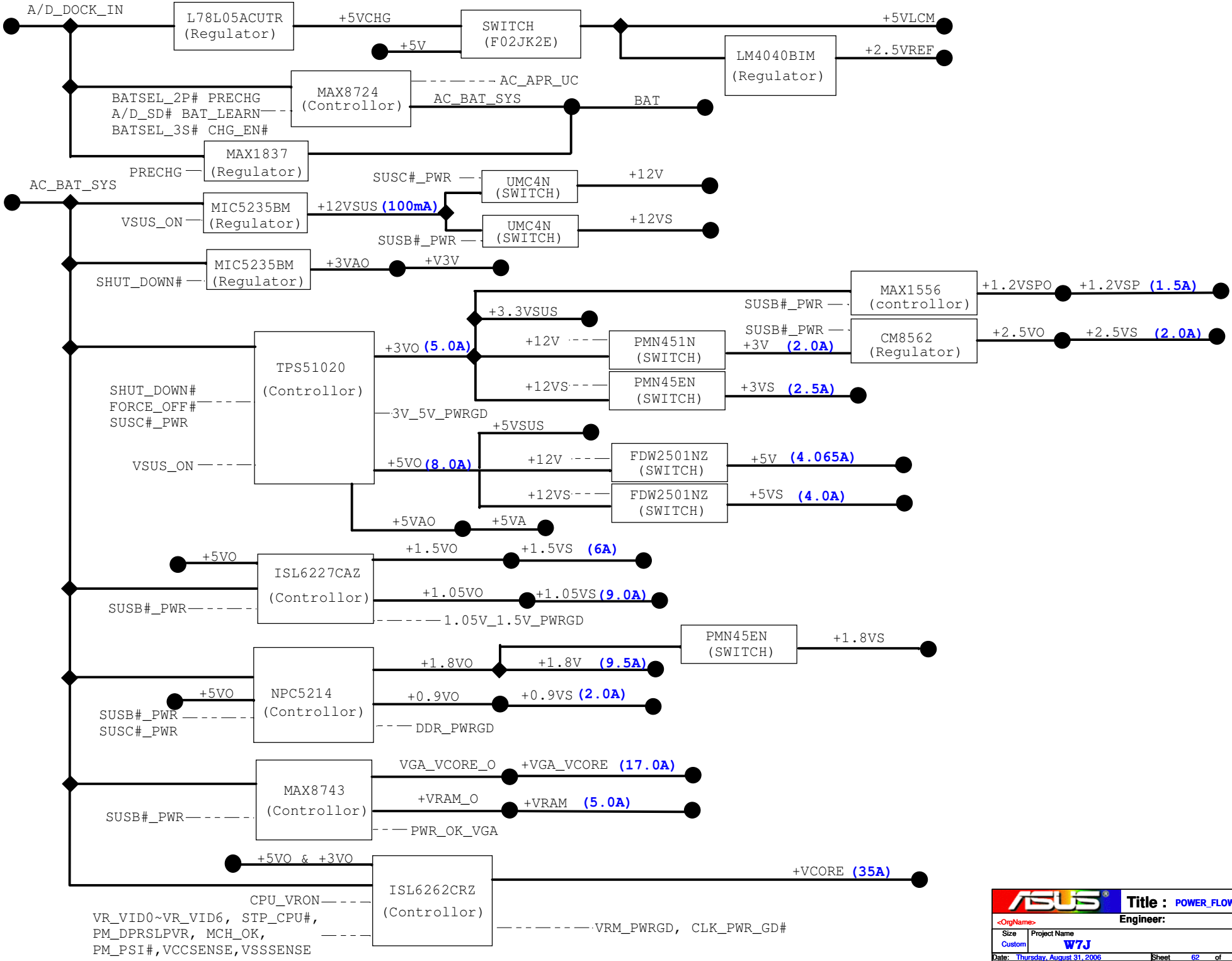
SUSB#_PWR POWER





V1.2

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 61 of 64	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 62 of 64	

AC_BAT_SYS → AC_BAT_SYS 23,50,51,52,53,54,55,57

+3VA → +3VA 25,29,47,54

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3VSUS → +3VSUS 26,27,28,29,32,38,41,51

+5VSUS → +5VSUS 28,51,60

+3V → +3V 26,29,39,40,41,44,48,54,61

+3VS → +3VS 5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,48,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 27,32,33,61

+12VS → +12VS 5,24,34,46,61

+5V → +5V 16,30,32,37,44,45,46,47,48,59,61

+5VS → +5VS 5,24,28,29,30,32,33,42,43,44,46,47,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 10,20,21,48,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,12,13,14,15,16,48,53

+1.8VS → +1.8VS 20,61

+VCCP → +VCCP 2,3,4,6,7,8,10,11,12,25,28,52

+0.9VS → +0.9VS 16,53

BAT → BAT 57

+5VCHG → +5VCHG 29,57,59

+5VLCM → +5VLCM 23,44,46,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,4,5,44,50

+VGA_VCORE → +VGA_VCORE 17,55

+VRAM → +VRAM 18,19,22,55

+1.2VSP → +1.2VSP 17,18,48,56

BAT_CON → BAT_CON 47,57

FOR POWER TEST

+3VA → PJP6300 (1 2 2) SGL_JUMP @ → CPU_VRON_PWR 50

+3VA → PJP6301 (1 2 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,55,56,57,61

+3VA → PJP6302 (1 2 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 53,61

+3VA → PJP6303 (1 2 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 63 of 64	

Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/29	1. Change Project name from W6J/H to W7J/F 2. Add NET: PWRLMT# to CPU pin: PROCHOT# (Page 2) 3. Add NET: DREFCLKSS,DREFCLKSS# to CLK GEN: pin17,pin18 (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# to GMCH: C40,D41 (Page 8) 5. Pull high GMCH VCCA_LVDC to +2.5VS (Page 10) 6. Add Jumper at G72M pin: B4 (Page 20) 7. Change R6811 from 200Kohm to 100Kohm (Page 23) 8. Change U57,U58 from 74LVC1G32GV to NC7SZ08M5 (Page 24) 9. Change D2 from EC31QS04 to RB751V_40 (Page 24) 10. Add Double-pi filter in VGA port (Page 24) 11. Swap ICH PCIE lans (Page 26) 12. Change GPIO7 NET from WB_AP to MUTE_POP_ICHGPIO# (Page 27) 13. Add NET: PWR_LED_1HZ to ICH: GPIO13 (Page 27) 14. Add Q6197 in net: PCIE_WAKE# (Page 27) 15. Add Q6192 in net: PWR_SW#_Q (Page 29) 16. Change R719 from 100Kohm to 1Mohm (Page 29) 17. Change R306 from 1Mohm to 10Mohm (Page 29) 18. Change C388 from 0.33uF to 1uF (Page 29) 19. Change Pull-high LID_EC# from +3VSUS to +3V (Page 29) 20. Change Audio CODEC from ADI1986 to ALC660 (Page 30) 21. Change R6614 from 0ohm to 4.7Kohm (Page 32) 22. Change R6616 from 10Kohm to 51KOhm (Page 32) 23. Change R6613 from 0ohm to 4.7Kohm (Page 32) 24. Change R6615 from 10Kohm to 51KOhm (Page 32) 25. Add NET: MUTE_POP_ICHGPIO# to MUTE_POP# circuit (Page 32) 26. Add Q6193 in net: SUSCLK (Page 34) 27. Change SLB9635TT pin16 from PLT_RST# to BUF_PLT_RST# (Page 34) 28. Delete NET PME# (Page 36) 29. Change Pull-high MDIO04 from +3V to +3VS (Page 37) 30. Change Pull-high XD_PWR_EN from +3V to +3VS (Page 37) 31. Change PCIE lans from port 1 to port 2 (Page 38) 32. Add C6625,C6626 in phone connector (Page 39) 33. Change PCIE lans from port 3 to port 1 (Page 40) 34. Add NET: EXPD# to R5538 pin20 (Page 40) 35. Add NET: C_PRESENT# to R5538 pin9,pin10 (Page 40) 36. Change PCIE lans from port 2 to port 3 (Page 41) 37. Change Pull-high 802WLAN_ON# from +3V to +3VSUS (Page 41) 38. Change FWH packaging from PLCC to TSOP (Page 43) 39. Add NET: EXPD# to M38857 P53 (Page 44) 40. Add NET: WB_AP to M38857 P67 (Page 44) 41. Add NET: C_PRESENT# to M38857 P62 (Page 44) 42. Add NET: ACZ_RST#_AUD to M38857 P61 (Page 44) 43. Change U10,U6012 pin4 from SUSC# to SUSC (Page 45) 44. Add Q6196 in net: BTPWRCL# (Page 45) 45. Add R6922 between net: WIRELESS_LAN_ON/OFF# and WB_AP (Page 47) 46. Add Q6198 in +3VS discharge (Page 48) 47. Change Power LED ON circuit (Page 48)

Rev	Date	Description
R1.2	2005/12/20	1. Change R6491 from 23.2KOhm to 51KOhm (Page 5) 2. Add Q6200 at U42 :D2+,D2- (Page 5) 3. Add NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 4. Add RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 5. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 6. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 7. Change R1001 from 1Kohm to C6631:0.1uF (Page 16) 8. Modify LCD enable circuit by U6059 (Page 23) 9. Change L89,L90,L92 to Bead 120Ohm/100MHz (Page 24) 10. Change Q60,Q61 from SI1906DL to SI1902DL (Page 24) 11. Add C6632 in Y1 (Page 25) 12. Connect H_DPRSTP# to PU5000 (Page 25) 13. Change U69 from SN74LVC1G32G to 74LVC1G32GV (Page 26) 14. Disonnect STP_CPU# to PU5000 (Page 27) 15. Add GPIO9:W_OLED# (Page 27) 16. Change R523 from 10KOhm to 100KOhm (Page 29) 17. Change R303 from 10KOhm to C6630:1uF (Page 29) 18. Add R6936 in Net:PWR_SW#_Q (Page 29) 19. Add R6633,R6634,R6635,R6636 in CN20(Page 31) 20. Add R6938 in +3.3Vaux (Page 41) 21. Change CE41,CE5705,CE25 from 100uF to 150uF (Page 45) 22. Add R6937 in BTPWRCL# (Page 45) 23. Change Q6180,Q6181 by Q6202 (Page 46) 24. Add Q6201,LED10 in WIRELESS_OLED# (Page 46) 25. Change R6686 from 0Ohm to 470Ohm (Page 47) 26. Add R6940 in Power Board +5Vs (Page 47)
R2.0	2006/2/23	1. Change R6491 from 51KOhm to 36.5KOhm (Page 5) 2. Del NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 3. Del RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 5. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 6. Add R6945 at U6028: H22 (Page 18) 7. Add R6944 in MUTE_POP# (Page 32) 8. Change L5708 to R6943 (Page 38) 9. Del R6915,R6916,R6917 in CON15 (Page 40) 10. Change R613 from 10K ohm to 0 ohm(Page 42) 11. Change CON11 from 8 pin to 6 pin (Page 45) 12. Add R6946,R6947 at BATT_GND (Page 47) 13. Add D6040 at CN14 (Page 47)

<Variant Name>

Title : History

ASUSTek Computer INC. NB1

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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