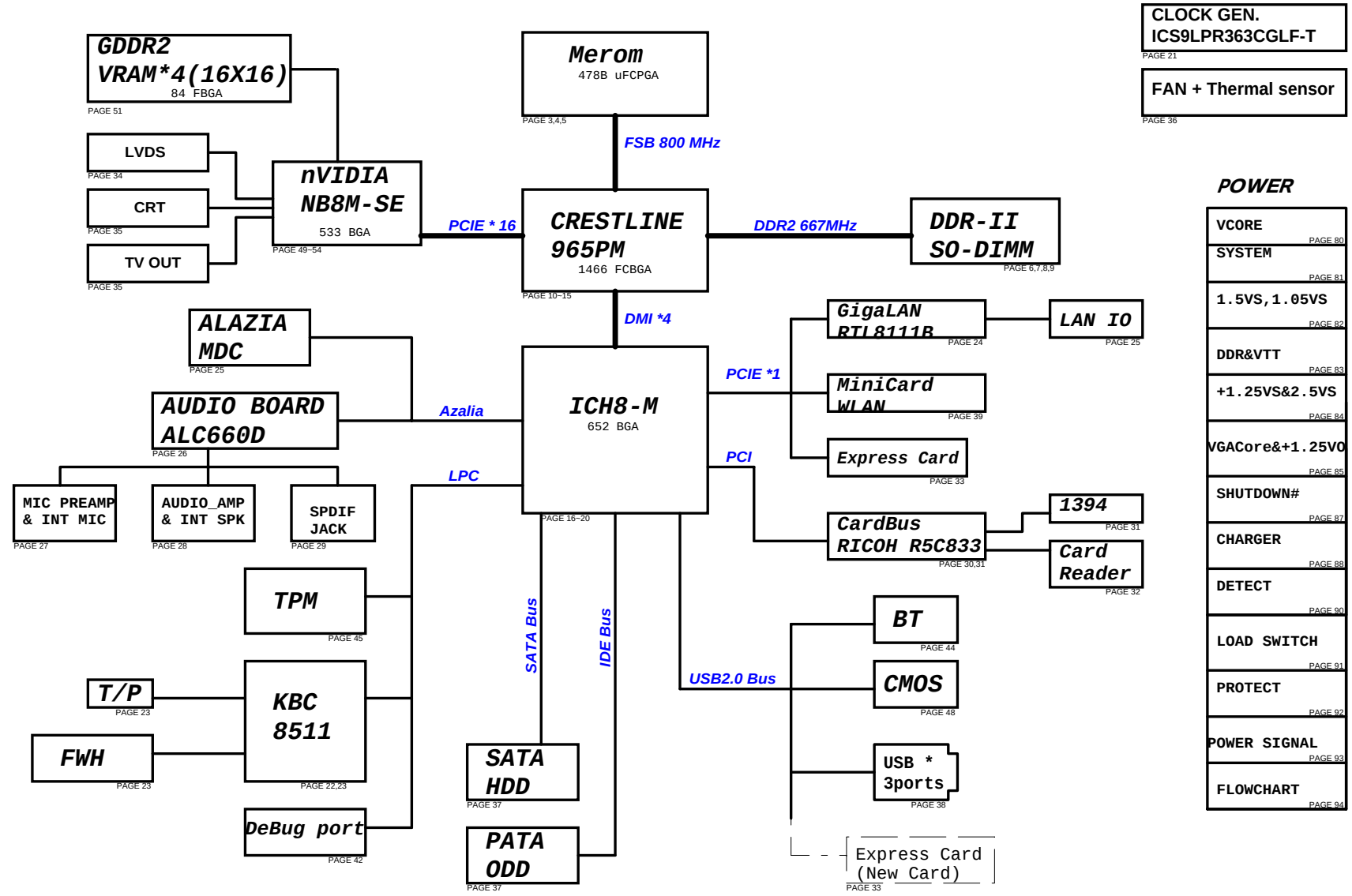
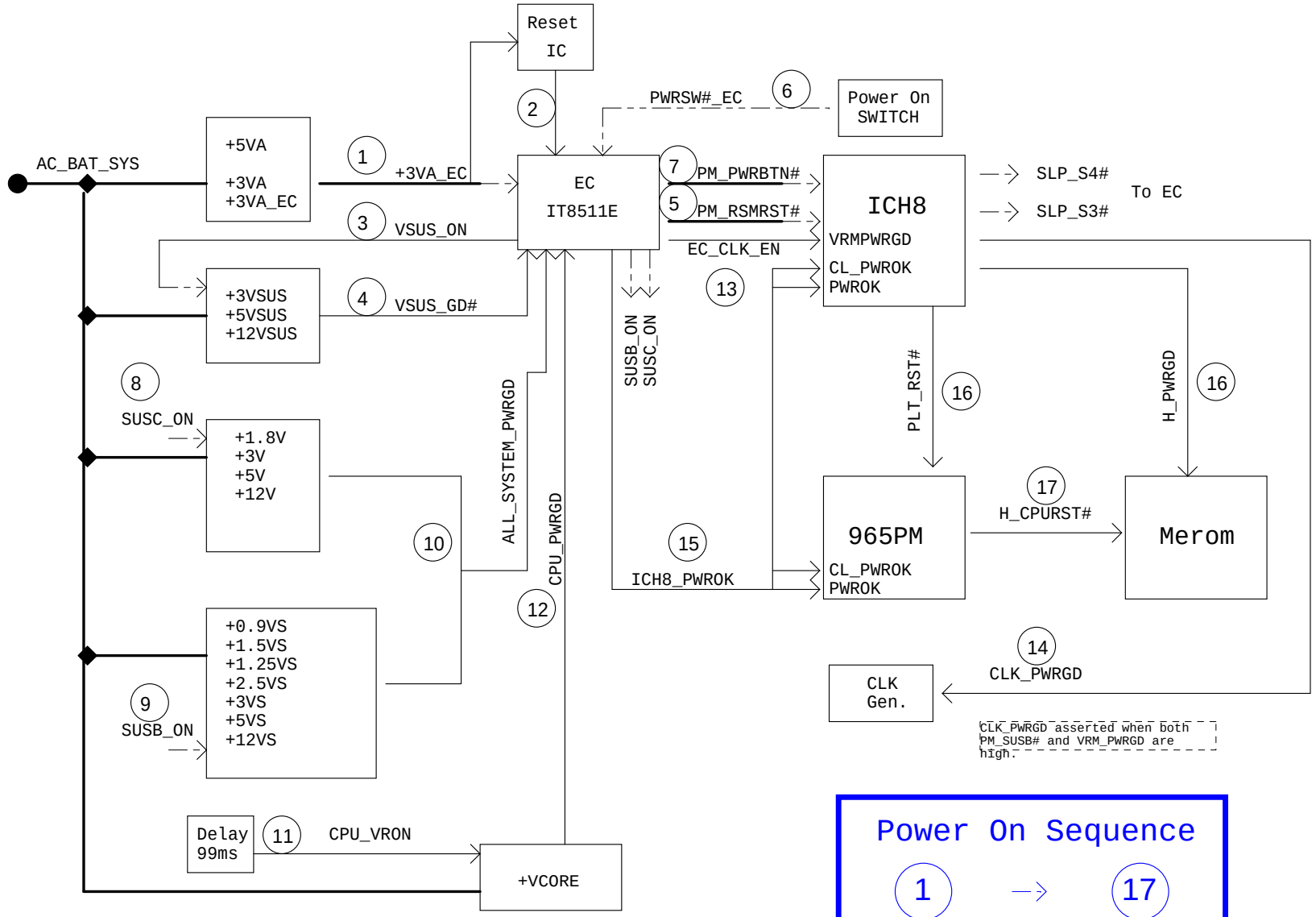
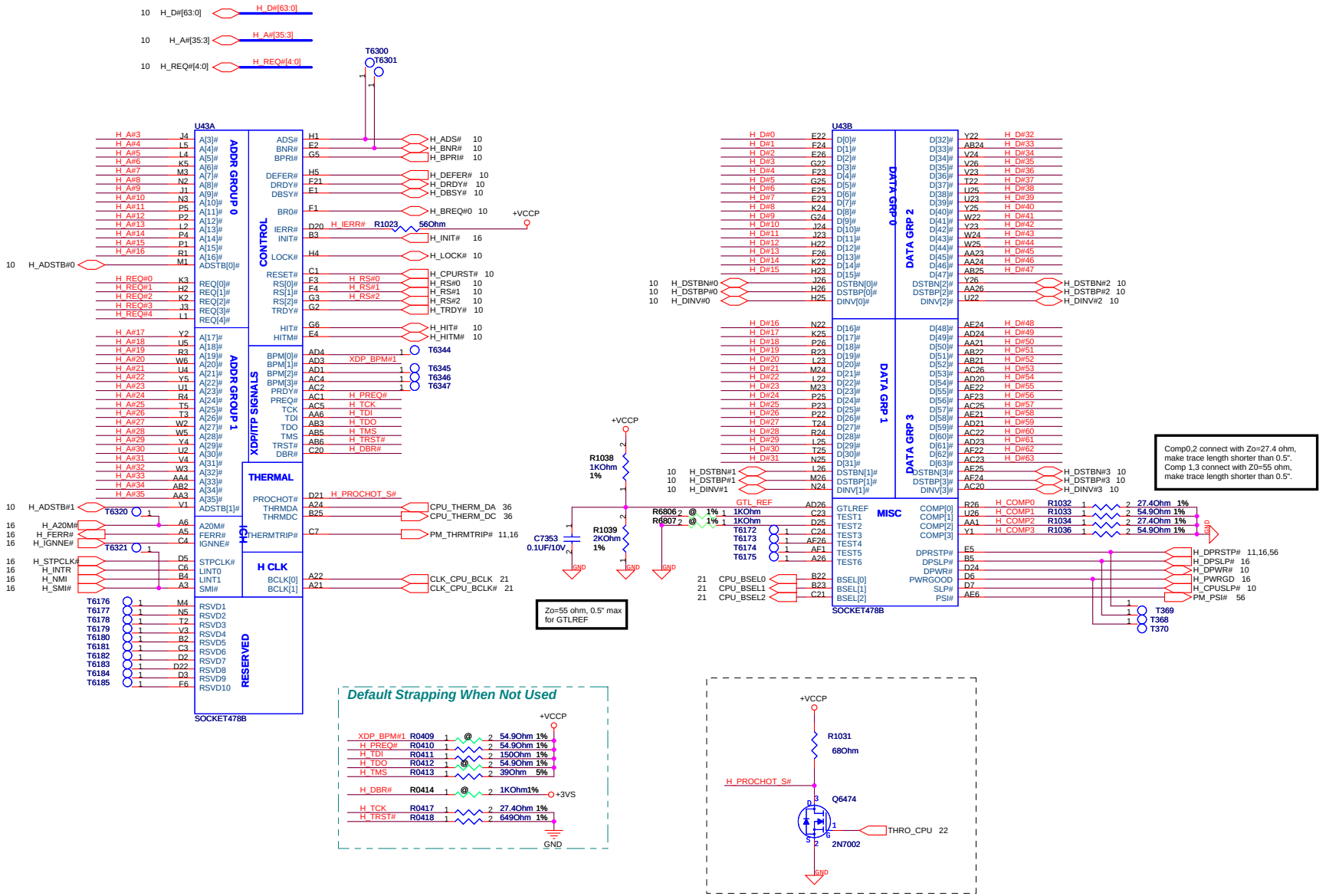
T76S: MEROM/965-PM/ICH8-M/NB8M-SE BLOCK DIAGRAM



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 1 of 70	



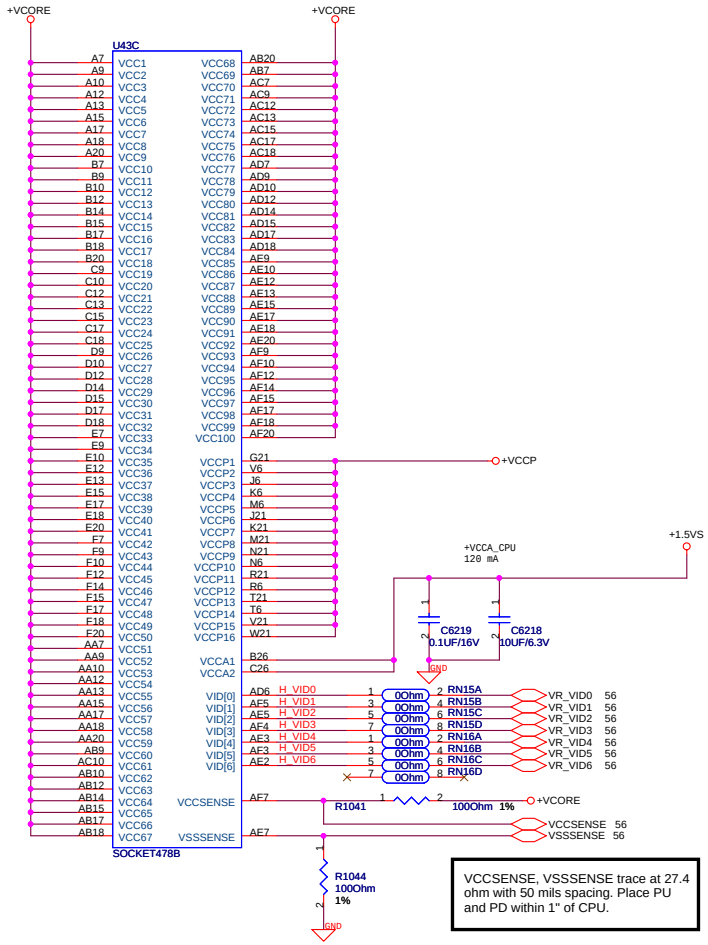
ASUSTeK COMPUTER INC	Title : PowerOn sequence		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 2 of 70		



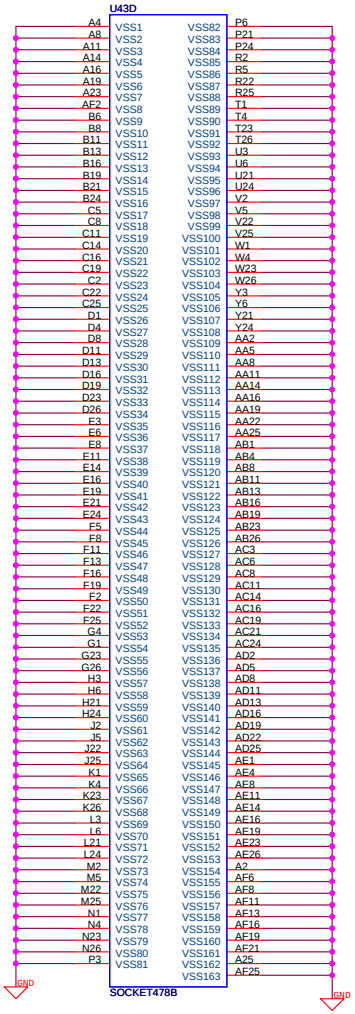
ASUSTeK COMPUTER INC	Title : MEROM CPU (1)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 3 of 70		

MEROM FSB800 Vcore		
	LFM	TYP	HFM
VCC	0.75V		1.325V
ICC	30.4A		41A

MEROM FSB800 Vcore			
	Min	Typ	Max
VCCP	1.0V	1.05V	1.1V
	Min	Typ	Max
ICCP			2.5A

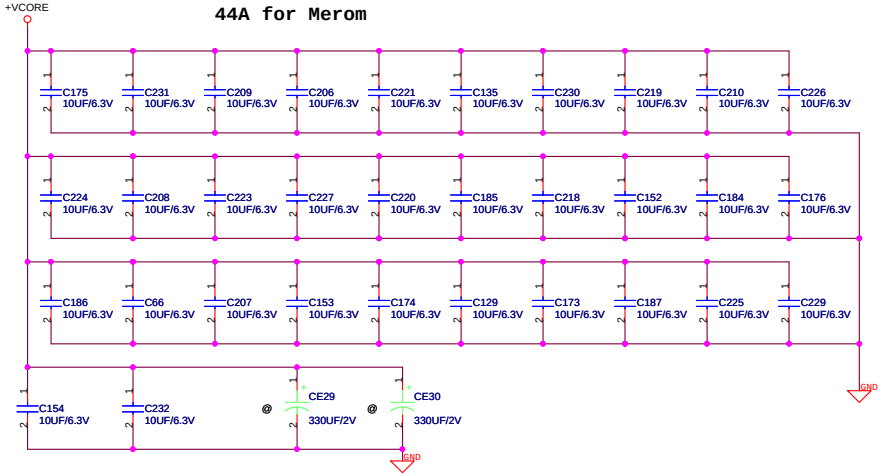


VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

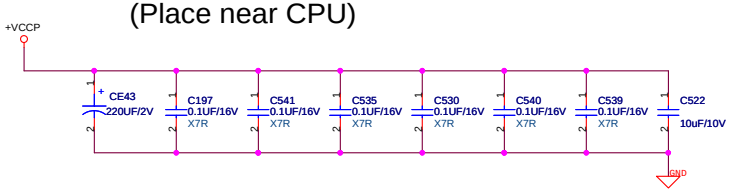


ASUSTeK COMPUTER INC	Title : MEROM CPU (2)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 4 of 70	

44A for Merom



+VCCP Decoupling Capacitor
(Place near CPU)



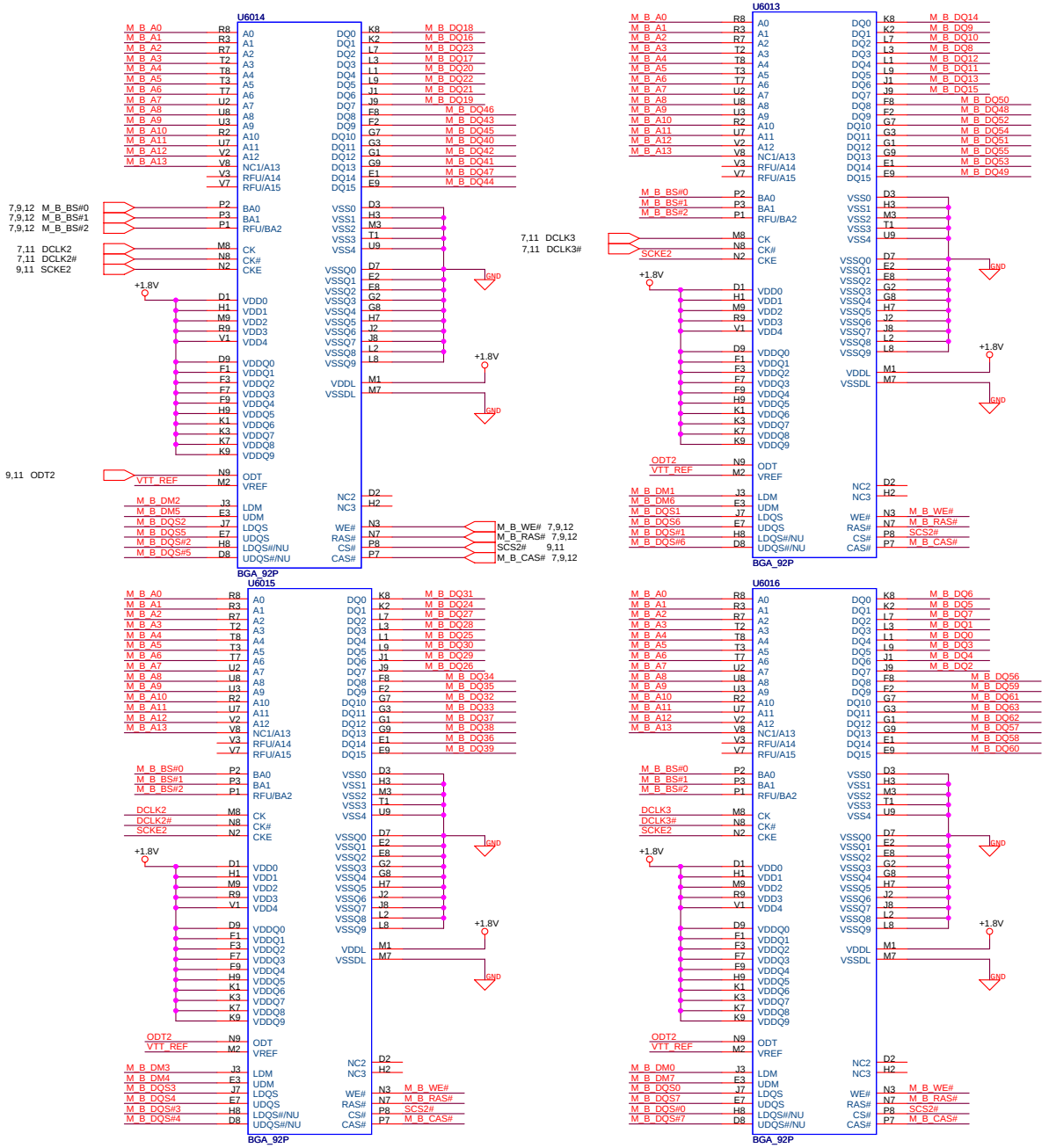
Decoupling guide from INTEL

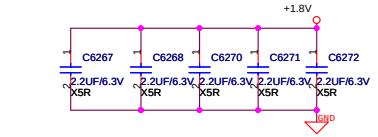
VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	270uF	* 1pcs for CPU

Decoupling for W7S

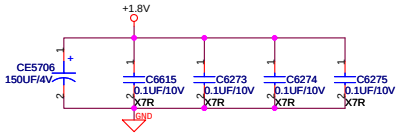
VCORE	10uF/6.3V	* 32pcs
	330uF/2V	* 2pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

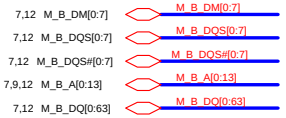
ASUS	Title : CPU CAP		
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 5 of 70		



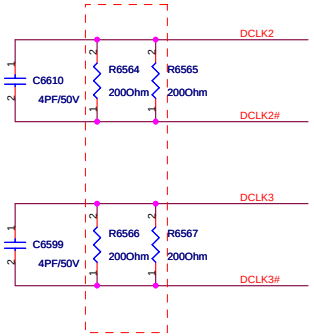


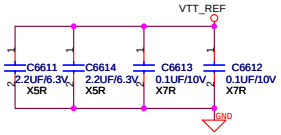
Layout Note: Place these Caps near Memory Module



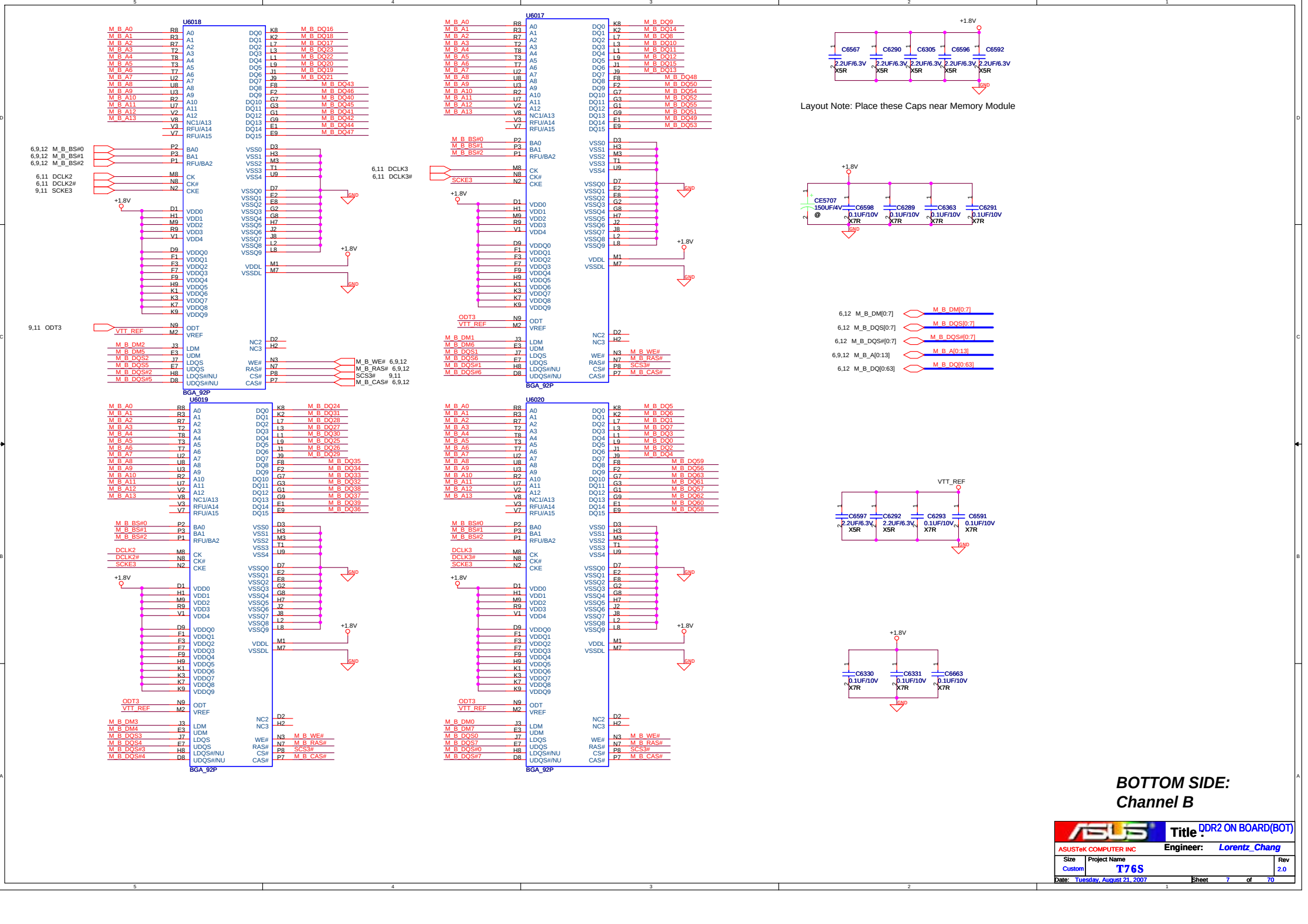


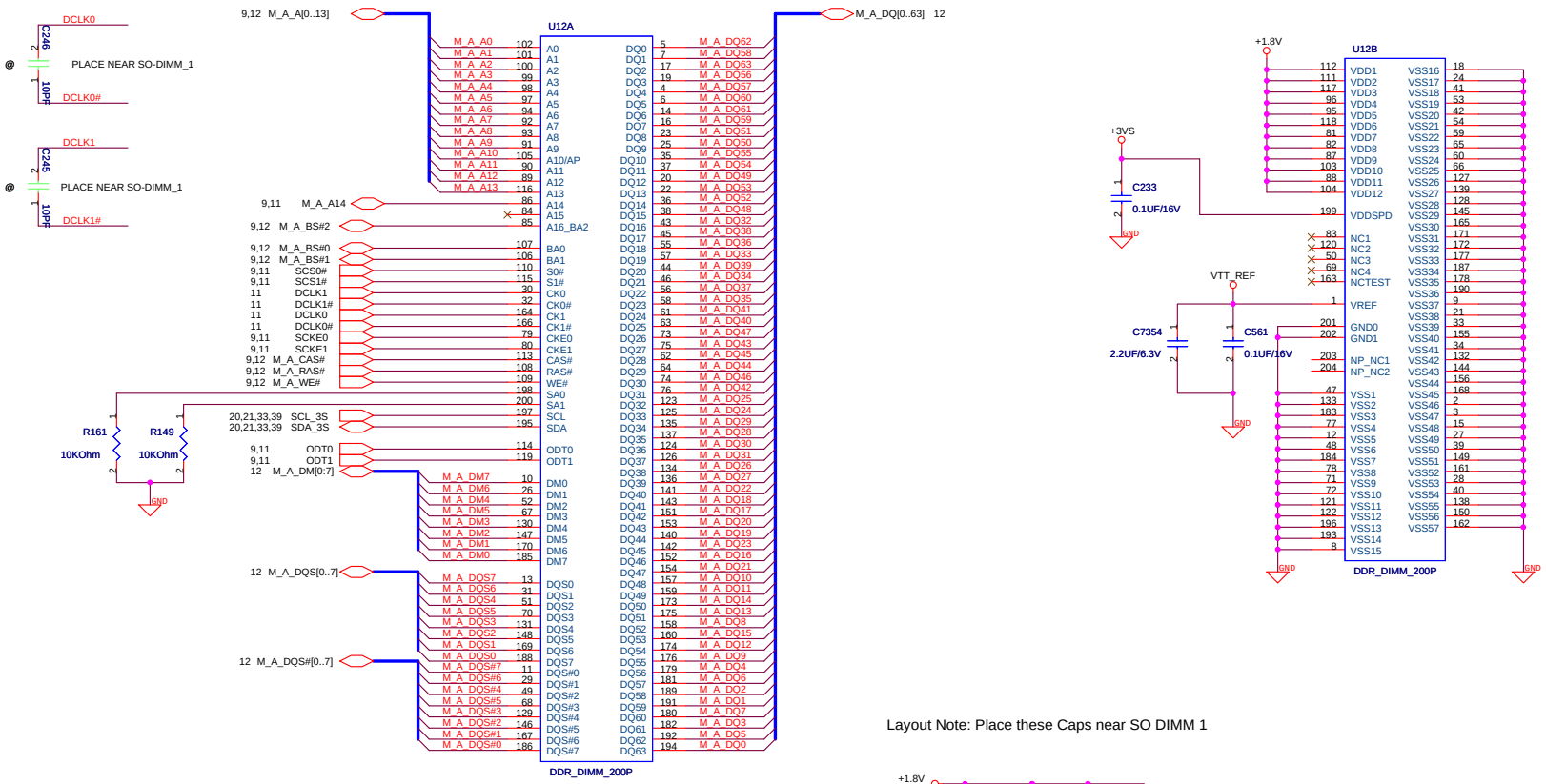
Place either terminator on each side



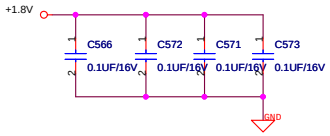


ASUSTeK COMPUTER INC	Title : DDR2 ON BOARD(TOP)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 6 of 70	

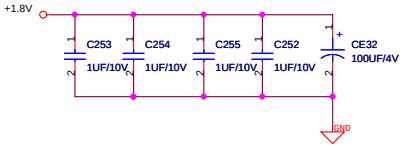

U6018
U6017
U6019
U6020
BGA_92P
+1.8V
GND
VTT_REF
C6567 C6290 C6305 C6596 C6592
2.2UF/6.3V X5R
Layout Note: Place these Caps near Memory Module
CE5707 150UF/4V @
C6598 C6289 C6363 C6291
0.1UF/10V X7R
6,12 M_B_DM[0:7]
6,12 M_B_DQS[0:7]
6,12 M_B_DQS#[0:7]
6,9,12 M_B_A[0:13]
6,12 M_B_DQ[0:63]
C6597 C6292 C6293 C6591
C6330 C6331 C6663
BOTTOM SIDE:
Channel B
Title : DDR2 ON BOARD(BOT)
ASUSTeK COMPUTER INC
Engineer: Lorentz_Chang
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 7 of 70



Layout Note: Place these Caps near SO DIMM 1

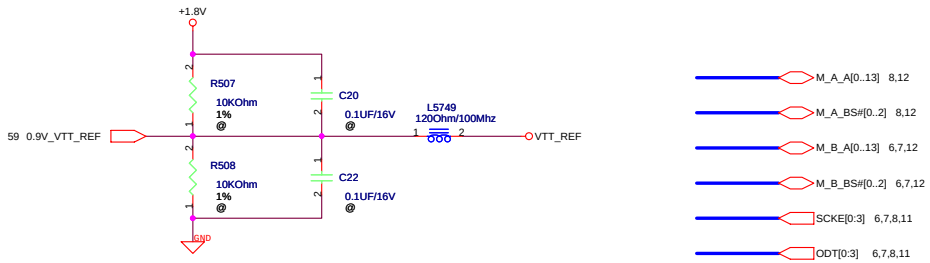


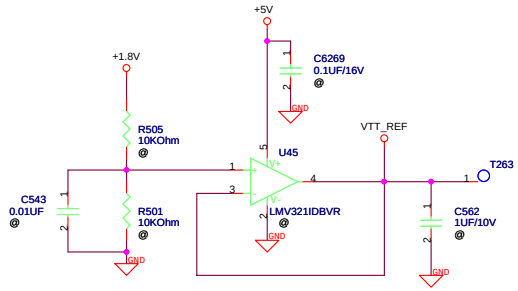
Layout Note: Place these Caps near SO DIMM 1

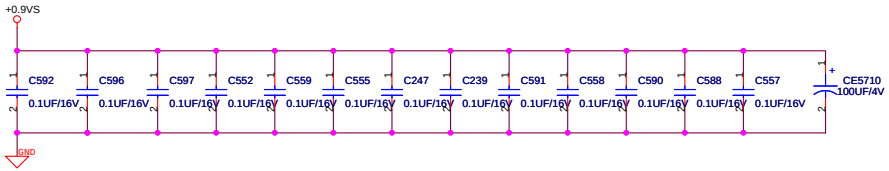


TOP SIDE:
Channel A

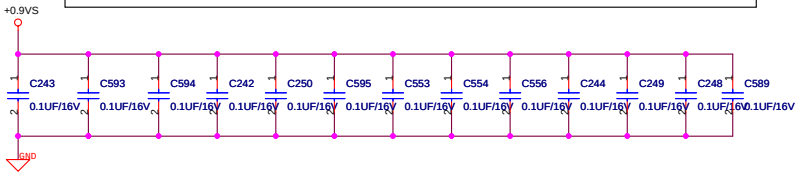
ASUSTeK COMPUTER INC	Title : DDR SO-DIMM		
	Engineer: *Lorentz_Chang*		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 8 of 70		

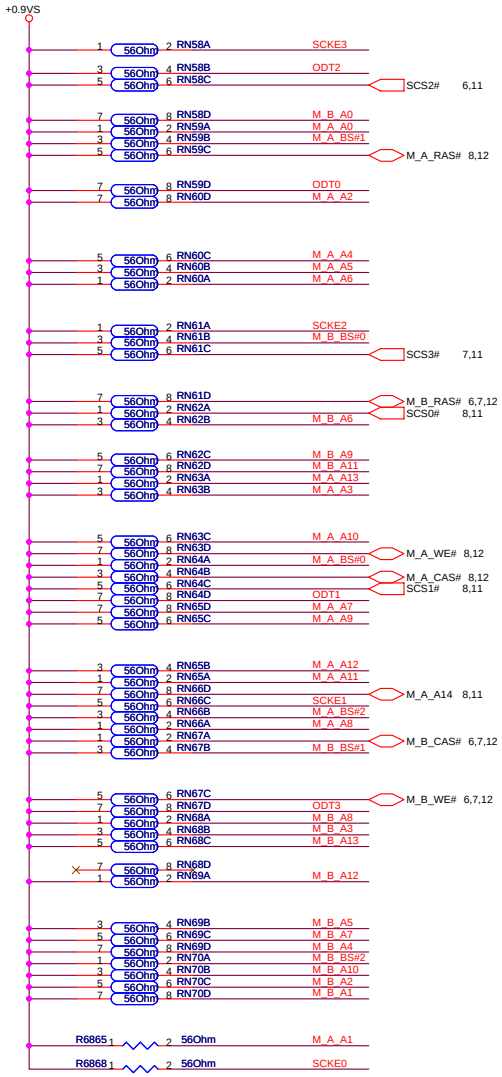




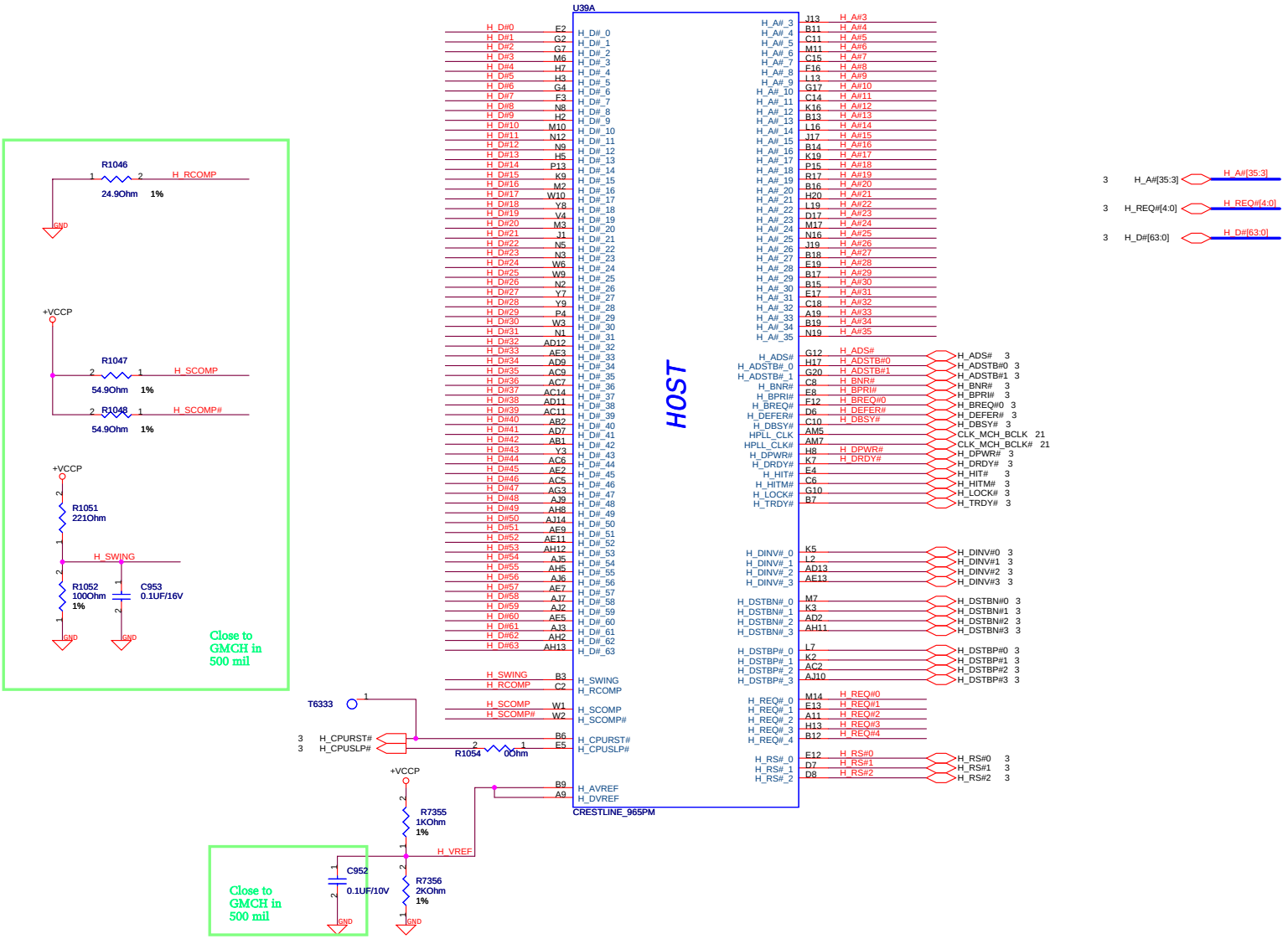


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

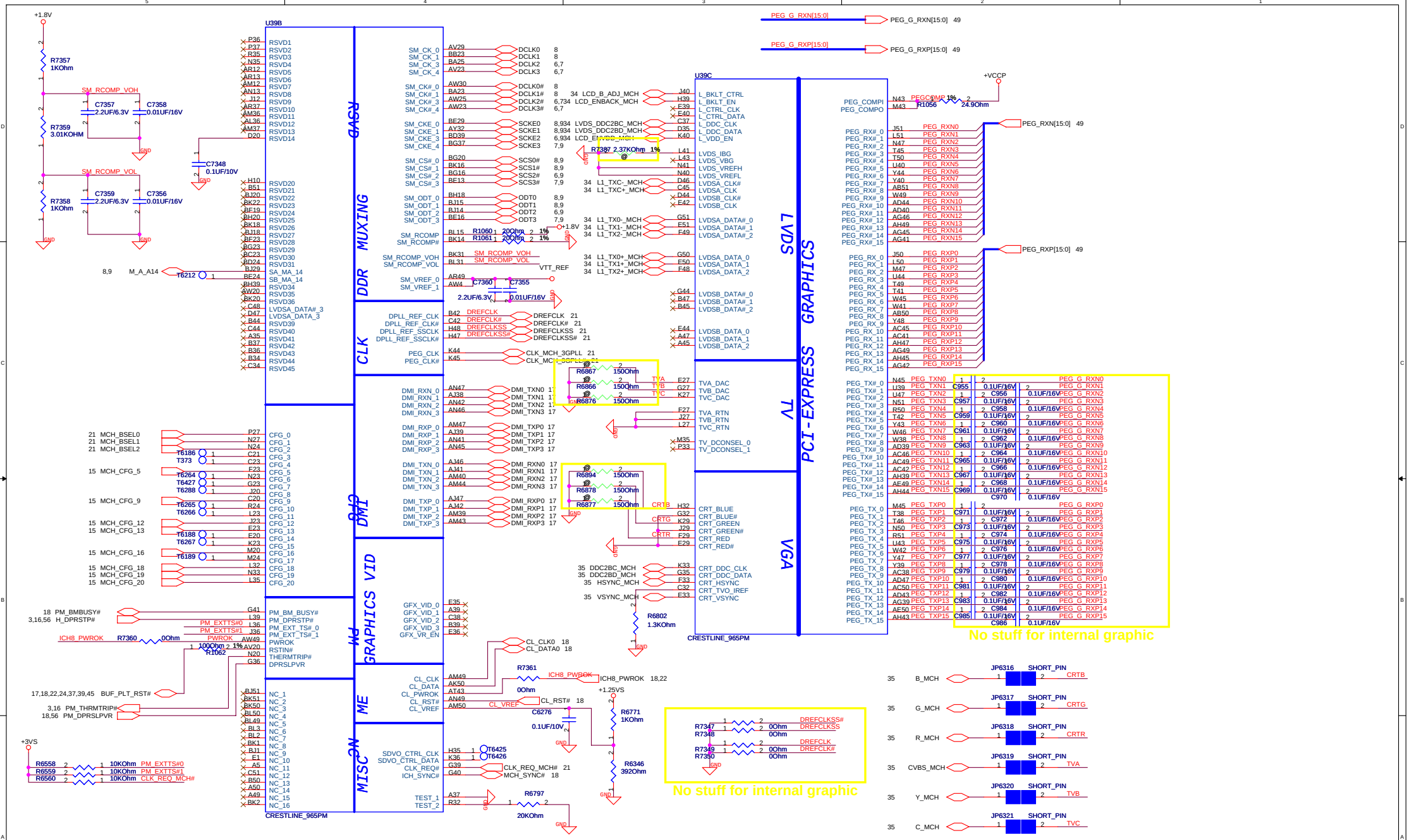




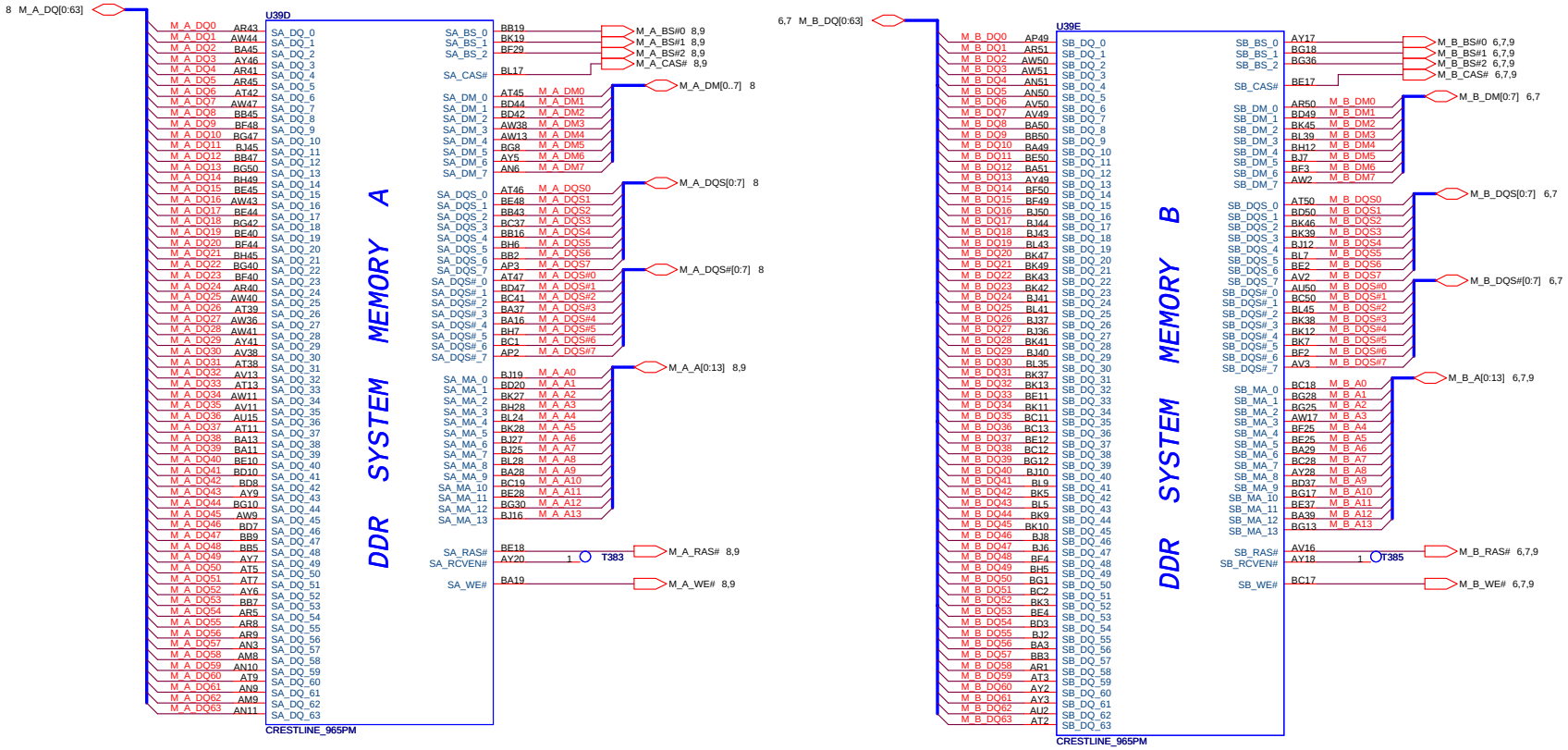
ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 9 of 70		



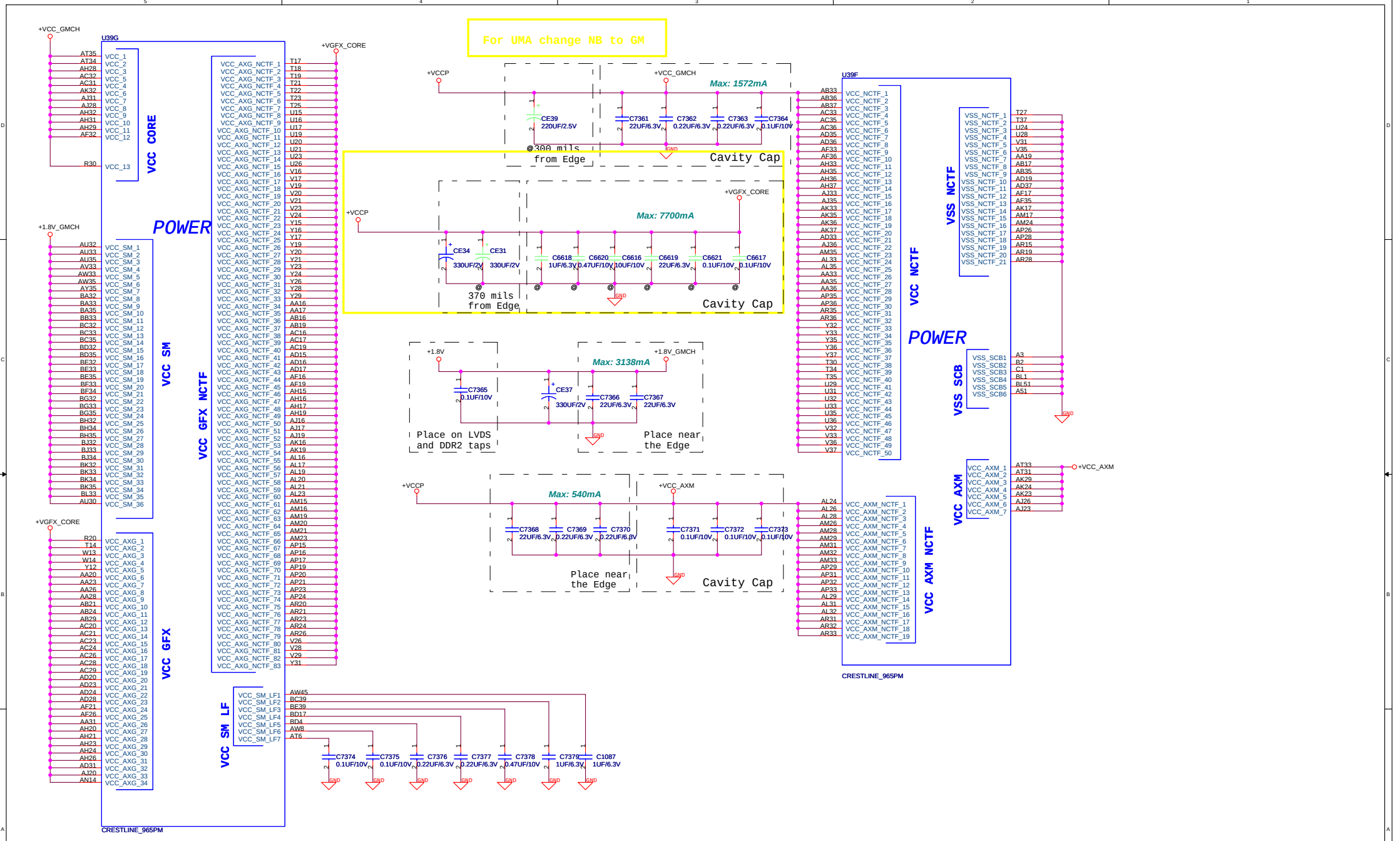
ASUSTeK COMPUTER INC	Title : 965PM -- CPU (1)
	Engineer: Lorentz_Chang
Size: Custom	Project Name: T76S
Rev: 2.0	
Date: Tuesday, August 21, 2007	Sheet 10 of 70



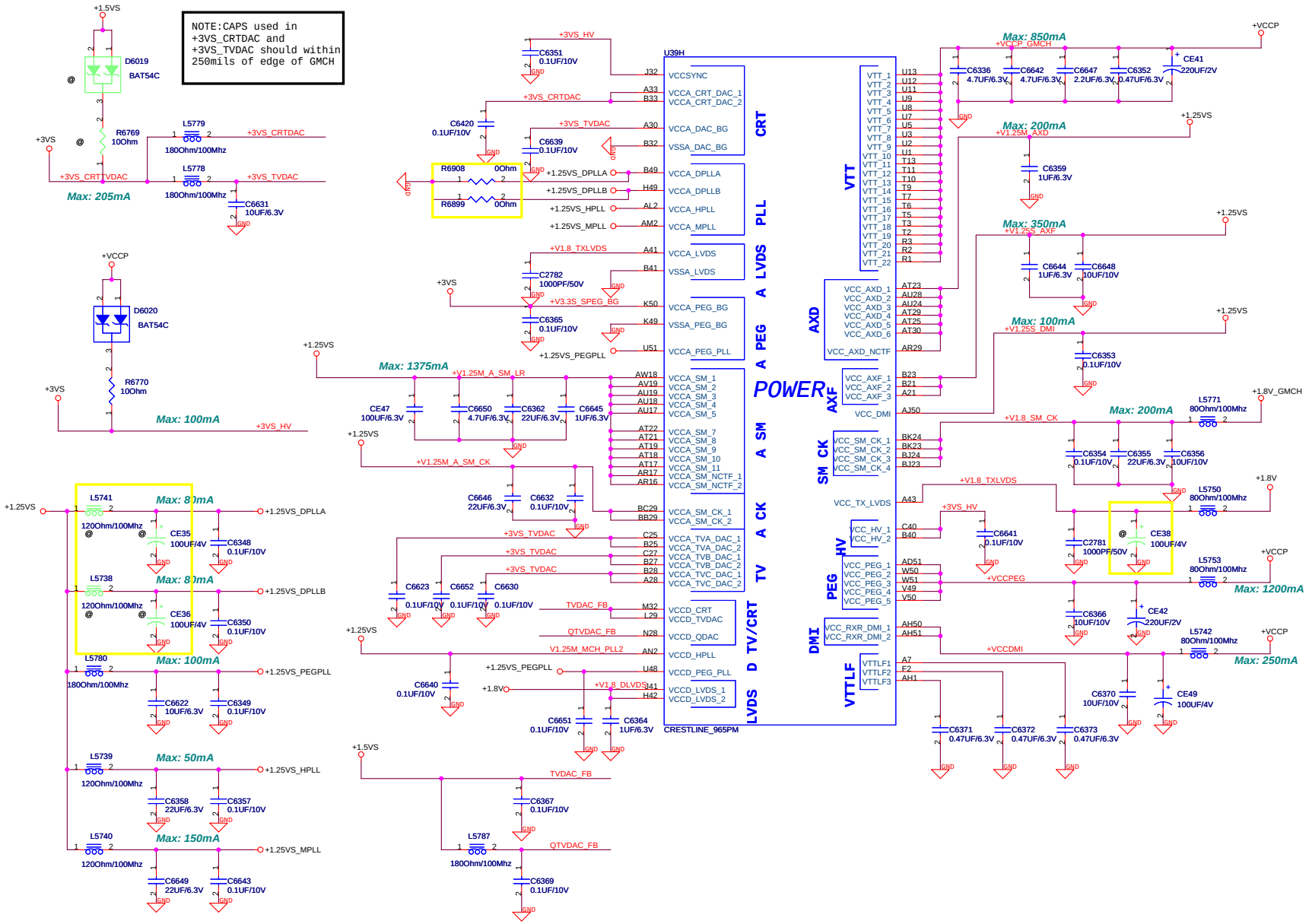
Title : 965PM-DDR2/PEG (2)		
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 11 of 70	



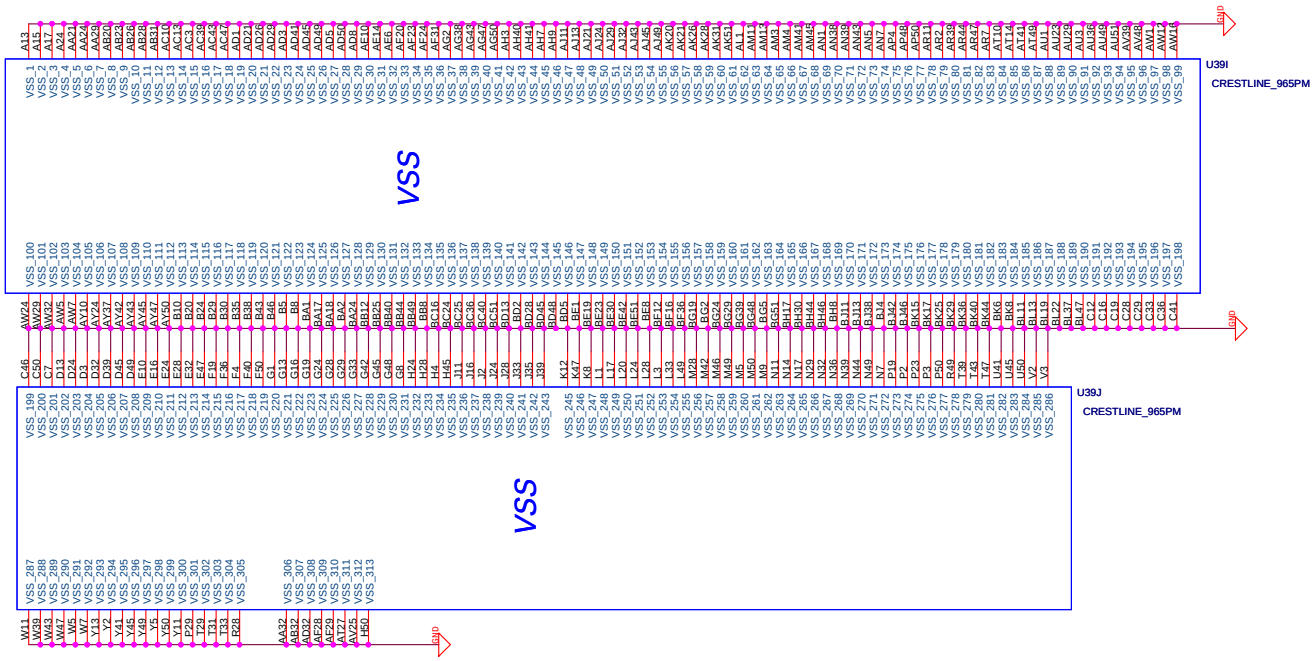
ASUSTeK COMPUTER INC	Title : 965PM-DDR2 bus (3)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 12 of 70		

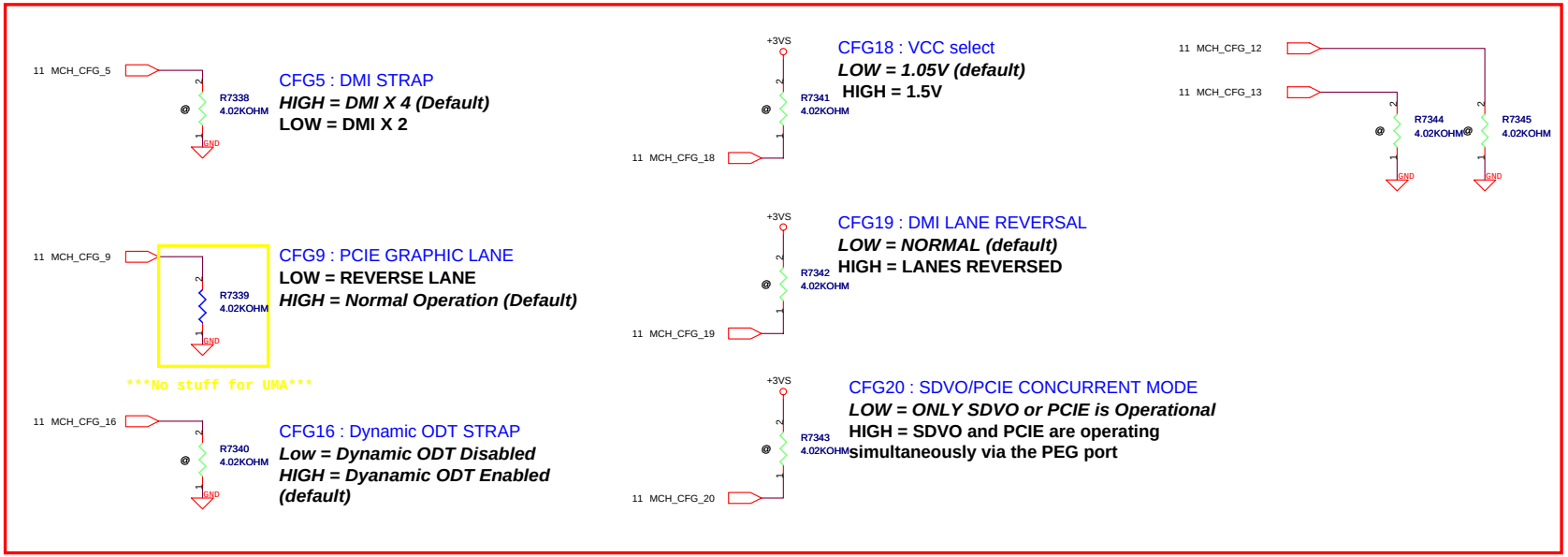


ASUSTeK COMPUTER INC	Title : 965PM--POWER (4)	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 13 of 70	

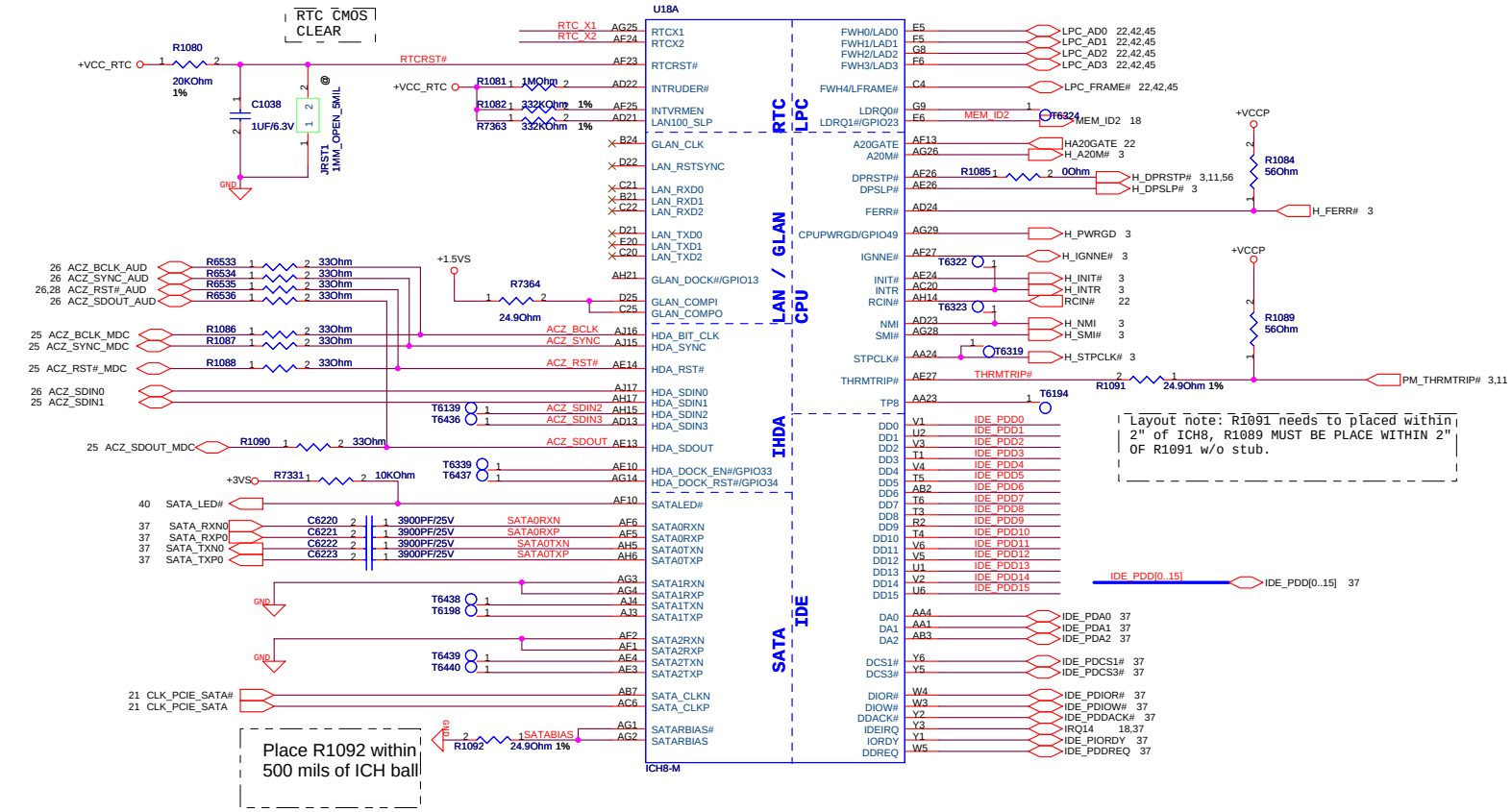


ASUSTeK COMPUTER INC	Title : 965PM-POWER (5)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 14 of 70		

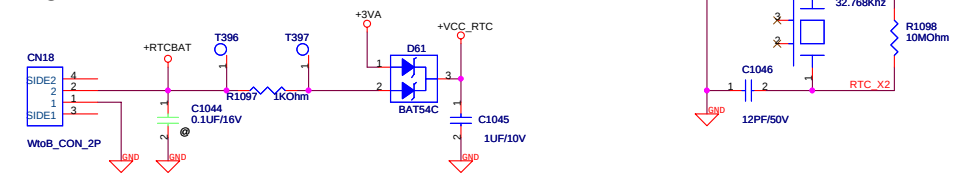




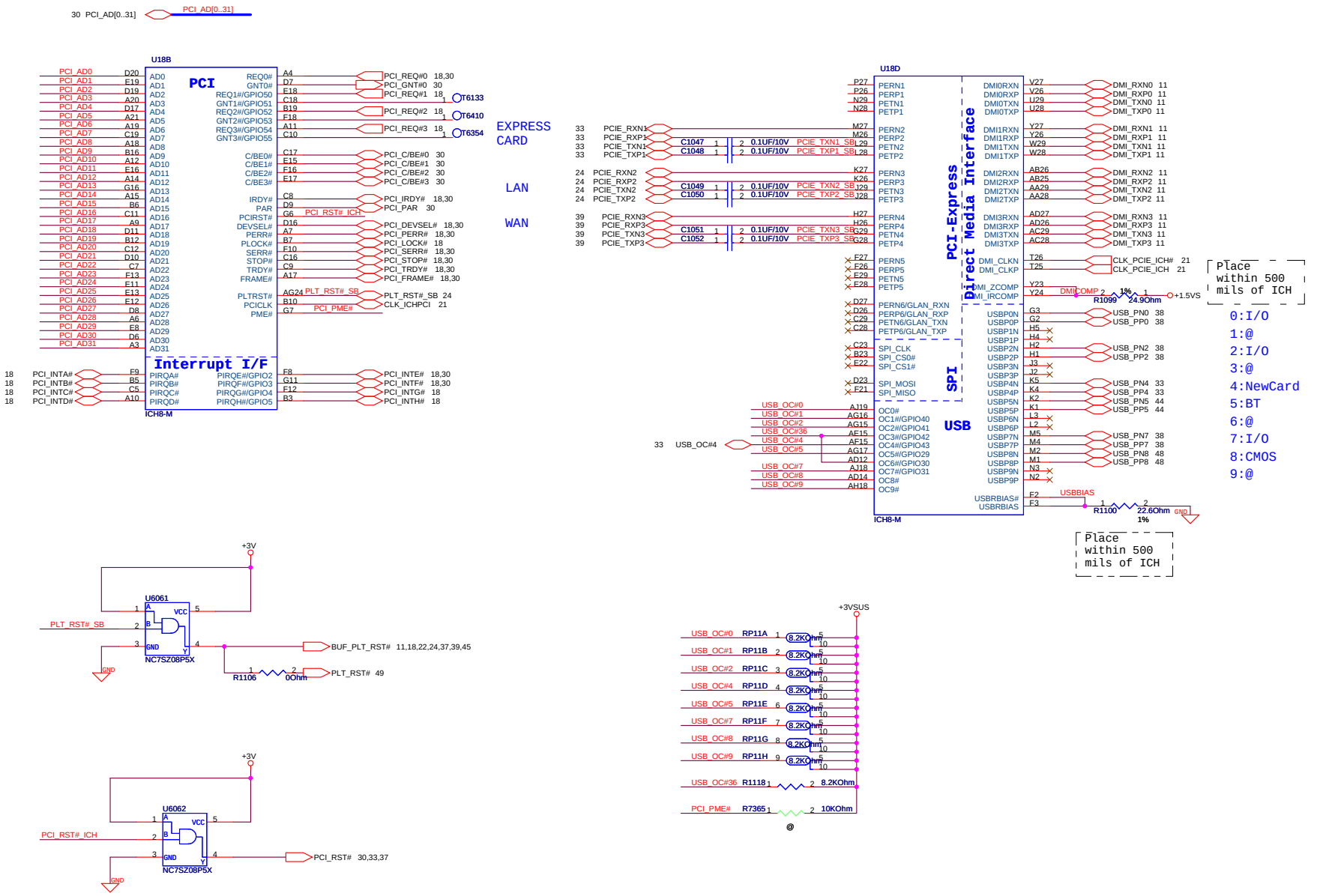
ASUSTeK COMPUTER INC	Title : GND/Strapping (6)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 15 of 70		



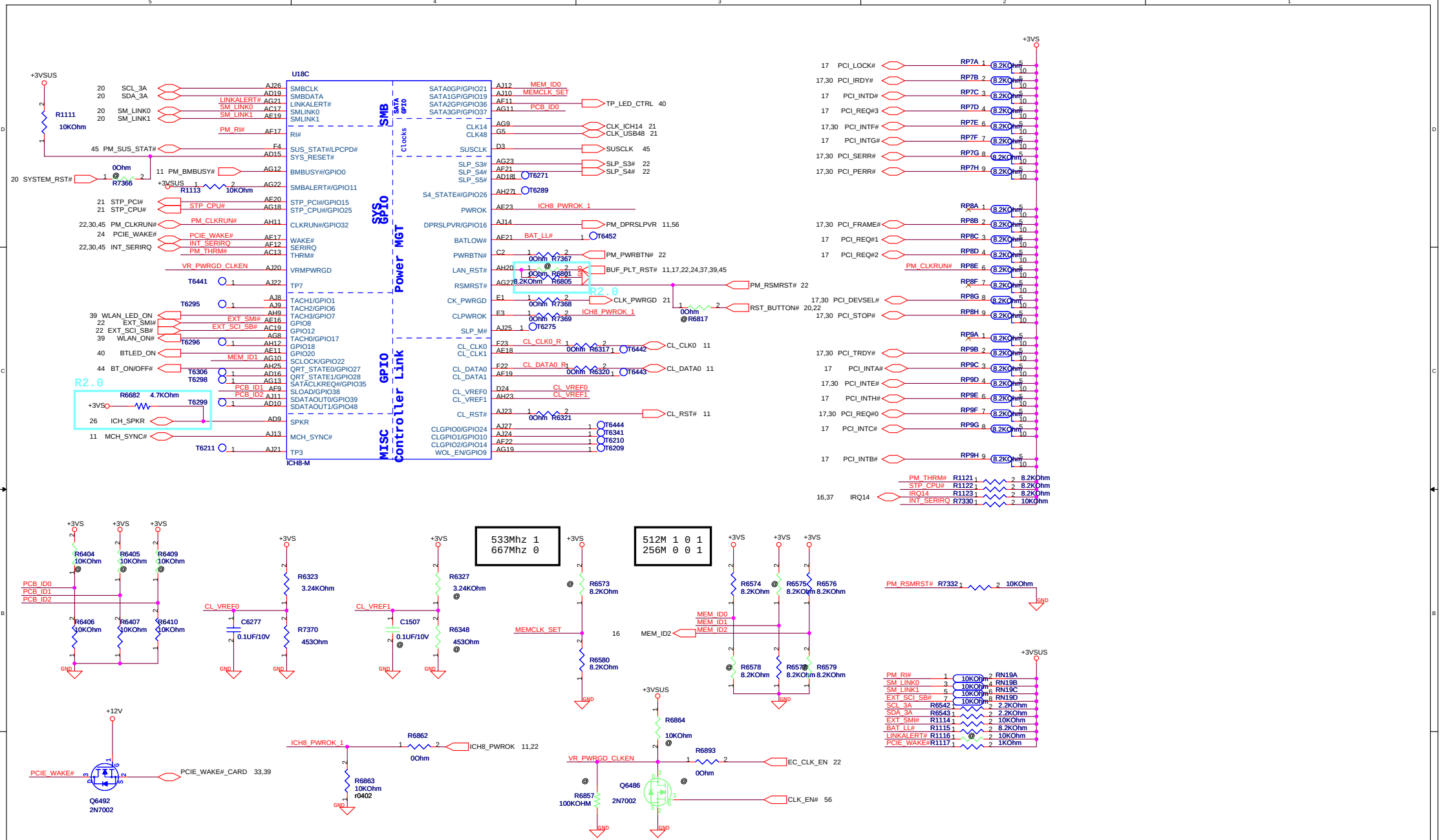
RTC BAT



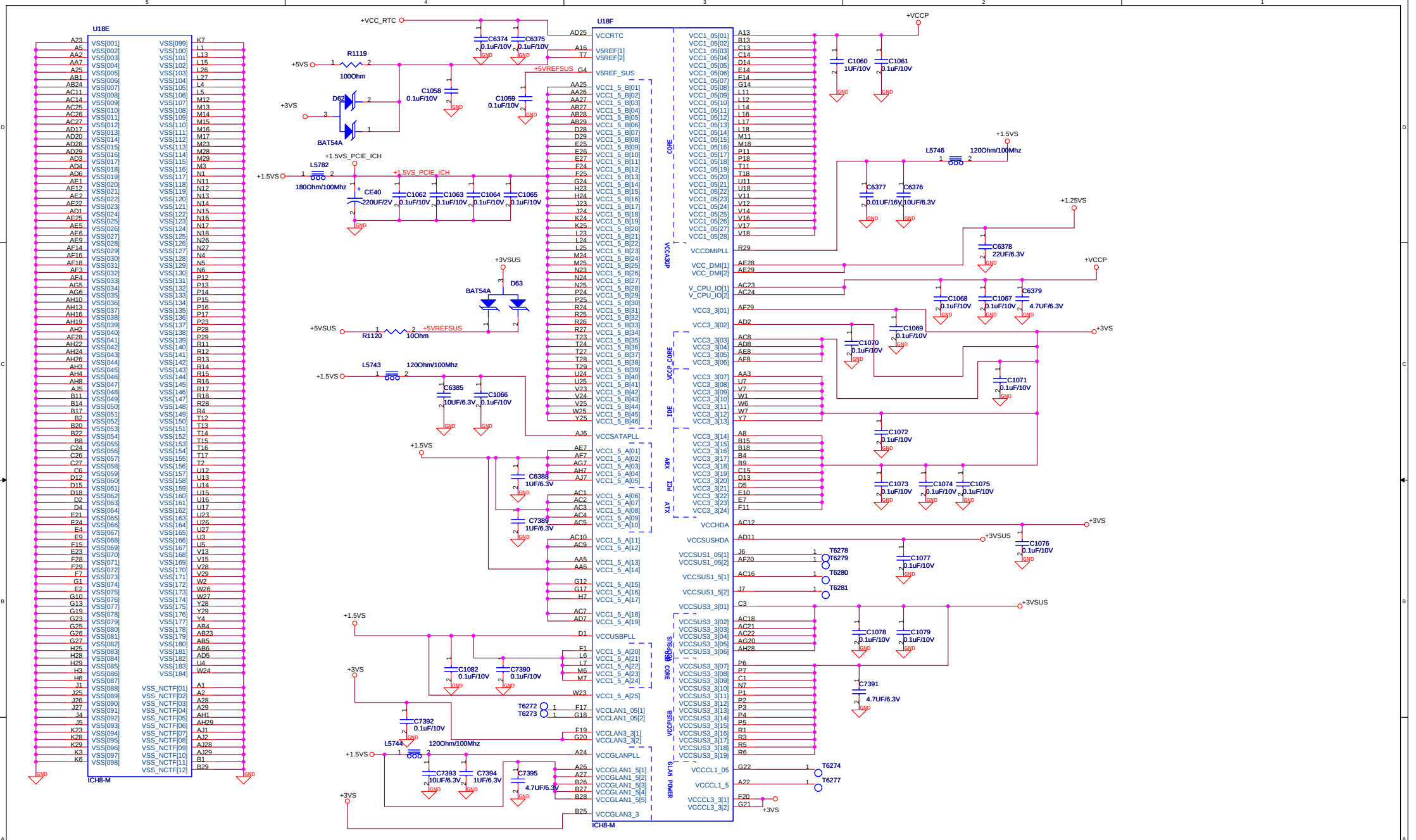
ASUSTeK COMPUTER INC	Title : ICH8-M (1)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 16 of 70		



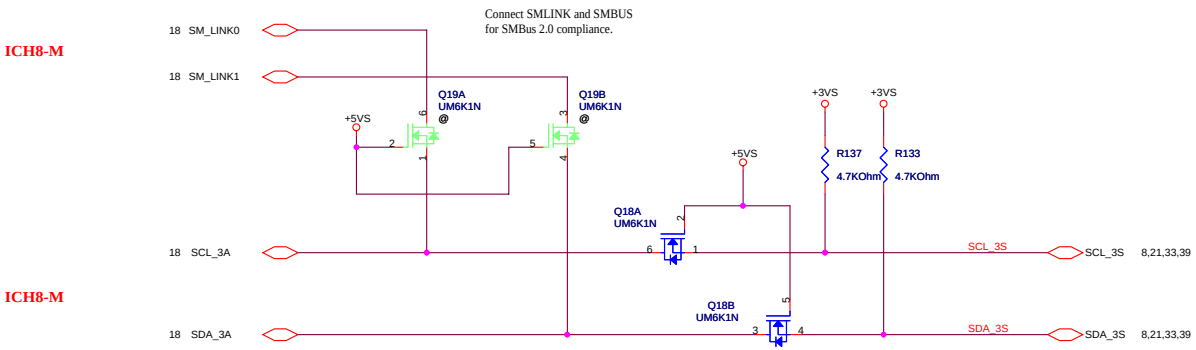
Title : ICH8-M (2)		
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 17 of 70	

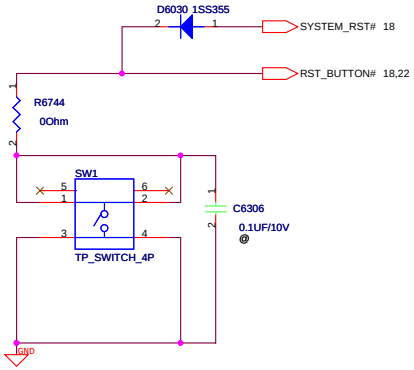


ASUSTeK COMPUTER INC	Title : ICH8-M (3)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 18 of 70		

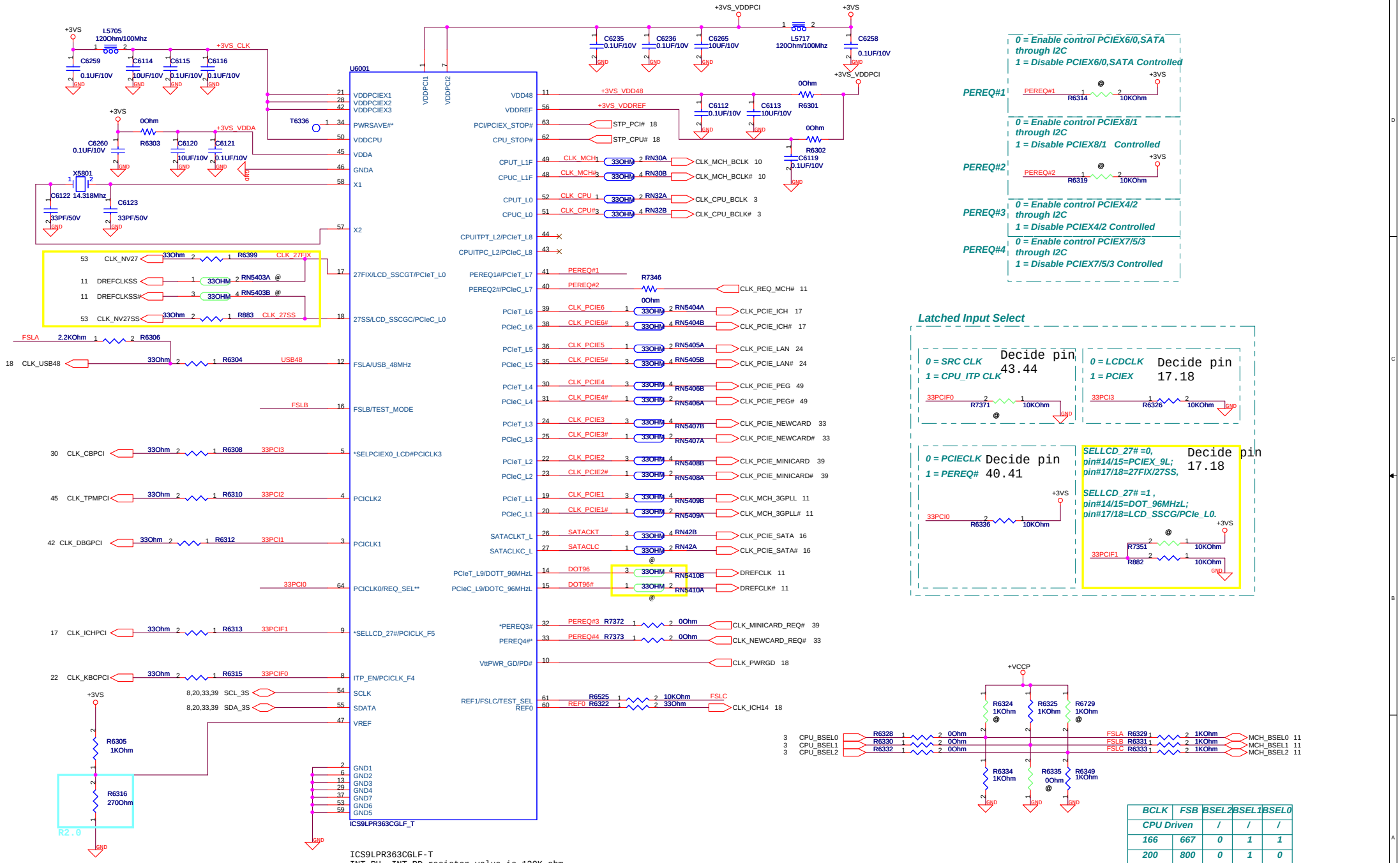


Title : ICH8-M (4)		
ASUSTeK COMPUTER INC	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 19 of 70	





ASUSTeK COMPUTER INC	Title : ICH8M--Other	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 20 of 70	



ICS9LPR363CGLF-T
INT-PU, INT-PD resistor value is 120K ohm.

PEREQ#1
0 = Enable control PCIEX6/0,SATA through I2C
1 = Disable PCIEX6/0,SATA Controlled

PEREQ#2
0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled

PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled

PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled

Latched Input Select

0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44

0 = LCDCLK
1 = PCIEX
Decide pin 17.18

0 = PCIECLK
1 = PEREQ#
Decide pin 40.41

SELLCD_27# =0,
pin#14/15=PCIEX_9L;
pin#17/18=27FIX/27SS,

SELLCD_27# =1 ,
pin#14/15=DOT_96MHzL;
pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18

BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven		/	/	/
166	667	0	1	1
200	800	0	1	0

ASUSTeK COMPUTER INC
Title : CLOCK GEN
Engineer: Lorentz_Chang
Size: Custom
Project Name: T76S
Rev: 2.0
Date: Tuesday, August 21, 2007
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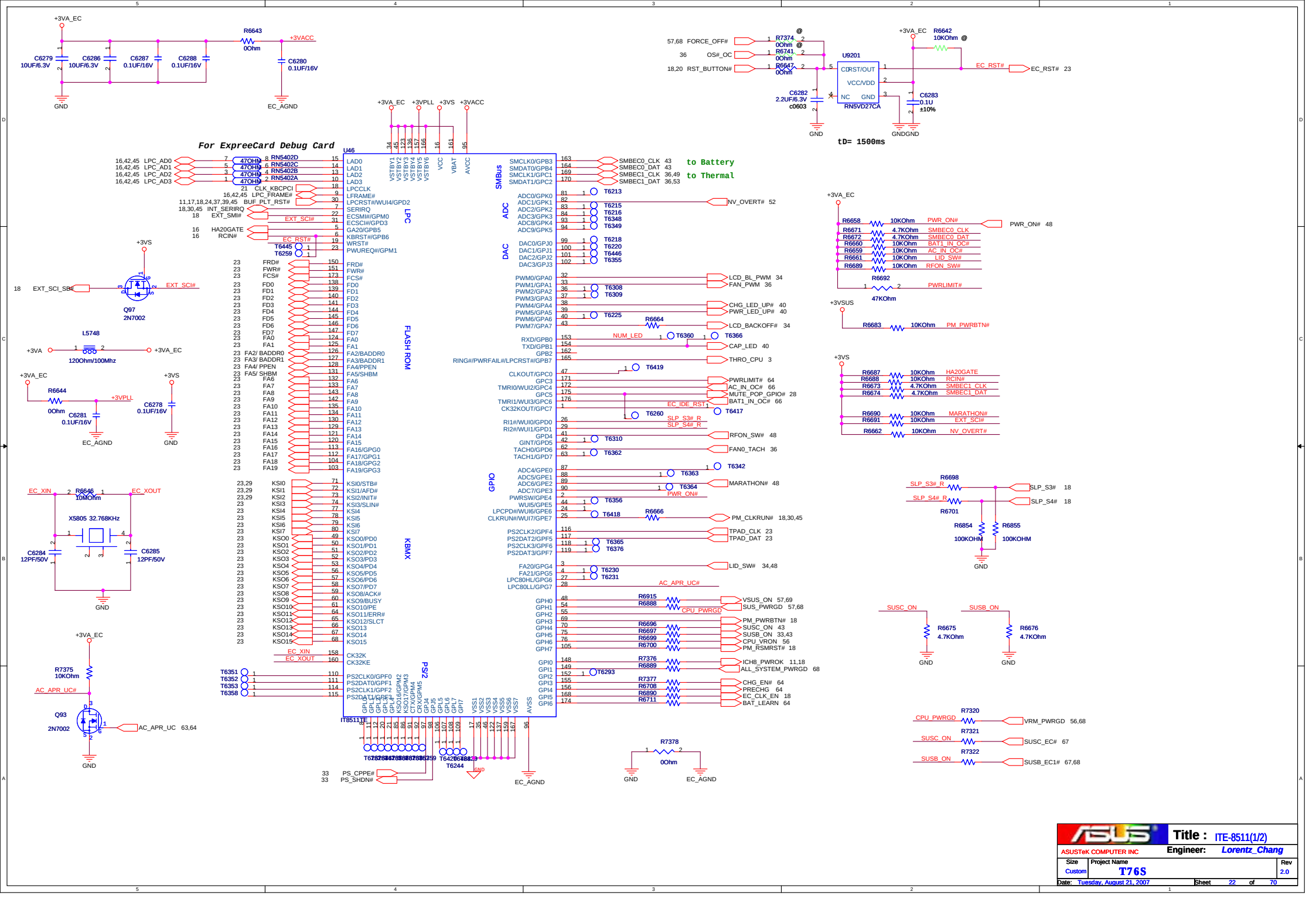
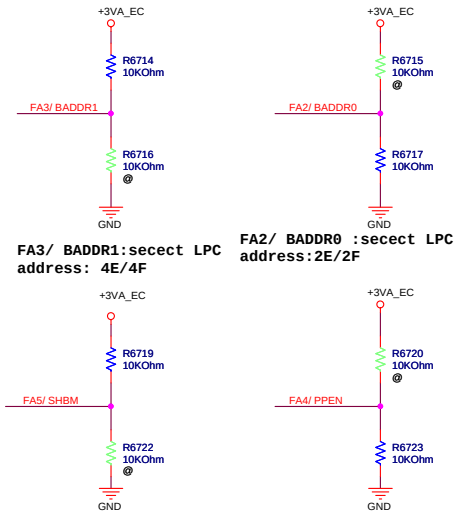

For ExpreeCard Debug Card
U46
IT8511TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
tD= 1500ms
U9201
RN5VD27CA
Title : ITE-8511(1/2)
ASUSTeK COMPUTER INC
Engineer: Lorentz_Chang
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 22 of 70

10:Determined by EC

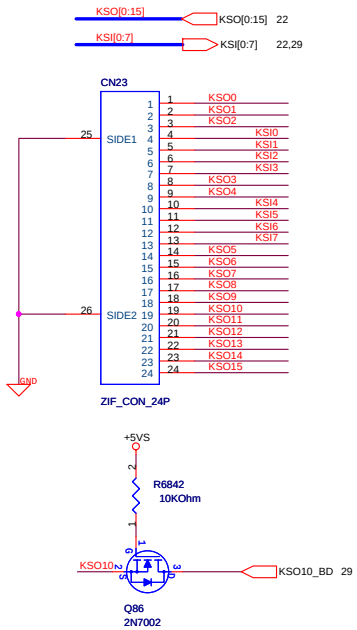


FA3/ BADDR1:secect LPC address: 4E/4F

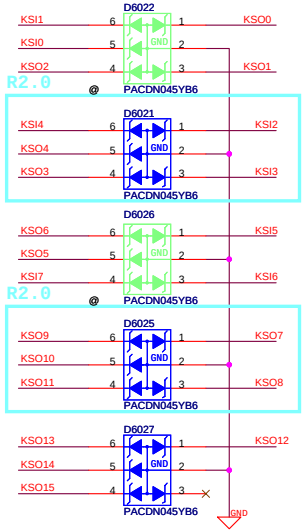
FA2/ BADDR0 :secect LPC address:2E/2F

FA5/ SHBM:share BIOS mode enable.

FA4/ PPEN:enable in-system program via parallel port interface.(KBS down)



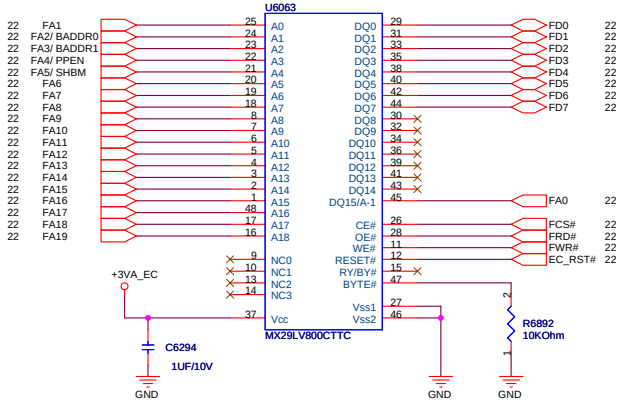
EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.



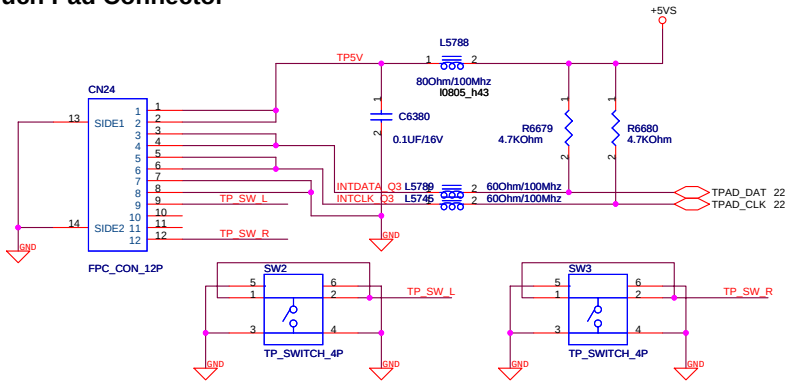
Each IC needs 2 vias to ground.

8M-ROM

8M TSOP

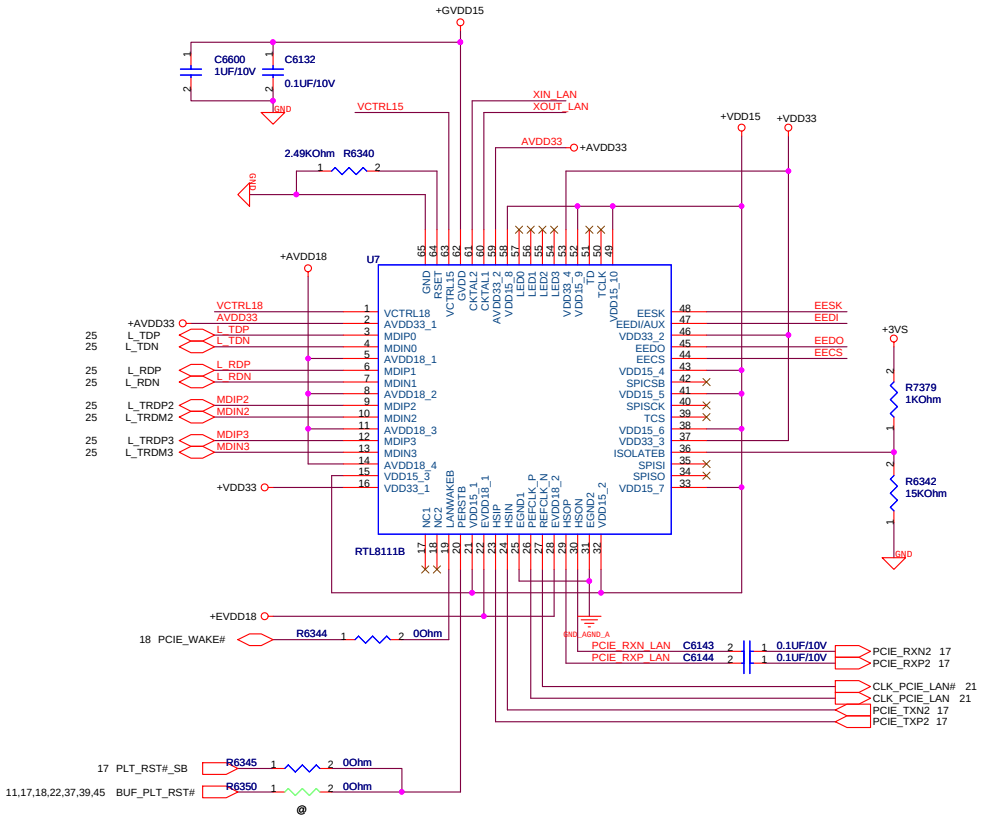


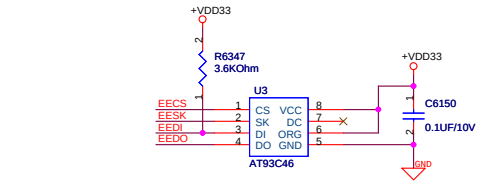
Touch Pad Connector

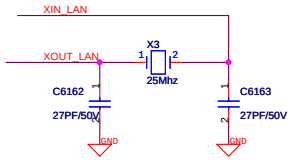


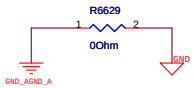
ASUSTeK COMPUTER INC	Title : ITE-8511(2/2)		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 23 of 70		

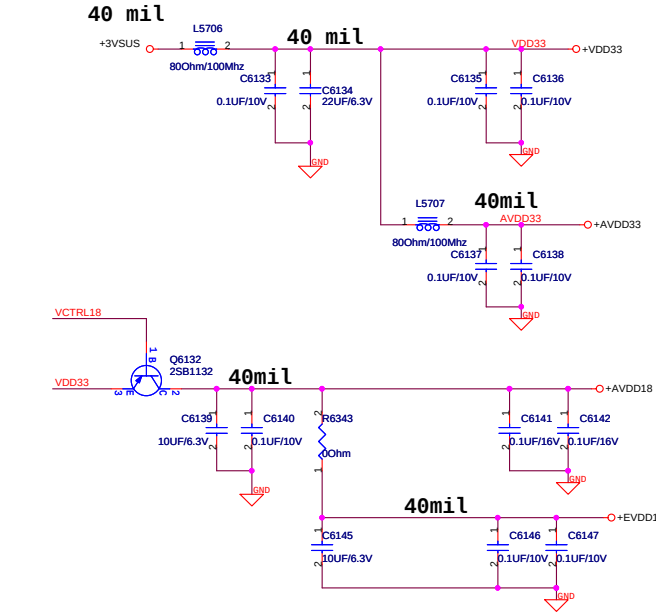
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

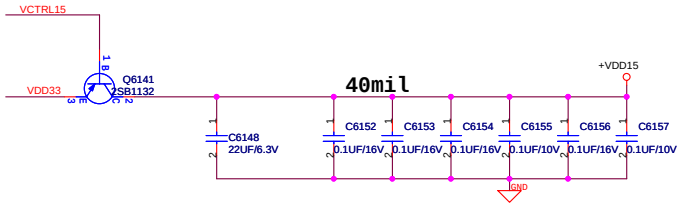




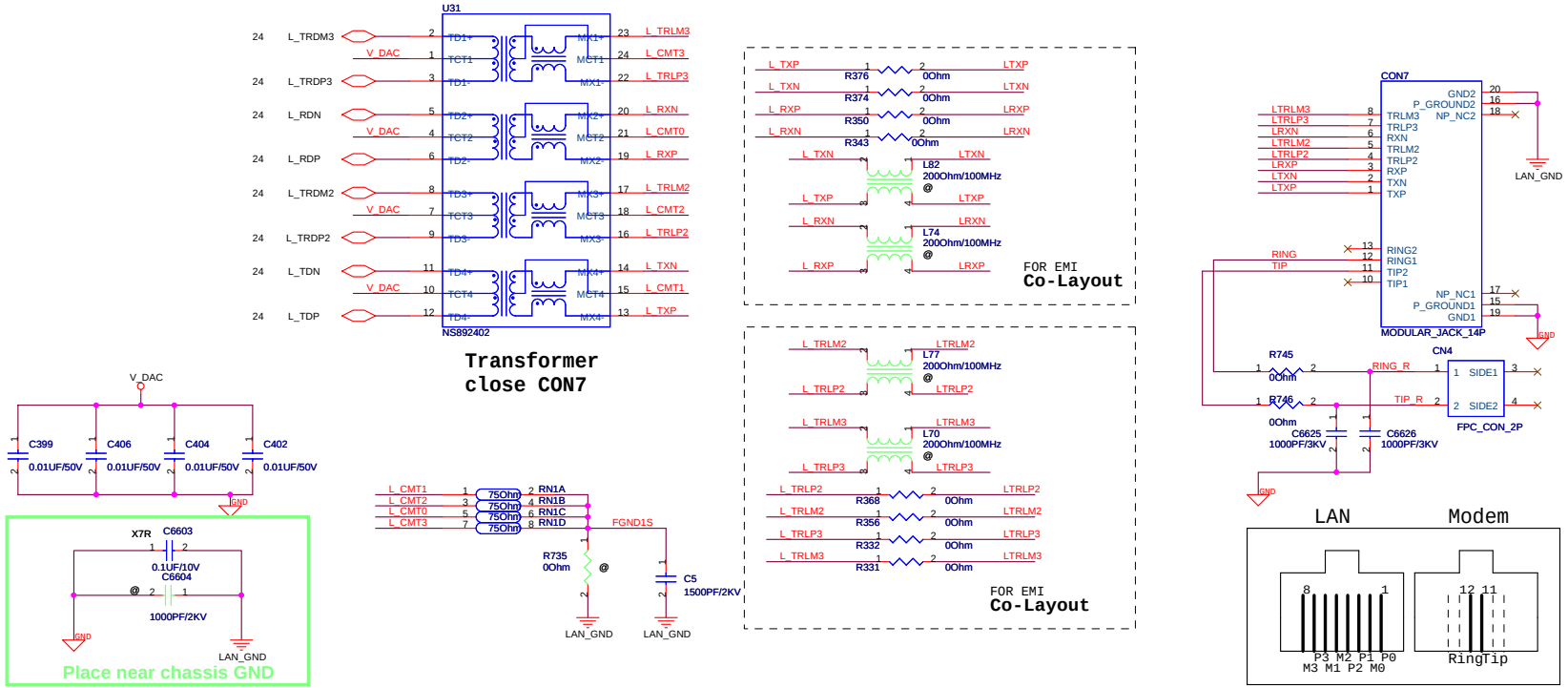




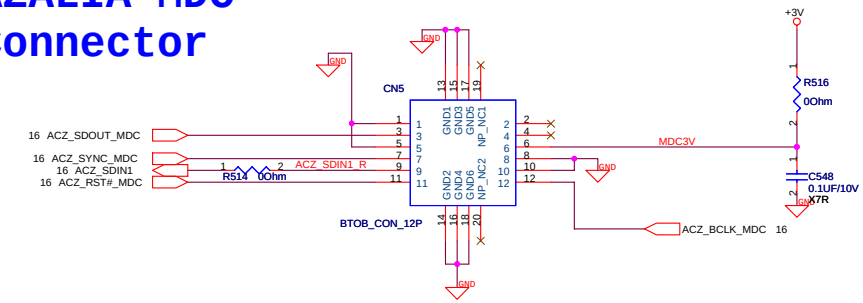




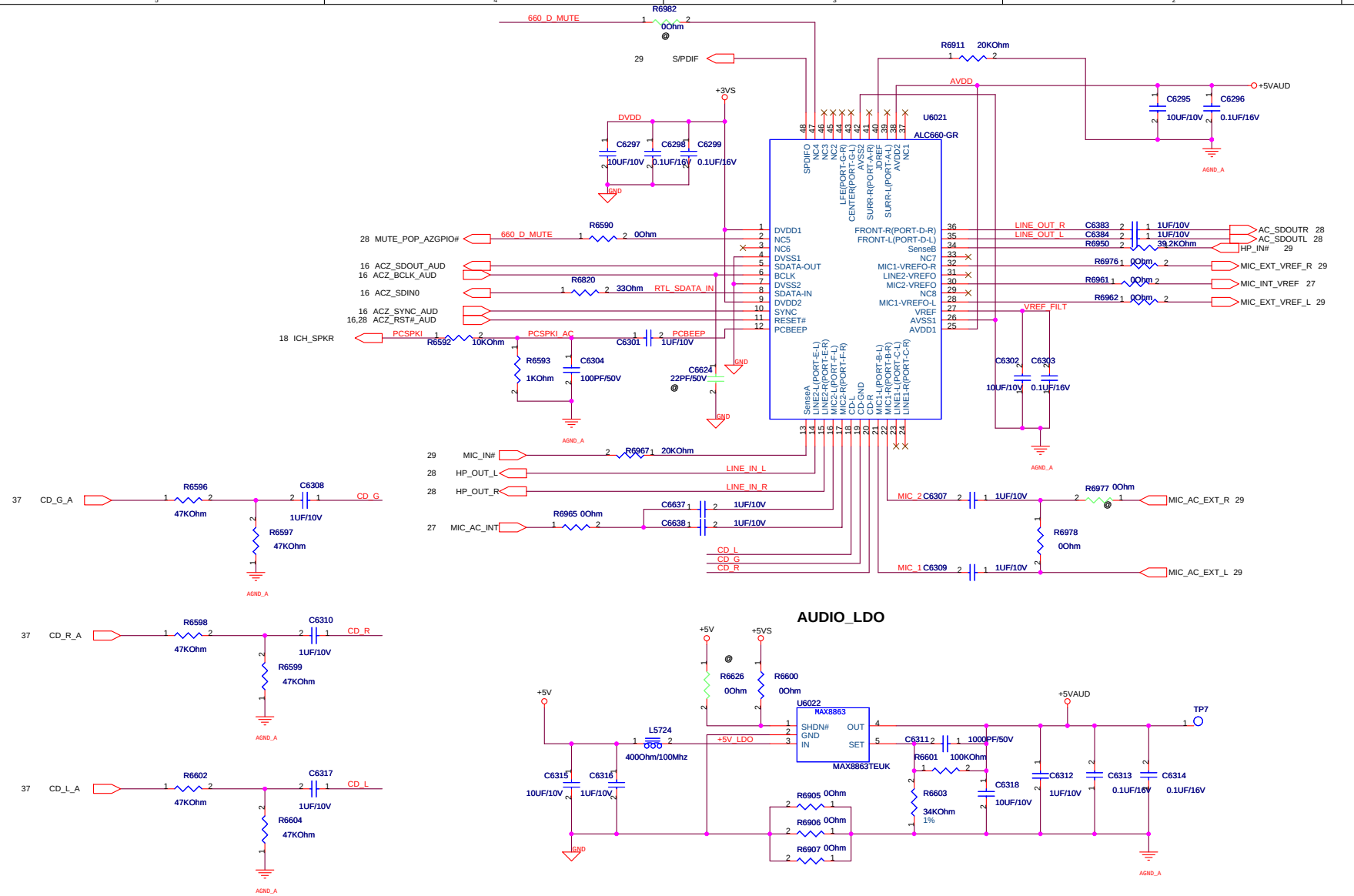
ASUSTeK COMPUTER INC	Title : GigaLAN	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 24 of 70	



AZALIA MDC Connector



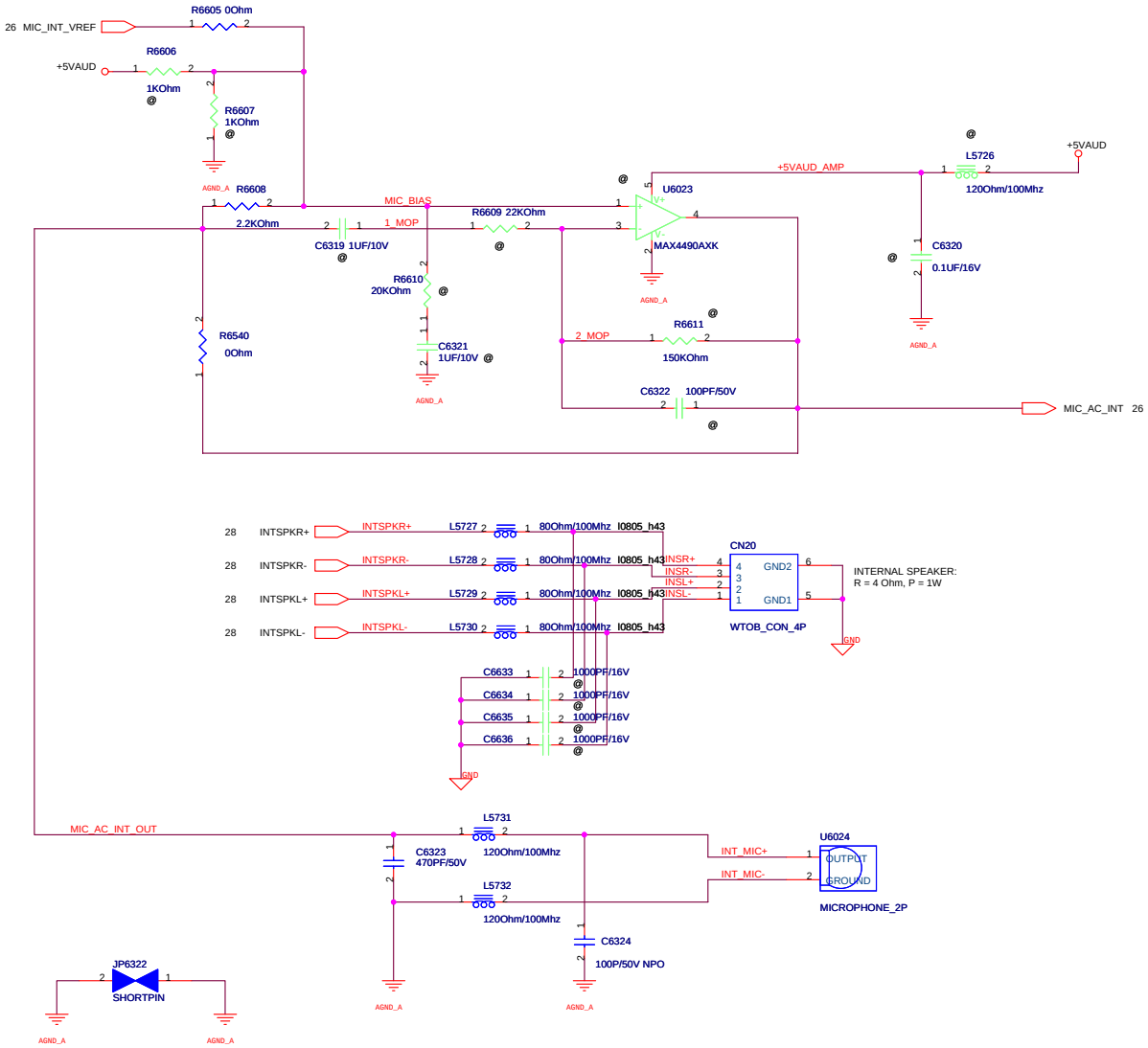
ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 25 of 70	



<Variant Name>

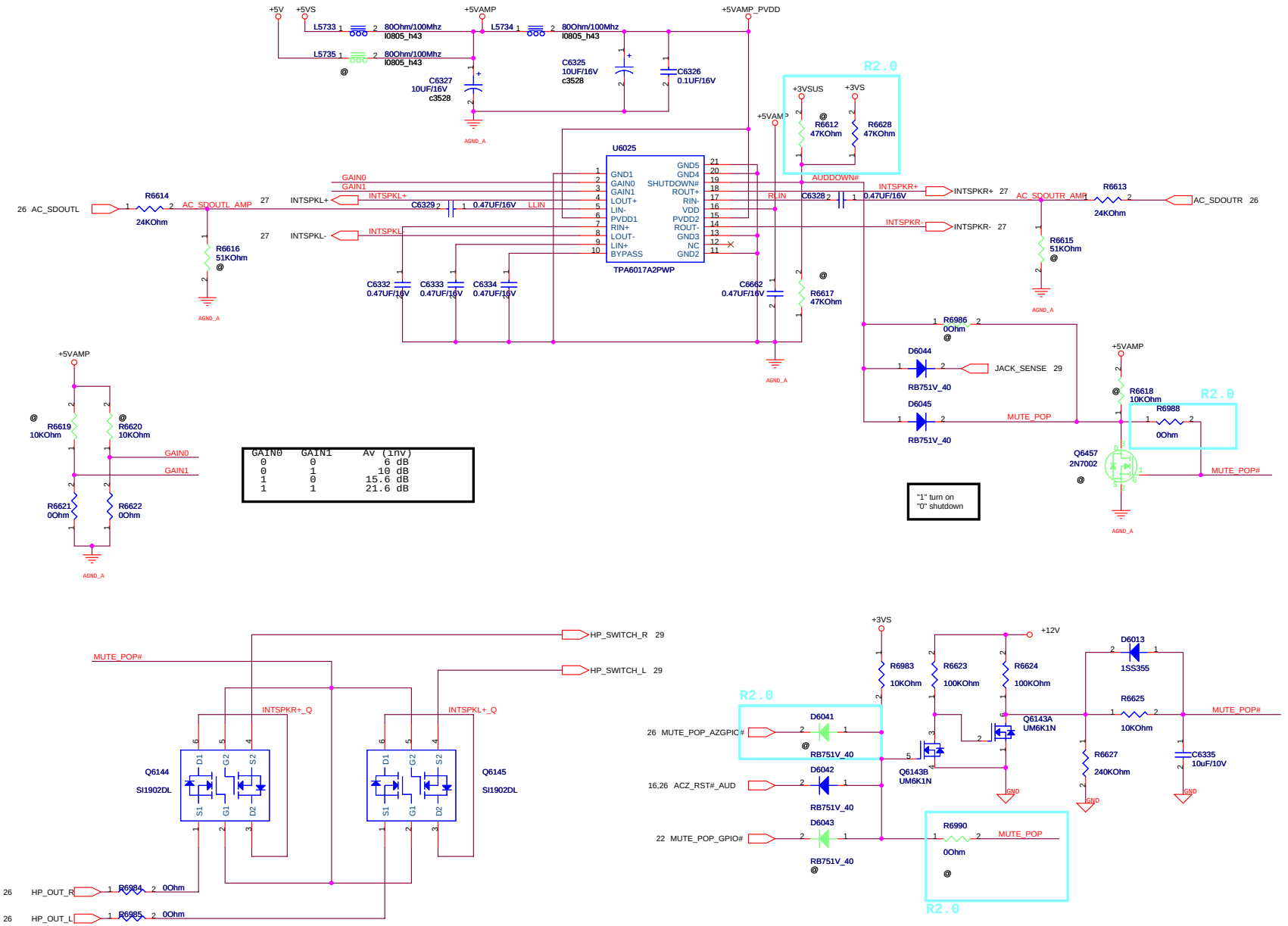
ASUSTeK COMPUTER INC	Title : AZALIA_ALC660	
	Engineer:	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 26 of 70	

MIC PreAmp & Mic Jack



<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC PREAMP & INT MIC	Engineer:
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 27 of 70	



GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

<Variant Name>

Title : AUDIO_AMP & INT SPK

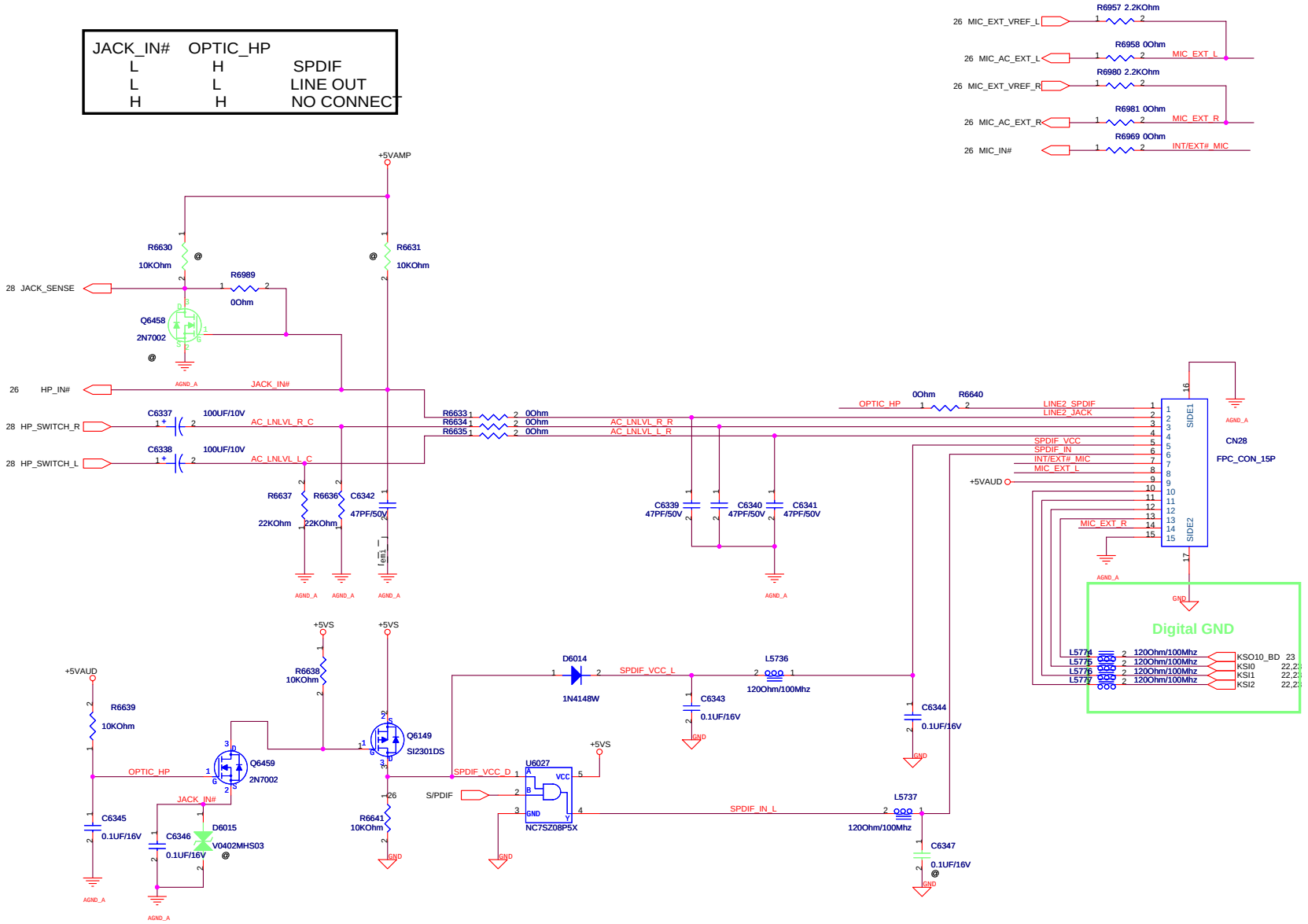
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	T76S	2.0

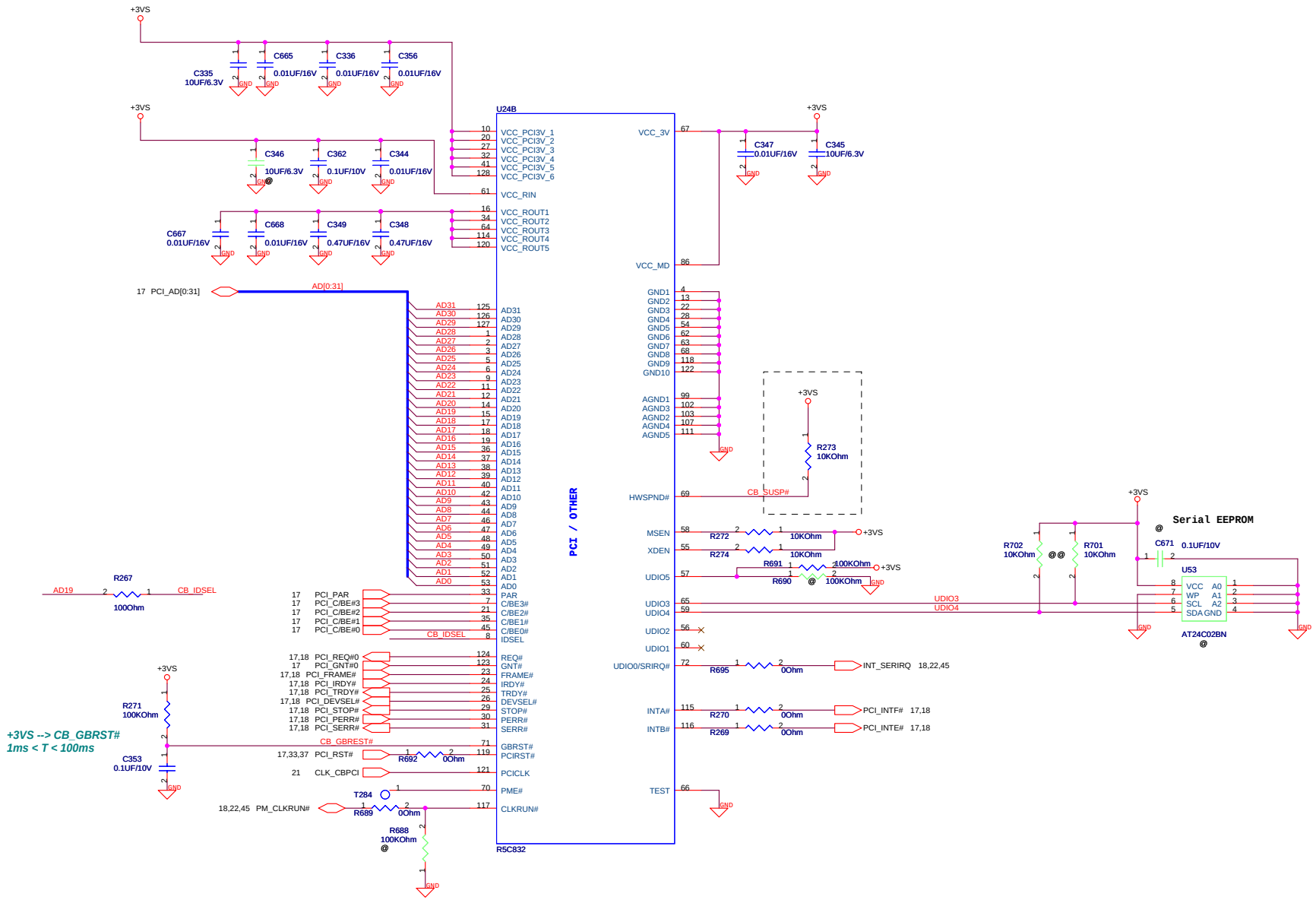
Date: Tuesday, August 21, 2007 Sheet 28 of 70

JACK_IN#	OPTIC_HP	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT

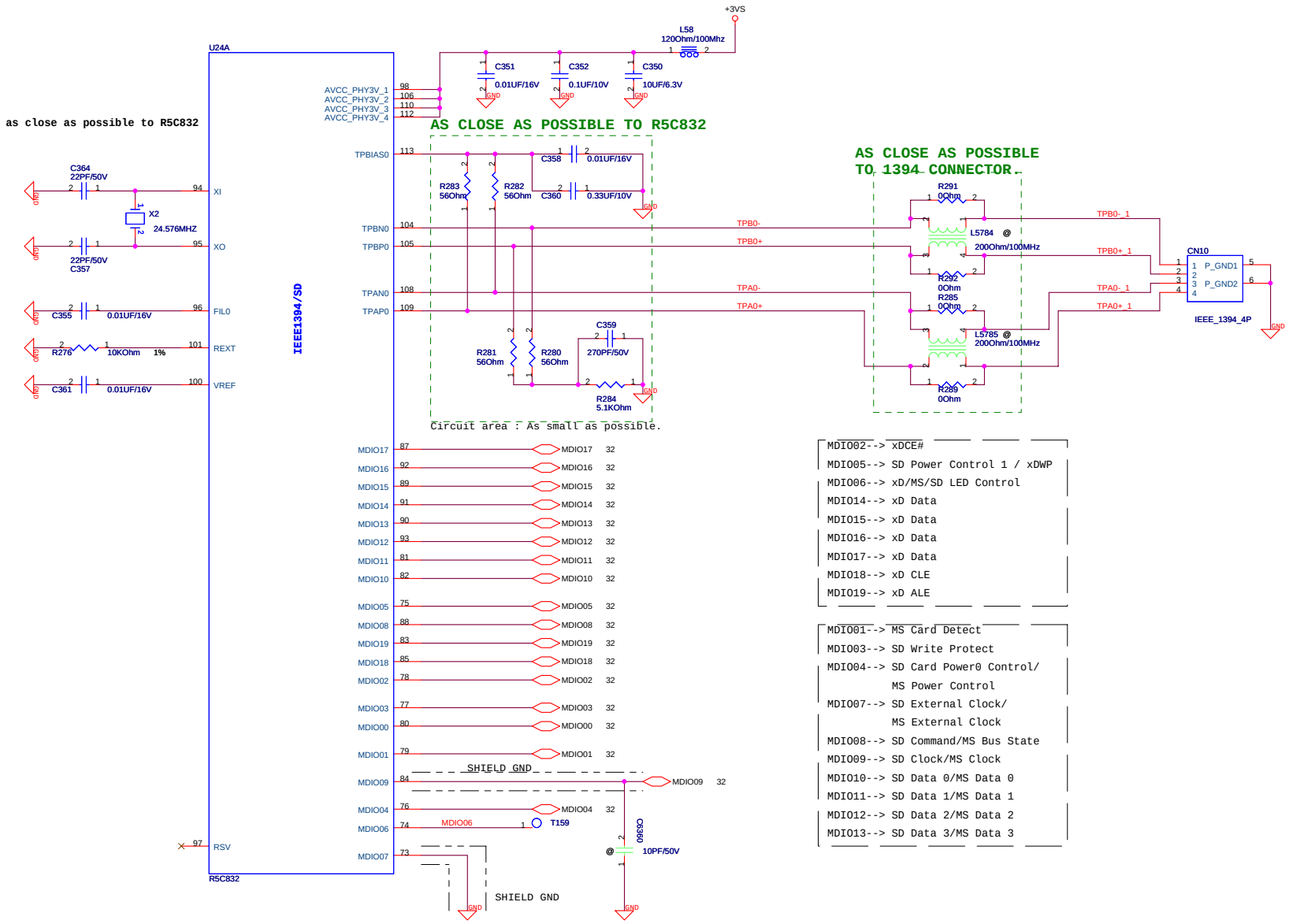


<Variant Name>

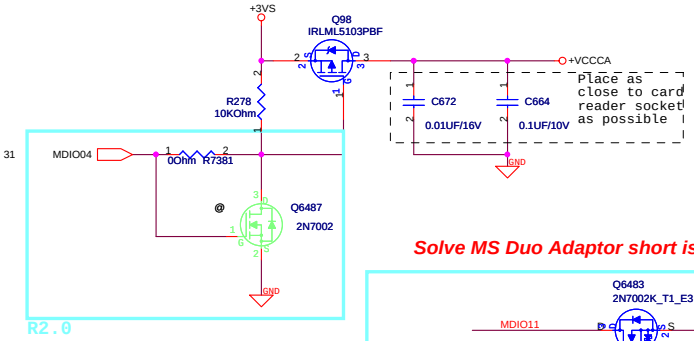
ASUSTeK COMPUTER INC	Title : SPDIF JACK	
	Engineer:	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 29 of 70	



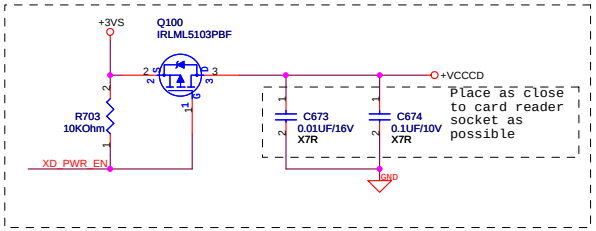
ASUSTeK COMPUTER INC	Title : RICOH R5C832/PCI_B
	Engineer: Lorentz_Chang
Size: Custom	Project Name: T76S
Rev: 2.0	
Date: Tuesday, August 21, 2007	Sheet 30 of 70



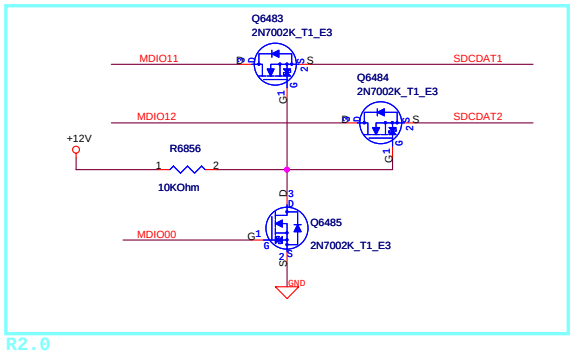
ASUSTeK COMPUTER INC	Title : RICOH R5C832/PCI_A	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 31 of 70	



To correct the problem when MS Duo adaptor is in use.

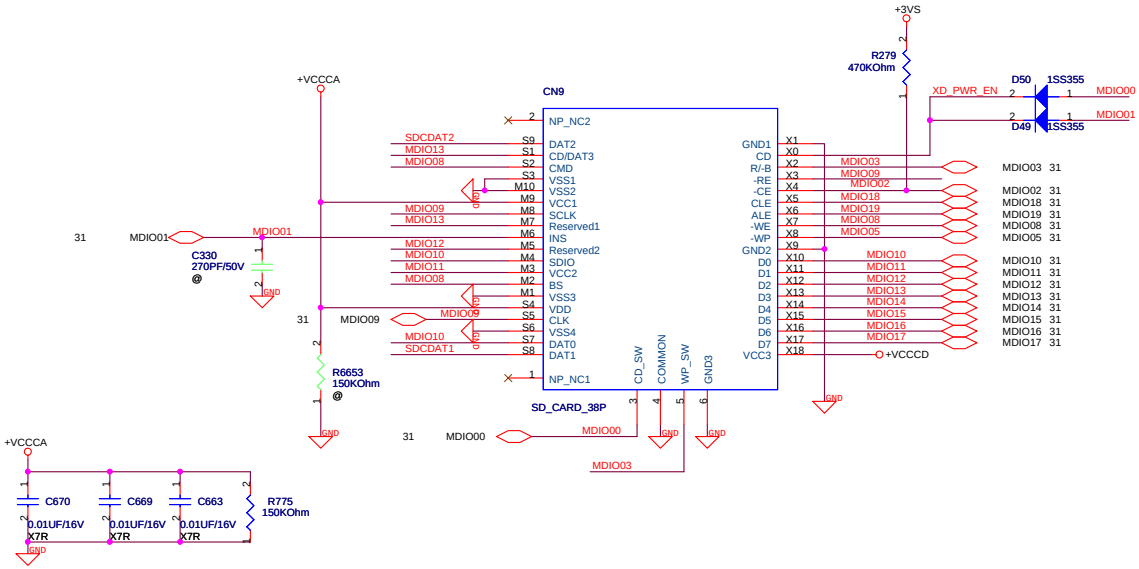


Solve MS Duo Adaptor short issue.

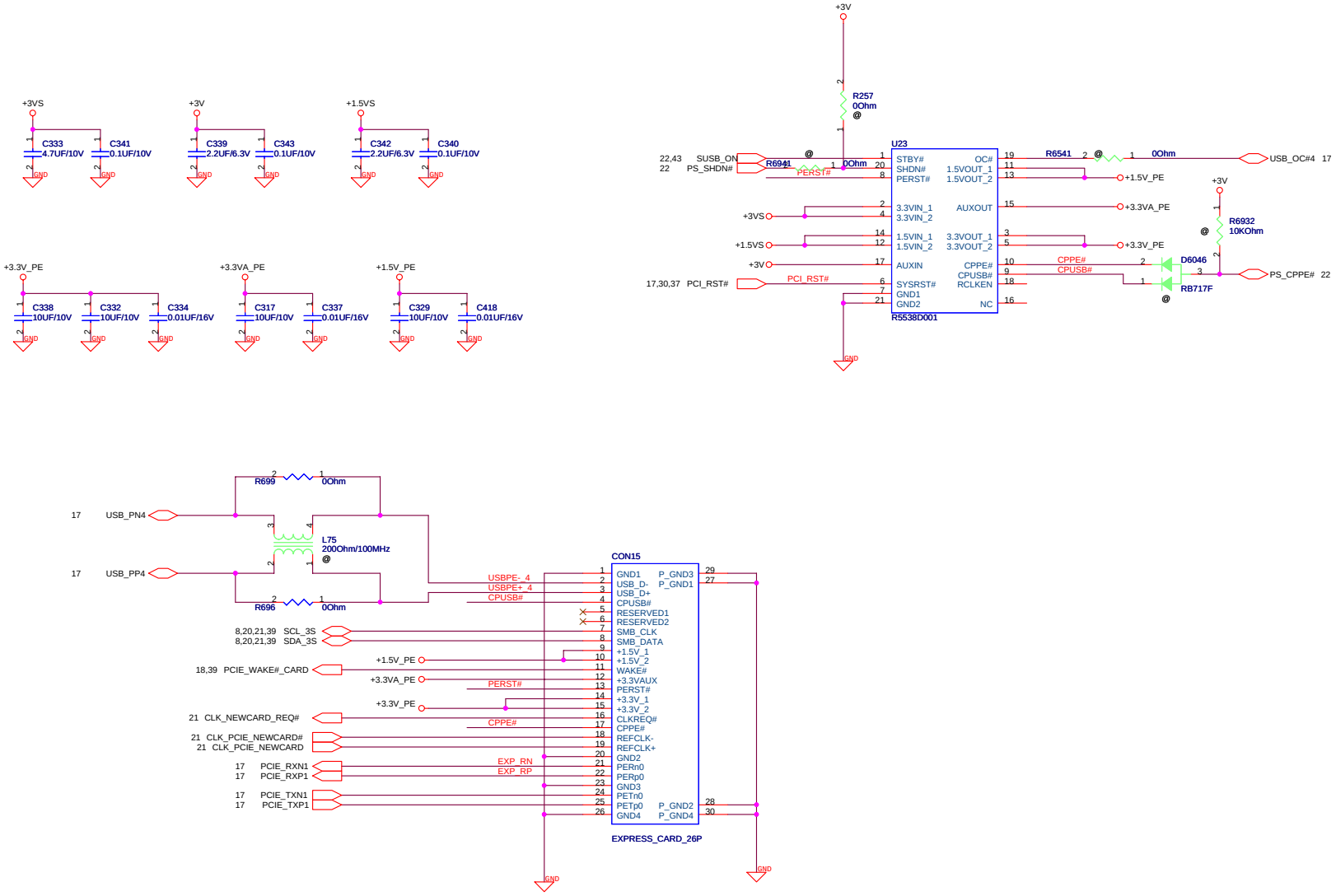


MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

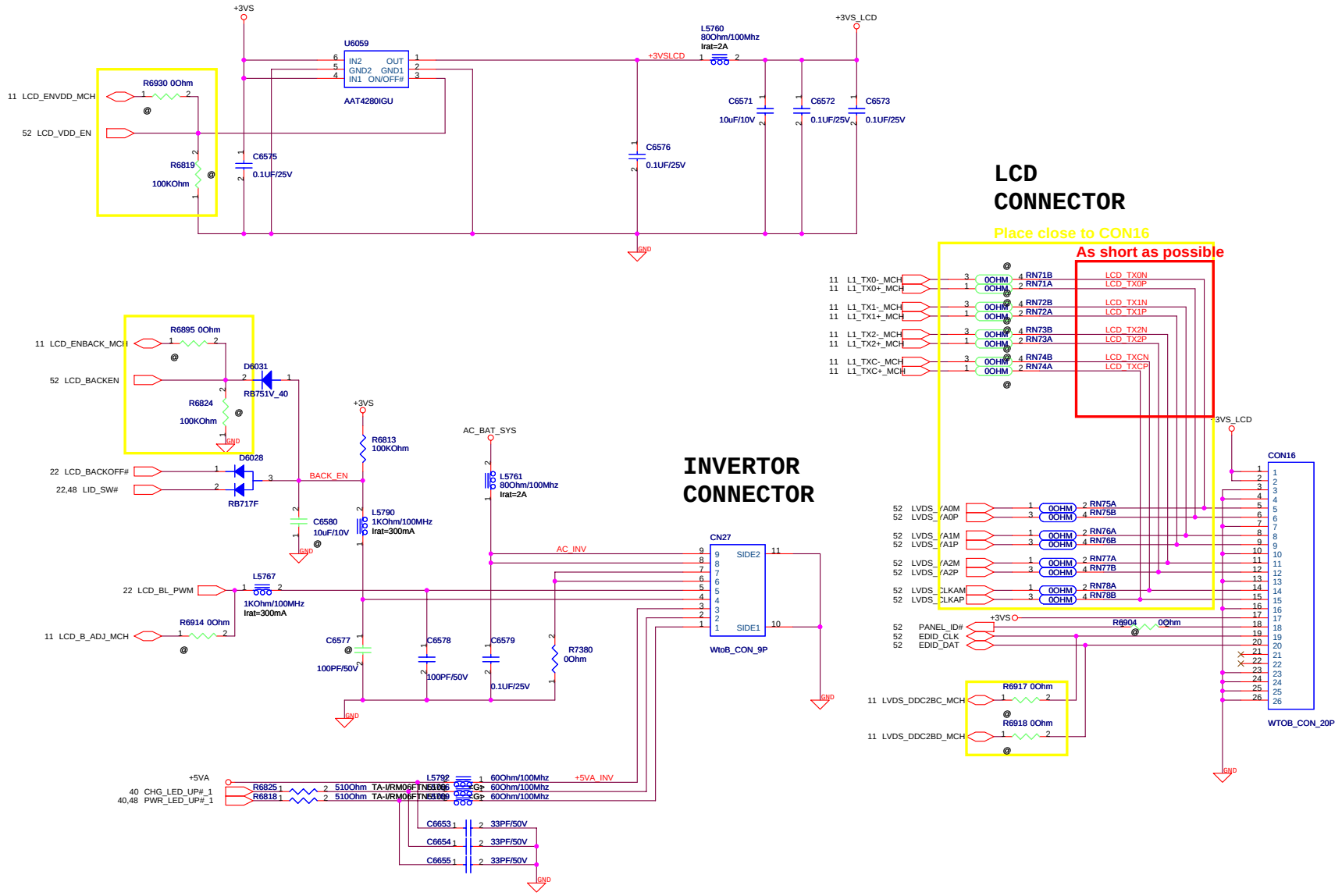
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE



ASUSTeK COMPUTER INC	Title : CardReader		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 32 of 70		



ASUSTeK COMPUTER INC	Title : Express Card	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 33 of 70	



ASUSTeK COMPUTER INC

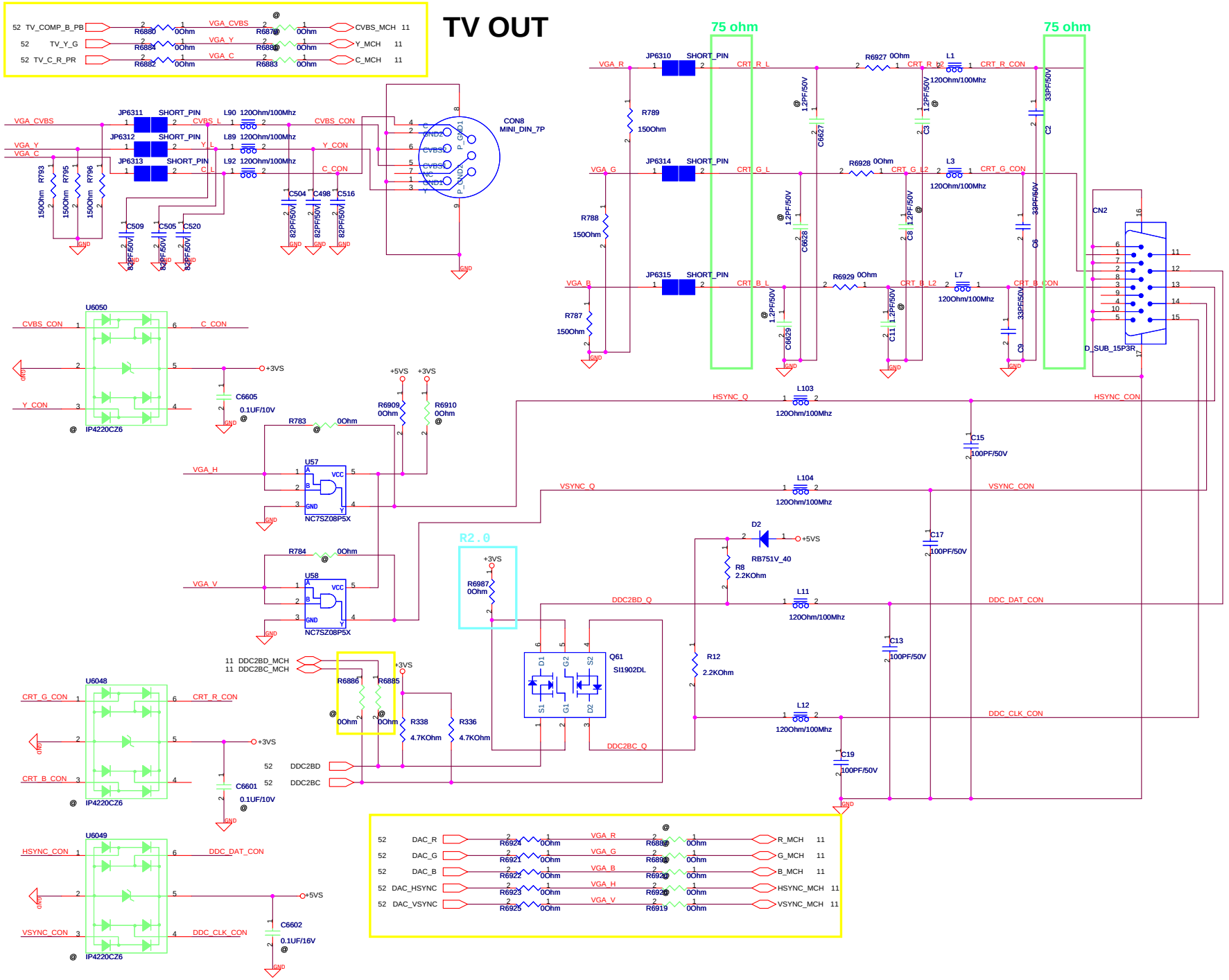
Title : LVDS & Inverter

Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

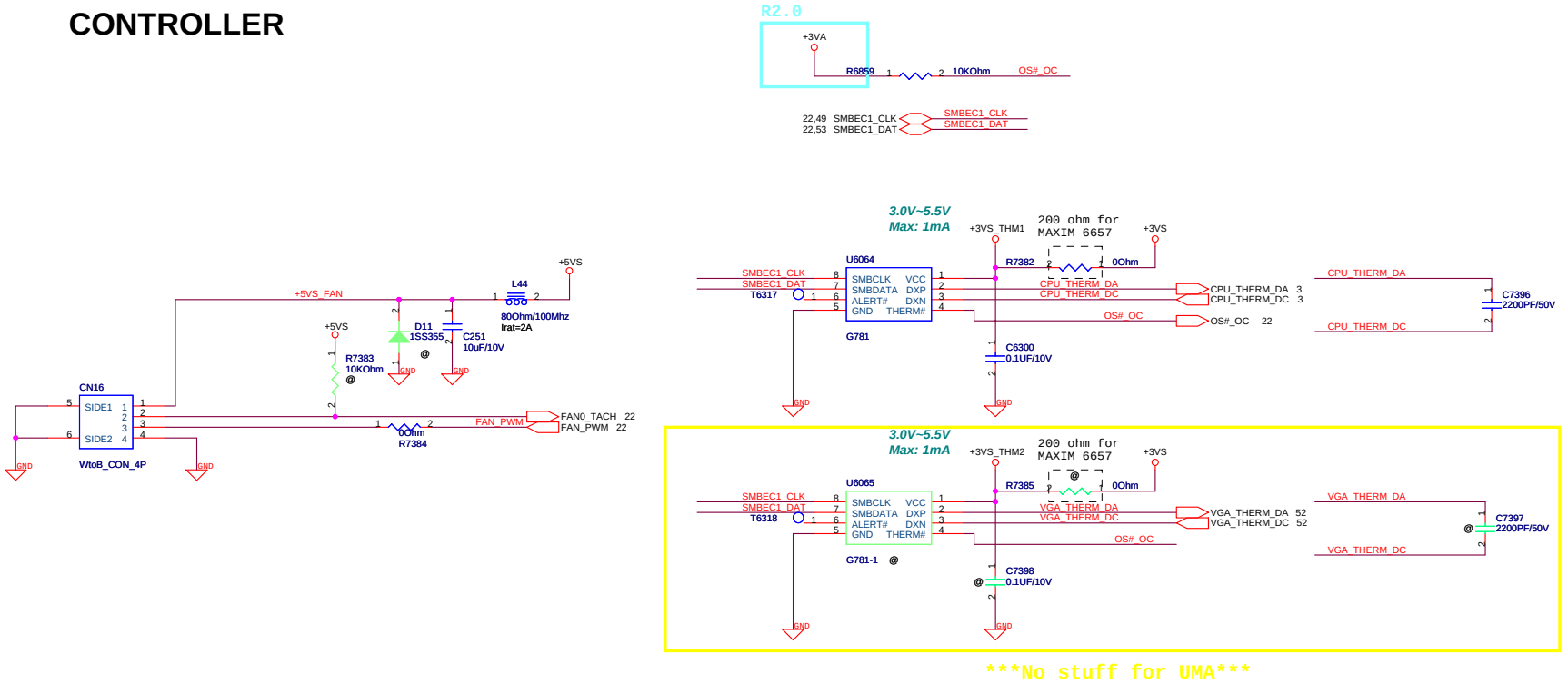
Date: Tuesday, August 21, 2007 Sheet 34 of 70

TV OUT



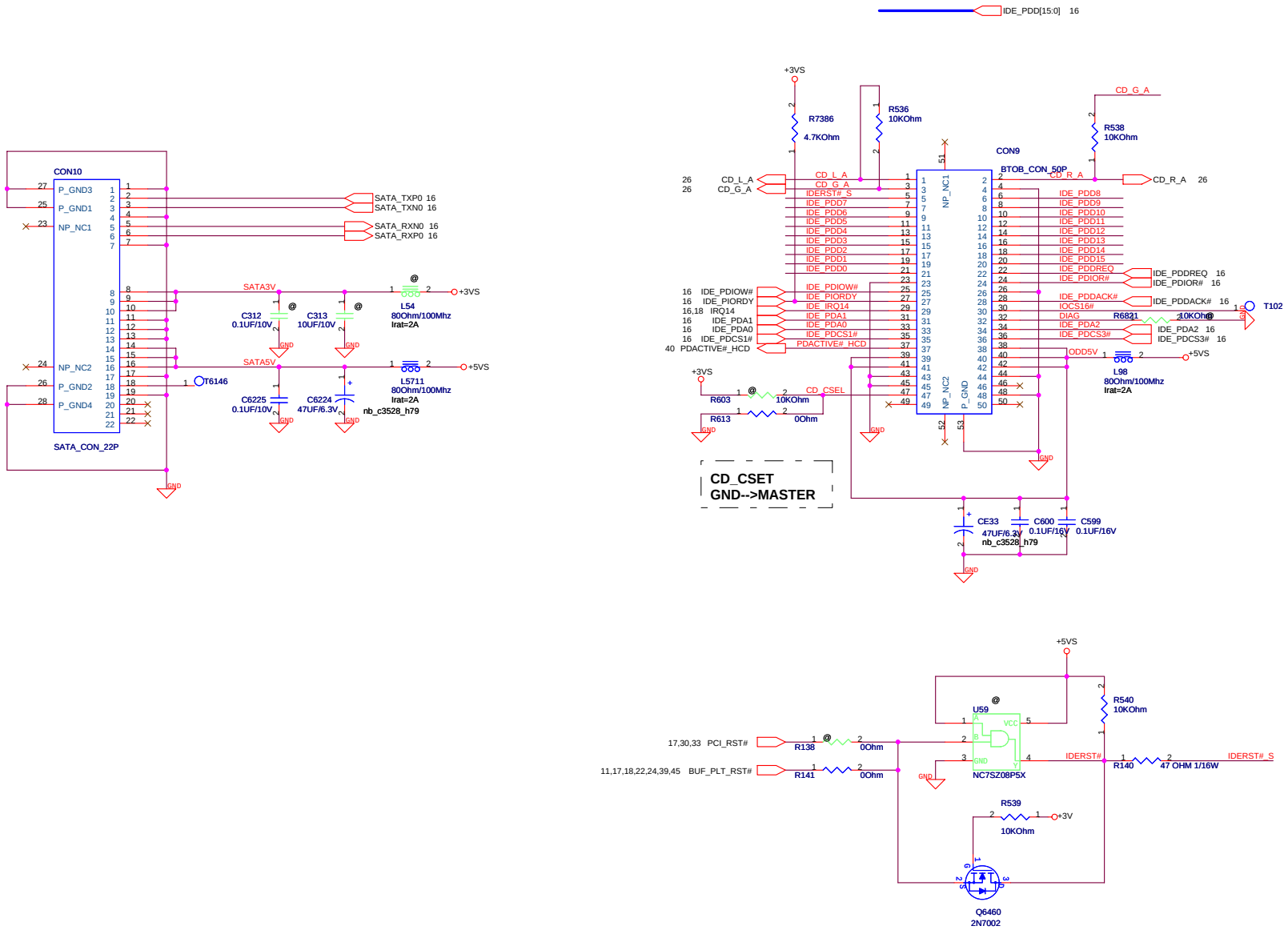
ASUSTeK COMPUTER INC	Title : CRT & TV-Out		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 35 of 70		

FAN & THERMAL CONTROLLER

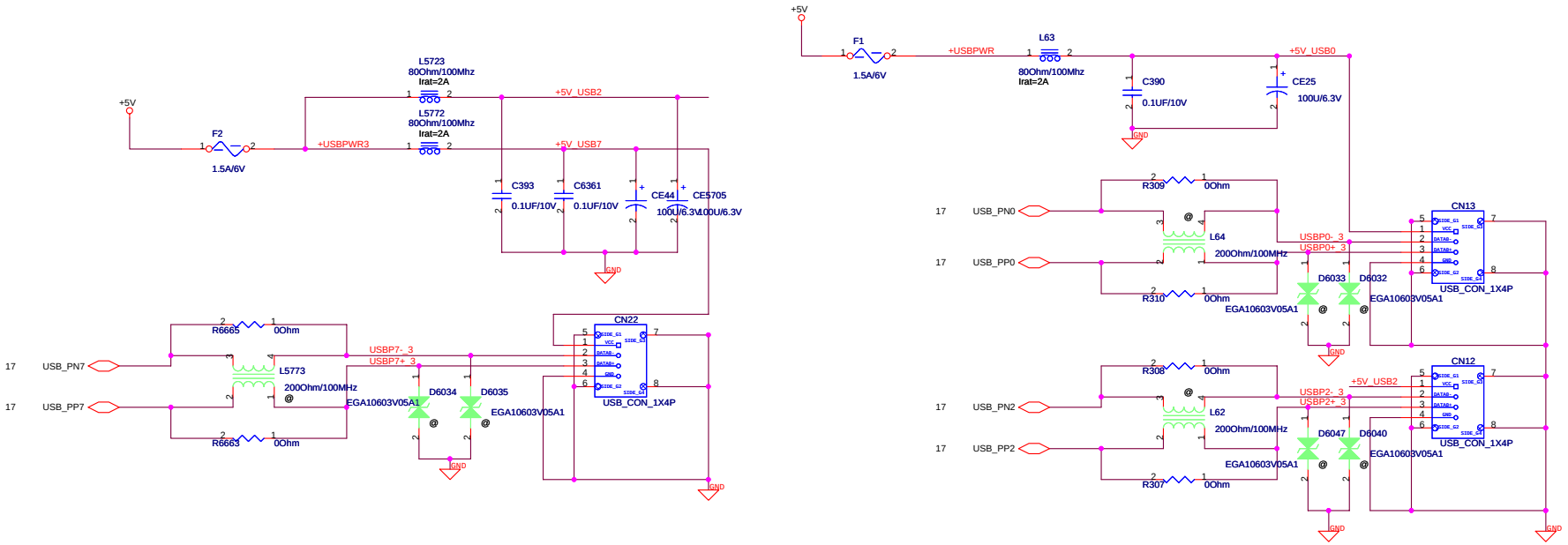


No stuff for UMA

ASUSTeK COMPUTER INC	Title : FAN	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 36 of 70	

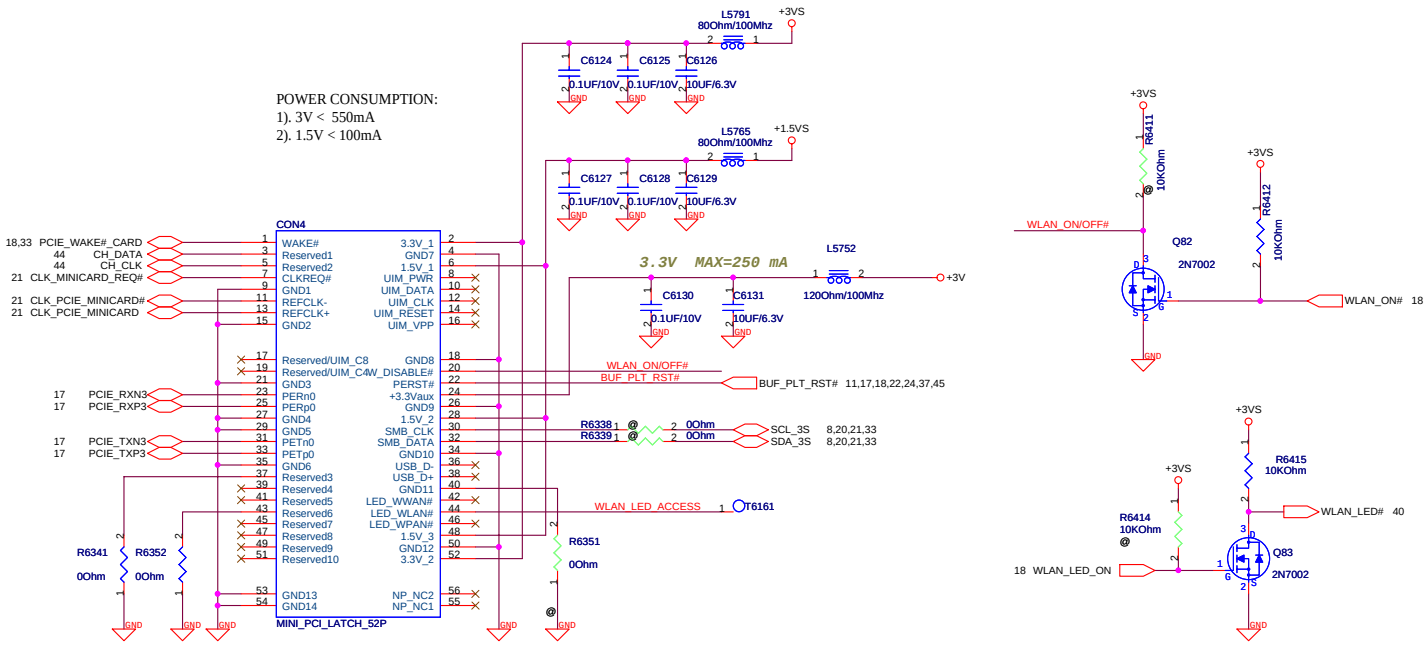


ASUSTeK COMPUTER INC	Title : HD+ODD	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 37 of 70	



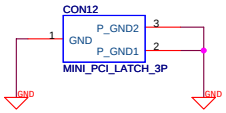
ASUSTeK COMPUTER INC	Title : USB CON* 3	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 38 of 70	

WLAN CON



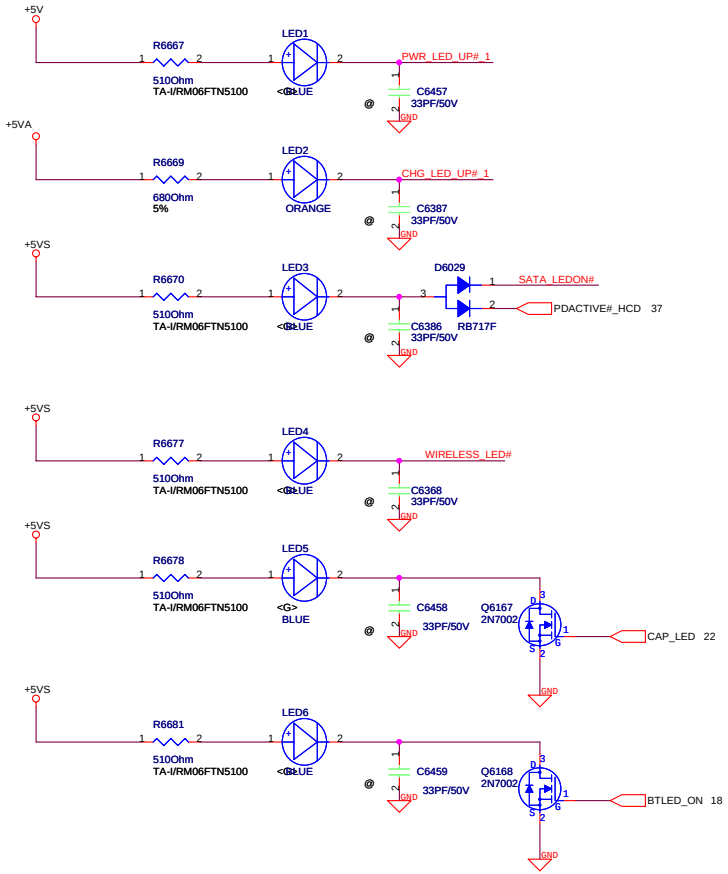
PCB Height =0mm

Mini Card Latch

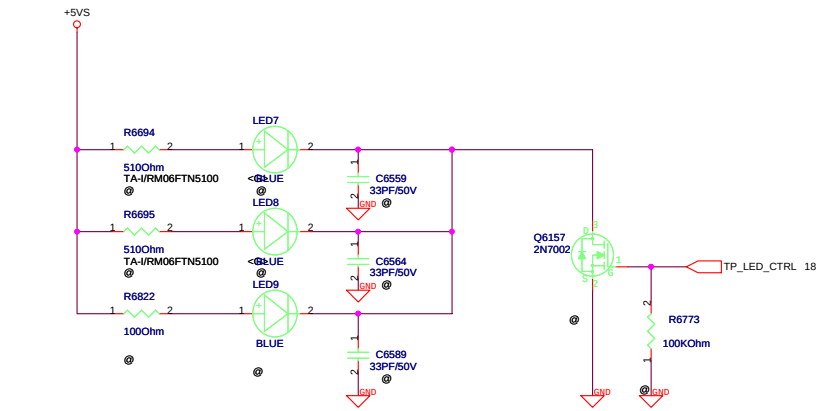


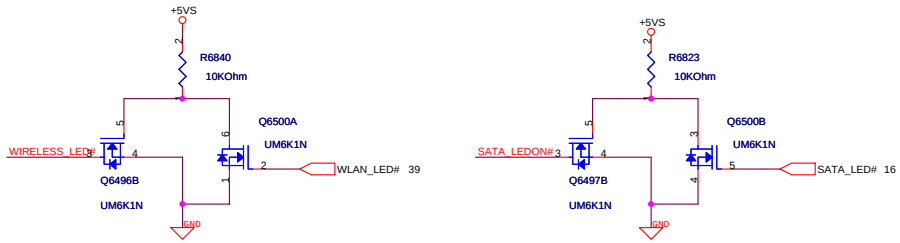
ASUSTeK COMPUTER INC	Title : MINICARD		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 39 of 70		

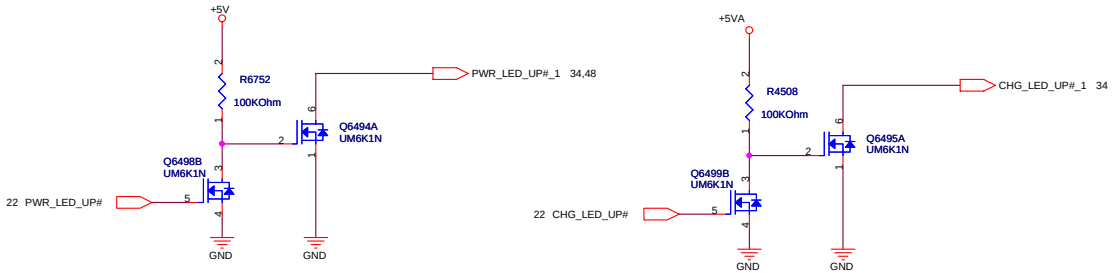
MB/LEDs



Touch Pad LED

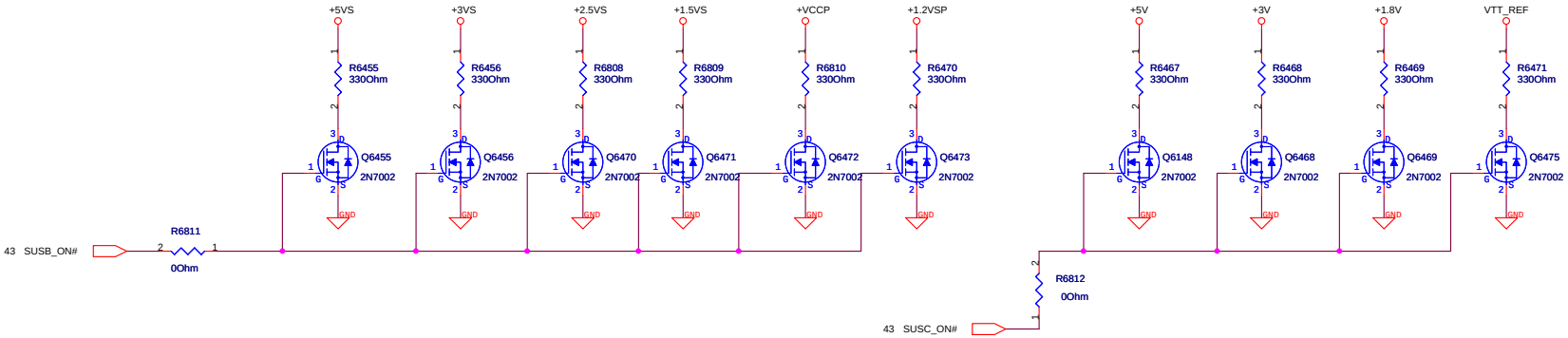






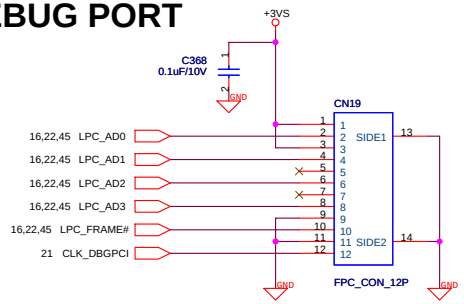
ASUSTeK COMPUTER INC	Title : LED	Engineer: Lorentz_Chang
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 40 of 70	

Discharge Circuit



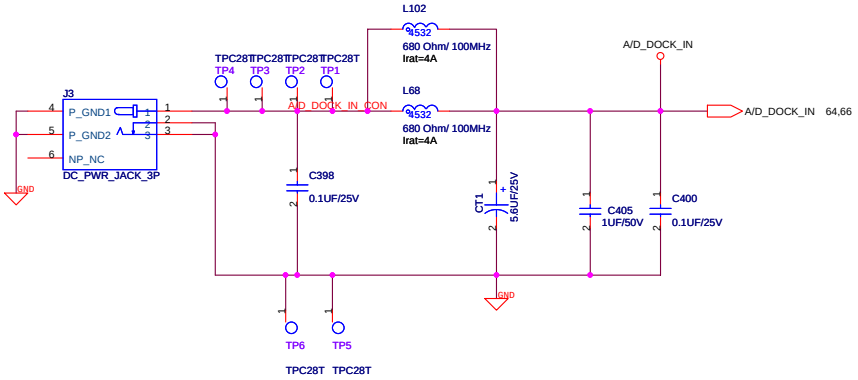
ASUSTeK COMPUTER INC	Title : Discharge		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 41 of 70		

LPC DEBUG PORT

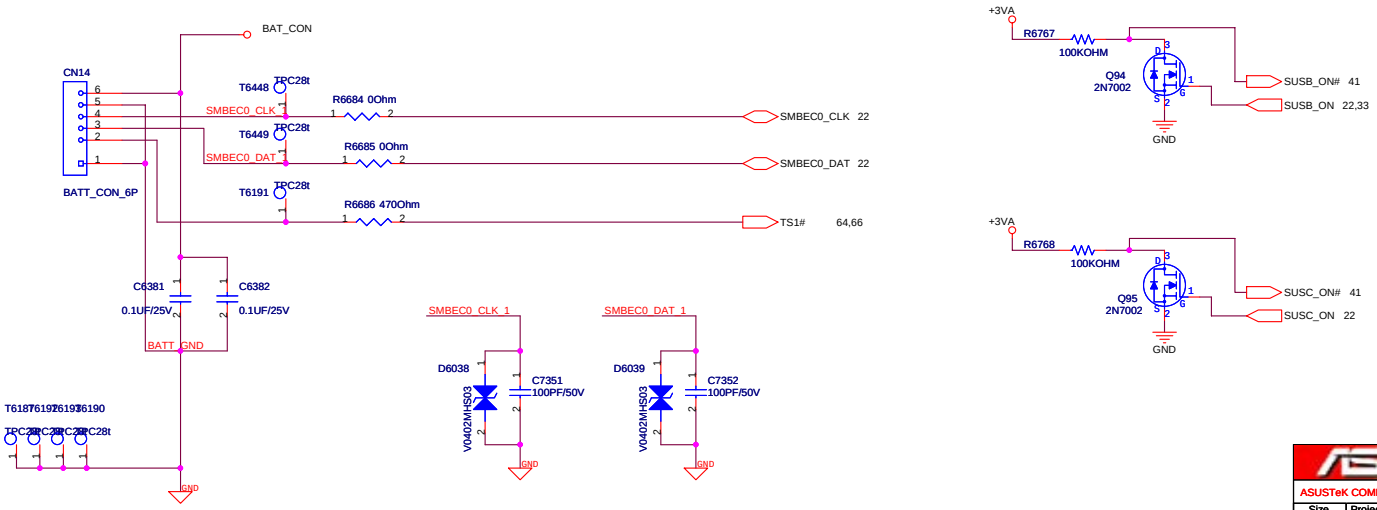


ASUSTeK COMPUTER INC	Title : Debug Port	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 42 of 70	

DC-IN

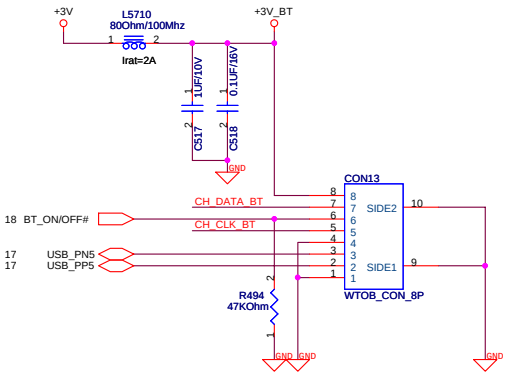


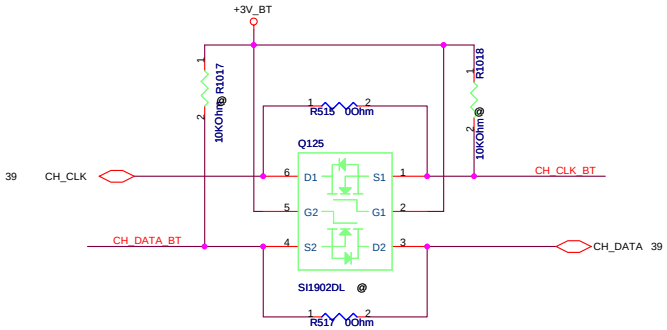
Battery Connector



ASUSTeK COMPUTER INC	Title : DC-in / BAT con		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 43 of 70		

Bluetooth Module
Connector

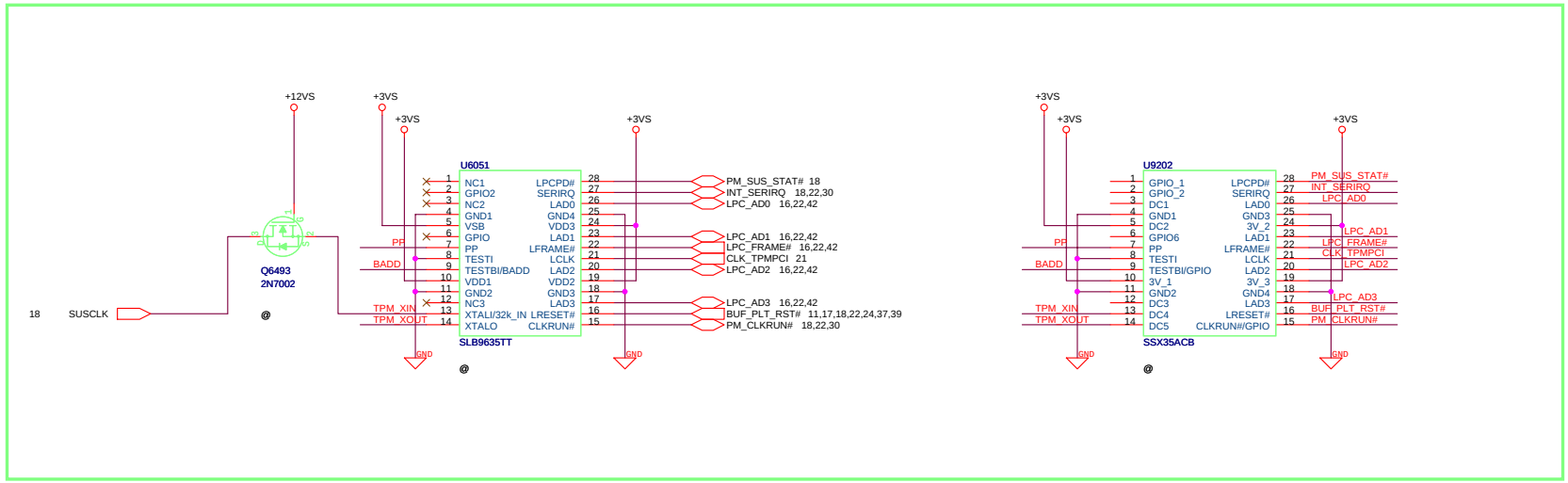


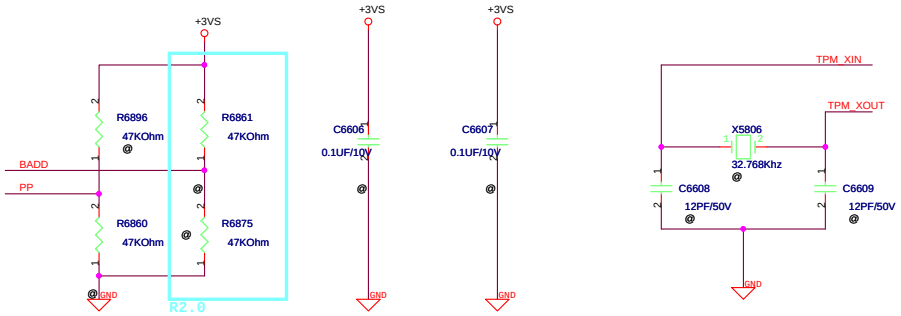


ASUSTeK COMPUTER INC	Title : BT	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 44 of 70	

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.

CO-LAYOUT





ASUSTeK COMPUTER INC	Title : TPM		
	Engineer: Lorentz_Chang		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 45 of 70		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
VGA	AD16		A
LAN	AD16	0	B
CARD READER	AD17	1	B
CARDBUS	AD19	1	C
1394	AD17	1	D
MINIPCI 2 (802.11)	AD17	3	D,C

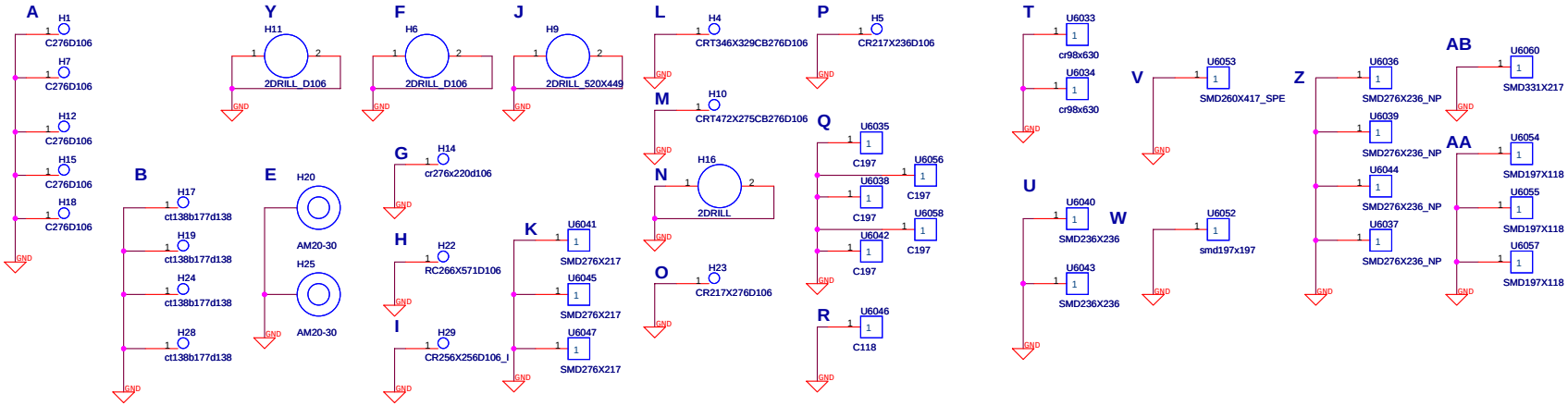
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

ICH8-M GPIO	W7S
GPIO 0	PM_BMBUSY#
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 7	WLAN_LED_ON
GPIO 8	EXT_SMI#
GPIO 11	SMBALERT#
GPIO 12	EXT_SCI_SB#
GPIO 15	STP_PCI#
GPIO 16	DPRSLPVR
GPIO 17	WLAN_ON#
GPIO 19	MEM_ID1
GPIO 20	BTLED_ON
GPIO 21	MEM_ID0
GPIO 22	MEMCLK_SET
GPIO 25	STP_CPU#
GPIO 27	BT_ON/OFF#
GPIO 29	USB_OC#5
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 36	MEM_ID2
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 40	USB_OC#1
GPIO 41	USB_OC#2
GPIO 43	USB_OC#4
GPIO 49	CPUPWRGD
GPIO 50	PCI_REQ#1
GPIO 52	PCI_REQ#2
GPIO 54	PCI_REQ#3

ITE8511 GPIO	W7S
GPA0	LCD_BL_PWM
GPA1	FAN_PWN
GPA4	CHG_LED_UP#
GPA5	PWR_LED_UP#
GPA7	LCD_BACKOFF#
GPB1	CAP_LED
GPB2	TP_LED_CTRL
GPB3	SMBEC0_CLK
GPB4	SMBEC0_DAT
GPB5	A20GATE
GPB6	RC_IN#
GPB7	THRO_CPU
GPC1	SMBEC1_CLK
GPC2	SMBEC1_DAT
GPC4	ACIN_OC#
GPC5	MUTE_POP_GPIO#
GPC6	BAT_IN_OC#
GPD0	SLP_S3#_R
GPD1	SLP_S4#_R
GPD2	BUF_PLT_RST#
GPD3	EXT_SCI#
GPD4	RFON_SW#
GPD6	FAN0_TACH
GPE2	MARATHON#
GPE4	PWR_ON#
GPE7	PM_CLKRUN#
GPF4	TPAD_CLK
GPF5	TPAD_DAT
GPG0	FA16
GPG1	FA17
GPG2	FA18
GPG3	FA19
GPG4	LID_SW#
GPG7	AC_APR_UC#
GPH0	VSUS_ON
GPH1	SUS_PWRGD
GPH2	CPU_PWRGD
GPH3	PM_PWRBTN#
GPH4	SUSC_ON
GPH5	SUSB_ON
GPH6	CPU_VRON
GPH7	PM_RSMRST#
GPI0	ICH8_PWROK
GPI1	ALL_SYSTEM_PWRGD
GPI3	CHG_EN#
GPI4	PRECHG
GPI5	EC_CLK_EN
GPI6	BAT_LEARN
GPJ4	PS_CPPE#
GPJ5	PS_SHDN#
GPM0	EXT_SMI#

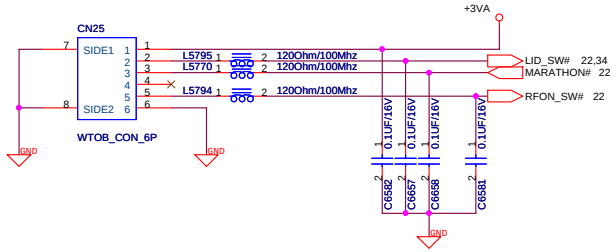
ASUSTeK COMPUTER INC	Title : System Resource	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 46 of 70	

SCREW HOLE



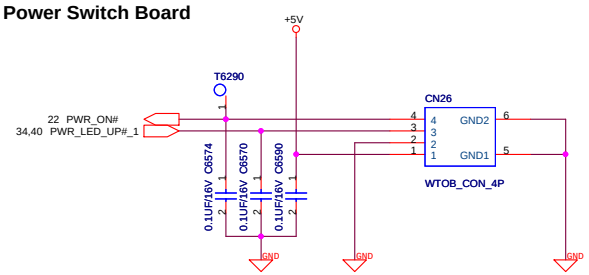
ASUSTeK COMPUTER INC	Title : ME	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 47 of 70	

LID_SW_Board

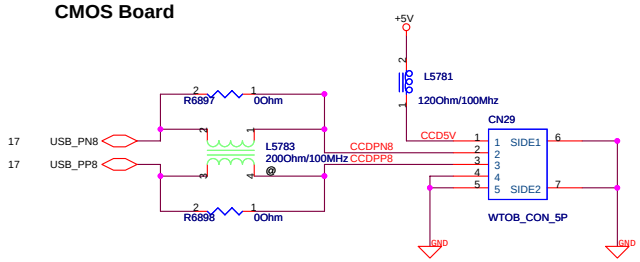



```
RFON_SW#(RF OFF)
----------------------------
right off --->  high
left  on  --->  low
```

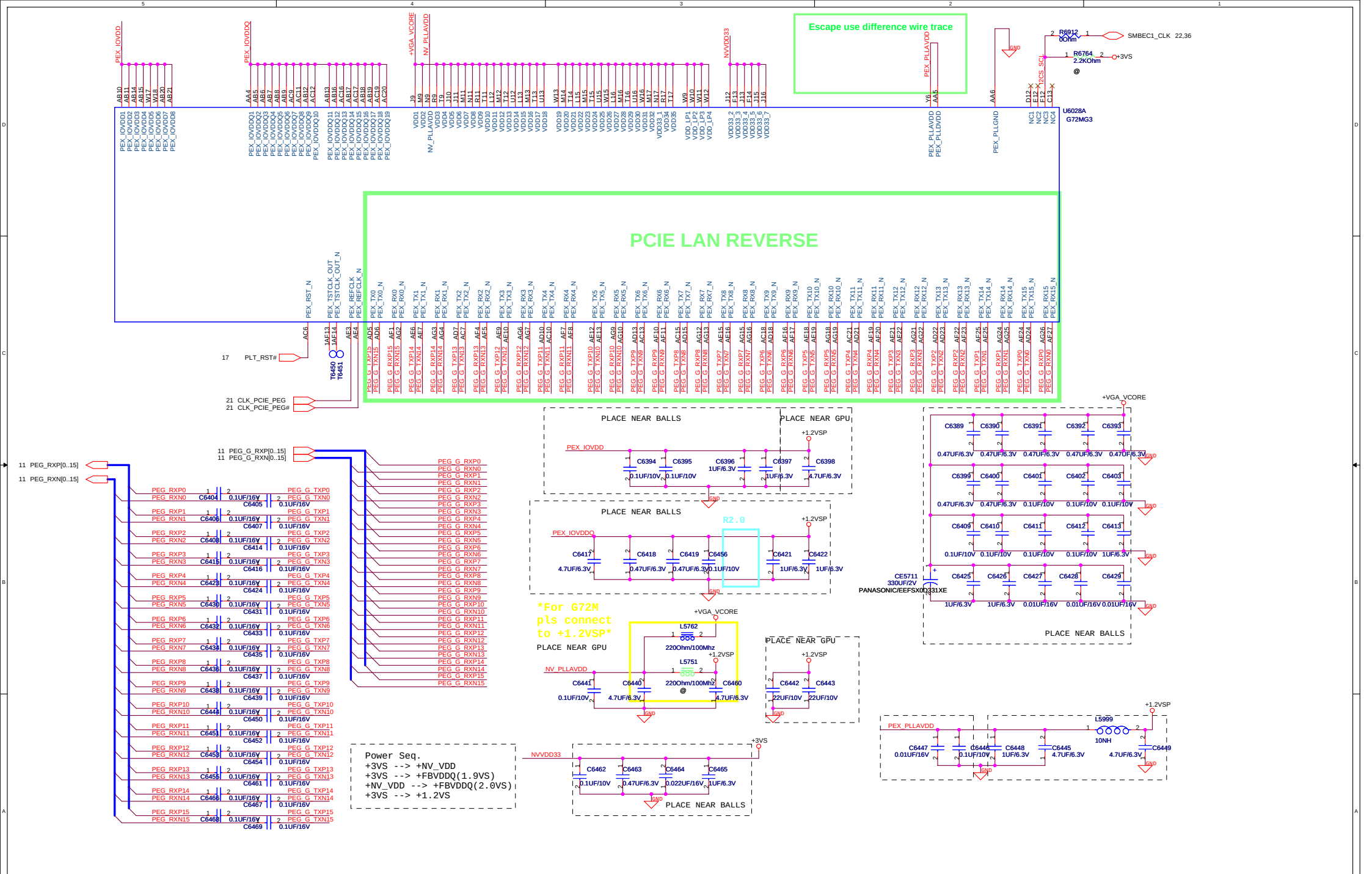
Power Switch Board

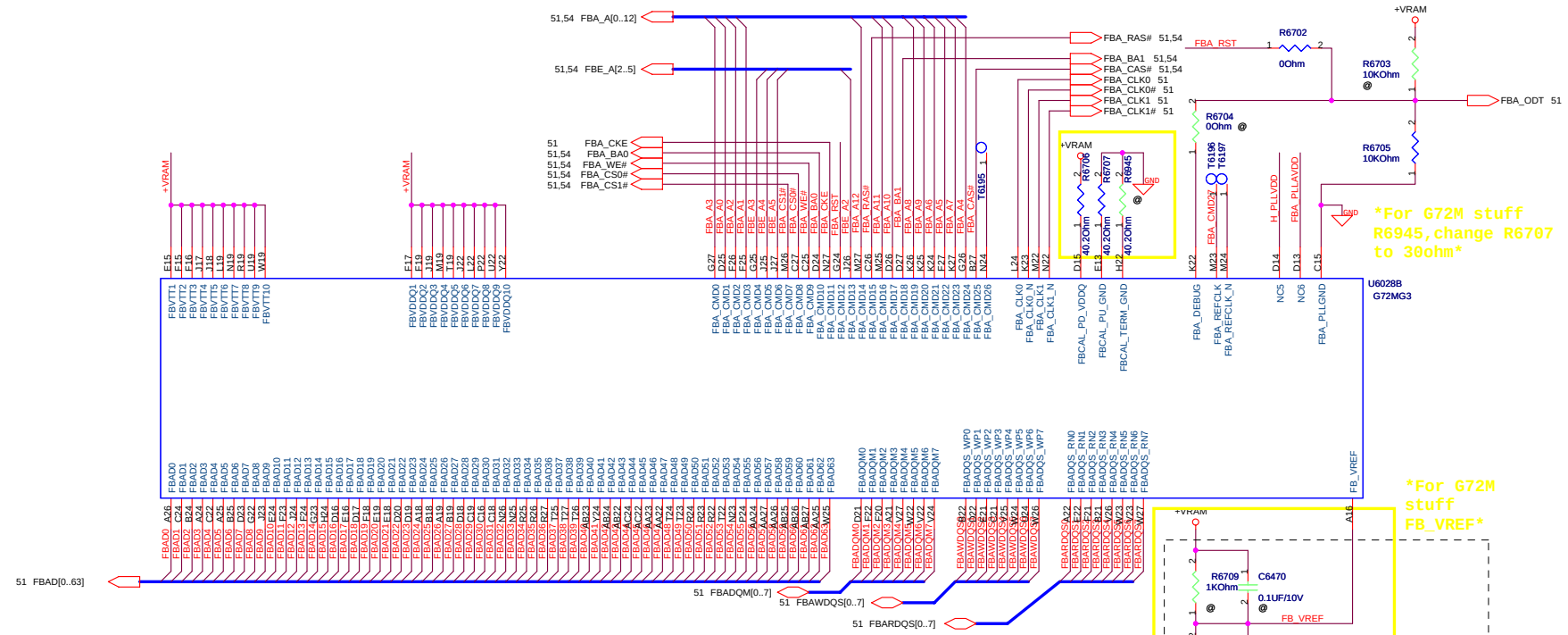


CMOS Board

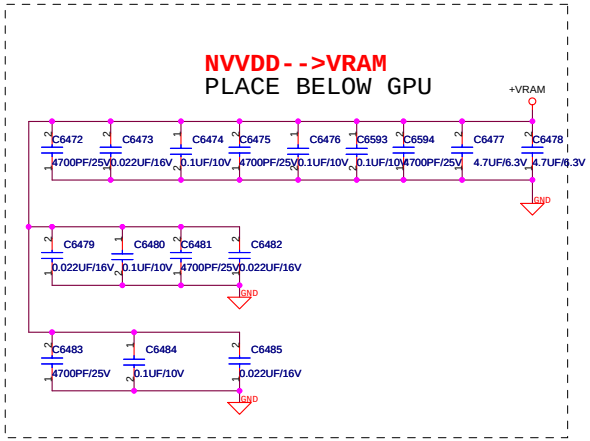


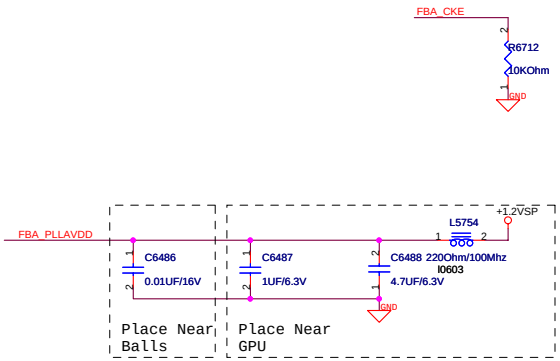
ASUSTeK COMPUTER INC	Title : Sub_Board	
	Engineer: Lorentz_Chang	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 48 of 70	

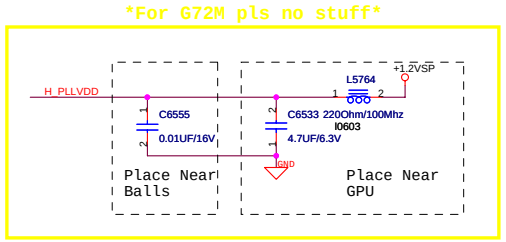

Escape use difference wire trace
PCIE LAN REVERSE
U6028A
G72MG3
PLACE NEAR BALLS
PLACE NEAR GPU
*For G72M
pls connect
to +1.2VSP*
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS
PROJECT: W7S
REVISION
2.0
DATE: Tuesday, August 21, 2007
SHEET 49 OF 70
DESCRIPTION: T76S
SCHEMATIC FILE NAME :
RELEASE DATE :
<OrgName>
DESIGN ENGINEER :



GDDR2 16x16 FBVDDQ 1.8V 84PIN

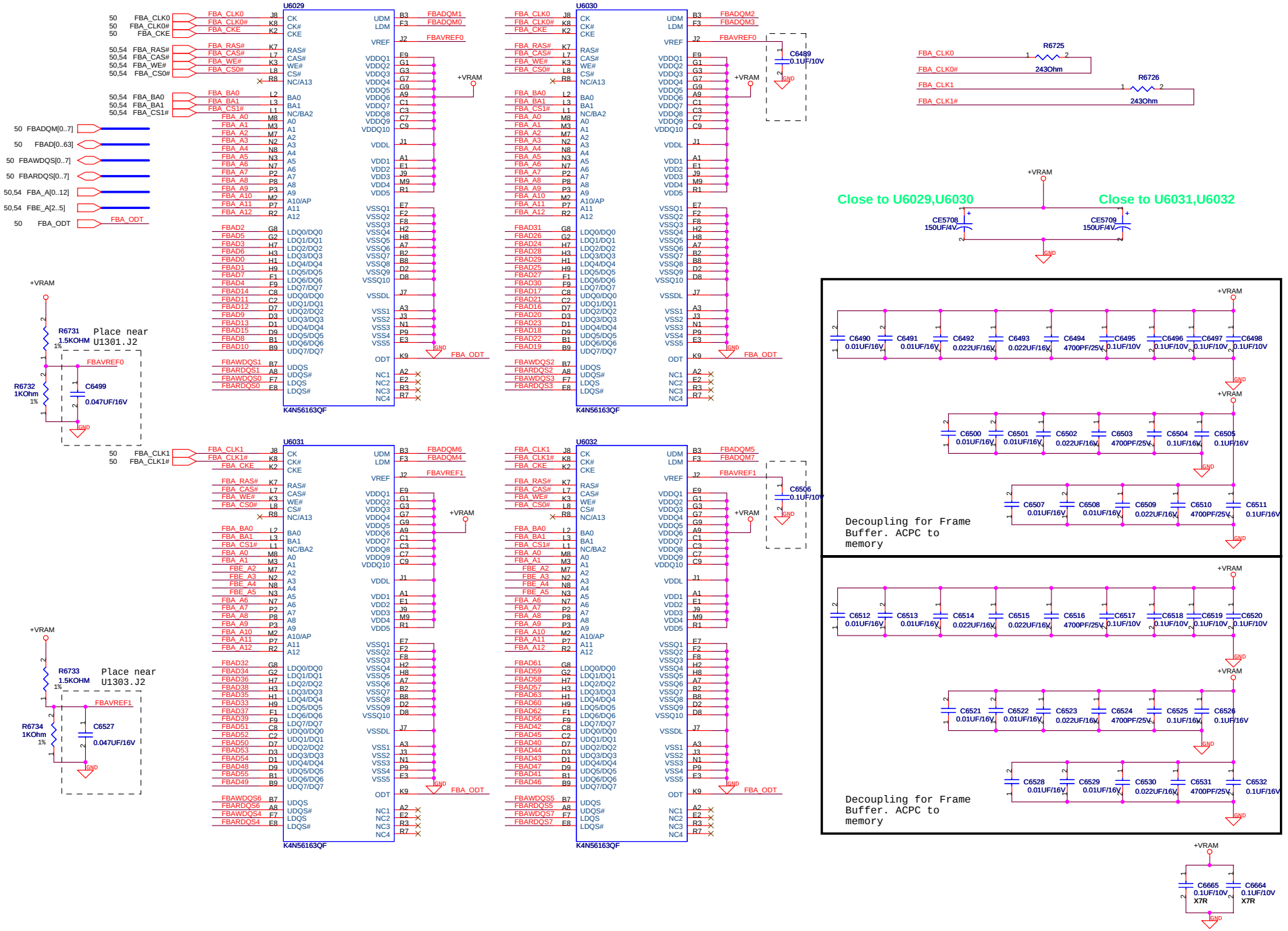






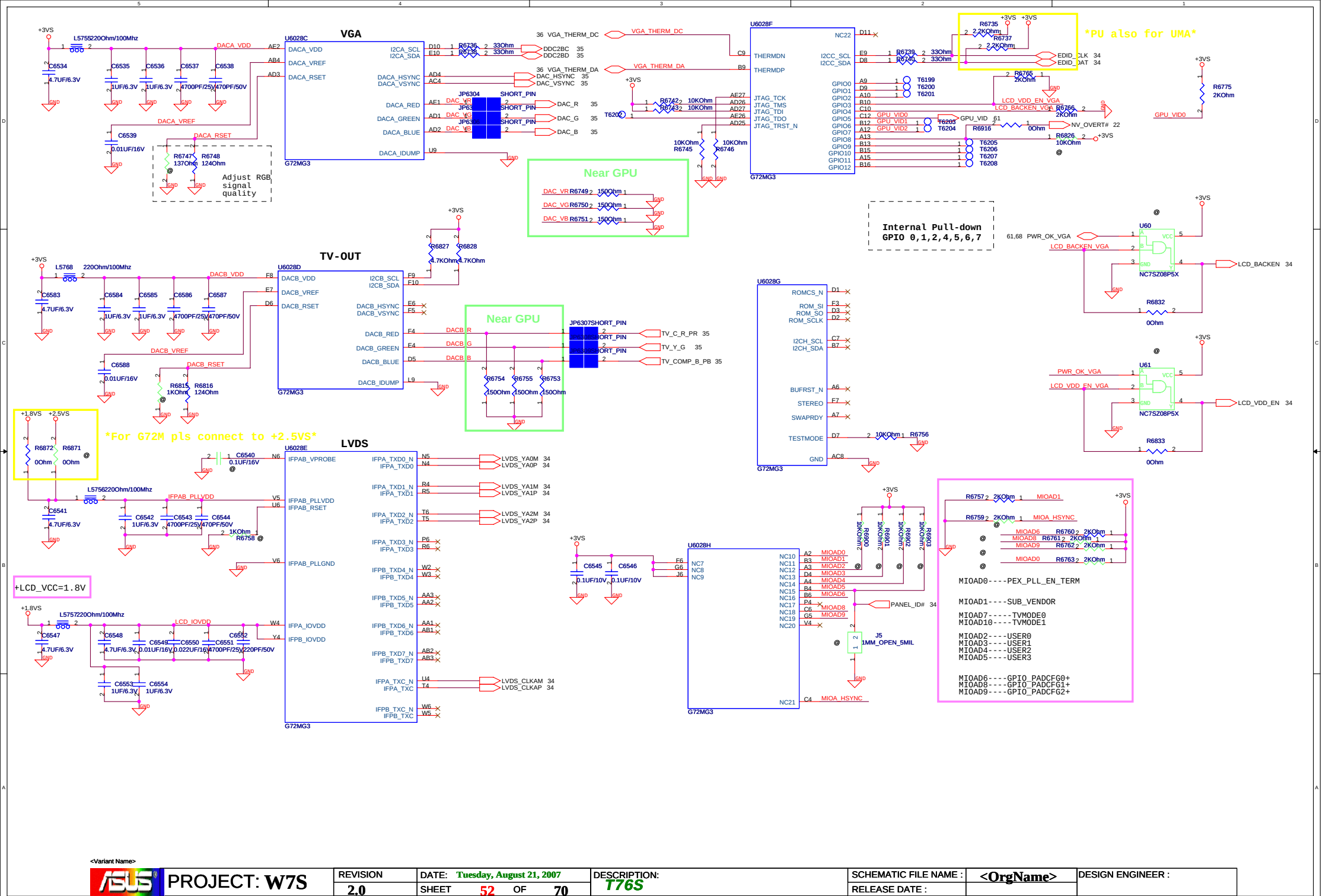
<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 50 OF 70		RELEASE DATE :	



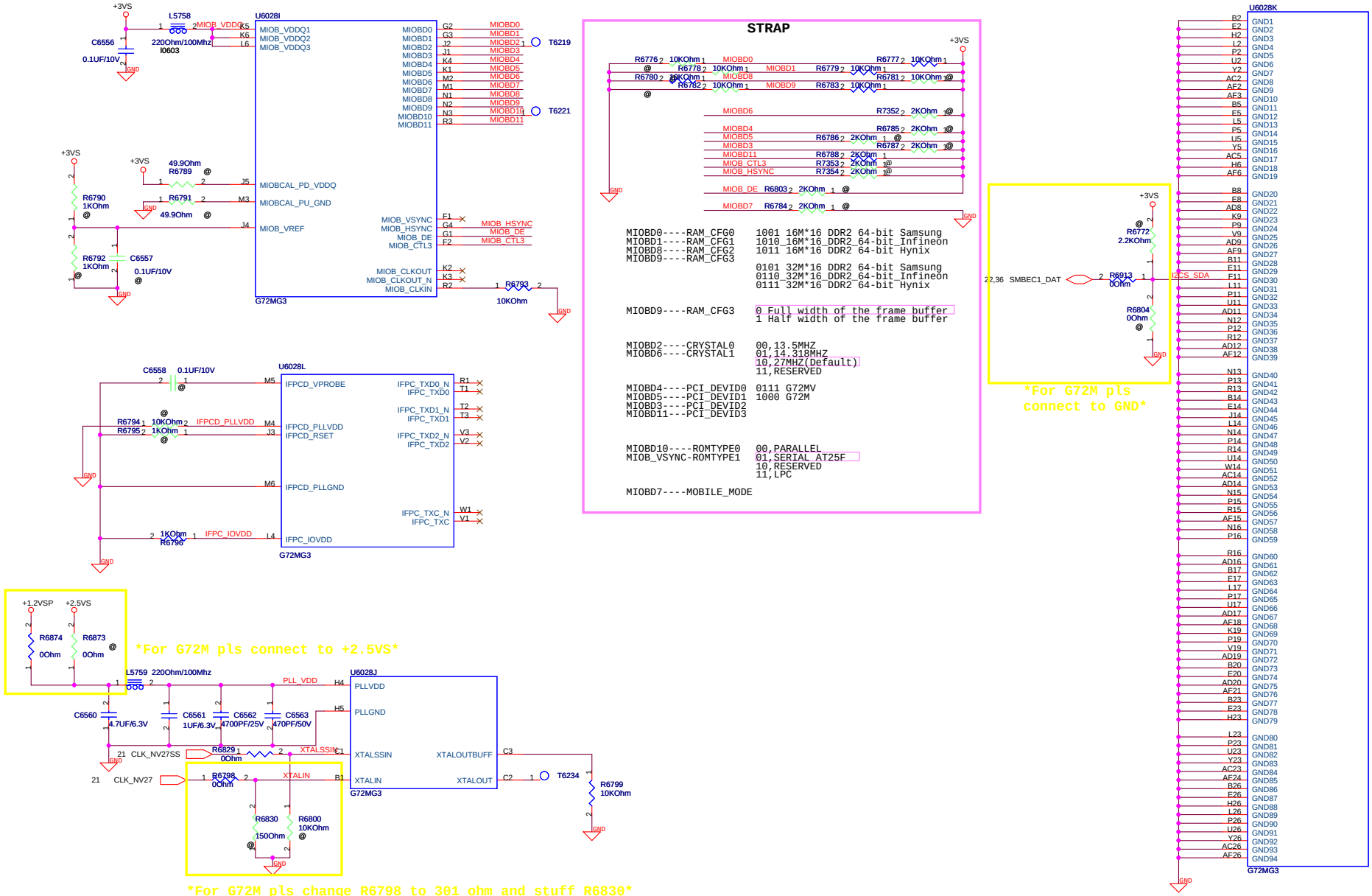
<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 51 OF 70		RELEASE DATE :	



<Variant Name>

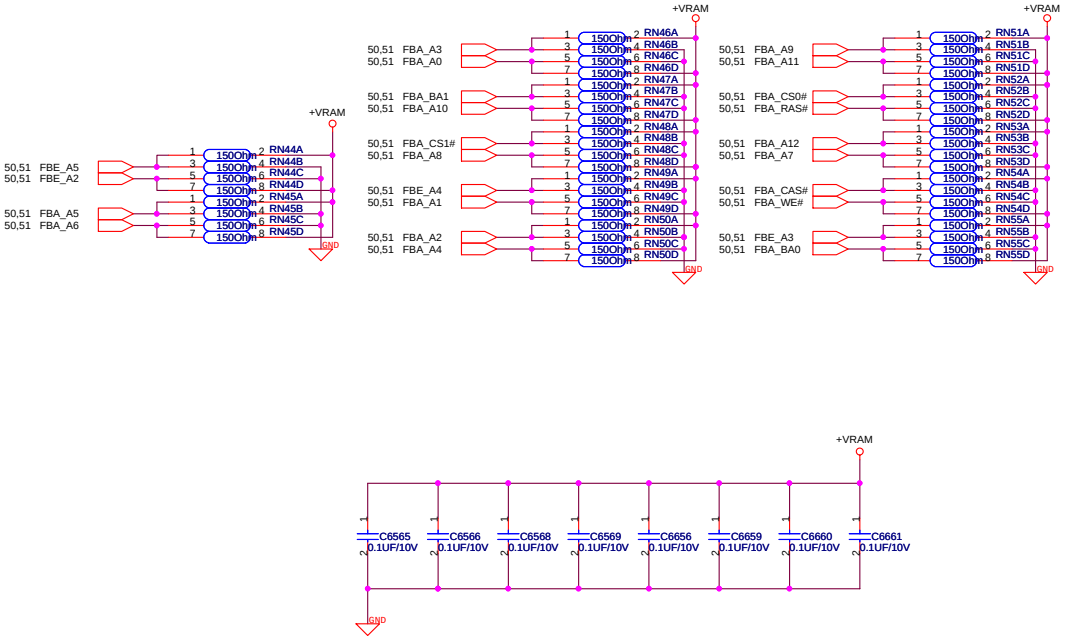
PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	SHEET 52 OF 70	DESCRIPTION: T76S	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
					RELEASE DATE :		



<Variant Name>

PROJECT: W7S	REVISION 2.0	DATE: Tuesday, August 21, 2007	DESCRIPTION: T76S	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 53 OF 70		RELEASE DATE :		

FBA CMD/ADDR Termination



<Variant Name>

ASUSTeK COMPUTER INC	Title : VGA-Terminator		
	Engineer:		
Size: Custom	Project Name: T76S		Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 54 of 70		

Rev	Date	Description
R1.0	2006/10/25	1. Initial release.
R1.1	2007/01/12	1. Change R6316 to 390 ohm page.21 2. Add R6662 and NET NV_OVERT# page.22 3. Del R6026 Add D6044,D6045,R6988 and R6990 page.28 4. Add R6989 page.29 5. Add R691 page.30 6. Add R6415 page.39 7. Add R6471 and Q6475 page.41 8. Add R6912 page.49 9. Change R6731,R6733 to 1.5Kohm and R6725, R6726 to 243ohm page.51 10. Add R6916 page.52 11. Add R6913 page.53
R2.0	2007/03/14	1. Add R6805 page.18 2. Change R6316 to 270 ohm page.21 3. Add R6628 page.28 4. Add R7381,Q6487 page.32 5. Change Q6483,Q6484,Q6485 to ESD protect device page.32 6. Change R6987 to 0 ohm page.35 7. Change R6859 pull high to +3VA page.36 8. Del C6595 page.49

Rev	Date	Description

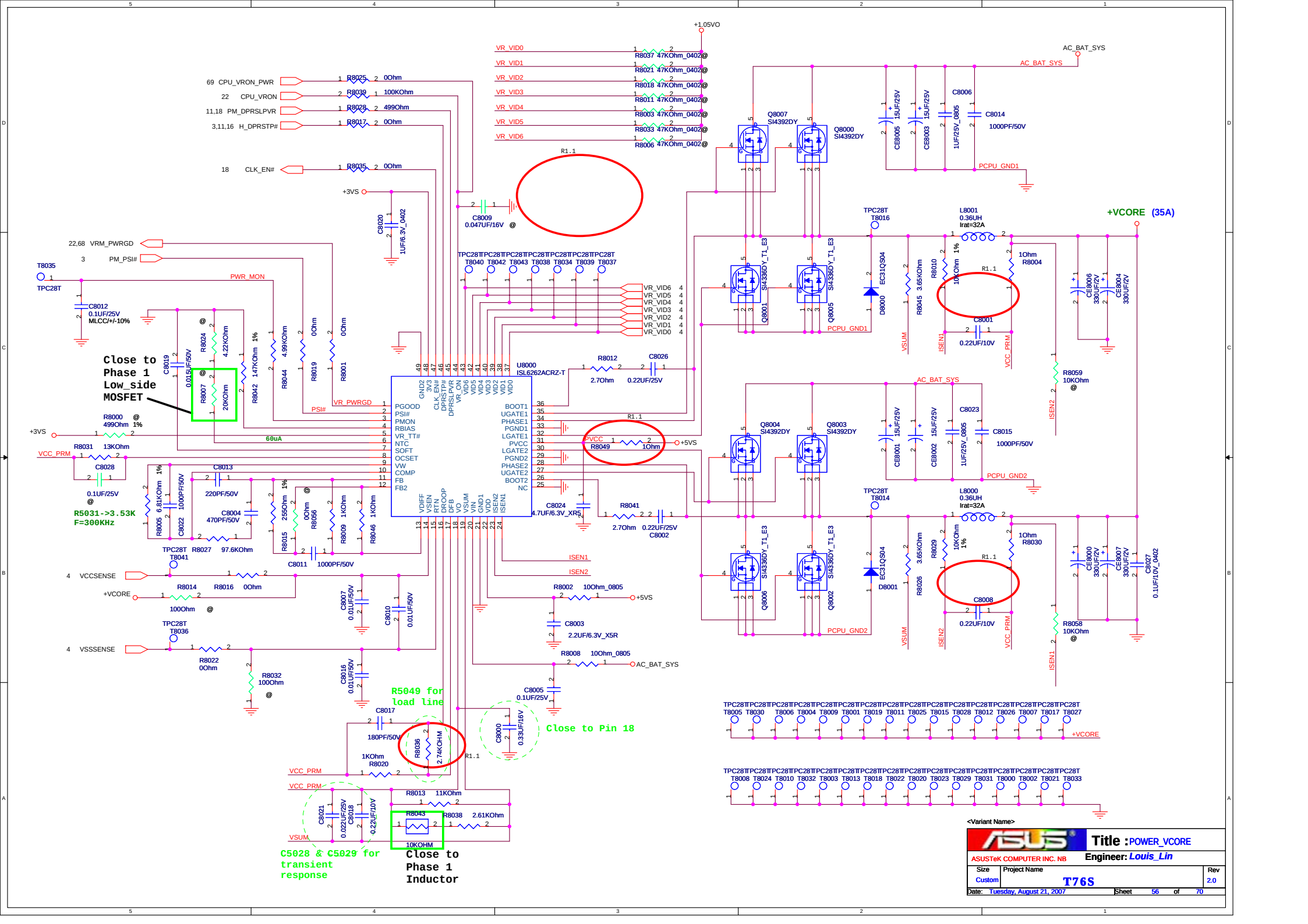
ASUSTeK COMPUTER INC

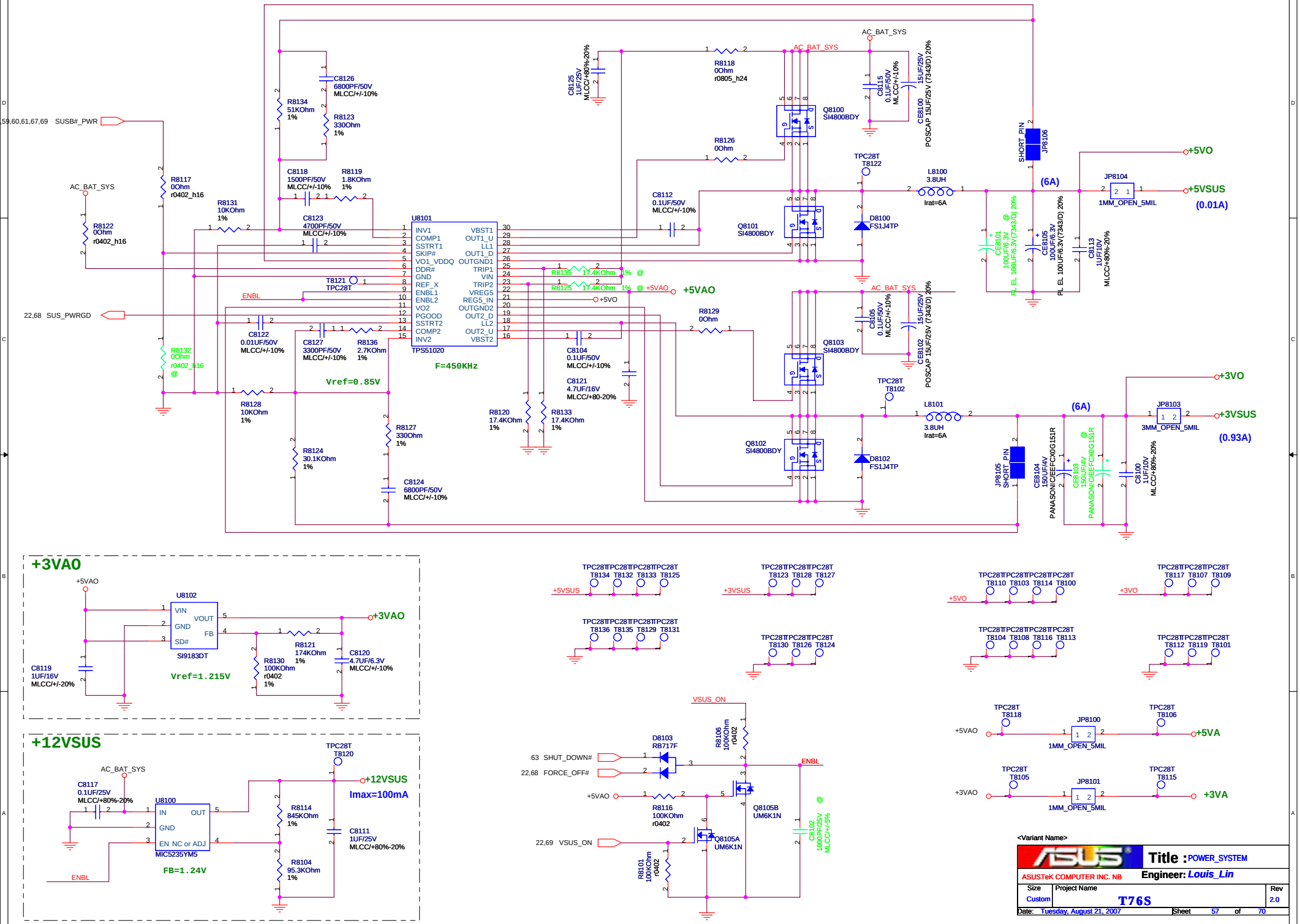
Title : History

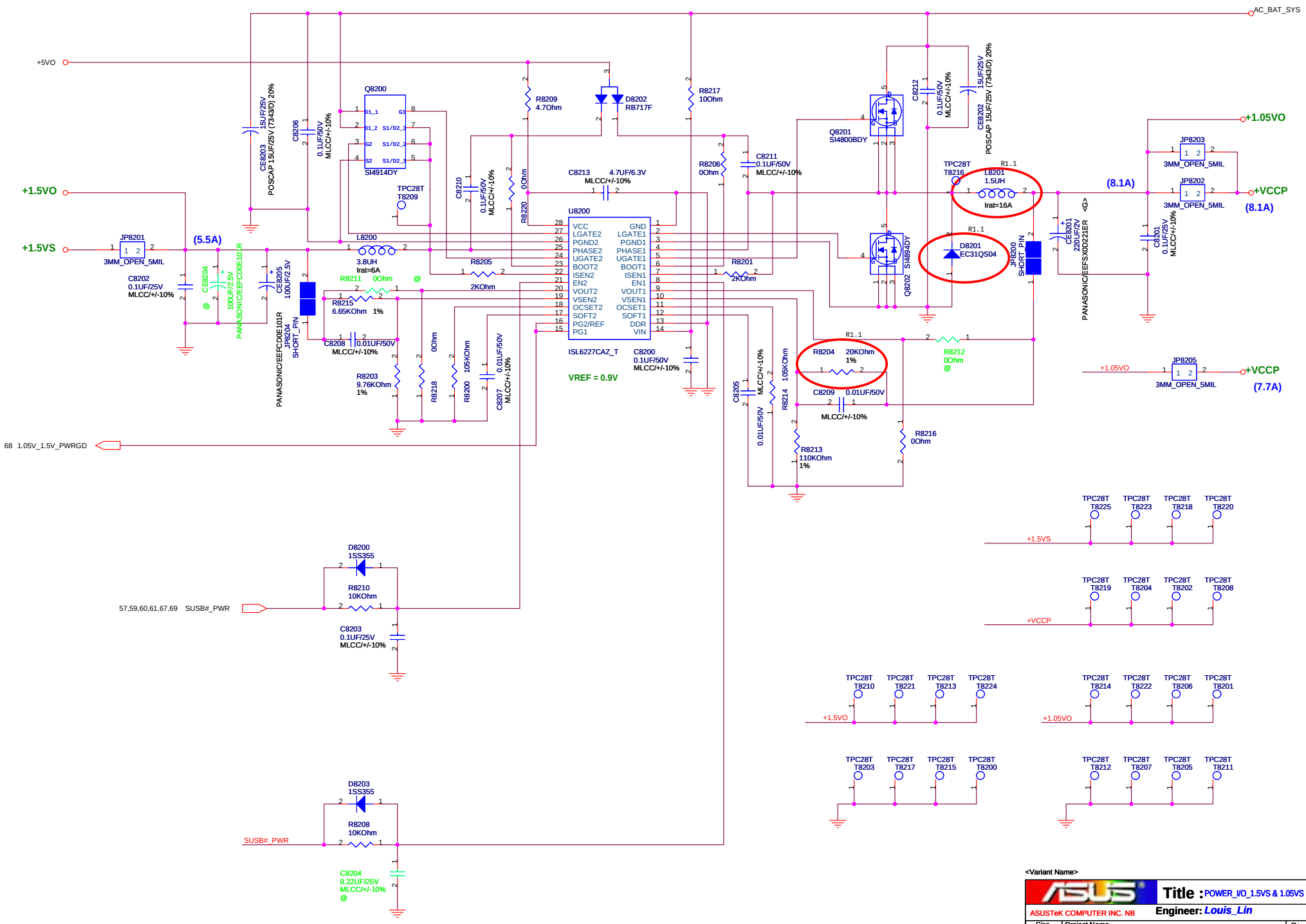
Engineer: Lorentz_Chang

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 55 of 70


+VCORE (35A)
U8000
ISL6262ACRZ-T
Close to Phase 1 Low_side MOSFET
R5031->3.53K
F=300KHz
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 56 of 70


U8101
TPS51020
F=450KHz
Vref=0.85V
+5VAO
+5VO
+5VSUS
(0.01A)
+3VO
+3VSUS
(0.93A)
(6A)
AC_BAT_SYS
SUSB#_PWR
SUS_PWRGD
ENBL
+3VA0
U8102
SI9183DT
Vref=1.215V
+3VAO
+12VSUS
Imax=100mA
U8100
MIC5235YM5
FB=1.24V
VSUS_ON
SHUT_DOWN#
FORCE_OFF#
+5VA
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Louis_Lin
Size Custom
Project Name T76S
Rev 2.0
Date: Tuesday, August 21, 2007
Sheet 57 of 70



<Variant Name>

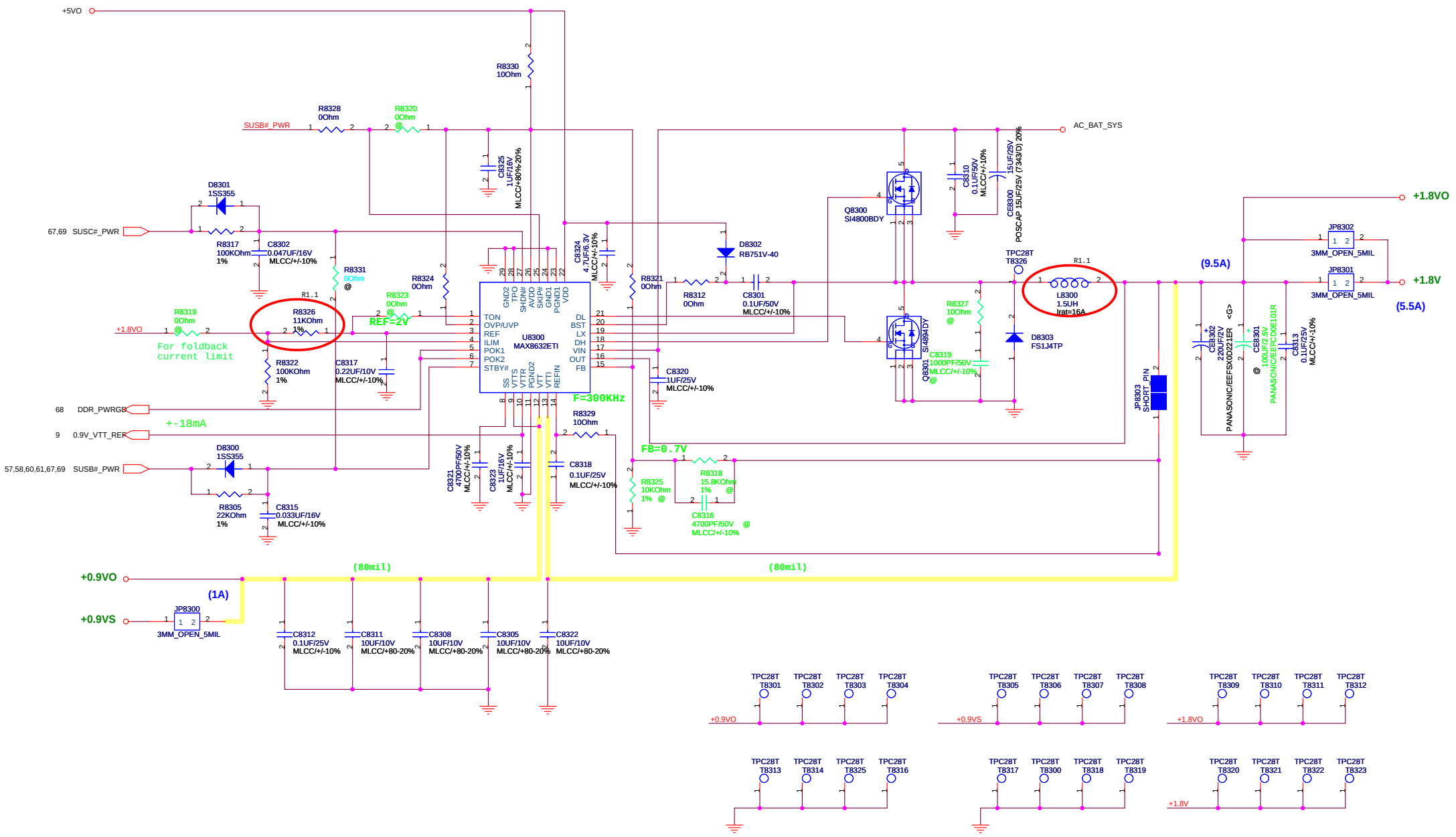
ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_1.5VS & 1.05VS

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

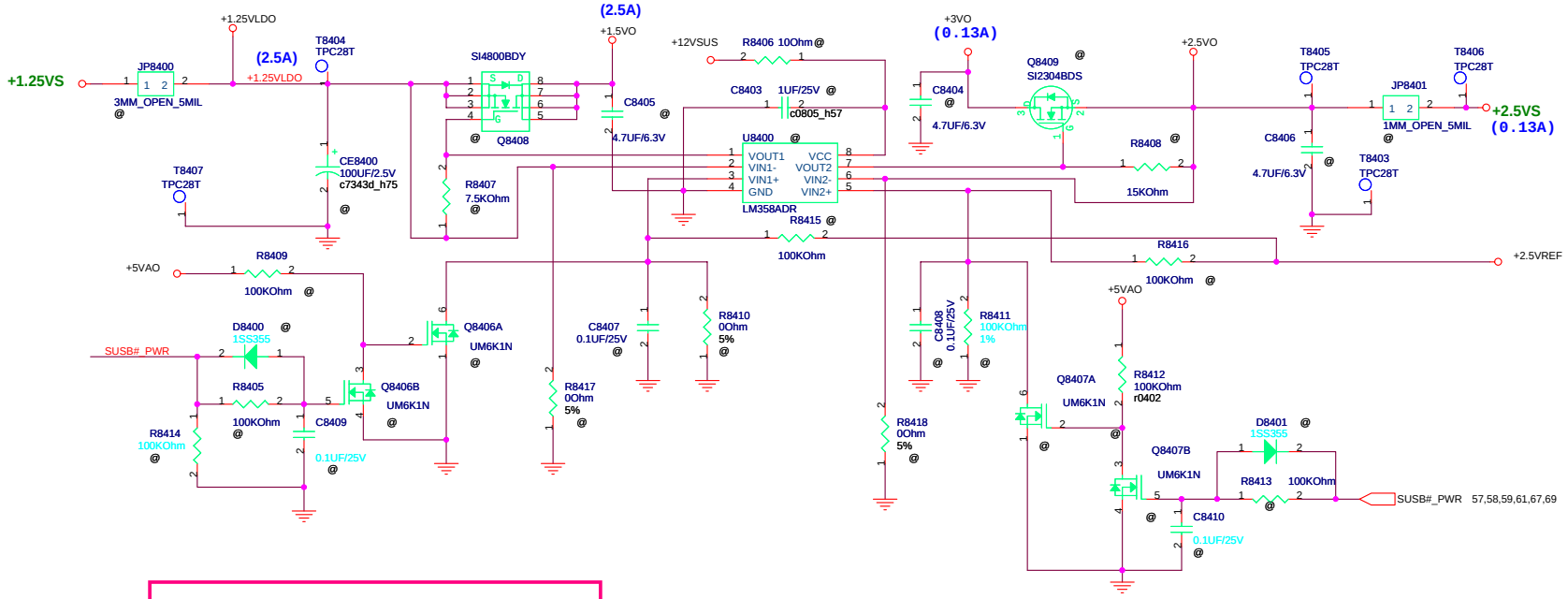
Date: Tuesday, August 21, 2007 Sheet 58 of 70



<Variant Name>

ASUS	Title : POWER_I/O_DDR & VTT	
ASUSTeK COMPUTER INC. NB	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 59 of 70	

+1.25VS & +2.5VS



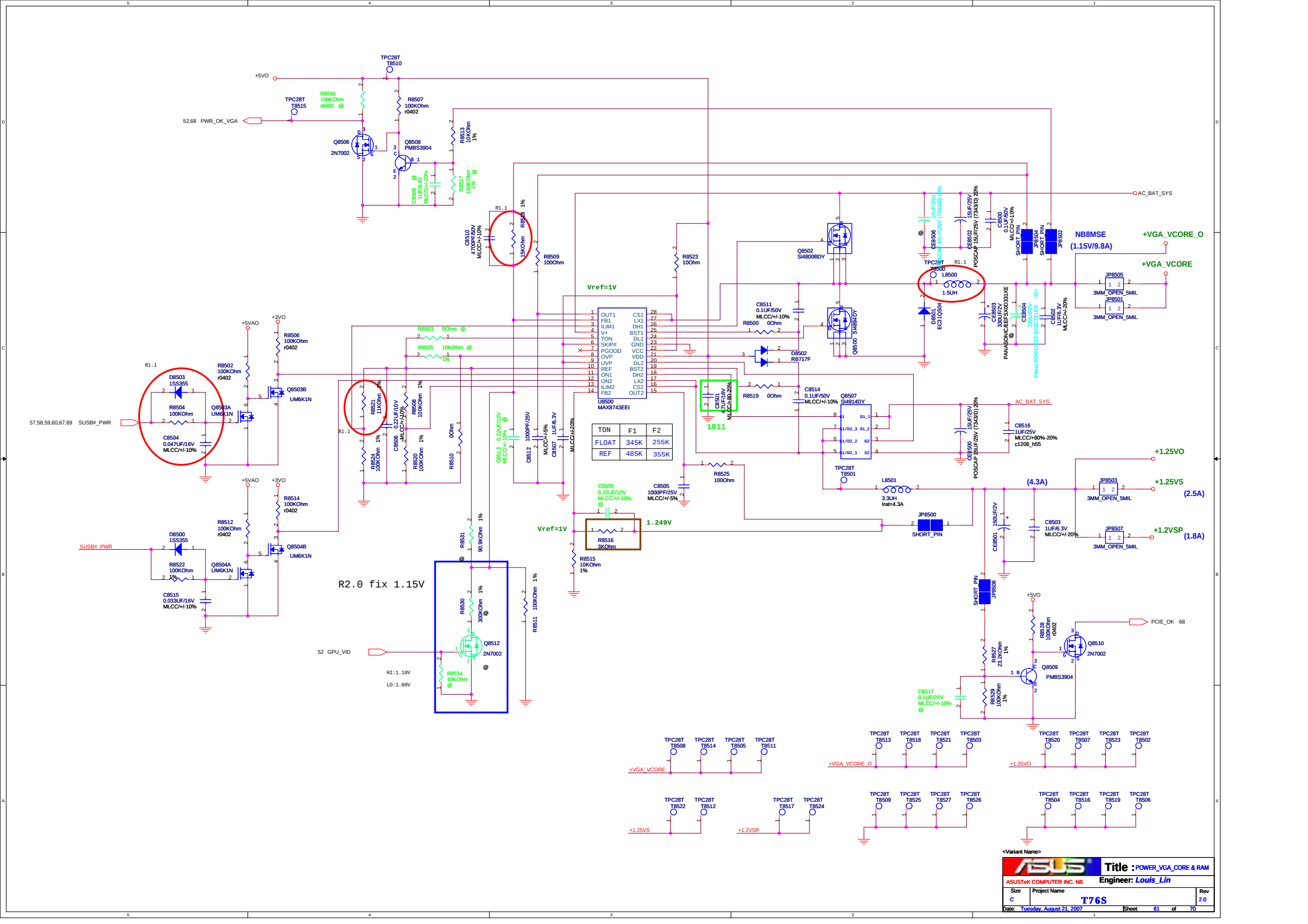
UMA Enable +1.25VS
R8417 UNMOUNT, R8410 100K 10G212100314010

Discrete VGA Disable +1.25VS
R8417 MOUNT, R8410 0 ohm 10G212000004030
And other UNMOUNT.

R8414,D8400,C8409 Always Keep UNMOUNT

<Variant Name>

ASUS	Title : POWER_I/O_ +1.25VS&+2.5VS	
ASUSTeK COMPUTER INC. NB	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 60 of 70	

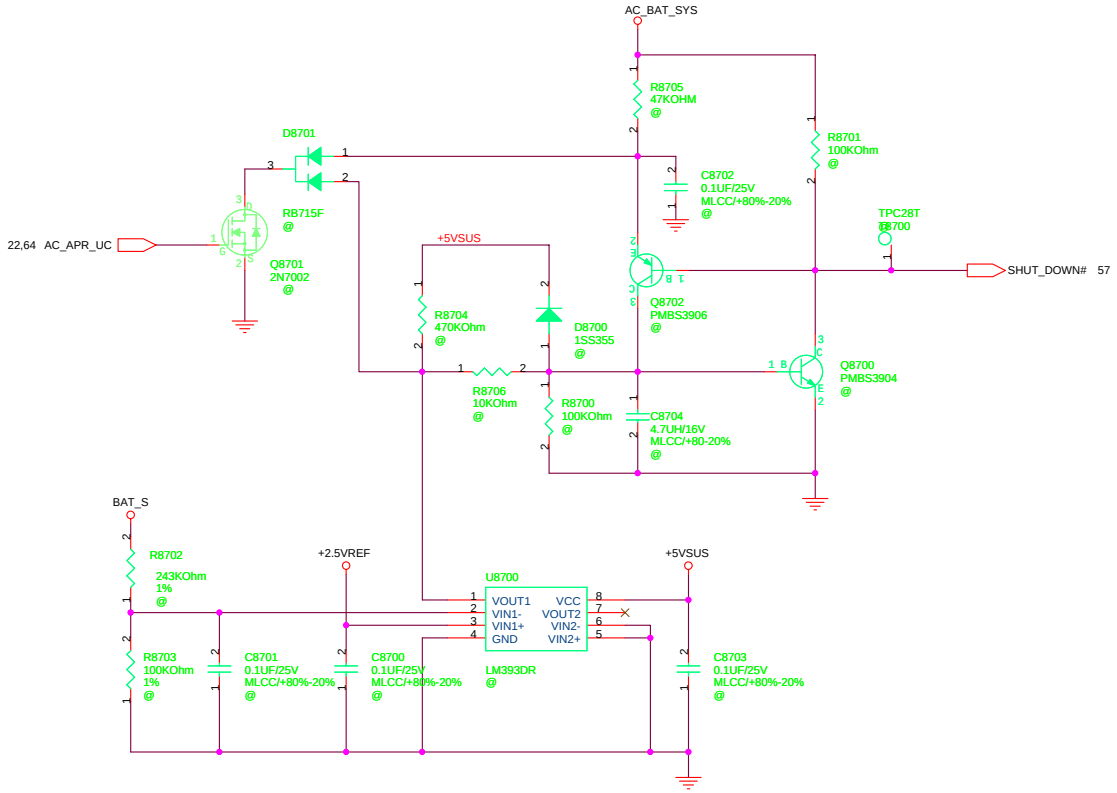


TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

<Variant Name>

Title : N/A		
ASUSTeK COMPUTER INC. NB	Engineer: *Louis_Lin*	
Size: B	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 62 of 70	

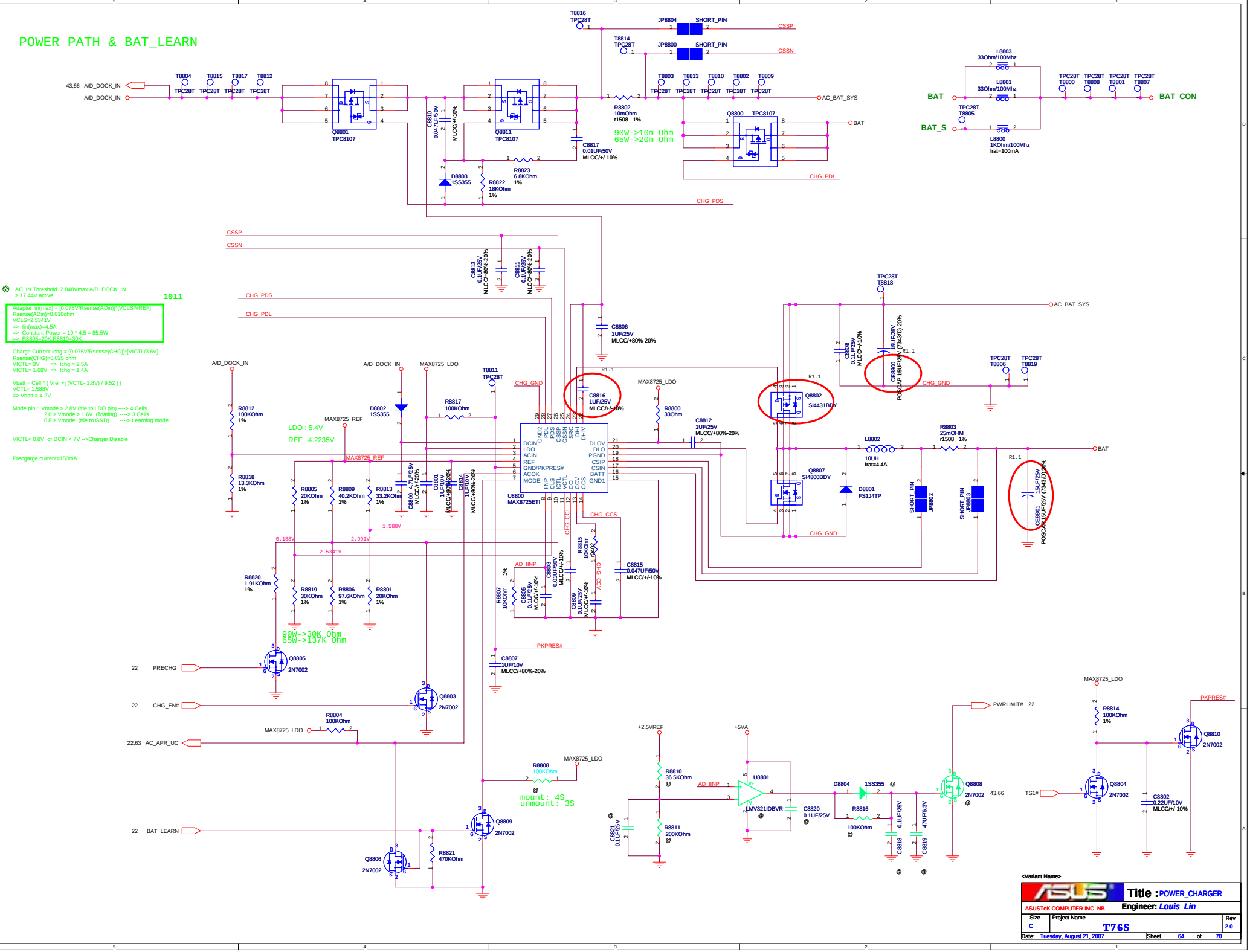
PIC only



<Variant Name>

ASUS	Title : POWER_SHUTDOWN#	
ASUSTeK COMPUTER INC. NB	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 63 of 70	

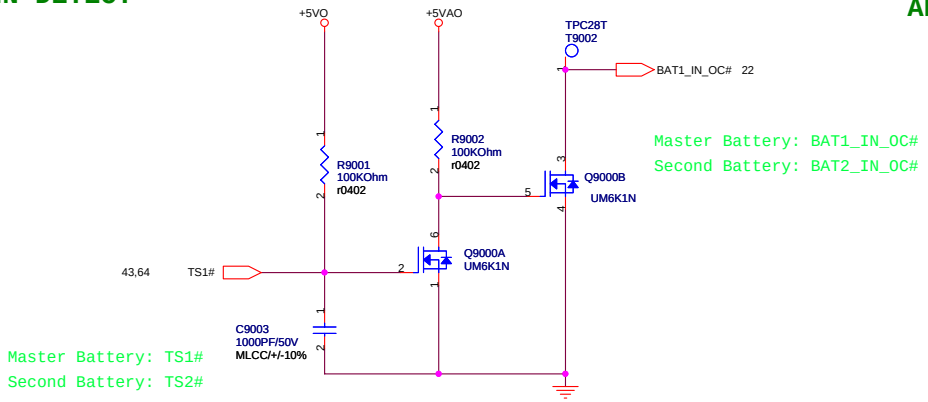
POWER PATH & BAT_LEARN



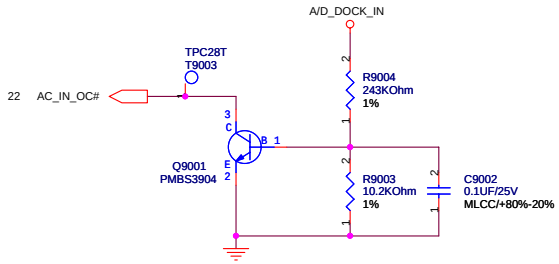
<Variant Name>

Title : N/A		
ASUSTeK COMPUTER INC. NB	Engineer: *Louis_Lin*	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 65 of 70	

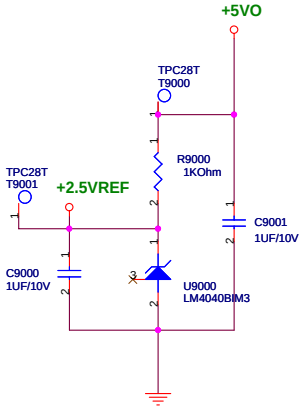
BATTERY IN DETECT



ADAPTER IN DETECT

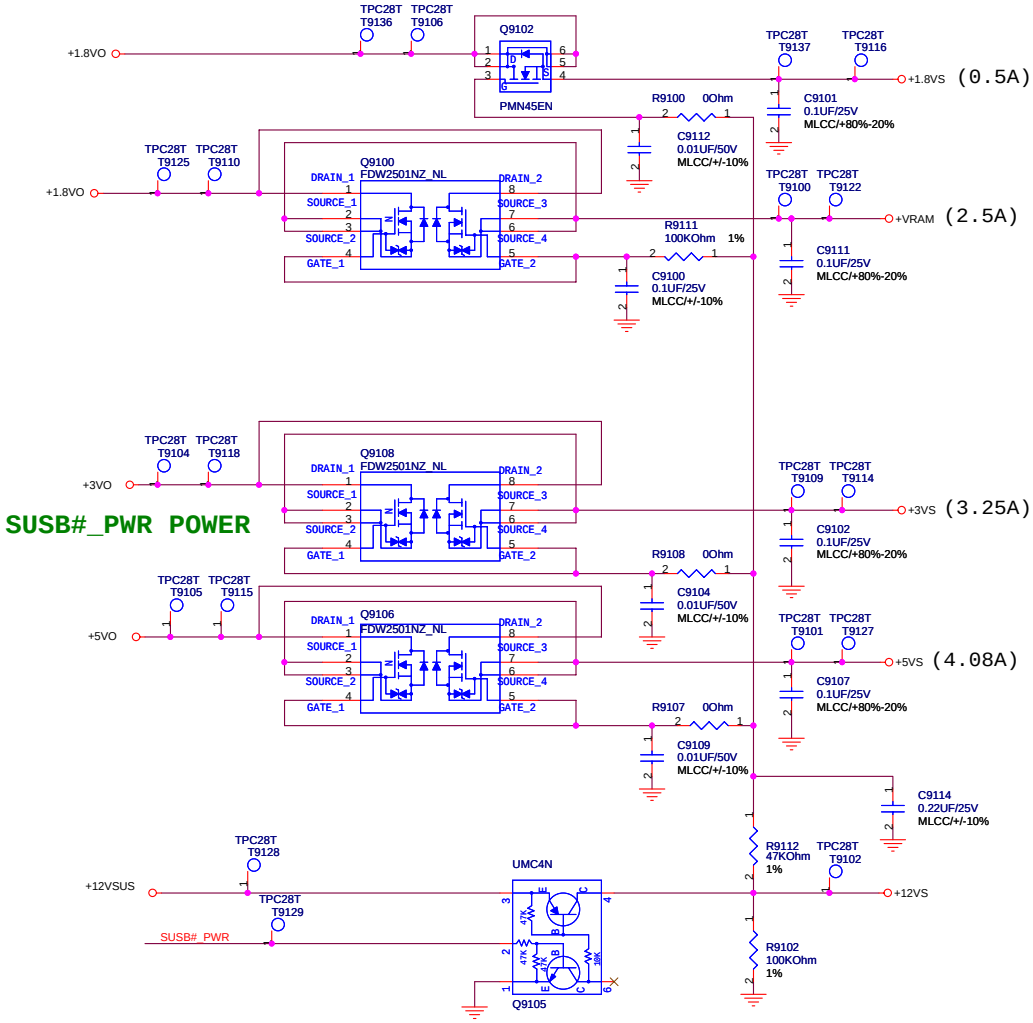


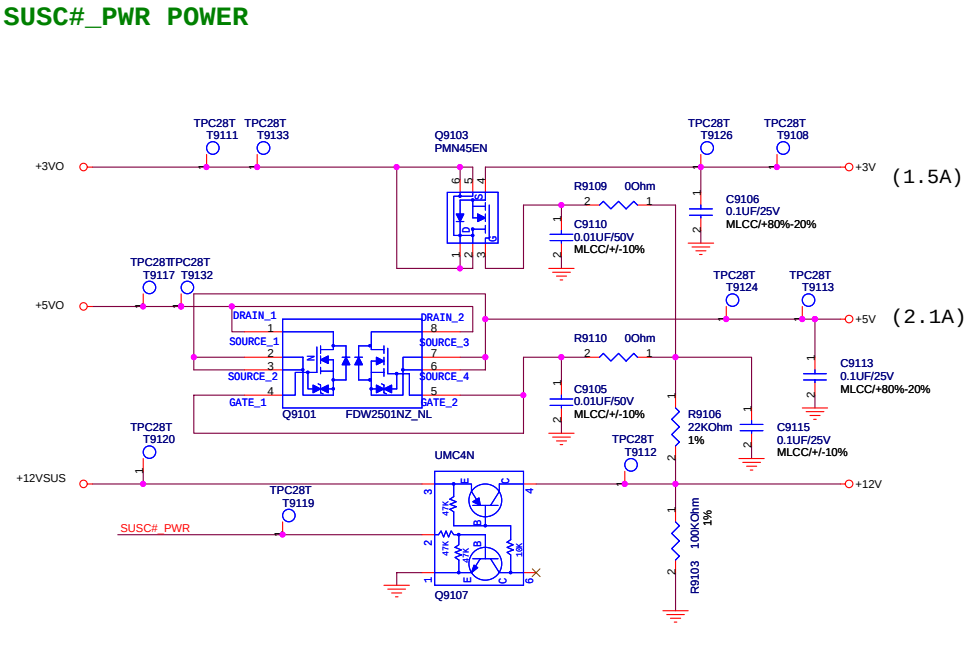
+2.5VREF

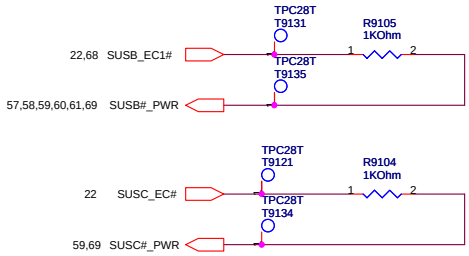


<Variant Name>

Title : POWER_DETECT		
ASUSTeK COMPUTER INC. NB	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 66 of 70	







<Variant Name>

Title : POWER_LOAD SWITCH

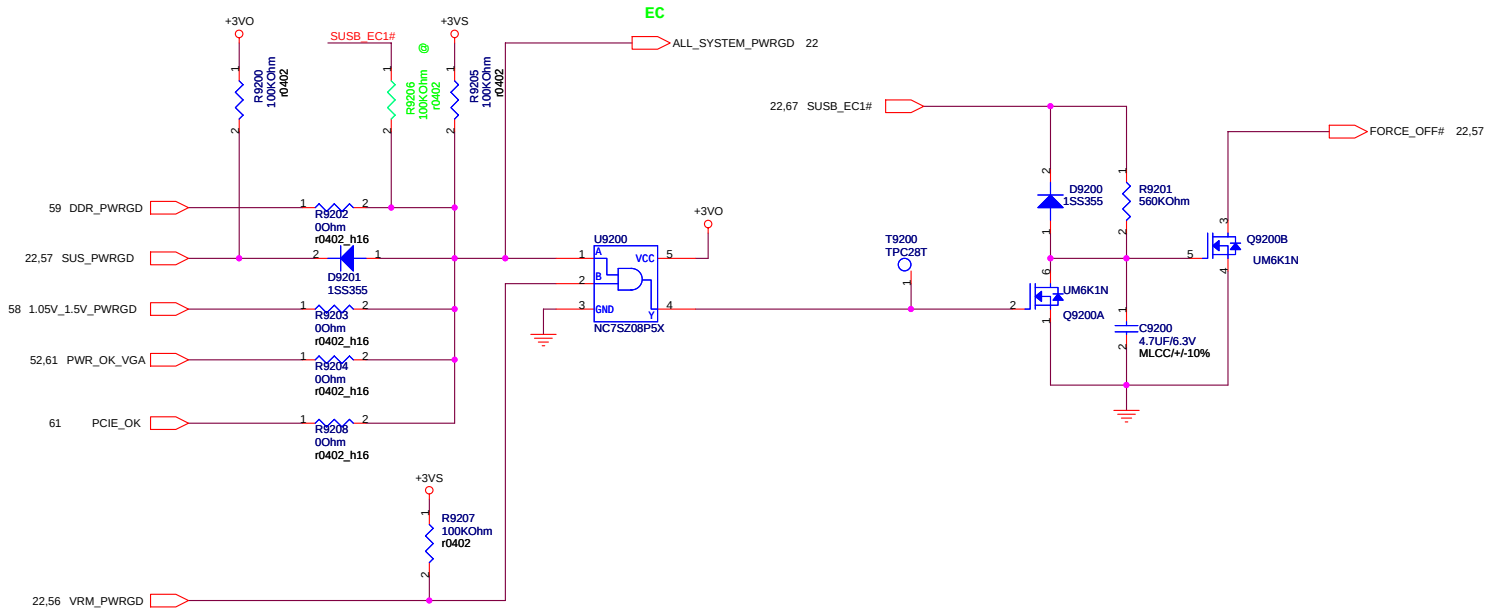
ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

Date: Tuesday, August 21, 2007 Sheet 67 of 70

POWER GOOD DETECTER

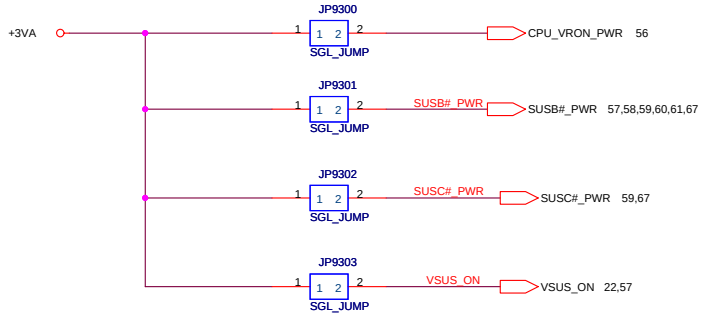


<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Louis_Lin	
Size: Custom	Project Name: T76S	Rev: 2.0
Date: Tuesday, August 21, 2007	Sheet 68 of 70	

AC_BAT_SYS	AC_BAT_SYS	34,56,57,58,59,61,63,64
BAT	BAT	64
BAT_CON	BAT_CON	43,64
+2.5VREF	+2.5VREF	60,63,64,66
+3VA	+3VA	16,22,43,48,57
+5VAO	+5VAO	57,60,61,66
+5VO	+5VO	57,58,59,61,66,67
+5VSUS	+5VSUS	19,57,63
+5V	+5V	9,26,28,38,40,41,48,67
+5VS	+5VS	19,20,23,26,28,29,35,36,37,40,41,56,67
+3VO	+3VO	57,60,61,67,68
+3VSUS	+3VSUS	17,18,19,22,24,28,57
+3V	+3V	17,25,33,37,39,41,44,67
+3VS	+3VS	3,8,11,14,15,16,18,19,20,21,22,24,26,28,30,31,32,33,34,35,36,37,39,41,42,45,49,52,53,56,67,68
+12VSUS	+12VSUS	57,60,67
+12V	+12V	18,28,32,67
+12VS	+12VS	45,67
+1.8VO	+1.8VO	59,67
+1.8V	+1.8V	6,7,8,9,11,13,14,41,59
+1.8VS	+1.8VS	52,67
+0.9VS	+0.9VS	9,59
+0.9VO	+0.9VO	59
+1.05VO	+1.05VO	56,58
+VCCP	+VCCP	3,4,5,10,11,13,14,16,19,21,41,58
+1.5VO	+1.5VO	58,60
+1.5VS	+1.5VS	4,14,16,17,19,33,39,41,58
+2.5VO	+2.5VO	60
+2.5VS	+2.5VS	41,52,53,60
+VCORE	+VCORE	4,5,56
+VGA_VCORE	+VGA_VCORE	49,61
+VRAM	+VRAM	50,51,54,67
+1.2VSP	+1.2VSP	41,49,50,53,61
+1.25VS	+1.25VS	11,14,19,60,61

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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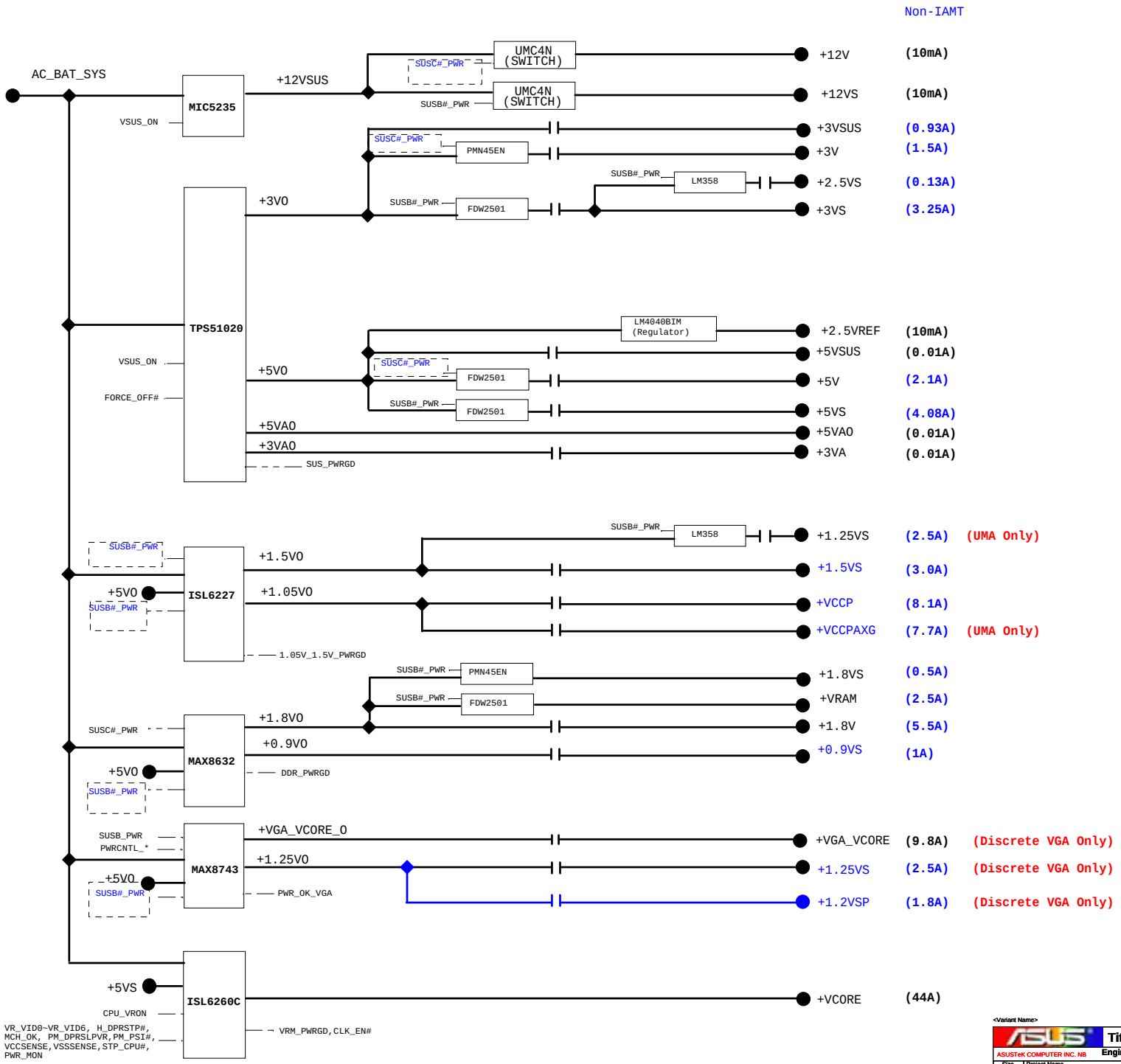

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Louis_Lin

Size	Project Name	Rev
Custom	T76S	2.0

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