PROJECT U5A

Revision History

R1.0	SR	2005/05/17
R1.1	ER	2005/08/04
R2.0	PR	2005/10/07

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK,SMBDA	ICH6-M	10h
		ADT7473(Thermal)	2Eh
		ICS954213(Clock Genertor)	D2h
		DDR2 SO-DIMM	A0h

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+*VALWAYS	+*V	+*VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Sort OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCI Devices

Bus#	Device#	Function#	REQ/GNT#	IDSEL	APIC Interrupts	Device Function
Bus0	Device00	Function0				Intel 915GM Host Bridge / DRAM Controller
Bus0	Device01	Function0				Intel 915GM Virtual PCI to PCI
Bus0	Device02	Function0				Intel 915GM GMCH Integrated Graphics Device
Bus0	Device27	Function0				Azalia Controller
Bus0	Device28	Function0				PCI Express Port1
Bus0	Device28	Function1				PCI Express Port2
Bus0	Device28	Function2				PCI Express Port3
Bus0	Device28	Function3				PCI Express Port4
Bus0	Device29	Function0			A#	Intel UHCI USB Controller
Bus0	Device29	Function1			D#	Intel UHCI USB Controller
Bus0	Device29	Function2			C#	Intel UHCI USB Controller
Bus0	Device29	Function3			A#	Intel UHCI USB Controller
Bus0	Device29	Function7			H#	Intel EHCI USB Controller
Bus0	Device30	Function0				PCI to PCI Bridge
Bus0	Device30	Function2			B#	Intel Audio Controller
Bus0	Device30	Function3			B#	Intel Modem Controller
Bus0	Device31	Function0				Intel PCI-to-LPC Bridge
Bus0	Device31	Function1			C#	Intel IDE Controller
Bus0	Device31	Function2				SATA Controller
Bus1	Device03	Function0	2	AD19	F#	CardBus Bridge
Bus1	Device03	Function1	2	AD19	G#	IEEE 1394
Bus1	Device03	Function2	2	AD19	E#	SD Card Interface
Bus1	Device03	Function3	2	AD19	E#	Memory Stick Interface
Bus1	Device03	Function4	2	AD19	E#	xD Picture Card Interface
Bus1	Device04	Function0	1	AD20	E#	Ethernet Controller
Bus1	Device05	Function0	3	AD21	C#/D#	Mini PCI

ASUSTek COMPUTER INC

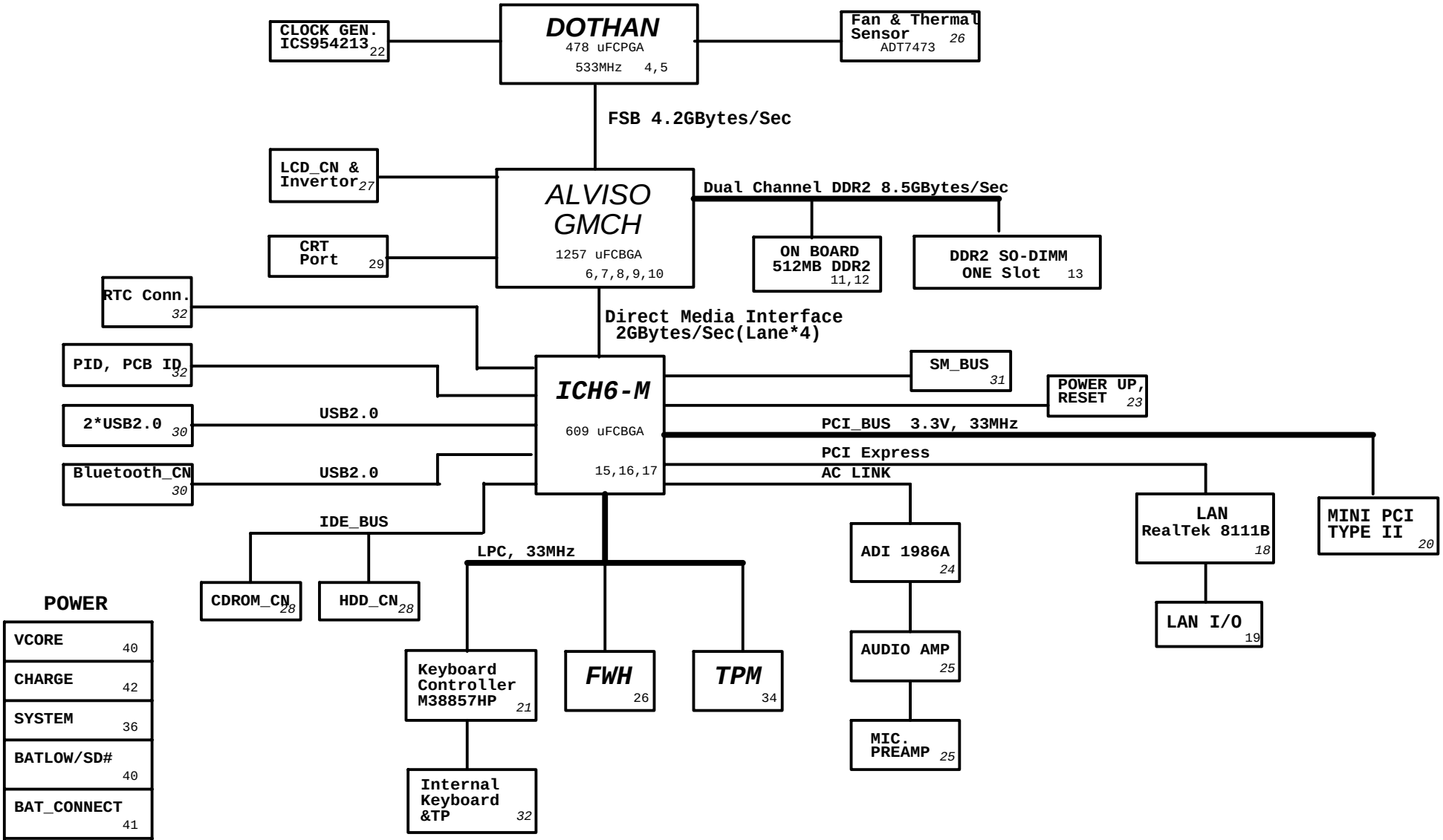
Project Name: U5A

Engineer: HF_Lin

Size: Custom | Title : Table of Contens | Rev: 2.0

Date: Tuesday, September 27, 2005 | Sheet 1 of 46

DOTHAN/ALVISO-GM BLOCK DIAGRAM



POWER

- VCORE 40
- CHARGE 42
- SYSTEM 36
- BATLOW/SD# 40
- BAT_CONNECT 41
- 1.8V 37
- 1.5VS & 1.05VS 38
- LOAD Switch 35

TOUCH PAD

TP SW TP CONN. | LED

AUDIO BOARD

HP JACK | MIC JACK | LEDs

IO SUB BD

MDC | R5C841 | DC JACK

INSTANT BD

PWR BUT. | LEDs | HALL Sensor

ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : BLOCK DIAGRAM	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 2 of 46	

M38857MB_GPIO	Use As	Signal Name	Describtion
P20	GPO	ANKEY_RSM	Anykey wakeup
P21			
P22	GPO	BAT_LEARN	Switch AC power on or off
P23	GPO	802_ON#	Notify wireless LED status change
P27	GPO	SCROLLOCK#_3	
P42	GPO		
P43	GPI	LID_RSM#	Notify LID switch status
P44	GPO	KBDCPURST_3Q	
P45	GPO	A20GATE_3Q	
P46	GPO	KBDSCI_3Q	Trigger EC's SCI event
P47	GPIO	CLKRUN#_3	
P50	GPI	BAT_LLOW#_OC	Battery low event
P51			
P52	GPO		
P53	GPO	BTPWRCL#	Control Bule Tooth on/off
P54	GPI	BAT_TYPE_3S1P#	Show battery type
P55	GPI	BAT_IN#_OC	Battery IN/OUT event
P56	GPO	CODEC_SHDN#	Switch CODEC power on/off
P57	GPO	TPD_LED_OFF#	Switch TPD LED on/off
P67	GPO	WIRELESS_LAN_ON#	Control wireless LAN module on/off
P66	GPI	BAT_SAVING#	
P65			
P64	GPI	ACIN_OC	AC IN / OUT event
P63	GPO		
P62	GPI	CHG_FULL_OC	End of charger status
P61			
P60			
P77	GPO	SMC_BAT	
P76	GPIO	SMD_BAT	
P26	GPI	KBNUM#_3	Notify NUM key status change
P25	GPI	KBCAP#_3	Notify CAP key status change
P24	GPO	PCIRST#_GATE	Block PCIRST# during S3 resume
P40			

ICH6_GPIO	Use As	Signal Name
GPI7	GPI	MEMORY_FREQ
GPI8	GPI	EXTSMI#
GPI11	GPI	LID_RSM#
GPI12	GPI	KB_SCI#
GPI13	GPI	
GPO18	GPO	STP_PCI#
GPO19	GPO	PWRLED_1HZ
GPO21		
GPO23	GPO	FWH_WP#
GPIO25	GPO	CB_SD#
GPIO27	GPI	PCB_ID0
GPIO28	GPI	PCB_ID1
GPI40	GPI	PANEL__ID0
GPI41	GPI	PANEL__ID1

ASUSTek COMPUTER INC

Project Name: U5A

Engineer: HF_Lin

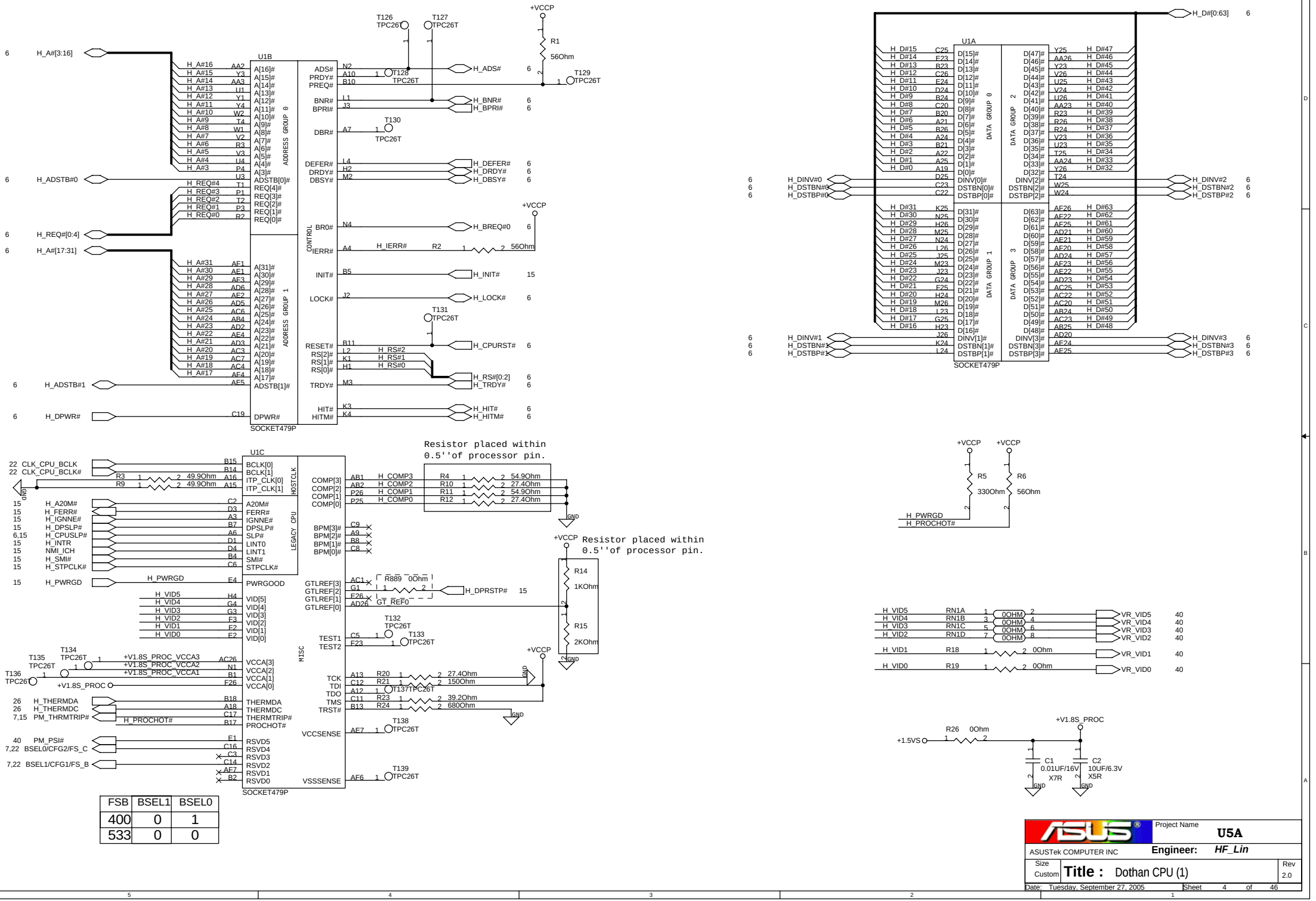
Size: Custom

Title : SYSTEM INFORMATION

Rev: 2.0

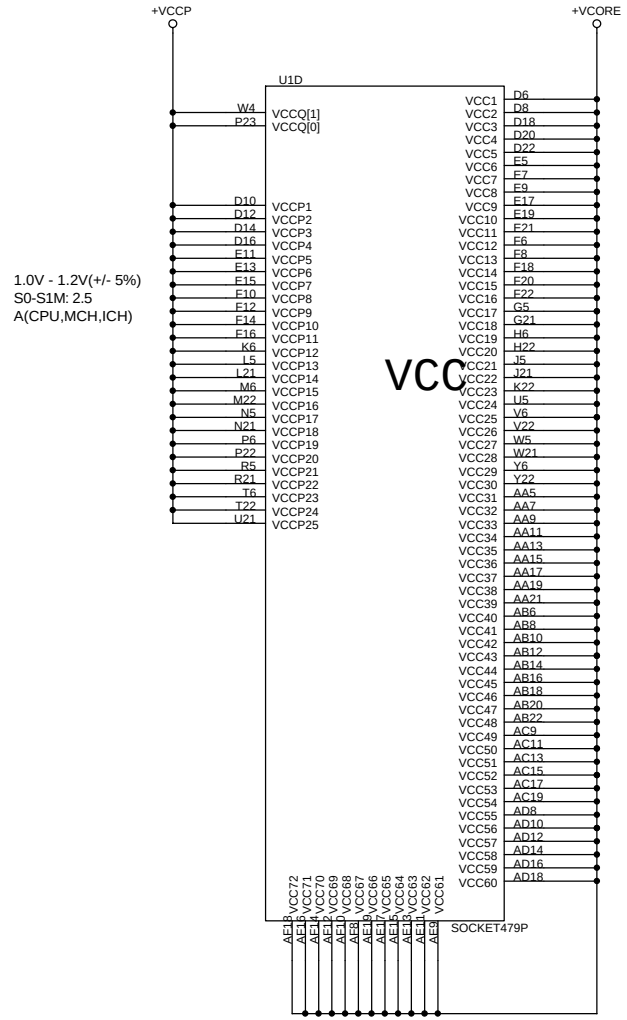
Date: Tuesday, September 27, 2005

Sheet 3 of 46

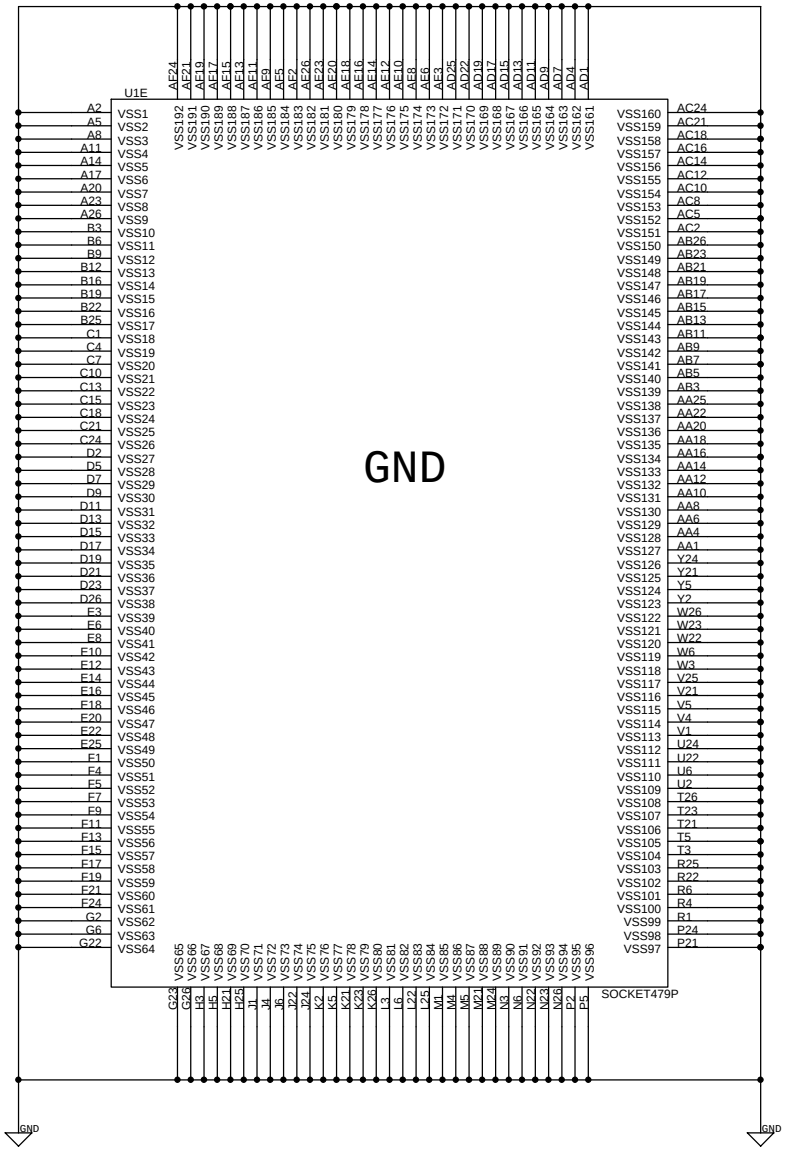


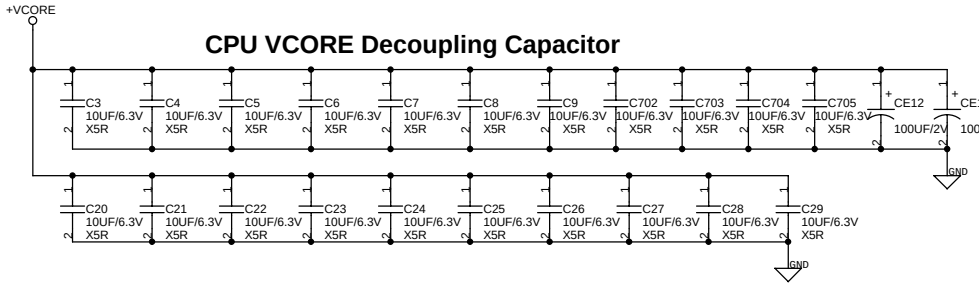
FSB	BSEL1	BSEL0
400	0	1
533	0	0

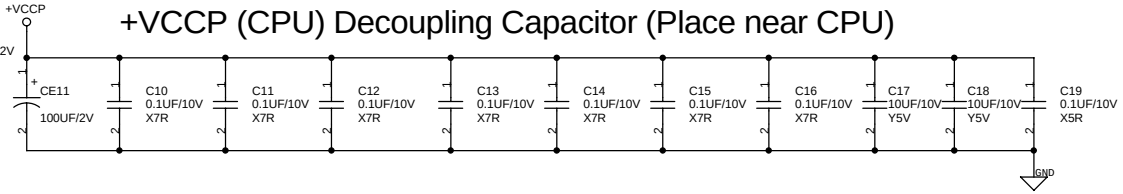
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : Dothan CPU (1)	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 4 of 46	



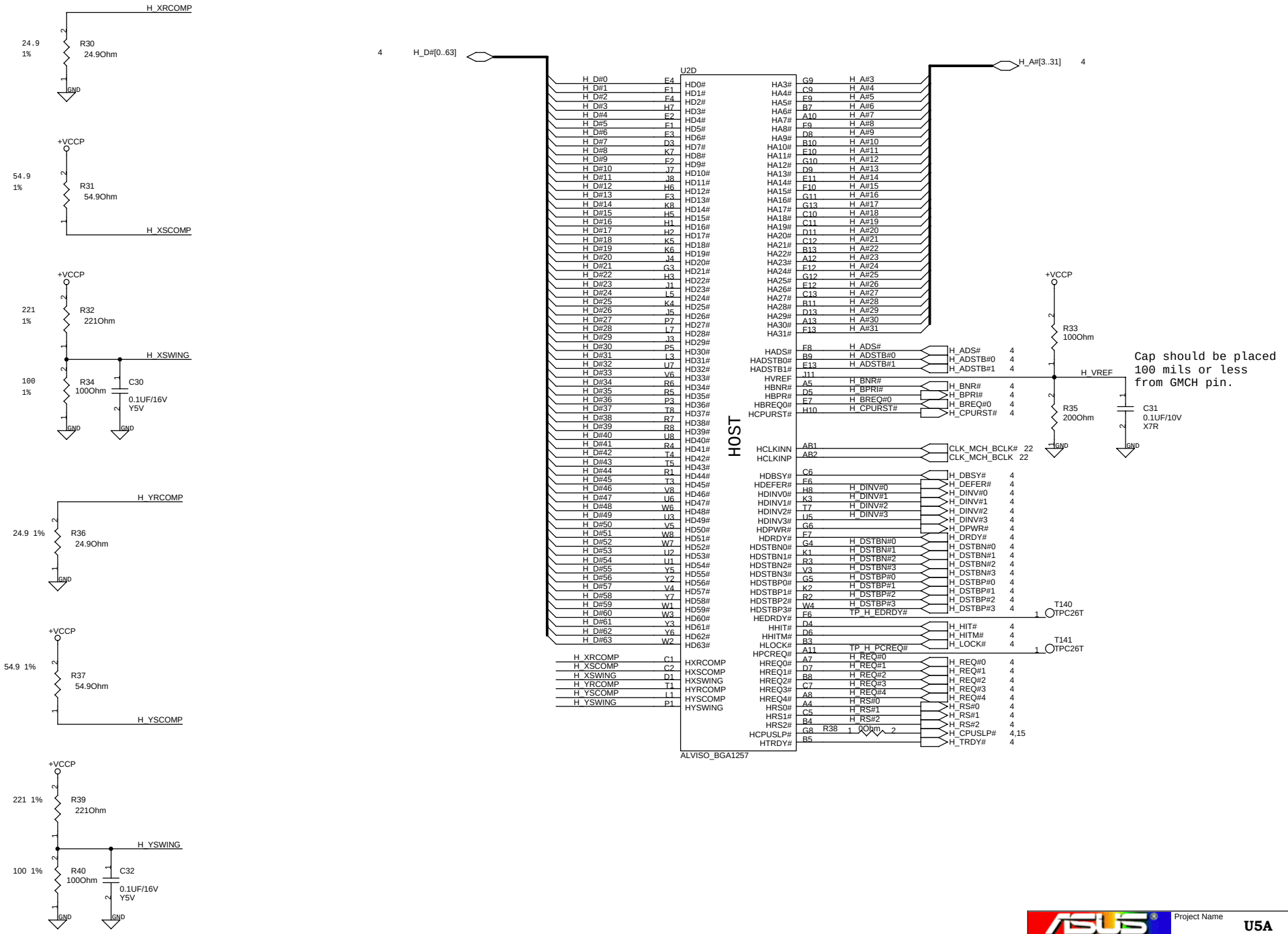
0.745V - 1.356V(+/- 1.5%)
C0: 27 A
C3: 7.59A
C4: 0.9A





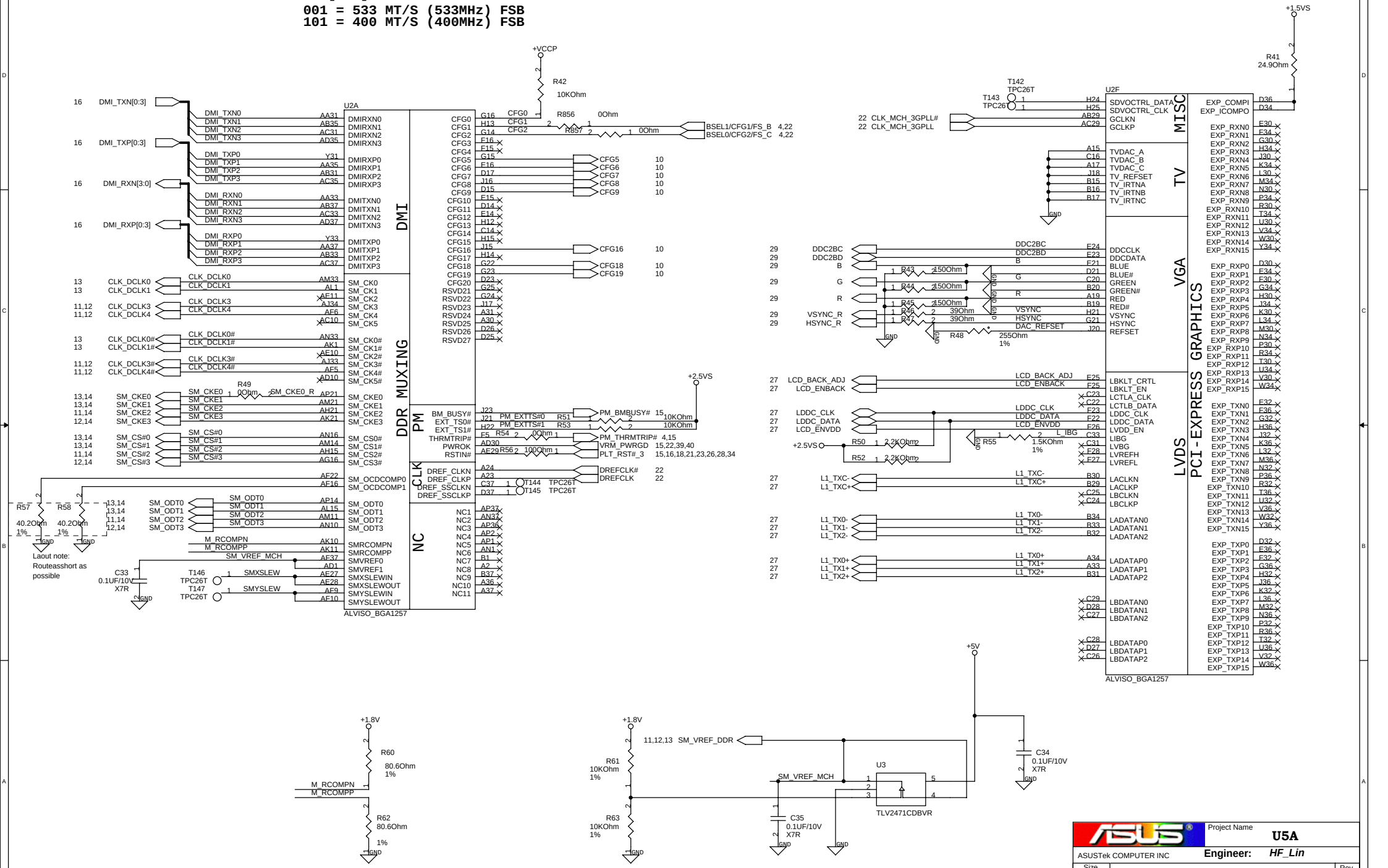


ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : Dothan CPU (2)	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 5 of 46	

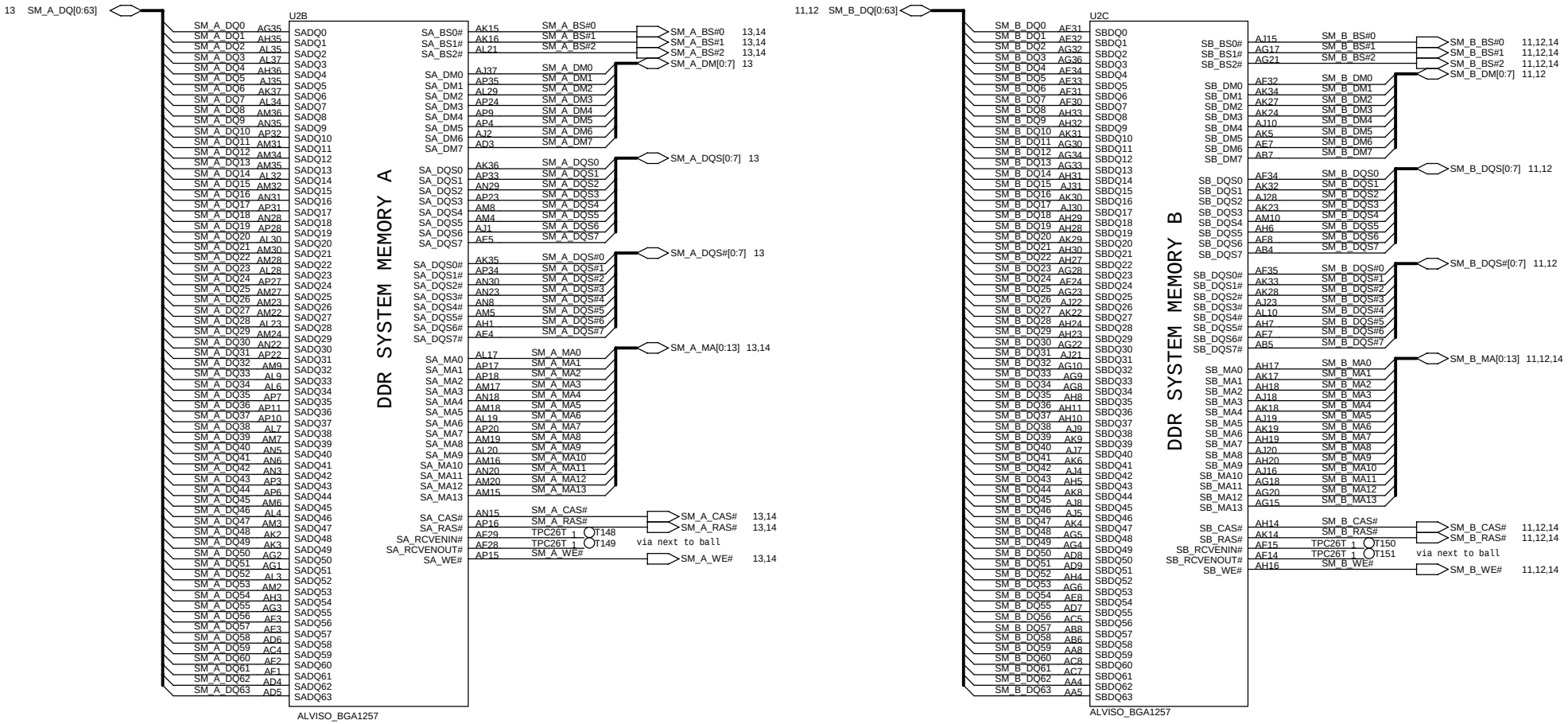


ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title: ALVISO GMCH (1) - HOST	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 6 of 46	

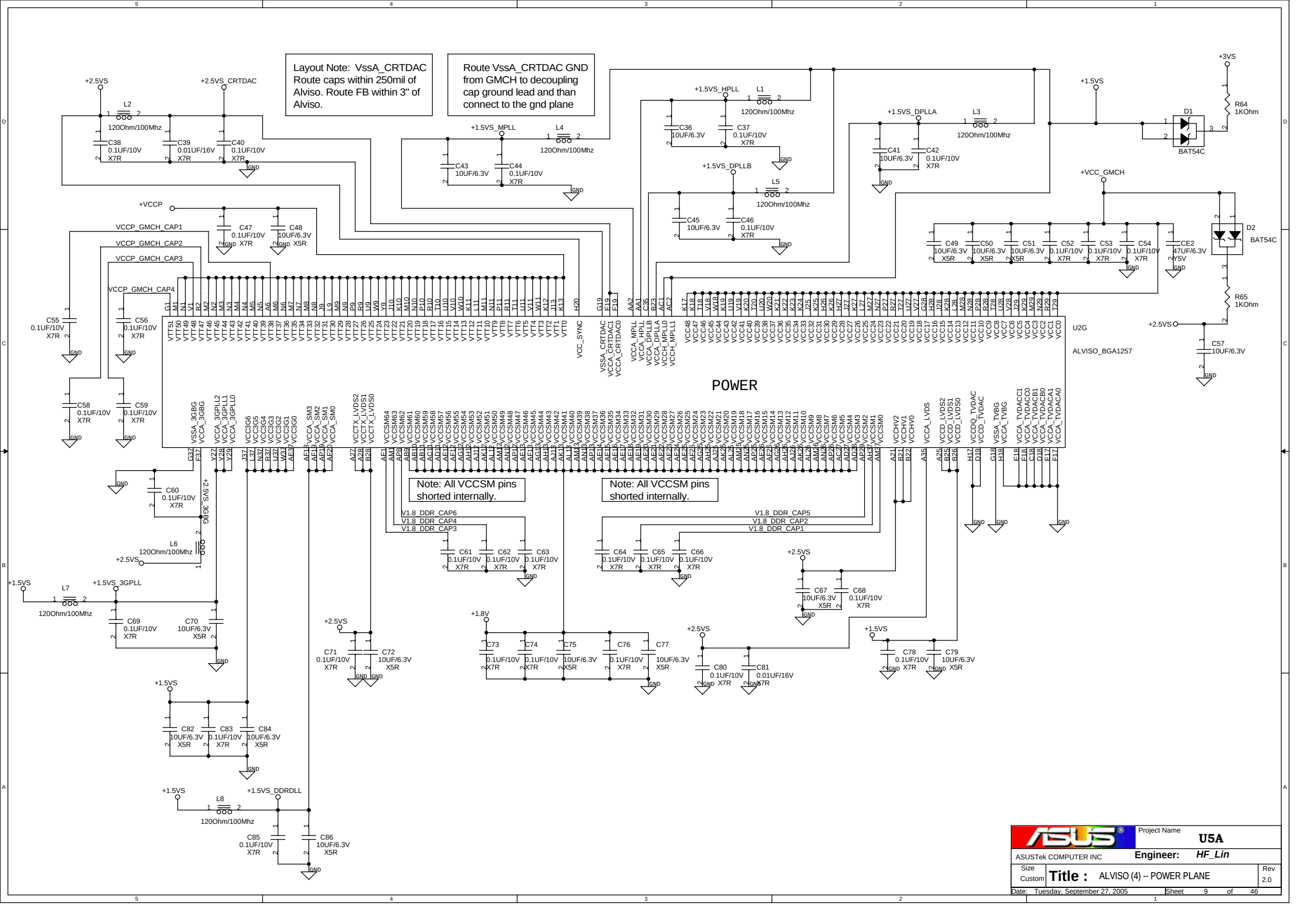
CGF[2:0]
001 = 533 MT/S (533MHz) FSB
101 = 400 MT/S (400MHz) FSB

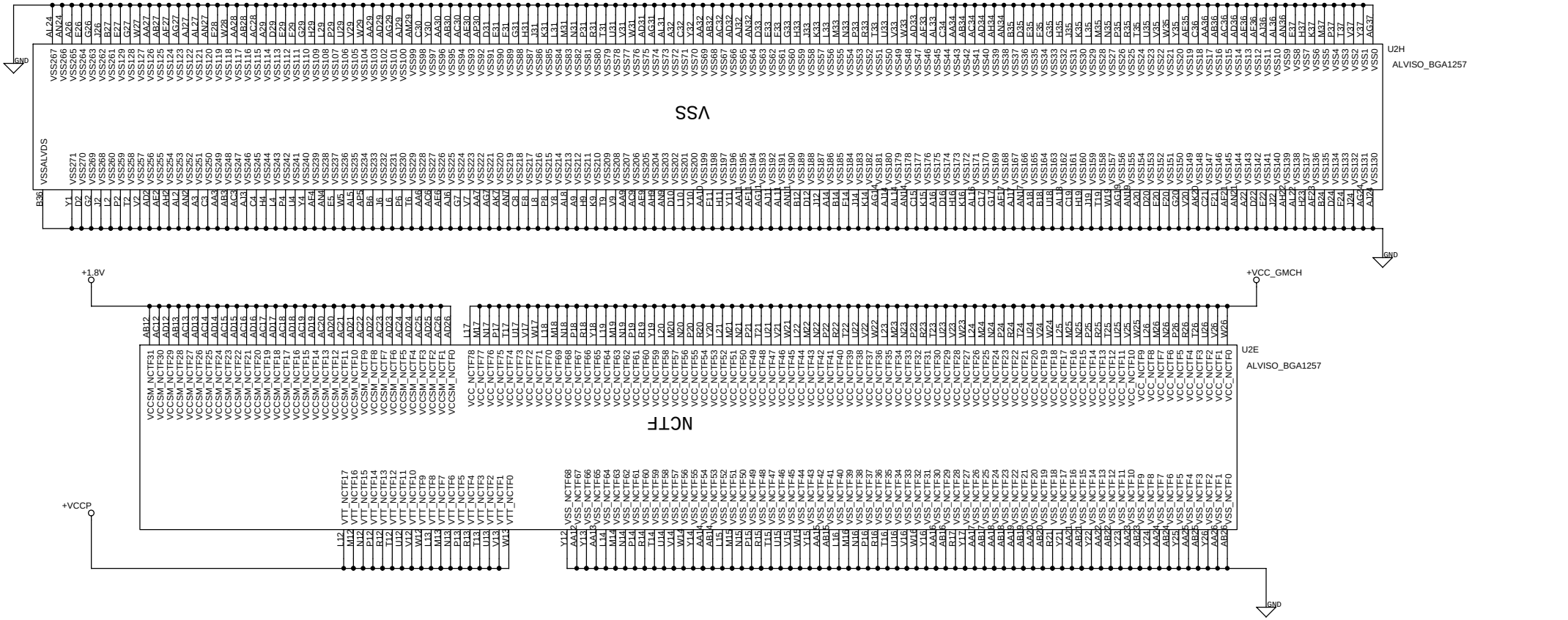


ASUSTek COMPUTER INC	Project Name	U5A	
	Engineer:	HF_Lin	
Size: Custom	Title :	ALVISO (2) - GRAPHICS INTERFACE	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet	7 of 46	

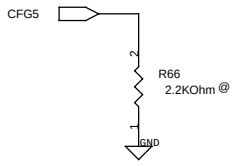


ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title: ALVISO (3) -- DDR2 INTERFACE	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 8 of 46	

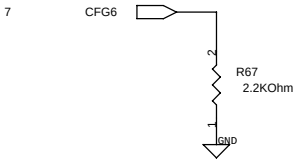

Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
POWER
U2G
ALVISO_BGA1257
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
+2.5VS
+2.5VS_CRTDAC
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS_DPLLA
+1.5VS_DPLLB
+VCCP
+VCC_GMCH
+3VS
+1.5VS
+1.8V
+2.5VS_3GBG
+1.5VS_3GPLL
+1.5VS_DDRDLL
VCCP_GMCH_CAP1
VCCP_GMCH_CAP2
VCCP_GMCH_CAP3
VCCP_GMCH_CAP4
V1.8_DDR_CAP6
V1.8_DDR_CAP4
V1.8_DDR_CAP3
V1.8_DDR_CAP5
V1.8_DDR_CAP2
V1.8_DDR_CAP1
L1 120Ohm/100Mhz
L2 120Ohm/100Mhz
L3 120Ohm/100Mhz
L4 120Ohm/100Mhz
L5 120Ohm/100Mhz
L6 120Ohm/100Mhz
L7 120Ohm/100Mhz
L8 120Ohm/100Mhz
D1 BAT54C
D2 BAT54C
R64 1KOhm
R65 1KOhm
GND
Project Name U5A
ASUSTek COMPUTER INC
Engineer: HF_Lin
Size Custom
Title : ALVISO (4) -- POWER PLANE
Rev 2.0
Date: Tuesday, September 27, 2005
Sheet 9 of 46



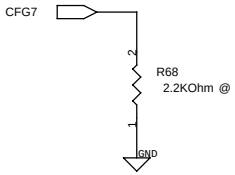
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



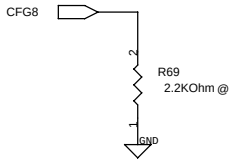
CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



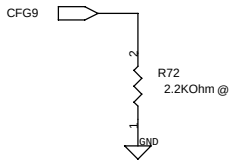
CFG8 : PCI-X POWER SAVING
LOW = PCI-X Power Saving
HIGH = Default



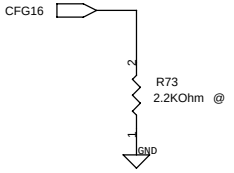
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

SDVOCRTL_DATA LOW = No SDVO device present (Default)

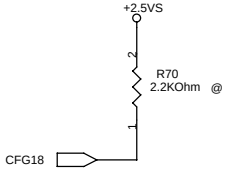
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



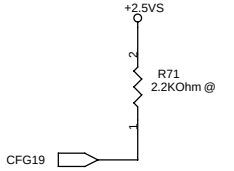
CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



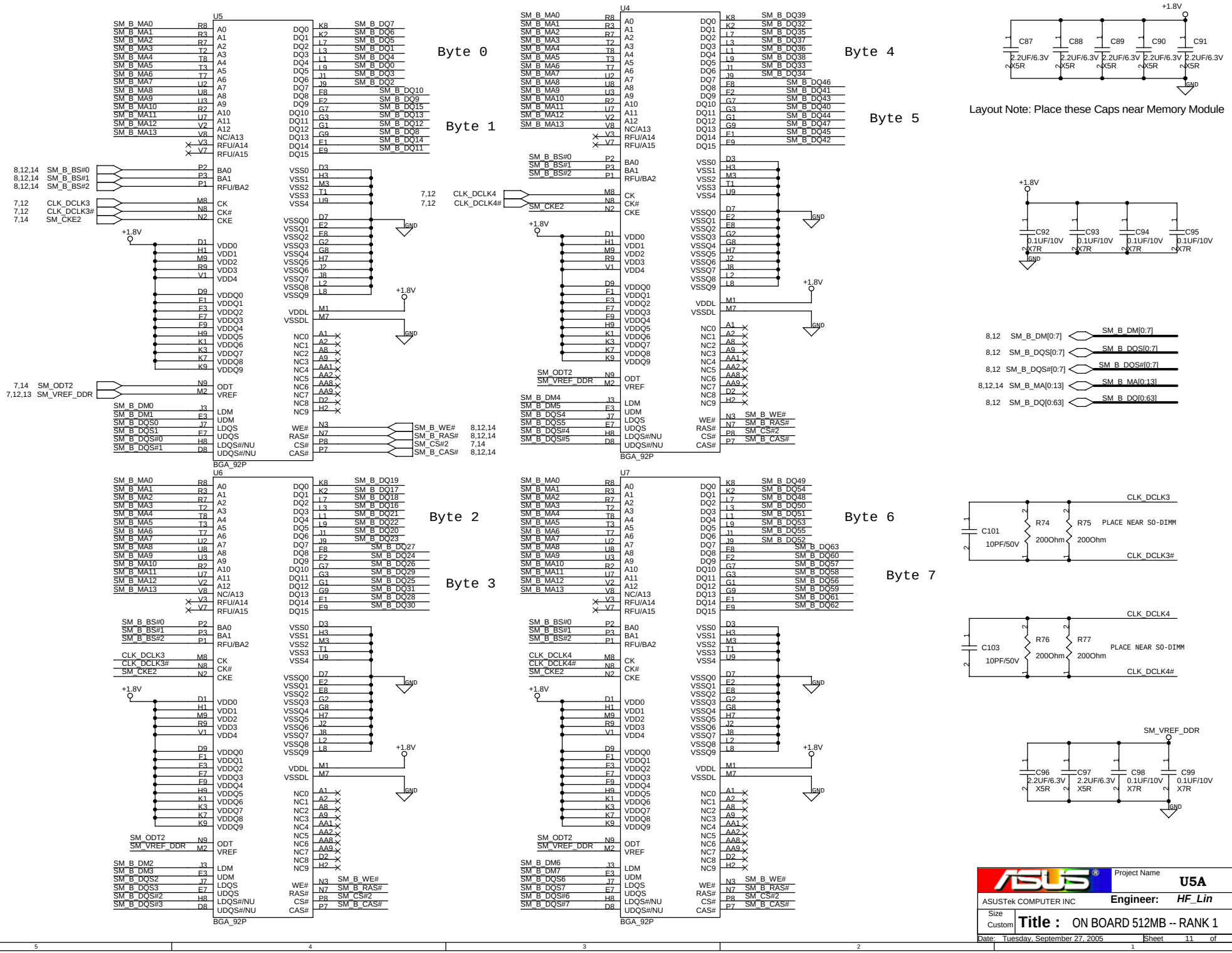
CFG18 : VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V



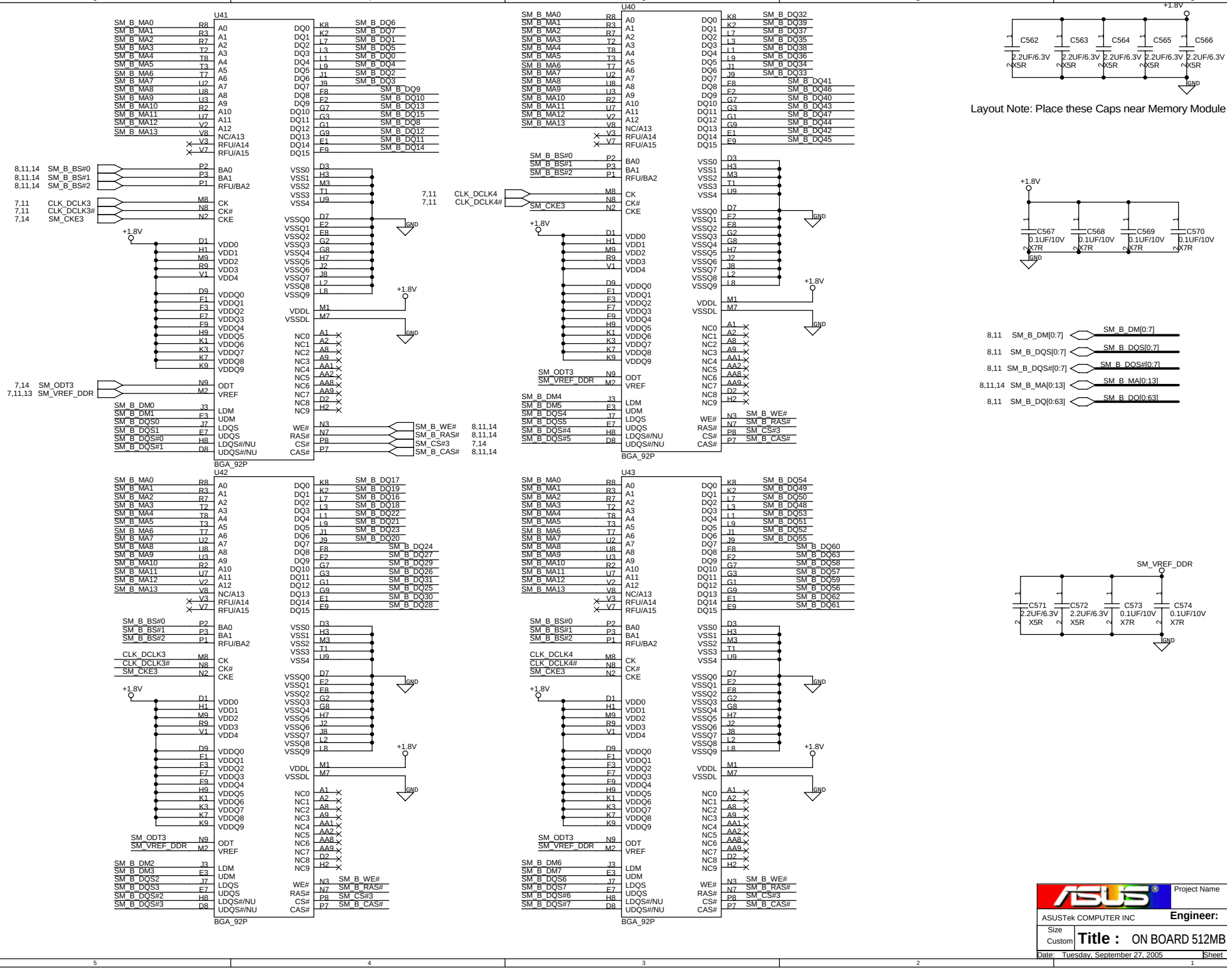
CFG19 : VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V



ASUSTek COMPUTER INC	Project Name: U5A		
	Engineer: HF_Lin		
Size: Custom	Title : ALVISO (5) -- GND		Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 10 of 46		



Project Name	**U5A**
ASUSTek COMPUTER INC	**Engineer:** *HF_Lin*
Size: Custom	**Title :** ON BOARD 512MB -- RANK 1
Rev	2.0
Date: Tuesday, September 27, 2005	Sheet 11 of 46



Project Name	U5A
ASUSTek COMPUTER INC	Engineer: HF_Lin
Size: Custom	Title : ON BOARD 512MB -- RANK 2
Rev	2.0
Date: Tuesday, September 27, 2005	Sheet 12 of 46

SM_A_MA[0:13] SM_A_MA[0:13] 8,14

SM_A_DQ[0:63] SM_A_DQ[0:63] 8

SM_A_DM[0:7] SM_A_DM[0:7] 8

SM_A_DQS[0:7] SM_A_DQS[0:7] 8

SM_A_DQS#[0:7] SM_A_DQS#[0:7] 8

U8A

DDR_DIMM_200P

Byte 0

Byte 1

Byte 2

Byte 3

Byte 5

Byte 4

Byte 6

Byte 7

U8B

DDR_DIMM_200P

+3VS

C100 0.1UF/10V X7R

C102 2.2UF/6.3V X5R

7,11,12 SM_VREF_DDR

+1.8V

C104 0.1UF/10V X7R

C105 0.1UF/10V X7R

C106 0.1UF/10V X7R

C107 0.1UF/10V X7R

Layout Note: Place these Caps near uDIMM

C108 0.1UF/10V X7R

C109 0.1UF/10V X7R

C110 0.1UF/10V X7R

C111 0.1UF/10V X7R

Layout Note: Place these High-Freq decoupling Caps near the GMCH

C113 2.2UF/6.3V X5R

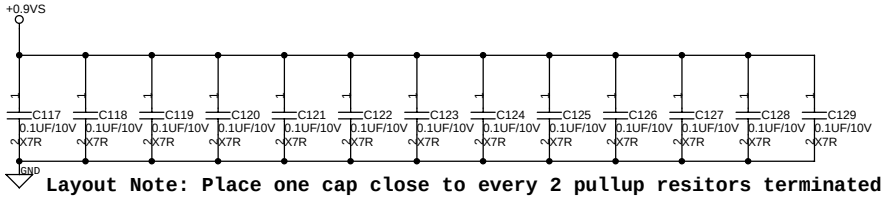
C114 2.2UF/6.3V X5R

C115 2.2UF/6.3V X5R

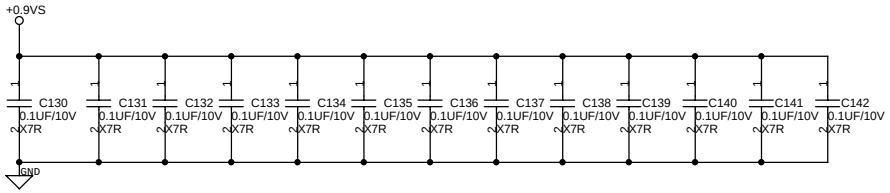
C116 2.2UF/6.3V X5R

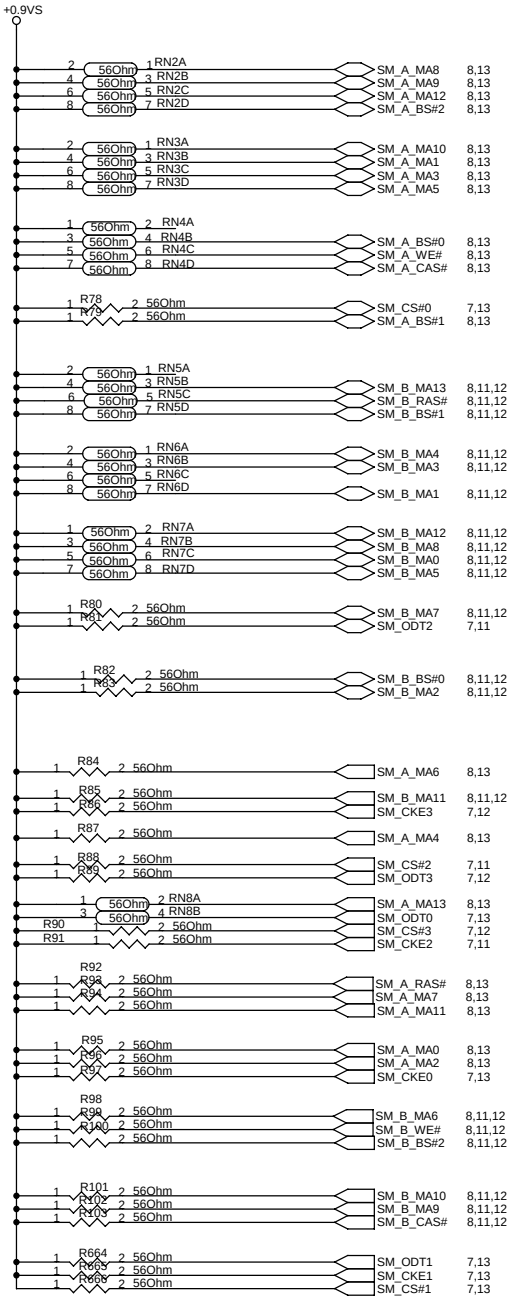
Layout Note: Place these Caps near uDIMM

ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : DDR2 SO-DIMM	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 13 of 46	



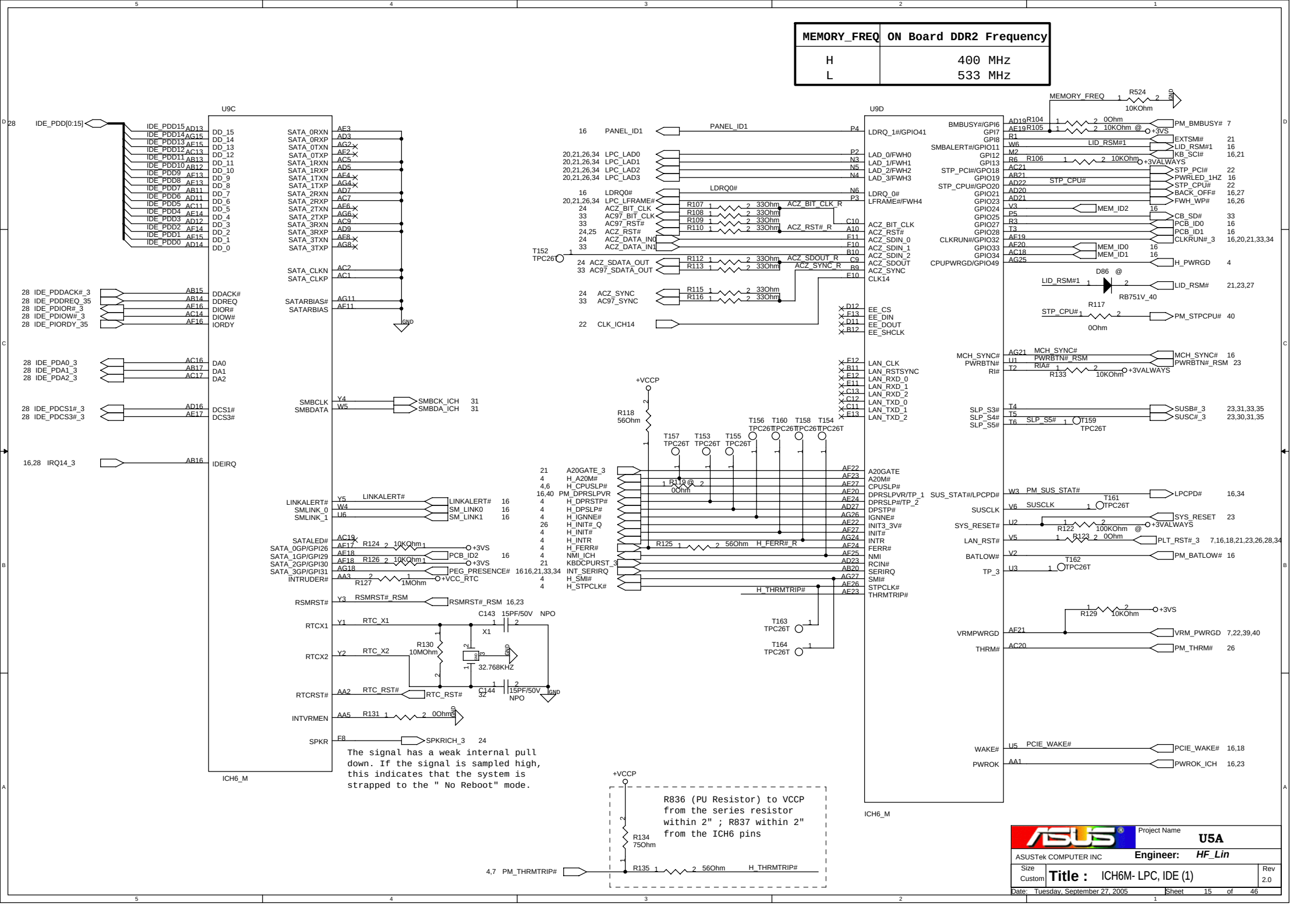
Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9VS



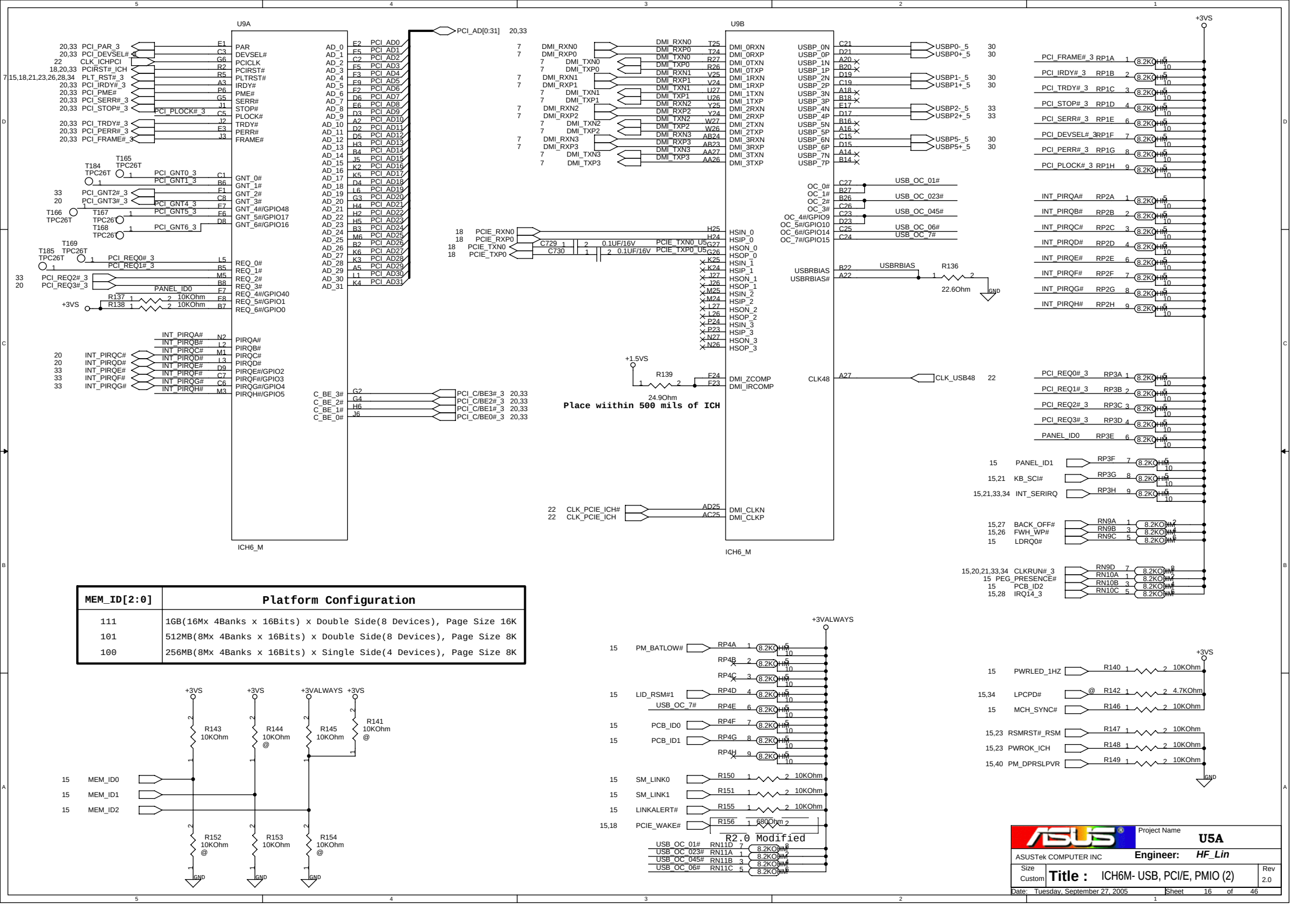


ASUSTek COMPUTER INC	Project Name: **U5A**	
	Engineer: *HF_Lin*	
Size: Custom	**Title :** DDR2 Termination	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 14 of 46	

MEMORY_FREQ	ON Board DDR2 Frequency
H	400 MHz
L	533 MHz

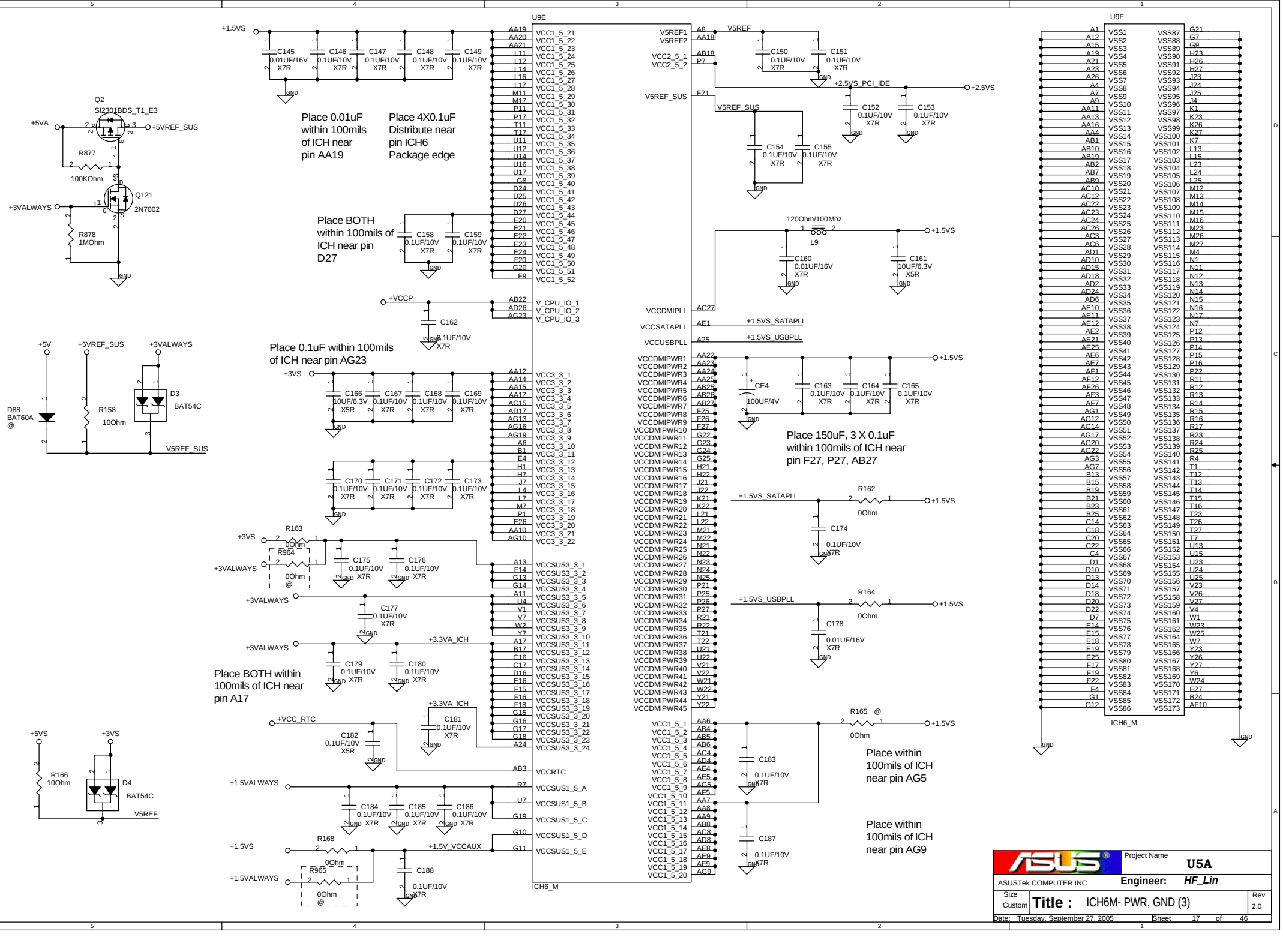


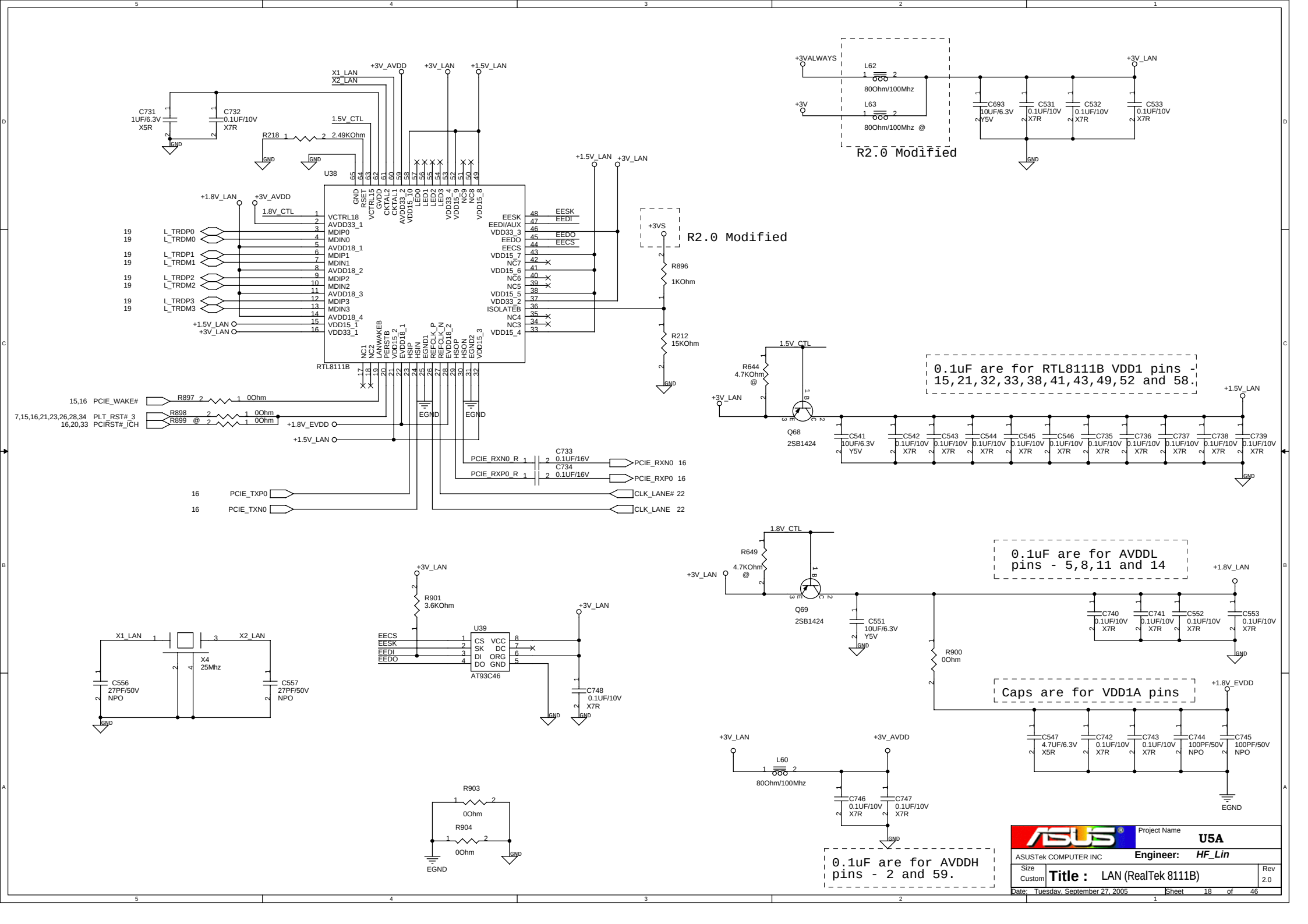
Project Name	U5A
ASUSTek COMPUTER INC	Engineer: HF_Lin
Size: Custom	Title : ICH6M- LPC, IDE (1)
Rev	2.0
Date: Tuesday, September 27, 2005	Sheet 15 of 46

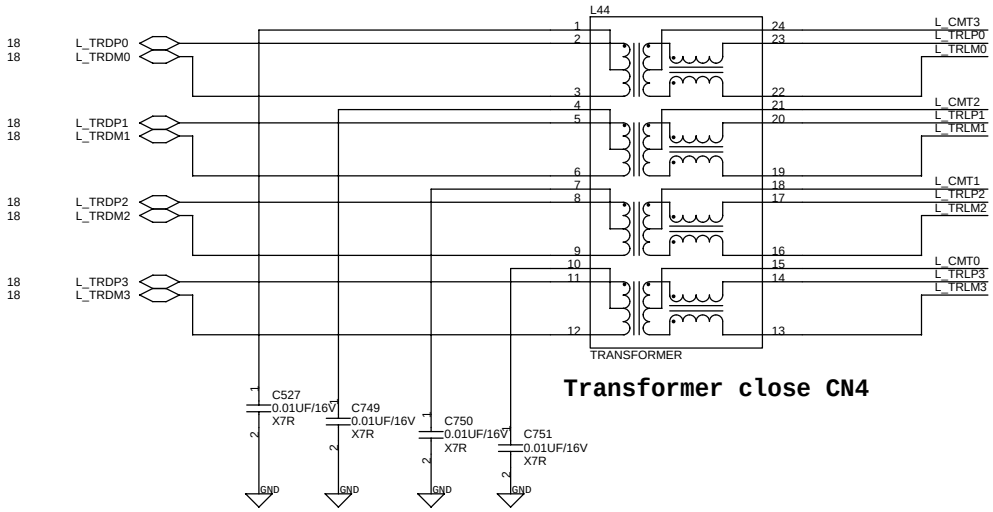


MEM_ID[2:0]	Platform Configuration
111	1GB(16Mx 4Banks x 16Bits) x Double Side(8 Devices), Page Size 16K
101	512MB(8Mx 4Banks x 16Bits) x Double Side(8 Devices), Page Size 8K
100	256MB(8Mx 4Banks x 16Bits) x Single Side(4 Devices), Page Size 8K

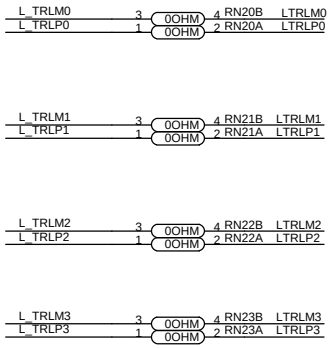
Project Name	U5A
ASUSTek COMPUTER INC	Engineer: HF_Lin
Size: Custom	Title : ICH6M- USB, PCI/E, PMIO (2)
Rev	2.0
Date: Tuesday, September 27, 2005	Sheet 16 of 46

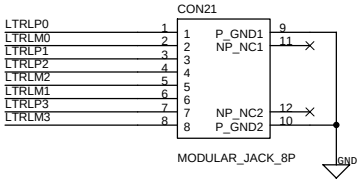

Q2
SI2301BDS_T1_E3
+5VA
+5VREF_SUS
R877
100KOhm
Q121
2N7002
+3VALWAYS
R878
1MOhm
GND
+5V
+5VREF_SUS
+3VALWAYS
D88
BAT60A
@
R158
10Ohm
D3
BAT54C
V5REF_SUS
+5VS
+3VS
R166
10Ohm
D4
BAT54C
V5REF
U9E
+1.5VS
C145 0.01UF/16V X7R
C146 0.1UF/10V X7R
C147 0.1UF/10V X7R
C148 0.1UF/10V X7R
C149 0.1UF/10V X7R
Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
C158 0.1UF/10V X7R
C159 0.1UF/10V X7R
+VCCP
C162 0.1UF/10V X7R
Place 0.1uF within 100mils of ICH near pin AG23
+3VS
C166 10UF/6.3V X5R
C167 0.1UF/10V X7R
C168 0.1UF/10V X7R
C169 0.1UF/10V X7R
C170 0.1UF/10V X7R
C171 0.1UF/10V X7R
C172 0.1UF/10V X7R
C173 0.1UF/10V X7R
R163
0Ohm
R964
0Ohm
@
C175 0.1UF/10V X7R
C176 0.1UF/10V X7R
C177 0.1UF/10V X7R
+3.3VA_ICH
C179 0.1UF/10V X7R
C180 0.1UF/10V X7R
Place BOTH within 100mils of ICH near pin A17
C181 0.1UF/10V X7R
+VCC_RTC
C182 0.1UF/10V X5R
+1.5VALWAYS
C184 0.1UF/10V X7R
C185 0.1UF/10V X7R
C186 0.1UF/10V X7R
R168
0Ohm
R965
0Ohm
@
+1.5V_VCCAUX
C188 0.1UF/10V X7R
VCC1_5_21 VCC1_5_22 VCC1_5_23 VCC1_5_24 VCC1_5_25 VCC1_5_26 VCC1_5_27 VCC1_5_28 VCC1_5_29 VCC1_5_30 VCC1_5_31 VCC1_5_32 VCC1_5_33 VCC1_5_34 VCC1_5_35 VCC1_5_36 VCC1_5_37 VCC1_5_38 VCC1_5_39 VCC1_5_40 VCC1_5_41 VCC1_5_42 VCC1_5_43 VCC1_5_44 VCC1_5_45 VCC1_5_46 VCC1_5_47 VCC1_5_48 VCC1_5_49 VCC1_5_50 VCC1_5_51 VCC1_5_52
V_CPU_IO_1 V_CPU_IO_2 V_CPU_IO_3
VCC3_3_1 VCC3_3_2 VCC3_3_3 VCC3_3_4 VCC3_3_5 VCC3_3_6 VCC3_3_7 VCC3_3_8 VCC3_3_9 VCC3_3_10 VCC3_3_11 VCC3_3_12 VCC3_3_13 VCC3_3_14 VCC3_3_15 VCC3_3_16 VCC3_3_17 VCC3_3_18 VCC3_3_19 VCC3_3_20 VCC3_3_21 VCC3_3_22
VCCSUS3_3_1 VCCSUS3_3_2 VCCSUS3_3_3 VCCSUS3_3_4 VCCSUS3_3_5 VCCSUS3_3_6 VCCSUS3_3_7 VCCSUS3_3_8 VCCSUS3_3_9 VCCSUS3_3_10 VCCSUS3_3_11 VCCSUS3_3_12 VCCSUS3_3_13 VCCSUS3_3_14 VCCSUS3_3_15 VCCSUS3_3_16 VCCSUS3_3_17 VCCSUS3_3_18 VCCSUS3_3_19 VCCSUS3_3_20 VCCSUS3_3_21 VCCSUS3_3_22 VCCSUS3_3_23 VCCSUS3_3_24
VCCRTC
VCCSUS1_5_A VCCSUS1_5_B VCCSUS1_5_C VCCSUS1_5_D VCCSUS1_5_E
ICH6_M
V5REF1 V5REF2 VCC2_5_1 VCC2_5_2 V5REF_SUS
V5REF
C150 0.1UF/10V X7R
C151 0.1UF/10V X7R
+2.5VS_PCI_IDE
+2.5VS
C152 0.1UF/10V X7R
C153 0.1UF/10V X7R
C154 0.1UF/10V X7R
C155 0.1UF/10V X7R
120Ohm/100Mhz
L9
C160 0.01UF/16V X7R
C161 10UF/6.3V X5R
VCCDMIPLL VCCSATAPLL VCCUSBPLL
+1.5VS_SATAPLL
+1.5VS_USBPLL
VCCDMIPWR1 VCCDMIPWR2 VCCDMIPWR3 VCCDMIPWR4 VCCDMIPWR5 VCCDMIPWR6 VCCDMIPWR7 VCCDMIPWR8 VCCDMIPWR9 VCCDMIPWR10 VCCDMIPWR11 VCCDMIPWR12 VCCDMIPWR13 VCCDMIPWR14 VCCDMIPWR15 VCCDMIPWR16 VCCDMIPWR17 VCCDMIPWR18 VCCDMIPWR19 VCCDMIPWR20 VCCDMIPWR21 VCCDMIPWR22 VCCDMIPWR23 VCCDMIPWR24 VCCDMIPWR25 VCCDMIPWR26 VCCDMIPWR27 VCCDMIPWR28 VCCDMIPWR29 VCCDMIPWR30 VCCDMIPWR31 VCCDMIPWR32 VCCDMIPWR33 VCCDMIPWR34 VCCDMIPWR35 VCCDMIPWR36 VCCDMIPWR37 VCCDMIPWR38 VCCDMIPWR39 VCCDMIPWR40 VCCDMIPWR41 VCCDMIPWR42 VCCDMIPWR43 VCCDMIPWR44 VCCDMIPWR45
CE4 100UF/4V
C163 0.1UF/10V X7R
C164 0.1UF/10V X7R
C165 0.1UF/10V X7R
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
R162
0Ohm
C174 0.1UF/10V X7R
R164
0Ohm
C178 0.01UF/16V X7R
VCC1_5_1 VCC1_5_2 VCC1_5_3 VCC1_5_4 VCC1_5_5 VCC1_5_6 VCC1_5_7 VCC1_5_8 VCC1_5_9 VCC1_5_10 VCC1_5_11 VCC1_5_12 VCC1_5_13 VCC1_5_14 VCC1_5_15 VCC1_5_16 VCC1_5_17 VCC1_5_18 VCC1_5_19 VCC1_5_20
R165 @
0Ohm
C183 0.1UF/10V X7R
Place within 100mils of ICH near pin AG5
C187 0.1UF/10V X7R
Place within 100mils of ICH near pin AG9
U9F
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129 VSS130 VSS131 VSS132 VSS133 VSS134 VSS135 VSS136 VSS137 VSS138 VSS139 VSS140 VSS141 VSS142 VSS143 VSS144 VSS145 VSS146 VSS147 VSS148 VSS149 VSS150 VSS151 VSS152 VSS153 VSS154 VSS155 VSS156 VSS157 VSS158 VSS159 VSS160 VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173
ICH6_M
GND
ASUSTek COMPUTER INC
Project Name U5A
Engineer: HF_Lin
Size Custom
Title : ICH6M- PWR, GND (3)
Rev 2.0
Date: Tuesday, September 27, 2005
Sheet 17 of 46

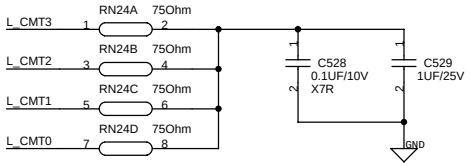

+3VALWAYS
L62
80Ohm/100Mhz
+3V
L63
80Ohm/100Mhz @
+3V_LAN
C693 10UF/6.3V Y5V
C531 0.1UF/10V X7R
C532 0.1UF/10V X7R
C533 0.1UF/10V X7R
GND
R2.0 Modified
X1_LAN
X2_LAN
+3V_AVDD
+3V_LAN
+1.5V_LAN
C731 1UF/6.3V X5R
C732 0.1UF/10V X7R
1.5V_CTL
R218 2.49KOhm
U38
+1.8V_LAN
+3V_AVDD
1.8V_CTL
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_1
VDD33_1
L_TRDP0
L_TRDM0
L_TRDP1
L_TRDM1
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
VDD15_7
NC7
VDD15_6
NC6
NC5
VDD15_5
VDD33_2
ISOLATEB
NC4
NC3
VDD15_4
EESK
EEDI
EEDO
EECS
RTL8111B
+3VS
R896 1KOhm
R212 15KOhm
R2.0 Modified
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
R644 4.7KOhm @
Q68 2SB1424
C541 10UF/6.3V Y5V
C542 0.1UF/10V X7R
C543 0.1UF/10V X7R
C544 0.1UF/10V X7R
C545 0.1UF/10V X7R
C546 0.1UF/10V X7R
C735 0.1UF/10V X7R
C736 0.1UF/10V X7R
C737 0.1UF/10V X7R
C738 0.1UF/10V X7R
C739 0.1UF/10V X7R
R897 0Ohm
R898 0Ohm
R899 @ 0Ohm
15,16 PCIE_WAKE#
7,15,16,21,23,26,28,34 PLT_RST#_3
16,20,33 PCIRST#_ICH
+1.8V_EVDD
EGND
C733 0.1UF/16V
C734 0.1UF/16V
PCIE_RXN0_R
PCIE_RXP0_R
PCIE_RXN0 16
PCIE_RXP0 16
16 PCIE_TXP0
16 PCIE_TXN0
CLK_LANE# 22
CLK_LANE 22
X4 25Mhz
C556 27PF/50V NPO
C557 27PF/50V NPO
R901 3.6KOhm
U39
CS VCC
SK DC
DI ORG
DO GND
AT93C46
C748 0.1UF/10V X7R
R903 0Ohm
R904 0Ohm
R649 4.7KOhm @
Q69 2SB1424
C551 10UF/6.3V Y5V
0.1uF are for AVDDL pins - 5,8,11 and 14
C740 0.1UF/10V X7R
C741 0.1UF/10V X7R
C552 0.1UF/10V X7R
C553 0.1UF/10V X7R
R900 0Ohm
Caps are for VDD1A pins
C547 4.7UF/6.3V X5R
C742 0.1UF/10V X7R
C743 0.1UF/10V X7R
C744 100PF/50V NPO
C745 100PF/50V NPO
L60
80Ohm/100Mhz
C746 0.1UF/10V X7R
C747 0.1UF/10V X7R
0.1uF are for AVDDH pins - 2 and 59.
ASUSTek COMPUTER INC
Project Name U5A
Engineer: HF_Lin
Size Custom
Title : LAN (RealTek 8111B)
Rev 2.0
Date: Tuesday, September 27, 2005
Sheet 18 of 46



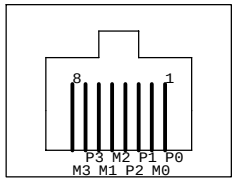
Transformer close CN4



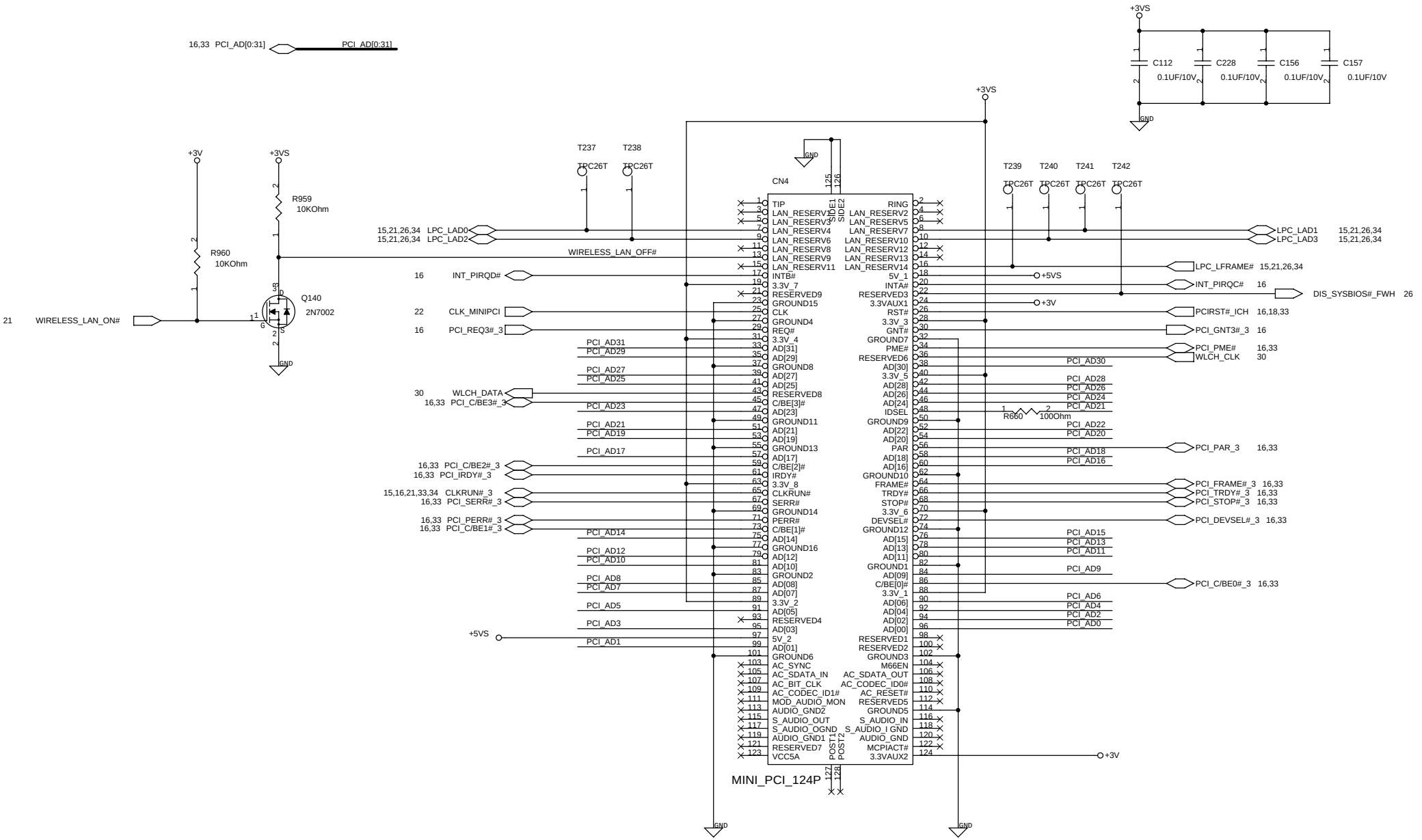




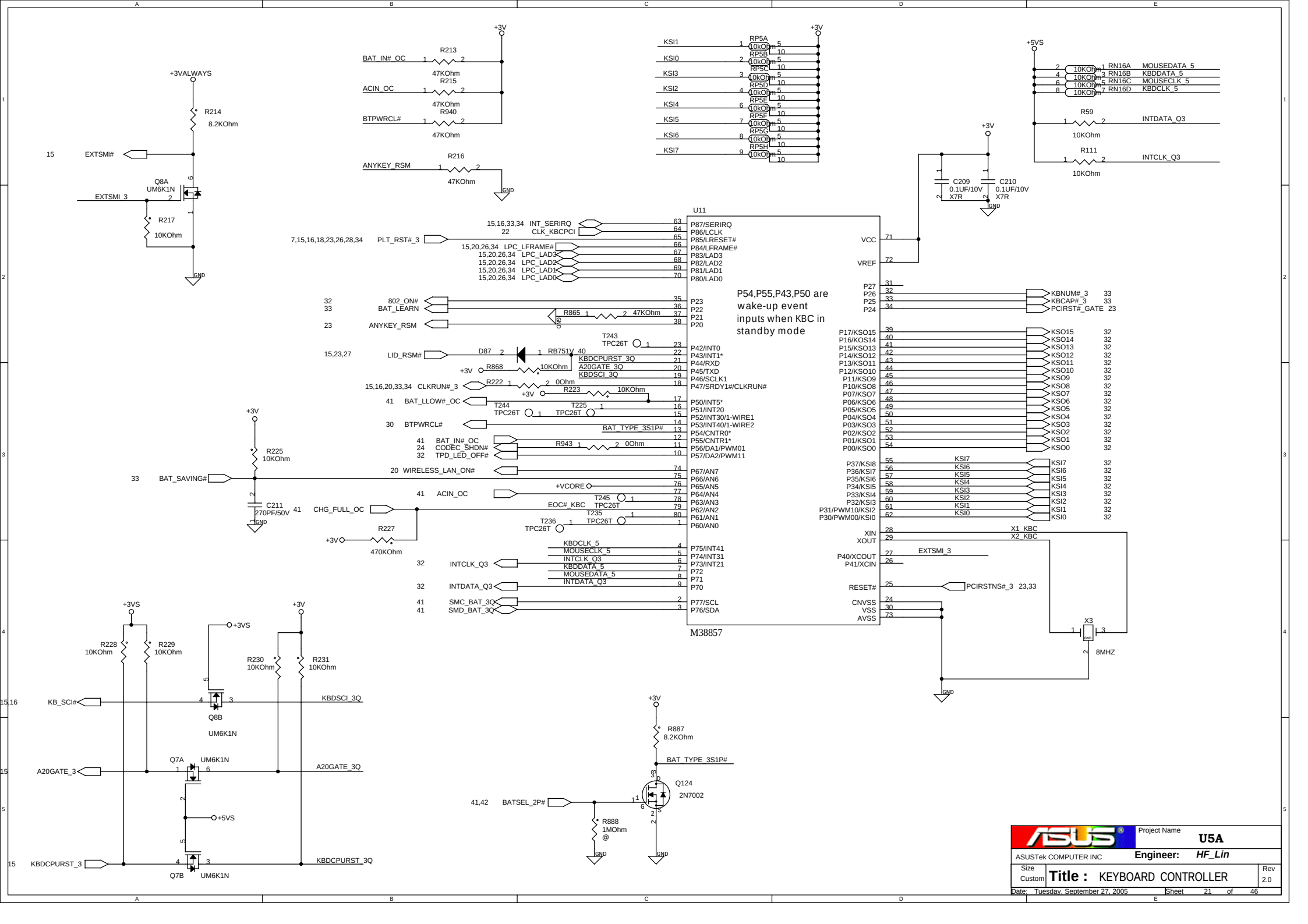
LAN



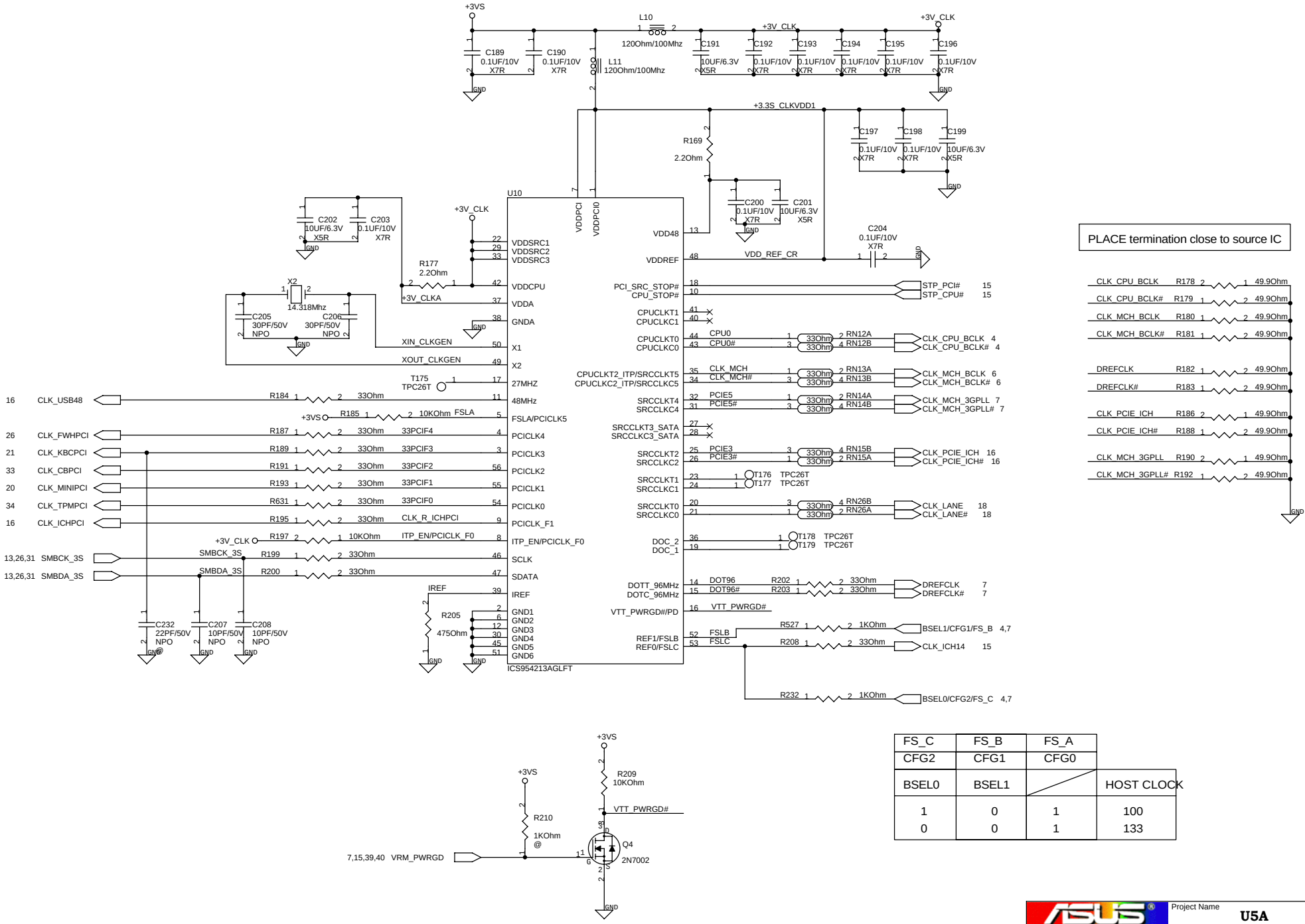
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : LAN I/O	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 19 of 46	



ASUSTek COMPUTER INC	Project Name	U5A	
	Engineer:	HF_Lin	
Size: Custom	Title :	MINI PCI	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet	20 of 46	

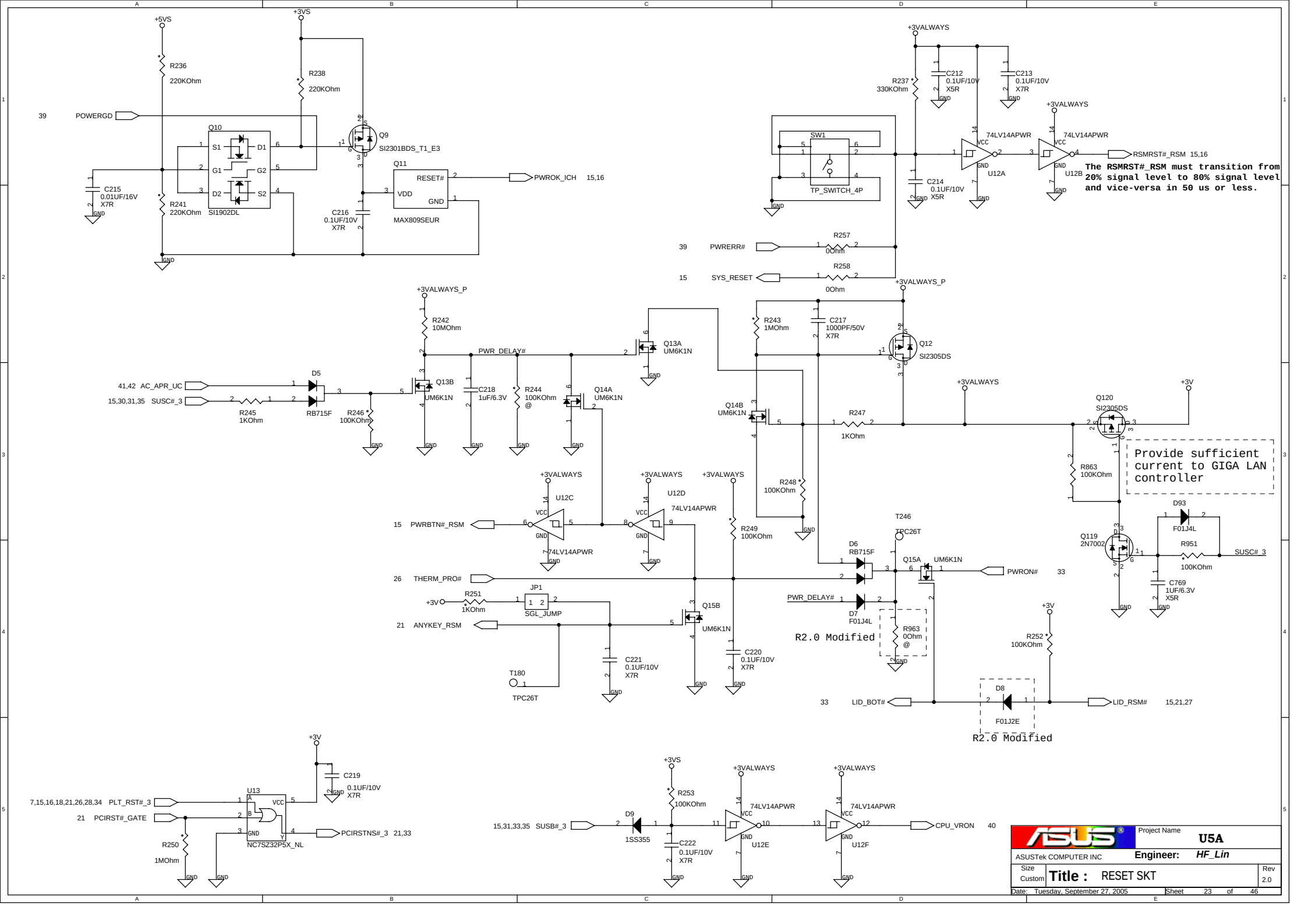


ASUSTek COMPUTER INC	Project Name	U5A	
	Engineer:	*HF_Lin*	
Size: Custom	Title :	KEYBOARD CONTROLLER	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet	21 of 46	

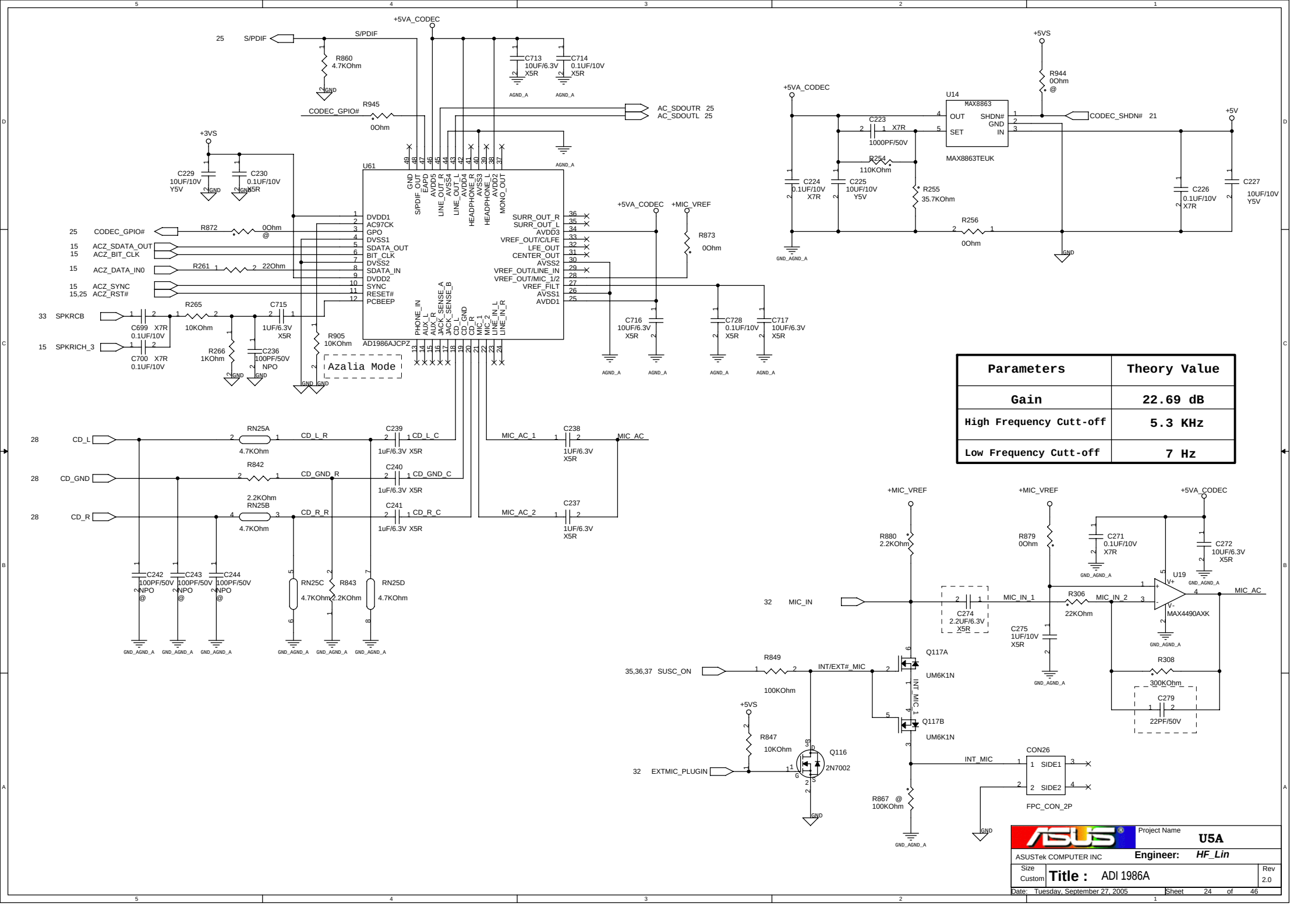


FS_C	FS_B	FS_A	
CFG2	CFG1	CFG0	
BSEL0	BSEL1		HOST CLOCK
1	0	1	100
0	0	1	133

ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : CLOCK GENERATOR	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 22 of 46	



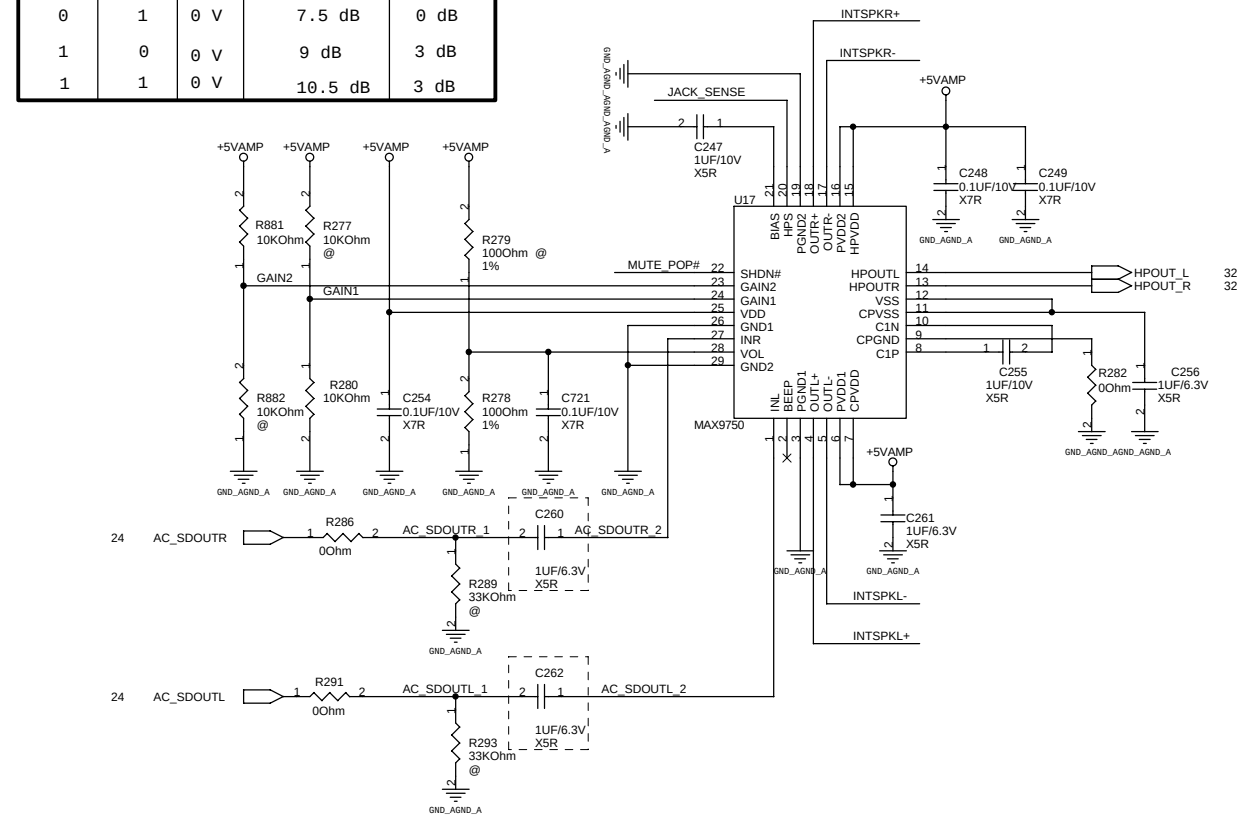
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title: RESET SKT	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 23 of 46	

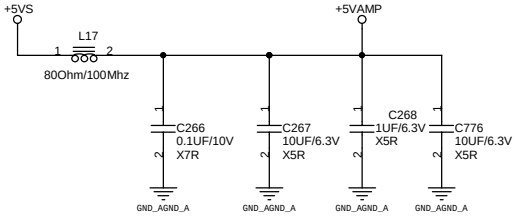


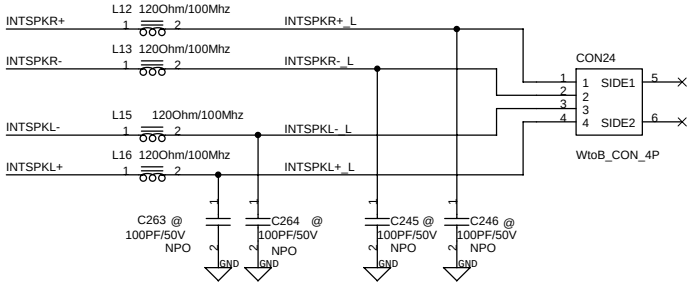
Parameters	Theory Value
Gain	22.69 dB
High Frequency Cutt-off	5.3 KHz
Low Frequency Cutt-off	7 Hz

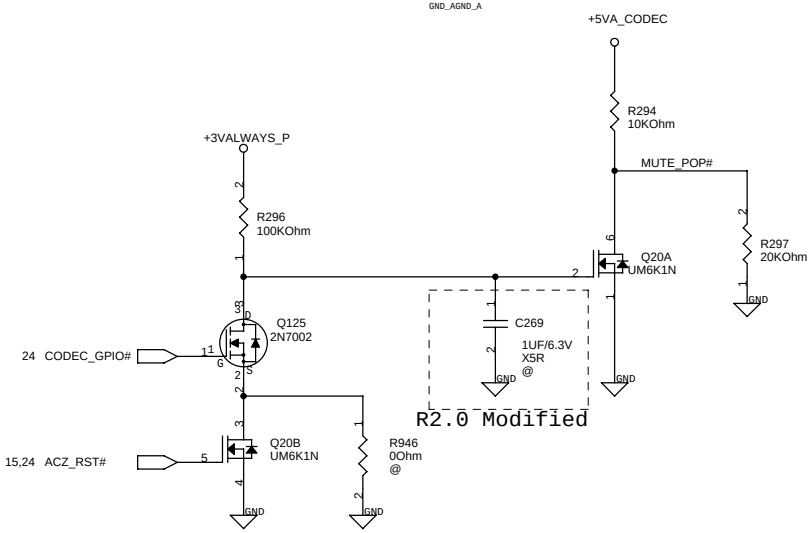
Project Name	U5A
ASUSTek COMPUTER INC	Engineer: HF_Lin
Size: Custom	Title : ADI 1986A
Rev	2.0
Date: Tuesday, September 27, 2005	Sheet 24 of 46

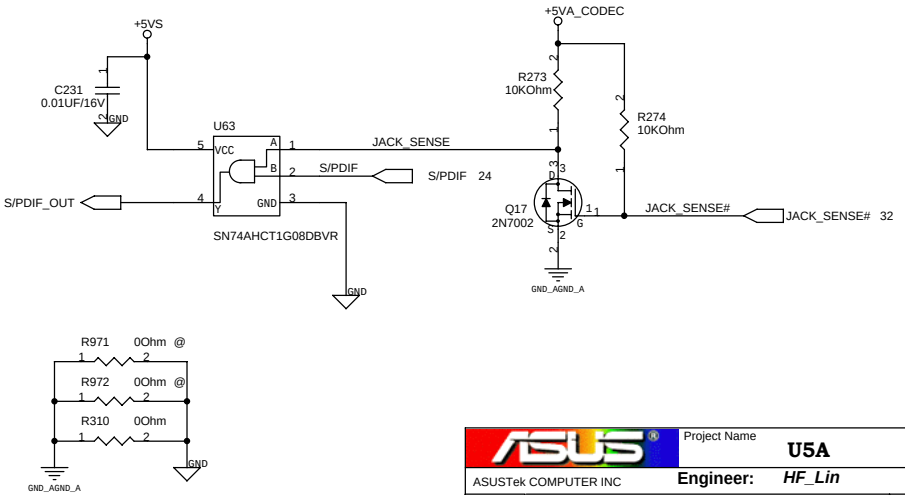
GAIN 2	GAIN 1	VOL	Speaker Gain	HP Gain
0	0	0 V	6 dB	0 dB
0	1	0 V	7.5 dB	0 dB
1	0	0 V	9 dB	3 dB
1	1	0 V	10.5 dB	3 dB



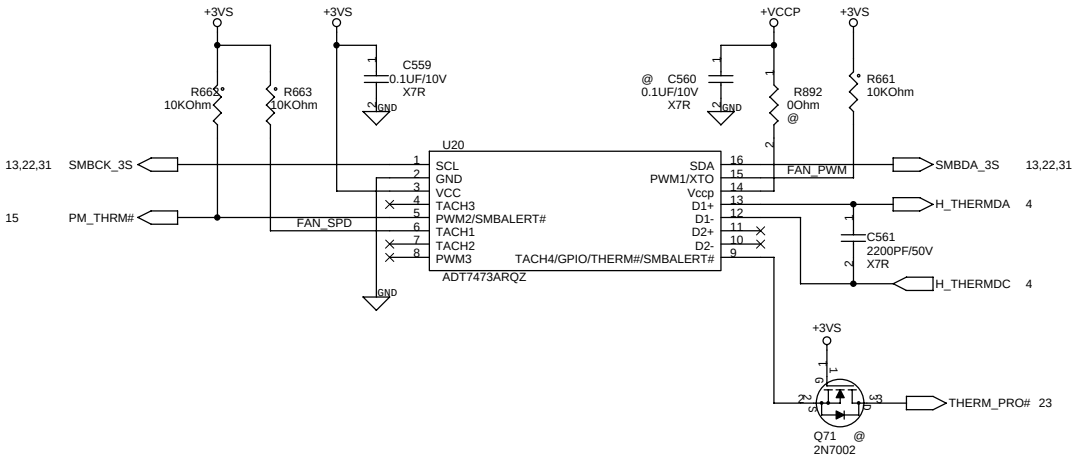


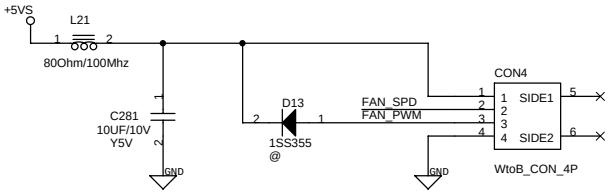


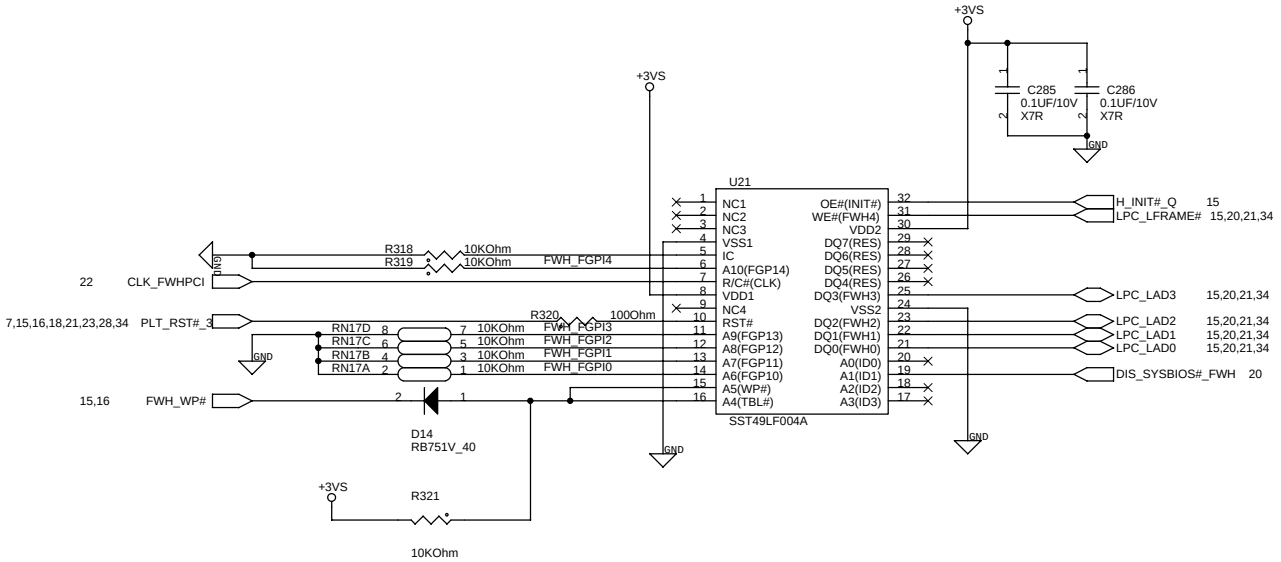




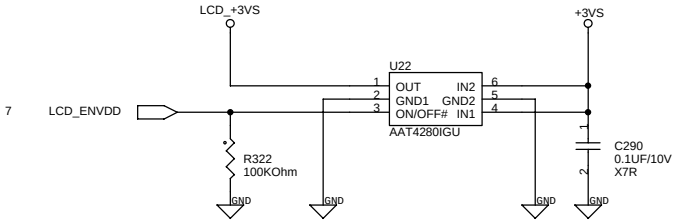
ASUSTek COMPUTER INC	Project Name: U5A	Engineer: HF_Lin	
Size: Custom	Title: AUDIO AMP -- MAXIM 9750		Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 25 of 46		

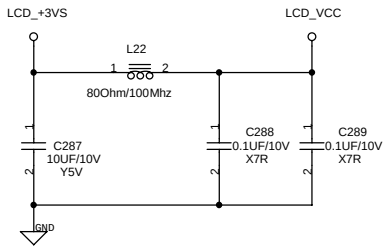


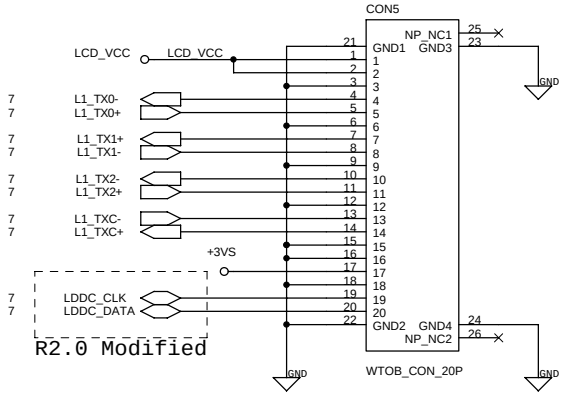




ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : FAN CONTROLLER / FWH	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 26 of 46	

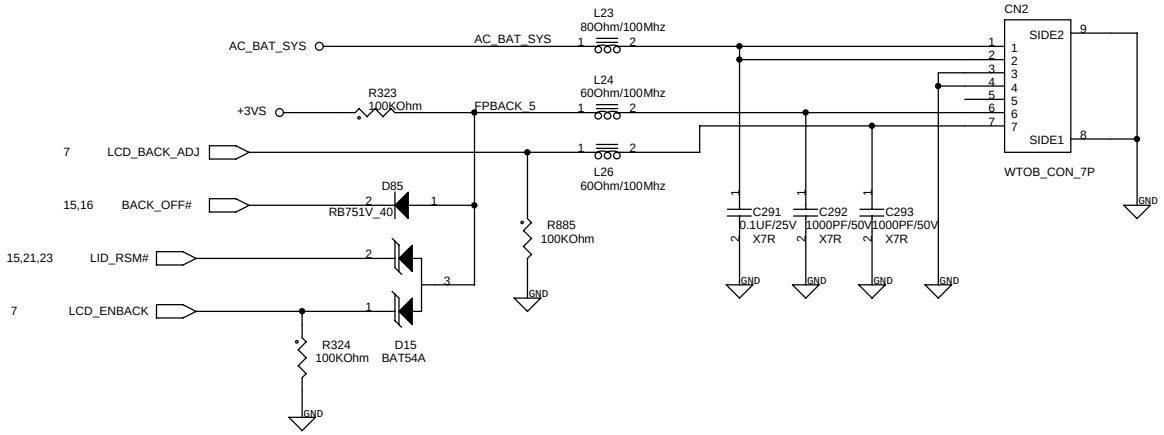




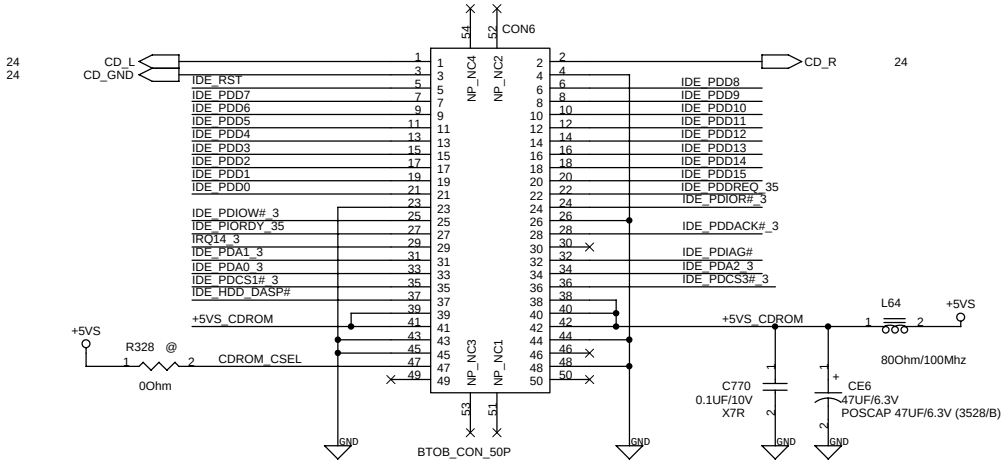


R2.0 Modified

current rating = 0.3A

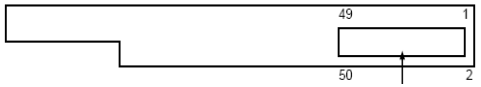


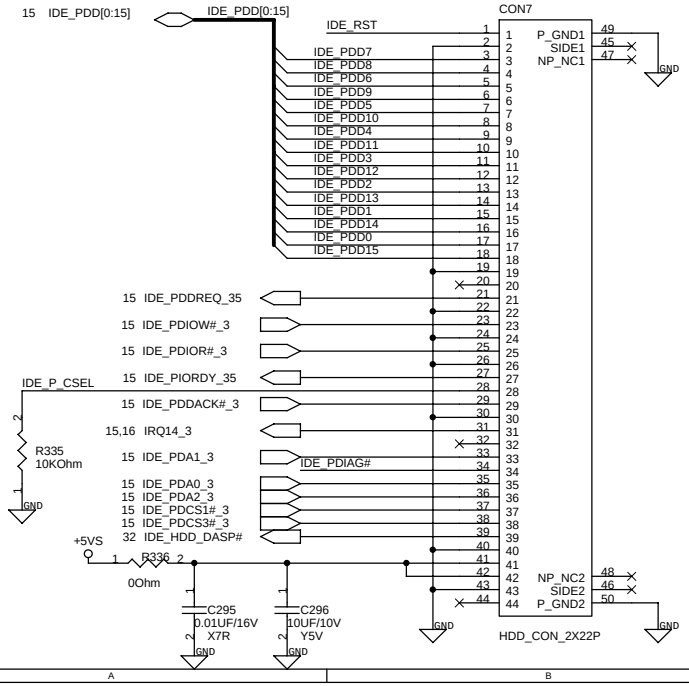
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : LCD CON	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 27 of 46	

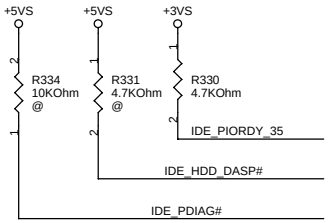


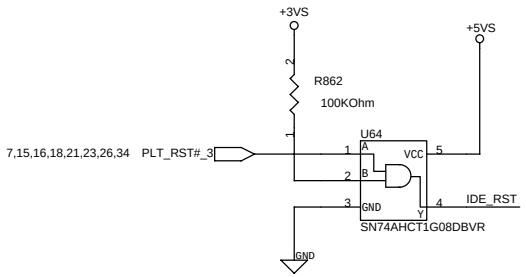
DVD/CDRW ROM
CSEL: H level = Slave
L level = Master

1	AUDIO-L	2	AUDIO-R
3	AUDIO-G	4	GND
5	-RESET	6	DD8
7	DD7	8	DD9
9	DD6	10	DD10
11	DD5	12	DD11
13	DD4	14	DD12
15	DD3	16	DD13
17	DD2	18	DD14
19	DD1	20	DD15
21	DD0	22	DMARQ
23	GND	24	-DIOR
25	-DIOW	26	GND
27	IORDY	28	-DMACK
29	INTRQ	30	-IOCS16
31	DA1	32	-PDIAG
33	DA0	34	DA2
35	-CS0	36	-CS1
37	-DASP	38	+5V
39	+5V	40	+5V
41	+5V	42	+5V
43	GND	44	GND
45	GND	46	Vender
47	CSEL	48	GND
49	Vender	50	Vender

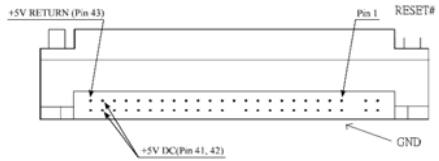








1	RESET-	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	(KEY)
21	DMARQ	22	GND
23	DIOW-	24	GND
25	DIOR-,	26	GND
27	IORDY,	28	CSEL
29	DMACK	30	GND
31	INTRQ	32	
33	DA1	34	PDIAG
35	DA0	36	DA2
37	CS0	38	CS1
39	DASP	40	GND
41	+5VDC	42	+5VDC
43	GND	44	Reserved



ASUSTek COMPUTER INC

Project Name: U5A

Engineer: HF_Lin

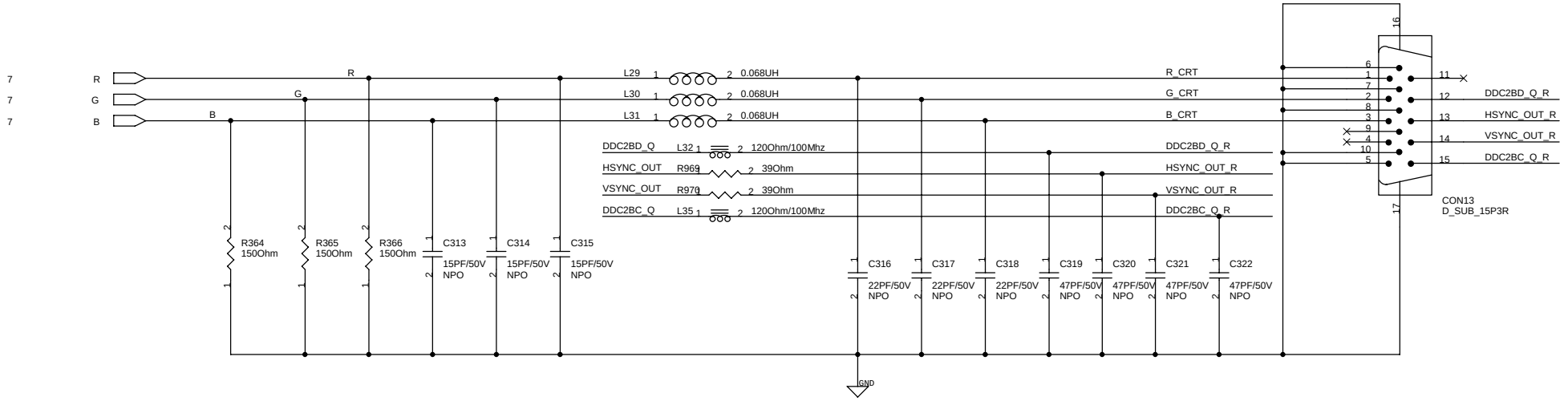
Size: Custom

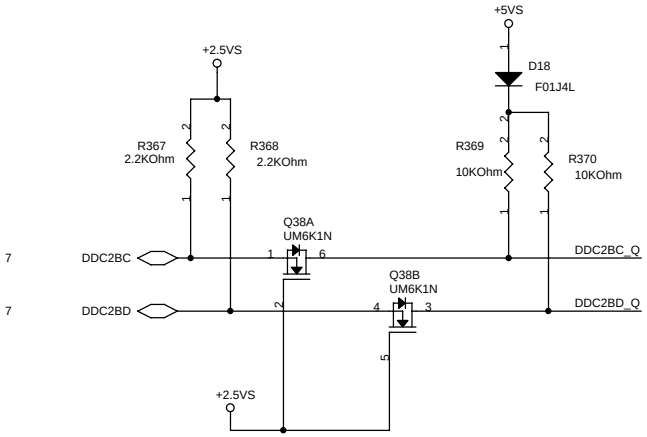
Title : HDD / CDROM CON.

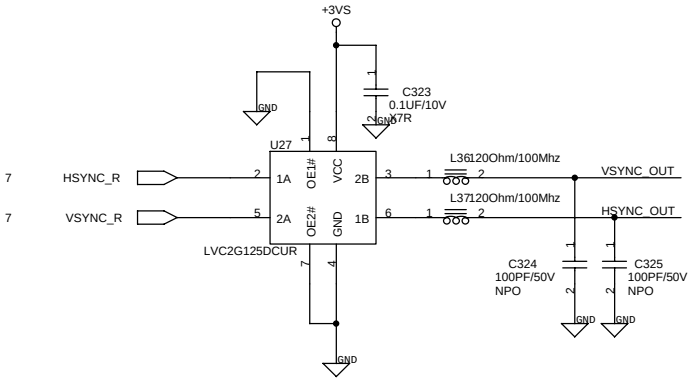
Rev: 2.0

Date: Tuesday, September 27, 2005

Sheet 28 of 46

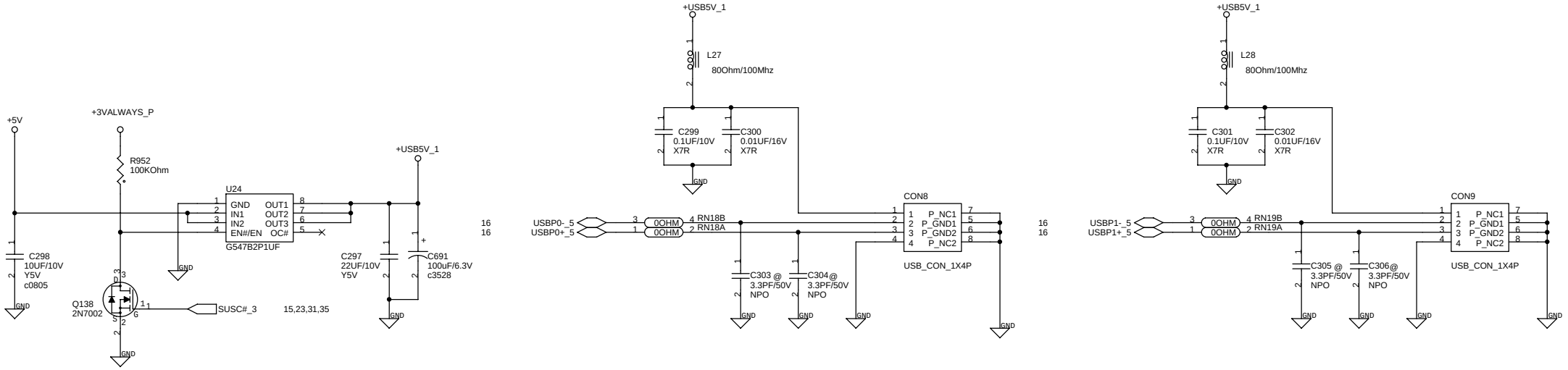


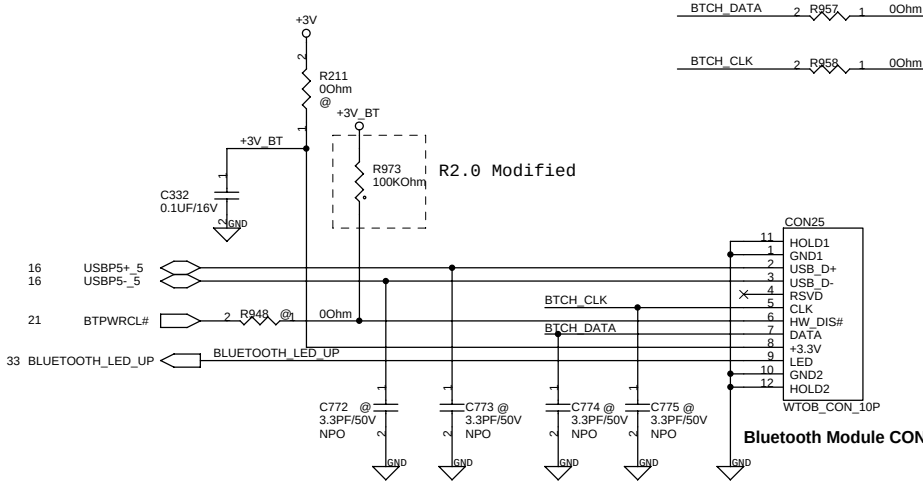




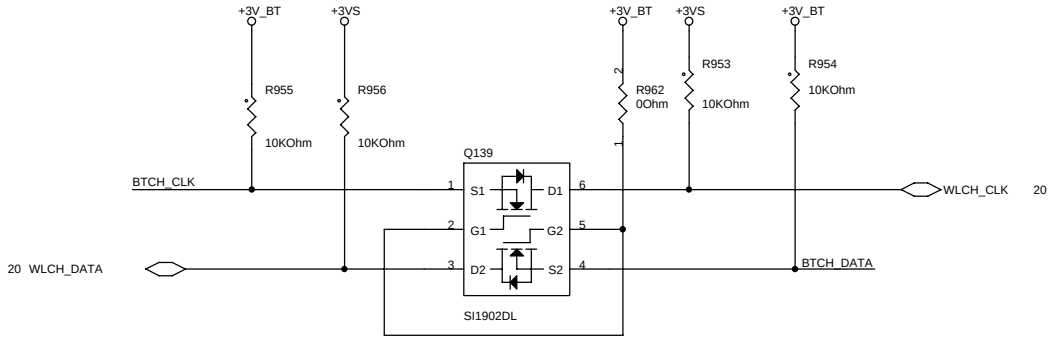
Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

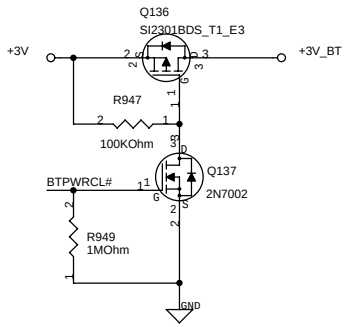
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 29 of 46	





Bluetooth Module CON

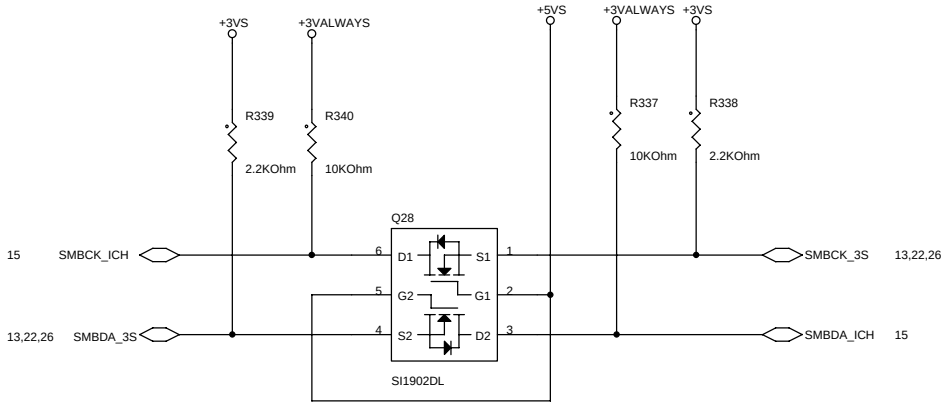


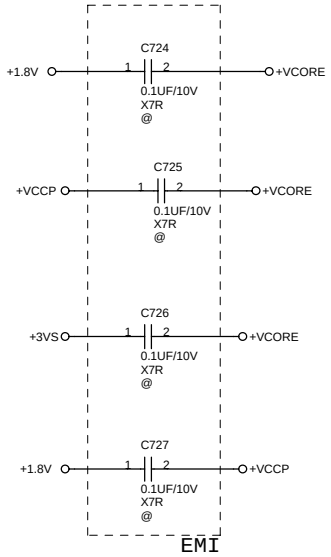


Pin Number Name Description

4 RSVD(PIO5) Reserved for BT_Active output to 802.11g for co-existence. This is optional if you need activity signaling scheme
5 BT_Priority/CH_Clk (PIO4) BT Priority AND Channel Clock for WCS
6 HW_DIS#(Optional) Disable BT Device when low
7 CH_Data(PIO6) Channel Data for WCS(Standard), or WLAN_Active input from 802.11b for Activity Signaling which is optional

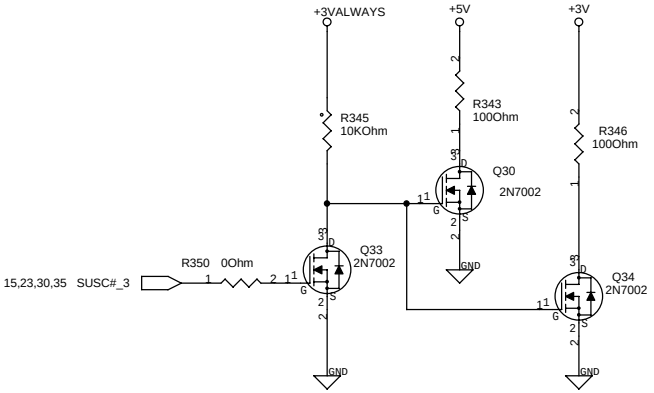
ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : USB / BLUE TOOTH CON.	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 30 of 46	

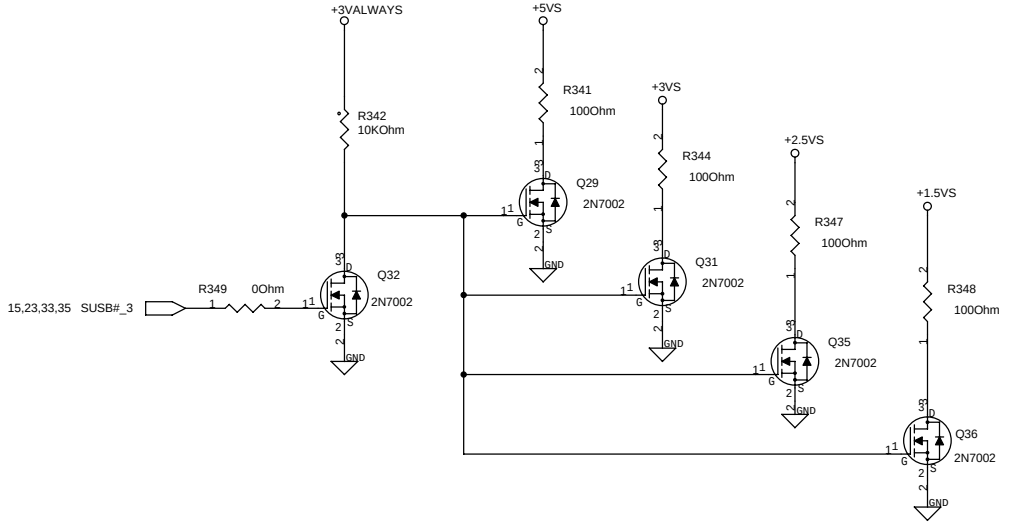




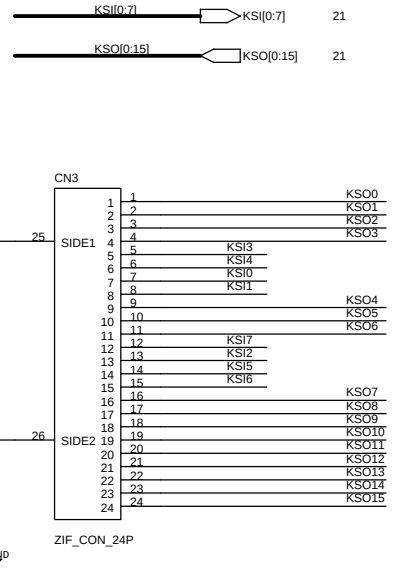
AC_BAT_SYS	AC_BAT_SYS	27,35,36,37,38,40,42
A/D_VIN	A/D_VIN	33,42
+5V	+5V	7,17,24,30,32,33,35,41
+5VS	+5VS	17,20,21,23,24,25,26,28,29,32,35
+3VALWAYS	+3VALWAYS	15,16,17,18,21,23,35
+3VALWAYS_P	+3VALWAYS_P	23,25,30,32,33,35
+3V	+3V	18,20,21,23,30,32,33,35,37,41
+3VS	+3VS	9,13,15,16,17,18,20,21,22,23,24,26,27,28,29,30,32,34,35,37,38,39,40
+2.5VS	+2.5VS	7,9,10,17,29,39
+1.8V	+1.8V	7,9,10,11,12,13,37
+1.5VS	+1.5VS	4,7,9,16,17,38
+1.5VALWAYS	+1.5VALWAYS	17,35
+0.9VS	+0.9VS	14,37
+VCC_GMCH	+VCC_GMCH	4,5,6,7,9,10,15,17,26,38
+VCCP	+VCCP	4,5,6,7,9,10,15,17,26,38
+VCORE	+VCORE	5,21,40
+VCC_RTC	+VCC_RTC	15,17,32
+5VA_CODEC	+5VA_CODEC	24,25
+5VA	+5VA	17,36,39
+2.5VREF	+2.5VREF	39,41,42

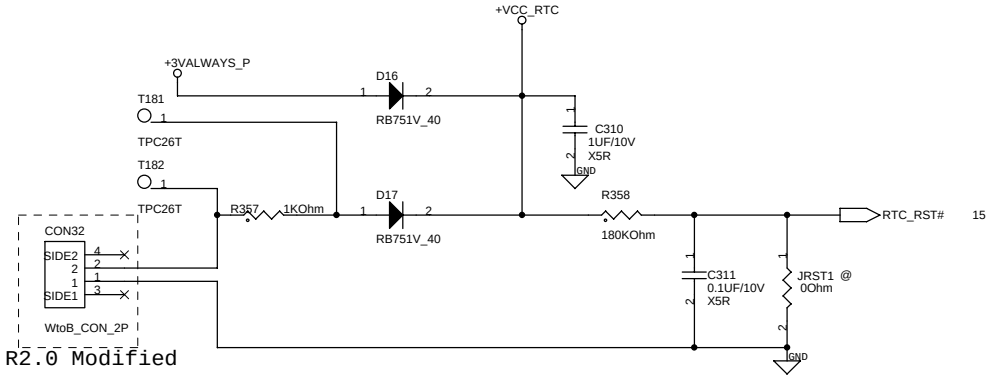
Discharge circuit for power fast down



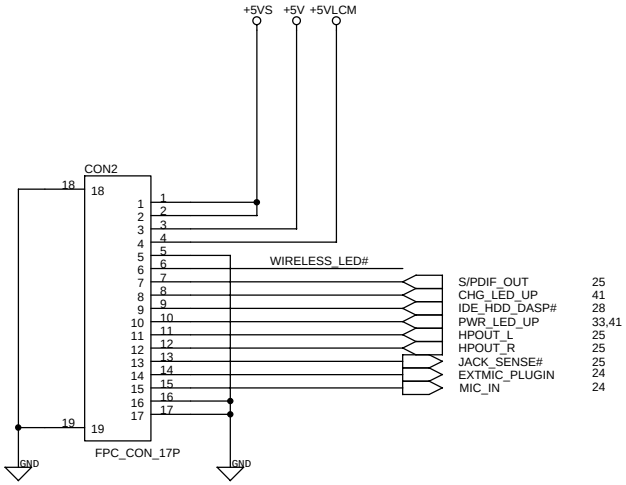


ASUSTek COMPUTER INC	Project Name	U5A	
	Engineer:	*HF_Lin*	
Size: Custom	Title :	SMBUS / DISCHARGE CIRCUIT	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet	31 of 46	

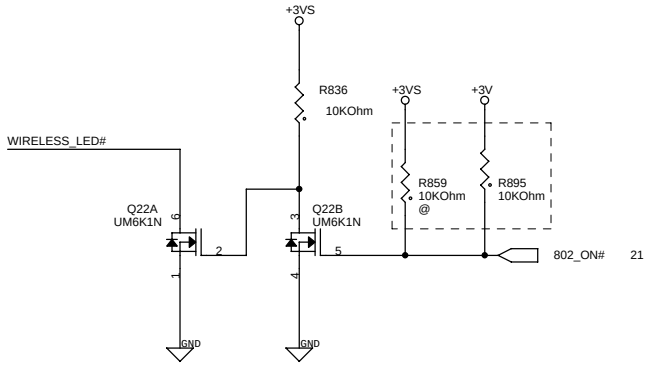


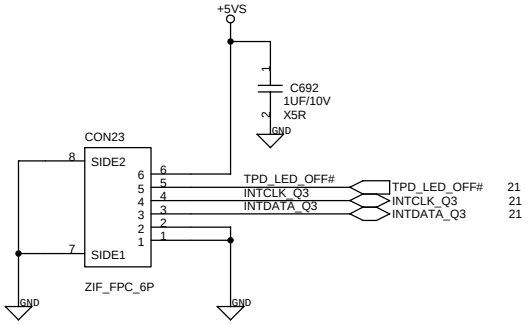


R2.0 Modified



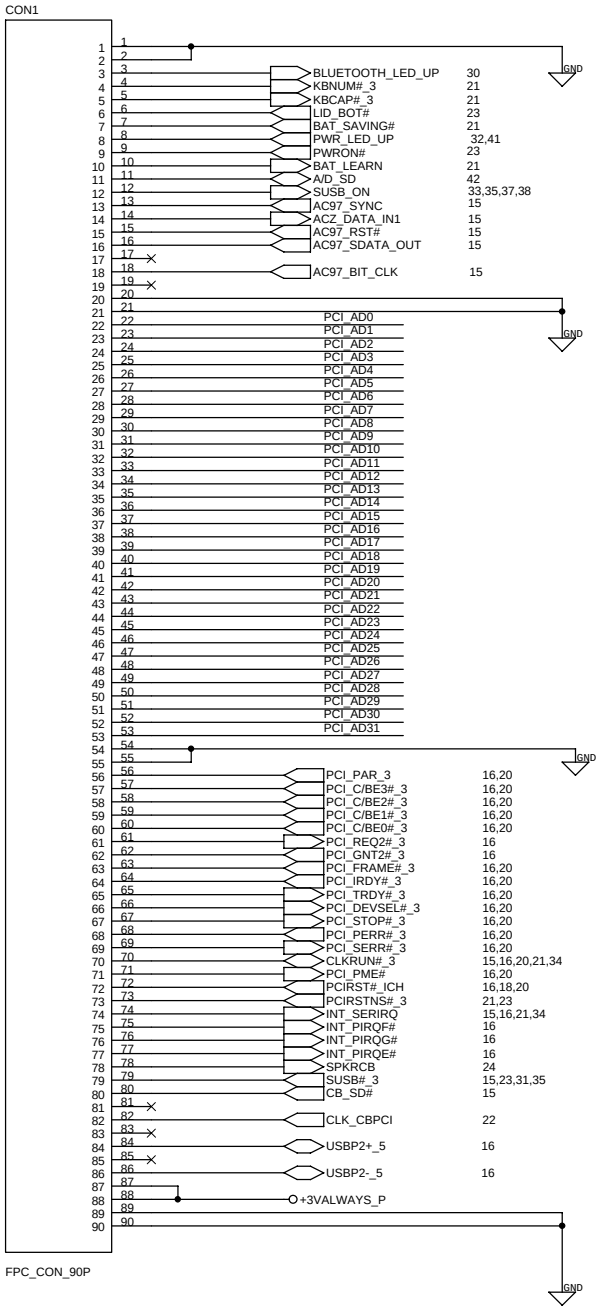
Audio Board



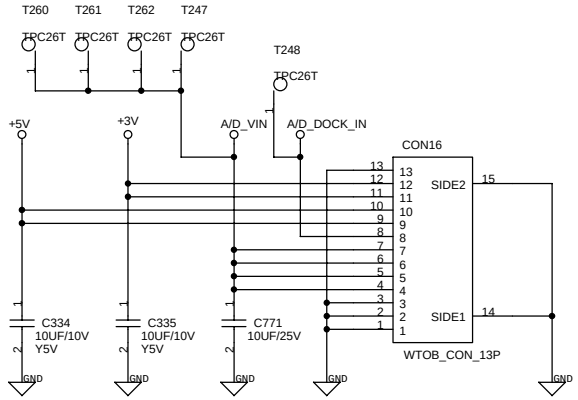


Touch PAD

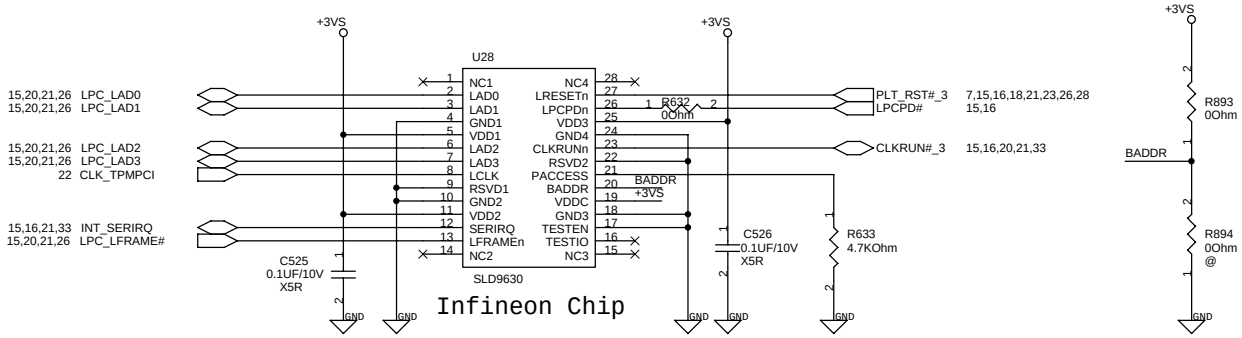
ASUSTek COMPUTER INC	Project Name	U5A	
	Engineer:	*HF_Lin*	
Size: Custom	Title :	RTCIN / KB / TPD	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet	32 of 46	

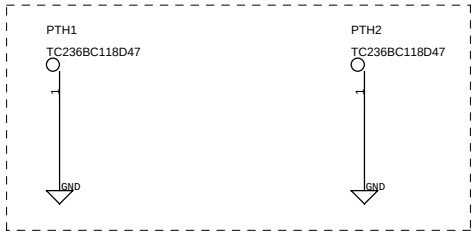


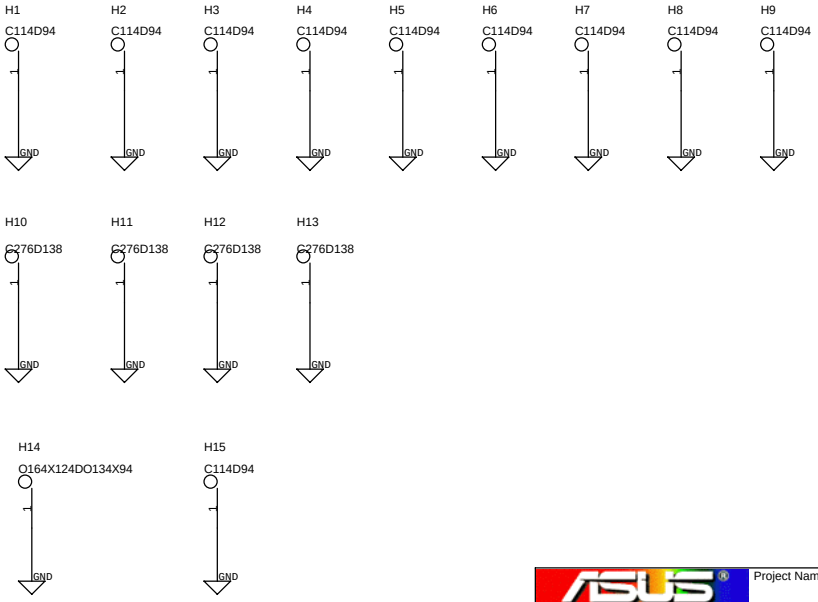
PCI_AD[0:31] PCI_AD[0:31] 16,20



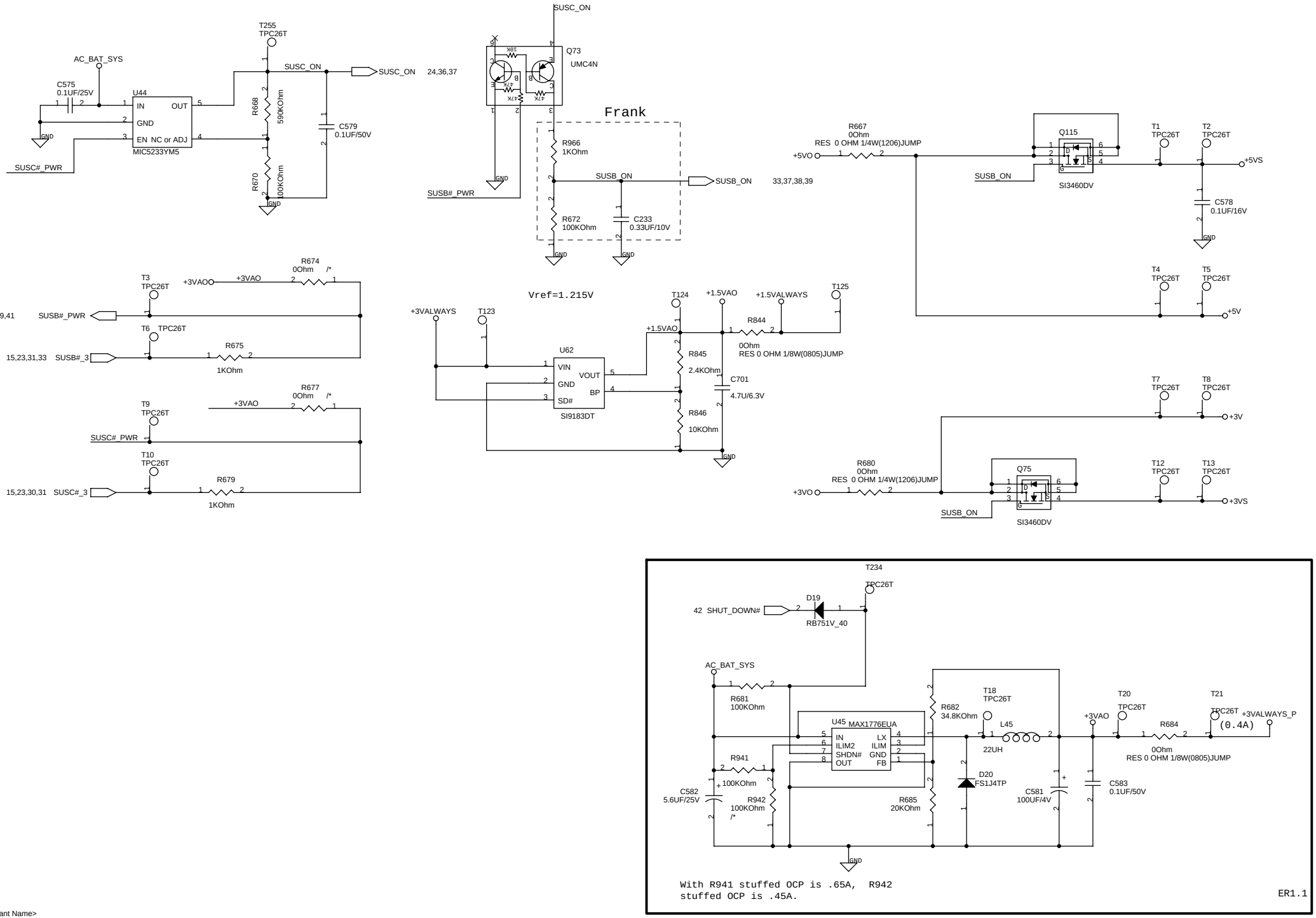
ASUSTek COMPUTER INC	Project Name: U5A		
	Engineer: *HF_Lin*		
Size: Custom	Title : BRIDGE MB and Sub_Board		Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 33 of 46		





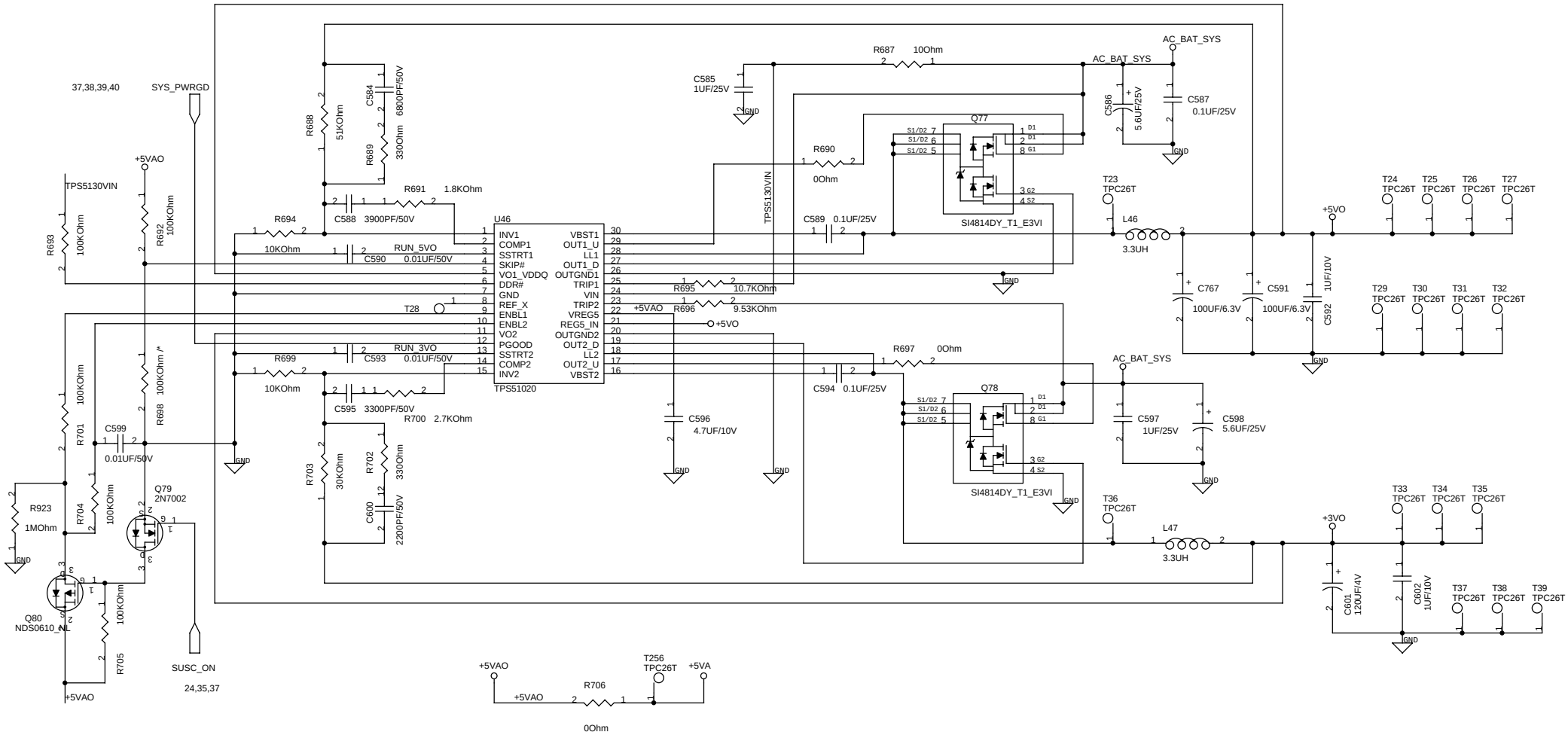


ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : TRUST PLATEFORM MODULE	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 34 of 46	



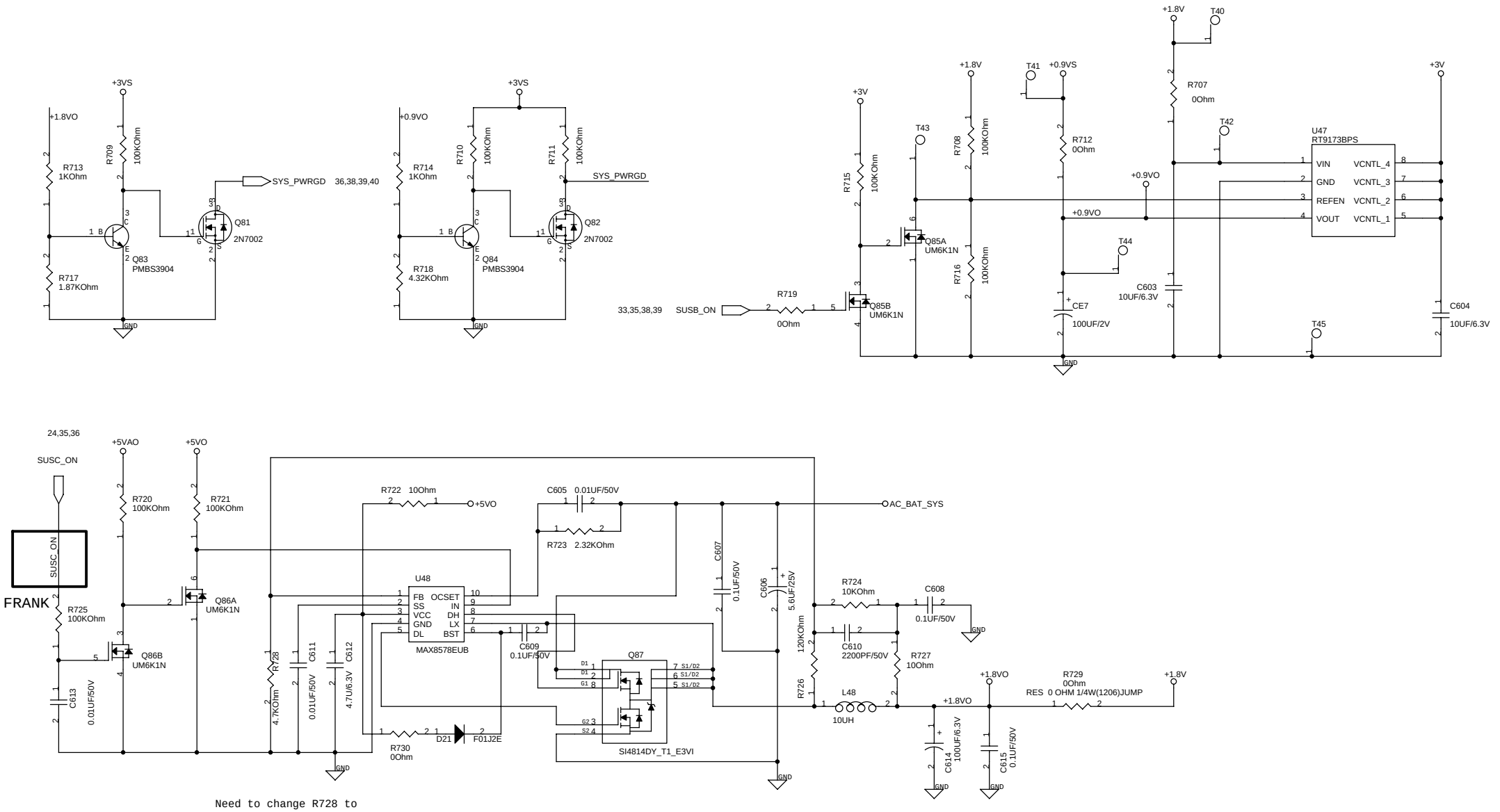
<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: LOAD SHITCH +3VALWAYS PWRGD	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 35 OF 46		RELEASE DATE :	



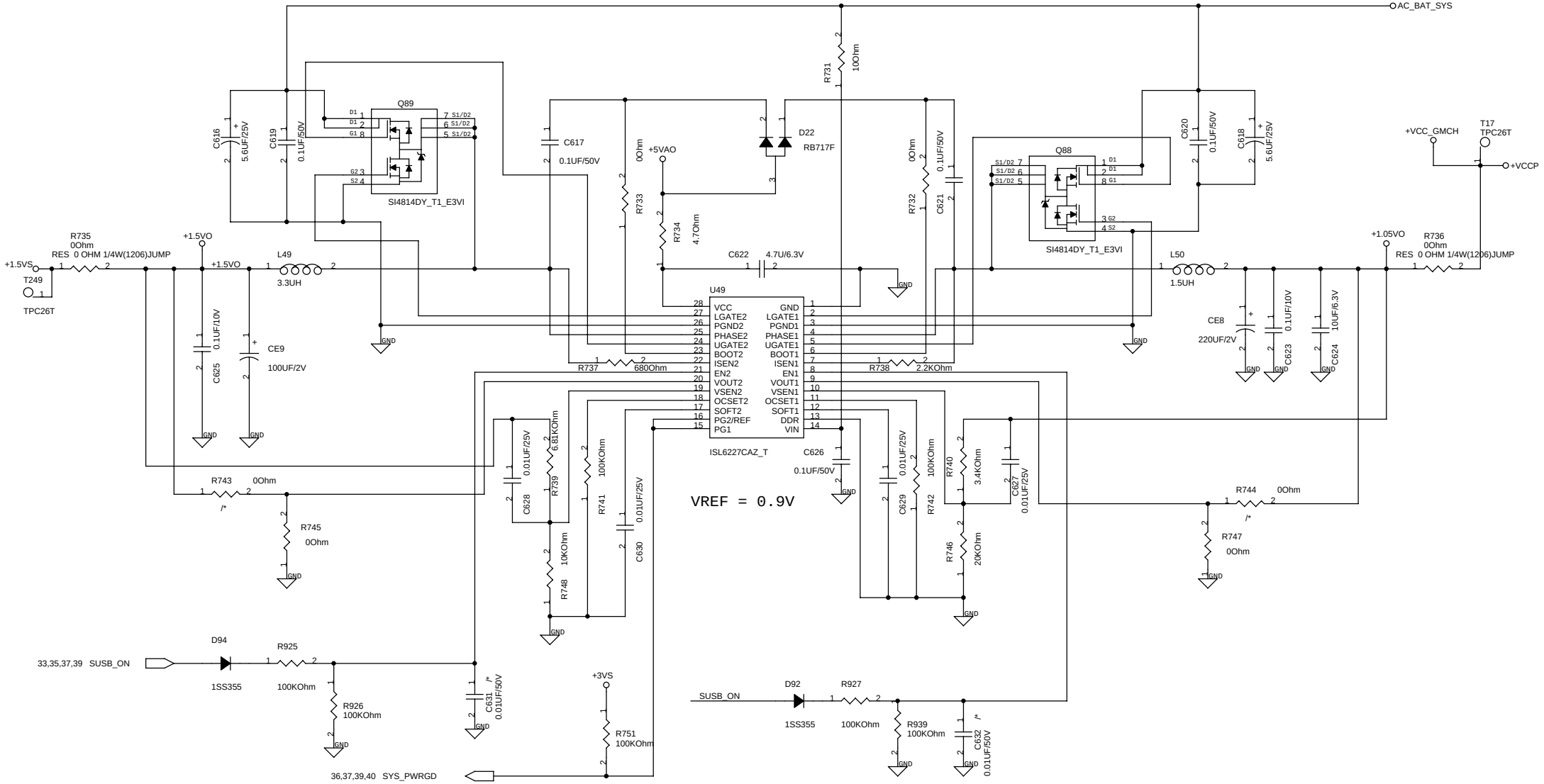
<Variant Name>

PROJECT: **U5A**	REVISION **2.0**	DATE: **Tuesday, September 27, 2005**	DESCRIPTION: ***SYSTEM***	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET **36** OF **46**		RELEASE DATE :	



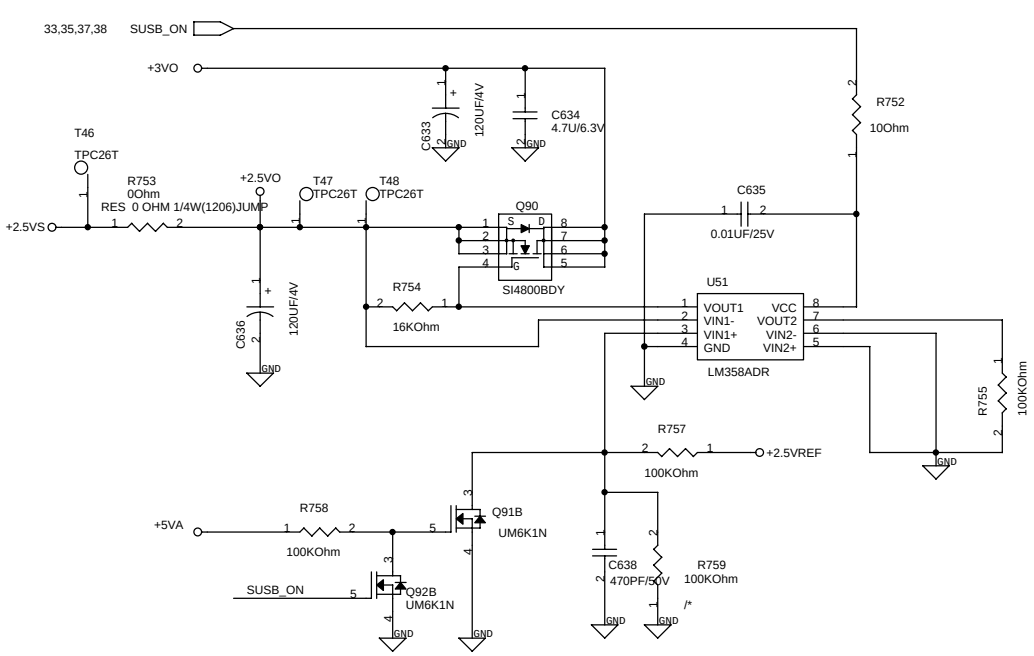
<Variant Name>

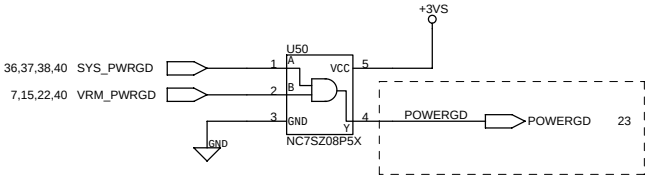
PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: 1.8V & DDR2	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 37 OF 46		RELEASE DATE :	

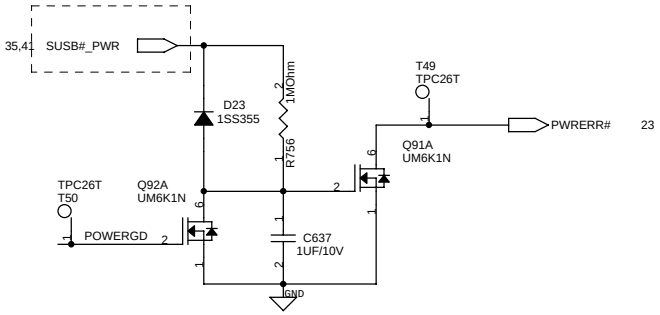


<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: 1.05VS/1.5VS	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 38 OF 46		RELEASE DATE :	

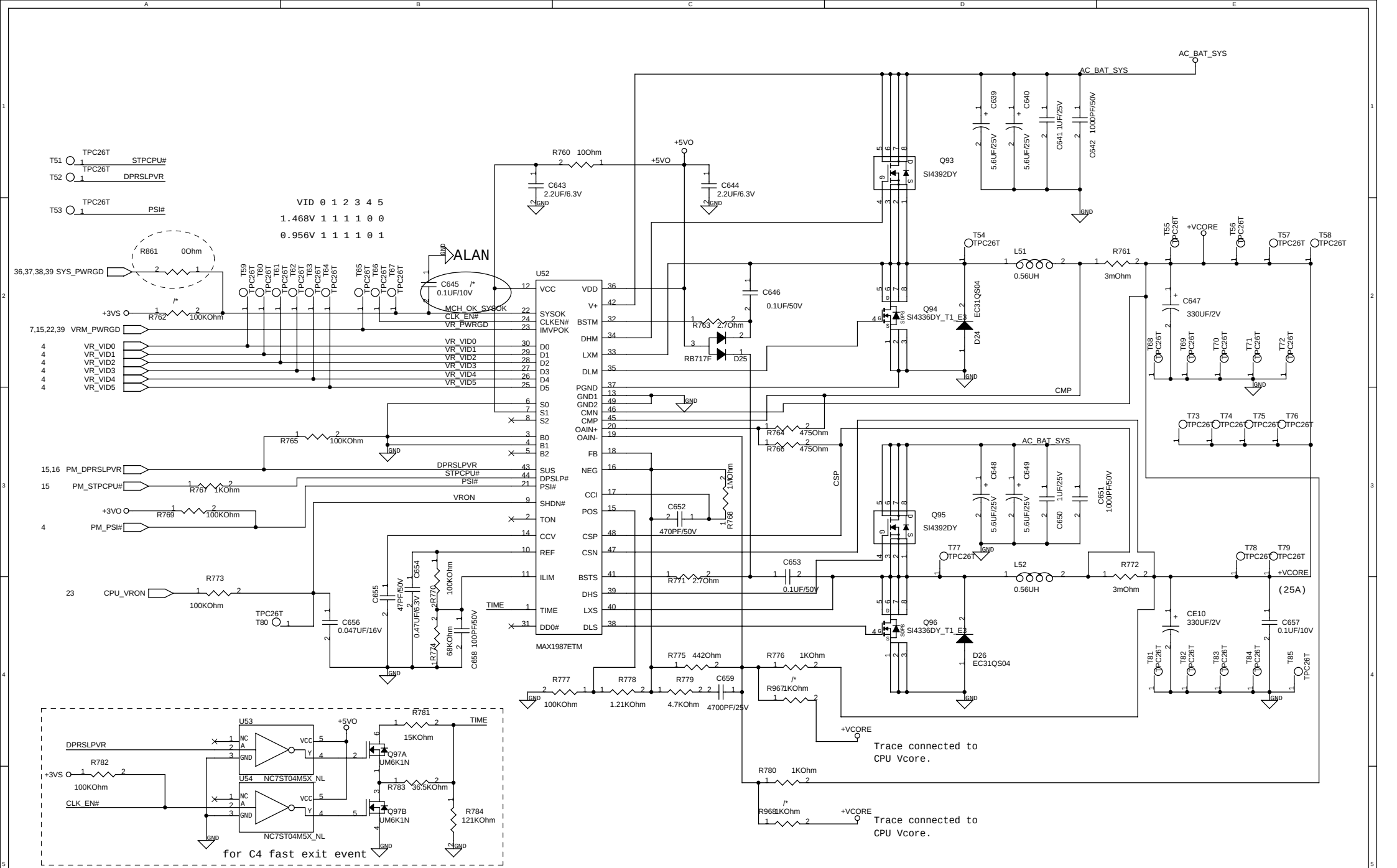






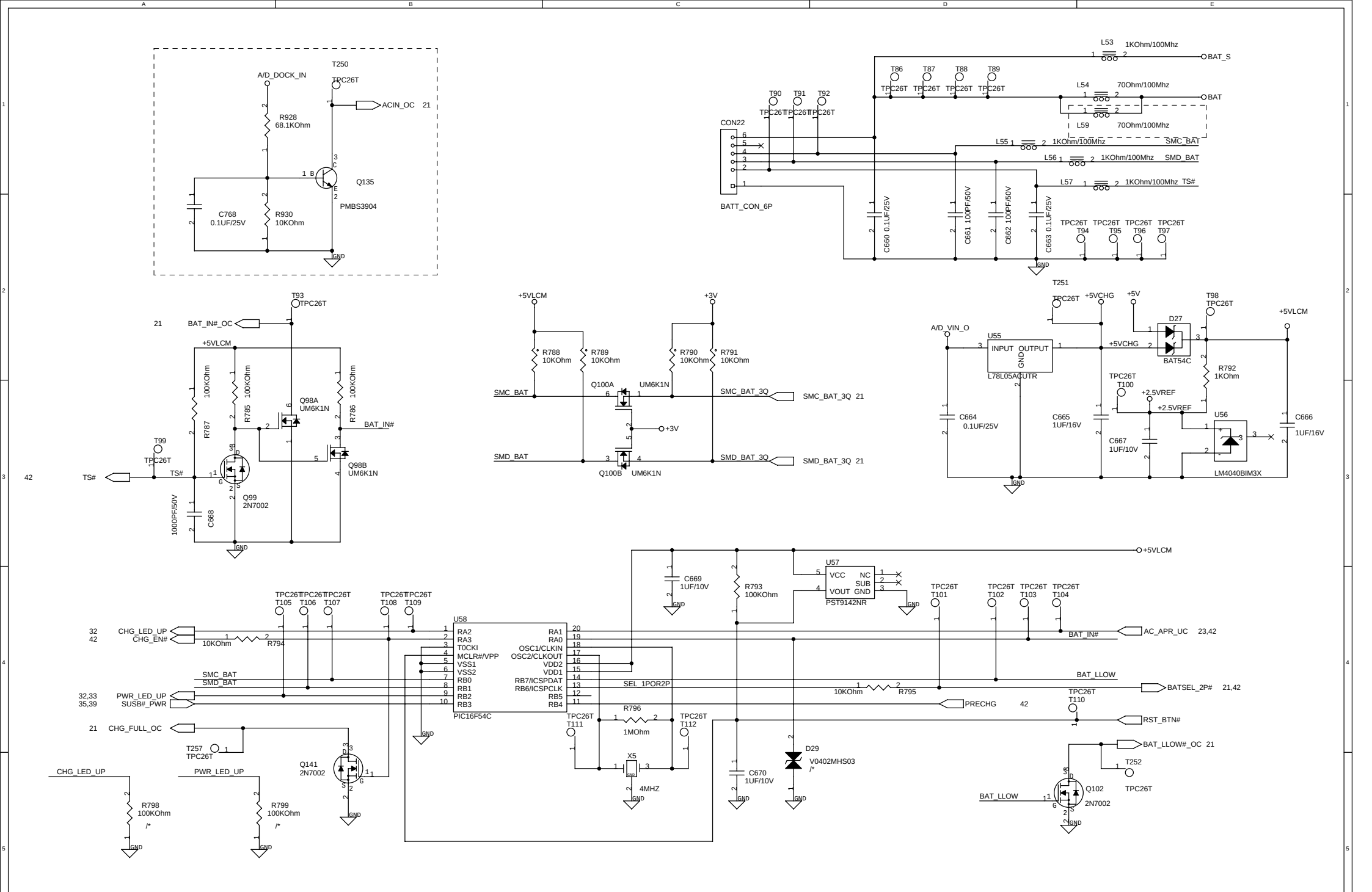
<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: 2.5VS_PWRGD	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 39 OF 46		RELEASE DATE :	



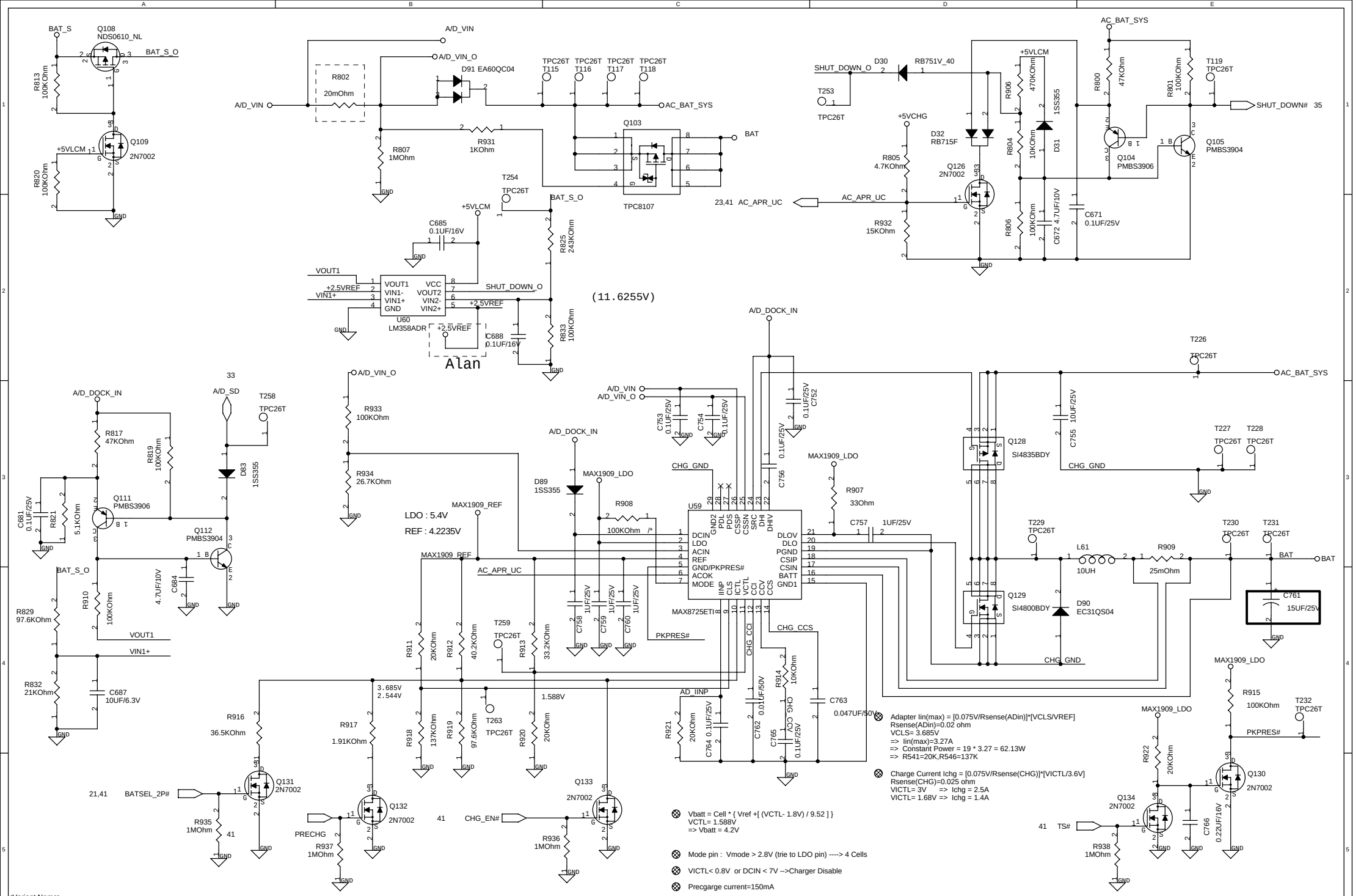
<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: VCORE	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 40 OF 46		RELEASE DATE :	



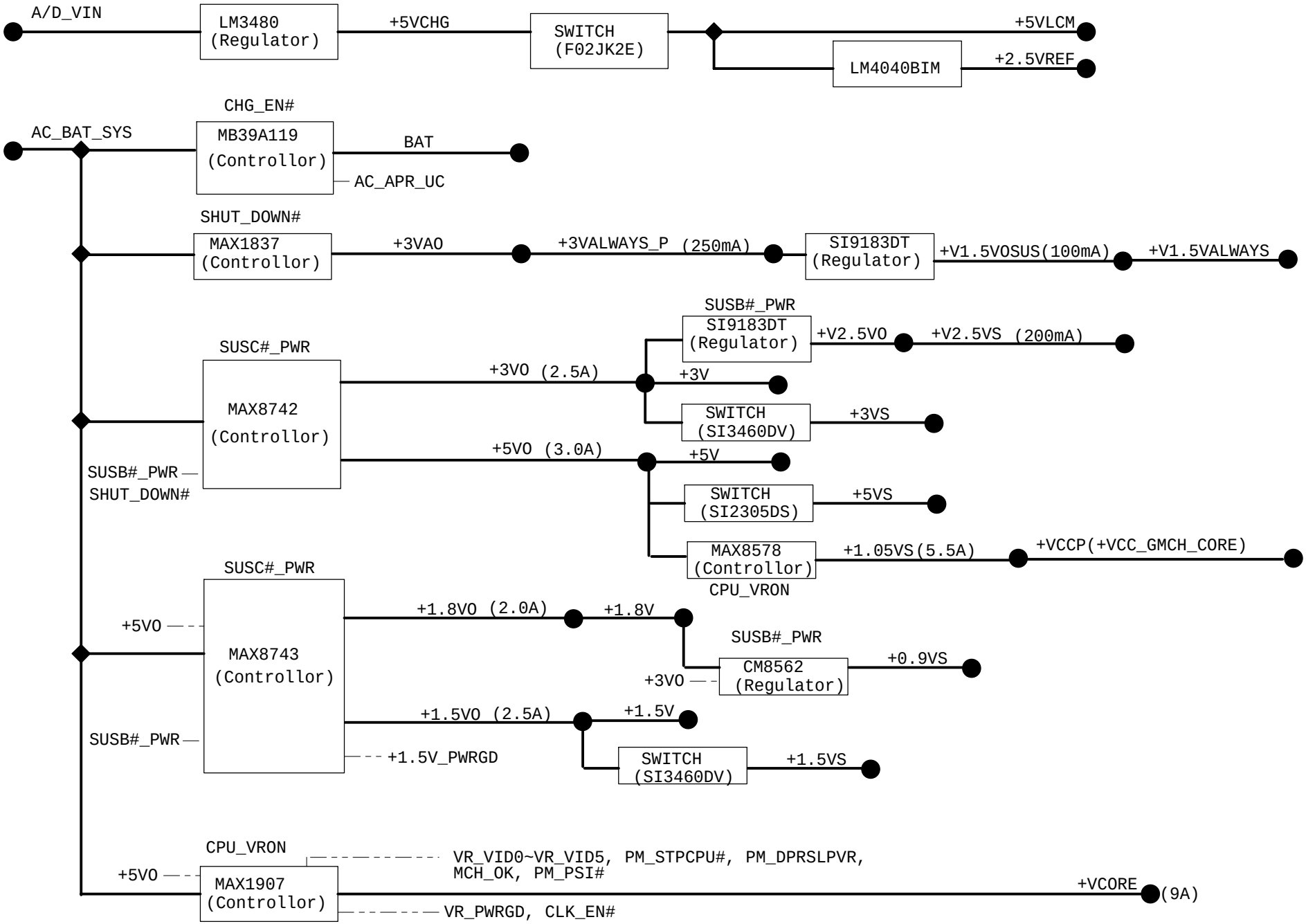
<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 41 OF 46	DCIN_BATCON_BATIN_+5VLCM_PIC	RELEASE DATE :	

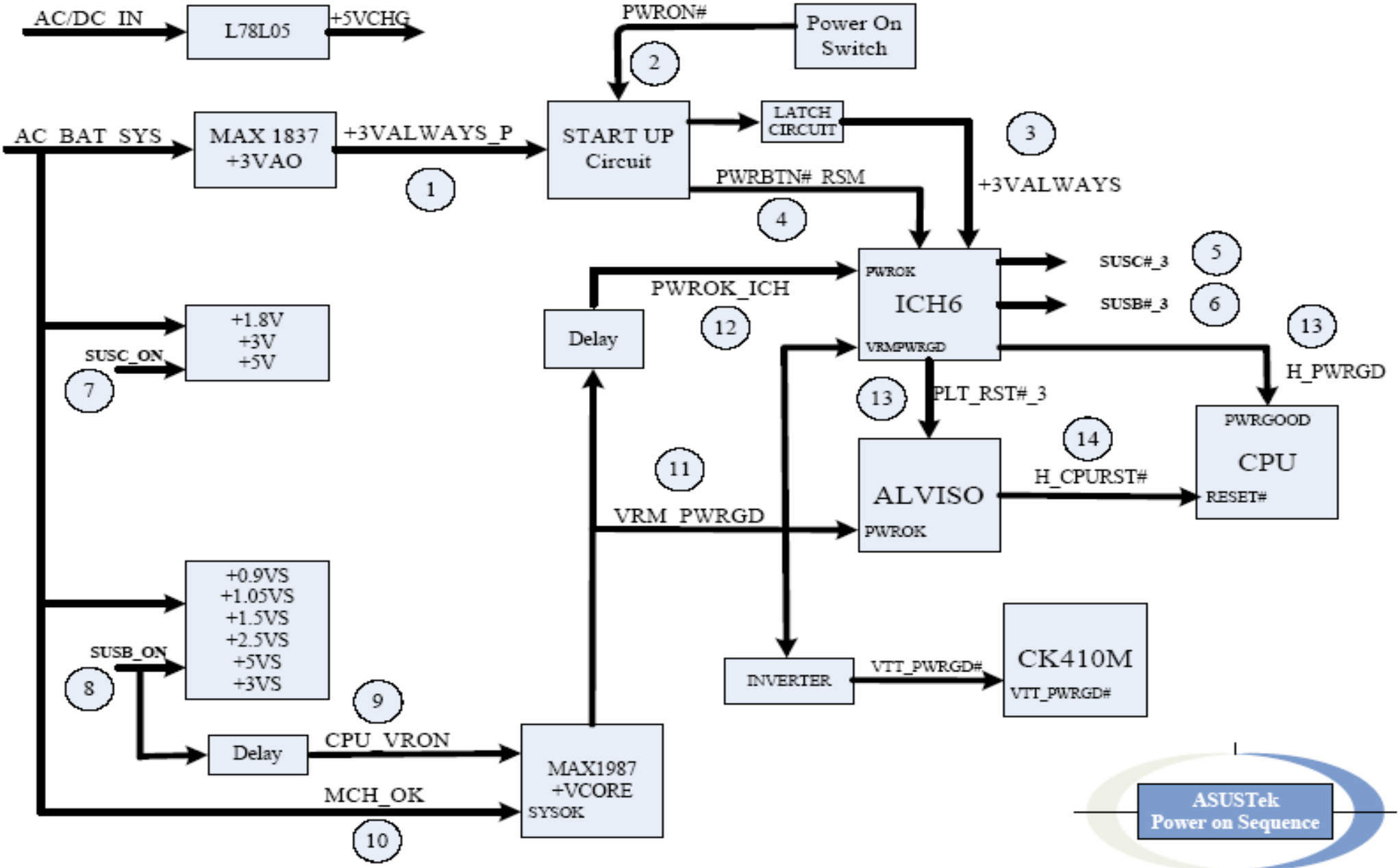


<Variant Name>

PROJECT: U5A	REVISION 2.0	DATE: Tuesday, September 27, 2005	DESCRIPTION: CHARGER	SCHEMATIC FILE NAME :		DESIGN ENGINEER :
		SHEET 42 OF 46		RELEASE DATE :		



ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : Power Flowchart	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 43 of 46	



ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : Revision History	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 44 of 46	

Revision History

Rev1.1_EE

1. Replace LAN controller Marvell 8001 with RealTek 8111B because of large power consumption of 8001 when system power on----------Page 18.
2. Change audio codec vender from RealTek ALC861VS to ADI1986A for cost issue. ----------Page 24.
3. Add a cap (22pF) to CLK_KBCPCI for EMI issue ----------Page 22.
4. The net BTPWRCL# need be pulled up to +3V through a resistor due to port 53 is open drain ---------- Page 21.
5. Replace internal mic near codec to solve the white noise problem ---------- Page 24.
6. Remove C620 to avoid damage HDD motor. ----------Page .
7. Add a EC pin (port 57)to control the TPD LED on / off (synchronous to Fn+F9) ----------Page 21 .
8. Delete the Pin 5 of CON2 (LID_BOT#) and connect to ground. ----------Page 32.
9. Replace net AC/DC_In with A/D_DOCK_IN due to D91 is removed to main board from I/O board ----------Page 33.
10. Connect pin 88 of CON1 to +3VALWAYS_P and swap PWR_LED_UP from pin 88 to pin 8 ----------Page 33.
11. Add a GPIO pin (CODEC_SHDN#) to switch +5VA_CODEC power on or off ----------Page 24.
12. Add a circuit to control power of blue tooth ----------Page 30.
13. Remove HDD protection IC circuit----------Page 34.
14. Add a control circuit to dominate USB power for avoiding that self power leakage current flow into +5V when system is powered off. ----------Page 30.
15. Add a MOS to control wirless on or off ----------Page 20.
16. Change vender of DDR2 SODIMM connector from QUASAR to TYCO for cost issue. ----------Page 13.

Rev 2.0_EE

1. Swap pin of RTC battery to match battery module define. ----------Page 32.
2. R896 need be pulled up to +3VS to solve problem S3 (S4) wake on LAN failed issue. ----------Page 18.
3. Change R156 value from 1K ohm (2.2 volt) to 680 ohm (3.3 volt) for correcting PCIE_WAKE# level. ----------Page 18.
4. Remove C269 to solve pop noise when entry S3 state----------Page 25.
5. Remove LAN power control circuit ----------Page 18.
6. Remove ODD device power control circuit ----------Page 28.
7. Redefine pin define of CON5 to support EDI and color enhanced function----------Page 27.
8. Change D8 compoment from F01J4L to F01J2E to provide corrct level (0.42 volt --> 0.24 volt)of back_off# after LID_RSM# actived----------Page 23.
9. Change C579 value to sovle that power button LED and power LED will flash once after power off system----------Page 35.
10. Add a 100k ohm to CON25.6 to provide correct level----------Page 30.
11. Reserve caps on each pin of CON26 for ESD issue----------Page 30.

ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: *HF_Lin*	
Size: Custom	Title : Revision History	Rev: 1.0
Date: Tuesday, September 27, 2005	Sheet 45 of 46	

Revision History

Rev1.1_Power

1. Page 40: Changed net name from "MCH_OK" to "SYS_PWRGD"
2. Page 36: Added R923(1M) ohm resistor for dischargging voltage to Q80.3; R695 changed to 7.47K(increase OCP); R696 changed to 9.53K(increase OCP).
3. Page 36: +5V ouput current upgraded from 2.5A to 4.5A changed L46 to 3.3uH and added C767 (100uF/6.3V). Changed L46 to 3.3uH.
4. Page 37: Changed C610 to 3300pF (increase frequency to reduce ripple current); R726 changed to 120K, R728 changed to 4.7K, R723 changed to 4.7K.
5. Page 38: Changed L50 to 3.3uH (to meet transient spec). R742 to 100K ohm (OCP). R741 to 100K ohm (OCP).
6. Page 40: R775 to 442 ohm, R764 and R766 to 475 ohm to lower the droop voltage. C647 and CE10 to 330uF to meet transient spec. R774 to 63.4K (OCP 30A).
7. Page 42: Changed charger IC (U59) from MB39A119 to MAX8725.
8. Page 38: Added components (D924, R925, R926, D92, R927, R939) to make sure the enable pins (U49.21, U49.8) does not exceed 5V.
9. Page 42: Added D91, this diode is removed from the I/O BD.
10. Page 41: Changed net name on U55.3 to "A/D_VIN_O".
11. Page 35: Updated 3VAO circuit to 600mA.
12. Page 37: The enable signal to +1.8V changed to“SUSC_ON.
13. Page 42: Q103 source is connected to AC_BAT-SYS.
14. Page 42: C761 foot print changed to C7343d-h122.

Rev1.2_Power

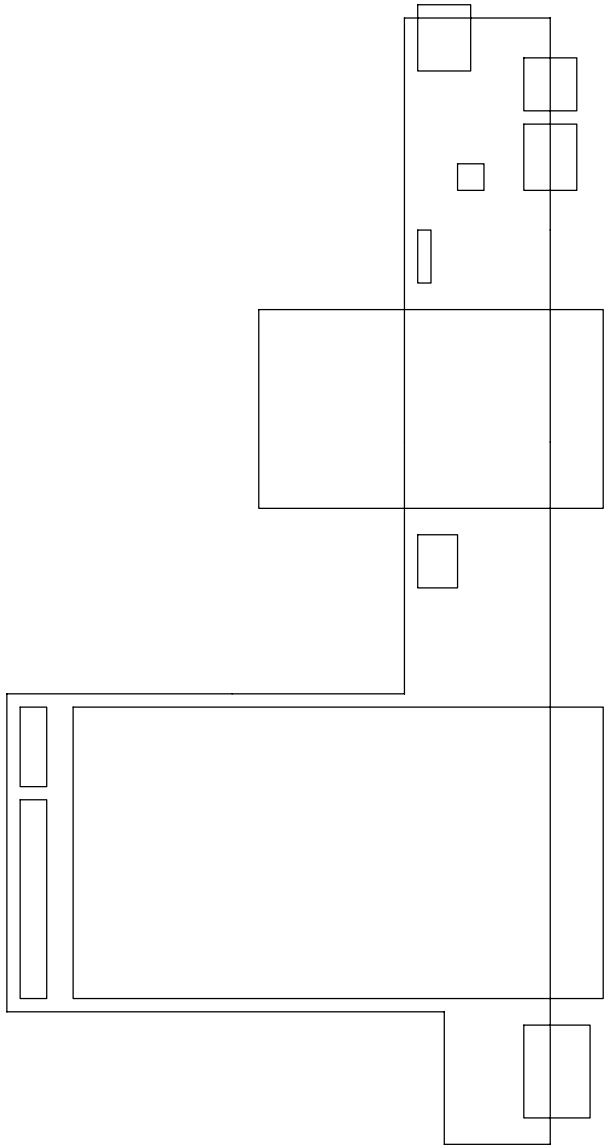
1. Page 42: After SMT, changed R908 to /*, this is 3 battery charge voltage setting. Replaced R802 with 20m Ohm resistor to improve total power.
2. Page 36: Changed C585 footrpint to C0805.
3. Page 35: After SMT, changed R942 to /*, R941 is stuffed with 100KOhm. This is to increase OCP for +3VALWAYS from .45A to .65A. Changed C579 from 1uF to 0.1uF to speed up SUSC_ON time.
4. Page 37: Changed R723 to 2.32K OCP2.5A. Changed C610 to 2200pF, increase frequency from 190KHz to 240KHz. Changed R728 to 4.53K, Vout 1.811V.
5. Page 38: Changed L50 to 1.5uH/10A, changed L49 to 3.3uH/3.5A to improve transient response.
6. Page 40: Changed C641, C651 to 1000pF/50V X7R 10%.
7. Page 37: Changed D21 footprint to "sod323".
8. Page 40: 8/31/05 Added two more resistors for sensing the Vcore voltage more accurately.
9. Page 42: 9/5/05: changed Q103 to Fairchild part because Toshiba does not respond to GA.
10. Page 35: 9/5/05: changed Q73 to Rohm part because Toshiba does not respond to GA.
11. Page 41: 9/5/05: Changed L54 and L59 to 3A bead. U58.3 tied to Gnd.
12. Page 40: 9/8/05: Changed Q93 and Q95 to SI4932, changed Q94 and Q96 to SI4336.
13. Page 40: 9/9/05: Changed L51 and L52 to .56uH/15A 10 x 10 mm packaging to solve thermal issue.

ASUSTek COMPUTER INC	Project Name: U5A	
	Engineer: HF_Lin	
Size: Custom	Title : Revision History	Rev: 2.0
Date: Tuesday, September 27, 2005	Sheet 46 of 46	

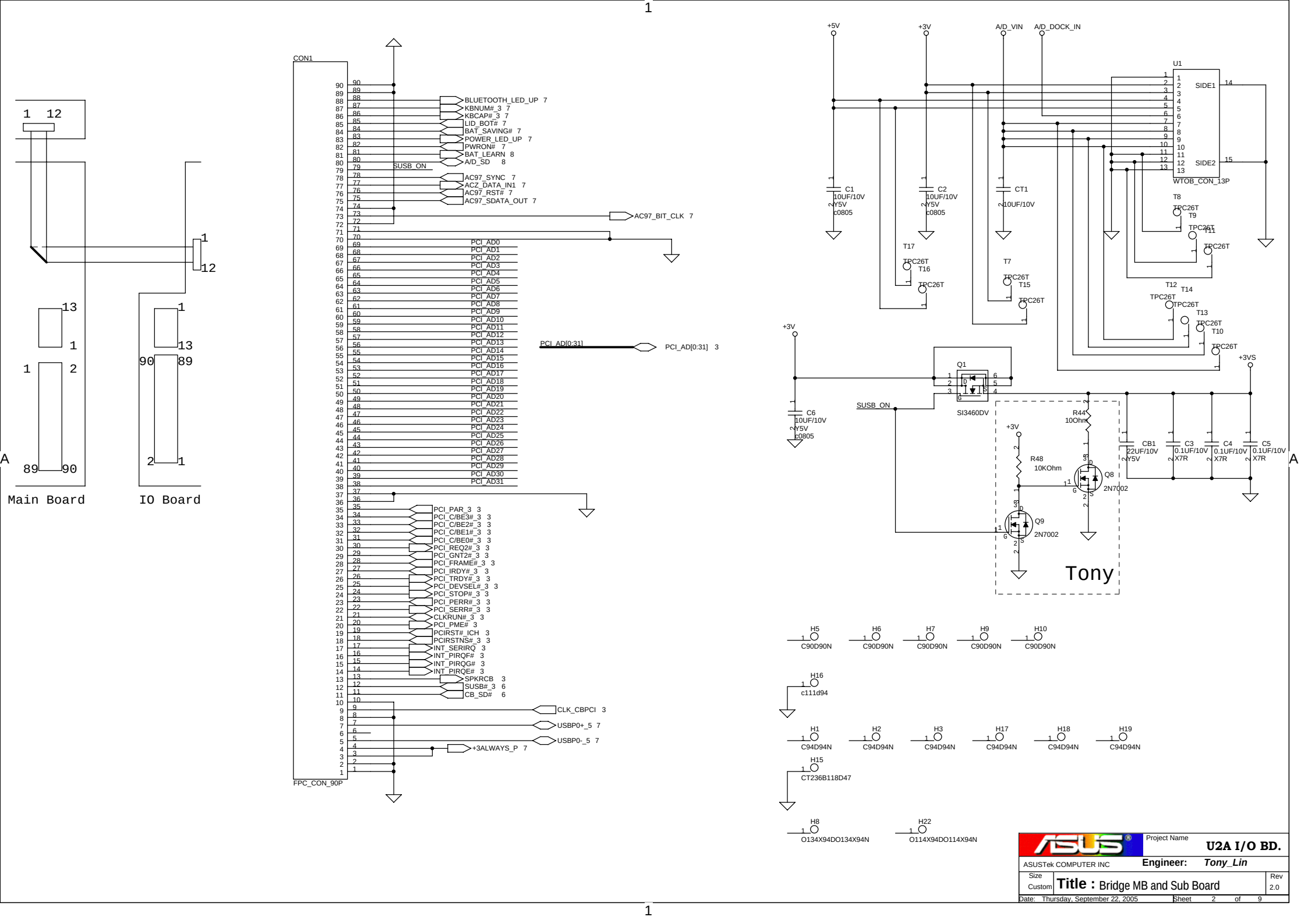
PROJECT U5A IO & Audio Board

Revision History

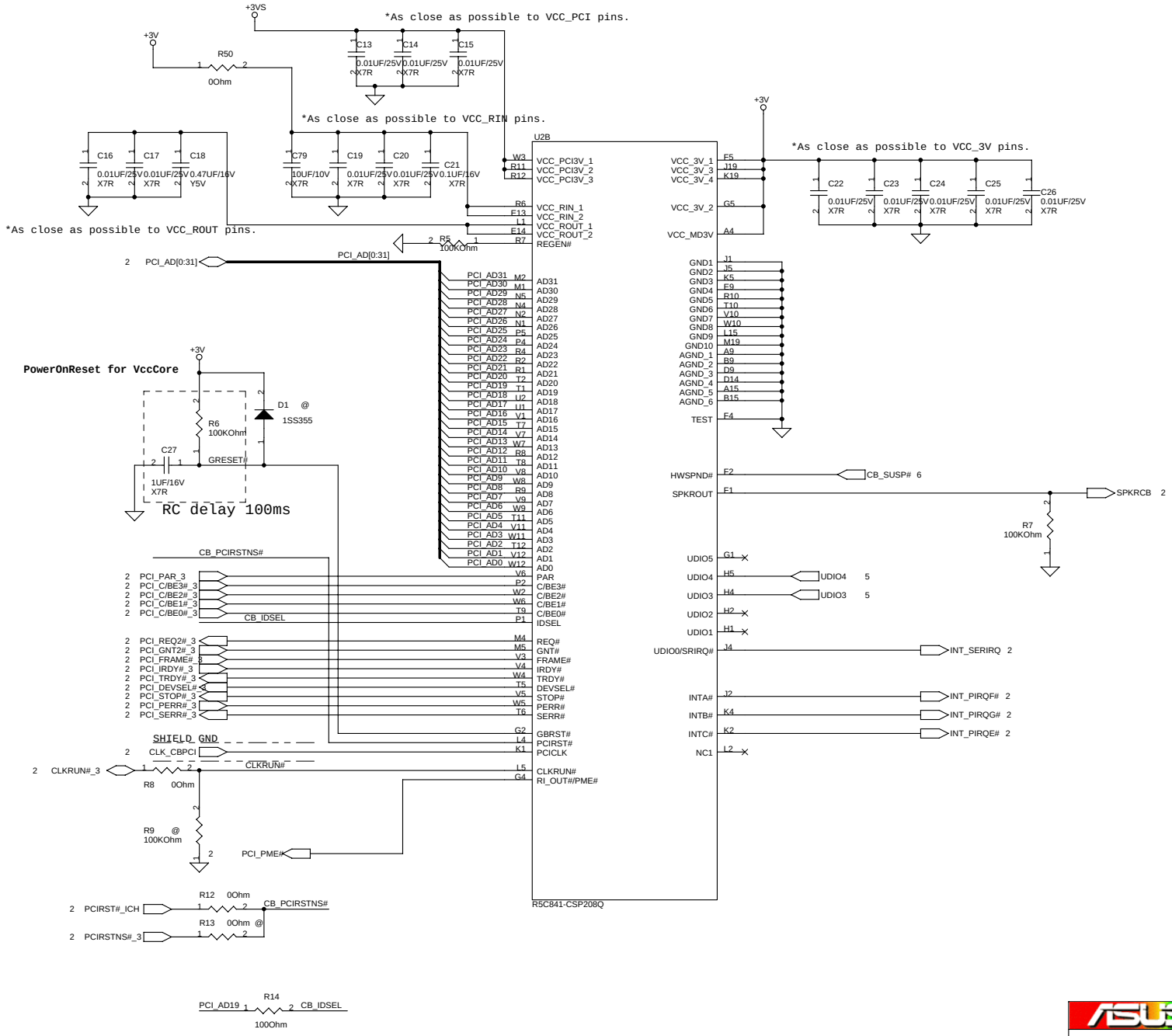
R1.0	SR	2005/01/17
R1.1	SR	2005/06/2
R1.2	ER	2005/07/6
R2.0	PR	2005/09/21



ASUSTek COMPUTER INC	Project Name: U2A I/O BD.	
	Engineer: Tony_Lin	
Size: Custom	Title : Table of Contens	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 1 of 9	



ASUSTek COMPUTER INC	Project Name: U2A I/O BD.	Engineer: Tony_Lin
Size: Custom	Title : Bridge MB and Sub Board	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 2 of 9	


*As close as possible to VCC_PCI pins.
*As close as possible to VCC_RIN pins.
*As close as possible to VCC_ROUT pins.
*As close as possible to VCC_3V pins.
U2B
R5C841-CSP208Q
PCI_AD[0:31]
PowerOnReset for VccCore
RC delay 100ms
SHIELD_GND
CB_PCIRSTNS#
CB_IDSEL
CLKRUN#
PCI_PME#
R14
100Ohm
Project Name
U2A I/O BD.
ASUSTek COMPUTER INC
Engineer: Tony_Lin
Title : RICOH 5C841/PCI_B
Size Custom
Rev 2.0
Date: Thursday, September 22, 2005
Sheet 3 of 9

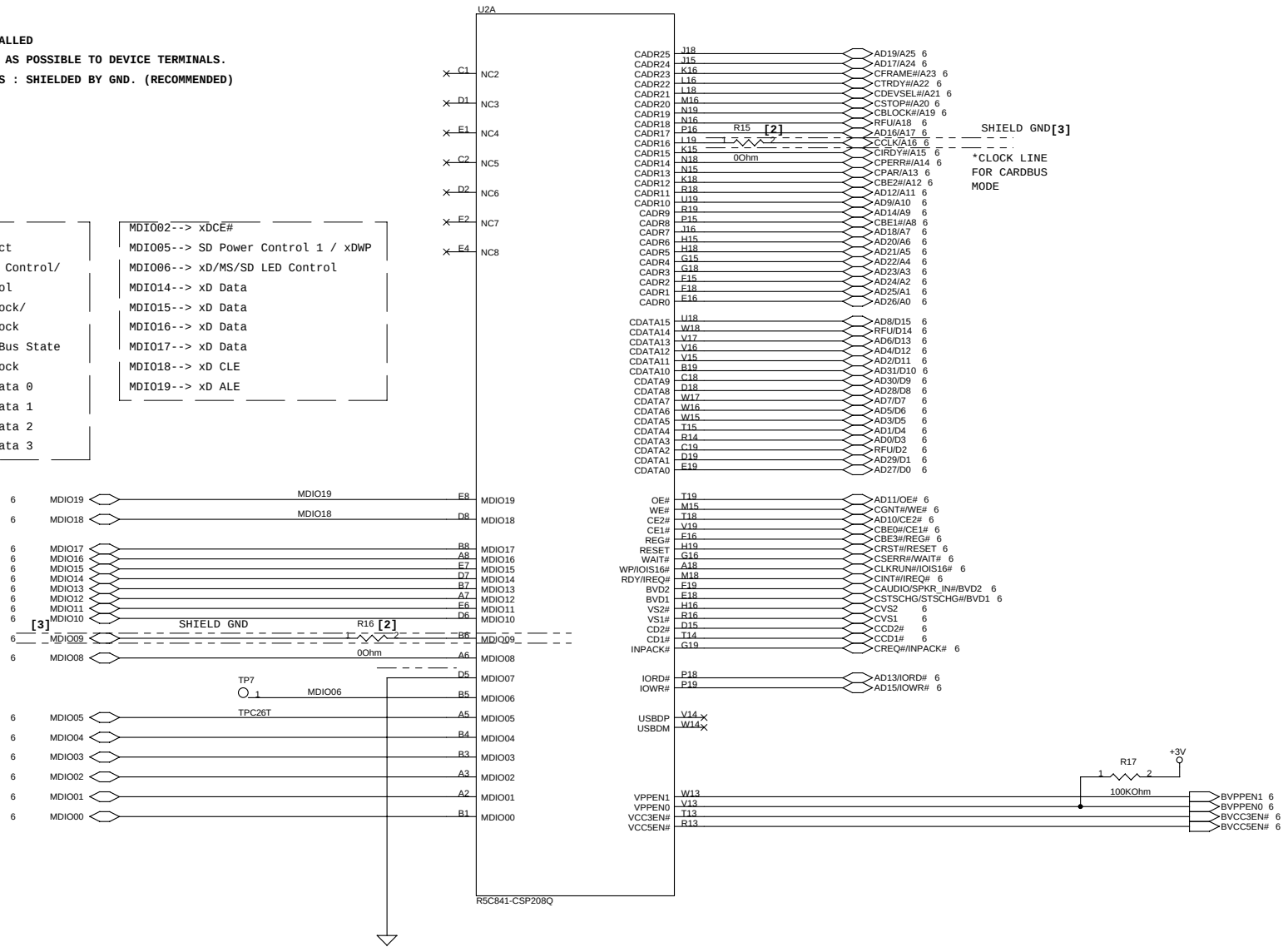
[1] NOT INSTALLED

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

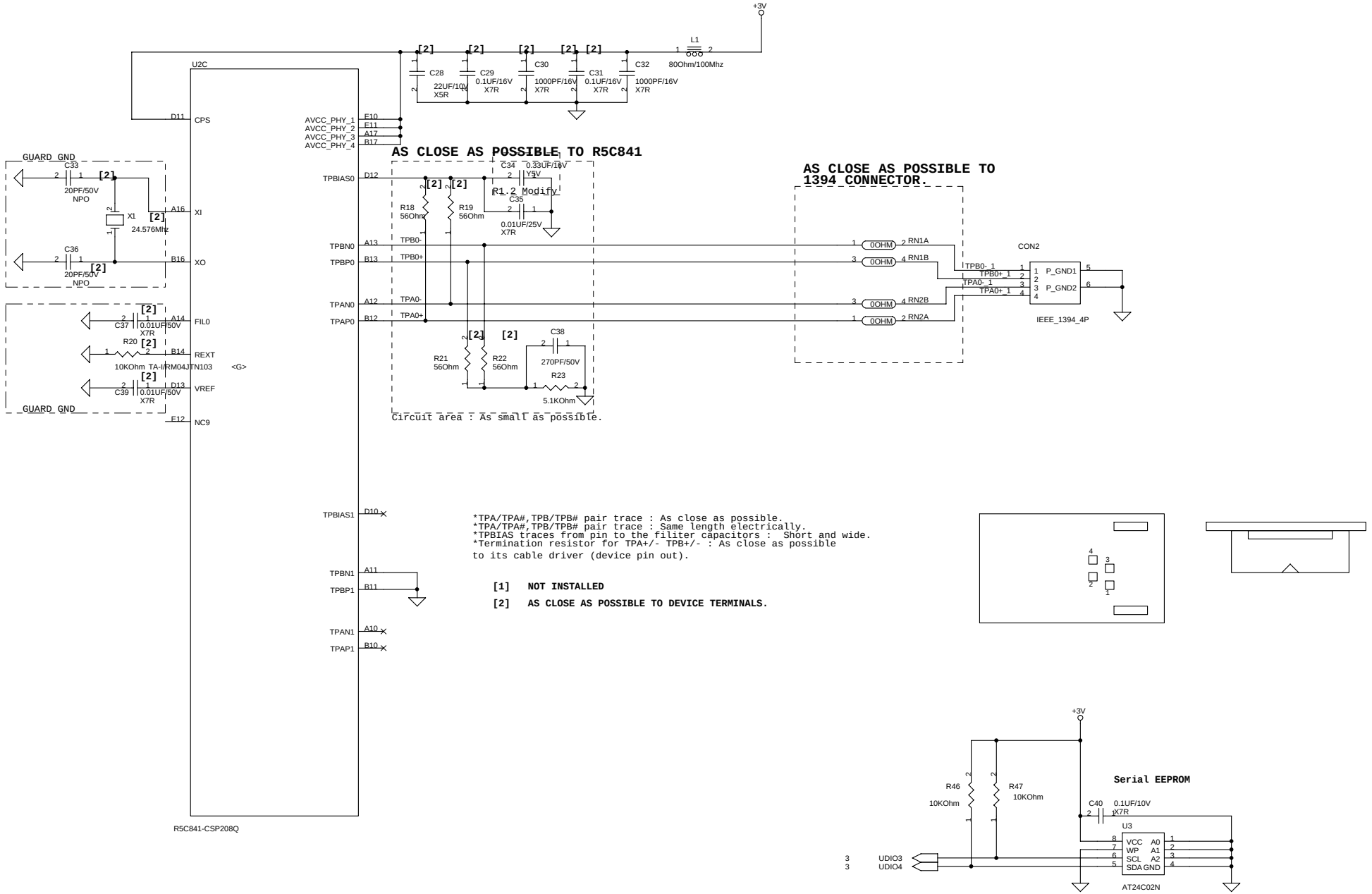
[3] CLK LINES : SHIELDED BY GND. (RECOMMENDED)

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

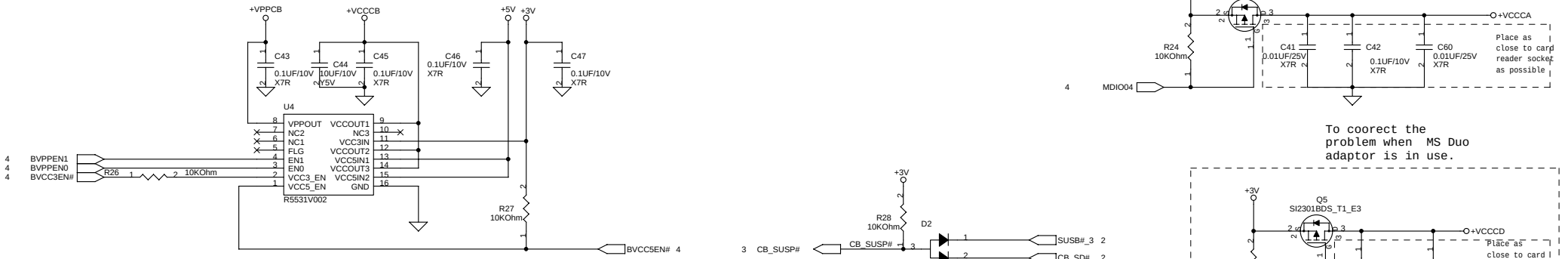


ASUSTek COMPUTER INC	Project Name: **U2A I/O BD.**	
	Engineer: *Tony_Lin*	
Size: Custom	Title : RICOH 5C841/PCI_A	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 4 of 9	



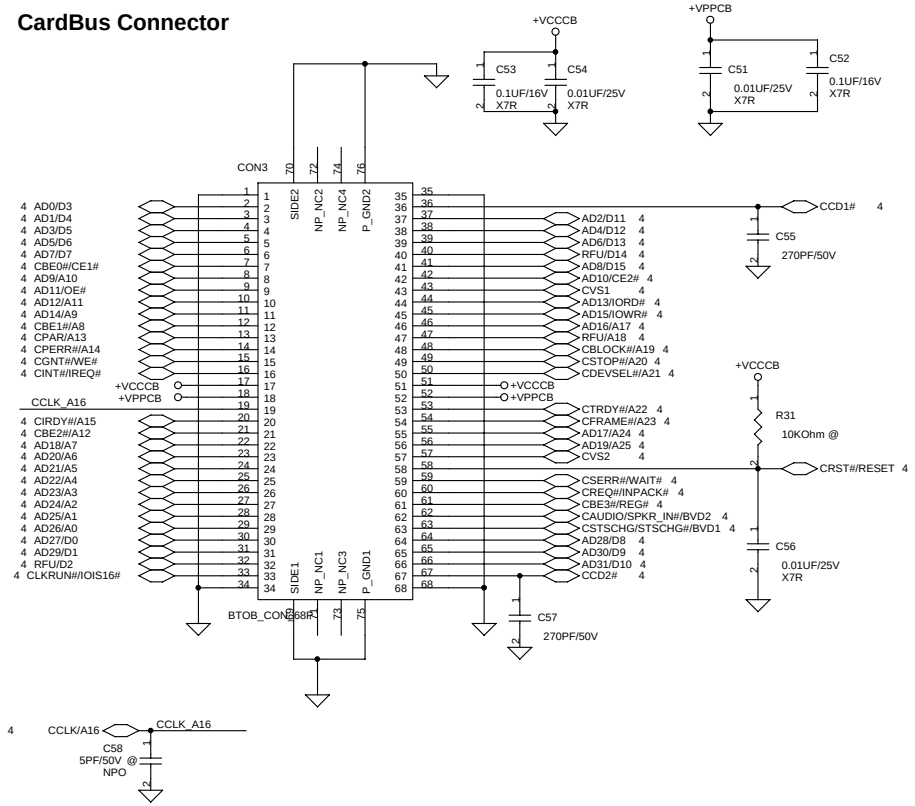
ASUSTek COMPUTER INC	Project Name	U2A I/O BD.	
	Engineer:	*Tony_Lin*	
Size: Custom	Title :	RICOH 5C841/PCI_C	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet	5 of 9	

Power Switch



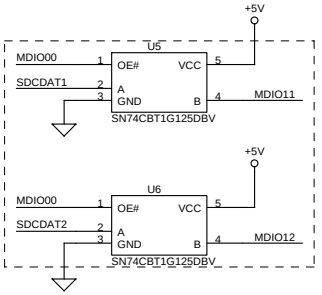
To coorect the problem when MS Duo adaptor is in use.

CardBus Connector

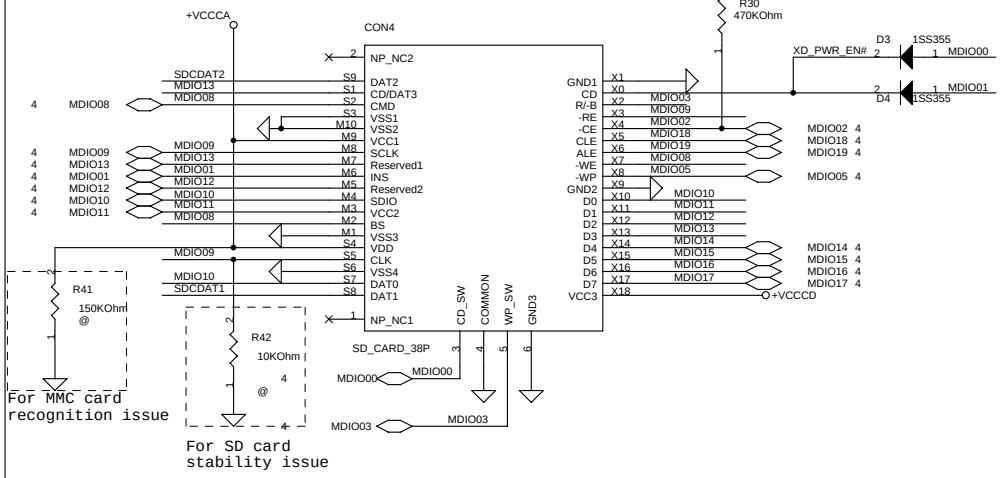


SD/MMC/MS/MS-PRO Card Reader Socket

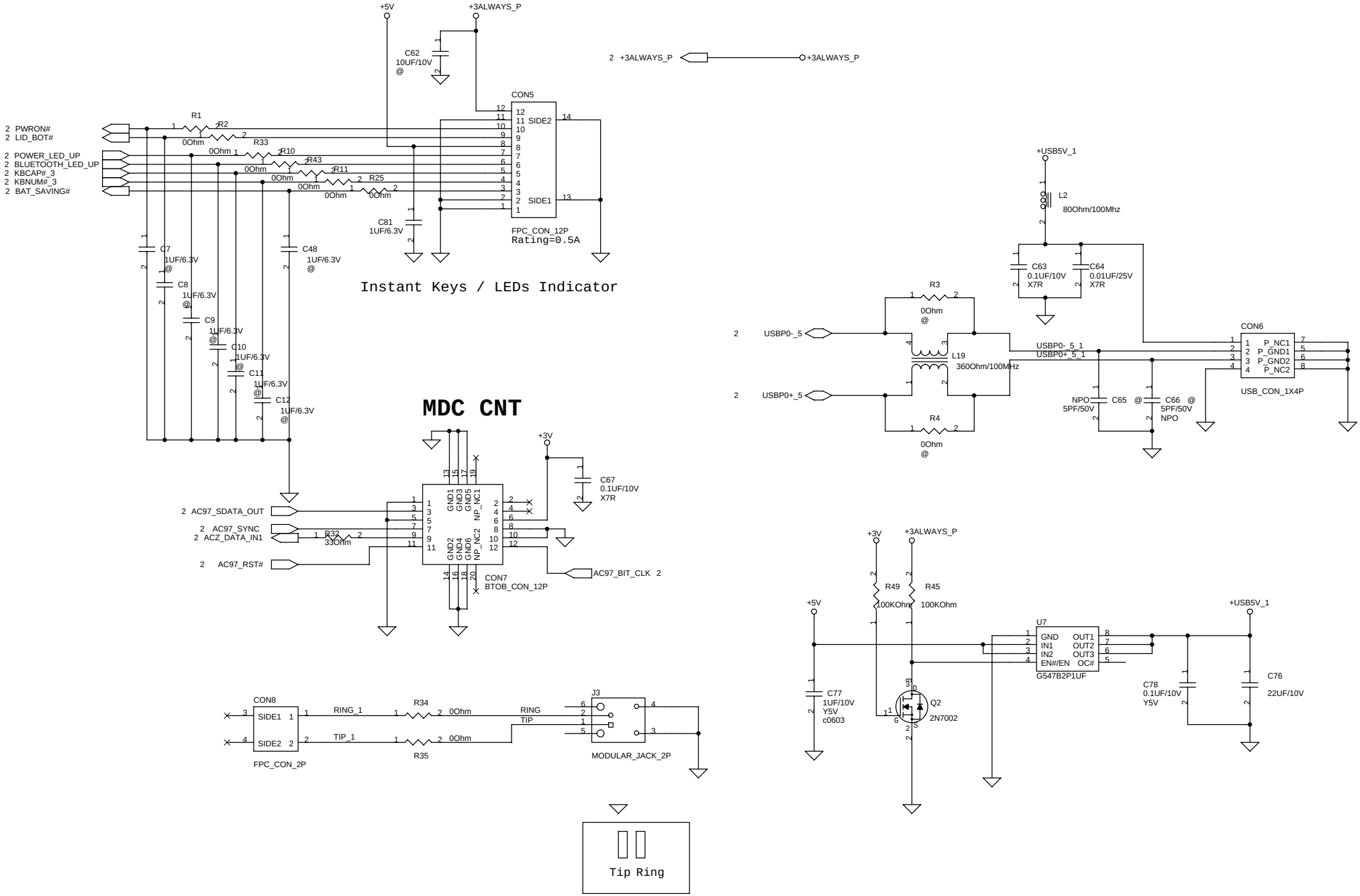
To coorect the problem when MS Duo adaptor is in use.



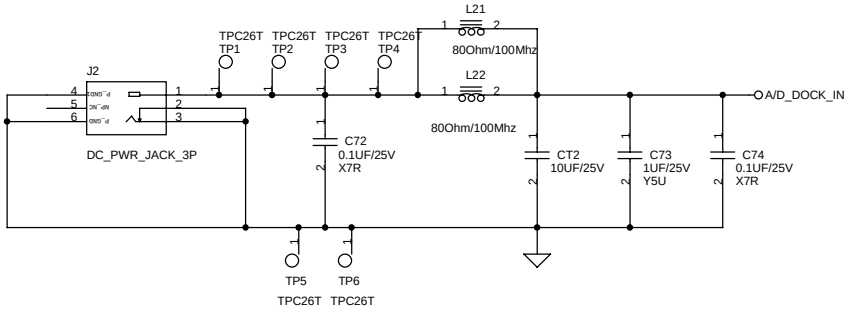

```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect  XD Card Ready/Busy#
MDIO04--> SD/MS/XD  Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MS/XD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14-->       XD Data 4
MDIO15-->       XD Data 5
MDIO16-->       XD Data 6
MDIO17-->       XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
```



Project Name	U2A I/O BD.
ASUSTek COMPUTER INC	Engineer: Tony_Lin
Size: Custom	Title : R5C841 PWR SW
Rev	2.0
Date: Thursday, September 22, 2005	Sheet 6 of 9

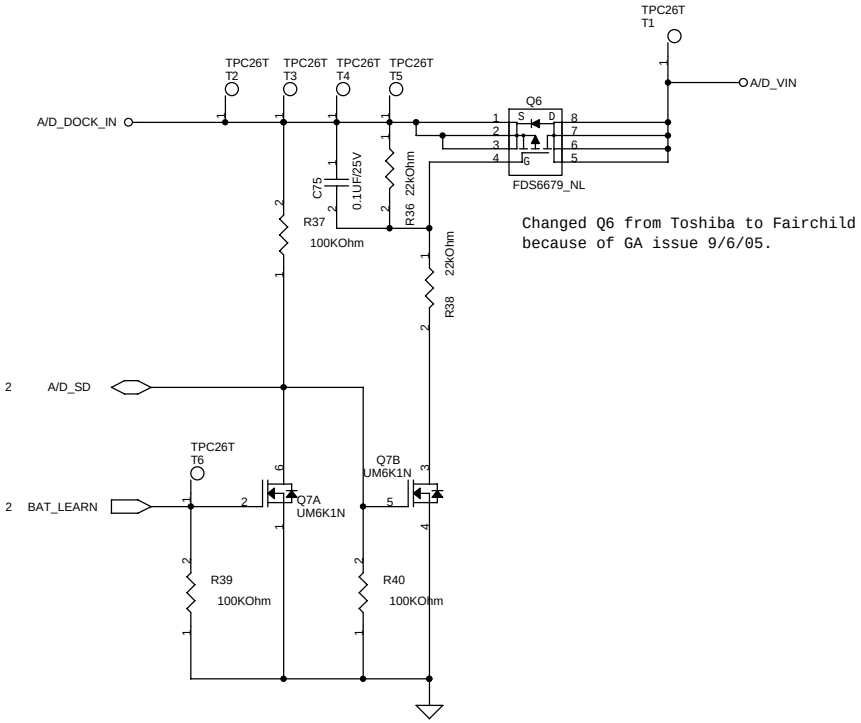


ASUSTek COMPUTER INC	Project Name: U2A I/O BD.	
	Engineer: Tony_Lin	
Size: Custom	Title : MDC & USB CON	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 7 of 9	



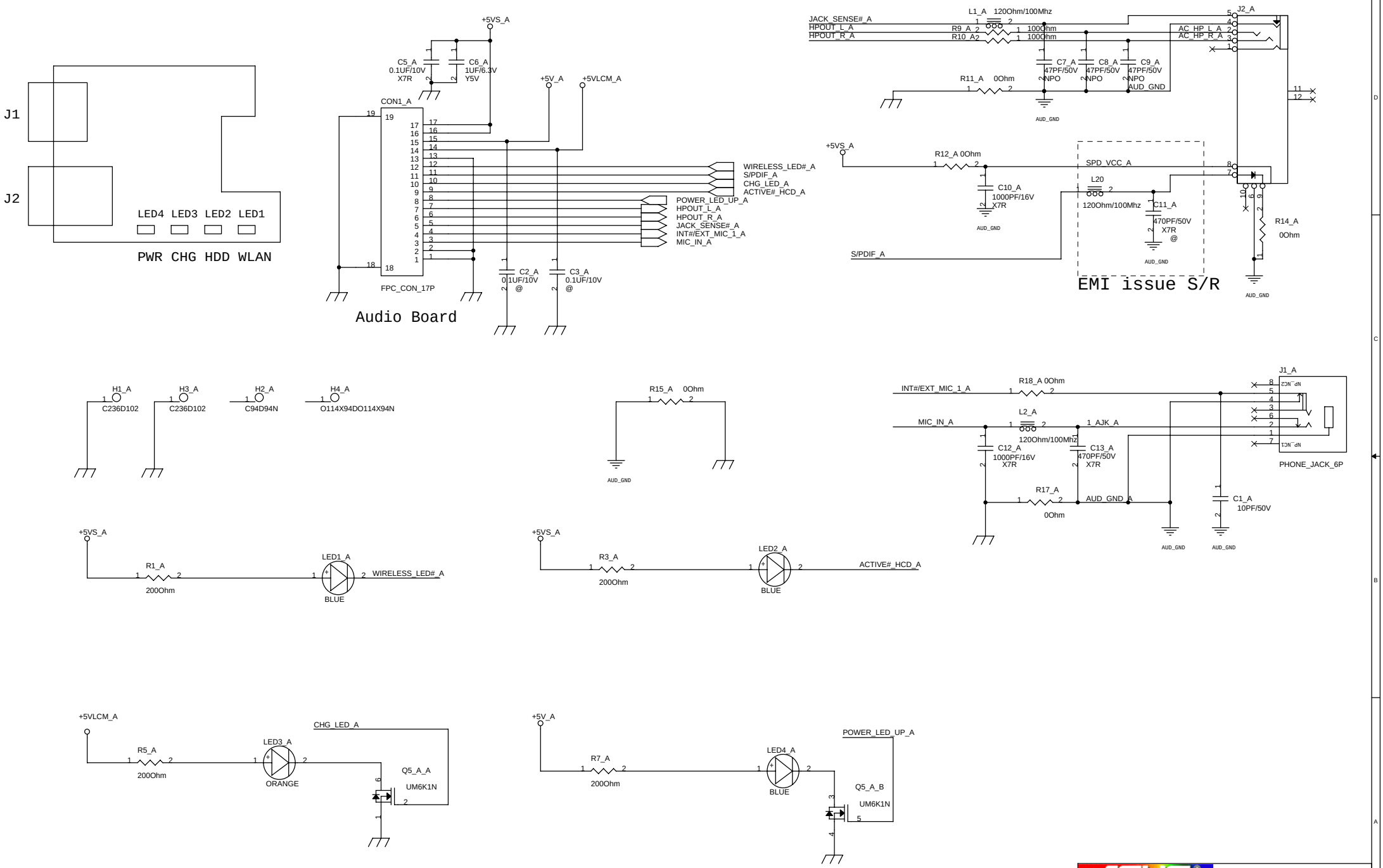
2 A/D_VIN — A/D_VIN

2 A/D_DOCK_IN — A/D_DOCK_IN



Changed Q6 from Toshiba to Fairchild because of GA issue 9/6/05.

ASUSTek COMPUTER INC	Project Name: U2A I/O BD.	
	Engineer: *Tony_Lin*	
Size: Custom	Title : DC In & BAT Learn	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 8 of 9	



ASUS Tek COMPUTER INC	Engineer: *Tony_Lin*	
Size: Custom	Project Name: **U2A I/O BD.**	Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 9 of 9	

Title : LEDs & Head Phone

Revision History

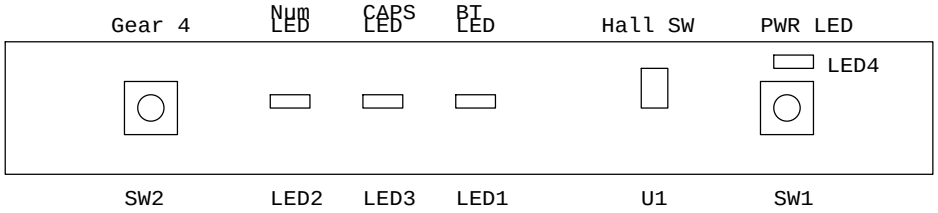
Rev1.2

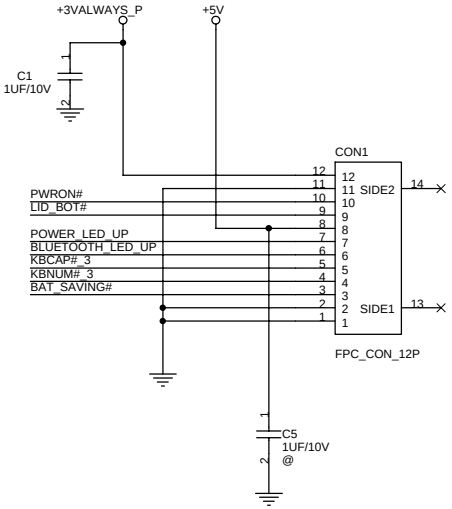
1. Add on 3VS discharge circuit.
2. Add on EMI solution.
3. Replace X1, C33 and C36 for cost issue.
4. Add on USB Power isolation circuit for S4 state.

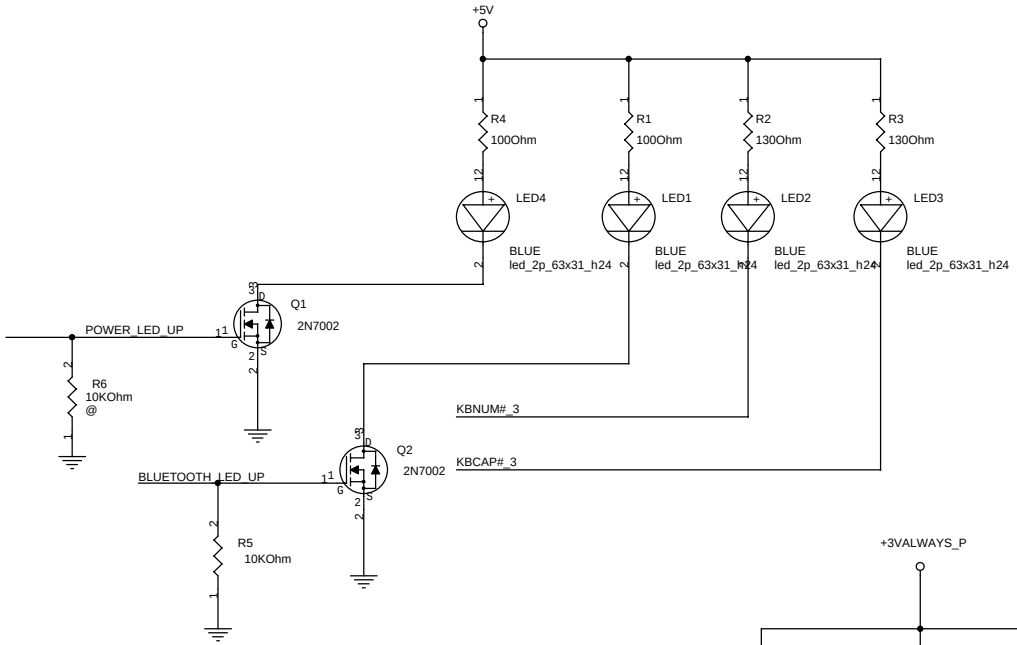
Rev2.0

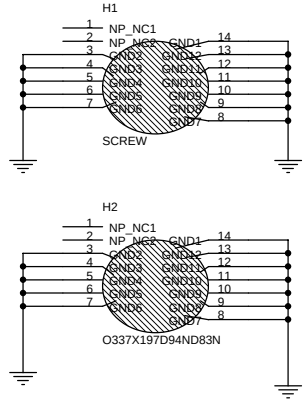
1. U7.1 link to GND
2. Add on Pull low 10K for PowerOnLED and BT LED in Indicator Board.

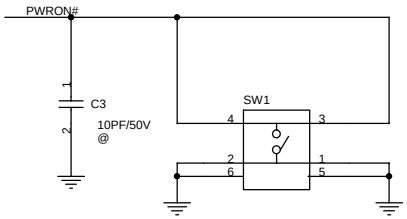
ASUSTek COMPUTER INC	Project Name	U2A I/O BD.	
	Engineer:	*Tony_Lin*	
Size: Custom	Title : Revision History		Rev: 2.0
Date: Thursday, September 22, 2005	Sheet 10 of 10		

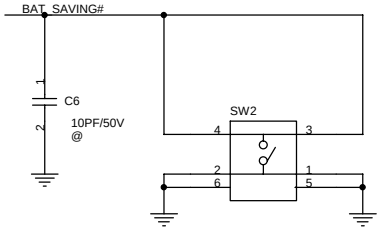


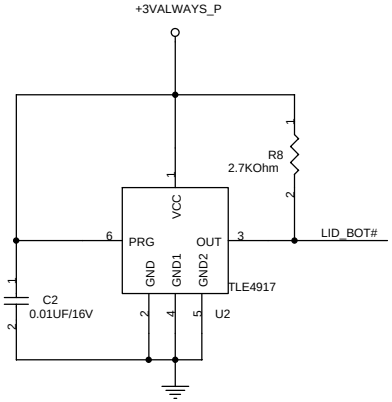








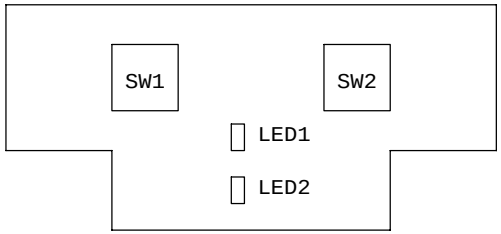




ASUSTek COMPUTER INC	Project Name: U2A		
	Engineer: Tony_Lin		
Size: Custom	Title : LEDs Indicator		Rev: 2.0
Date: Thursday, September 29, 2005	Sheet 1 of 1		

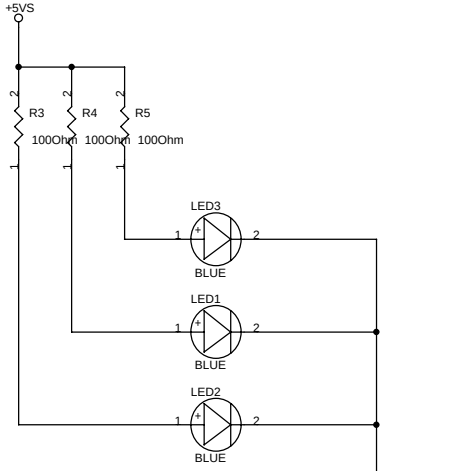
H15 O291X94DO291X94N
H16 O291X94DO291X94N
H17 O291X94DO291X94N
H18 O291X94DO291X94N
H19 O291X94DO291X94N
H20 O291X94DO291X94N

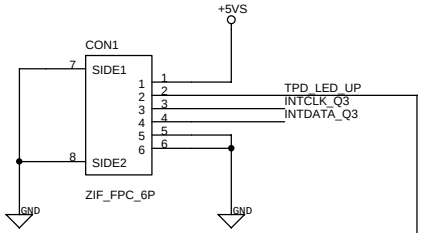
H21 O291X94DO291X94N
H22 O291X94DO291X94N
H23 O291X94DO291X94N

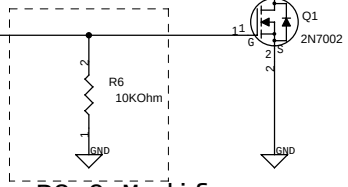


H24 C59D59N
H25 C59D59N
H26 C59D59N

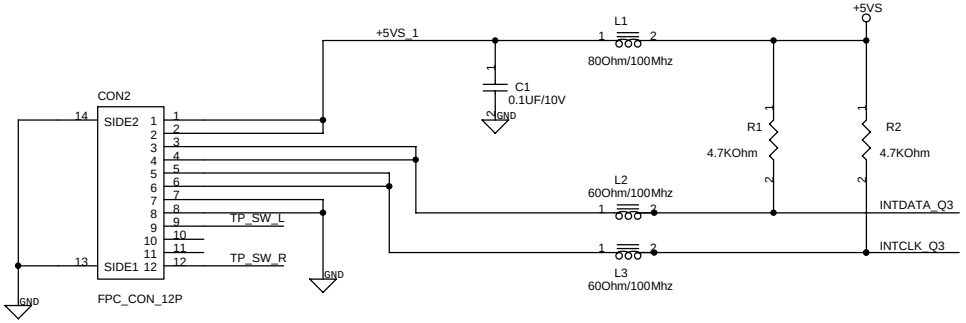
H27 O291X94DO291X94N

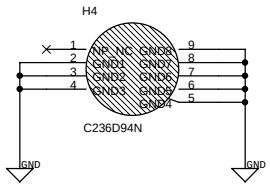


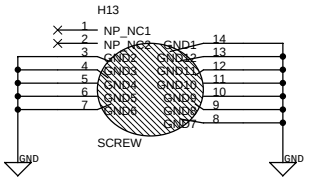


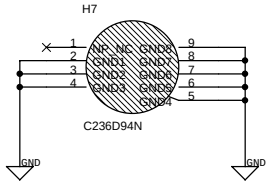


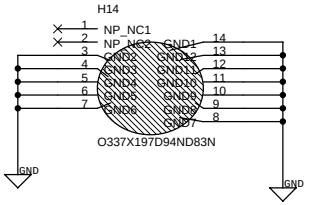
R2.0 Modify

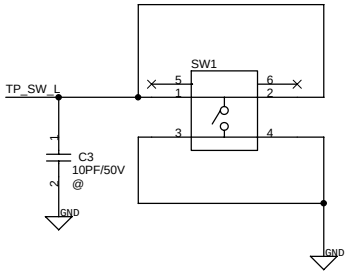


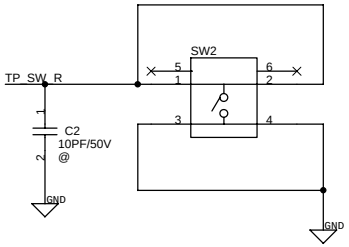












ASUSTek COMPUTER INC	Project Name: TOUCHPAD BD	
	Engineer: *Tony_Lin*	
Size: Custom	Title : Touch Pad	Rev: 2.0
Date: Wednesday, September 21, 2005	Sheet 1 of 1	