# UL20A SCHEMATIC Revision 2.0

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<Variant Name>

Title : PAGE REF.

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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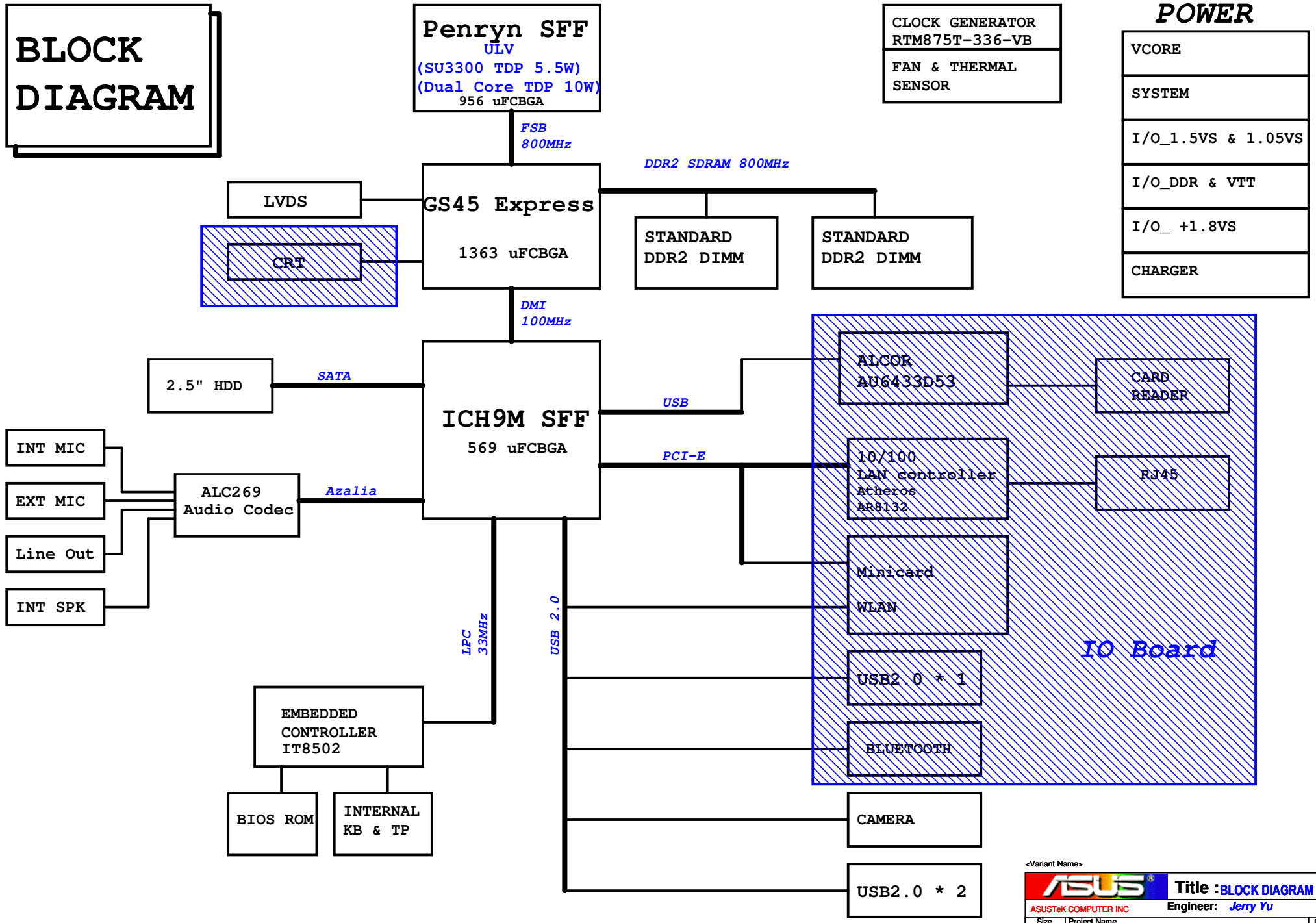
# BLOCK DIAGRAM




<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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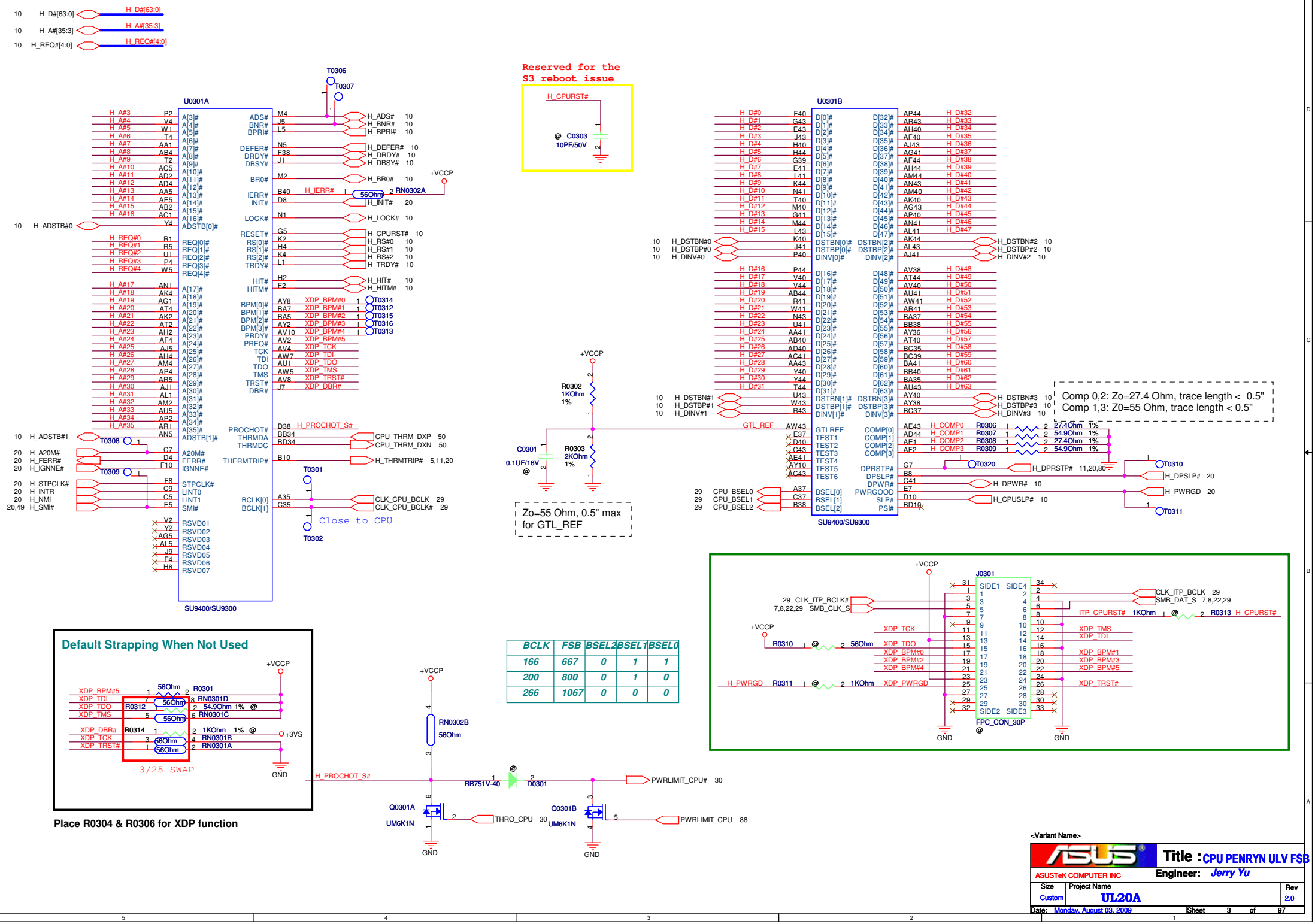


| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 166 | 667 | 0 | 1 | 1 |
| 200 | 800 | 0 | 1 | 0 |
| 266 | 1067 | 0 | 0 | 0 |

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU PENRYN ULV FSB

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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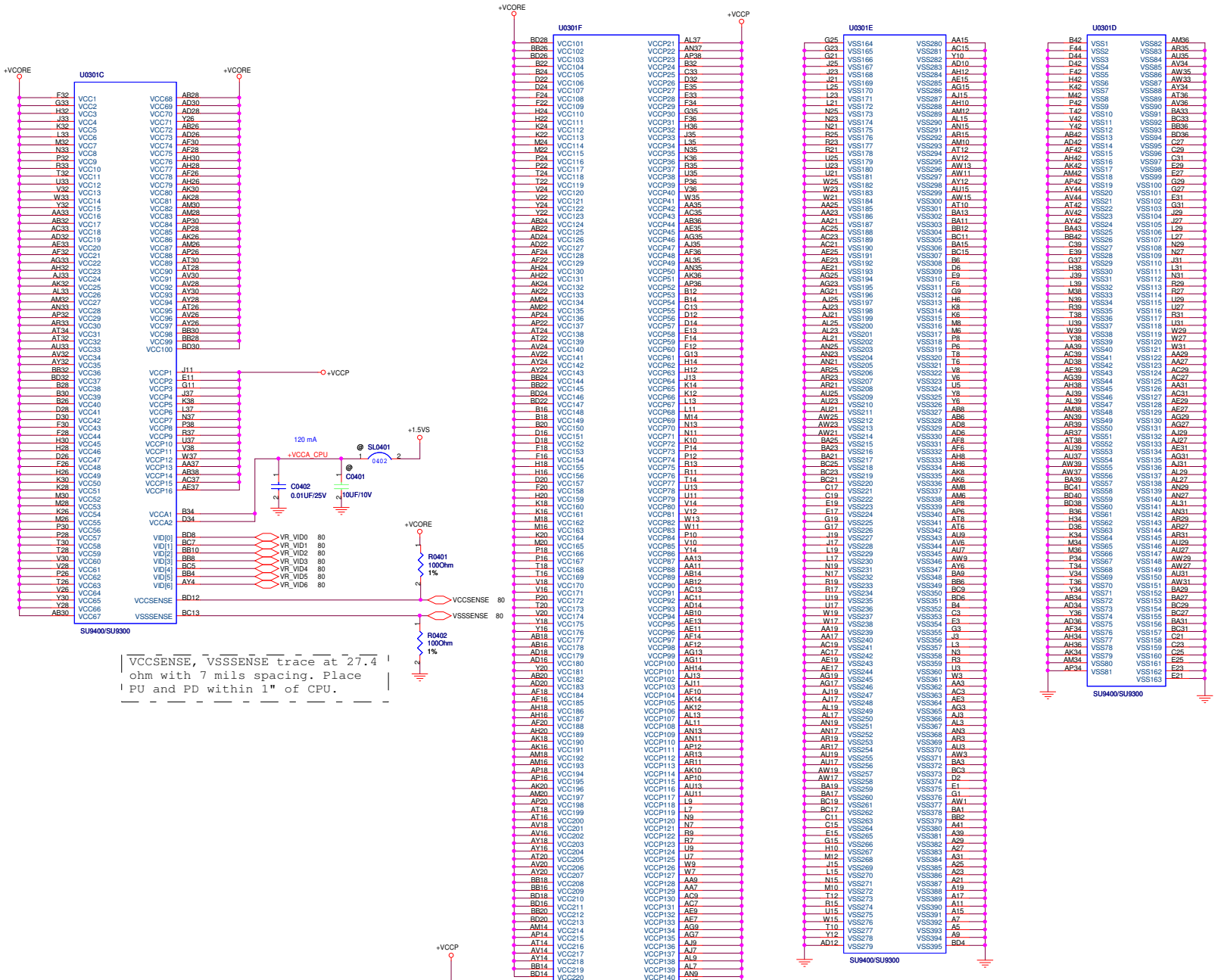
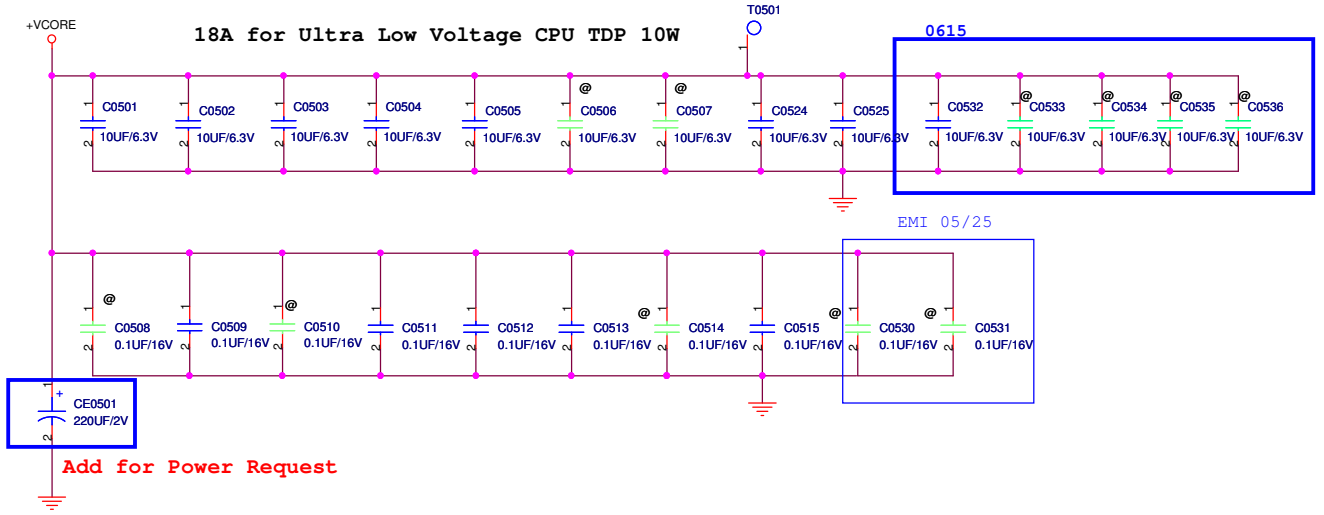
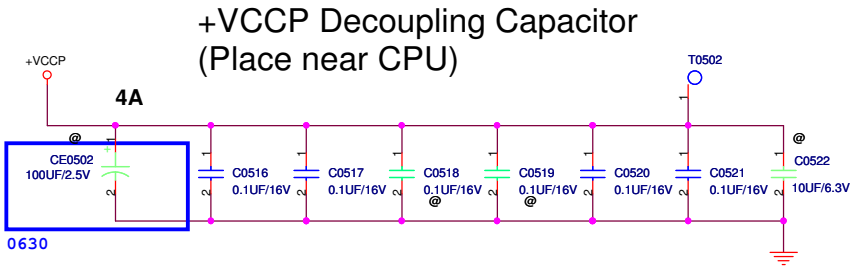
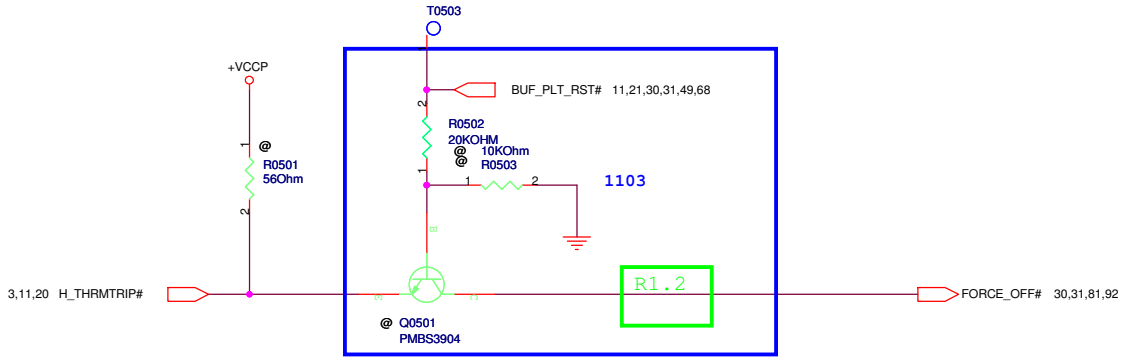

U0301C
SU9400/SU9300
+VCORE
+VCCP
U0301F
U0301E
U0301D
+1.5VS
120 mA
+VCCA_CPU
@ SL0401
0402
C0402
0.01UF/25V
@ C0401
10UF/10V
R0401
100Ohm
1%
R0402
100Ohm
1%
VCCSENSE
VSSSENSE
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place PU and PD within 1" of CPU.




Thermal Trip signal (From CPU to ICH-9M and sequence)

**Decoupling guide from Intel**

| | | |
|---|---|---|
| VCORE | 10uF mount | *4pcs |
| | 0.1uF mount | *5pcs |
| VCCP | 1uF | * 12pcs |
| | 270uF | * 1pcs |
| VCCA | 0.01uF | * 1 pcs |
| | 10uF | * 1 pcs |

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU CAPACITORS

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
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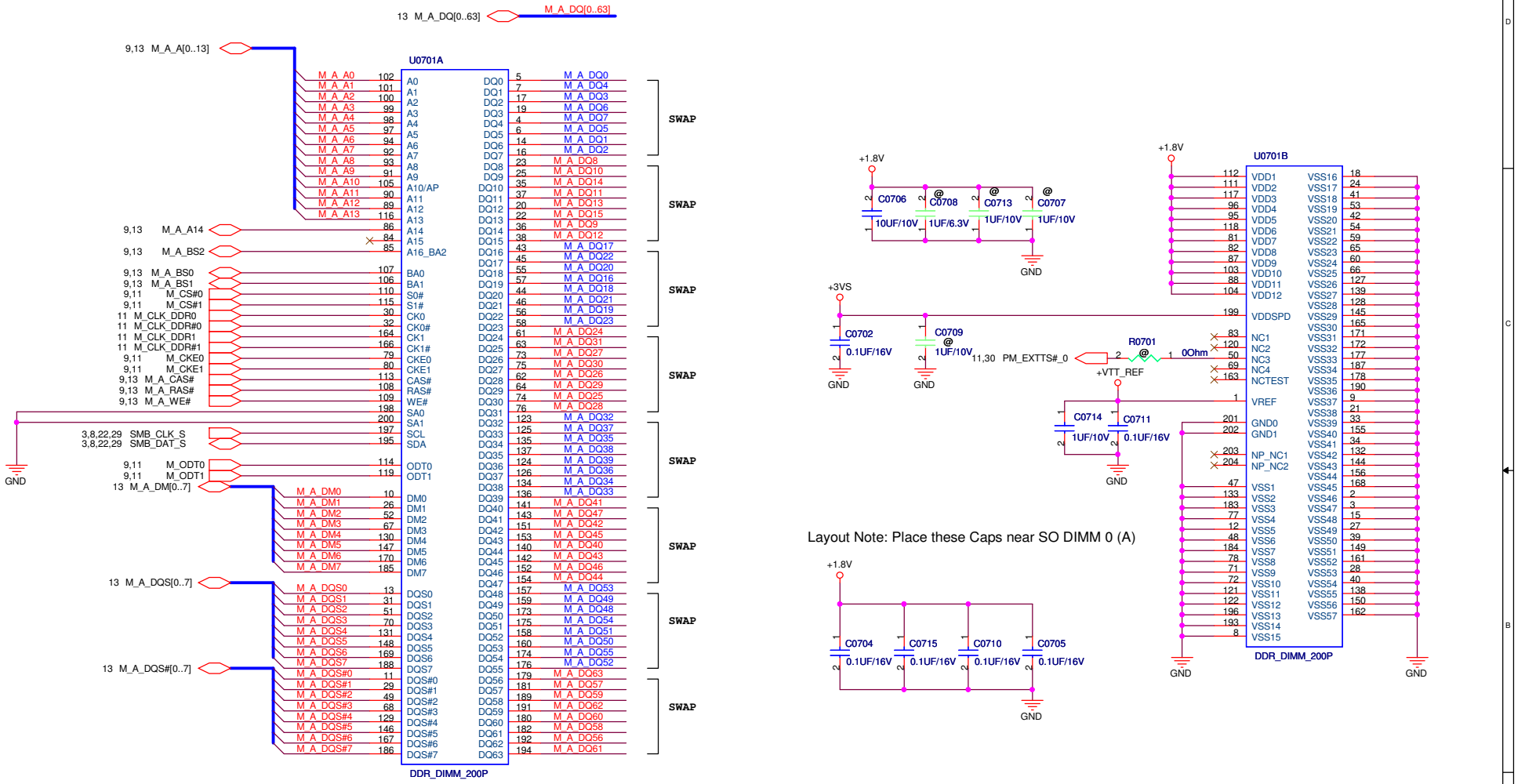
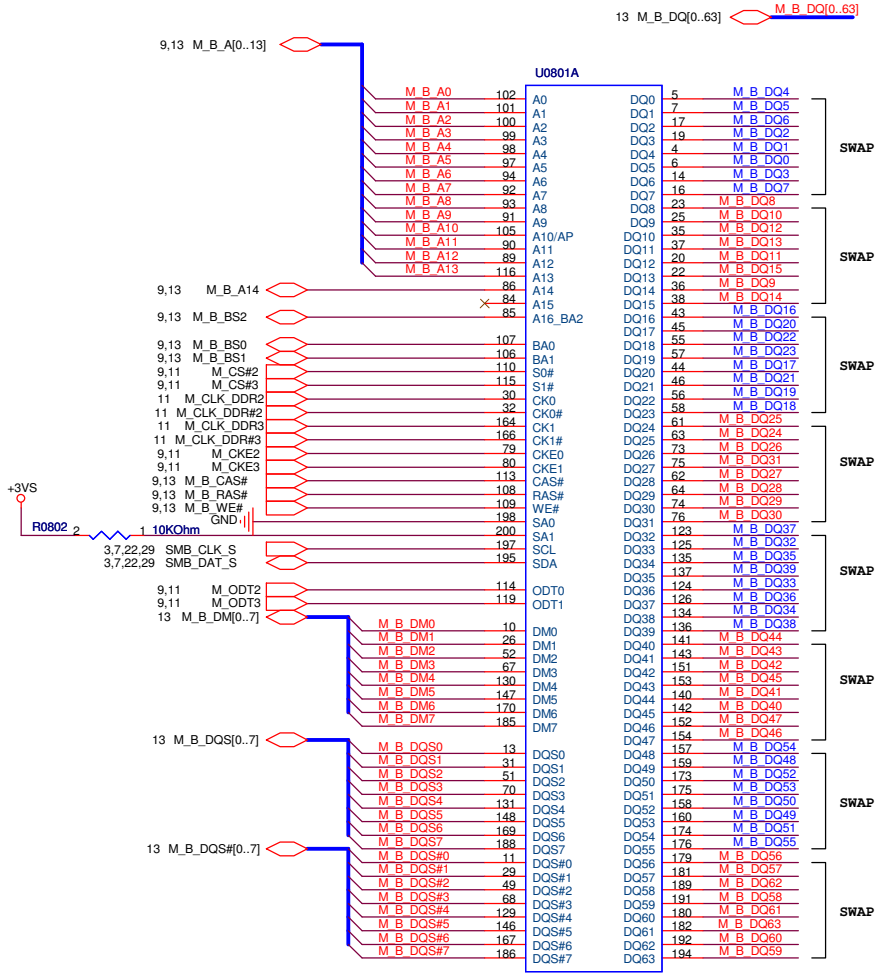


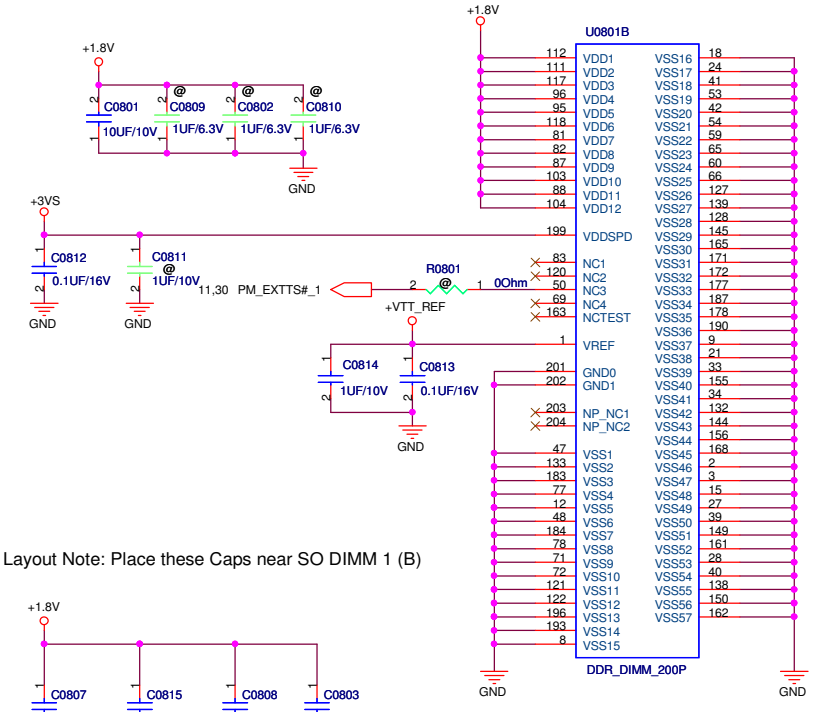

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DDR3 SO-DIMM CHANNEL A | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 7 of 97 | |

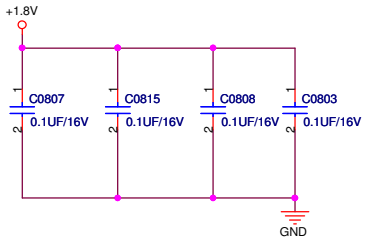



**PN : 12G02533200D**

***REV***




Layout Note: Place these Caps near SO DIMM 1 (B)




<Variant Name>

Title : M_DDR3 SO-DIMM CHANNEL B

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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M_A_A[0..13] 7,13
M_A_BS[0..2] 7,13
M_B_A[0..13] 8,13
M_B_BS[0..2] 8,13
M_CKE[0:3] 7,8,11
M_ODT[0:3] 7,8,11

+0.9VS

1 0.1UF 2 CN0901A
3 0.1UF 4 CN0901B
5 0.1UF 6 CN0901C
7 0.1UF 8 CN0901D
GND

1 56Ohm 16 RN0901A M_B_BS1
2 56Ohm 15 RN0901B M_B_A0
3 56Ohm 14 RN0901C M_B_A2
4 56Ohm 13 RN0901D M_ODT2

1 0.1UF 2 CN0902A
3 0.1UF 4 CN0902B
5 0.1UF 6 CN0902C
7 0.1UF 8 CN0902D
GND

4 56Ohm 13 RN0902D M_CS#0 → M_CS#0 7,11
3 56Ohm 14 RN0902C M_CS#1 → M_CS#1 7,11
5 56Ohm 12 RN0902E M_ODT0
6 56Ohm 11 RN0902F M_A_WE# → M_A_WE# 7,13
2 56Ohm 15 RN0906B M_A_A2
7 56Ohm 10 RN0902G M_A_CAS# → M_A_CAS# 7,13
8 56Ohm 9 RN0902H M_A_A13

1 0.1UF 2 CN0903A
3 0.1UF 4 CN0903B
5 0.1UF 6 CN0903C
7 0.1UF 8 CN0903D
GND

2 56Ohm 15 RN0903B M_B_A5
4 56Ohm 13 RN0904D M_A_A9
3 56Ohm 14 RN0903C M_B_A9
6 56Ohm 11 RN0904F M_CKE0
5 56Ohm 12 RN0903E M_B_BS2
4 56Ohm 13 RN0903D M_B_A12
5 56Ohm 12 RN0904E M_A_BS2
1 56Ohm 16 RN0903A M_B_A4

**Layout note: Place array cap close to each pullup resistors terminated to +0.9VS**

1 0.1UF 2 CN0904A
3 0.1UF 4 CN0904B
5 0.1UF 6 CN0904C
7 0.1UF 8 CN0904D
GND

3 56Ohm 14 RN0905C M_A_A8
4 56Ohm 13 RN0905D M_A_A3
6 56Ohm 11 RN0905F M_A_A14 → M_A_A14 7,13
7 56Ohm 10 RN0905G M_A_A5
2 56Ohm 15 RN0902B M_ODT1
1 56Ohm 16 RN0906A M_A_A11
4 56Ohm 13 RN0906D M_A_A4
3 56Ohm 14 RN0906C M_A_A6

1 0.1UF 2 CN0905A
3 0.1UF 4 CN0905B
5 0.1UF 6 CN0905C
7 0.1UF 8 CN0905D
GND

2 56Ohm 15 RN0905B M_A_A0
8 56Ohm 9 RN0906H M_A_BS1
1 56Ohm 16 RN0905A M_A_A1
6 56Ohm 11 RN0906F M_A_A10
7 56Ohm 10 RN0906G M_A_RAS# → M_A_RAS# 7,13
5 56Ohm 12 RN0906E M_A_BS0
5 56Ohm 12 RN0905E M_A_A7
8 56Ohm 9 RN0905H M_A_A12
7 56Ohm 10 RN0904G M_CKE1

1 56Ohm 16 RN0904A M_B_A14 → M_B_A14 8,13
2 56Ohm 15 RN0904B M_CKE3
4 56Ohm 13 RN0907D M_CS#3 → M_CS#3 8,11
3 56Ohm 14 RN0904C M_CKE2
5 56Ohm 12 RN0901E M_CS#2 → M_CS#2 8,11
8 56Ohm 9 RN0901H M_ODT3
7 56Ohm 10 RN0901G M_B_A13
6 56Ohm 11 RN0901F M_B_RAS# → M_B_RAS# 8,13

7 56Ohm 10 RN0903G M_B_A7
8 56Ohm 9 RN0903H M_B_A11
3 56Ohm 14 RN0907C M_B_BS0
6 56Ohm 11 RN0903F M_B_A8
2 56Ohm 15 RN0907B M_B_WE# → M_B_WE# 8,13
1 56Ohm 16 RN0907A M_B_CAS# → M_B_CAS# 8,13
6 56Ohm 11 RN0907F M_B_A1
5 56Ohm 12 RN0907E M_B_A3

7 56Ohm 10 RN0907G M_B_A10
8 56Ohm 9 RN0907H M_B_A6

8 56Ohm 9 RN0904H
1 56Ohm 16 RN0902A

@ C0902 10UF/10V
GND

+1.8V
T0901
C0901 0.1UF/16V
R0901 1KOhm 1%
L0901 120Ohm/100Mhz
R0903
83 +0.9VTT_REF
0Ohm @
+VTT_REF
C0903 0.1UF/16V
R0902 1KOhm 1%

<Variant Name>

ASUSTeK COMPUTER INC

Title : DIM DDR2 VREF

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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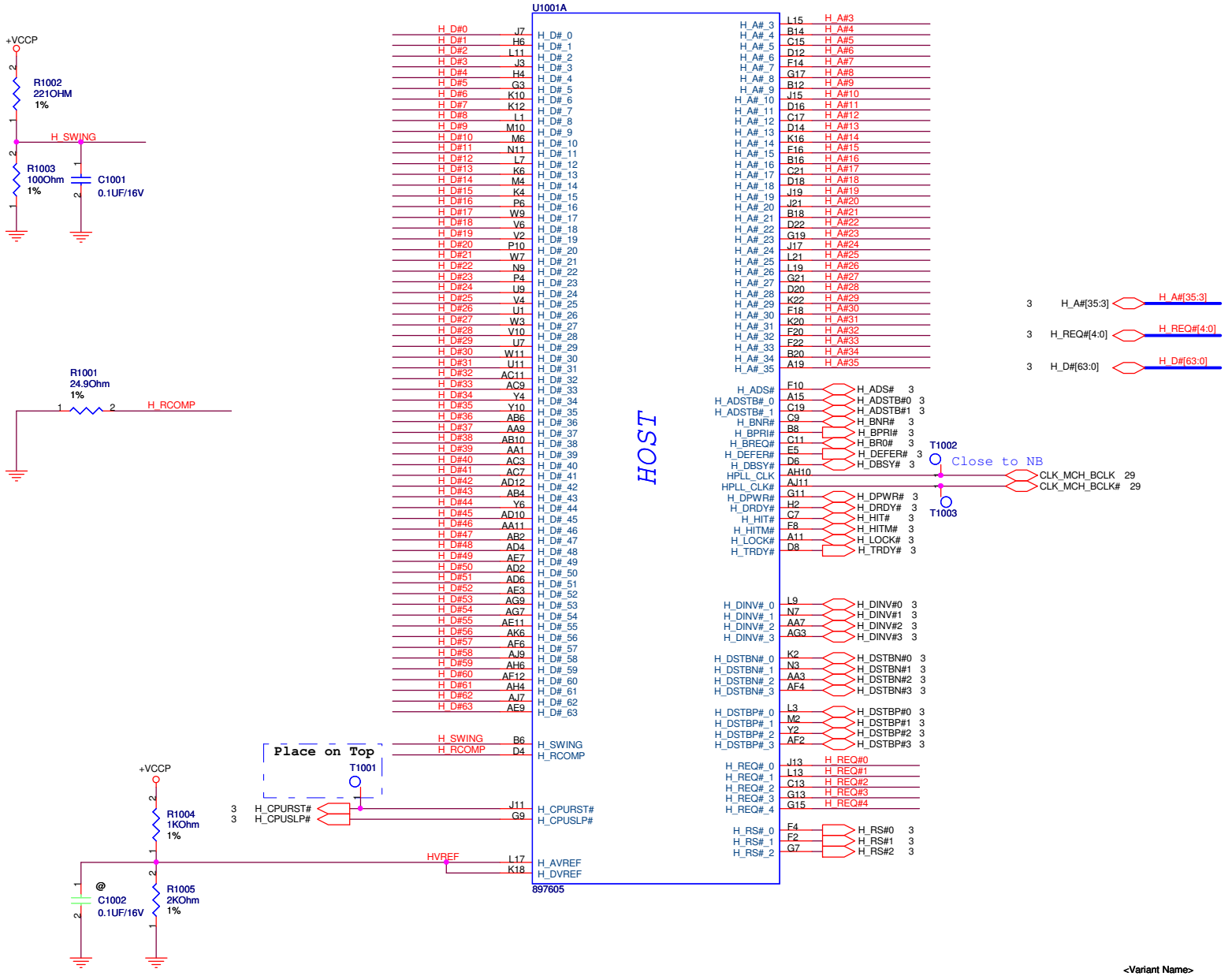
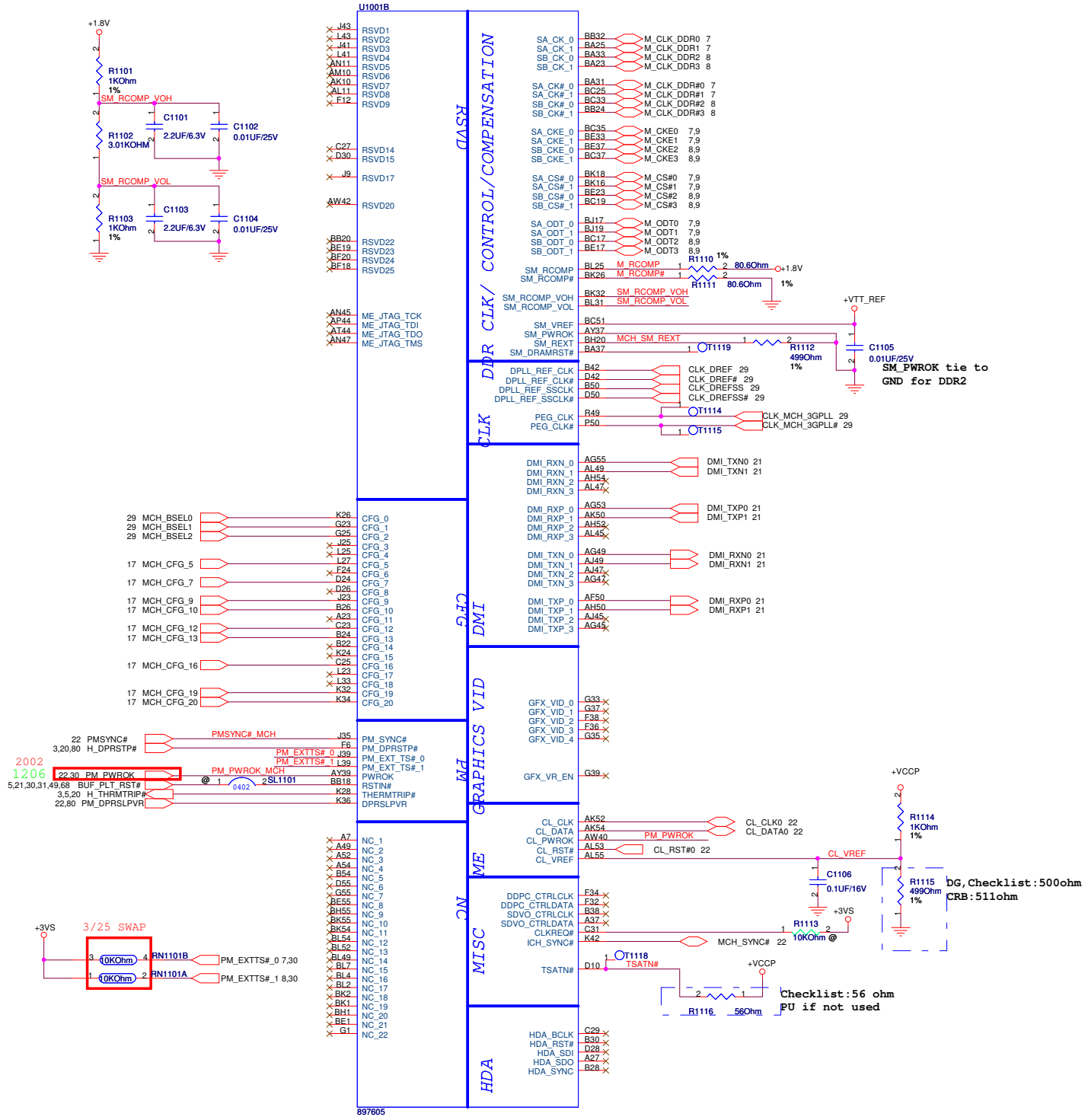



<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : NB GS45 HOST | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 10 of 97 | |




<Variant Name>

Title : NB GS45 DMI

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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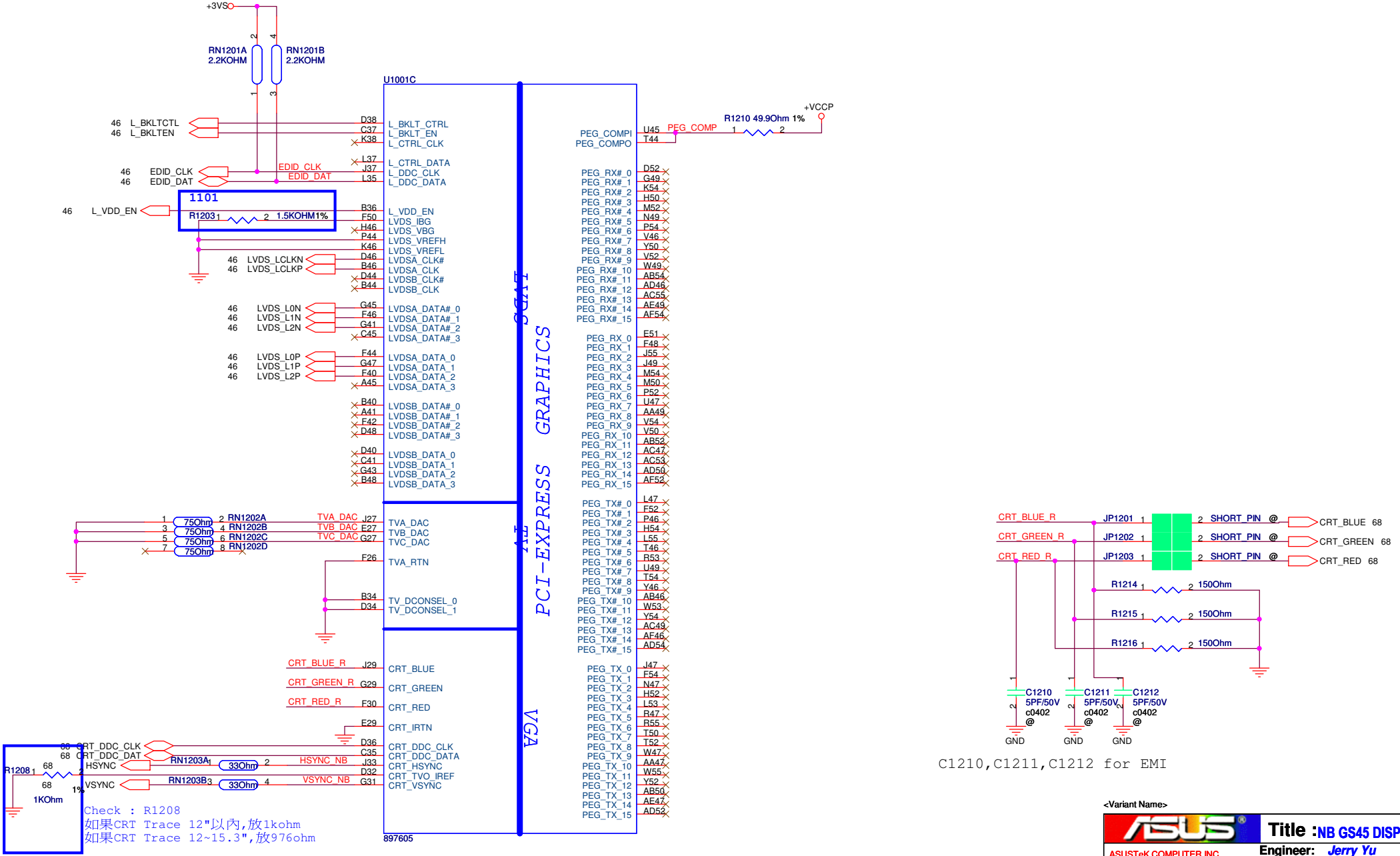
+3VS
RN1201A 2.2KOHM
RN1201B 2.2KOHM
U1001C
46 L_BKLTCTL
46 L_BKLTEN
D38 L_BKLT_CTRL
C37 L_BKLT_EN
K38 L_CTRL_CLK
46 EDID_CLK
46 EDID_DAT
EDID_CLK
EDID_DAT
L37 L_CTRL_DATA
J37 L_DDC_CLK
L35 L_DDC_DATA
1101
46 L_VDD_EN
R1203 1.5KOHM1%
B36 L_VDD_EN
F50 LVDS_IBG
H46 LVDS_VBG
P44 LVDS_VREFH
K46 LVDS_VREFL
46 LVDS_LCLKN
46 LVDS_LCLKP
D46 LVDSA_CLK#
B46 LVDSA_CLK
D44 LVDSB_CLK#
B44 LVDSB_CLK
46 LVDS_L0N
46 LVDS_L1N
46 LVDS_L2N
G45 LVDSA_DATA#_0
F46 LVDSA_DATA#_1
G41 LVDSA_DATA#_2
C45 LVDSA_DATA#_3
46 LVDS_L0P
46 LVDS_L1P
46 LVDS_L2P
F44 LVDSA_DATA_0
G47 LVDSA_DATA_1
F40 LVDSA_DATA_2
A45 LVDSA_DATA_3
B40 LVDSB_DATA#_0
A41 LVDSB_DATA#_1
F42 LVDSB_DATA#_2
D48 LVDSB_DATA#_3
D40 LVDSB_DATA_0
C41 LVDSB_DATA_1
G43 LVDSB_DATA_2
B48 LVDSB_DATA_3
LVDS
PEG_COMPI
PEG_COMPO
U45 PEG_COMP
T44
+VCCP
R1210 49.9Ohm 1%
PEG_RX#_0 D52
PEG_RX#_1 G49
PEG_RX#_2 K54
PEG_RX#_3 H50
PEG_RX#_4 M52
PEG_RX#_5 N49
PEG_RX#_6 P54
PEG_RX#_7 V46
PEG_RX#_8 V50
PEG_RX#_9 V52
PEG_RX#_10 W49
PEG_RX#_11 AB54
PEG_RX#_12 AD46
PEG_RX#_13 AC55
PEG_RX#_14 AE49
PEG_RX#_15 AF54
PEG_RX_0 E51
PEG_RX_1 F48
PEG_RX_2 J55
PEG_RX_3 J49
PEG_RX_4 M54
PEG_RX_5 M50
PEG_RX_6 P52
PEG_RX_7 U47
PEG_RX_8 AA49
PEG_RX_9 V54
PEG_RX_10 V50
PEG_RX_11 AB52
PEG_RX_12 AC47
PEG_RX_13 AC53
PEG_RX_14 AD50
PEG_RX_15 AF52
PEG_TX#_0 L47
PEG_TX#_1 F52
PEG_TX#_2 P46
PEG_TX#_3 H54
PEG_TX#_4 L55
PEG_TX#_5 T46
PEG_TX#_6 R53
PEG_TX#_7 U49
PEG_TX#_8 T54
PEG_TX#_9 Y46
PEG_TX#_10 AB46
PEG_TX#_11 W53
PEG_TX#_12 Y54
PEG_TX#_13 AC49
PEG_TX#_14 AF46
PEG_TX#_15 AD54
PEG_TX_0 J47
PEG_TX_1 F54
PEG_TX_2 N47
PEG_TX_3 H52
PEG_TX_4 L53
PEG_TX_5 R47
PEG_TX_6 R55
PEG_TX_7 T50
PEG_TX_8 T52
PEG_TX_9 W47
PEG_TX_10 AA47
PEG_TX_11 W55
PEG_TX_12 Y52
PEG_TX_13 AB50
PEG_TX_14 AE47
PEG_TX_15 AD52
PCI-EXPRESS GRAPHICS
1 75Ohm 2 RN1202A
3 75Ohm 4 RN1202B
5 75Ohm 6 RN1202C
7 75Ohm 8 RN1202D
TVA_DAC J27
TVB_DAC E27
TVC_DAC G27
TVA_DAC
TVB_DAC
TVC_DAC
F26 TVA_RTN
B34 TV_DCONSEL_0
D34 TV_DCONSEL_1
CRT_BLUE_R J29
CRT_GREEN_R G29
CRT_RED_R F30
CRT_BLUE
CRT_GREEN
CRT_RED
E29 CRT_IRTN
68 CRT_DDC_CLK
68 CRT_DDC_DAT
HSYNC
VSYNC
R1208 68
68
1%
1KOhm
RN1203A 33Ohm
RN1203B 33Ohm
HSYNC_NB
VSYNC_NB
D36 CRT_DDC_CLK
C35 CRT_DDC_DATA
J33 CRT_HSYNC
D32 CRT_TVO_IREF
G31 CRT_VSYNC
VGA
897605
Check : R1208
如果CRT Trace 12"以內,放1kohm
如果CRT Trace 12~15.3",放976ohm
CRT_BLUE_R
CRT_GREEN_R
CRT_RED_R
JP1201 SHORT_PIN @ CRT_BLUE 68
JP1202 SHORT_PIN @ CRT_GREEN 68
JP1203 SHORT_PIN @ CRT_RED 68
R1214 150Ohm
R1215 150Ohm
R1216 150Ohm
C1210 5PF/50V c0402 @
C1211 5PF/50V c0402 @
C1212 5PF/50V c0402 @
GND
GND
GND
C1210,C1211,C1212 for EMI
<Variant Name>
Title :NB GS45 DISPLAY
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size B
Project Name UL20A
Rev 2.0
Date: Monday, August 03, 2009
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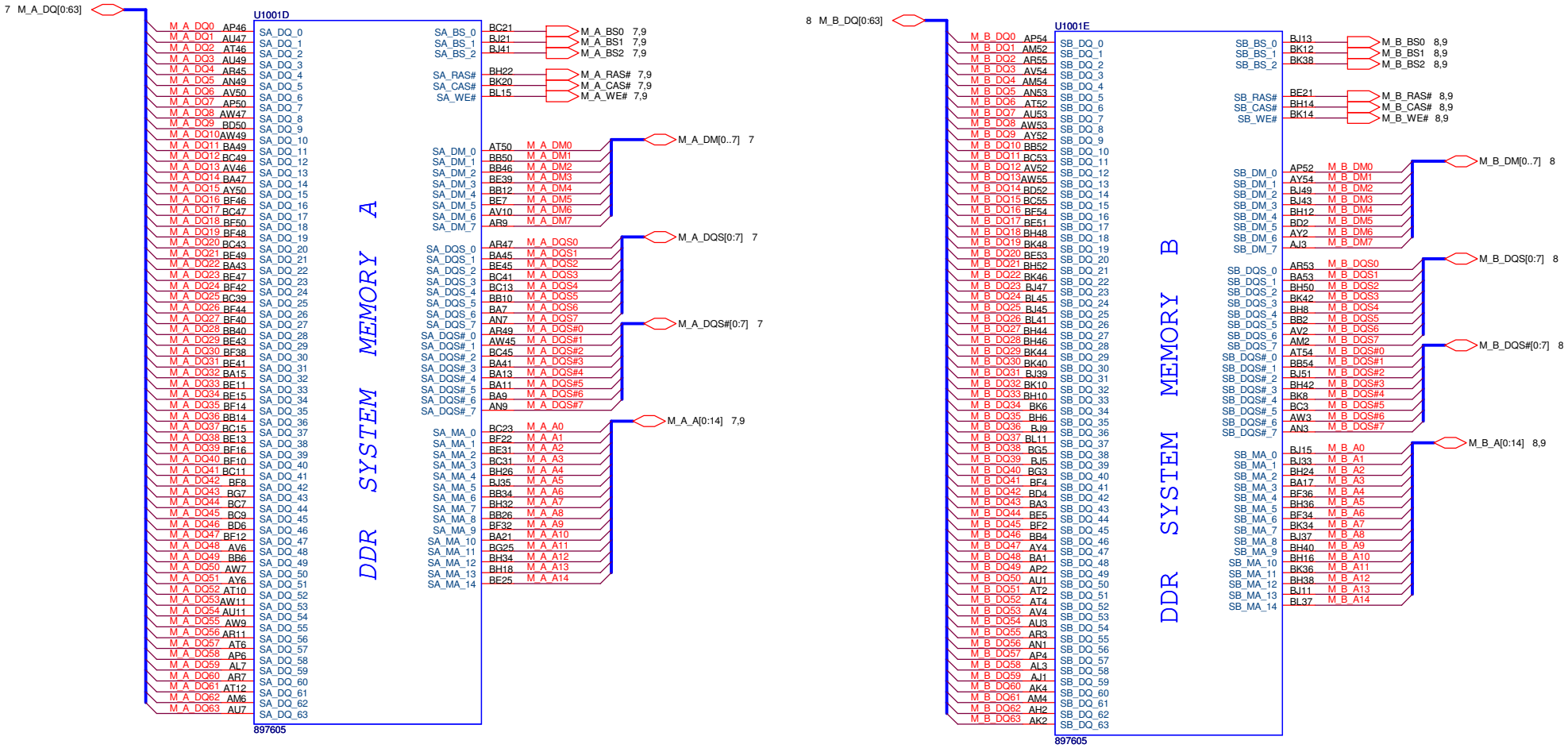


<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : NB GS45 DDR3 BUS | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
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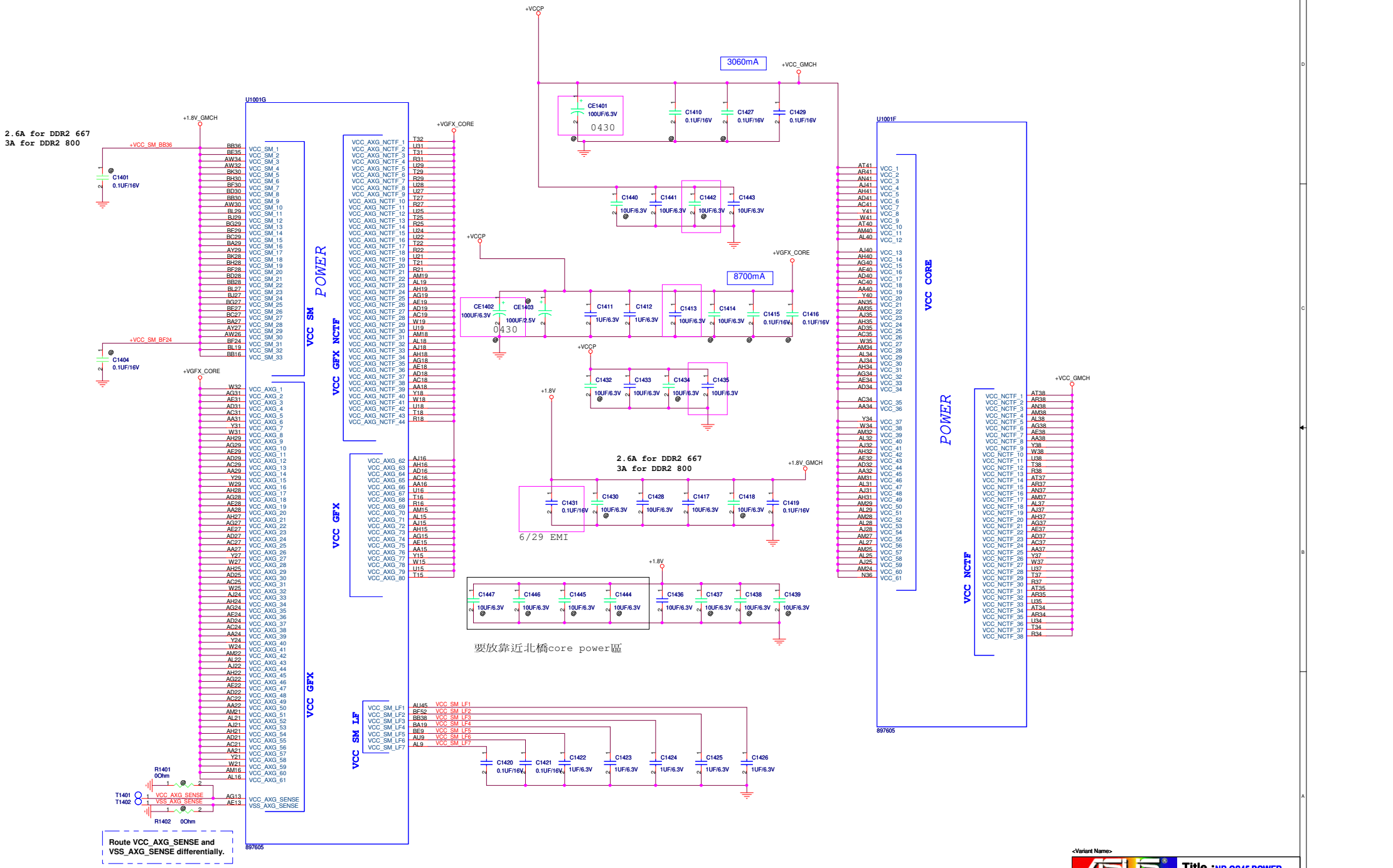
2.6A for DDR2 667
3A for DDR2 800
U1001G
+1.8V_GMCH
+VCC_SM_BB36
+VCC_SM_BF24
+VGFX_CORE
+VCCP
3060mA
8700mA
2.6A for DDR2 667
3A for DDR2 800
6/29 EMI
要放靠近北橋core power區
U1001F
+VCC_GMCH
VCC_SM
VCC_GFX_NCTF
VCC_GFX
VCC_SM_LF
VCC_CORE
VCC_NCTF
POWER
897605
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.

Variant Name
Title : NB GS45 POWER
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size C
Project Name UL20A
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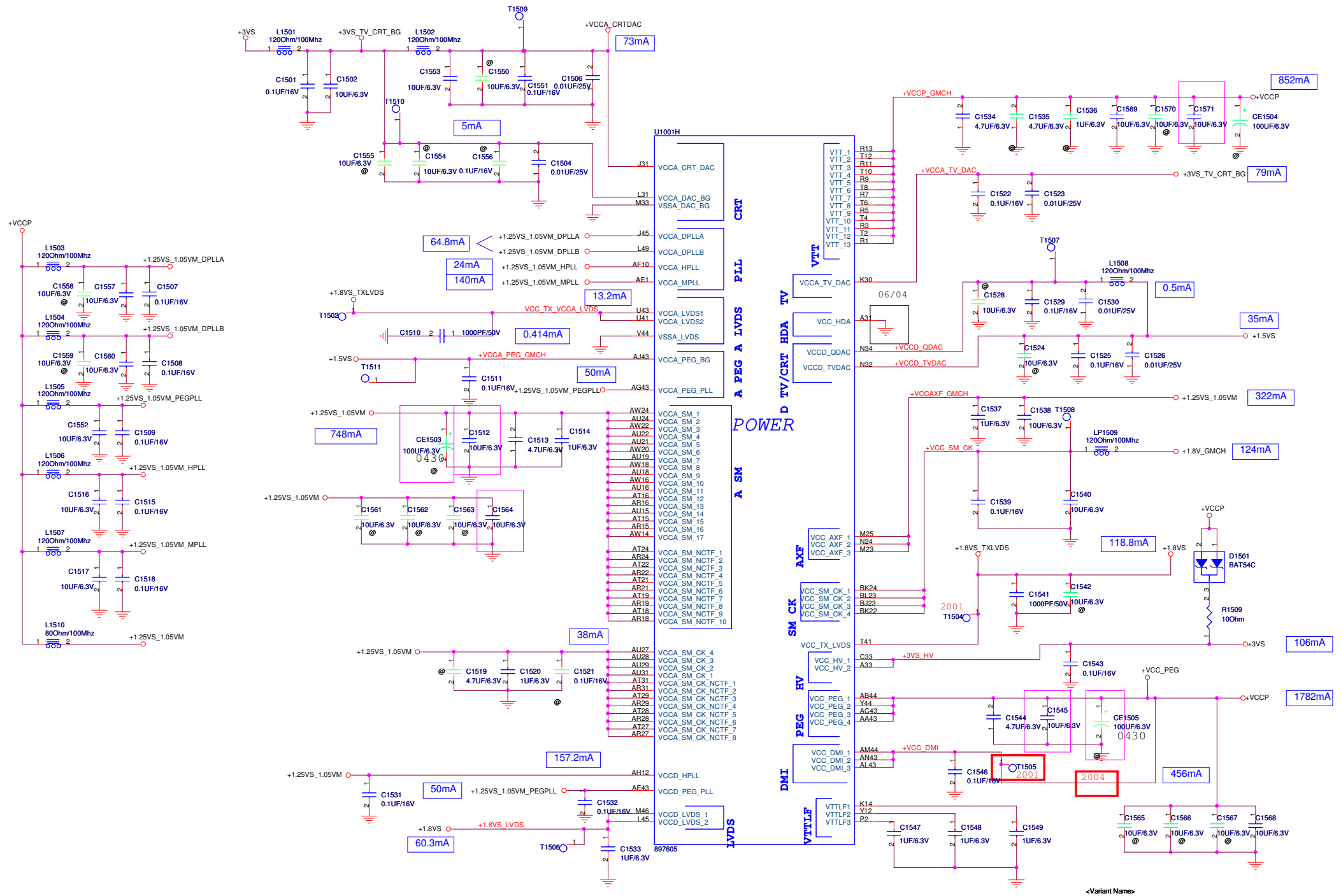
U1001H
POWER
CRT
PLL
LVDS
TV
HDA
TV/CRT
PEG
A
SM
CK
AXF
HV
DMI
VTT
VTTLF
73mA
852mA
5mA
64.8mA
24mA
140mA
79mA
13.2mA
0.5mA
0.414mA
35mA
50mA
322mA
748mA
124mA
118.8mA
38mA
106mA
1782mA
157.2mA
456mA
50mA
60.3mA
897605
Title :NB GS45 POWER
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size Custom
Project Name UL20A
Rev 2.0
Date: Wednesday, July 29, 2009
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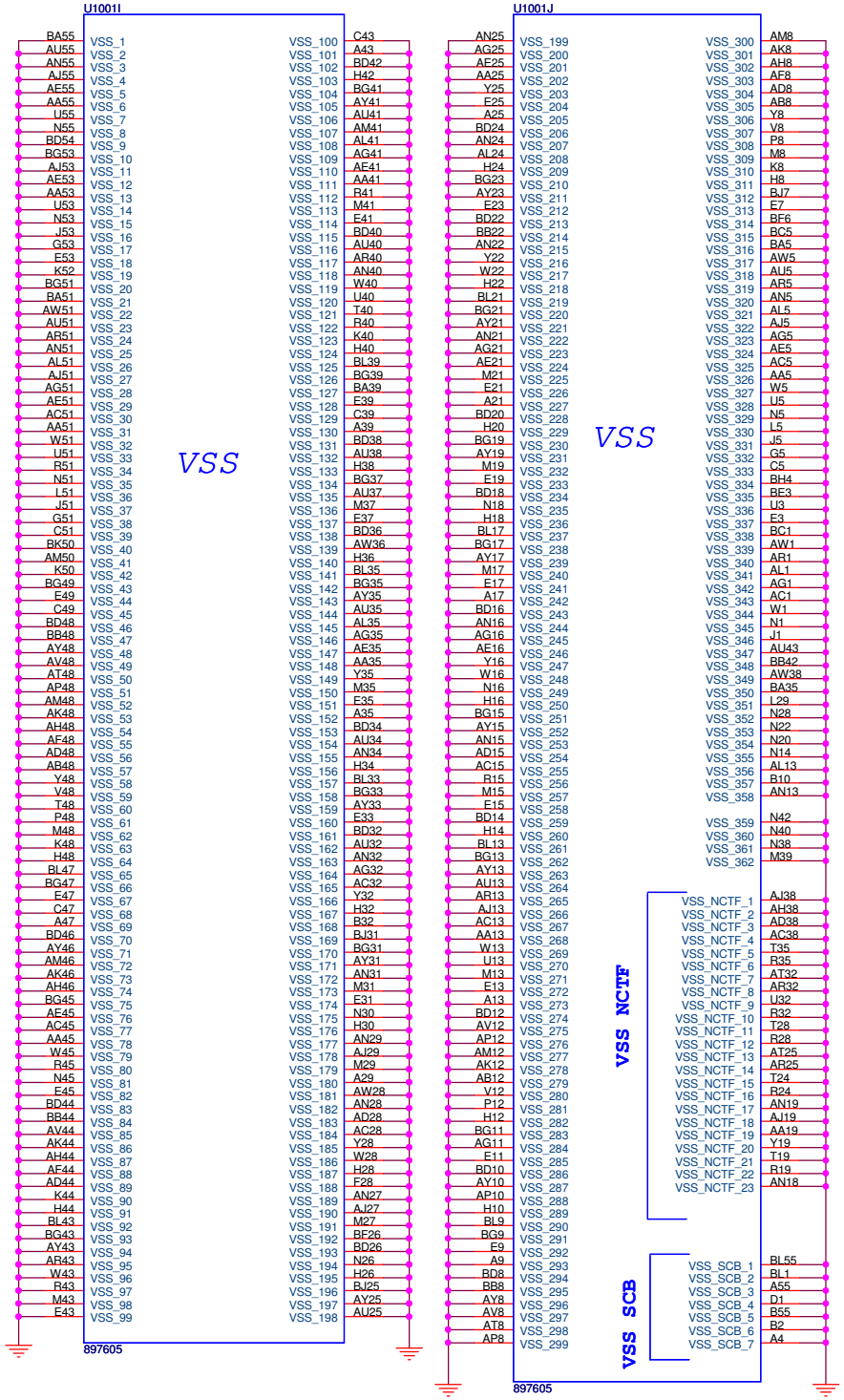
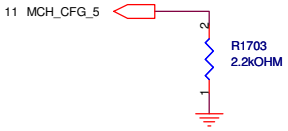


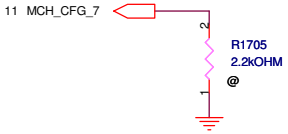

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : NB GS45 GND | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 16 of 97 | |

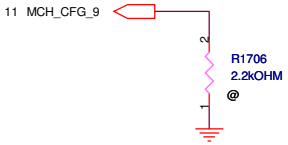



**CFG5 : DMI STRAP**
**H = DMI X 4 (Default)**
**L = DMI X 2**

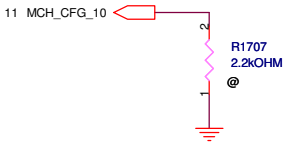
**CFG6 : ITPM Host Interface (Relate to SPI_MOSI)**
H = ITPM Disable (Default)
**L = ITPM enable(Can disable by SW)**



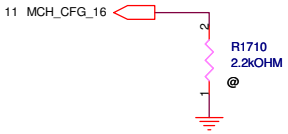

**CFG7 : Intel ME Crypto Strap**
**H = With confidentiality (Default)**
**L = Without confidentiality**



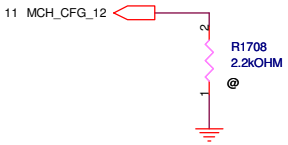

**CFG9 : PCIE Graphic Lane Reverse**
**H = Normal (Default)**
L = Lanes Reverse



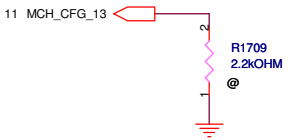

**CFG10 : PCIE Loopback**
**H = Disable (Default)**
L = Enable




**CFG16 : FSB Dynamic ODT**
**H =Enable (Default)**
L = Disable

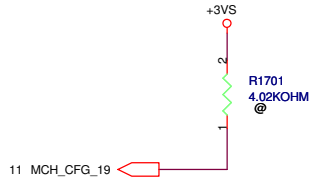



**CFG12 : ALL-Z Mode**
**H =Disable (Default)**
L = Enable

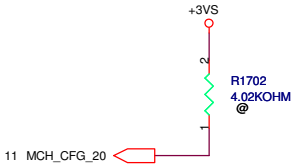



**CFG13 : XOR Mode**
**H = Disable (Default)**
L = Enable

**CFG [13:12] : XOR/ALL-Z**
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
**11= Normal Operation (Default)**




**CFG19 : DMI Lane Reversal**
H =DMI Lane Reversal
**L = Normal (Default)**




**CFG20 : SDVO/PCIE CONCURRENT MODE**
**L = Only Digital display port or PCIE is Operational (Default)**
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : NB GS45 STRAPPING | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 17 of 97 | |

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| C | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 18 of 97

<Variant Name>

Title :

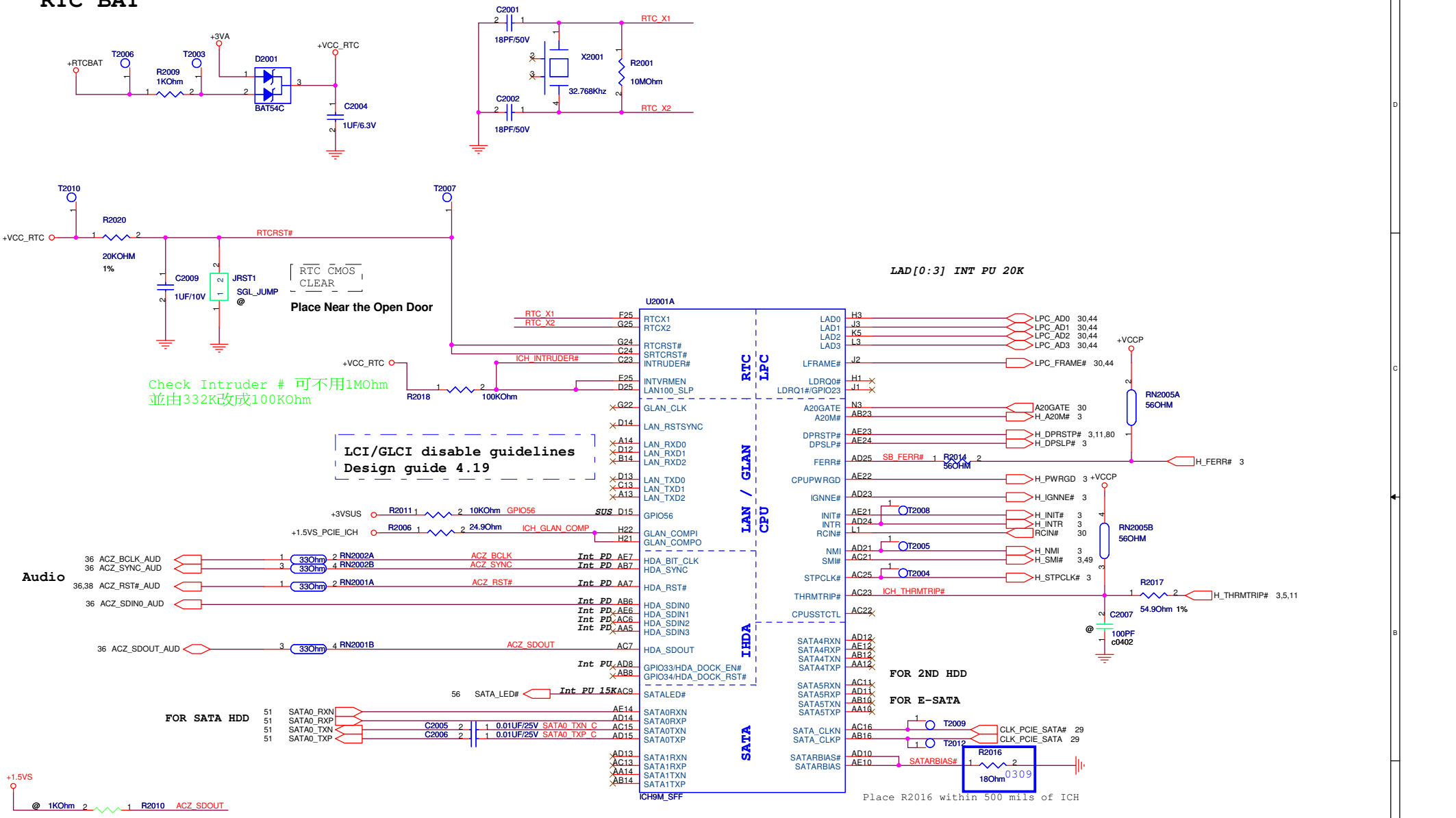
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 19 of 97

# RTC BAT




**[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap**

***00 = Reserved***
***01= Enter XOR Chain***
***10= Normal Operation (Default)***
***11= Set PCIe Port Config Bit 1***

**GPIO33:Flash Descriptor Security Override**

**High = Enable ( Default )**
**Low = Overridden**

<Variant Name>

SB ICH9M PCI PCIE DMI USB

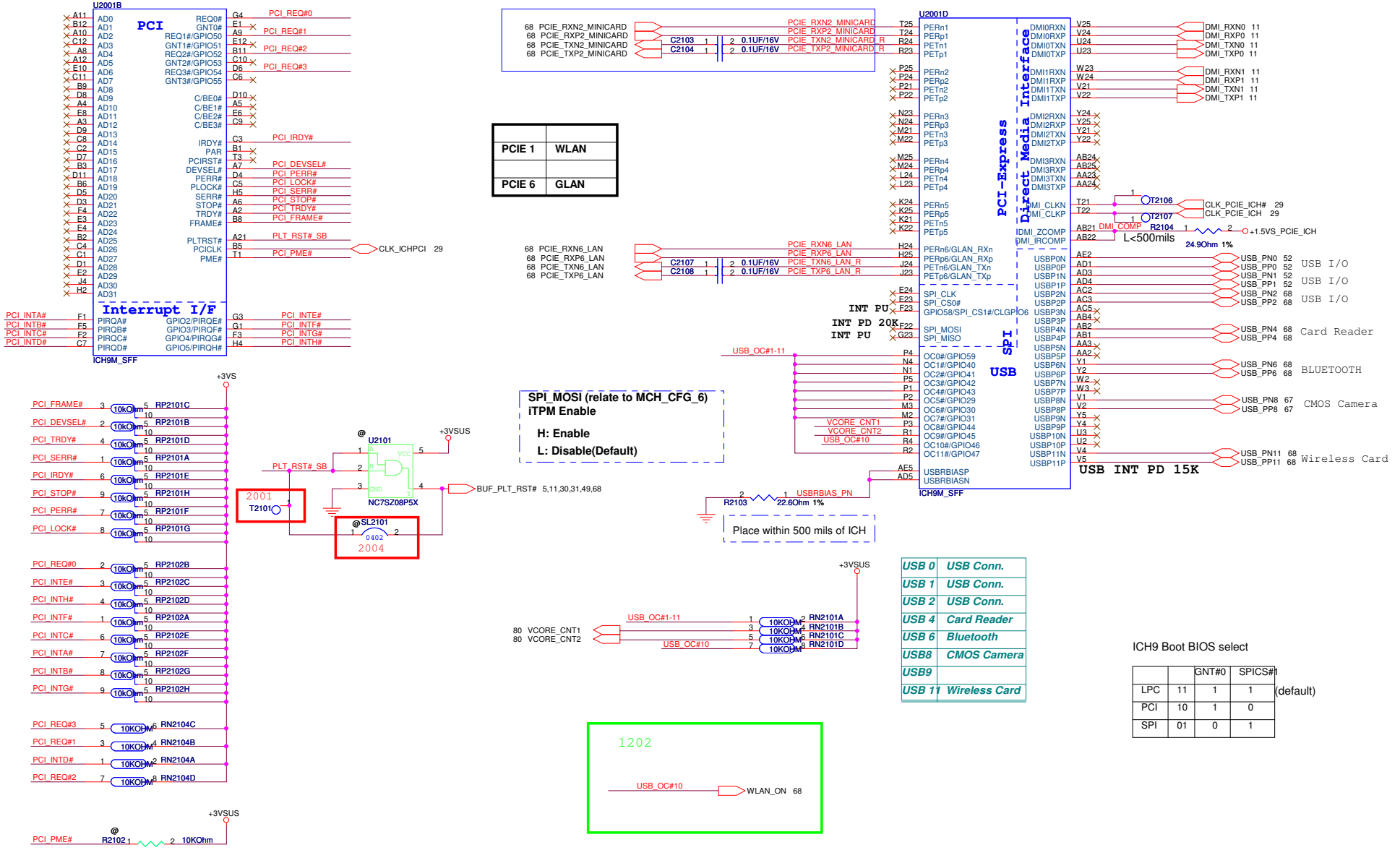
Title :

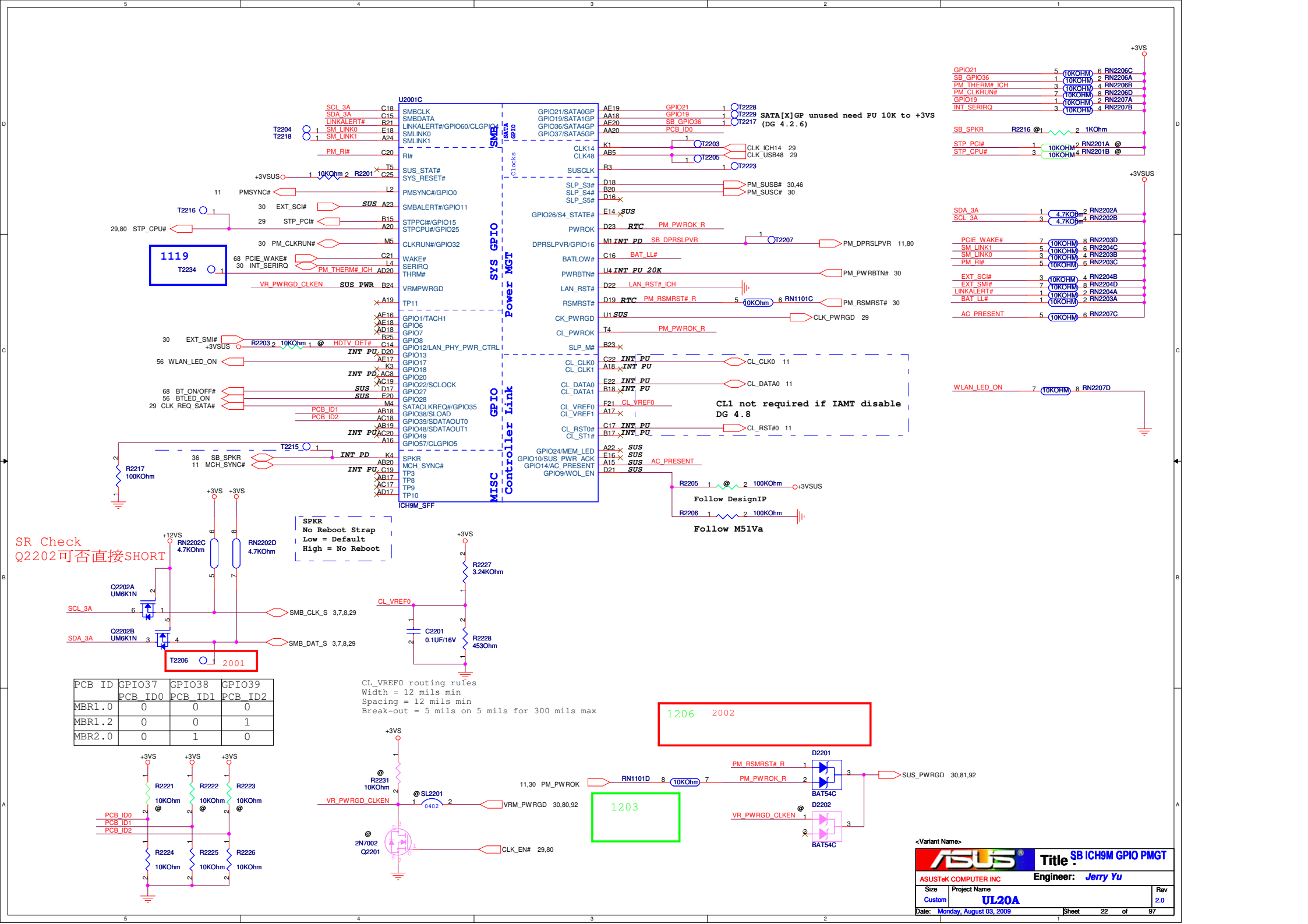
ASUSTeK COMPUTER INC

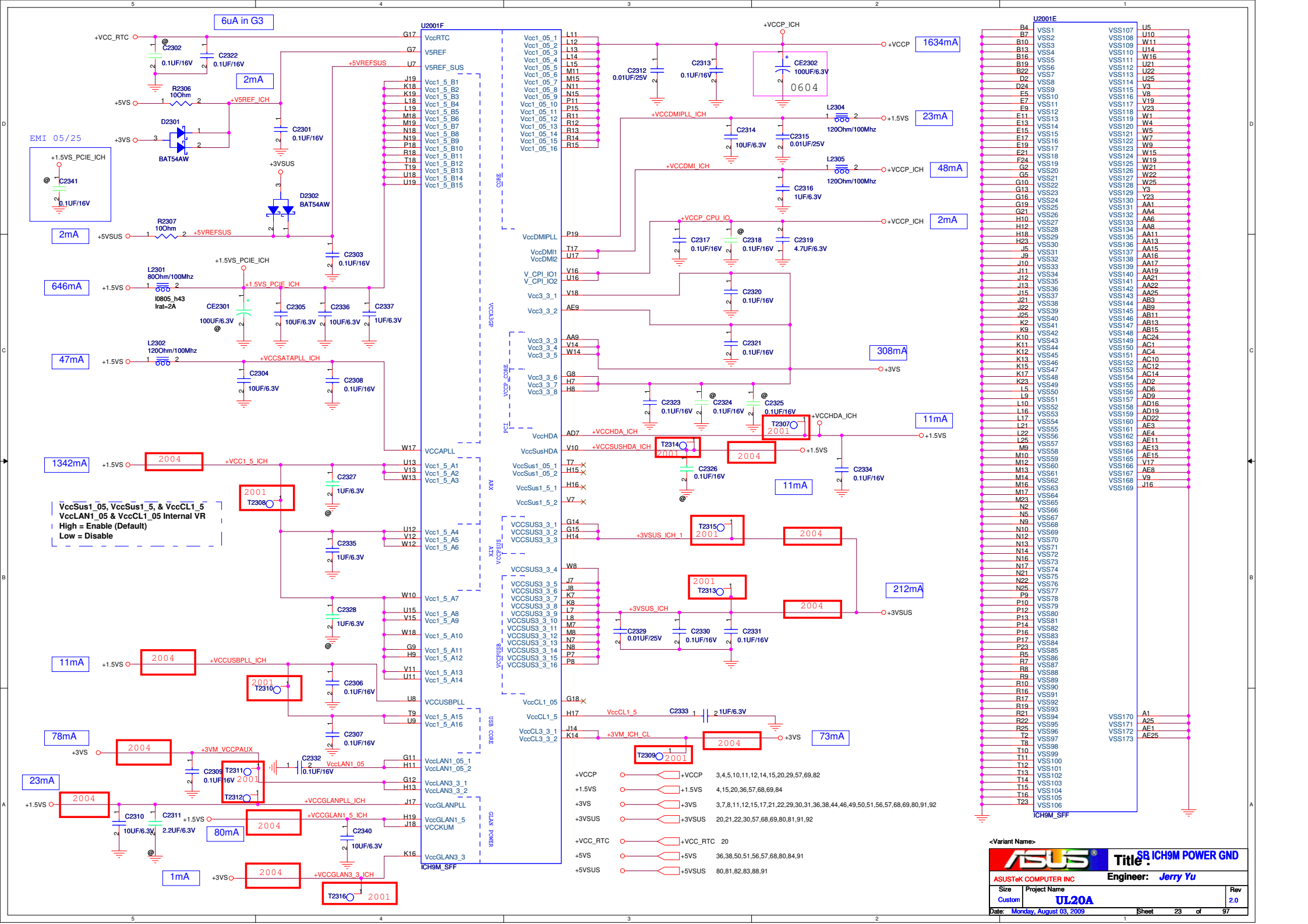
Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 20 of 97


U2001B
PCI
Interrupt I/F
ICH9M_SFF
U2001D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M_SFF
PCIE 1 WLAN
PCIE 6 GLAN
SPI_MOSI (relate to MCH_CFG_6)
iTPM Enable
H: Enable
L: Disable(Default)
INT PU
INT PD 20K
INT PU
USB INT PD 15K
Place within 500 mils of ICH
1202
USB_OC#10
WLAN_ON 68
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 4 Card Reader
USB 6 Bluetooth
USB8 CMOS Camera
USB9
USB 11 Wireless Card
ICH9 Boot BIOS select
LPC 11 1 1 (default)
PCI 10 1 0
SPI 01 0 1
SB ICH9M PCI PCIE DMI USB
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Project Name UL20A
Size Custom
Rev 2.0
Date: Monday, August 03, 2009
Sheet 21 of 97


U2001C
ICH9M_SFF
SMB
GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA GPIO
Clocks
SCL_3A
SDA_3A
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
SUS_STAT#
SYS_RESET#
PMSYNC#
SMBALERT#/GPIO11
STPPCI#/GPIO15
STPCPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP11
GPIO1/TACH1
GPIO6
GPIO7
GPIO8
GPIO12/LAN_PHY_PWR_CTRL
GPIO13
GPIO17
GPIO18
GPIO20
GPIO22/SCLOCK
GPIO27
GPIO28
SATACLKREQ#/GPIO35
GPIO38/SLOAD
GPIO39/SDATAOUT0
GPIO48/SDATAOUT1
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP8
TP9
TP10
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO3
SMLINK0
SMLINK1
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA4GP
GPIO37/SATA5GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
GPIO26/S4_STATE#
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CL_PWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RSTO#
CL_ST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
SATA[X]GP unused need PU 10K to +3VS (DG 4.2.6)
CL1 not required if IAMT disable DG 4.8
SPKR
No Reboot Strap
Low = Default
High = No Reboot
Follow DesignIP
Follow M51Va
SR Check
Q2202可否直接SHORT
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max
1119
2001
1206 2002
1203
PCB_ID | GPIO37 PCB_ID0 | GPIO38 PCB_ID1 | GPIO39 PCB_ID2
MBR1.0 | 0 | 0 | 0
MBR1.2 | 0 | 0 | 1
MBR2.0 | 0 | 1 | 0
ASUSTeK COMPUTER INC
Title: SB ICH9M GPIO PMGT
Engineer: Jerry Yu
Size: Custom
Project Name: UL20A
Rev: 2.0
Date: Monday, August 03, 2009
Sheet 22 of 97


6uA in G3
U2001F
ICH9M_SFF
U2001E
ICH9M_SFF
EMI 05/25
VccVRM
VccRTC
V5REF
V5REF_SUS
VCCA3GP
VCCA_CORE
VCCP
VccHDA
VccSusHDA
VccSus1_05
VccSus1_5
VCCSUS3_3
VCCSUS1_5
VccCL1_05
VccCL1_5
VccCL3_3
VccLAN1_05
VccLAN3_3
VccGLANPLL
VccGLAN1_5
VCCKUM
VccGLAN3_3
VCCAPLL
VCCUSBPLL
VccLAN1_05_1
VccLAN1_05_2
VccLAN3_3_1
VccLAN3_3_2
VccGLAN1_5
VccGLAN3_3
VccDMIPLL
VccDMI1
VccDMI2
V_CPI_IO1
V_CPI_IO2
Vcc3_3_1
Vcc3_3_2
Vcc3_3_3
Vcc3_3_4
Vcc3_3_5
Vcc3_3_6
Vcc3_3_7
Vcc3_3_8
VccSus1_05_1
VccSus1_05_2
VccSus1_5_1
VccSus1_5_2
VCCSUS3_3_1
VCCSUS3_3_2
VCCSUS3_3_3
VCCSUS3_3_4
VCCSUS3_3_5
VCCSUS3_3_6
VCCSUS3_3_7
VCCSUS3_3_8
VCCSUS3_3_9
VCCSUS3_3_10
VCCSUS3_3_11
VCCSUS3_3_12
VCCSUS3_3_13
VCCSUS3_3_14
VCCSUS3_3_15
VCCSUS3_3_16
VccCL1_5
VccCL3_3_1
VccCL3_3_2
Vcc1_05_1
Vcc1_05_2
Vcc1_05_3
Vcc1_05_4
Vcc1_05_5
Vcc1_05_6
Vcc1_05_7
Vcc1_05_8
Vcc1_05_9
Vcc1_05_10
Vcc1_05_11
Vcc1_05_12
Vcc1_05_13
Vcc1_05_14
Vcc1_05_15
Vcc1_05_16
Vcc1_5_B1
Vcc1_5_B2
Vcc1_5_B3
Vcc1_5_B4
Vcc1_5_B5
Vcc1_5_B6
Vcc1_5_B7
Vcc1_5_B8
Vcc1_5_B9
Vcc1_5_B10
Vcc1_5_B11
Vcc1_5_B12
Vcc1_5_B13
Vcc1_5_B14
Vcc1_5_B15
Vcc1_5_A1
Vcc1_5_A2
Vcc1_5_A3
Vcc1_5_A4
Vcc1_5_A5
Vcc1_5_A6
Vcc1_5_A7
Vcc1_5_A8
Vcc1_5_A9
Vcc1_5_A10
Vcc1_5_A11
Vcc1_5_A12
Vcc1_5_A13
Vcc1_5_A14
Vcc1_5_A15
Vcc1_5_A16
+VCC_RTC
+5VSUS
+5VREFSUS
+5VS
+3VS
+3VSUS
+1.5VS_PCIE_ICH
+1.5VS
+VCCP_ICH
+VCCP
+VCCDMIPLL_ICH
+VCCDMI_ICH
+VCCP_CPU_IO
+V5REF_ICH
+VCCSATAPLL_ICH
+VCC1_5_ICH
+VCCUSBPLL_ICH
+3VM_VCCPAUX
+VCCGLANPLL_ICH
+VCCGLAN1_5_ICH
+VCCGLAN3_3_ICH
+VCCHDA_ICH
+VCCSUSHDA_ICH
+3VSUS_ICH_1
+3VSUS_ICH
+3VM_ICH_CL
VccLAN1_05
VccCL1_5
C2302 0.1UF/16V
C2322 0.1UF/16V
C2301 0.1UF/16V
C2303 0.1UF/16V
C2341 0.1UF/16V
C2312 0.01UF/25V
C2313 0.1UF/16V
CE2302 100UF/6.3V 0604
C2314 10UF/6.3V
C2315 0.01UF/25V
C2316 1UF/6.3V
C2317 0.1UF/16V
C2318 0.1UF/16V
C2319 4.7UF/6.3V
C2320 0.1UF/16V
C2321 0.1UF/16V
C2323 0.1UF/16V
C2324 0.1UF/16V
C2325 0.1UF/16V
C2326 0.1UF/16V
C2327 1UF/6.3V
C2328 1UF/6.3V
C2329 0.01UF/25V
C2330 0.1UF/16V
C2331 0.1UF/16V
C2333 1UF/6.3V
C2334 0.1UF/16V
C2335 1UF/6.3V
C2304 10UF/6.3V
C2305 10UF/6.3V
C2306 0.1UF/16V
C2307 0.1UF/16V
C2308 0.1UF/16V
C2309 0.1UF/16V
C2310 10UF/6.3V
C2311 2.2UF/6.3V
C2332 0.1UF/16V
C2336 10UF/6.3V
C2337 1UF/6.3V
C2340 10UF/6.3V
CE2301 100UF/6.3V
R2306 10Ohm
R2307 10Ohm
D2301 BAT54AW
D2302 BAT54AW
L2301 80Ohm/100Mhz I0805_h43 Irat=2A
L2302 120Ohm/100Mhz
L2304 120Ohm/100Mhz
L2305 120Ohm/100Mhz
T2307 2001
T2314 2001
T2315 2001
T2313 2001
T2309 2001
T2308 2001
T2310 2001
T2311 2001
T2312 2001
T2316 2001
2004
1634mA
23mA
48mA
2mA
308mA
11mA
212mA
73mA
646mA
47mA
1342mA
78mA
80mA
1mA
VccSus1_05, VccSus1_5, & VccCL1_5
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
+VCCP 3,4,5,10,11,12,14,15,20,29,57,69,82
+1.5VS 4,15,20,36,57,68,69,84
+3VS 3,7,8,11,12,15,17,21,22,29,30,31,36,38,44,46,49,50,51,56,57,68,69,80,91,92
+3VSUS 20,21,22,30,57,68,69,80,81,91,92
+VCC_RTC 20
+5VS 36,38,50,51,56,57,68,80,84,91
+5VSUS 80,81,82,83,88,91
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66 VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129 VSS130 VSS131 VSS132 VSS133 VSS134 VSS135 VSS136 VSS137 VSS138 VSS139 VSS140 VSS141 VSS142 VSS143 VSS144 VSS145 VSS146 VSS147 VSS148 VSS149 VSS150 VSS151 VSS152 VSS153 VSS154 VSS155 VSS156 VSS157 VSS158 VSS159 VSS160 VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173
<Variant Name>
Title: SB ICH9M POWER GND
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size: Custom
Project Name: UL20A
Rev: 2.0
Date: Monday, August 03, 2009
Sheet 23 of 97

<Variant Name>

SB ICH9M SPI ROM & HDCP

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 24 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 25 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 26 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 27 of 97

<Variant Name>

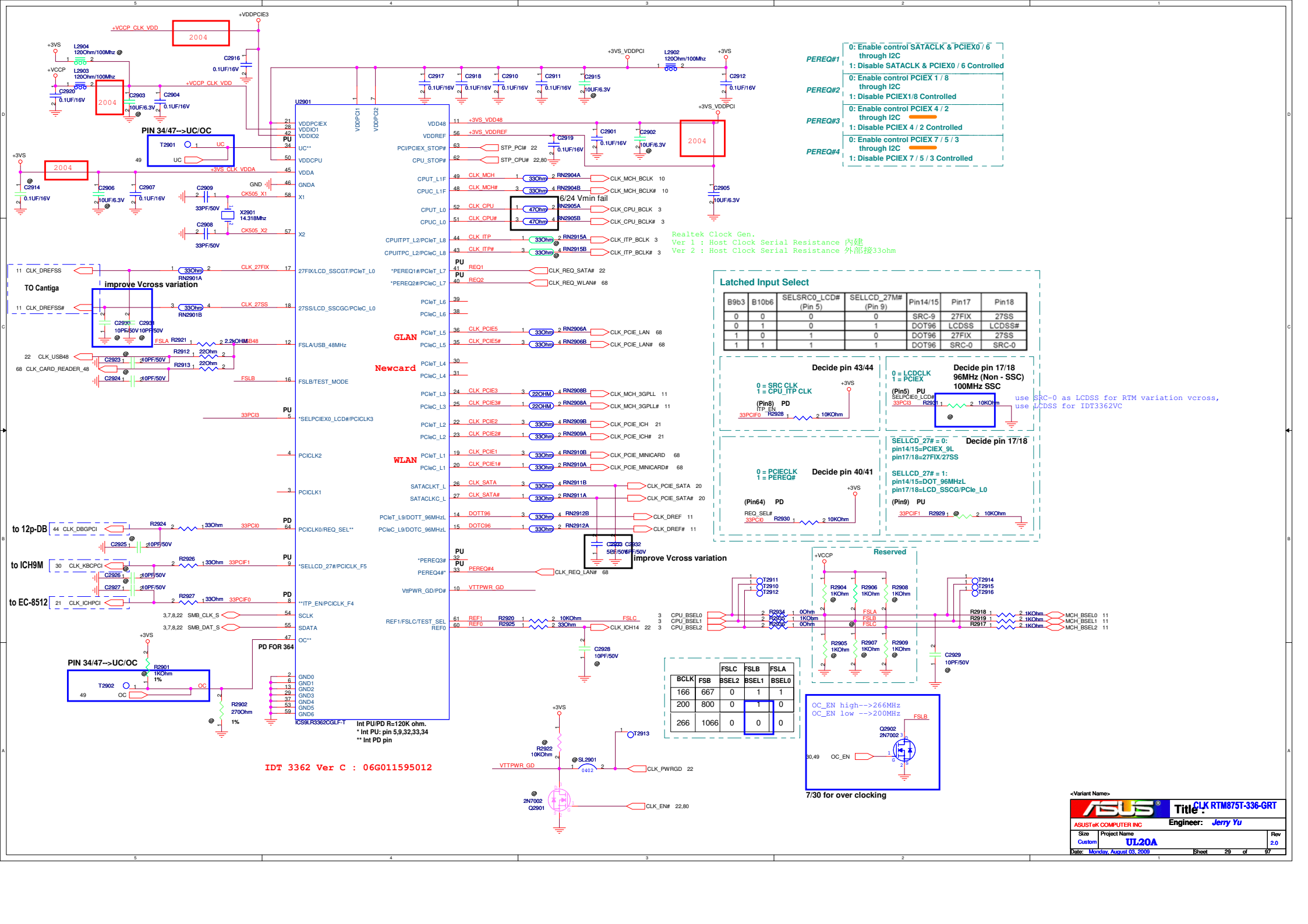
Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 28 of 97


U2901
ICS9LR3362CGLF-T
PIN 34/47-->UC/OC
PIN 34/47-->UC/OC
PD FOR 364
TO Cantiga
improve Vcross variation
improve Vcross variation
6/24 Vmin fail
Realtek Clock Gen.
Ver 1 : Host Clock Serial Resistance 內建
Ver 2 : Host Clock Serial Resistance 外部接33ohm
GLAN
Newcard
WLAN
to 12p-DB
to ICH9M
to EC-8512
Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin
IDT 3362 Ver C : 06G011595012
PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled
PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled
PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled
PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled
Latched Input Select
B9b3 B10b6 SELSRC0_LCD# (Pin 5) SELLCD_27M# (Pin 9) Pin14/15 Pin17 Pin18
0 0 0 0 SRC-9 27FIX 27SS
0 1 0 1 DOT96 LCDSS LCDSS#
1 0 1 0 DOT96 27FIX 27SS
1 1 1 1 DOT96 SRC-0 SRC-0
Decide pin 43/44
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 17/18
96MHz (Non - SSC)
100MHz SSC
0 = LCDCLK
1 = PCIEX
use SRC-0 as LCDSS for RTM variation vcross,
use LCDSS for IDT3362VC
Decide pin 40/41
0 = PCIECLK
1 = PEREQ#
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
Reserved
BCLK FSB FSLC BSEL2 FSLB BSEL1 FSLA BSEL0
166 667 0 1 1
200 800 0 1 0
266 1066 0 0 0
OC_EN high-->266MHz
OC_EN low -->200MHz
7/30 for over clocking
<Variant Name>
Title : CLK RTM875T-336-GRT
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size Custom
Project Name UL20A
Rev 2.0
Date: Monday, August 03, 2009
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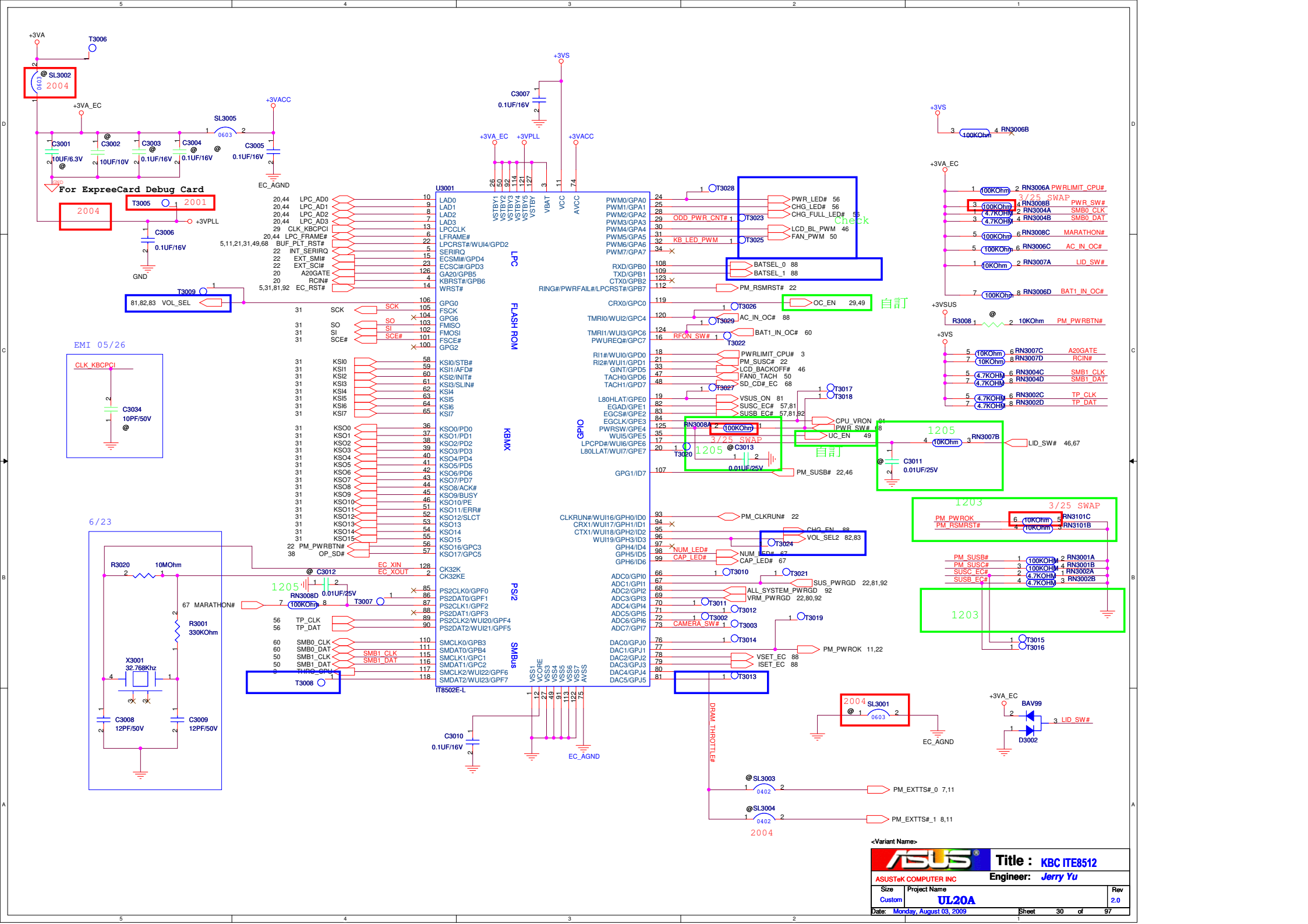
U3001
IT8502E-L
LPC
FLASH ROM
KBMX
PS2
SMBus
GPIO
LAD0
LAD1
LAD2
LAD3
LPCCLK
LFRAME#
LPCRST#/WUI4/GPD2
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
GA20/GPB5
KBRST#/GPB6
WRST#
GPG0
FSCK
GPG6
FMISO
FMOSI
FSCE#
GPG2
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSO16/GPC3
KSO17/GPC5
CK32K
CK32KE
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/WUI20/GPF4
PS2DAT2/WUI21/GPF5
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/WUI22/GPF6
SMDAT2/WUI23/GPF7
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7
RXD/GPB0
TXD/GPB1
CTX0/GPB2
RING#/PWRFAIL#/LPCRST#/GPB7
CRX0/GPC0
TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6
PWUREQ#/GPC7
RI1#/WUI0/GPD0
RI2#/WUI1/GPD1
GINT/GPD5
TACH0/GPD6
TACH1/GPD7
L80HLAT/GPE0
EGAD/GPE1
EGCS#/GPE2
EGCLK/GPE3
PWRSW/GPE4
WUI5/GPE5
LPCPD#/WUI6/GPE6
L80LLAT/WUI7/GPE7
GPG1/ID7
CLKRUN#/WUI16/GPH0/ID0
CRX1/WUI17/GPH1/ID1
CTX1/WUI18/GPH2/ID2
WUI19/GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7
DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5
VSTBY1
VSTBY2
VSTBY3
VSTBY4
VSTBY5
VSTBY
VBAT
VCC
AVCC
VSS1
VCORE
VSS3
VSS4
VSS5
VSS6
VSS7
AVSS
+3VA
+3VS
+3VACC
+3VA_EC
+3VPLL
+3VSUS
EC_AGND
GND
T3006
SL3002
SL3005
C3001
C3002
C3003
C3004
C3005
C3006
C3007
C3008
C3009
C3010
C3011
C3012
C3013
C3034
10UF/6.3V
10UF/10V
0.1UF/16V
10PF/50V
12PF/50V
0.01UF/25V
For ExpreeCard Debug Card
T3005
T3009
VOL_SEL
SCK
SO
SI
SCE#
KSI[0..7]
KSO[0..15]
PM_PWRBTN#
OP_SD#
EC_XIN
EC_XOUT
TP_CLK
TP_DAT
SMB0_CLK
SMB0_DAT
SMB1_CLK
SMB1_DAT
T3008
R3020
10MOhm
R3001
330KOhm
X3001
32.768Khz
RN3008D
0.01UF/25V
T3007
MARATHON#
EMI 05/26
CLK_KBCPCI
6/23
T3028
PWR_LED# 56
CHG_LED# 56
CHG_FULL_LED# 56
ODD_PWR_CNT#
T3023
LCD_BL_PWM 46
FAN_PWM 50
KB_LED_PWM
T3025
BATSEL_0 88
BATSEL_1 88
PM_RSMRST# 22
OC_EN 29,49
T3026
AC_IN_OC# 88
T3029
RFON_SW#
BAT1_IN_OC# 60
T3022
PWRLIMIT_CPU# 3
PM_SUSC# 22
LCD_BACKOFF# 46
FAN0_TACH 50
SD_CD#_EC 68
T3027
VSUS_ON 81
SUSC_EC# 57,81
SUSB_EC# 57,81,92
T3017
T3018
CPU_VRON 91
PWR_SW# 48
UC_EN 49
RN3008A
T3020
@C3013
PM_SUSB# 22,46
PM_CLKRUN# 22
CHG_EN 88
VOL_SEL2 82,83
T3024
NUM_LED#
CAP_LED#
NUM_LED# 67
CAP_LED# 67
T3010
T3021
SUS_PWRGD 22,81,92
ALL_SYSTEM_PWRGD 92
VRM_PWRGD 22,80,92
T3011
T3012
T3002
T3019
CAMERA_SW#
T3003
T3014
PM_PWROK 11,22
VSET_EC 88
ISET_EC 88
T3013
DRAM_THROTTLE#
SL3001
BAV99
D3002
LID_SW# 46,67
SL3003
PM_EXTTS#_0 7,11
SL3004
PM_EXTTS#_1 8,11
RN3006B
RN3006A PWRLIMIT_CPU#
RN3008B PWR_SW#
RN3004A SMB0_CLK
RN3004B SMB0_DAT
RN3008C MARATHON#
RN3006C AC_IN_OC#
RN3007A LID_SW#
RN3006D BAT1_IN_OC#
R3008
PM_PWRBTN#
RN3007C A20GATE
RN3007D RCIN#
RN3004C SMB1_CLK
RN3004D SMB1_DAT
RN3002C TP_CLK
RN3002D TP_DAT
RN3007B
RN3101C
RN3101B
PM_PWROK
PM_RSMRST#
RN3001A
RN3001B
RN3002A
RN3002B
PM_SUSB#
PM_SUSC#
SUSC_EC#
SUSB_EC#
T3015
T3016
3/25 SWAP
1205
1203
2004
2001
Check
自訂
<Variant Name>
Title : KBC ITE8512
ASUSTeK COMPUTER INC
Engineer: Jerry Yu
Size: Custom
Project Name: UL20A
Rev: 2.0
Date: Monday, August 03, 2009
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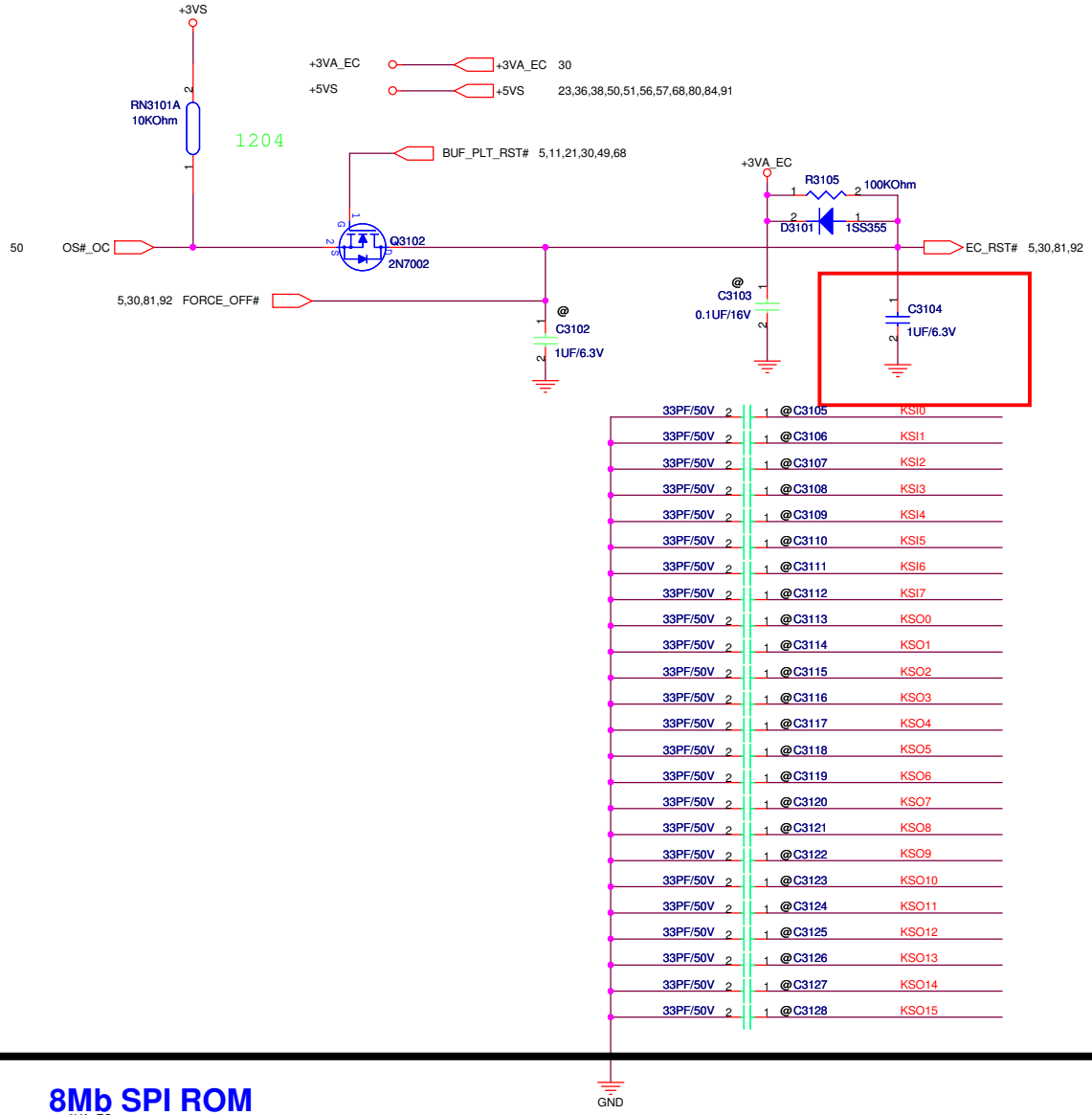
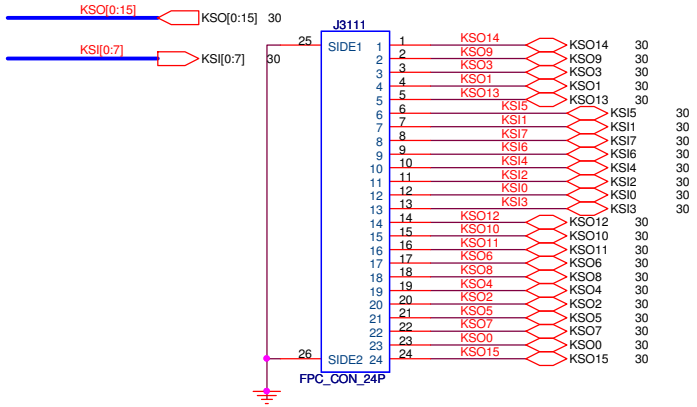
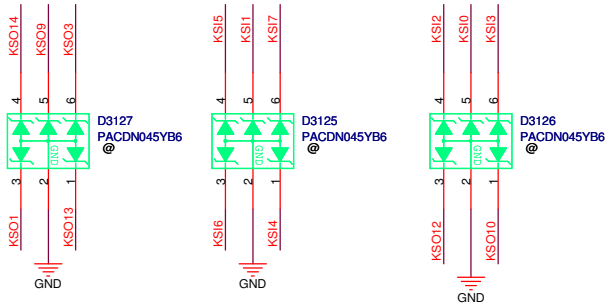
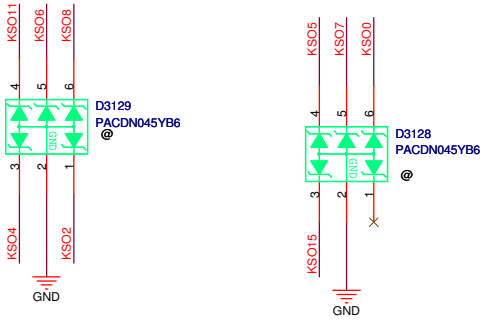
# Internal Keyboard

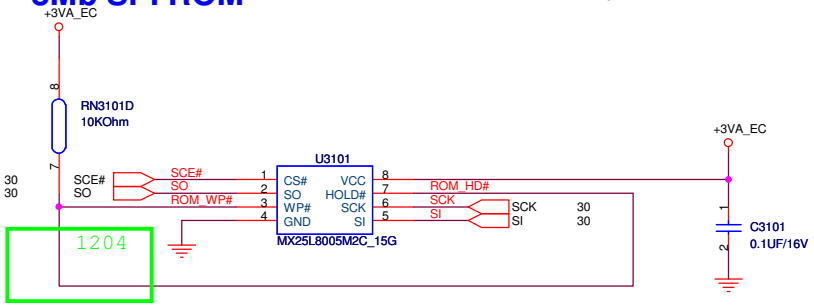



## 8Mb SPI ROM




<Variant Name> ROM FLASH ROM TOUCH PAD KB

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 31 of 97 | |

Parade PS8101T:  Optional /PS
Stuff: R3216 R3219 R3201 R3215
No stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202
R3210 R3208 R3209 R3206 Q3201.

PERICOM PI3VDP411LSZDE:  Optional /PI
No stuff: R3216 R3219 R3201 R3215
Stuff:R3202 R3207 R3204 R3205 R3203 R3220 R3211 Q3202
R3210 R3208 R3209 R3206 Q3201.

<Variant Name>

ASUSTeK COMPUTER INC

Title : LIMA LEVEL SHIFTERS

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| C | UL20A | 2.0 |

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<Variant Name>

Title : AR8131 LAN

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| B | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 33 of 97

<Variant Name>

Title : LAN RJ45 CONN

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 34 of 97

<Variant Name>

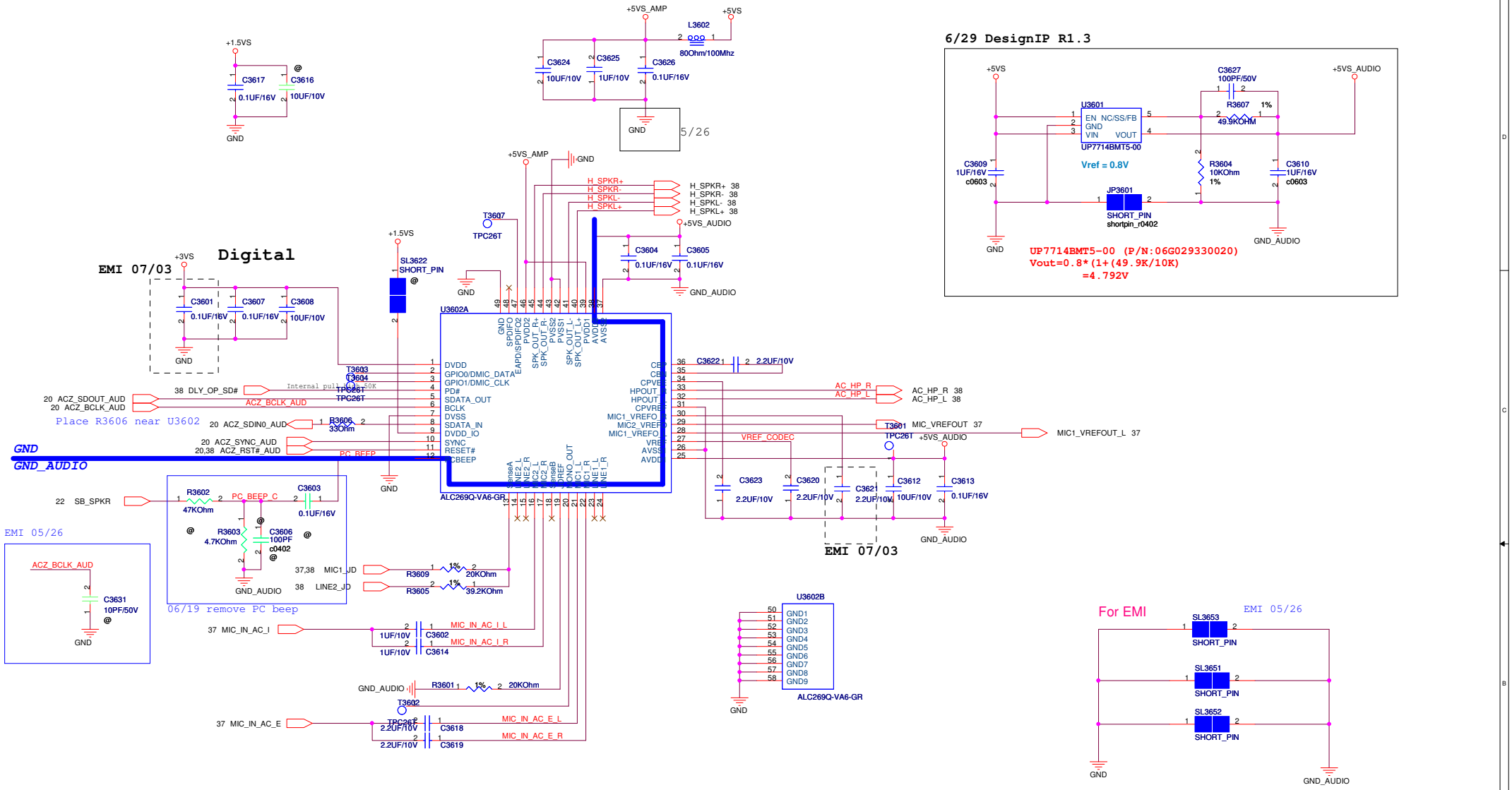
Title :

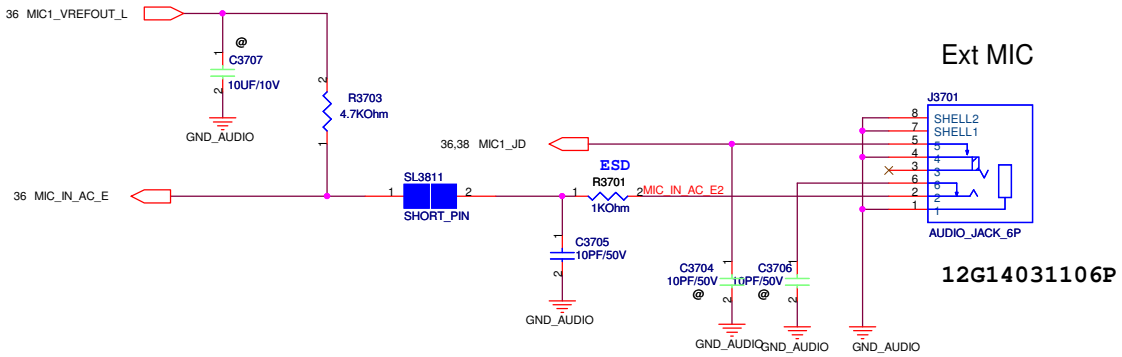
ASUSTeK COMPUTER INC

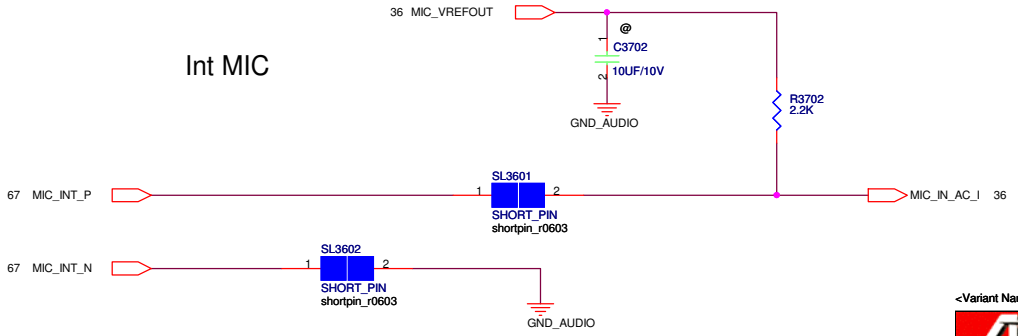
Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 35 of 97

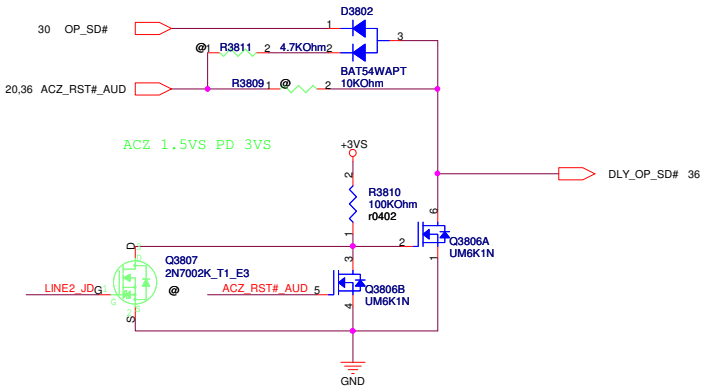

6/29 DesignIP R1.3
UP7714BMT5-00 (P/N:06G029330020)
Vout=0.8*(1+(49.9K/10K)
=4.792V
Vref = 0.8V
Digital
EMI 07/03
EMI 05/26
Place R3606 near U3602
06/19 remove PC beep
For EMI
ALC269Q-VA6-GR
GND
GND_AUDIO
5/26

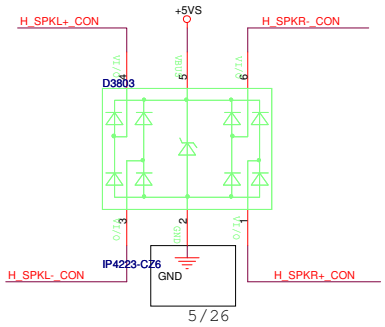


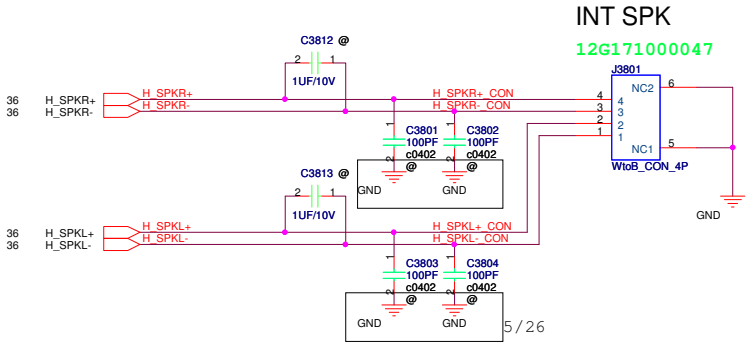



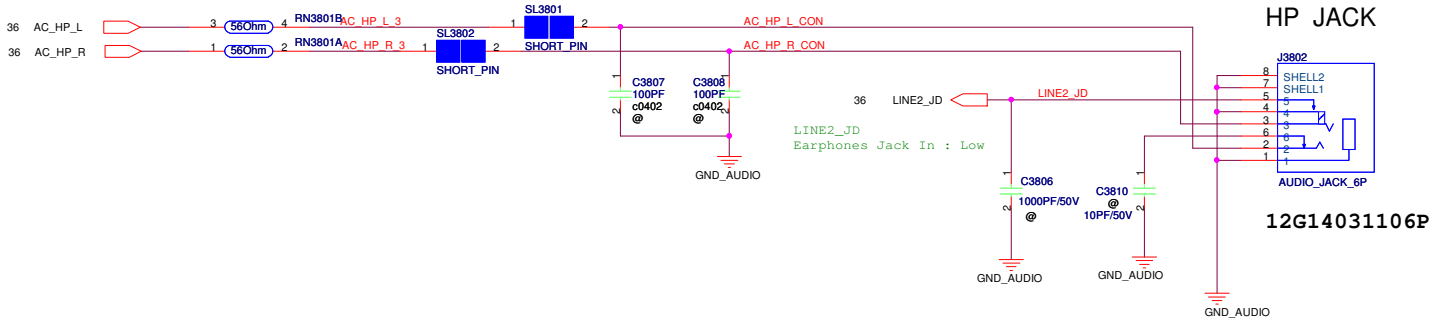

<Variant Name>

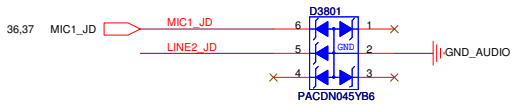
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : AUD MIC CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 37 of 97 | |


30 OP_SD#
D3802
@ R3811 2 4.7KOhm 2
BAT54WAPT
20,36 ACZ_RST#_AUD
R3809 1 @ 2 10KOhm
ACZ 1.5VS PD 3VS
+3VS
R3810
100KOhm
r0402
DLY_OP_SD# 36
Q3806A
UM6K1N
Q3807
2N7002K_T1_E3
@
LINE2_JD
ACZ_RST#_AUD 5
Q3806B
UM6K1N
GND


H_SPKL+_CON
+5VS
H_SPKR-_CON
D3803
IP4223-CZ6
GND
H_SPKL-_CON
H_SPKR+_CON
5/26


INT SPK
12G171000047
C3812 @
1UF/10V
36 H_SPKR+
36 H_SPKR-
H_SPKR+
H_SPKR-
H_SPKR+_CON
H_SPKR-_CON
C3801
100PF
c0402
@
C3802
100PF
c0402
@
GND
C3813 @
1UF/10V
36 H_SPKL+
36 H_SPKL-
H_SPKL+
H_SPKL-
H_SPKL+_CON
H_SPKL-_CON
C3803
100PF
c0402
@
C3804
100PF
c0402
@
J3801
NC2
NC1
W1oB_CON_4P
5/26


HP JACK
36 AC_HP_L
36 AC_HP_R
56Ohm
RN3801B
RN3801A
AC_HP_L_3
AC_HP_R_3
SL3802
SHORT_PIN
SL3801
SHORT_PIN
AC_HP_L_CON
AC_HP_R_CON
C3807
100PF
c0402
@
C3808
100PF
c0402
@
GND_AUDIO
36 LINE2_JD
LINE2_JD
LINE2_JD
Earphones Jack In : Low
C3806
1000PF/50V
@
C3810
@
10PF/50V
J3802
SHELL2
SHELL1
AUDIO_JACK_6P
12G14031106P


36,37 MIC1_JD
MIC1_JD
LINE2_JD
D3801
GND
GND_AUDIO
PACDN045YB6

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

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<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 40 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 41 of 97

<Variant Name>

Title : CARD READER AU6371

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

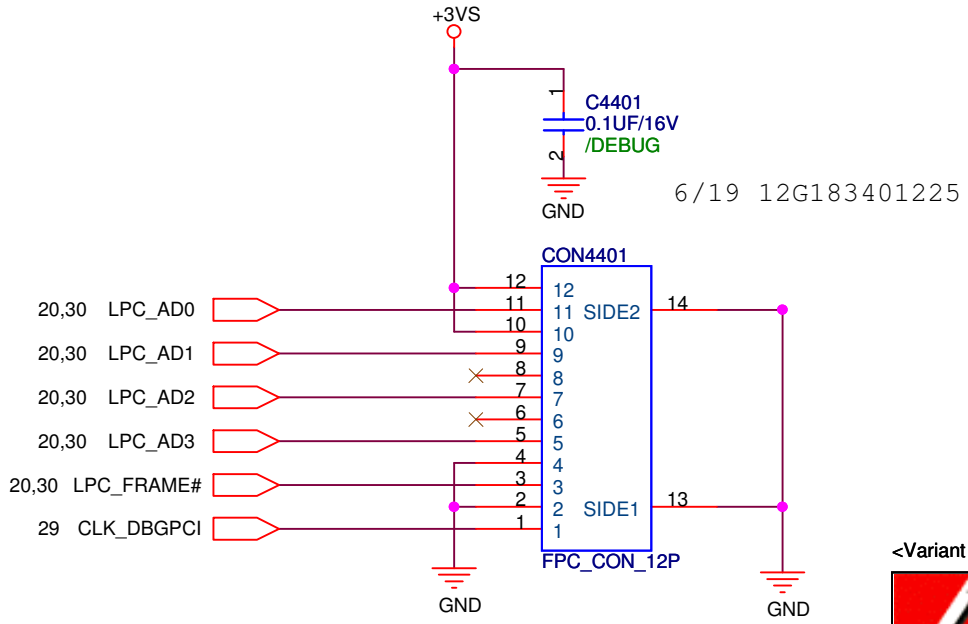
| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 42 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CR EXPRESS CARD CONN | |
| | Engineer: Jerry Yu | |
| Size: A | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 43 of 97 | |

# LPC DEBUG PORT




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : BUG DEBUG PORT | |
| | Engineer: Jerry Yu | |
| Size: A | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 44 of 97 | |

<Variant Name>

Title : HDMI CONN

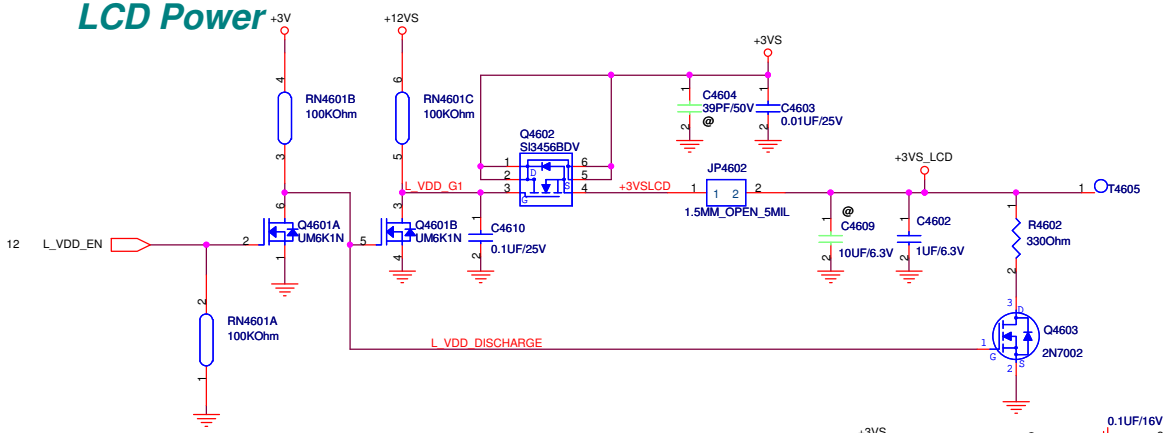
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| C | UL20A | 2.0 |

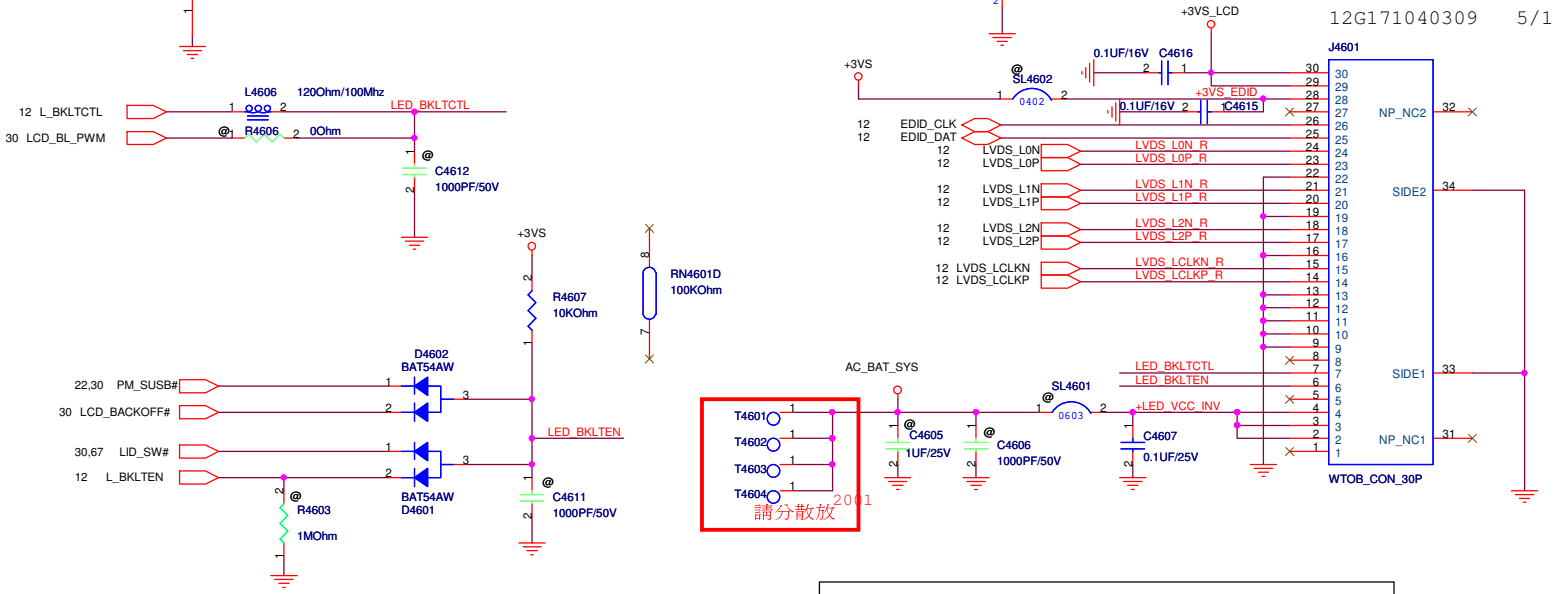
Date: Wednesday, July 29, 2009 Sheet 45 of 97

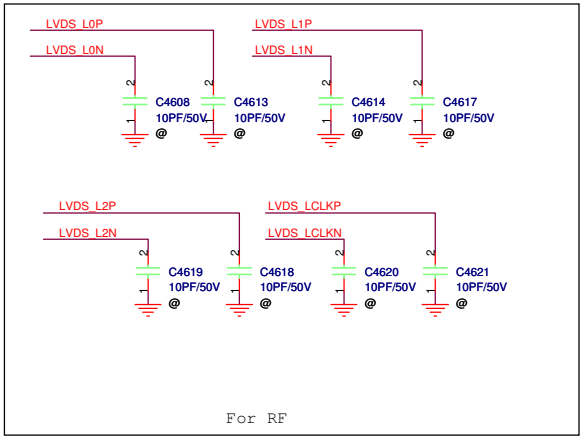
# LCD Power




# LVDS CONN

12G171040309 5/19




<Variant Name>

ASUSTeK COMPUTER INC

Title : LVDS CONN

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 46 of 97

<Variant Name>

Title : CRT D-SUB CONN

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 47 of 97

<Variant Name>

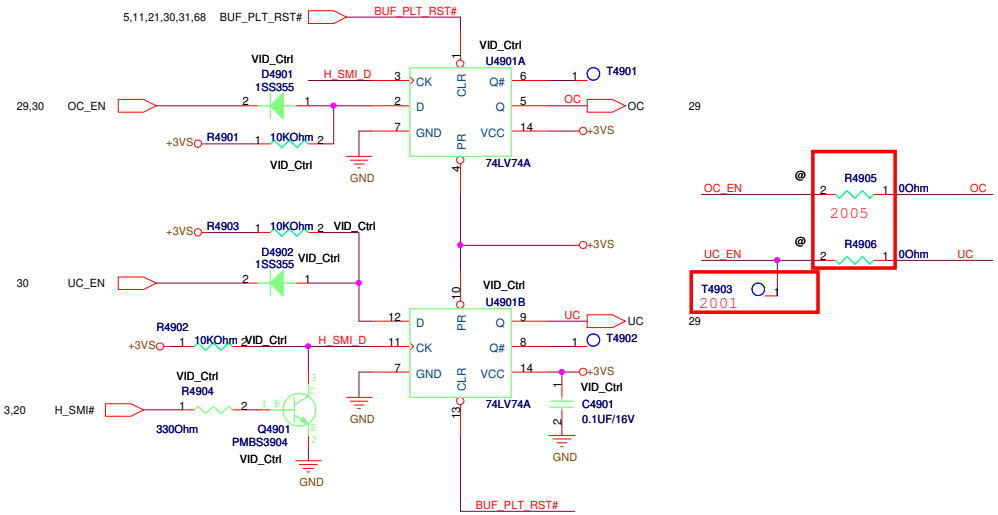
Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 48 of 97







<Variant Name>

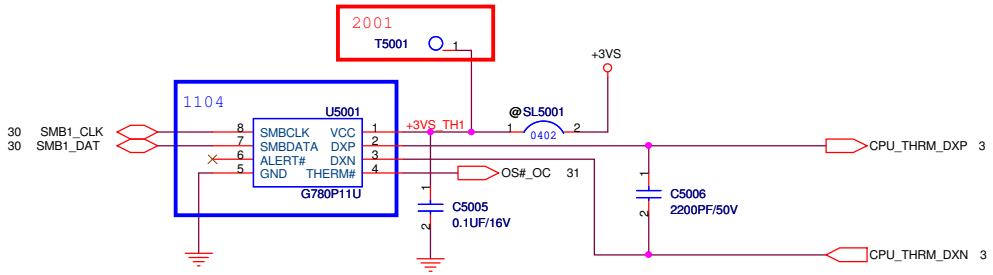
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CRT D-SUB CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 49 of 97 | |

# Thermal Seneor

+3VS — +3VS — 3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,51,56,57,68,69,80,91,92

+VCORE — +VCORE — 4,5,69,80

+5VS — +5VS — 23,36,38,51,56,57,68,80,84,91




U5001 Close to CPU

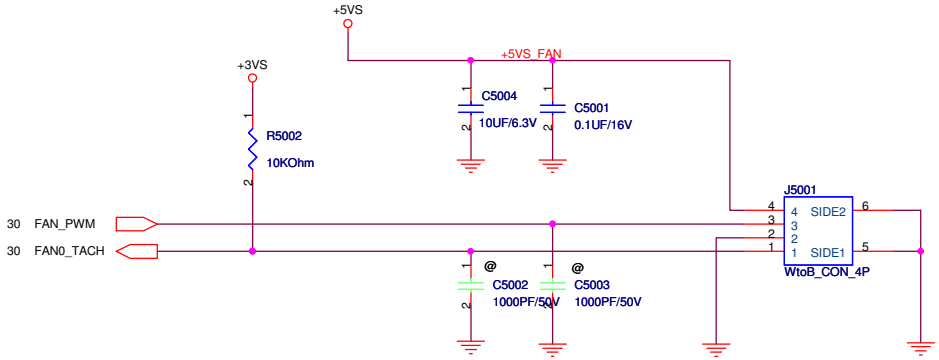
SMBus Address: G780 98H

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

# FAN CONN




<Variant Name>

FAN THERMAL SENSOR FAN CONN

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

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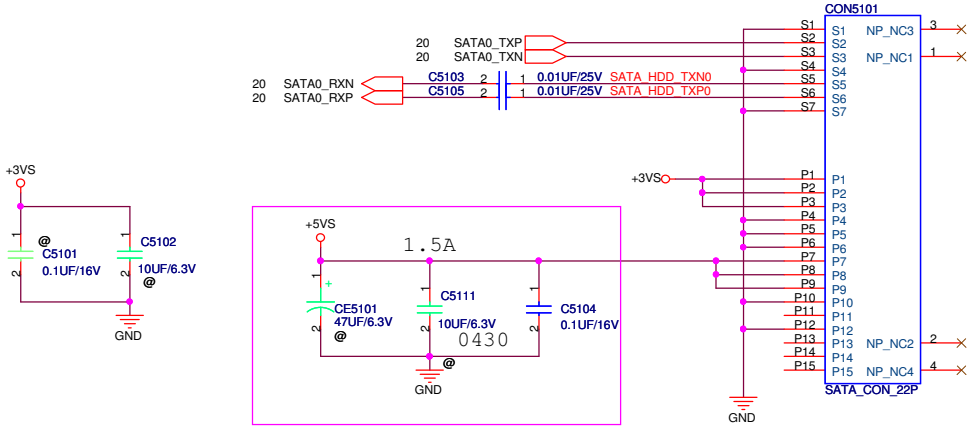
# SATA HDD

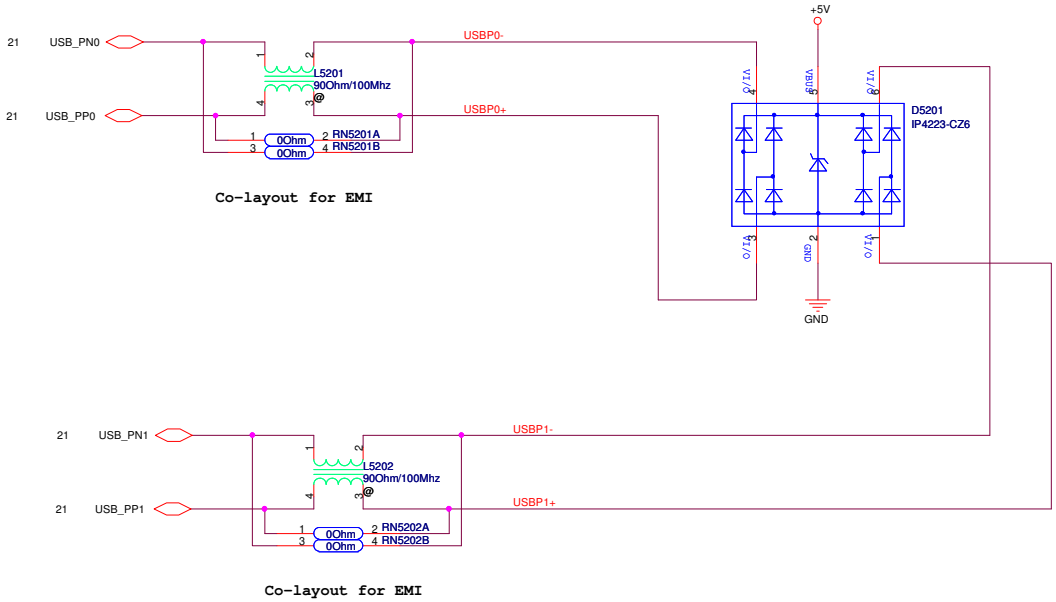


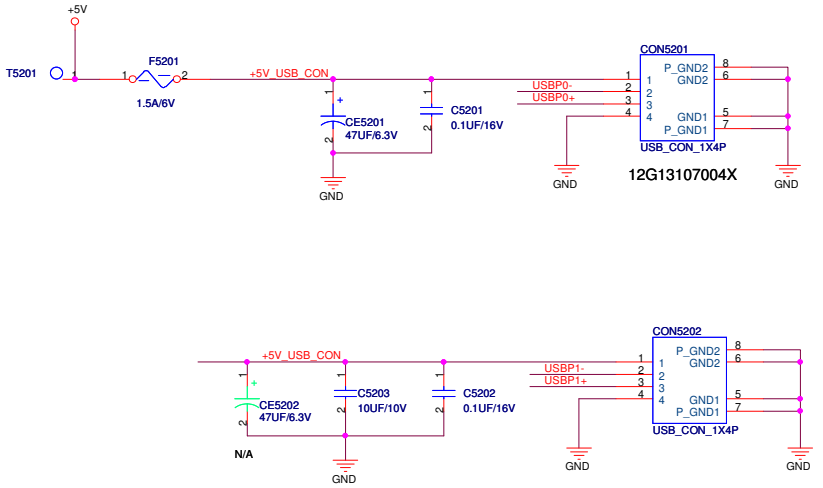

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : XDD SATA HDD CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 51 of 97 | |

# USB CONN *2

## USB : MB




<Variant Name>

ASUSTeK COMPUTER INC

Title : USB 2.0 CONN*2

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 52 of 97

<Variant Name>

Title : PCI MINICARD CONN

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 53 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 54 of 97

<Variant Name>

Title :

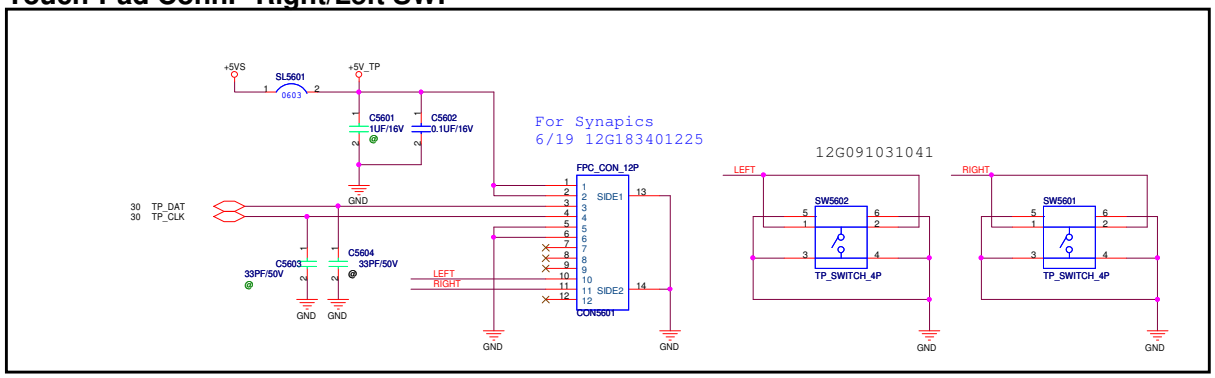
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

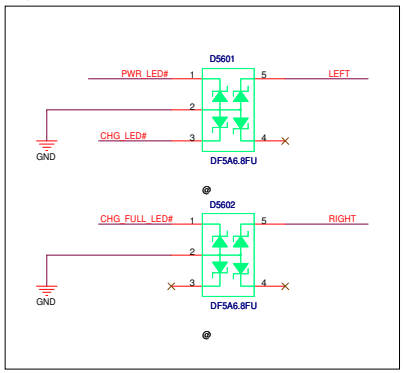
| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 55 of 97

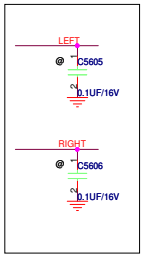
## Touch-Pad Conn. Right/Left SW.



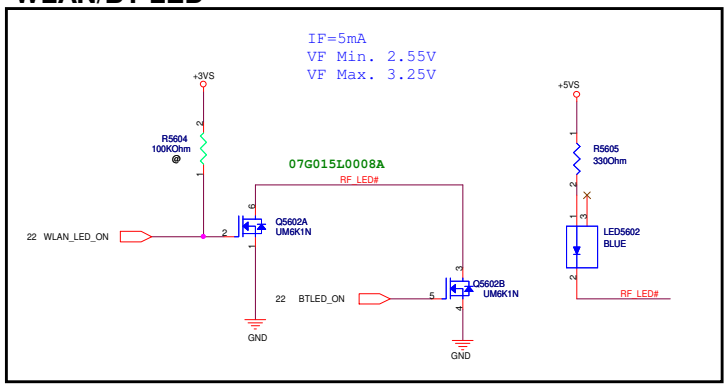

6/22 for ESD



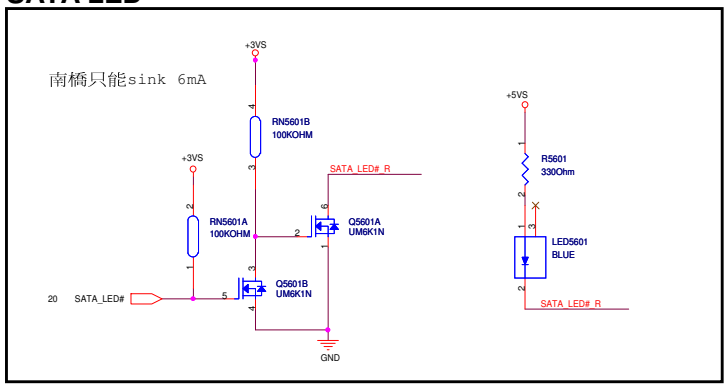

6/30 EMI near BTN



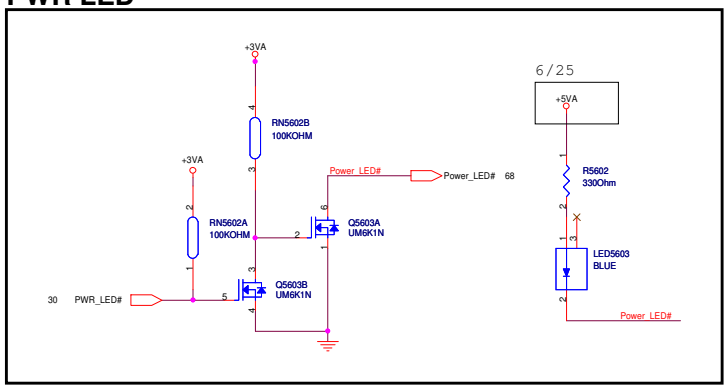

## WLAN/BT LED



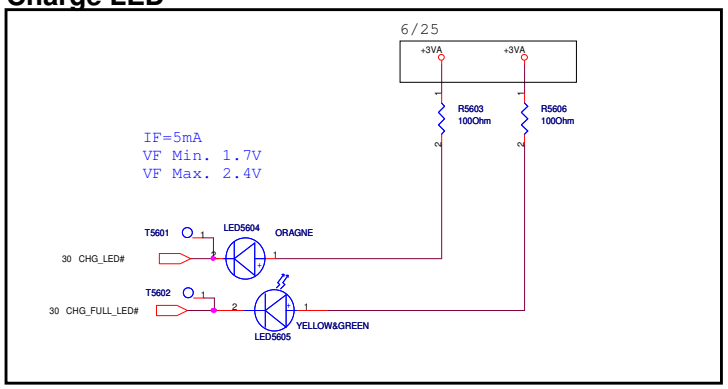

## SATA LED




## PWR LED




## Charge LED




<Variant Name>

LED PWR LED FOC CONN

Title :

ASUSTeK COMPUTER INC

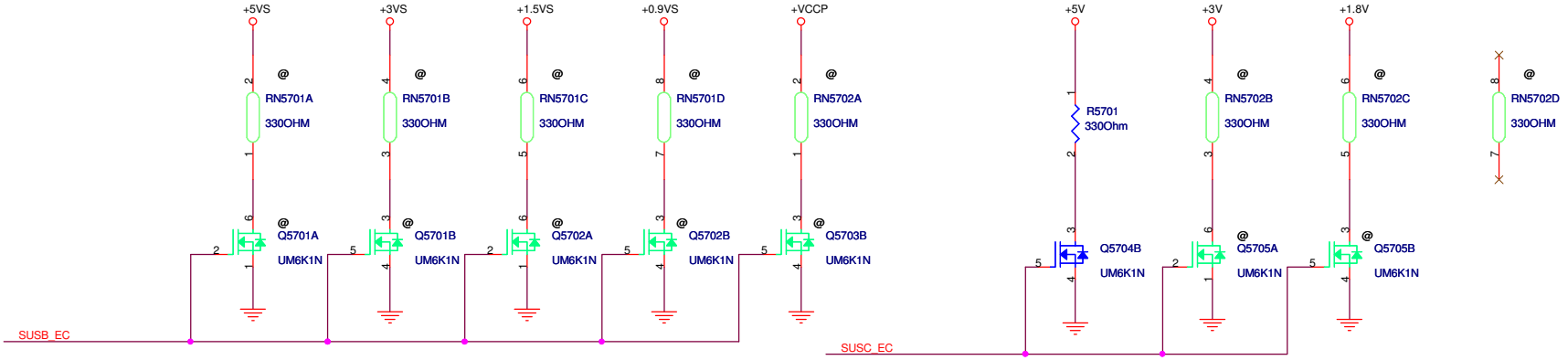
Engineer: Jerry Yu

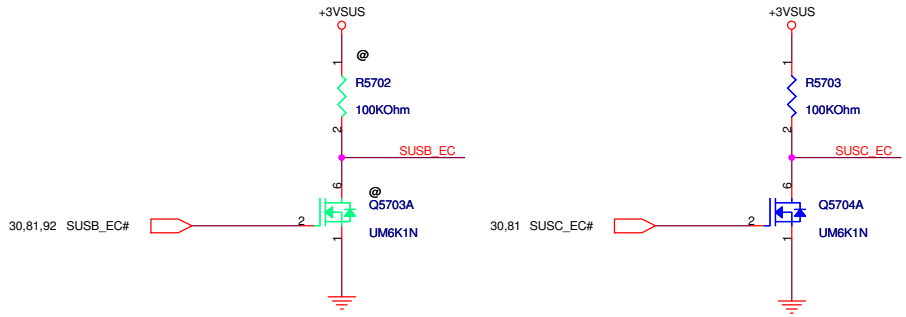
| Size | Project Name | Rev |
|---|---|---|
| C | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 56 of 97

# Discharge Circuit

| | | |
|---|---|---|
| +5VS | +5VS | 23,36,38,50,51,56,68,80,84,91 |
| +3VS | +3VS | 3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,68,69,80,91,92 |
| +1.5VS | +1.5VS | 4,15,20,23,36,68,69,84 |
| +VCCP | +VCCP | 3,4,5,10,11,12,14,15,20,23,29,69,82 |
| +5V | +5V | 52,67,68,91 |
| +3V | +3V | 46,68,91 |
| +1.8V | +1.8V | 7,8,9,11,14,15,83,84,91 |
| +0.9VS | +0.9VS | 9,83 |
| +3VSUS | +3VSUS | 20,21,22,23,30,68,69,80,81,91,92 |




<Variant Name>

DSG DISCHARHE CIRCUIT

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 57 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : | |
| | Engineer: *Jerry Yu* | |
| Size: A | Project Name: **UL20A** | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 58 of 97 | |

<Variant Name>

Title :

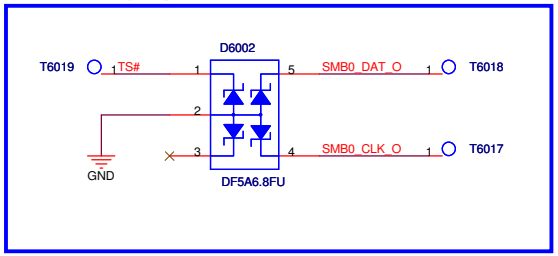
ASUSTeK COMPUTER INC

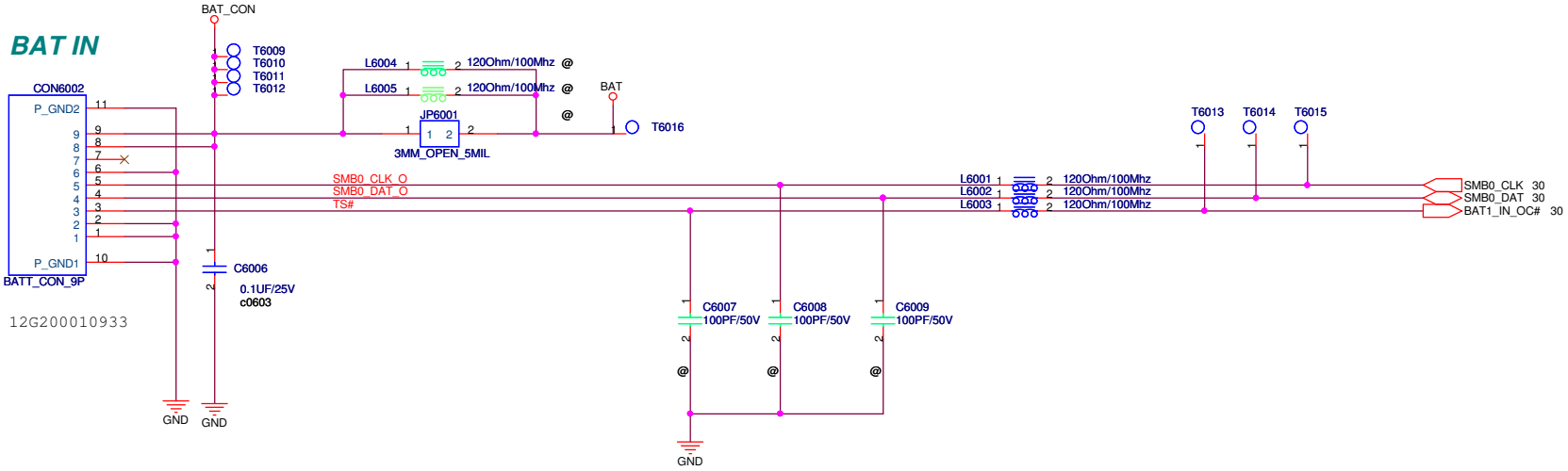
Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 59 of 97

6/22 change part




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : DC DC&BATT CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 60 of 97 | |

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : BT BLUETOOTH CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 61 of 97 | |

<Variant Name>

Title : TPM

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 62 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 63 of 97

<Variant Name>

Title :

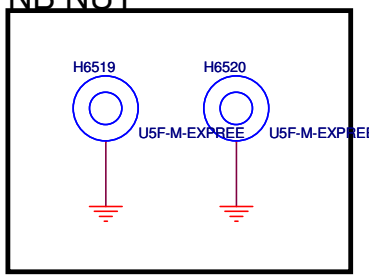
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

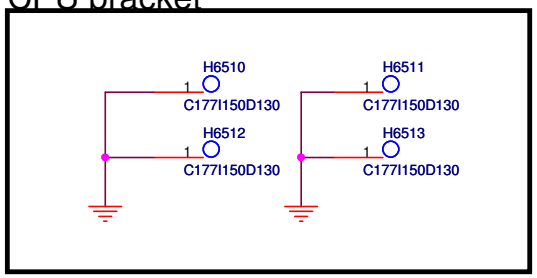
| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 64 of 97

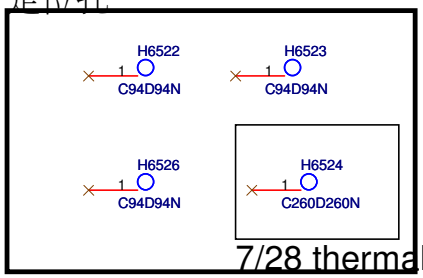
## NB NUT




## CPU bracket



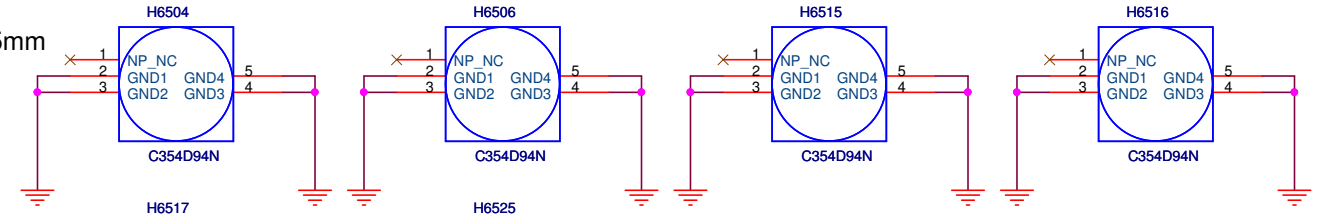

## 定位孔

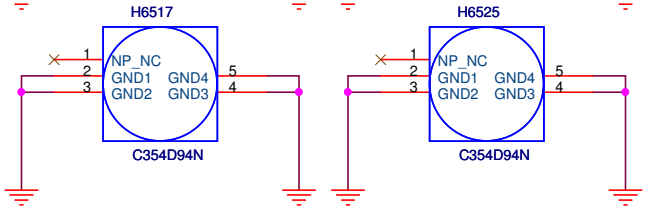



7/28 thermal request

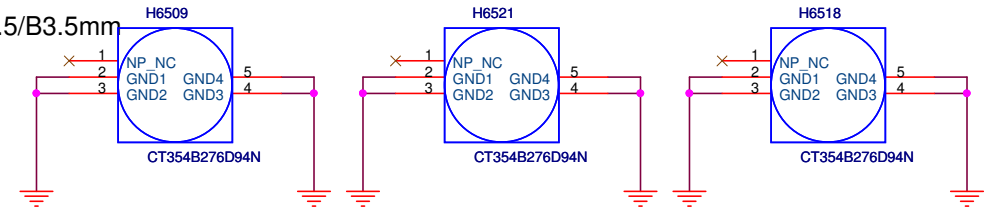
## Screw Holes

1.2/4.5mm

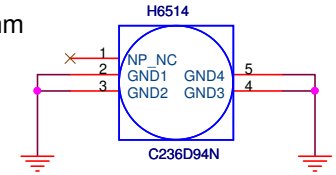


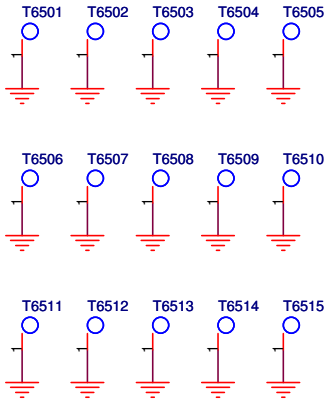




1.2/T4.5/B3.5mm




1.2/3mm




<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : ME SCREW HOLE AMT NUT | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 65 of 97 | |

<Variant Name>

Title :

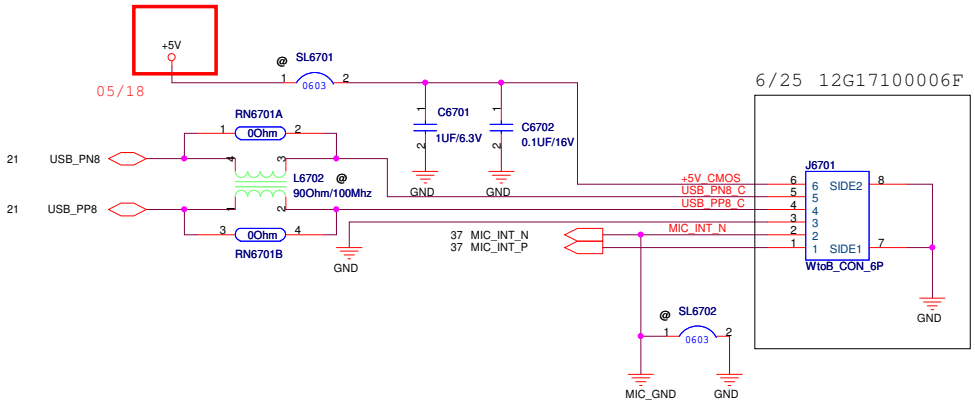
ASUSTeK COMPUTER INC

Engineer: Jerry Yu

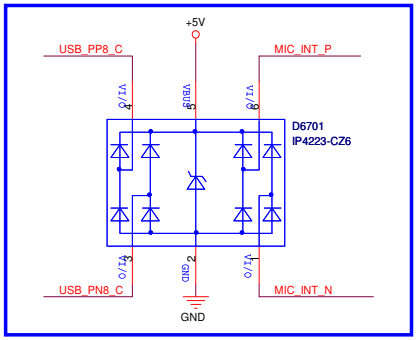
| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 66 of 97

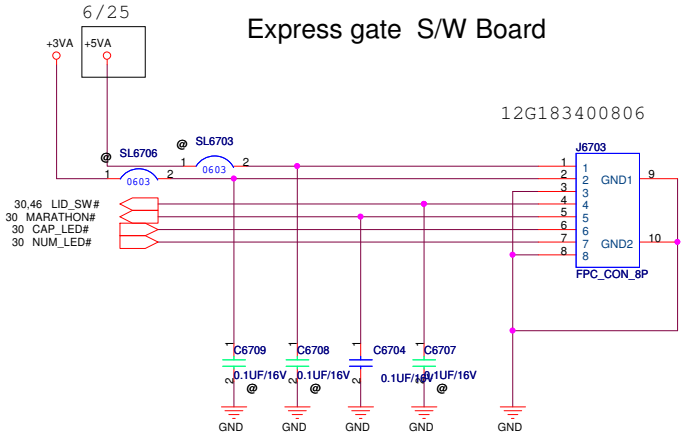
# Camera Module & Mic.



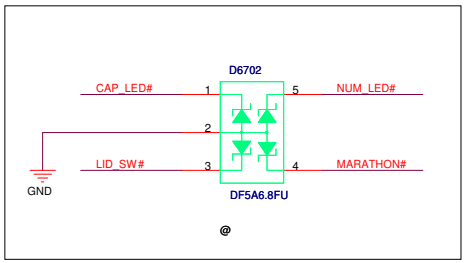

D6701 Close to J6701




# Express gate S/W Board

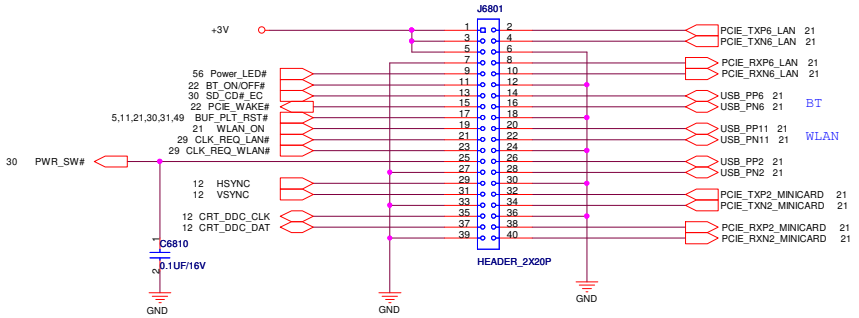


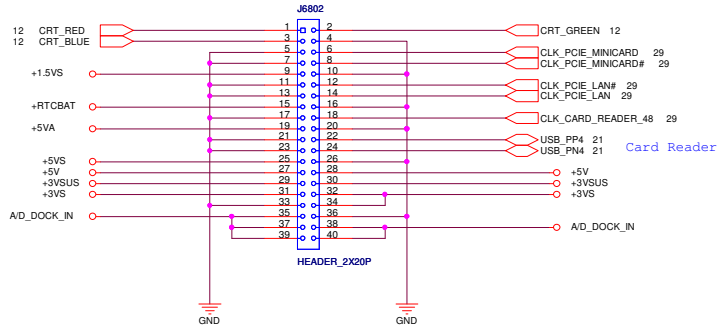

6/22 for ESD




<Variant Name>

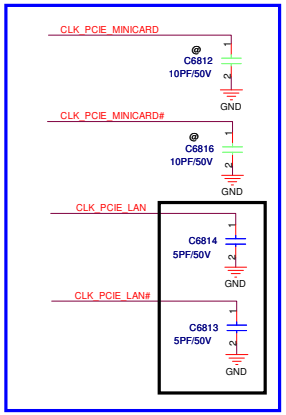
| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : CMO CMOS CAMERA | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 67 of 97 | |



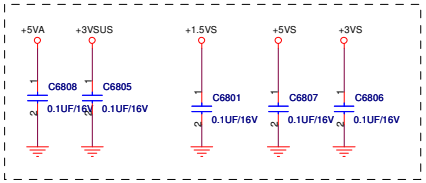




每一根估0.5A,connector spec 1A

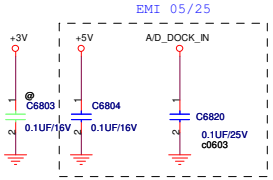
For Clock signal quality




EMI 07/03




EMI 05/25



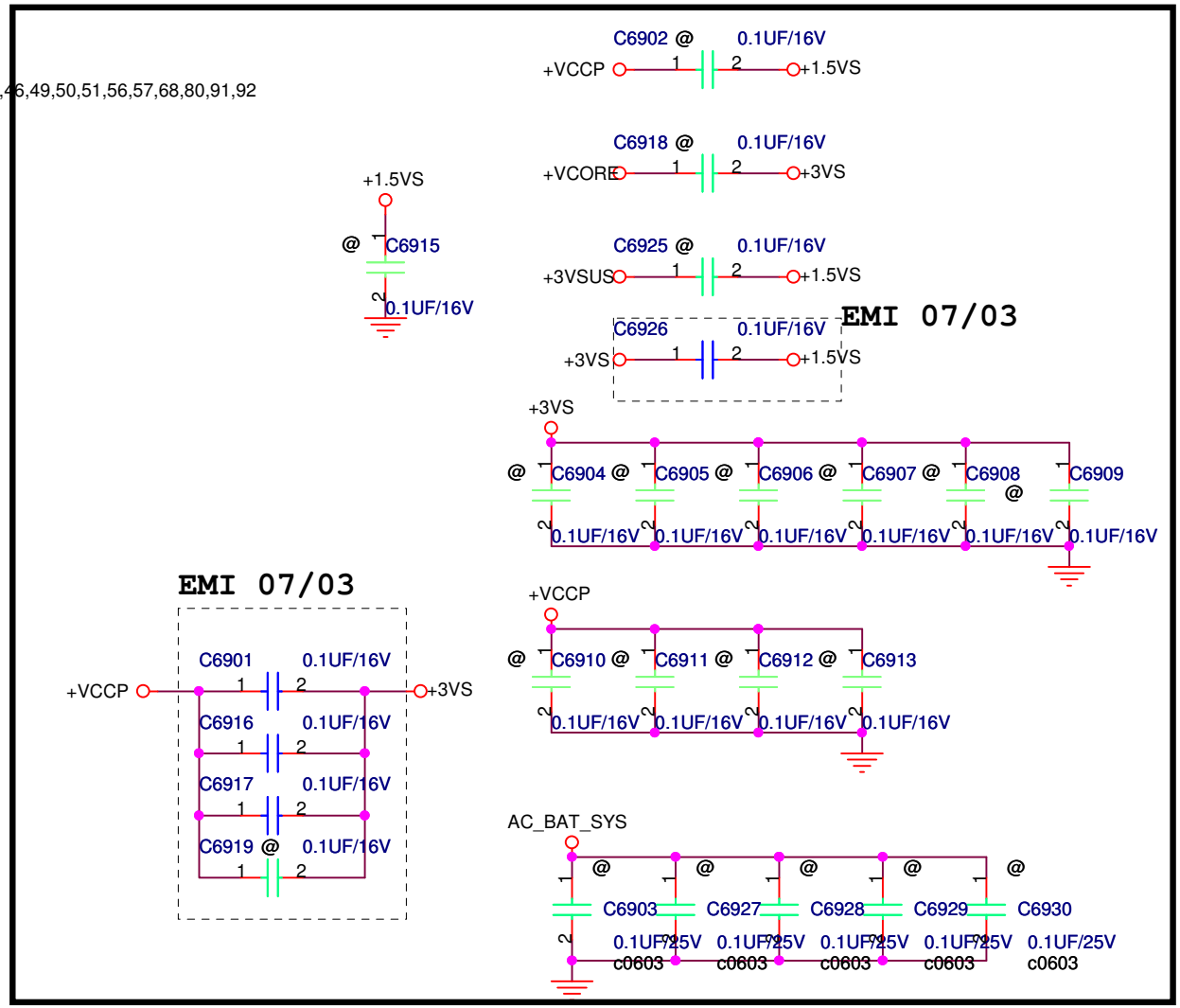

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : B TO B CONN | |
| | Engineer: Jerry Yu | |
| Size: Custom | Project Name: UL20A | Rev: 2.0 |
| Date: Monday, August 03, 2009 | Sheet 68 of 97 | |

# SYSTEM

| | | |
|---|---|---|
| +VCCP | +VCCP | 3,4,5,10,11,12,14,15,20,23,29,57,82 |
| +VCC_GMCH | +VCC_GMCH | 3,4,5,10,11,12,14,15,20,23,29,57,82 |
| +VGFX_CORE | +VGFX_CORE | 3,4,5,10,11,12,14,15,20,23,29,57,82 |
| +3VS | +3VS | 3,7,8,11,12,15,17,21,22,23,29,30,31,36,38,44,46,49,50,51,56,57,68,80,91,92 |
| +VCORE | +VCORE | 4,5,80 |
| +1.5VS | +1.5VS | 4,15,20,23,36,57,68,84 |
| +1.8V | +1.8V | 7,8,9,11,14,15,57,83,84,91 |
| +5V | +5V | 52,57,67,68,91 |
| +5VS | +5VS | 23,36,38,50,51,56,57,68,80,84,91 |
| +3VA | +3VA | 20,30,56,67,81,88 |
| +VCC_RTC | +VCC_RTC | 20,23 |
| +3V | +3V | 46,57,68,91 |
| +3VSUS | +3VSUS | 20,21,22,23,30,57,68,80,81,91,92 |
| +5VSUS | +5VSUS | 23,80,81,82,83,88,91 |
| +3VPLL | +3VPLL | 30,31 |
| +3VACC | +3VACC | 30 |
| +3VA_EC | +3VA_EC | 30,31 |
| +5VS_AMP | +5VS_AMP | 36 |
| +12V | +12V | 91 |
| +12VS | +12VS | 22,46,91 |
| AC_BAT_SYS | AC_BAT_SYS | 46,80,81,82,83,88 |
| +5VA | +5VA | 56,67,68,81 |

## EMI 05/25




<Variant Name>

ASUSTeK COMPUTER INC

Title :

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Monday, August 03, 2009 Sheet 69 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : | |
| | Engineer: Jerry Yu | |
| Size: A | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 70 of 97 | |

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 71 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 72 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 73 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC | Title : | |
| | Engineer: Jerry Yu | |
| Size: A | Project Name: UL20A | Rev: 2.0 |
| Date: Wednesday, July 29, 2009 | Sheet 74 of 97 | |

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 75 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 76 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 77 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 78 of 97

<Variant Name>

Title :

ASUSTeK COMPUTER INC

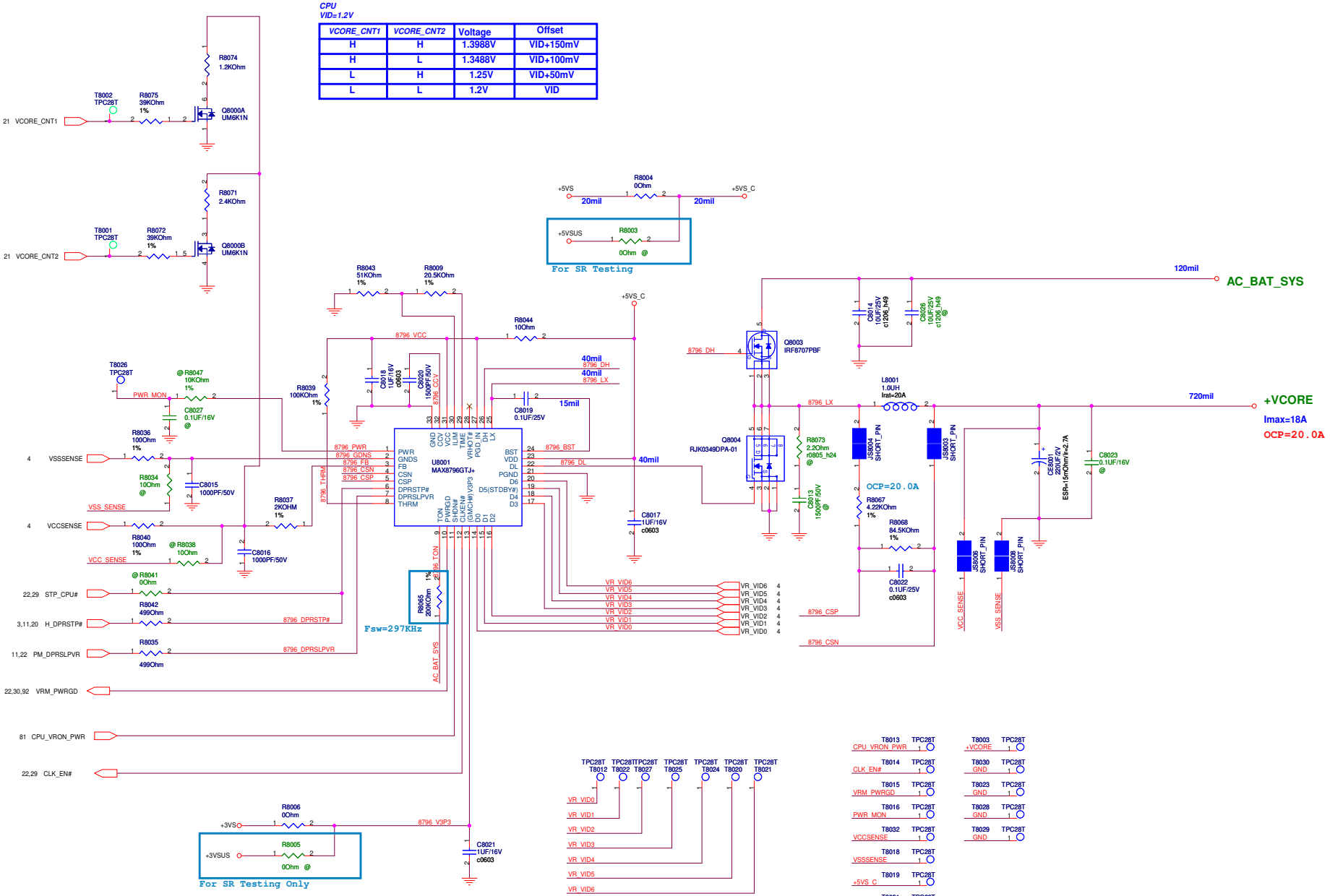
Engineer: Jerry Yu

| Size | Project Name | Rev |
|---|---|---|
| A | UL20A | 2.0 |

Date: Wednesday, July 29, 2009 Sheet 79 of 97

CPU
VID=1.2V

| VCORE_CNT1 | VCORE_CNT2 | Voltage | Offset |
|---|---|---|---|
| H | H | 1.3988V | VID+150mV |
| H | L | 1.3488V | VID+100mV |
| L | H | 1.25V | VID+50mV |
| L | L | 1.2V | VID |




<Variant Name>

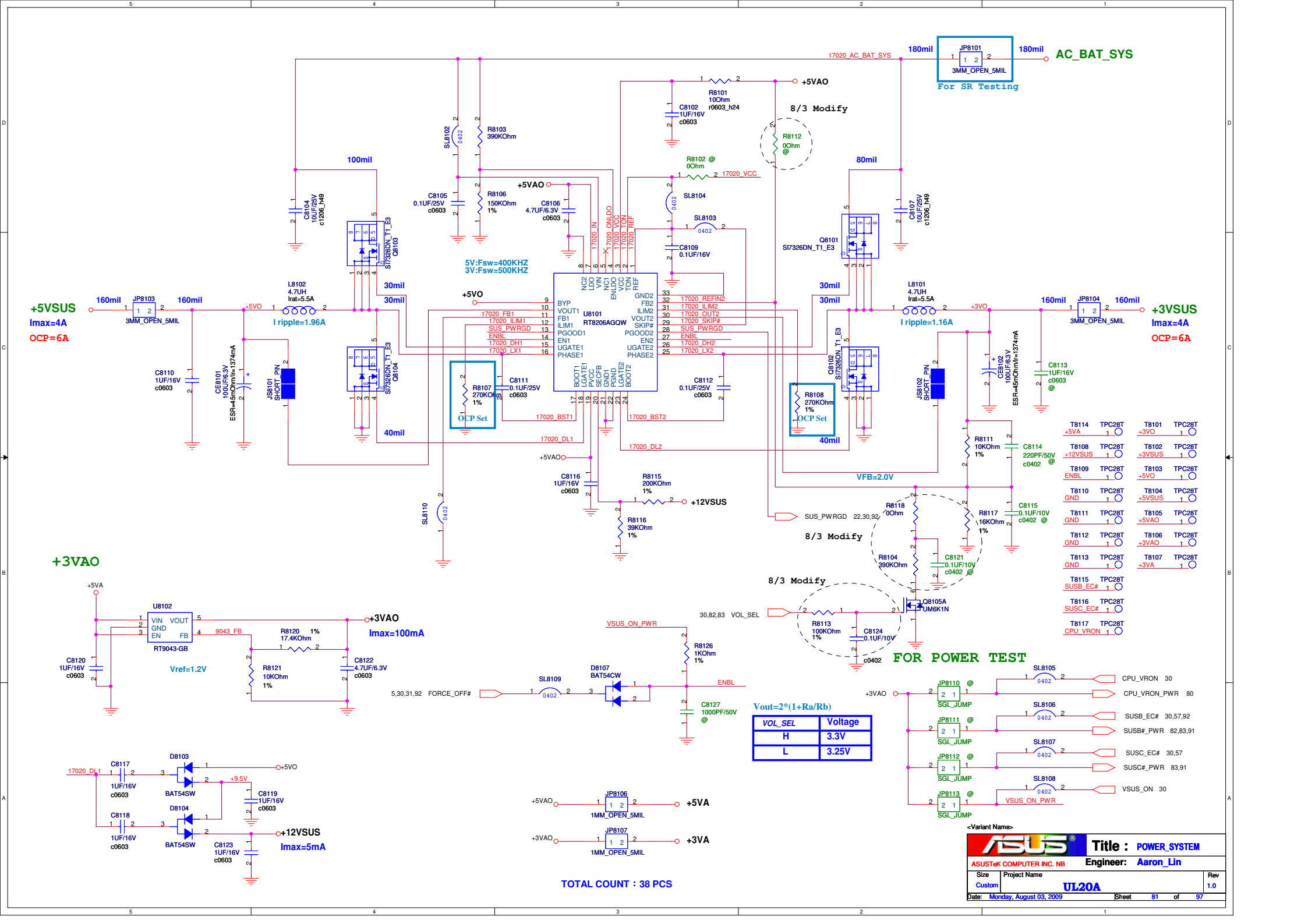
ASUSTeK COMPUTER INC. NB

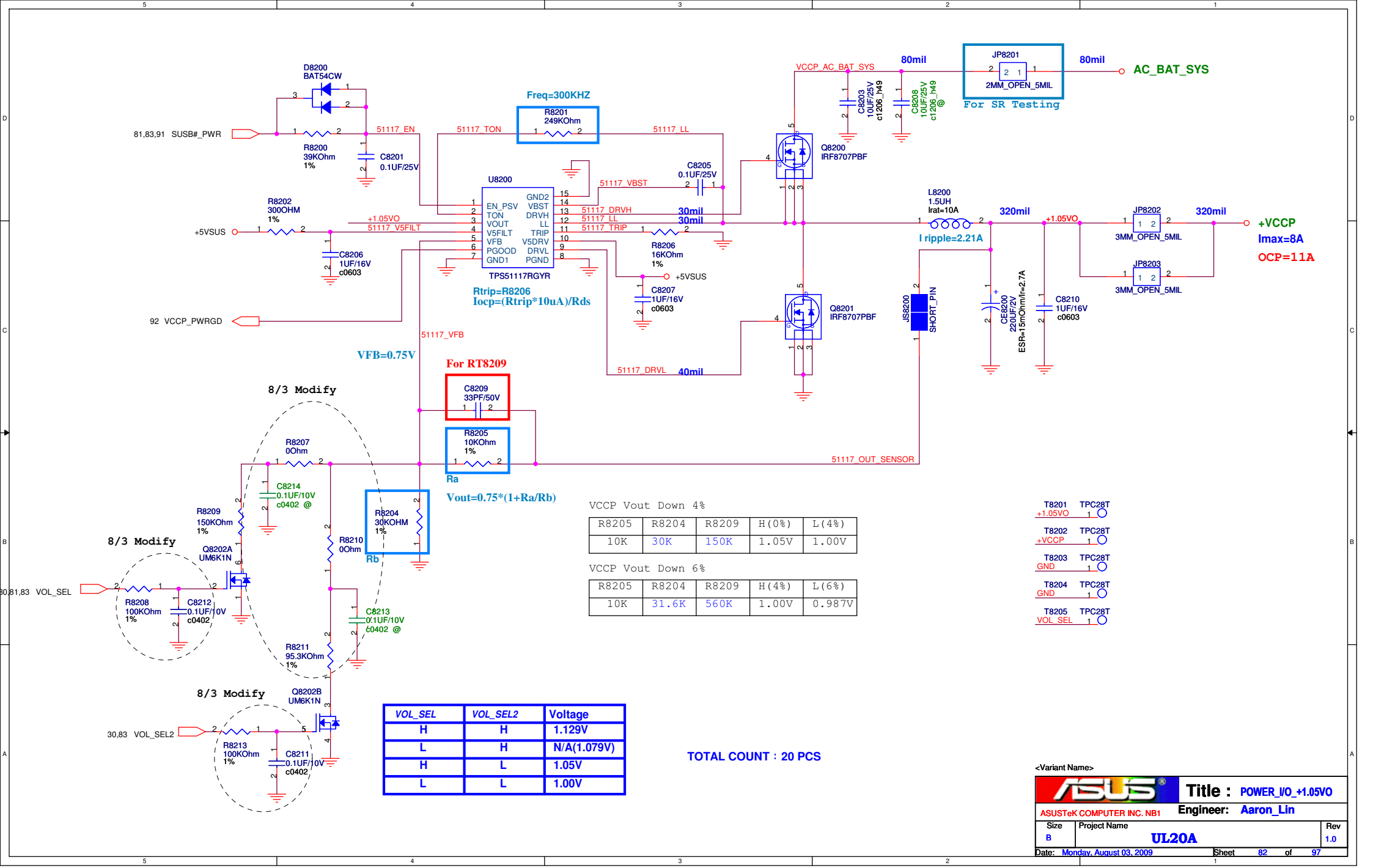
Title : POWER_VCORE

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| C | UL20A | 1.0 |

Date: Monday, August 03, 2009 Sheet 80 of 97


17020_AC_BAT_SYS
180mil
JP8101
3MM_OPEN_5MIL
180mil
AC_BAT_SYS
For SR Testing
+5VAO
R8101
10Ohm
r0603_h24
C8102
1UF/16V
c0603
8/3 Modify
R8112
0Ohm
@
R8102 @
0Ohm
17020_VCC
SL8104
SL8103
C8109
0.1UF/16V
80mil
Q8101
SI7326DN_T1_E3
C8107
10UF/25V
c1206_h49
R8103
390KOhm
SL8102
0402
C8105
0.1UF/25V
c0603
R8106
150KOhm
1%
C8106
4.7UF/6.3V
c0603
C8104
10UF/25V
c1206_h49
100mil
Q8103
SI7326DN_T1_E3
5V:Fsw=400KHZ
3V:Fsw=500KHZ
+5VO
U8101
RT8206AGQW
BYP
VOUT1
FB1
ILIM1
PGOOD1
EN1
UGATE1
PHASE1
BOOT1
LGATE1
PVCC
SECFB
GND1
PGND
LGATE2
BOOT2
NC2
LDO
VIN
NC1
ENLDO
VCC
TON
REF
GND2
FB2
ILIM2
VOUT2
SKIP#
PGOOD2
EN2
UGATE2
PHASE2
17020_FB1
17020_ILIM1
SUS_PWRGD
ENBL
17020_DH1
17020_LX1
17020_REFIN2
17020_ILIM2
17020_OUT2
17020_SKIP#
SUS_PWRGD
ENBL
17020_DH2
17020_LX2
17020_BST1
17020_BST2
17020_DL1
17020_DL2
17020_IN
17020_ONLDO
17020_VCC
17020_TON
17020_REF
+5VSUS
Imax=4A
OCP=6A
160mil
JP8103
3MM_OPEN_5MIL
160mil
+5VO
L8102
4.7UH
Irat=5.5A
I ripple=1.96A
30mil
30mil
40mil
C8110
1UF/16V
c0603
CE8101
100UF/6.3V
ESR=45mOhm/Ir=1374mA
JS8101
SHORT_PIN
R8107
270KOhm
1%
OCP Set
C8111
0.1UF/25V
c0603
C8112
0.1UF/25V
c0603
R8108
270KOhm
1%
OCP Set
40mil
Q8102
SI7326DN_T1_E3
30mil
30mil
L8101
4.7UH
Irat=5.5A
I ripple=1.16A
+3VO
160mil
JP8104
3MM_OPEN_5MIL
160mil
+3VSUS
Imax=4A
OCP=6A
JS8102
SHORT_PIN
CE8102
100UF/6.3V
ESR=45mOhm/Ir=1374mA
C8113
1UF/16V
c0603
@
VFB=2.0V
R8111
10KOhm
1%
C8114
220PF/50V
c0402 @
C8115
0.1UF/10V
c0402 @
R8117
16KOhm
1%
R8118
0Ohm
R8104
390KOhm
C8121
0.1UF/10V
c0402 @
8/3 Modify
8/3 Modify
Q8105A
UM6K1N
R8113
100KOhm
1%
C8124
0.1UF/10V
c0402
30,82,83 VOL_SEL
FOR POWER TEST
C8116
1UF/16V
c0603
R8115
200KOhm
1%
+12VSUS
R8116
39KOhm
1%
SL8110
0402
SUS_PWRGD 22,30,92
+5VAO
+3VAO
+5VA
U8102
RT9043-GB
VIN
VOUT
GND
EN
FB
9043_FB
R8120 1%
17.4KOhm
R8121
10KOhm
1%
C8120
1UF/16V
c0603
C8122
4.7UF/6.3V
c0603
Vref=1.2V
+3VAO
Imax=100mA
VSUS_ON_PWR
R8126
1KOhm
1%
SL8109
0402
D8107
BAT54CW
5,30,31,92 FORCE_OFF#
ENBL
C8127
1000PF/50V
@
Vout=2*(1+Ra/Rb)
VOL_SEL
Voltage
H
3.3V
L
3.25V
D8103
D8104
BAT54SW
C8117
1UF/16V
c0603
C8118
1UF/16V
c0603
C8119
1UF/16V
c0603
C8123
1UF/16V
c0603
+9.5V
+12VSUS
Imax=5mA
JP8106
1MM_OPEN_5MIL
JP8107
1MM_OPEN_5MIL
+5VA
+3VA
JP8110 @
JP8111 @
JP8112 @
JP8113 @
SGL_JUMP
SL8105
SL8106
SL8107
SL8108
CPU_VRON 30
CPU_VRON_PWR 80
SUSB_EC# 30,57,92
SUSB#_PWR 82,83,91
SUSC_EC# 30,57
SUSC#_PWR 83,91
VSUS_ON 30
VSUS_ON_PWR
T8114 +5VA
T8108 +12VSUS
T8109 ENBL
T8110 GND
T8111 GND
T8112 GND
T8113 GND
T8115 SUSB_EC#
T8116 SUSC_EC#
T8117 CPU_VRON
T8101 +3VO
T8102 +3VSUS
T8103 +5VO
T8104 +5VSUS
T8105 +5VAO
T8106 +3VAO
T8107 +3VA
TPC28T
TOTAL COUNT : 38 PCS
<Variant Name>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Aaron_Lin
Size
Custom
Project Name
UL20A
Rev
1.0
Date: Monday, August 03, 2009
Sheet 81 of 97




VCCP Vout Down 4%

| R8205 | R8204 | R8209 | H(0%) | L(4%) |
|---|---|---|---|---|
| 10K | 30K | 150K | 1.05V | 1.00V |

VCCP Vout Down 6%

| R8205 | R8204 | R8209 | H(4%) | L(6%) |
|---|---|---|---|---|
| 10K | 31.6K | 560K | 1.00V | 0.987V |

| VOL_SEL | VOL_SEL2 | Voltage |
|---|---|---|
| H | H | 1.129V |
| L | H | N/A(1.079V) |
| H | L | 1.05V |
| L | L | 1.00V |

TOTAL COUNT : 20 PCS

T8201 TPC28T +1.05VO
T8202 TPC28T +VCCP
T8203 TPC28T GND
T8204 TPC28T GND
T8205 TPC28T VOL_SEL

<Variant Name>

Title : POWER_I/O_+1.05VO

ASUSTeK COMPUTER INC. NB1 Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| B | UL20A | 1.0 |

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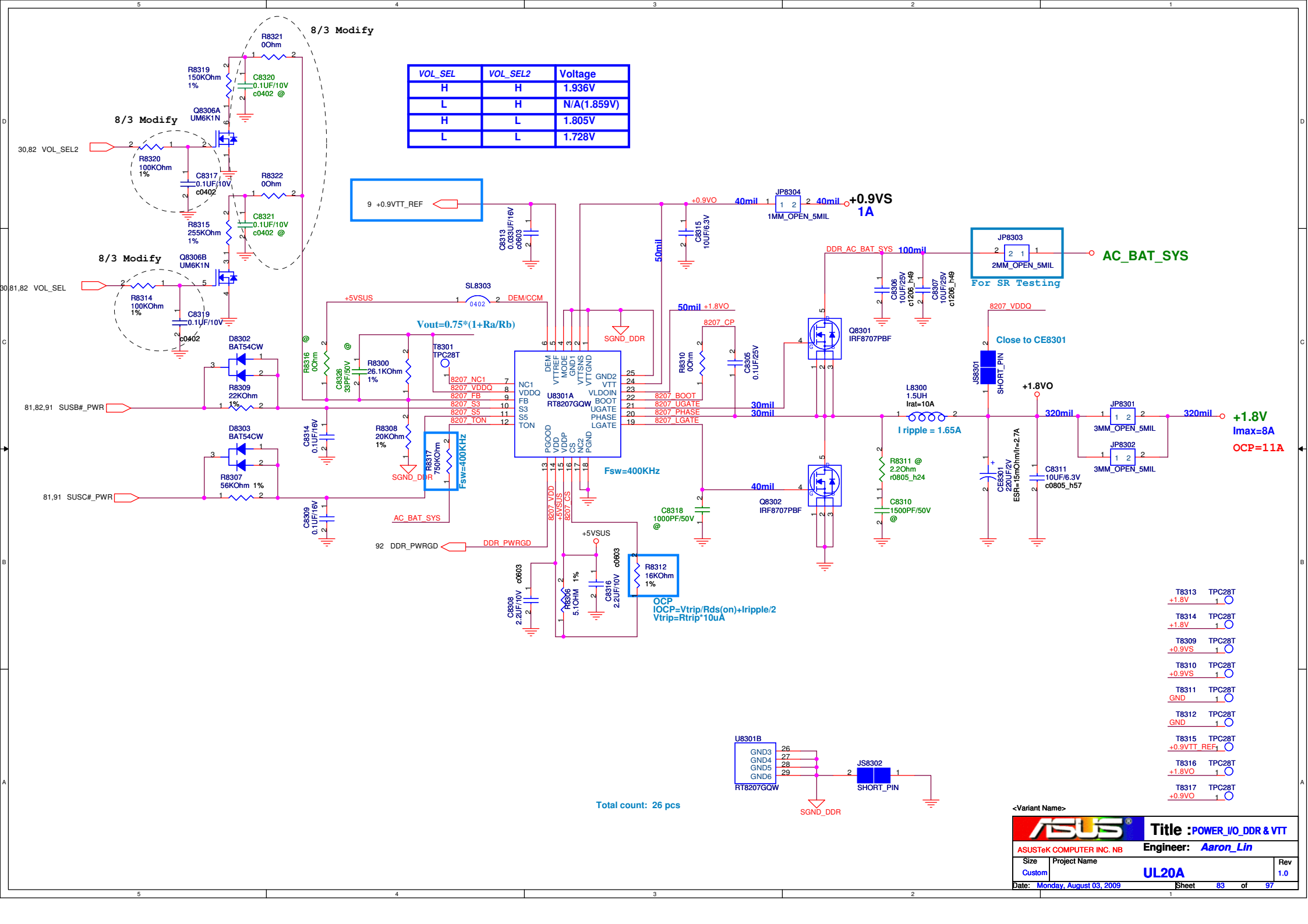
8/3 Modify
R8321 0Ohm
R8319 150KOhm 1%
C8320 0.1UF/10V c0402 @
Q8306A UM6K1N
8/3 Modify
30,82 VOL_SEL2
R8320 100KOhm 1%
C8317 0.1UF/10V c0402
R8322 0Ohm
C8321 0.1UF/10V c0402 @
R8315 255KOhm 1%
8/3 Modify
Q8306B UM6K1N
30,81,82 VOL_SEL
R8314 100KOhm 1%
C8319 0.1UF/10V c0402
VOL_SEL VOL_SEL2 Voltage
H H 1.936V
L H N/A(1.859V)
H L 1.805V
L L 1.728V
9 +0.9VTT_REF
C8313 0.033UF/16V c0603
+0.9VO
40mil
JP8304
40mil
1MM_OPEN_5MIL
+0.9VS
1A
C8315 10UF/6.3V
50mil
DDR_AC_BAT_SYS
100mil
JP8303
2MM_OPEN_5MIL
AC_BAT_SYS
For SR Testing
C8306 10UF/25V c1206_h49
C8307 10UF/25V c1206_h49
SL8303
0402
+5VSUS
DEM/CCM
Vout=0.75*(1+Ra/Rb)
SGND_DDR
50mil +1.8VO
8207_CP
8207_VDDQ
Close to CE8301
R8316 0Ohm @
C8326 33PF/50V @
R8300 26.1KOhm 1%
T8301 TPC28T
D8302 BAT54CW
R8309 22KOhm 1%
81,82,91 SUSB#_PWR
D8303 BAT54CW
R8307 56KOhm 1%
81,91 SUSC#_PWR
8207_NC1
8207_VDDQ
8207_FB
8207_S3
8207_S5
8207_TON
U8301A RT8207GQW
NC1 VDDQ FB S3 S5 TON
DEM VTTREF MODE GND1 VTTSNS VTTGND GND2 VTT VLDOIN BOOT UGATE PHASE LGATE
PGOOD VDD VDDP CS NC2 PGND
8207_BOOT
8207_UGATE
8207_PHASE
8207_LGATE
R8310 0Ohm
C8305 0.1UF/25V
Q8301 IRF8707PBF
30mil
30mil
L8300 1.5UH Irat=10A
I ripple = 1.65A
JS8301 SHORT_PIN
+1.8VO
320mil
JP8301
3MM_OPEN_5MIL
320mil
+1.8V
Imax=8A
OCP=11A
JP8302
3MM_OPEN_5MIL
C8314 0.1UF/16V
R8308 20KOhm 1%
R8317 750KOhm
Fsw=400KHz
Fsw=400KHz
SGND_DDR
AC_BAT_SYS
C8309 0.1UF/16V
92 DDR_PWRGD
DDR_PWRGD
8207_VDD
+5VSUS
8207_CS
+5VSUS
C8318 1000PF/50V @
40mil
Q8302 IRF8707PBF
R8311 @ 2.2Ohm r0805_h24
C8310 1500PF/50V @
CE8301 220UF/2V ESR=15mOhm/Ir=2.7A
C8311 10UF/6.3V c0805_h57
C8808 2.2UF/10V c0603
R8306 5.1OHM 1%
C8316 2.2UF/10V c0603
R8312 16KOhm 1%
OCP
IOCP=Vtrip/Rds(on)+Iripple/2
Vtrip=Rtrip*10uA
U8301B
GND3 GND4 GND5 GND6
RT8207GQW
JS8302
SHORT_PIN
SGND_DDR
Total count: 26 pcs
T8313 TPC28T +1.8V
T8314 TPC28T +1.8V
T8309 TPC28T +0.9VS
T8310 TPC28T +0.9VS
T8311 TPC28T GND
T8312 TPC28T GND
T8315 TPC28T +0.9VTT_REF
T8316 TPC28T +1.8VO
T8317 TPC28T +0.9VO
<Variant Name>
Title :POWER_I/O_DDR & VTT
ASUSTeK COMPUTER INC. NB
Engineer: Aaron_Lin
Size Custom
Project Name UL20A
Rev 1.0
Date: Monday, August 03, 2009
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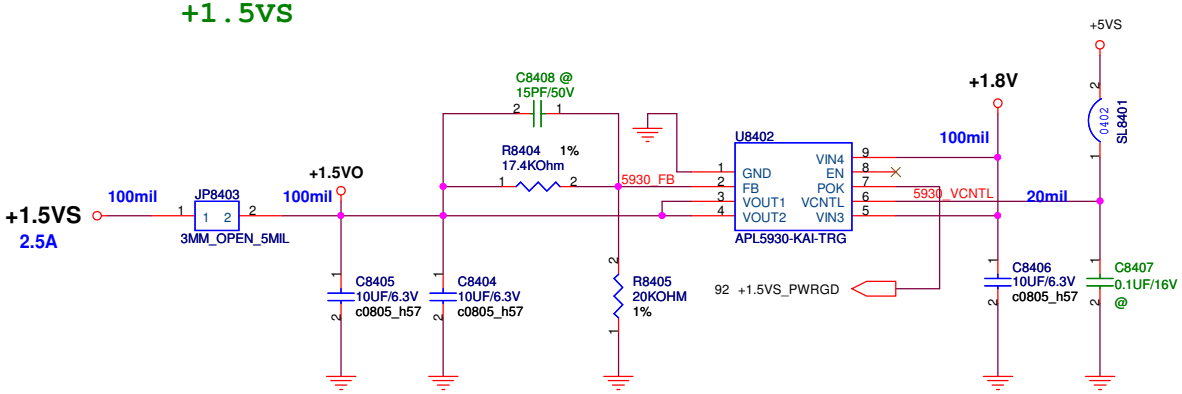
# +1.5VS




T8405 TPC28T +1.5VO 1

T8406 TPC28T +1.5VS 1

T8407 TPC28T GND 1

T8408 TPC28T GND 1

Total count: 6 pcs

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : POWER_I/O_ +1.8VS | |
| | Engineer: Aaron_Lin | |
| Size: B | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 84 of 97 | |

<Variant Name>

Title : +MCP_VDD_CORE

ASUSTeK COMPUTER INC. NB

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 1.0 |

Date: Monday, August 03, 2009 Sheet 85 of 97

<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| B | UL20A | 1.0 |

Date: Monday, August 03, 2009 Sheet 86 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : N/A | |
| | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 87 of 97 | |

# N31 Adaptor：19V/2.1A (40W)

| Adaptor | 65W |
|---|---|
| Power Limit | 63W |
| Total Power | 60W |

| Adaptor | 40W |
|---|---|
| Power Limit | 39W |
| Total Power | 37W |

| Adaptor | 36W |
|---|---|
| Power Limit | 35W |
| Total Power | 34W |

T8802 TPC28T AC_BAT_SYS | T8805 TPC28T AC_BAT_SYS | T8808 TPC28T A/D_DOCK_IN | T8811 TPC28T A/D_DOCK_IN | T8814 TPC28T BAT | T8817 TPC28T BAT | T8820 TPC28T BATSEL_0 | T8824 TPC28T AC_IN_OC# | T8827 TPC28T PWRLIMIT_CRU | T8829 TPC28T GND | T8833 TPC28T CHG_ACIN_OK#

T8803 TPC28T AC_BAT_SYS | T8806 TPC28T AC_BAT_SYS | T8809 TPC28T A/D_DOCK_IN | T8812 TPC28T A/D_DOCK_IN | T8815 TPC28T BAT | T8818 TPC28T BAT | T8821 TPC28T BATSEL_1 | T8825 TPC28T ISET_EC | T8828 TPC28T GND | T8830 TPC28T GND | T8834 TPC28T CHG_VREF

T8804 TPC28T AC_BAT_SYS | T8807 TPC28T AC_BAT_SYS | T8810 TPC28T A/D_DOCK_IN | T8813 TPC28T A/D_DOCK_IN | T8816 TPC28T BAT | T8819 TPC28T BAT | T8822 TPC28T CHG_EN | T8826 TPC28T VSET_EC | T8832 TPC28T GND | T8831 TPC28T GND

A/D_DOCK_IN — 150mil — Q8801 FDS4435BZ — CHG_PATH_19V — C8806 0.1UF/25V c0603 — CHG_SW_GATE — R8803 200KOhm 1% — 150mil — R8801 20mOHM 1% — JS8803 SHORT_PIN — JS8804 SHORT_PIN — 280mil — AC_BAT_SYS

+3VA — RN8802B 100KOHM — RN8802A 100KOHM — RN8801D 100KOHM — RN8801C 100KOHM — RN8801A 100KOHM — RN8801B 100KOHM

30 AC_IN_OC# — Q8809A UM6K1N — Q8809B UM6K1N — 2ACIN_OK_EN — 5CHG_ACIN_OK#

CHG_GATE_A — Q8812A UM6K1N — 2CHG_GATE_B — Q8812B UM6K1N

A/D_DOCK_IN — SL8801 0402 — R8827 130KOhm 1% — CHG_ACIN — ADP>=17.5V — R8823 10KOhm 1% — C8822 0.01UF/25V @ — CHG_ACIN_OK# — SGND_CHG

AC_BAT_SYS — CHG_VCC — C8821 0.01UF/25V @ — SGND_CHG — C8810 1UF/25V c0603 — CLOSE TO VCC(PIN 1)

A/D_DOCK_IN — SL8803 0402 — SEL_EN — R8837 100KOhm 1% — Q8802 FDS4435BZ — 200mil

CHG_VREF — Total Power ADJ — Total Power = 37W

60W: R8822 = 39.2K
37W: R8822 = 75K
34W: R8822 = 84.5K

R8822 75KOhm 1% — R8826 20KOHM 1% — CHG_TOTALPWR — CHG_COMP1_R — R8820 1KOhm 1% — CHG_COMP1 — C8819 0.01UF/25V — SGND_CHG

T8801 TPC28T — 1CHG_-INE1 — CHG_-INE3 — R8816 1KOhm 1% — CHG_-INE3_R — C8816 100PF/50V c0402 — CHG_-INE3_C

CHG_CSIP — CHG_CSIN

U8801A MB39A132 — COMP1 ADJ1 -INE3 AGND ACIN +INC1 -INC1 VCC — -INE1 OUTC1 OUTC2 +INC2 -INC2 ADJ2 COMP2 COMP3 — GND2 CTL2 CB OUT1 LX VB OUT2 PGND CELLS — CHG_CB CHG_HG CHG_LX CHG_VB CHG_LG — BATT ADJ3 CS TE VREF GND1 CTL1 VIN — CHG_BATT CHG_CS CHG_RT

D8801 BAT54CW — CP_BAT — C8802 0.1UF/25V c0603 — R8829 0Ohm — 160mil — C8804 10UF/25V c1206_H49 — C8807 10UF/25V c1206_H49 — AC_BAT_SYS — Q8803 SI7326DN_T1_E3 — JS8807 SHORT_PIN

L8802 6.8UH Irat=3.4A — R8802 20mOHM 1% — 160mil — BAT — 30mil — 30mil — 40mil

Q8813 SI7326DN_T1_E3 — R8828 2.2Ohm r0805_h24 @ — C8827 1500PF/50V @ — JS8801 SHORT_PIN — JS8802 SHORT_PIN — JS8806 SHORT_PIN — C8835 10UF/25V c1206_H49 — C8808 10UF/25V c1206_H49

CHG_CSIP — CHG_CSIN — CHG_BATT

Charge Current ADJ — 30 ISET_EC — R8818 10KOhm 1% — R8819 16.9KOhm 1% — C8820 0.1UF/25V c0603 — C8817 2200PF/50V — CHG_OUTC3 — R8824 10KOhm 1% — CHG_ISET — CHG_COMP2 — CHG_COMP3 — C8815 0.01UF/25V @ — C8814 1000PF/50V — CHG_COMP3_C — R8815 20KOHM 1% — C8818 1UF/16V c0603 — SL8802 0402 — CHG_ENBLE#

| ISET_EC | CHG CURRENT |
|---|---|
| 0.2588V | 0.175A |
| 2.1V | 2.5A |
| 3.3V | 4..0A |

Charge Voltage ADJ — 30 VSET_EC — R8814 0.1% 13.7KOhm nb_r0603_h22 — CHG_VREF — RN8802C 100KOHM — CHG_CELLS — R8813 20KOhm r0603 0.1% — CHG_ADJ3 — C8811 0.1UF/25V c0603 — RN8802D 100KOHM — R8812 10KOhm r0603 0.1% — C8812 0.1UF/16V — R8811 33KOhm 1% — C8813 0.1UF/16V — CELLS_SEL — Q8808A UM6K1N — Q8808B UM6K1N

| VSET_EC | BAT VOLTAGE | CELLS |
|---|---|---|
| 3.0V | 8.4V | 2S |
| 3.0V | 12.6V | 3S |
| 3.145V | 12.9V | 3S |
| 3.0V | 16.8V | 4S |

CHG_EN 30 — BATSEL_0 30 — BATSEL_1 30

Fsw=515KHz

CLOSE TO VIN(PIN 24)

## Power Limit

Power Limit = 39W

+3VA — R8833 100KOhm 1% — R8821 10KOhm 1% — CHG_-INE1 — CHG_V+ — +5VSUS — U8803 LMV321IDBVR — CHG_REFIN — 1.023V — CHG_PWRLIMIT — D8806 1SS355 — PWRLIMIT_CPU 3 — R8834 49.9KOHM 1% — C8826 0.01UF/25V — C8823 0.1UF/25V c0603 — R8832 100KOhm 1% — C8824 1UF/16V c0603 — C8825 0.1UF/25V

63W: R8834 = 102K
39W: R8834 =49.9K
35W: R8834= 39K

U8801B MB39A132 — GND3 GND4 GND5 GND6 — JS8805 @ SHORT_PIN — SGND_CHG

TOTAL COUNT：58 PCS

## Battery Cells

| BATSEL_1 | BATSEL_0 | CELLS |
|---|---|---|
| H | H | 2 CELLS |
| L | H | 2 CELLS |
| H | L | 3 CELLS |
| L | L | 4 CELLS |

Charger IC and EC Code correlation sheet：
Charger MAX8725 => EC CODE：200
Charger MAX17015 => EC CODE：201
Charger MB39A132 => EC CODE：202

ASUSTeK COMPUTER INC. NB3

Title : CHARGER_202

Engineer: Aaron_Lin

Size: Custom | Project Name: UL20A | Rev: 1.0

Date: Monday, August 03, 2009 | Sheet 88 of 97

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : N/A | |
| | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 89 of 97 | |

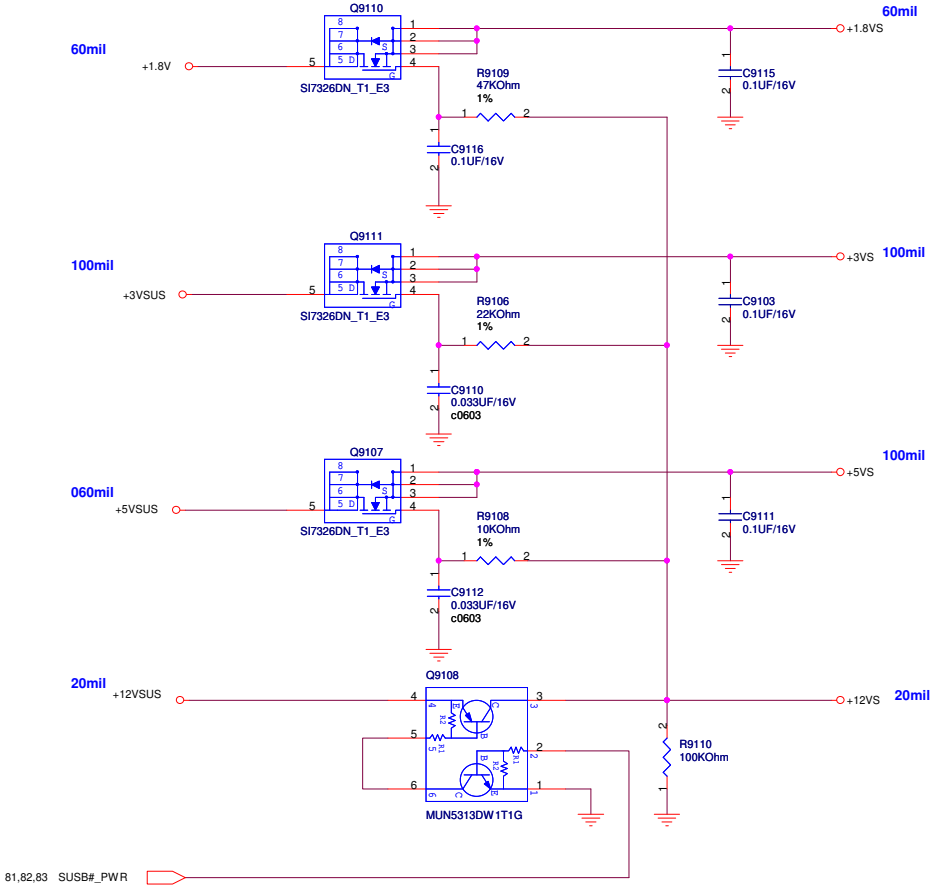
## BATTERY IN DETECT

## ADAPTER IN DETECT

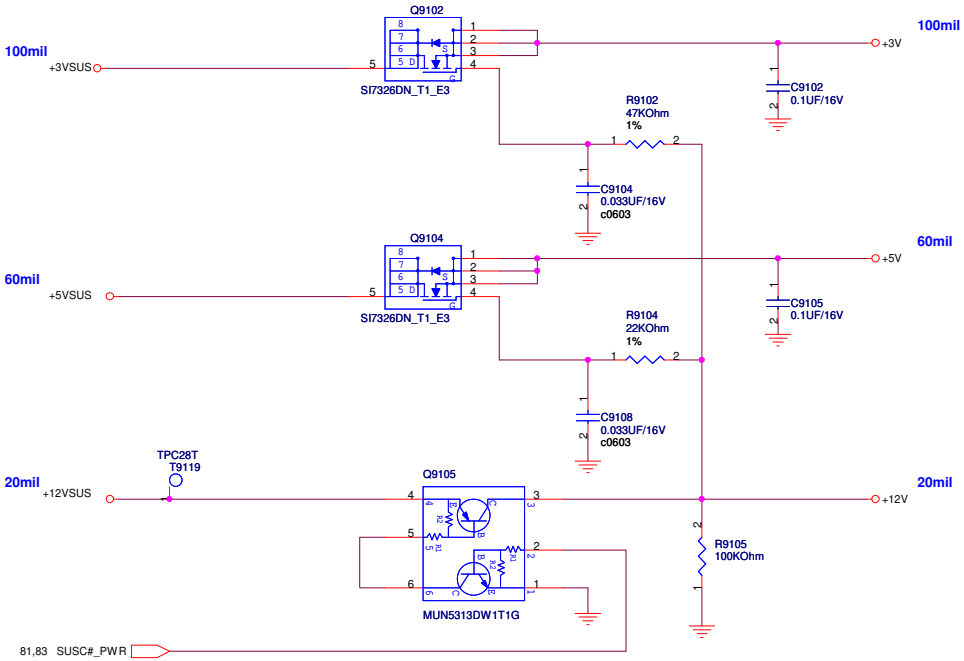
<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : POWER_DETECT | |
| | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 90 of 97 | |

## SUSB#_PWR POWER




## SUSC#_PWR POWER



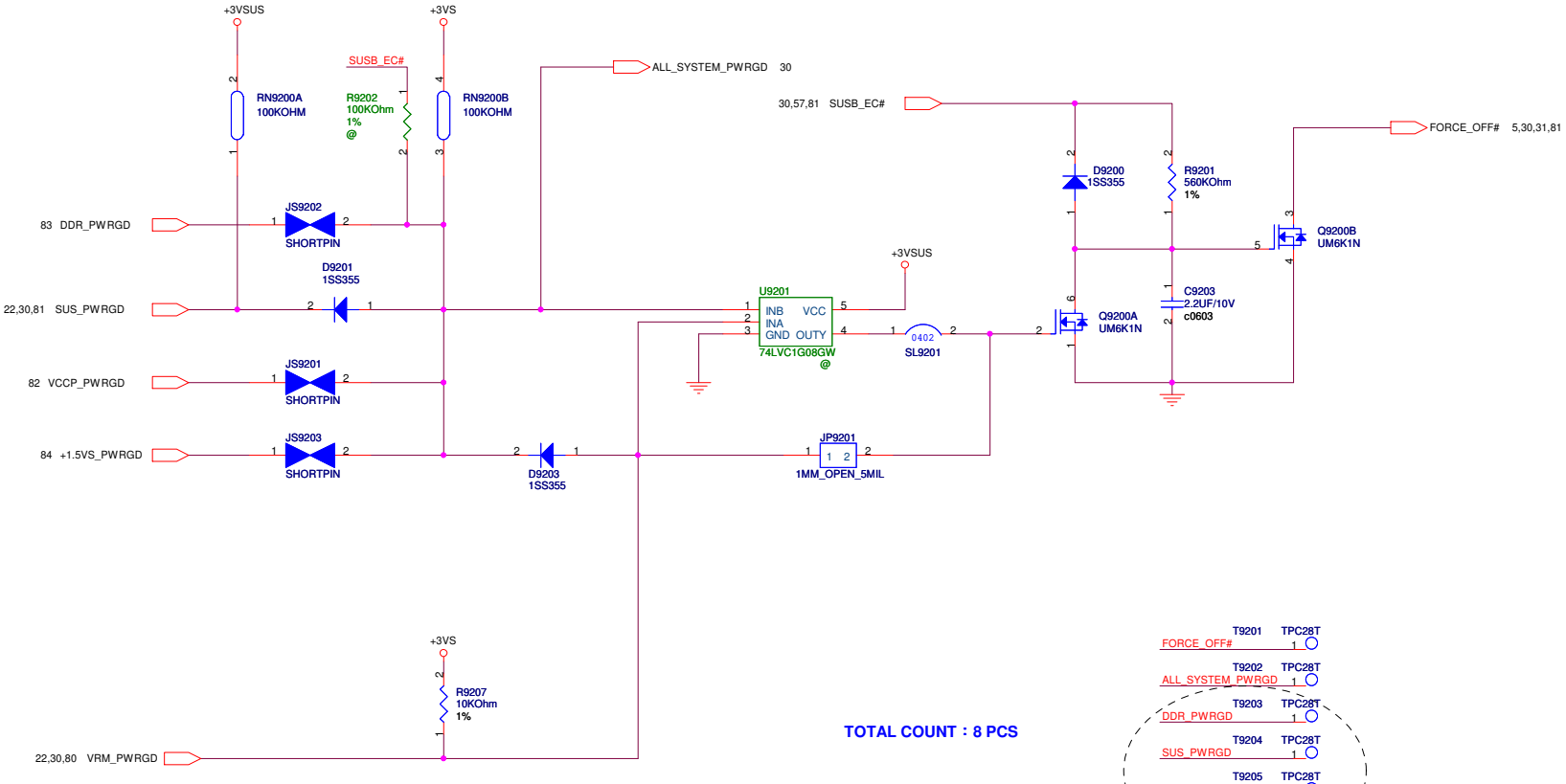

| | | | |
|---|---|---|---|
| T9101 TPC28T +12VSUS 1 | | T9111 TPC28T +3VSUS 1 | |
| T9102 TPC28T +12VS 1 | | T9113 TPC28T +3VS 1 | |
| T9103 TPC28T +12V 1 | | T9115 TPC28T +3V 1 | |
| T9104 TPC28T +5VSUS 1 | | T9120 TPC28T +1.8V 1 | |
| T9106 TPC28T +5VS 1 | | T9121 TPC28T +1.8VS 1 | |
| T9110 TPC28T +5V 1 | | T9123 TPC28T SUSB# PWR 1 | |
| | | T9114 TPC28T SUSC# PWR 1 | |

**TOTAL COUNT : 19 PCS**

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : POWER_LOAD SWITCH | |
| | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 91 of 97 | |

# POWER GOOD DETECTER



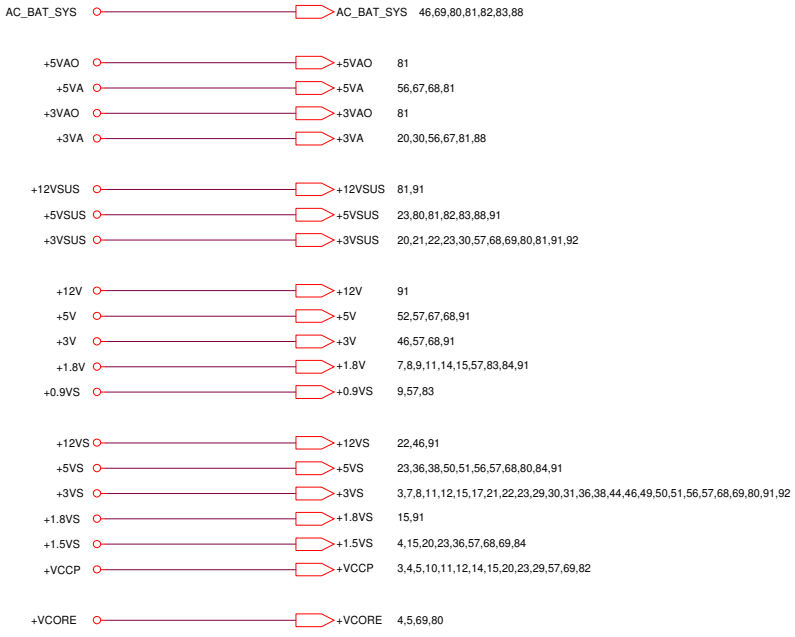

**TOTAL COUNT : 8 PCS**




7/20 Modify

<Variant Name>

| | | |
|---|---|---|
| ASUSTeK COMPUTER INC. NB | Title : POWER_PROTECT | |
| | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 92 of 97 | |




<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 1.0 |

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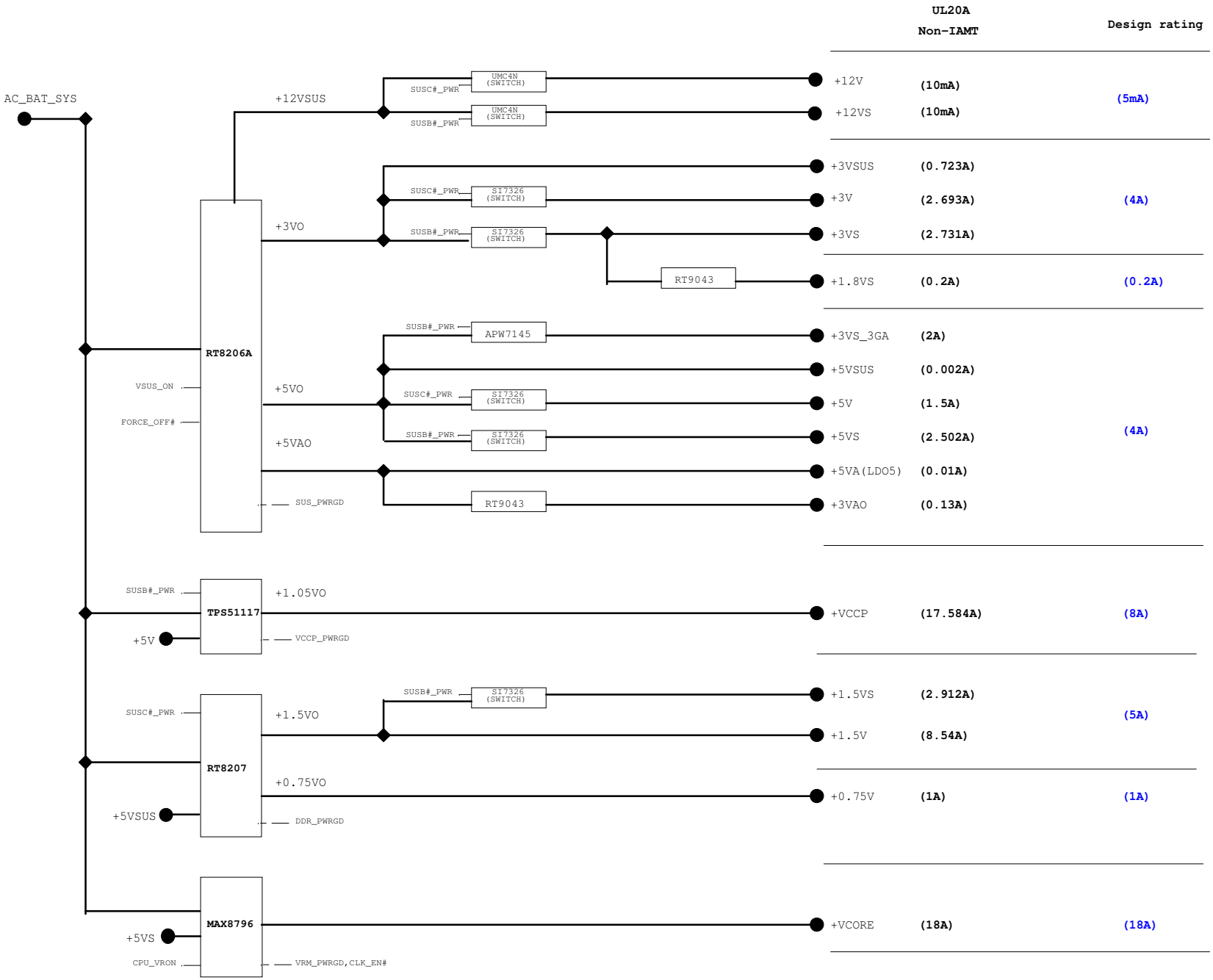


<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 1.0 |

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<Variant Name>

Title : POWER_LED_VCC BOOST

ASUSTeK COMPUTER INC. NB

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 1.0 |

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| Rev | Date | Description |
|---|---|---|
| 1.2a | 2009/06/15 | Item 1 remove CE0502 220uF, C0501,C0503,C0504 10uF/10V (0805)<br>add C0532,C0533,C0534,C0535,C0536,C0501,C0503,C0504 10uF/6.3V(0603)<br>Item 2 connect SW5601,SW5602 pin5&6 to GND<br>Item 3 change TP/DeBUG conn to 12G183401225 ME request<br>Item 4 unmount R3602,R3603,C3603 disable PC beep function |
| 1.2b | 2009/06/22 | Item 1 change D6002 to 07G001023010<br>Item 2 add D5601,D5602,D6702 for ESD<br>Item 3 add R3001 to reduce xtal DL<br>Item 4 EA CLK: RN2905->47ohm, C2932=C2933=C6813=C6814->5pF<br>Item 5 EA CRT: R1208->1k ohm<br>Item 6 change Camera conn to 12G17100006F for cost down<br>Item 7 charge/PWR LED connect from VSUS to VA (P.56),<br>cap/num lock LED connect from VS to VA (P.67) |
| 1.2c | 2009/06/29 | Item 1 update PWR schematic 0701<br>Item 2 change audio 5V LDO 06G029330020 by designIP (P.36)<br>Item 3 restore CE0502 220uF<br>Item 4 EMI: add C5605, C5606 0.1uF on Left/Right<br>Item 5 Thermal: change H6524 to 2.4mm hole |
| 1.2 | 2009/07/03 | Item 1 EMI: mount C6801,C6804,C6805,C6806,C6807,C6808,C6820,C6901,C6916,C6917,<br>C6926,C1431,C3601,C3621 |
| 2.0a | 2009/07/20 | Item 1 change J6802.19 to +5VA |
| 2.0b | 2009/07/28<br>2009/07/30 | Item 1 Thermal: change H6524 to 6.6mm hole<br>Item 2 update PWR circuit: 1.8V low voltage circuit<br>Item 3 add vol_sel2 on EC GPH3<br>Item 4 update PWR circuit: Vcore/Vccp/1.8V/3.3V voltage control<br>Item 5 add BSEL strap Q2902 circuit for over clocking (P.29) |
| 2.0 | 2009/08/03 | Item 1 PWR: update 3.3V/VCCP/DDR power control circuit |

| Rev | Date | Description |
|---|---|---|
| | | |

Title : HISTORY

<OrgName>

Engineer: Aaron_Lin

| Size | Project Name | Rev |
|---|---|---|
| Custom | UL20A | 1.0 |

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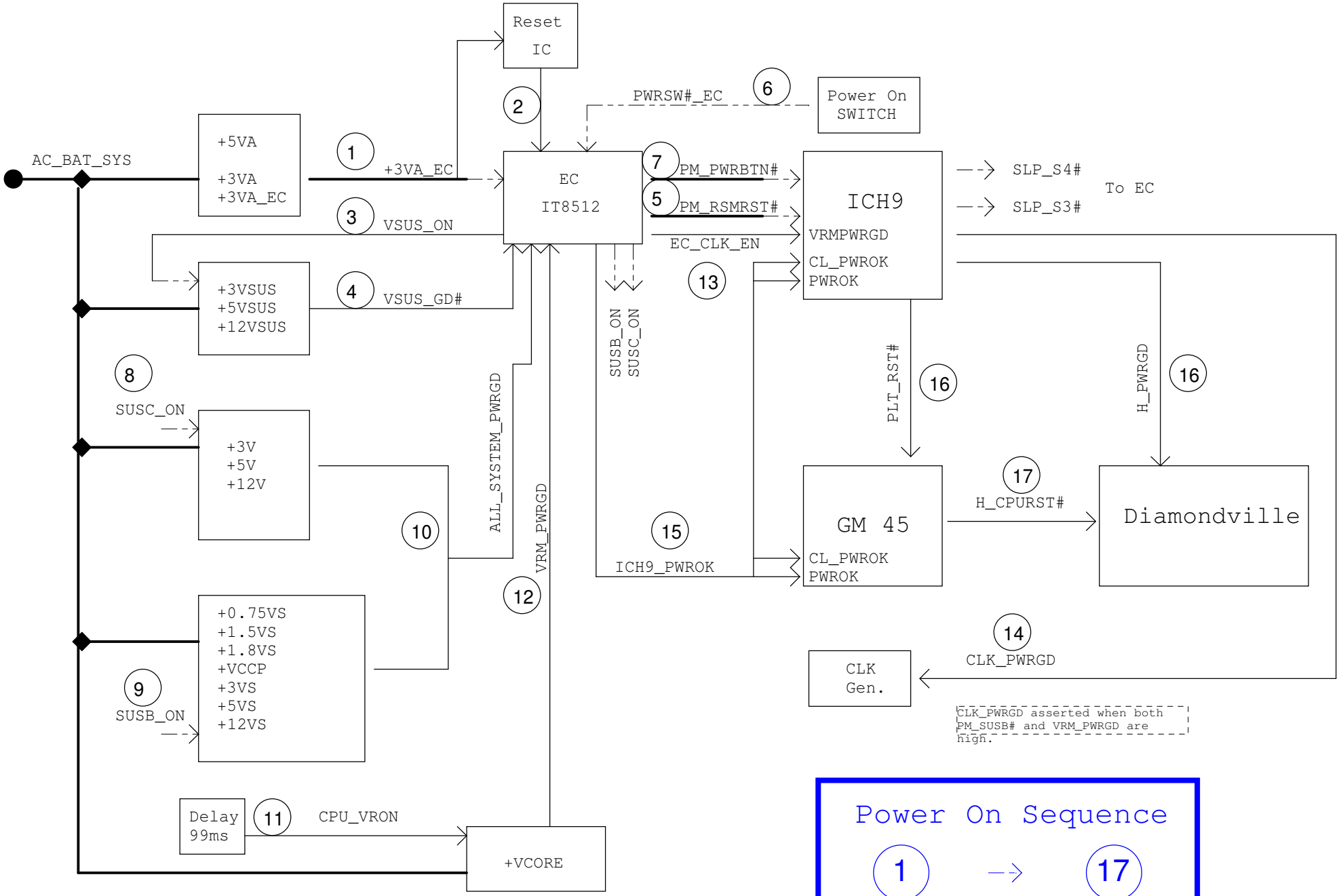


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|---|---|---|
| ASUS | Title : POWER SEQUENCE | |
| <OrgName> | Engineer: Aaron_Lin | |
| Size: Custom | Project Name: UL20A | Rev: 1.0 |
| Date: Monday, August 03, 2009 | Sheet 97 of 97 | |