

V6J SCHEMATIC V2.0

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PROJECT: V6J

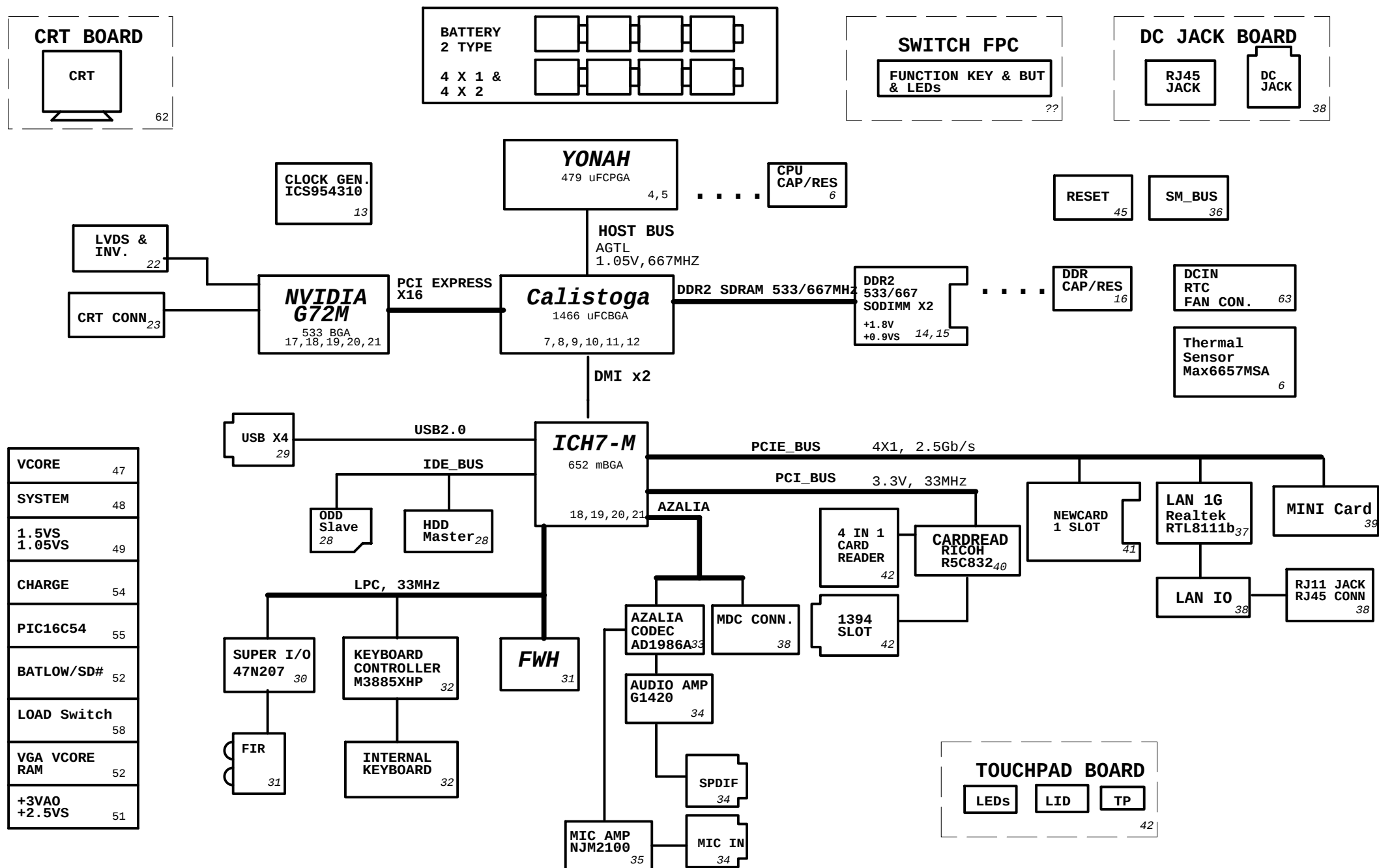
REVISION: 2.0
DATE: Friday, November 25, 2005
SHEET 1 OF 63

DESCRIPTION: Content & History

SCHEMATIC FILE NAME :
RELEASE DATE :

DESIGN ENGINEER : Feng Lin

V6J: YONAH/Calistoga/G72M BLOCK DIAGRAM



PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B, D	
LAN --88E8001	AD16	0	B	
CardBus	AD17	1	B	
1394	AD17	1	A	
4 IN 1		1	C	

AZALIA : PCI_INTB#
USB 0,1 : PCI_INTA#
USB 2,3 : PCI_INTD#
USB 4,5 : PCI_INTC#

CLK = 1101001x (D2)
DDR_SODIMM0 = 1010010x (A4)
DDR_SODIMM1 = 1010000x (A0)
THERMAL = 1001100x (98)
TPM = TBD

SMBUS ADDRESS :

ICH7M_GPIO	Use As	Signal Name	Power
GPI000	GPI	PM_BMBUSY#	+3VS
GPI001	GPI	PCI_REQ#5	+3VS
GPI002	GPI	G72M_THRM#(reserve)	+3VS
GPI0[3:5]	GPI	PCI_INT[E:H]	+3VS
GPI006	GPO	BACK_OFF#	+3VS
GPI007	GPI	WIRELESS_#	+3VS
GPI008	GPI	EXTSMI#_3A	+3VSUS
GPI009	GPI	ACIN_OC_ICH(reserve)	+3VSUS
GPI010	GPI	CHG_FULL_OC	+3VSUS
GPI011	NATIVE	SMBALERT#	+3VSUS
GPI012	GPI	KBCSCI_3	+3VSUS
GPI013	GPI	BATIN_OC#_ICH(reserve)	+3VSUS
GPI014	GPO	LID_ICH#_3A(reserve)	+3VSUS
GPI015	GPI	802_LED#	+3VSUS
GPI016	GPO	PM DPRSLPVR	+3VSUS
GPI017	GPO	PCI_GNT#5	+3VSUS
GPI018	GPO	STP_PCI#	+3VSUS
GPI019	GPI	SATA_DET_#1	+3VSUS
GPI020	GPO	STP_CPU#	+3VS
GPI021	GPI	BATSEL_2P(reserve)	+3VS
GPI022	NATIVE	PCI_REQ#4	+3VS
GPI023	NATIVE	LDRQ1#	+3VS
GPI024	GPO		+3VSUS
GPI025	GPO		+3VSUS
GPI026	GPO	OP_SD#	+3VSUS
GPI027	GPO	WLAN_ON	+3VSUS
GPI028	GPO	PWR_1HZ	+3VSUS
GPI029	NATIVE	USB_OC#45	+3VSUS
GPI030	NATIVE	USB_OC#67	+3VSUS
GPI031	NATIVE	USB_OC#67	+3VSUS
GPI032	GPO	PM_CLKRUN#	+3VSUS
GPI033	GPO	BT_ON	+3VS
GPI034	GPO	FWH_WP#	+3VS
GPI035	GPO		+3VS
GPI036	GPO	BT_LED#	+3VS
GPI037	GPI	PCB_VID0	+3VS
GPI038	GPI	PCB_VID1	+3VS
GPI039	GPI	PCB_VID2	+3VS
GPI0[40:47]	N/A	N/A	N/A
GPI048	NATIVE	FWH_TBL#	+3VS
GPI049	NATIVE	H_PWRGD	+3VS

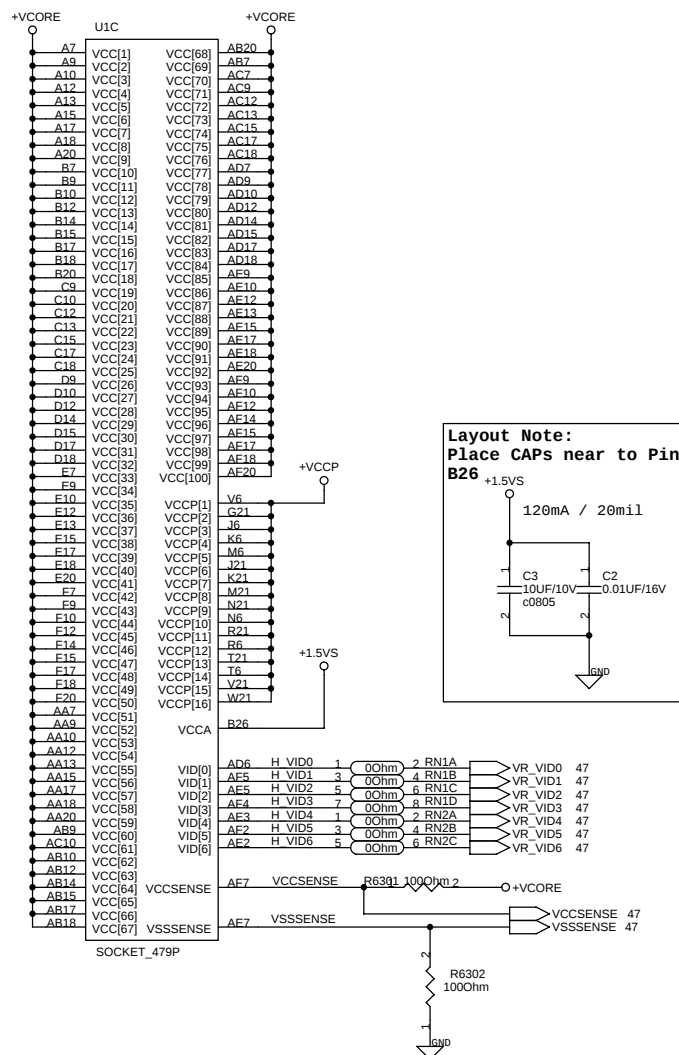
M38857_GPIO	Use As	Signal Name
P20	GPO	KBCRSM
P21	GPI	
P22	GPO	BAT_LEARN
P23	GPO	CPPE_EN
P24	GPO	SET_PCIRSTNS#
P25	GPO	CAP_LED#
P26	GPO	NUM_LED#
P27	GPO	SCROLL_LED#
P40	GPO	KBC_EXTSMI
P41	GPO	PANLOCK_LED#
P42	GPO	WATCHDOG
P43	GPO	CHG_FULL_KBC(reserve)
P44	GPO	KBDCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LOW#_KBC
P51	GPO	
P52	GPI	KBDDT0
P53	GPI	KBDDT1
P54	GPI	LID_ICH#_3A
P55	GPI	BAT_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	BLUETOOTH_#
P61	GPI	INTERNET#
P62	GPI	CPPE#
P63	GPI	
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPI	PANLOCK_#
P67	GPI	
P76	GPI/O	SMD_BAT
P77	GPI/O	SMC_BAT

G72M_GPIO	Use As	Signal Name
GPI000	GPI	
GPI001	GPI	
GPI002	GPO	
GPI003	GPO	LCD_VDD_EN#
GPI004	GPO	LCD_BACKEN
GPI005	GPO	
GPI006	GPO	
GPI007	GPO	
GPI008	GPI	GPI08/ALERT#
GPI009	GPO	
GPI010	GPI0	G72M_GPIO12
GPI011	GPO	
GPI012	GPO	

47N207_GPIO	Use As	Signal Name
GP10	GPI0	
GP11	GPI0	
GP12	GPO	
GP13	GPO	
GP14	GPO	FIR_SEL
GP15	GPI0	PWR_THRO#
GP16	GPI0	ODD_DIS#
GP17	GPI0	RST#_XCARD
GP30	GPI0	PID0
GP31	GPI0	
GP32	GPI0	G72M_THRO#
GP33	GPI0	CPUFAN_SPD_A
GP34	GPI0	SW_RST#
GP35	GPI0	
GP36	GPI0	
GP37	GPI0	

YONAH FSB667			
	LFM	TYP	HFM
CPU State	C4	C3	C0
VCC	1.14V	1.2V	1.356V
ICC	0.9A	7.59A	27A

YONAH FSB667			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
ICCP			2.5A



UID			
A4	VSS[1]	VSS[82]	P6
A8	VSS[2]	VSS[83]	P21
A11	VSS[3]	VSS[84]	P24
A14	VSS[4]	VSS[85]	R5
A16	VSS[5]	VSS[86]	R2
A19	VSS[6]	VSS[87]	R22
A23	VSS[6]	VSS[87]	R25
A26	VSS[7]	VSS[88]	T1
B6	VSS[8]	VSS[89]	T4
B8	VSS[9]	VSS[90]	T3
B9	VSS[10]	VSS[91]	T26
B11	VSS[11]	VSS[92]	T26
B12	VSS[12]	VSS[93]	U3
B16	VSS[13]	VSS[94]	U3
B19	VSS[14]	VSS[95]	U21
B21	VSS[15]	VSS[96]	U24
B24	VSS[16]	VSS[97]	V2
C5	VSS[17]	VSS[98]	V5
C3	VSS[18]	VSS[99]	V22
C11	VSS[19]	VSS[100]	V26
C14	VSS[20]	VSS[101]	W1
C16	VSS[21]	VSS[102]	W3
C19	VSS[22]	VSS[103]	W4
C2	VSS[23]	VSS[104]	W6
C22	VSS[24]	VSS[105]	Y2
C25	VSS[25]	VSS[106]	Y21
D1	VSS[26]	VSS[107]	Y2
D4	VSS[27]	VSS[108]	AA5
D8	VSS[28]	VSS[109]	AA7
D11	VSS[29]	VSS[110]	AA8
D13	VSS[30]	VSS[111]	AA8
D16	VSS[31]	VSS[112]	AA11
D23	VSS[32]	VSS[113]	AA16
D26	VSS[33]	VSS[114]	AA19
E3	VSS[34]	VSS[115]	AA22
E6	VSS[35]	VSS[116]	AA25
F8	VSS[37]	VSS[118]	AB1
F11	VSS[38]	VSS[119]	AB8
F16	VSS[39]	VSS[120]	AB11
F19	VSS[40]	VSS[121]	AB13
F21	VSS[41]	VSS[122]	AB16
F24	VSS[43]	VSS[124]	AB19
E5	VSS[44]	VSS[125]	AB23
F3	VSS[45]	VSS[126]	AB25
F11	VSS[46]	VSS[126]	AC3
F13	VSS[46]	VSS[127]	AC6
F16	VSS[47]	VSS[128]	AC8
F19	VSS[48]	VSS[129]	AC11
F19	VSS[49]	VSS[130]	AC12
F22	VSS[50]	VSS[131]	AC16
F25	VSS[51]	VSS[132]	AC19
G4	VSS[52]	VSS[133]	AC21
G5	VSS[53]	VSS[133]	AC24
G11	VSS[54]	VSS[134]	AD2
G23	VSS[55]	VSS[136]	AD5
G26	VSS[56]	VSS[137]	AD8
H6	VSS[57]	VSS[138]	AD11
H21	VSS[58]	VSS[139]	AD13
H24	VSS[59]	VSS[140]	AD16
J5	VSS[60]	VSS[141]	AD19
J2	VSS[61]	VSS[142]	AD22
J22	VSS[63]	VSS[144]	AD25
K5	VSS[64]	VSS[145]	AE1
K1	VSS[65]	VSS[145]	AE4
K1	VSS[65]	VSS[146]	AE8
K23	VSS[66]	VSS[147]	AE11
K26	VSS[67]	VSS[148]	AE14
K26	VSS[68]	VSS[149]	AE16
L6	VSS[69]	VSS[150]	AE19
L21	VSS[70]	VSS[151]	AE23
L24	VSS[71]	VSS[152]	AE26
M2	VSS[72]	VSS[153]	AF3
M2	VSS[73]	VSS[154]	AF6
M5	VSS[74]	VSS[155]	AF8
M22	VSS[75]	VSS[156]	AF11
M25	VSS[76]	VSS[157]	AF13
N1	VSS[77]	VSS[158]	AF16
N3	VSS[78]	VSS[159]	AF19
N26	VSS[79]	VSS[160]	AF21
P3	VSS[81]	VSS[162]	

MOBILE YONAH VID TABLE

VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage
0 0 0 0 0 0 0	1.5000V	0 1 0 0 0 0 0	1.1000V	1 0 0 0 0 0 0	0.7000V	1 1 0 0 0 0 0	0.3000V
0 0 0 0 0 0 1	1.4875V	0 1 0 0 0 0 1	1.0875V	1 0 0 0 0 0 1	0.6875V	1 1 0 0 0 0 1	0.2875V
0 0 0 0 0 1 0	1.4750V	0 1 0 0 0 1 0	1.0750V	1 0 0 0 0 1 0	0.6750V	1 1 0 0 0 1 0	0.2750V
0 0 0 0 0 1 1	1.4625V	0 1 0 0 0 1 1	1.0625V	1 0 0 0 0 1 1	0.6625V	1 1 0 0 0 1 1	0.2650V
0 0 0 0 1 0 0	1.4500V	0 1 0 0 1 0 0	1.0500V	1 0 0 0 1 0 0	0.6500V	1 1 0 0 1 0 0	0.2500V
0 0 0 0 1 0 1	1.4375V	0 1 0 0 1 0 1	1.0375V	1 0 0 0 1 0 1	0.6375V	1 1 0 0 1 0 1	0.2375V
0 0 0 0 1 1 0	1.4250V	0 1 0 0 1 1 0	1.0250V	1 0 0 0 1 1 0	0.6250V	1 1 0 0 1 1 0	0.2250V
0 0 0 0 1 1 1	1.4125V	0 1 0 0 1 1 1	1.0125V	1 0 0 0 1 1 1	0.6125V	1 1 0 0 1 1 1	0.2125V
0 0 0 1 0 0 0	1.4000V	0 1 0 1 0 0 0	1.0000V	1 0 0 1 0 0 0	0.6000V	1 1 0 1 0 0 0	0.2000V
0 0 0 1 0 0 1	1.3875V	0 1 0 1 0 0 1	0.9875V	1 0 0 1 0 0 1	0.5875V	1 1 0 1 0 0 1	0.1875V
0 0 0 1 0 1 0	1.3750V	0 1 0 1 0 1 0	0.9750V	1 0 0 1 0 1 0	0.5750V	1 1 0 1 0 1 0	0.1750V
0 0 0 1 0 1 1	1.3625V	0 1 0 1 0 1 1	0.9625V	1 0 0 1 0 1 1	0.5625V	1 1 0 1 0 1 1	0.1625V
0 0 0 1 1 0 0	1.3500V	0 1 0 1 1 0 0	0.9500V	1 0 0 1 1 0 0	0.5500V	1 1 0 1 1 0 0	0.1500V
0 0 0 1 1 0 1	1.3375V	0 1 0 1 1 0 1	0.9375V	1 0 0 1 1 0 1	0.5375V	1 1 0 1 1 0 1	0.1375V
0 0 0 1 1 1 0	1.3250V	0 1 0 1 1 1 0	0.9250V	1 0 0 1 1 1 0	0.5250V	1 1 0 1 1 1 0	0.1250V
0 0 0 1 1 1 1	1.3125V	0 1 0 1 1 1 1	0.9125V	1 0 0 1 1 1 1	0.5125V	1 1 0 1 1 1 1	0.1125V
0 0 1 0 0 0 0	1.3000V	0 1 1 0 0 0 0	0.9000V	1 0 1 0 0 0 0	0.5000V	1 1 1 0 0 0 0	0.1000V
0 0 1 0 0 0 1	1.2875V	0 1 1 0 0 0 1	0.8875V	1 0 1 0 0 0 1	0.4875V	1 1 1 0 0 0 1	0.0875V
0 0 1 0 0 1 0	1.2750V	0 1 1 0 0 1 0	0.8750V	1 0 1 0 0 1 0	0.4750V	1 1 1 0 0 1 0	0.0750V
0 0 1 0 0 1 1	1.2625V	0 1 1 0 0 1 1	0.8625V	1 0 1 0 0 1 1	0.4625V	1 1 1 0 0 1 1	0.0625V
0 0 1 0 1 0 0	1.2500V	0 1 1 0 1 0 0	0.8500V	1 0 1 0 1 0 0	0.4500V	1 1 1 0 1 0 0	0.0500V
0 0 1 0 1 0 1	1.2375V	0 1 1 0 1 0 1	0.8375V	1 0 1 0 1 0 1	0.4375V	1 1 1 0 1 0 1	0.0375V
0 0 1 0 1 1 0	1.2250V	0 1 1 0 1 1 0	0.8250V	1 0 1 0 1 1 0	0.4250V	1 1 1 0 1 1 0	0.0250V
0 0 1 0 1 1 1	1.2125V	0 1 1 0 1 1 1	0.8125V	1 0 1 0 1 1 1	0.4125V	1 1 1 0 1 1 1	0.0125V
0 0 1 1 0 0 0	1.2000V	0 1 1 1 0 0 0	0.8000V	1 0 1 1 0 0 0	0.4000V	1 1 1 1 0 0 0	0.0000V
0 0 1 1 0 0 1	1.1875V	0 1 1 1 0 0 1	0.7875V	1 0 1 1 0 0 1	0.3875V	1 1 1 1 0 0 1	0.0000V
0 0 1 1 0 1 0	1.1750V	0 1 1 1 0 1 0	0.7750V	1 0 1 1 0 1 0	0.3750V	1 1 1 1 0 1 0	0.0000V
0 0 1 1 0 1 1	1.1625V	0 1 1 1 0 1 1	0.7625V	1 0 1 1 0 1 1	0.3625V	1 1 1 1 0 1 1	0.0000V
0 0 1 1 1 0 0	1.1500V	0 1 1 1 1 0 0	0.7500V	1 0 1 1 1 0 0	0.3500V	1 1 1 1 1 0 0	0.0000V
0 0 1 1 1 0 1	1.1375V	0 1 1 1 1 0 1	0.7375V	1 0 1 1 1 0 1	0.3375V	1 1 1 1 1 0 1	0.0000V
0 0 1 1 1 1 0	1.1250V	0 1 1 1 1 1 0	0.7250V	1 0 1 1 1 1 0	0.3250V	1 1 1 1 1 1 0	0.0000V
0 0 1 1 1 1 1	1.1125V	0 1 1 1 1 1 1	0.7125V	1 0 1 1 1 1 1	0.3125V	1 1 1 1 1 1 1	0.0000V

YONAH VID TABLE

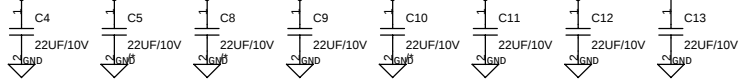
YONAH VID TABLE							
CPU FREQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.8G	C3/C4
2.13G/B1	1.372V					0.988V	0.726V
2.0G/B1	1.356V					0.988V	0.726V
1.87G/B1	1.356V					0.988V	0.726V
1.73G/B1	1.356V					0.988V	0.726V
1.6G/B1	1.356V					0.988V	0.726V
1.6G/A2	1.388V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V

Layout Note :
All of VCore Decoupling Caps
Place these on bottom side of PCB.

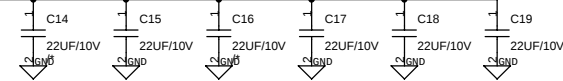
Place these caps on North of PCB bottom



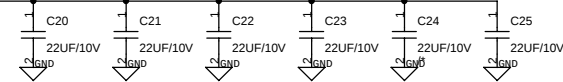
Place these caps on North of PCB bottom



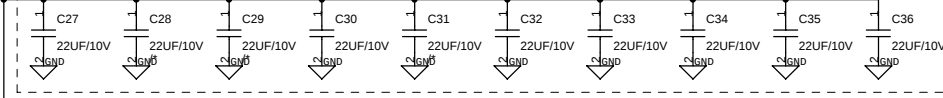
Place these caps on North of PCB bottom



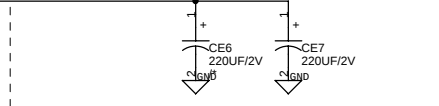
Place these caps on South of PCB bottom



Place these caps on South of PCB bottom

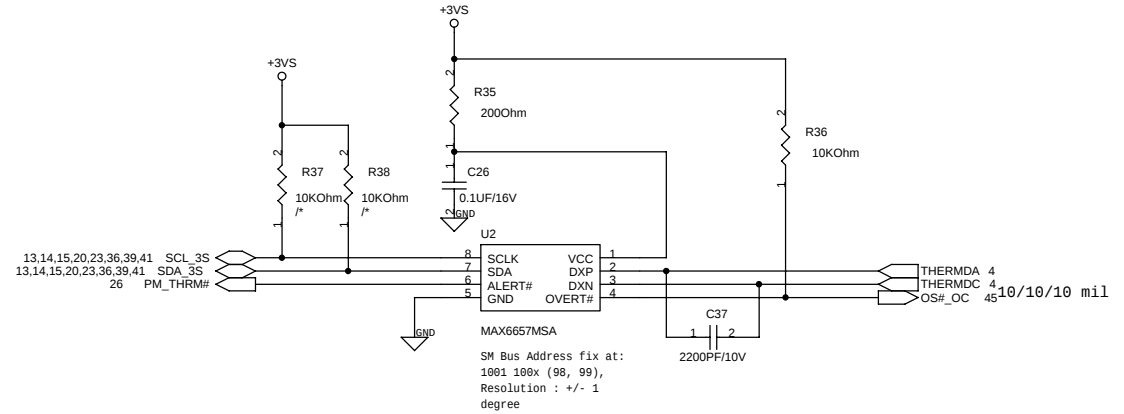


Place these caps on South of PCB bottom

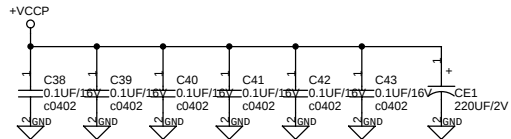


VCore	22uF/6.3V	* 20
	330uF/2V	* 6
VCCP	0.1uF	* 5 for CPU
	220uF	* 1 for CPU
	220uF	* 1 for Calistoga
	4.7uF	* 1 for Calistoga
	2.2uF	* 1 for Calistoga
	0.47uF	* 1 for Calistoga
	0.22uF	* 1 for Calistoga

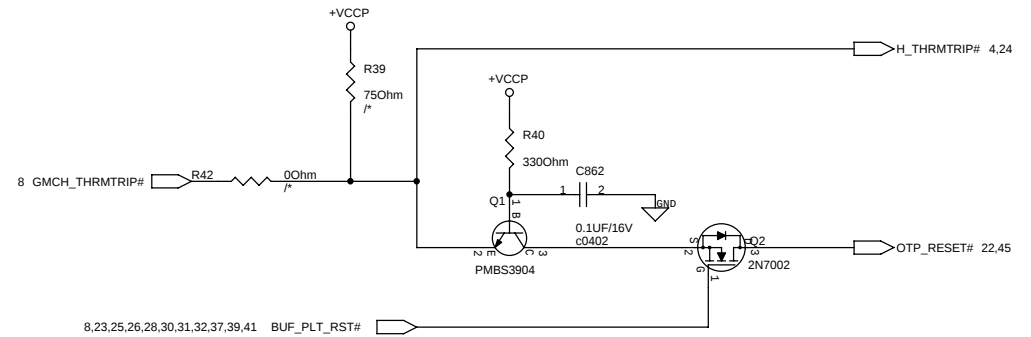
Decoupling guide from INTEL



THERMAL SENSOR



Layout Note :
+V1.05S (VCCP) Decoupling Capacitor
(Place near CPU)



PROJECT: V6J

REVISION

2.0

DATE: Friday, November 25, 2005

SHEET 6 OF 63

DESCRIPTION:

Caps & THERMAL & ITP

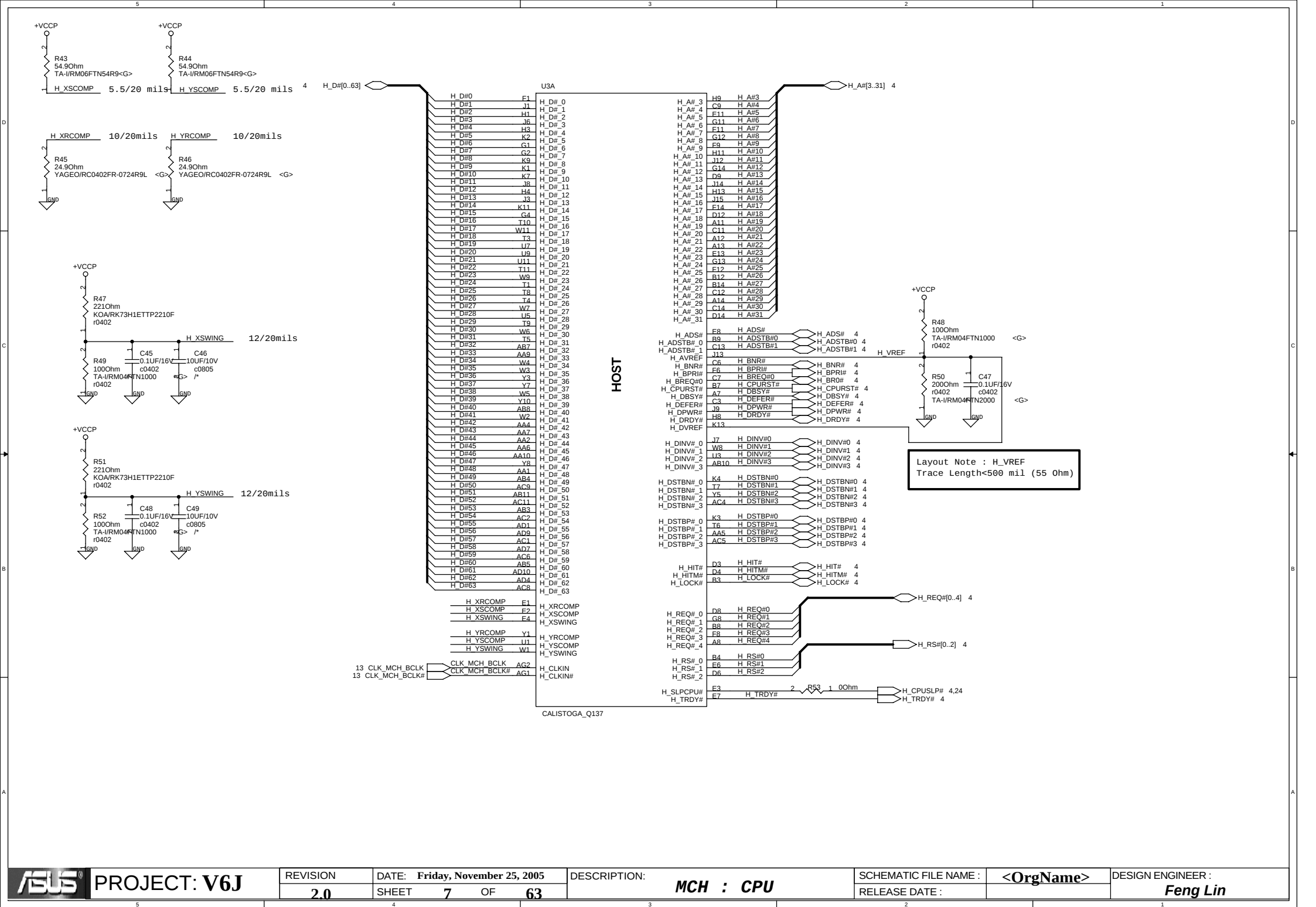
SCHEMATIC FILE NAME :

<OrgName>

DESIGN ENGINEER :

Feng Lin

RELEASE DATE :



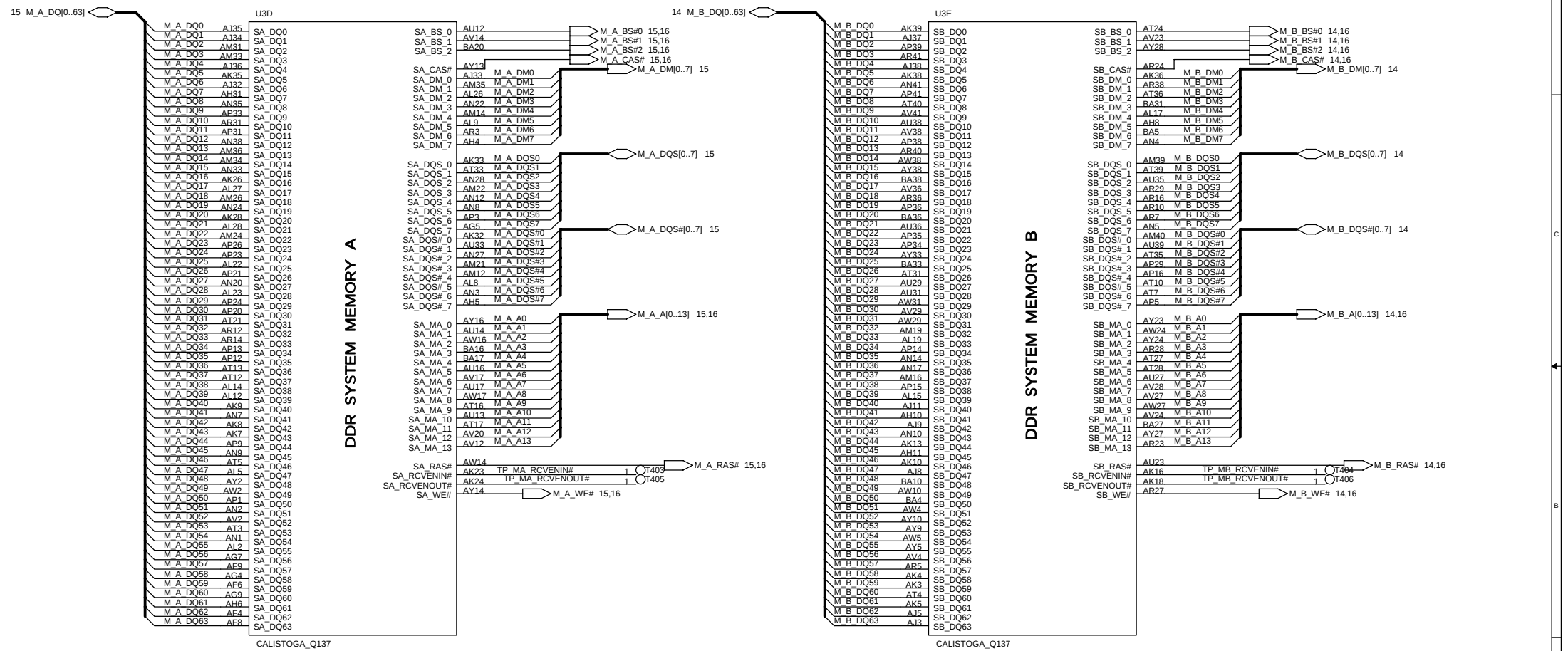
PROJECT: V6J

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DATE: Friday, November 25, 2005
SHEET: 7 OF 63

DESCRIPTION: MCH : CPU

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

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NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

1.5VS

R69 00hms

1.5VS_DPLL A

R70 00hms

1.5VS_DPLL B

L1 120Ohm/100Mhz I0603

L3 120Ohm/100Mhz I0603

L4 90nH

C87 0.1UF/16V c0402

C84 22UF/10V

C89 0.1UF/16V c0402

C85 22UF/10V

C91 0.1UF/16V c0402

C86 22UF/10V

1.5VS_HPLL

1.5VS_MPLL

1.5VS_PCIE

CE8 220UF/2V

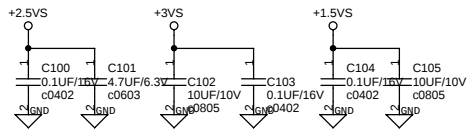
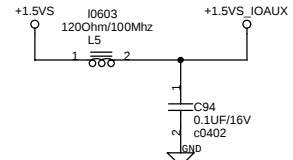
C92 10UF/10V c0805

C93 10UF/10V c0805

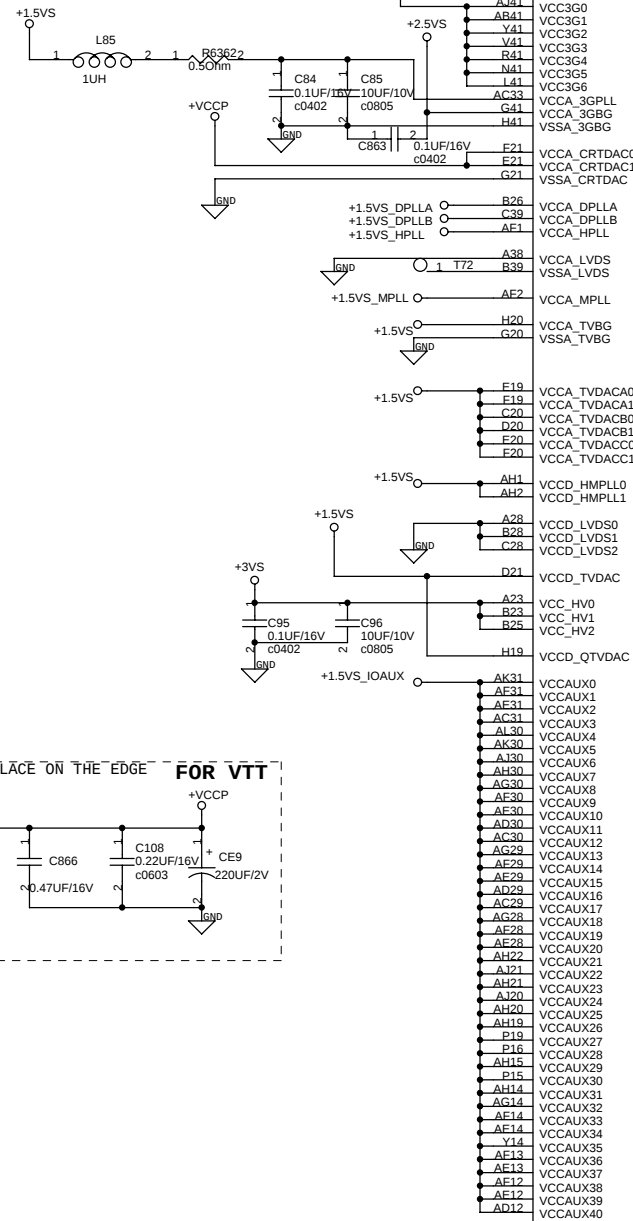
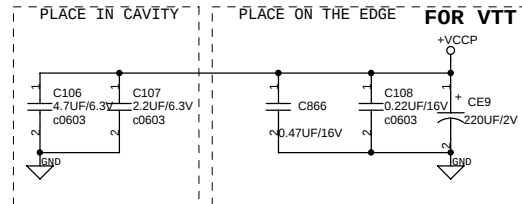
OLD: 09G028901110IN

NEW: 09G028901110

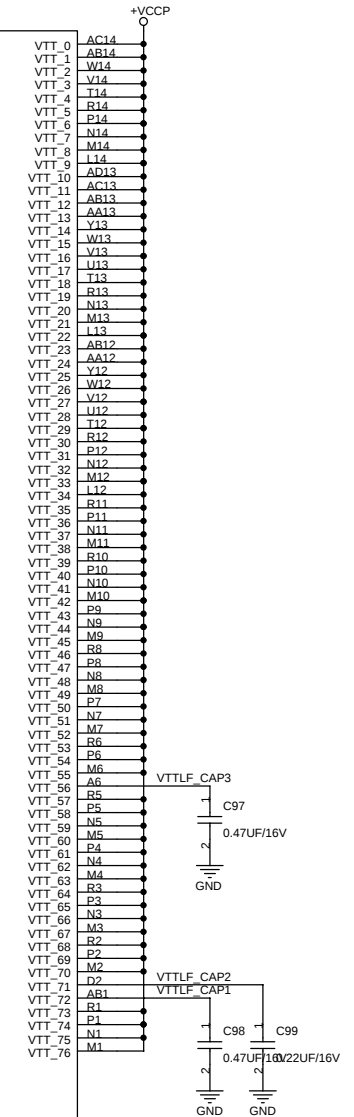
OLD: 09G028901110IN
NEW: 09G028901110



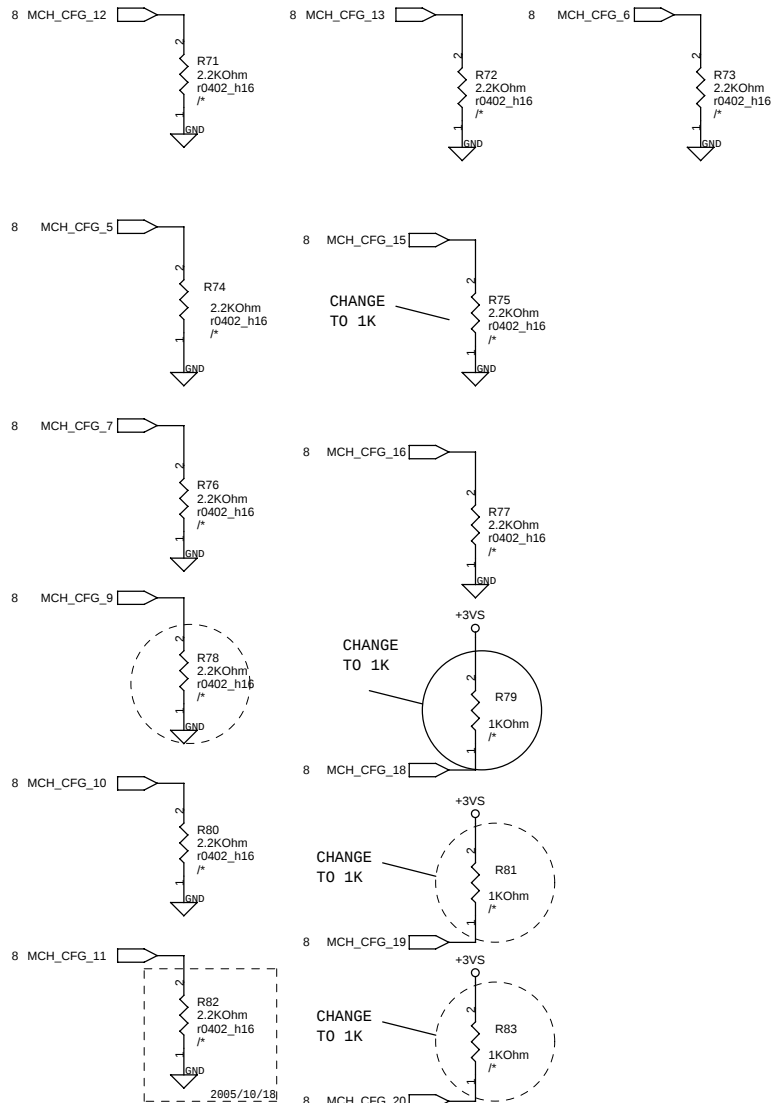
NOTE: 0.1UF CAPS USED IN
+1.5VS, +3.3VS
+2.5VS should be placed within
200 mils of edge.



POWER



CALISTOGA_Q137



Signal Name	Configuration	Notes
CFG[2:0]	011= 667 FSB 001= 533 FSB	Selection the FSB frequency
CFG5	0= DMIX2 1= DMIX4	Selection between DMIX2 and DMIX4
CFG7	0= Reserved 1= Mobil Yonah	Control the target processor
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG[13:12]	01= XOR 10= Z 11= Normal Operation	
CFG16	0= Dynamic ODT DIS 1= Dynamic ODT EN	Control FSB Dynamic ODT
CFG18	0= 1.05V 1= 1.5V	Control GMCH Vcore level
CFG19	0= Normal Operation 1= DMI Lane Revesal EN	
SDVOCTRL_DATA	0= No SDVO device 1= SDVO device present	
Intel Demo Circuit		
CFG6	0= Moby Dick 1= Calistoga	
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG11	0= Reserved 1= 8x Enable	PSB 4x CLK Enable
CFG20	0= Only SDVO or PCIE x1 (Default) 1= SDVO and PCIE x1 are operating	
CFG[2..0] need external pullup resistors. CFG[17..3] have internal pullup resistors. CFG[19..18] have internal pulldown resistors. SDVOCTRL_DATA has internal pulldown resistors.		



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DESCRIPTION:

MCH: Strapping

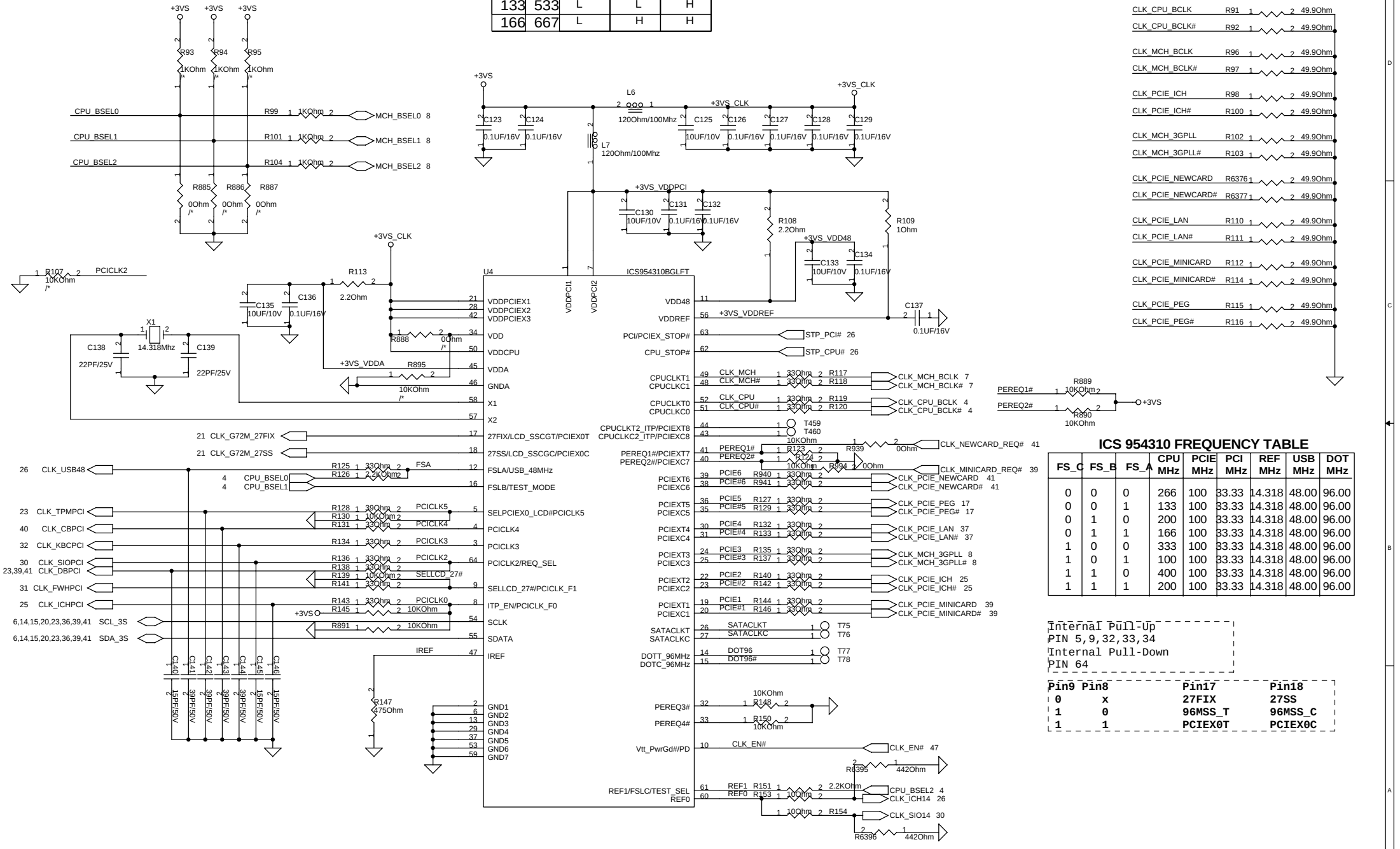
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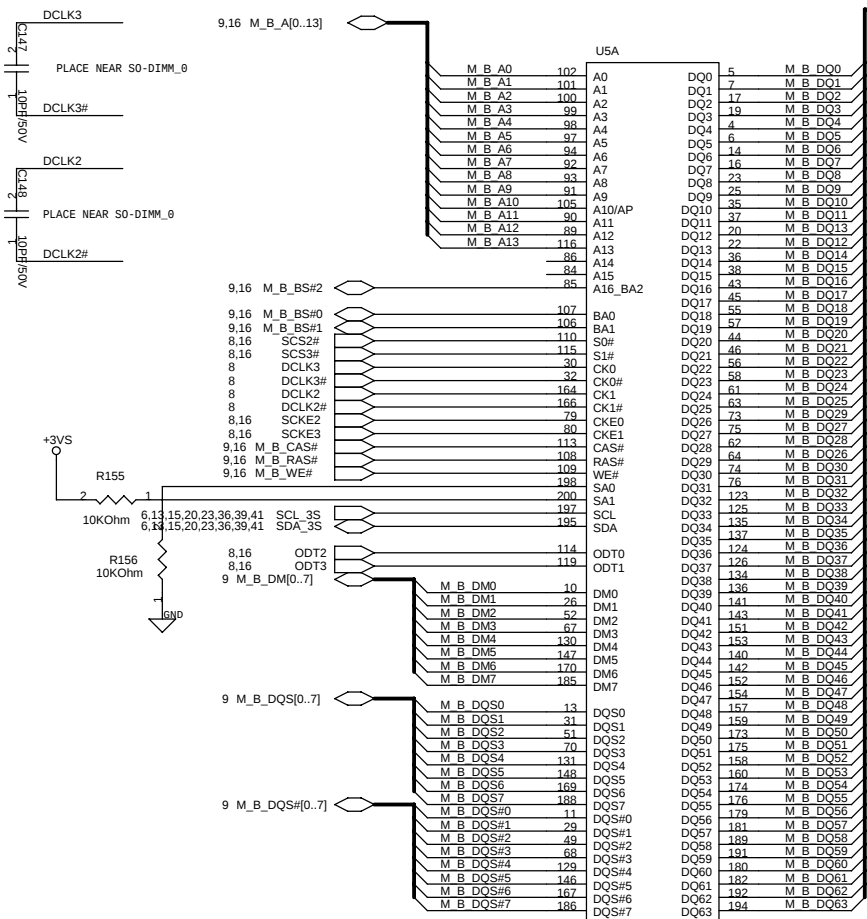
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DESIGN ENGINEER :

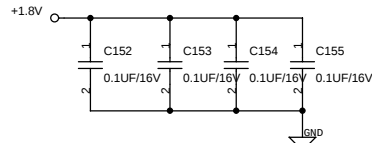
Feng Lin

RELEASE DATE :

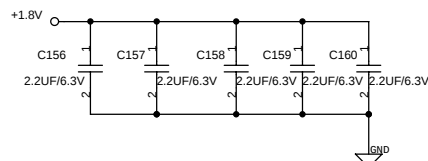




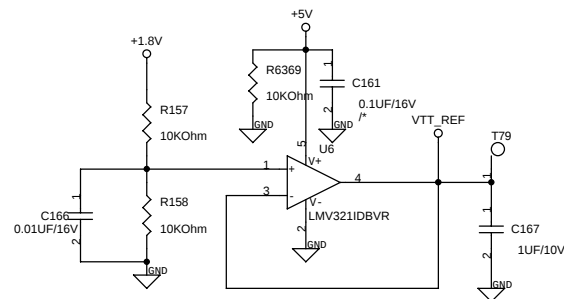
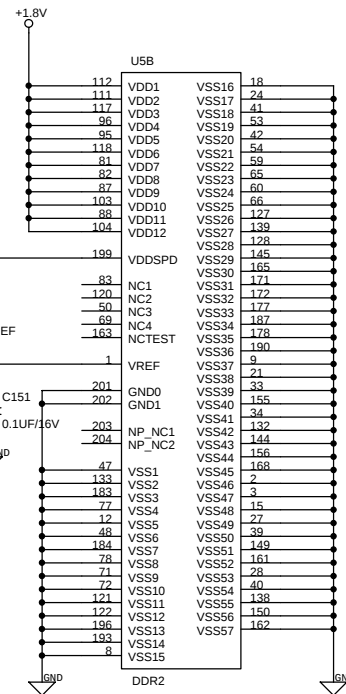
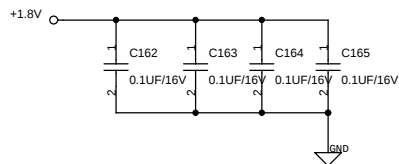
Layout Note: Place these Caps near SO DIMM 0



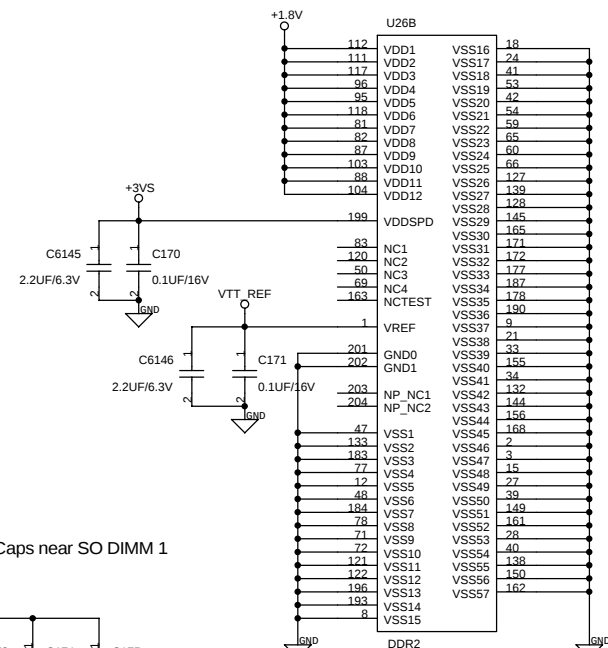
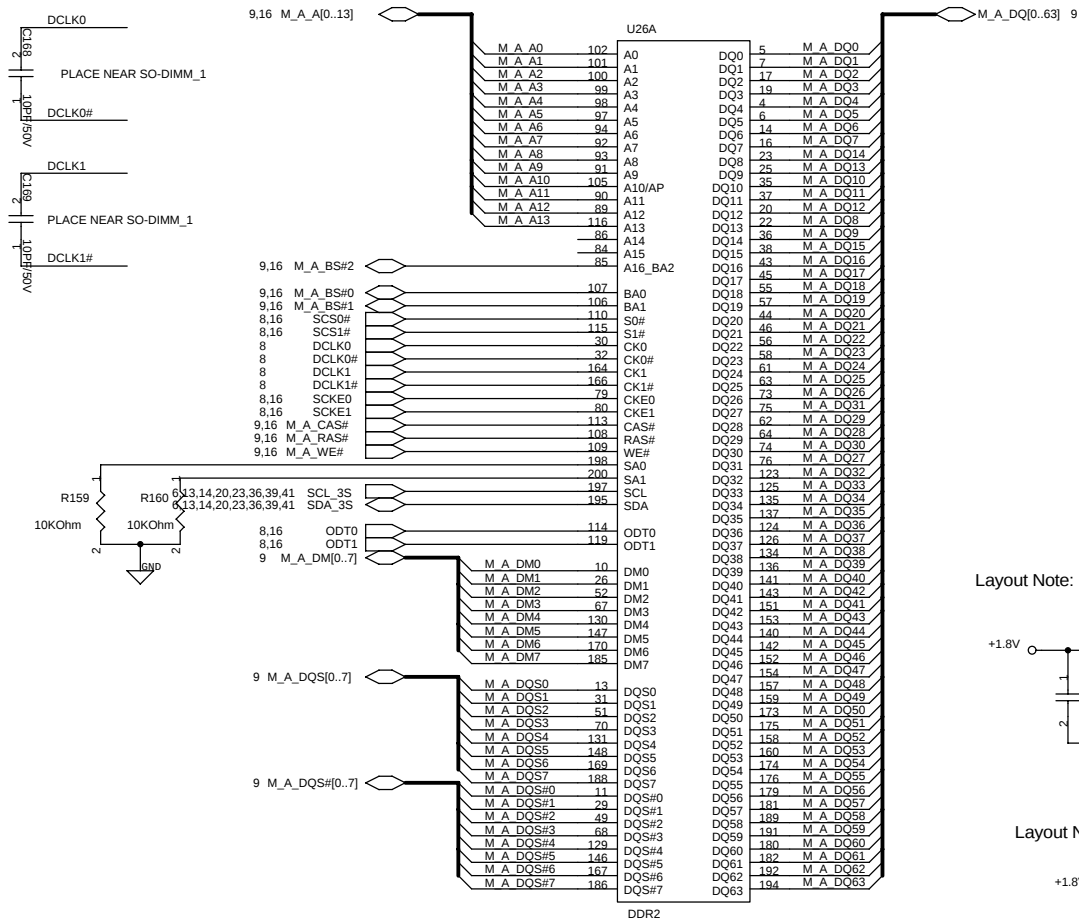
Layout Note: Place these Caps near SO DIMM 0



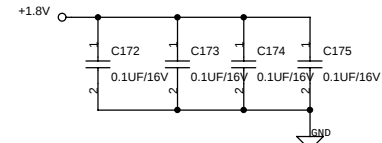
Layout Note: Place these High-Freq decoupling Caps near the GMCH



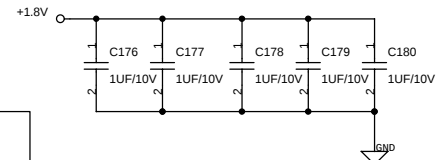
SO-DIMM Part is QUASAR
BOM is TYCO



Layout Note: Place these Caps near SO DIMM 1

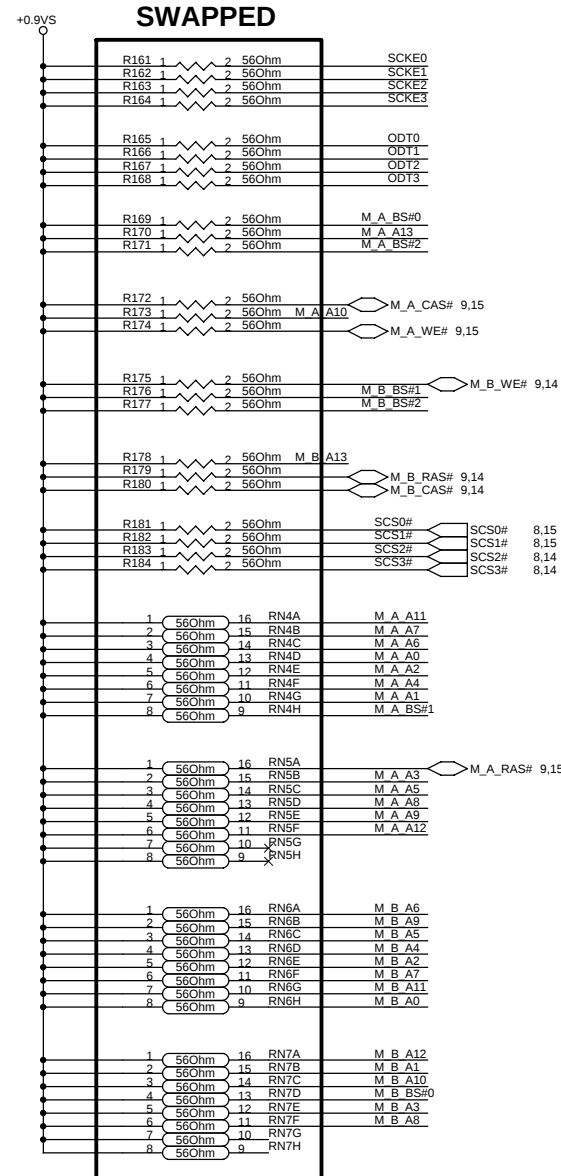
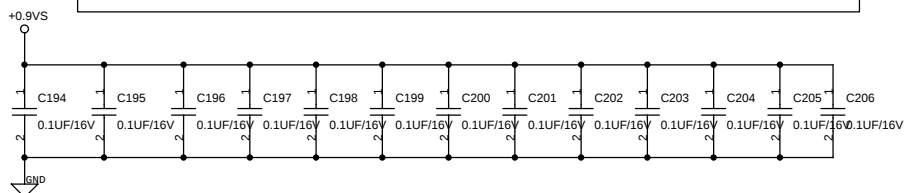
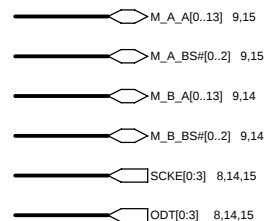


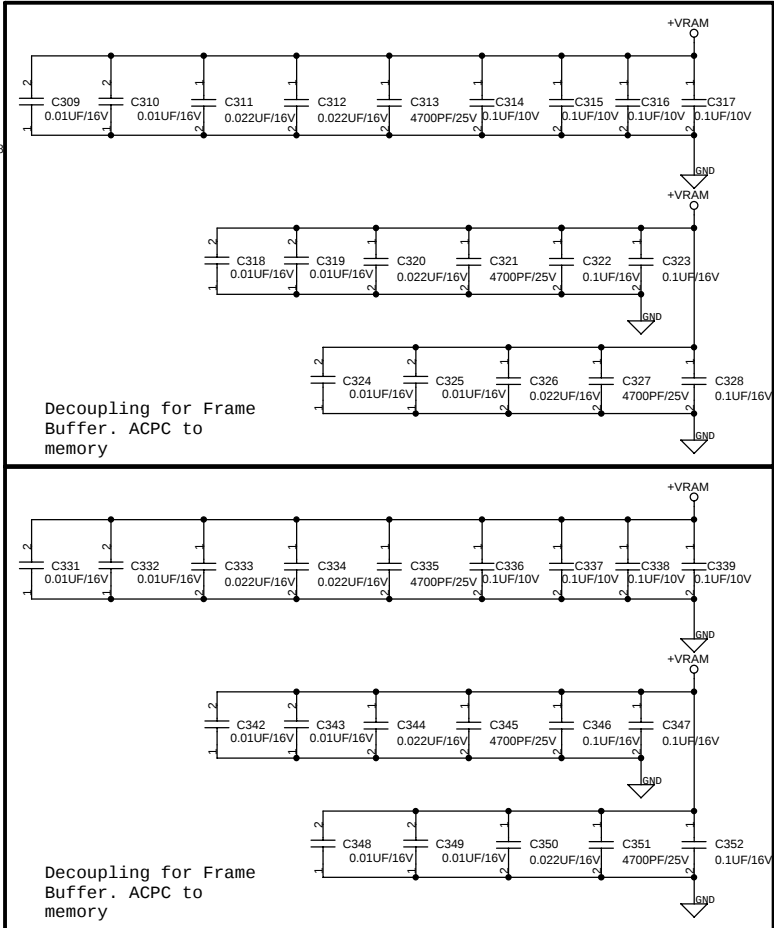
Layout Note: Place these Caps near SO DIMM 1

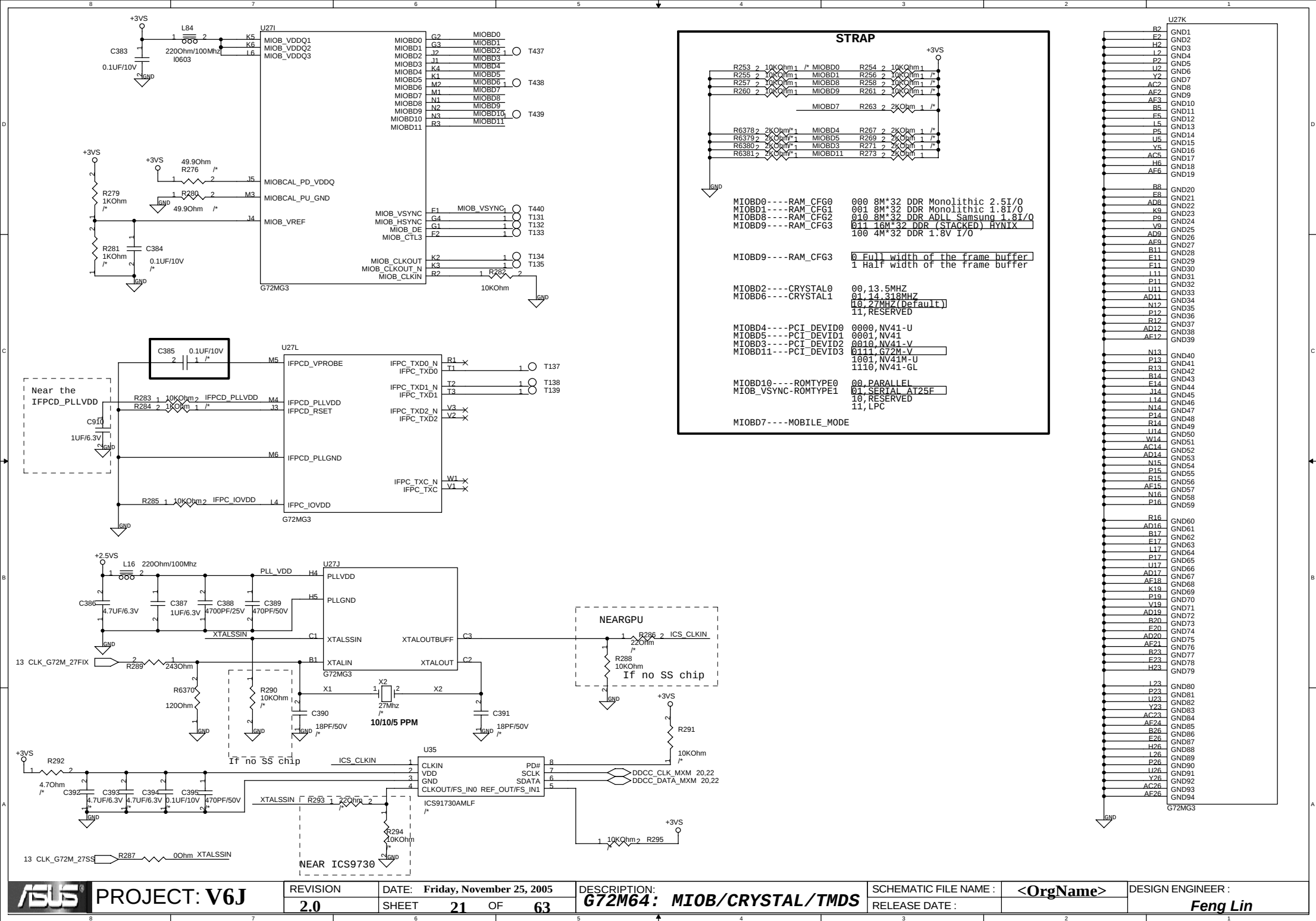


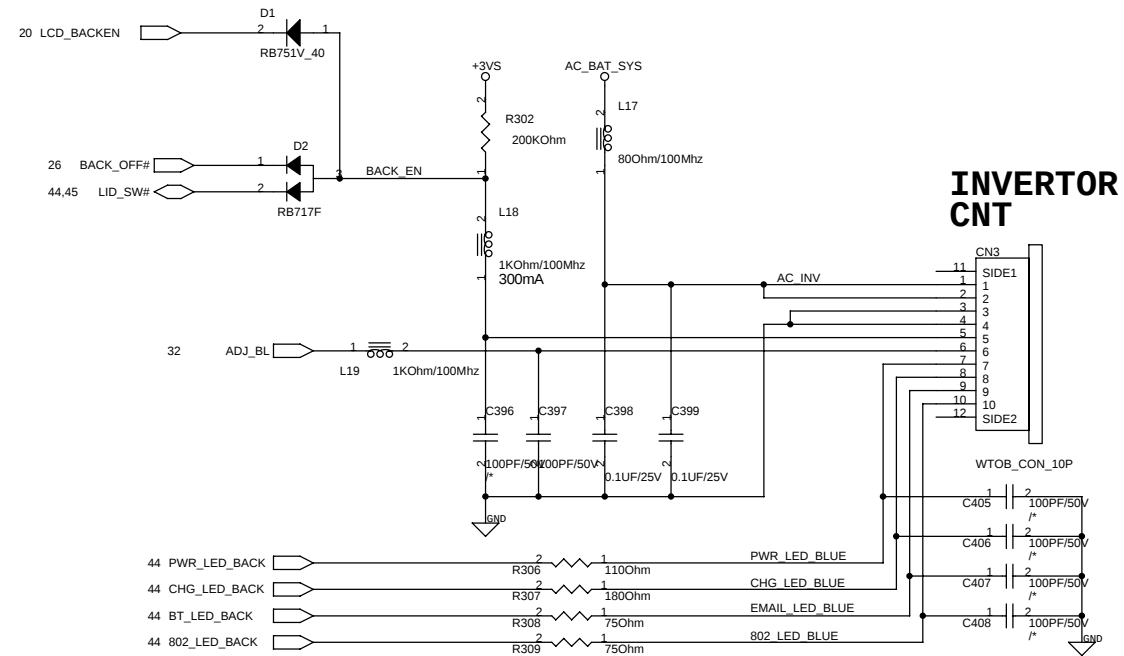
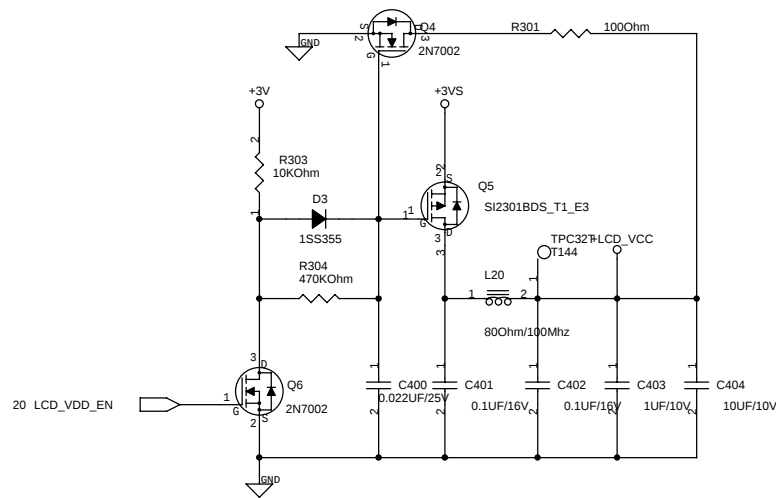
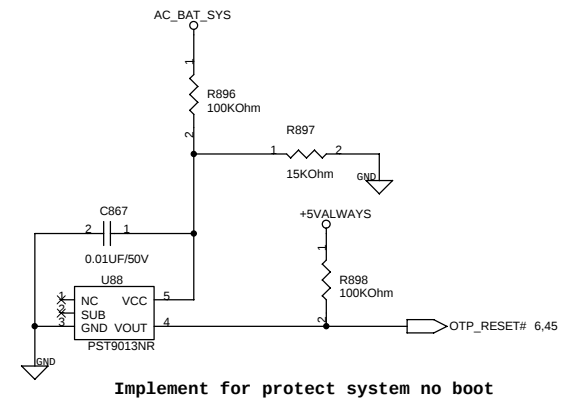
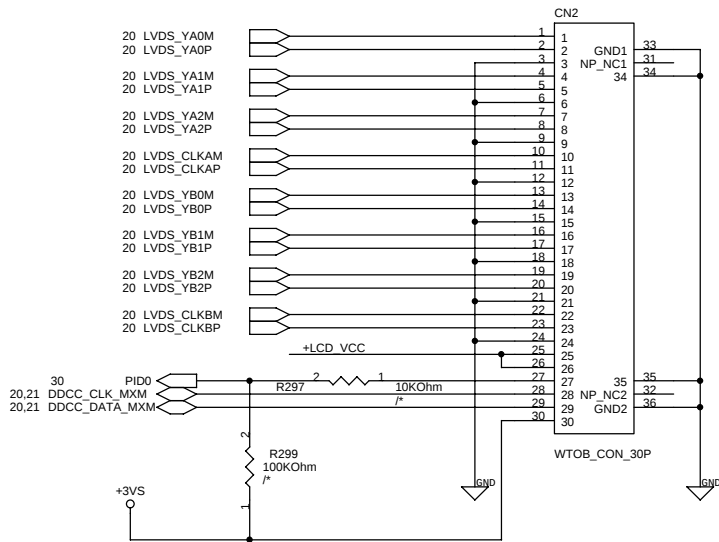
SO-DIMM Part is QUASAR
BOM is TYCO

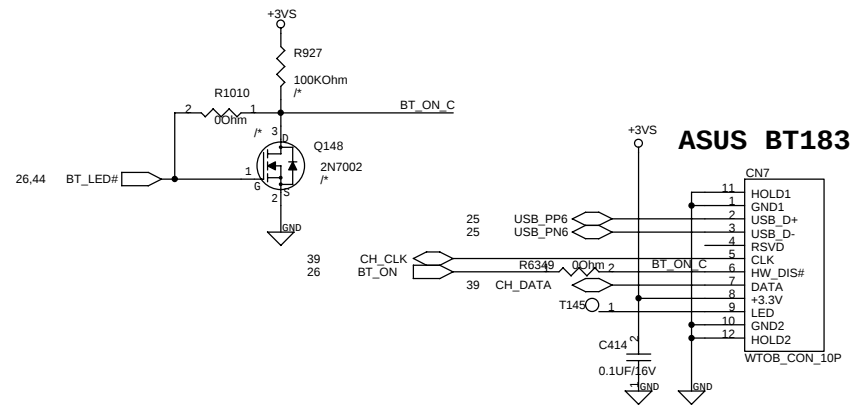
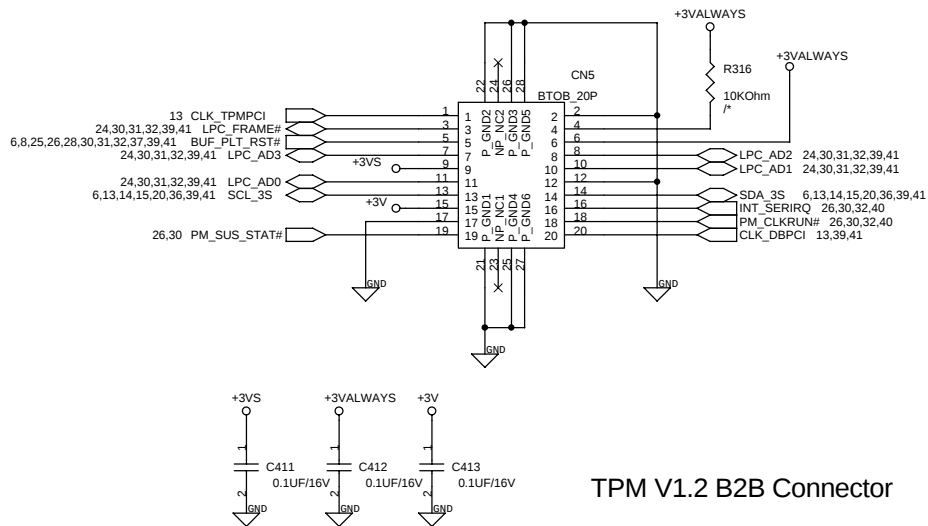
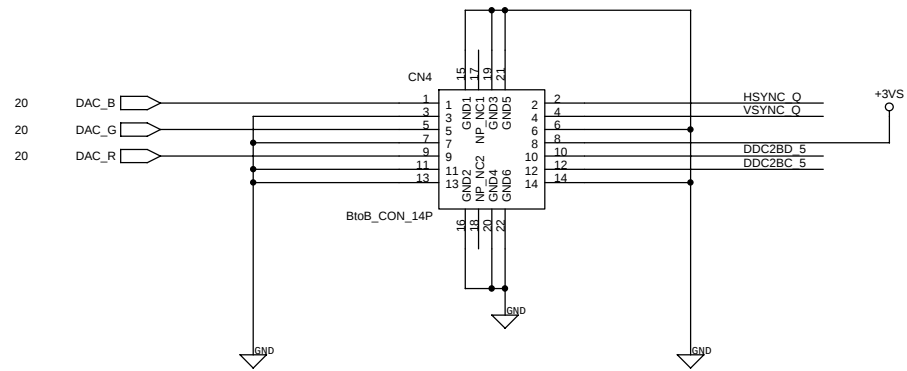
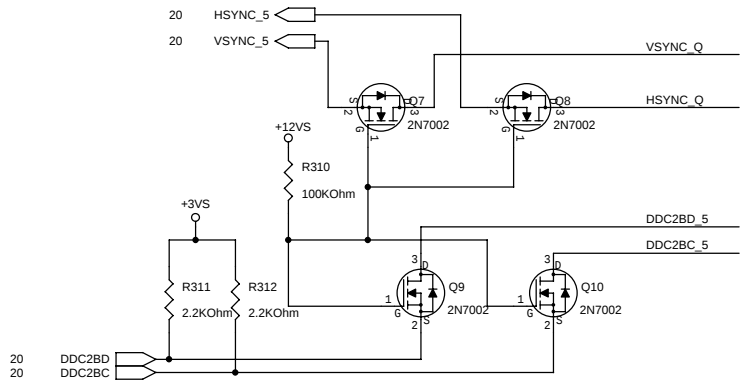
SO-DIMM 1 is placed farther
from the GMCH than SO-DIMM 0

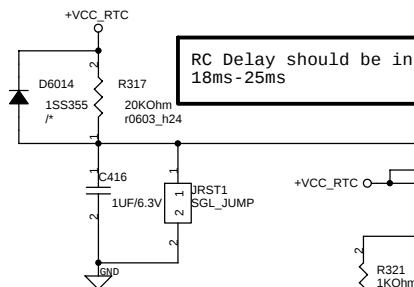
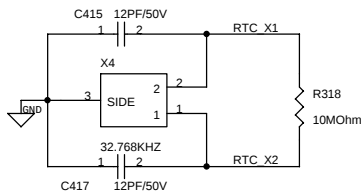




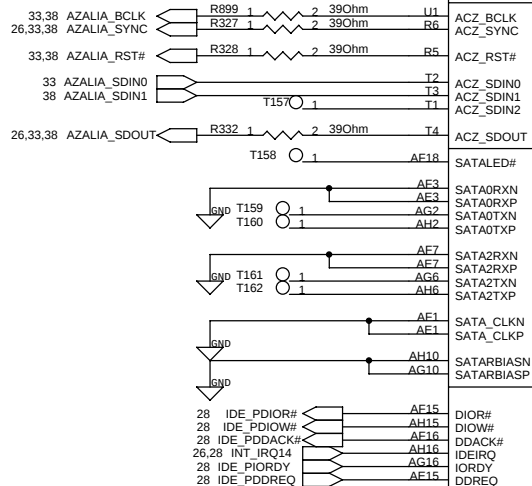




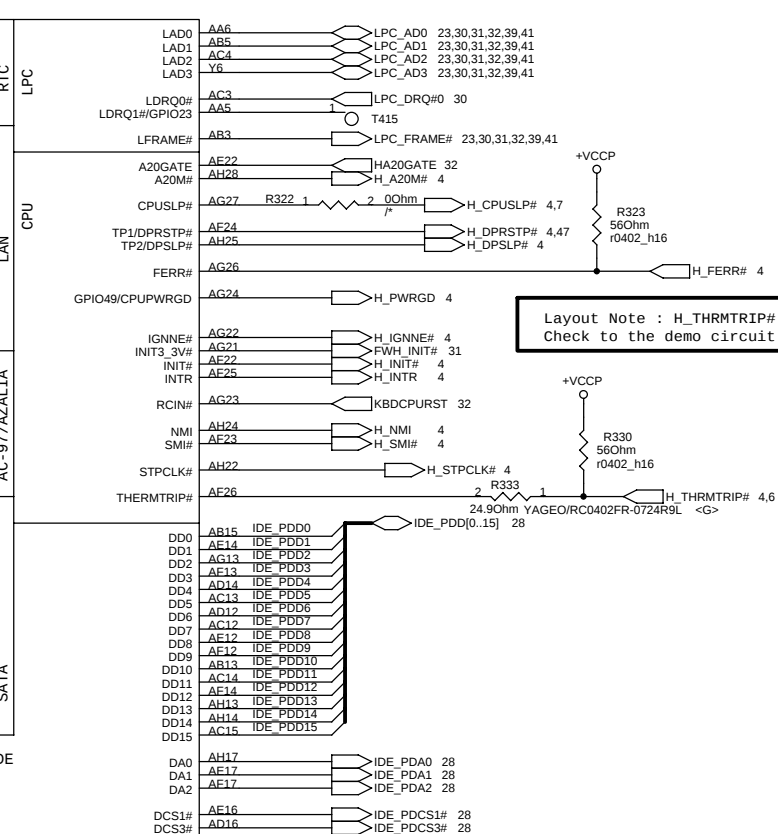
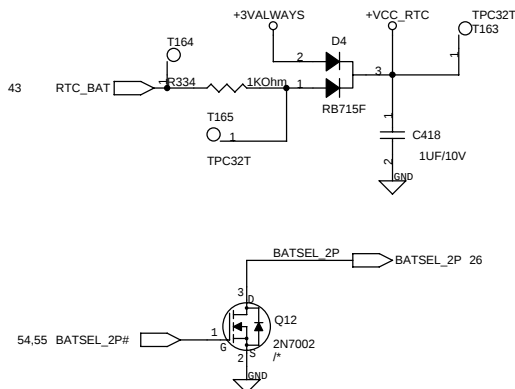




ACZ_SDIN[2:0] Integrated pull-down resistors.



Power Plane	Max Power Consumption			
	S0	S3cold	S4/S5	G3
Vcc1_05	0.86A	NA	NA	NA
VccSus1_05	NOTE1	NA	NA	NA
Vcc1_5	1.78A	NA	NA	NA
Vcc3_3	0.33A	NA	NA	NA
VccSus3_3	52mA	30mA	30mA	NA
VccRTC	NA	NA	NA	6uA
V5REF	6mA	NA	NA	NA
V5REF_Sus	10mA	10mA	10mA	NA
V_CPU_I0	14mA	NA	NA	NA
VccUSBPLL	10mA	NA	NA	NA
VccDMIPLL	50mA	NA	NA	NA
VccSATAPLL	50mA	NA	NA	NA



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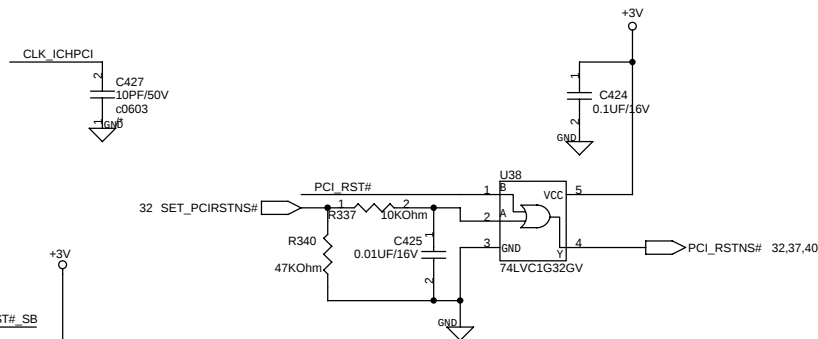
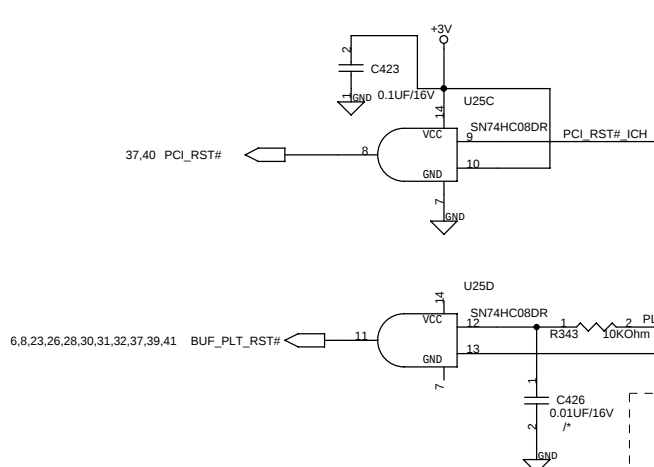
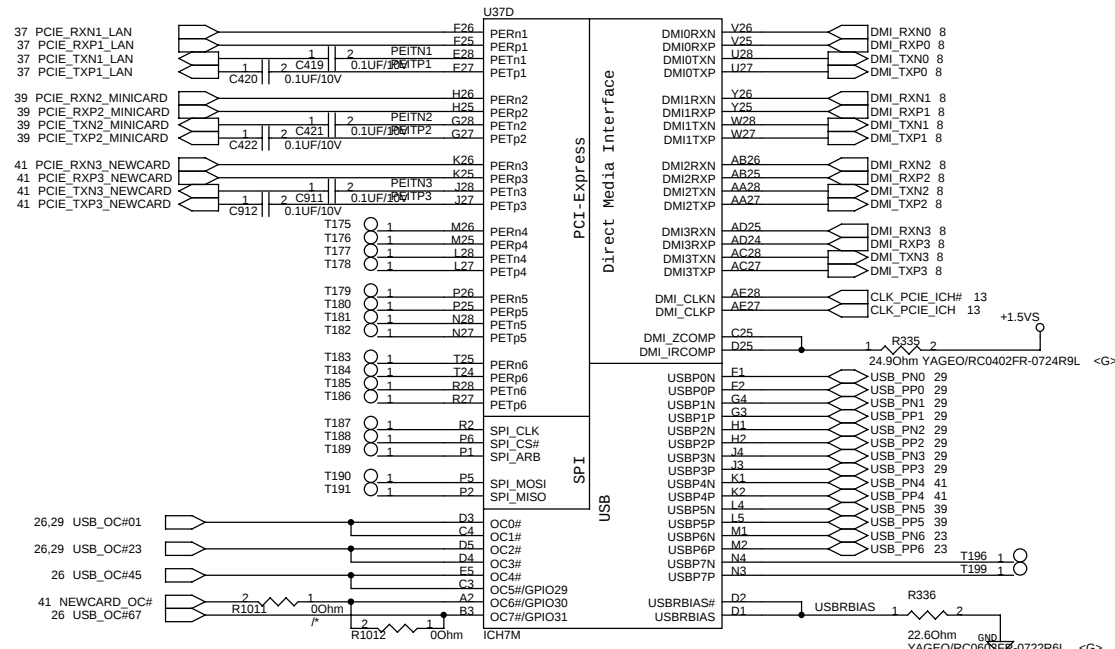
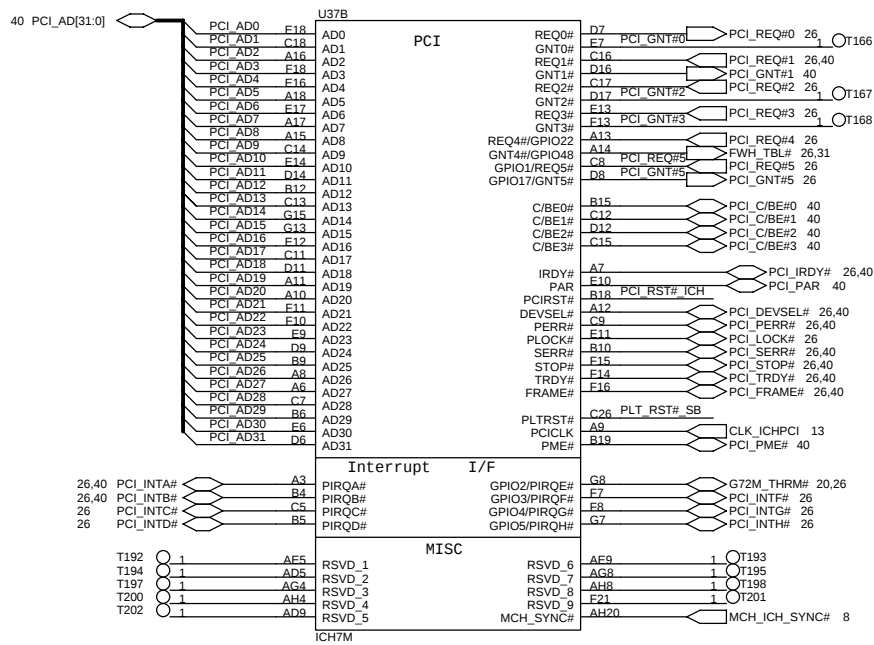
REVISION
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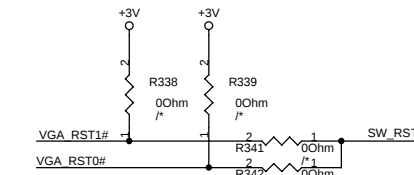
DESCRIPTION:
ICH7: IDE/AC97/LPC/RTC

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

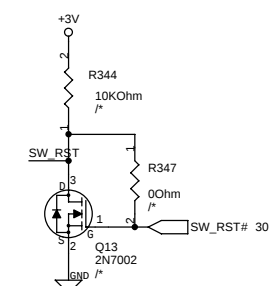
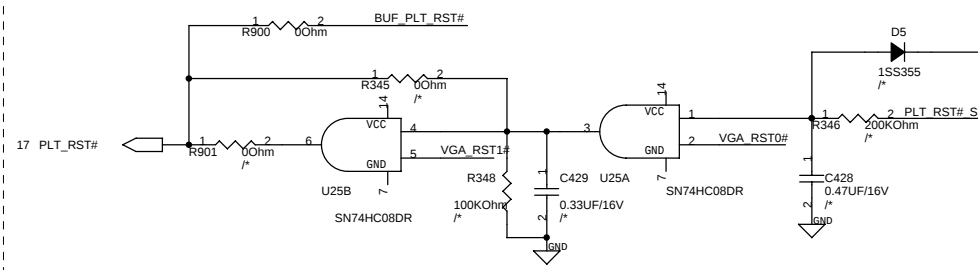
DESIGN ENGINEER :
Feng Lin



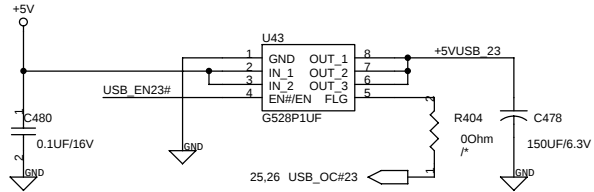
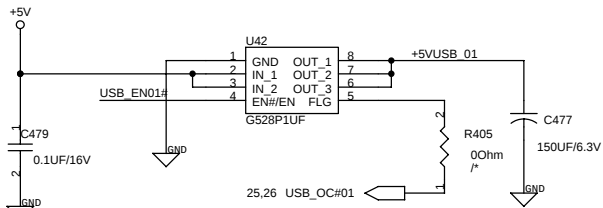
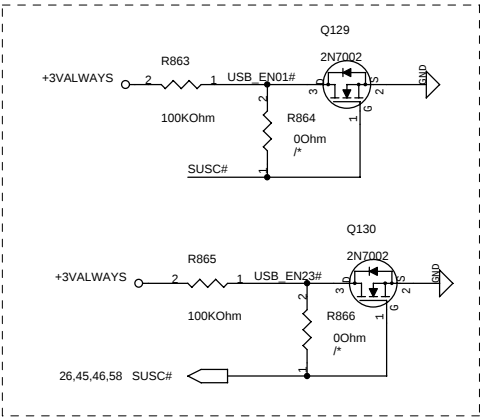
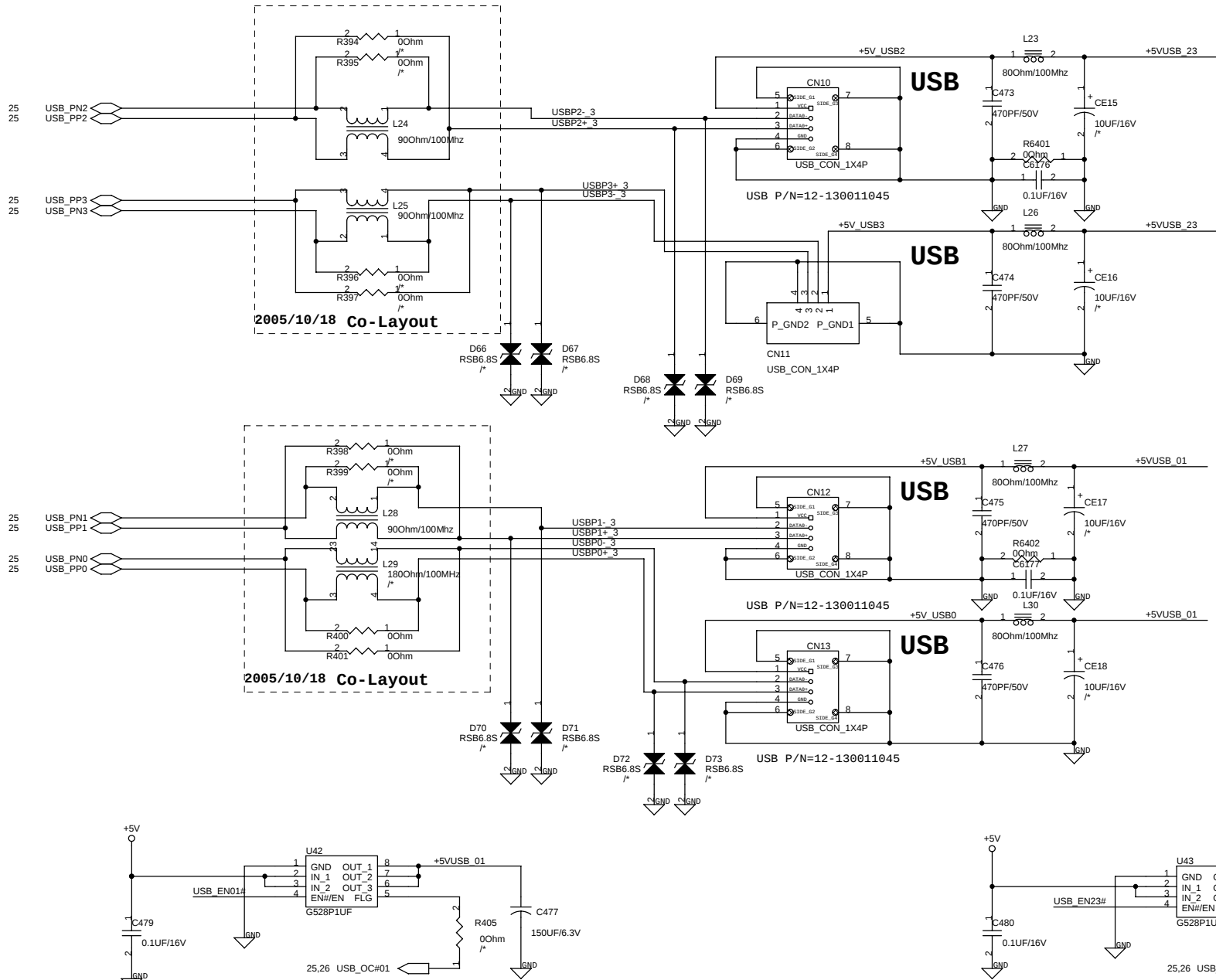
Reserve for VGA reset



Reserve for VGA reset







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DATE: Friday, November 25, 2005
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DESCRIPTION:

USB PORTS

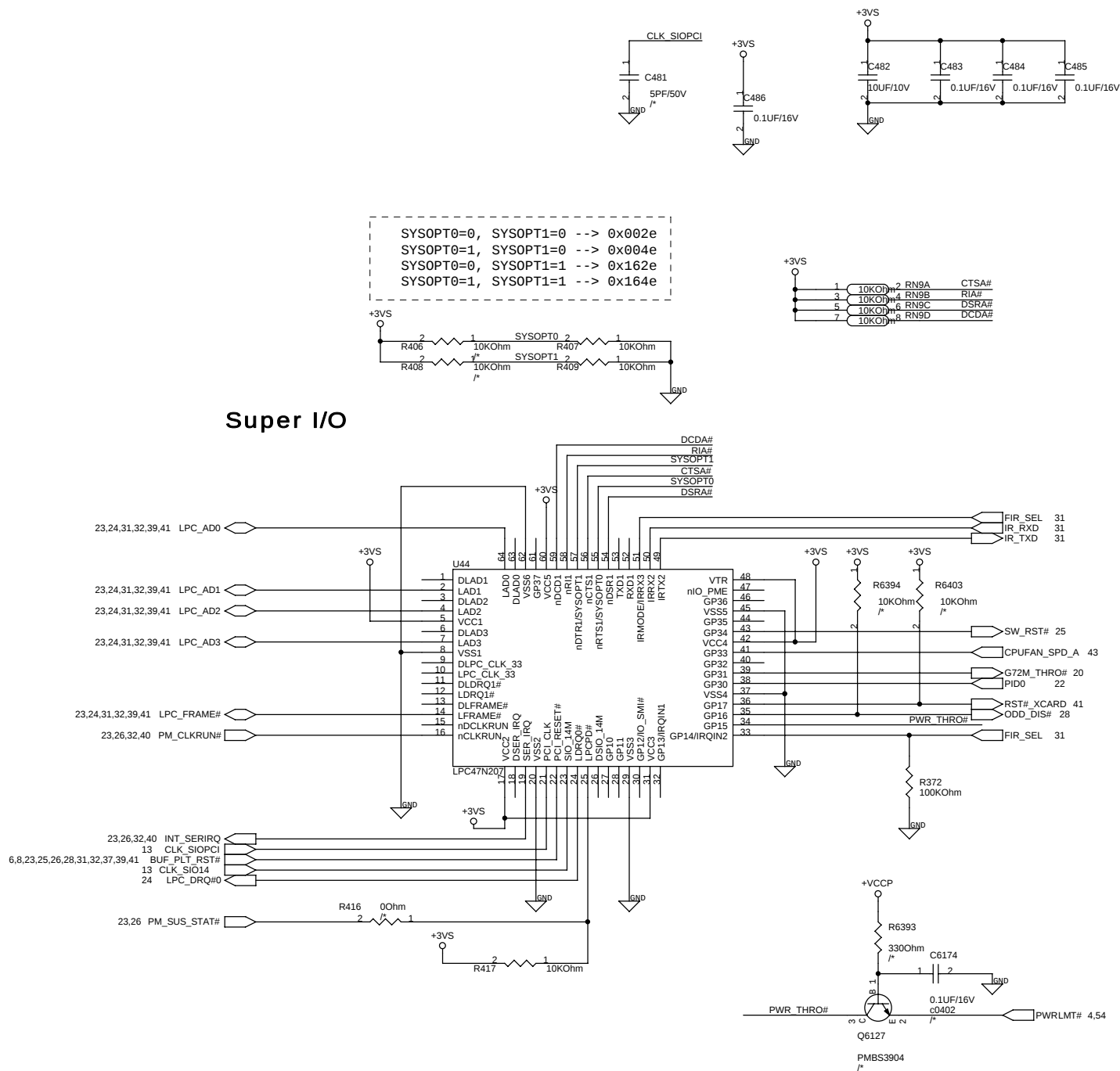
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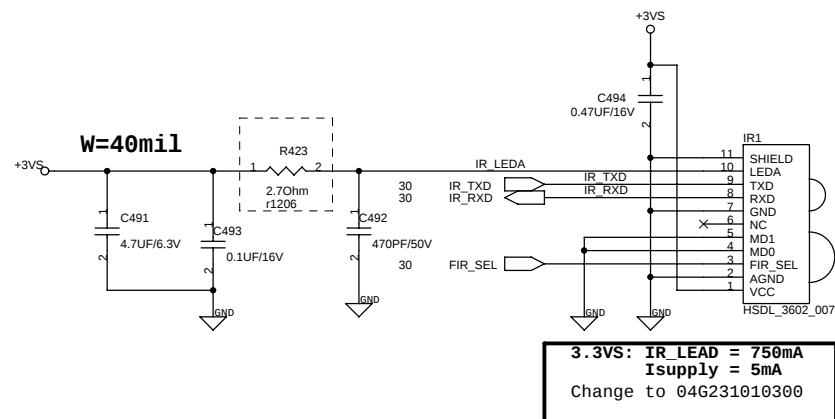
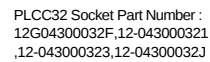
<OrgName>

RELEASE DATE :

DESIGN ENGINEER :

Julian Kuo



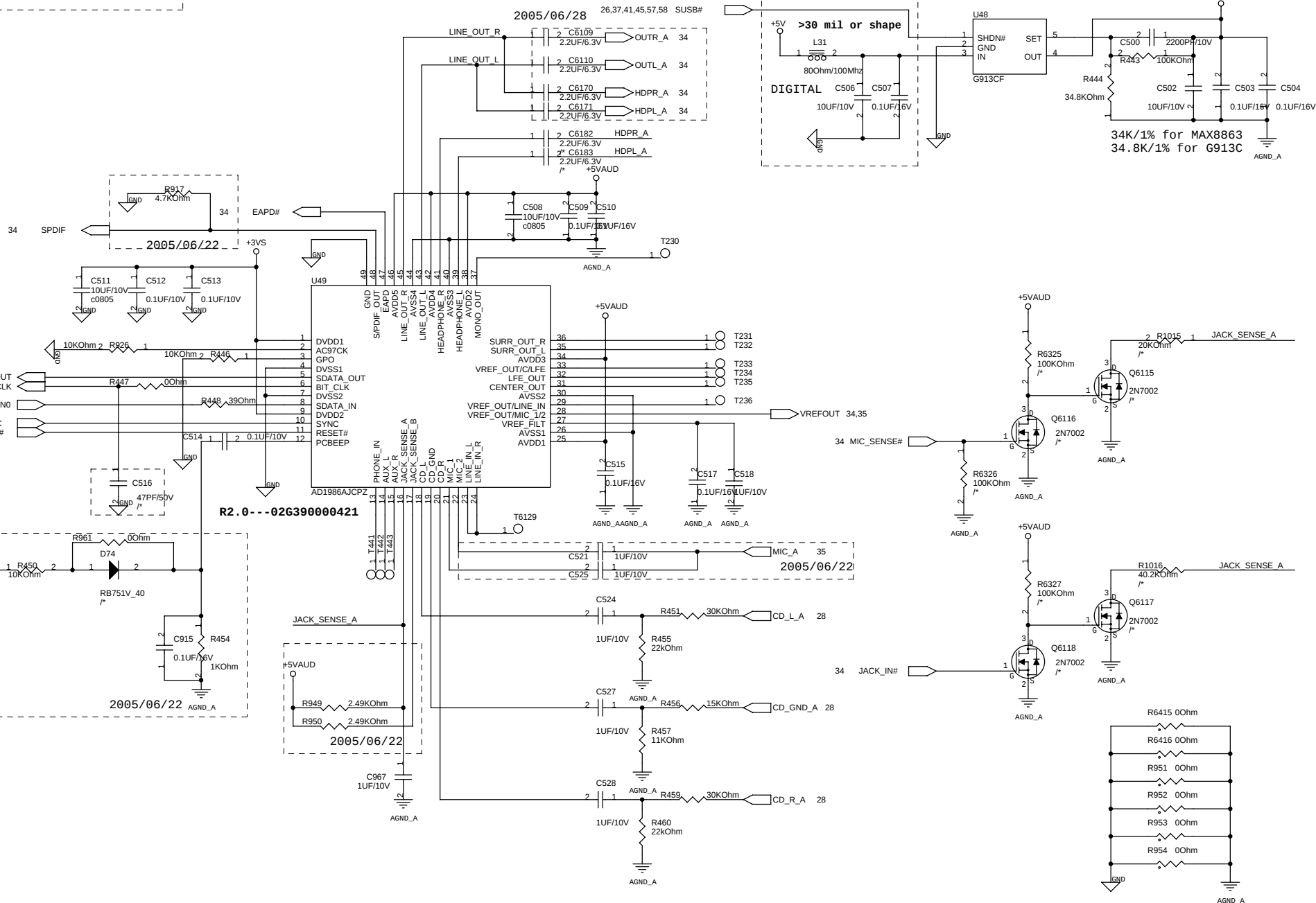


P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode



Internal pull low: SDATA-IN
Internal pull up: JD0, JD1, JD2, XTLSSEL

$$V_o = V_{ref} = (1.250) * (1 + R_{428}/R_{429}) - G_{913C}$$



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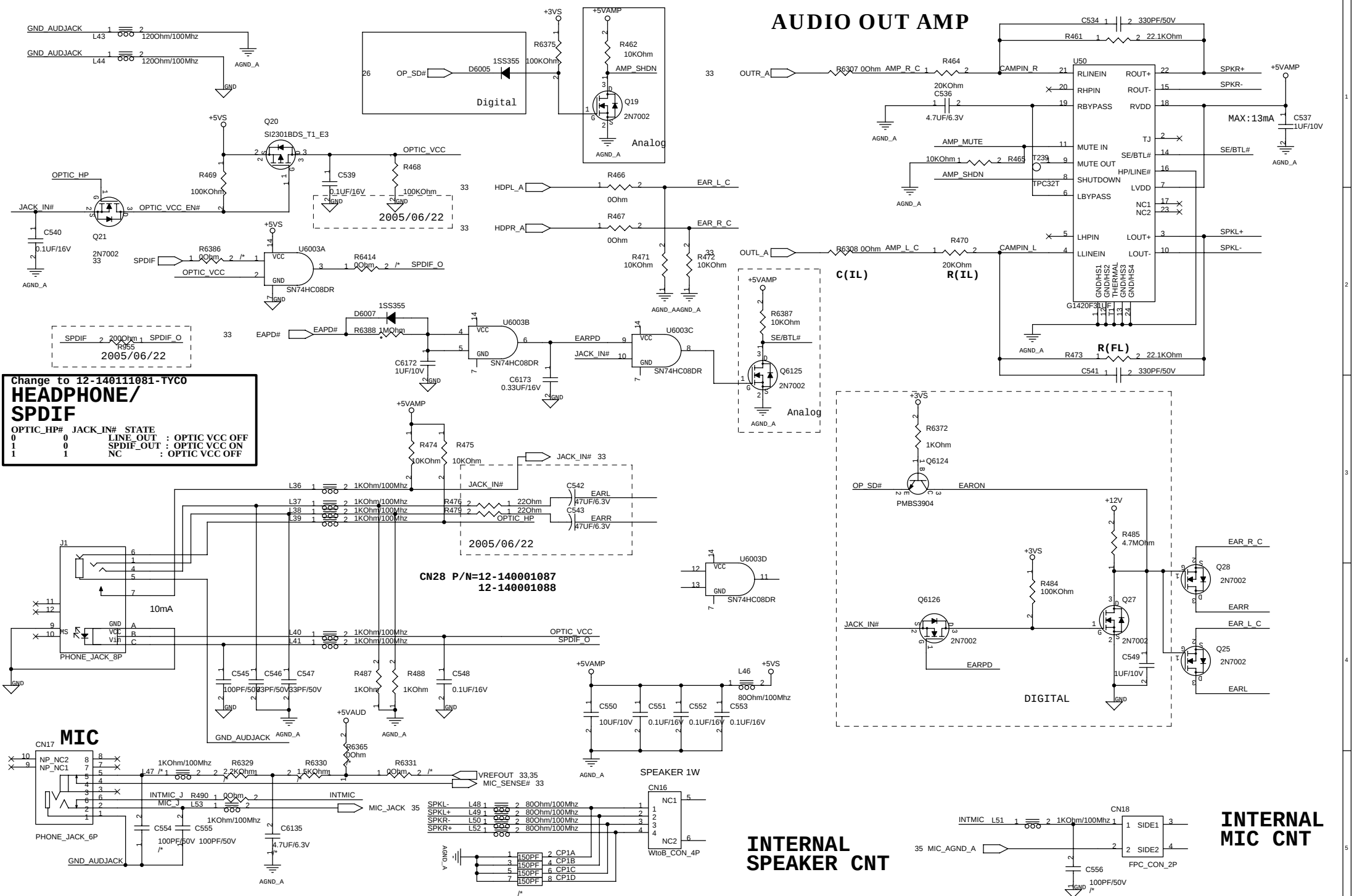
REVISION
2.0

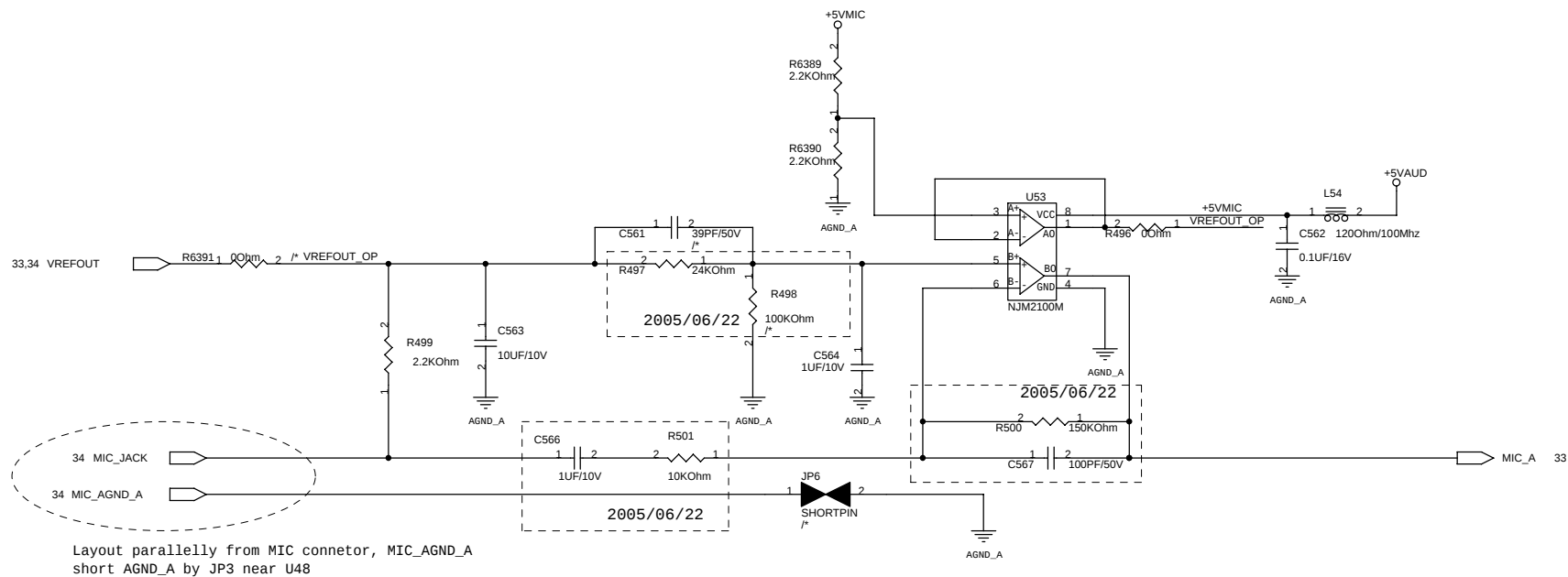
DATE: Friday, November 25, 2005
SHEET 33 OF 63

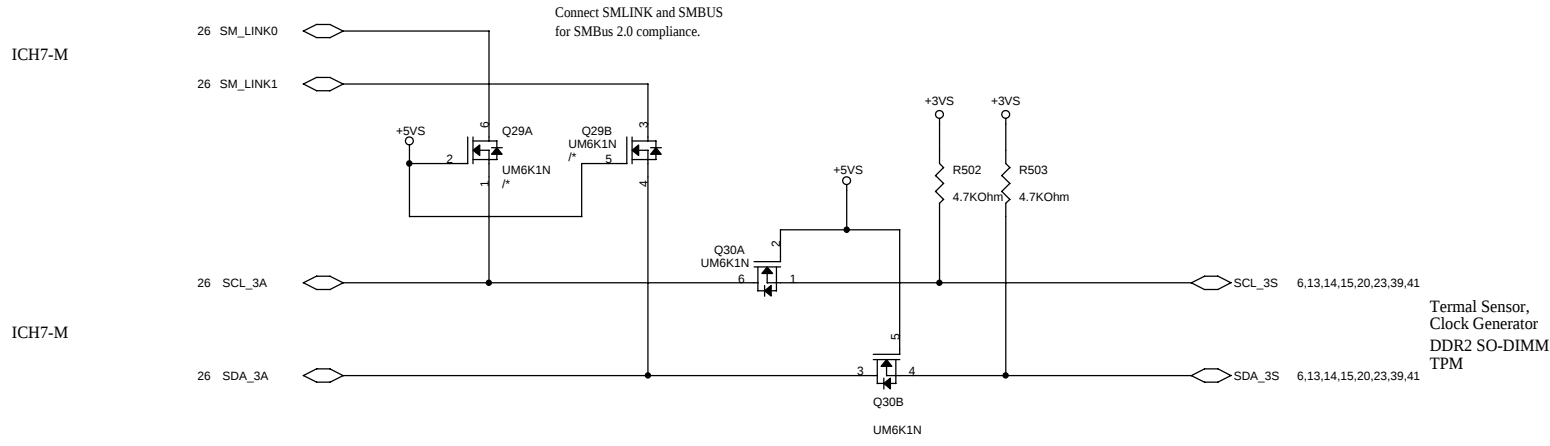
DESCRIPTION:
AUDIO AD1986

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
Feng Lin







+3VALWAYS	O	+	3VALWAYS	23,24,29,32,44,45,46,51,60
+3VSUS	O	+	3VSUS	26,27,32,37,41,45,48
+5VALWAYS	O	+	5VALWAYS	22,48,51,54
+5VSUS	O	+	5VSUS	27,44,48
+3VO	O	+	3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+5VO	O	+	5V	14,29,33,41,44,46,56,58
+12VO	O	+	12V	34,42,58
+3VS	O	+	3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+5VS	O	+	5VS	20,27,28,32,34,39,43,44,45,46,47,58
+12VS	O	+	12VS	23,44,58
VTT_REFO	O	+	VTT_REF	8,14,15,16
+2.5VS	O	+	2.5VS	10,20,21,46,51
+1.8VS	O	+	1.8V	20,46,58
+0.9VS	O	+	0.9V	16,50
+1.5VS	O	+	1.5VS	5,8,10,11,25,27,39,41,46,49
+VCC_RTC	O	+	VCC_RTC	24,27
+1.8VO	O	+	1.8V	8,11,14,15,46,50
+3VA	O	+	3VALWAYS	23,24,29,32,44,45,46,51,60
+5VA	O	+	5VALWAYS	22,48,51,54
+5VAUD	O	+	5VAUD	33,34,35
VTT_REFO	O	+	VTT_REF	8,14,15,16
A/D_DOCK_IN	O	+	A/D_DOCK_IN	43,54,56,57
+3VSUS_PE	O	+	3VSUS_PE	41
+3VS_PE	O	+	3VS_PE	41
+1.5VS_PE	O	+	1.5VS_PE	41

NEWCARD

YONAH

+VCCP	O	+	VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+VCORE	O	+	VCORE	5,6,46,47
+1.5VS	O	+	1.5VS	5,8,10,11,25,27,39,41,46,49

Calistoga

+VCCP	O	+	VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+1.5VS	O	+	1.5VS	5,8,10,11,25,27,39,41,46,49
+3VS	O	+	3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+1.8VS	O	+	1.8VS	20,46,58
+VTT_REFO	O	+	VTT_REF	8,14,15,16
+2.5VS	O	+	2.5VS	10,20,21,46,51
+1.8V	O	+	1.8V	8,11,14,15,46,50

G72M G3-64

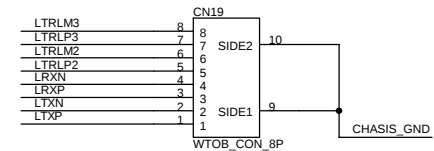
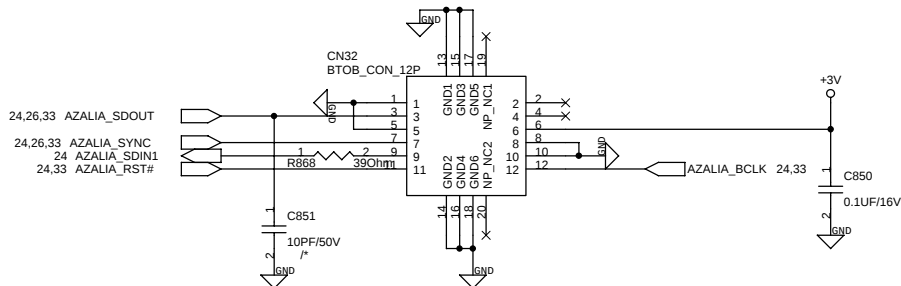
+VGA_VCORE	O	+	VGA_VCORE	17,46,52
+1.2VSP	O	+	1.2VSP	17,18,46,53
+3VS	O	+	3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+VRAM	O	+	VRAM	18,19,46,52
+2.5VS	O	+	2.5VS	10,20,21,46,51
+1.8VS	O	+	1.8VS	20,46,58
+5VS	O	+	5VS	20,27,28,32,34,39,43,44,45,46,47,58

ICH7

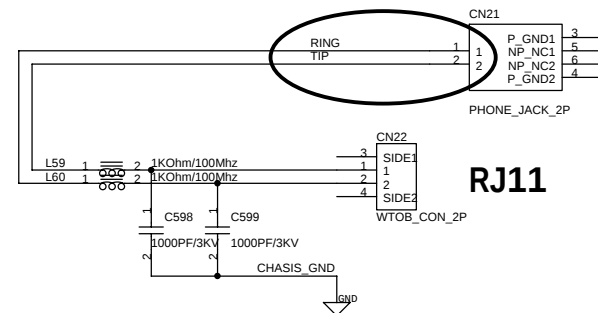
+VCC_RTC	O	+	VCC_RTC	24,27
+VCCP	O	+	VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+3VO	O	+	3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+1.5VS	O	+	1.5VS	5,8,10,11,25,27,39,41,46,49
+3VSUS	O	+	3VSUS	26,27,32,37,41,45,48
+5VSUS	O	+	5VSUS	27,44,48

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM

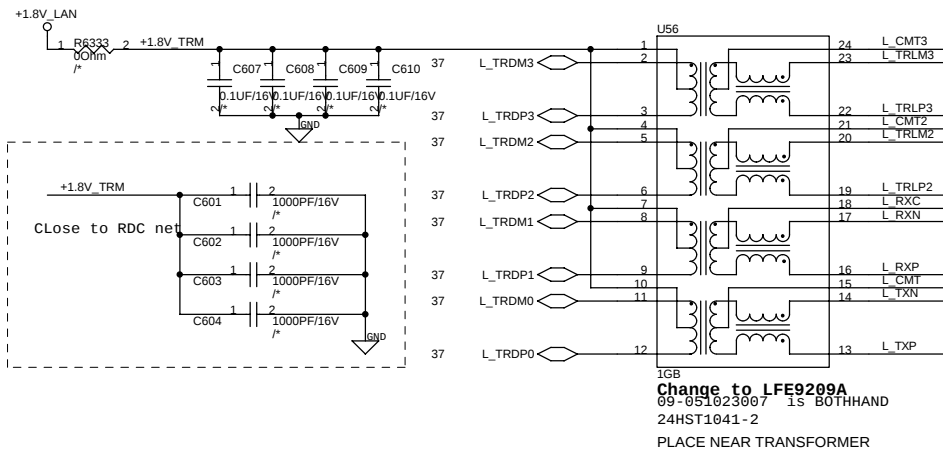
MDC CNT



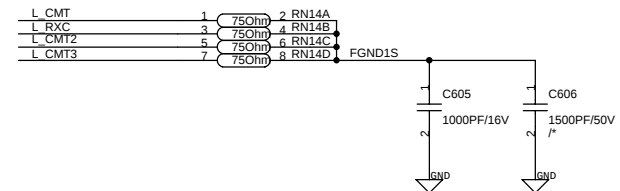
RJ45



RJ11



L_TRLP2	LTRLP2	L_TXP	LTXP
L_TRLM2	LTRLM2	L_TXN	LTXN
L_TRLP3	LTRLP3	L_RXP	LRXP
L_TRLM3	LTRLM3	L_RXN	LRXN



PROJECT: V6J

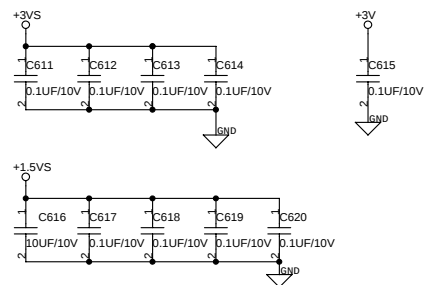
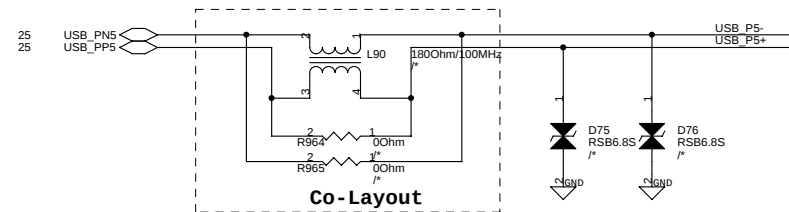
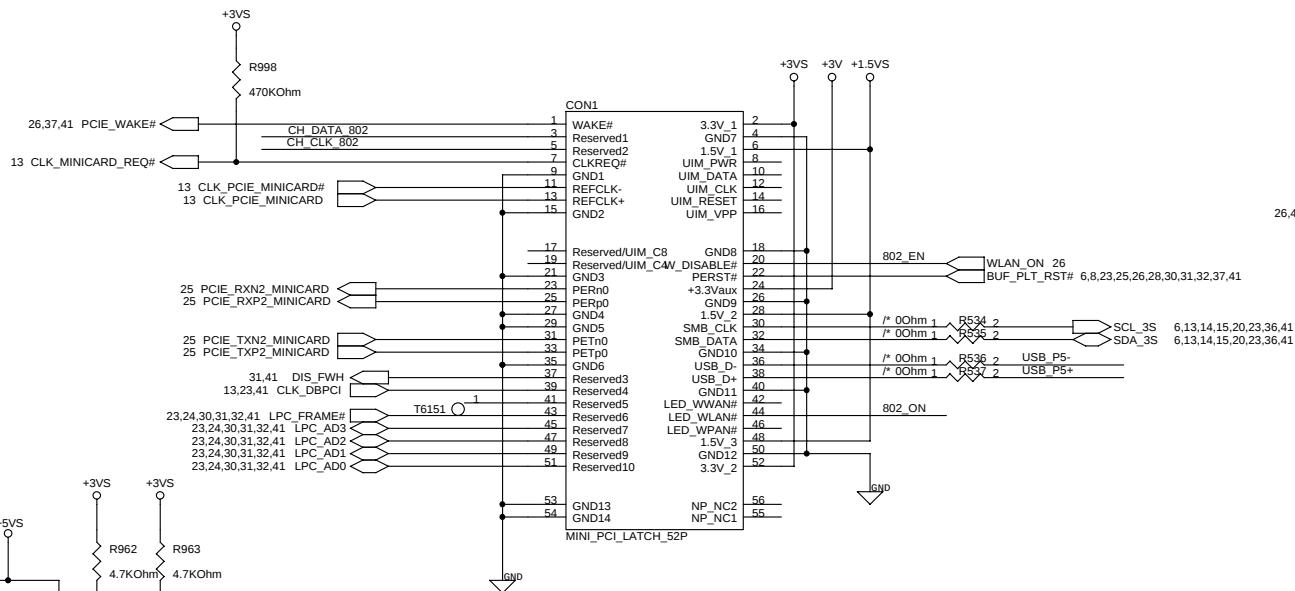
REVISION
2.0

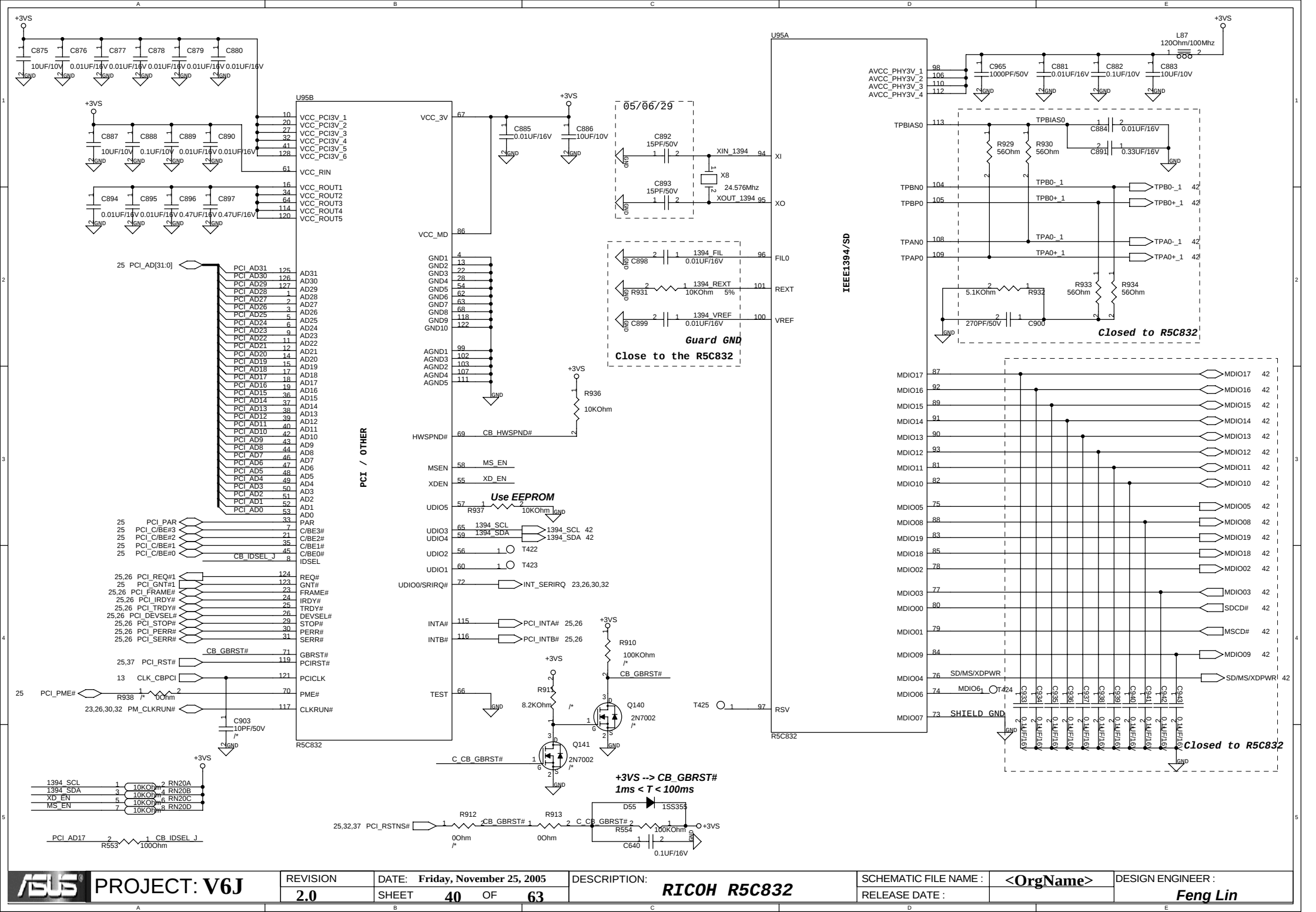
DATE: Friday, November 25, 2005
SHEET 38 OF 63

DESCRIPTION:
RJ45/RJ11/MDC

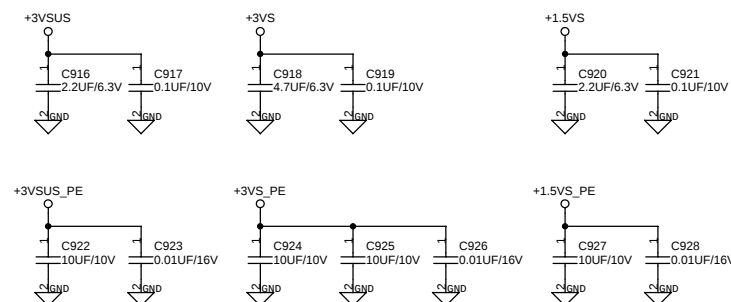
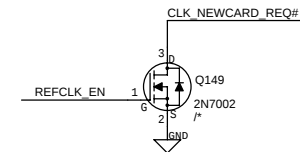
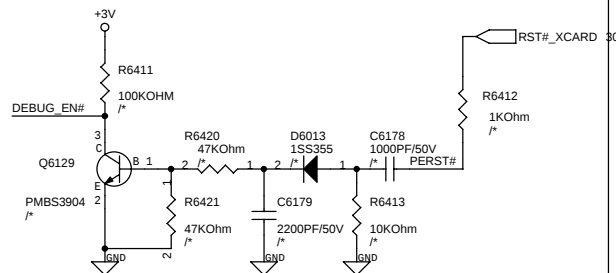
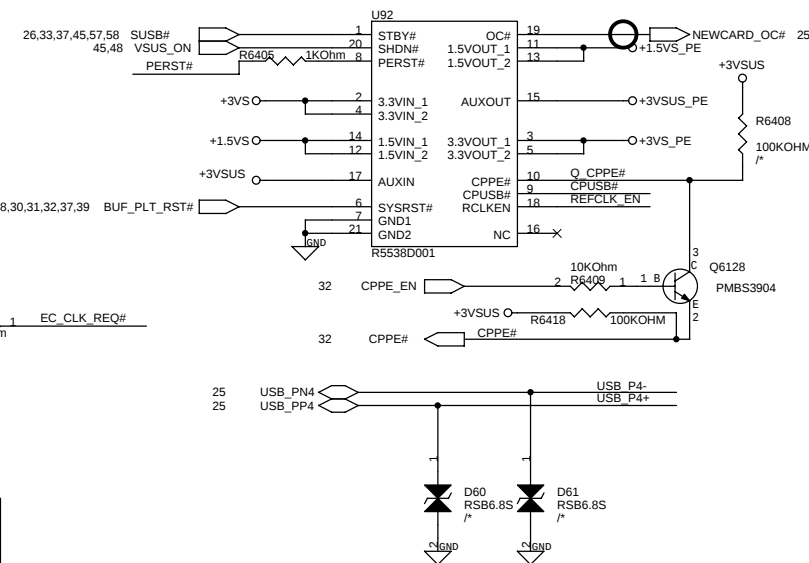
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DESIGN ENGINEER :
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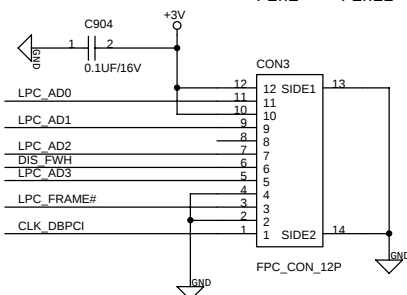




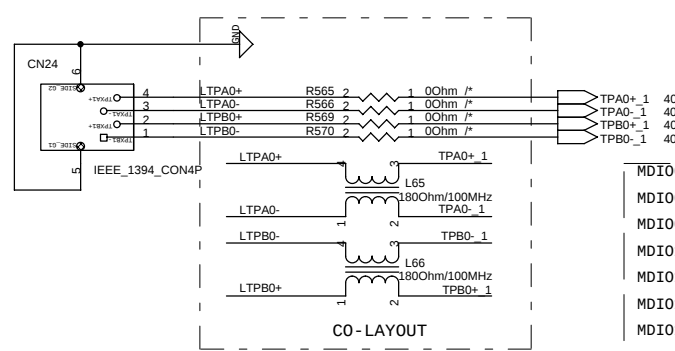
Change Pin9 from SMBDATA to +1.5V



Note: Layout define
Pin1--->Pin12

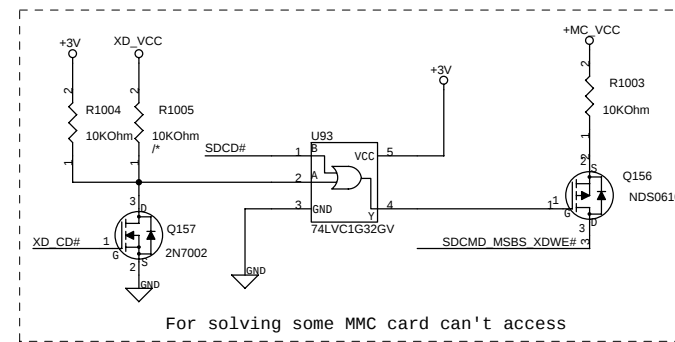
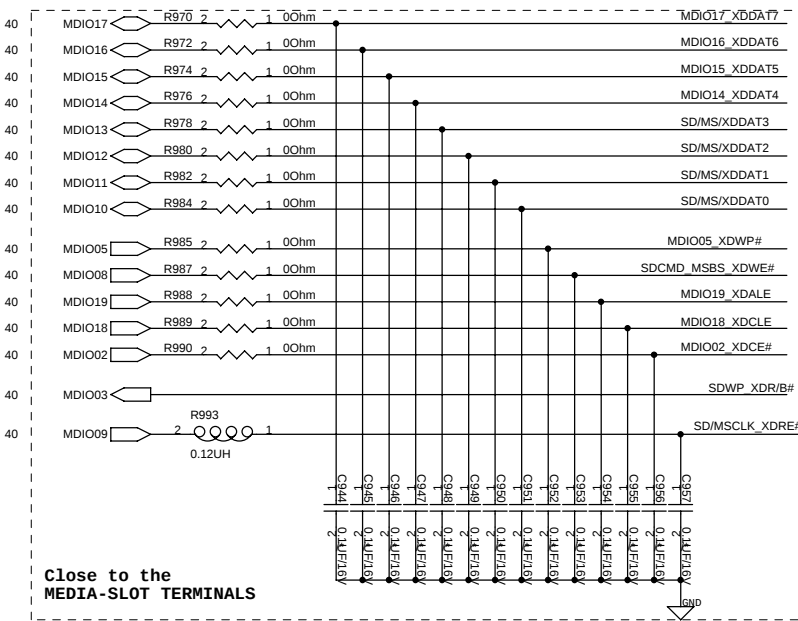
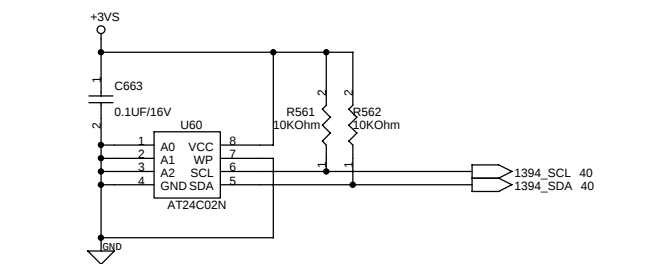


1394A

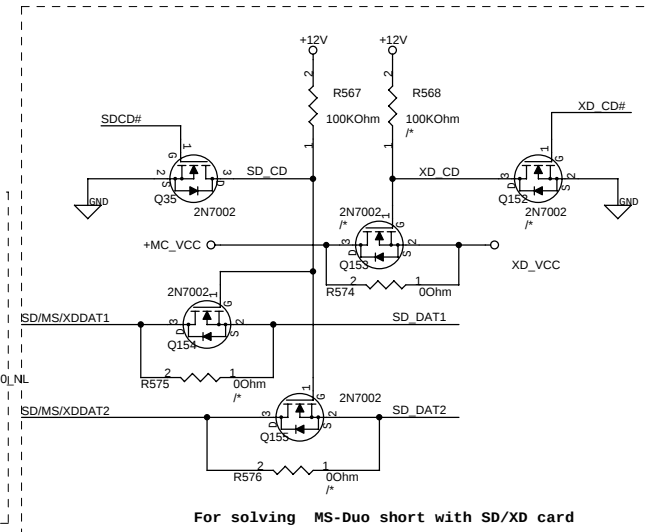


- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE

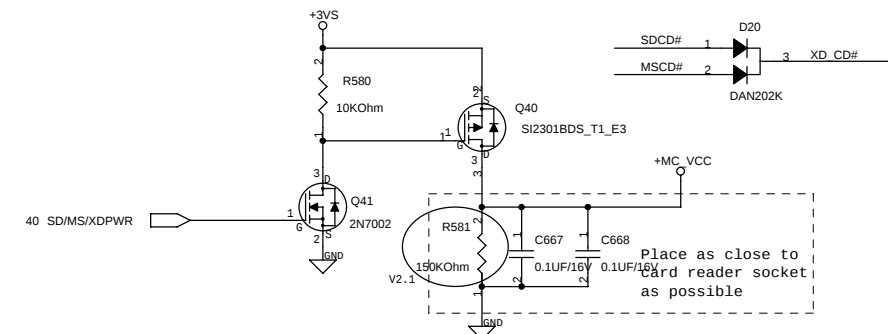
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/ MS Power Control
- MDIO07--> SD External Clock/ MS External Clock
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3



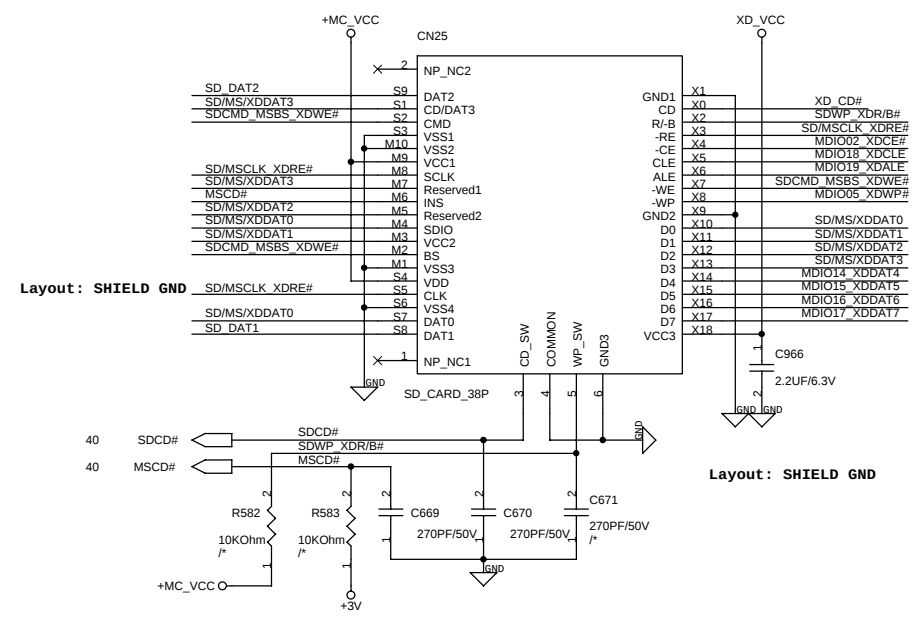
For solving some MMC card can't access



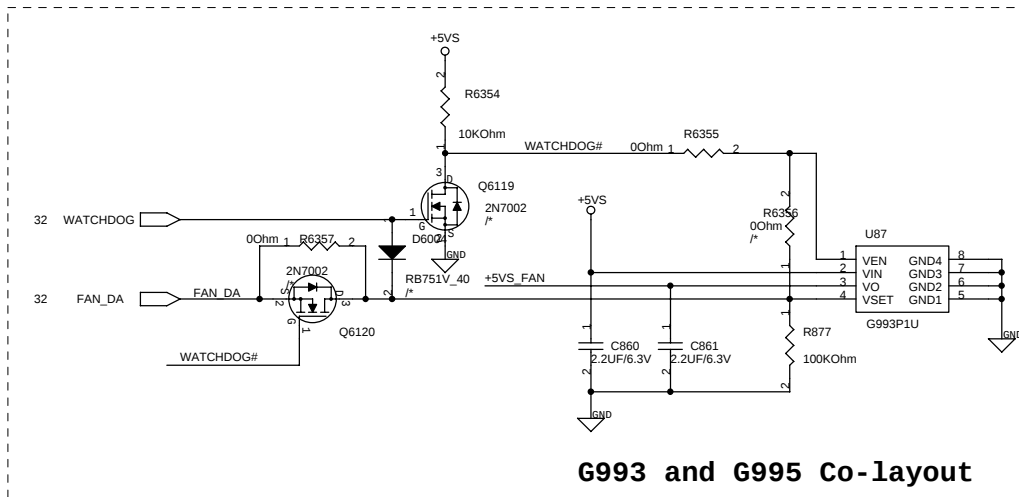
For solving MS-Duo short with SD/XD card



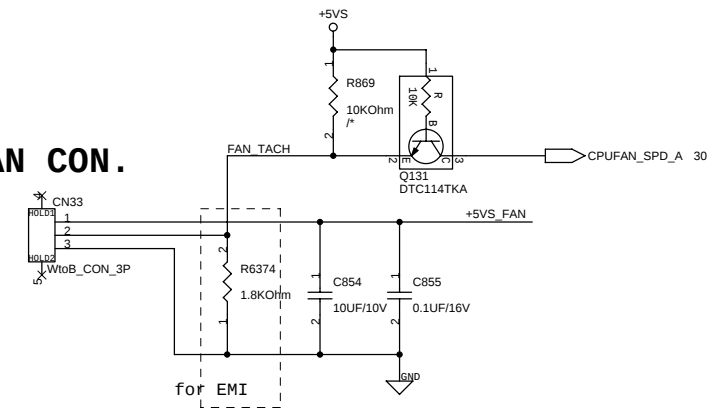
Place as close to card reader socket as possible



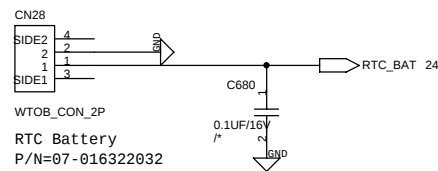
Layout: SHIELD GND



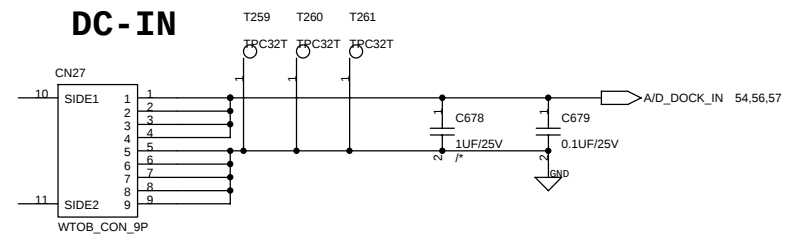
FAN CON.

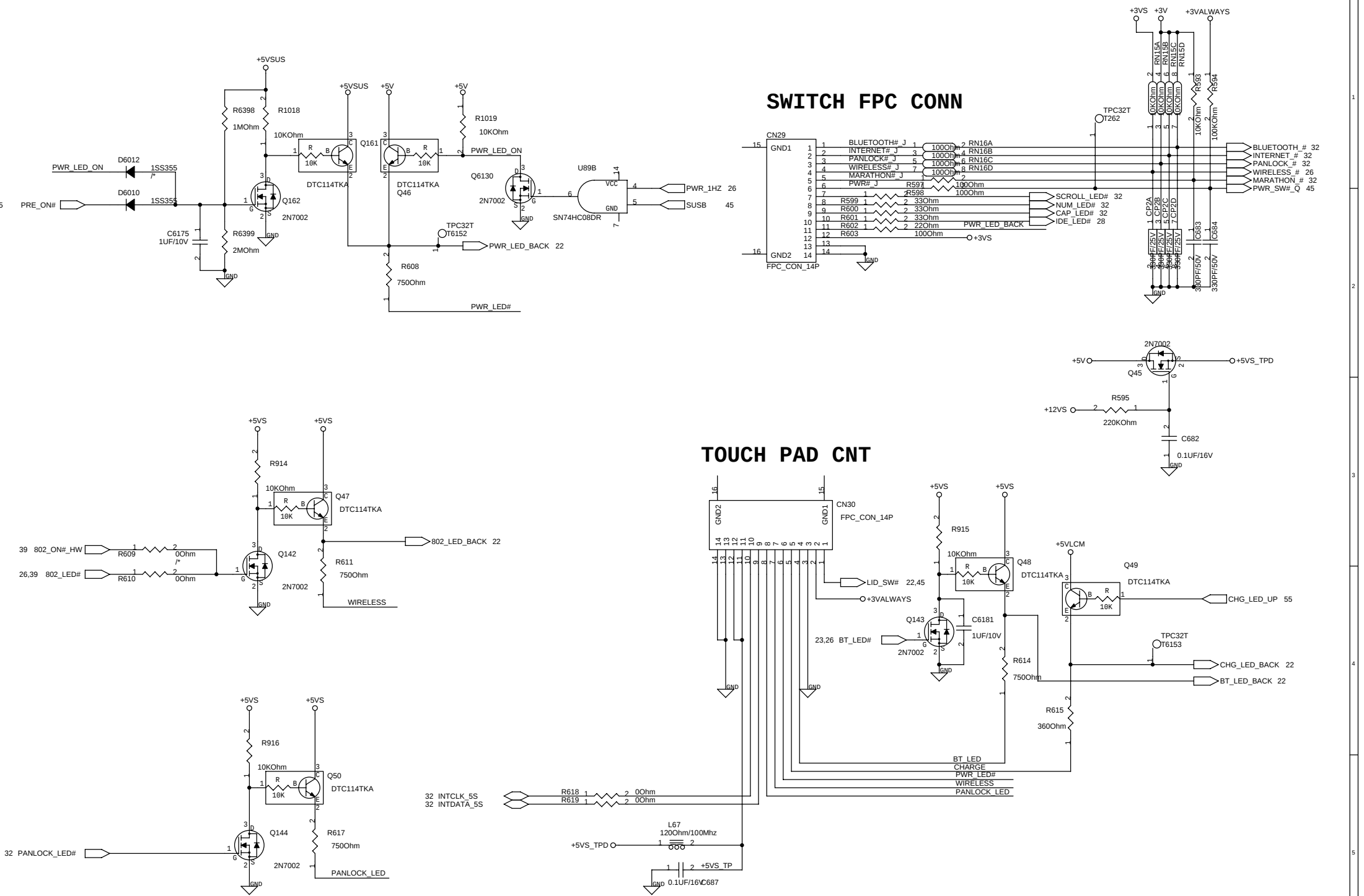


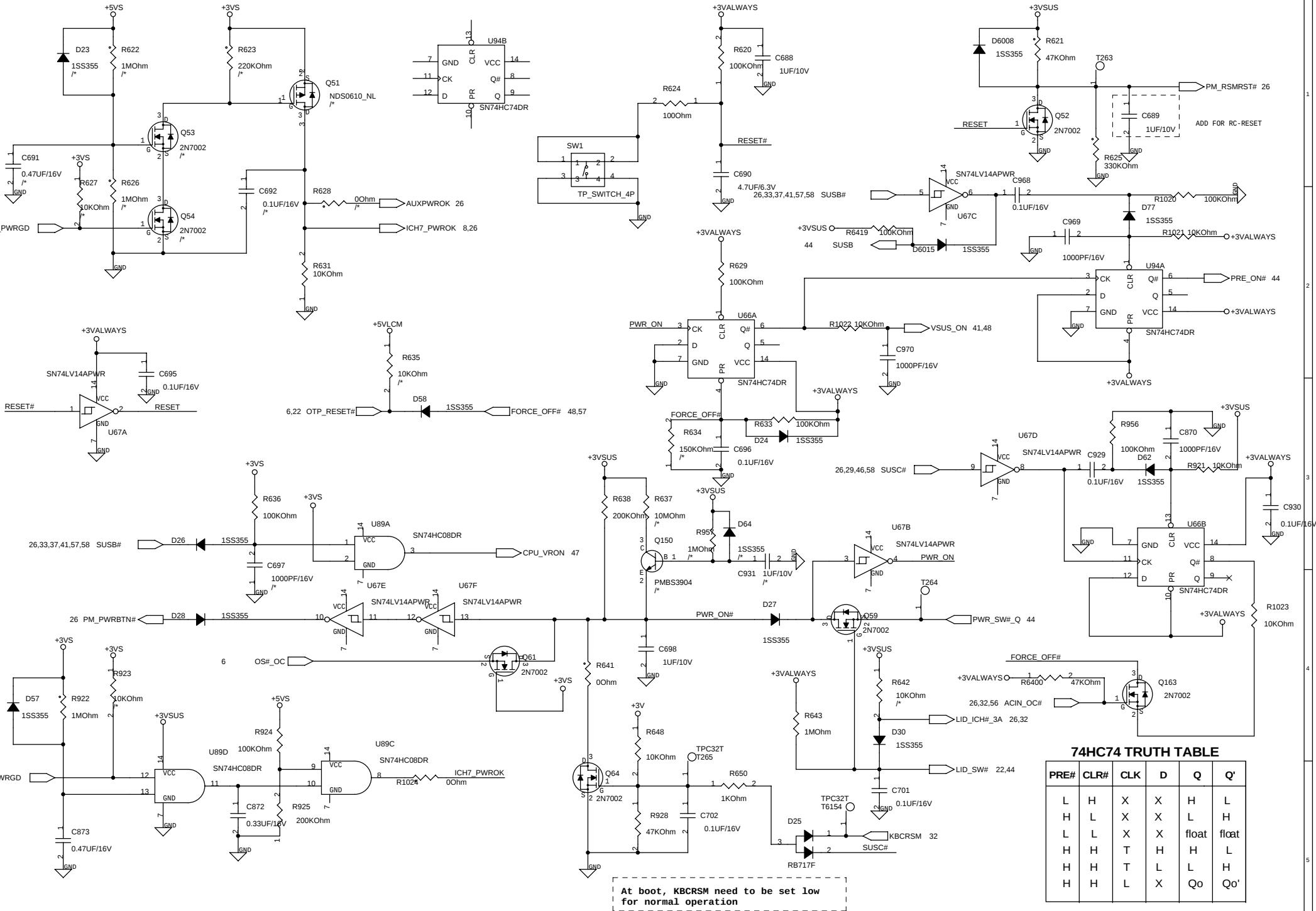
RTC BAT



DC-IN

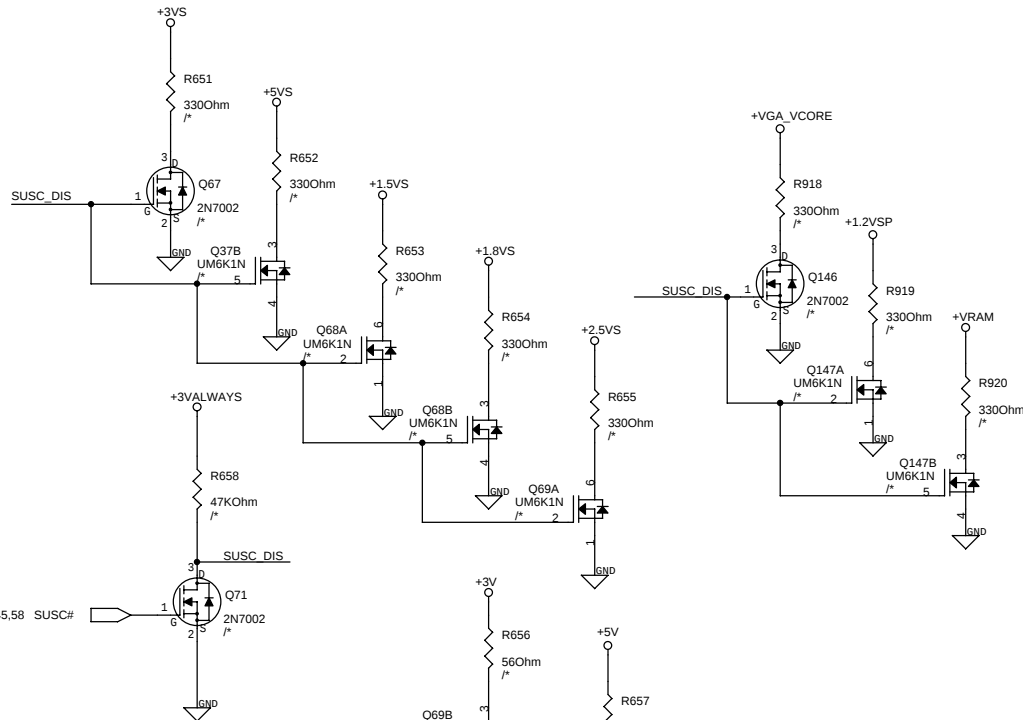






74HC74 TRUTH TABLE

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'



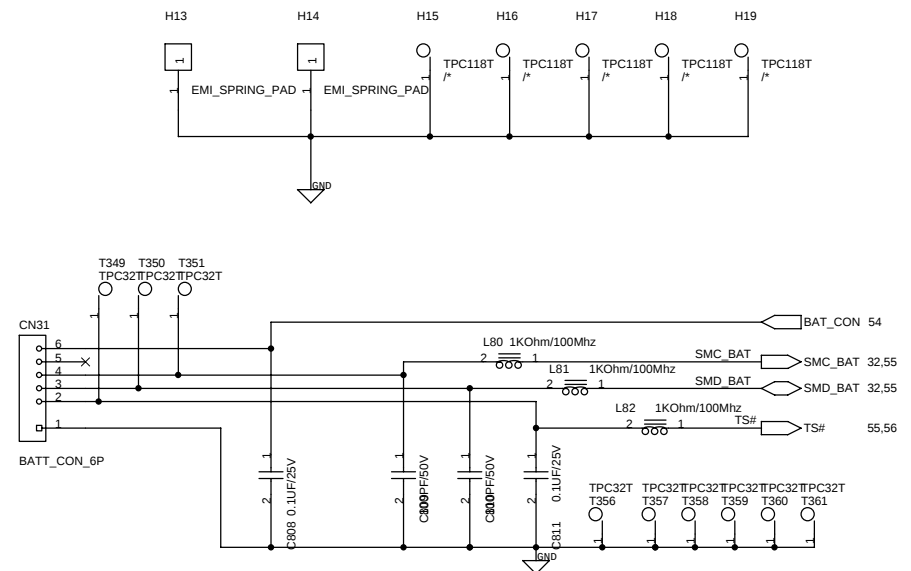
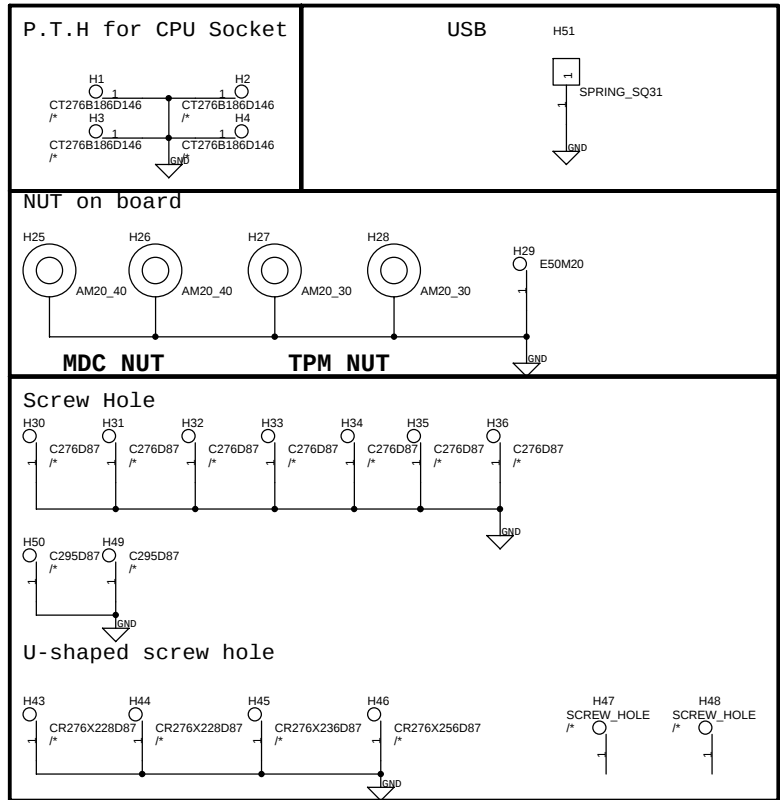
CROSS MOD

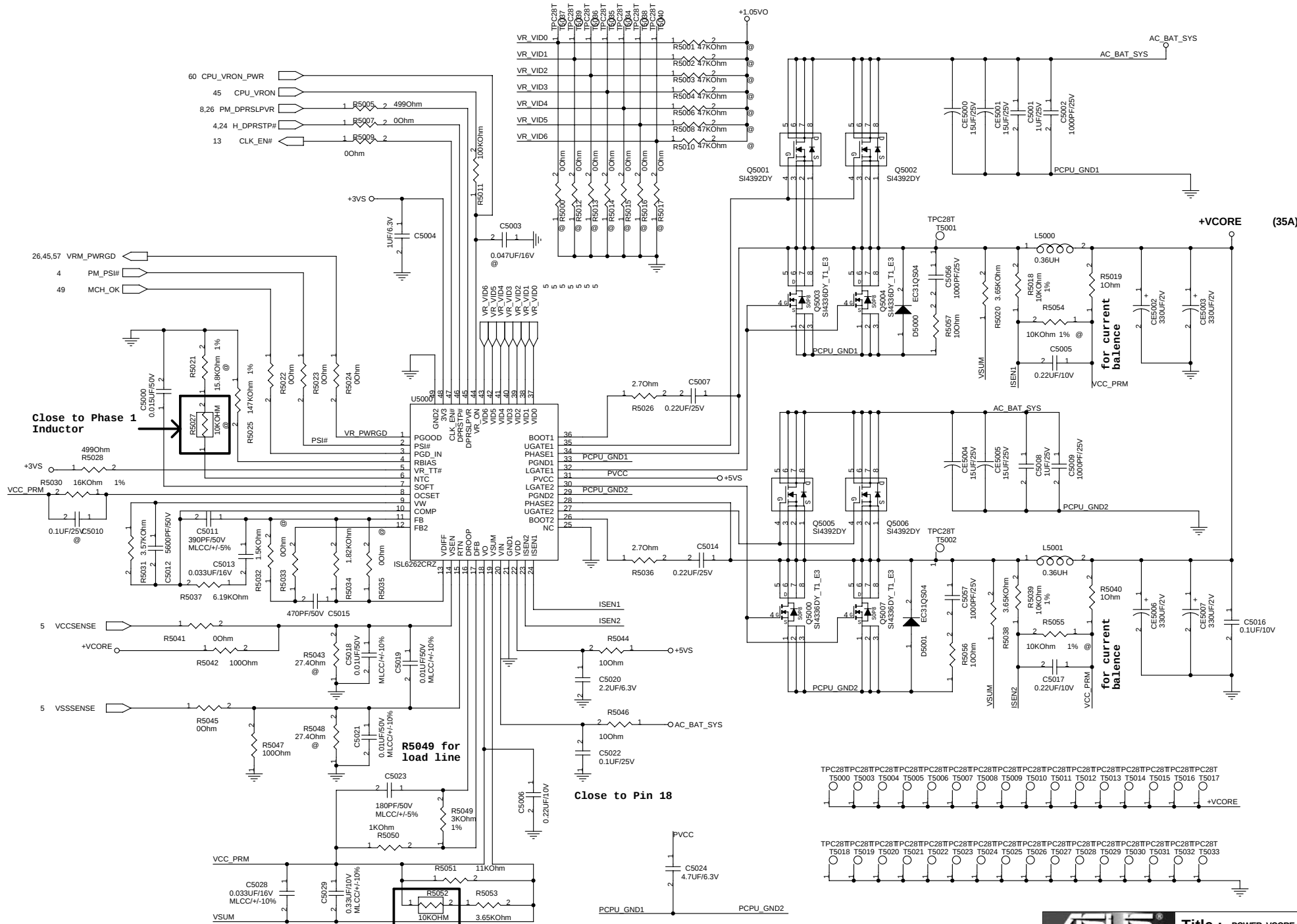
+1.8V C6150 2 1 0.1UF/10V +VGA_VCORE
 +1.8V C6158 2 1 0.1UF/10V +VGA_VCORE
 +1.5VS C6159 2 1 0.1UF/10V +VGA_VCORE
 +1.5VS C6160 2 1 0.1UF/10V +VGA_VCORE

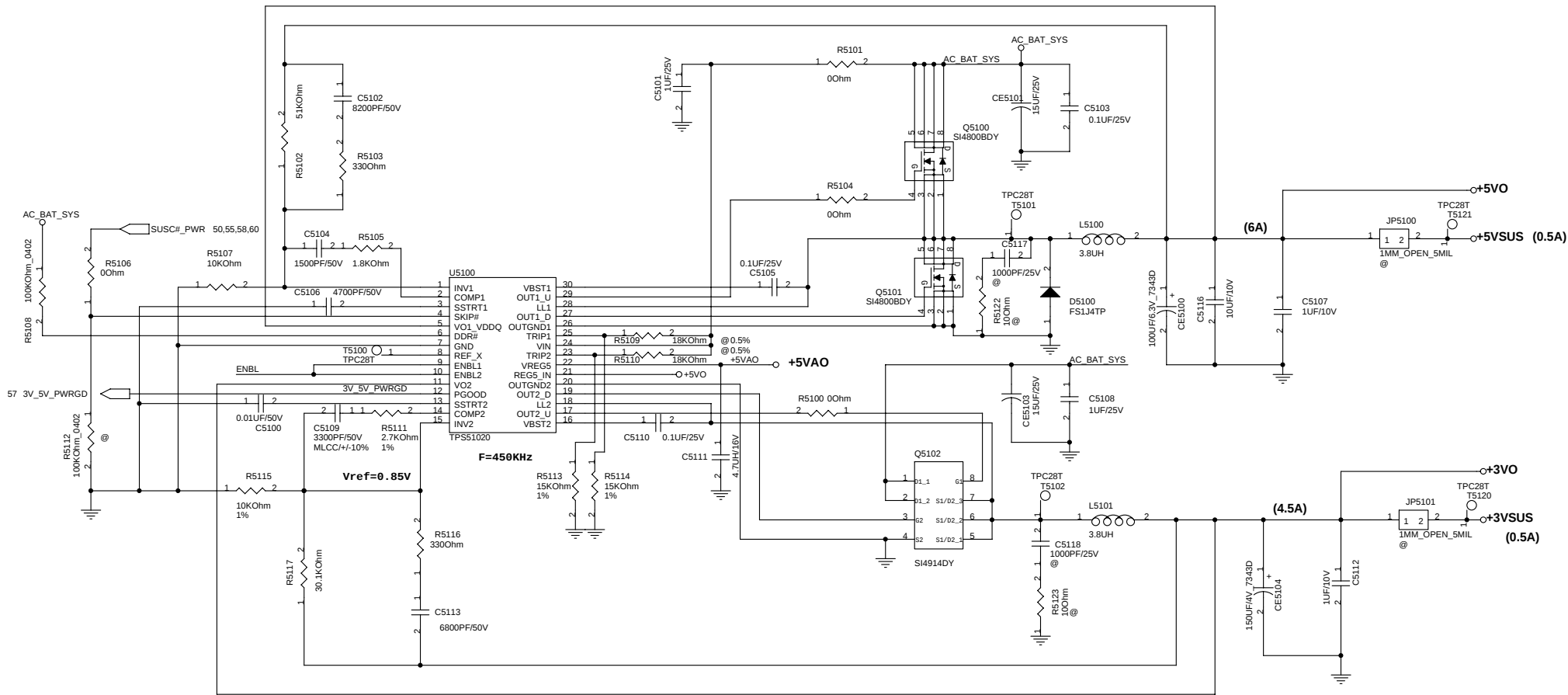
+1.5VS C6152 2 1 0.1UF/10V +1.8V
 +1.8V C6161 2 1 0.1UF/10V +3VS
 +1.8V C6162 2 1 0.1UF/10V +3VS

+1.5VS C6165 2 1 0.1UF/10V +3VS
 +1.5VS C6166 2 1 0.1UF/10V +3VS

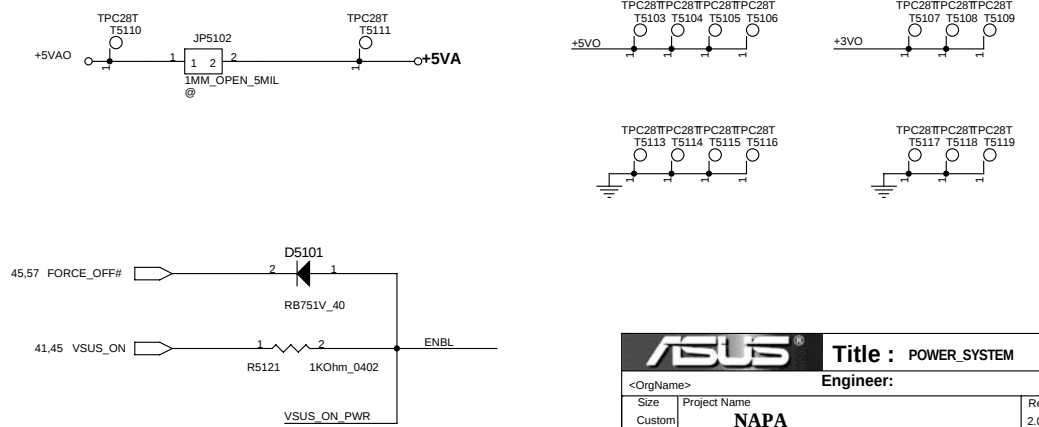
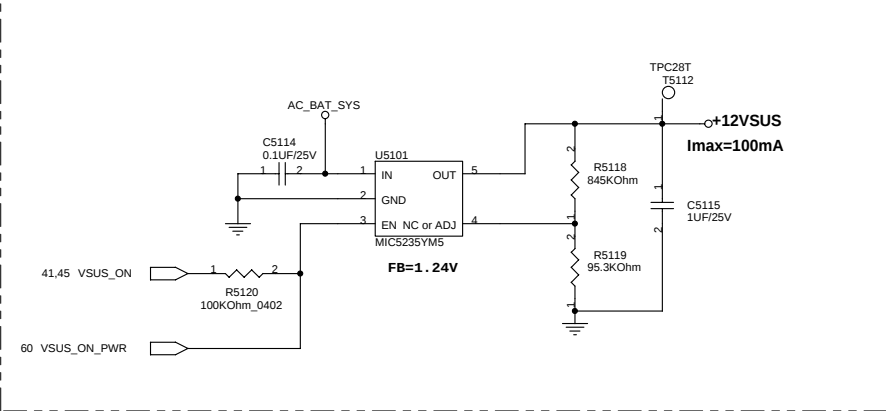
+3VS C6155 2 1 0.1UF/25V AC_BAT_SYS
 +3VS C6167 2 1 0.1UF/25V AC_BAT_SYS
 +VCCP C6156 2 1 0.1UF/25V AC_BAT_SYS
 +VCCP C6168 2 1 0.1UF/25V AC_BAT_SYS
 +VCORE C6169 2 1 0.1UF/25V AC_BAT_SYS

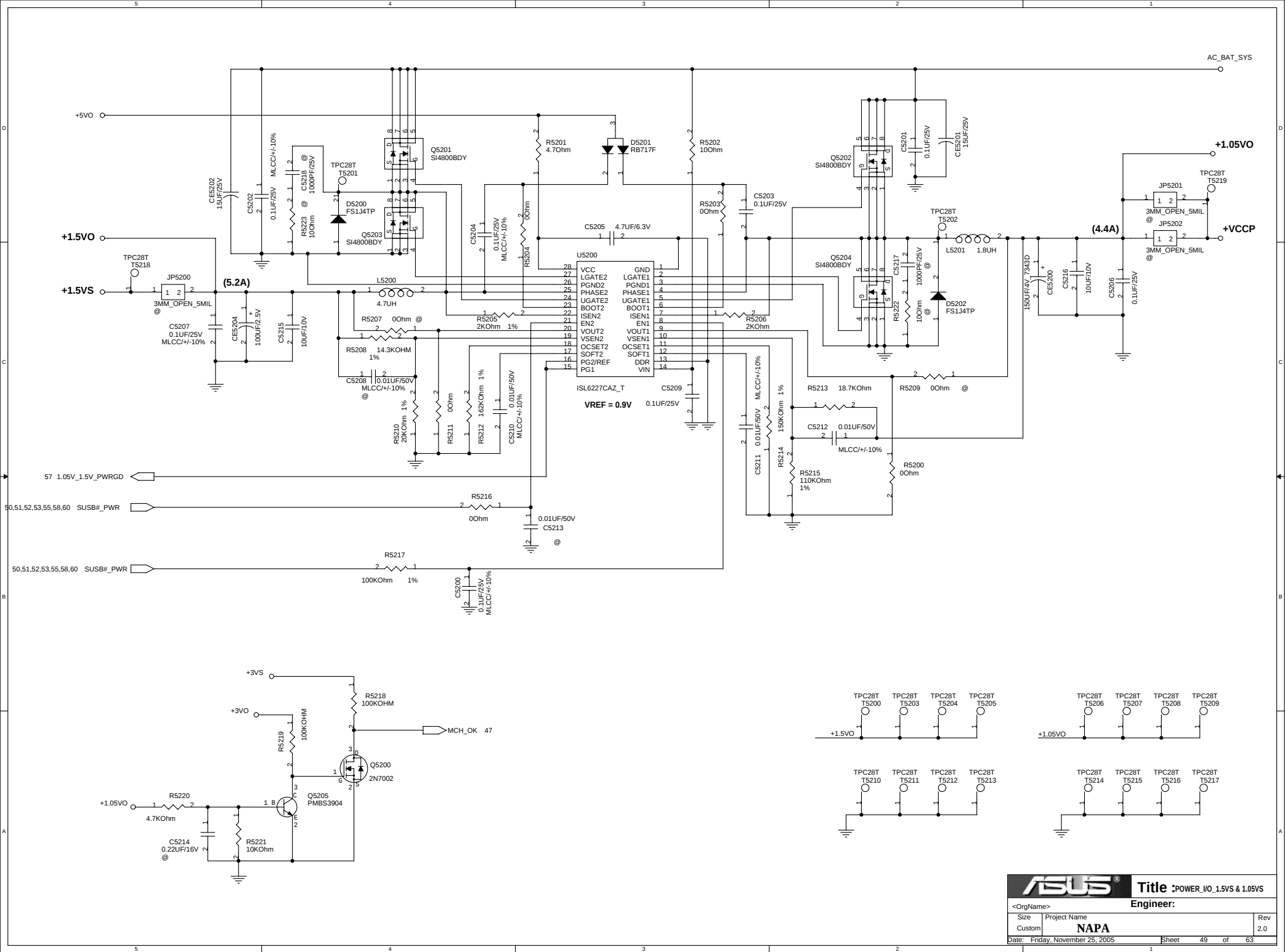


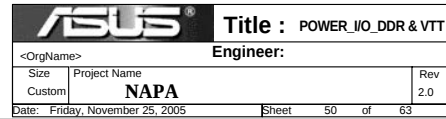




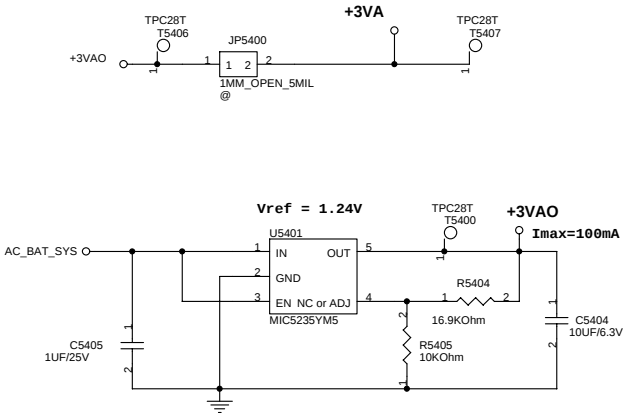
+12VSUS



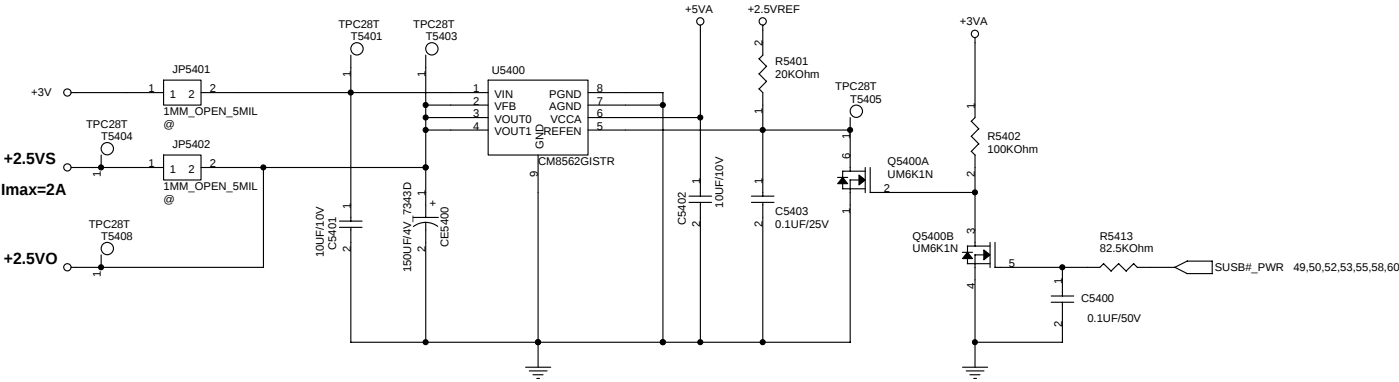


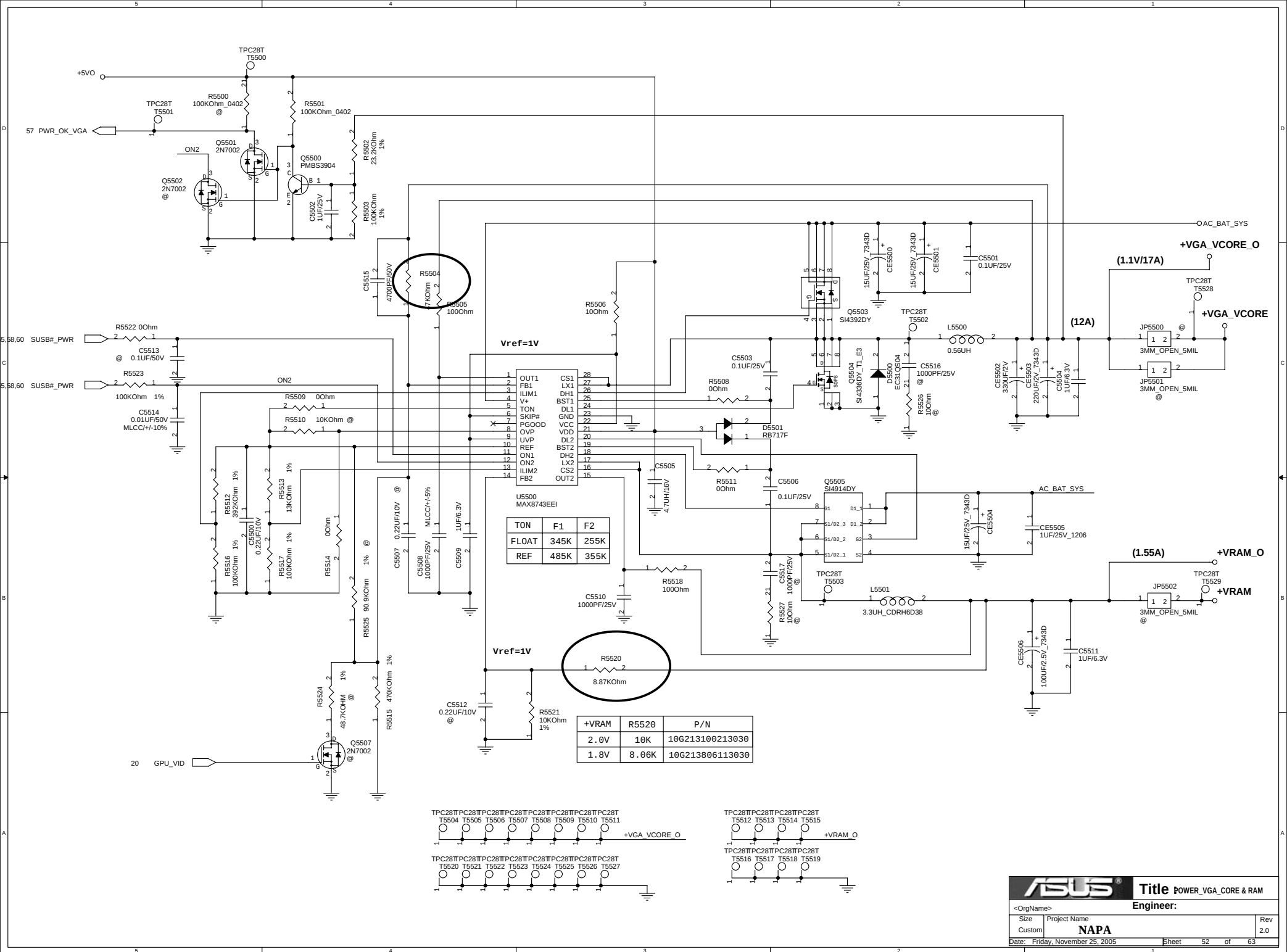


+3VA0

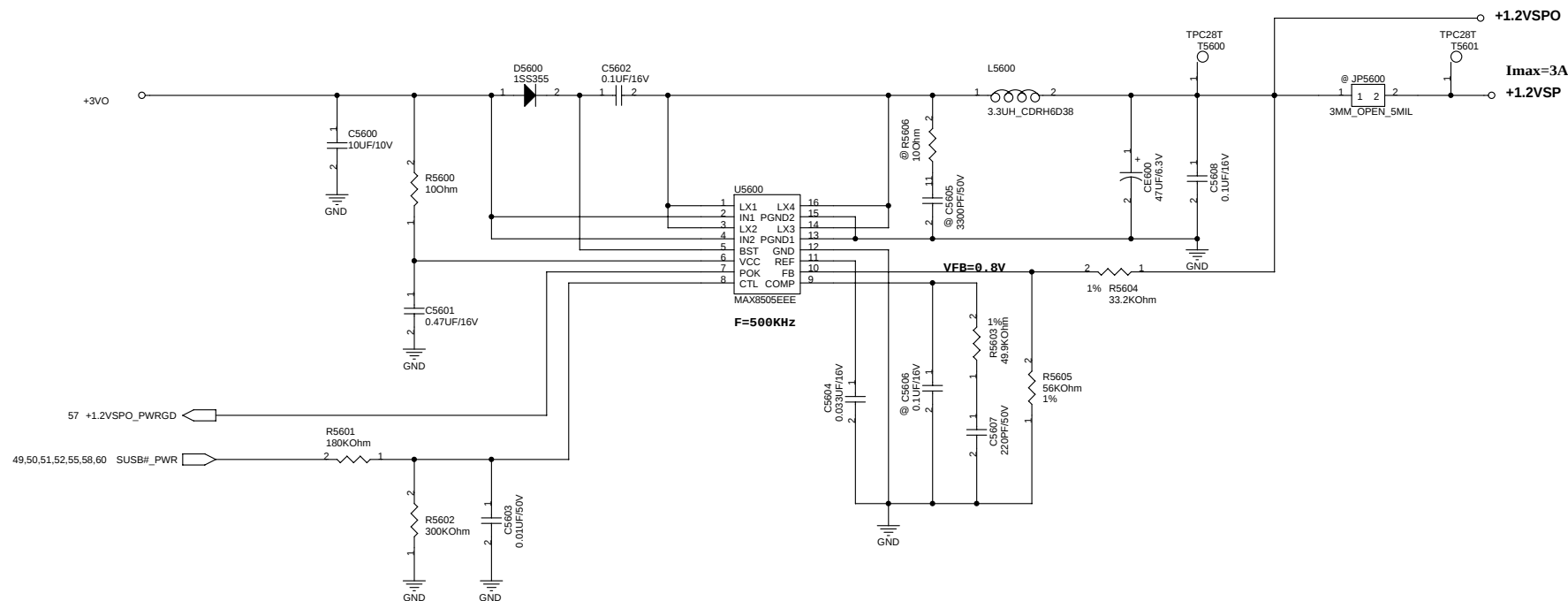


+2.5VS



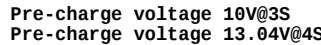
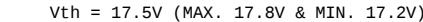


+1.2VSP

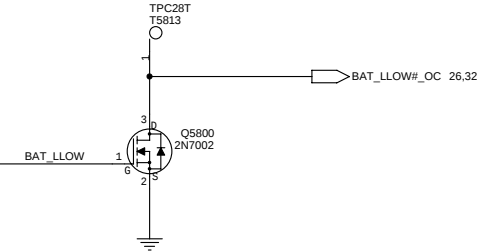
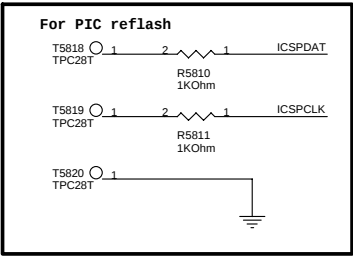
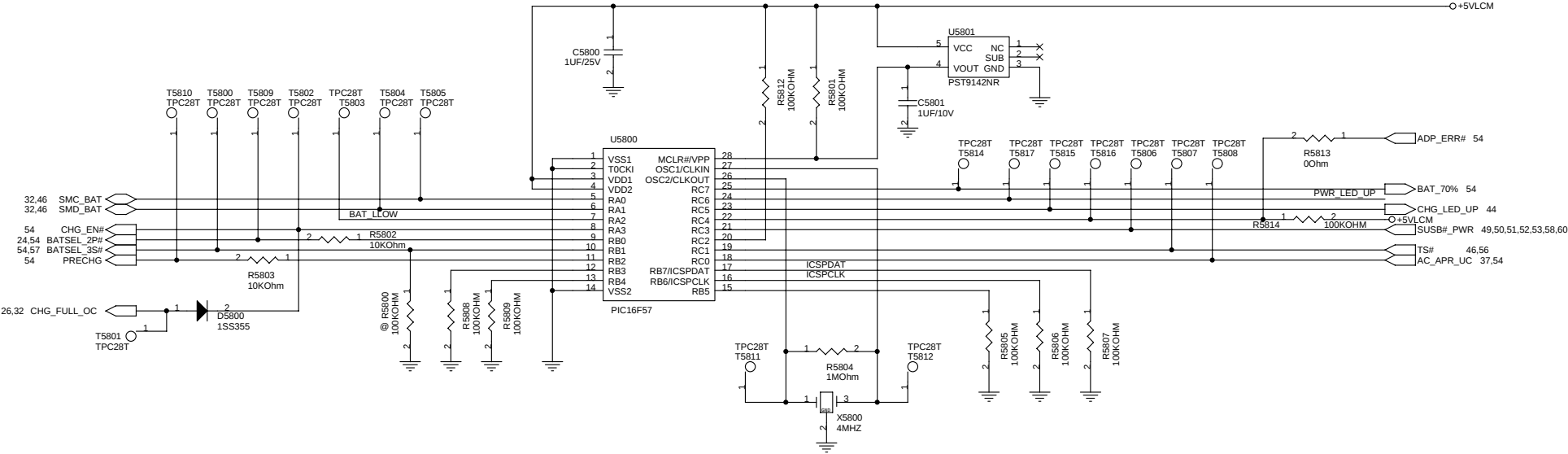


- - > 3.42A

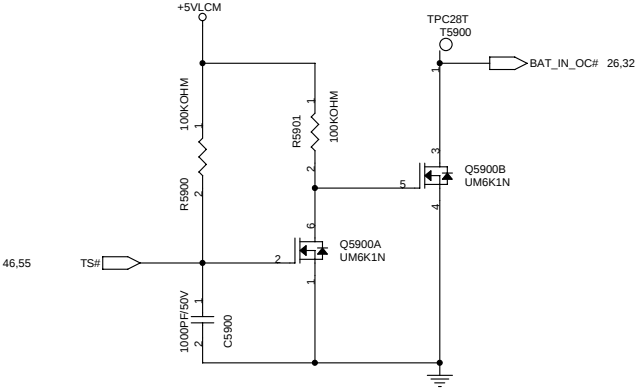
Charge Current $I_{chg} =$
 $[0.075V/R_{sense}(CHG)] \cdot [V_{CLS}/4.096V]$
 $R_{sense}(CHG) = 0.025 \text{ ohm}$
 $V_{CTL} = 3.4632V \Rightarrow I_{chg} = 2.53A$



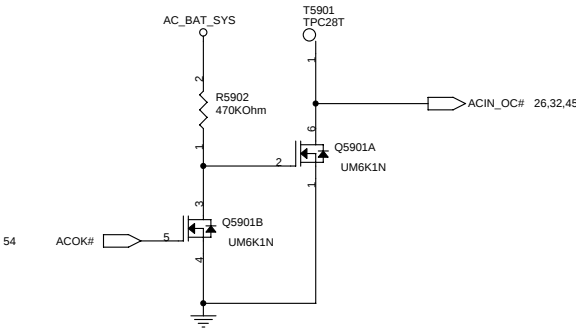
PIC16F57



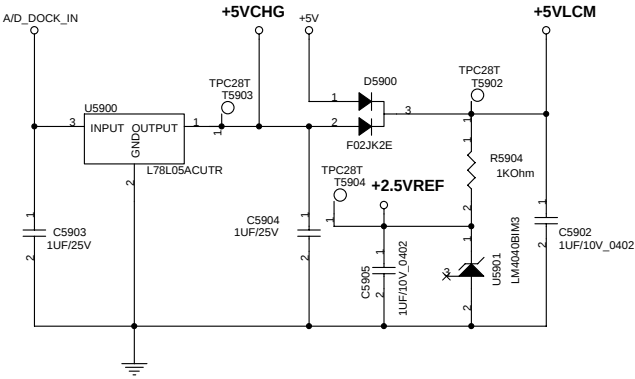
BATTERY IN DETECT



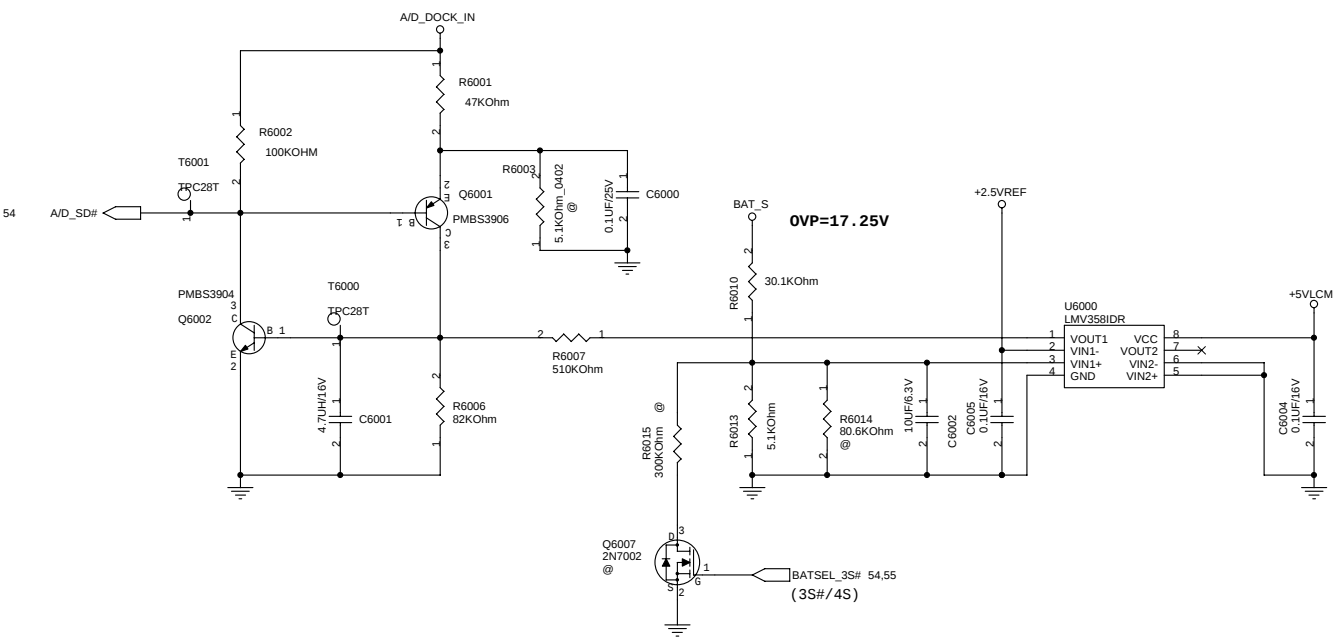
ADAPTER IN DETECT



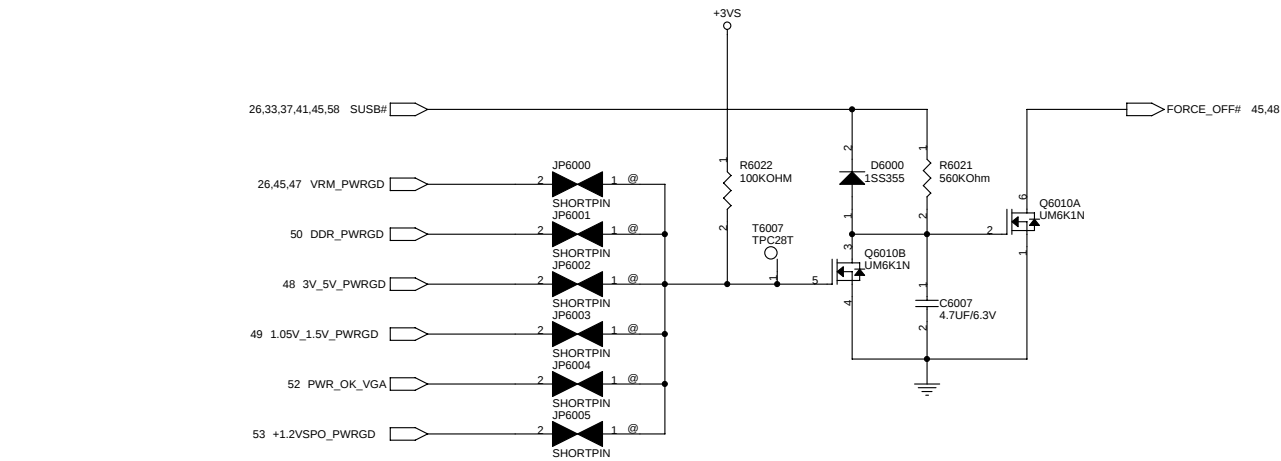
+5VLCM, +5VCHG & +2.5VREF



BATTERY A/D_SD# (OVP)

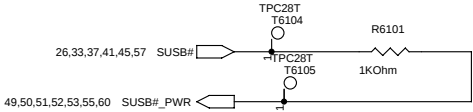
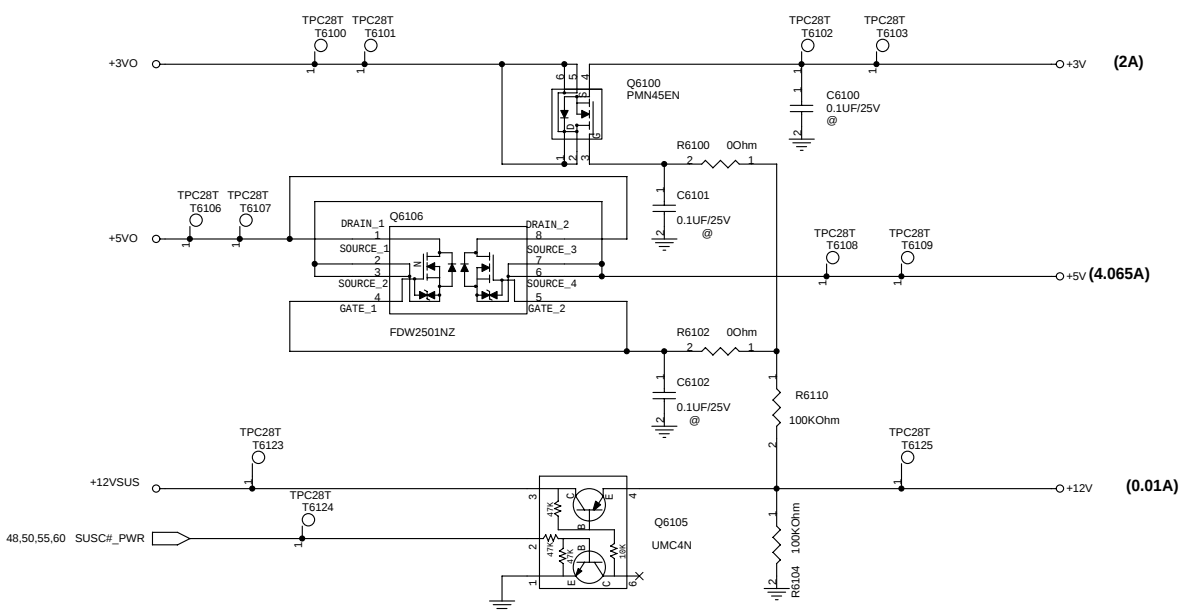


POWER GOOD DETECTOR

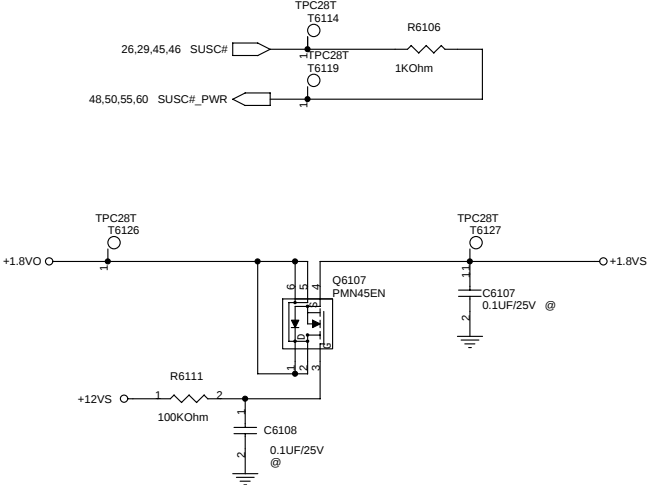
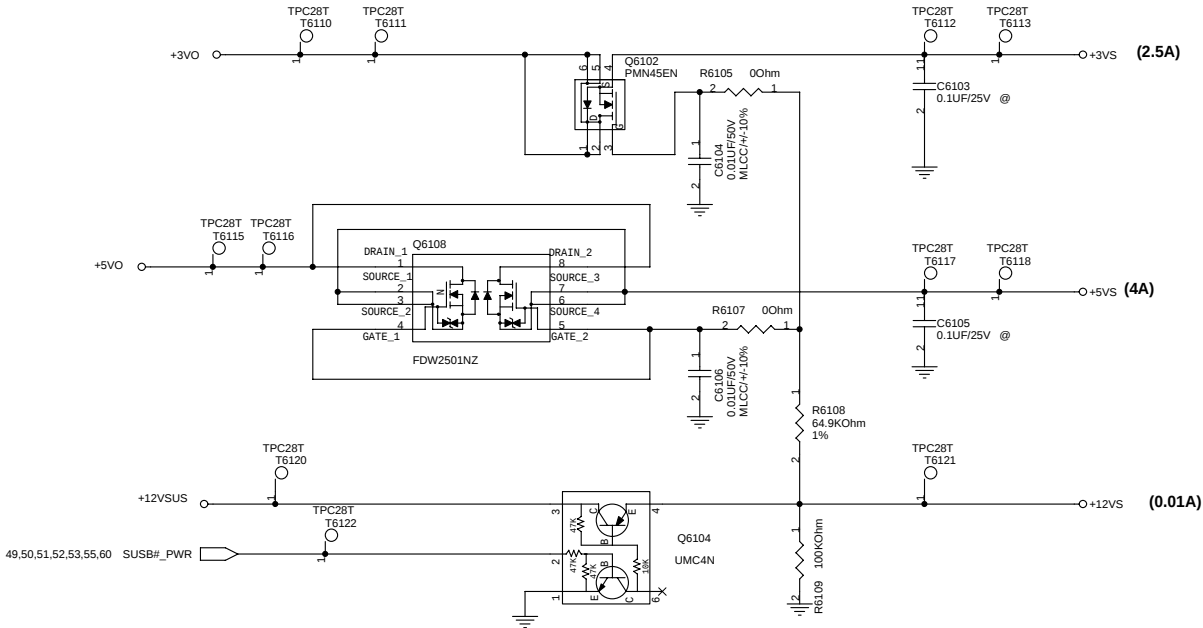


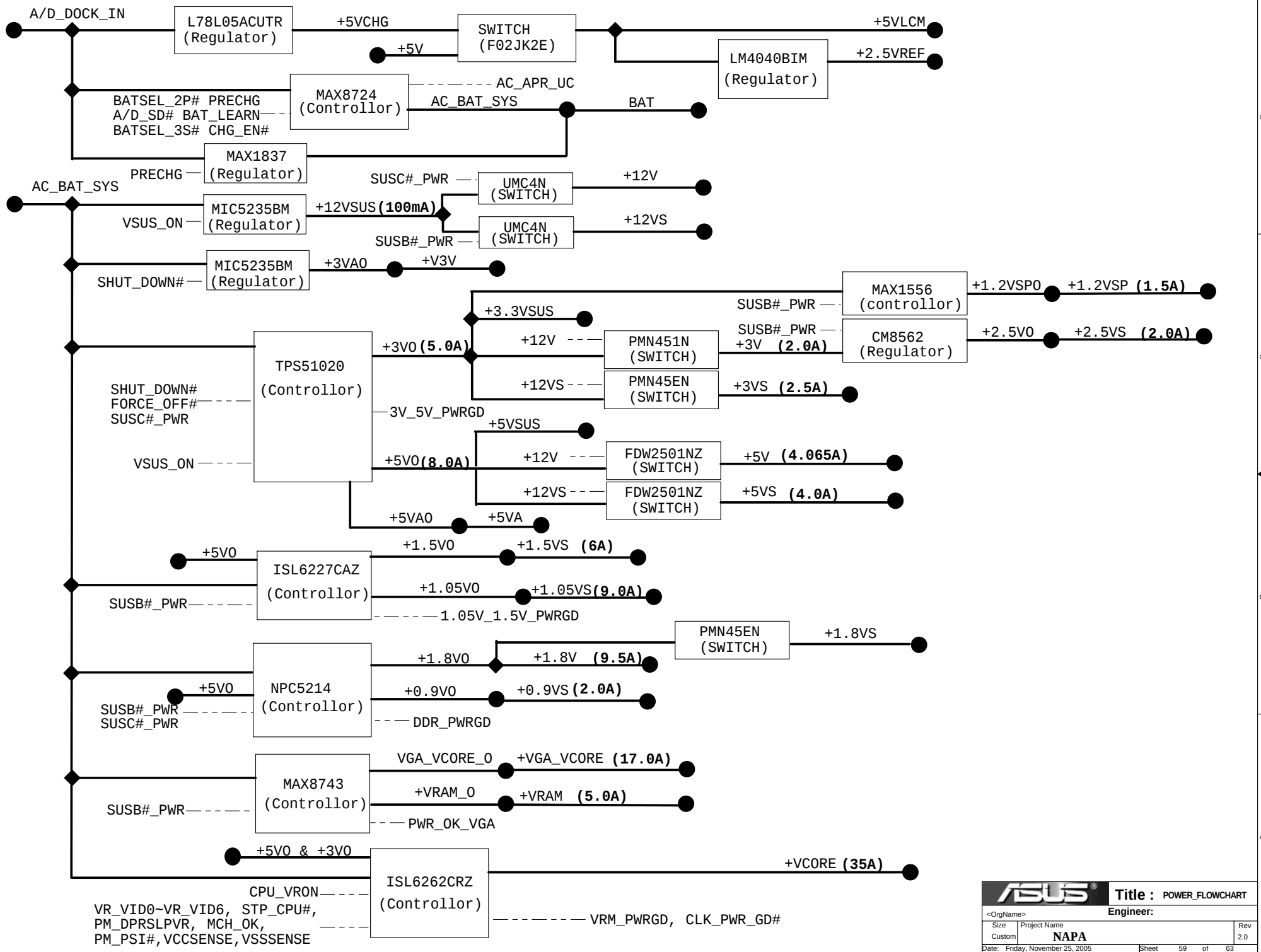
- TPC28T T6003 1 VRM_PWRGD
- TPC28T T6004 1 DDR_PWRGD
- TPC28T T6005 1 3V_5V_PWRGD
- TPC28T T6006 1 1.05V_1.5V_PWRGD

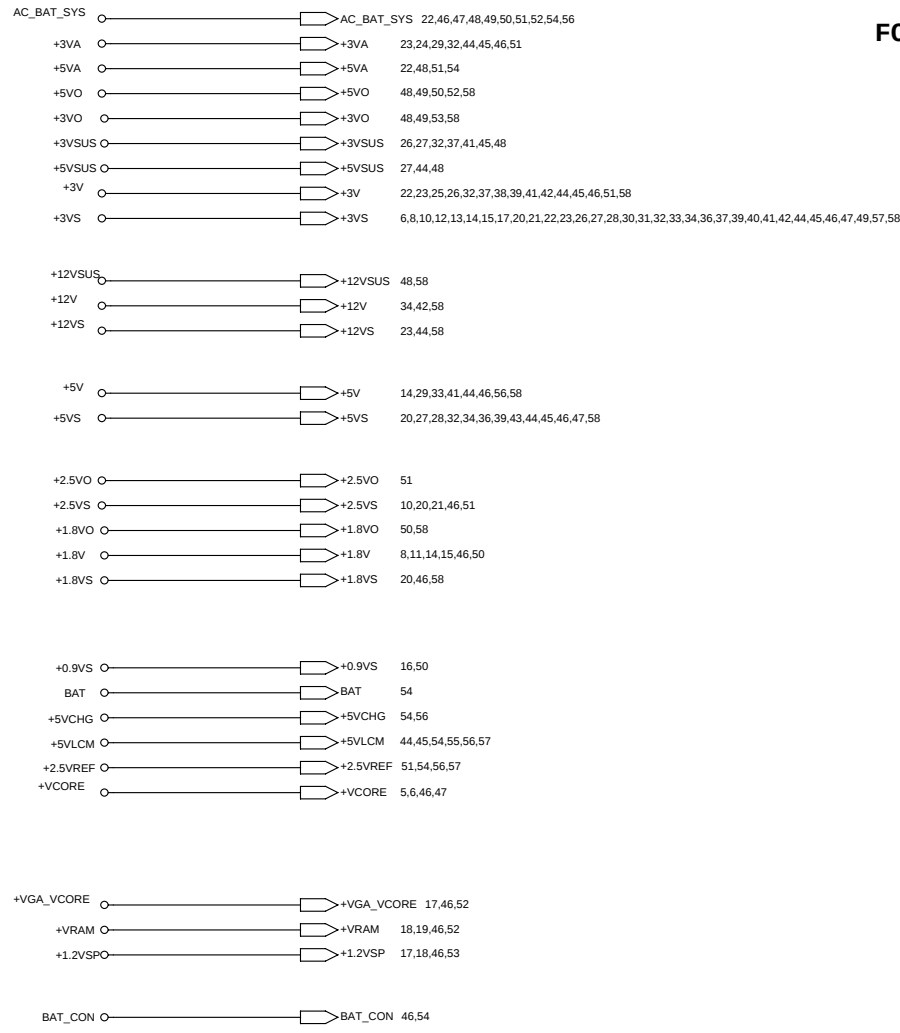
SUSC#_PWR POWER



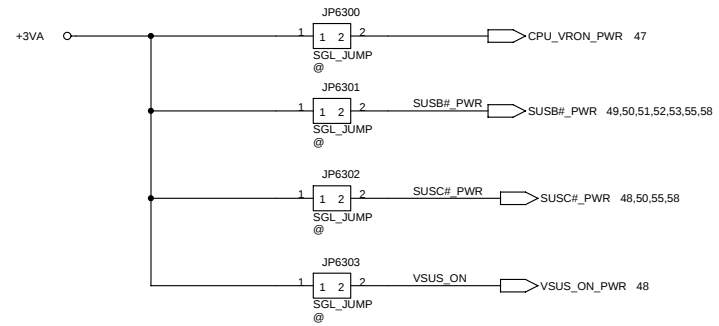
SUSB#_PWR POWER







FOR POWER TEST



Revision History

V1.0 to V1.1

- 1. D58 change from DAP202 to 1ss355
- 2. Panel detection chagne from PID to EDID method.
- 3. Reserve panel dectection by PID method.
- 4. Tuning power sequence by power circuitry.
- 5. TP_MA_RCVEN* net can't connect with TP_MB_RCVEN*, so cut it.
- 6. CPU address A14 and A15 is swap for booting.
- 7. Populate R6347 = R6348 =120 Ohm by nVIDIA recommend.
- 8. Change VGA chip from G72M-V to G72M, so change device ID strapping.
- 9. CHG_FULL_OC net has doubled pull-up to +3vs and +3vsus, so remove +3vsus pull-up for leakage.
- 10. CLK_EN# pull-up to +3vs will has leakage current from cpu vcore controller. so remove it.
- 11. Lan chip reset signal has leakage current output to system reset signal, so add D6006 to solve it.
- 12. +1.5VS power trace is too small from source to calistoga IC, so increase trace width.
- 13. Remove R639 because system has no shutdown signal from POWER.
- 14. R638 change to 200k and C698 change to 1uF for power on button feeling.
- 15. CF618, 16, 15 has wrong connection, correct it.
- 16. C138=C139=22pF for tunning 14.318MHz crystal freauency.
- 17. RN15 pin 2 pull-up power change from +3V to +3VS for solving leakage current at S3 state.
- 18. Change audio circuitry for solving pop noise.
- 19. Change pci-express decoupling caps from 0.1uF/Y5V to 0.1uF/X5R.
- 20. Microphone pull-up power source change to OP AMP generate.
- 21. R287=0 Ohm and R290 remove for G72M need +3VS level input about 27MHz spread spectrum input pin.
- 22. MAX6649 be used on G72M has wrong connection, so correct it.
- 23. Populate R574=0 Ohm for XD card work fine.
- 24. Remove R6360, R6361, R6358, R6359 for JTAG pin pull-up/down on G72M.
- 25. Populate C563, C566 for improve microphone quality.
- 26. Add D6008 for PM_RSMRST# discharge quickly.
- 27. Tunning C141~C146, R128, C490 value base on EVT report about clk signal quality issue.
- 28. Add ODD disable function support.

V1.1 to V2.0

- 1. Calistoga CRT disable guide change, so IREF pin connect to power directly.
- 2. Add circuitry for newcard disable support.
- 3. R381 change to 1K Ohm for ODD disable support.
- 4. Reserve newcard type debug card support circuitry.
- 5. Add mini card type debug card support circuitry.
- 6. MAX6649 be used on G72M change to MAX6657.
- 7. Add TPM connector debug card support.
- 8. The reset signal of lan chip pull-down 10K Ohm.
- 9. RTCRST# delay time control add diode for quick discharge.
- 10. Populate R6351, C? for solving led will flash once when system power on.
- 11. Add usb spring and beas on agnd and dgnd for EMI request.
- 12. Disable audio jack sense feature.
- 13. Add Q6130 for 1HZ flash



PROJECT: V6J

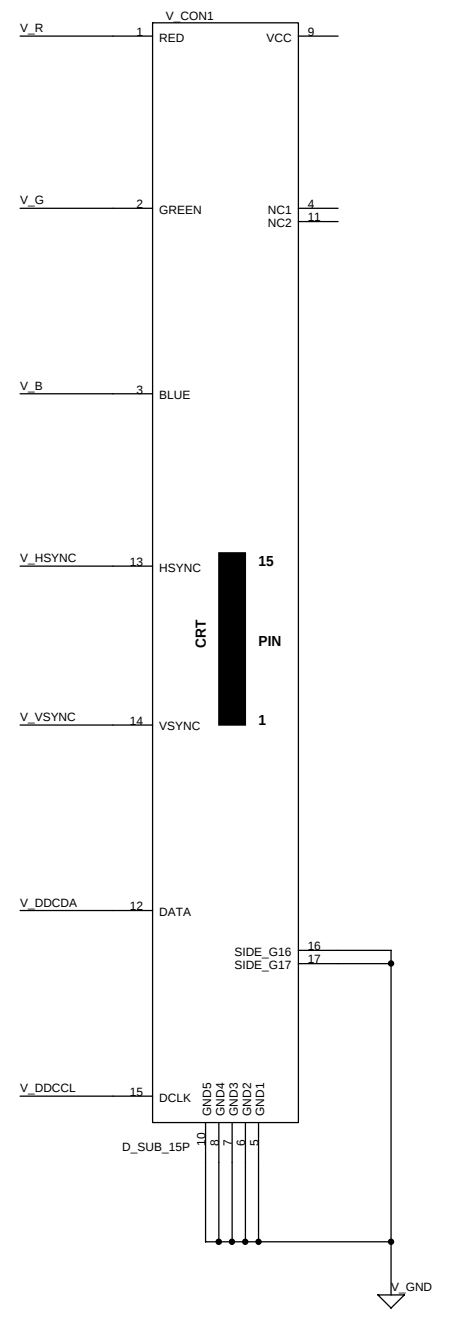
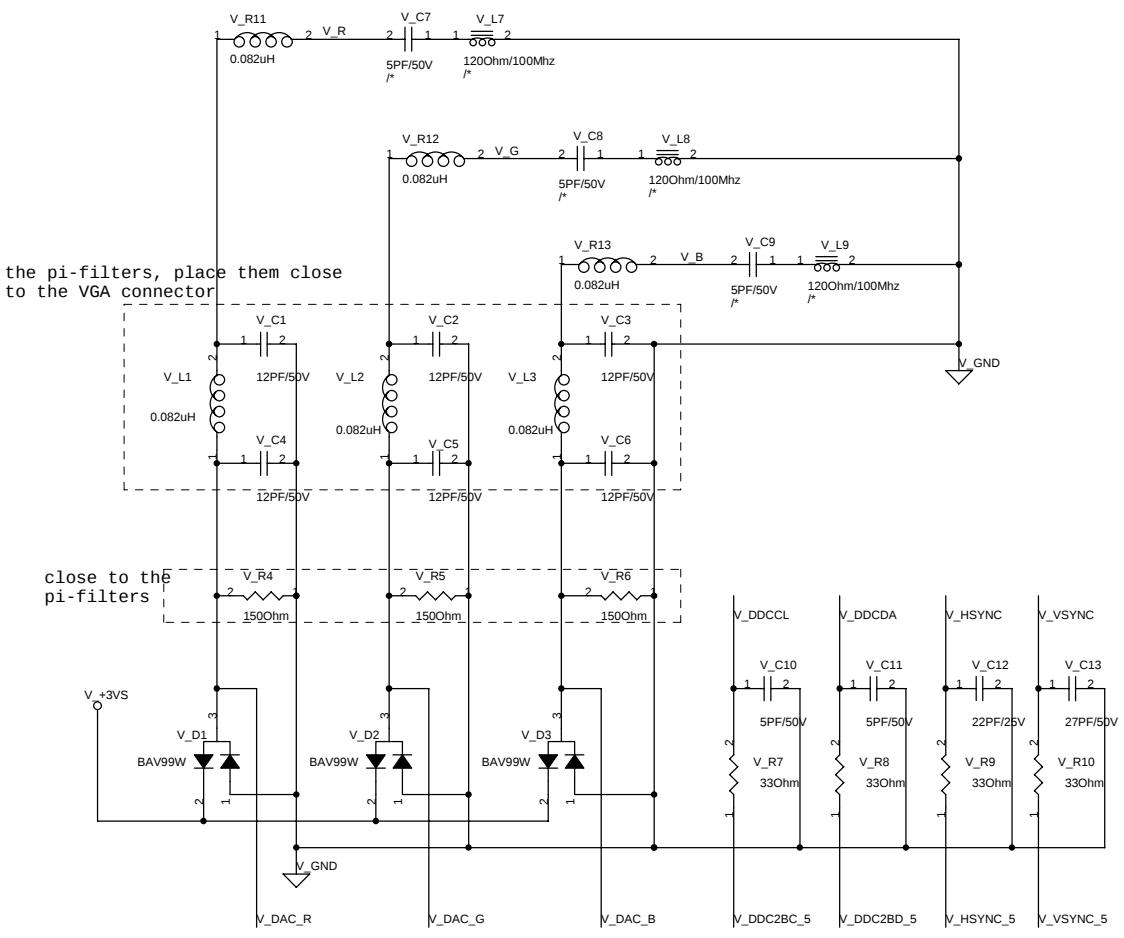
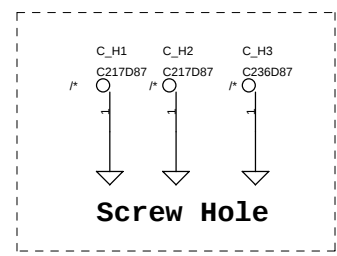
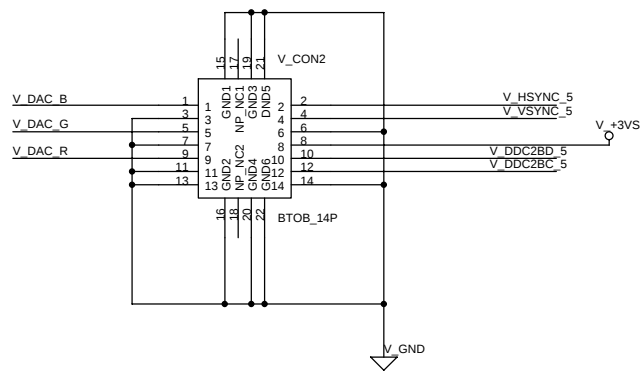
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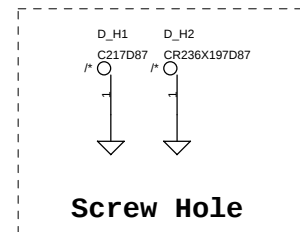
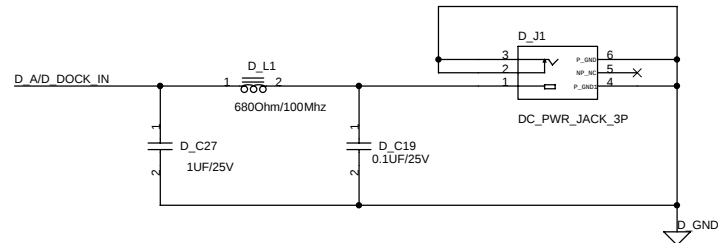
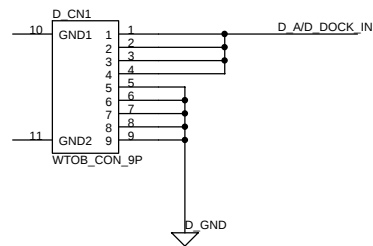
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SHEET 61 OF 63

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Content

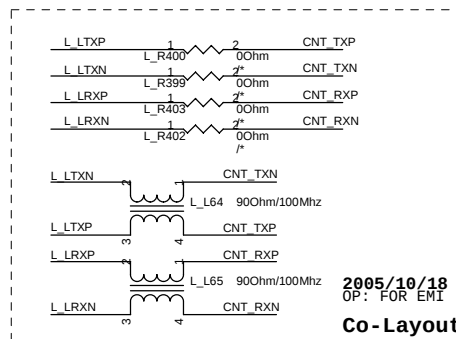
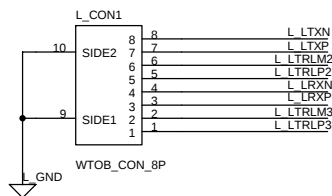
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RELEASE DATE :

DESIGN ENGINEER :
Feng Lin



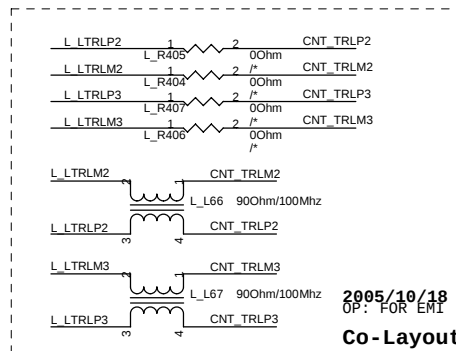


Screw Hole



2005/10/18
OP: FOR EMI

Co-Layout



2005/10/18
OP: FOR EMI

Co-Layout

