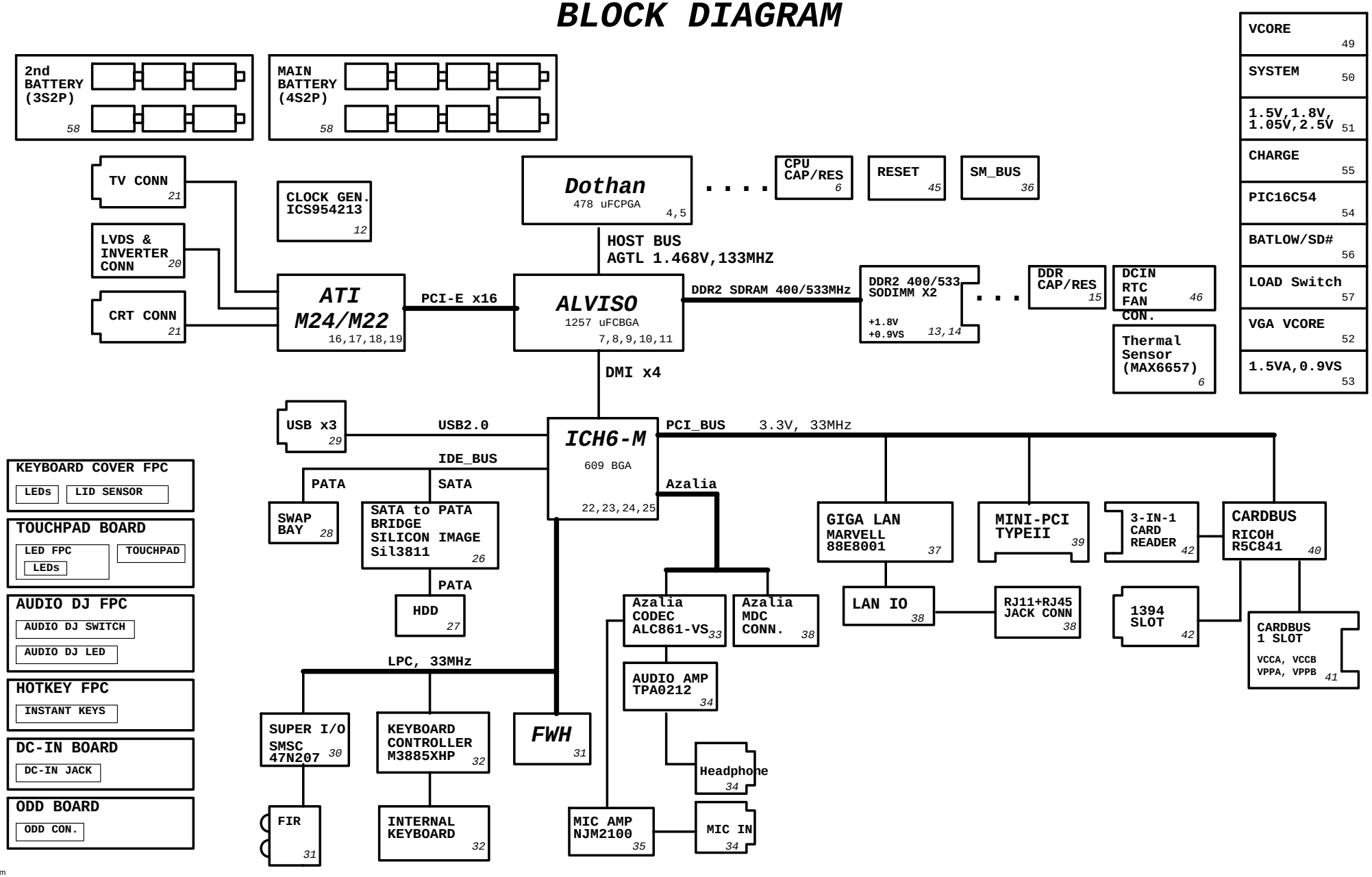
W3V/A SCHEMATIC V2.1

bom

PROJECT: **W3V**	REVISION: 2.1	DATE: Monday, January 17, 2005	DESCRIPTION: ***Content & History***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Alice Shih***
		SHEET 1 OF 63		RELEASE DATE :	

W3V/A:Dothan & Alviso-PM+M24-CSP/Alviso-GM
BLOCK DIAGRAM



bom

PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Alice Shih
		SHEET 2 OF 63		RELEASE DATE :	

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	C	
CardBus	AD17	1	B	
1394	AD17	1	A	
3 IN 1		1	C	

Azalia : PCI_INTB#
USB 0,1 : PCI_INTA#
USB 2,3 : PCI_INTD#
USB 4,5 : PCI_INTC#

SMBUS ADDRESS :

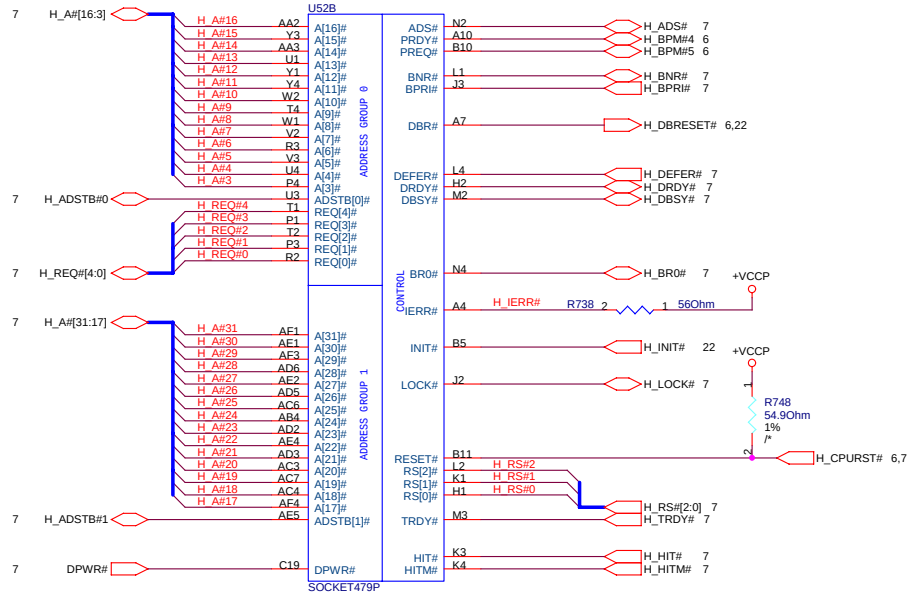
CLK = 1101001x (D2)
DDR_SODIMM0 = 1010010x (A4)
DDR_SODIMM1 = 1010000x (A0)
THERMAL = 1001100x (98)

ICH6M_GPIO	Used As	Signal Name
GPIO00	GPI	KBDDT0
GPIO01	GPI	KBDDT1
GPIO06	GPI	PM_BMBUSY#
GPIO07	GPI	FIR_SEL
GPIO08	GPI	EXTSMI#_3A
GPIO11	GPI	LID_ICH#_3A
GPIO12	GPI	KBDSCI_3
GPIO13	GPI	ATI_OVERTEMP#
GPIO14	GPI	GPI14
GPIO15	GPI	CHG_EN#_OC
GPIO16	GPO	GPO16
GPIO17	GPO	GPO17
GPIO21	GPO	BACK_OFF#
GPIO23	GPO	FWH_WP#
GPIO24	GPO	CB_SD#
GPIO25	BLINK	ICH6_1HZ
GPIO26	GPI	SATA_DET_#0
GPIO27	GPI	PCB_VID0
GPIO28	GPI	PCB_VID1
GPIO29	GPI	PCB_VID2
GPIO30	GPI	SATA_DET_#2
GPIO31	GPI	AGP_EXT
GPIO33	GPO	XIDE_EN#_3
GPIO34	GPO	OP_SD#
GPIO40	GPI	PID0
GPIO41	GPI	PID1

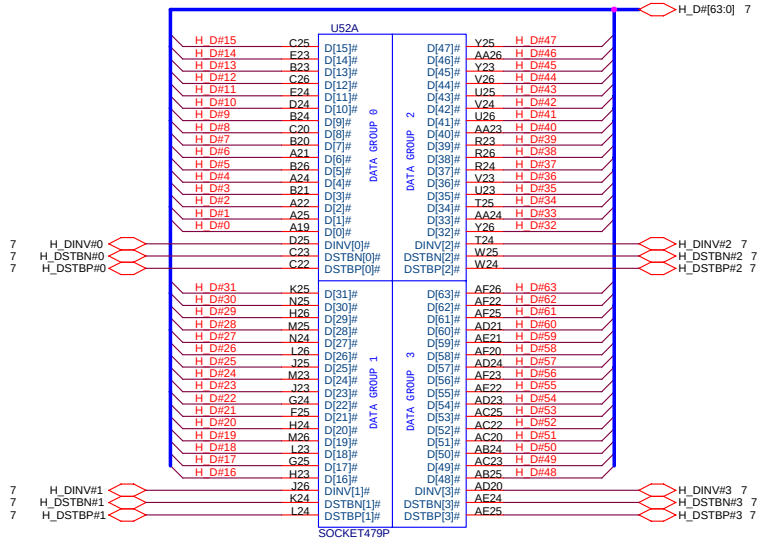
M38857_GPIO	Used_As	Signal_Name
P20	GPO	KBCRSM
P21	GPO	BAT_SEL
P22	GPO	BAT_LEARN
P23	GPO	MSK_INSTKEY#
P42	GPO	WATCHDOG
P43	GPI	SWDJ_EN#
P44	GPO	KBCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LLOW#_KBC
P51	GPO	DJ_LED_EN
P52	GPO	WIRELESS_LED#
P53	GPO	BAT_LOW#_KBC
P54	GPI	BAYDOCK_IN#
P55	GPI	BAT1_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	BT_#
P61	GPI	INTERNET_#
P62	GPI	CPUFAN_SPD_A
P63	GPI	WIRELESS_#
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPO	PANLOCK_#
P67	GPI	BAT2_IN#_OC
P76	GPIO	SMD_BAT_KBC
P77	GPO	SMC_BAT_KBC

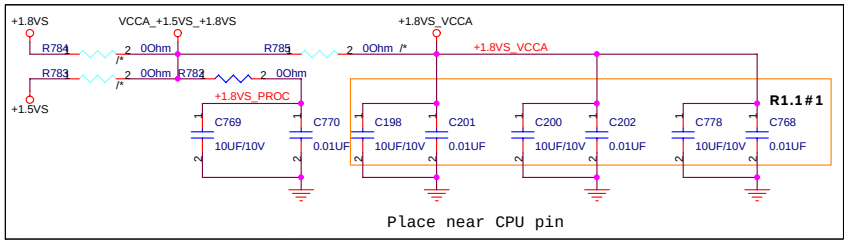
M38857_GPIO	Used_As	Signal_Name
P27	GPO	--
P26	GPO	NUM_LED#
P25	GPO	CAP_LED#
P24	GPO	SET_PCIRSTNS#
P41	GPO	BT_LED#
P40	GPO	KBC_EXTSMI

47N207_GPIO	Used_As	Signal_Name
GP10	GPI	BAY_IN0
GP11	GPI	BAY_IN1
GP12	GPI	--
GP13	GPI	SW_RST#
GP14	GPIO	--
GP15	GPO	BAY_RST
GP16	GPO	DJKEY_EN
GP17	GPO	802_EN#
GP34	GPO	OVER_CLK1
GP35	GPO	OVER_CLK2
GP36	GPO	--

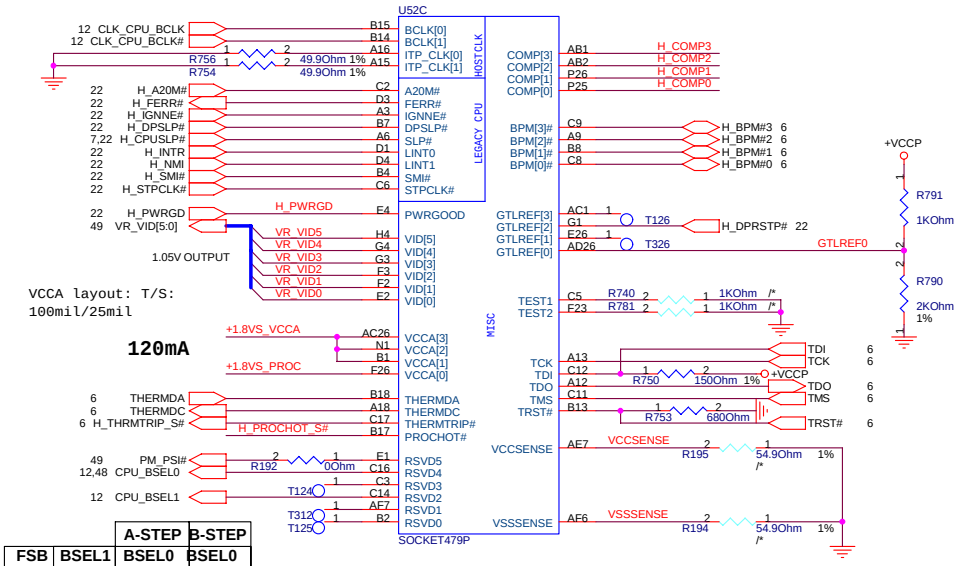


P/N = 12-046004791



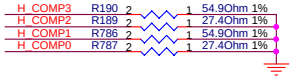


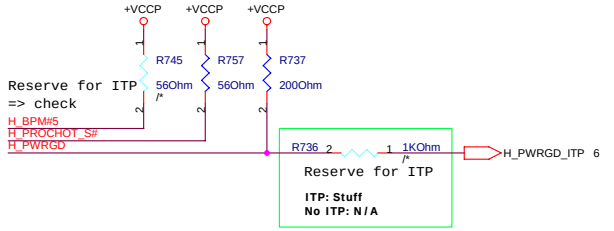
Place near CPU pin



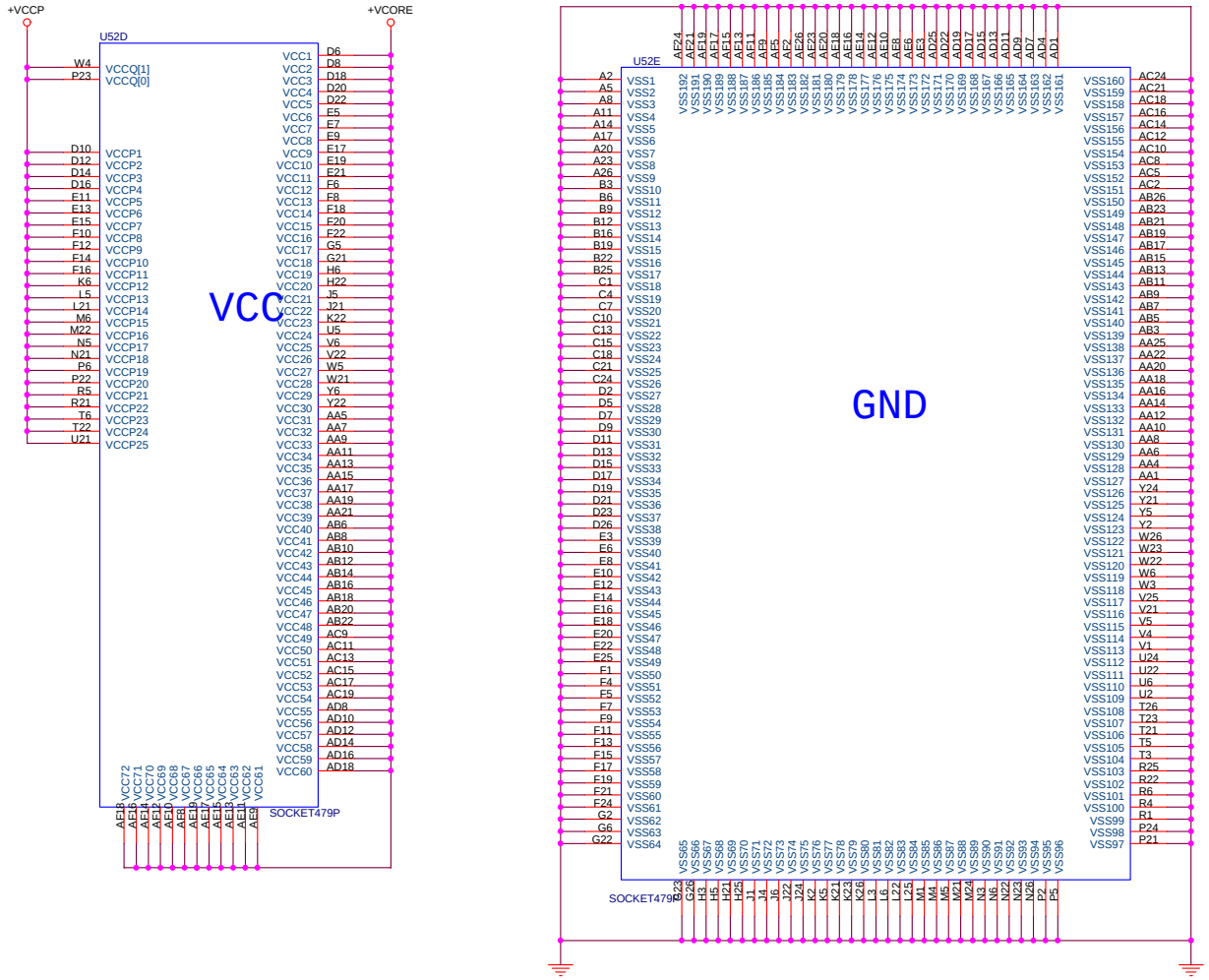
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"





PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 4 OF 63	DESCRIPTION: DOTHAN CPU(1)	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : M.Y.



Mobile Dothan VID Table

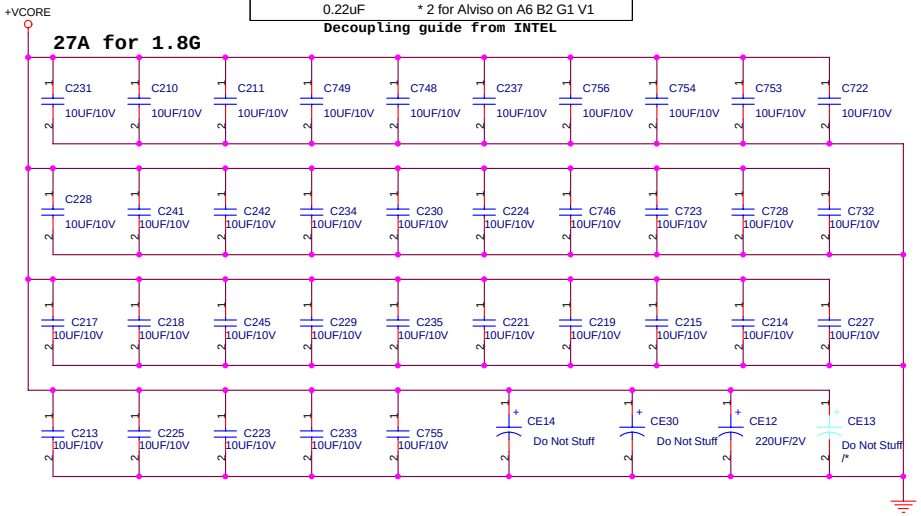
VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

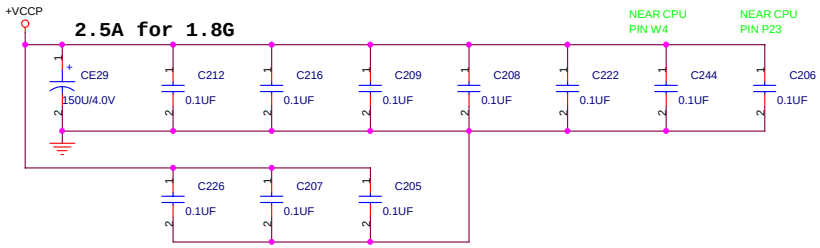
bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***DOTHAN CPU (2)***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***M.Y.***
		SHEET **5** OF **63**		RELEASE DATE:	

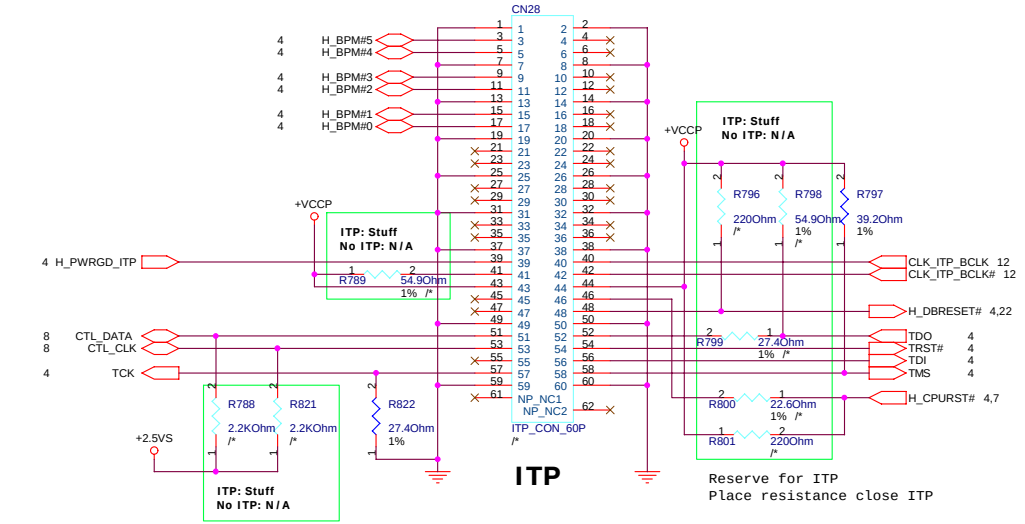
VCORE 10uF/10V * 35
220uF/2V * 4
VCCP 0.1uF * 10 for CPU
150uF * 1 for CPU
0.1uF * 10 for Alviso
150uF * 2 for Alviso
4.7uF * 1 for Alviso
2.2uF * 1 for Alviso
0.47uF * 2 for Alviso on A6 B2 G1 V1
0.22uF * 2 for Alviso on A6 B2 G1 V1

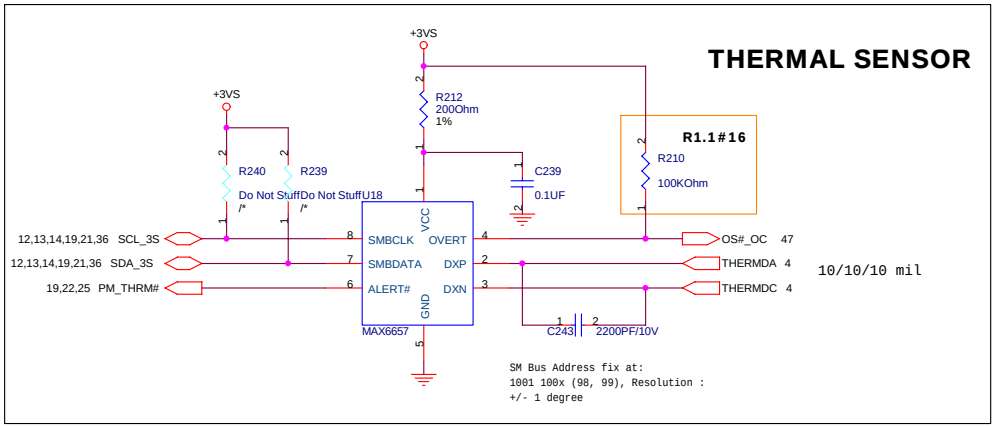
Decoupling guide from INTEL

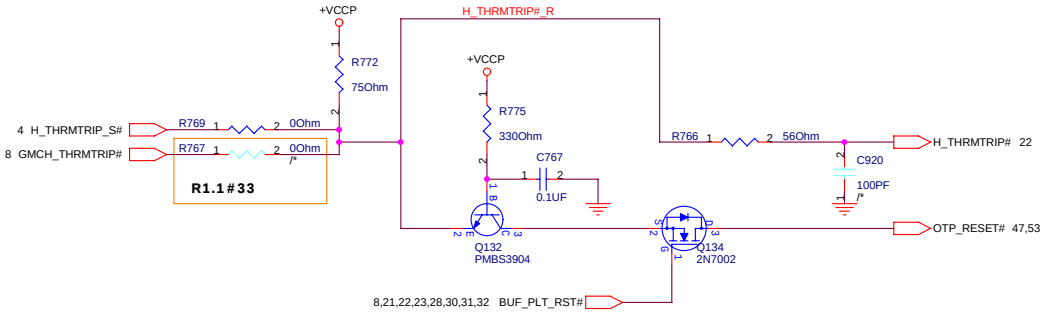




DOTHAN VID TABLE							
CPU FREQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.6G	C3/C4
1.8G	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V
1.7G							

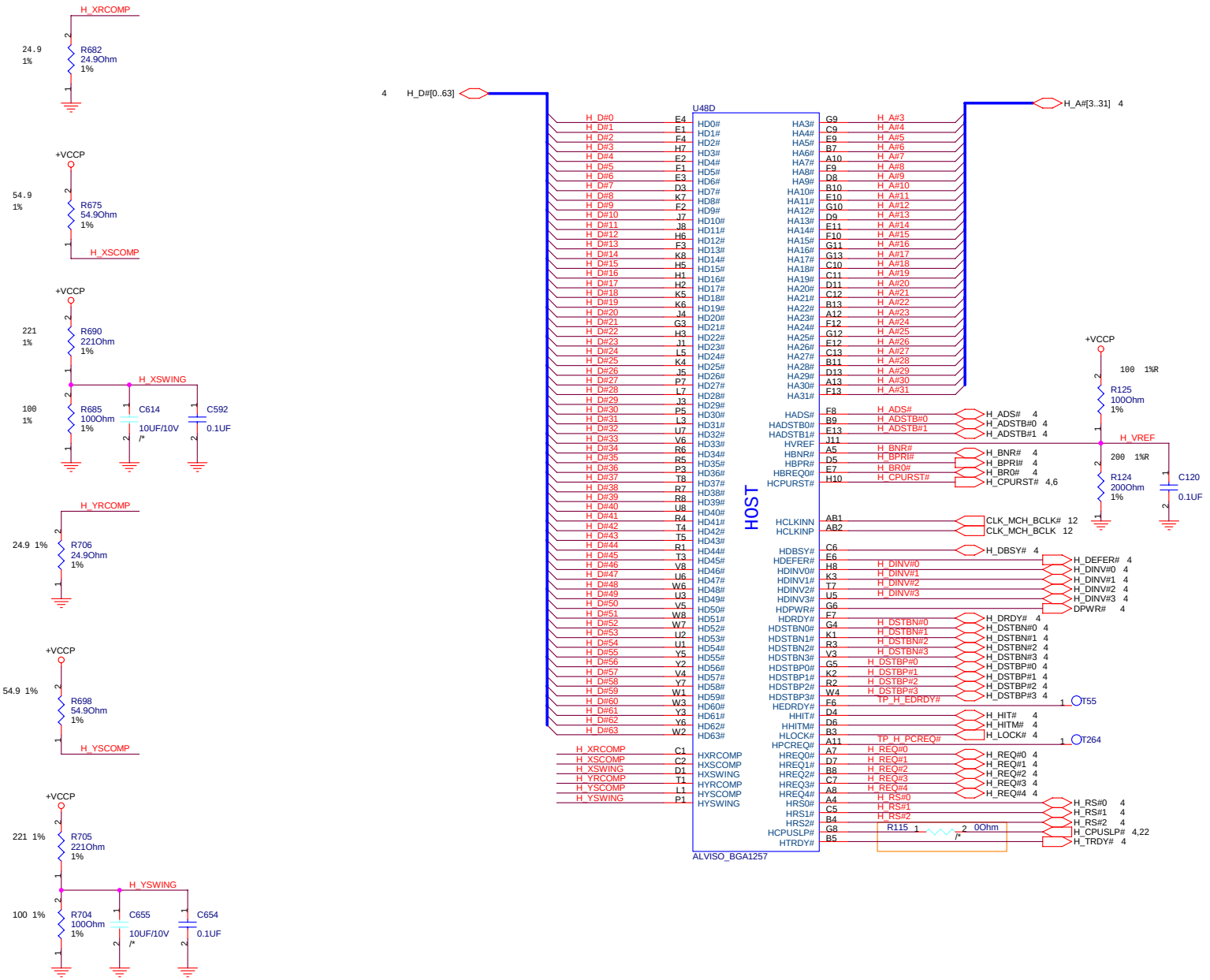






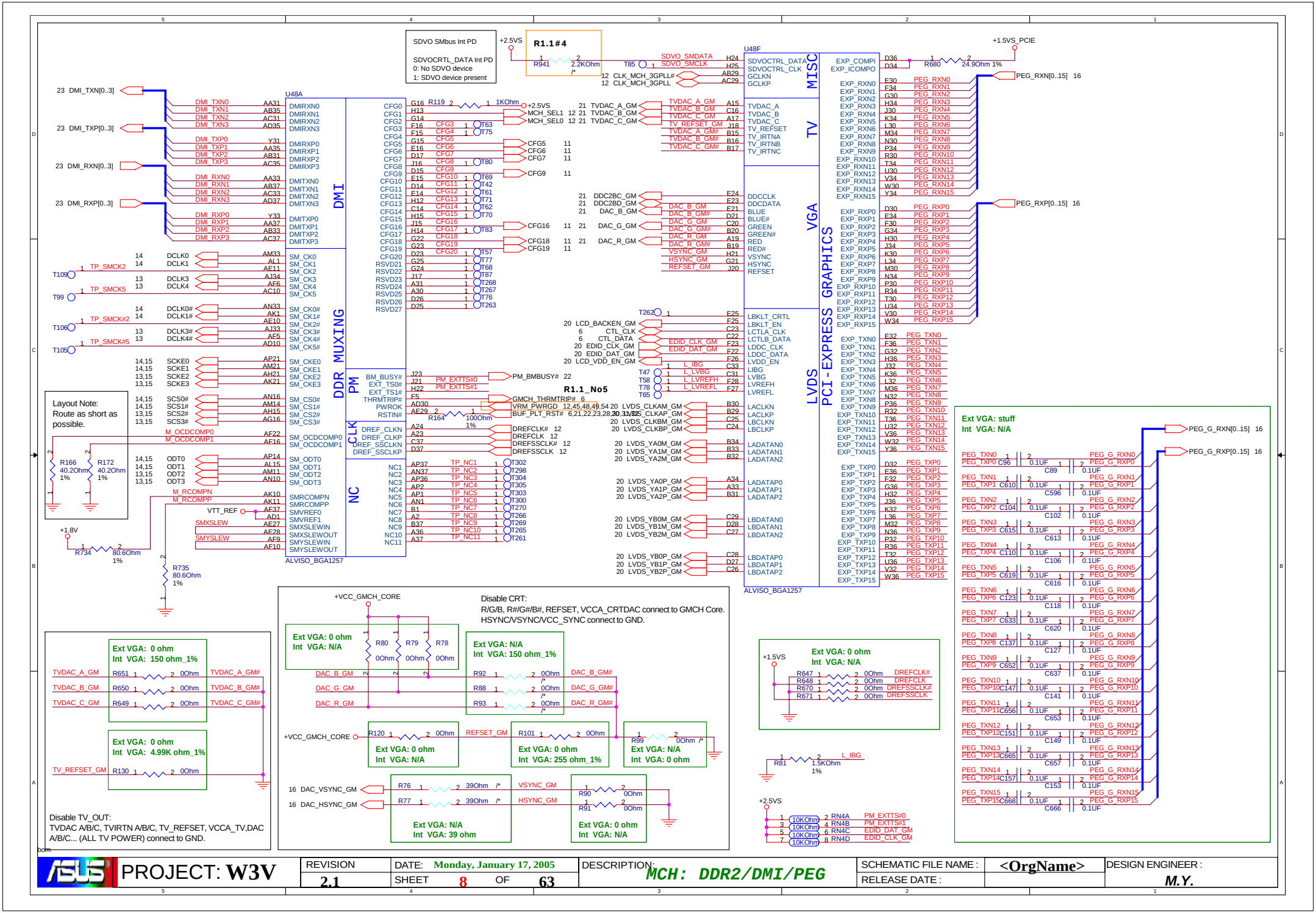
bom

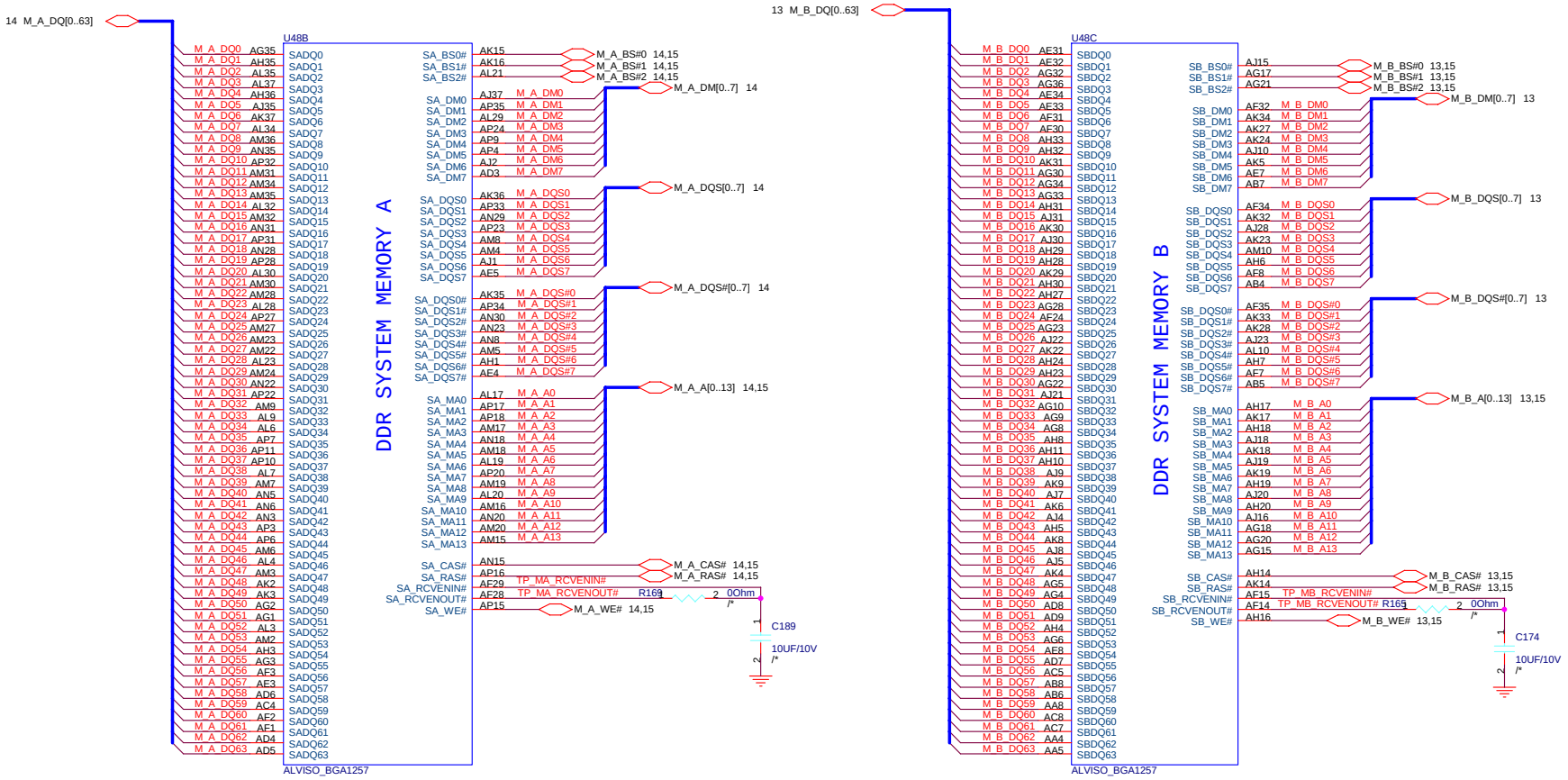
PROJECT: W3V	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 6 OF 63	Caps & THERMAL & ITP	RELEASE DATE :	M.Y.



bom

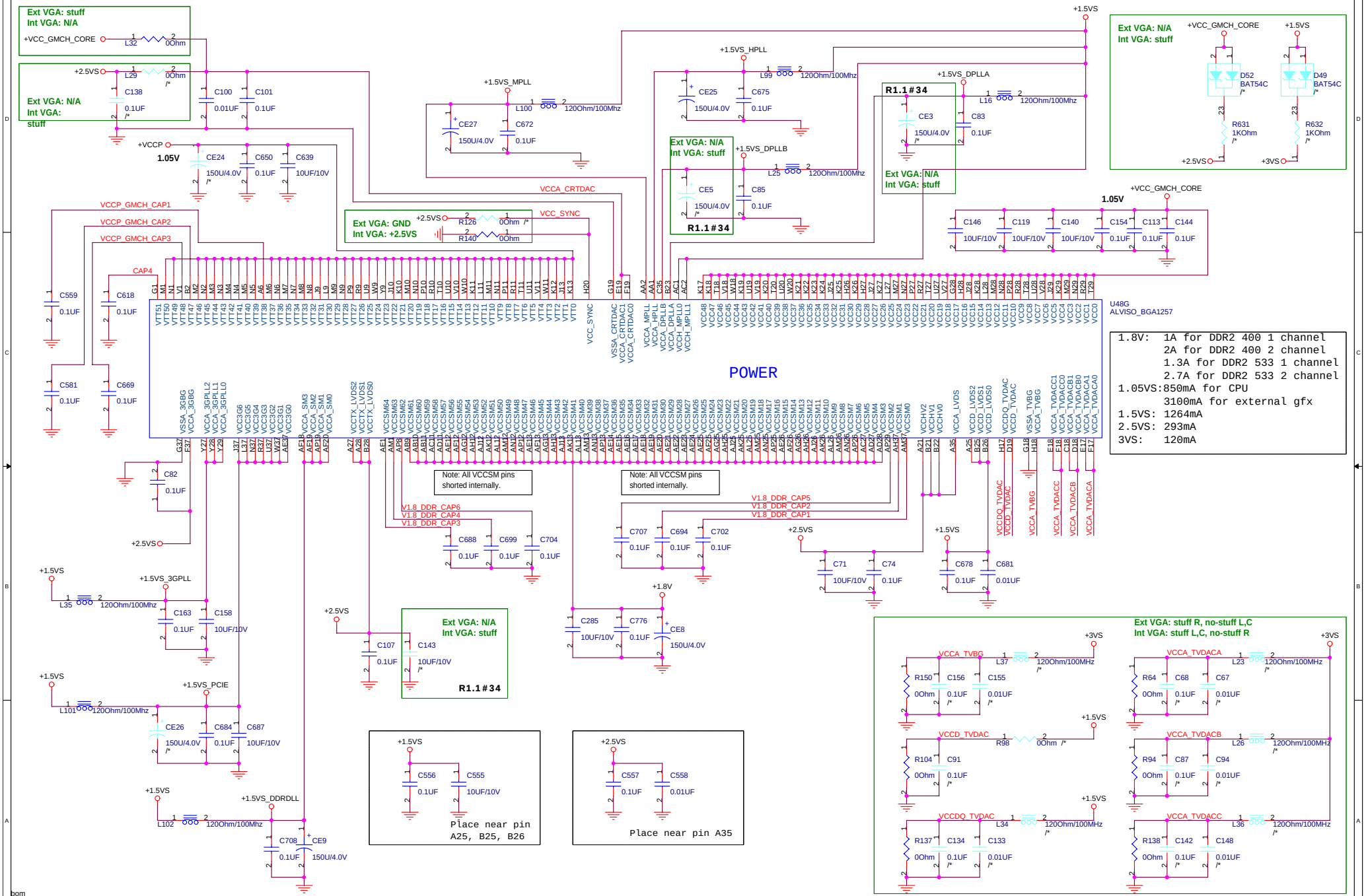
PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***MCH: CPU***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***M.Y.***
		SHEET **7** OF **63**		RELEASE DATE :	


SDVO SMbus Int PD
SDVOCRTL_DATA Int PD
0: No SDVO device
1: SDVO device present
R1.1#4
U48A
U48F
DMI
DDR MUXING
PM
CLK
NC
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO_BGA1257
R1.1_No5
Layout Note:
Route as short as possible.
Disable TV_OUT:
TVDAC A/B/C, TVIRTN A/B/C, TV_REFSET, VCCA_TV,DAC A/B/C... (ALL TV POWER) connect to GND.
Disable CRT:
R/G/B, R#/G#/B#, REFSET, VCCA_CRTDAC connect to GMCH Core.
HSYNC/VSYNC/VCC_SYNC connect to GND.
Ext VGA: stuff
Int VGA: N/A
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 8 OF 63
DESCRIPTION: MCH: DDR2/DMI/PEG
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : M.Y.



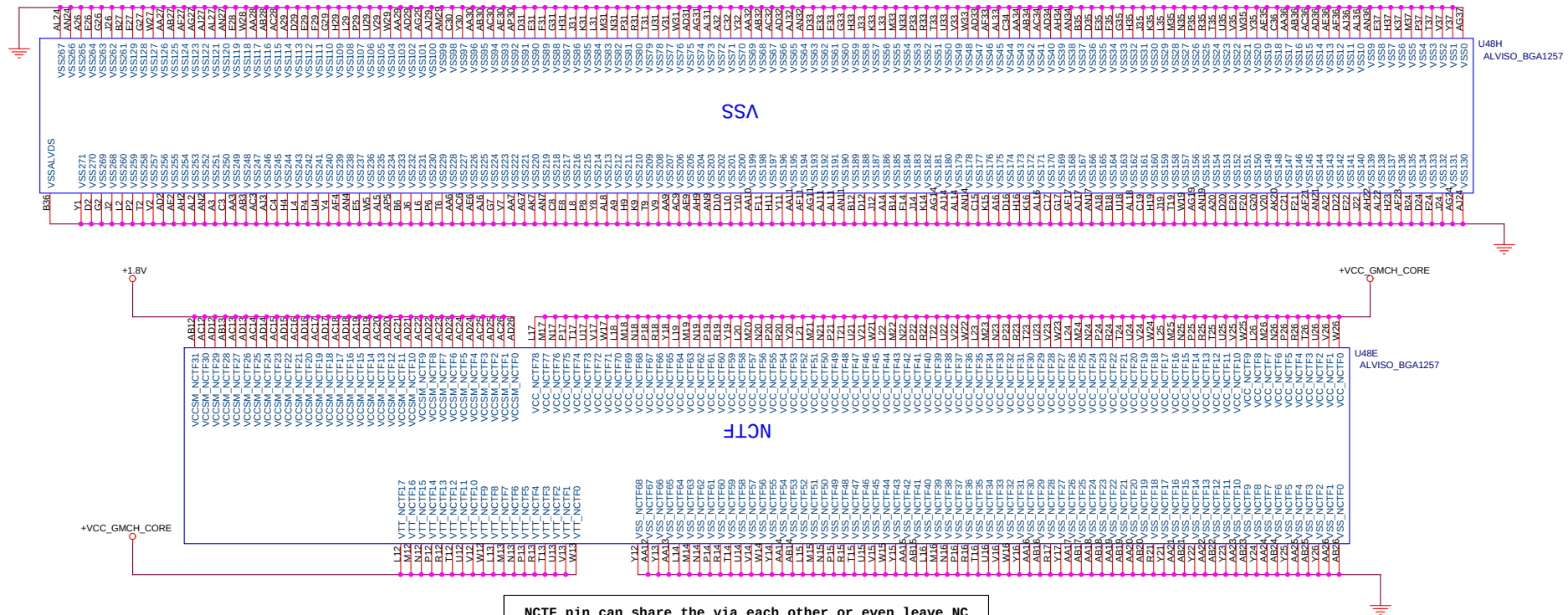
bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***MCH: DDR2***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***M.Y.***
		SHEET **9** OF **63**		RELEASE DATE :		

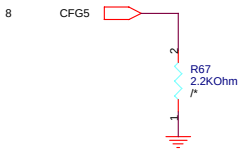


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***MCH: POWER***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***M.Y.***
		SHEET **10** OF **63**		RELEASE DATE :	

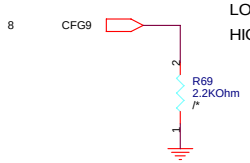


CFG5: LOW = DMI X 2
HIGH = DMI X 4 (Default)



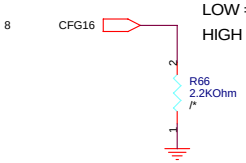
CFG9: PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



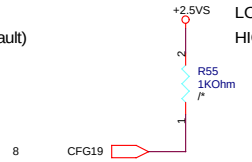
CFG16: FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



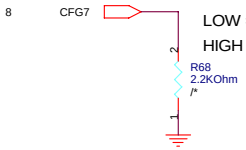
CFG19: CPU VTT SELECT

LOW = 1.05V (Default)
HIGH = 1.2V



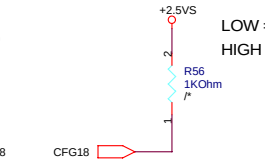
CFG7: CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



CFG18: CPU VCC SELECT

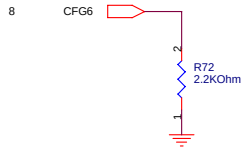
LOW = 1.05V (Default)
HIGH = 1.5V



SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

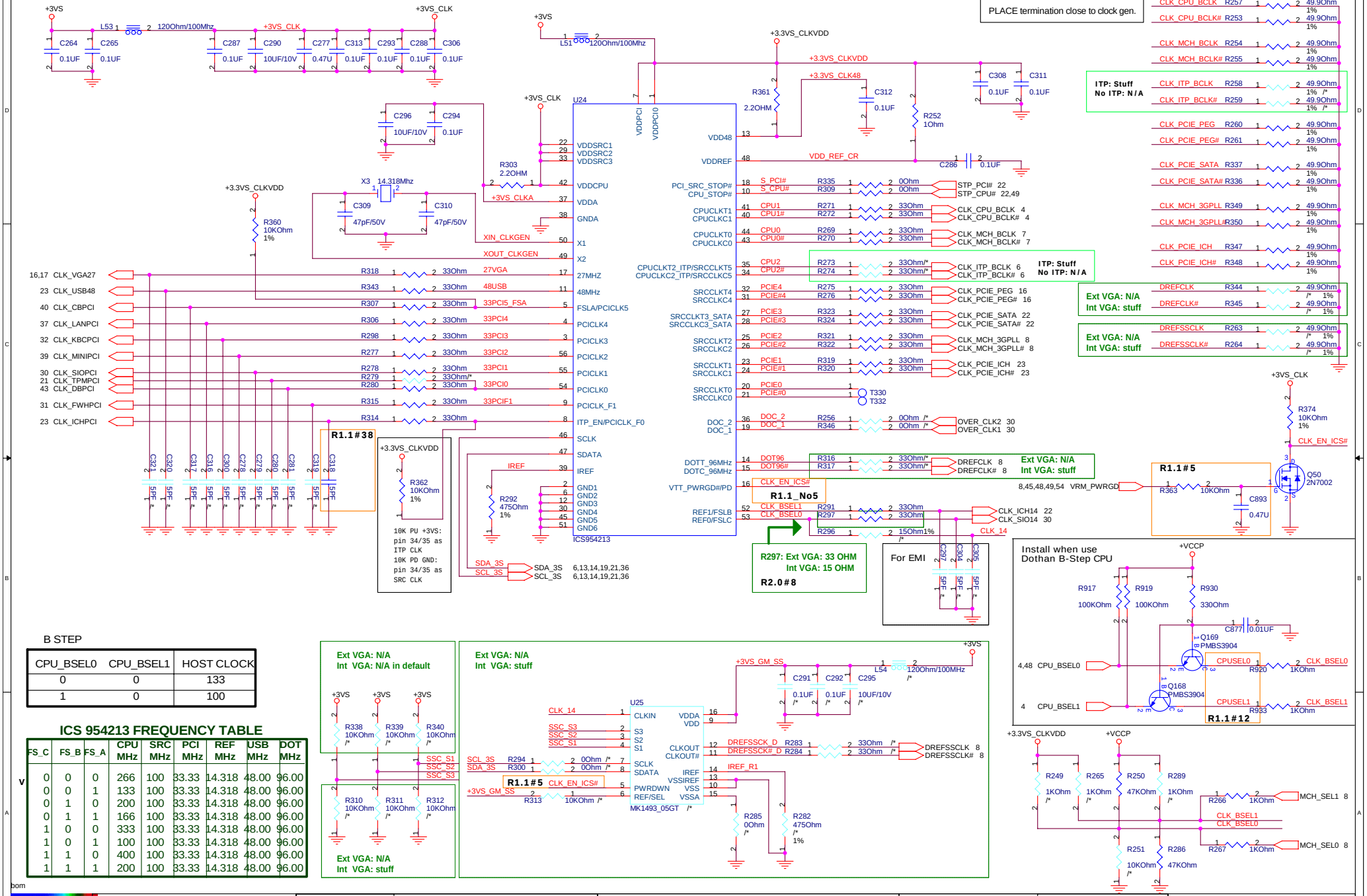
CFG6: LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

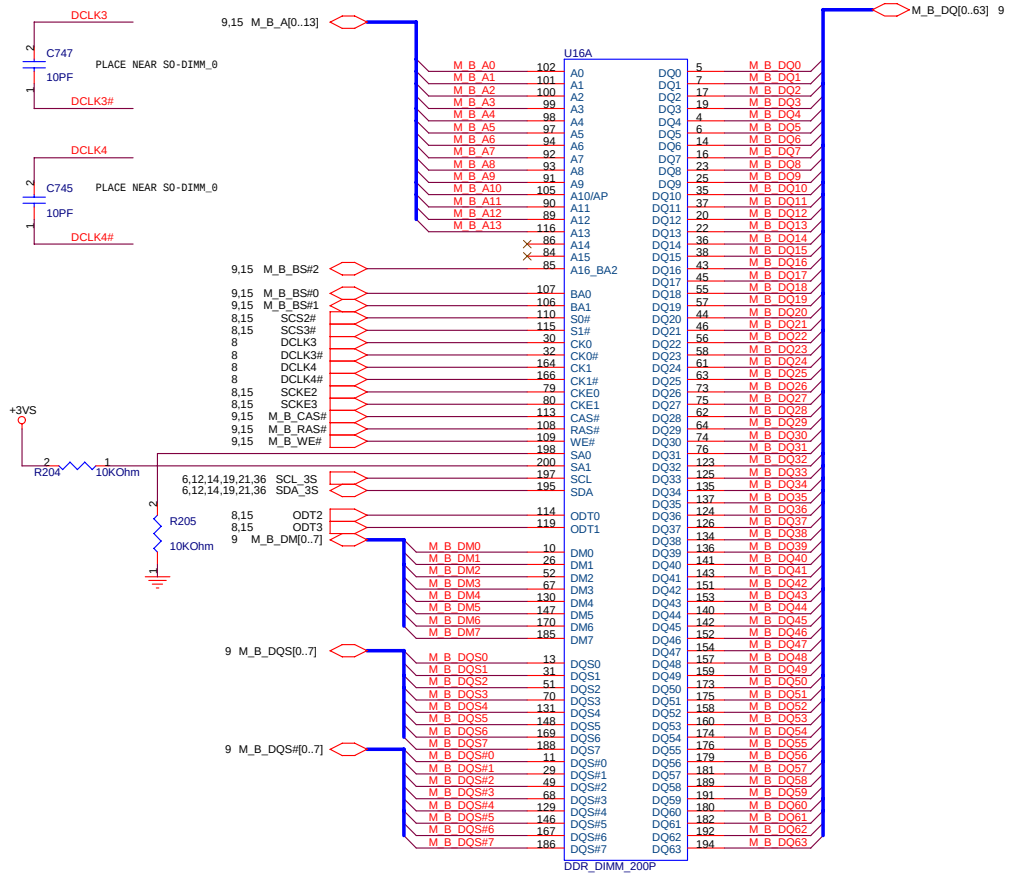


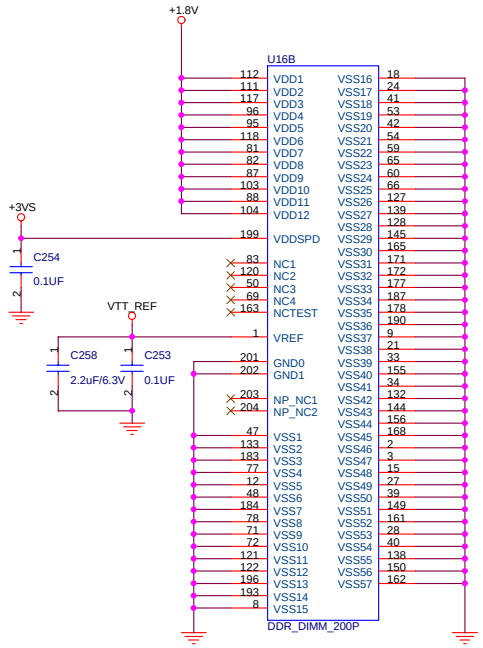
bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: **Monday, January 17, 2005** SHEET **11** OF **63**	DESCRIPTION: ***MCH: GND/NCTF/Strap***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

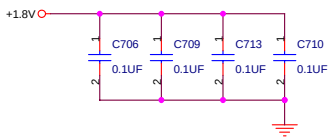
DESIGN ENGINEER : ***M.Y.***


PLACE termination close to clock gen.
U24
ICS954213
MK1493_05GT
U25
ITP: Stuff
No ITP: N/A
Ext VGA: N/A
Int VGA: stuff
Ext VGA: N/A
Int VGA: N/A in default
R297: Ext VGA: 33 OHM
Int VGA: 15 OHM
R2.0#8
R1.1_No5
R1.1#38
R1.1#5
R1.1#12
For EMI
Install when use
Dothan B-Step CPU
10K PU +3VS:
pin 34/35 as
ITP CLK
10K PD GND:
pin 34/35 as
SRC CLK
B STEP
CPU_BSEL0 CPU_BSEL1 HOST CLOCK
0 0 133
1 0 100
ICS 954213 FREQUENCY TABLE
FS_C FS_B FS_A CPU MHz SRC MHz PCI MHz REF MHz USB MHz DOT MHz
0 0 0 266 100 33.33 14.318 48.00 96.00
0 0 1 133 100 33.33 14.318 48.00 96.00
0 1 0 200 100 33.33 14.318 48.00 96.00
0 1 1 166 100 33.33 14.318 48.00 96.00
1 0 0 333 100 33.33 14.318 48.00 96.00
1 0 1 100 100 33.33 14.318 48.00 96.00
1 1 0 400 100 33.33 14.318 48.00 96.00
1 1 1 200 100 33.33 14.318 48.00 96.00
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 12 OF 63
DESCRIPTION: CLOCK GEN (ICS954213)
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : M.Y.

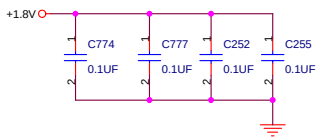




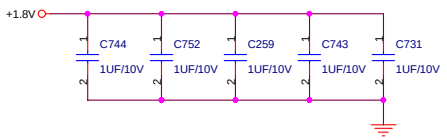
Layout Note: Place these High-Freq decoupling Caps near the GMCH

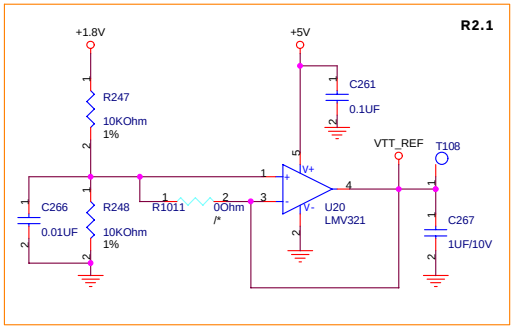


Layout Note: Place these Caps near SO DIMM 0



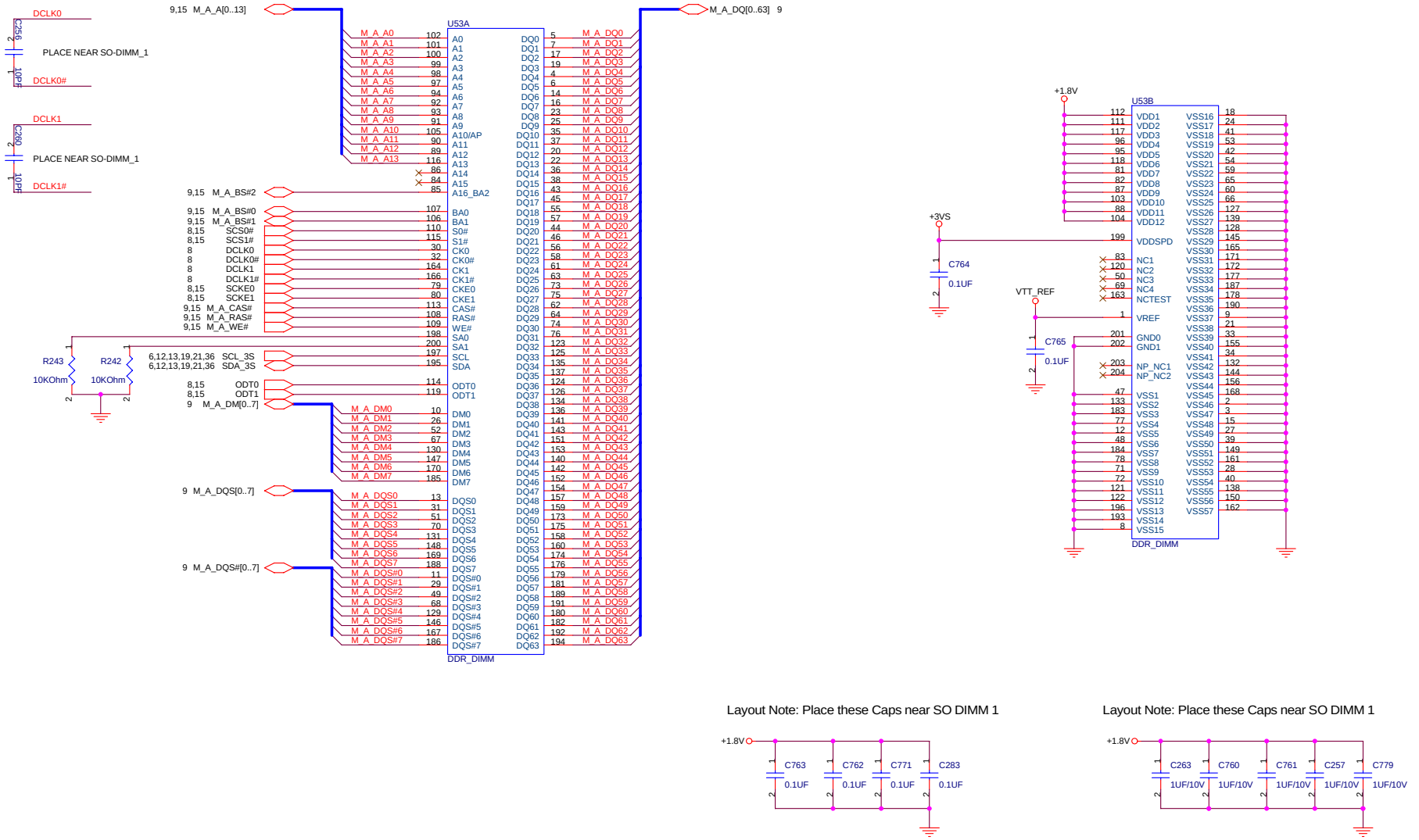
Layout Note: Place these Caps near SO DIMM 0





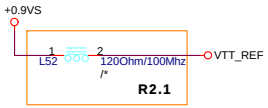
bom

PROJECT: **W3V**	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.1	SHEET 13 OF 63	***DDR2 SO-DIMM (1)***	RELEASE DATE :		***M.Y.***

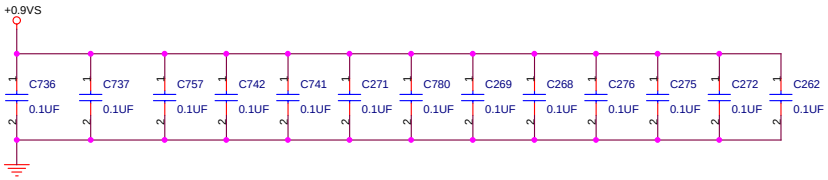


bom

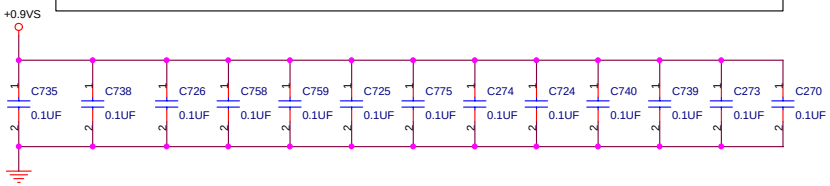
PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***DDR2 SO-DIMM (2)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***M.Y.***
		SHEET **14** OF **63**		RELEASE DATE :	

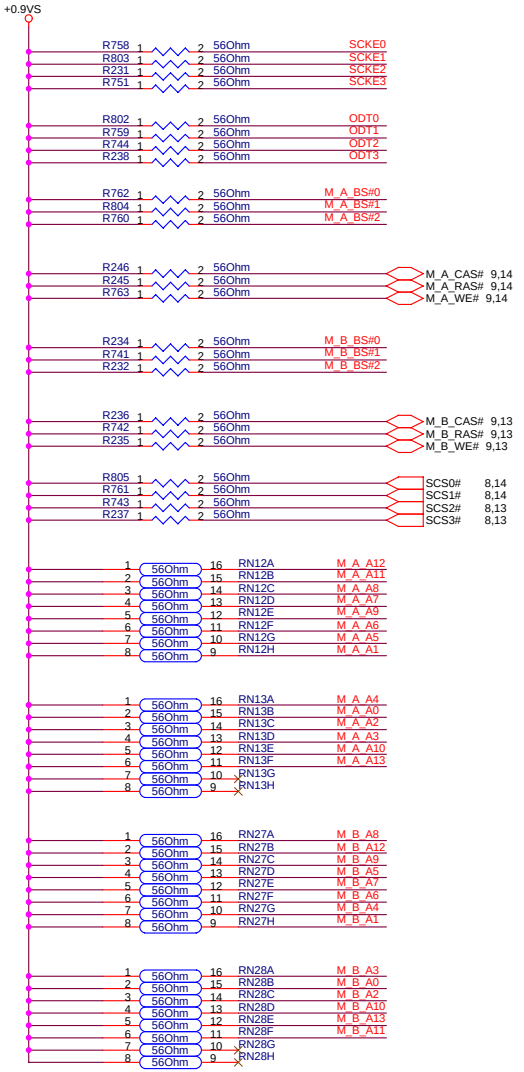


M_A_A[0..13] 9,14
M_A_BS#[0..2] 9,14
M_B_A[0..13] 9,13
M_B_BS#[0..2] 9,13
SCKE[0:3] 8,13,14
ODT[0:3] 8,13,14



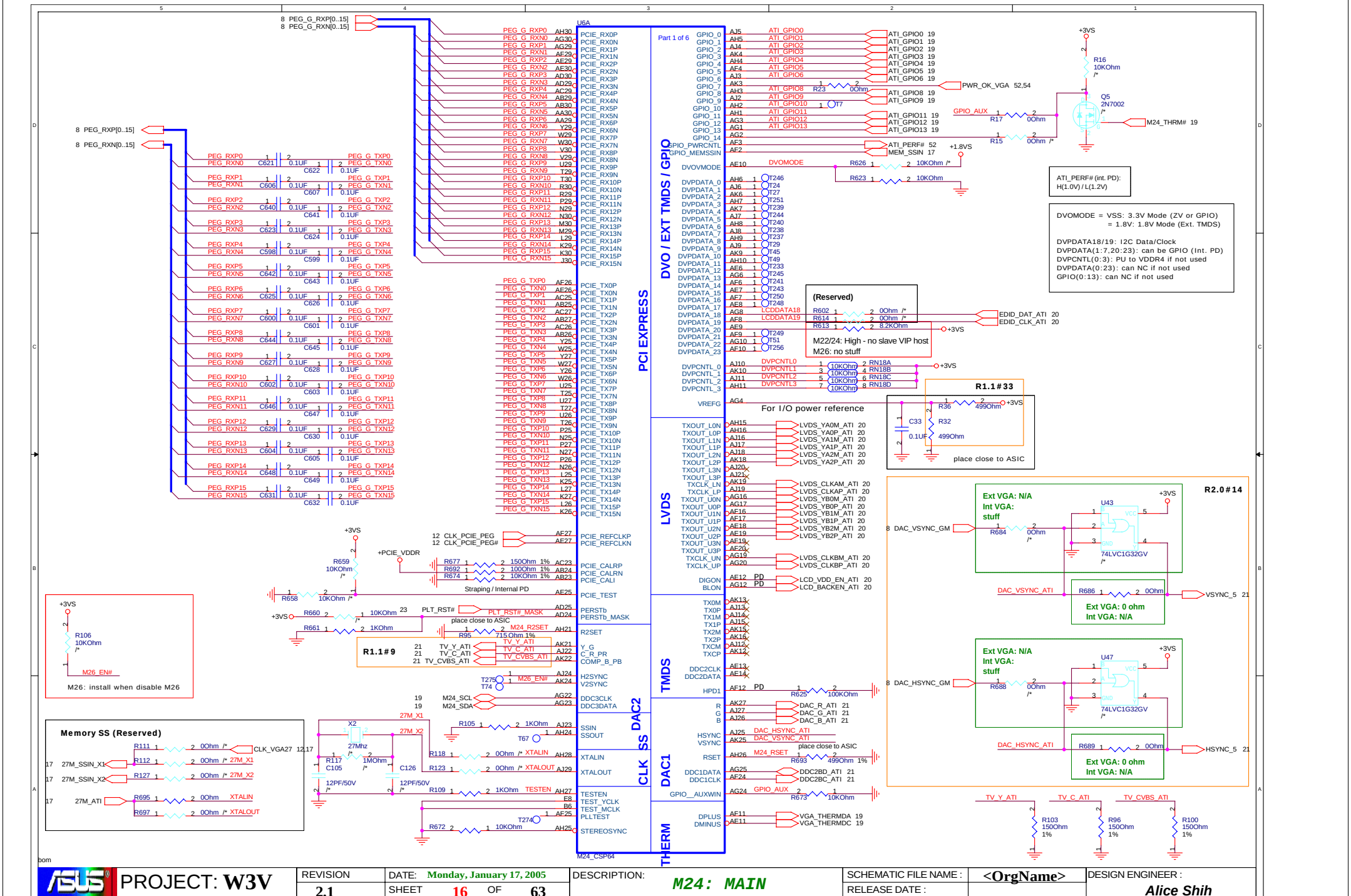
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

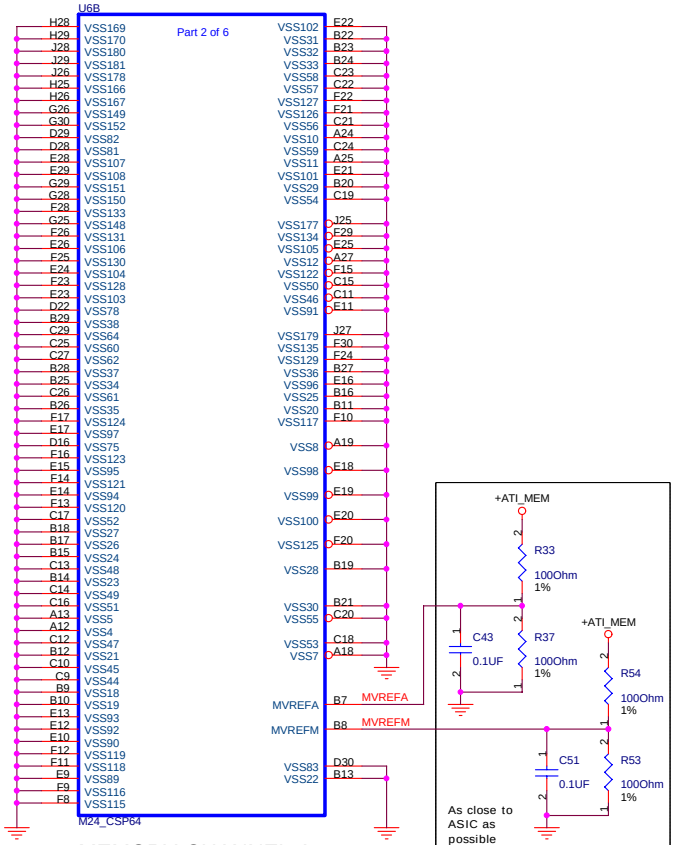


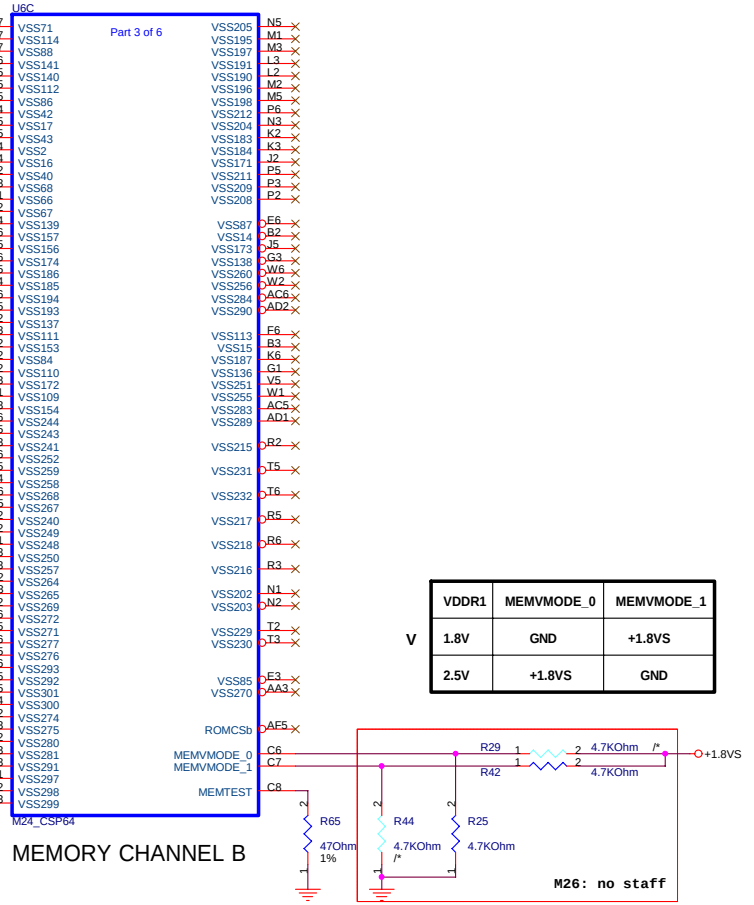


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005** SHEET **15** OF **63**	DESCRIPTION: ***DDR2 Res***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***M.Y.***


8 PEG_G_RXP[0..15]
8 PEG_G_RXN[0..15]
U6A
Part 1 of 6
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC2
DAC1
CLK_SS
THERM
M24_CSP64
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TEST
PERSTb
PERSTb_MASK
R2SET
Y_G
C_R_PR
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
SSIN
SSOUT
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_PWRCNTL
GPIO_MEMSSIN
DVOVMODE
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_3
VREFG
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP
DIGON
BLON
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCM
TXCP
DDC2CLK
DDC2DATA
HPD1
R
G
B
HSYNC
VSYNC
RSET
DDC1DATA
DDC1CLK
GPIO__AUXWIN
DPLUS
DMINUS
ATI_GPIO0
ATI_GPIO1
ATI_GPIO2
ATI_GPIO3
ATI_GPIO4
ATI_GPIO5
ATI_GPIO6
ATI_GPIO8
ATI_GPIO9
ATI_GPIO10
ATI_GPIO11
ATI_GPIO12
ATI_GPIO13
ATI_PERF# 52
MEM_SSIN 17
PWR_OK_VGA 52,54
GPIO_AUX
M24_THRM# 19
+3VS
+1.8VS
DVOMODE
LCDDATA18
LCDDATA19
EDID_DAT_ATI 20
EDID_CLK_ATI 20
DVPCNTL0
DVPCNTL1
DVPCNTL2
DVPCNTL3
RN18A
RN18B
RN18C
RN18D
LVDS_YA0M_ATI 20
LVDS_YA0P_ATI 20
LVDS_YA1M_ATI 20
LVDS_YA1P_ATI 20
LVDS_YA2M_ATI 20
LVDS_YA2P_ATI 20
LVDS_CLKAM_ATI 20
LVDS_CLKAP_ATI 20
LVDS_YB0M_ATI 20
LVDS_YB0P_ATI 20
LVDS_YB1M_ATI 20
LVDS_YB1P_ATI 20
LVDS_YB2M_ATI 20
LVDS_YB2P_ATI 20
LVDS_CLKBM_ATI 20
LVDS_CLKBP_ATI 20
LCD_VDD_EN_ATI 20
LCD_BACKEN_ATI 20
DAC_R_ATI 21
DAC_G_ATI 21
DAC_B_ATI 21
DAC_HSYNC_ATI
DAC_VSYNC_ATI
M24_RSET
DDC2BD_ATI 21
DDC2BC_ATI 21
VGA_THERMDA 19
VGA_THERMDC 19
(Reserved)
M22/24: High - no slave VIP host
M26: no stuff
For I/O power reference
R1.1#33
place close to ASIC
ATI_PERF# (int. PD):
H(1.0V) / L(1.2V)
DVOMODE = VSS: 3.3V Mode (ZV or GPIO)
= 1.8V: 1.8V Mode (Ext. TMDS)
DVPDATA18/19: I2C Data/Clock
DVPDATA(1:7,20:23): can be GPIO (Int. PD)
DVPCNTL(0:3): PU to VDDR4 if not used
DVPDATA(0:23): can NC if not used
GPIO(0:13): can NC if not used
Straping / Internal PD
+PCIE_VDDR
PLT_RST#
PLT_RST#_MASK
place close to ASIC
R1.1#9
TV_Y_ATI
TV_C_ATI
TV_CVBS_ATI
M26_EN#
M26: install when disable M26
Memory SS (Reserved)
CLK_VGA27
27M_SSIN_X1
27M_SSIN_X2
27M_ATI
27M_X1
27M_X2
27Mhz
XTALIN
XTALOUT
TESTEN
M24_SCL
M24_SDA
R2.0#14
Ext VGA: N/A
Int VGA: stuff
Ext VGA: 0 ohm
Int VGA: N/A
74LVC1G32GV
DAC_VSYNC_GM
DAC_HSYNC_GM
VSYNC_5 21
HSYNC_5 21
TV_Y_ATI
TV_C_ATI
TV_CVBS_ATI
bom
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 16 OF 63
DESCRIPTION: M24: MAIN
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Alice Shih



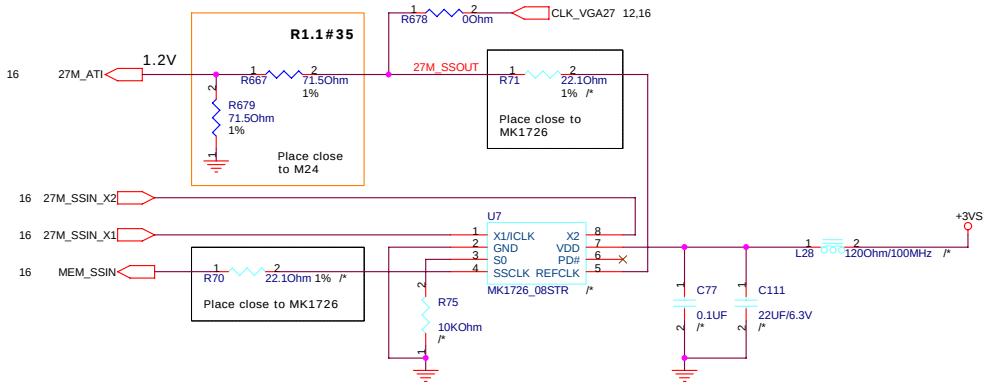


V

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+1.8VS
2.5V	+1.8VS	GND

Memory Clock SS (Reserved)

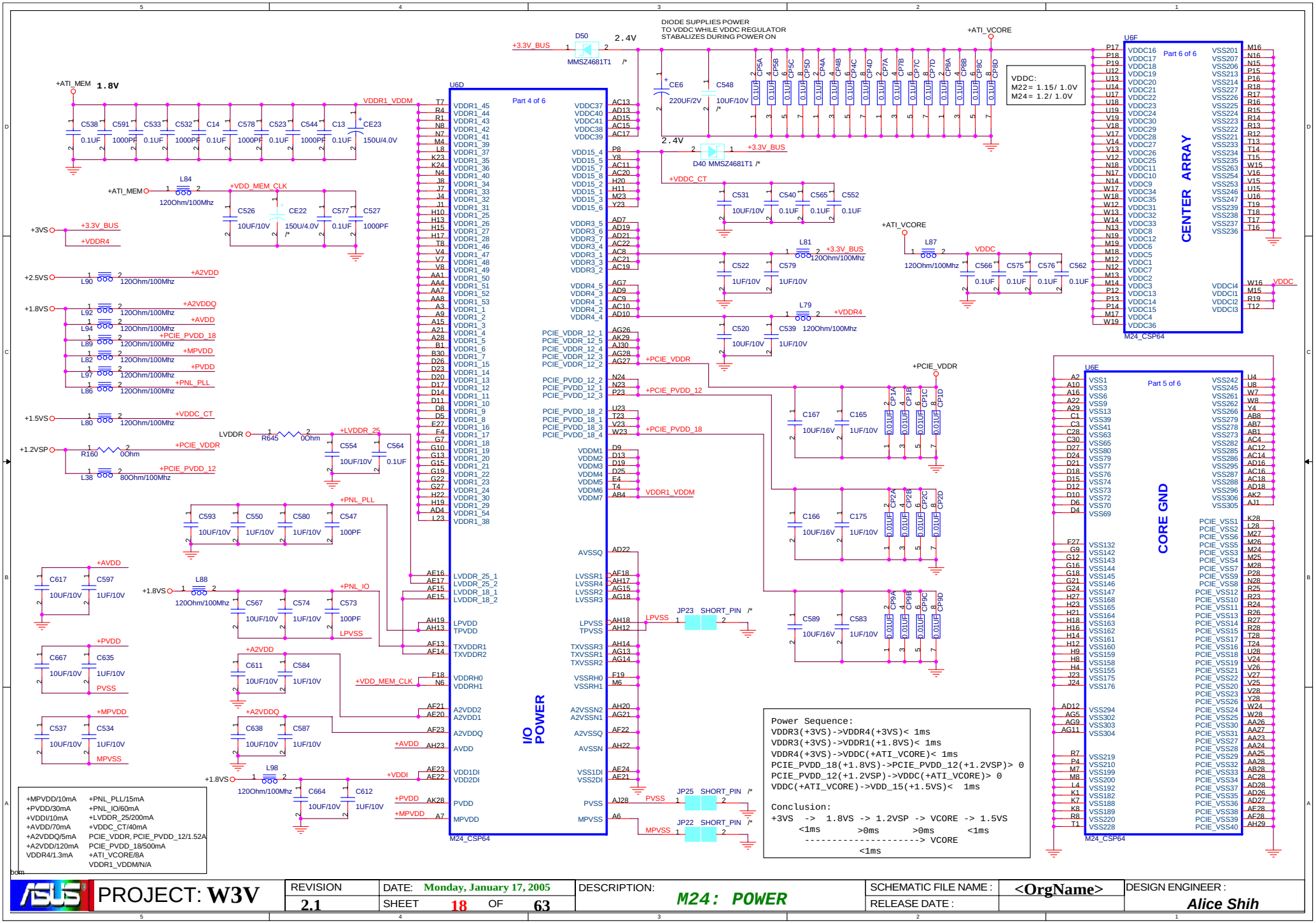
S0 (Spread Percentage Select):
GND: -1.8%
VDD: -2.5% (default PU)
NC : -0.6%



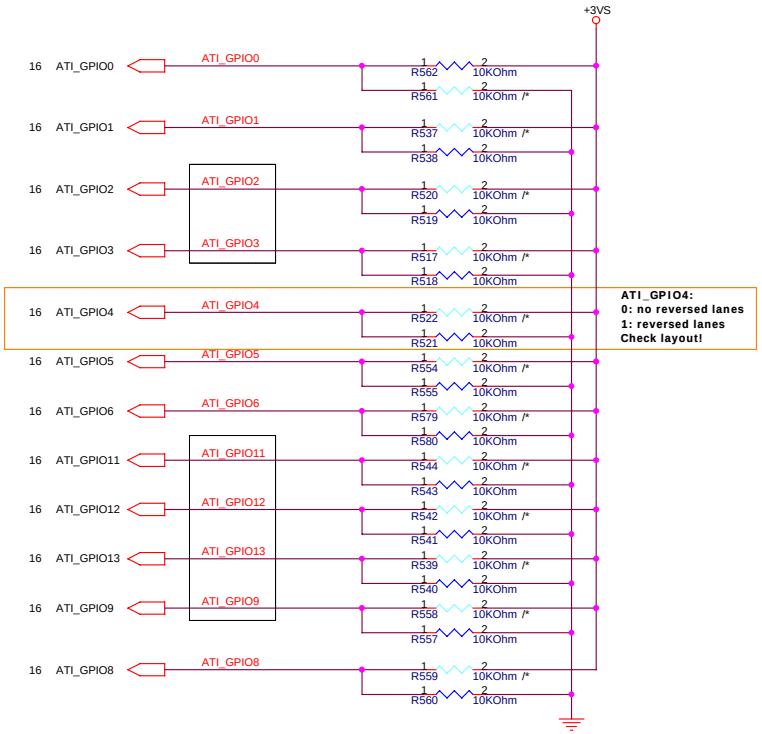
bom

PROJECT: W3V	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 17 OF 63	M24: MEMORY & SS	RELEASE DATE :	Alice Shih

<OrgName>


DIODE SUPPLIES POWER
TO VDDC WHILE VDDC REGULATOR
STABALIZES DURING POWER ON
U6D
Part 4 of 6
I/O POWER
M24_CSP64
U6F
Part 6 of 6
CENTER ARRAY
VDDC:
M22= 1.15/ 1.0V
M24= 1.2/ 1.0V
U6E
Part 5 of 6
CORE GND
Power Sequence:
VDDR3(+3VS)->VDDR4(+3VS)< 1ms
VDDR3(+3VS)->VDDR1(+1.8VS)< 1ms
VDDR4(+3VS)->VDDC(+ATI_VCORE)< 1ms
PCIE_PVDD_18(+1.8VS)->PCIE_PVDD_12(+1.2VSP)> 0
PCIE_PVDD_12(+1.2VSP)->VDDC(+ATI_VCORE)> 0
VDDC(+ATI_VCORE)->VDD_15(+1.5VS)< 1ms
Conclusion:
+3VS -> 1.8VS -> 1.2VSP -> VCORE -> 1.5VS
<1ms >0ms >0ms <1ms
----------> VCORE
<1ms
+MPVDD/10mA
+PVDD/30mA
+VDDI/10mA
+AVDD/70mA
+A2VDDQ/5mA
+A2VDD/120mA
VDDR4/1.3mA
+PNL_PLL/15mA
+PNL_IO/60mA
+LVDDR_25/200mA
+VDDC_CT/40mA
PCIE_VDDR, PCIE_PVDD_12/1.52A
PCIE_PVDD_18/500mA
+ATI_VCORE/8A
VDDR1_VDDM/N/A
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 18 OF 63
DESCRIPTION: M24 : POWER
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Alice Shih

OPTION STRAPS



GPIO[0:13] : Internal PD

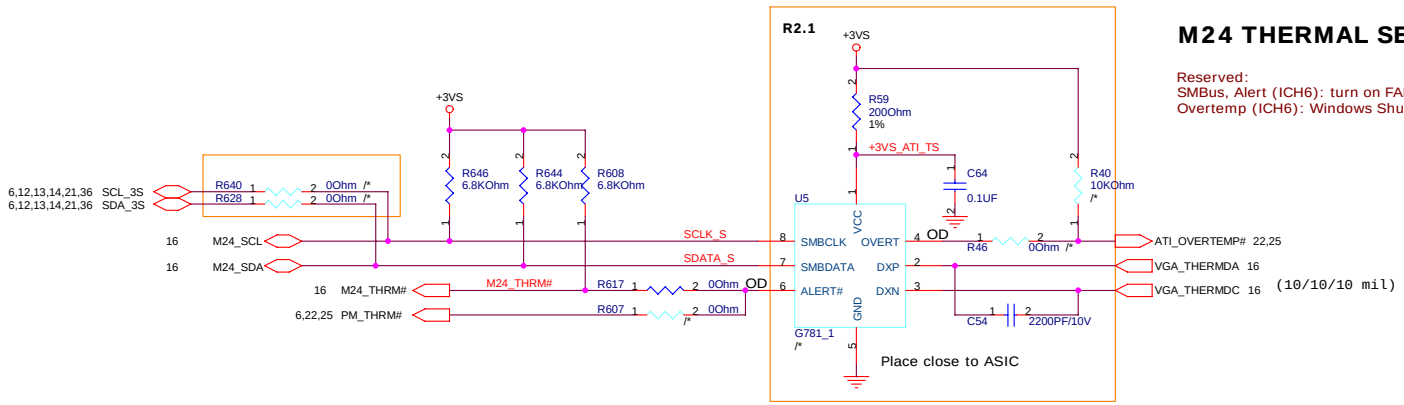
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
B_PRX_IDLE_MODE (for A21) B_PTX_PDNB_MODE	PCIE_TEST	(For A21) PHY Receiver Idle Detector 0: Normal idle detector / 1: Alternate idle detector ATI internal use only. Other logic must not affect this signal during RESET	0
B_PTX_PWRS_ENB	GPIO0	V Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (recommended) Must have an external 10K pullup to 3.3V	0
B_PTX_DEEMPH_EN	GPIO1	V Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de_emphasis enable	0
PCIE_MODE(1:0)	GPIO(3:2)	V 00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
B_PTX_IEXT (For M24 A21/M22 A11)	GPIO4	V **0: normal mode 1: extra current in Tx output stage**	0
REVERSE LANES (For M24A23/M22 A13)		V **0: non-reversed lanes layout 1: reversed lanes layout**	0
FORCE_COMPLIANCE	GPIO5	Force chip to go to compliance state quickly for test purposes	0
B_PPLL_BW (For M24 A21/M22 A11)	GPIO6	V 0: Full PLL Bandwidth 1: Reduced PLL Bandwidth (ATI internal use only. Other logic must not attect this during RESET.)	0
CM_RANGE (For M24A23/M22 A13)		V 0: normal common-mode range 1: extended commeon-mode range	0
DEBUG_ACCESS	GPIO8	Controls whether ROM bytes 77-76 are used as SUBSYS_VEN_ID strap or DEBUG_PORT_MUX_SELECT strap.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	V If no ROM attached, controls chip IDis. If ROM attached identifies ROM type 0x0x - No ROM, CHG_ID=0 0x1x - No ROM, CHG_ID=1 1000 - Parallel ROM, chip IDis from ROM 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 (SST), W45B512 (Winbond), 512K W45B012 (Winbond) 1110 - 1M SST25VF010 (SST), 512K SST25VF512 (SST) 1111 - 1M Serial NX25F011B (NextFlash)	0000 (internal PD)
VIP_DEVICE	DVPDATA_20	V 0: Slave VIP host port device peesent 1: No slave VIP host port device	(internal PD)
PKGTYPE(4:0)	DVPDATA(15:11)	ATI internal use only Identifies package/memory combinations	

M26: GPIO11 is memory aperture size (0=128M, 1=256M)

M24 THERMAL SENSOR

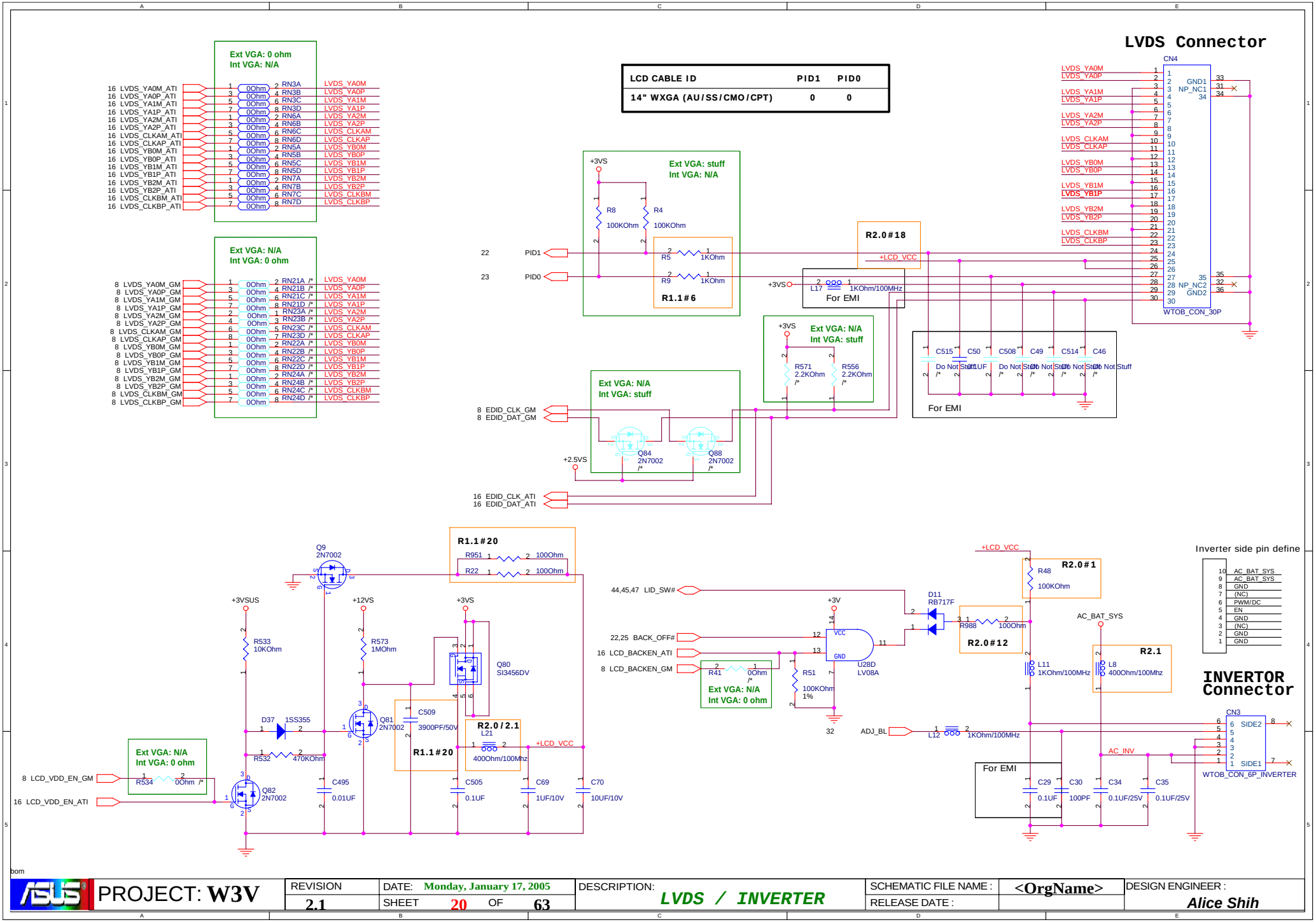
Ext VGA: stuff
Int VGA: N/A

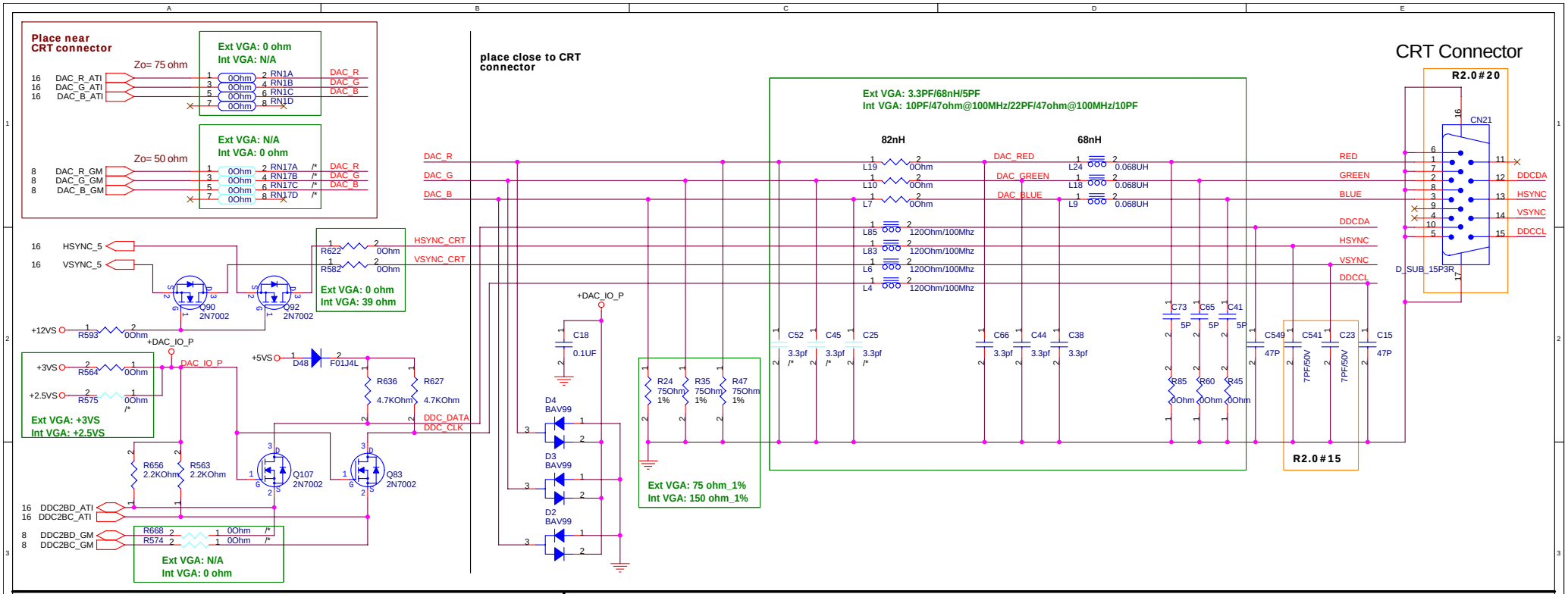
Reserved:
SMBus, Alert (ICH6): turn on FAN
Overtemp (ICH6): Windows Shutdown

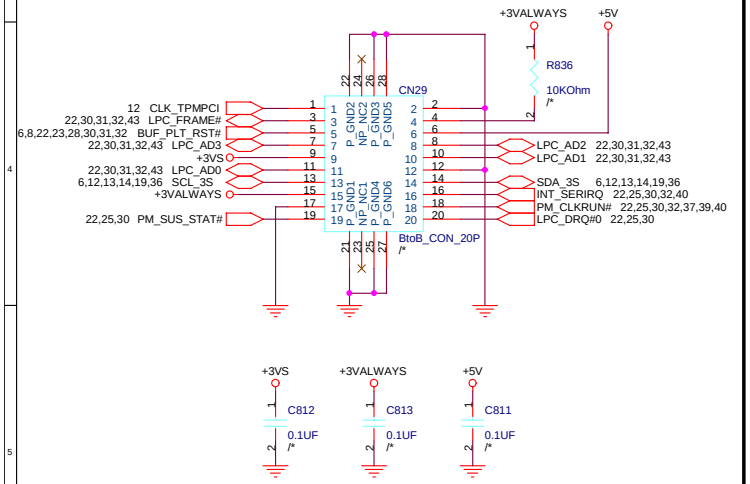


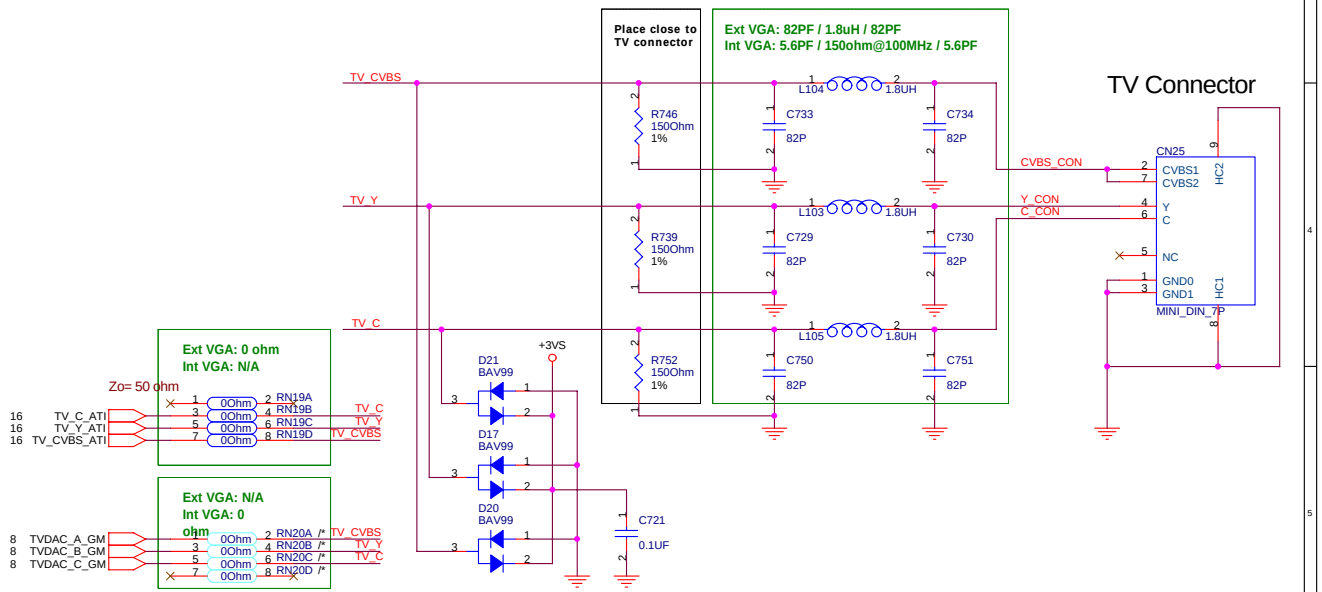
bom

PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 19 OF 63	DESCRIPTION: M24: STRAPING/THERMAL	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Alice Shih


LVDS Connector
Ext VGA: 0 ohm
Int VGA: N/A
Ext VGA: N/A
Int VGA: 0 ohm
LCD CABLE ID | PID1 | PID0
14" WXGA (AU/SS/CMO/CPT) | 0 | 0
Ext VGA: stuff
Int VGA: N/A
Ext VGA: N/A
Int VGA: stuff
R2.0#18
R1.1#6
For EMI
WTOB_CON_30P
Ext VGA: N/A
Int VGA: stuff
Ext VGA: N/A
Int VGA: 0 ohm
R1.1#20
R2.0 / 2.1
R2.0#1
R2.0#12
R2.1
Inverter side pin define
INVERTOR Connector
WTOB_CON_6P_INVERTER
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 20 OF 63
DESCRIPTION: LVDS / INVERTER
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Alice Shih

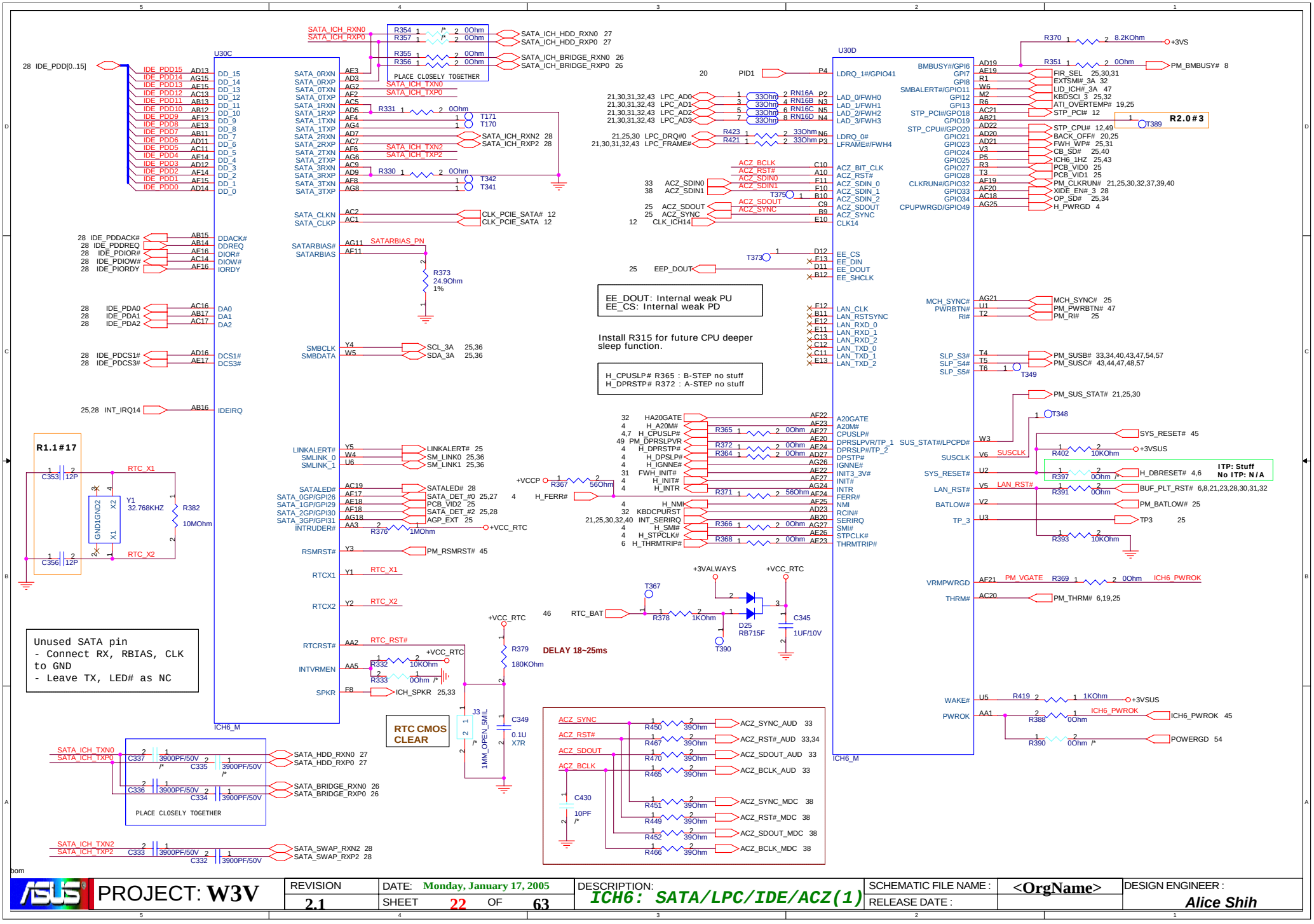






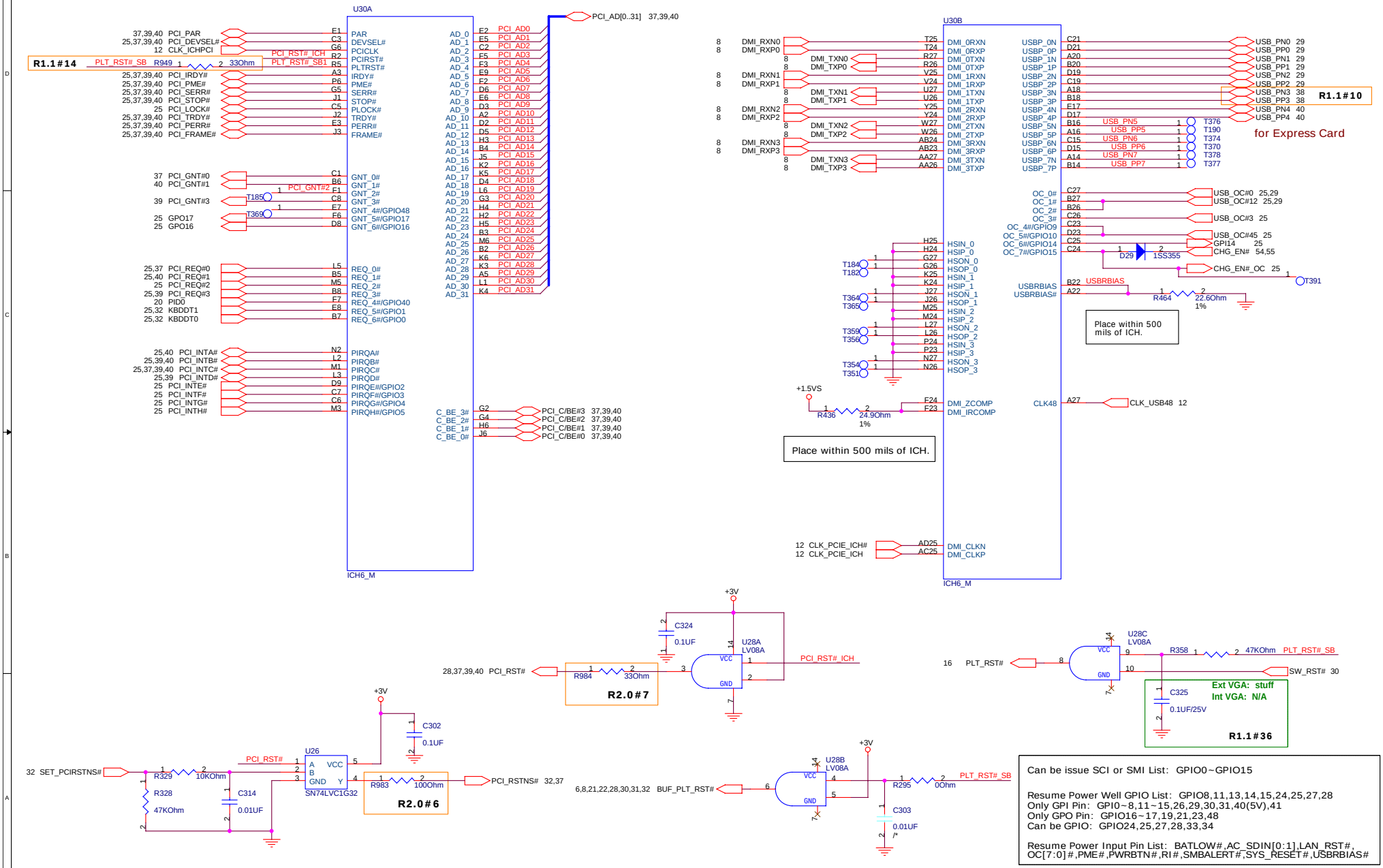
bom

PROJECT: **W3V**	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 21 OF 63	DESCRIPTION: CRT, TV, TPM CONN	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Alice Shih



bom

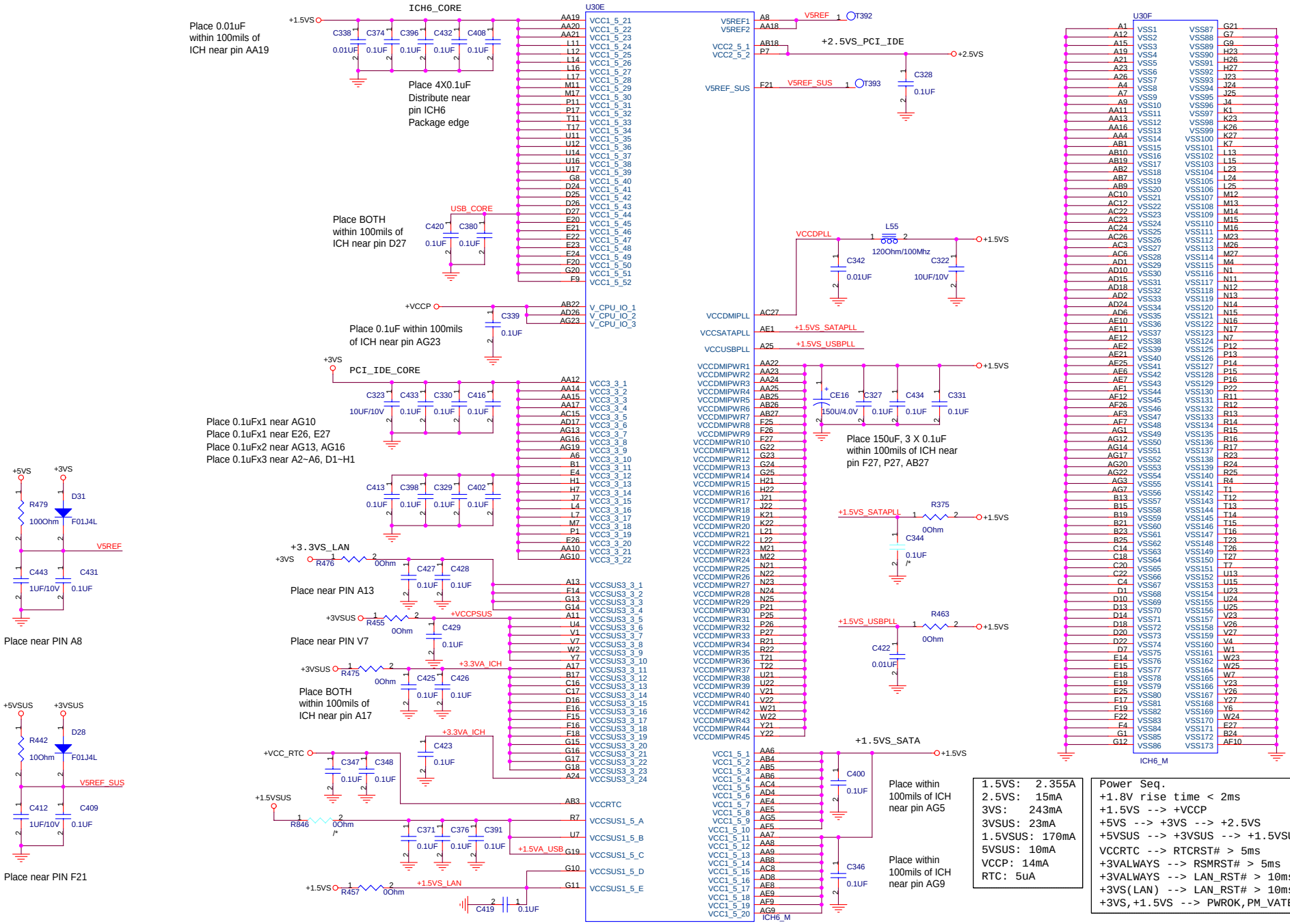
PROJECT: **W3V**	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 22 OF 63	DESCRIPTION: ICH6: SATA/LPC/IDE/ACZ(1)	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Alice Shih



bom

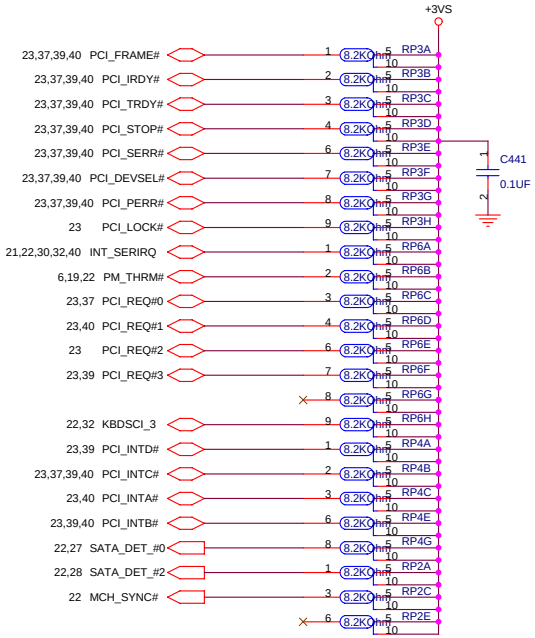
PROJECT: W3V	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 23 OF 63	ICH6: PCI/DMI/USB/PCIE(2)	RELEASE DATE :	Alice Shih

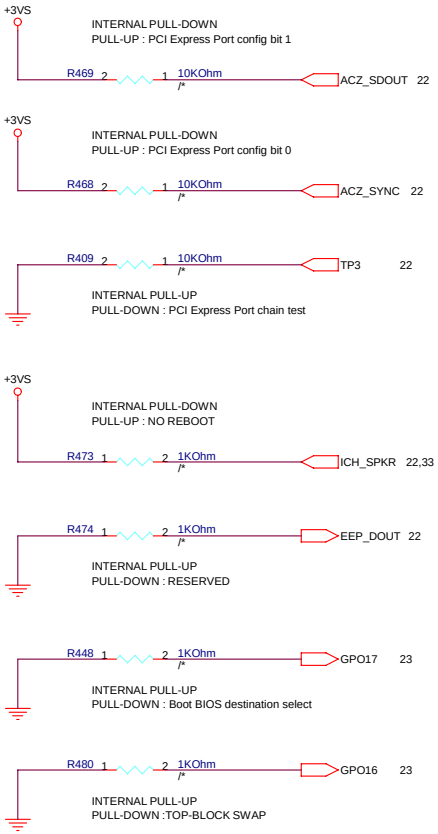
<OrgName>

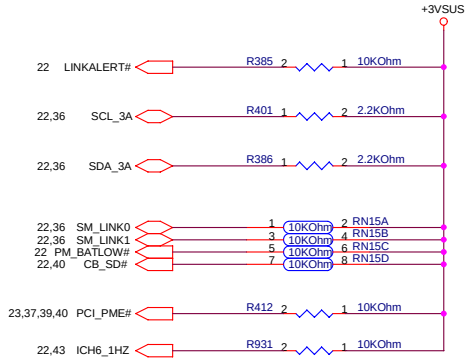


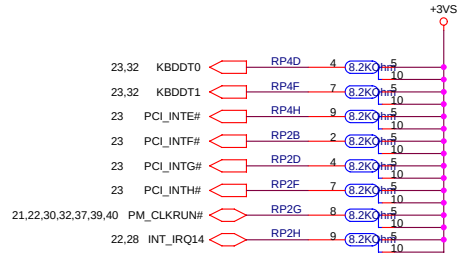
bom

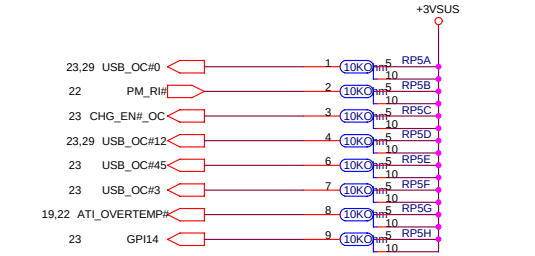
PROJECT: **W3V**	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.1	SHEET 24 OF 63	ICH6: PWR/GND/CAPS(3)	RELEASE DATE :		M.Y.

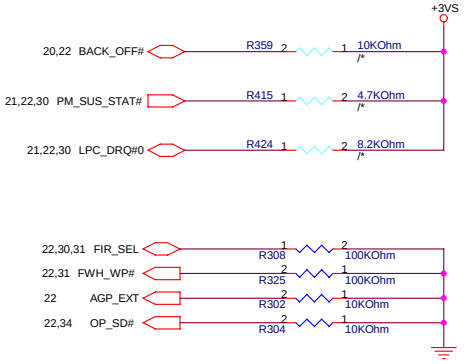


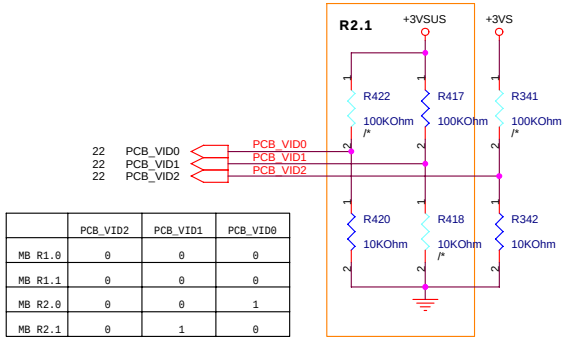












	PCB_VID2	PCB_VID1	PCB_VID0
MB R1.0	0	0	0
MB R1.1	0	0	0
MB R2.0	0	0	1
MB R2.1	0	1	0

INTERNAL PULL-DOWN SIGNALS :

AC_BITCLK, AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , PDDREQ , SPKR , USB[7:0][P,N]

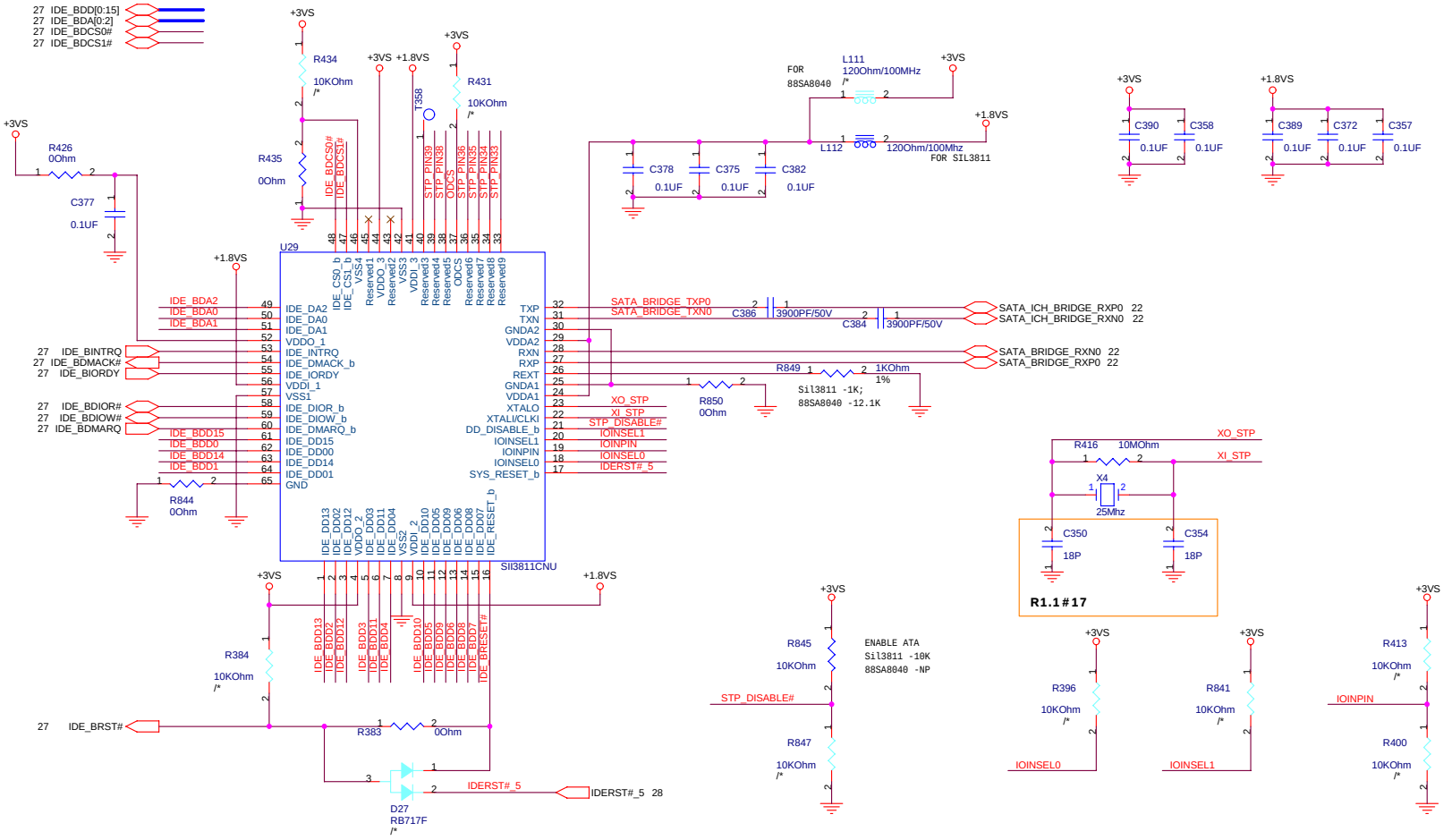
INTERNAL PULL-UP SIGNALS :

EE_DIN , EE_DOUT , EE_CS , GPIO[17:16] , LAD[3:0]# , LDRQ[0:1] , LAN_RXD[2:0] , PME# , PWRBTN# , TP3 , SATALED# , GNT[4:0]

bom

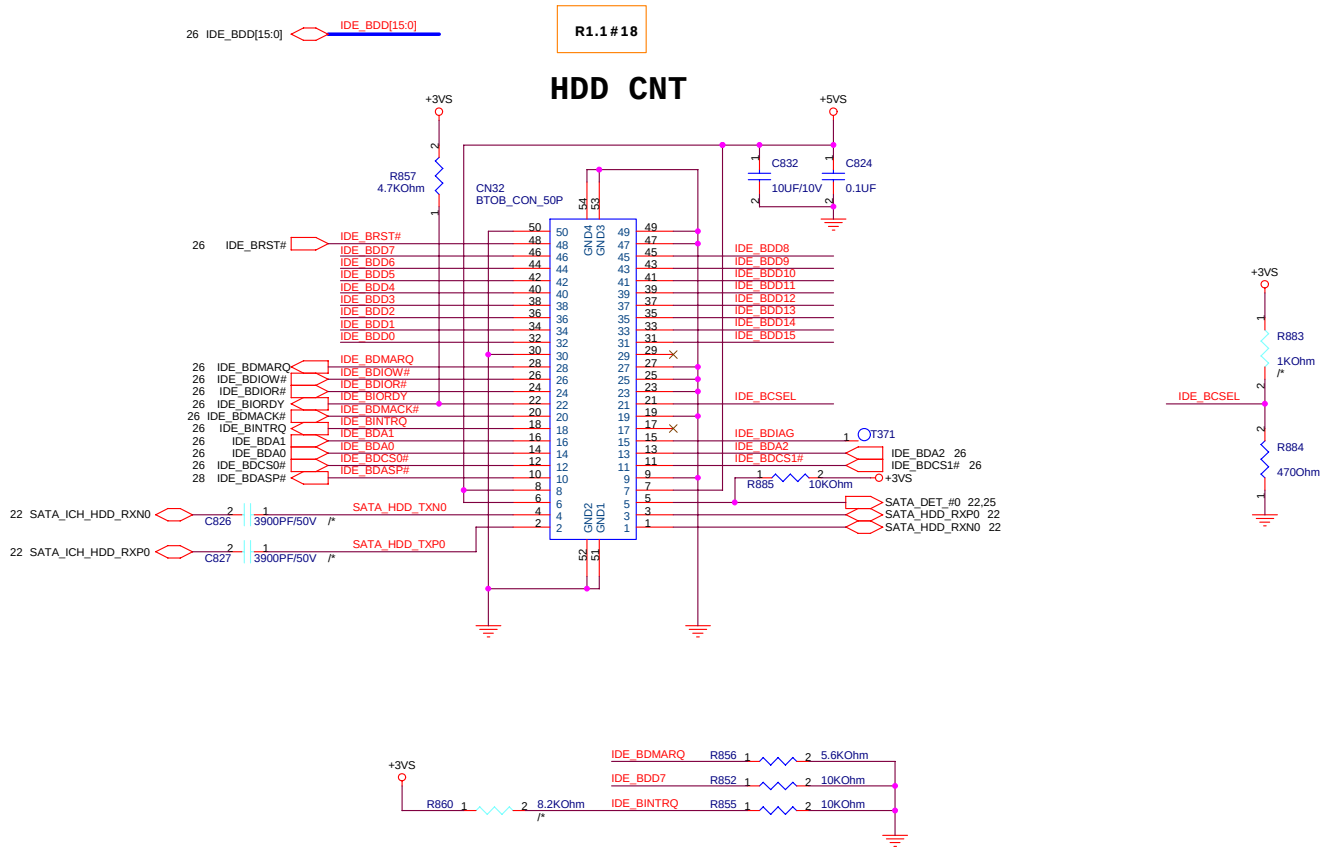
PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005** SHEET **25** OF **63**	DESCRIPTION: ***ICH6M:Res & Straps***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**

DESIGN ENGINEER : ***M.Y.***



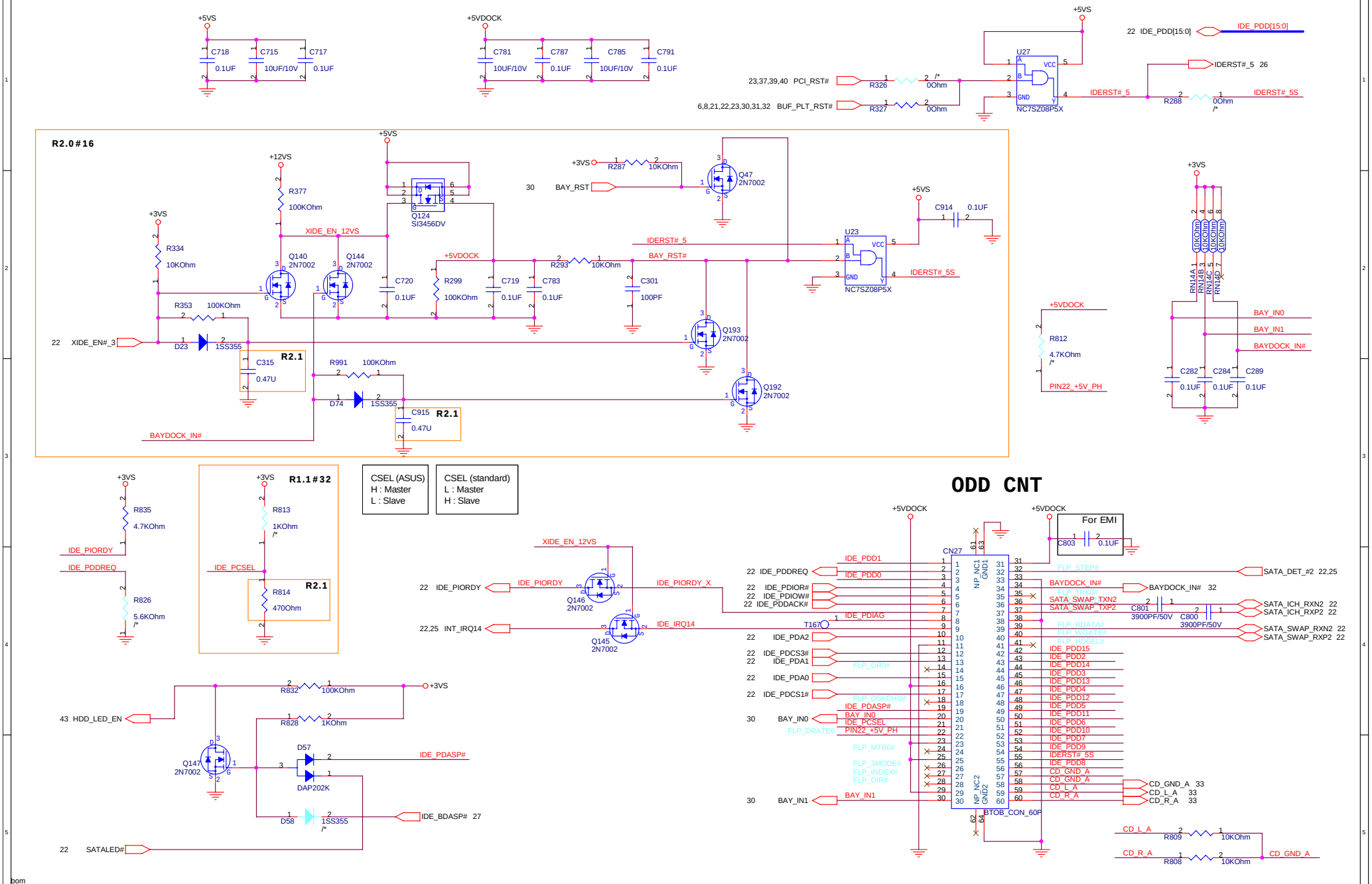
bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***SATA TO PATA BRIDGE***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***M.Y.***
		SHEET **26** OF **63**		RELEASE DATE :	



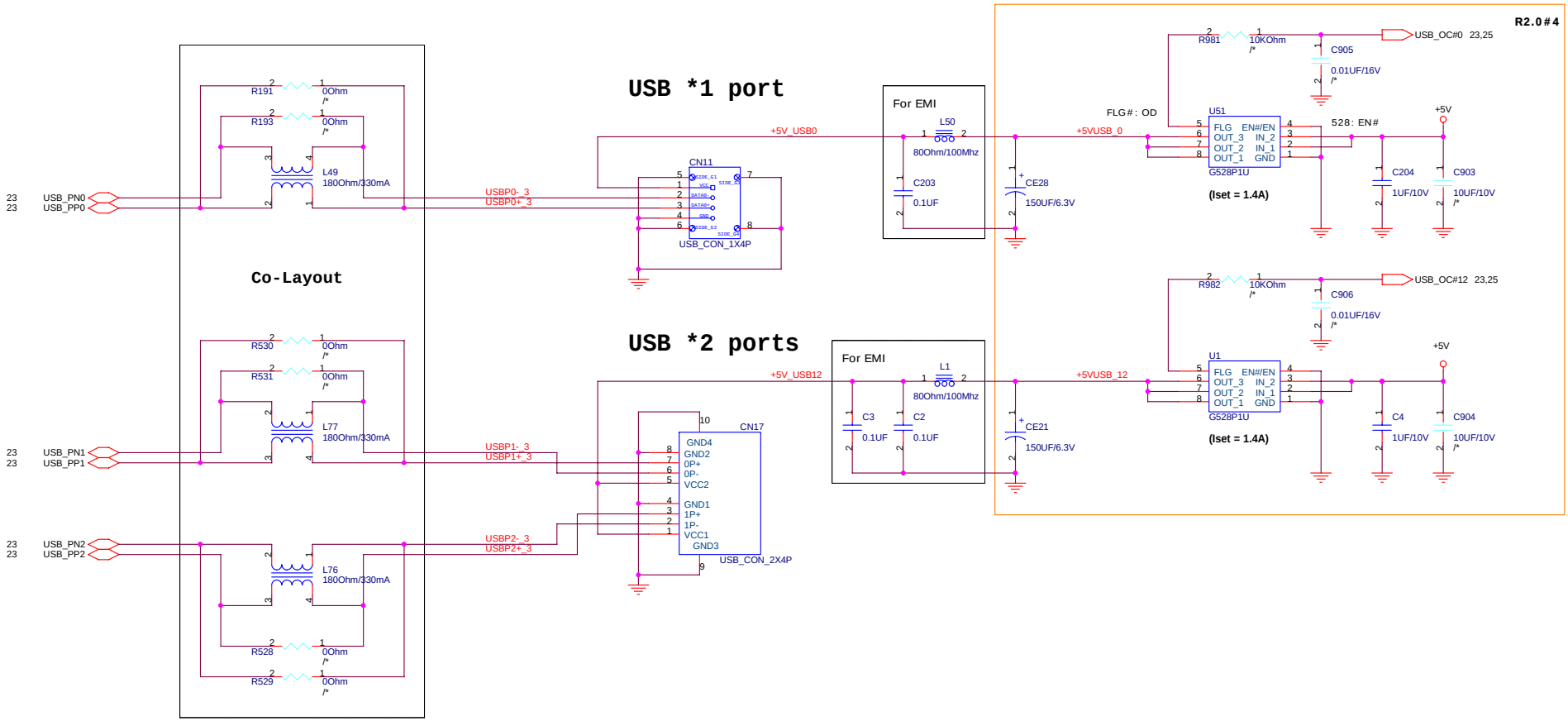
bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***HDD CON.***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***M.Y.***
		SHEET **27** OF **63**		RELEASE DATE :	



bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005** SHEET **28** OF **63**	DESCRIPTION: ***SWAP BAY***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***M.Y.***

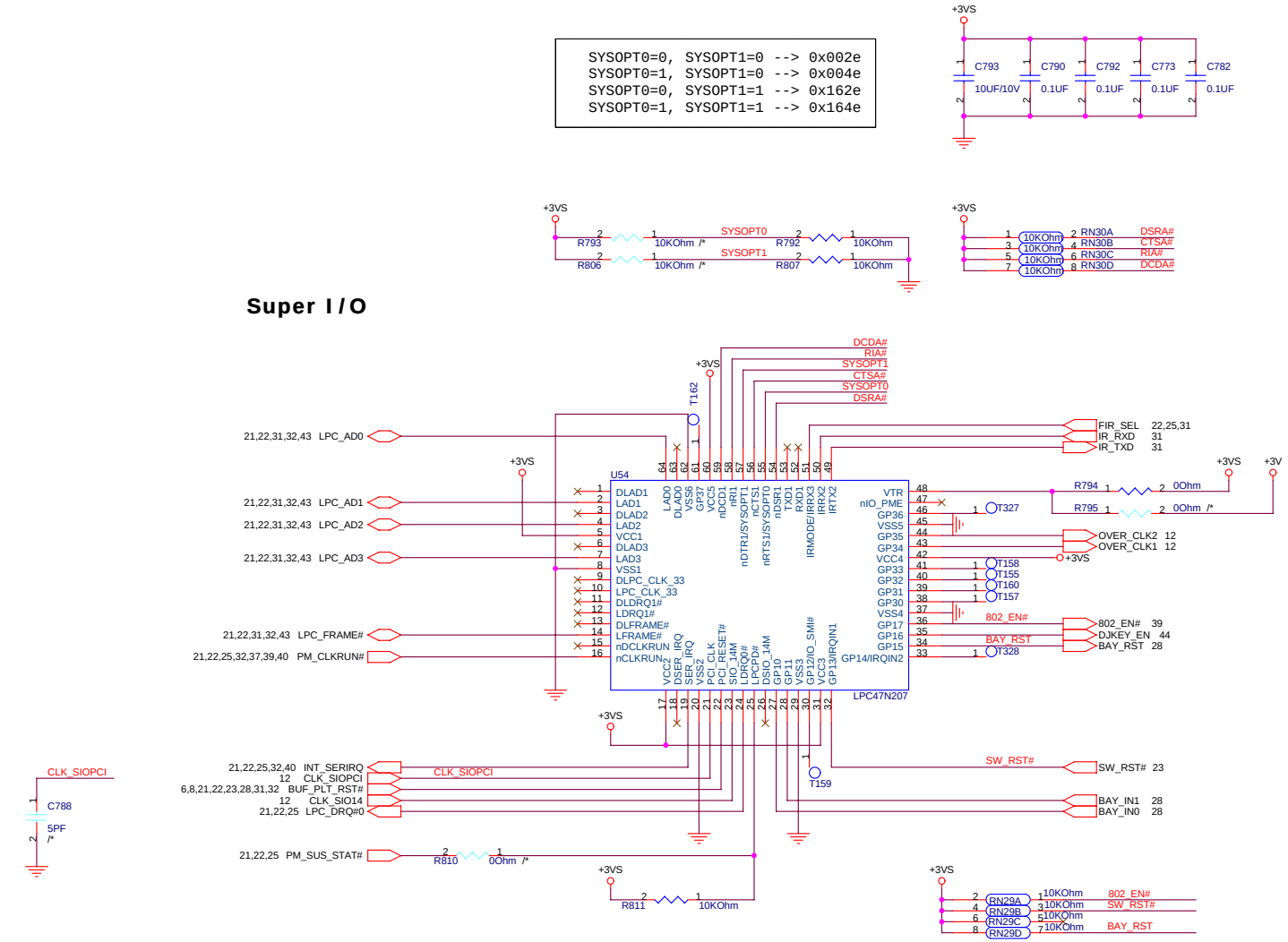


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***USB PORTS***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***M.Y.***
		SHEET **29** OF **63**		RELEASE DATE:	

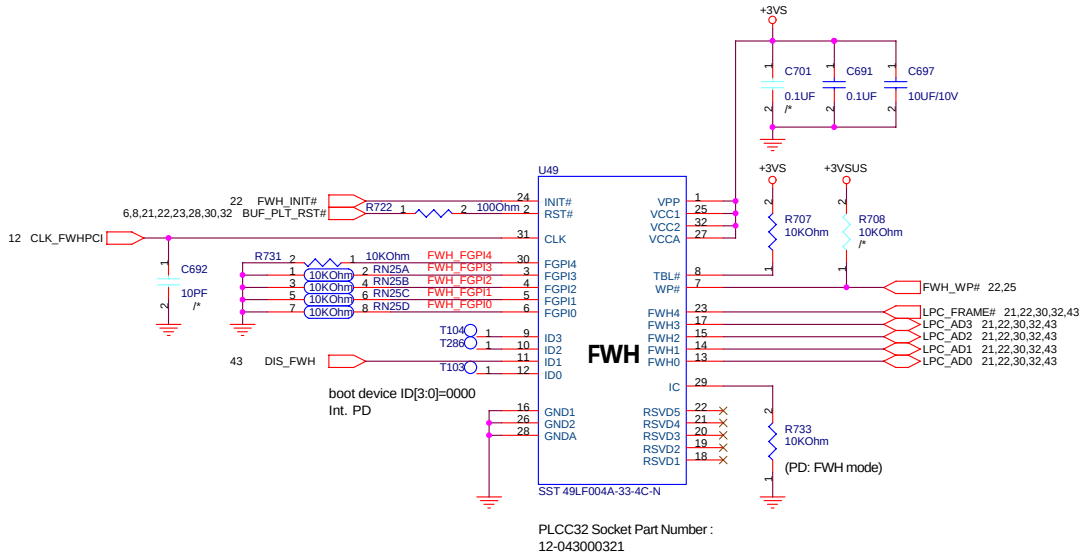
SYSOPT0=0, SYSOPT1=0 --> 0x002e
SYSOPT0=1, SYSOPT1=0 --> 0x004e
SYSOPT0=0, SYSOPT1=1 --> 0x162e
SYSOPT0=1, SYSOPT1=1 --> 0x164e

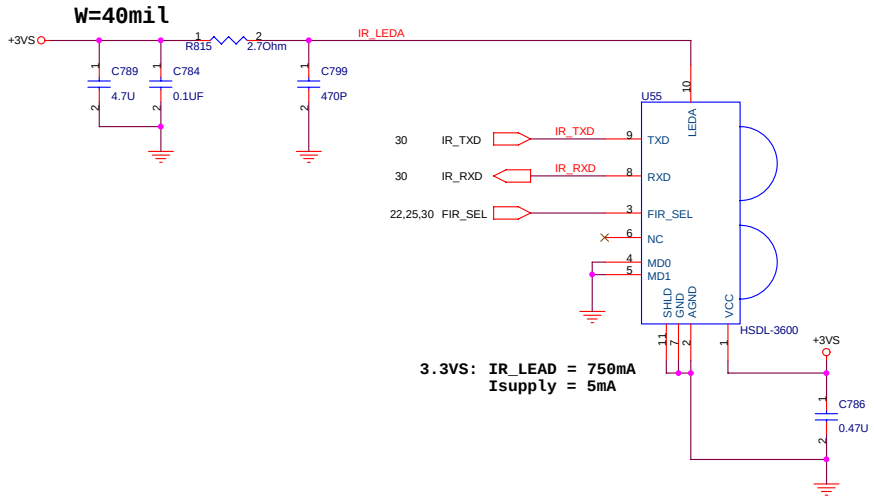
Super I/O



bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***SUPER I/O (LPC47N207)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
		SHEET **30** OF **63**		RELEASE DATE :	





bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: Monday, January 17, 2005	DESCRIPTION: ***FIR & FWH***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Alice Shih***
		SHEET **31** OF **63**		RELEASE DATE:	

KEYBOARD CON.

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

R2.0#5

R1.1#29

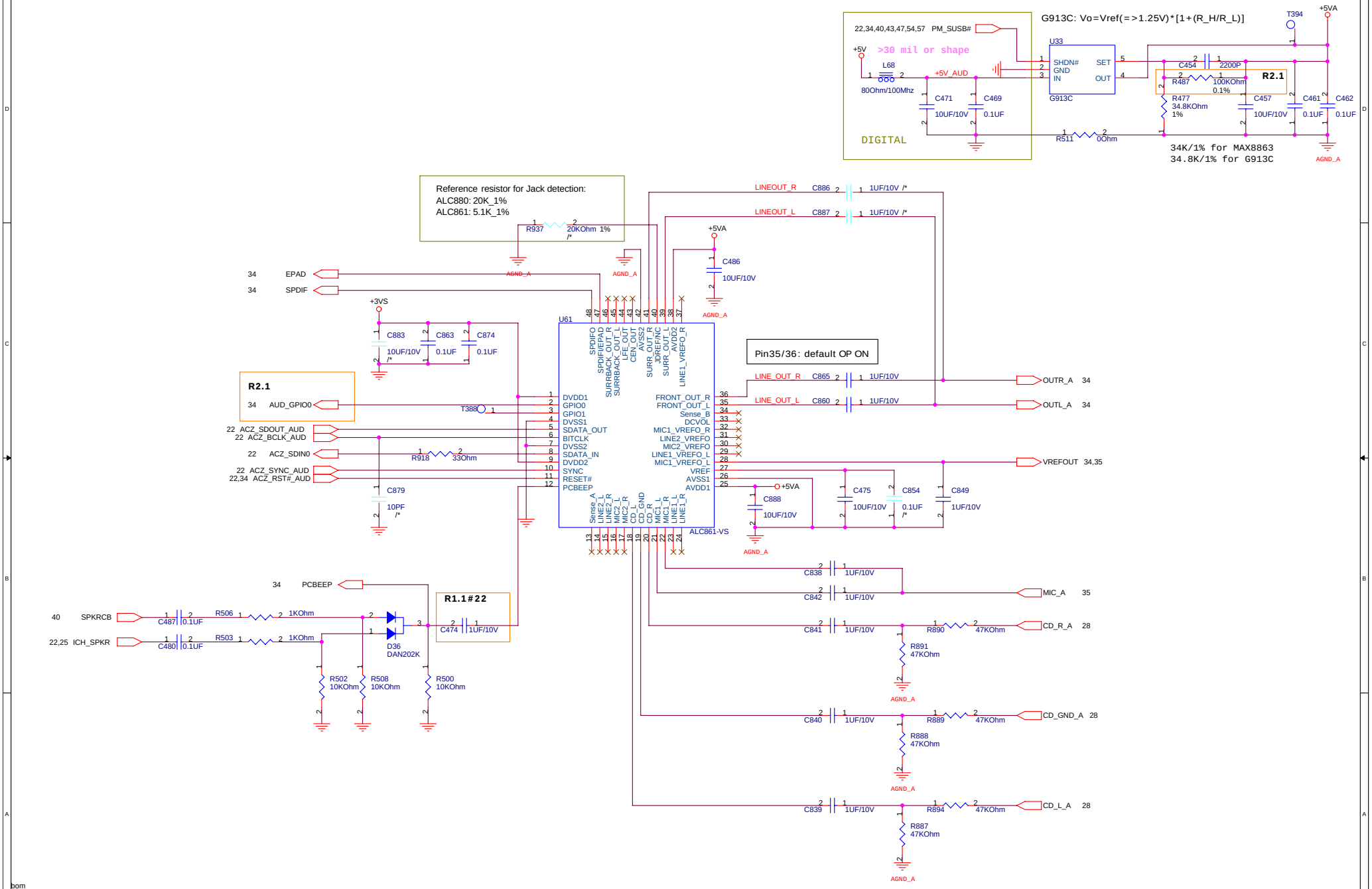
R1.1#17

U8 M38857 80mA

U10 PI5C3257

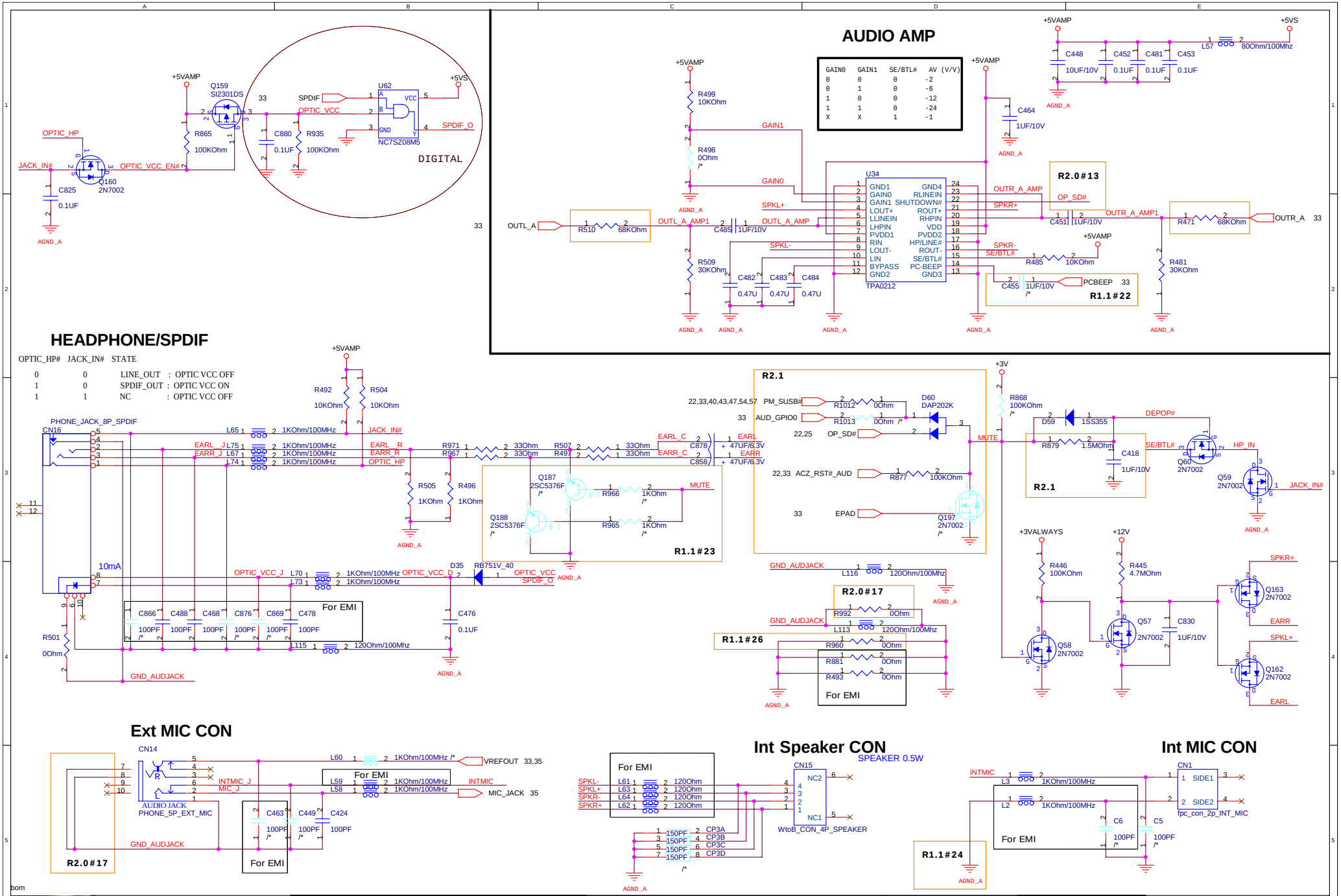
PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005
	SHEET 32 OF 63	DESCRIPTION: KBC (M38857)
	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : M.Y.
	RELEASE DATE :	

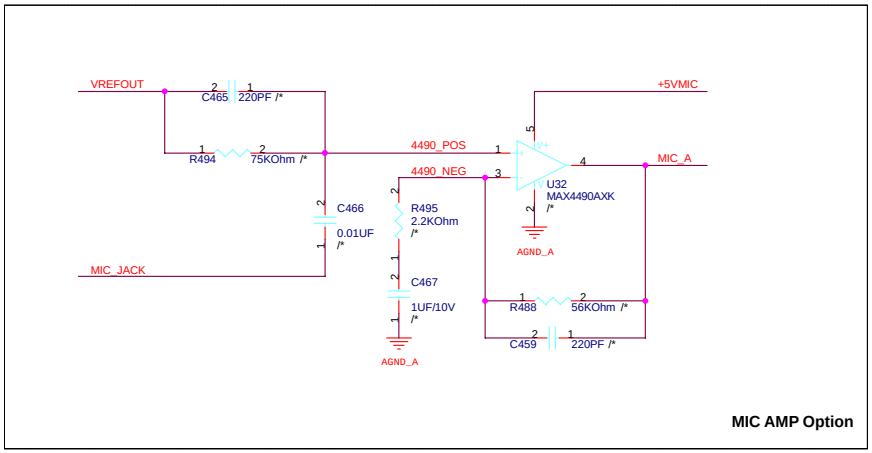
bom

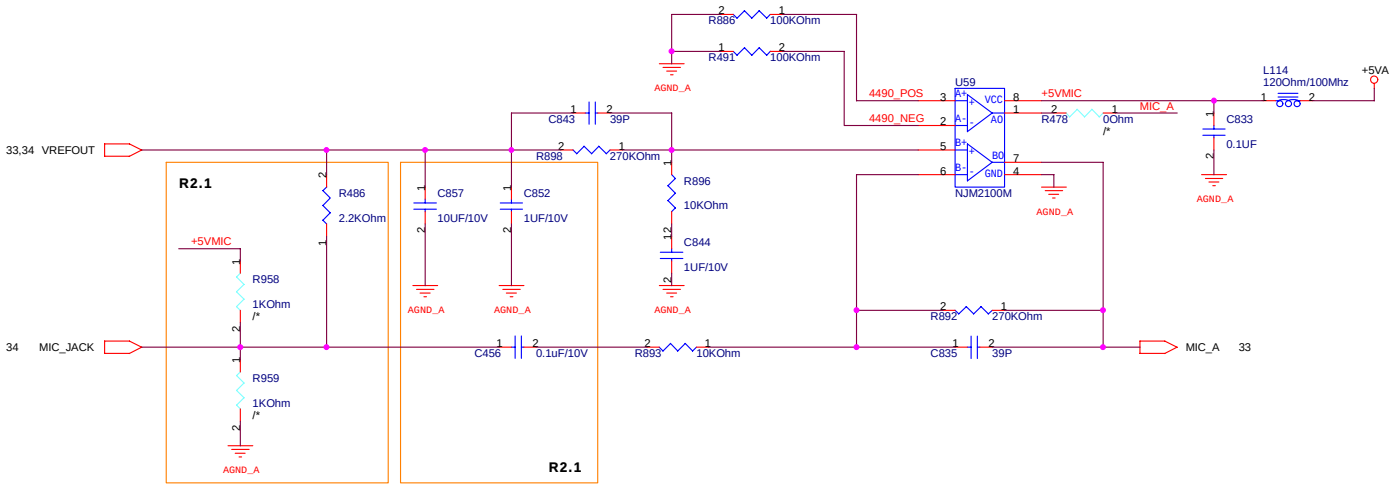


bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: Monday, January 17, 2005	DESCRIPTION: ***Azalia AUDIO (ALC861-VS)***	SCHEMATIC FILE NAME:	**<OrgName>**	DESIGN ENGINEER: ***Alice Shih***
		SHEET **33** OF **63**		RELEASE DATE:		


AUDIO AMP
HEADPHONE/SPDIF
Ext MIC CON
Int Speaker CON
Int MIC CON
DIGITAL
SPEAKER 0.5W
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 17, 2005
SHEET 34 OF 63
DESCRIPTION: AUDIO AMP / JACKS
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Alice Shih



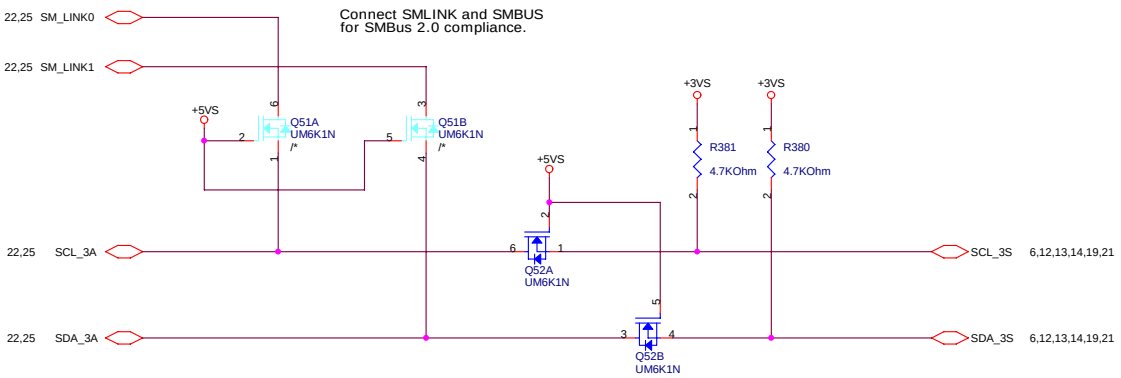


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: Monday, January 17, 2005	DESCRIPTION: ***MIC AMP***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
		SHEET **35** OF **63**		RELEASE DATE :	

ICH6-M

ICH6-M

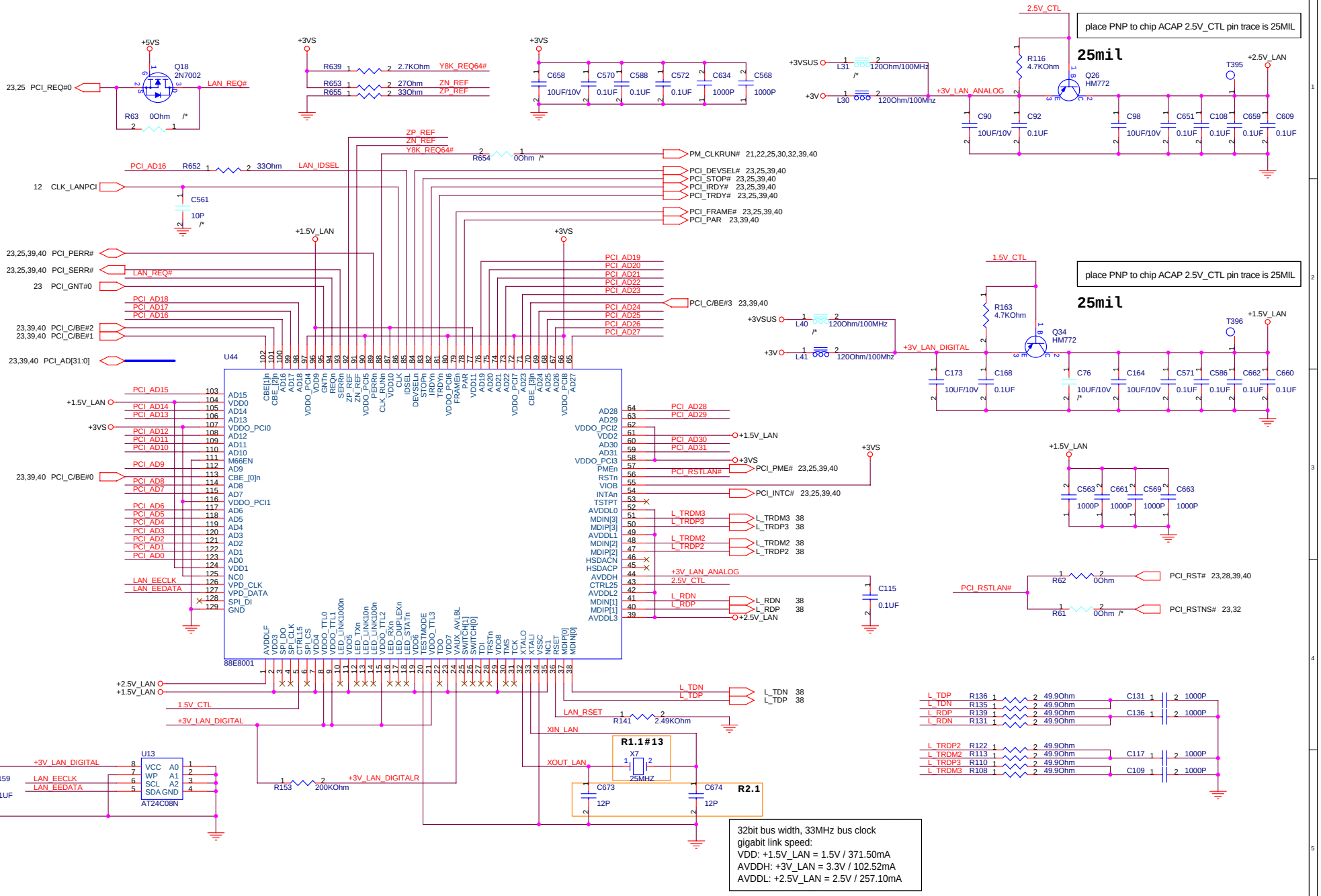


System Thermal Sensor
ATI Thermal Sensor
Clock Generator
DDR2 SO-DIMM
TPM

+3VALWAYS	+3VALWAYS	21,22,32,34,43,44,45,47,48,50,51,57
+3VSUS	+3VSUS	20,22,24,25,31,32,37,45,47,53,57
+5VALWAYS	+5VALWAYS	48,51,53
+5VSUS	+5VSUS	24,57
+1.5VSUS	+1.5VSUS	24,53
+3V	+3V	20,23,30,32,34,37,38,39,40,41,42,43,44,47,48,53,57
+5V	+5V	13,21,29,32,33,41,43,44,45,48,52,56,57
+12V	+12V	34,42,57
+3VS	+3VS	6,10,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,30,31,32,33,37,38,39,40,43,45,47,48,49,52,53,54,57
+5VS	+5VS	21,24,27,28,32,34,37,39,43,45,46,48,57
+12VS	+12VS	20,21,28,44,57
+VCORE	+VCORE	5,6,49
+VCCP	+VCCP	4,5,6,7,10,12,22,24,48,53
+1.2VSP	+1.2VSP	18,52
+2.5VS	+2.5VS	6,8,10,11,18,20,21,24,48,51,52
+1.8VS	+1.8VS	4,16,17,18,26,48,52,53,57
+0.9VS	+0.9VS	15,53
+1.5VS	+1.5VS	4,8,10,18,23,24,48,51
+VCC_RTC	+VCC_RTC	22,24
+1.8V	+1.8V	8,10,11,13,14,40,51,53
+VCC_GMCH_CORE	+VCC_GMCH_CORE	8,10,11,53
+VCCCB	+VCCCB	40,41
+VPPCB	+VPPCB	41
VTT_REF	VTT_REF	8,13,14,15
A/D_DOCK_IN	A/D_DOCK_IN	46,55,56
+ATI_VCORE	+ATI_VCORE	18,52

bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***SMBUS***	SCHEMATIC FILE NAME:	**<OrgName>**	DESIGN ENGINEER: ***M.Y.***
		SHEET **36** OF **63**		RELEASE DATE:		

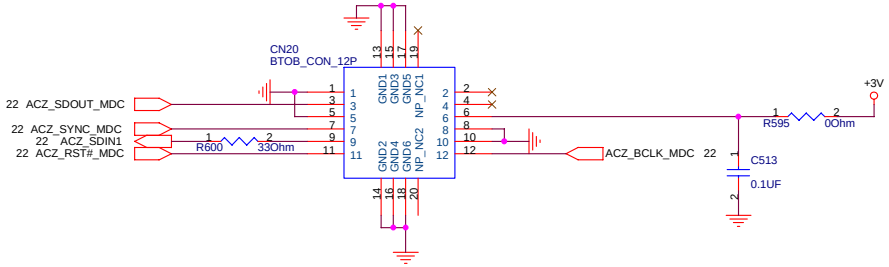


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***PCI GIGA LAN (88E8001)***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
		SHEET **37** OF **63**		RELEASE DATE :		

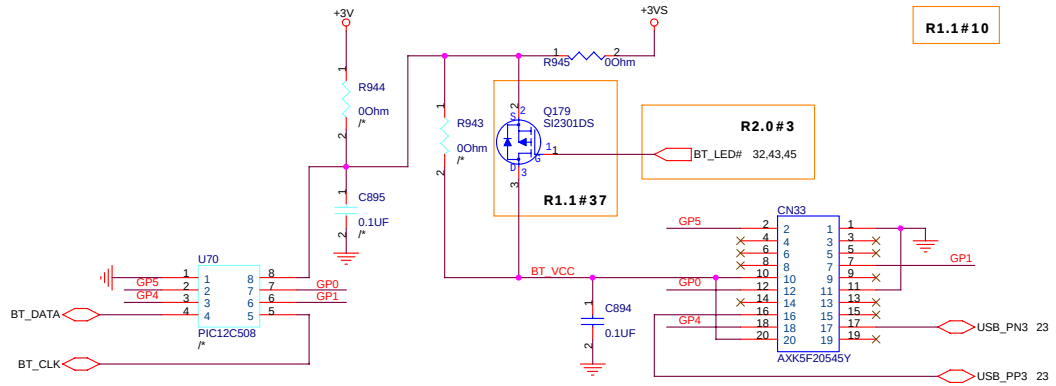
Azalia MDC MODEM

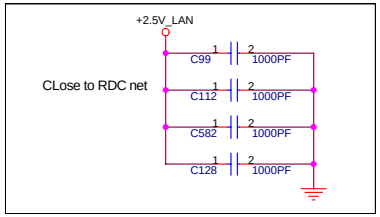
[ACZ_SDOUT/SYNC/BITCLK/RST#]:
ICH6: 39 ohm to Audio / 39 ohm to MDC
[ACZ_SDIN]:
Audio 33 ohm to ICH6 / MDC 33 ohm to ICH6



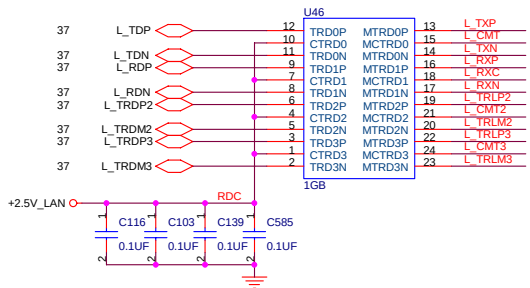
BT

R1.1#10

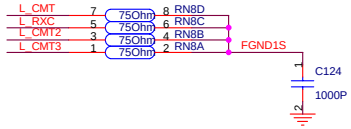


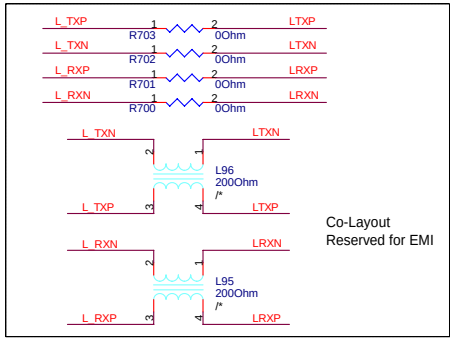


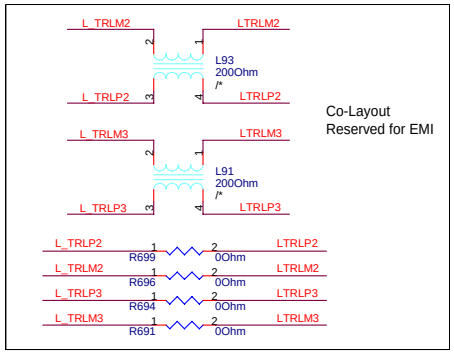
PLACE NEAR RJ45



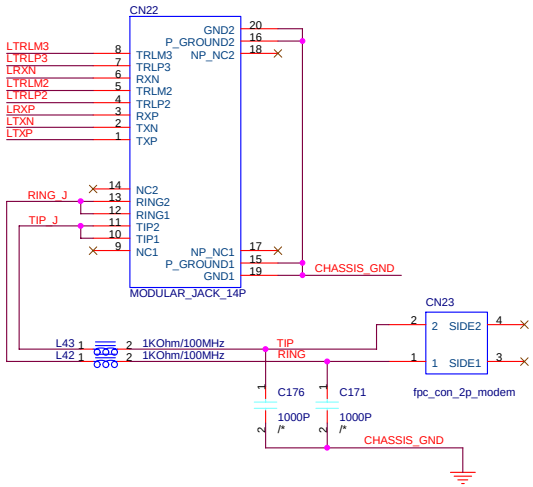
PLACE NEAR TRANSFORMER





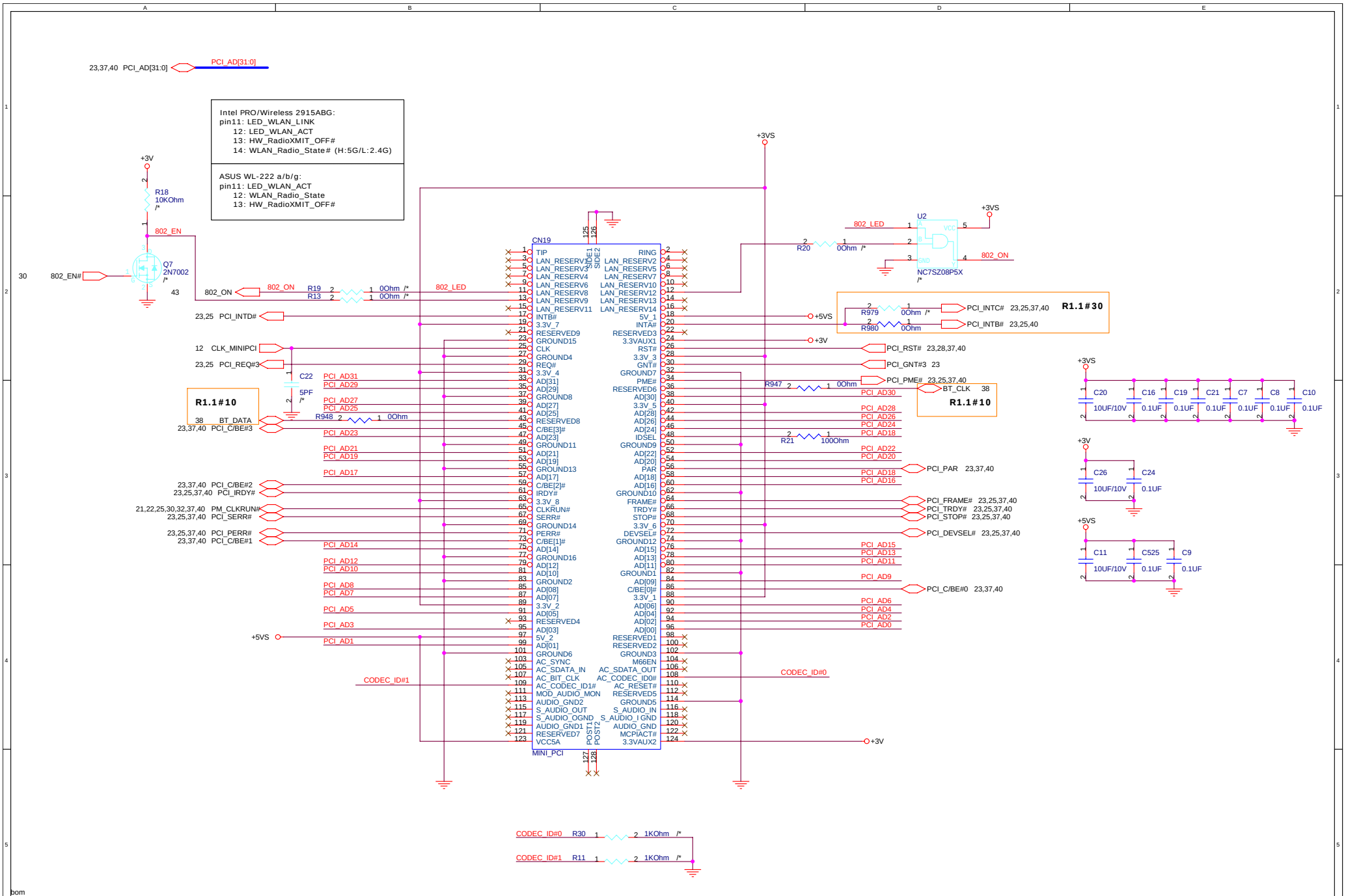


RJ11+RJ45



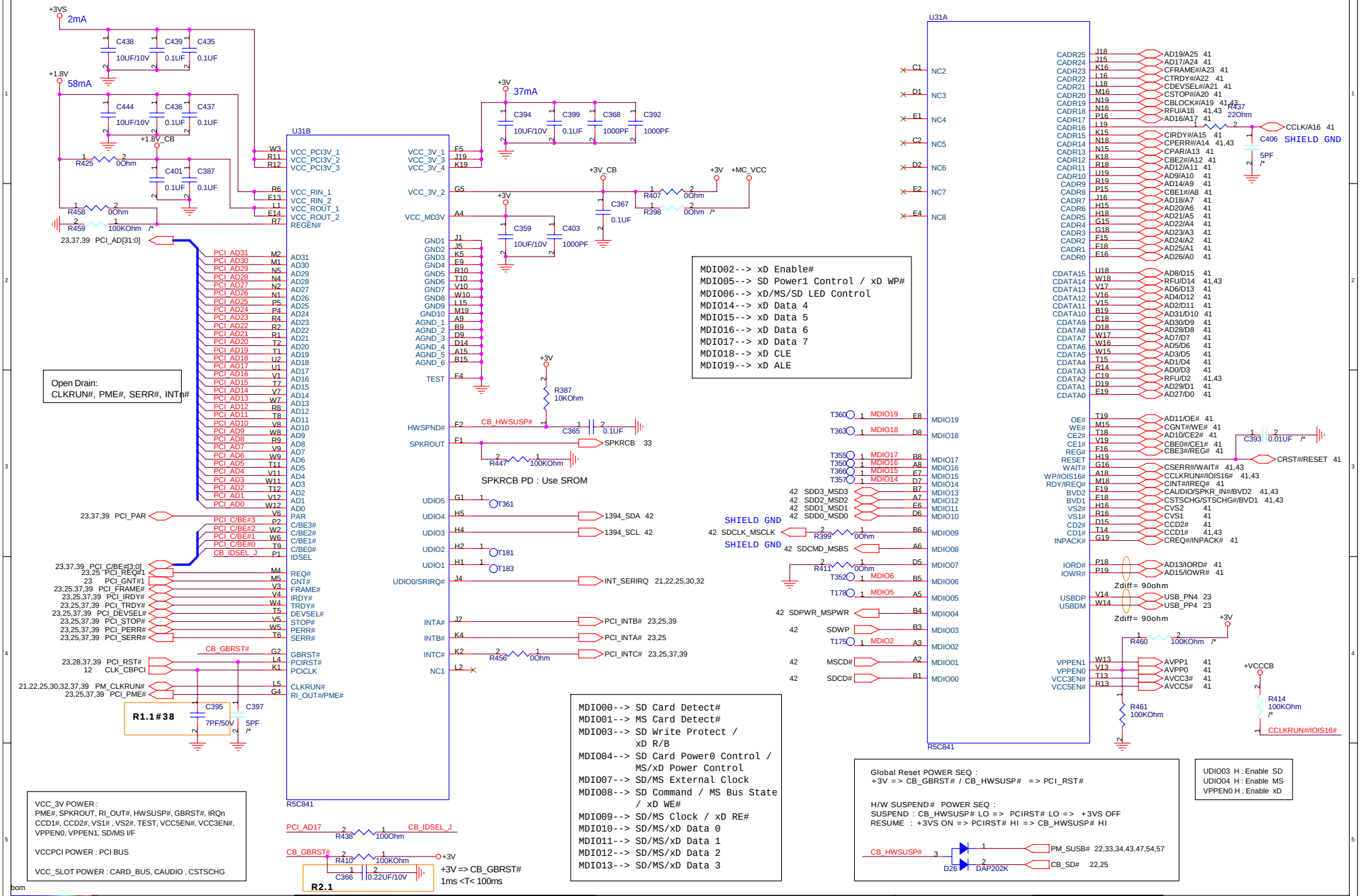
PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 38 OF 63	DESCRIPTION: RJ11+RJ45 / MDC	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName>	DESIGN ENGINEER : Alice Shih

bom

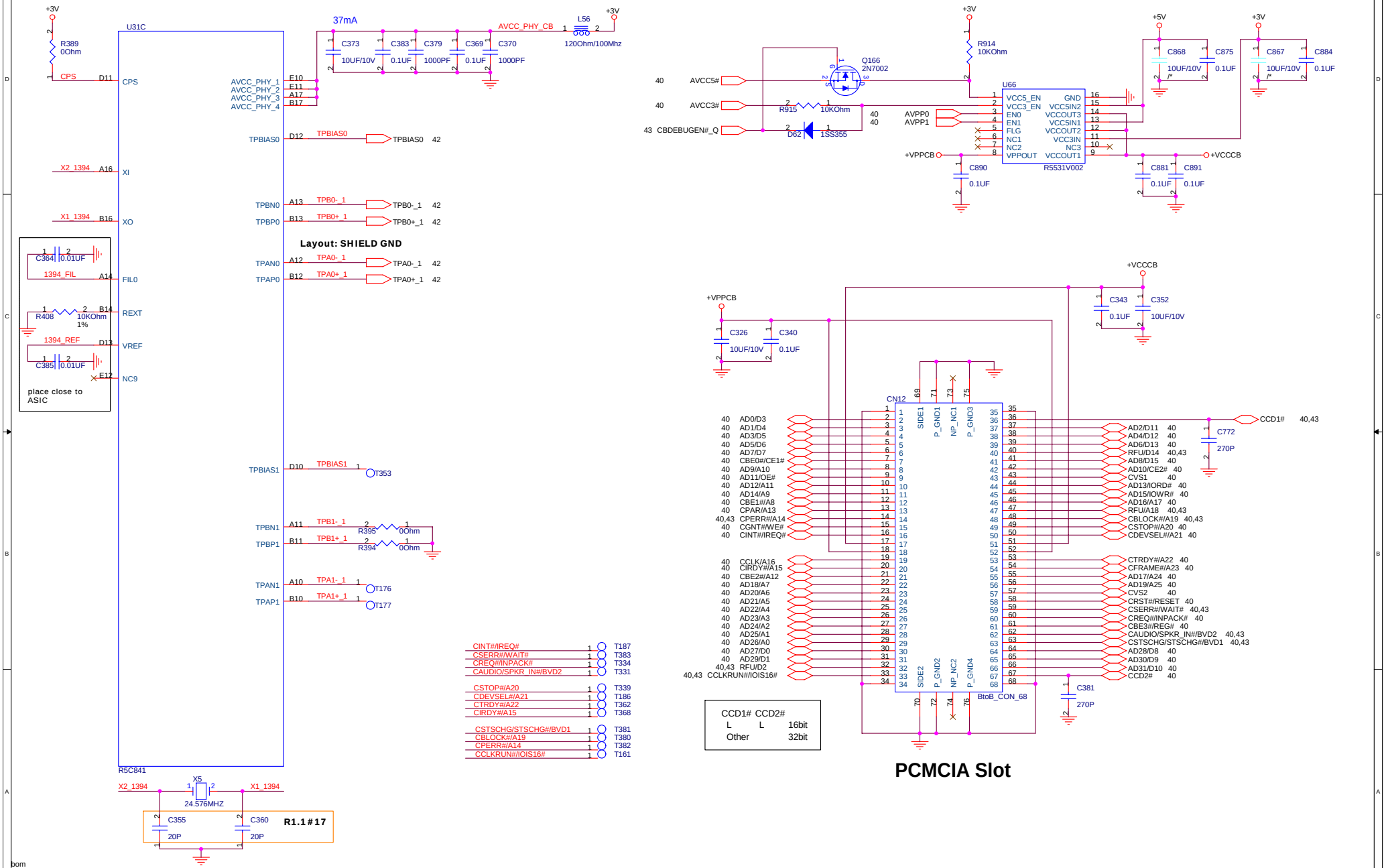


bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	SHEET **39** OF **63**	DESCRIPTION: ***MINIPCI***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
					RELEASE DATE :		

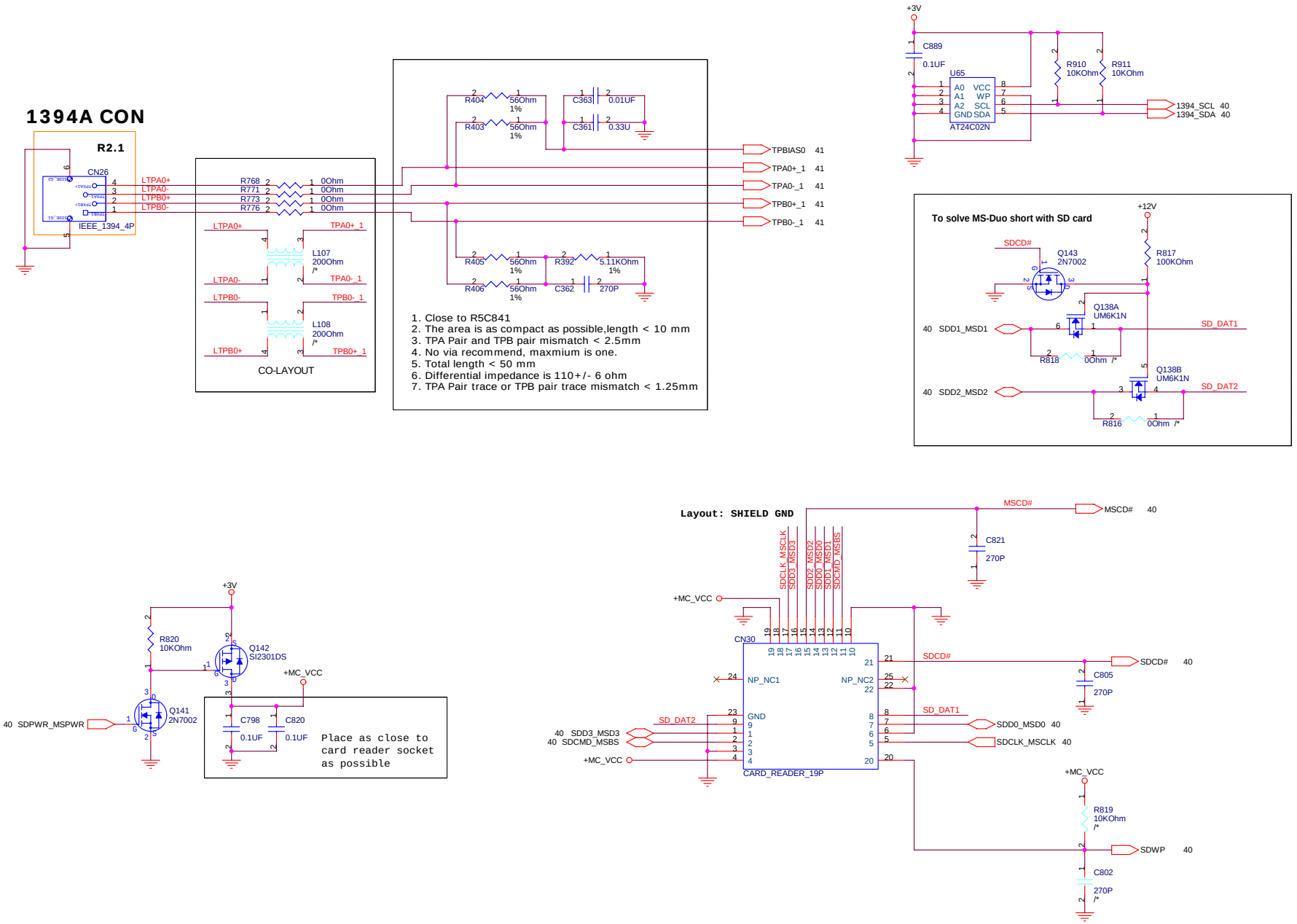


PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 40 OF 63	DESCRIPTION: PCI CARDBUS (R5C841)	SCHEMATIC FILE NAME : <OrgName>	RELEASE DATE :	DESIGN ENGINEER : Alice Shih



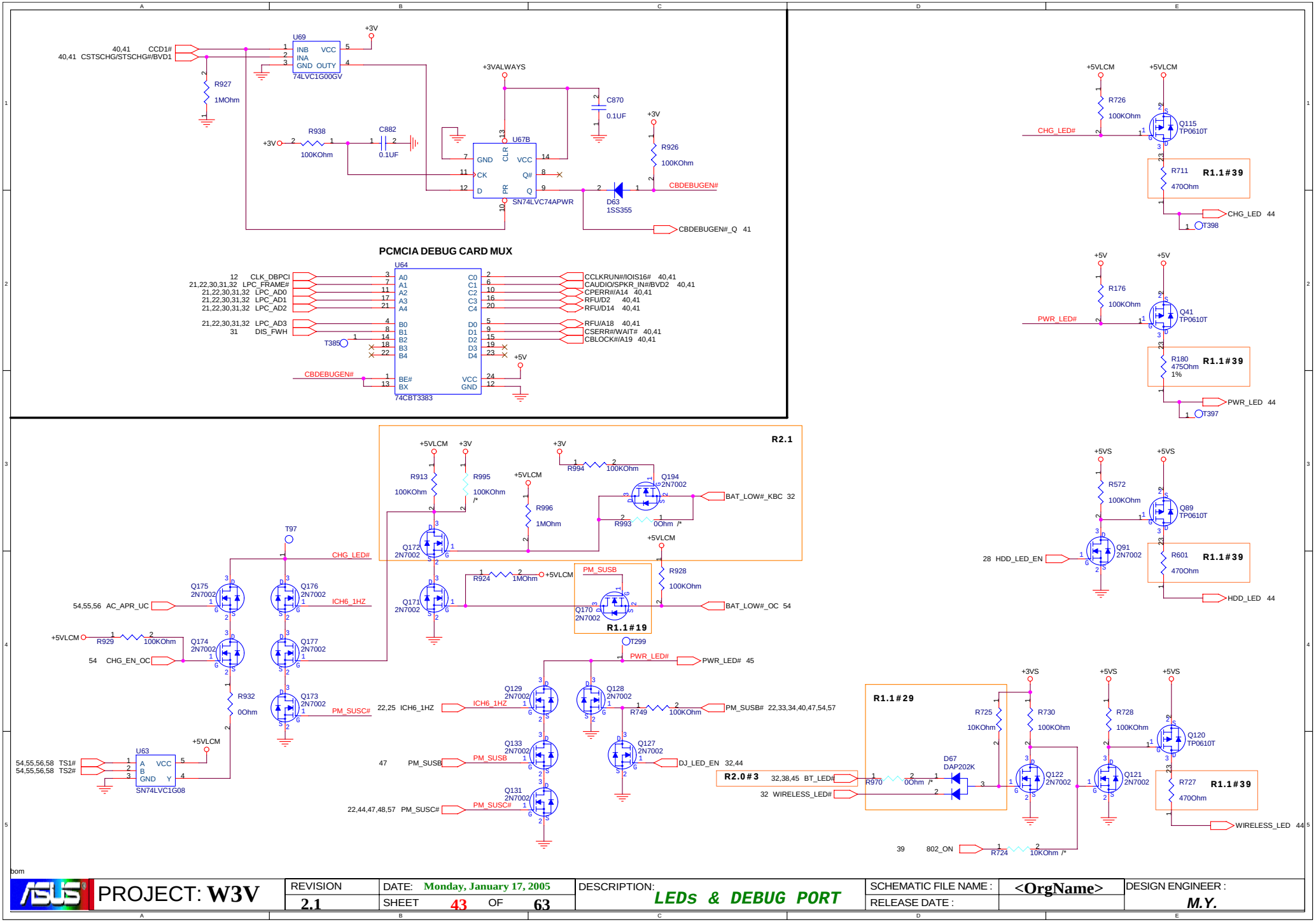
PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005**	DESCRIPTION: ***CARDBUS SOCKET***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
		SHEET **41** OF **63**		RELEASE DATE :	

bom



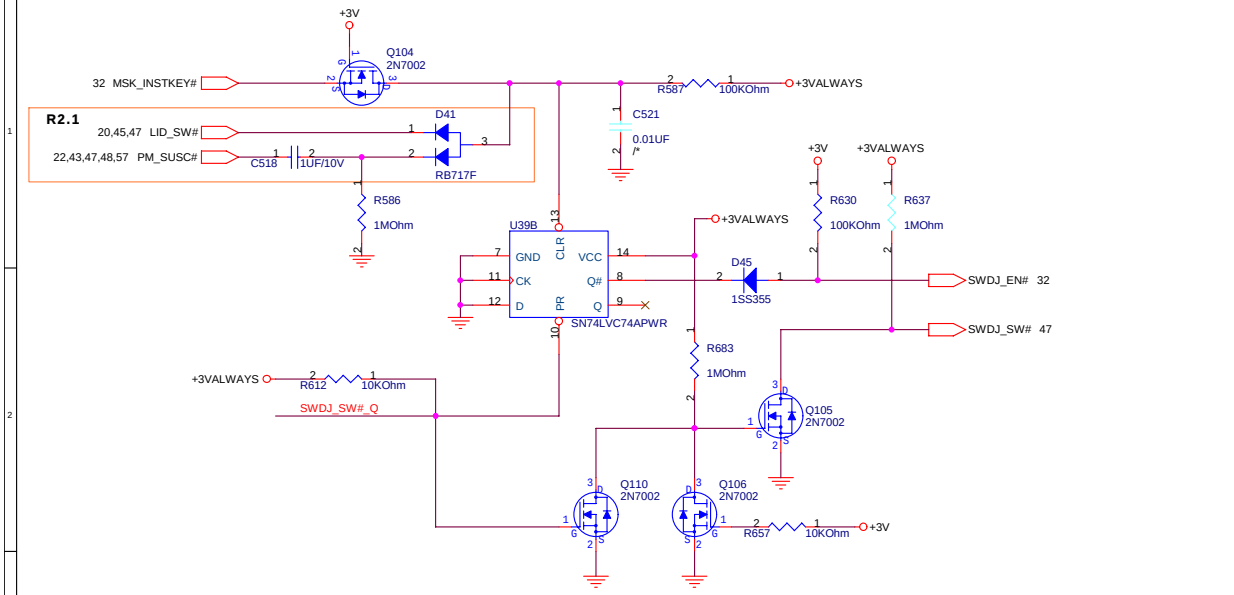
bom

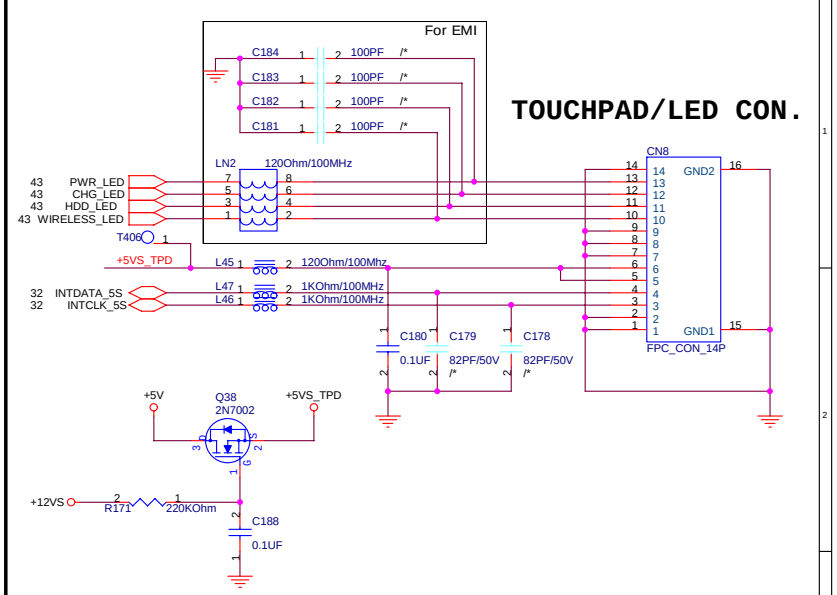
PROJECT: **W3V**	REVISION **2.1**	DATE: Monday, January 17, 2005	DESCRIPTION: ***IEEE1394A / 3in1 CONN***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Alice Shih***
		SHEET **42** OF **63**		RELEASE DATE :	

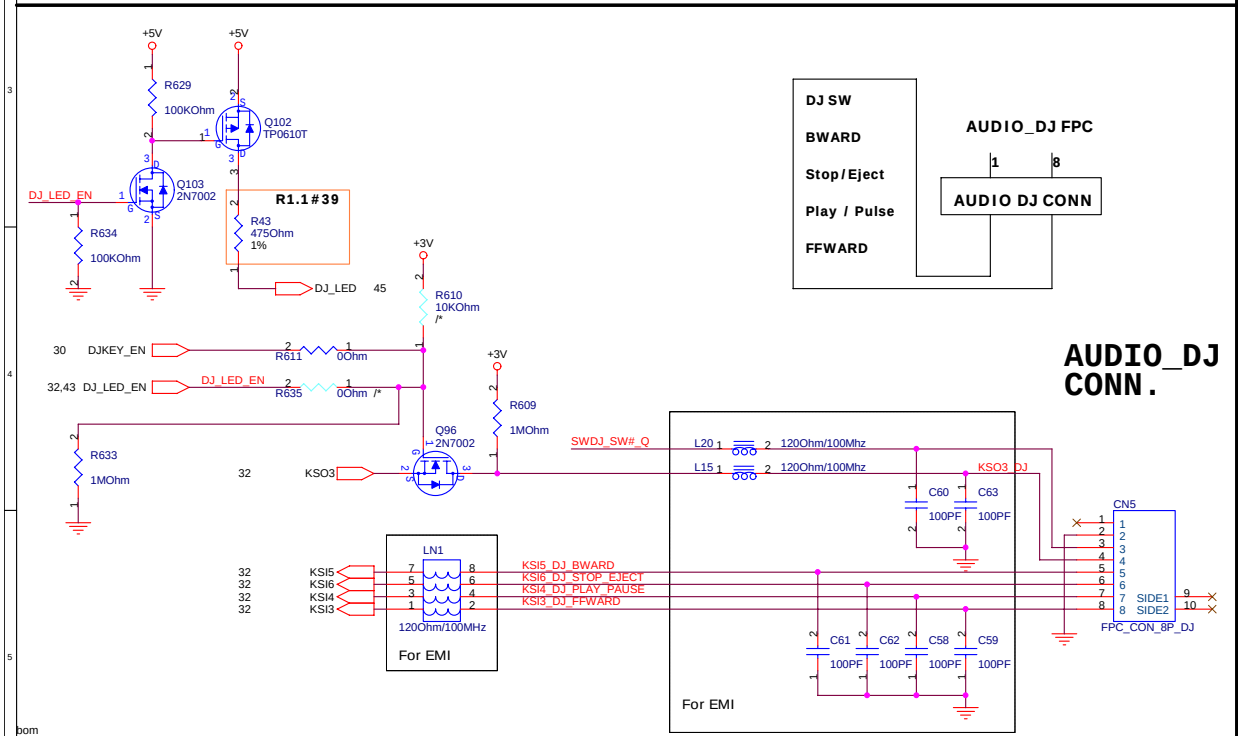


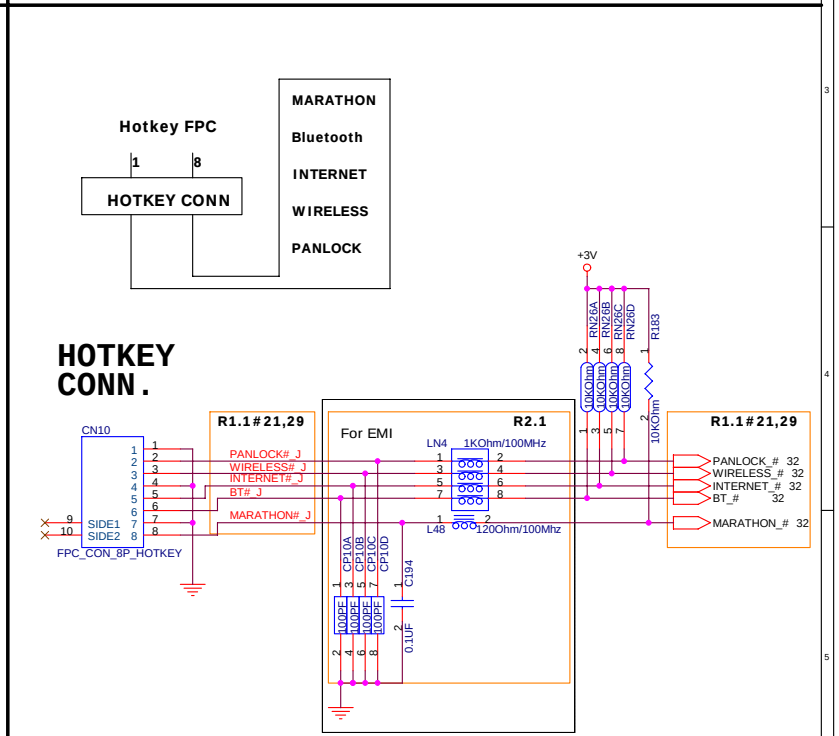
bom

PROJECT: W3V	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 43 OF 63	LEDs & DEBUG PORT	RELEASE DATE :	M.Y.



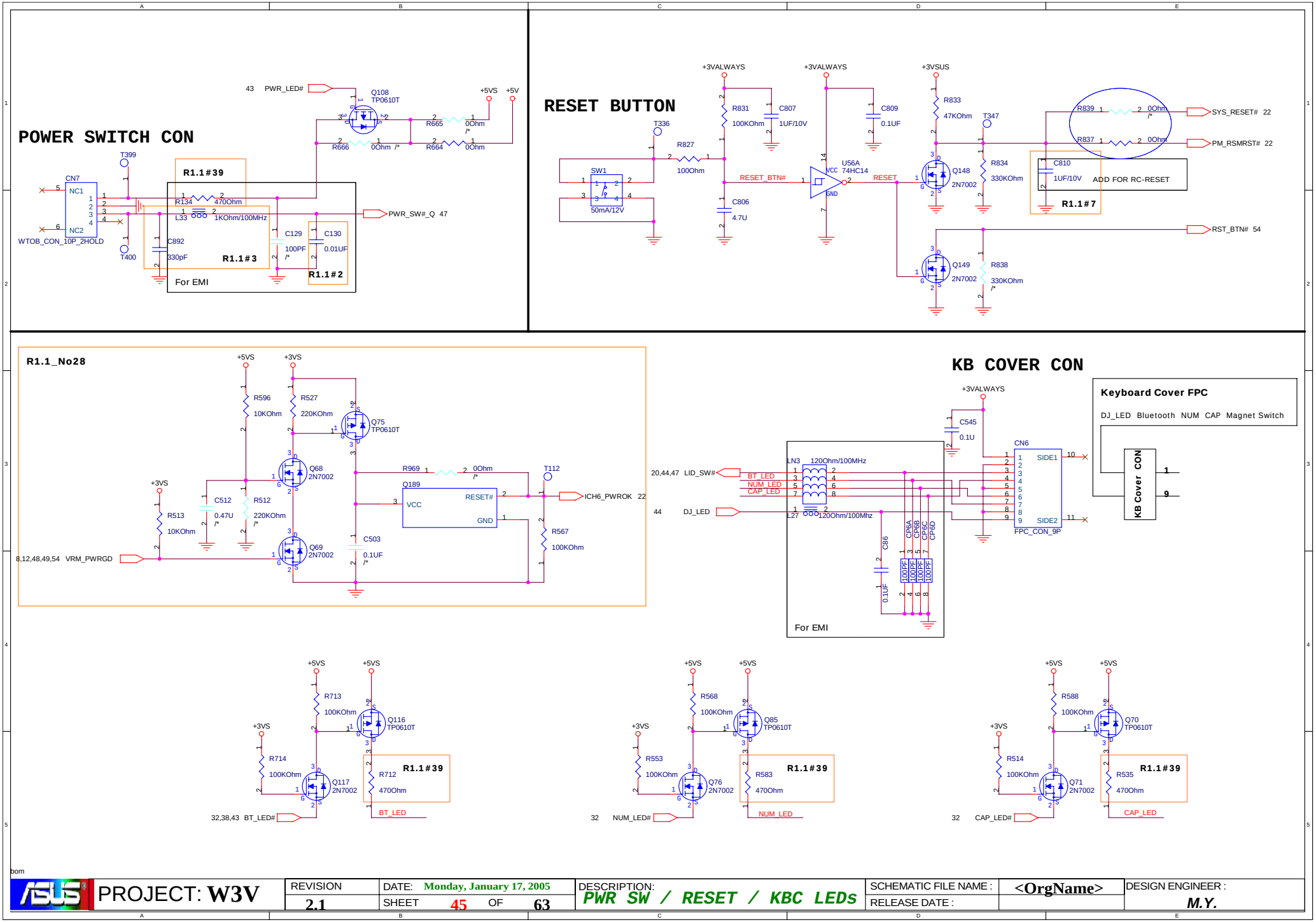






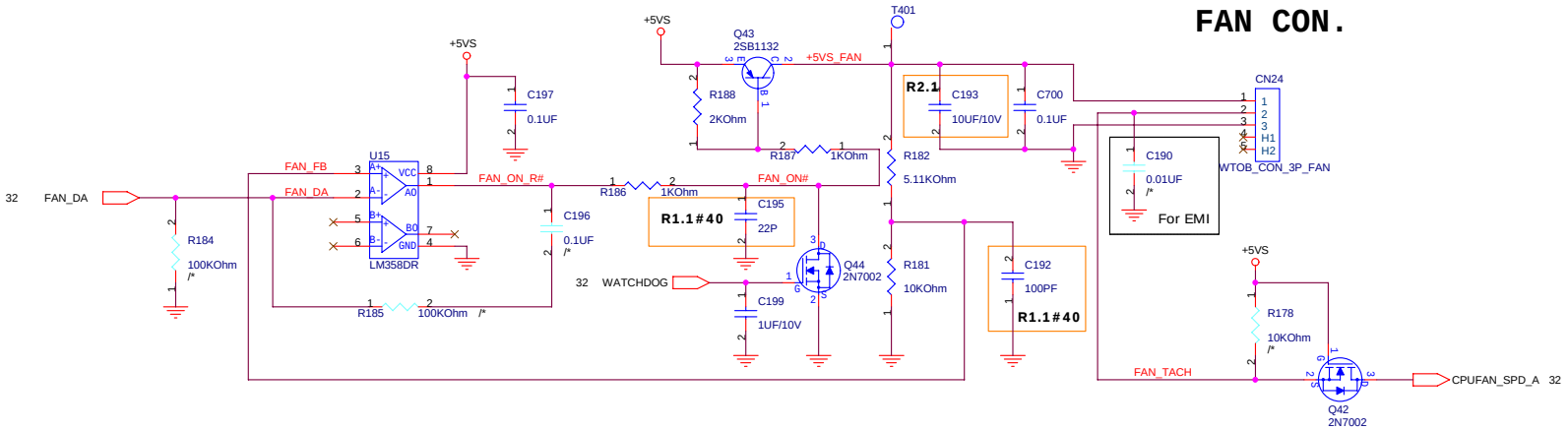
bom

PROJECT: W3V	REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 44 OF 63	AUDIO DJ/ HOTKEY/ TP+LEDs	RELEASE DATE :	M.Y.



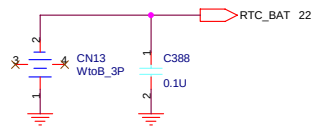
PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	DESCRIPTION: PWR SW / RESET / KBC LEDs	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : M.Y.
		SHEET 45 OF 63		RELEASE DATE :	

FAN CON.



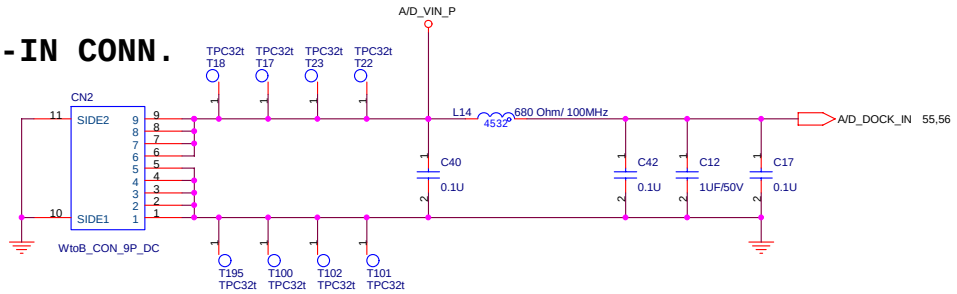
FAN CONTROL

RTC BAT CON.



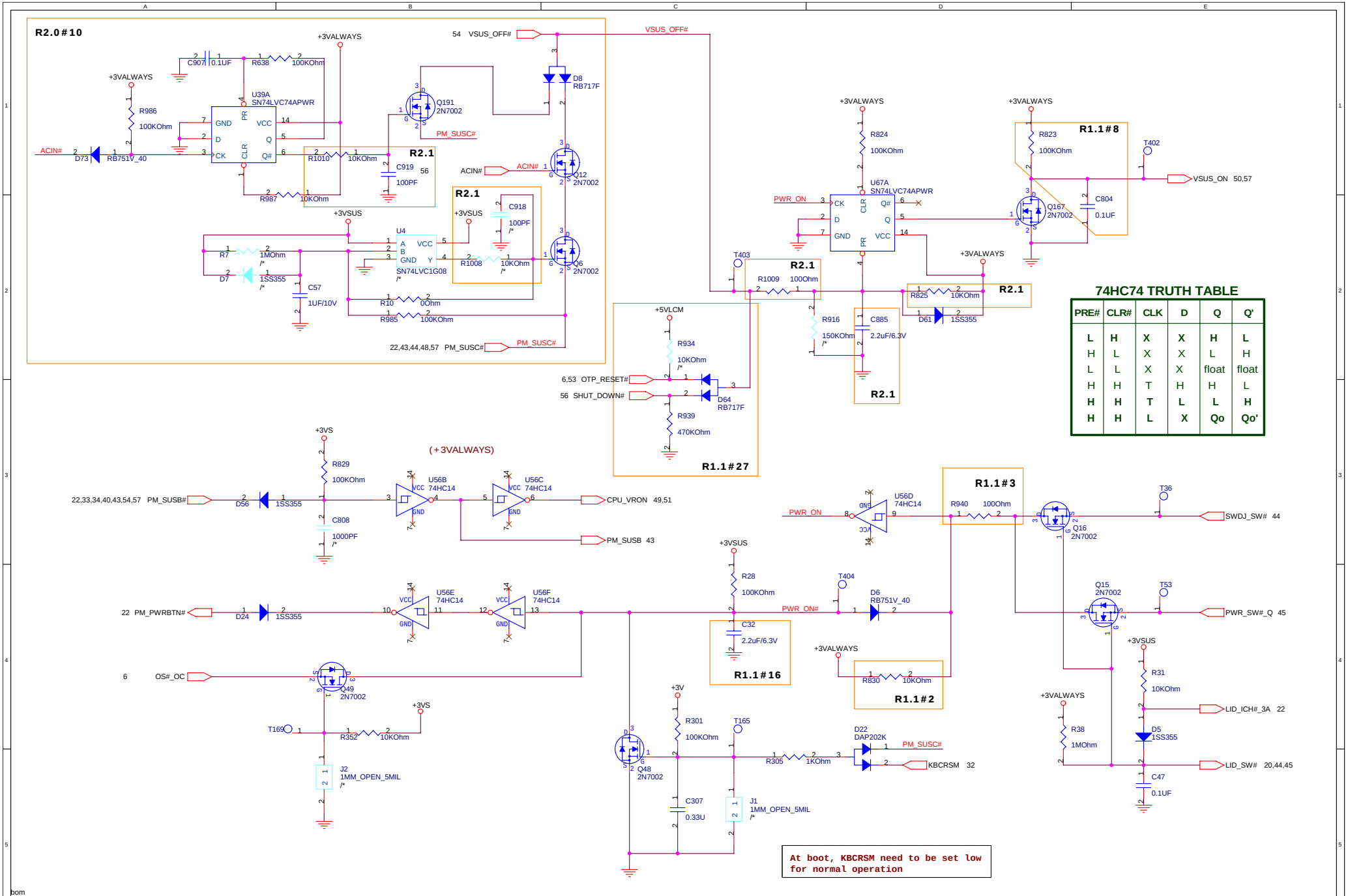
RTC Battery
P/N=07-016322032

DC-IN CONN.



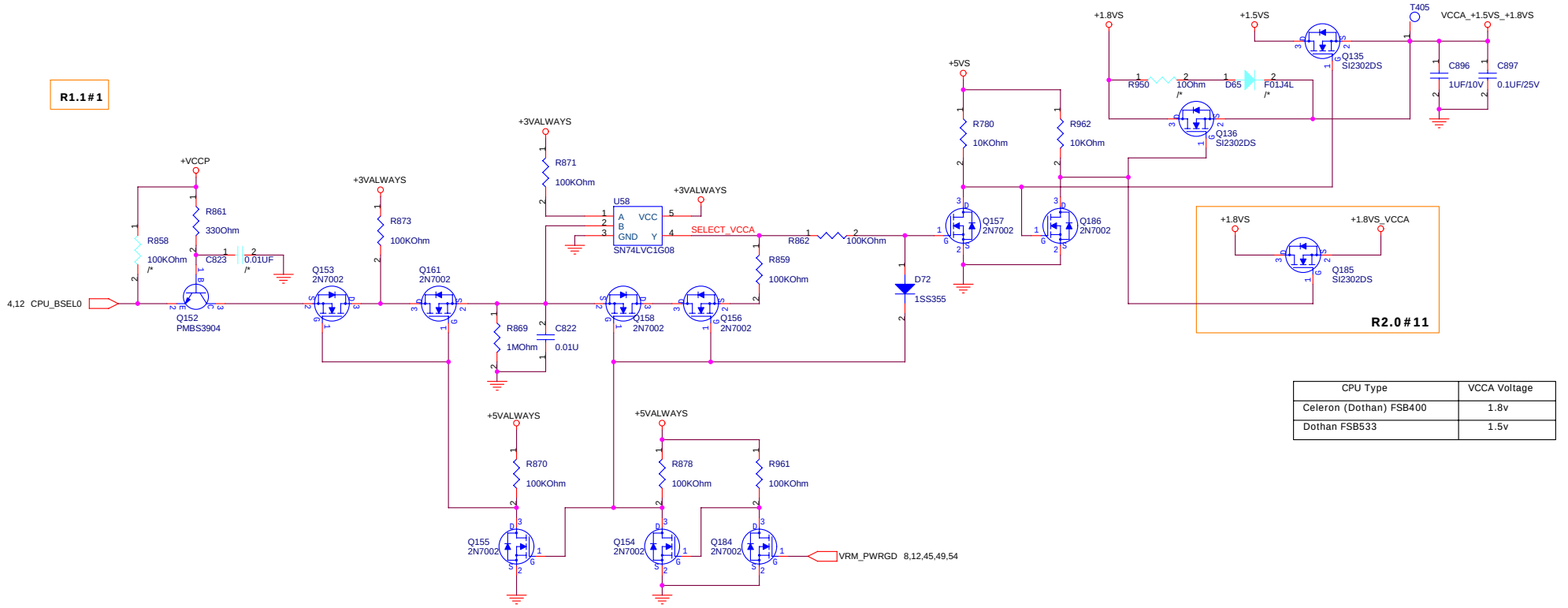
bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 17, 2005** SHEET **46** OF **63**	DESCRIPTION: ***FAN / RTC / DC_IN***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**
					DESIGN ENGINEER : ***M.Y.***

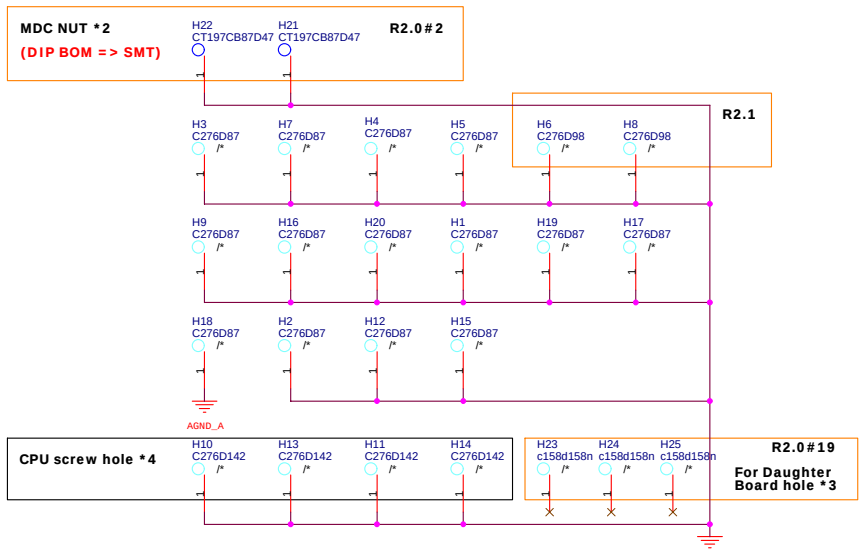


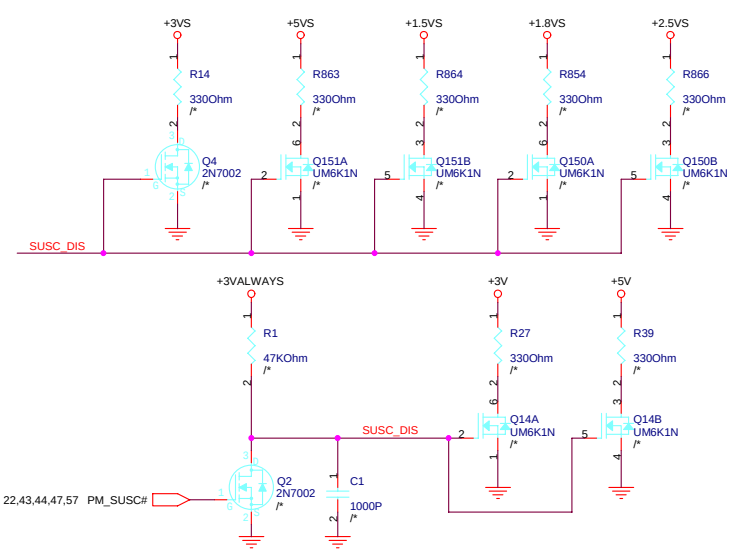
bom

PROJECT: **W3V**	REVISION: **2.1**	DATE: **Monday, January 17, 2005** SHEET **47** OF **63**	DESCRIPTION: ***POWER ON SEQUENCE***	SCHEMATIC FILE NAME: **<OrgName>** RELEASE DATE:	DESIGN ENGINEER: ***M.Y.***



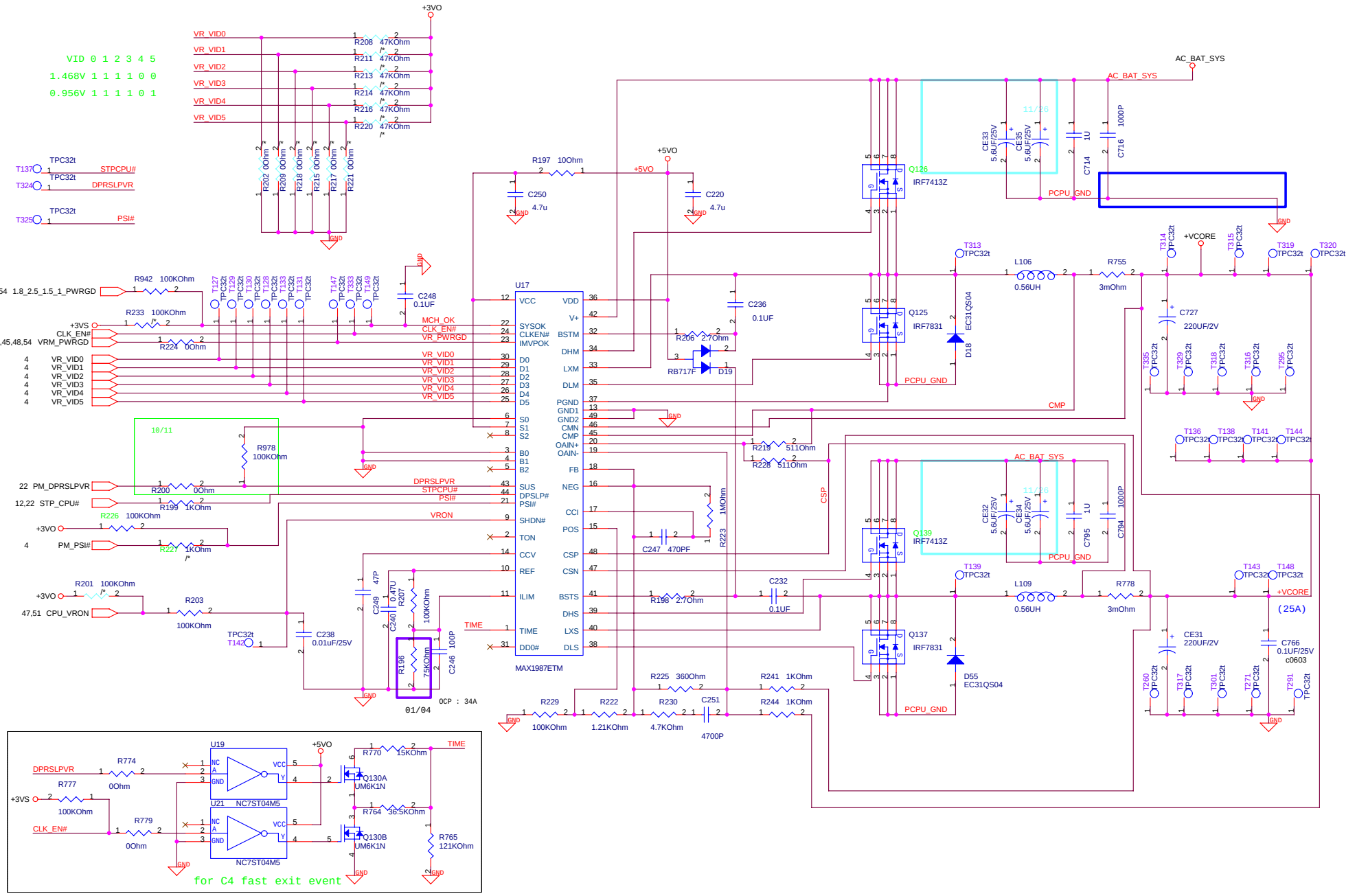
CPU Type	VCCA Voltage
Celeron (Dothan) FSB400	1.8v
Dothan FSB533	1.5v





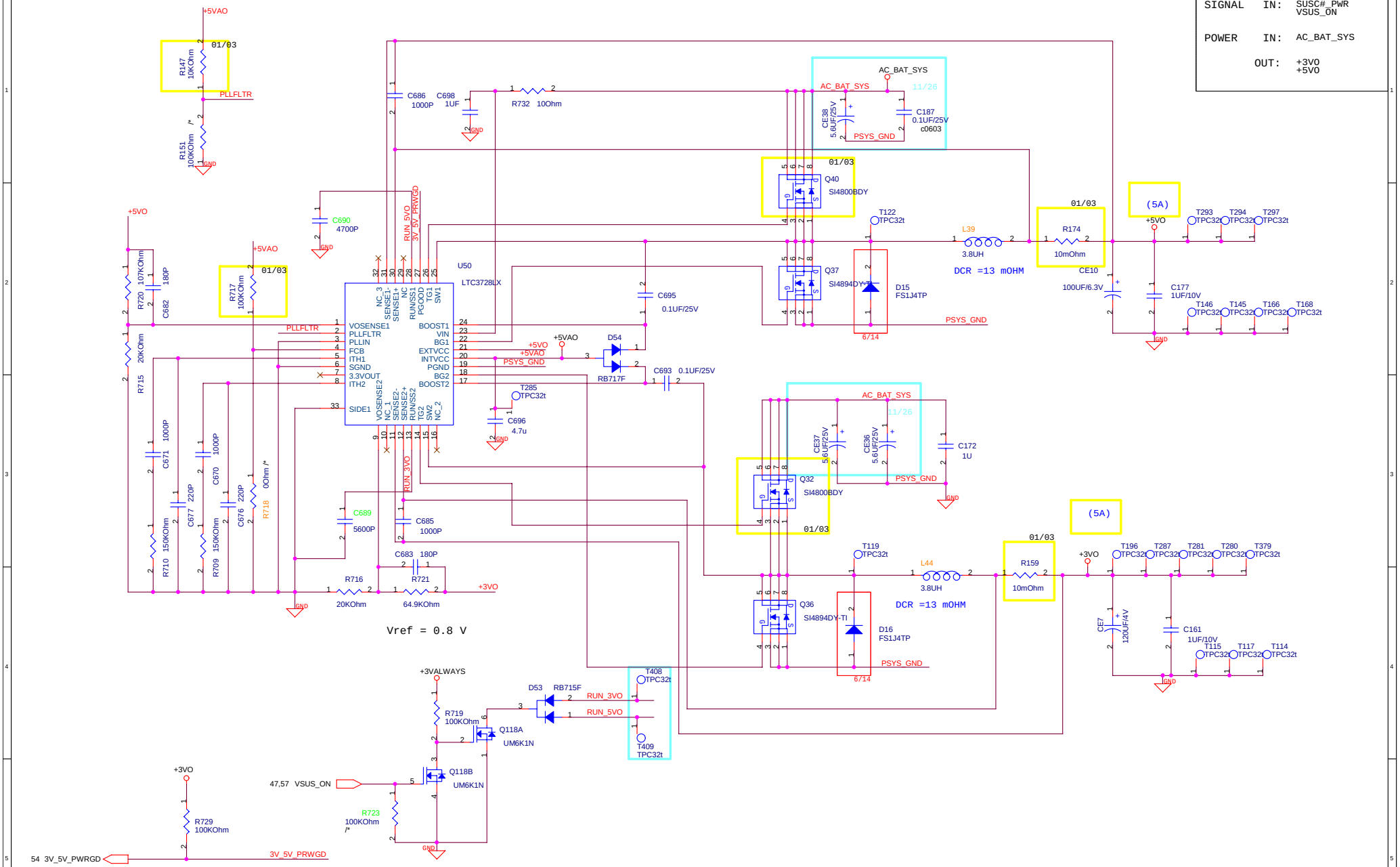
bom

PROJECT: W3V	REVISION 2.1	DATE: Monday, January 17, 2005	SHEET 48 OF 63	DESCRIPTION: DISCHARGE & EMI	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : M.Y.
					RELEASE DATE :		

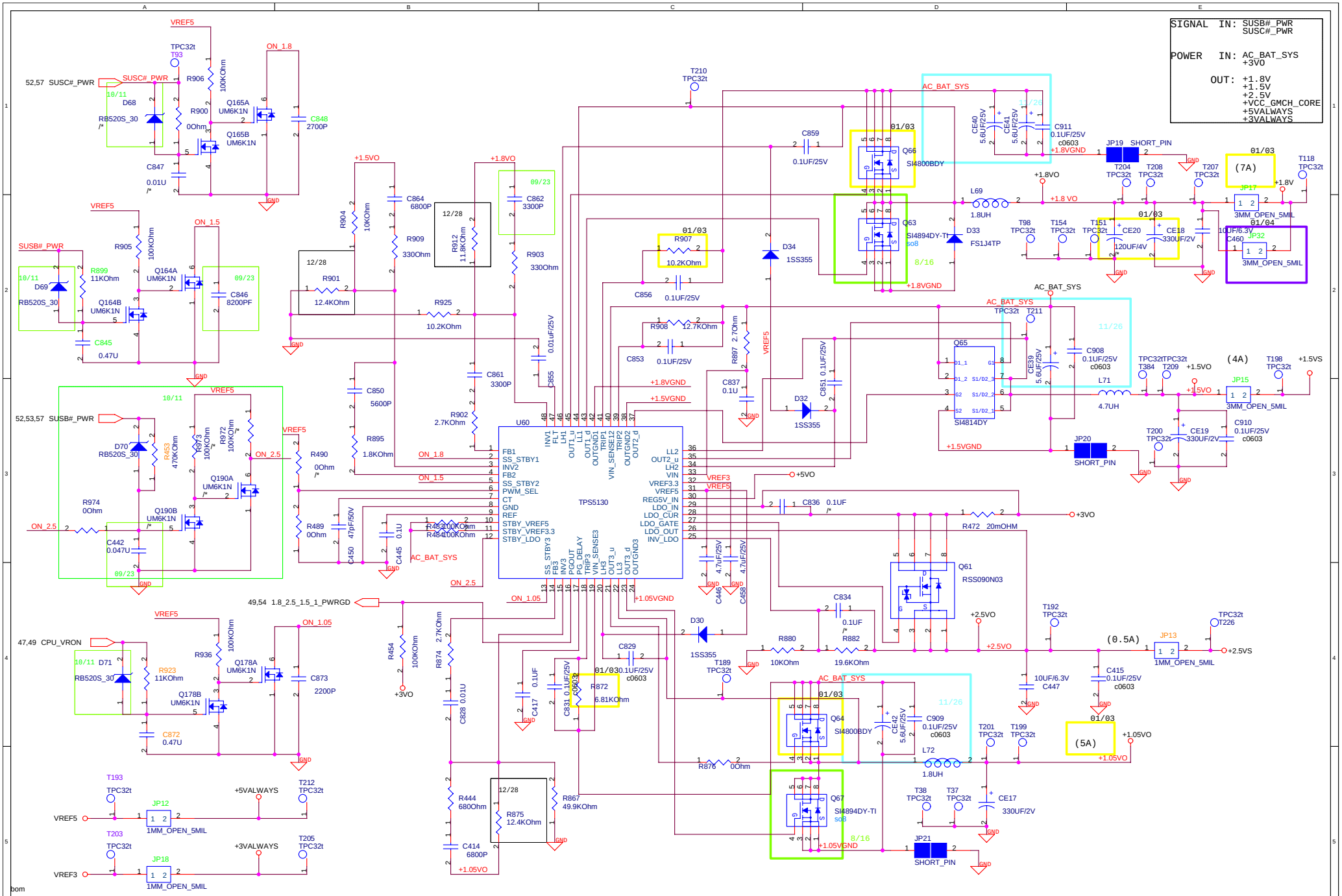


bom

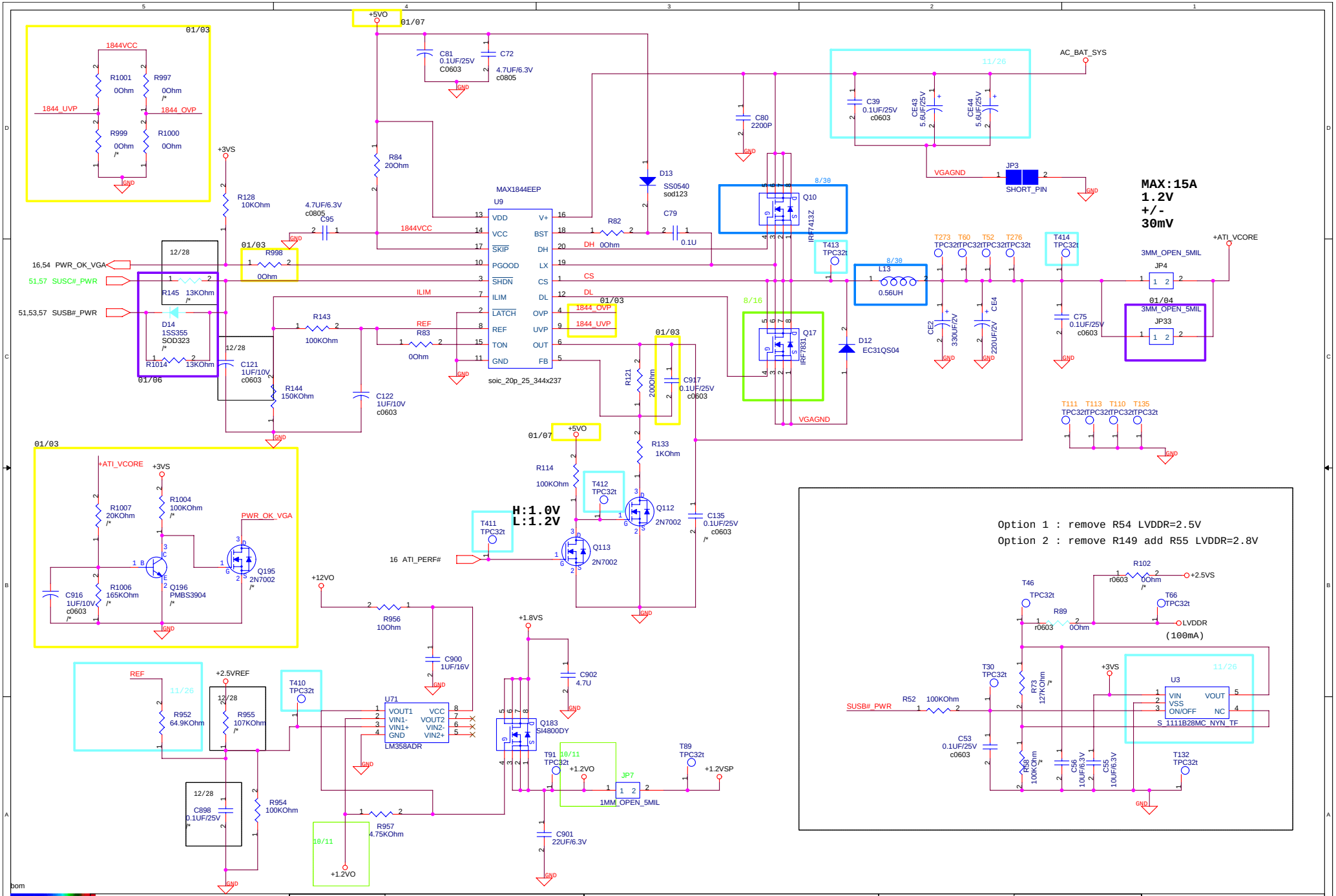
PROJECT: **W3V**	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: ***VCORE***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER : ***Amos Yu***
		SHEET 49 OF 63		RELEASE DATE :		



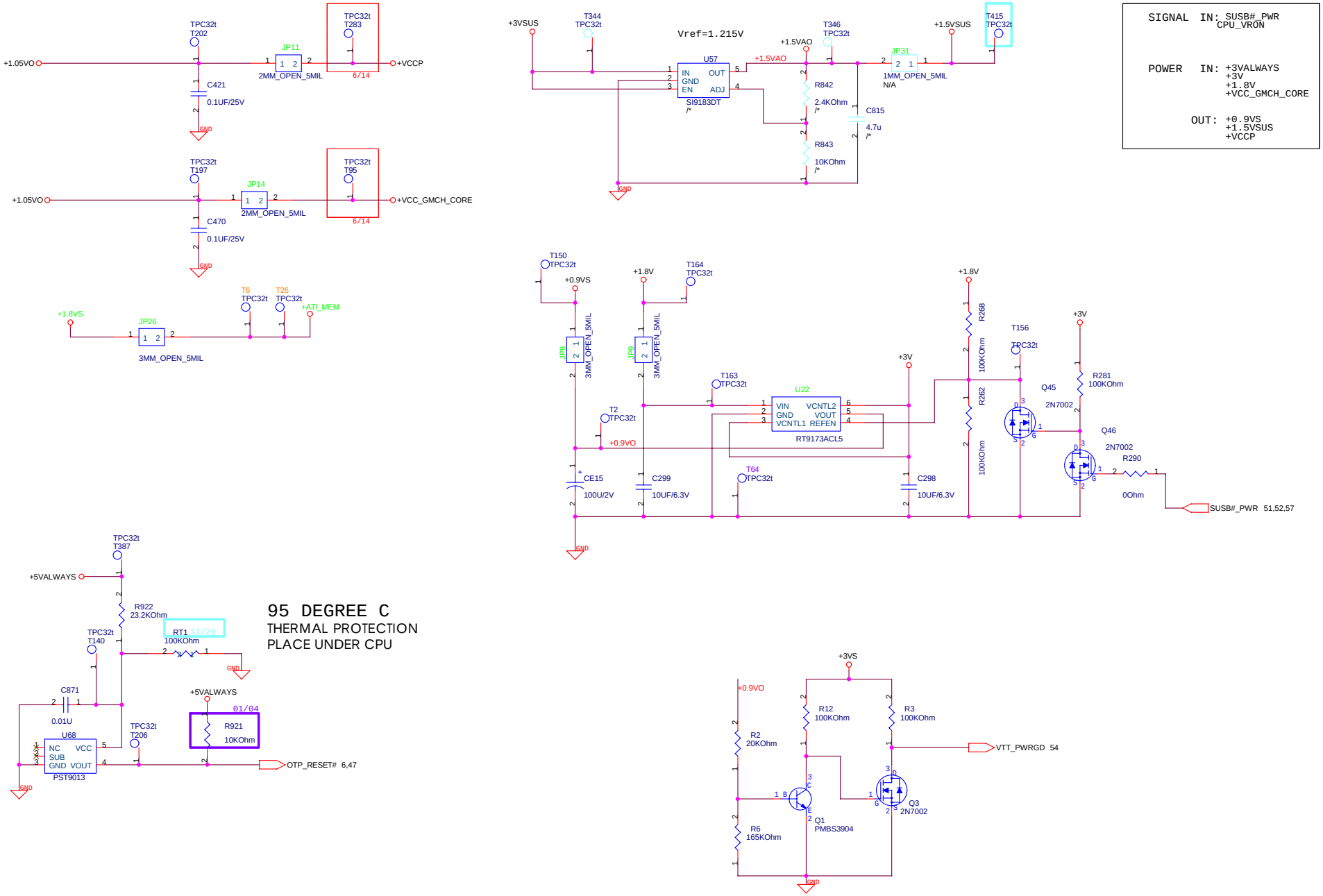
PROJECT: W3V	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: SYSTEM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Amos Yu
		SHEET 50 OF 63		RELEASE DATE :	



PROJECT: **W3V**	REVISION: **2.1**	DATE: **Monday, January 24, 2005**	DESCRIPTION: ***2.5V/1.5V/1.8V/1.05V***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Amos Yu***
		SHEET **51** OF **63**		RELEASE DATE:	

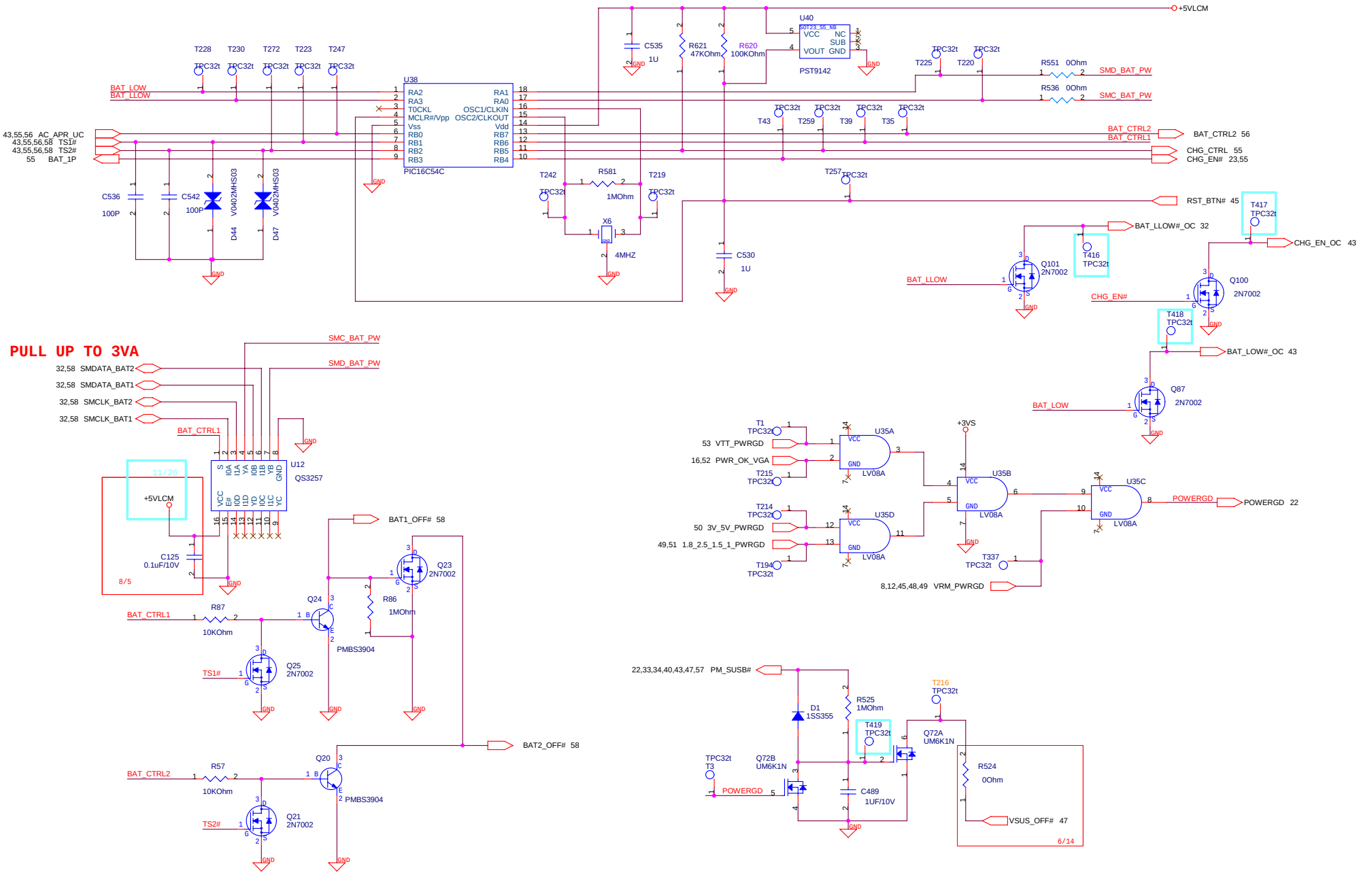


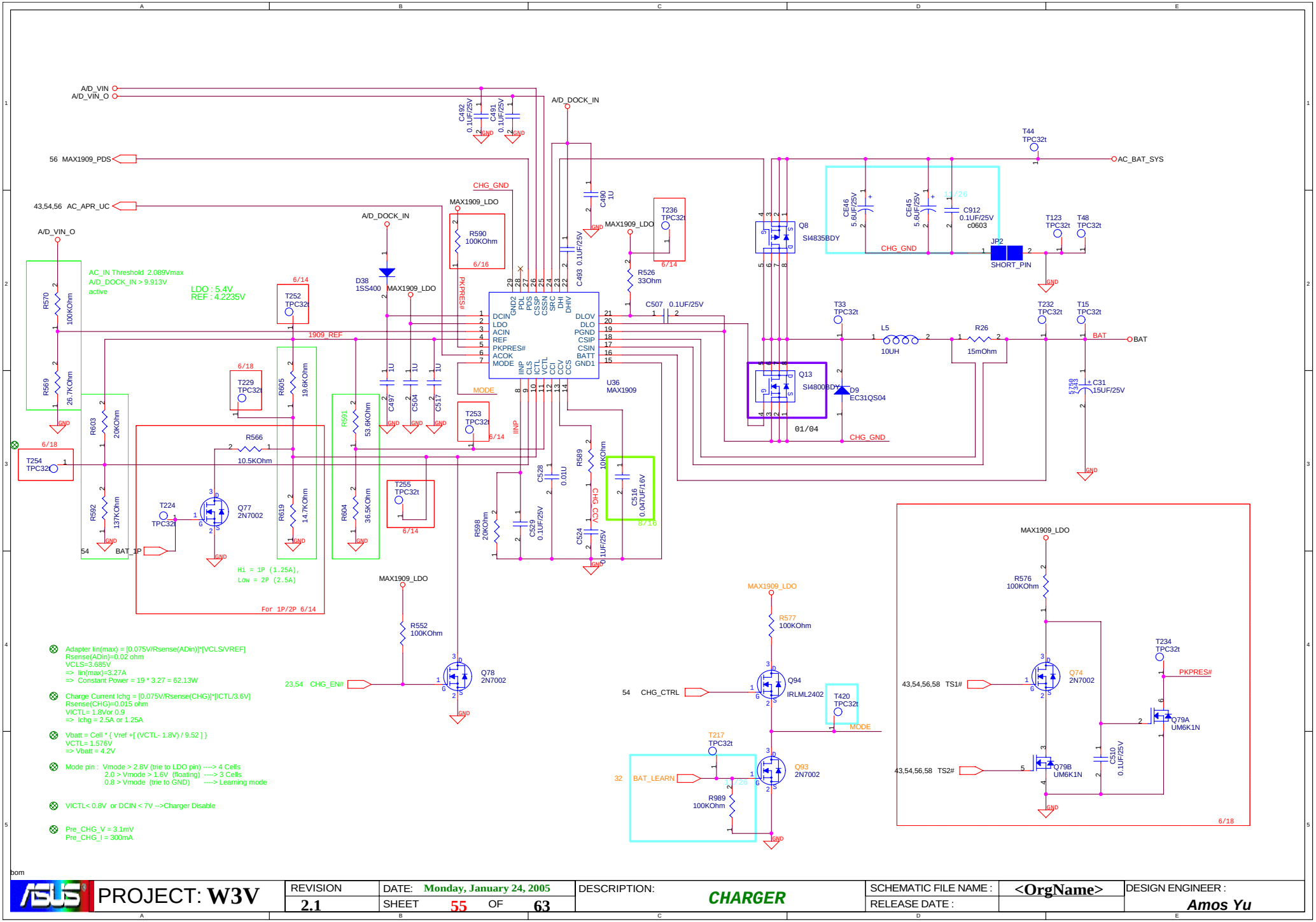
PROJECT: W3V	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: VGA VCORE	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Amos Yu
		SHEET 52 OF 63		RELEASE DATE :	



bom

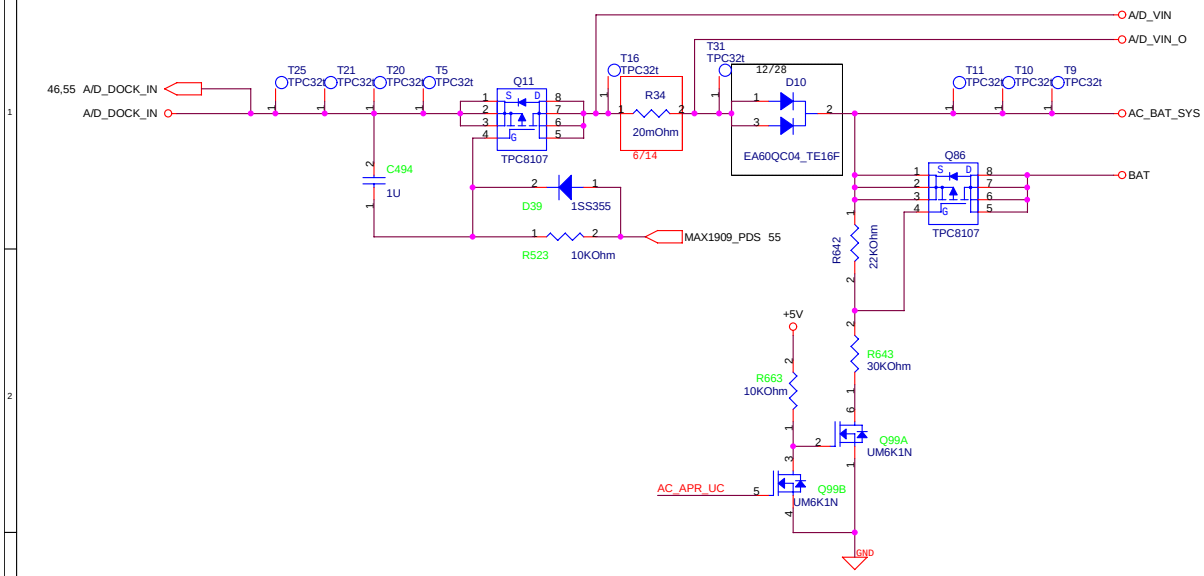
PROJECT: **W3V**	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: ***0.9VS/1.05VS/1.5VSUS***	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : ***Amos Yu***
		SHEET 53 OF 63		RELEASE DATE :	


PULL UP TO 3VA
U38
PIC16C54C
U40
PST9142
U12
QS3257
U35A
U35B
U35C
U35D
LV08A
Q87
Q100
Q101
Q23
Q24
Q25
Q20
Q21
Q72A
Q72B
2N7002
PMBS3904
UM6K1N
+5VLCM
+3VS
SMC_BAT_PW
SMD_BAT_PW
BAT_LOW
BAT_LLOW
BAT_CTRL1
BAT_CTRL2
BAT_CTRL2 56
CHG_CTRL 55
CHG_EN# 23,55
RST_BTN# 45
BAT_LLOW#_OC 32
CHG_EN_OC 43
BAT_LOW#_OC 43
POWERGD
POWERGD 22
BAT1_OFF# 58
BAT2_OFF# 58
VSUS_OFF# 47
VRM_PWRGD
PROJECT: W3V
REVISION 2.1
DATE: Monday, January 24, 2005
SHEET 54 OF 63
DESCRIPTION: PIC16C54/BATCON/PWOK
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Amos Yu

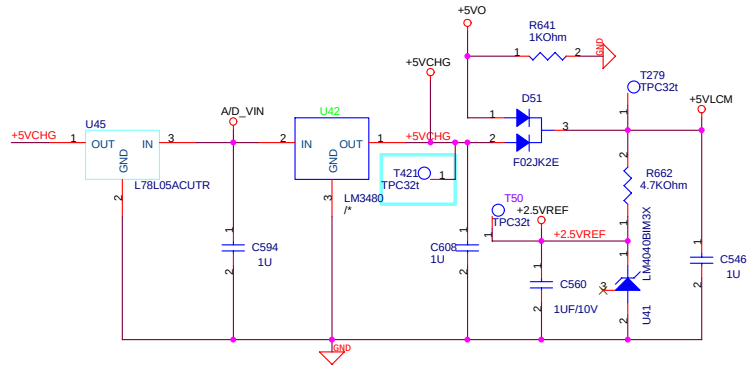


bom

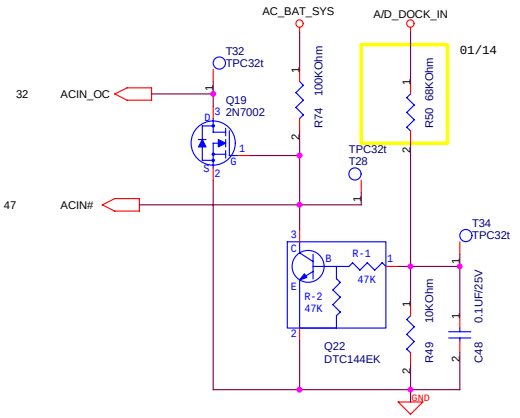
PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 24, 2005**	DESCRIPTION: ***CHARGER***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Amos Yu***
		SHEET **55** OF **63**		RELEASE DATE :	



AC_BAT_SYS, BATTERY LEARN CIRCUIT

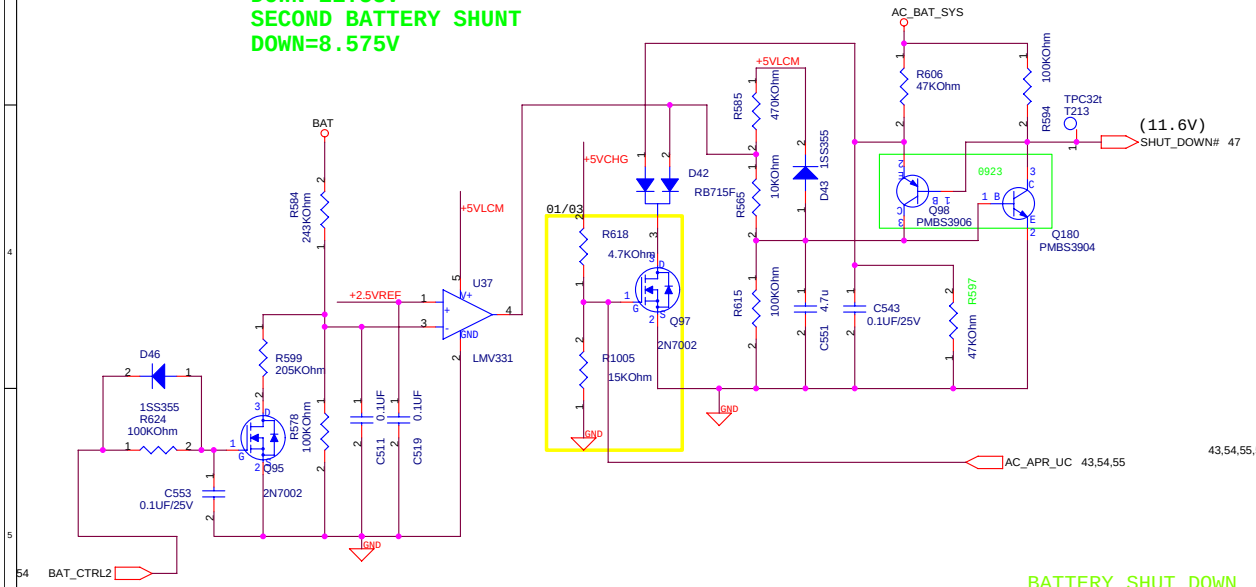


+5VCHG, +5VLCM, +2.5VREF

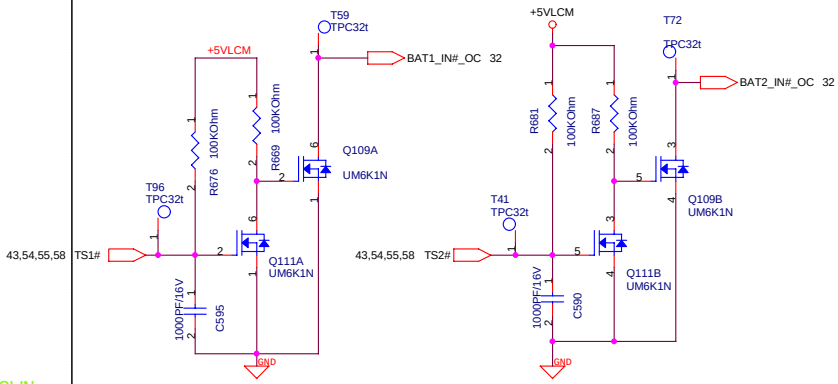


ADAPTER IN CIRCUIT

MAIN BATTERY SHUNT
DOWN=11.53V
SECOND BATTERY SHUNT
DOWN=8.575V



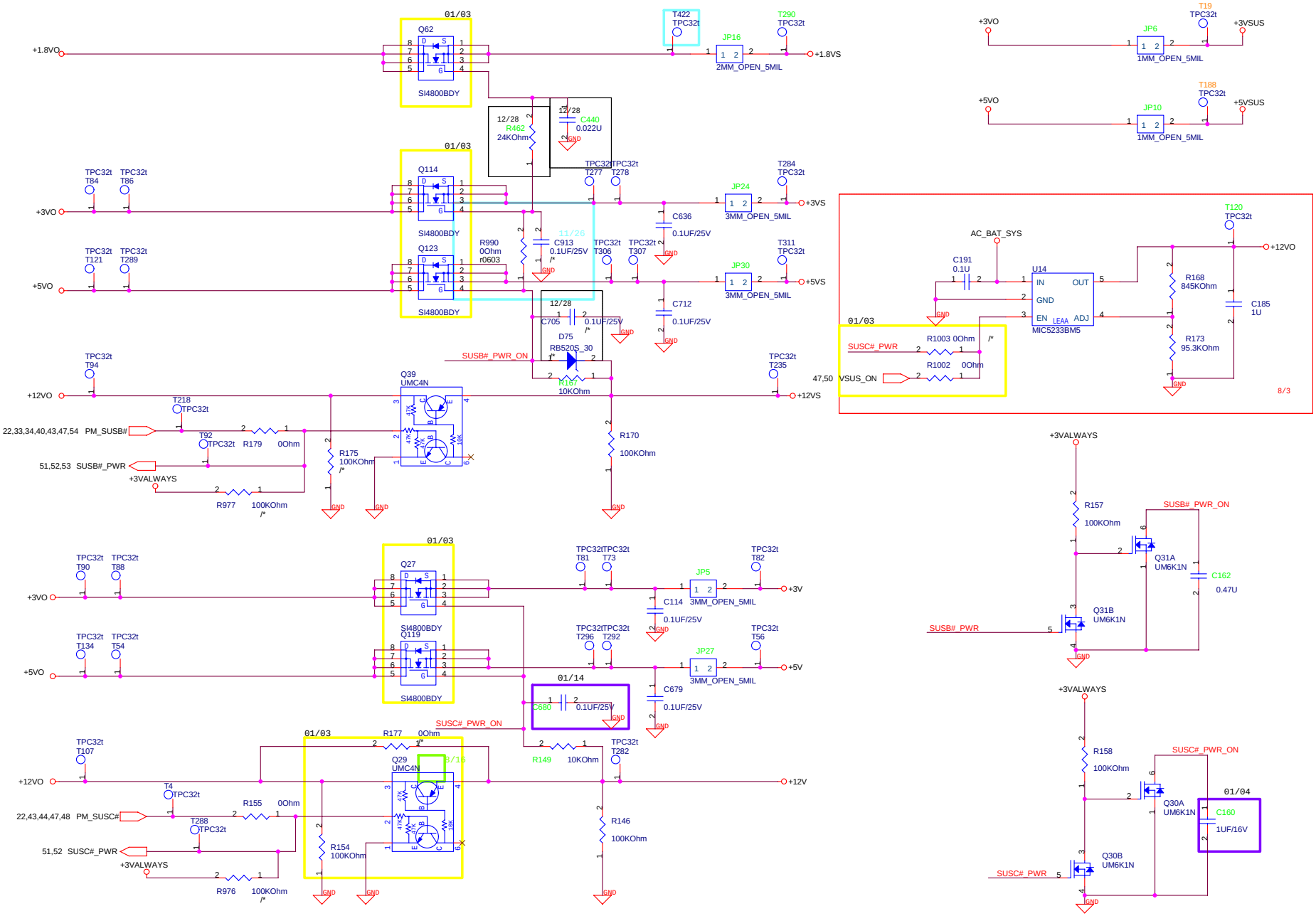
BATTERY SHUT_DOWN



BATTERY IN CIRCUIT

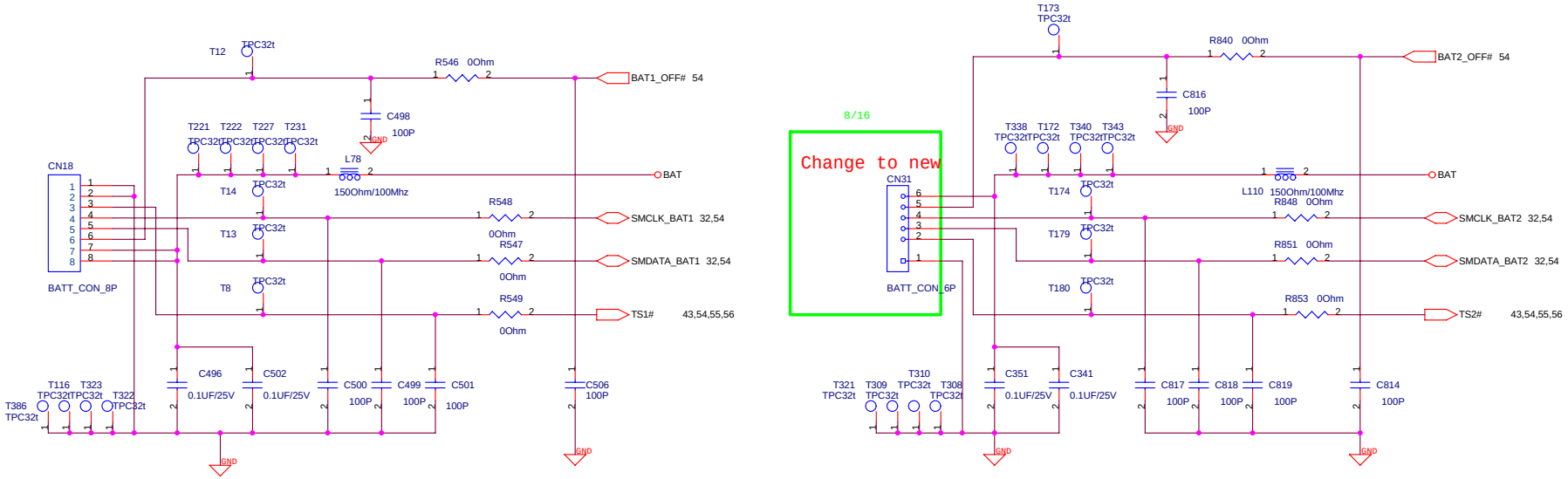
bom

PROJECT: W3V	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: BATLOW#/SD#	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Amos Yu
		SHEET 56 OF 63		RELEASE DATE :	



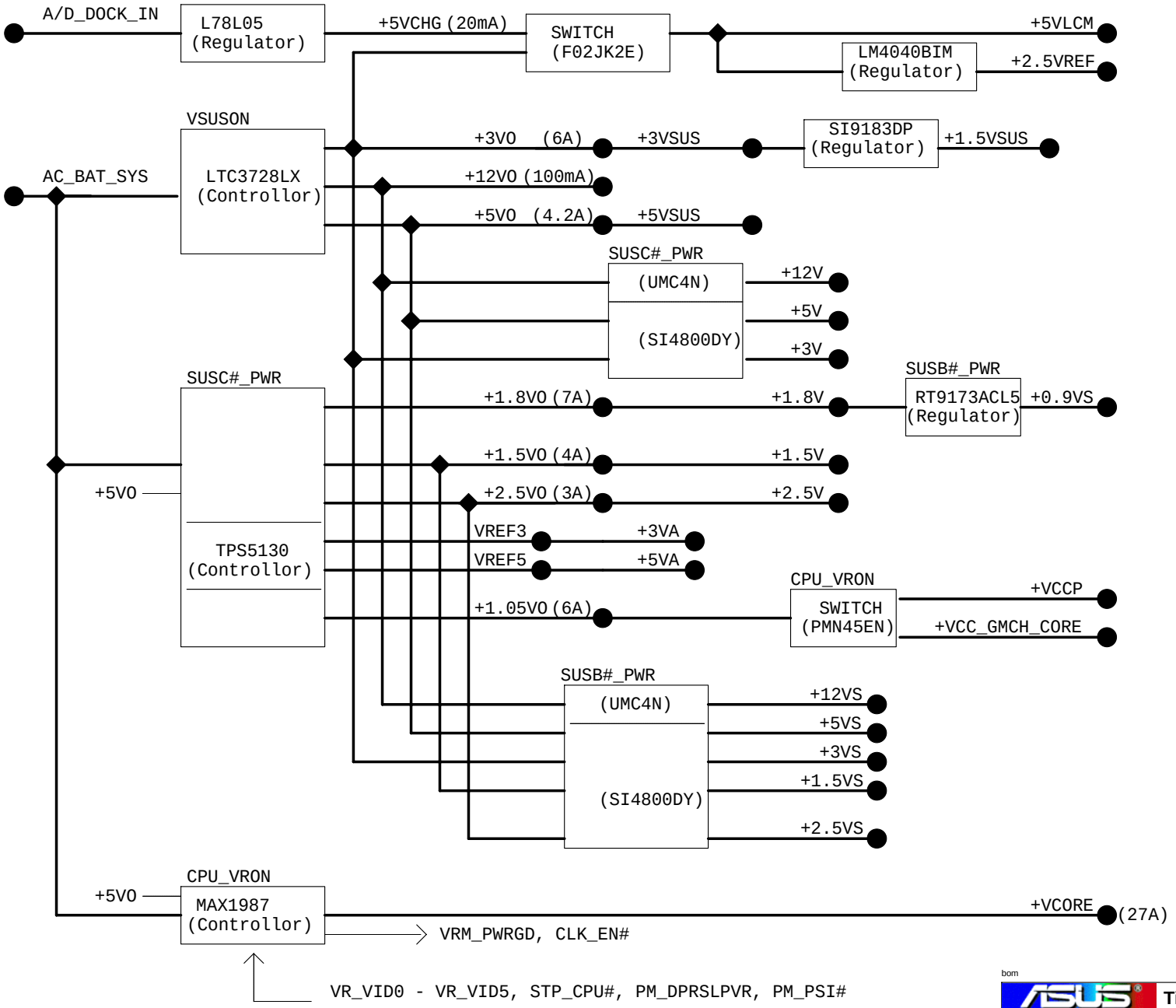
bom

PROJECT: **W3V**	REVISION 2.1	DATE: Monday, January 24, 2005	DESCRIPTION: ***LOAD SWITCH***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 57 OF 63		RELEASE DATE :		***Amos Yu***



bom

PROJECT: **W3V**	REVISION **2.1**	DATE: **Monday, January 24, 2005**	DESCRIPTION: ***PIC16C54/BATCON/PWOK***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Amos Yu***
		SHEET **58** OF **63**		RELEASE DATE :	



bom

Title : POWER FLOWCHART

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W3V	2.1

Date: Wednesday, January 26, 2005 Sheet 59 of 63

Revision History

R1.1

SYSTEM

1. (p48) Modify CPU +VCCA
2. (p45,47) Fix auto power on when AC in in AC mode
3. (p45,57) Solve U56 easily damaged
4. (p8) Add R941 for BIOS internal VGA strapping
5. (p8) U48, D30 change from ICH6_PWROK to VRM_PWRGD (p12) R363 change to 10K, C893=0.47uF
6. (p20) Fix PID1 can't strapped low
7. (p45) Modify power sequence of +3VSUS -> PM_RSMRST#
8. (p47) Fix that +3VSUS/+5VSUS may be turned on for a while when the power comes in at the first time
9. (p16) Fix TV out can't work
10. Add Bluetooth support
11. (p24) DEL reserved V5REF_SUS circuit
12. (p12) ADD net "CPUSEL0/1" for layout
13. (p37) Change X7 part
14. (p23) Add R949 to reduce overshoot
15. (p34) Solve pop noise in Windows boot
16. (p47) Power button debounce
17. Tune X'tal freq. (p22) C353/C356 (p26) C350/C354 (p32) C78/C93 (p41) C355/C360
18. (p27) Change CN32 part
19. (p43) Change R924 to +5VLCM to solve +5V leakage in power off.
20. (p20) Tune LCD_VCC timing
21. (p44) Modify CN10 pin define for ID change
22. (p23,34) Add ALC861VS PC-Beep support
23. (p33) ADD T388, U61.3 ADD "AUD_GPIO0" (p34) DEL R482, ADD U72
24. (p34,35) DEL net "MIC_AGND_A"
25. (p39) ADD voltage divider for Mic VREF
26. (p34) for EMI request
27. (p47) VSUS_OFF#
28. (p45) Modify power on sequence
29. (p43,p32) Reserved for bluetooth LED
30. (p39) Reserved PCI_INTC# for MINI-PCI.
31. (p29) Solve USB power surge warning when USB HDD plug-in
32. (p28) Support CSEL+ ODD
33. (p6) GMCH_THRMTRIP# no function in high temperature
34. (p10) unstuff for W3V
35. (p17) Adjust ATI 27MHz Vhigh
36. (p23) Aviod logic output unstable
37. (p4) Fix BT_VCC unstable
38. (p40) Tune clock timing
39. (p43) Tune LED current for LED spec
40. (p46) Adjust for +5VS_FAN stable
41. (p47) Fix can't power on in batttery mode

POWER

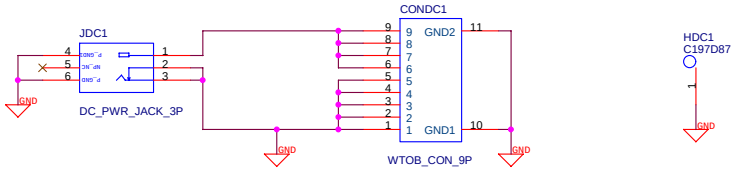
1 (p49) Add R942, MCH_OK connect to 1.8_2.5_1.5_1_PWRGD, C248, R233 unstuff

R2.0

SYSTEM

1. (p20) Adjust BACK_EN Vhigh
2. (p48) Change MDC nut
3. (p22,38,43) DEL BT_ON#, control BT_VCC by BT_LED#
4. (p29) Adjust for USB-IF spec
5. (p32) Solve SMBus loss pull-high power in power-off.
6. (p23) Reduce PCI_RSTNS# overshoot
7. (p23) Reduce 2V step on PCI_RST#
8. (p12) Tune W3V clock
9. (p25) Update PCB_VID
10. (p47) Solve system can't power on in battery mode
11. (p48) Modify +1.8VS_VCCA gate ckt
12. (p20) Avoid U28 damage
13. (p34) Remove reserved Windows de-pop Ckt
14. (p16) Tune W3A HSYNC/VSYNC timing
15. (p21) Tune W3V HSYNC/VSYNC timing
16. (p28) Modify for swap bay detection.
17. (p34) For EMI
18. (p20) For EMI
19. (p48) For PD4
20. (p21) For ME
21. (p33) DEL net "AUD_GPIO0"

DC IN

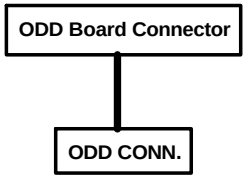


bom

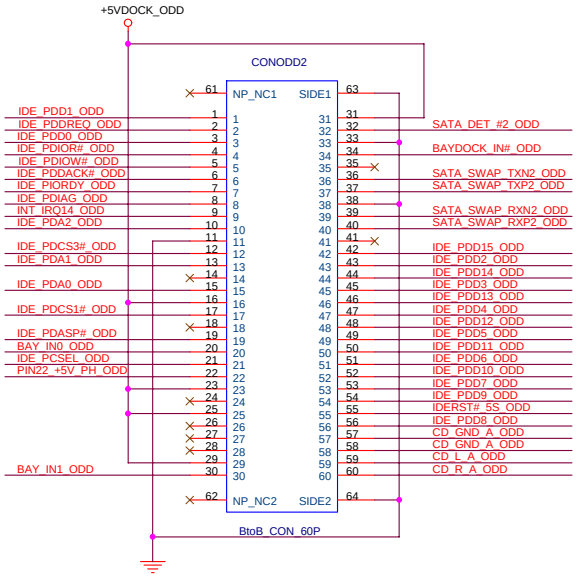
PROJECT: **W3V**	REVISION **2.1**	DESCRIPTION: ***DC_IN CONNECTOR***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Renyu Wang***
	DATE: **Wednesday, January 26, 2005**		RELEASE DATE :	
	SHEET **61** OF **63**			

W3V ODD Board

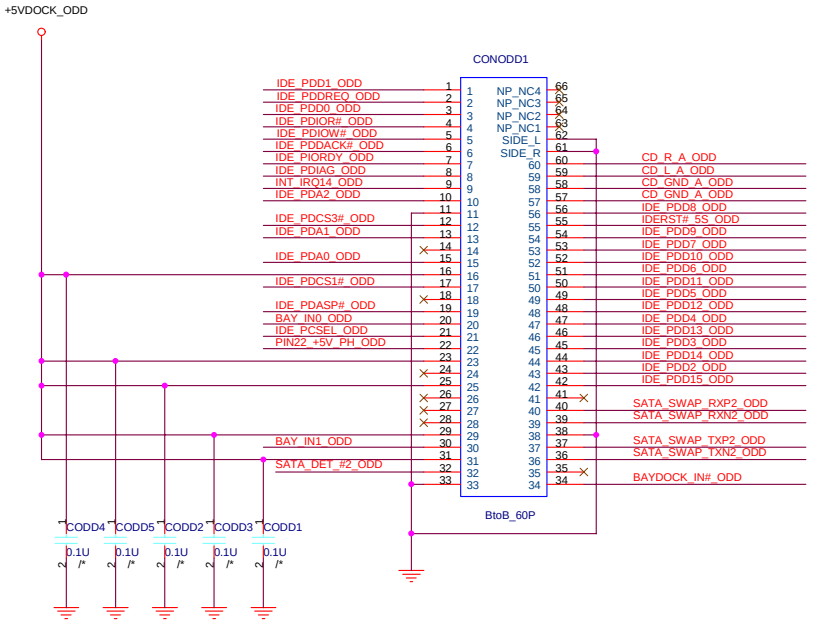
Block Diagram



ODD BOARD CONN.



ODD CONN.

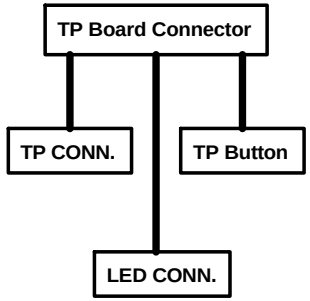


bom

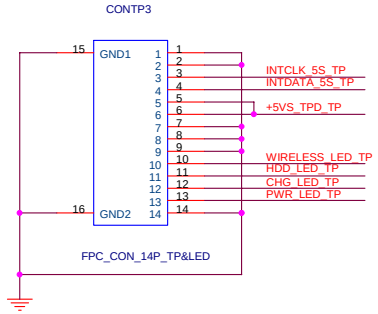
PROJECT: **W3V**	REVISION: **2.1**	DATE: Wednesday, January 26, 2005	DESCRIPTION: **ODD BOARD**	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: **Joe Wu**
		SHEET 62 OF 63		RELEASE DATE:	

W3V TP & LED Board

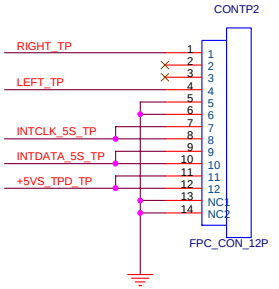
Block Diagram



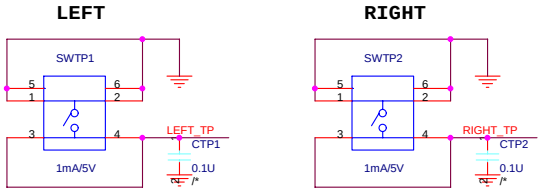
TOUCHPAD & LED BOARD CONN.



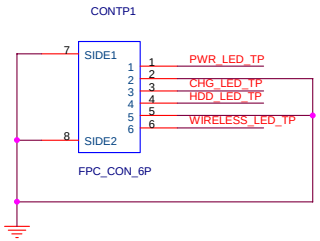
TP CONN.

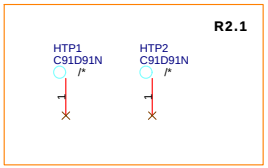


TOUCHPAD BUTTON



LED CONN.





bom

PROJECT: W3V	REVISION 2.1	DATE: Wednesday, January 26, 2005	DESCRIPTION: TP&LED BOARD	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Joe Wu
		SHEET 63 OF 63		RELEASE DATE :	