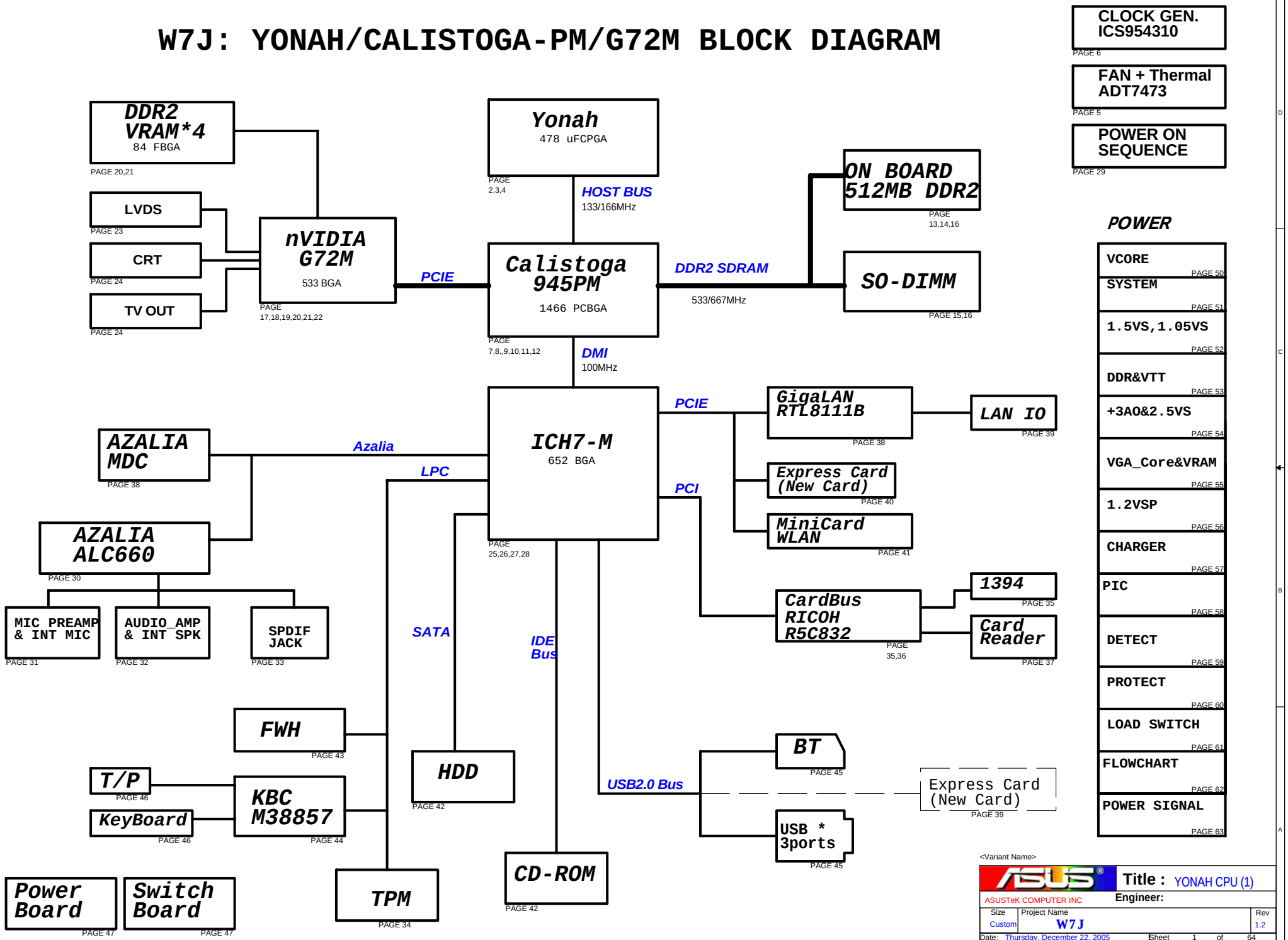
W7J: YONAH/CALISTOGA-PM/G72M BLOCK DIAGRAM



<Variant Name>

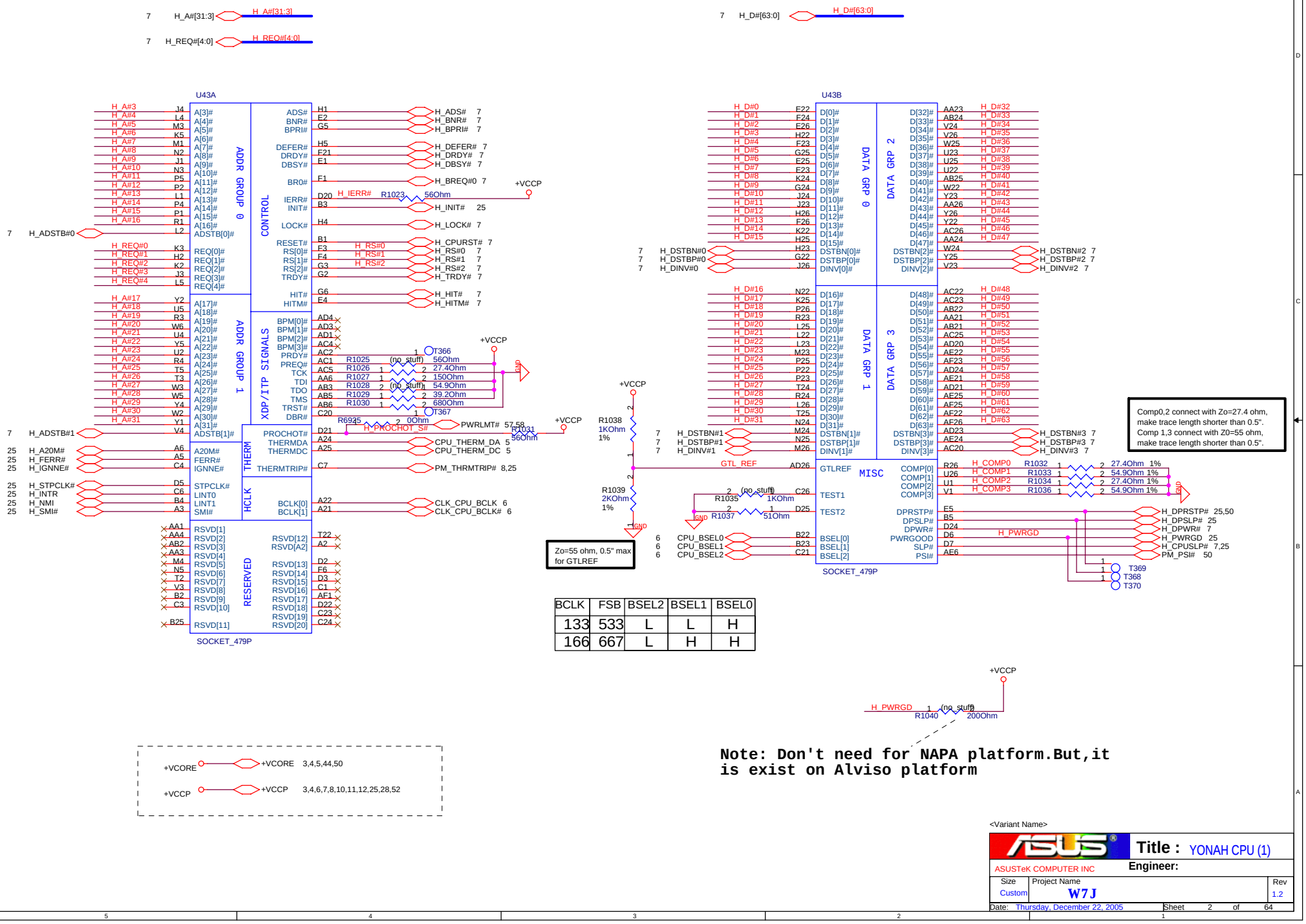
ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 1 of 64

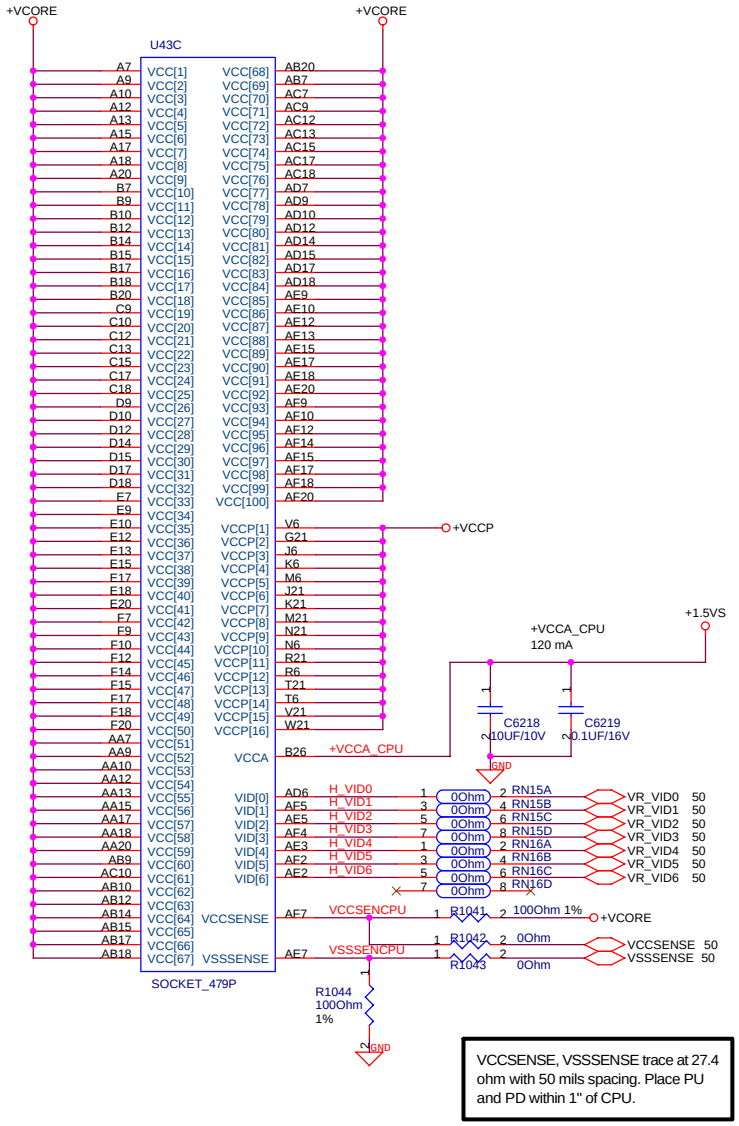


BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

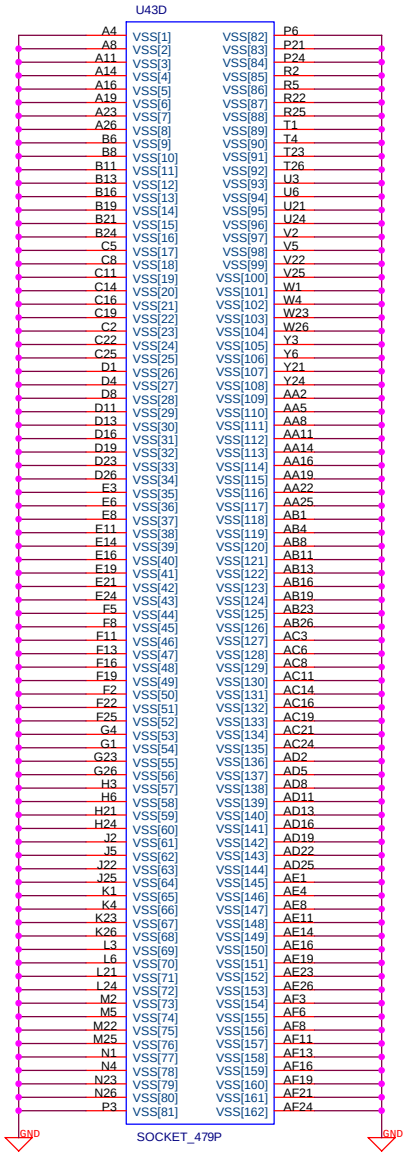
<Variant Name>
Title : YONAH CPU (1)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom | Project Name: W7J | Rev: 1.2
Date: Thursday, December 22, 2005 | Sheet 2 of 64

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



<Variant Name>

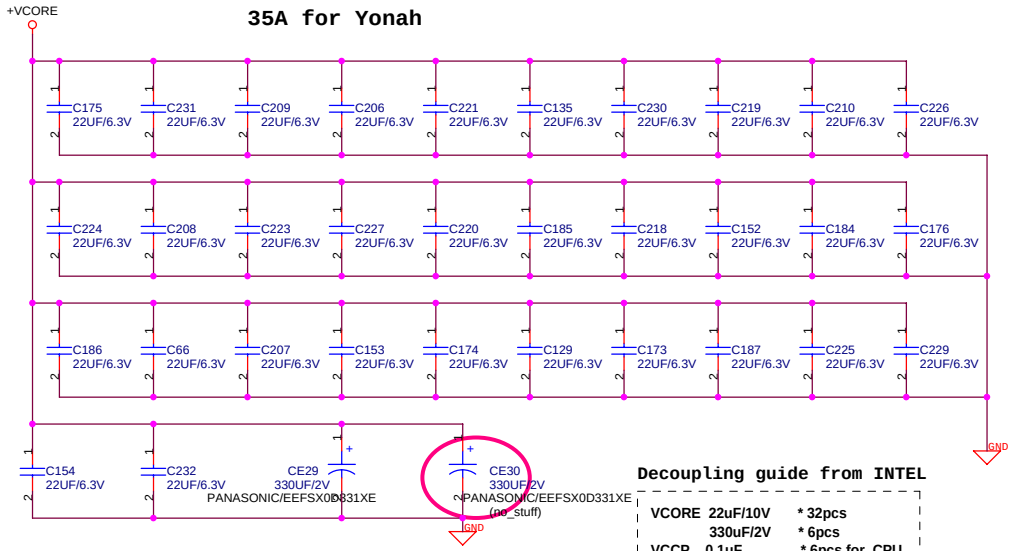
ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

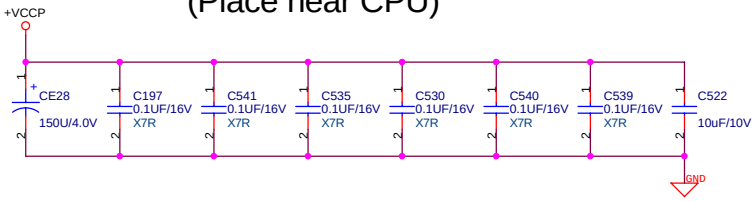
Date: Thursday, December 22, 2005 Sheet 3 of 64



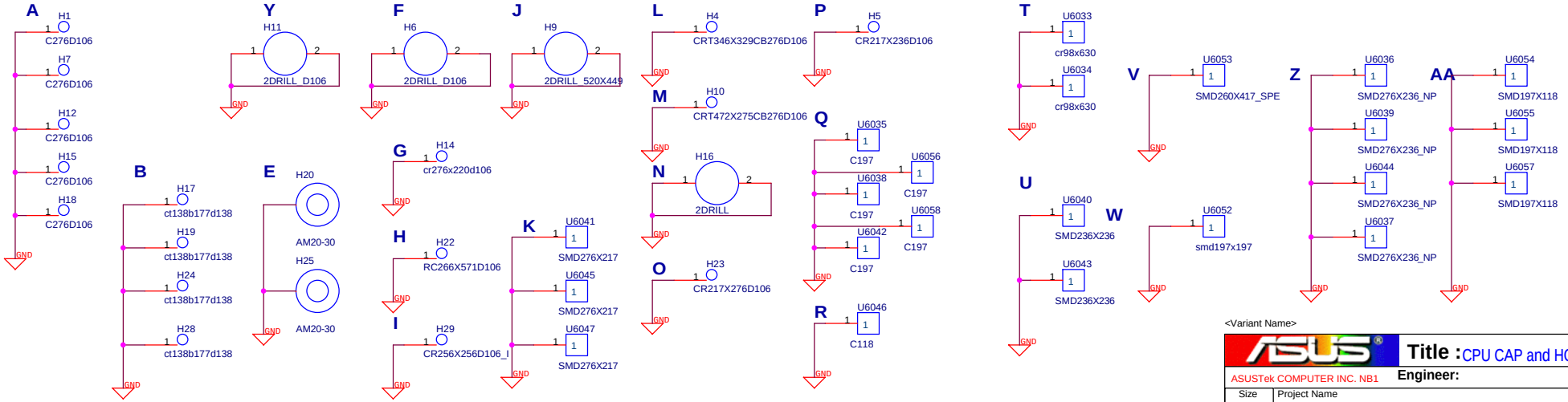
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



SCREW HOLE



<Variant Name>

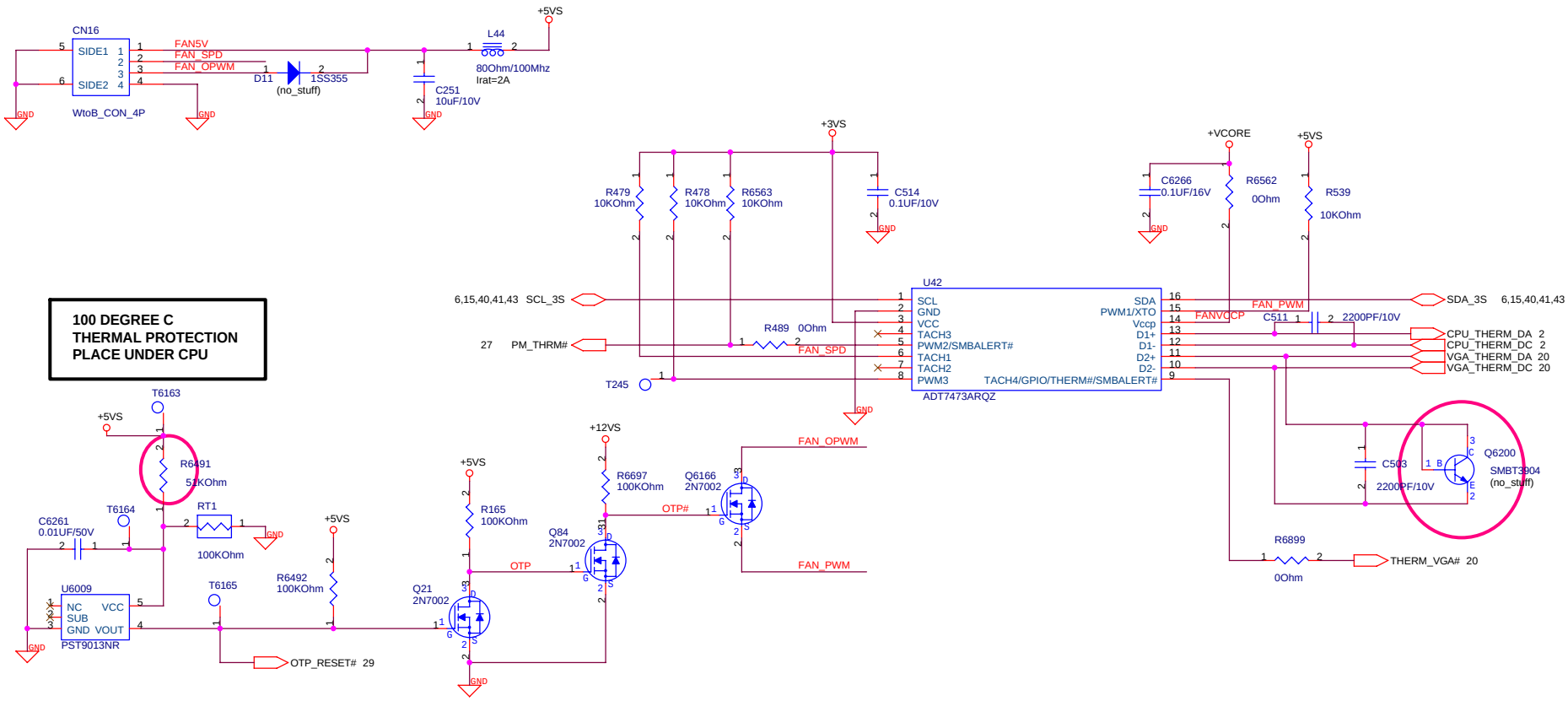
Title : CPU CAP and HOLES

ASUSTek COMPUTER INC. NB1 **Engineer:**

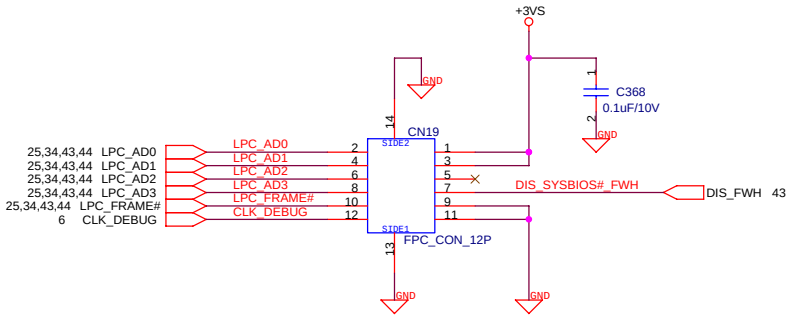
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 4 of 64

FAN & THERMAL CONTROLLER

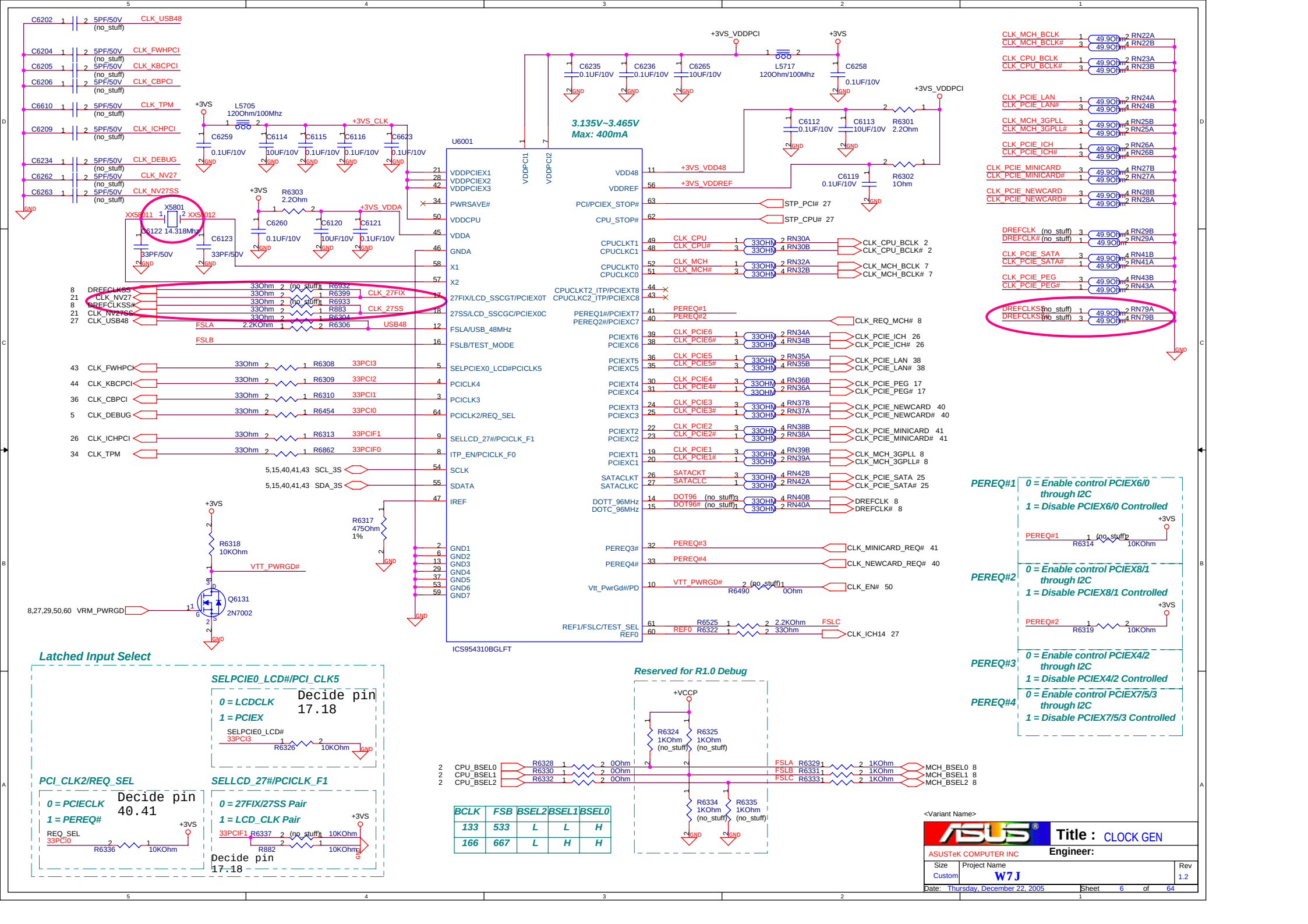


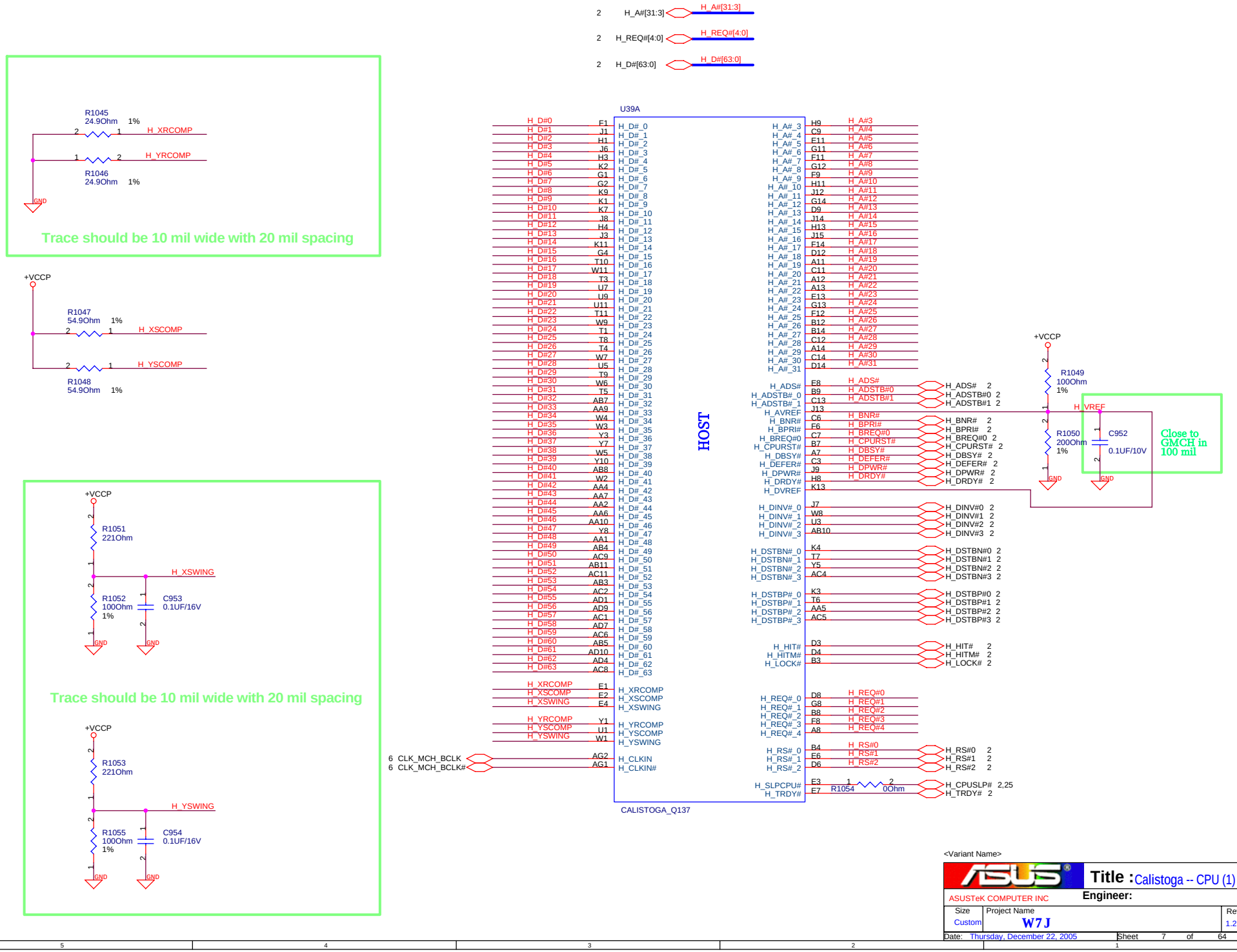
LPC DEBUG PORT

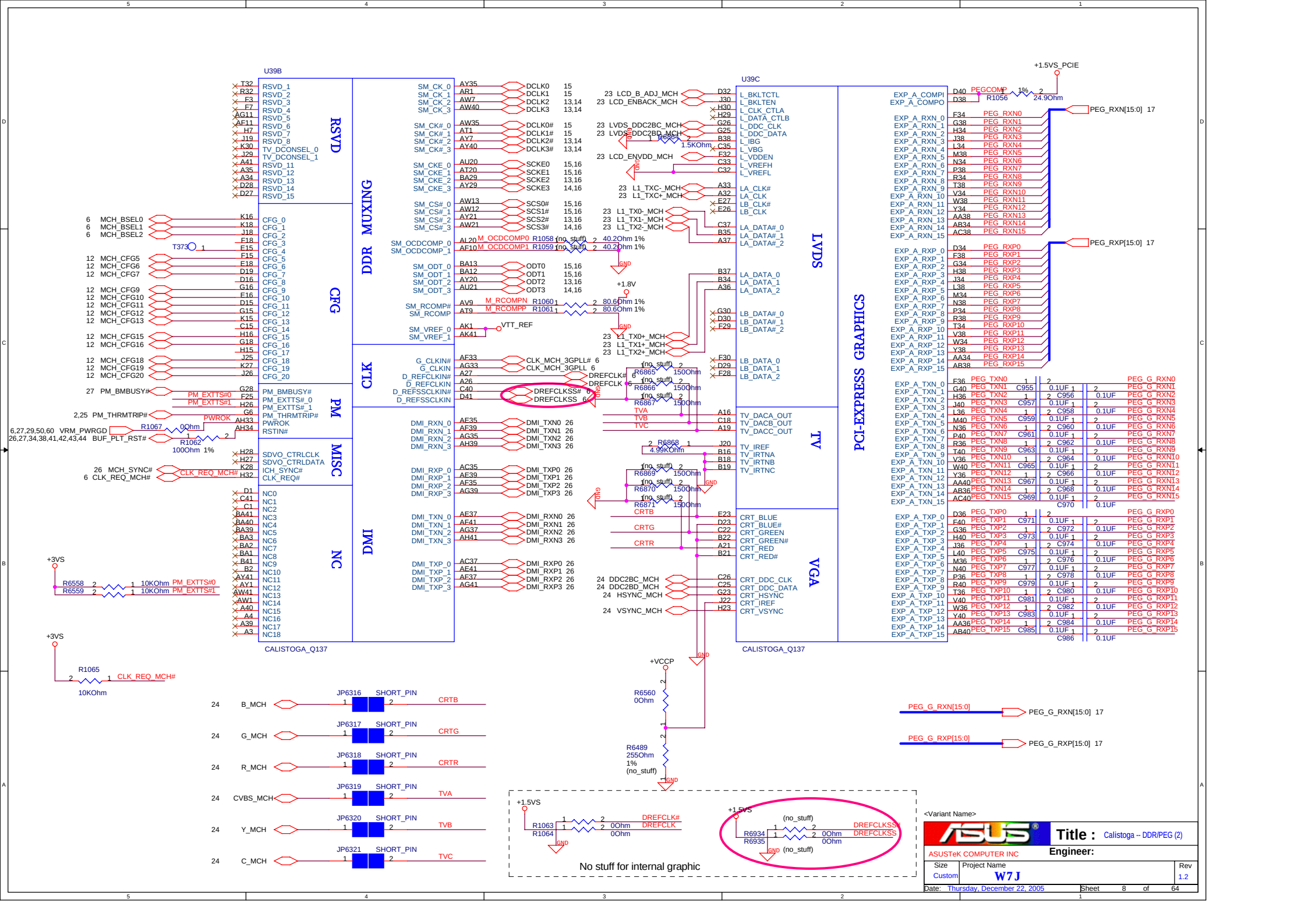


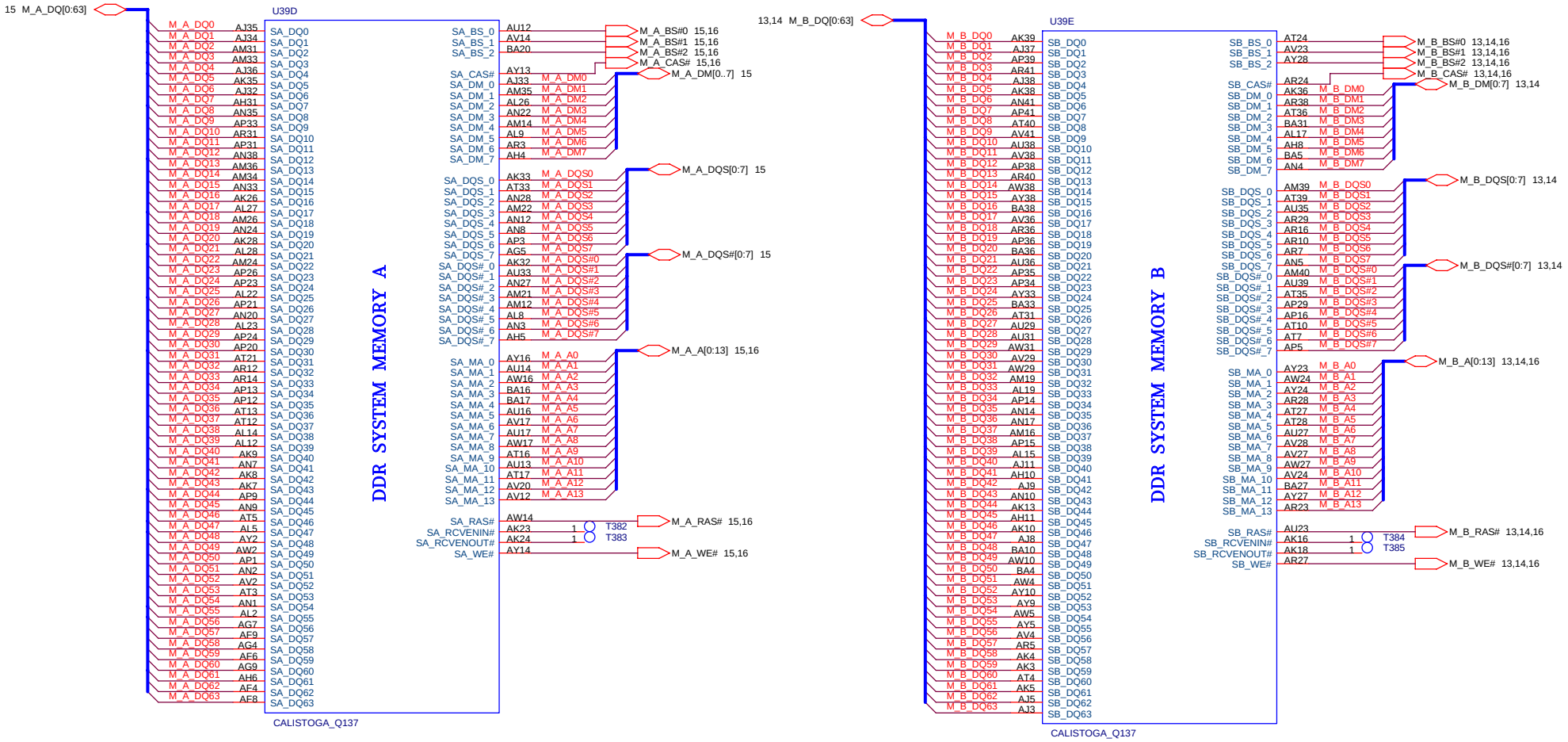
<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN & debug port	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 5 of 64	


U6001
ICS954310BGLFT
3.135V~3.465V
Max: 400mA
Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
PCI_CLK2/REQ_SEL
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27#/PCICLK_F1
0 = 27FIX/27SS Pair
1 = LCD_CLK Pair
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#1
0 = Enable control PCIEX6/0 through I2C
1 = Disable PCIEX6/0 Controlled
PEREQ#2
0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer:
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 6 of 64


2 H_A#[31:3] H_A#[31:3]
2 H_REQ#[4:0] H_REQ#[4:0]
2 H_D#[63:0] H_D#[63:0]
R1045 24.9Ohm 1%
H_XRCOMP
H_YRCOMP
R1046 24.9Ohm 1%
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1047 54.9Ohm 1%
H_XSCOMP
H_YSCOMP
R1048 54.9Ohm 1%
+VCCP
R1051 221Ohm
H_XSWING
R1052 100Ohm 1%
C953 0.1UF/16V
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1053 221Ohm
H_YSWING
R1055 100Ohm 1%
C954 0.1UF/16V
GND
U39A
HOST
H_D#0 H_D#1 H_D#2 H_D#3 H_D#4 H_D#5 H_D#6 H_D#7 H_D#8 H_D#9 H_D#10 H_D#11 H_D#12 H_D#13 H_D#14 H_D#15 H_D#16 H_D#17 H_D#18 H_D#19 H_D#20 H_D#21 H_D#22 H_D#23 H_D#24 H_D#25 H_D#26 H_D#27 H_D#28 H_D#29 H_D#30 H_D#31 H_D#32 H_D#33 H_D#34 H_D#35 H_D#36 H_D#37 H_D#38 H_D#39 H_D#40 H_D#41 H_D#42 H_D#43 H_D#44 H_D#45 H_D#46 H_D#47 H_D#48 H_D#49 H_D#50 H_D#51 H_D#52 H_D#53 H_D#54 H_D#55 H_D#56 H_D#57 H_D#58 H_D#59 H_D#60 H_D#61 H_D#62 H_D#63
H_XRCOMP H_XSCOMP H_XSWING
H_YRCOMP H_YSCOMP H_YSWING
6 CLK_MCH_BCLK
6 CLK_MCH_BCLK#
H_CLKIN H_CLKIN#
H_A#3 H_A#4 H_A#5 H_A#6 H_A#7 H_A#8 H_A#9 H_A#10 H_A#11 H_A#12 H_A#13 H_A#14 H_A#15 H_A#16 H_A#17 H_A#18 H_A#19 H_A#20 H_A#21 H_A#22 H_A#23 H_A#24 H_A#25 H_A#26 H_A#27 H_A#28 H_A#29 H_A#30 H_A#31
H_ADS# H_ADSTB#0 H_ADSTB#1
H_AVREF
H_BNR# H_BPRI# H_BREQ#0 H_CPURST# H_DBSY# H_DEFER# H_DPWR# H_DRDY#
H_DVREF
H_DINV#0 H_DINV#1 H_DINV#2 H_DINV#3
H_DSTBN#0 H_DSTBN#1 H_DSTBN#2 H_DSTBN#3
H_DSTBP#0 H_DSTBP#1 H_DSTBP#2 H_DSTBP#3
H_HIT# H_HITM# H_LOCK#
H_REQ#0 H_REQ#1 H_REQ#2 H_REQ#3 H_REQ#4
H_RS#0 H_RS#1 H_RS#2
H_SLPCPU# H_TRDY#
R1054 0Ohm
H_CPUSLP# 2,25
H_TRDY# 2
CALISTOGA_Q137
+VCCP
R1049 100Ohm 1%
H_VREF
R1050 200Ohm 1%
C952 0.1UF/10V
GND
Close to GMCH in 100 mil
<Variant Name>
Title : Calistoga -- CPU (1)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 7 of 64


U39B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
CALISTOGA_Q137
U39C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
+1.5VS_PCIE
+3VS
+VCCP
+1.8V
VTT_REF
GND
No stuff for internal graphic
<Variant Name>
Title : Calistoga -- DDR/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 8 of 64



<Variant Name>

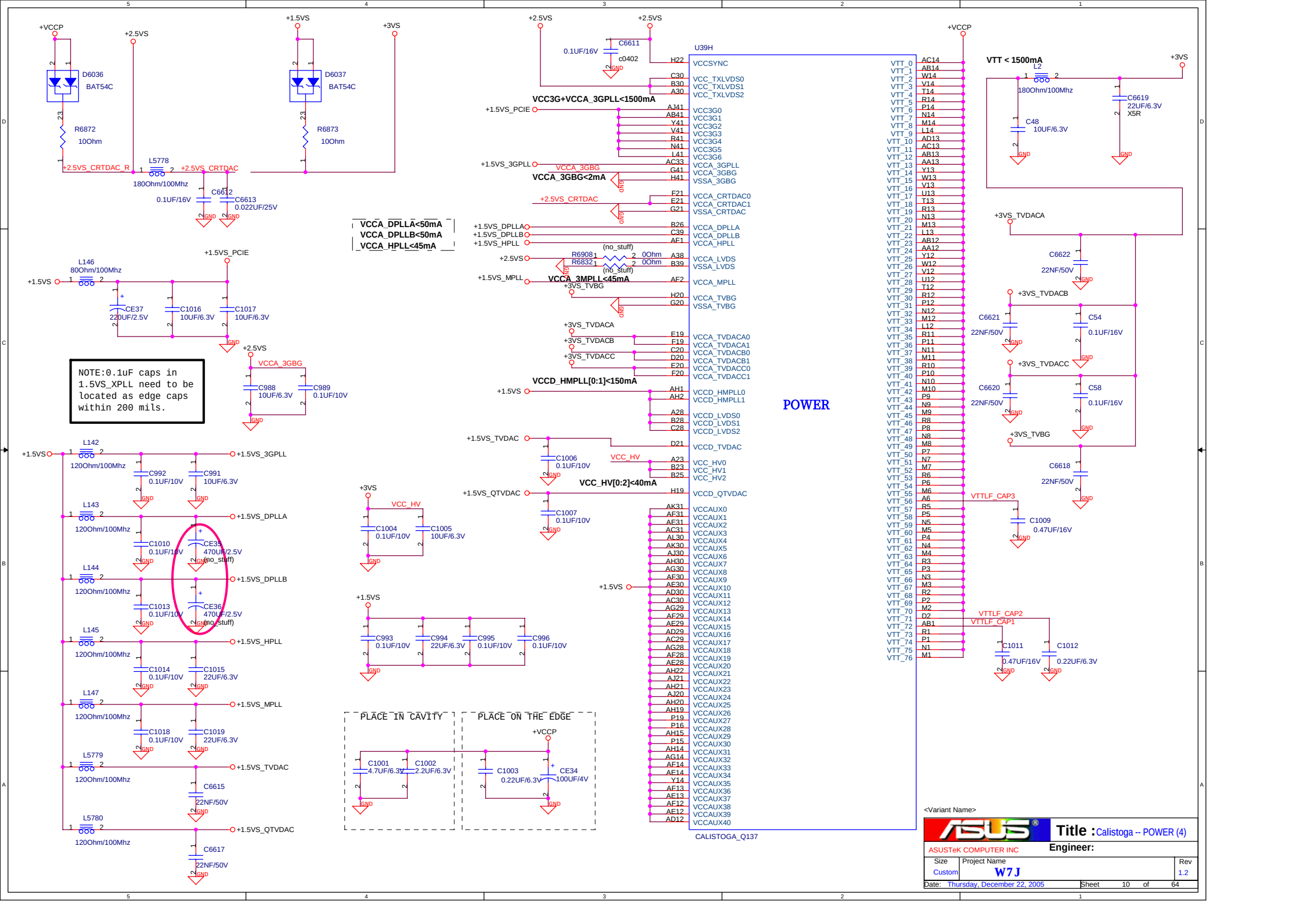
ASUSTeK COMPUTER INC

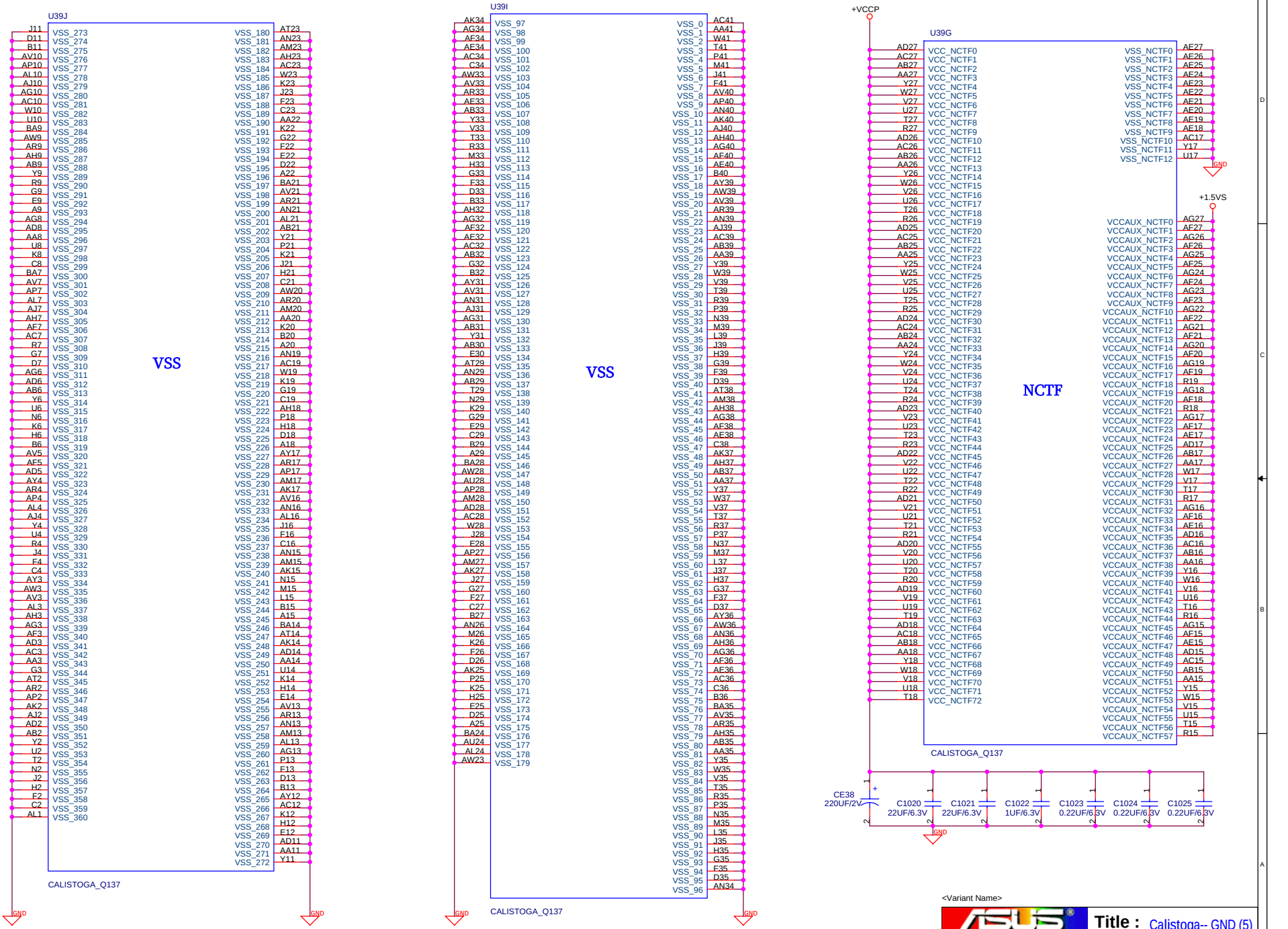
Title : Calistoga -- DDR bus (3)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 9 of 64


+VCCP
+2.5VS
+1.5VS
+3VS
D6036
BAT54C
D6037
BAT54C
R6872
10Ohm
R6873
10Ohm
+2.5VS_CRTDAC_R
L5778
180Ohm/100Mhz
+2.5VS_CRTDAC
C6612
0.1UF/16V
C6613
0.022UF/25V
GND
L146
80Ohm/100Mhz
+1.5VS_PCIE
CE37
220UF/2.5V
C1016
10UF/6.3V
C1017
10UF/6.3V
VCCA_3GBG
C988
10UF/6.3V
C989
0.1UF/10V
NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
L142
120Ohm/100Mhz
+1.5VS_3GPLL
C992
0.1UF/10V
C991
10UF/6.3V
L143
+1.5VS_DPLLA
C1010
0.1UF/10V
CE35
470UF/2.5V
(no_stuff)
L144
+1.5VS_DPLLB
C1013
0.1UF/10V
CE36
470UF/2.5V
(no_stuff)
L145
+1.5VS_HPLL
C1014
0.1UF/10V
C1015
22UF/6.3V
L147
+1.5VS_MPLL
C1018
0.1UF/10V
C1019
22UF/6.3V
L5779
+1.5VS_TVDAC
C6615
22NF/50V
L5780
+1.5VS_QTVDAC
C6617
22NF/50V
VCC_HV
C1004
0.1UF/10V
C1005
10UF/6.3V
C993
0.1UF/10V
C994
22UF/6.3V
C995
0.1UF/10V
C996
0.1UF/10V
PLACE IN CAVITY
C1001
4.7UF/6.3V
C1002
2.2UF/6.3V
PLACE ON THE EDGE
C1003
0.22UF/6.3V
CE34
100UF/4V
VCCA_DPLLA<50mA
VCCA_DPLLB<50mA
VCCA_HPLL<45mA
C6611
0.1UF/16V
c0402
U39H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G+VCCA_3GPLL<1500mA
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_3GBG<2mA
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
R6908
R6832
0Ohm
(no_stuff)
VCCA_LVDS
VSSA_LVDS
VCCA_3MPLL<45mA
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL[0:1]<150mA
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
C1006
0.1UF/10V
VCC_HV0
VCC_HV1
VCC_HV2
VCC_HV[0:2]<40mA
C1007
0.1UF/10V
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
CALISTOGA_Q137
POWER
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
VTT_26
VTT_27
VTT_28
VTT_29
VTT_30
VTT_31
VTT_32
VTT_33
VTT_34
VTT_35
VTT_36
VTT_37
VTT_38
VTT_39
VTT_40
VTT_41
VTT_42
VTT_43
VTT_44
VTT_45
VTT_46
VTT_47
VTT_48
VTT_49
VTT_50
VTT_51
VTT_52
VTT_53
VTT_54
VTT_55
VTT_56
VTT_57
VTT_58
VTT_59
VTT_60
VTT_61
VTT_62
VTT_63
VTT_64
VTT_65
VTT_66
VTT_67
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VTT < 1500mA
L2
180Ohm/100Mhz
C48
10UF/6.3V
C6619
22UF/6.3V
X5R
+3VS_TVDACA
C6622
22NF/50V
+3VS_TVDACB
C6621
22NF/50V
C54
0.1UF/16V
+3VS_TVDACC
C6620
22NF/50V
C58
0.1UF/16V
+3VS_TVBG
C6618
22NF/50V
VTTLF_CAP3
C1009
0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C1011
0.47UF/16V
C1012
0.22UF/6.3V
<Variant Name>
Title : Calistoga -- POWER (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 10 of 64



<Variant Name>

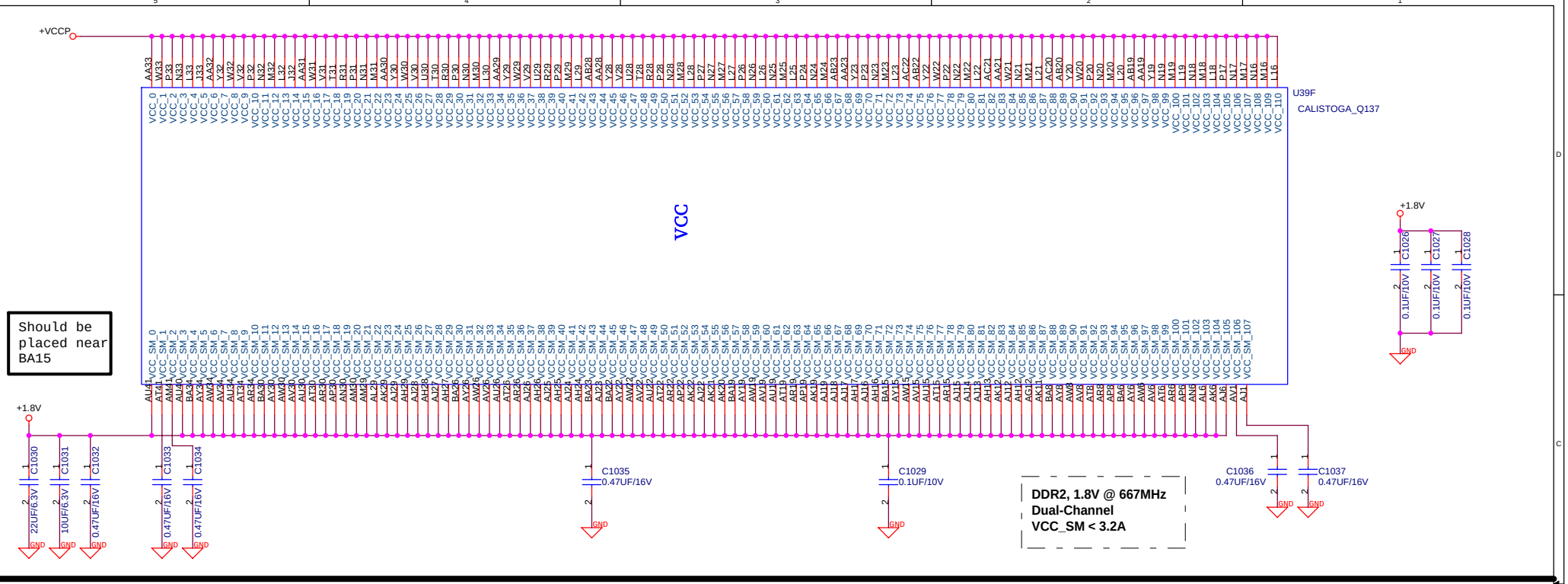
ASUSTeK COMPUTER INC

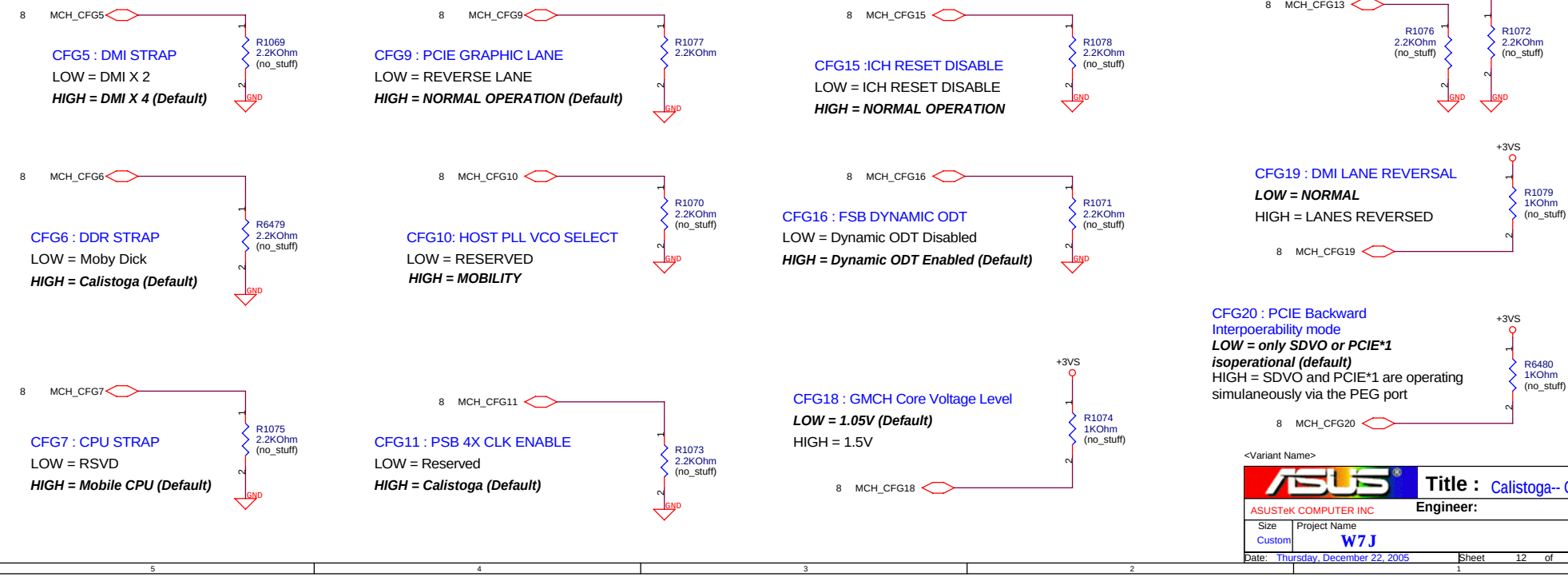
Title : Calistoga-- GND (5)

Engineer:

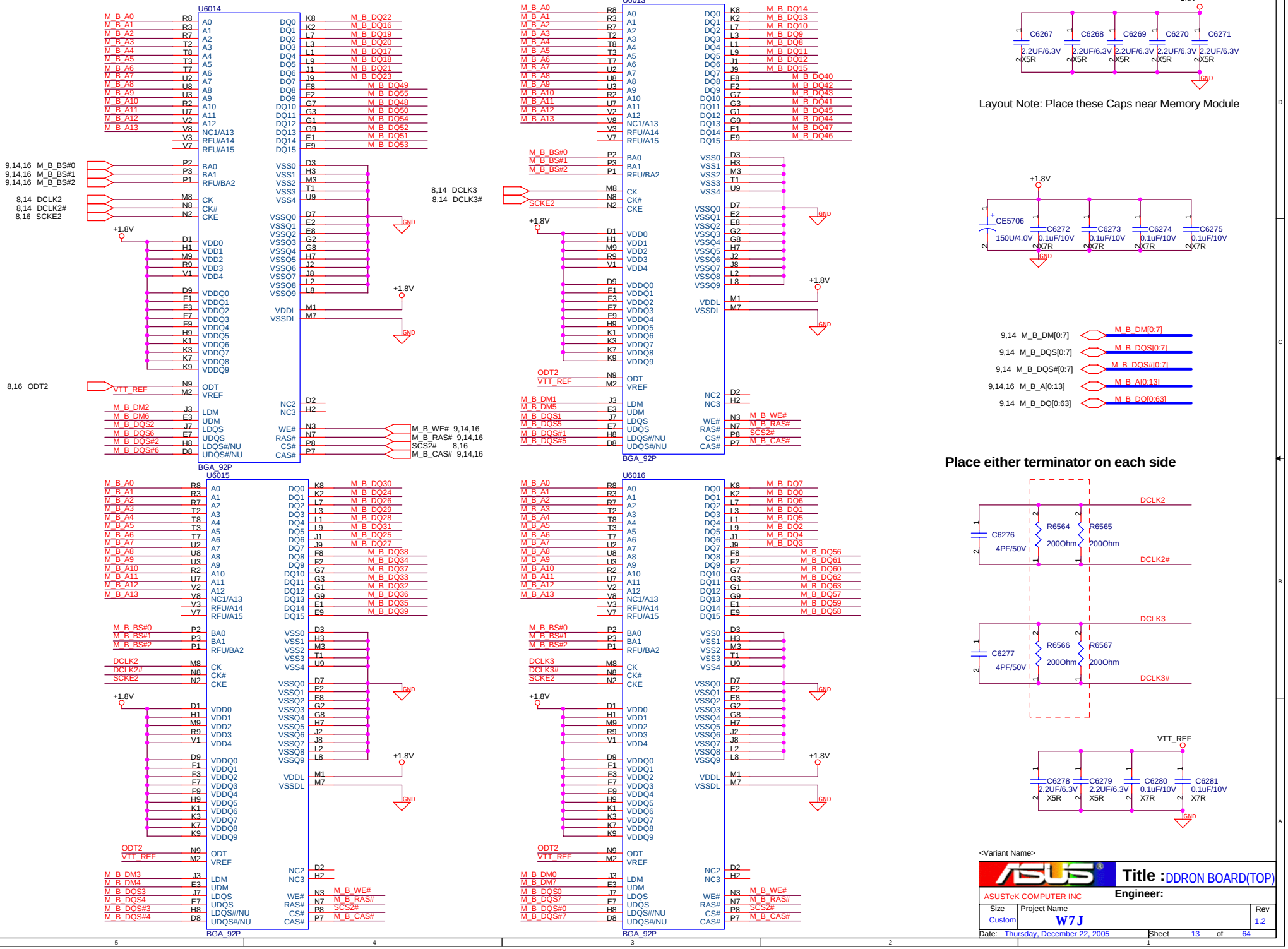
Size	Project Name	Rev
Custom	W7J	1.2

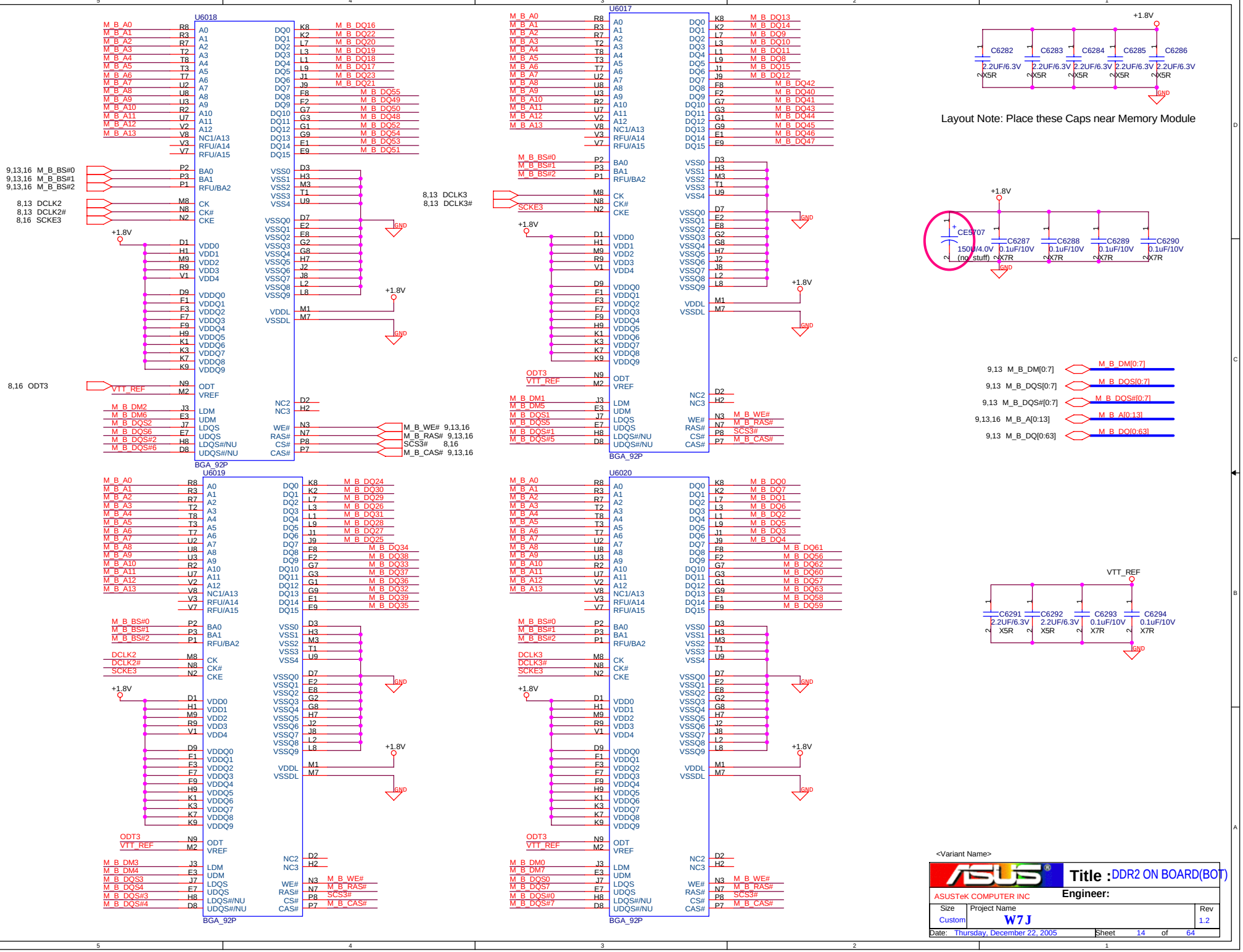
Date: Thursday, December 22, 2005 Sheet 11 of 64

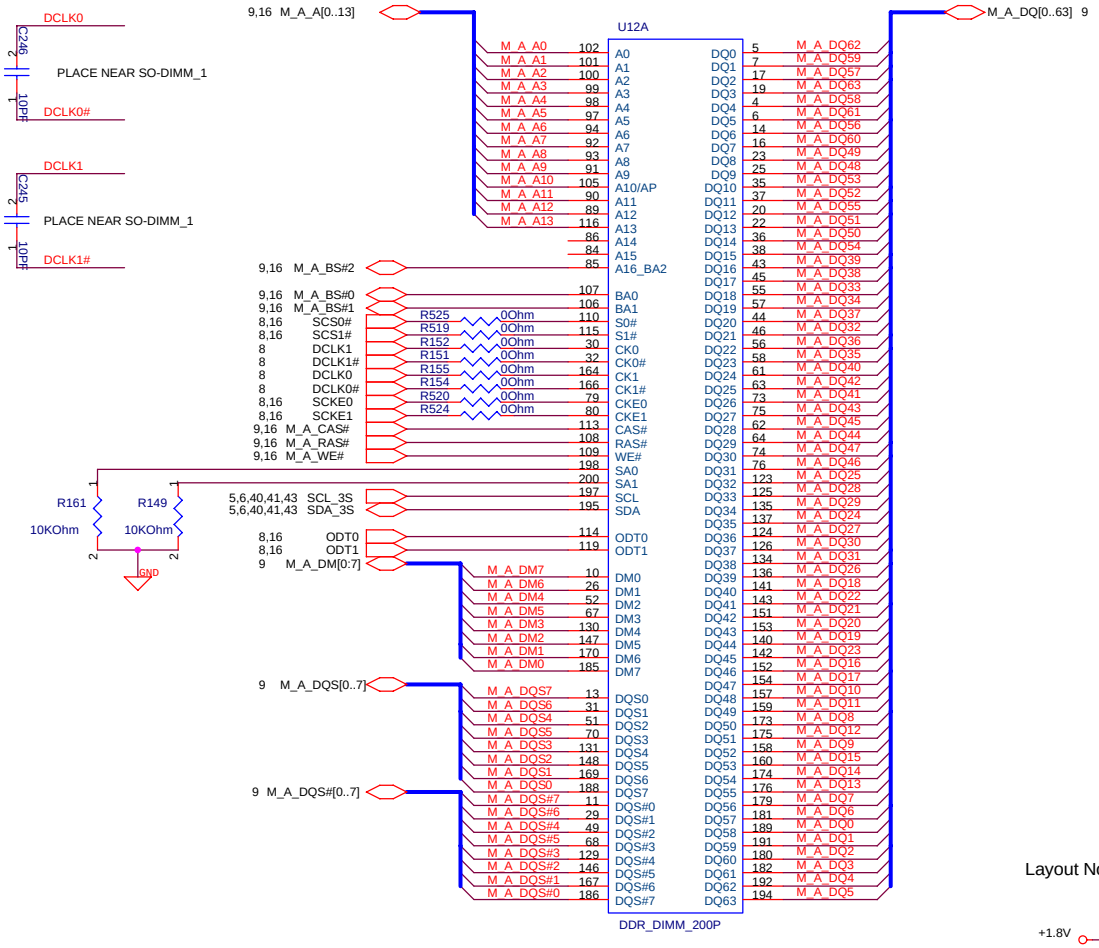




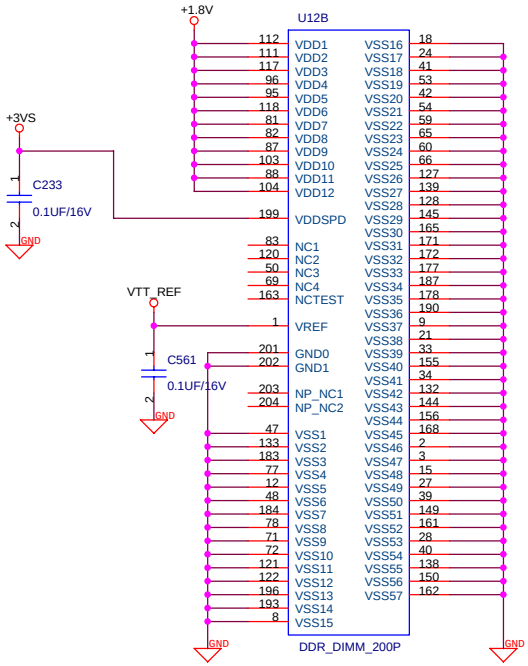
HIGH = LANES REVERSED


U6014
U6013
U6015
U6016
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
DCLK3
DCLK3#
SCKE2
ODT2
VTT_REF
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7
M_B_WE#
M_B_RAS#
M_B_CAS#
SCS2#
GND
+1.8V
9,14,16 M_B_BS#0
9,14,16 M_B_BS#1
9,14,16 M_B_BS#2
8,14 DCLK2
8,14 DCLK2#
8,16 SCKE2
8,14 DCLK3
8,14 DCLK3#
8,16 ODT2
M_B_WE# 9,14,16
M_B_RAS# 9,14,16
SCS2# 8,16
M_B_CAS# 9,14,16
C6267
C6268
C6269
C6270
C6271
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5706
150U/4.0V
C6272
C6273
C6274
C6275
0.1uF/10V
X7R
9,14 M_B_DM[0:7]
9,14 M_B_DQS[0:7]
9,14 M_B_DQS#[0:7]
9,14,16 M_B_A[0:13]
9,14 M_B_DQ[0:63]
Place either terminator on each side
C6276
4PF/50V
R6564
R6565
200Ohm
C6277
R6566
R6567
C6278
C6279
C6280
C6281
VTT_REF
<Variant Name>
Title : DDRON BOARD(TOP)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 13 of 64

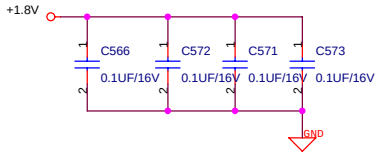

U6018
U6017
U6019
U6020
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
SCKE3
DCLK3
DCLK3#
ODT3
VTT_REF
M_B_DM2
M_B_DM6
M_B_DQS2
M_B_DQS6
M_B_DQS#2
M_B_DQS#6
M_B_DM3
M_B_DM4
M_B_DQS3
M_B_DQS4
M_B_DQS#3
M_B_DQS#4
M_B_DM1
M_B_DM5
M_B_DQS1
M_B_DQS5
M_B_DQS#1
M_B_DQS#5
M_B_DM0
M_B_DM7
M_B_DQS0
M_B_DQS7
M_B_DQS#0
M_B_DQS#7
M_B_WE#
M_B_RAS#
SCS3#
M_B_CAS#
+1.8V
GND
VTT_REF
C6282
C6283
C6284
C6285
C6286
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5707
150UF/4.0V
(no_stuff)
C6287
C6288
C6289
C6290
0.1uF/10V
X7R
M_B_DM[0:7]
M_B_DQS[0:7]
M_B_DQS#[0:7]
M_B_A[0:13]
M_B_DQ[0:63]
C6291
C6292
C6293
C6294
<Variant Name>
Title : DDR2 ON BOARD(BOT)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7 J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 14 of 64



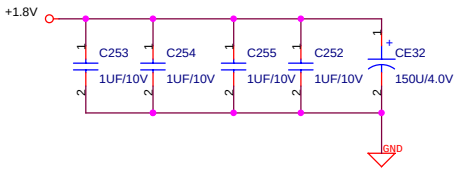
Top SO-DIMM:
12-025122005



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1



TOP SIDE:
Channel A

<Variant Name>

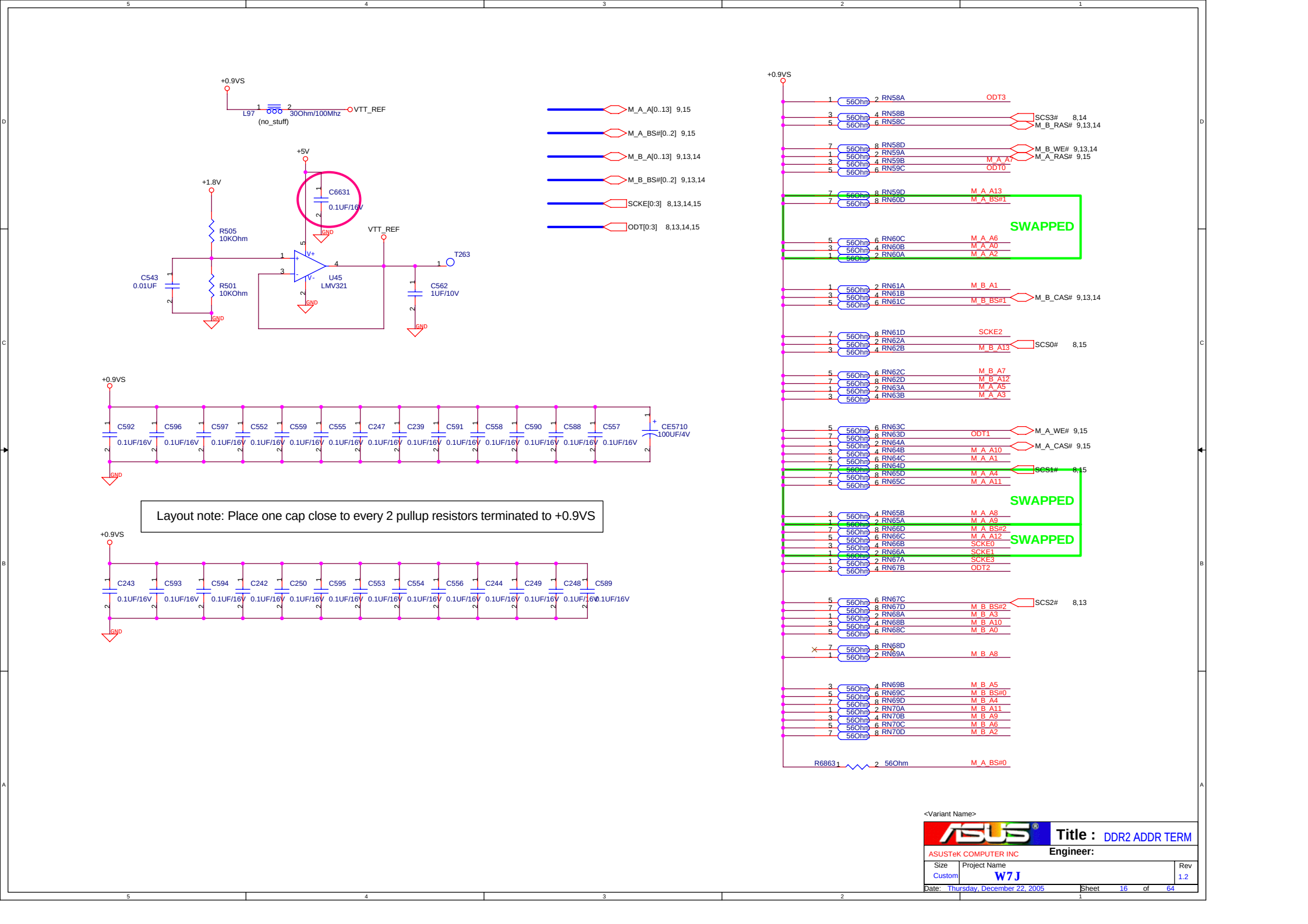
Title : DDR2 SO-DIMM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 15 of 64



<Variant Name>

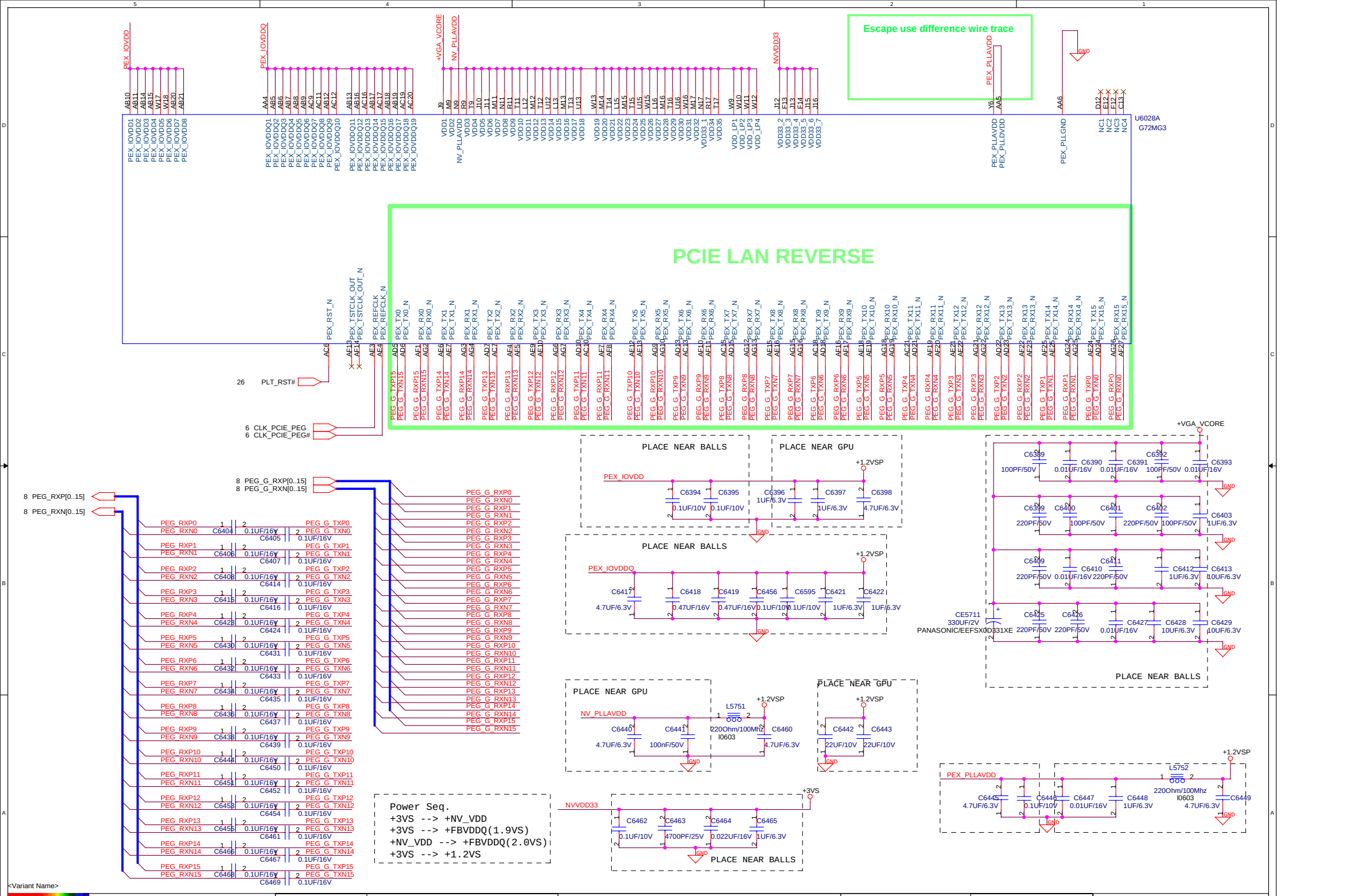
Title : DDR2 ADDR TERM

ASUSTeK COMPUTER INC

Engineer:

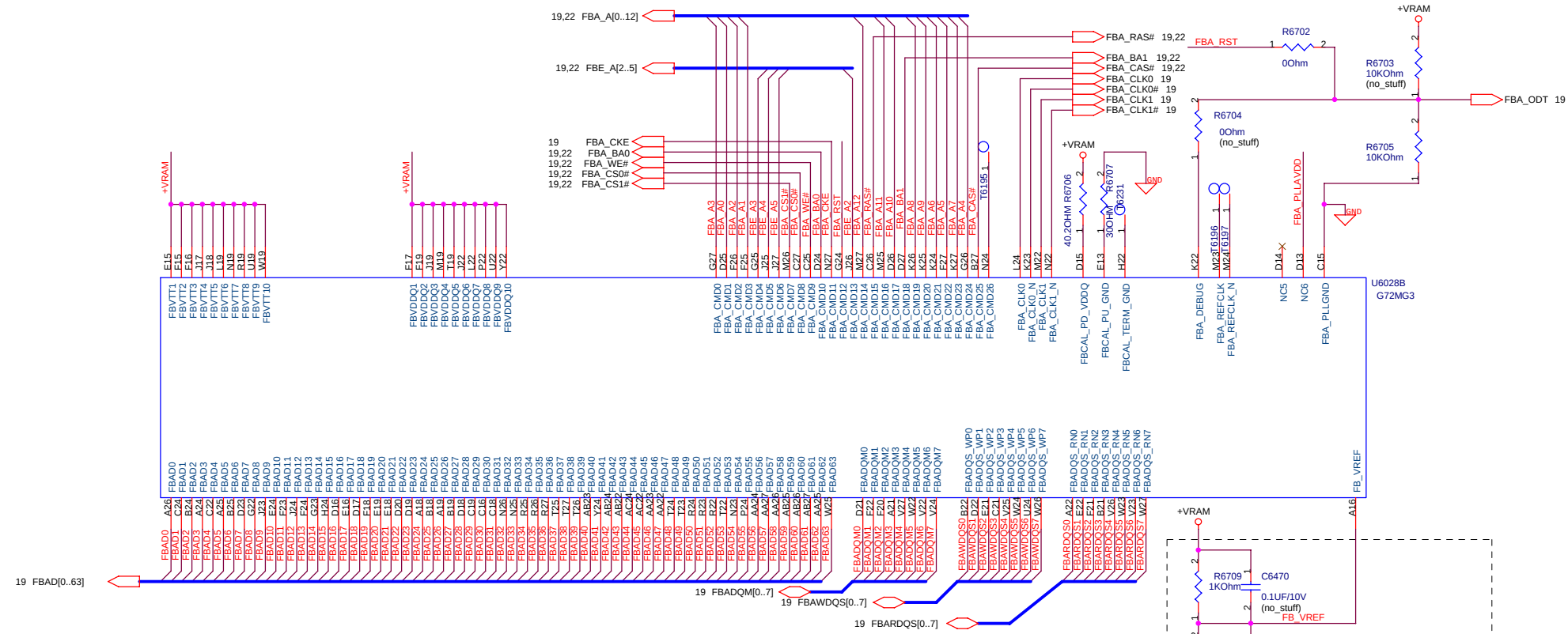
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 16 of 64

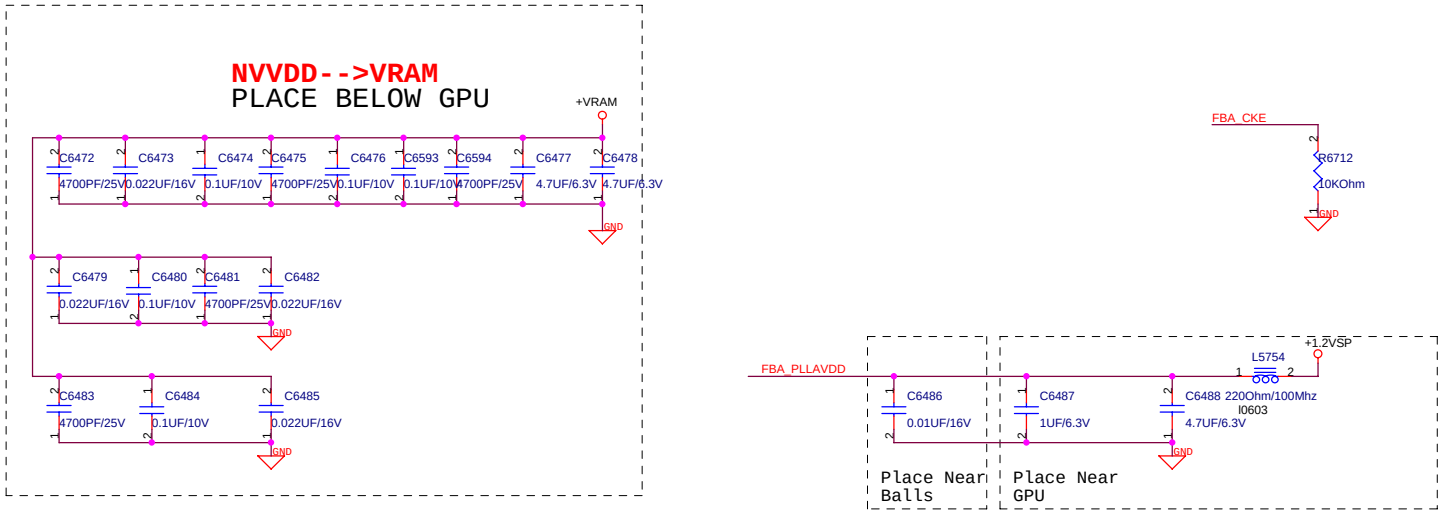


<Variant Name>

PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005 SHEET 17 OF 64	DESCRIPTION: G72M64: PCIE	SCHEMATIC FILE NAME : <OrgName> RELEASE DATE :	DESIGN ENGINEER :

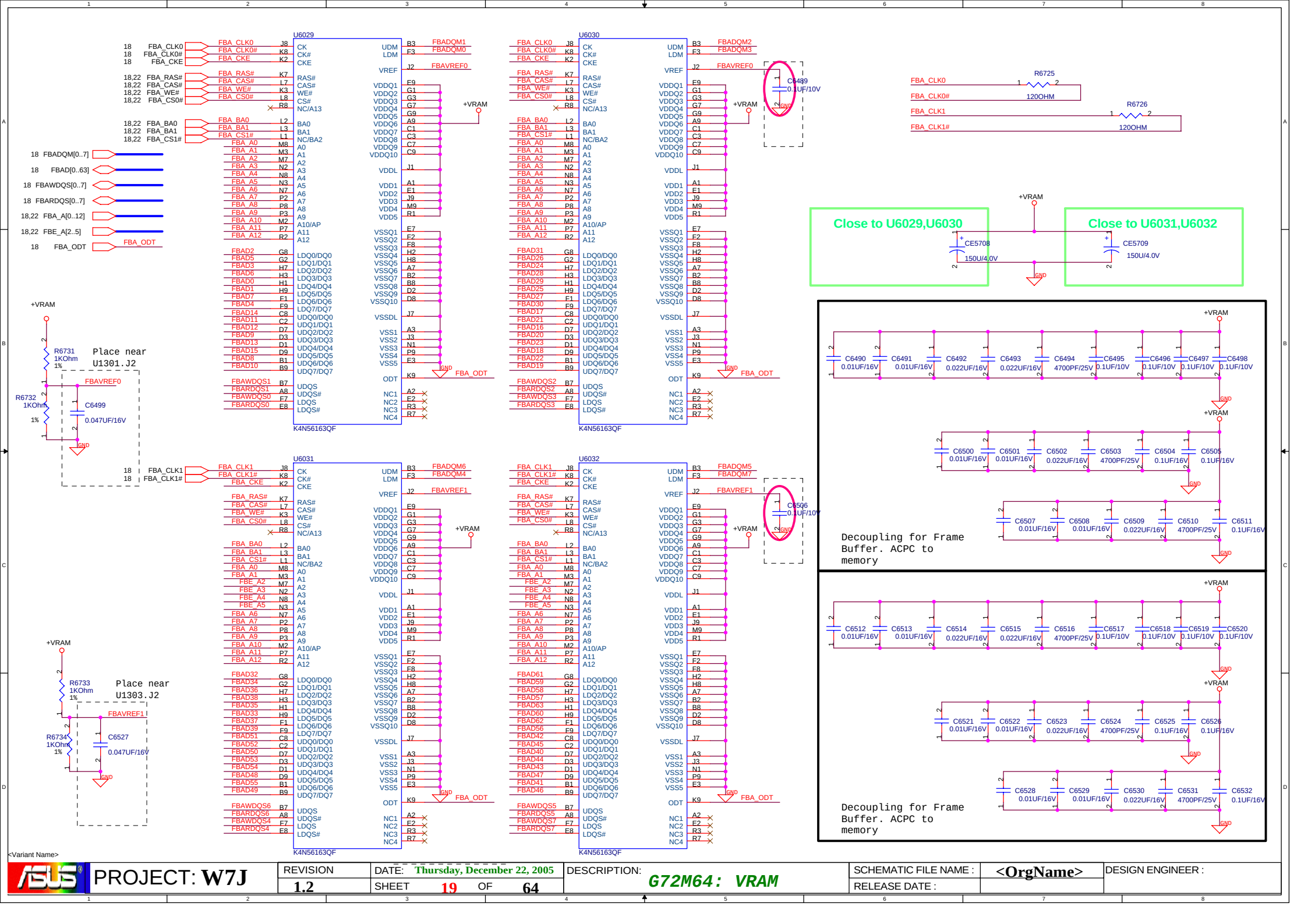


GDDR2 16x16 FBVDDQ 1.8V 84PIN



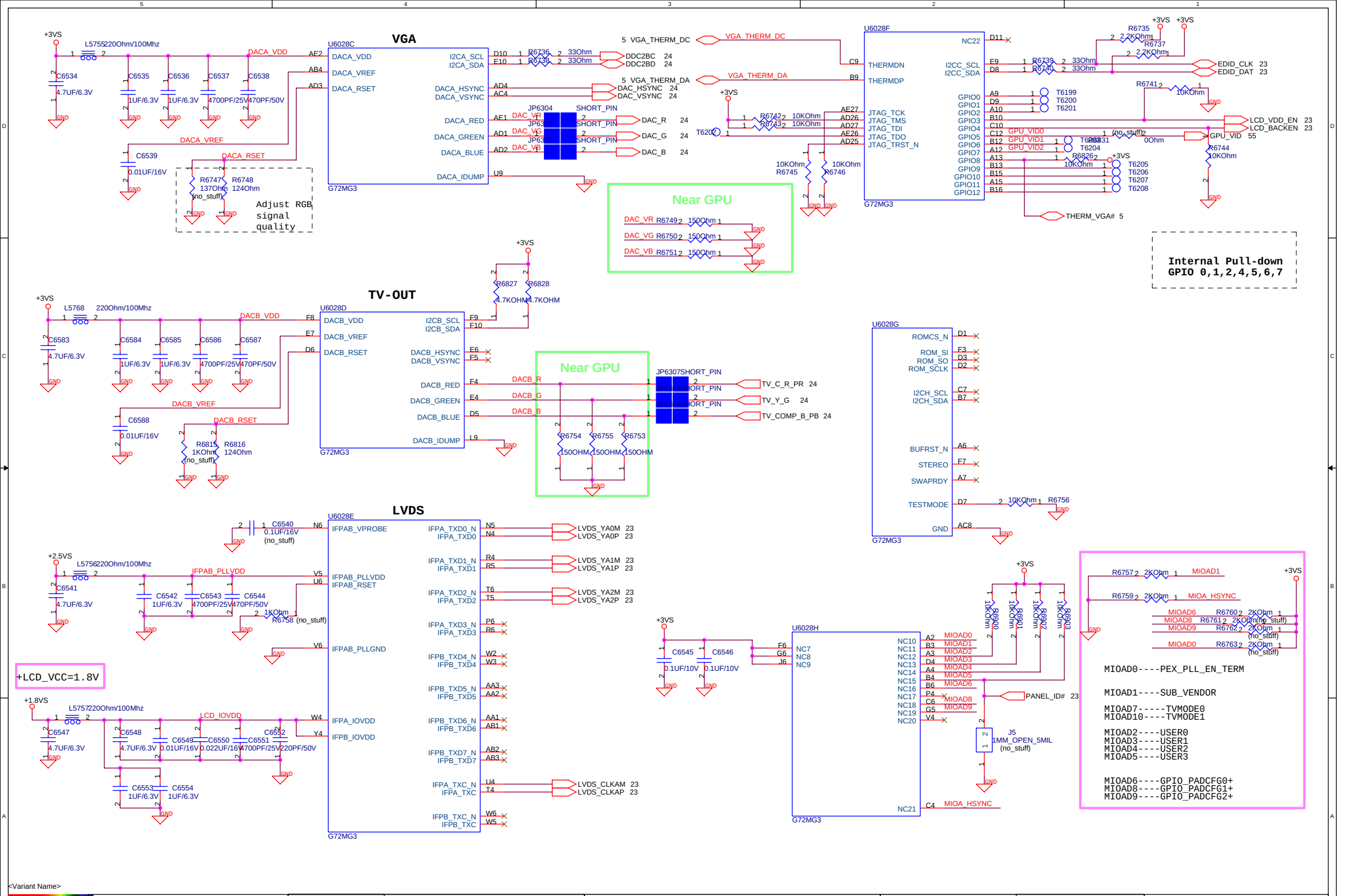
<Variant Name>

PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005 SHEET 18 OF 64	DESCRIPTION: G72M64: FB	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER :



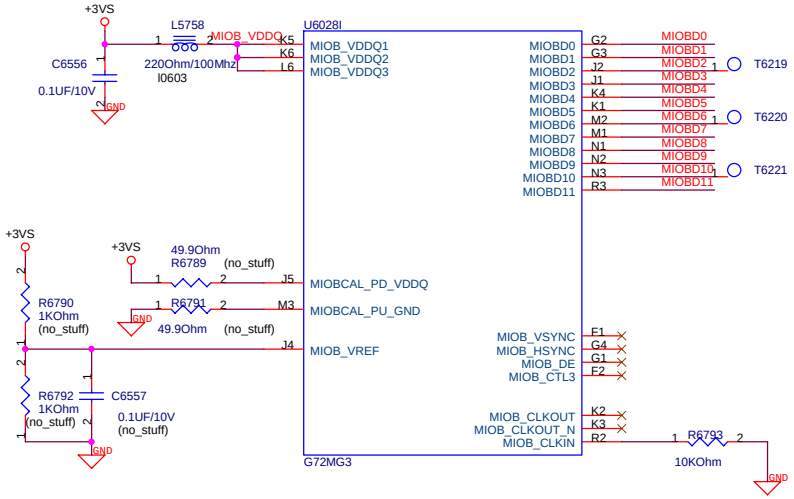
<Variant Name>

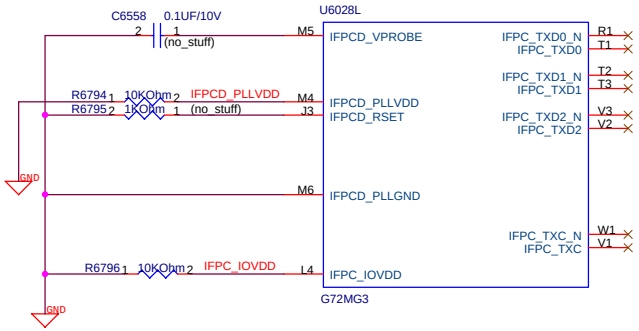
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: VRAM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 19 OF 64		RELEASE DATE :	

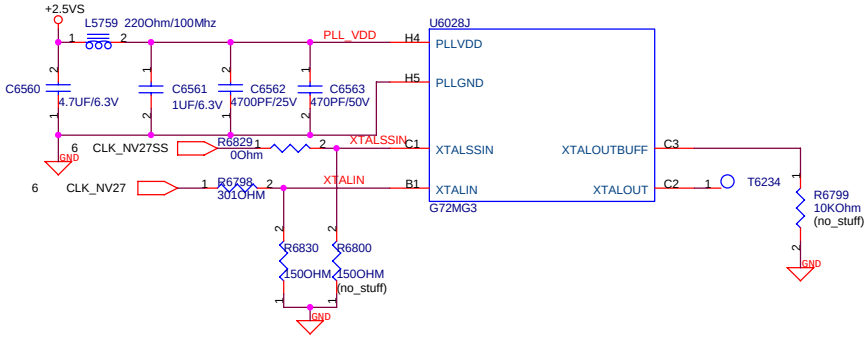


<Variant Name>

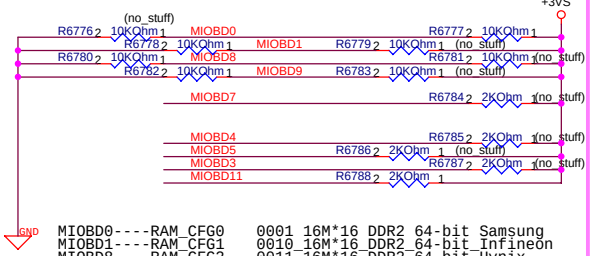
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005 SHEET 20 OF 64	DESCRIPTION: G72M64: RGB/LCD/ROM/GPIO	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER :



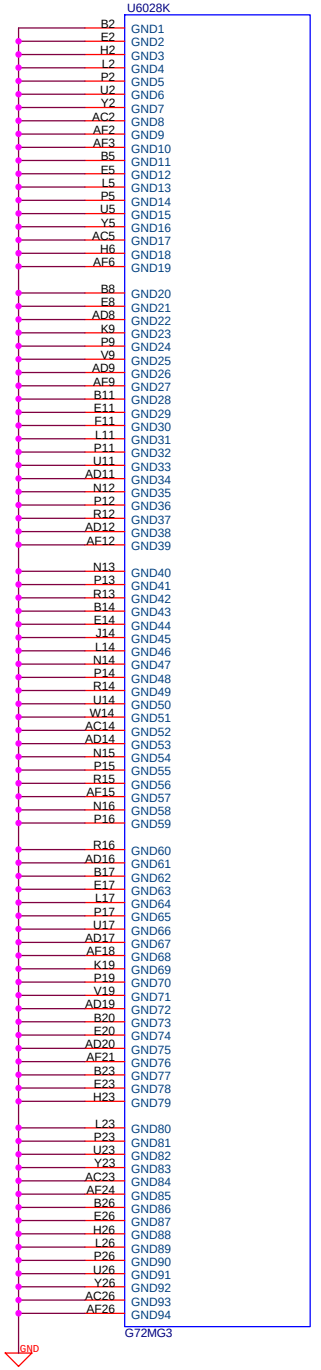




STRAP



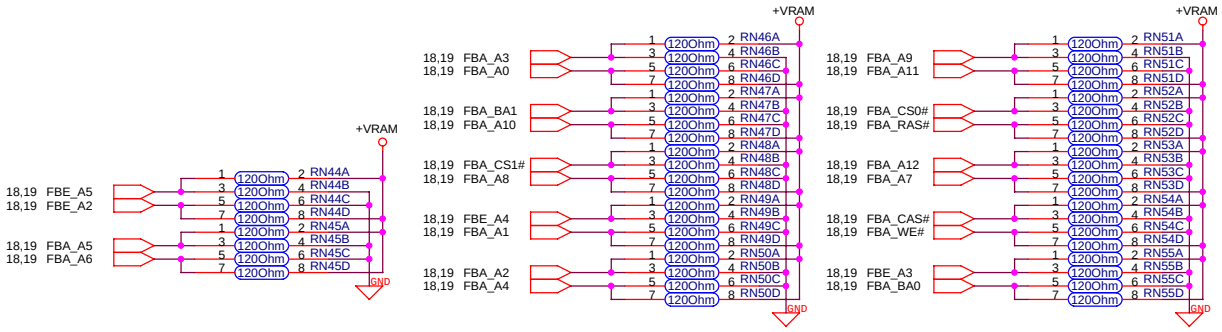

```
MIOBD0----RAM_CFG0    0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1    0010 16M*16 DDR2 64-bit Infineon
MIOBD8----RAM_CFG2    0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3
                      0101 32M*16 DDR2 64-bit Samsung
                      0110 32M*16 DDR2 64-bit Infineon
                      0111 32M*16 DDR2 64-bit Hynix


MIOBD9----RAM_CFG3    0 Full width of the frame buffer
                      1 Half width of the frame buffer


MIOBD2----CRYSTAL0    00,13.5MHZ
MIOBD6----CRYSTAL1    01,14.318MHZ
                      10,27MHZ(Default)
                      11,RESERVED

MIOBD4----PCI_DEVID0  0111 G72MV
MIOBD5----PCI_DEVID1  1000 G72M
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3


MIOBD10----ROMTYPE0   00,PARALLEL
MIOB_VSYNC-ROMTYPE1   01,SERIAL_AT25F
                      10,RESERVED
                      11,LPC

MIOBD7----MOBILE_MODE
```



<Variant Name>

PROJECT: **W7J**	REVISION **1.2**	DATE: **Thursday, December 22, 2005**	DESCRIPTION: ***G72M64: MIOB/CRYSTAL/TMDS***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **21** OF **64**		RELEASE DATE :		

FBA CMD/ADDR Termination



<Variant Name>

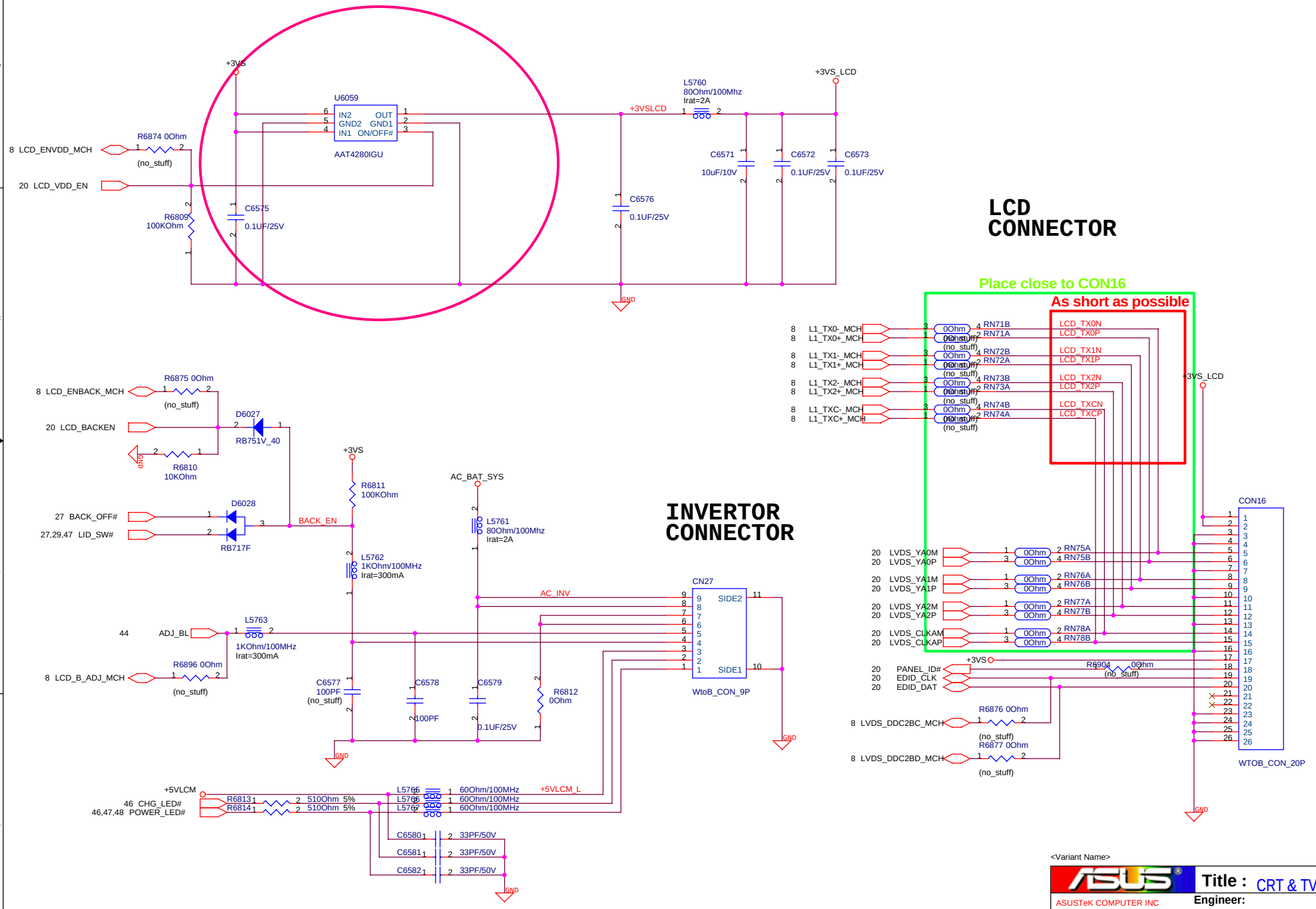
Title : G72M-Terminator

ASUSTeK COMPUTER INC

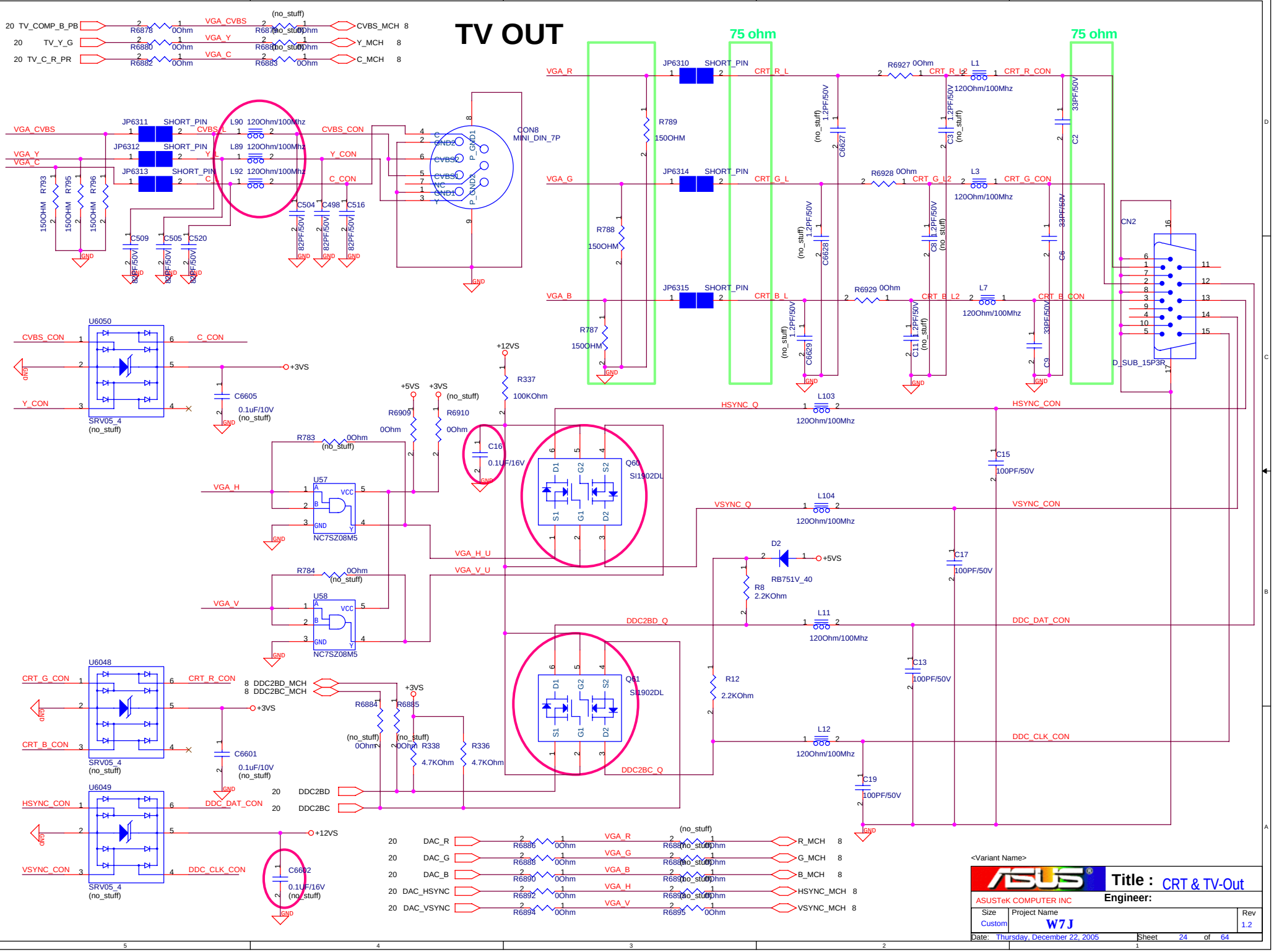
Engineer:

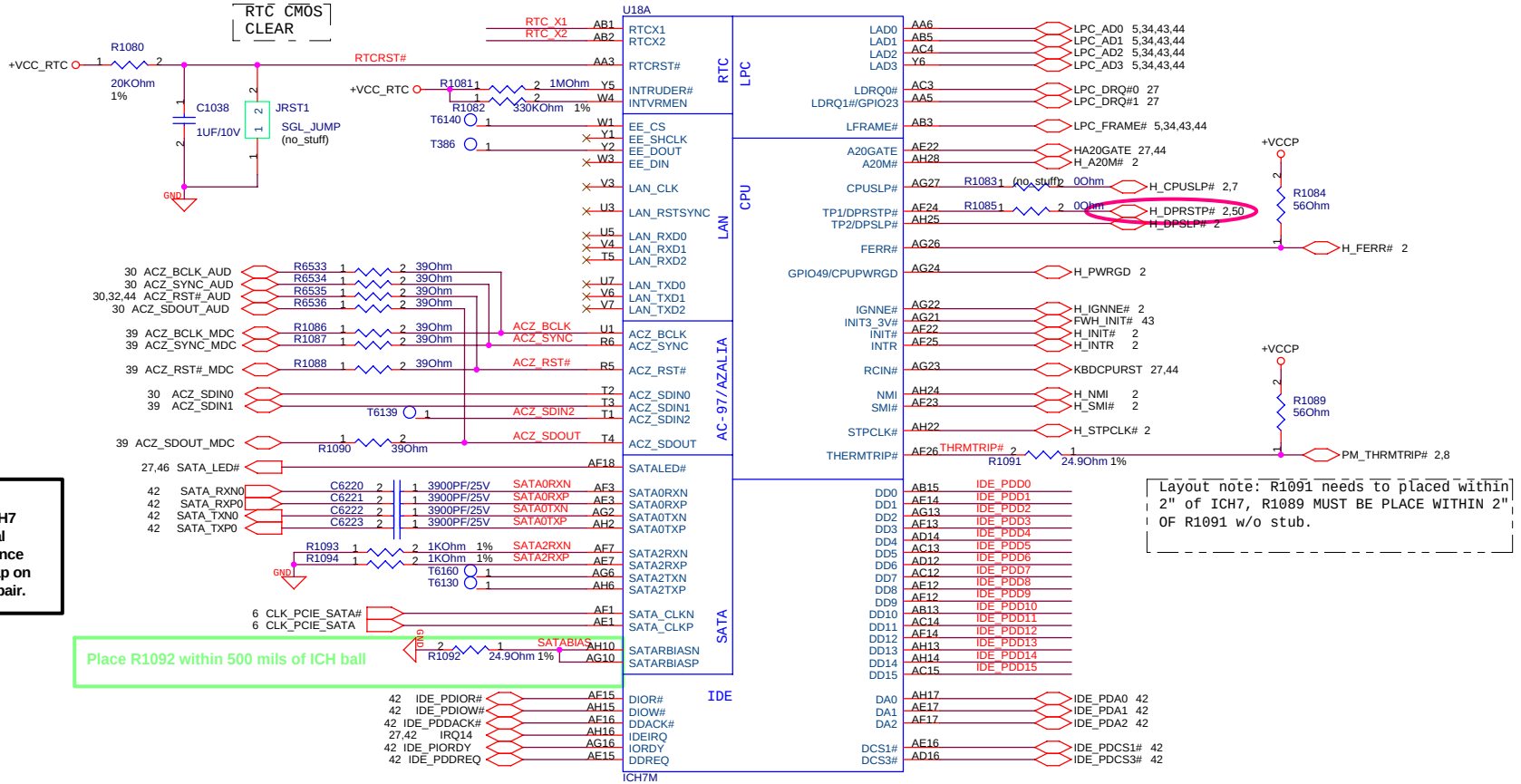
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 22 of 64


+3VS
U6059
IN2 OUT
GND2 GND1
IN1 ON/OFF#
AAT4280IGU
+3VSLCD
L5760
80Ohm/100Mhz
Irat=2A
+3VS_LCD
8 LCD_ENVDD_MCH
R6874 0Ohm
(no_stuff)
20 LCD_VDD_EN
R6809
100KOhm
C6575
0.1UF/25V
C6576
0.1UF/25V
C6571
10uF/10V
C6572
0.1UF/25V
C6573
0.1UF/25V
GND
LCD
CONNECTOR
Place close to CON16
As short as possible
8 L1_TX0-_MCH
8 L1_TX0+_MCH
8 L1_TX1-_MCH
8 L1_TX1+_MCH
8 L1_TX2-_MCH
8 L1_TX2+_MCH
8 L1_TXC-_MCH
8 L1_TXC+_MCH
0Ohm
(no_stuff)
RN71B
RN71A
RN72B
RN72A
RN73B
RN73A
RN74B
RN74A
LCD_TX0N
LCD_TX0P
LCD_TX1N
LCD_TX1P
LCD_TX2N
LCD_TX2P
LCD_TXCN
LCD_TXCP
+3VS_LCD
CON16
WTOB_CON_20P
8 LCD_ENBACK_MCH
R6875 0Ohm
(no_stuff)
20 LCD_BACKEN
D6027
RB751V_40
R6810
10KOhm
GND
+3VS
R6811
100KOhm
27 BACK_OFF#
27,29,47 LID_SW#
D6028
RB717F
BACK_EN
AC_BAT_SYS
L5761
80Ohm/100Mhz
Irat=2A
L5762
1KOhm/100MHz
Irat=300mA
INVERTOR
CONNECTOR
AC_INV
CN27
SIDE2
SIDE1
WtoB_CON_9P
44 ADJ_BL
L5763
1KOhm/100MHz
Irat=300mA
8 LCD_B_ADJ_MCH
R6896 0Ohm
(no_stuff)
C6577
100PF
(no_stuff)
C6578
100PF
C6579
0.1UF/25V
R6812
0Ohm
GND
20 LVDS_YA0M
20 LVDS_YA0P
20 LVDS_YA1M
20 LVDS_YA1P
20 LVDS_YA2M
20 LVDS_YA2P
20 LVDS_CLKAM
20 LVDS_CLKAP
RN75A
RN75B
RN76A
RN76B
RN77A
RN77B
RN78A
RN78B
+3VS
R6904 0Ohm
(no_stuff)
20 PANEL_ID#
20 EDID_CLK
20 EDID_DAT
R6876 0Ohm
8 LVDS_DDC2BC_MCH
(no_stuff)
R6877 0Ohm
8 LVDS_DDC2BD_MCH
(no_stuff)
+5VLCM
46 CHG_LED#
46,47,48 POWER_LED#
R6813 510Ohm 5%
R6814 510Ohm 5%
L5765 60Ohm/100MHz
L5766 60Ohm/100MHz
L5767 60Ohm/100MHz
+5VLCM_L
C6580 33PF/50V
C6581 33PF/50V
C6582 33PF/50V
GND
<Variant Name>
Title : CRT & TV-Out
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 23 of 64

TV OUT


75 ohm
75 ohm
CON8
MINI_DIN_7P
D_SUB_15P3R
SRV05_4
NC7SZ08M5
SI1902DL
RB751V_40
<Variant Name>
Title : CRT & TV-Out
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 24 of 64

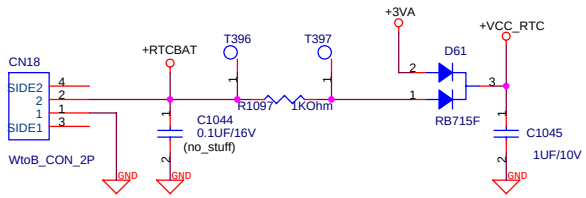


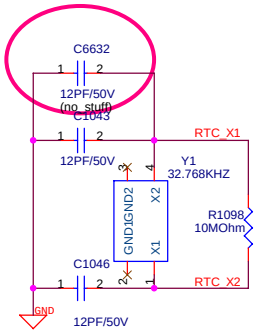
SATA:
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

IDE_PDD[0..15] — IDE_PDD[0..15] 42

RTC BAT





RTC Battery
P/N=07-016322032

<Variant Name>

Title : ICH7-M (1)
Engineer:
ASUSTeK COMPUTER INC
Size: Custom | Project Name: W7J | Rev: 1.2
Date: Thursday, December 22, 2005 | Sheet 25 of 64

36 PCI_AD[0..31] PCI_AD[0..31]

ICH7 Boot BIOS select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

GNT#3 without PD, if NOT top-block swap(inter high)

U18B

PCI_AD0 E18 … PCI_AD31 D6

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

PCI

REQ0# D7 → PCI_REQ#0 27,36
GNT0# E7 → PCI_GNT#0 36
REQ1# C16 → PCI_REQ#1 27
GNT1# D16 T6133
REQ2# C17 → PCI_REQ#2 27
GNT2# D17 T6170
REQ3# E13 → PCI_REQ#3 27
GNT3# F13 R6403 1KOhm (no_stuff) GND
REQ4#/GPIO22 A13 → PCI_REQ#4 27
GNT4#/GPIO48 A14 T6135
GPIO1/REQ5# C8 → PCI_REQ#5 27
GPIO17/GNT5# D8 T6136

C/BE0# B15 → PCI_C/BE#0 36
C/BE1# C12 → PCI_C/BE#1 36
C/BE2# D12 → PCI_C/BE#2 36
C/BE3# C15 → PCI_C/BE#3 36

IRDY# A7 → PCI_IRDY# 27,36
PAR E10 → PCI_PAR 36
PCIRST# B18 PCI_RST#_ICH
DEVSEL# A12 → PCI_DEVSEL# 27,36
PERR# C9 → PCI_PERR# 27,36
PLOCK# E11 → PCI_LOCK# 27
SERR# B10 → PCI_SERR# 27,36
STOP# F15 → PCI_STOP# 27,36
TRDY# F14 → PCI_TRDY# 27,36
FRAME# F16 → PCI_FRAME# 27,36

PLTRST# C26 PLT_RST#_SB
PCICLK A9 → CLK_ICHPCI 6
PME# B19

+3VSUS R6568 10KOhm

Interrupt I/F

27 PCI_INTA# A3 PIRQA# G8 GPIO2/PIRQE# → PCI_INTE# 27,36
27 PCI_INTB# B4 PIRQB# F7 GPIO3/PIRQF# → PCI_INTF# 27,36
27 PCI_INTC# C5 PIRQC# F8 GPIO4/PIRQG# → PCI_INTG# 27
27 PCI_INTD# B5 PIRQD# G7 GPIO5/PIRQH# → PCI_INTH# 27

MISC

T400 AE5 RSVD_1 AE9 T401
T403 AD5 RSVD_2 AG8 T404
T406 AG4 RSVD_3 AH8 T407
T409 AH4 RSVD_4 F21 T410
T411 AD9 RSVD_5 AH20 MCH_SYNC# 8
RSVD_6 RSVD_7 RSVD_8 RSVD_9

ICH7M

pull up to +3VS by internal pull-up resistor

U18D

40 PCIE_RXN1 F26 PERn1 … PCIE_TXP1 E27 PETp1
0.1UF/10V C1047 PETN1 C1048 PETP1
38 PCIE_RXN2 H26 PERn2 … PCIE_TXP2 G27 PETp2
C1049 PETN2 C1050 PETP2
41 PCIE_RXN3 K26 PERn3 … PCIE_TXP3 J27 PETp3
C1051 PETN3 C1052 PETP3
M26 PERn4 M25 PERp4 L28 PETn4 L27 PETp4
P26 PERn5 P25 PERp5 N28 PETn5 N27 PETp5
T25 PERn6 T24 PERp6 R28 PETn6 R27 PETp6

PCI-Express

Direct Media Interface

DMI0RXN V26 → DMI_RXN0 8
DMI0RXP V25 → DMI_RXP0 8
DMI0TXN U28 → DMI_TXN0 8
DMI0TXP U27 → DMI_TXP0 8
DMI1RXN Y26 → DMI_RXN1 8
DMI1RXP Y25 → DMI_RXP1 8
DMI1TXN W28 → DMI_TXN1 8
DMI1TXP W27 → DMI_TXP1 8
DMI2RXN AB26 → DMI_RXN2 8
DMI2RXP AB25 → DMI_RXP2 8
DMI2TXN AA28 → DMI_TXN2 8
DMI2TXP AA27 → DMI_TXP2 8
DMI3RXN AD25 → DMI_RXN3 8
DMI3RXP AD24 → DMI_RXP3 8
DMI3TXN AC28 → DMI_TXN3 8
DMI3TXP AC27 → DMI_TXP3 8
DMI_CLKN AE28 → CLK_PCIE_ICH# 6
DMI_CLKP AE27 → CLK_PCIE_ICH 6
DMI_ZCOMP C25
DMI_IRCOMP D25 DMICOMP
R1099 1% 24.9Ohm +1.5VS
Place within 500 mils of ICH

SPI_CLK R2
SPI_CS# P6
SPI_ARB P1
SPI_MOSI P5
SPI_MISO P2

SPI

USB

USBP0N E1 → USB_PN0 40
USBP0P F2 → USB_PP0 40
USBP1N G4 → USB_PN1 45
USBP1P G3 → USB_PP1 45
USBP2N H1 → USB_PN2 47
USBP2P H2 → USB_PP2 47
USBP3N J4 → USB_PN3 45
USBP3P J3 → USB_PP3 45
USBP4N K1 → USB_PN4 45
USBP4P K2 → USB_PP4 45
USBP5N L4 → USB_PN5 45
USBP5P L5 → USB_PP5 45
USBP6N M1
USBP6P M2
USBP7N N4 T405
N3 T408
USBRBIAS# D2 USBBIAS
USBRBIAS D1 R1100 22.6Ohm 1% GND
Place within 500 mils of ICH

+3V RN18A 10KOhm (no stuff) RN18B 10KOhm (no stuff)
RN18C 10KOhm (no stuff) RN18D 10KOhm (no stuff)

27,40 USB_OC#0 D3
27 USB_OC#2 C4
27,45 USB_OC#13 D5
27,45 USB_OC#4 D4
27 USB_OC#5 E5
27 USB_OC#6 C3
27 USB_OC#7 A2
B3

OC0# OC1# OC2# OC3# OC4# OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31

ICH7M

8,27,34,38,41,42,43,44 BUF_PLT_RST# → U68D 74HC08 (VCC 14, GND 7) 11 → 12 PLT_RST#_SB
+3V
C1056 0.01UF (no_stuff) GND

+3V
R1102 10KOhm C1054 0.1UF/16V GND

17 PLT_RST# R6408 0Ohm (no_stuff) → U68C 74HC08 (VCC 14, GND 7) 8 → 9
10 PLT_RST#_SB
R1104 0Ohm (no_stuff) SW_RST# 27
R1106 0Ohm

+3V C1053 0.1UF/16V GND
36,40,42 PCI_RST# → U68A 74HC08 (VCC 14, GND 7) 3 → 1 PCI_RST#_ICH

44 SET_PCIRSTNS# R1108 10KOhm
PCI_RST#
R1109 47KOhm
C1057 0.01UF GND
U69 74LVC1G32GV (VCC 5, GND 3, A 2, B 1, Y 4)
+3V C1055 0.1UF/16V GND
PCI_RSTNS# 36,44

Can be issue SCI or SMI List: GPI00~GPIO15
Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28

Only GPI Pin: GPI0~8,11~15,26,29,30,31,40(5V),41
Only GPO Pin: GPIO16~17,19,21,23,48
Can be GPIO: GPIO24,25,27,28,33,34
Resume Power Input Pin List:
BATLOW#,AC_SDIN[0:1],LAN_RST#,
OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#

<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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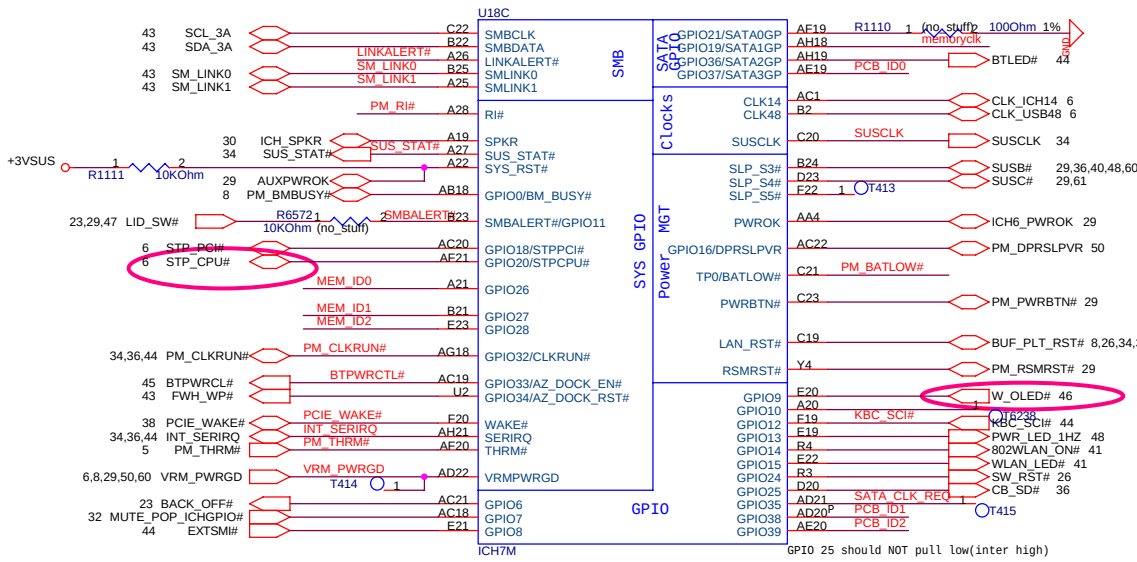
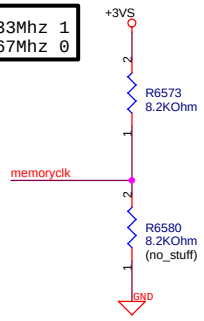
The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

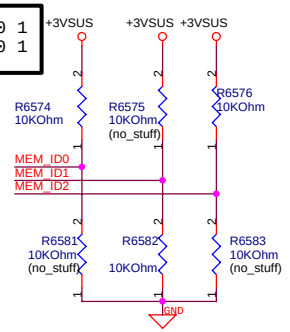


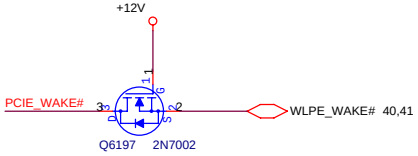
GPIO 16 should NOT pull high(inter low)

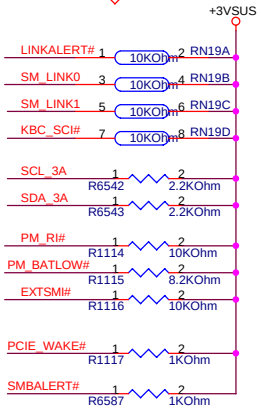
533Mhz 1
667Mhz 0

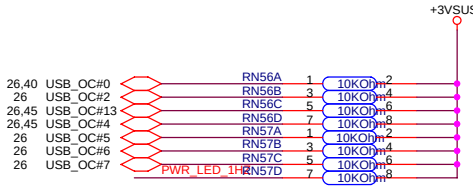


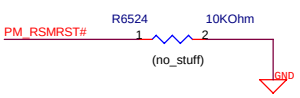
512M 1 0 1
256M 0 0 1

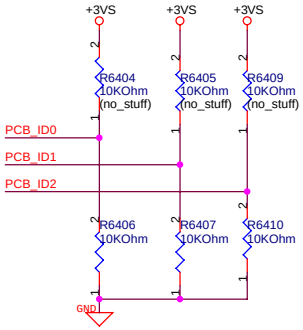


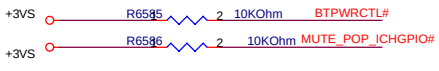


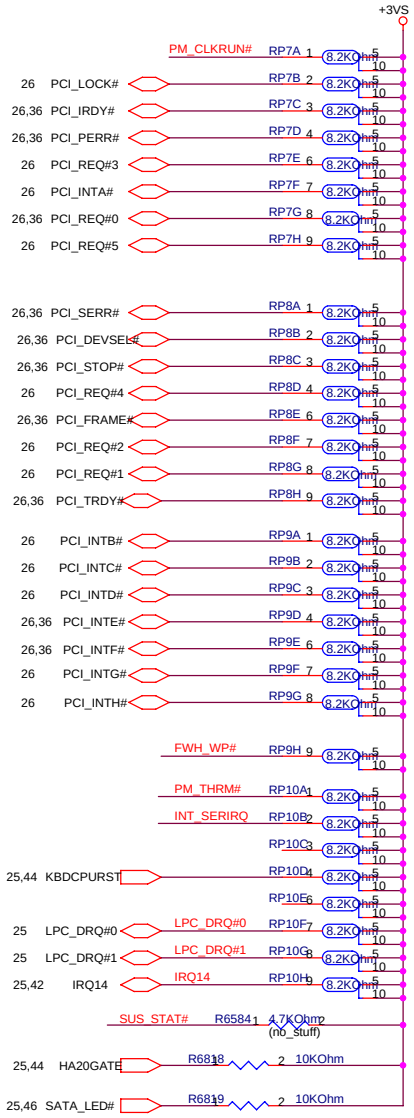












<Variant Name>

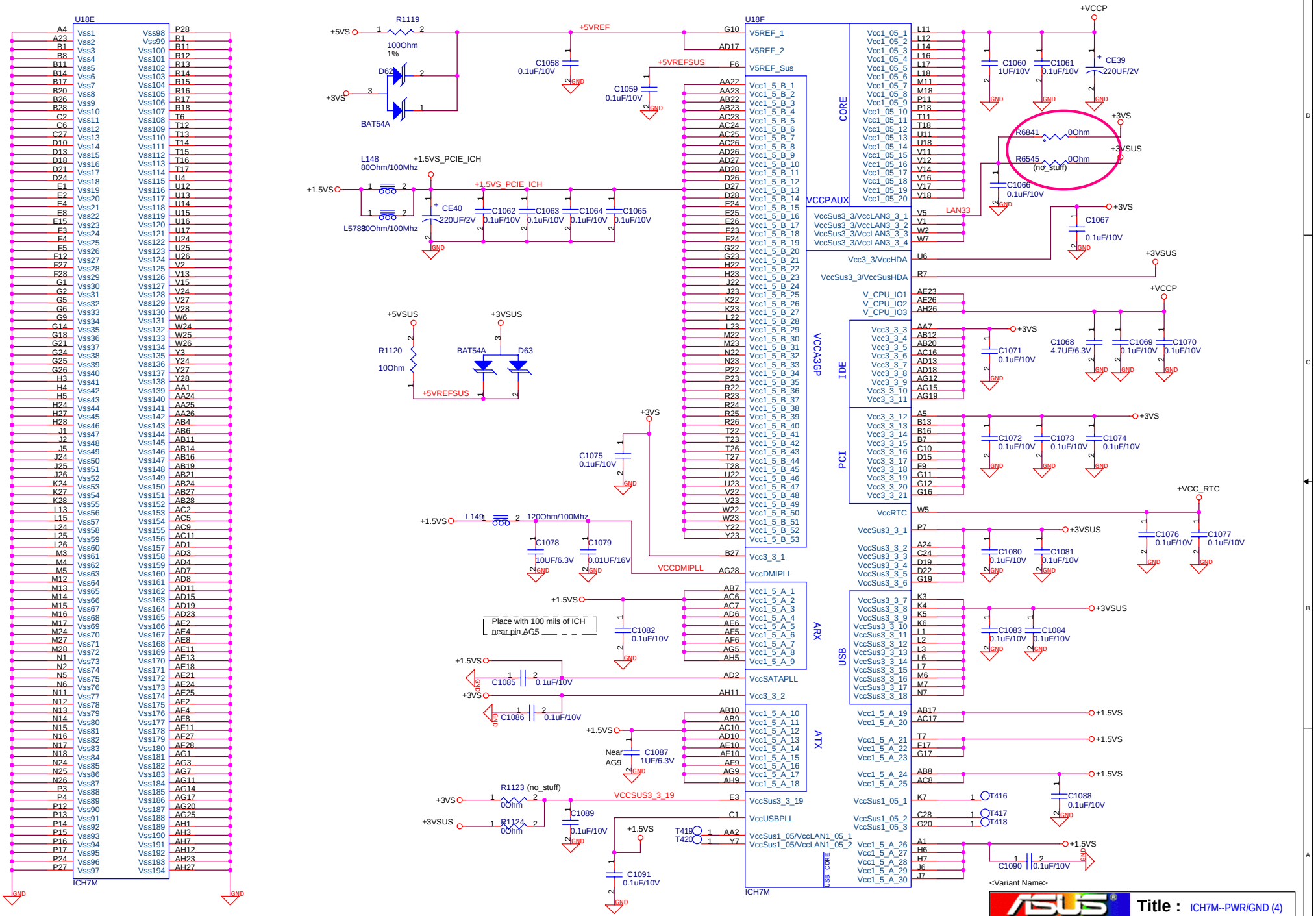
ASUSTeK COMPUTER INC

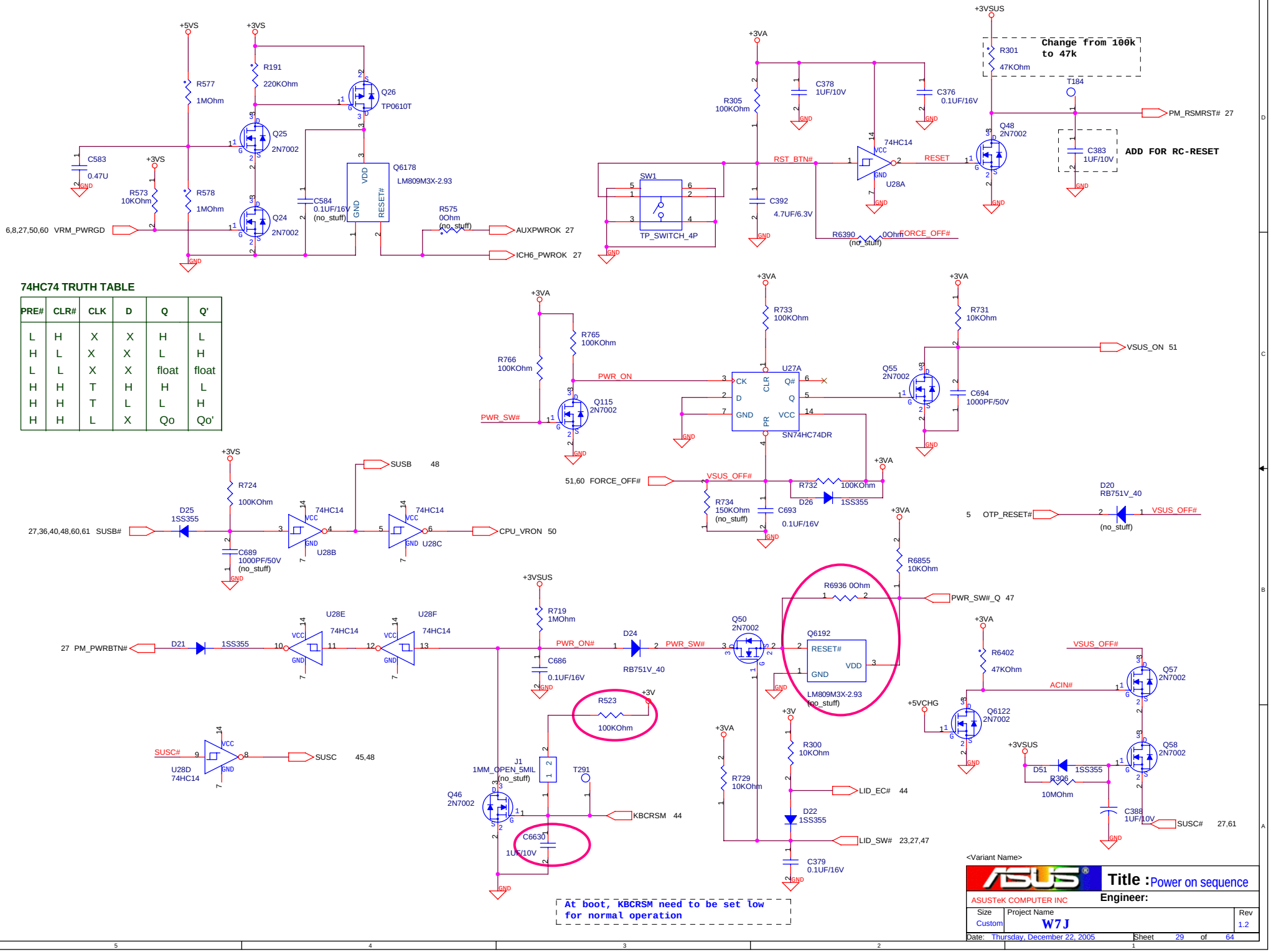
Title : ICH7M--(3)

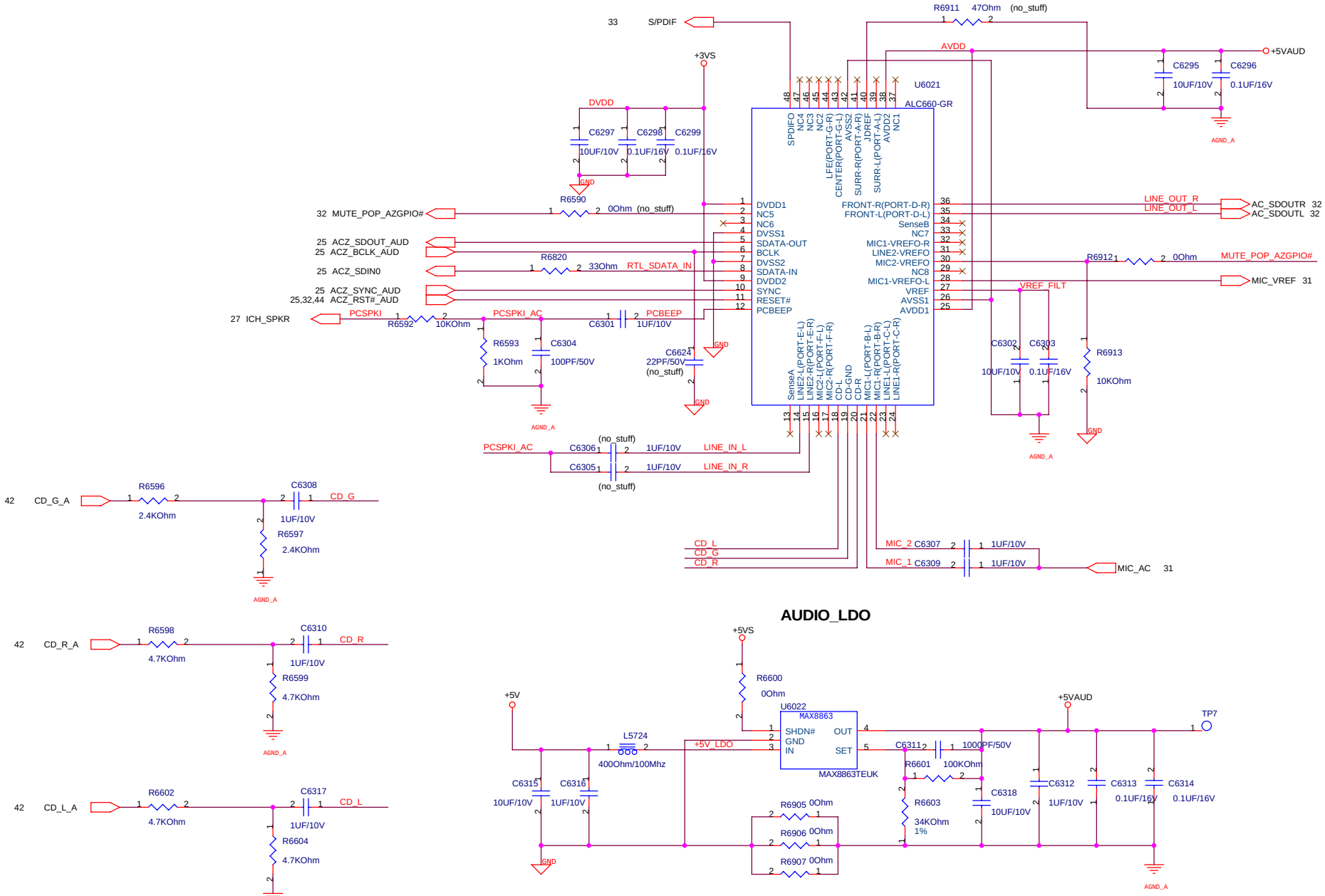
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 27 of 64


U18E
ICH7M
U18F
ICH7M
R1119
100Ohm
1%
BAT54A
D62
+5VS
+3VS
+5VREF
+5VREFSUS
C1058
0.1uF/10V
C1059
0.1uF/10V
L148
80Ohm/100Mhz
L57880Ohm/100Mhz
+1.5VS
+1.5VS_PCIE_ICH
CE40
220UF/2V
C1062
C1063
C1064
C1065
0.1uF/10V
R1120
10Ohm
+5VSUS
+3VSUS
BAT54A
D63
+5VREFSUS
C1075
0.1uF/10V
L149
120Ohm/100Mhz
C1078
10UF/6.3V
C1079
0.01UF/16V
VCCDMIPLL
Place with 100 mils of ICH
near pin AG5
C1082
0.1uF/10V
C1085
C1086
0.1uF/10V
Near
AG9
C1087
1UF/6.3V
R1123 (no_stuff)
0Ohm
R1124
0Ohm
VCCSUS3_3_19
C1089
0.1uF/10V
C1091
0.1uF/10V
T419
T420
CORE
VCCPAUX
VCCA3GP
IDE
PCI
ARX
ATX
USB
LAN3
C1060
1UF/10V
C1061
0.1uF/10V
CE39
220UF/2V
R6841
0Ohm
R6545
0Ohm
(no_stuff)
C1066
0.1uF/10V
C1067
0.1uF/10V
C1068
4.7UF/6.3V
C1069
0.1uF/10V
C1070
0.1uF/10V
C1071
0.1uF/10V
C1072
0.1uF/10V
C1073
0.1uF/10V
C1074
0.1uF/10V
C1076
0.1uF/10V
C1077
0.1uF/10V
C1080
0.1uF/10V
C1081
0.1uF/10V
C1083
0.1uF/10V
C1084
0.1uF/10V
C1088
0.1uF/10V
C1090
0.1uF/10V
T416
T417
T418
+VCCP
+VCC_RTC
+3VSUS
+1.5VS
GND
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICH7M--PWR/GND (4)
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 28 of 64


+5VS
+3VS
R577
1MOhm
R191
220KOhm
Q26
TP0610T
Q25
2N7002
C583
0.47U
R573
10KOhm
R578
1MOhm
Q24
2N7002
C584
0.1UF/16V
(no_stuff)
Q6178
LM809M3X-2.93
VDD
GND
RESET#
R575
0Ohm
(no_stuff)
6,8,27,50,60 VRM_PWRGD
AUXPWROK 27
ICH6_PWROK 27
+3VA
R305
100KOhm
C378
1UF/10V
C376
0.1UF/16V
SW1
TP_SWITCH_4P
RST_BTN#
74HC14
VCC
GND
U28A
RESET
C392
4.7UF/6.3V
R6390
0Ohm
(no_stuff)
FORCE_OFF#
+3VSUS
R301
47KOhm
Change from 100k
to 47k
T184
PM_RSMRST# 27
Q48
2N7002
C383
1UF/10V
ADD FOR RC-RESET
74HC74 TRUTH TABLE
PRE# CLR# CLK D Q Q'
L H X X H L
H L X X L H
L L X X float float
H H T H H L
H H T L L H
H H L X Qo Qo'
R765
100KOhm
R766
100KOhm
PWR_ON
PWR_SW#
Q115
2N7002
R733
100KOhm
U27A
CK
D
GND
CLR
PR
Q#
Q
VCC
SN74HC74DR
R731
10KOhm
VSUS_ON 51
Q55
2N7002
C694
1000PF/50V
51,60 FORCE_OFF#
VSUS_OFF#
R732
100KOhm
D26
1SS355
R734
150KOhm
(no_stuff)
C693
0.1UF/16V
D20
RB751V_40
(no_stuff)
5 OTP_RESET#
R724
100KOhm
SUSB 48
D25
1SS355
27,36,40,48,60,61 SUSB#
74HC14
U28B
U28C
C689
1000PF/50V
(no_stuff)
CPU_VRON 50
R6855
10KOhm
PWR_SW#_Q 47
R6936 0Ohm
+3VSUS
R719
1MOhm
U28E
U28F
27 PM_PWRBTN#
D21
1SS355
PWR_ON#
D24
RB751V_40
PWR_SW#
Q50
2N7002
Q6192
RESET#
VDD
GND
LM809M3X-2.93
(no_stuff)
C686
0.1UF/16V
R523
100KOhm
+3V
SUSC# 45,48
U28D
74HC14
J1
1MM_OPEN_5MIL
(no_stuff)
T291
Q46
2N7002
KBCRSM 44
C6630
1UF/10V
R729
10KOhm
R300
10KOhm
LID_EC# 44
D22
1SS355
LID_SW# 23,27,47
C379
0.1UF/16V
R6402
47KOhm
ACIN#
+5VCHG
Q6122
2N7002
Q57
2N7002
Q58
2N7002
D51
1SS355
R306
10MOhm
C388
1UF/10V
SUSC# 27,61
At boot, KBCRSM need to be set low
for normal operation
<Variant Name>
Title : Power on sequence
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 29 of 64



<Variant Name>

ASUSTeK COMPUTER INC

Title : AZALIA_ALC660

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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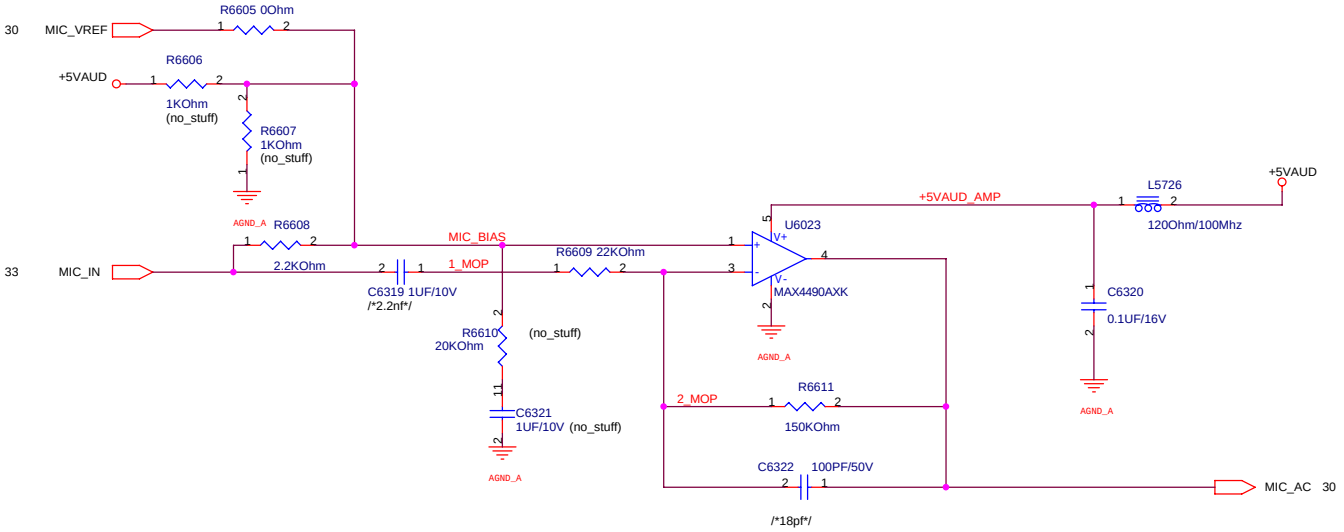
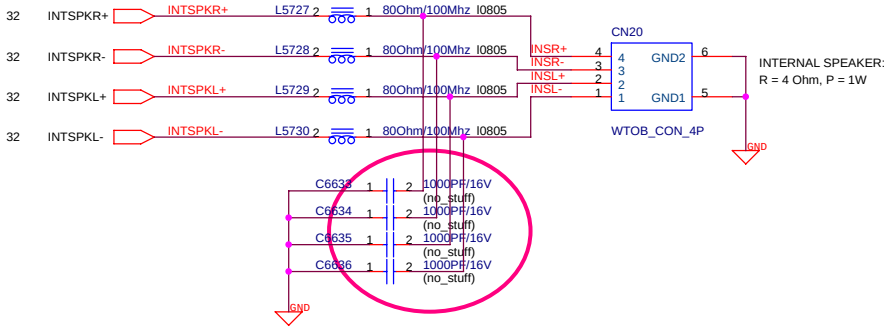
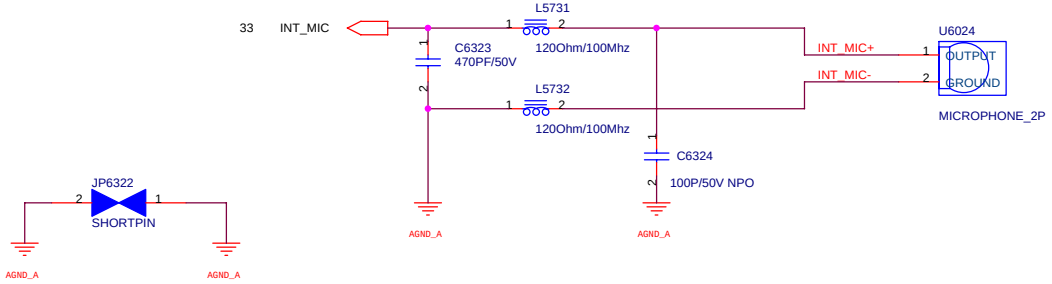
MIC PreAmp & Mic Jack







<Variant Name>

Title : MIC PREAMP & INT MIC

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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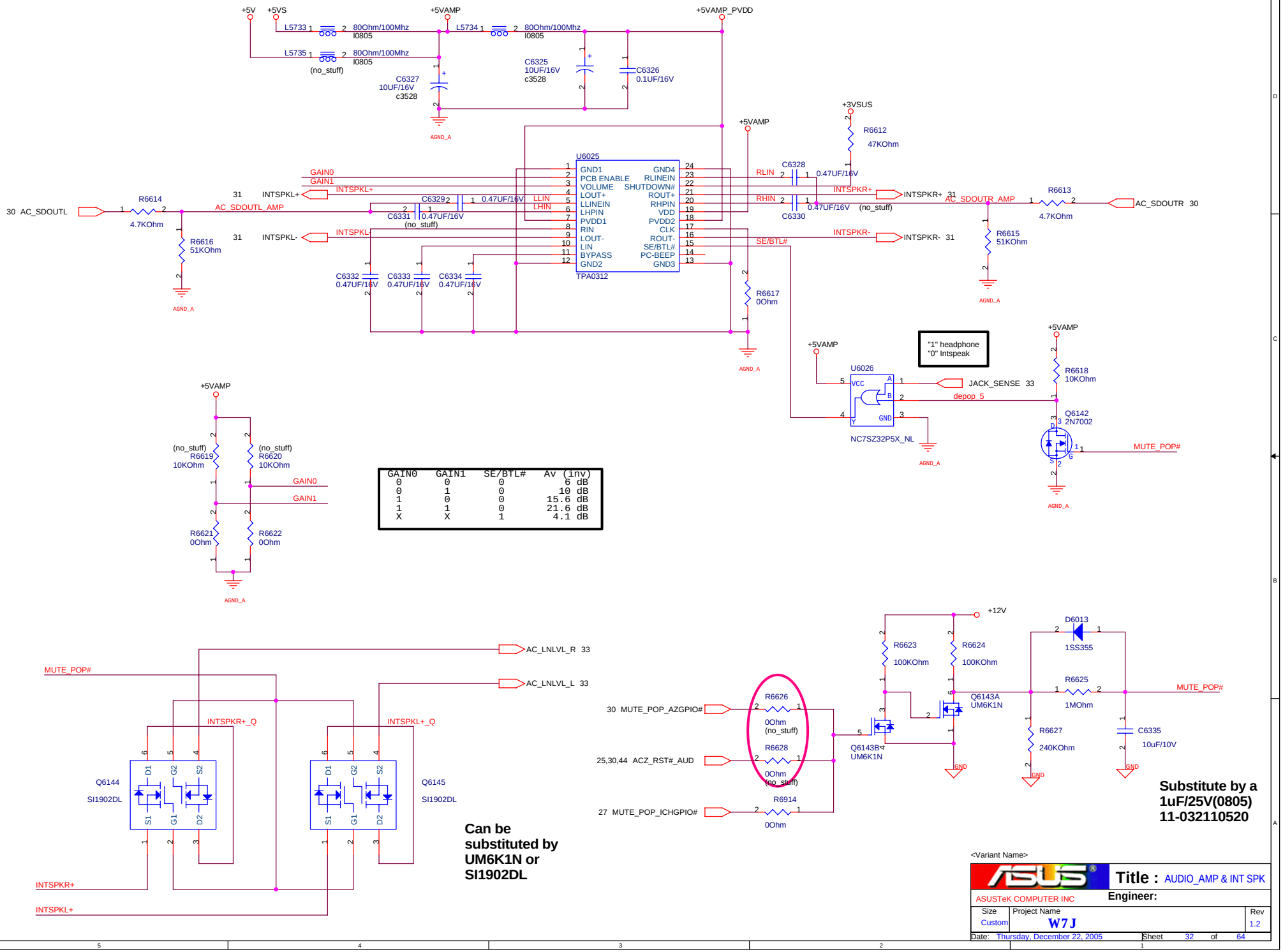
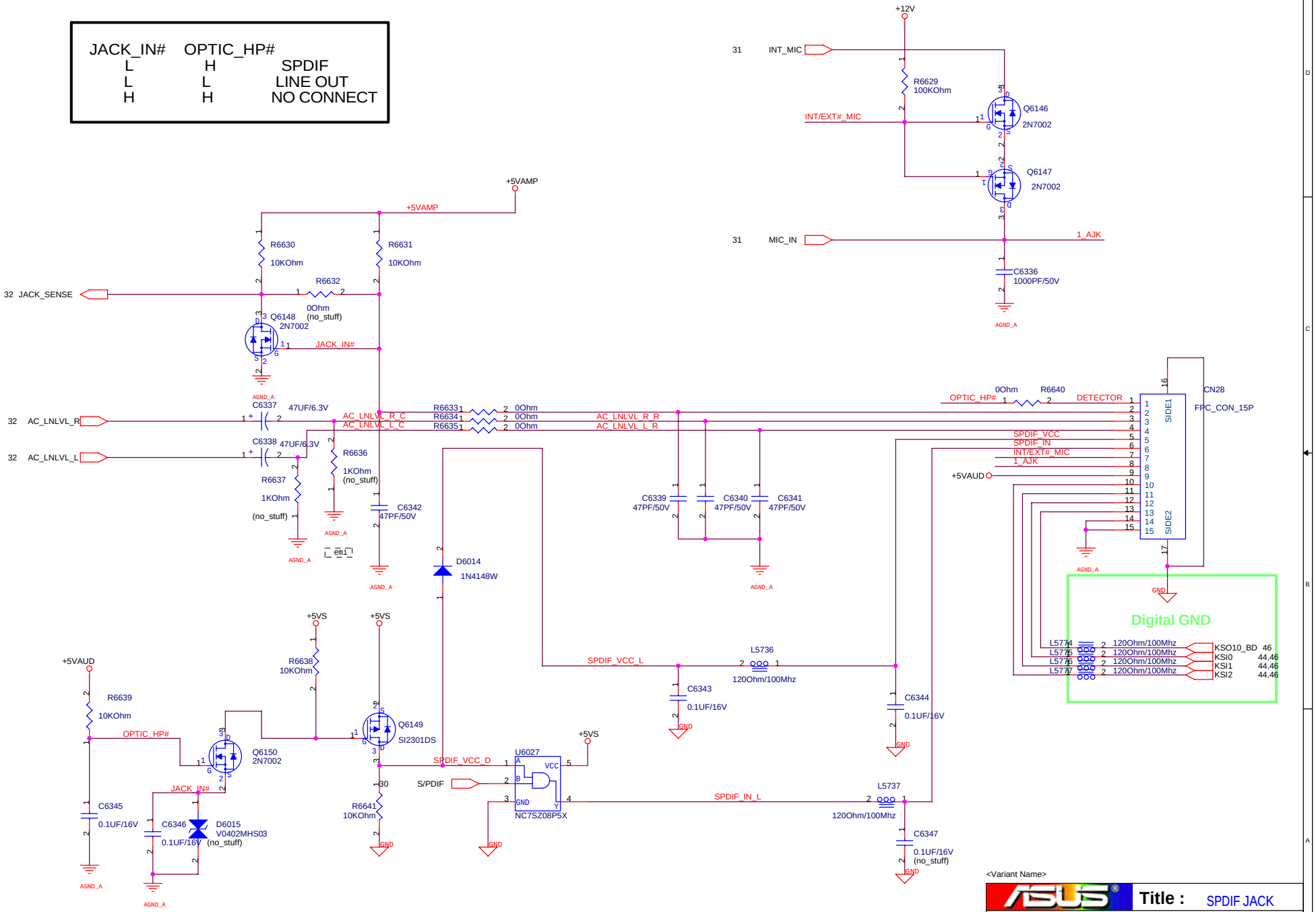

+5V
+5VS
+5VAMP
+5VAMP_PVDD
L5733 80Ohm/100Mhz l0805
L5734 80Ohm/100Mhz l0805
L5735 80Ohm/100Mhz l0805
(no_stuff)
C6327 10UF/16V c3528
C6325 10UF/16V c3528
C6326 0.1UF/16V
AGND_A
+3VSUS
R6612 47KOhm
U6025
GND1
PCB ENABLE
VOLUME
LOUT+
LLINEIN
LHPIN
PVDD1
RIN
LOUT-
LIN
BYPASS
GND2
GND4
RLINEIN
SHUTDOWN#
ROUT+
RHPIN
VDD
PVDD2
CLK
ROUT-
SE/BTL#
PC-BEEP
GND3
TPA0312
GAIN0
GAIN1
INTSPKL+
INTSPKL-
INTSPKL
INTSPKR+
INTSPKR-
RLIN
RHIN
LLIN
LHIN
SE/BTL#
C6328 0.47UF/16V
C6330 0.47UF/16V (no_stuff)
C6329 0.47UF/16V
C6331 0.47UF/16V (no_stuff)
C6332 0.47UF/16V
C6333 0.47UF/16V
C6334 0.47UF/16V
R6614 4.7KOhm
R6616 51KOhm
R6613 4.7KOhm
R6615 51KOhm
R6617 0Ohm
30 AC_SDOUTL
AC_SDOUTL_AMP
AC_SDOUTR_AMP
AC_SDOUTR 30
31 INTSPKL+
31 INTSPKL-
INTSPKR+ 31
INTSPKR- 31
"1" headphone
"0" Intspeak
U6026
VCC
GND
NC7SZ32P5X_NL
JACK_SENSE 33
depop_5
R6618 10KOhm
Q6142 2N7002
MUTE_POP#
(no_stuff) R6619 10KOhm
(no_stuff) R6620 10KOhm
R6621 0Ohm
R6622 0Ohm
GAIN0
GAIN1
GAIN0 GAIN1 SE/BTL# Av (inv)
0 0 0 6 dB
0 1 0 10 dB
1 0 0 15.6 dB
1 1 0 21.6 dB
X X 1 4.1 dB
AC_LNLVL_R 33
AC_LNLVL_L 33
MUTE_POP#
INTSPKR+_Q
INTSPKL+_Q
Q6144 SI1902DL
Q6145 SI1902DL
D1 G2 S2 S1 G1 D2
INTSPKR+
INTSPKL+
Can be substituted by UM6K1N or SI1902DL
+12V
R6623 100KOhm
R6624 100KOhm
D6013 1SS355
R6625 1MOhm
MUTE_POP#
Q6143A UM6K1N
Q6143B4 UM6K1N
30 MUTE_POP_AZGPIO#
25,30,44 ACZ_RST#_AUD
27 MUTE_POP_ICHGPIO#
R6626 0Ohm (no_stuff)
R6628 0Ohm (no_stuff)
R6914 0Ohm
R6627 240KOhm
C6335 10uF/10V
GND
Substitute by a 1uF/25V(0805) 11-032110520
<Variant Name>
Title : AUDIO_AMP & INT SPK
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 32 of 64

JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

ASUSTeK COMPUTER INC

Title : SPDIF JACK

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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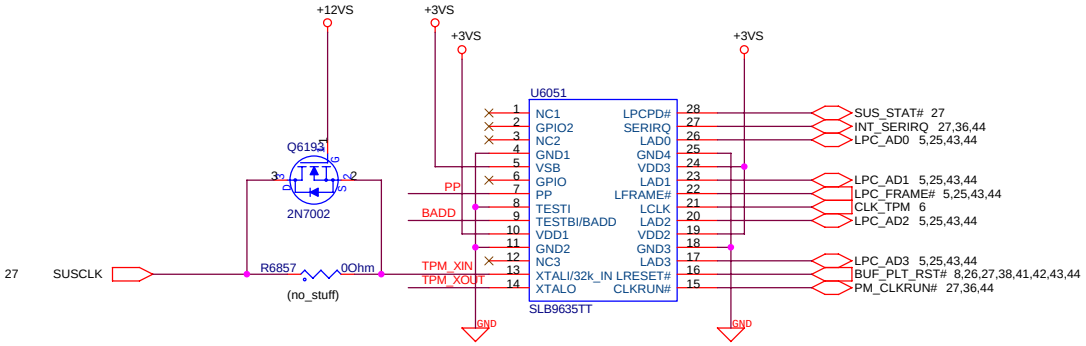
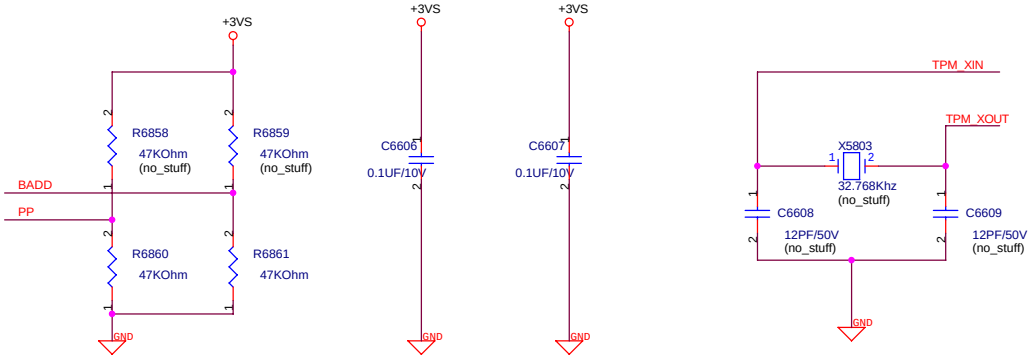
TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.





<Variant Name>

ASUSTeK COMPUTER INC

Title : TPM 1.2

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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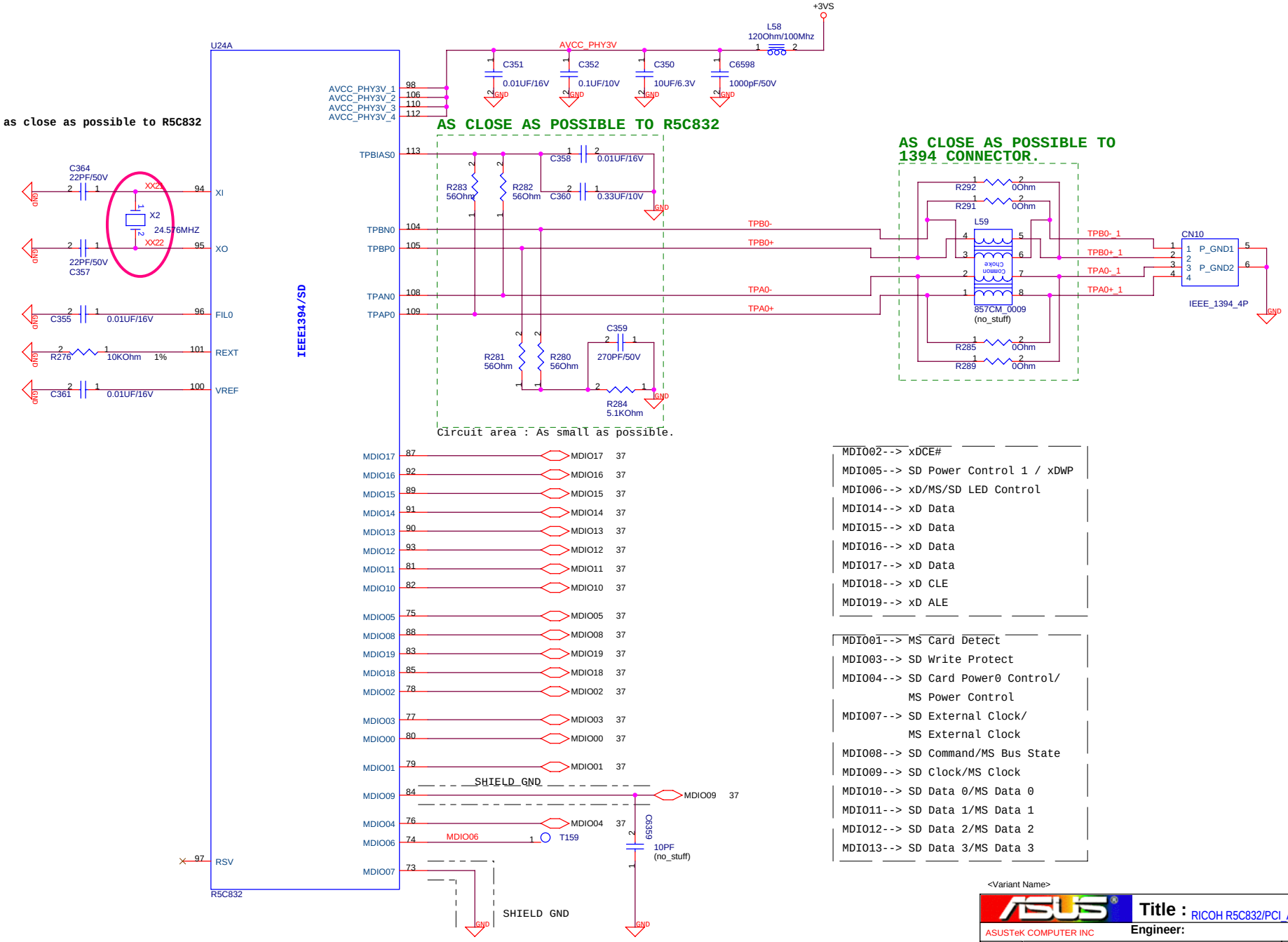
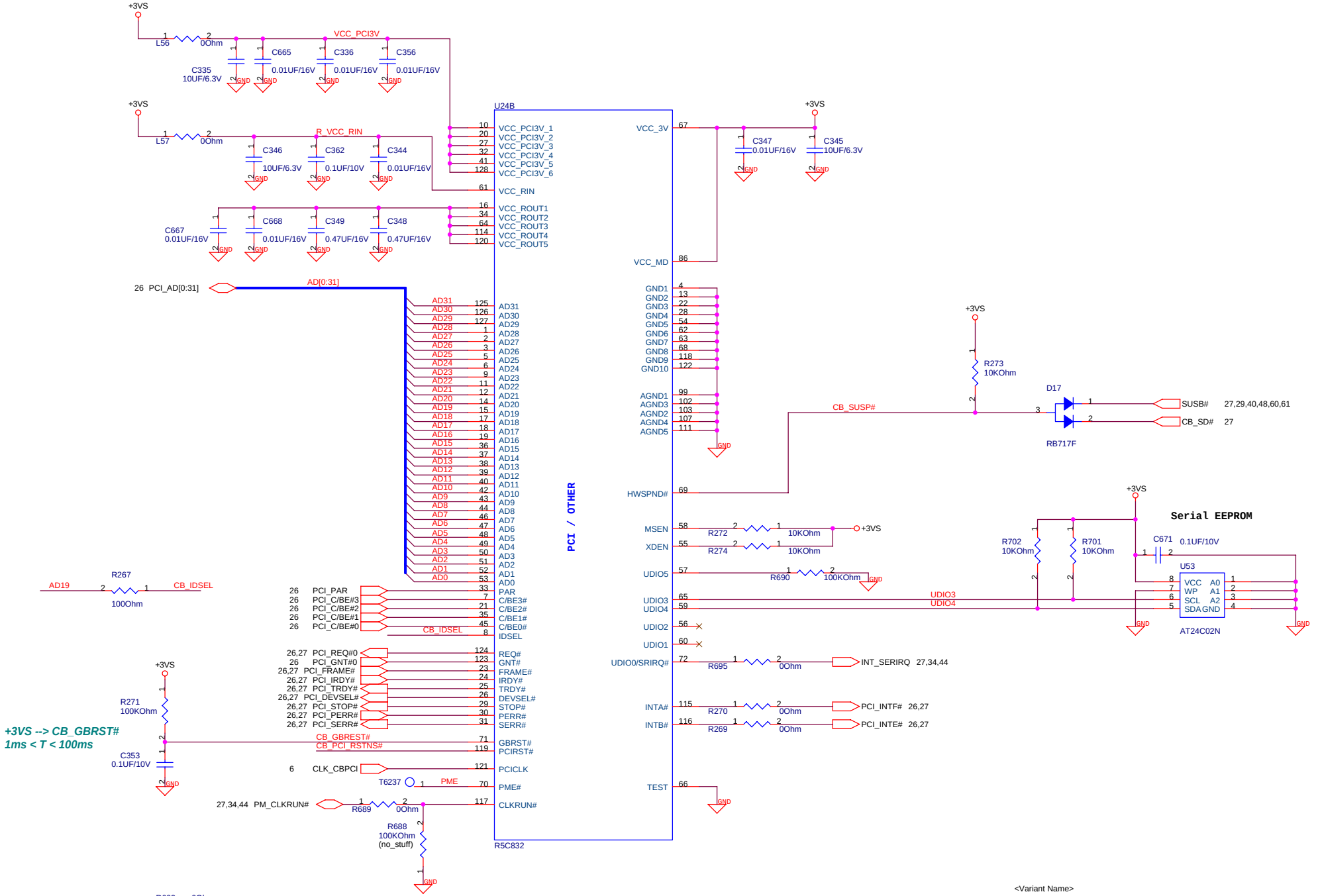

as close as possible to R5C832
U24A
IEEE1394/SD
R5C832
C364
22PF/50V
X2
24.576MHZ
22PF/50V
C357
C355
0.01UF/16V
R276
10KOhm
1%
C361
0.01UF/16V
XI
XO
FIL0
REXT
VREF
RSV
+3VS
L58
120Ohm/100Mhz
AVCC_PHY3V
C351
0.01UF/16V
C352
0.1UF/10V
C350
10UF/6.3V
C6598
1000pF/50V
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
AS CLOSE AS POSSIBLE TO R5C832
TPBIAS0
C358
0.01UF/16V
R283
56Ohm
R282
56Ohm
C360
0.33UF/10V
TPBN0
TPBP0
TPAN0
TPAP0
TPB0-
TPB0+
TPA0-
TPA0+
R281
56Ohm
R280
56Ohm
C359
270PF/50V
R284
5.1KOhm
Circuit area : As small as possible.
AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.
R292
0Ohm
R291
0Ohm
L59
Common Choke
857CM_0009
(no_stuff)
R285
0Ohm
R289
0Ohm
TPB0-_1
TPB0+_1
TPA0-_1
TPA0+_1
CN10
P_GND1
P_GND2
IEEE_1394_4P
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
SHIELD GND
T159
C6359
10PF
(no_stuff)
SHIELD GND
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
<Variant Name>
Title : RICOH R5C832/PCI_A
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7 J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 35 of 64



<Variant Name>

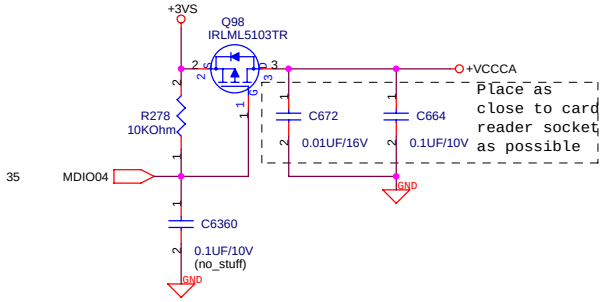
ASUSTeK COMPUTER INC

Title : RICOH R5C832/PCI_B

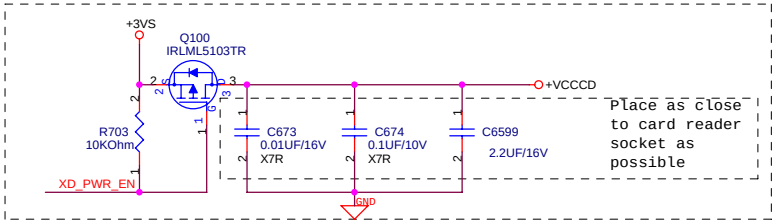
Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

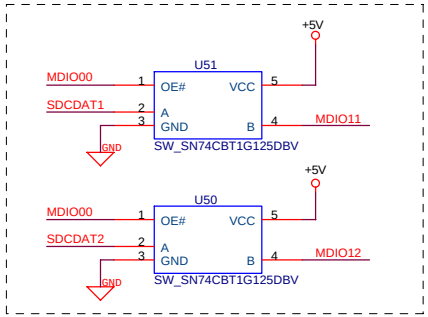
Date: Thursday, December 22, 2005 Sheet 36 of 64



To correct the problem when MS Duo adaptor is in use.

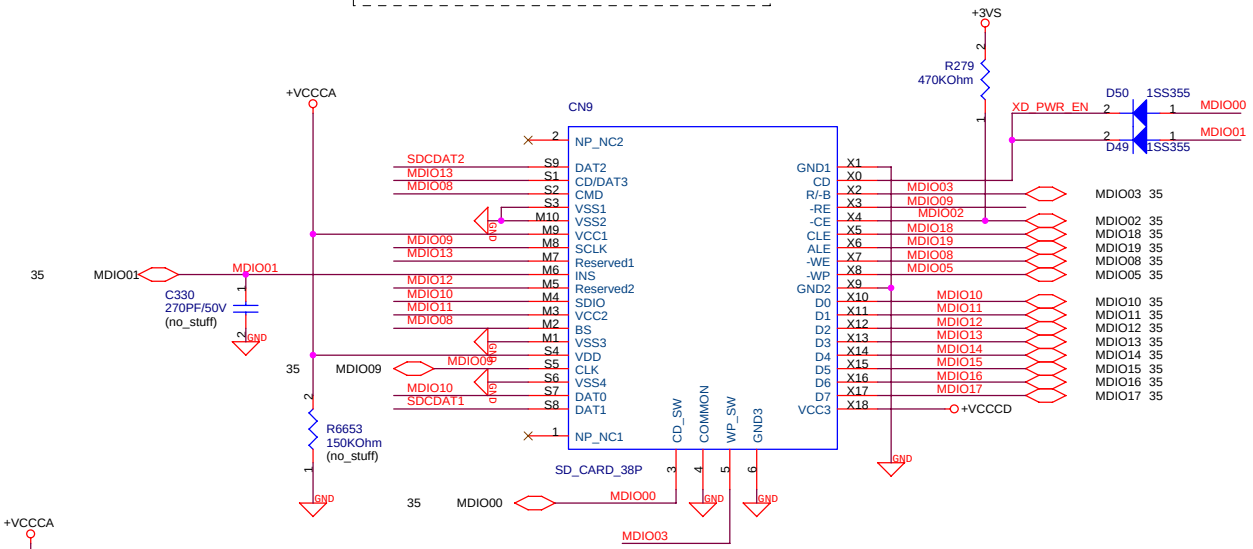


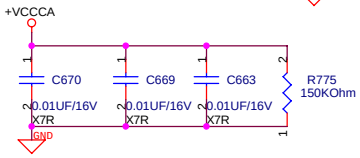
SD/MMC/MS/MS-PRO Card Reader Socket



MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

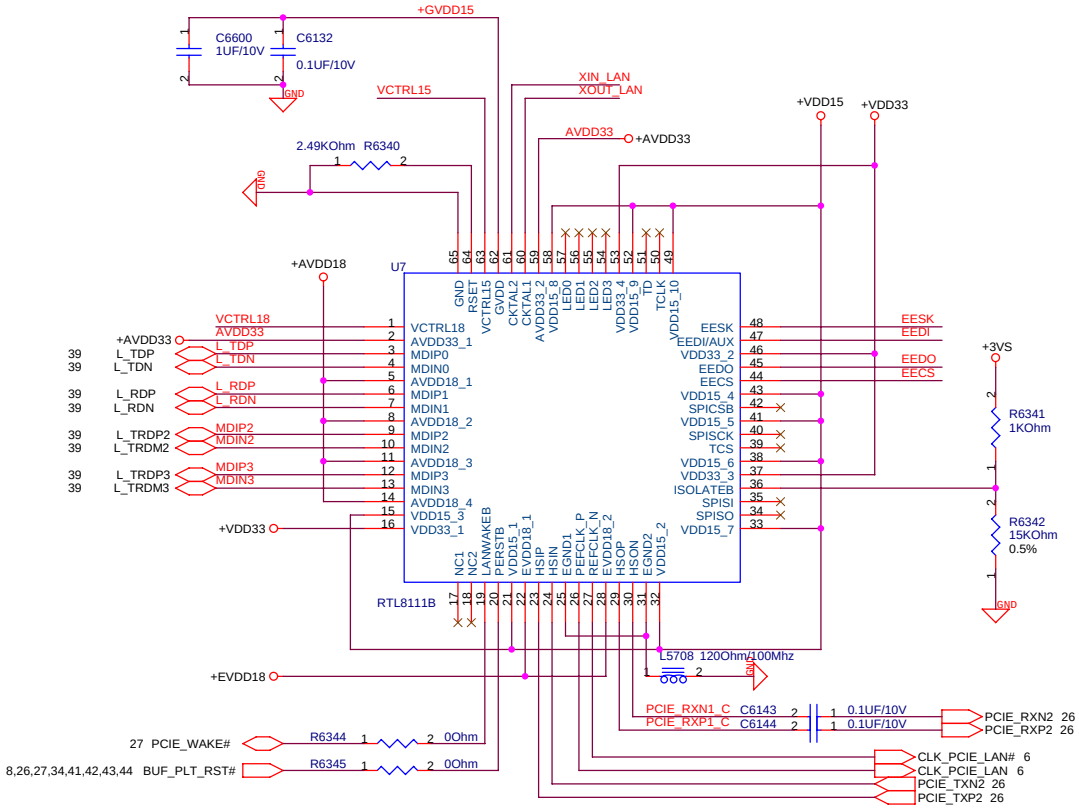


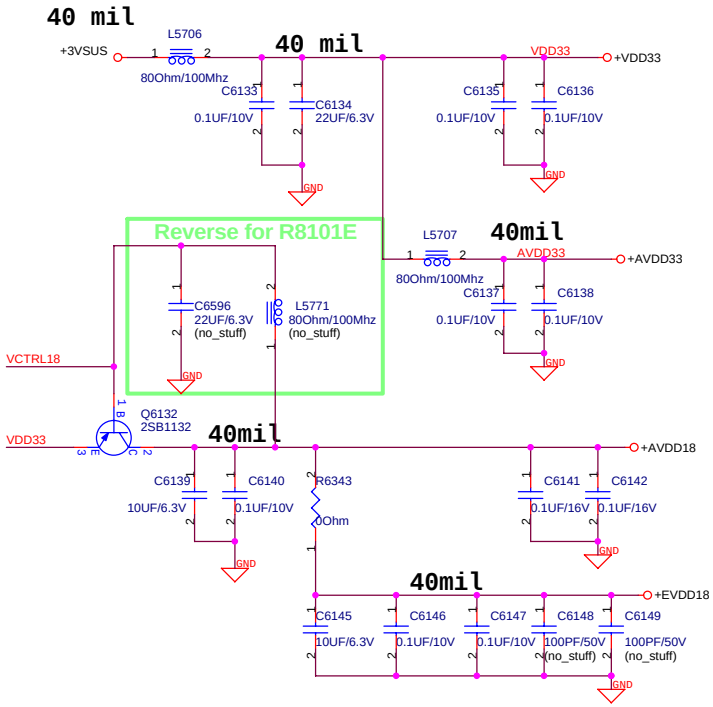


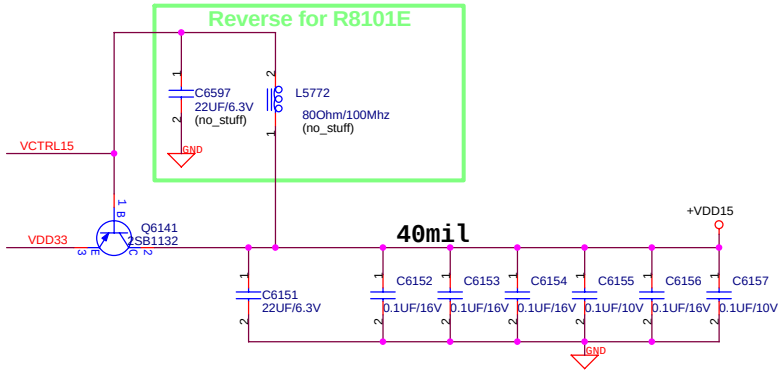
<Variant Name>

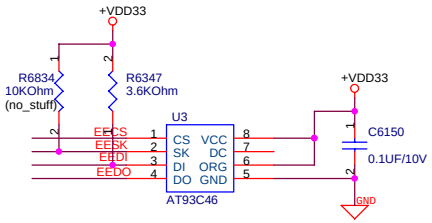
ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 37 of 64	

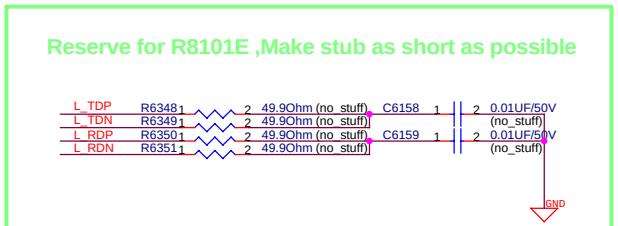
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

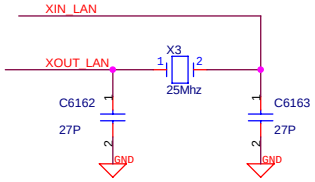


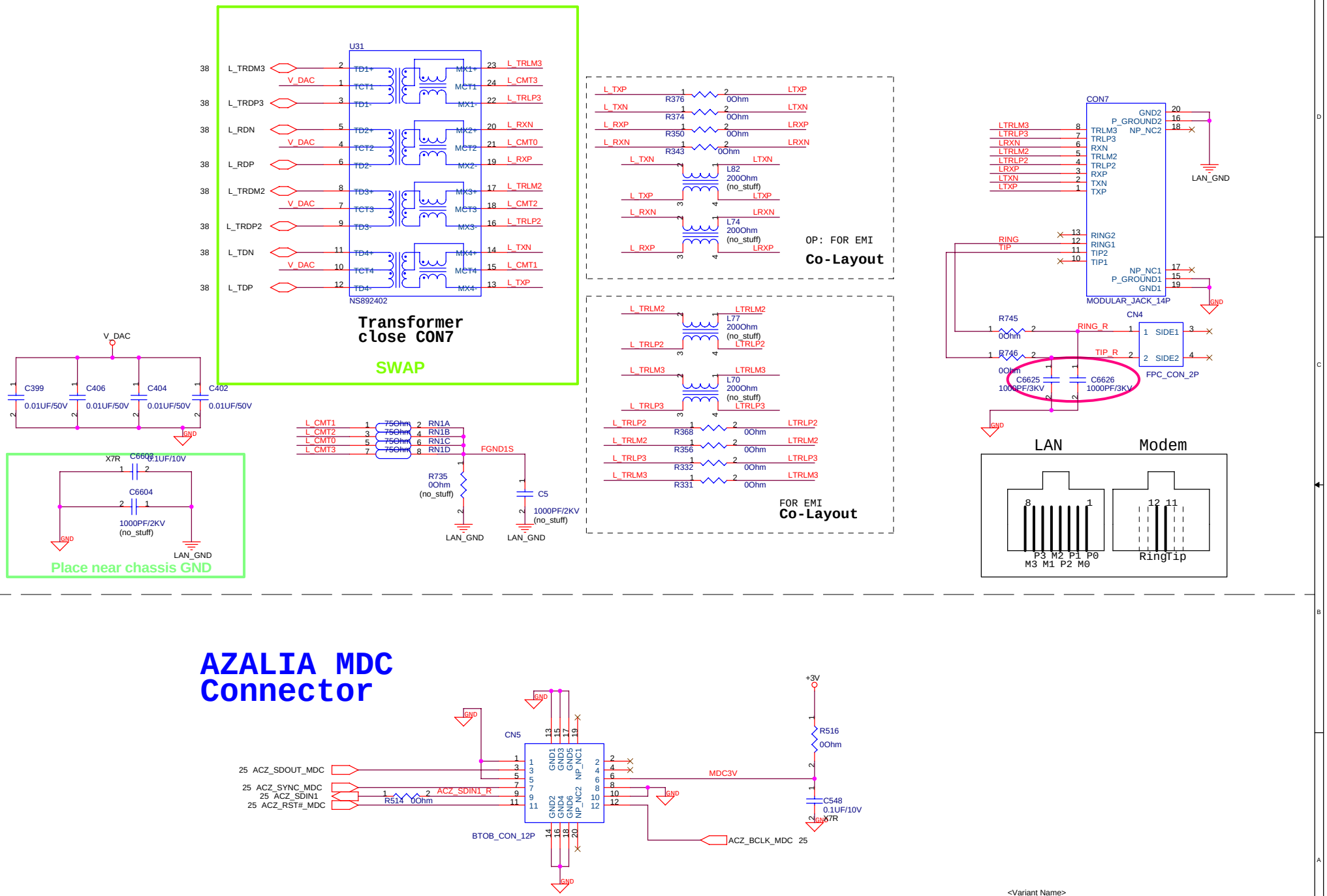












AZALIA MDC Connector

<Variant Name>

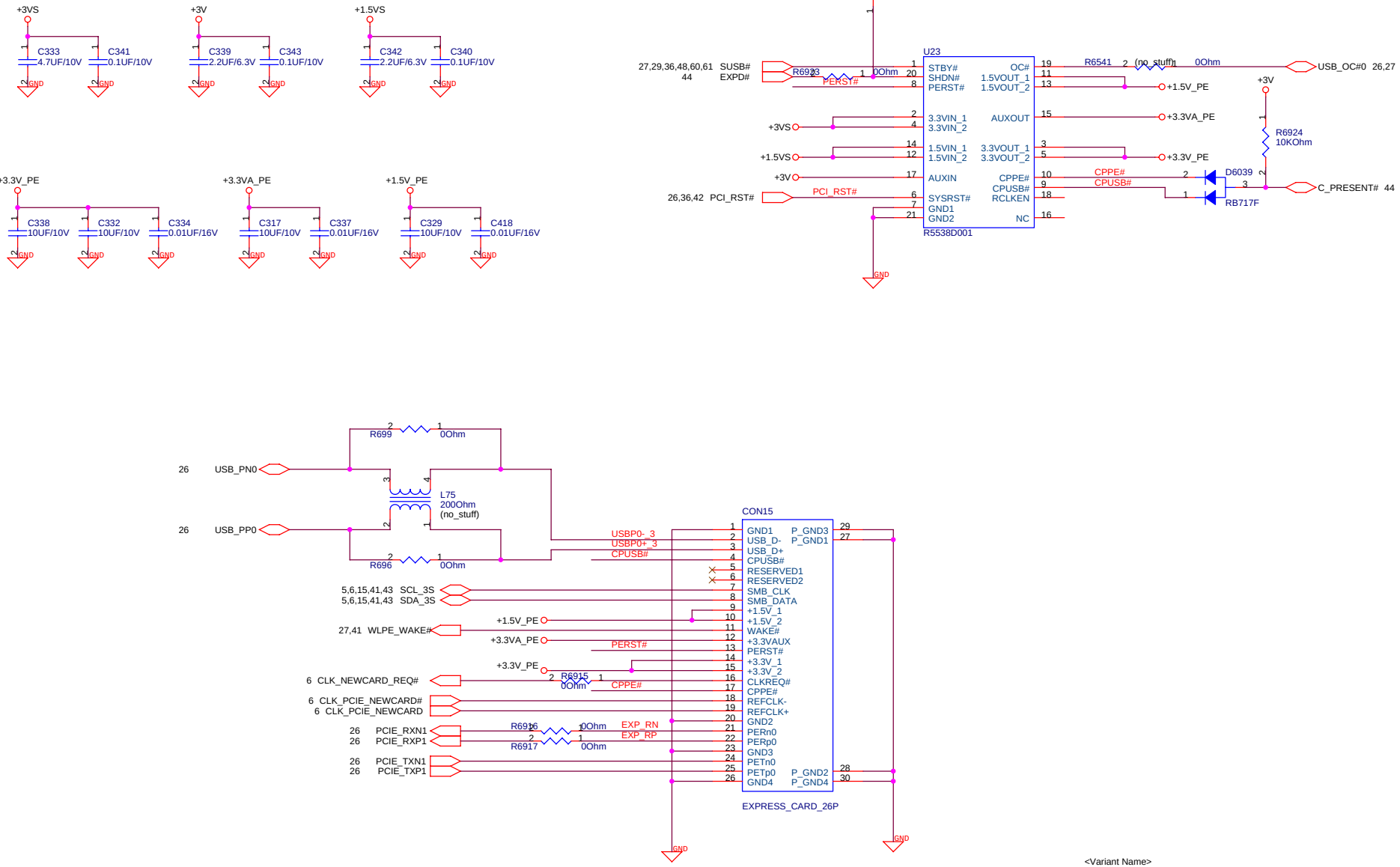
ASUSTeK COMPUTER INC

Title : RJ11+45 , MDC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 39 of 64



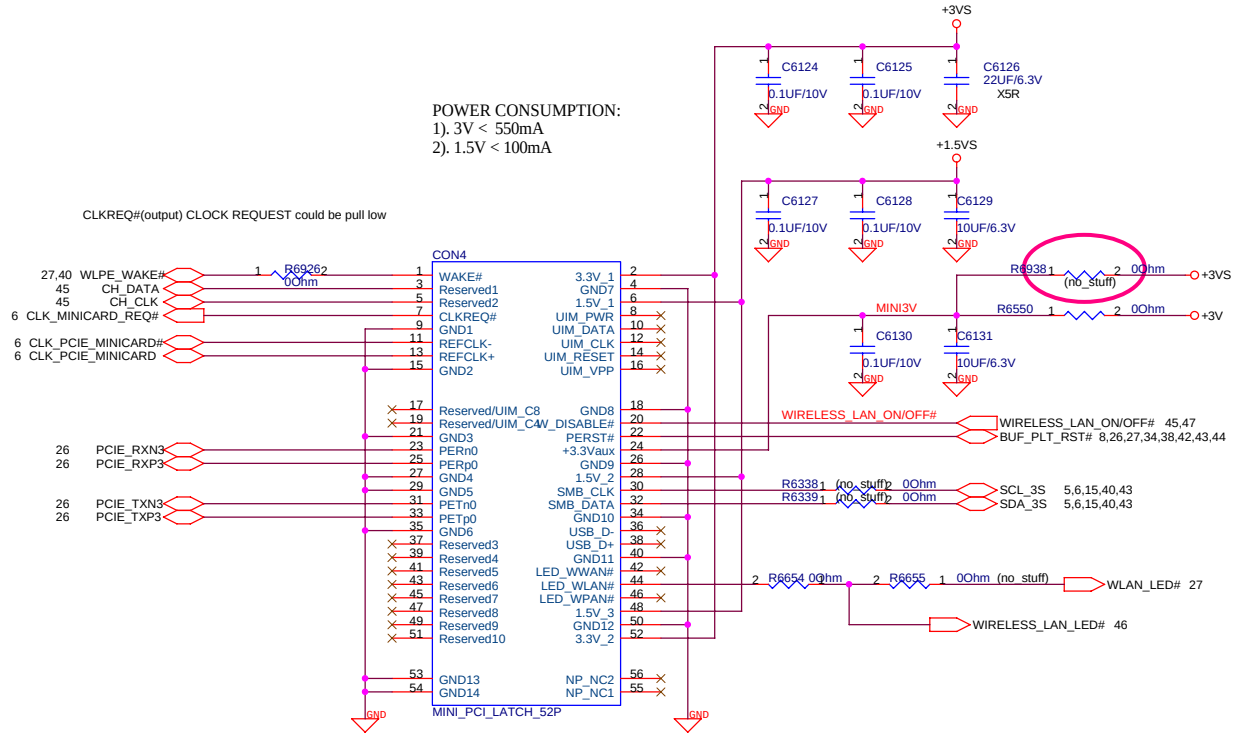
<Variant Name>

Title : Express Card

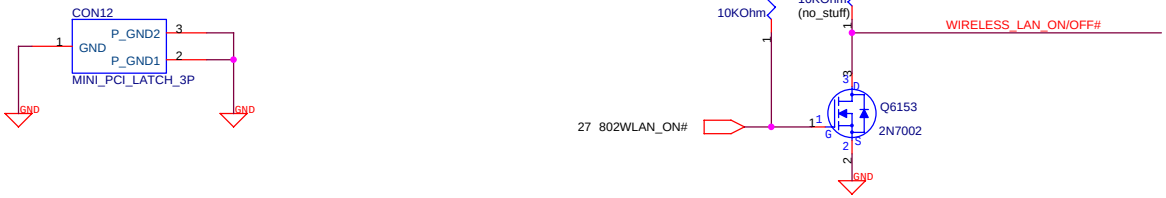
ASUSTeK COMPUTER INC **Engineer:**

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 40 of 64

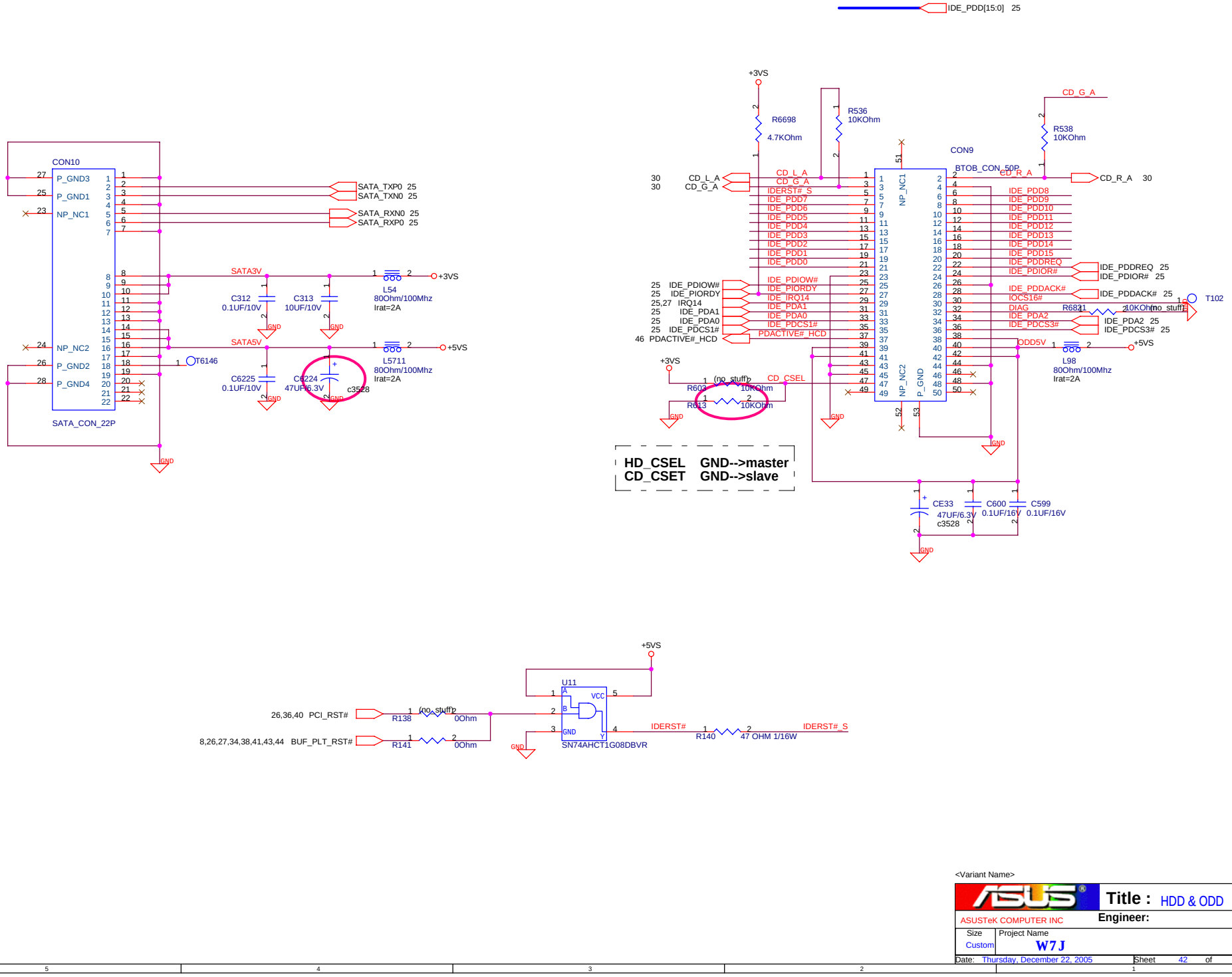


Mini Card Latch



<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD (802.11)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 41 of 64	



<Variant Name>

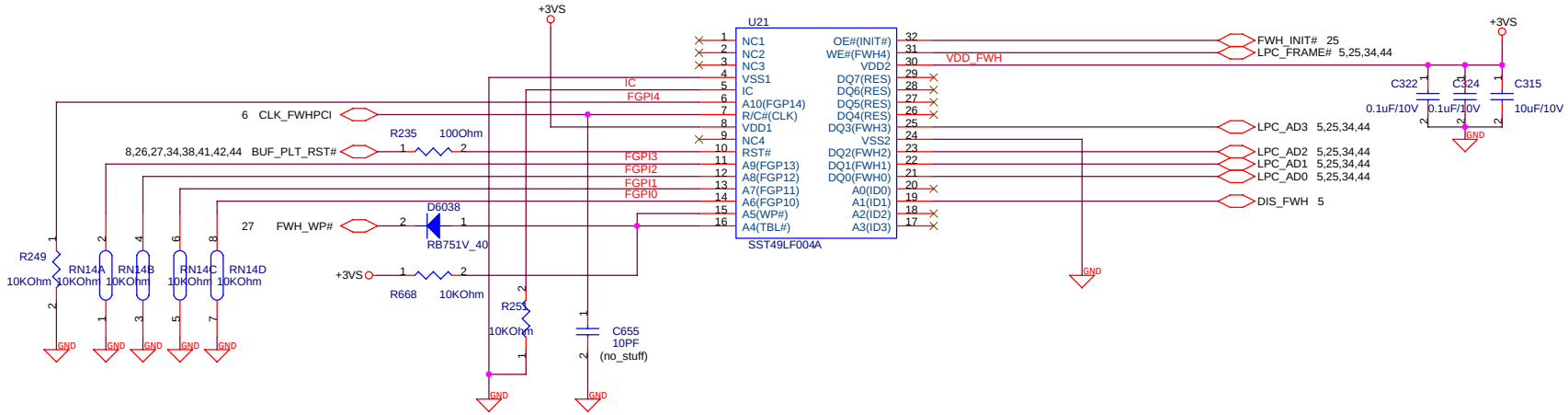
ASUSTeK COMPUTER INC

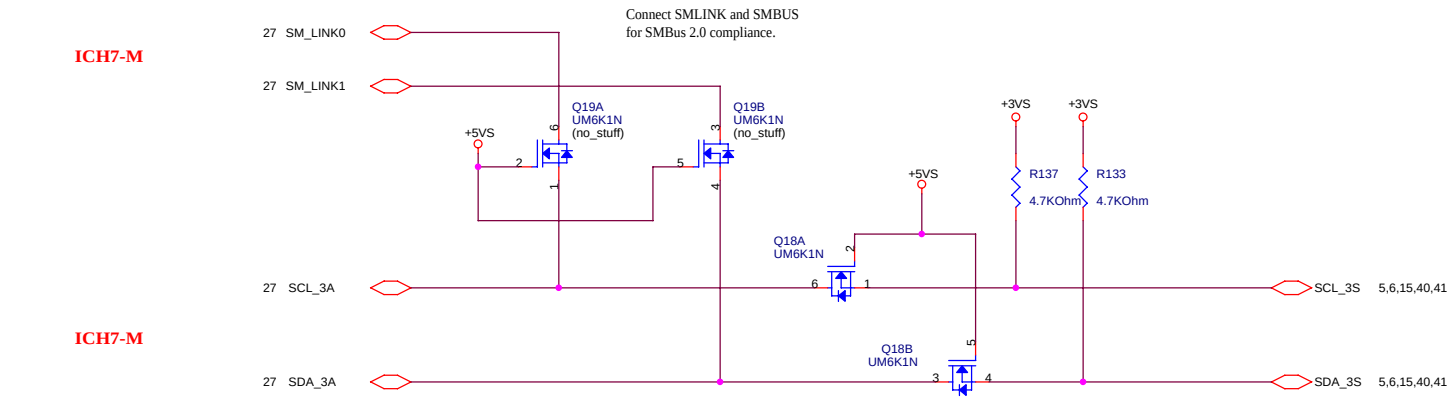
Title : HDD & ODD

Engineer:

Size	Project Name	Rev
Custom	W7 J	1.2

Date: Thursday, December 22, 2005 Sheet 42 of 64





ICH7-M

ICH7-M

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
EXPRESS CARD
MINI-CARD

<Variant Name>

ASUSTeK COMPUTER INC	Title : FWH , SM BUS	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 43 of 64	

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

KID1	KID0	Matrix
0	0	US
1	1	UK
0	1	JP

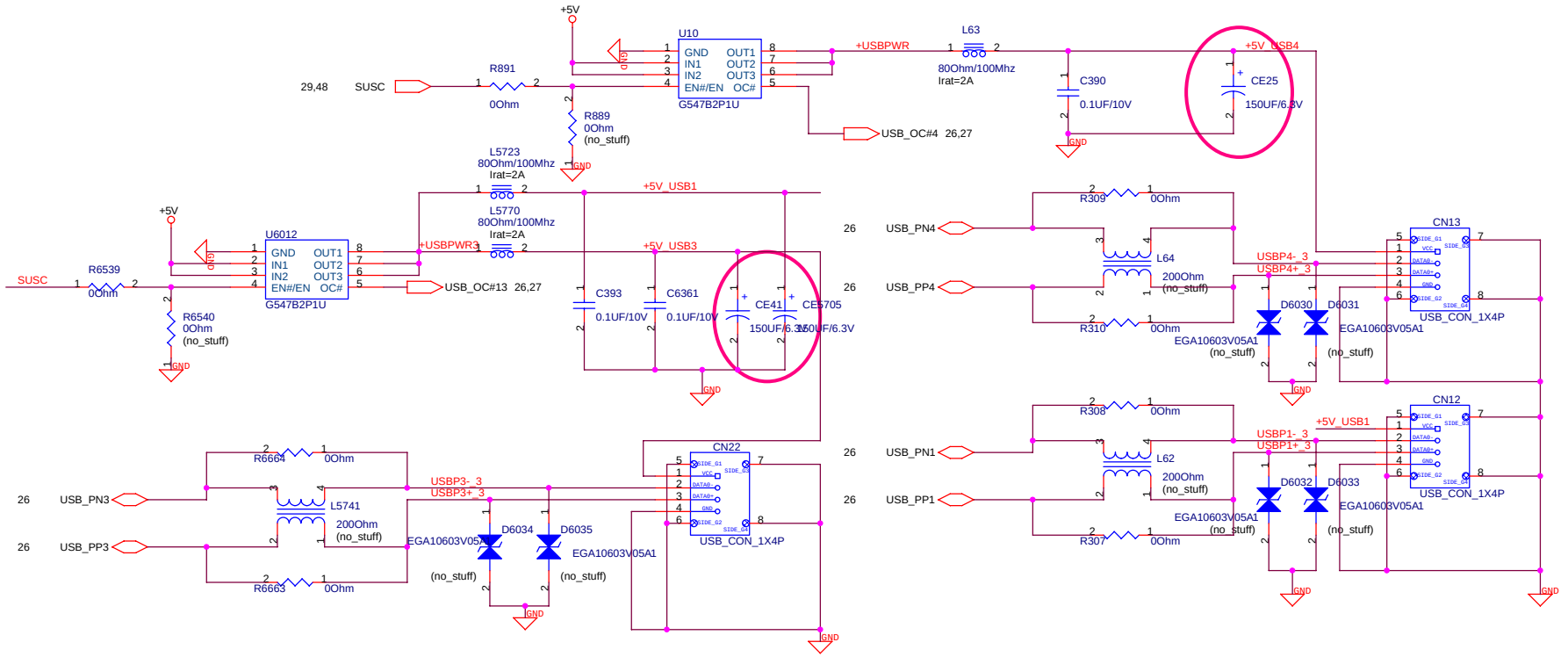
U46

M38857

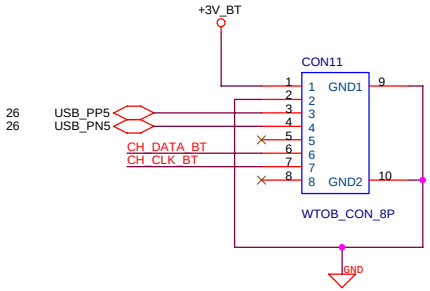
80mA

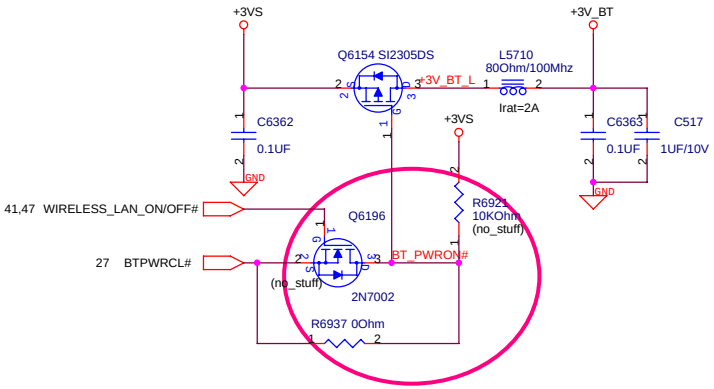
<Variant Name>

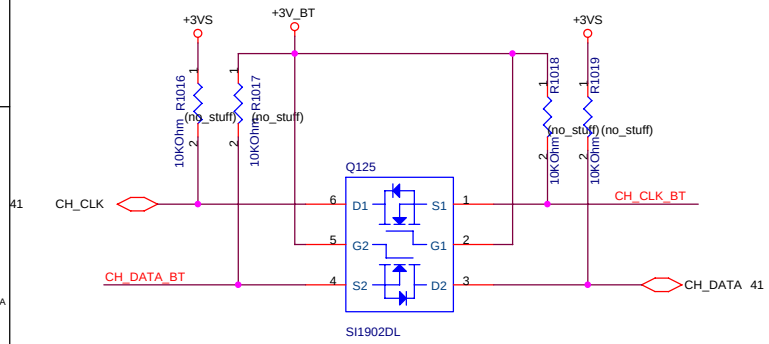
ASUSTeK COMPUTER INC	Title : KBC M38857	
	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 44 of 64	



Bluetooth Module Connector







<Variant Name>

ASUSTeK COMPUTER INC

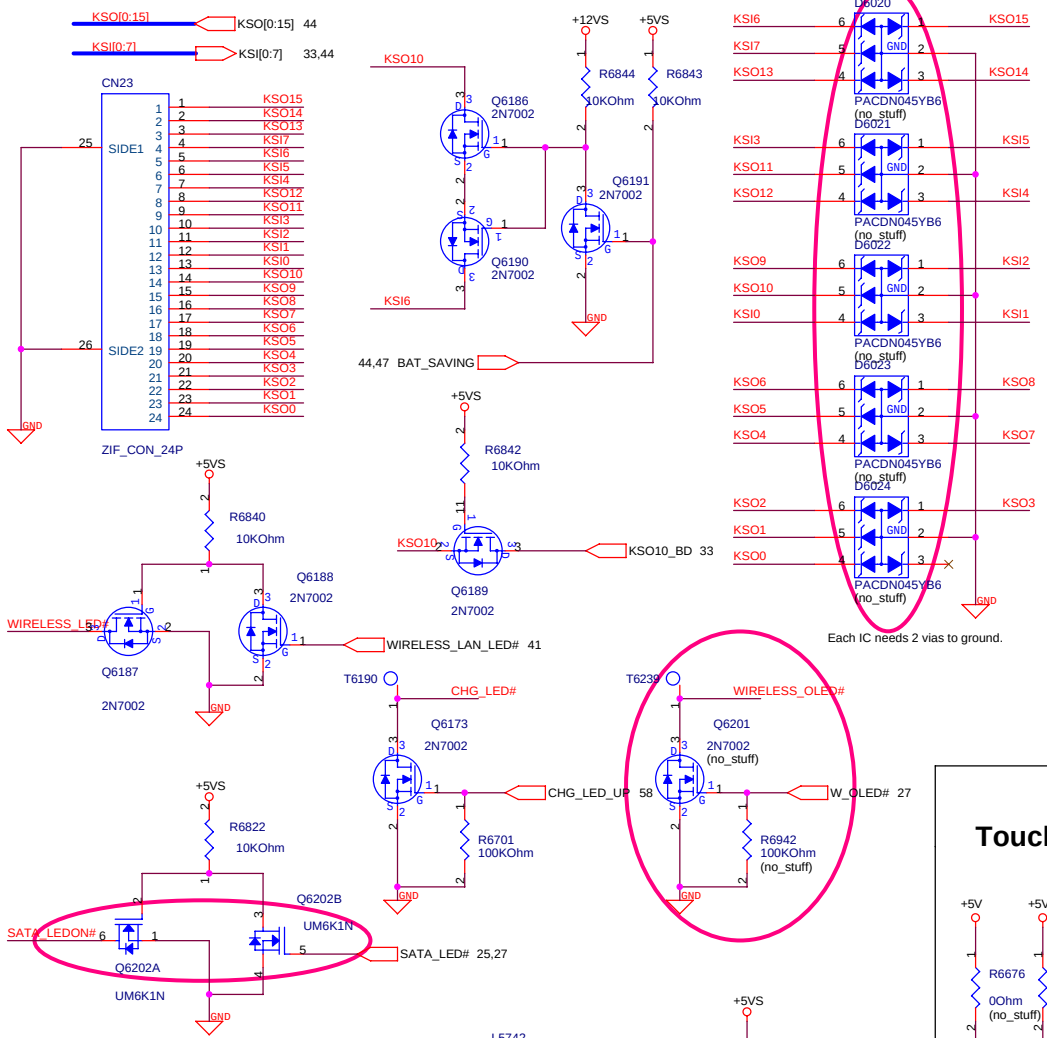
Title : USB * 3ports & BT

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 45 of 64

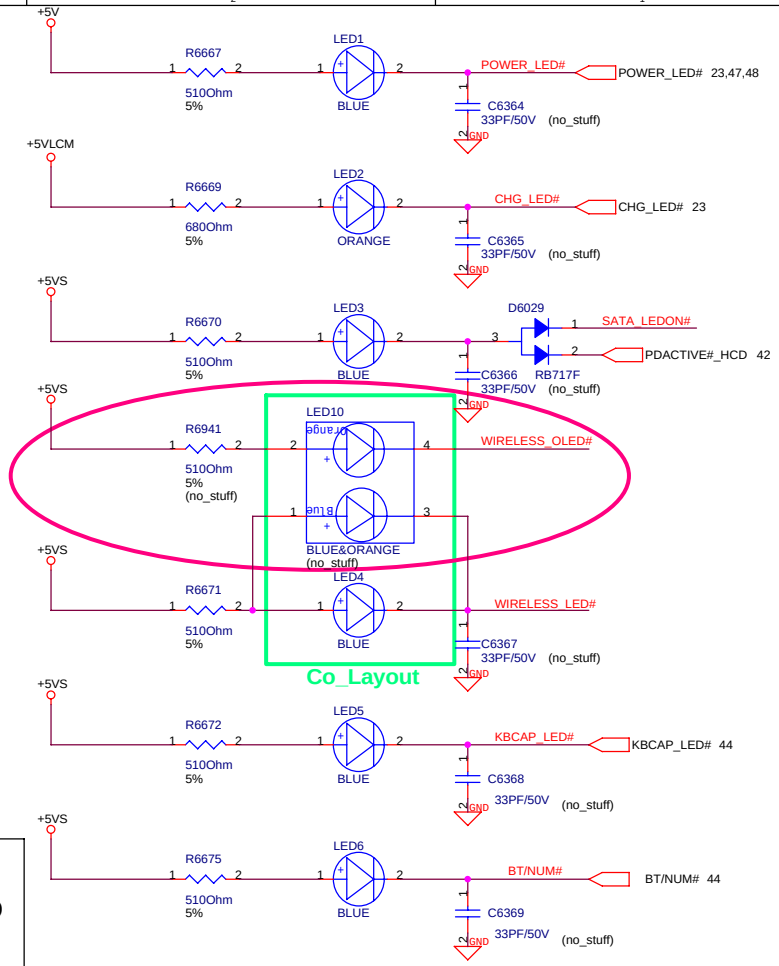
Internal Keyboard Connector



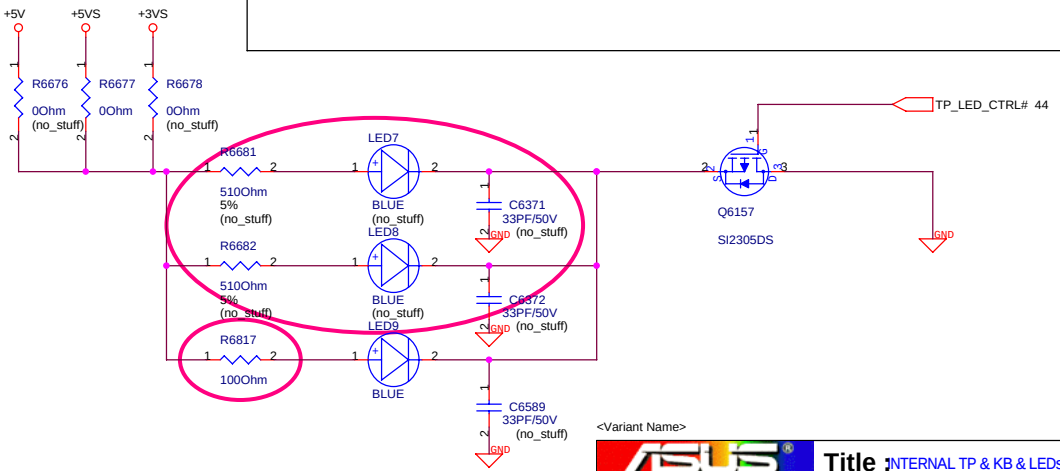
EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.

Each IC needs 2 vias to ground.

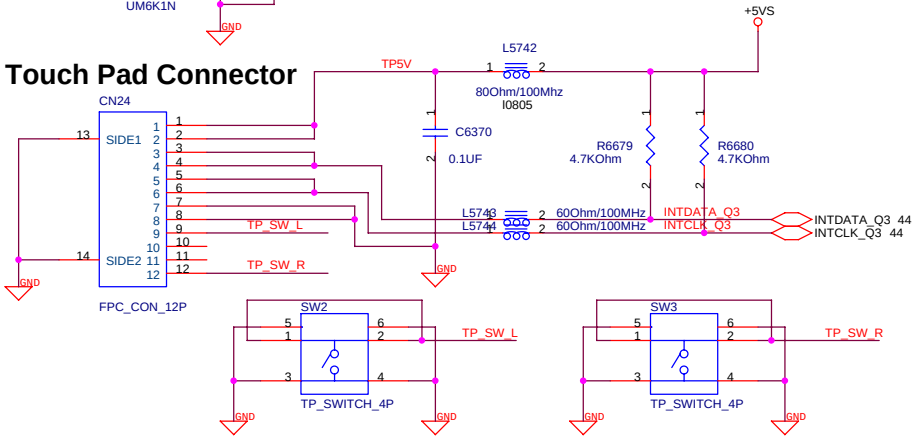
LEDs



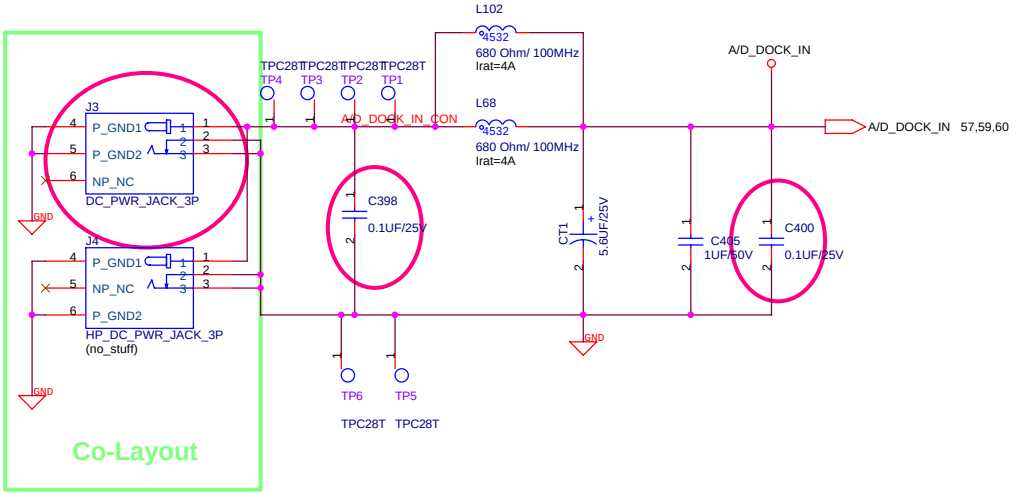
Touch Pad LED



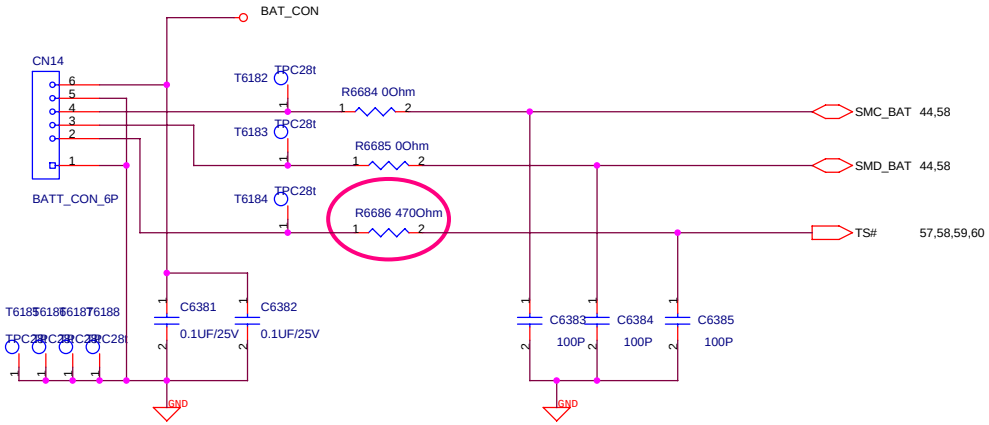
Touch Pad Connector



DC-IN

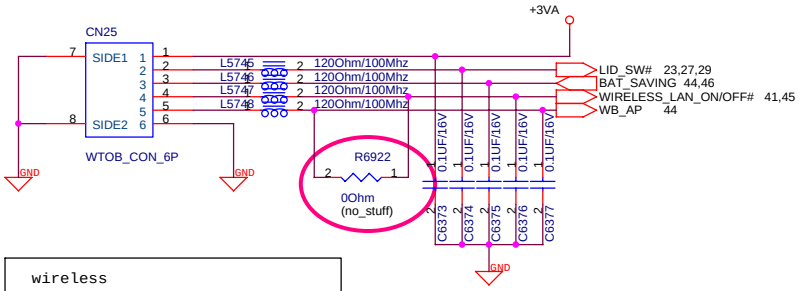


Battery Connector



EXT BOARD

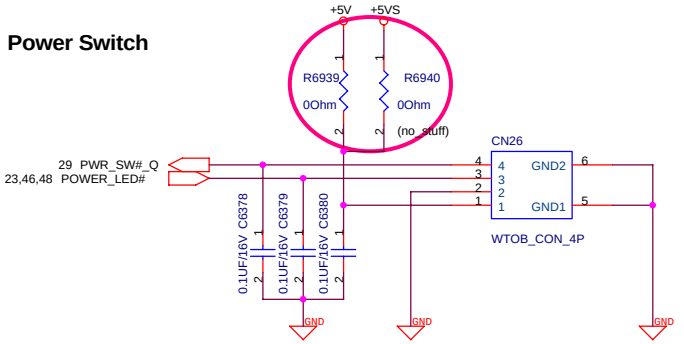
LID_SW_BD CN



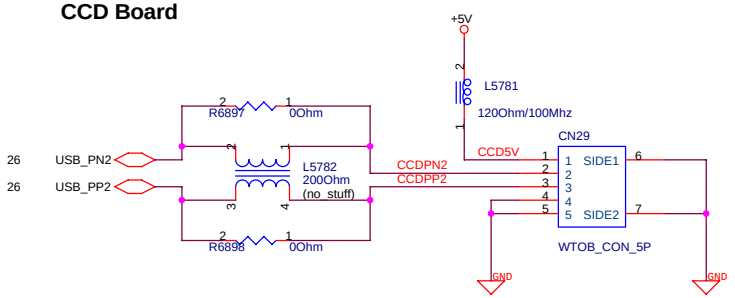

```
wireless
-----------------------------
right on ---> active high
left off ---> active low

WB_AP
-----------------------------
right off ---> active high
left  on  ---> active low
```

Power Switch



CCD Board



<Variant Name>

ASUSTeK COMPUTER INC

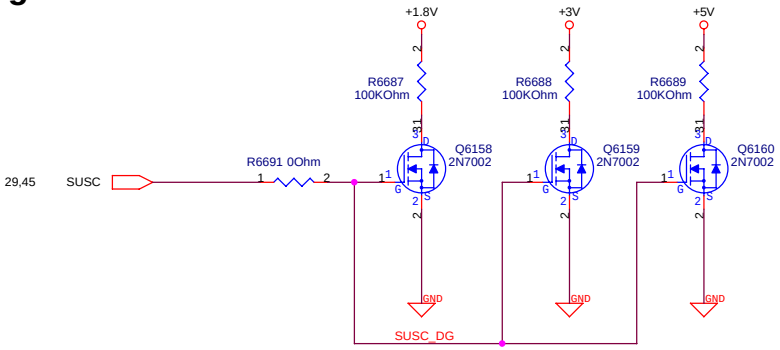
Title : DCIN,BATT CON,EXT BOARD

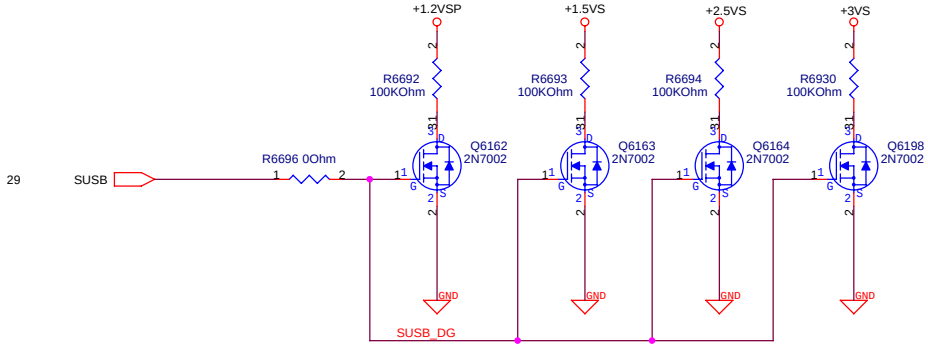
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 47 of 64

Discharge



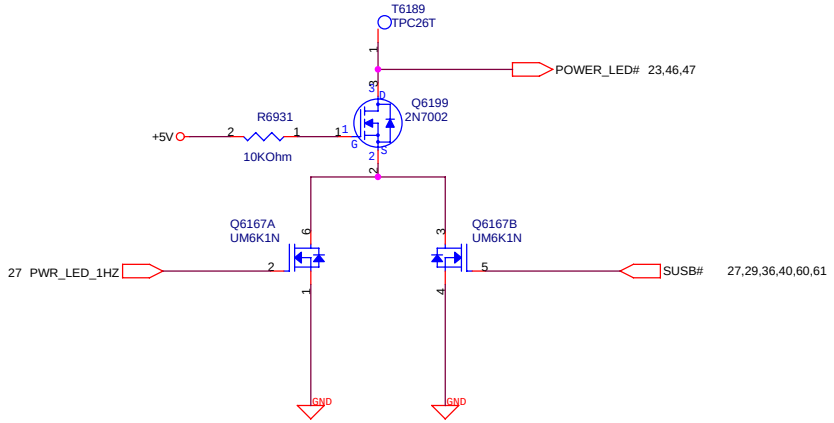


Poewr List

+3VA	+3VA	25,29,47,54,63
+3VSUS	+3VSUS	26,27,28,29,32,38,41,51
+5VA	+5VA	51,54,60
+5VSUS	+5VSUS	28,51,60
+3V	+3V	26,29,39,40,41,44,54,61
+5V	+5V	16,30,32,37,44,45,46,47,59,61
+12V	+12V	27,32,33,61
+3VS	+3VS	5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,50,52,60,61
+5VS	+5VS	5,24,28,29,30,32,33,42,43,44,46,47,50,61
+12VS	+12VS	5,24,34,46,61
+VCORE	+VCORE	3,4,5,44,50
+VCCP	+VCCP	2,3,4,6,7,8,10,11,12,25,28,52
+1.2VSP	+1.2VSP	17,18,56
+2.5VS	+2.5VS	10,20,21,54
+1.8VS	+1.8VS	20,61
+0.9VS	+0.9VS	16,53
+1.5VS	+1.5VS	3,8,10,11,26,28,40,41,52
+VCC_RTC	+VCC_RTC	25,28
+1.8V	+1.8V	8,12,13,14,15,16,53
VTT_REF	VTT_REF	8,13,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	47,57,59,60
+VGA_VCORE	+VGA_VCORE	17,55

GND

Power LED On



<Variant Name>

Discharge,Power Rail & Power LED On

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 48 of 64

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARD READER	AD19	0	E
1394	AD19	0	F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor	0101110x (2E)
PIC	1001001x (92)
Express Card	TBD
Mini Card	TBD

ICH7-M GPIO	W7J
GPIO 0	PM_BMBUSY#
GPIO 1	PCI_REQ#5
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 6	BACK_OFF#
GPIO 7	MUTE_POP_ICHGPIO#
GPIO 8	EXTSMI#
GPIO 9	W_OLED#
GPIO 10	(PWRLMT#)
GPIO 11	SMBALERT#
GPIO 12	KBC_SCI#
GPIO 13	PWR_LED_1HZ
GPIO 14	WLAN_ON#
GPIO 15	802_LED_EN#
GPIO 16	DPRSLPVR
GPIO 17	GNT5#
GPIO 18	STP_PCI#
GPIO 19	Memoryclk
GPIO 20	STP_CPU#
GPIO 21	
GPIO 22	PCI_REQ#4
GPIO 23	LPC_DRQ#1
GPIO 24	SW_RST#
GPIO 25	CB_SD#
GPIO 26	MEM ID0
GPIO 27	MEM ID1
GPIO 28	MEM ID2
GPIO 29	USB_OC#5
GPIO 30	USB_OC#6
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 33	BT_ON#
GPIO 34	FWH_WP#
GPIO 35	SATACLKREQ#
GPIO 36	BT_LED_EN#
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 48	GNT4#
GPIO 49	CPUPWRGD

KBC GPIO	W7J
P23	
P22	BAT_LEARN
P21	
P20	KBCRSM
P42	WATCHDOG
P43	
P44	xKBRC
P45	GA20
P46	KBDSCI
P47	CLKRUN#
P50	BAT_LLOW#
P51	TP_LED_CTRL#
P52	
P53	EXPD#
P54	LID_EC#
P55	BAT_IN#
P56	CPU_FAN_PWM
P57	ADJ_BL
P67	WB_AP
P66	M_MODE#
P65	
P64	ACIN#
P63	EOC#_LED
P62	C_PRESENT#
P61	ACZ_RST#_AUD
P60	
P75	KBDCLK_5S
P74	MOUSECLK_5S
P73	INTCLK_Q3
P72	KBDDATA_5S
P71	MOUSEDATA_5S
P70	INTDATA_Q3
P77	SMC_KBC
P76	SMD_KBC
P27	SCROLL_LED#
P26	NUM_LED#
P25	CAP_LED#
P24	SET_RSTNS#
P40	EXT_SMI#
P41	

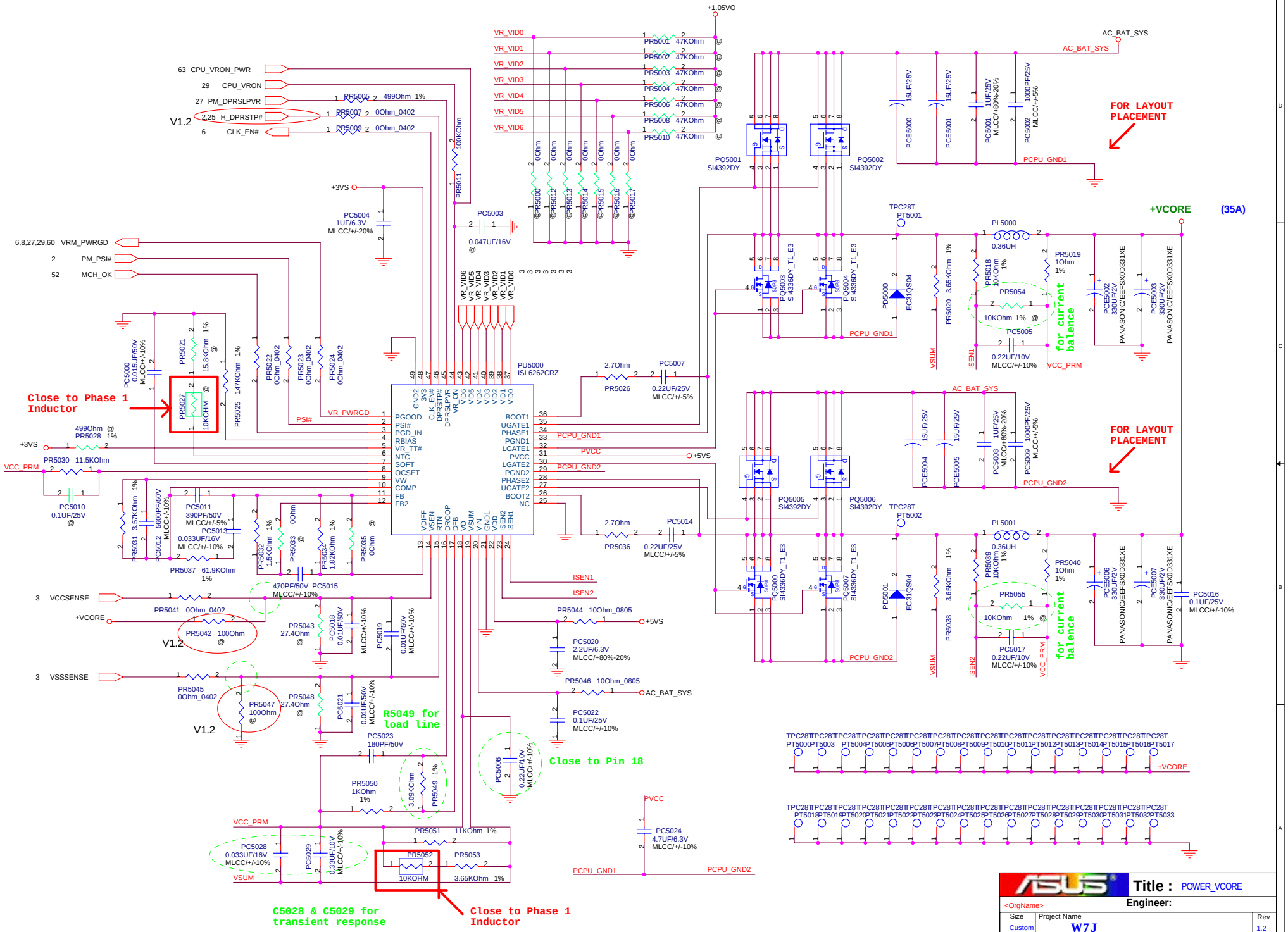
<Variant Name>

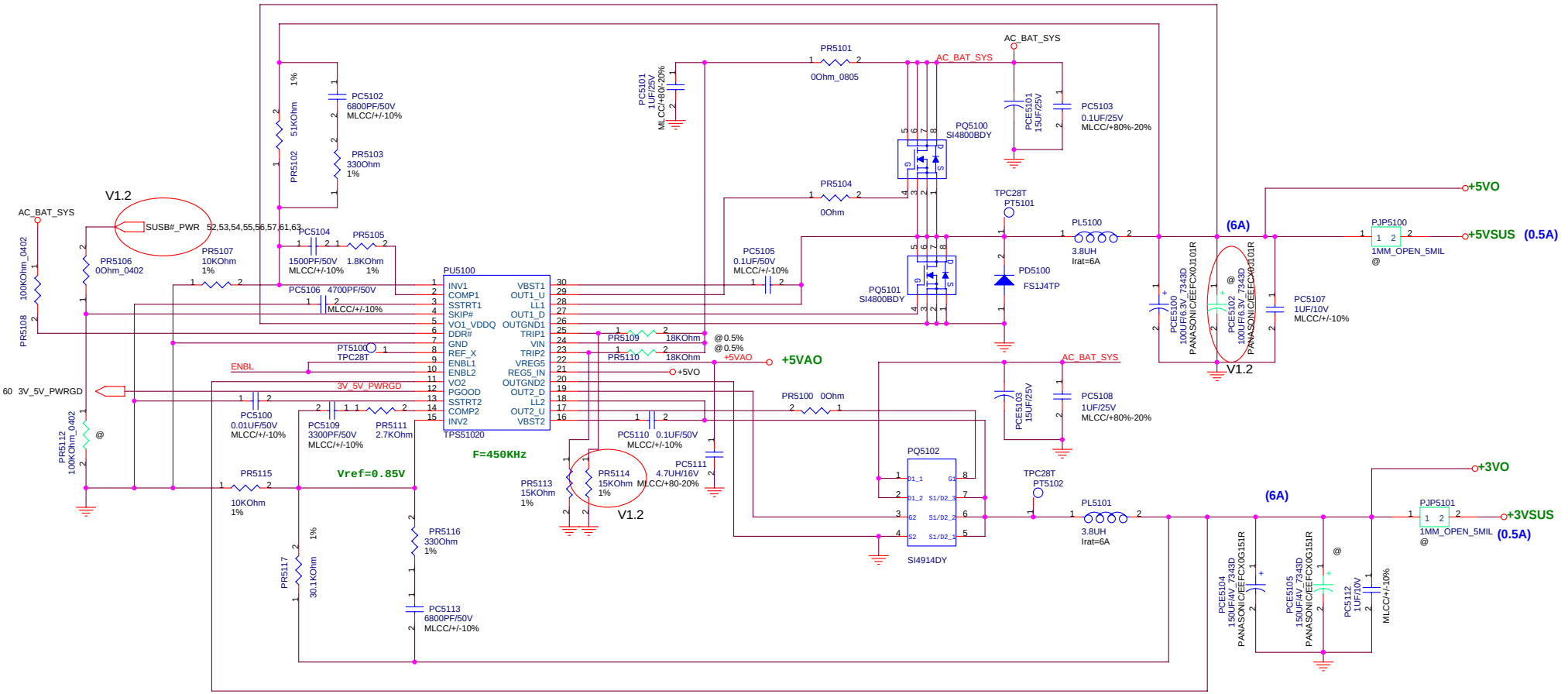
Title : System Resource

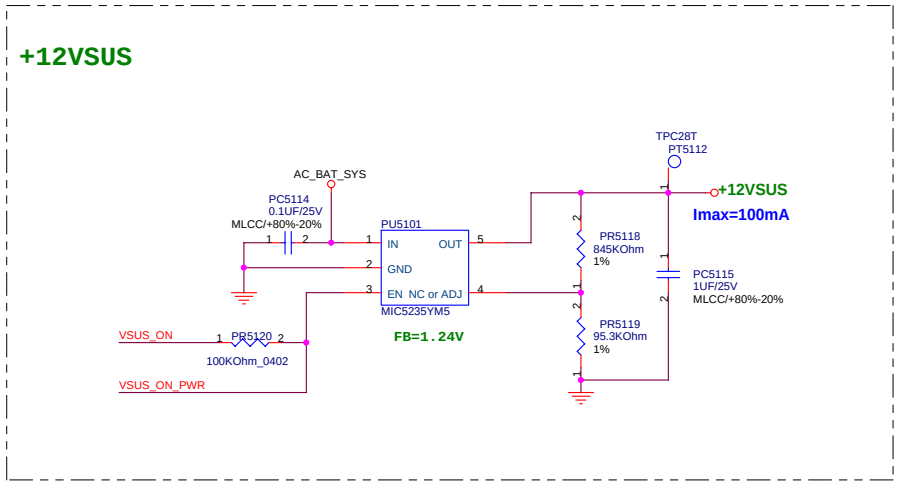
ASUSTeK COMPUTER INC Engineer:

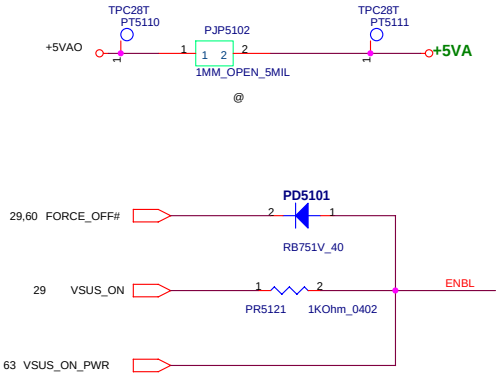
Size	Project Name	Rev
Custom	W7J	1.2

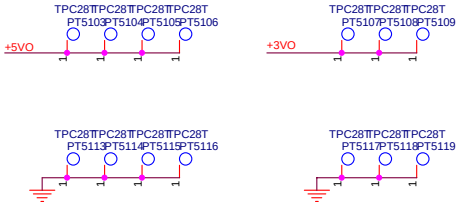
Date: Thursday, December 22, 2005 Sheet 49 of 64


+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5006 47KOhm
PR5008 47KOhm
PR5010 47KOhm
PR5000 0Ohm
PR5012 0Ohm
PR5013 0Ohm
PR5014 0Ohm
PR5015 0Ohm
PR5016 0Ohm
PR5017 0Ohm
63 CPU_VRON_PWR
29 CPU_VRON
27 PM_DPRSLPVR
2,25 H_DPRSTP#
6 CLK_EN#
V1.2
PR5005 499Ohm 1%
PR5007 0Ohm_0402
PR5009 0Ohm_0402
PR5011 100KOhm
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5003 0.047UF/16V @
6,8,27,29,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
PC5000 0.015UF/50V MLCC/+/-10%
PR5021
PR5027 10KOHM @
15.8KOhm 1% @
PR5025 147KOhm 1%
PR5022 0Ohm_0402
PR5023 0Ohm_0402
PR5024 0Ohm_0402
Close to Phase 1 Inductor
PU5000 ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VID1
VDD
ISEN2
ISEN1
VR_PWRGD
PSI#
PCPU_GND1
PCPU_GND2
PVCC
+5VS
499Ohm @ PR5028 1%
VCC_PRM
PR5030 11.5KOhm
PC5010 0.1UF/25V @
PR5031 3.57KOhm 1%
PC5012 5600PF/50V MLCC/+/-10%
PC5011 390PF/50V MLCC/+/-5%
PC5013 0.033UF/16V MLCC/+/-10%
PR5037 61.9KOhm 1%
PR5032 1.5KOhm 1%
PR5033 0Ohm @
PR5034 1.82KOhm 1%
PR5035 0Ohm @
2.7Ohm PR5026
PC5007 0.22UF/25V MLCC/+/-5%
2.7Ohm PR5036
PC5014 0.22UF/25V MLCC/+/-5%
470PF/50V PC5015 MLCC/+/-10%
3 VCCSENSE
+VCORE
PR5041 0Ohm_0402
PR5042 100Ohm @
PR5043 27.4Ohm @
PC5018 0.01UF/50V MLCC/+/-10%
PC5019 0.01UF/50V MLCC/+/-10%
3 VSSENSE
PR5045 0Ohm_0402
PR5047 100Ohm @
PR5048 27.4Ohm @
PC5021 0.01UF/50V MLCC/+/-10%
R5049 for load line
PC5023 180PF/50V
PR5050 1KOhm 1%
PR5049 3.09KOhm 1%
PC5006 0.22UF/10V MLCC/+/-10%
Close to Pin 18
PR5044 10Ohm_0805
PC5020 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
PC5022 0.1UF/25V MLCC/+/-10%
PC5024 4.7UF/6.3V MLCC/+/-10%
VCC_PRM
PC5028 0.033UF/16V MLCC/+/-10%
PC5029 0.33UF/10V MLCC/+/-10%
VSUM
PR5051 11KOhm 1%
PR5052 10KOHM
PR5053 3.65KOhm 1%
C5028 & C5029 for transient response
Close to Phase 1 Inductor
AC_BAT_SYS
PQ5001 SI4392DY
PQ5002 SI4392DY
PCE5000 15UF/25V
PCE5001 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/25V MLCC/+/-5%
FOR LAYOUT PLACEMENT
PCPU_GND1
+VCORE (35A)
TPC28T PT5001
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PD5000 EC31QS04
PR5020 3.65KOhm 1%
PR5018 10KOhm 1%
PR5019 1Ohm 1%
PR5054 10KOhm 1% @
PC5005 0.22UF/10V MLCC/+/-10%
for current balence
PL5000 0.36UH
PCE5002 330UF/2V PANASONIC/EEFSX0D331XE
PCE5003 330UF/2V PANASONIC/EEFSX0D331XE
VSUM
ISEN1
VCC_PRM
PQ5005 SI4392DY
PQ5006 SI4392DY
PCE5004 15UF/25V
PCE5005 15UF/25V
PC5008 1UF/25V MLCC/+80%-20%
PC5009 1000PF/25V MLCC/+/-5%
PCPU_GND2
TPC28T PT5002
PQ5007 SI4336DY_T1_E3
PD5001 EC31QS04
PR5038 3.65KOhm 1%
PR5039 10KOhm 1%
PR5040 1Ohm 1%
PR5055 10KOhm 1% @
PC5017 0.22UF/10V MLCC/+/-10%
PL5001 0.36UH
PCE5006 330UF/2V PANASONIC/EEFSX0D331XE
PCE5007 330UF/2V PANASONIC/EEFSX0D331XE
PC5016 0.1UF/25V MLCC/+/-10%
TPC28T PT5000 PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Title : POWER_VCORE
<OrgName>
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 50 of 64

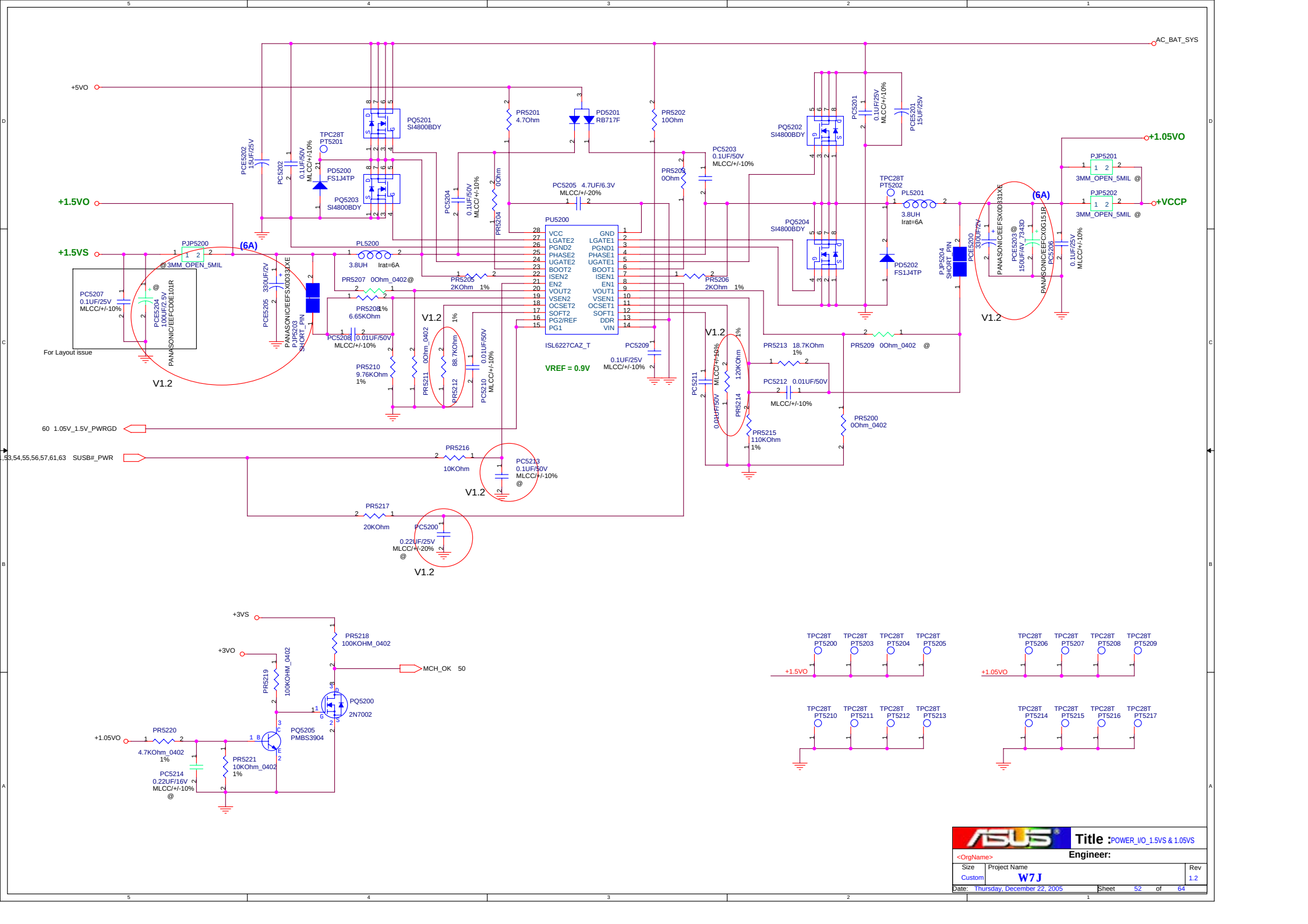




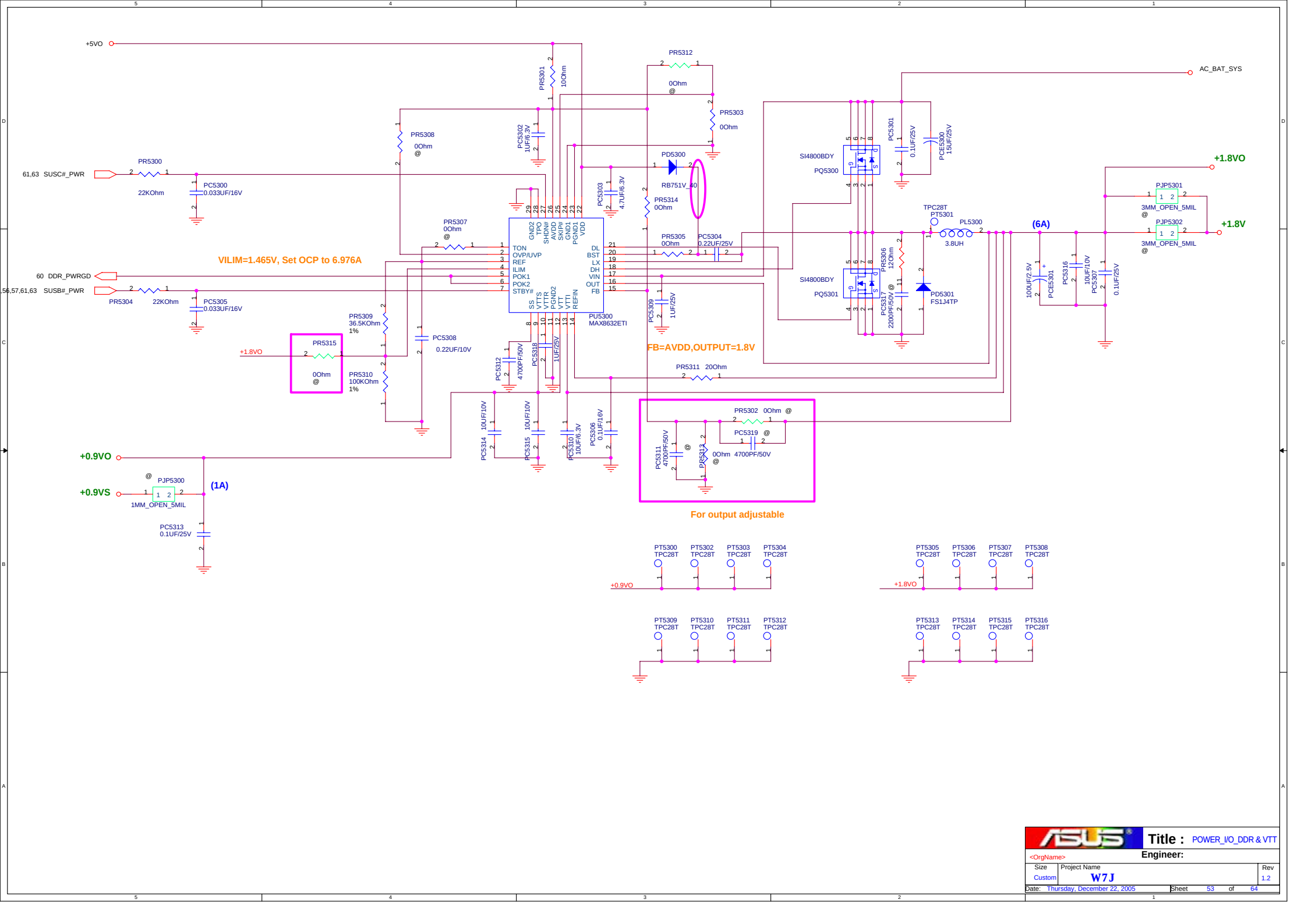




ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 51 of 64	

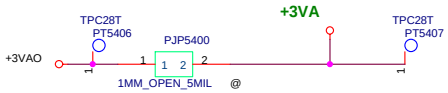


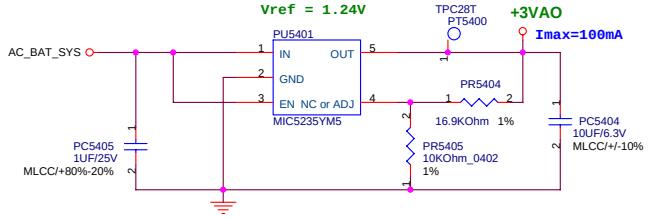
ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 52 of 64	



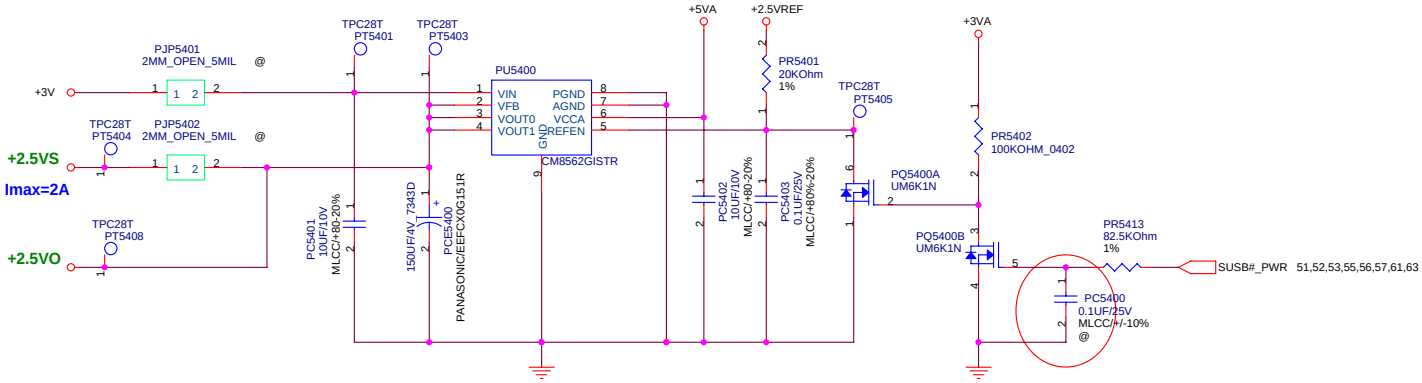
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 53 of 64	

+3VA0

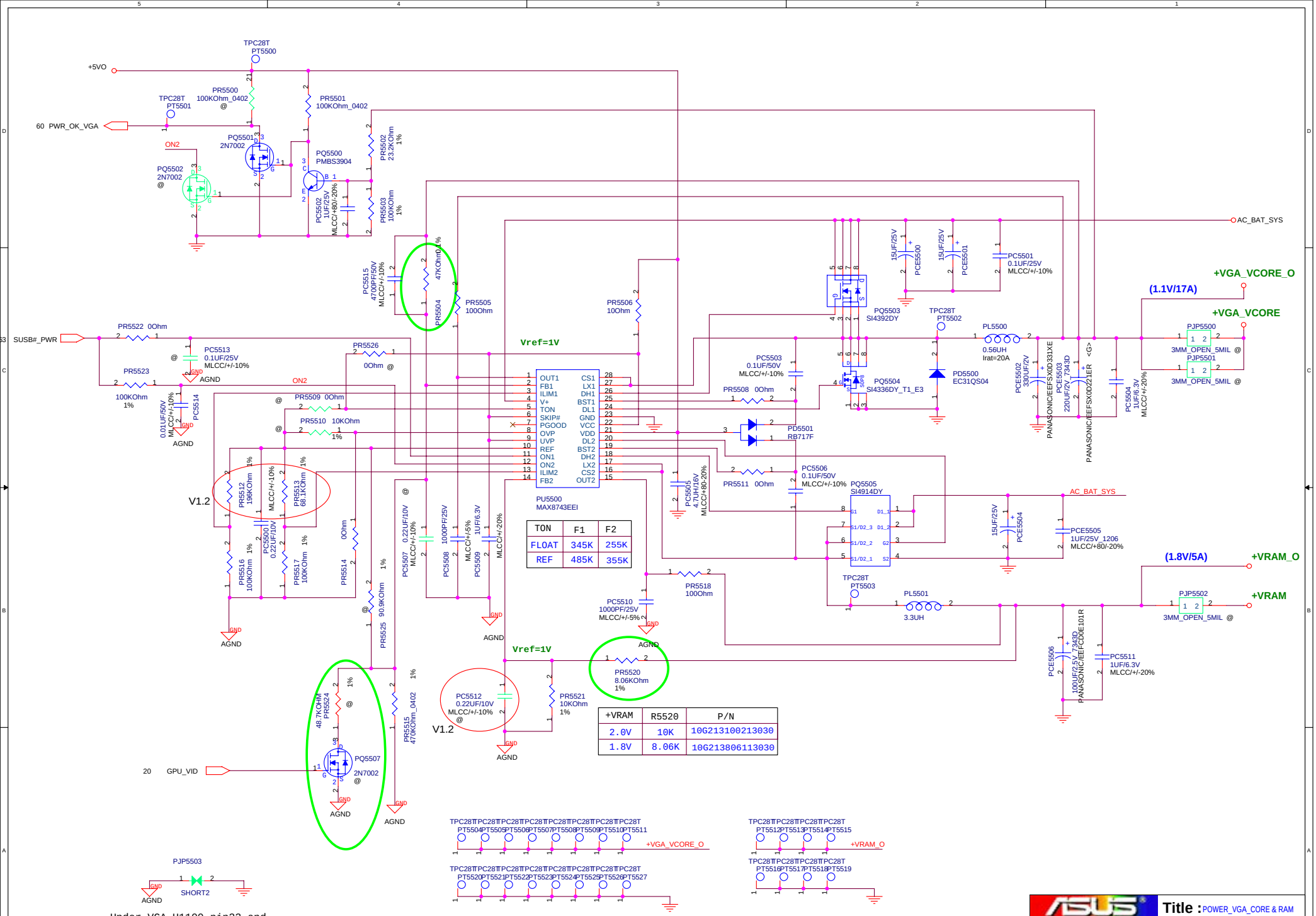




+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 54 of 64	


+5VO
60 PWR_OK_VGA
ON2
SUSB#_PWR
AC_BAT_SYS
+VGA_VCORE_O
(1.1V/17A)
+VGA_VCORE
+VRAM_O
(1.8V/5A)
+VRAM
Vref=1V
PU5500
MAX8743EEI
TON F1 F2
FLOAT 345K 255K
REF 485K 355K
+VRAM R5520 P/N
2.0V 10K 10G213100213030
1.8V 8.06K 10G213806113030
20 GPU_VID
Under VGA_U1100 pin23 and VGA_JP1100 pin2 via to GND
Title : POWER_VGA_CORE & RAM
Engineer:
Project Name W7 J
Rev 1.2
Date: Thursday, December 22, 2005
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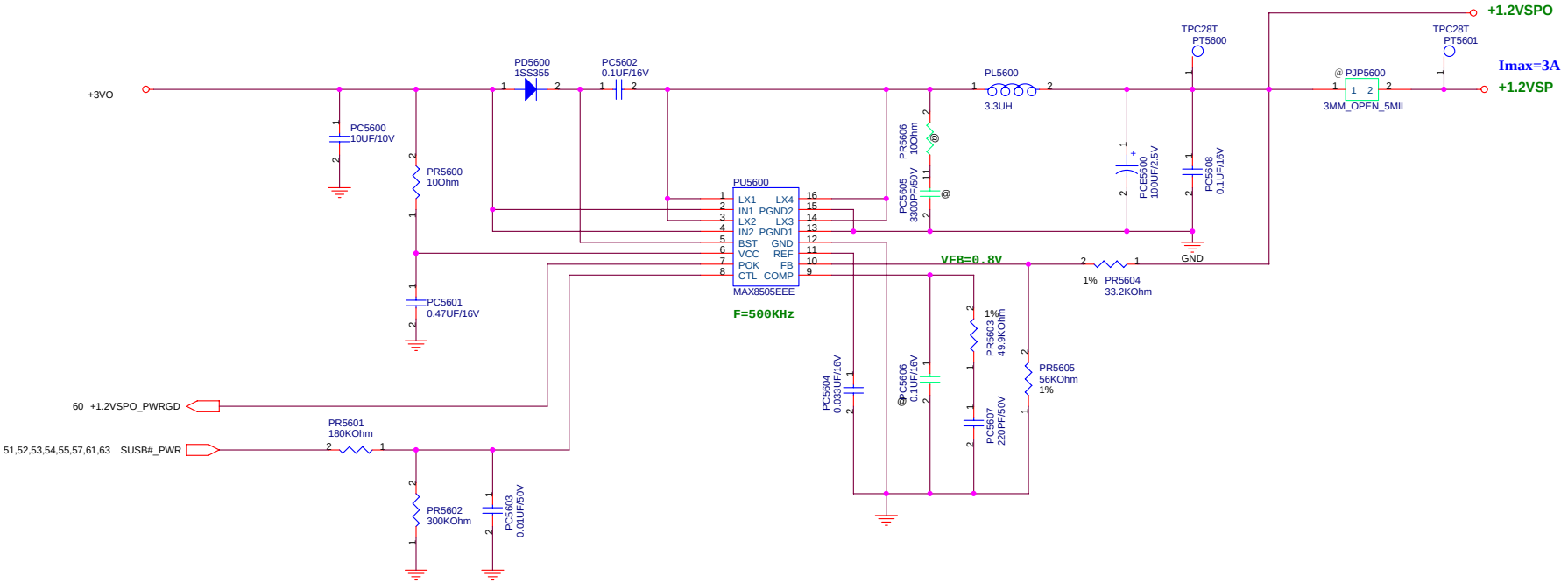
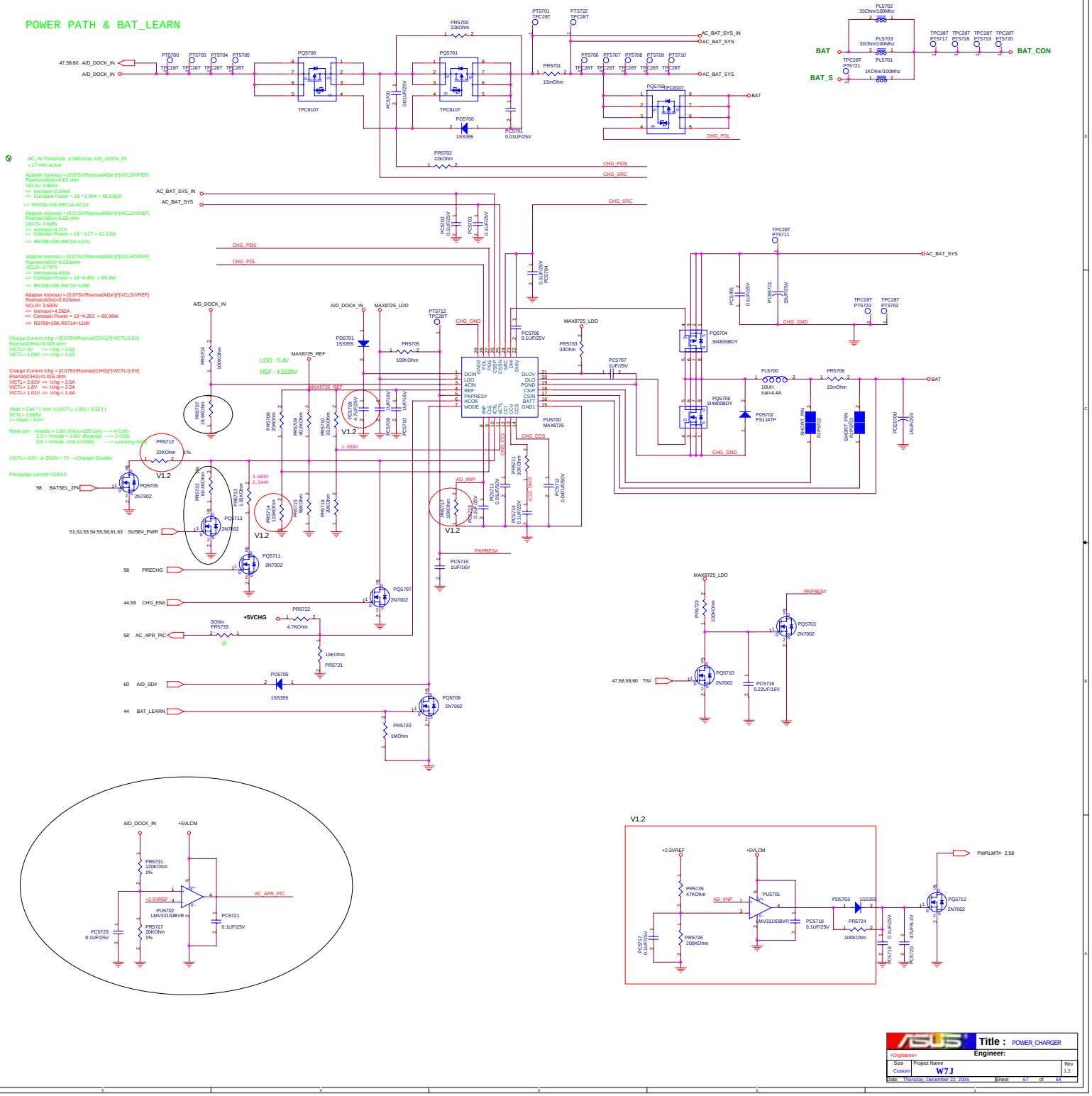
+1.2VSP

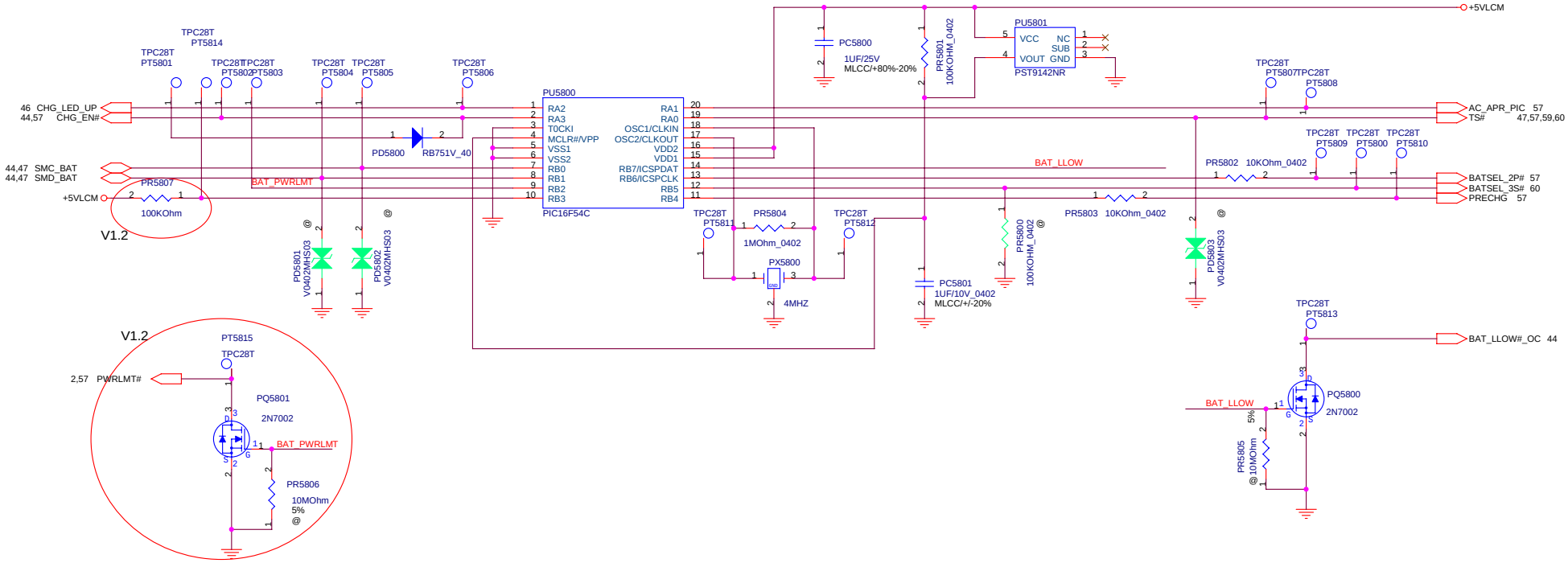


ASUS	Title : POWER_VGA_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 56 of 64	

POWER PATH & BAT_LEARN

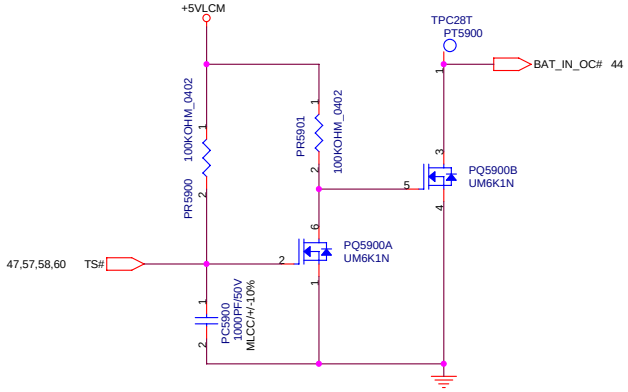


PIC16F54C

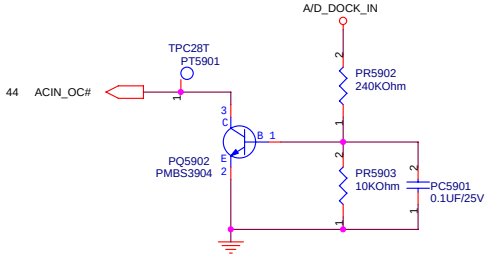


ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 58 of 64	

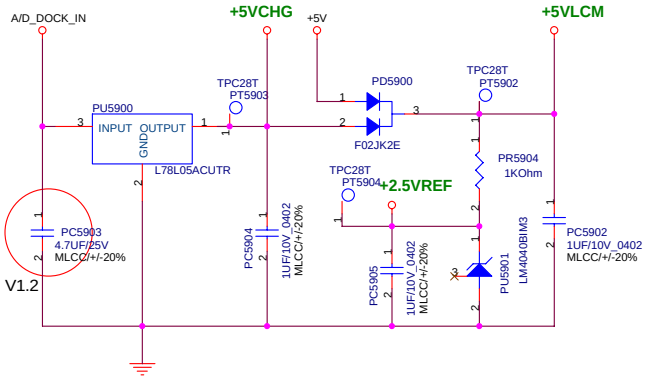
BATTERY IN DETECT



ADAPTER IN DETECT

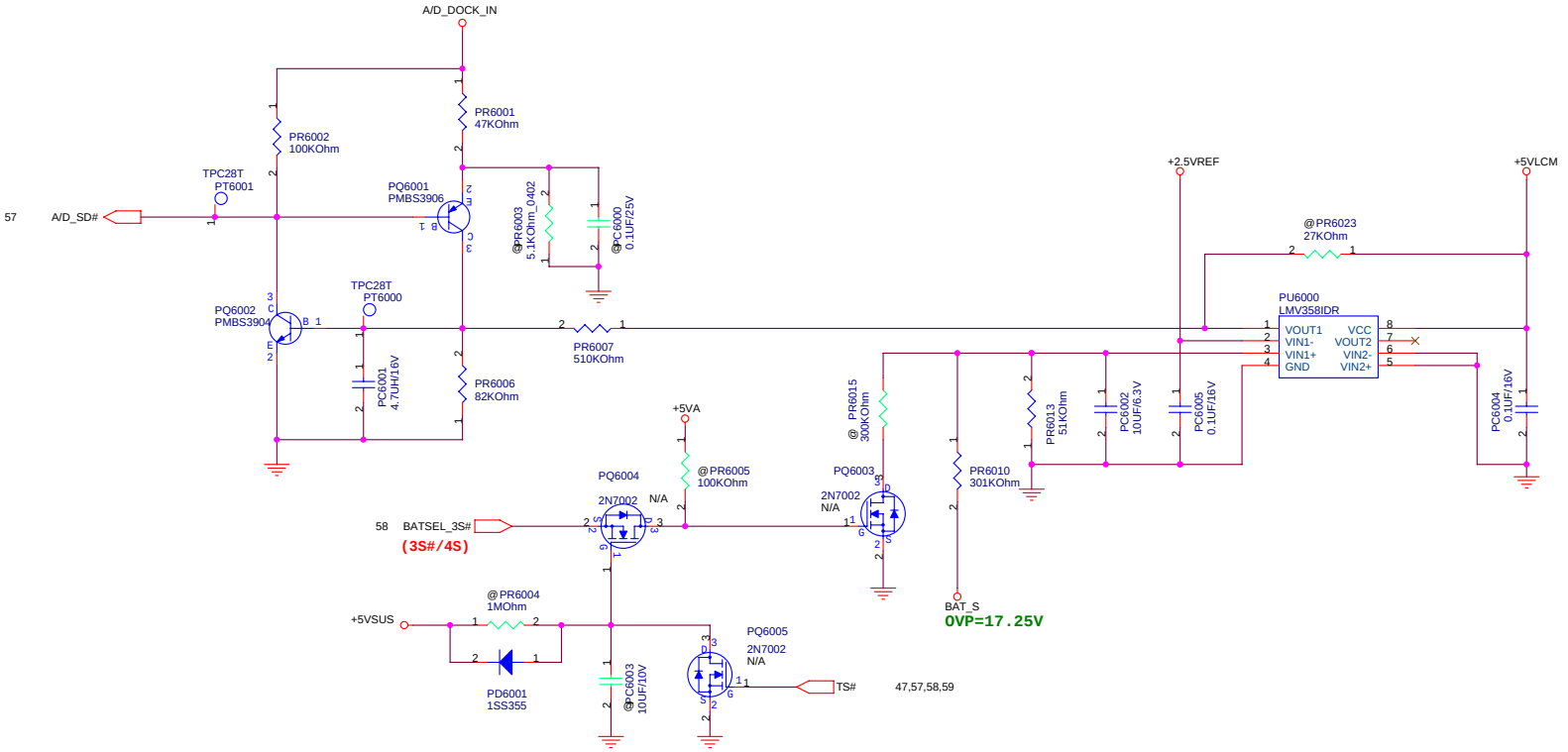


+5VLCM, +5VCHG & +2.5VREF

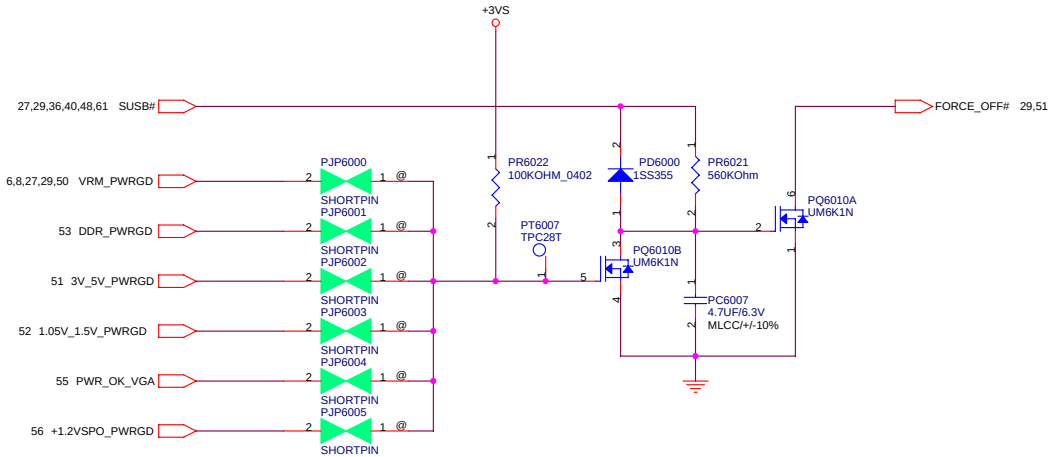


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 59 of 64	

BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.5V_PWRGD

ASUS

Title : POWER_PROTECT

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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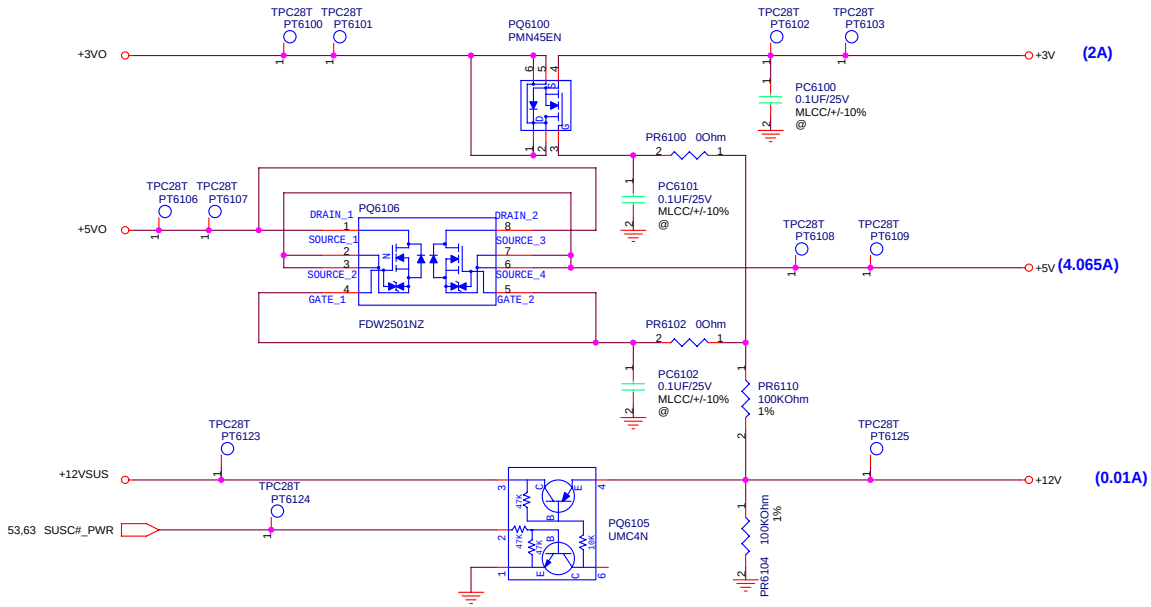
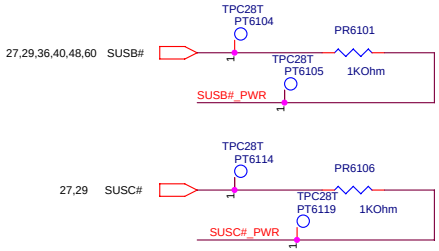
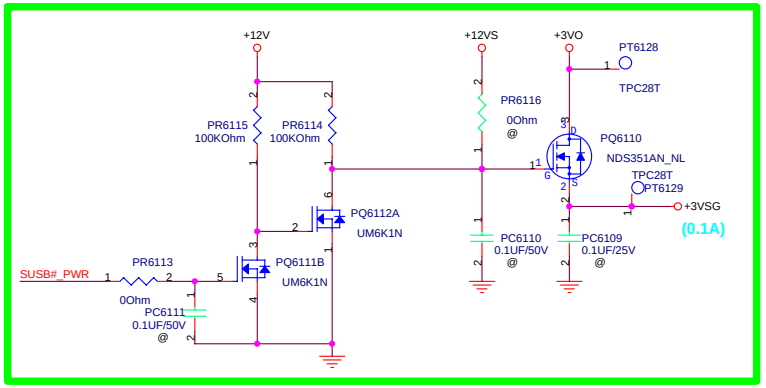
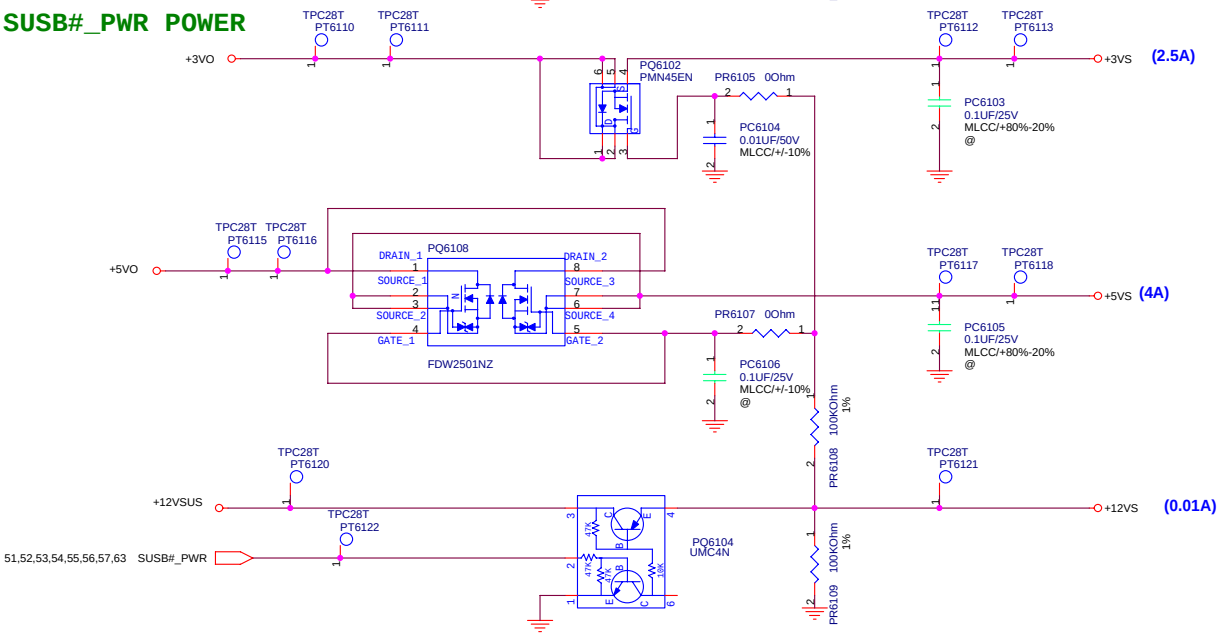
SUSC#_PWR POWER

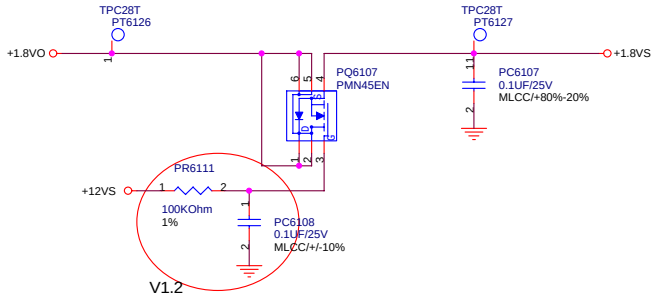




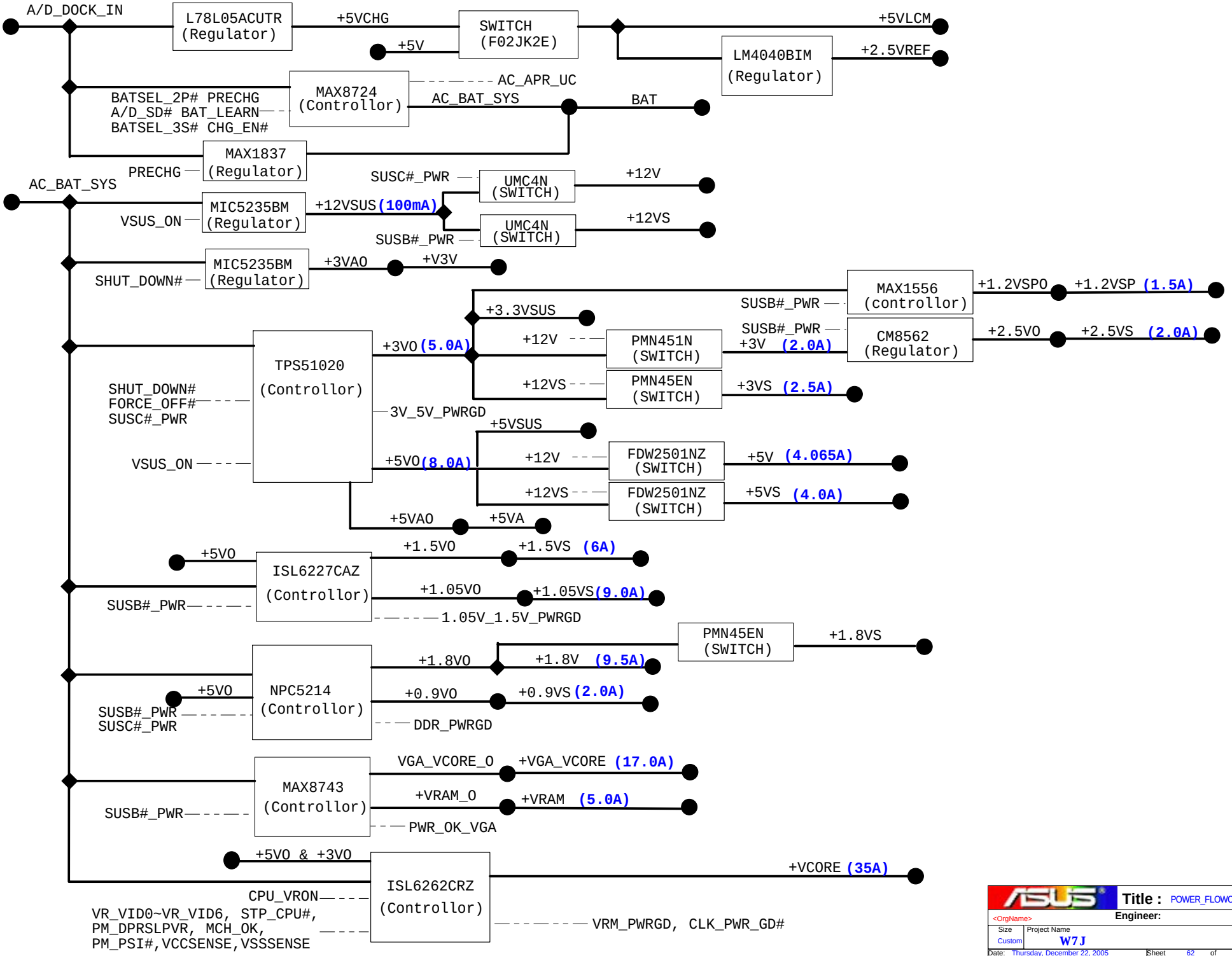


SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 61 of 64	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 62 of 64	

AC_BAT_SYS → AC_BAT_SYS 23,50,51,52,53,54,55,57

+3VA → +3VA 25,29,47,54

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3VSUS → +3VSUS 26,27,28,29,32,38,41,51

+5VSUS → +5VSUS 28,51,60

+3V → +3V 26,29,39,40,41,44,48,54,61

+3VS → +3VS 5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,48,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 27,32,33,61

+12VS → +12VS 5,24,34,46,61

+5V → +5V 16,30,32,37,44,45,46,47,48,59,61

+5VS → +5VS 5,24,28,29,30,32,33,42,43,44,46,47,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 10,20,21,48,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,12,13,14,15,16,48,53

+1.8VS → +1.8VS 20,61

+VCCP → +VCCP 2,3,4,6,7,8,10,11,12,25,28,52

+0.9VS → +0.9VS 16,53

BAT → BAT 57

+5VCHG → +5VCHG 29,57,59

+5VLCM → +5VLCM 23,44,46,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,4,5,44,50

+VGA_VCORE → +VGA_VCORE 17,55

+VRAM → +VRAM 18,19,22,55

+1.2VSP → +1.2VSP 17,18,48,56

BAT_CON → BAT_CON 47,57

FOR POWER TEST

+3VA

PJP6300 (1 2) SGL_JUMP @ → CPU_VRON_PWR 50

PJP6301 (1 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,55,56,57,61

PJP6302 (1 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 53,61

PJP6303 (1 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 63 of 64	

Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/29	1. Change Project name from W6J/H to W7J/F 2. Add NET: PWRLMT# to CPU pin: PROCHOT# (Page 2) 3. Add NET: DREFCLKSS,DREFCLKSS# to CLK GEN: pin17,pin18 (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# to GMCH: C40,D41 (Page 8) 5. Pull high GMCH VCCA_LVDC to +2.5VS (Page 10) 6. Add Jumper at G72M pin: B4 (Page 20) 7. Change R6811 from 200Kohm to 100Kohm (Page 23) 8. Change U57,U58 from 74LVC1G32GV to NC7SZ08M5 (Page 24) 9. Change D2 from EC31QS04 to RB751V_40 (Page 24) 10. Add Double-pi filter in VGA port (Page 24) 11. Swap ICH PCIE lans (Page 26) 12. Change GPIO7 NET from WB_AP to MUTE_POP_ICHGPIO# (Page 27) 13. Add NET: PWR_LED_1HZ to ICH: GPIO13 (Page 27) 14. Add Q6197 in net: PCIE_WAKE# (Page 27) 15. Add Q6192 in net: PWR_SW#_Q (Page 29) 16. Change R719 from 100Kohm to 1Mohm (Page 29) 17. Change R306 from 1Mohm to 10Mohm (Page 29) 18. Change C388 from 0.33uF to 1uF (Page 29) 19. Change Pull-high LID_EC# from +3VSUS to +3V (Page 29) 20. Change Audio CODEC from ADI1986 to ALC660 (Page 30) 21. Change R6614 from 0ohm to 4.7Kohm (Page 32) 22. Change R6616 from 10Kohm to 51KOhm (Page 32) 23. Change R6613 from 0ohm to 4.7Kohm (Page 32) 24. Change R6615 from 10Kohm to 51KOhm (Page 32) 25. Add NET: MUTE_POP_ICHGPIO# to MUTE_POP# circuit (Page 32) 26. Add Q6193 in net: SUSCLK (Page 34) 27. Change SLB9635TT pin16 from PLT_RST# to BUF_PLT_RST# (Page 34) 28. Delete NET PME# (Page 36) 29. Change Pull-high MDIO04 from +3V to +3VS (Page 37) 30. Change Pull-high XD_PWR_EN from +3V to +3VS (Page 37) 31. Change PCIE lans from port 1 to port 2 (Page 38) 32. Add C6625,C6626 in phone connector (Page 39) 33. Change PCIE lans from port 3 to port 1 (Page 40) 34. Add NET: EXPD# to R5538 pin20 (Page 40) 35. Add NET: C_PRESENT# to R5538 pin9,pin10 (Page 40) 36. Change PCIE lans from port 2 to port 3 (Page 41) 37. Change Pull-high 802WLAN_ON# from +3V to +3VSUS (Page 41) 38. Change FWH packaging from PLCC to TSOP (Page 43) 39. Add NET: EXPD# to M38857 P53 (Page 44) 40. Add NET: WB_AP to M38857 P67 (Page 44) 41. Add NET: C_PRESENT# to M38857 P62 (Page 44) 42. Add NET: ACZ_RST#_AUD to M38857 P61 (Page 44) 43. Change U10,U6012 pin4 from SUSC# to SUSC (Page 45) 44. Add Q6196 in net: BTPWRCL# (Page 45) 45. Add R6922 between net: WIRELESS_LAN_ON/OFF# and WB_AP (Page 47) 46. Add Q6198 in +3VS discharge (Page 48) 47. Change Power LED ON circuit (Page 48)

Rev	Date	Description
R1.2	2005/12/20	1. Change R6491 from 23.2KOhm to 51KOhm (Page 5) 2. Add Q6200 at U42 :D2+,D2- (Page 5) 3. Add NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 4. Add RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 5. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 4. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 5. Change R1001 from 1Kohm to C6631:0.1uF (Page 16) 6. Modify LCD enable circuit by U6059 (Page 23) 7. Change L89,L90,L92 to Bead 120Ohm/100MHz (Page 24) 8. Change Q60,Q61 from SI1906DL to SI1902DL (Page 24) 9. Add C6632 in Y1 (Page 25) 10. Connect H_DPRSTP# to PU5000 (Page 25) 11. Change U69 from SN74LVC1G32G to 74LVC1G32GV (Page 26) 12. Disonnect STP_CPU# to PU5000 (Page 27) 13. Add GPIO9:W_OLED# (Page 27) 14. Change R523 from 10KOhm to 100KOhm (Page 29) 15. Change R303 from 10KOhm to C6630:1uF (Page 29) 16. Add R6936 in Net:PWR_SW#_Q (Page 29) 17. Add R6633,R6634,R6635,R6636 in CN20(Page 31) 18. Add R6938 in +3.3Vaux (Page 41) 19. Change CE41,CE5705,CE25 from 100uF to 150uF (Page 45) 20. Add R6937 in BTPWRCL# (Page 45) 21. Change Q6180,Q6181 by Q6202 (Page 46) 22. Add Q6201,LED10 in WIRELESS_OLED# (Page 46) 23. Change R6686 from 0Ohm to 470Ohm (Page 47) 24. Add R6940 in Power Board +5Vs (Page 47)

<Variant Name>

Title : History

ASUSTek Computer INC. NB1

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 64 of 64