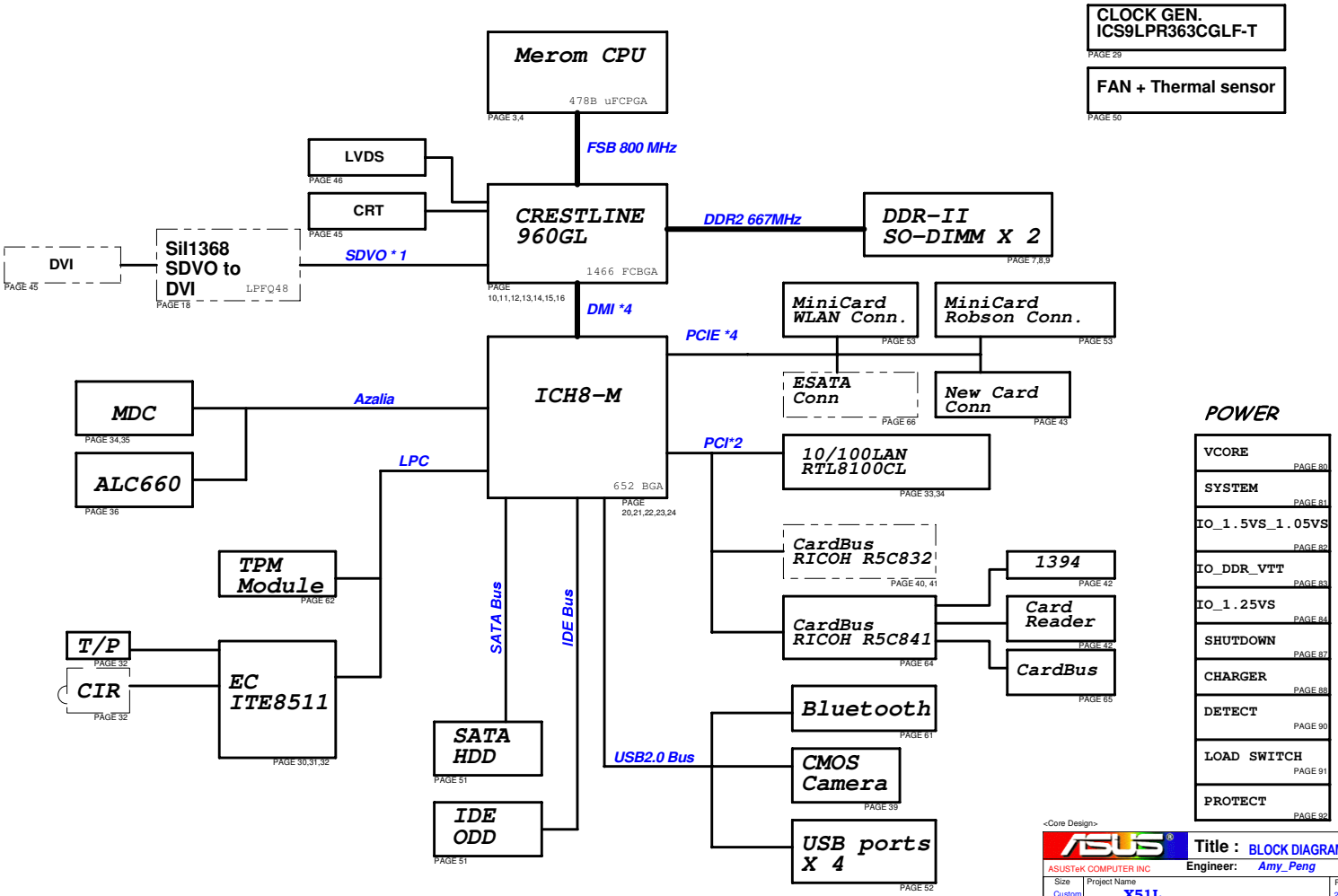
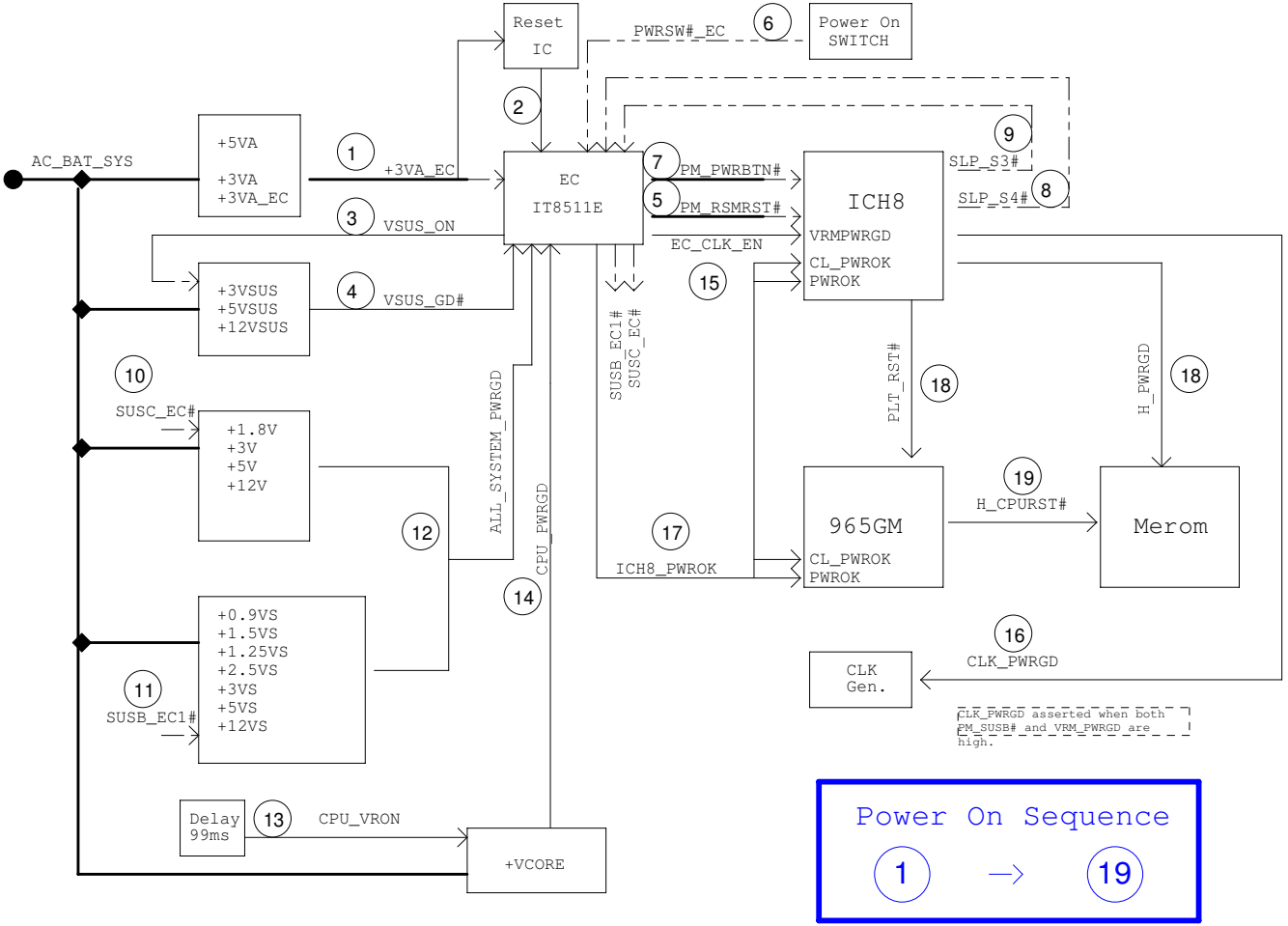
X51L Main BD. R2.0 BLOCK DIAGRAM



<Core Design>

ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Amy_Peng	
Size: Custom	Project Name: X51L	Rev: 2.2
Date: Friday, September 21, 2007	Sheet 1 of 94	



<Core Design>

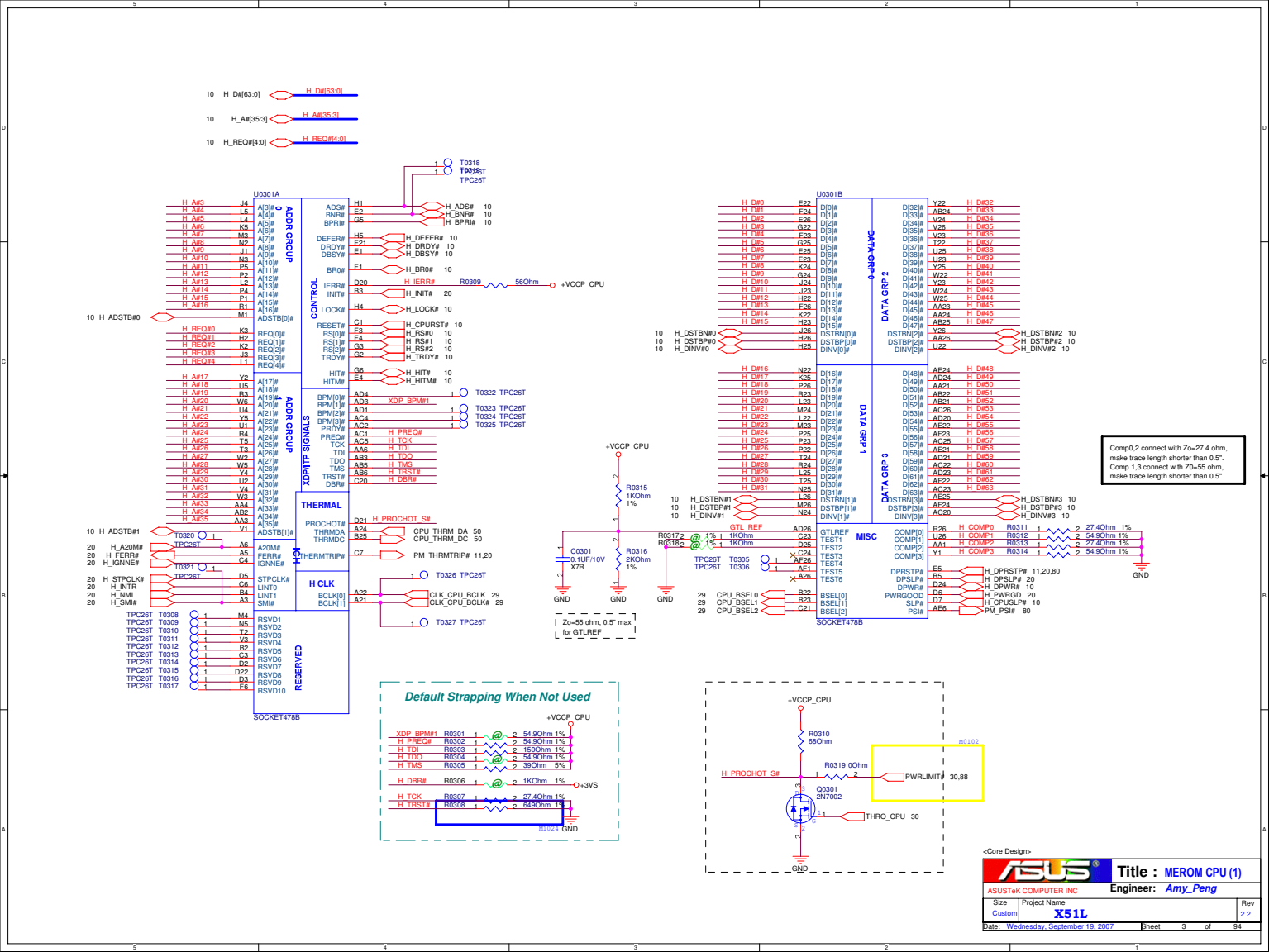
ASUSTeK COMPUTER INC

Title : PowerOn sequence

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 2 of 94


U0301A
U0301B
SOCKET478B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
H_D#[63:0]
H_A#[35:3]
H_REQ#[4:0]
H_ADSTB#0
H_ADSTB#1
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
H_PROCHOT_S#
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR#
H_INIT#
H_LOCK#
H_CPURST#
H_RS#0
H_RS#1
H_RS#2
H_TRDY#
H_HIT#
H_HITM#
H_PREQ#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
H_DBR#
CPU_THRM_DA
CPU_THRM_DC
PM_THRMTRIP#
CLK_CPU_BCLK
CLK_CPU_BCLK#
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
+VCCP_CPU
+3VS
GTL_REF
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
H_COMP0
H_COMP1
H_COMP2
H_COMP3
H_DPRSTP#
H_DPSLP#
H_DPWR#
H_PWRGD
H_CPUSLP#
PM_PSI#
PWRLIMIT#
THRO_CPU
Q0301
2N7002
R0309 56Ohm
R0310 68Ohm
R0319 0Ohm
C0301 0.1UF/10V X7R
R0316 2KOhm 1%
R0315 1KOhm 1%
R0317 1KOhm 1%
R0318 1KOhm 1%
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".
Default Strapping When Not Used
XDP_BPM#1 R0301 54.9Ohm 1%
H_PREQ# R0302 54.9Ohm 1%
H_TDI R0303 150Ohm 1%
H_TDO R0304 54.9Ohm 1%
H_TMS R0305 39Ohm 5%
H_DBR# R0306 1KOhm 1%
H_TCK R0307 27.4Ohm 1%
H_TRST# R0308 649Ohm 1%
M0102
M1024
GND
<Core Design>
ASUSTeK COMPUTER INC
Title : MEROM CPU (1)
Engineer: Amy_Peng
Size: Custom
Project Name: X51L
Rev: 2.2
Date: Wednesday, September 19, 2007
Sheet 3 of 94

Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)

+VCCP_CPU
CE0401
100UF/2.5V
GND

+VCORE
CE0402
330UF/2V
GND

+VCCP
JP0401
SHORT_PIN
@

+VCCP_CPU
C0401 C0402 C0403 C0404 C0405 C0406
0.1UF/10V X7R
GND

+VCORE
C0407 C0408 C0409 C0410 C0411 C0412
10UF/6.3V X5R
C0413 C0414 C0415 C0416 C0417 C0418
10UF/6.3V X5R
C0419 C0420 C0421 C0422
10UF/6.3V X5R
C0423 C0424 C0425 C0426
10UF/6.3V X5R
GND

+VCORE
+VCORE
U0301C
SOCKET478B

+VCORE
(CPU core power)
Max: 44000mA

+VCCP_CPU
(CPU AGTL+ power)
Max: 2500mA

+VCCA_CPU
(CPU PLL power)
Max: 130mA

+1.5VS
+VCCA_CPU
R0401 0Ohm r0603_h24
C0427 0.1UF/16V
C0428 10UF/6.3V X5R
GND

M1102
AD6_H_VID0 AF5_H_VID1 AE5_H_VID2 AF4_H_VID3 AE3_H_VID4 AF3_H_VID5 AE2_H_VID6
0Ohm
RNX0401B RNX0402C RNX0402B RNX0402A RNX0401A RNX0401D RNX0401C
VR_VID0 VR_VID1 VR_VID2 VR_VID3 VR_VID4 VR_VID5 VR_VID6 80
RNX0402D

R0402 100Ohm YAGEO/RC0402FR-07100RL <G>
+VCORE
VCCSENSE 80
VSSSENSE 80

R0403 100Ohm YAGEO/RC0402FR-07100RL <G>
GND

VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

U0301D
SOCKET478B
GND

<Core Design>

ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 4 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 5 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 6 of 94

P/N: 12G025022004
(T12F) 4.0mm, STD

M122.7

M_CLK_DDR0
R0701 69.8Ohm PLACE NEAR SO-DIMM_1
M_CLK_DDR#0
M_CLK_DDR1
R0702 69.8Ohm PLACE NEAR SO-DIMM_1
M_CLK_DDR#1

SMBus Slave Address:A0H

9,13 M_A_A[0..13]
M_A_DQ[0..63] 13
J0701A
DDR2_DIMM_200P

9,11 M_A_A14
9,13 M_A_BS2
9,13 M_A_BS0
9,13 M_A_BS1
9,11 M_CS#0
9,11 M_CS#1
11 M_CLK_DDR0
11 M_CLK_DDR#0
11 M_CLK_DDR1
11 M_CLK_DDR#1
9,11 M_CKE0
9,11 M_CKE1
9,13 M_A_CAS#
9,13 M_A_RAS#
9,13 M_A_WE#
8,24,29,43,53 SMB_CLK_S
8,24,29,43,53 SMB_DAT_S
9,11 M_ODT0
9,11 M_ODT1
13 M_A_DM[0..7]
13 M_A_DQS[0..7]
13 M_A_DQS#[0..7]
GND

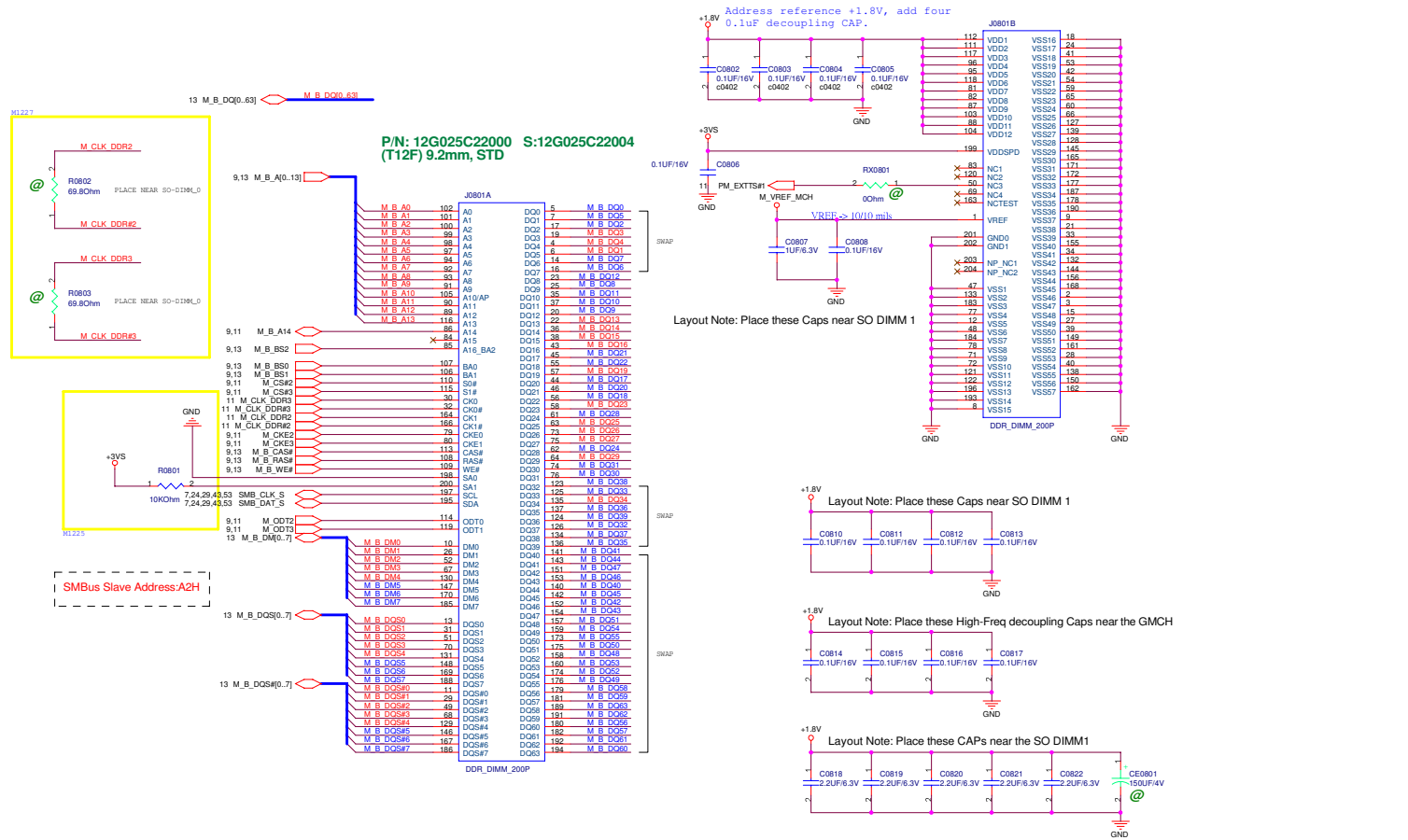
SMAP

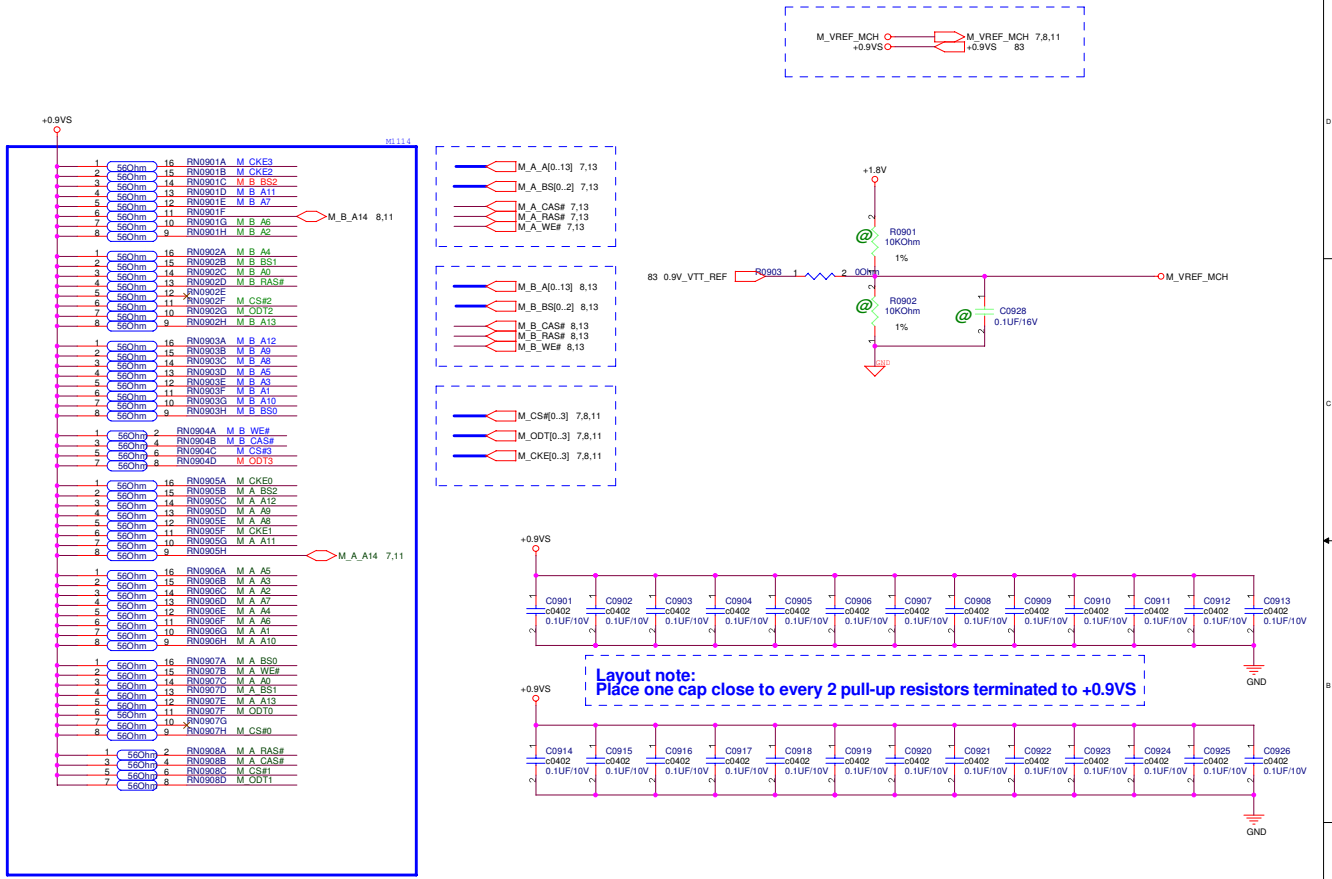
SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

Layout Note: Place these Caps near SO DIMM 0
+1.8V
C0702 0.1UF/16V
C0703 0.1UF/16V
C0704 0.1UF/16V
C0705 0.1UF/16V
GND
+3VS
C0707 0.1UF/16V
PM_EXTTS#0
RX0701 0Ohm
M_VREF_MCH
VREF=> 10/10 mils
C0708 2.2UF/6.3V
C0709 0.1UF/16V
J0701B
DDR2_DIMM_200P

Layout Note: Place these Caps near SO DIMM 0
+1.8V
C0710 1UF/6.3V
C0711 1UF/6.3V
C0712 1UF/6.3V
C0713 1UF/6.3V
C0714 1UF/6.3V
C0715 2.2UF/6.3V
C0716 2.2UF/6.3V
C0717 2.2UF/6.3V
C0718 2.2UF/6.3V
C0719 2.2UF/6.3V
CE0701 150UF/4V

<Core Design>
Title : DDR2 SO-DIMM_0
ASUSTeK COMPUTER INC
Engineer: Amy_Peng
Size: Custom
Project Name: X51L
Rev: 2.2
Date: Wednesday, September 19, 2007
Sheet 7 of 94


P/N: 12G025C22000 S:12G025C22004
(T12F) 9.2mm, STD
Address reference +1.8V, add four
0.1uF decoupling CAP.
Layout Note: Place these Caps near SO DIMM 1
Layout Note: Place these Caps near SO DIMM 1
Layout Note: Place these High-Freq decoupling Caps near the GMCH
Layout Note: Place these CAPs near the SO DIMM1
VREF -> 10/10 mils
SMBus Slave Address:A2H
J0801A
J0801B
DDR_DIMM_200P
DDR_DIMM_200P
M1227
M1225
SWAP
SWAP
SWAP



<Core Design>

ASUSTeK COMPUTER INC

Title : DDR2 TERM

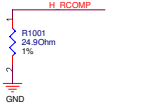
Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 9 of 94

RCOMP

For Calibrating the FSB I/O Buffer

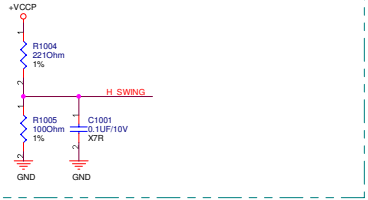


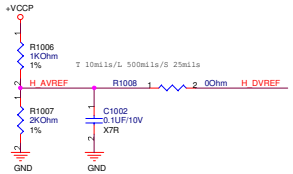
SCOMP

For Slew Rate Compenssation on the FSB

Voltage Swing

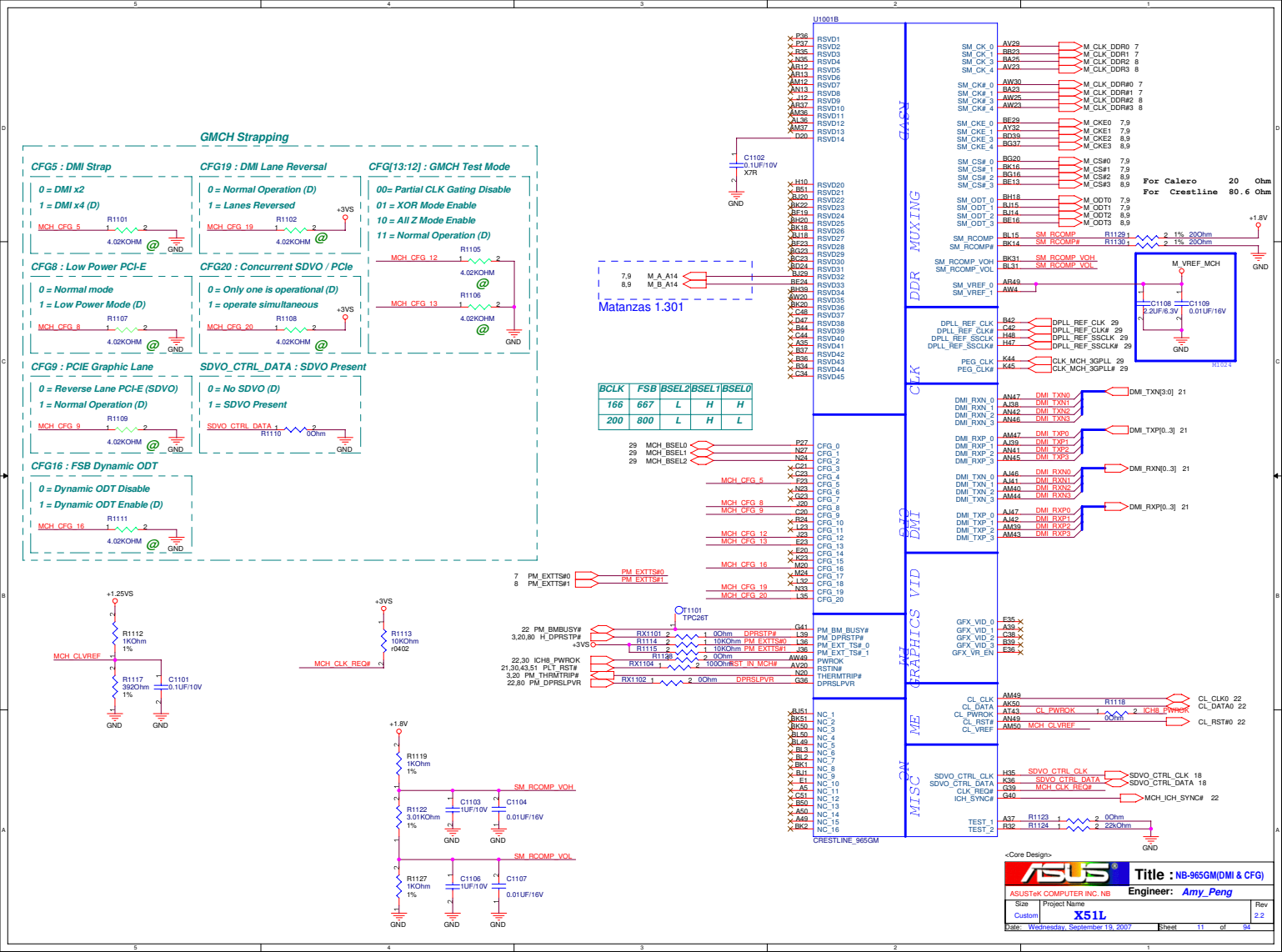
For Providing a Reference Voltage to The FSB RCOMP circuits

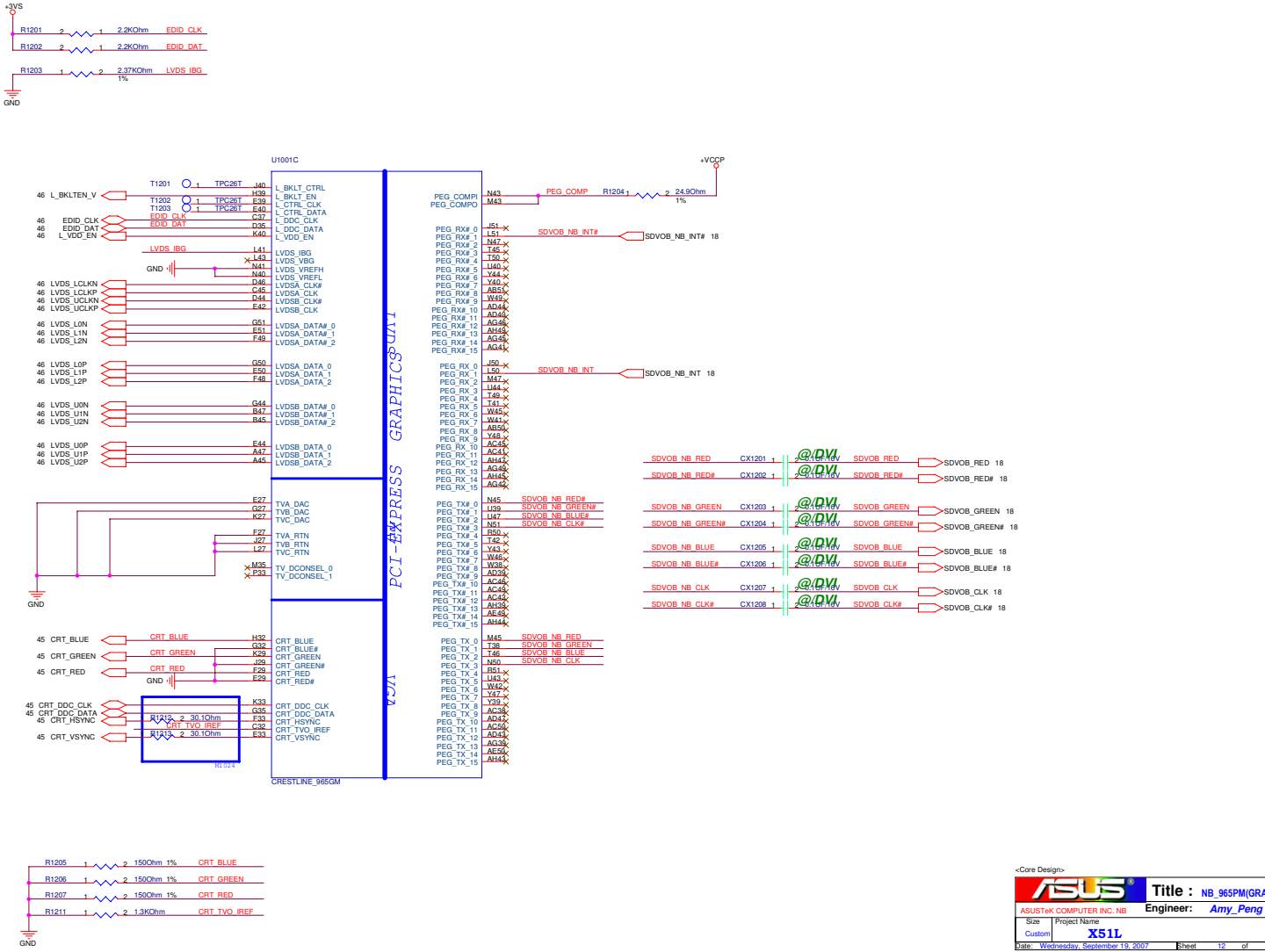




<Core Design>

ASUSTeK COMPUTER INC. NB	Title : NB-965GM (HOST)		
	Engineer: Amy_Peng		
Size: Custom	Project Name: X51L		Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 10 of 94		


GMCH Strapping
CFG5 : DMI Strap
0 = DMI x2
1 = DMI x4 (D)
R1101
MCH_CFG_5
4.02KOHM
GND
CFG19 : DMI Lane Reversal
0 = Normal Operation (D)
1 = Lanes Reversed
R1102
MCH_CFG_19
4.02KOHM
+3VS
CFG[13:12] : GMCH Test Mode
00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)
R1105
MCH_CFG_12
4.02KOHM
R1106
MCH_CFG_13
4.02KOHM
CFG8 : Low Power PCI-E
0 = Normal mode
1 = Low Power Mode (D)
R1107
MCH_CFG_8
4.02KOHM
CFG20 : Concurrent SDVO / PCIe
0 = Only one is operational (D)
1 = operate simultaneous
R1108
MCH_CFG_20
4.02KOHM
+3VS
CFG9 : PCIE Graphic Lane
0 = Reverse Lane PCI-E (SDVO)
1 = Normal Operation (D)
R1109
MCH_CFG_9
4.02KOHM
SDVO_CTRL_DATA : SDVO Present
0 = No SDVO (D)
1 = SDVO Present
SDVO_CTRL_DATA
R1110
0Ohm
CFG16 : FSB Dynamic ODT
0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)
R1111
MCH_CFG_16
4.02KOHM
U1001B
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
RSVD39
RSVD40
RSVD41
RSVD42
RSVD43
RSVD44
RSVD45
C1102
0.1UF/10V
X7R
GMCH
Matanzas 1.301
M_A_A14
M_B_A14
BCLK
FSB
BSEL2
BSEL1
BSEL0
166
667
L
H
H
200
800
L
H
L
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
PM_EXTTS#0
PM_EXTTS#1
T1101
TPC26T
PM_BM_BUSY#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
CRESTLINE_965GM
DDR MUXING
CLK
DMI
GRAPHICS VID
ME
MISC
SM_CK_0
SM_CK_1
SM_CK_3
SM_CK_4
SM_CK#_0
SM_CK#_1
SM_CK#_3
SM_CK#_4
SM_CKE_0
SM_CKE_1
SM_CKE_3
SM_CKE_4
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP
SM_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_VREF_0
SM_VREF_1
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#2
M_CLK_DDR#3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS#0
M_CS#1
M_CS#2
M_CS#3
M_ODT0
M_ODT1
M_ODT2
M_ODT3
For Calero 20 Ohm
For Crestline 80.6 Ohm
+1.8V
R1129
R1130
2 1% 200hm
M_VREF_MCH
C1108
2.2UF/6.3V
C1109
0.01UF/16V
R1024
DPLL_REF_CLK
DPLL_REF_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
PEG_CLK
PEG_CLK#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_TXN[3:0]
DMI_TXP[0..3]
DMI_RXN[0..3]
DMI_RXP[0..3]
GFX_VID_0
GFX_VID_1
GFX_VID_2
GFX_VID_3
GFX_VR_EN
CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
R1118
0Ohm
ICH8_PWROK
CL_CLK0
CL_DATA0
CL_RST#0
MCH_CLVREF
SDVO_CTRL_CLK
SDVO_CTRL_DATA
CLK_REQ#
ICH_SYNC#
MCH_ICH_SYNC#
TEST_1
TEST_2
R1123
R1124
22kOhm
+1.25VS
R1112
1KOhm
1%
R1117
392Ohm
C1101
0.1UF/10V
+3VS
R1113
10KOhm
r0402
MCH_CLK_REQ#
+1.8V
R1119
1KOhm
R1122
3.01KOhm
C1103
1UF/10V
C1104
0.01UF/16V
SM_RCOMP_VOH
R1127
1KOhm
C1106
1UF/10V
C1107
0.01UF/16V
SM_RCOMP_VOL
RX1101
RX1114
R1115
R1138
RX1104
RX1102
0Ohm
10KOhm
DPRSTP#
PM_EXTTS#0
PM_EXTTS#1
RST_IN_MCH#
DPRSLPVR
22 PM_BMBUSY#
3,20,80 H_DPRSTP#
22,30 ICH8_PWROK
21,30,43,51 PLT_RST#
3,20 PM_THRMTRIP#
22,80 PM_DPRSLPVR
<Core Design>
ASUSTeK COMPUTER INC. NB
Title : NB-965GM(DMI & CFG)
Engineer: Amy_Peng
Size
Custom
Project Name
X51L
Rev
2.2
Date: Wednesday, September 19, 2007
Sheet 11 of 94

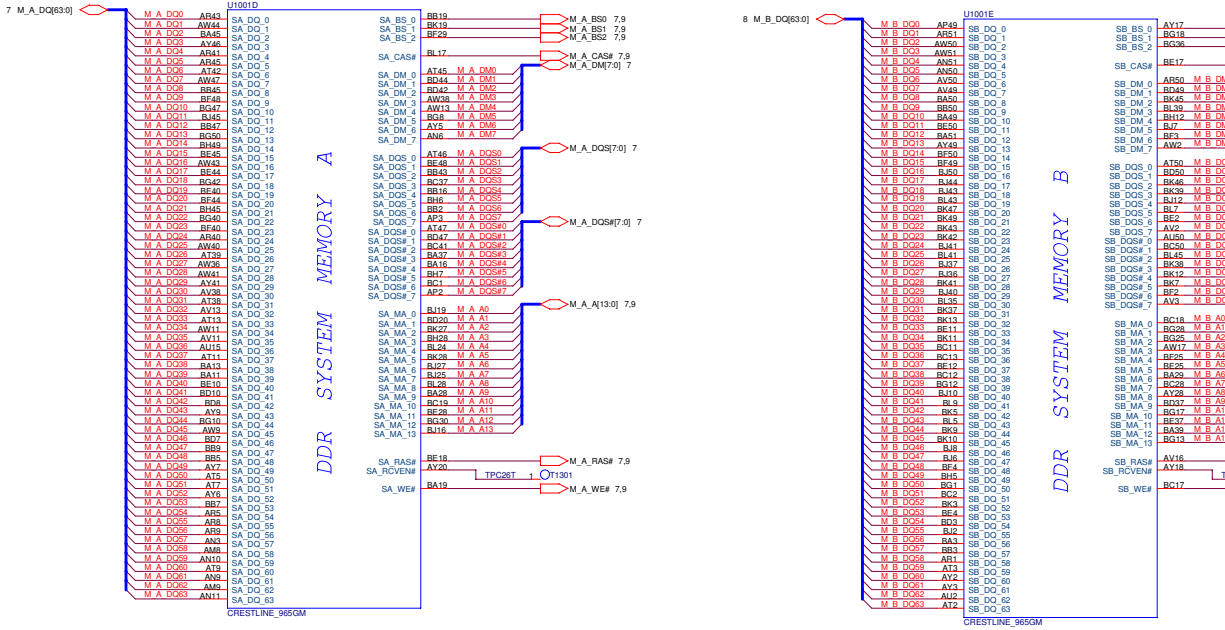


<Core Design>
ASUSTeK COMPUTER INC. NB
Engineer: Amy_Peng

Title : NB_965PM(GRAPHIC)

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 12 of 94



<Core Design>

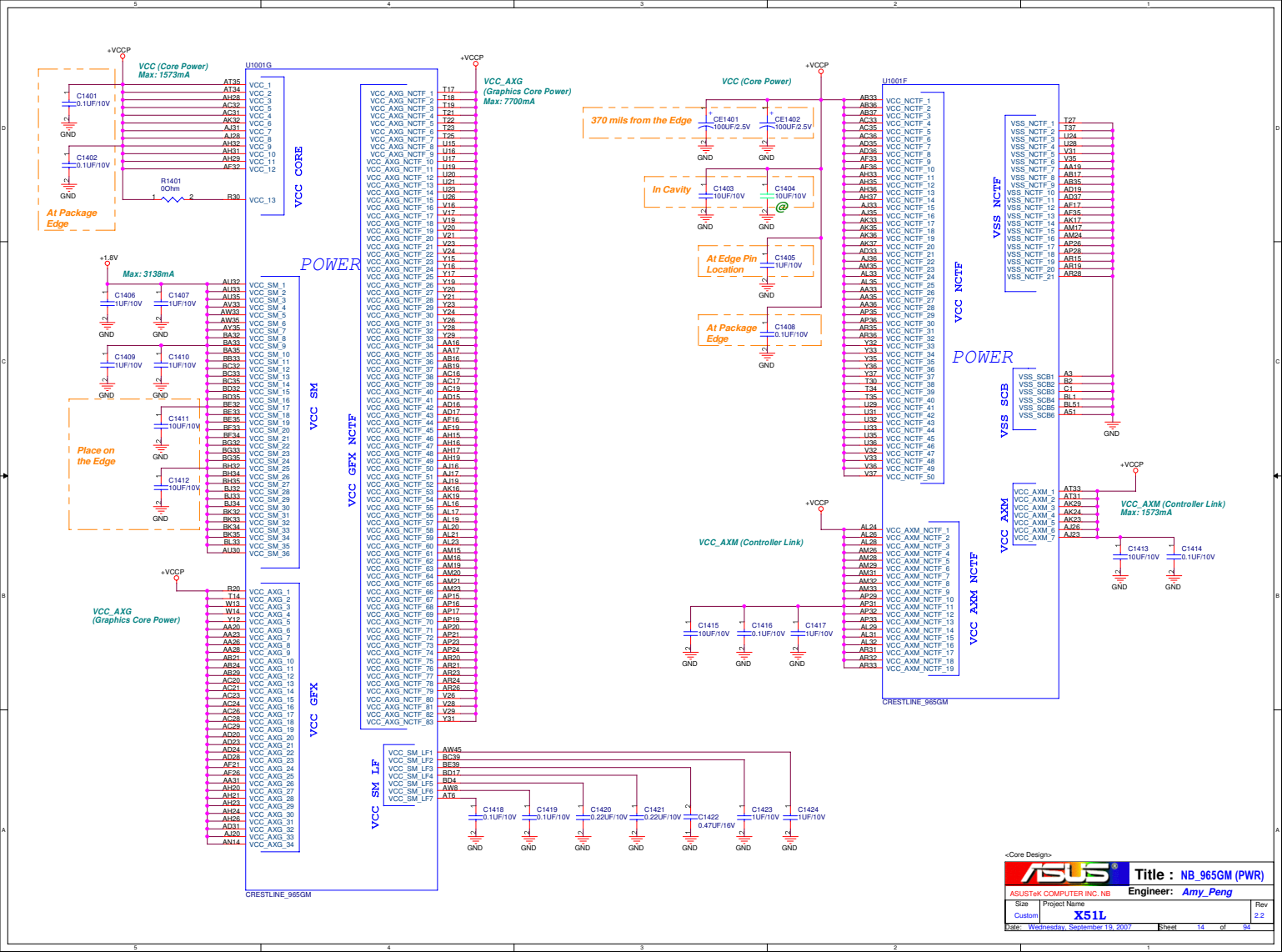
ASUSTeK COMPUTER INC. NB

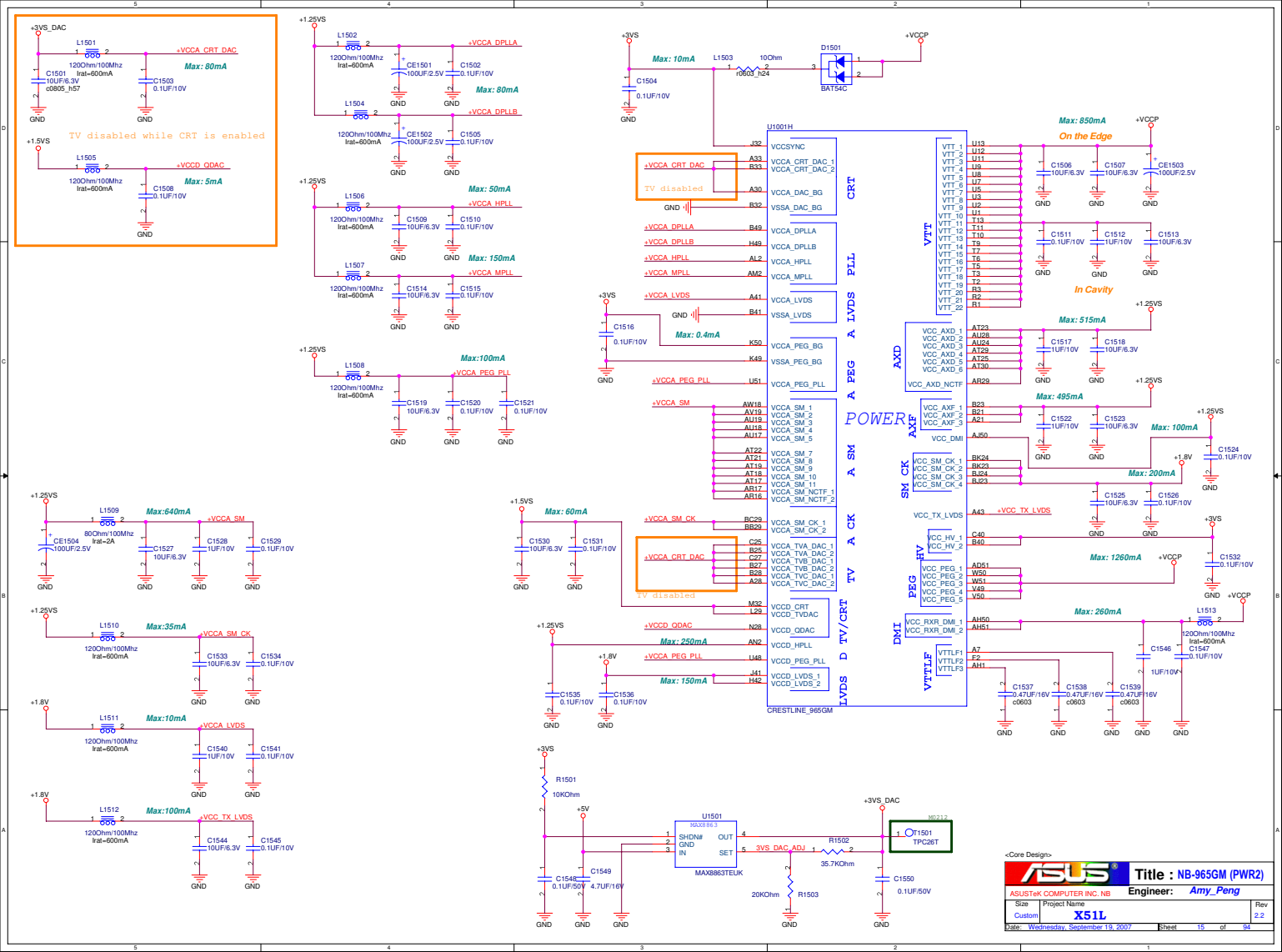
Title : NB-965PM(DDR2)

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 13 of 94


VCC (Core Power)
Max: 1573mA
U1001G
VCC CORE
VCC_AXG
(Graphics Core Power)
Max: 7700mA
370 mils from the Edge
In Cavity
At Edge Pin Location
At Package Edge
U1001F
VCC NCTF
VSS NCTF
VSS SCB
POWER
Max: 3138mA
VCC SM
VCC GFX NCTF
Place on the Edge
VCC_AXM (Controller Link)
Max: 1573mA
VCC AXM NCTF
VCC AXM
VCC GFX
VCC SM LF
CRESTLINE_965GM



<Core Design>

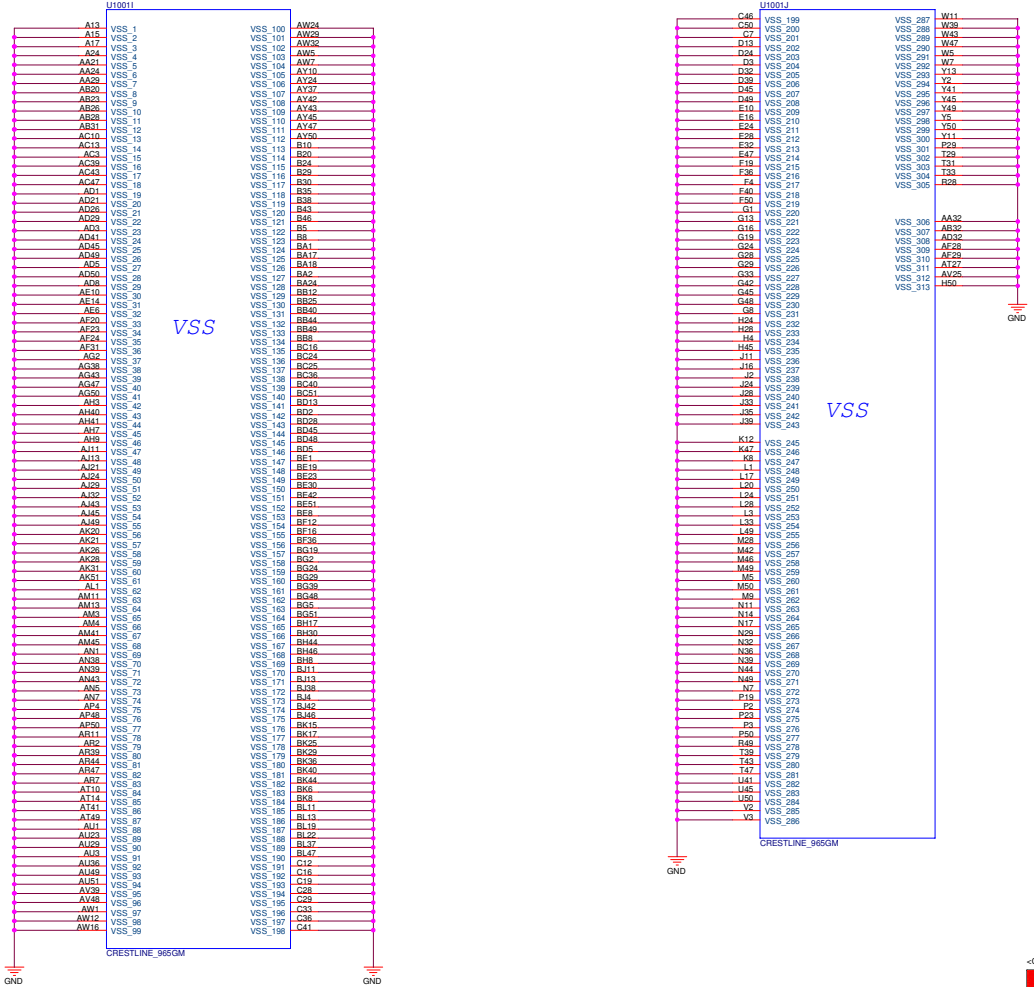
ASUSTeK COMPUTER INC. NB

Title : NB-965GM (PWR2)

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 15 of 94


U1001I
VSS
CRESTLINE_965GM
GND
GND
U1001J
VSS
CRESTLINE_965GM
GND

<Core Design>

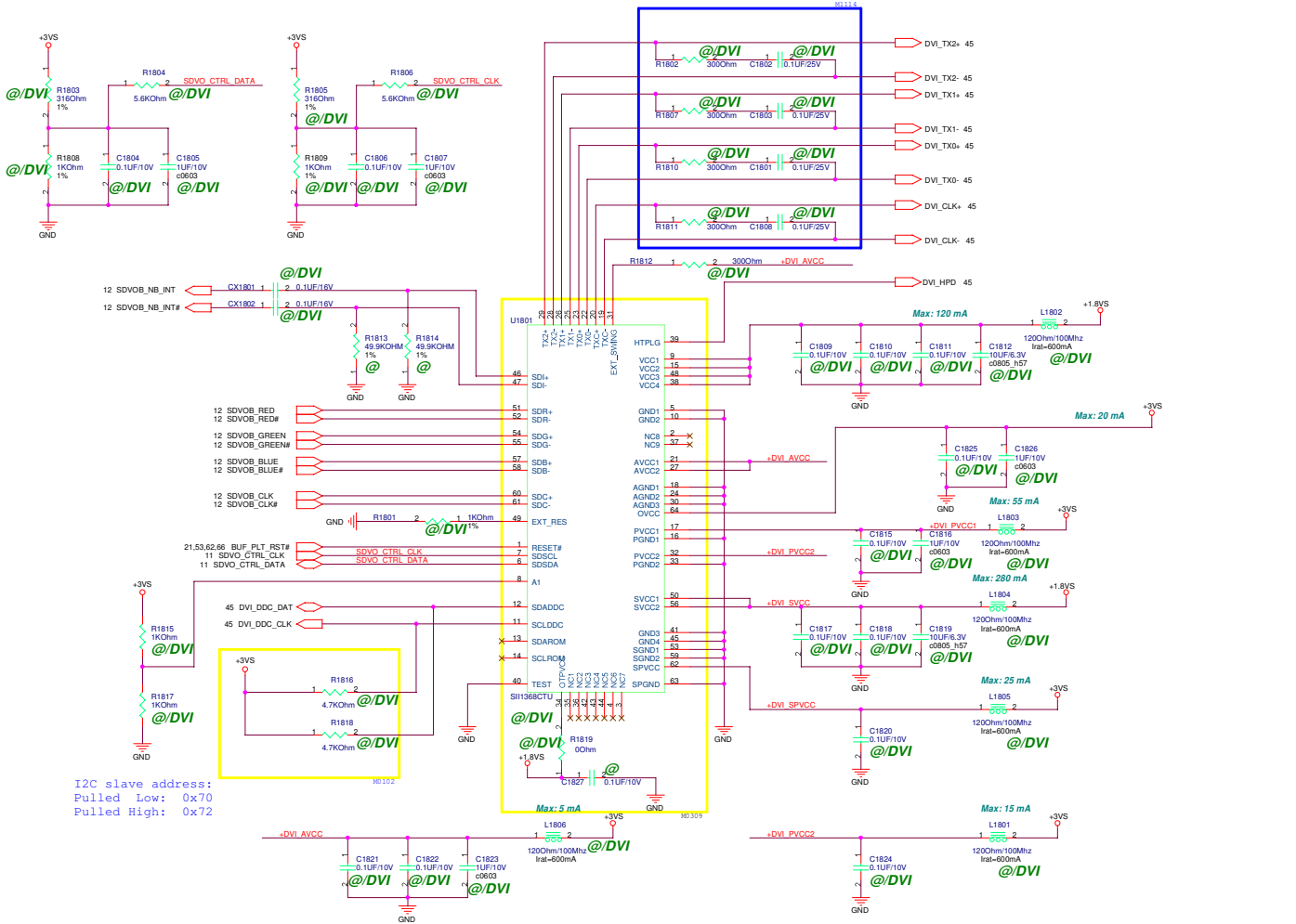
Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 17 of 94



<Core Design>

ASUSTeK COMPUTER INC	Title: Sil368 SDVO-DVI(HDCP)		
	Engineer: Amy_Peng		
Size: Custom	Project Name: X51L		Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 18 of 94		

<Core Design>

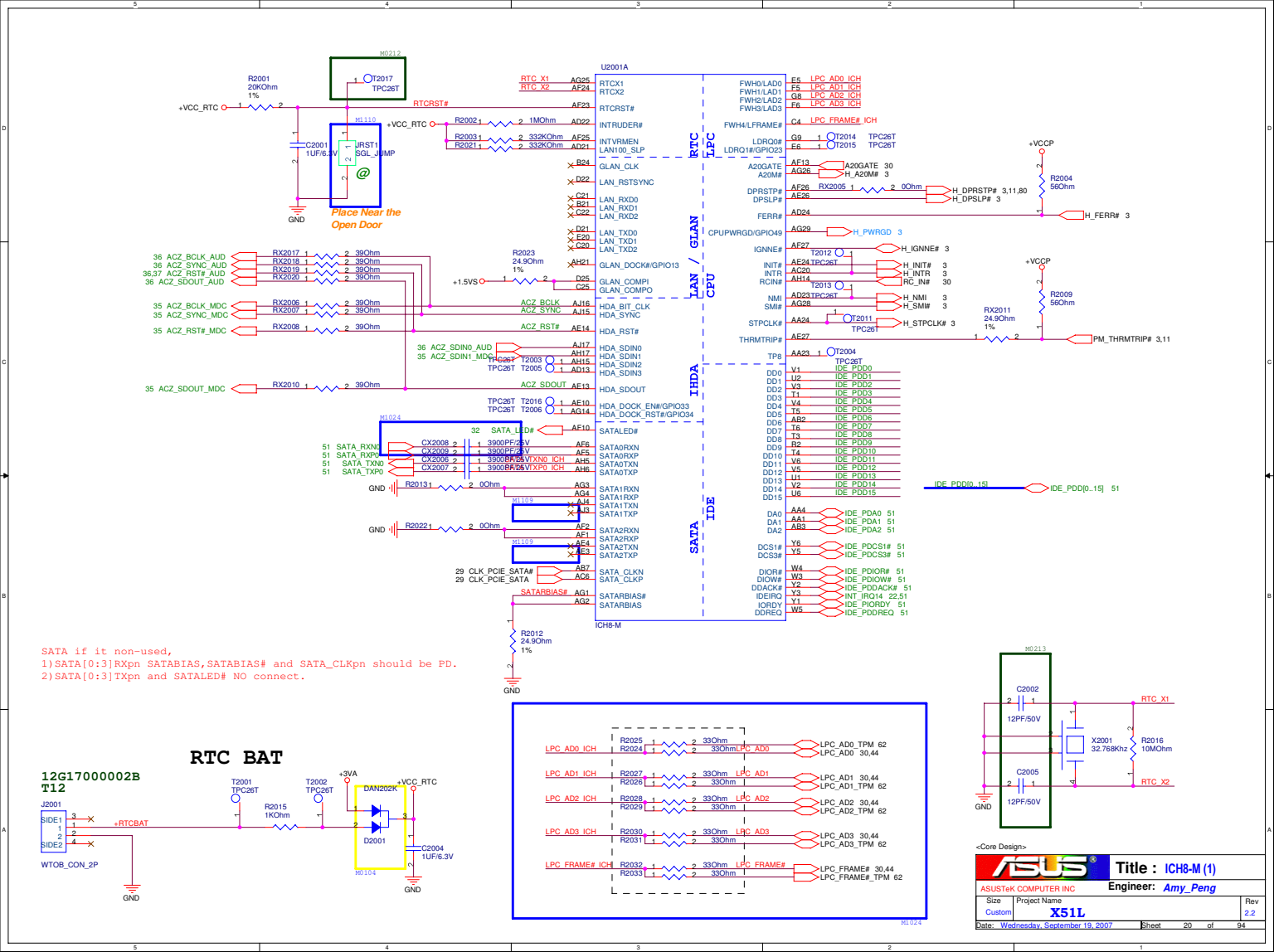
Title : NULL

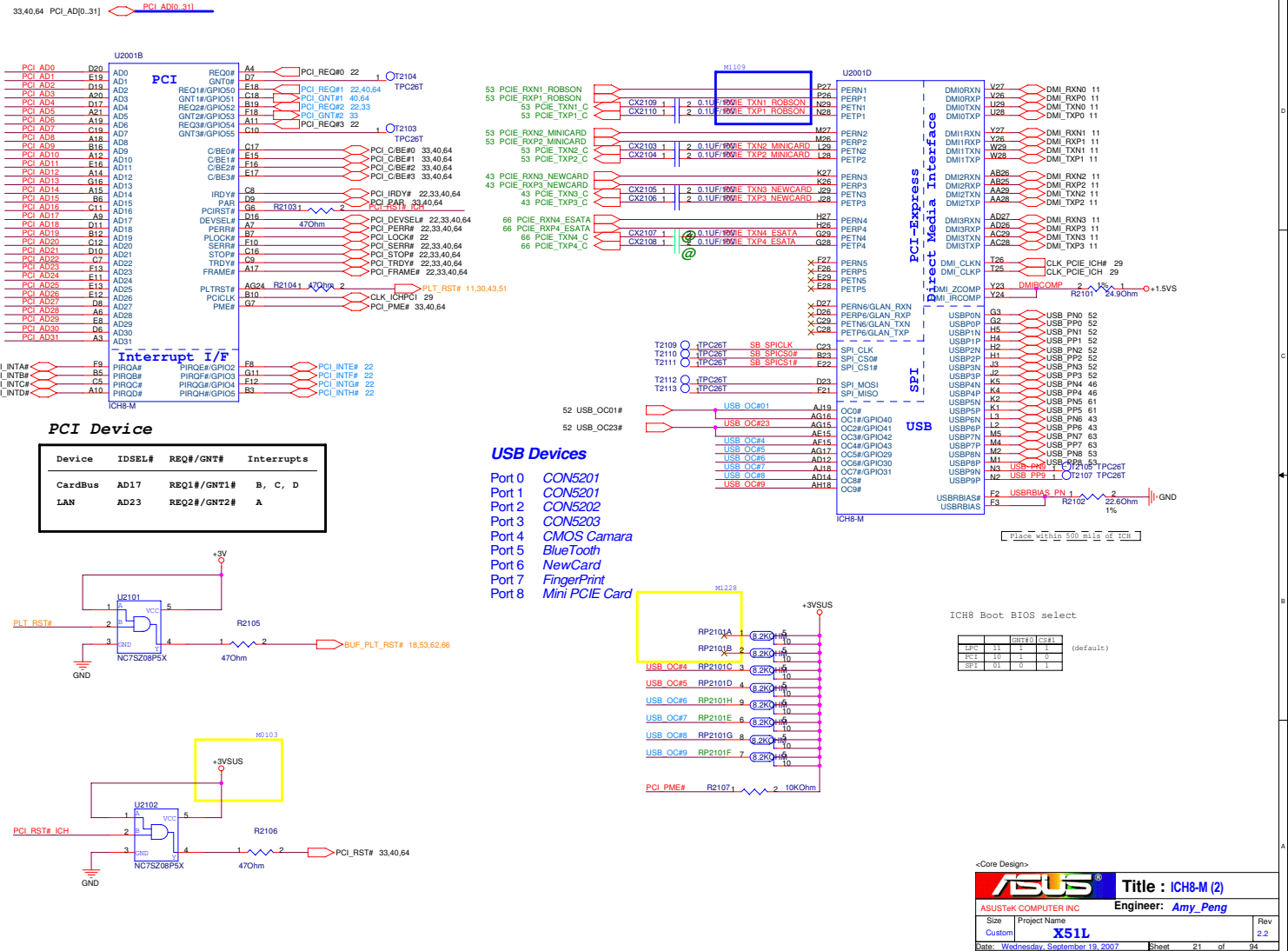
ASUSTeK COMPUTER INC

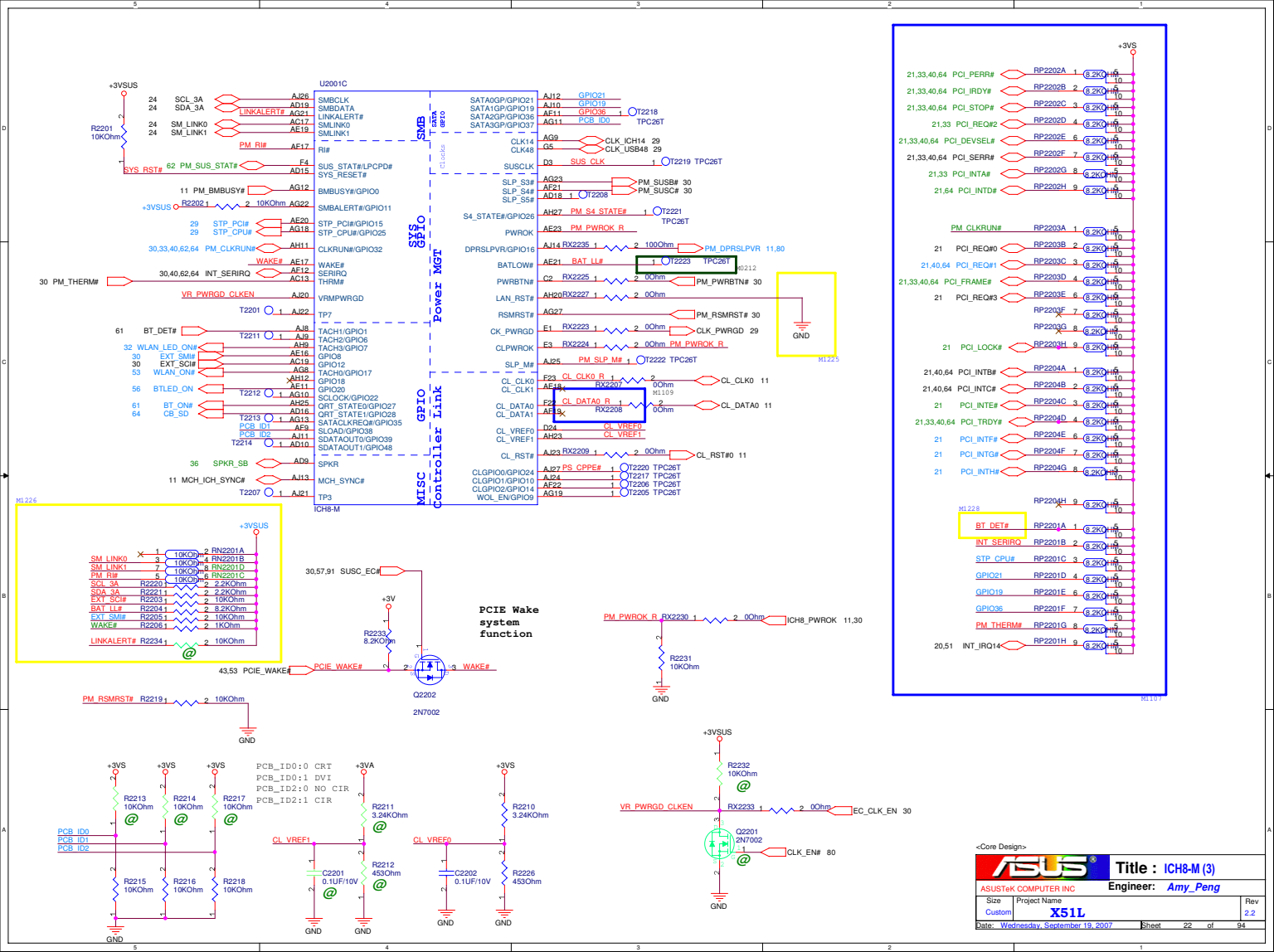
Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 19 of 94


U2001A
ICH8-M
RTC
LPC
GLAN
LAN / CPU
LHDA
IDE
SATA
RTC BAT
12G17000002B
T12
WTOB_CON_2P
Place Near the Open Door
SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.
<Core Design>
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: Amy_Peng
Size Custom
Project Name X51L
Rev 2.2
Date: Wednesday, September 19, 2007
Sheet 20 of 94


33,40,64 PCI_AD[0..31]
PCI_AD[0..31]
U2001B
PCI
PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25 PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31
REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
PCI_REQ#0 22
T2104 TPC26T
PCI_REQ#1 22,40,64
PCI_GNT#1 40,64
PCI_REQ#2 22,33
PCI_GNT#2 33
PCI_REQ#3 22
T2103 TPC26T
C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C/BE#0 33,40,64
PCI_C/BE#1 33,40,64
PCI_C/BE#2 33,40,64
PCI_C/BE#3 33,40,64
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PCI_IRDY# 22,33,40,64
PCI_PAR 33,40,64
PCI_RST# 33,41
R2103 1 47Ohm 2
PCI_DEVSEL# 22,33,40,64
PCI_PERR# 22,33,40,64
PCI_LOCK# 22
PCI_SERR# 22,33,40,64
PCI_STOP# 22,33,40,64
PCI_TRDY# 22,33,40,64
PCI_FRAME# 22,33,40,64
PLTRST# PCICLK PME#
AG24 R2104 1 47Ohm 2 PLT_RST# 11,30,43,51
CLK_ICHPCI 29
PCI_PME# 33,40,64
Interrupt I/F
PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PCI_INTA# 22,33
PCI_INTB# 22,40,64
PCI_INTC# 22,40,64
PCI_INTD# 22,64
PCI_INTE# 22
PCI_INTF# 22
PCI_INTG# 22
PCI_INTH# 22
ICH8-M
PCI Device
Device IDSEL# REQ#/GNT# Interrupts
CardBus AD17 REQ1#/GNT1# B, C, D
LAN AD23 REQ2#/GNT2# A
M1109
53 PCIE_RXN1_ROBSON
53 PCIE_RXP1_ROBSON
53 PCIE_TXN1_C
53 PCIE_TXP1_C
CX2109 1 2 0.1UF/10V PCIE_TXN1_ROBSON
CX2110 1 2 0.1UF/10V PCIE_TXP1_ROBSON
53 PCIE_RXN2_MINICARD
53 PCIE_RXP2_MINICARD
53 PCIE_TXN2_C
53 PCIE_TXP2_C
CX2103 1 2 0.1UF/10V PCIE_TXN2_MINICARD
CX2104 1 2 0.1UF/10V PCIE_TXP2_MINICARD
43 PCIE_RXN3_NEWCARD
43 PCIE_RXP3_NEWCARD
43 PCIE_TXN3_C
43 PCIE_TXP3_C
CX2105 1 2 0.1UF/10V PCIE_TXN3_NEWCARD
CX2106 1 2 0.1UF/10V PCIE_TXP3_NEWCARD
66 PCIE_RXN4_ESATA
66 PCIE_RXP4_ESATA
66 PCIE_TXN4_C
66 PCIE_TXP4_C
CX2107 1 2 0.1UF/10V PCIE_TXN4_ESATA
CX2108 1 2 0.1UF/10V PCIE_TXP4_ESATA
@
U2001D
PCI-Express Direct Media Interface
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP
DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_RXN0 11
DMI_RXP0 11
DMI_TXN0 11
DMI_TXP0 11
DMI_RXN1 11
DMI_RXP1 11
DMI_TXN1 11
DMI_TXP1 11
DMI_RXN2 11
DMI_RXP2 11
DMI_TXN2 11
DMI_TXP2 11
DMI_RXN3 11
DMI_RXP3 11
DMI_TXN3 11
DMI_TXP3 11
DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# 29
CLK_PCIE_ICH 29
DMI_ZCOMP DMI_IRCOMP
DMICOMP
R2101 24.9Ohm 1%
+1.5VS
SPI
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO
T2109 T2110 T2111 TPC26T SB_SPICLK SB_SPICS0# SB_SPICS1#
T2112 T2113 TPC26T
USB
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P
USB_PN9 USB_PP9 T2105 T2107 TPC26T
USBRBIAS USBRBIAS_PN
R2102 22.6Ohm 1%
GND
ICH8-M
Place within 500 mils of ICH
52 USB_OC01#
52 USB_OC23#
USB_OC#01 USB_OC#23 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
USB Devices
Port 0 CON5201
Port 1 CON5201
Port 2 CON5202
Port 3 CON5203
Port 4 CMOS Camara
Port 5 BlueTooth
Port 6 NewCard
Port 7 FingerPrint
Port 8 Mini PCIE Card
+3V
U2101
PLT_RST#
R2105
BUF_PLT_RST# 18,53,62,66
NC7SZ08P5X
47Ohm
GND
M1103
+3VSUS
U2102
PCI_RST# ICH
R2106
PCI_RST# 33,40,64
NC7SZ08P5X
47Ohm
GND
M1228
+3VSUS
RP2101A RP2101B RP2101C RP2101D RP2101E RP2101F RP2101G
8.2KOHM
USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9
PCI_PME# R2107 10KOhm
ICH8 Boot BIOS select
GNT#0 CS#1
LPC 11 1 1
PCI 10 1 0
SPI 01 0 1
(default)
<Core Design>
ASUSTeK COMPUTER INC
Title : ICH8-M (2)
Engineer: Amy_Peng
Size Custom
Project Name X51L
Rev 2.2
Date: Wednesday, September 19, 2007
Sheet 21 of 94


U2001C
ICH8-M
SMB
DATA
GPIO
CLOCKS
SYS
GPIO
Power MGT
GPIO
Controller Link
MISC
+3VSUS
+3V
+3VS
+3VA
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_ICH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
GPIO21
GPIO19
GPIO36
PCB_ID0
CLK_ICH14
CLK_USB48
SUS_CLK
PM_SUSB#
PM_SUSC#
PM_S4_STATE#
PM_PWROK_R
PM_DPRSLPVR
BAT_LL#
PM_PWRBTN#
PM_RSMRST#
CLK_PWRGD
PM_PWROK_R
PM_SLP_M#
CL_CLK0
CL_DATA0
CL_VREF0
CL_VREF1
CL_RST#0
PS_CPPE#
T2220 TPC26T
T2217 TPC26T
T2206 TPC26T
T2205 TPC26T
T2218 TPC26T
T2219 TPC26T
T2208 TPC26T
T2221 TPC26T
T2222 TPC26T
T2223 TPC26T
RX2207
RX2208
RX2209
RX2220
RX2221
RX2222
RX2223
RX2224
RX2225
RX2227
RX2235
M1212
M1225
M1109
M1226
M1228
M1107
SCL_3A
SDA_3A
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
PM_SUS_STAT#
SYS_RST#
PM_BMBUSY#
STP_PCI#
STP_CPU#
PM_CLKRUN#
WAKE#
INT_SERIRQ
PM_THERM#
VR_PWRGD_CLKEN
BT_DET#
WLAN_LED_ON#
EXT_SMI#
EXT_SCI#
WLAN_ON#
BTLED_ON
BT_ON#
CB_SD
PCB_ID1
PCB_ID2
SPKR_SB
MCH_ICH_SYNC#
SUSC_EC#
PCIE_WAKE#
WAKE#
Q2202
2N7002
PCIE Wake system function
PM_PWROK_R
ICH8_PWROK
PM_RSMRST#
PCB_ID0:0 CRT
PCB_ID0:1 DVI
PCB_ID1:0 NO CIR
PCB_ID1:1 CIR
CL_VREF1
CL_VREF0
VR_PWRGD_CLKEN
EC_CLK_EN
CLK_EN#
Q2201
2N7002
RP2202A
RP2202B
RP2202C
RP2202D
RP2202E
RP2202F
RP2202G
RP2202H
RP2203A
RP2203B
RP2203C
RP2203D
RP2203E
RP2203F
RP2203G
RP2203H
RP2204A
RP2204B
RP2204C
RP2204D
RP2204E
RP2204F
RP2204G
RP2204H
RP2201A
RP2201B
RP2201C
RP2201D
RP2201E
RP2201F
RP2201G
RP2201H
PCI_PERR#
PCI_IRDY#
PCI_STOP#
PCI_REQ#2
PCI_DEVSEL#
PCI_SERR#
PCI_INTA#
PCI_INTD#
PCI_REQ#0
PCI_REQ#1
PCI_FRAME#
PCI_REQ#3
PCI_LOCK#
PCI_INTB#
PCI_INTC#
PCI_INTE#
PCI_TRDY#
PCI_INTF#
PCI_INTG#
PCI_INTH#
INT_IRQ14
GND
<Core Design>
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: Amy_Peng
Size: Custom
Project Name: X51L
Rev: 2.2
Date: Wednesday, September 19, 2007
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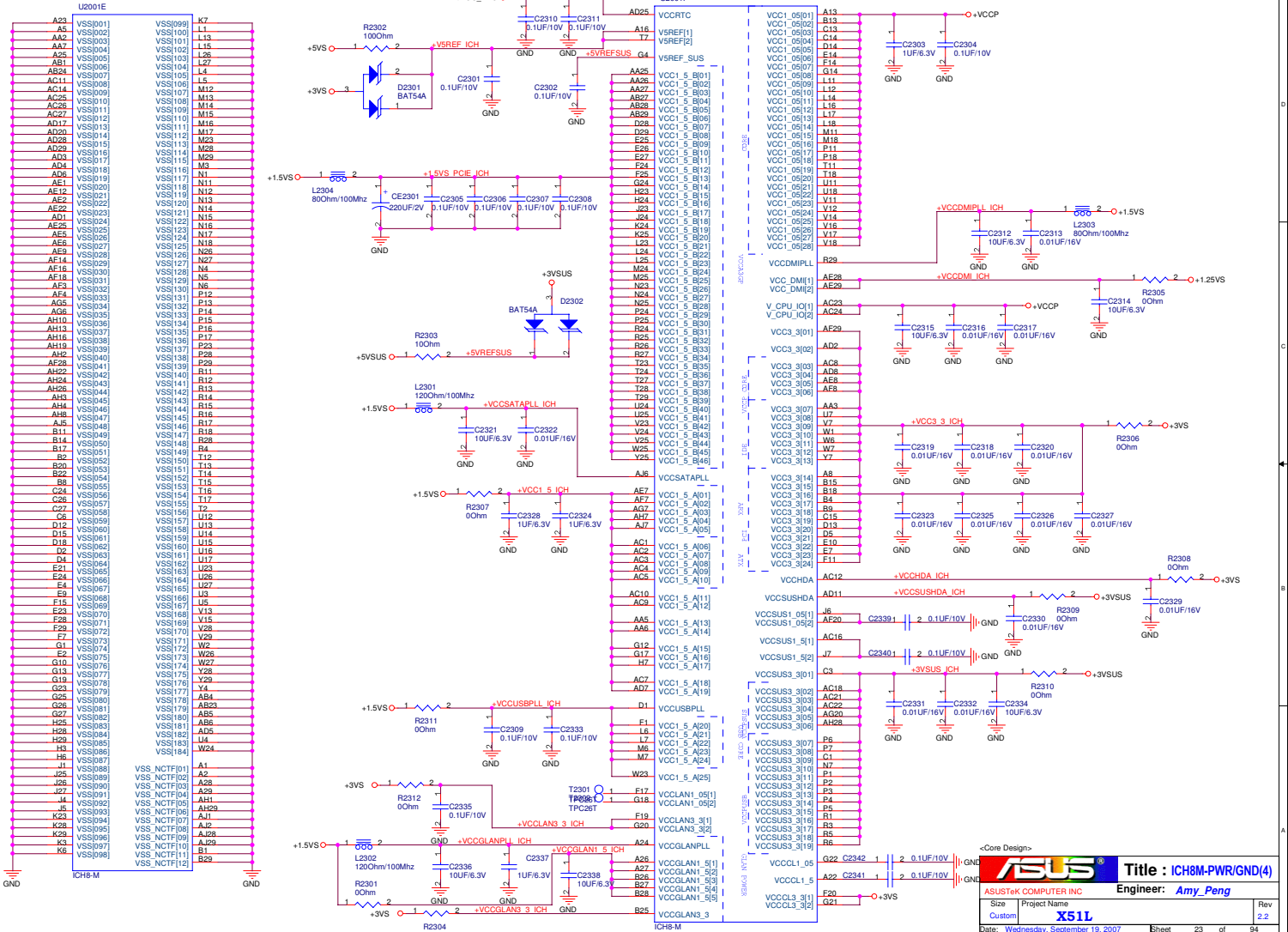
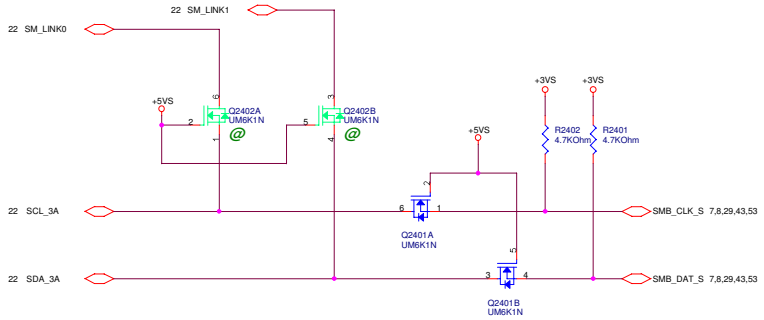

U2001E
ICH8-M
U2001F
ICH8-M
+VCC_RTC
R2302 100Ohm
+5VS
+3VS
D2301 BAT54A
+V5REF_ICH
+5VREFSUS
C2301 0.1UF/10V
C2302 0.1UF/10V
C2310 0.1UF/10V
C2311 0.1UF/10V
+1.5VS
L2304 80Ohm/100Mhz
CE2301 220UF/2V
C2305 0.1UF/10V
C2306 0.1UF/10V
C2307 0.1UF/10V
C2308 0.1UF/10V
+1.5V_PCIE_ICH
+3VSUS
D2302 BAT54A
R2303 10Ohm
+5VSUS
L2301 120Ohm/100Mhz
+VCCSATAPLL_ICH
C2321 10UF/6.3V
C2322 0.01UF/16V
R2307 0Ohm
+VCC1_5_ICH
C2328 1UF/6.3V
C2324 1UF/6.3V
R2311 0Ohm
+VCCUSBPLL_ICH
C2309 0.1UF/10V
C2333 0.1UF/10V
R2312 0Ohm
C2335 0.1UF/10V
+VCCLAN3_3_ICH
L2302 120Ohm/100Mhz
+VCCGLANPLL_ICH
C2336 10UF/6.3V
C2337 1UF/6.3V
+VCCGLAN1_5_ICH
C2338 10UF/6.3V
R2301 0Ohm
+VCCGLAN3_3_ICH
R2304 0Ohm
T2301 TP26T
+VCCP
C2303 1UF/6.3V
C2304 0.1UF/10V
+VCCDMIPLL_ICH
C2312 10UF/6.3V
C2313 0.01UF/16V
L2303 80Ohm/100Mhz
+VCCDMI_ICH
C2314 10UF/6.3V
R2305 0Ohm
+1.25VS
C2315 10UF/6.3V
C2316 0.01UF/16V
C2317 0.01UF/16V
+VCC3_3_ICH
C2319 0.01UF/16V
C2318 0.01UF/16V
C2320 0.01UF/16V
R2306 0Ohm
+3VS
C2323 0.01UF/16V
C2325 0.01UF/16V
C2326 0.01UF/16V
C2327 0.01UF/16V
+VCCHDA_ICH
R2308 0Ohm
+VCCSUSHDA_ICH
C2329 0.01UF/16V
R2309 0Ohm
C2330 0.01UF/16V
+3VSUS
C23391 0.1UF/10V
C23401 0.1UF/10V
+3VSUS_ICH
C2331 0.01UF/16V
C2332 0.01UF/16V
C2334 10UF/6.3V
R2310 0Ohm
C2342 0.1UF/10V
C2341 0.1UF/10V
GND

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

ICH8-M

ICH8-M



<Core Design>

ASUSTeK COMPUTER INC

Title : ICH8M-Other

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 24 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 25 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 26 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 27 of 94

<Core Design>

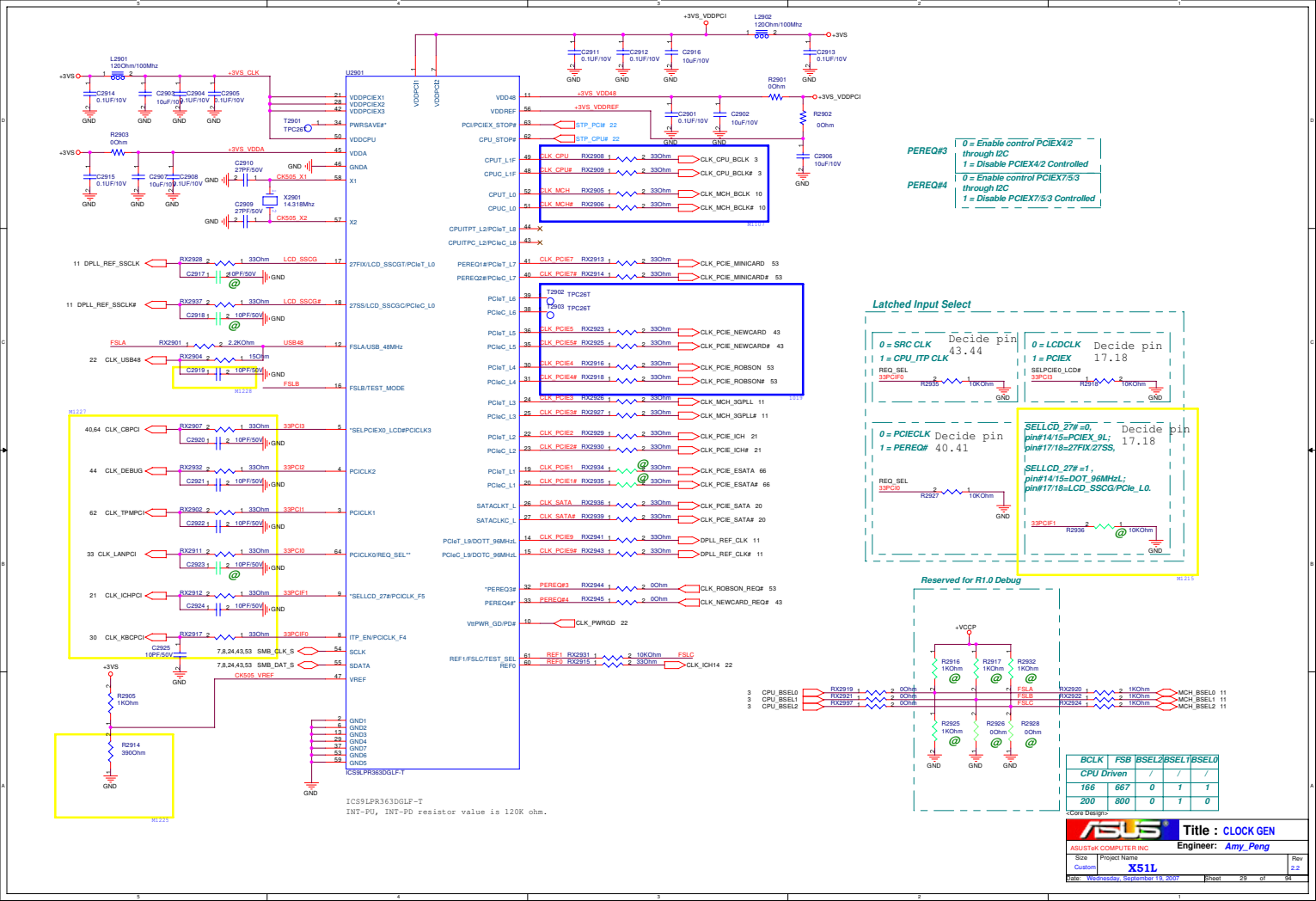
Title : NULL

ASUSTeK COMPUTER INC

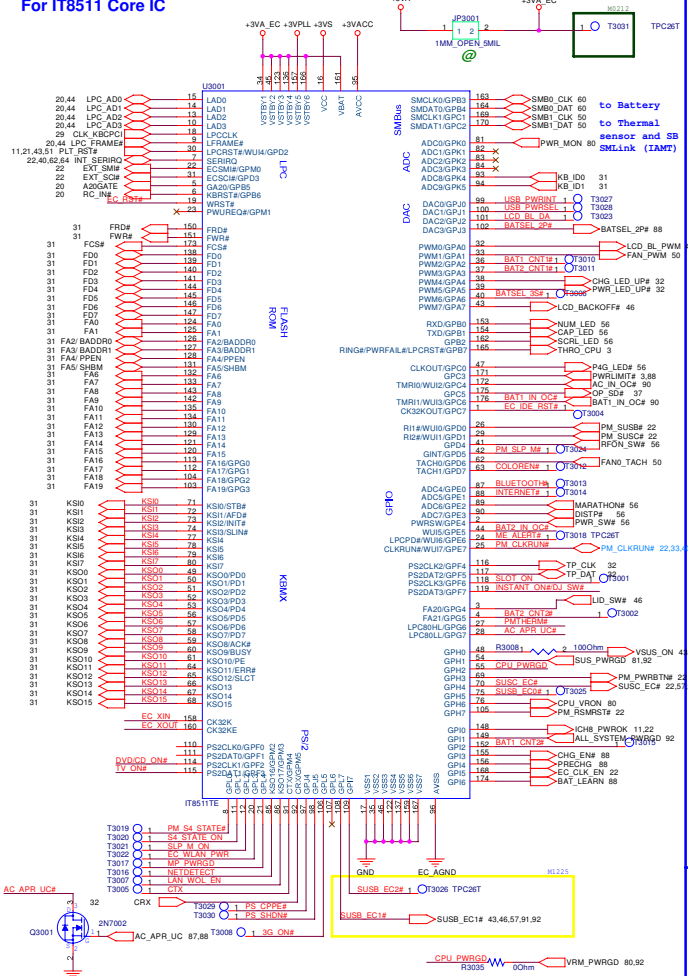
Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

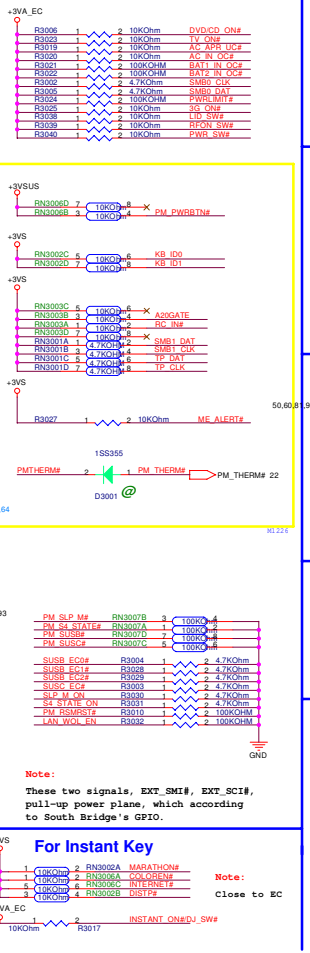
Date: Wednesday, September 19, 2007 Sheet 28 of 94


U2901
ICS9LPR363DGLF-T
INT-PU, INT-PD resistor value is 120K ohm.
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
CPU Driven / / /
166 667 0 1 1
200 800 0 1 0
Title : CLOCK GEN
Engineer: Amy_Peng
ASUSTeK COMPUTER INC
X51L
Wednesday, September 19, 2007
Sheet 29 of 94

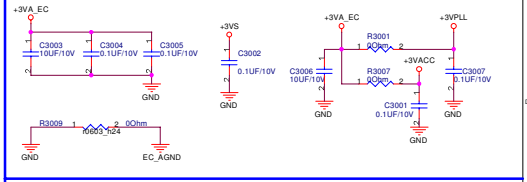
For IT8511 Core IC



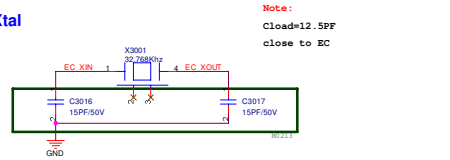
For Pull-up/Pull-down



For IT8511 Power

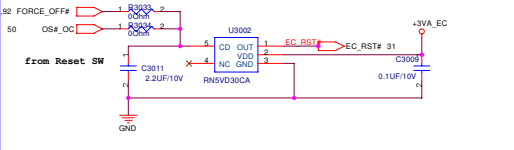


For Xtal



Note:
Cload=12.5PF
close to EC

For EC reset



Note:

For EC Hardware Strap

I/O Base Address	Share Memory	PP Enable
Note:	Note:	Note:
It can be programmable by EC fireware	It can be programmable by EC fireware	Default Internal Pull-Low

For Instant Key

Note:
These two signals, EXT_SMI#, EXT_SCI#, pull-up power plane, which according to South Bridge's GPIO.

For Intel IAMT pin name

ME_ALERT#	EC_WLAN_PWR
PM_S4_STATE#	MP_PWRGD
S4_STATE_ON	NETDETECT
PM_SLP_M#	LAN_WOL_EN
SLP_M_ON	
WLAN_SW#	

<Core Design>

ASUSTeK COMPUTER INC

Title : EC-ITE8511 (2)

Engineer: Amy_Peng

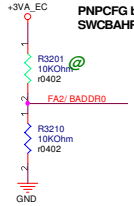
Size	Project Name	Rev
Custom	X51L	2.2

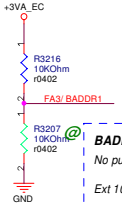
Date: Wednesday, September 19, 2007 Sheet 30 of 94

EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

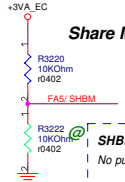




BADDR[1:0]

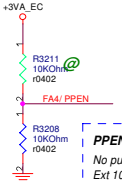
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*



PPEN

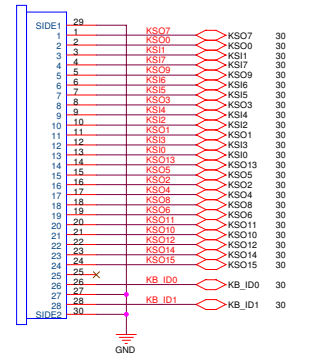
No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

Keyboard Conn.

J3101

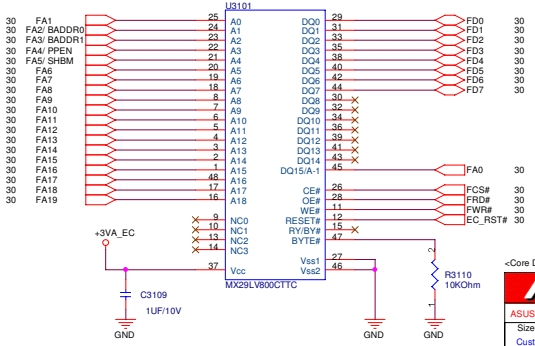
FPC_CON_28P

P/N: 12G182102805 Gold/0608



For 8M bits ISA ROM

8M TSOP



Note:

If you use 8M bits ROM, you need to connect FA19 to EC side.

<Core Design>

ASUSTeK COMPUTER INC

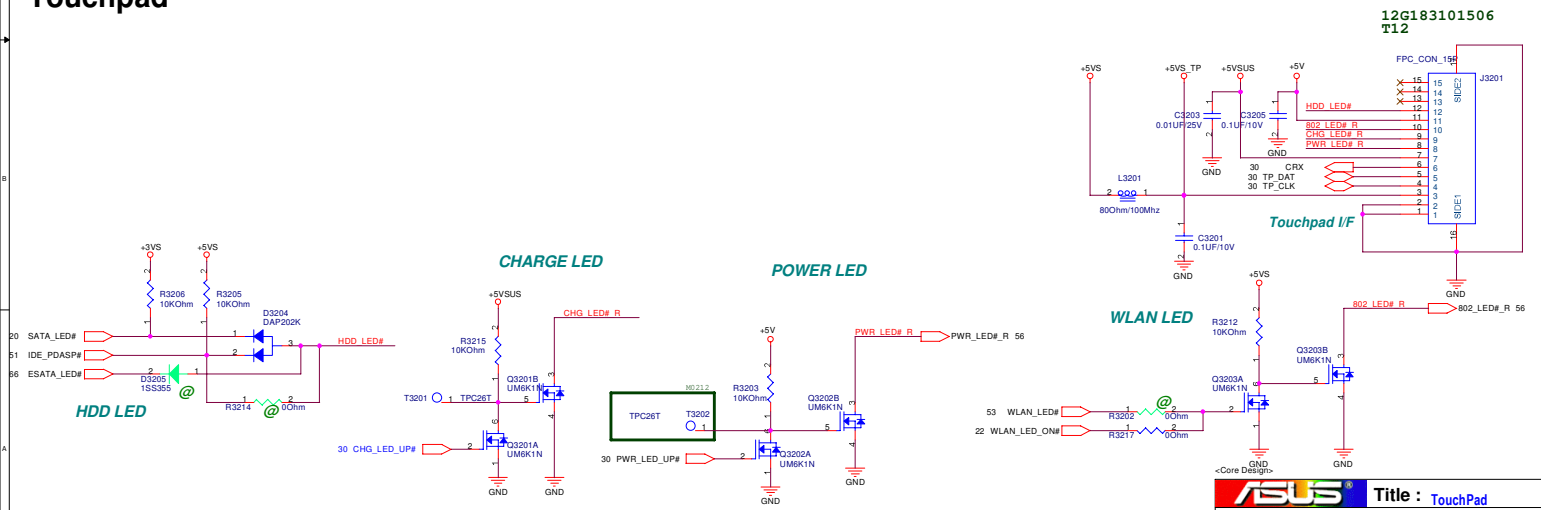
Title : EC-ITE8511(2)

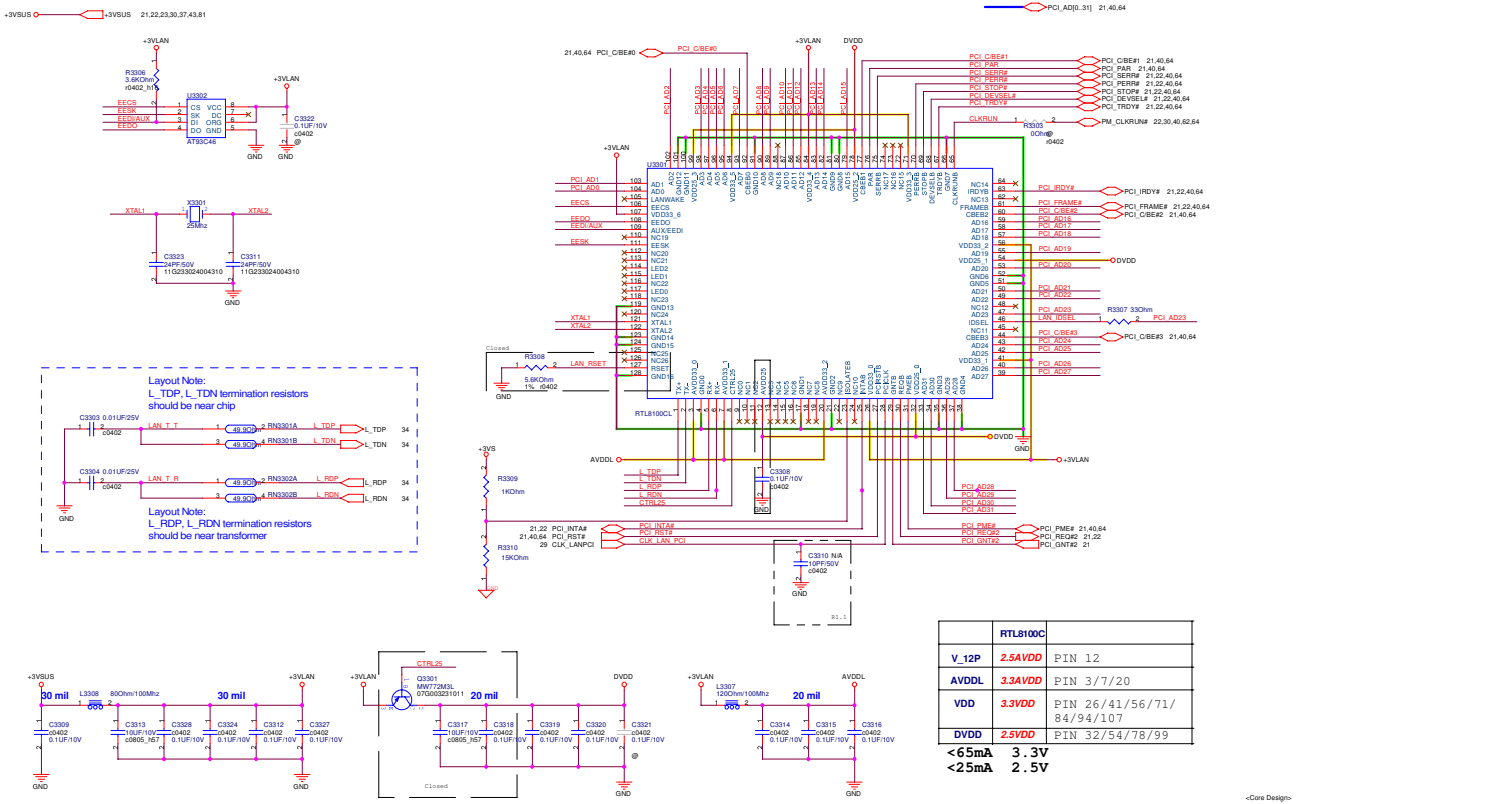
Engineer: *Amy_Peng*

Size	Project Name	Rev
Custom	**X51L**	2.2

Date: Wednesday, September 19, 2007 Sheet 31 of 94

Touchpad


12G183101506
T12
+3VS
+5VS
R3206
10KOhm
R3205
10KOhm
D3204
DAP202K
20 SATA_LED#
51 IDE_PDASP#
86 ESATA_LED#
HDD_LED#
D3205
1SS355
R3214
0Ohm
HDD LED
CHARGE LED
+5VSUS
R3215
10KOhm
CHG_LED# R
Q3201B
UM6K1N
T3201
TPC26T
30 CHG_LED_UP#
Q3201A
UM6K1N
GND
POWER LED
+5V
R3203
10KOhm
PWR_LED# R
PWR_LED#_R 56
Q3202B
UM6K1N
TPC26T
T3202
30 PWR_LED_UP#
Q3202A
UM6K1N
+5VS
+5VS_TP
+5VSUS
+5V
C3203
0.01UF/25V
C3205
0.1UF/10V
HDD_LED#
802_LED# R
CHG_LED# R
PWR_LED# R
FPC_CON_15P
J3201
SIDE2
SIDE1
30 CRX
30 TP_DAT
30 TP_CLK
L3201
80Ohm/100Mhz
C3201
0.1UF/10V
Touchpad I/F
WLAN LED
R3212
10KOhm
Q3203B
UM6K1N
Q3203A
UM6K1N
802_LED# R
802_LED#_R 56
53 WLAN_LED#
22 WLAN_LED_ON#
R3202
0Ohm
R3217
0Ohm
<Core Design>
Title : TouchPad
Engineer: Amy_Peng
ASUSTeK COMPUTER INC
Size A3
Project Name X51L
Rev 2.2
Date: Wednesday, September 19, 2007
Sheet 32 of 94

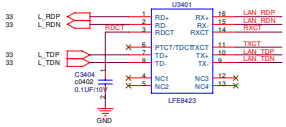


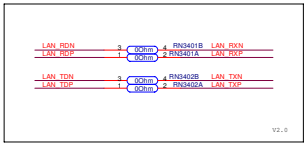
	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

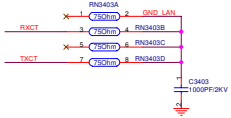
<65mA 3.3V
<25mA 2.5V

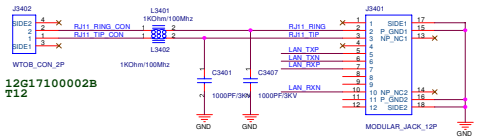
<Core Design>

ASUSTeK COMPUTER INC	Title : LAN_RTL8100CL	
	Engineer: Amy_Peng	
Size: C	Project Name: X51L	Rev: 2.0
Date: Wednesday, September 19, 2007	Sheet 33 of 63	

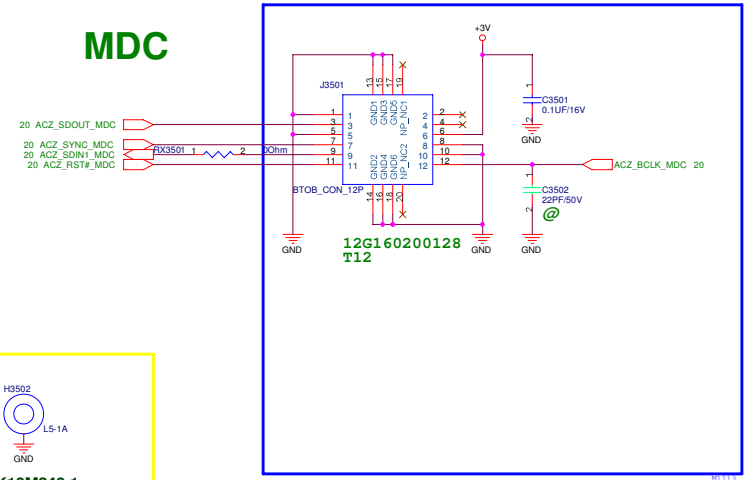

U3401
33 L_RDP
33 L_RDN
RDCT
RD+
RD-
RDCT
RX+
RX-
RXCT
LAN_RDP
LAN_RDN
RXCT
33 L_TDP
33 L_TDN
PTCT/TDCT
TD+
TD-
TX+
TX-
TXCT
LAN_TDP
LAN_TDN
C3404
c0402
0.1UF/10V
NC1
NC2
NC3
NC4
LFE8423
GND

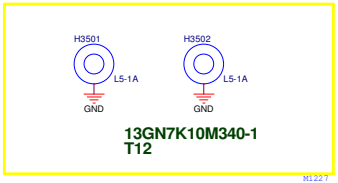

LAN_RDN
LAN_RDP
0ohm
RN3401B
RN3401A
LAN_RXN
LAN_RXP
LAN_TDN
LAN_TDP
RN3402B
RN3402A
LAN_TXN
LAN_TXP
V2.0


RN3403A
750hm
GND_LAN
RXCT
RN3403B
RN3403C
TXCT
RN3403D
C3403
1000PF/2KV


J3402
SIDE2
SIDE1
RJ11_RING_CON
RJ11_TIP_CON
WTOB_CON_2P
L3401
1KOhm/100Mhz
L3402
1KOhm/100Mhz
C3401
C3407
1000PF/3KV
GND
RJ11_RING
RJ11_TIP
LAN_TXP
LAN_TXN
LAN_RXP
LAN_RXN
J3401
SIDE1
P_GND1
NP_NC1
NP_NC2
P_GND2
SIDE2
MODULAR_JACK_12P
12G17100002B
T12
12G142111120
T12

MDC





<Core Design>

Title : MDC

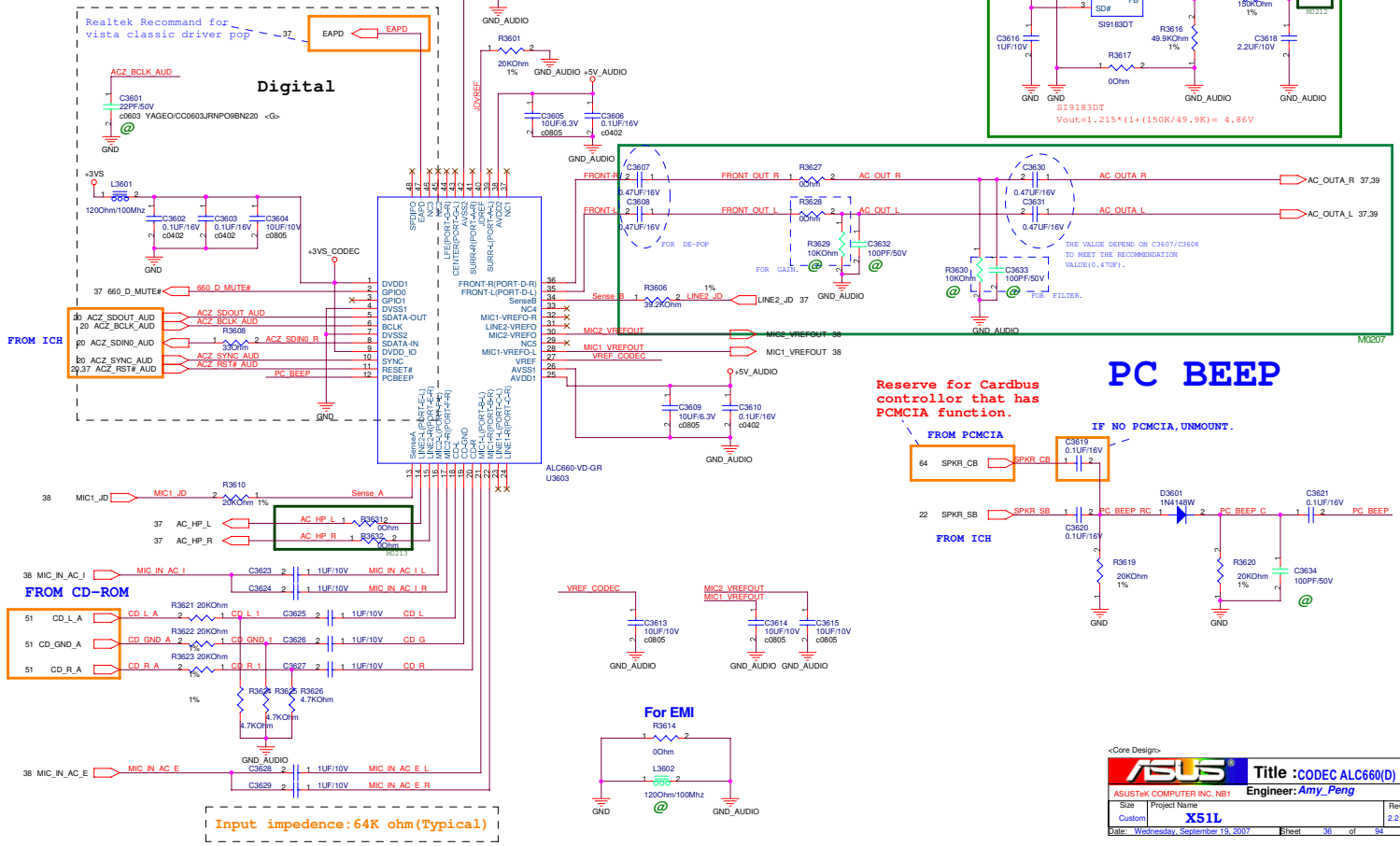
ASUSTeK COMPUTER INC. NB

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 35 of 94

CODEC ALC660 REV:D



AUDIO POWER

PC BEEP

<Core Design>

Title : CODEC ALC660(D)

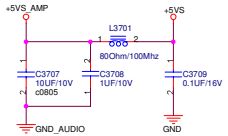
ASUSTeK COMPUTER INC. NB1

Engineer: Amy_Peng

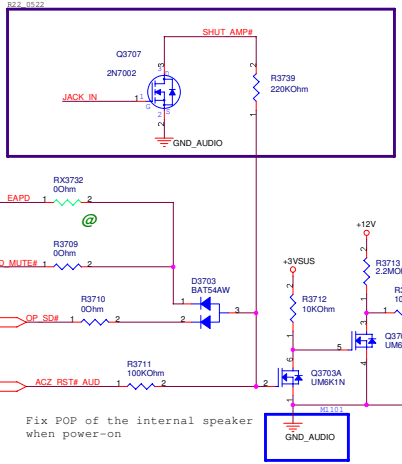
Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 36 of 94

AMP POWER

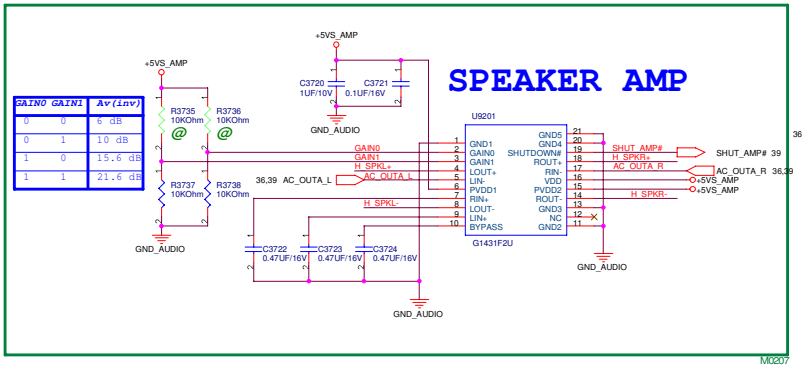


MUTE CONTROL

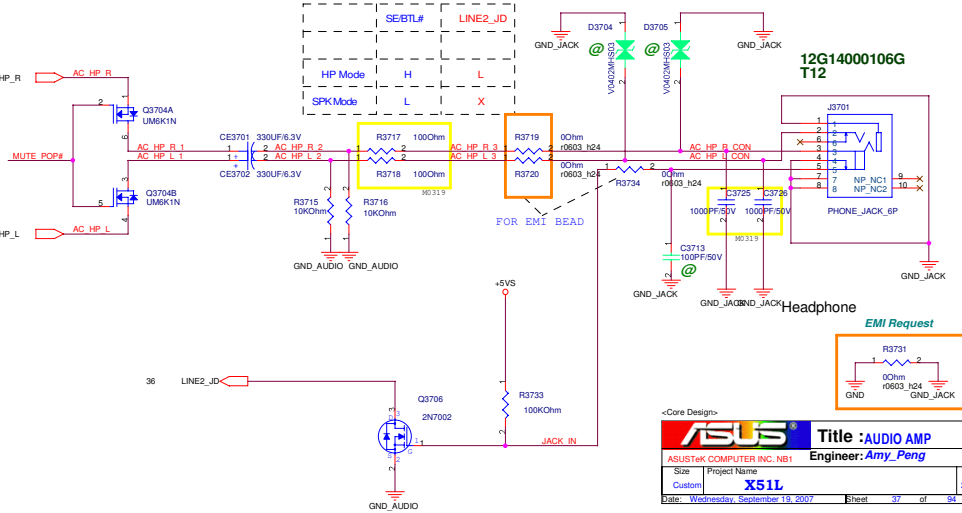


SPEAKER AMP

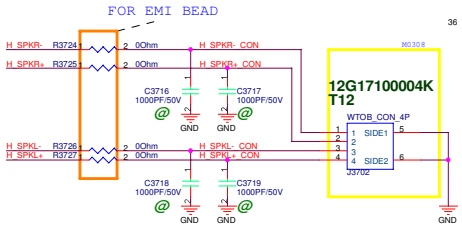
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



HP CONN

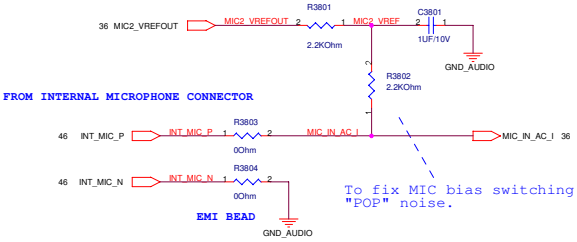


SPEAKER CONNECTOR

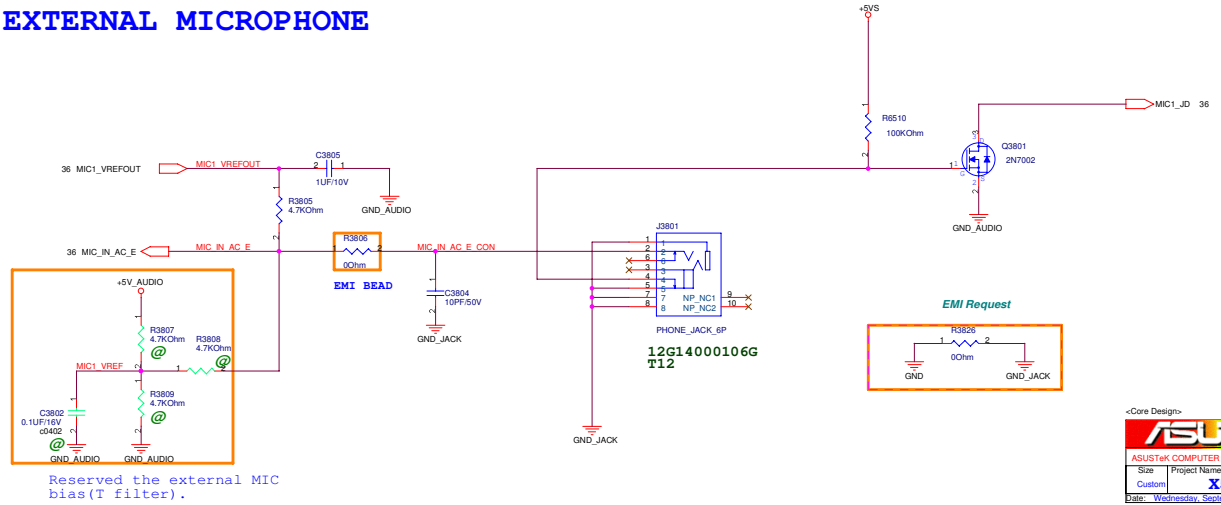


ASUSTeK COMPUTER INC. NB1	Title : AUDIO AMP	
	Engineer: Amy_Peng	
Size: Custom	Project Name: X51L	Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 37 of 94	

INTERNAL MICROPHONE



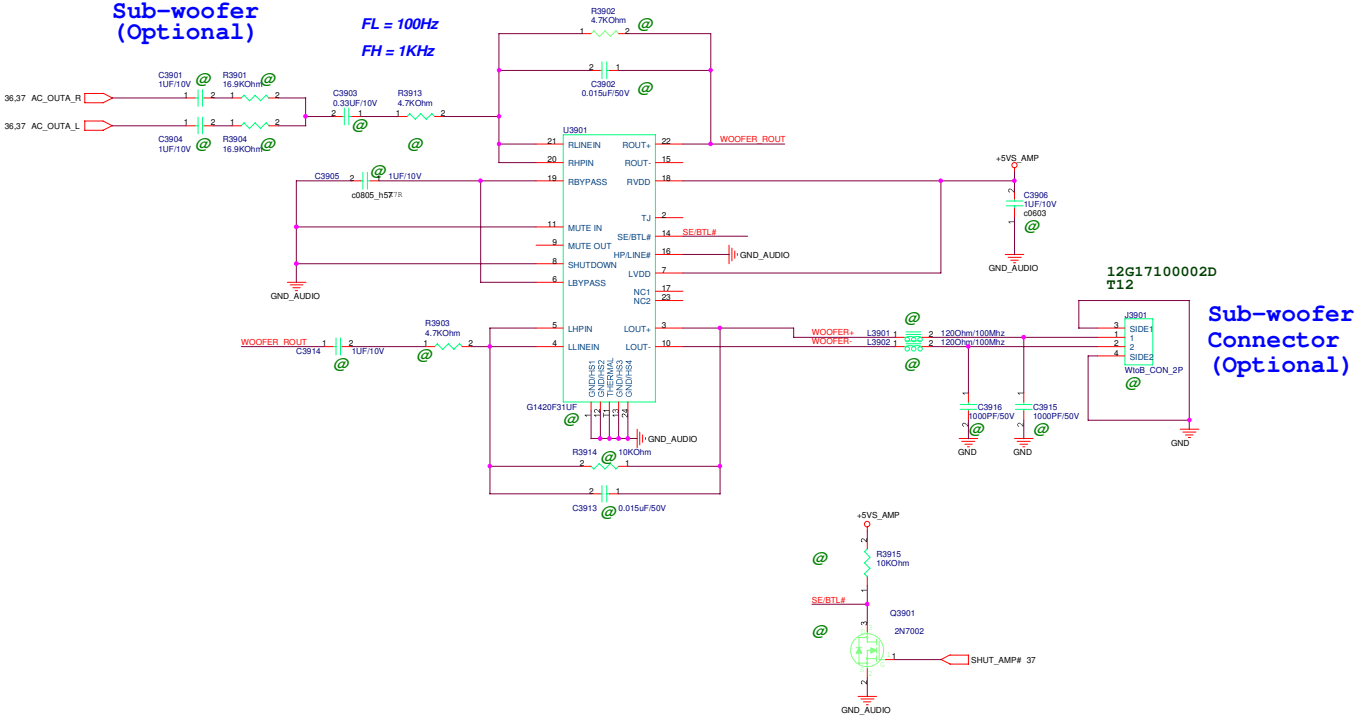
EXTERNAL MICROPHONE



Sub-woofer (Optional)

FL = 100Hz

FH = 1KHz

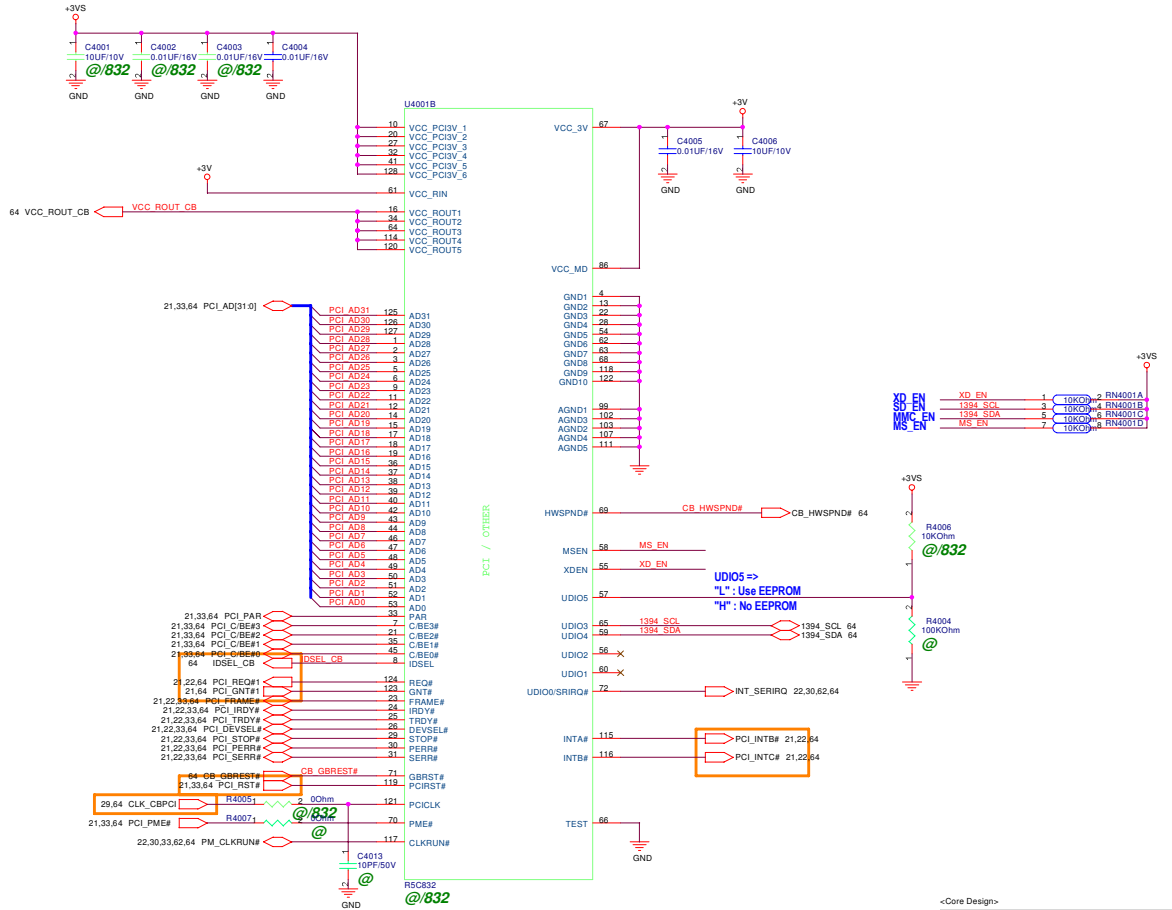


12G17100002D T12

Sub-woofer Connector (Optional)

<Core Design>

ASUSTek COMPUTER INC NPI	Title : Sub-Woofer		
	Engineer: Amy_Peng		
Size: Custom	Project Name: X51L		Rev: 2.2
	P/N: <OrgAddr2>		
Date: Wednesday, September 19, 2007	Sheet 39 of 94		



<Core Design>

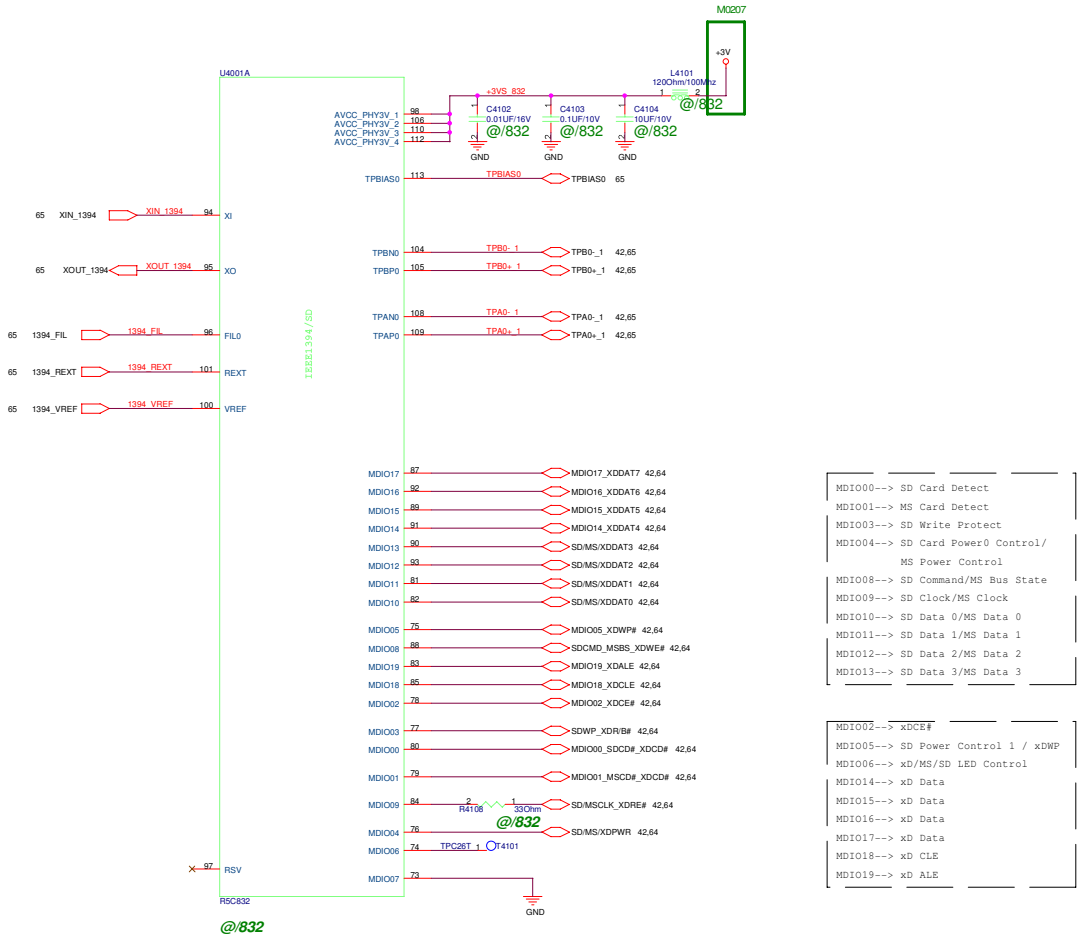
ASUSTeK COMPUTER INC

Title: CARDBUS R5C832 (1)

Engineer: Miller Liu

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 40 of 94




```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

<Core Design>

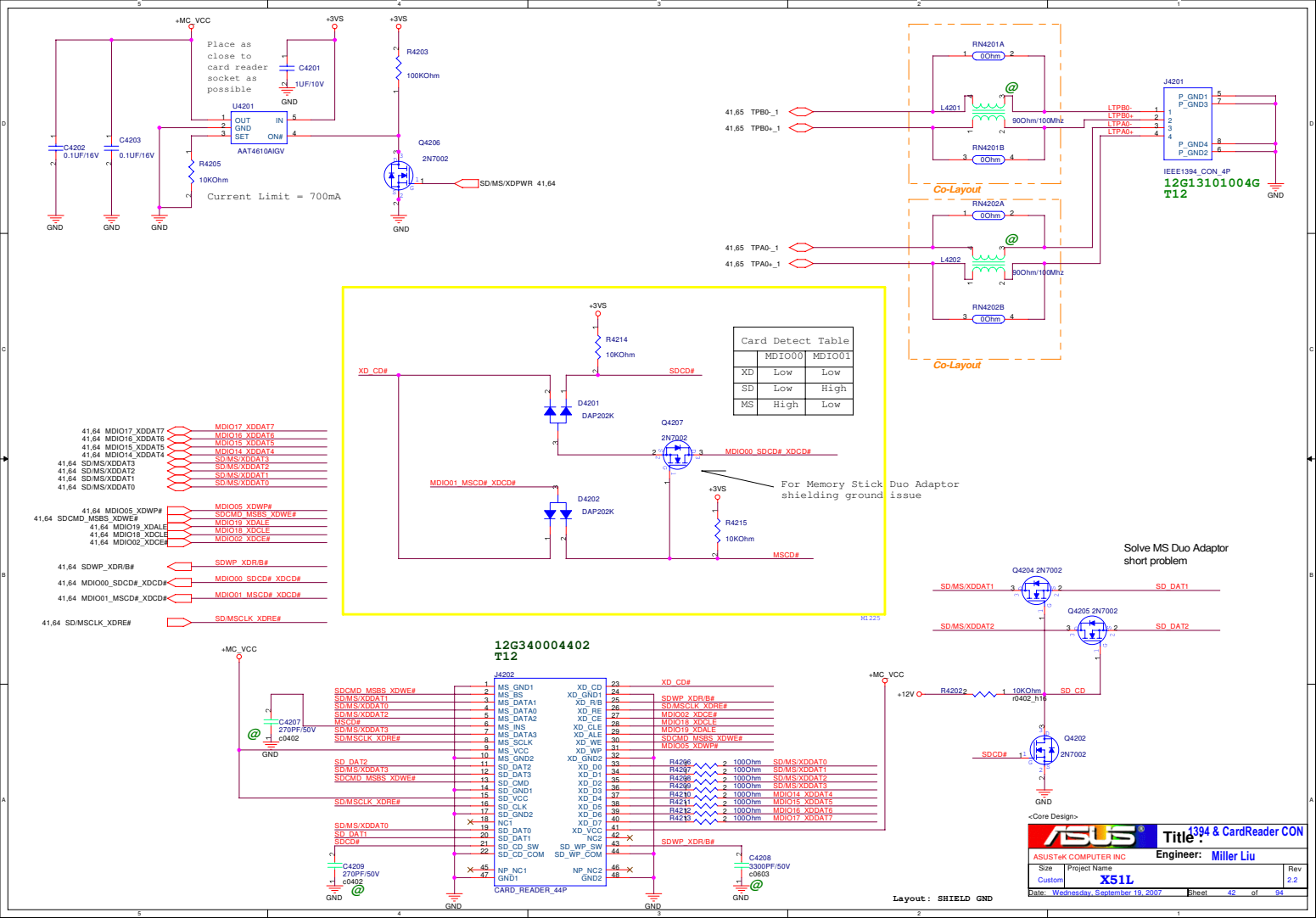
ASUSTeK COMPUTER INC

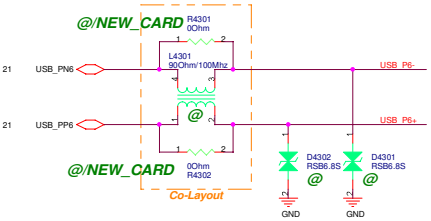
Title : CARDBUS R5C832 (2)

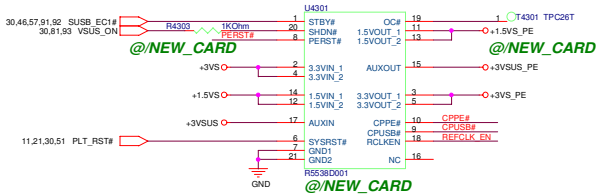
Engineer: Miller Liu

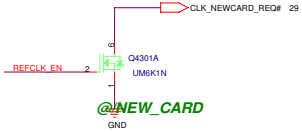
Size	Project Name	Rev
Custom	X51L	2.2

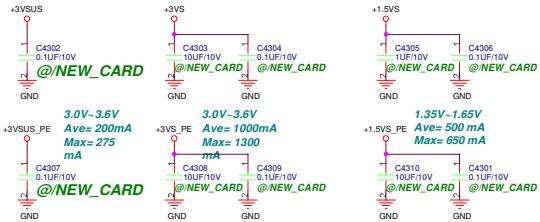
Date: Wednesday, September 19, 2007 Sheet 41 of 94


+MC_VCC
+3VS
+3VS
Place as close to card reader socket as possible
C4201
1UF/10V
GND
R4203
100KOhm
U4201
OUT
GND
SET
IN
ON#
AAT4610AIGV
C4202
0.1UF/16V
C4203
0.1UF/16V
R4205
10KOhm
Current Limit = 700mA
Q4206
2N7002
SD/MS/XDPWR 41,64
GND
GND
GND
GND
RN4201A
0Ohm
L4201
90Ohm/100Mhz
RN4201B
0Ohm
41,65 TPB0-_1
41,65 TPB0+_1
LTPB0-
LTPB0+
LTPA0-
LTPA0+
J4201
P_GND1
P_GND3
P_GND4
P_GND2
IEEE1394_CON_4P
12G13101004G
T12
GND
Co-Layout
RN4202A
0Ohm
L4202
90Ohm/100Mhz
RN4202B
0Ohm
41,65 TPA0-_1
41,65 TPA0+_1
Co-Layout
+3VS
R4214
10KOhm
XD_CD#
SDCD#
D4201
DAP202K
Q4207
2N7002
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D4202
DAP202K
+3VS
R4215
10KOhm
MSCD#
For Memory Stick Duo Adaptor shielding ground issue
Card Detect Table
MDIO00
MDIO01
XD Low Low
SD Low High
MS High Low
M1225
41,64 MDIO17_XDDAT7
41,64 MDIO16_XDDAT6
41,64 MDIO15_XDDAT5
41,64 MDIO14_XDDAT4
41,64 SD/MS/XDDAT3
41,64 SD/MS/XDDAT2
41,64 SD/MS/XDDAT1
41,64 SD/MS/XDDAT0
41,64 MDIO05_XDWP#
41,64 SDCMD_MSBS_XDWE#
41,64 MDIO19_XDALE
41,64 MDIO18_XDCLE
41,64 MDIO02_XDCE#
41,64 SDWP_XDR/B#
41,64 MDIO00_SDCD#_XDCD#
41,64 MDIO01_MSCD#_XDCD#
41,64 SD/MSCLK_XDRE#
Solve MS Duo Adaptor short problem
Q4204 2N7002
SD/MS/XDDAT1
SD_DAT1
Q4205 2N7002
SD/MS/XDDAT2
SD_DAT2
+12V
R42022
10KOhm
r0402_h16
SD_CD
Q4202
2N7002
SDCD#
GND
12G340004402
T12
+MC_VCC
C4207
270PF/50V
c0402
GND
J4202
MS_GND1
MS_BS
MS_DATA1
MS_DATA0
MS_DATA2
MS_INS
MS_DATA3
MS_SCLK
MS_VCC
MS_GND2
SD_DAT2
SD_DAT3
SD_CMD
SD_GND1
SD_VCC
SD_CLK
SD_GND2
NC1
SD_DAT0
SD_DAT1
SD_CD_SW
SD_CD_COM
NP_NC1
GND1
XD_CD
XD_GND1
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_GND2
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
XD_VCC
NC2
SD_WP_SW
SD_WP_COM
NP_NC2
GND2
CARD_READER_44P
SDCMD_MSBS_XDWE#
SD/MS/XDDAT1
SD/MS/XDDAT0
SD_DAT2
SD/MS/XDDAT3
SDCMD_MSBS_XDWE#
SD/MSCLK_XDRE#
SD/MS/XDDAT0
SD_DAT1
SDCD#
XD_CD#
SDWP_XDR/B#
SD/MSCLK_XDRE#
MDIO02_XDCE#
MDIO19_XDALE
SDCMD_MSBS_XDWE#
MDIO05_XDWP#
R4296 100Ohm SD/MS/XDDAT0
R4297 100Ohm SD/MS/XDDAT1
R4298 100Ohm SD/MS/XDDAT2
R4299 100Ohm SD/MS/XDDAT3
R4210 100Ohm MDIO14_XDDAT4
R4211 100Ohm MDIO15_XDDAT5
R4212 100Ohm MDIO16_XDDAT6
R4213 100Ohm MDIO17_XDDAT7
SDWP_XDR/B#
C4209
270PF/50V
c0402
C4208
3300PF/50V
c0603
GND
GND
GND
GND
GND
<Core Design>
Title: 1394 & CardReader CON
ASUSTeK COMPUTER INC
Engineer: Miller Liu
Size: Custom
Project Name: X51L
Rev: 2.2
Date: Wednesday, September 19, 2007
Sheet 42 of 94
Layout: SHIELD GND



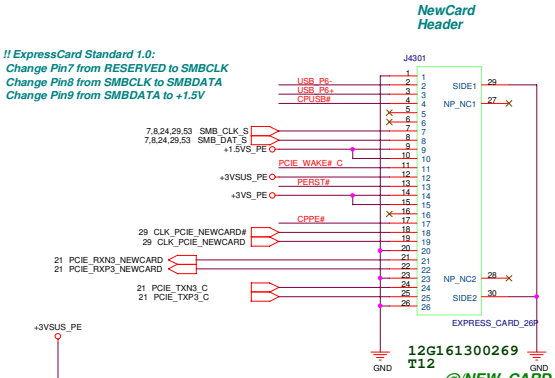


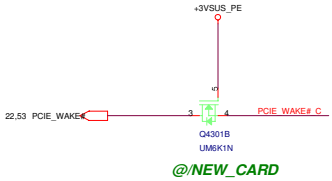


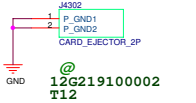


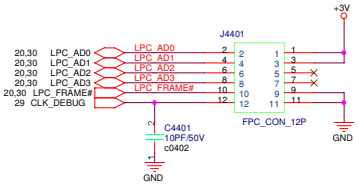
NewCard Header

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V









<Core Design>

Title : DEBUG

ASUSTeK COMPUTER INC. NB

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 44 of 94

CRT Connector

DVI-I Connector (Optional)

Impedence = 55 ohm
Trace Width = 5 mils

Impedence = 55 ohm
Trace Width = 5 mils
Distance =500 mils

12G10119029S
T12

12G10111215J
T12

Place near to CRT Port

<Core Design>

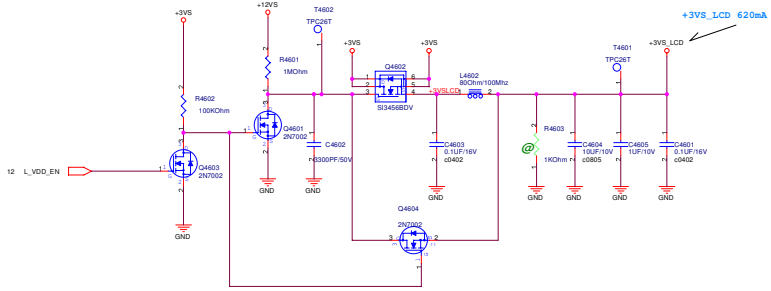
ASUSTeK COMPUTER INC

Title : CRT & DVI-I Conn.

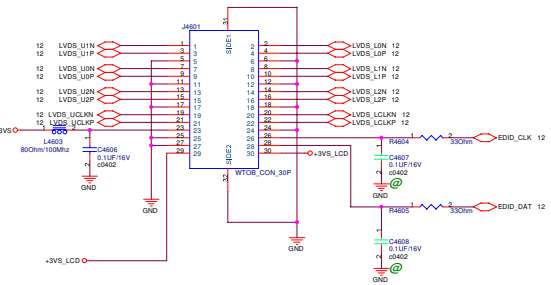
Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 45 of 94



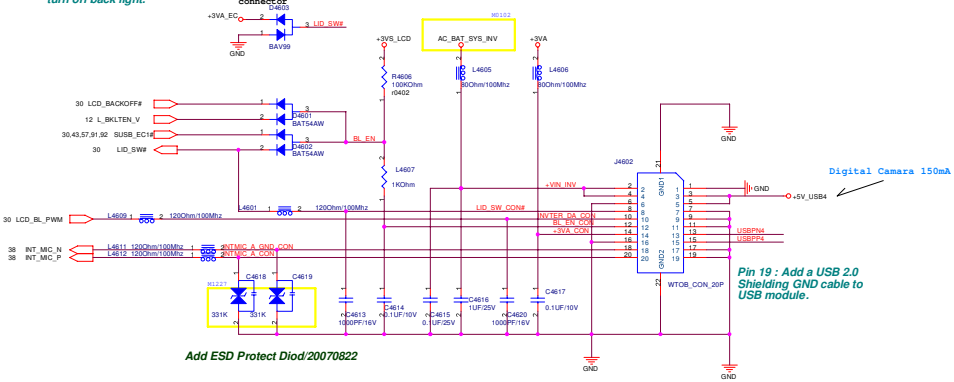
Pin define is the same as A7



LCD LVDS Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

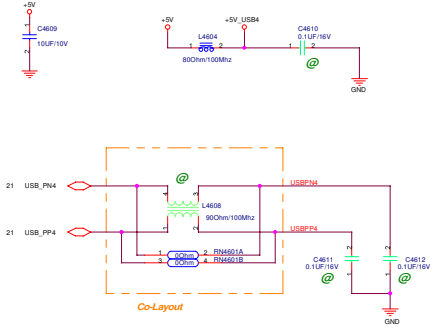
Layout note:close to connector



Digital Camara 150mA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

Add ESD Protect Diod/20070822



<Core Design>

ASUSTeK COMPUTER INC	Title : LVDS & Inverter Conn.		
	Engineer: Amy_Peng		
Size: Custom	Project Name: X51L		Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 46 of 94		

<Core Design>

Title : NULL

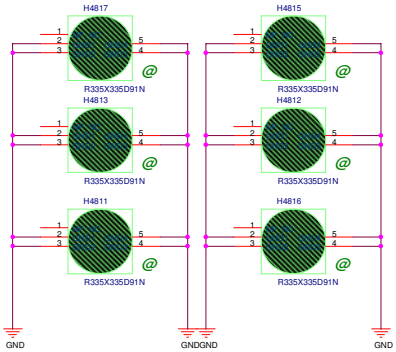
ASUSTeK COMPUTER INC

Engineer: Amy_Peng

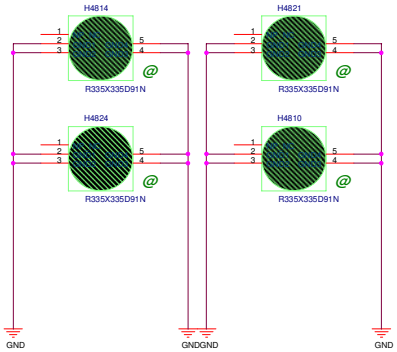
Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 47 of 94

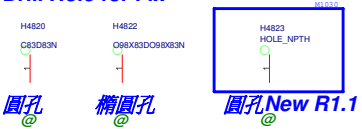
A Hole / TOP Side



A Hole / Bottom Side

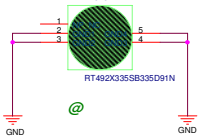


Drill Hole for Fix

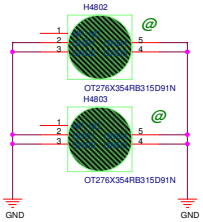


圓孔 @ 橢圓孔 @ 圓孔New R1.1 @

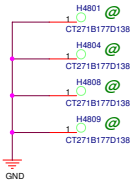
A Hole Special / Bottom Side



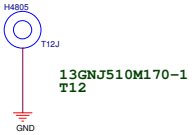
E Hole for Main board fix

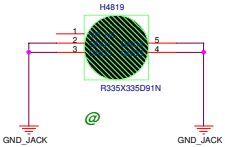


F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1





<Core Design>

Title : NULL

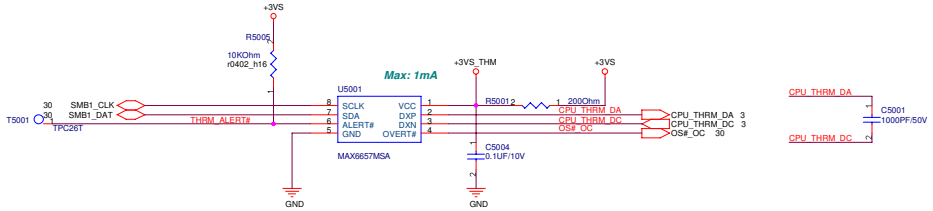
ASUSTeK COMPUTER INC

Engineer: Amy_Peng

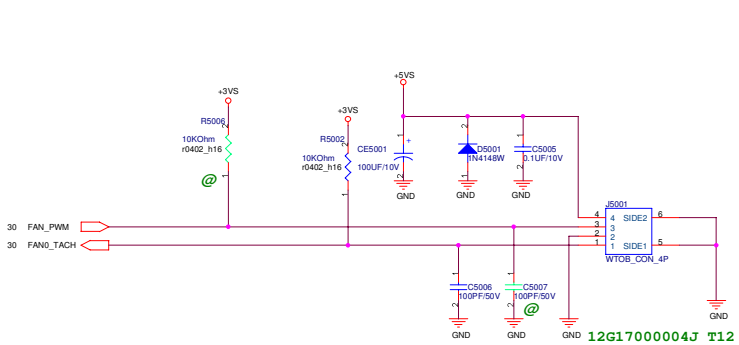
Size	Project Name	Rev
A	X51L	2.0

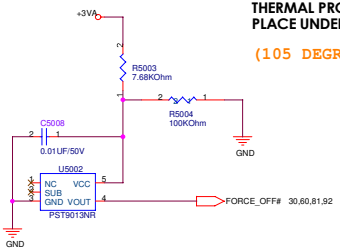
Date: Wednesday, September 19, 2007 Sheet 49 of 94

Thermal Sensor



DC FAN Control





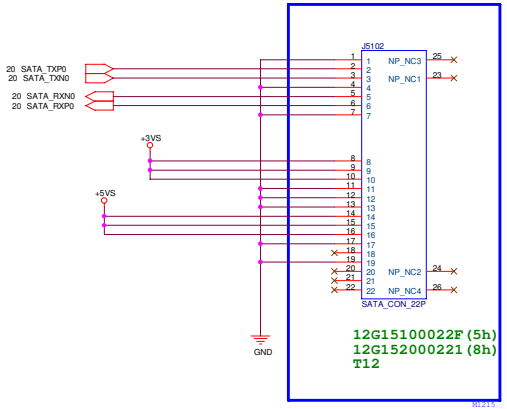
THERMAL PROTECTION PLACE UNDER CPU

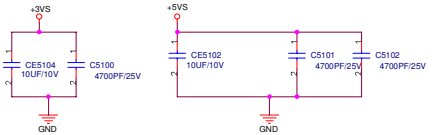
(105 DEGREE C)

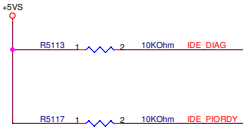
<Core Design>

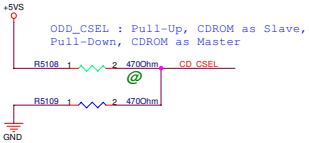
ASUSTeK COMPUTER INC. NB	Title : FAN	
	Engineer: Amy_Peng	
Size: Custom	Project Name: X51L	Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 50 of 94	

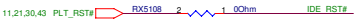
SATA HDD

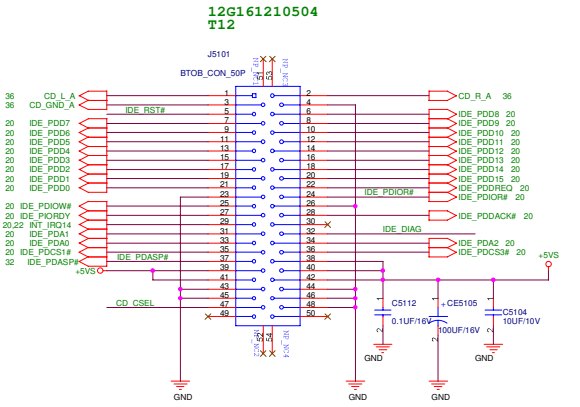




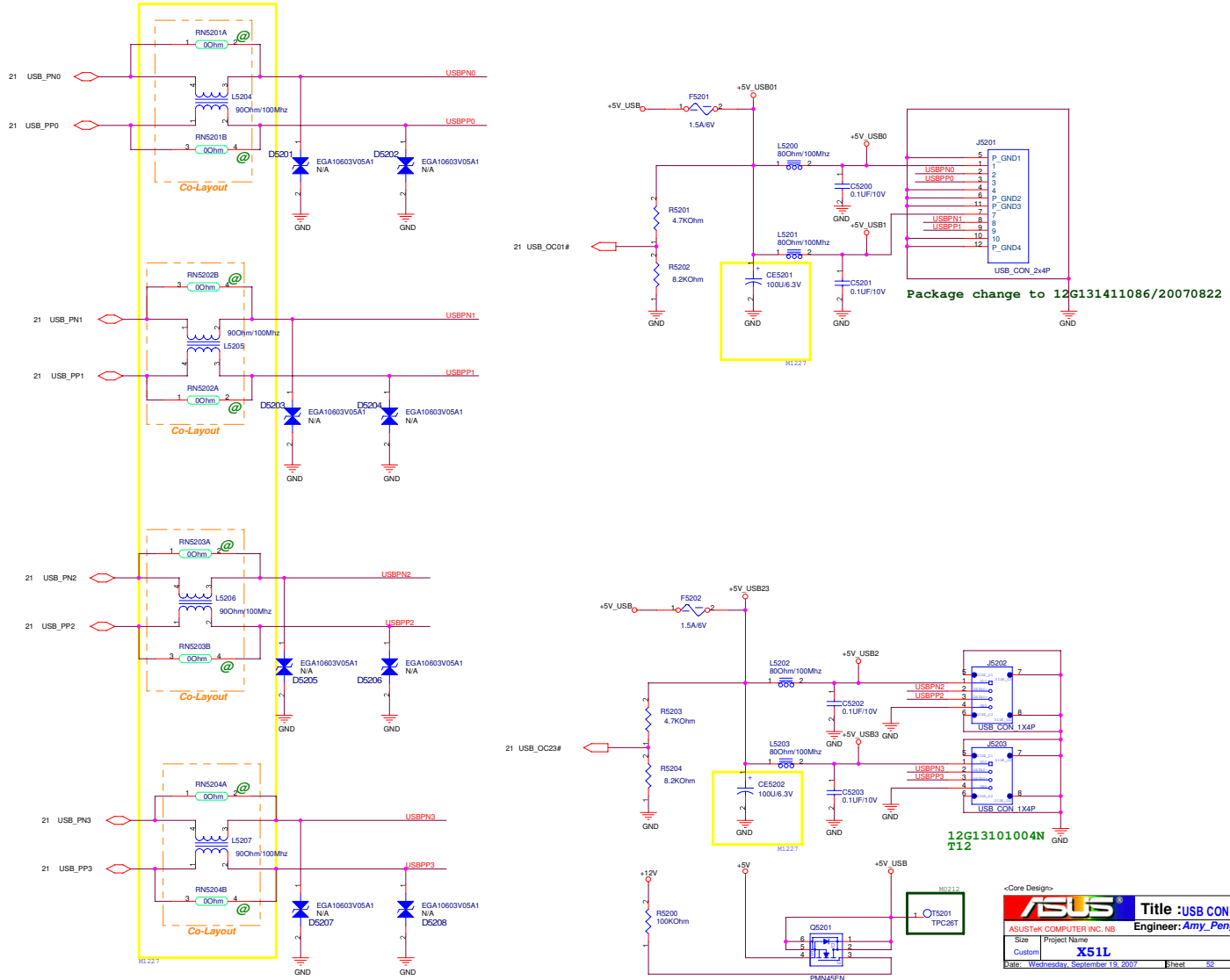




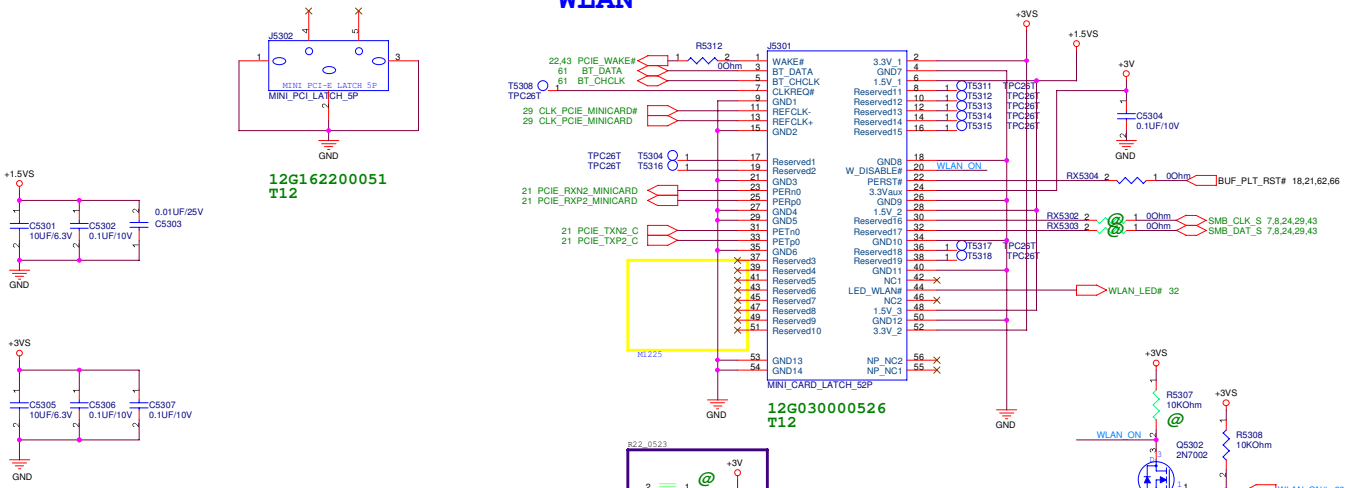




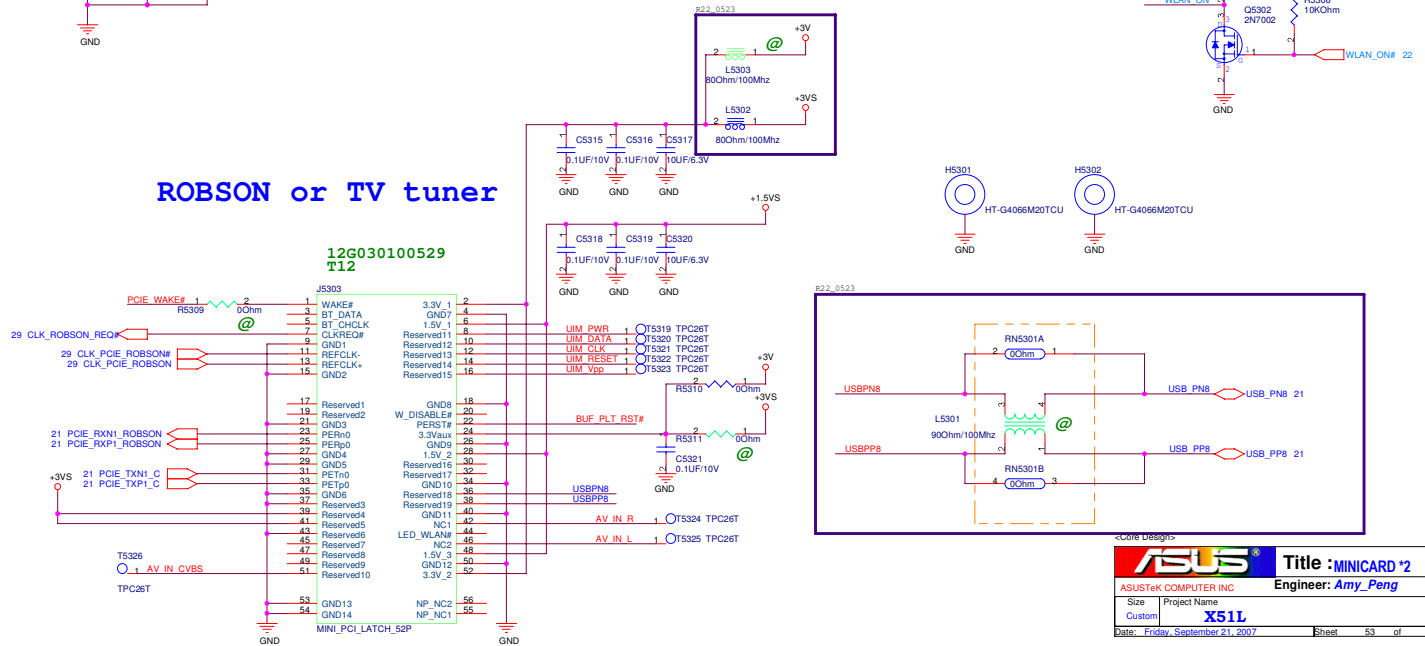
CE5105 Only use 11G041210754


RN5201A
0Ohm
21 USB_PN0
USBPN0
L5204
90Ohm/100Mhz
21 USB_PP0
USBPP0
RN5201B
0Ohm
D5201
EGA10603V05A1
N/A
D5202
EGA10603V05A1
N/A
GND
Co-Layout
RN5202B
0Ohm
21 USB_PN1
USBPN1
90Ohm/100Mhz
L5205
21 USB_PP1
USBPP1
RN5202A
0Ohm
D5203
EGA10603V05A1
N/A
D5204
EGA10603V05A1
N/A
Co-Layout
RN5203A
0Ohm
21 USB_PN2
USBPN2
L5206
90Ohm/100Mhz
21 USB_PP2
USBPP2
RN5203B
0Ohm
D5205
EGA10603V05A1
N/A
D5206
EGA10603V05A1
N/A
Co-Layout
RN5204A
0Ohm
21 USB_PN3
USBPN3
L5207
90Ohm/100Mhz
21 USB_PP3
USBPP3
RN5204B
0Ohm
D5207
EGA10603V05A1
N/A
D5208
EGA10603V05A1
N/A
Co-Layout
M1227
+5V_USB
F5201
1.5A/6V
+5V_USB01
L5200
80Ohm/100Mhz
+5V_USB0
C5200
0.1UF/10V
R5201
4.7KOhm
21 USB_OC01#
R5202
8.2KOhm
L5201
80Ohm/100Mhz
+5V_USB1
CE5201
100U/6.3V
C5201
0.1UF/10V
J5201
P_GND1
P_GND2
P_GND3
P_GND4
USBPN0
USBPP0
USBPN1
USBPP1
USB_CON_2x4P
Package change to 12G131411086/20070822
M1227
+5V_USB
F5202
1.5A/6V
+5V_USB23
L5202
80Ohm/100Mhz
+5V_USB2
C5202
0.1UF/10V
R5203
4.7KOhm
21 USB_OC23#
R5204
8.2KOhm
L5203
80Ohm/100Mhz
+5V_USB3
CE5202
100U/6.3V
C5203
0.1UF/10V
J5202
J5203
USBPN2
USBPP2
USBPN3
USBPP3
USB_CON_1X4P
12G13101004N
T12
M1227
+12V
R5200
100KOhm
+5V
+5V_USB
M2212
T5201
TPC26T
Q5201
PMN45EN
<Core Design>
Title : USB CONN X 4
ASUSTeK COMPUTER INC. NB
Engineer: Amy_Peng
Size
Custom
Project Name
X51L
Rev
2.2
Date: Wednesday, September 19, 2007
Sheet 52 of 94

WLAN



ROBSON or TV tuner



<Core Design>

Title : MINICARD *2

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Friday, September 21, 2007 Sheet 53 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 54 of 94

<Core Design>

Title : NULL

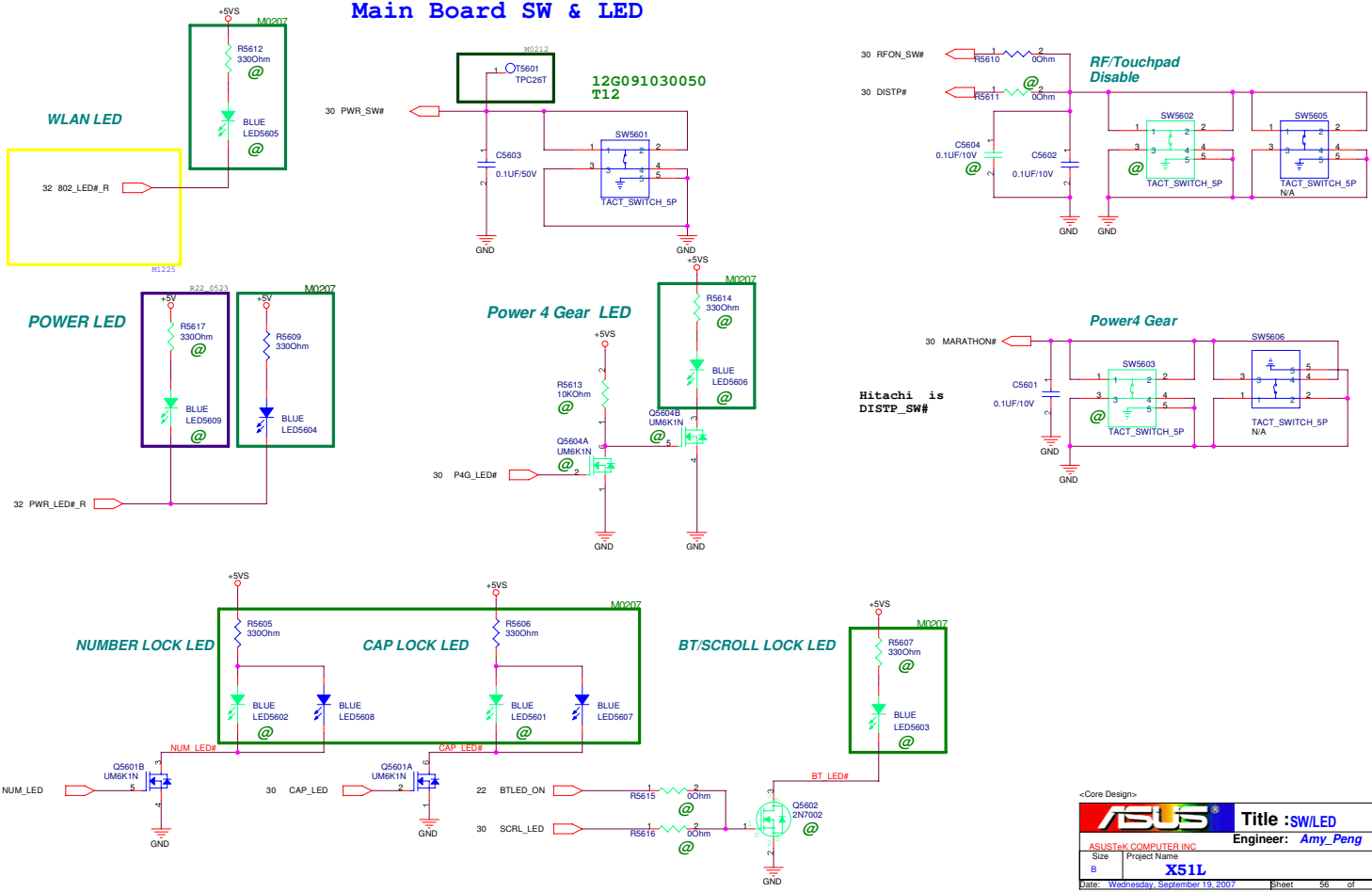
ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 55 of 94

Main Board SW & LED



<Core Design>

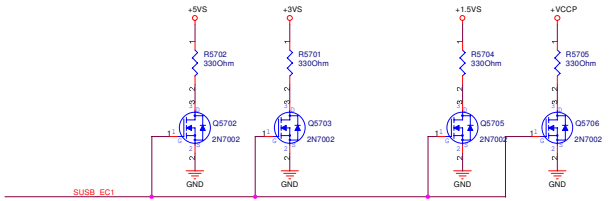
ASUSTeK COMPUTER INC

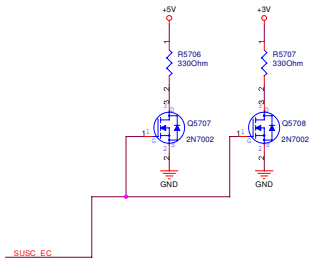
Title : SW/LED

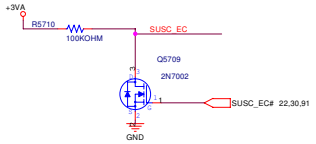
Engineer: Amy_Peng

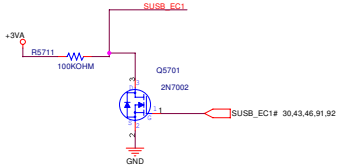
Size	Project Name	Rev
B	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 56 of 94









<Core Design>

ASUSTeK COMPUTER INC. NB

Title : DISCHARGE

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 57 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

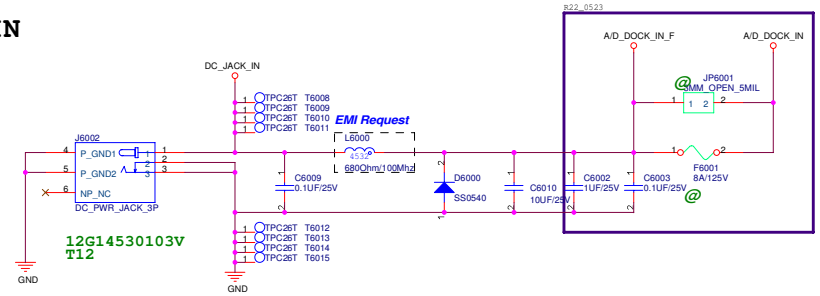
Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 58 of 94

<Core Design>

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: *Amy_Peng*	
Size: A	Project Name: **X51L**	Rev: 2.0
Date: Wednesday, September 19, 2007	Sheet 59 of 94	

DC-IN



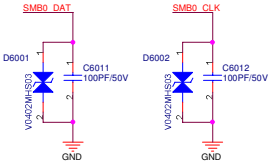
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# don't connect to Battery Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# must connect to Battery Connector.

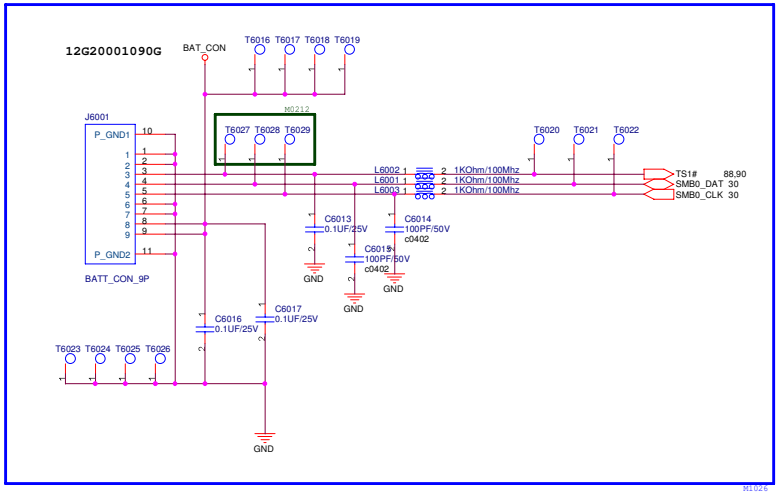


Note:

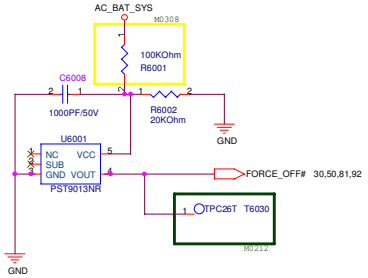
When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

Battery Connector



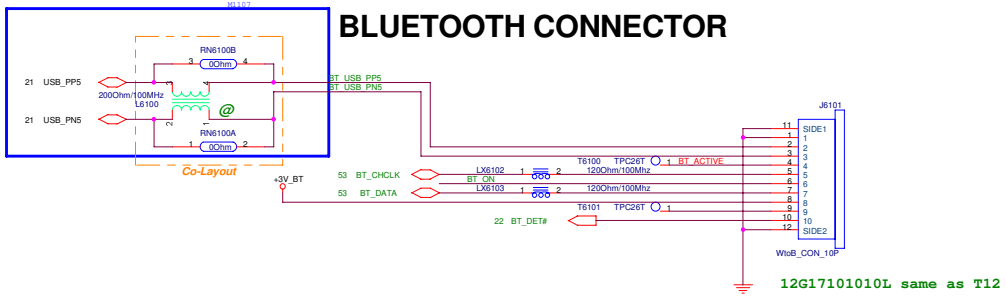
Without Battery & Pull out Adapter



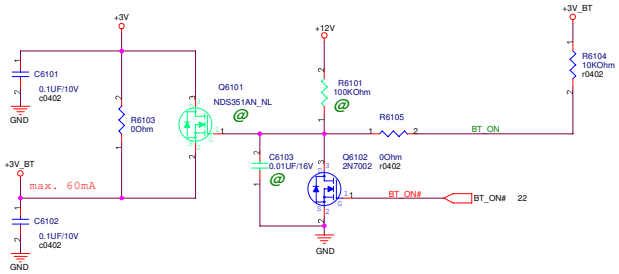
<Core Design>

ASUSTeK COMPUTER INC. NB	Title : DCIN/Batt conn.	
	Engineer: *Amy_Peng*	
Size: Custom	Project Name: X51L	Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 60 of 94	

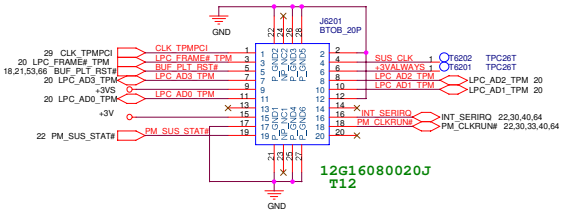
BLUETOOTH CONNECTOR

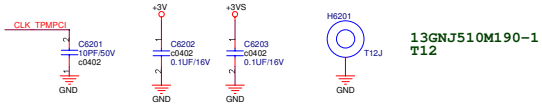


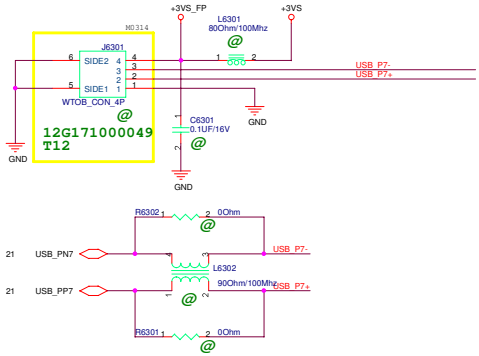
12G17101010L same as T12



TPM Connector







<Core Design>

ASUSTeK COMPUTER INC. NB

Title : Finger Print

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

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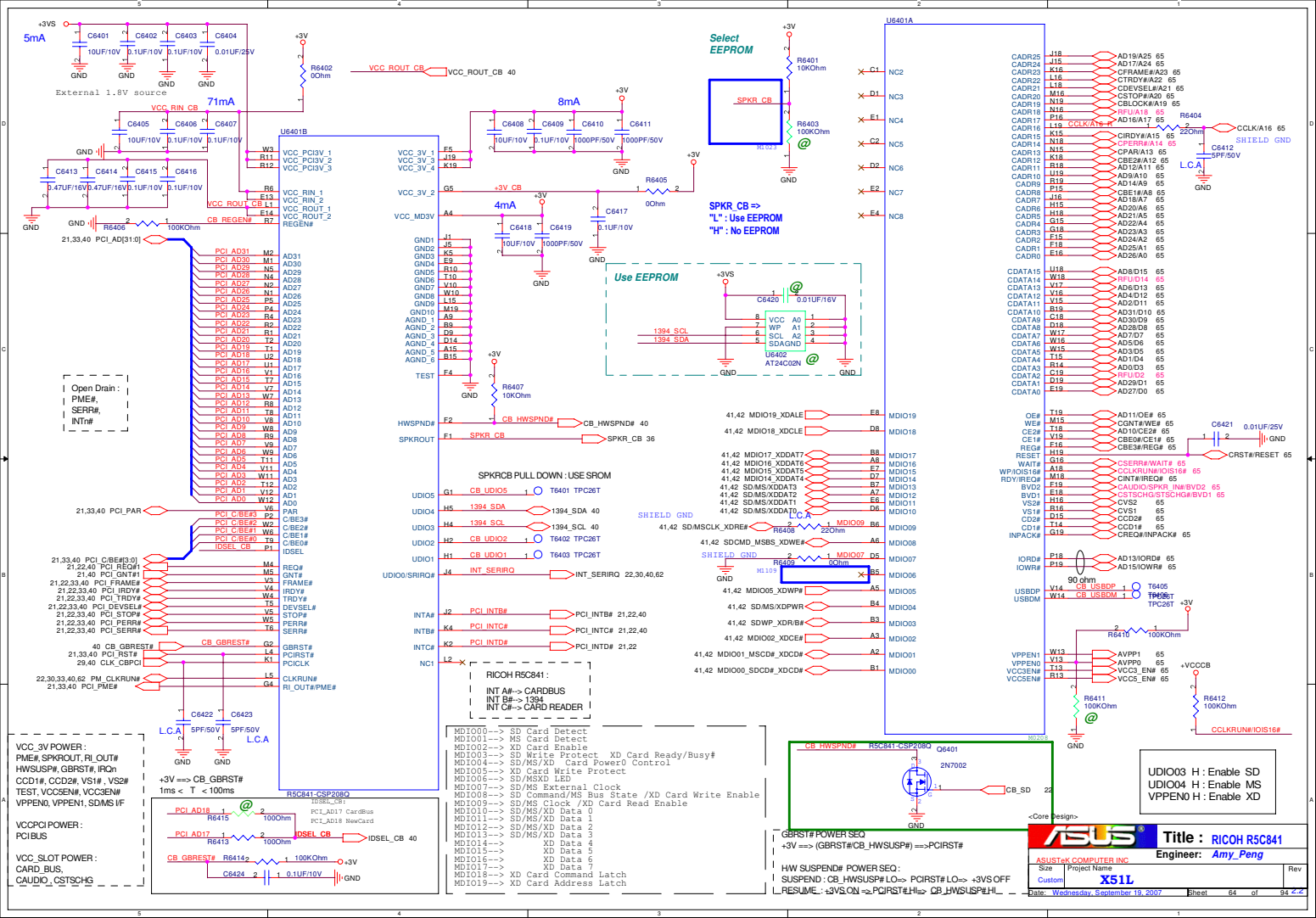
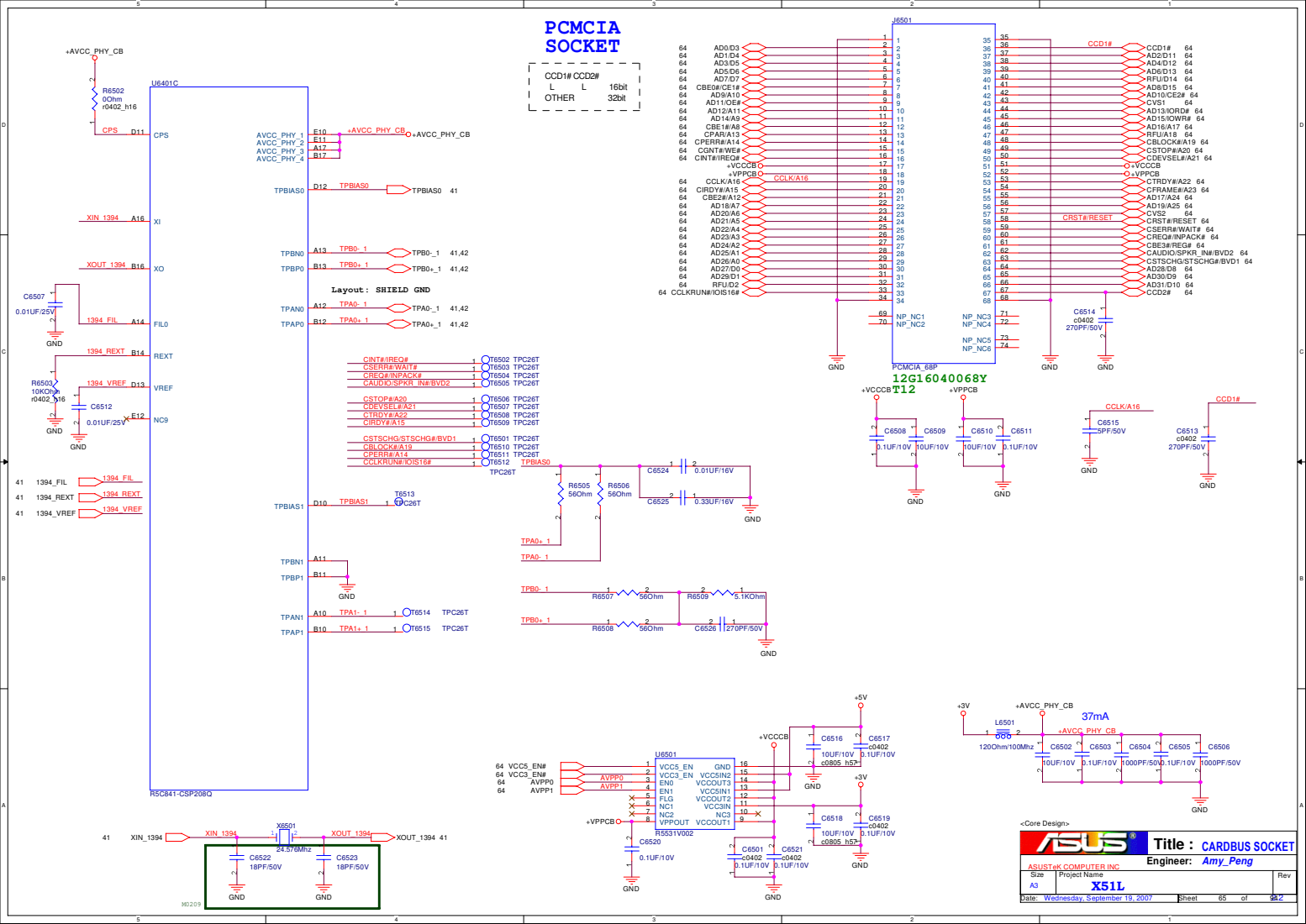

5mA
71mA
8mA
4mA
External 1.8V source
Select EEPROM
Use EEPROM
SPKR_CB =>
"L" : Use EEPROM
"H" : No EEPROM
Open Drain : PME#, SERR#, INTN#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#,SPKROUT,RI_OUT#
HWSUSP#,GBRST#,IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SDMS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD/Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO--> PCIRST# LO--> +3VS OFF
RESUME : +3VS ON --> PCIRST#↑ --> CB_HWSUSP#↑
Title : RICOH R5C841
Engineer: Amy_Peng
ASUSTeK COMPUTER INC
X51L
Wednesday, September 19, 2007


PCMCIA SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
J6501
PCMCIA_68P
12G16040068Y
U6401C
R5C841-CSP208Q
Layout: SHIELD GND
+AVCC_PHY_CB
+VCCCB
+VPPCB
+5V
+3V
37mA
X6501
24.576Mhz
U6501
R5531V002
<Core Design>
ASUS
Title : CARDBUS SOCKET
Engineer: Amy_Peng
ASUSTeK COMPUTER INC
Size A3
Project Name X51L
Rev
Date: Wednesday, September 19, 2007
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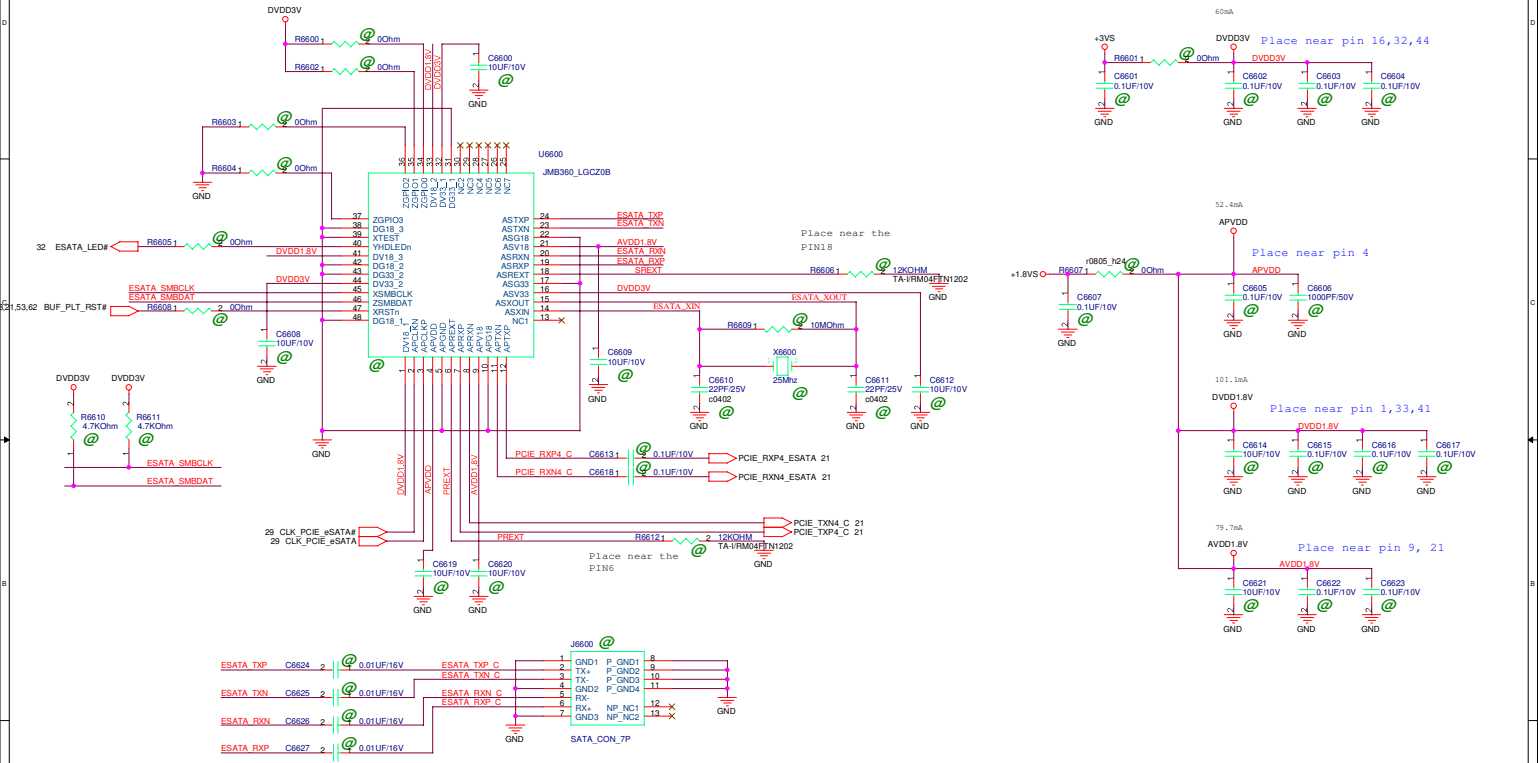

<core_design>


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PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	2	A
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

<Core Design>

ASUSTeK COMPUTER INC

Title : RESOURCE

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 67 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 68 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 69 of 94

<Core Design>

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: Amy_Peng	
Size: A	Project Name: X51L	Rev: 2.0
Date: Wednesday, September 19, 2007	Sheet 70 of 94	

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 71 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 72 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 73 of 94

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 74 of 94

<Core Design>

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: Amy_Peng	
Size: A	Project Name: X51L	Rev: 2.0
Date: Wednesday, September 19, 2007	Sheet 75 of 94	

<Core Design>

Title : Null

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 76 of 94

<Core Design>

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: Amy_Peng	
Size: A	Project Name: X51L	Rev: 2.0
Date: Wednesday, September 19, 2007	Sheet 77 of 94	

<Core Design>

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Amy_Peng

Size	Project Name	Rev
A	X51L	2.0

Date: Wednesday, September 19, 2007 Sheet 78 of 94

Change Note:

R1.1 :

1. Change CON0801 SM-Bus address to A2.
2. Unmount R2936.(SELLCD_27# =1)
3. RX2227 connect to GND.(Do not use Intel LAN)
4. Add R6415 to connect PCI_AD18(for R5C832).
5. Remove CON5301 Debug Pin.
6. Change CON4501.14 to VSYNC_CON.
7. Change CON3702 pin define(RL SWAP).
8. Change R2914 from 220 ohm to 390 ohm.
9. Mount C2920-22,C2924,C2925,C4618-19,L5204-07, Unmount RN5201-04 for EMI requst.
10. Add R4517,R4517,R4518 to prevent CON4501 short ground issue.
11. Change C0701,C0706,C0801,C0809 to R0701,R0702,R0802,R0803(68.9 ohm).
12. Change RNX4501-04 from 0 to 22ohm, and add R4519-4522(100 ohm).
13. SWAP SUSB_EC1#,SUSB_EC2#.

R2.0 :

1.Change Audio LDO(P36) and Audio AMP(P37).
2.Change CB_SD# to CB_SD (high active) to fix windows progress bar issue(P64).
3.Change LED color from Green to Blue (P56).
4.Change +3VS_832 to connect +3V to fix 1394 S3 issue (P41).
5.Change C6522,C6523 from 20pf to 18pf (ITTI suggestion).(P65).
6.Change C2002,C2005 from 22pf to 12pf (FUJICOM suggestion).(P20).
7.Change C3016,C3017 from 5pf to 15pf (FUJICOM suggestion).(P30).
8.Change R3313 from 2.49K to 2.43K to fix LAN low output peak voltage issue.(P33).

R2.1:

1.Change SII1362 to SII1368 to support DVI-HDCP(P18).
2.Change R3717,R3718 from 75ohm to 100ohm for EMI request(P18).
3.Add RNX 4505~4508 for EMI request(P18).

R2.2:

1.Add Power LED(LED5609) for Sotec(P56).
2.Change Audio AMP mute control circuit(P37).
3.Update Choke&Res Colay symbol(LAN,1394,CAMERA,USB,BT).
4.Add Fuse(F6001) and JUMP(JP6001) for Sotec(P60).
5.Add +3V power for TV-tuner card(P53).

R2.2 /EPSON:

1.J4401 debug connector delete(20070822)
2.J5201 USB package chanbe to 12G131411086(20070822)
3.C4618,C4619 add ESD protect diode 07G028011010(20070822)
4.C3311,C3319,C3330, Capacitor 10UF/10V change to 22UF/6.3V to reduce power noise meet Common Mode Voltage Spec(<50mV).(20070907)
5.C3307,C3313 Capacitor 10UF/10V change to 22UF/6.3V to reduce power noise meet Common Mode Voltage Spec(<50mV).(20070907)

<Core Design>

ASUSTeK COMPUTER INC

Title : NULL

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

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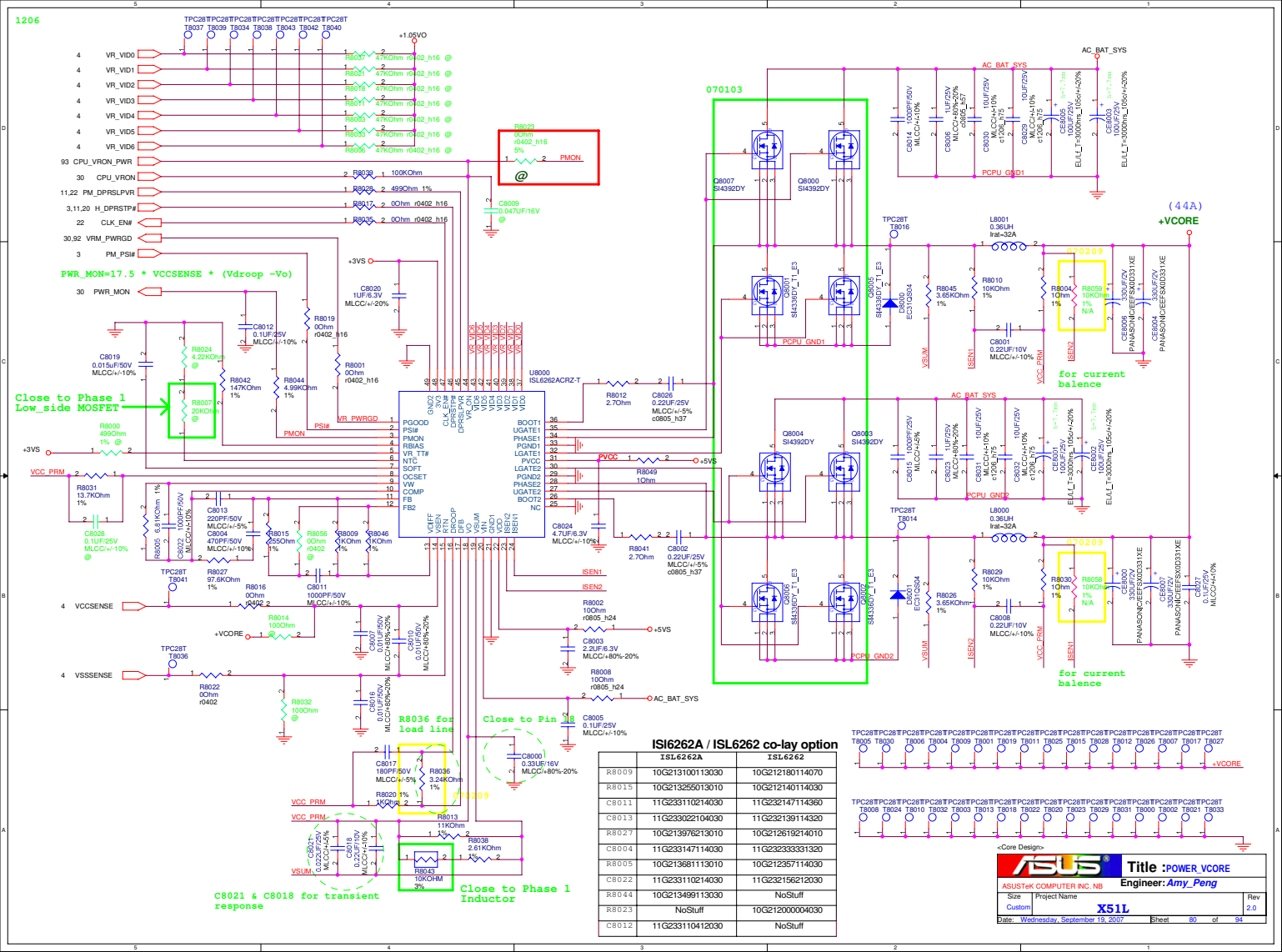
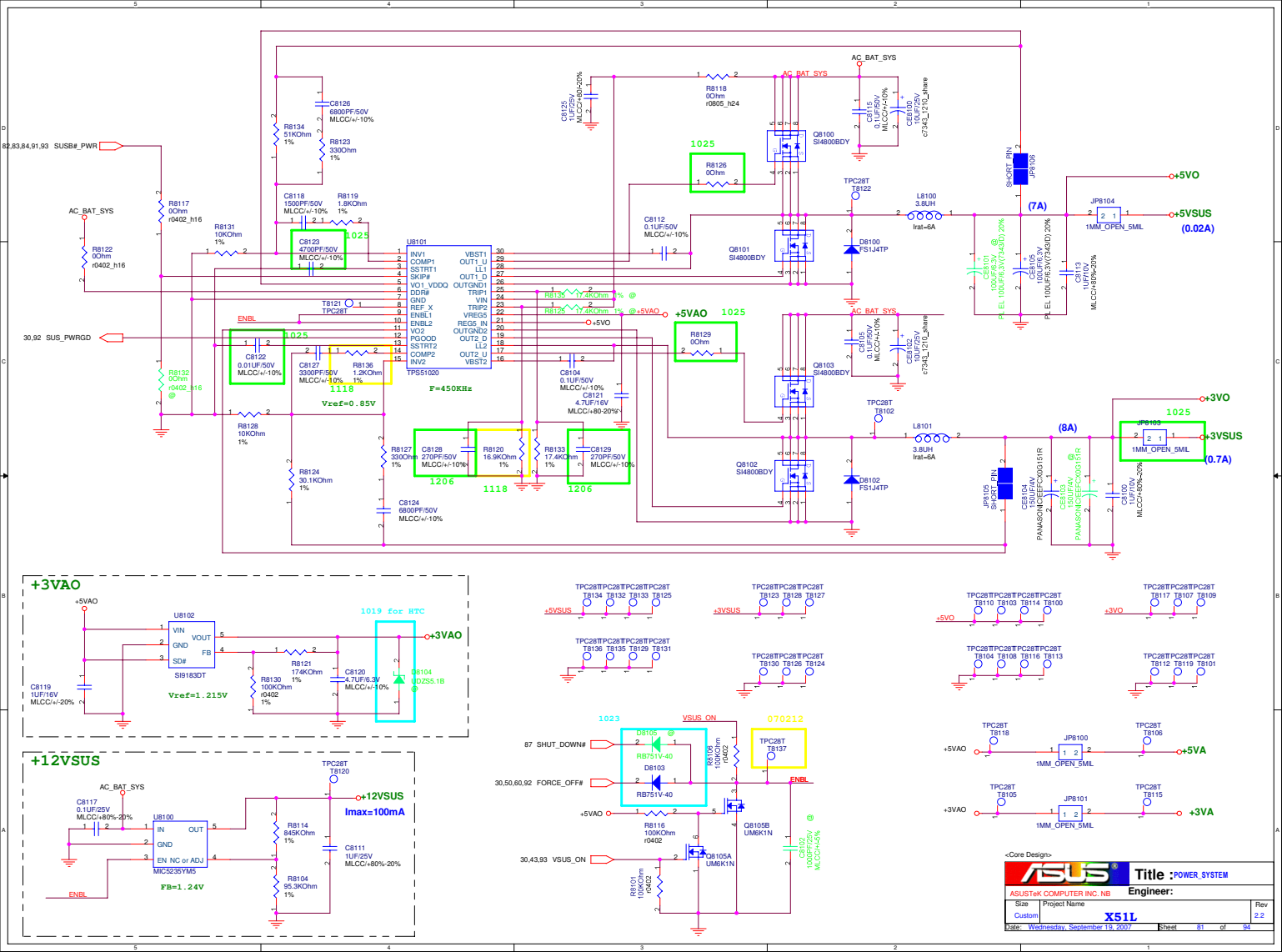


ISl6262A / ISL6262 co-lay option

	ISL6262A	ISL6262
R8009	10G213100113030	10G2121801140 70
R8015	10G213255013010	10G2121401140 30
C8011	11G233110214030	11G2321471143 60
C8013	11G233022104030	11G2321391143 20
R8027	10G213976213010	10G2126192140 10
C8004	11G233147114030	11G2323333313 20
R8005	10G213681113010	10G2123571140 30
C8022	11G233110214030	11G2321562120 30
R8044	10G213499113030	NoStuff
R8023	NoStuff	10G2120000040 30
C8012	11G233110412030	NoStuff


+3VAO
+5VAO
U8102
VIN
VOUT
GND
FB
SD#
SI9183DT
Vref=1.215V
1019 for HTC
+3VAO
C8119
1UF/16V
MLCC/+/-20%
R8121
174KOhm
1%
R8130
100KOhm
r0402
1%
C8120
4.7UF/6.3V
MLCC/+/-10%
D8104
UDZS5.1B
+12VSUS
Imax=100mA
AC_BAT_SYS
TPC28T
T8120
C8117
0.1UF/25V
MLCC/+80/-20%
U8100
IN
OUT
GND
EN NC or ADJ
MIC5235YM5
FB=1.24V
ENBL
R8114
845KOhm
1%
R8104
95.3KOhm
1%
C8111
1UF/25V
MLCC/+80%-20%
82,83,84,91,93 SUSB#_PWR
AC_BAT_SYS
R8117
0Ohm
r0402_h16
R8122
0Ohm
r0402_h16
R8131
10KOhm
1%
30,92 SUS_PWRGD
R8132
0Ohm
r0402_h16
@
R8134
51KOhm
1%
C8126
6800PF/50V
MLCC/+/-10%
R8123
330Ohm
1%
C8118
1500PF/50V
MLCC/+/-10%
R8119
1.8KOhm
1%
C8123
4700PF/50V
MLCC/+/-10%
1025
ENBL
C8122
0.01UF/50V
MLCC/+/-10%
C8127
3300PF/50V
MLCC/+/-10%
R8136
1.2KOhm
1%
1118
Vref=0.85V
R8128
10KOhm
1%
R8124
30.1KOhm
1%
C8124
6800PF/50V
MLCC/+/-10%
U8101
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
TPS51020
F=450KHz
R8135
17.4KOhm
1%
@
R8125
17.4KOhm
1%
@
+5VAO
+5VO
R8127
330Ohm
1%
C8128
270PF/50V
MLCC/+/-10%
R8120
16.9KOhm
1%
R8133
17.4KOhm
1%
C8129
270PF/50V
MLCC/+/-10%
1206
1118
1206
C8104
0.1UF/50V
MLCC/+/-10%
C8121
4.7UF/16V
MLCC/+80-20%
C8125
1UF/25V
MLCC/+80/-20%
R8118
0Ohm
r0805_h24
AC_BAT_SYS
C8115
0.1UF/50V
MLCC/+/-10%
CE8100
10UF/25V
c7343_1210_share
Q8100
SI4800BDY
1025
R8126
0Ohm
TPC28T
T8122
L8100
3.8UH
Irat=6A
D8100
FS1J4TP
Q8101
SI4800BDY
C8112
0.1UF/50V
MLCC/+/-10%
SHORT PIN
JP8105
(7A)
+5VO
JP8104
+5VSUS
(0.02A)
1MM_OPEN_5MIL
CE8101
100UF/6.3V
PL EL 100UF/6.3V(7343D) 20%
CE8105
100UF/6.3V
PL EL 100UF/6.3V(7343D) 20%
C8113
1UF/25V
MLCC/+80%-20%
AC_BAT_SYS
C8105
0.1UF/50V
MLCC/+/-10%
CE8102
10UF/25V
c7343_1210_share
Q8103
SI4800BDY
R8129
0Ohm
1025
TPC28T
T8102
L8101
3.8UH
Irat=6A
D8102
FS1J4TP
Q8102
SI4800BDY
(8A)
+3VO
JP8103
+3VSUS
(0.7A)
1MM_OPEN_5MIL
JP8105
SHORT PIN
CE8104
150UF/4V
PANASONICEFCX0G151R
CE8103
150UF/4V
PANASONICEFCX0G151R
C8100
1UF/25V
MLCC/+80%-20%
TPC28T TPC28T TPC28T TPC28T TPC28T
T8134 T8132 T8133 T8125
+5VSUS
TPC28T TPC28T TPC28T TPC28T TPC28T
T8136 T8135 T8129 T8131
TPC28T TPC28T TPC28T
T8123 T8128 T8127
+3VSUS
TPC28T TPC28T TPC28T
T8130 T8126 T8124
TPC28T TPC28T TPC28T TPC28T TPC28T
T8110 T8103 T8114 T8100
+5VO
TPC28T TPC28T TPC28T
T8117 T8107 T8109
+3VO
TPC28T TPC28T TPC28T TPC28T TPC28T
T8104 T8108 T8116 T8113
TPC28T TPC28T TPC28T
T8112 T8119 T8101
1023
VSUS_ON
070212
87 SHUT_DOWN#
30,50,60,92 FORCE_OFF#
30,43,93 VSUS_ON
D8105
RB751V-40
D8103
RB751V-40
TPC28T
T8137
ENBL
R8105
100KOhm
r0402
R8116
100KOhm
r0402
Q8105A
UM6K1N
Q8105B
UM6K1N
R8101
100KOhm
r0402
C8102
1000PF/25V
MLCC/+/-5%
@
TPC28T
T8118
JP8100
TPC28T
T8106
+5VA
1MM_OPEN_5MIL
TPC28T
T8105
JP8101
TPC28T
T8115
+3VA
1MM_OPEN_5MIL
<Core Design>
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer:
Size
Custom
Project Name
X51L
Rev
2.2
Date: Wednesday, September 19, 2007
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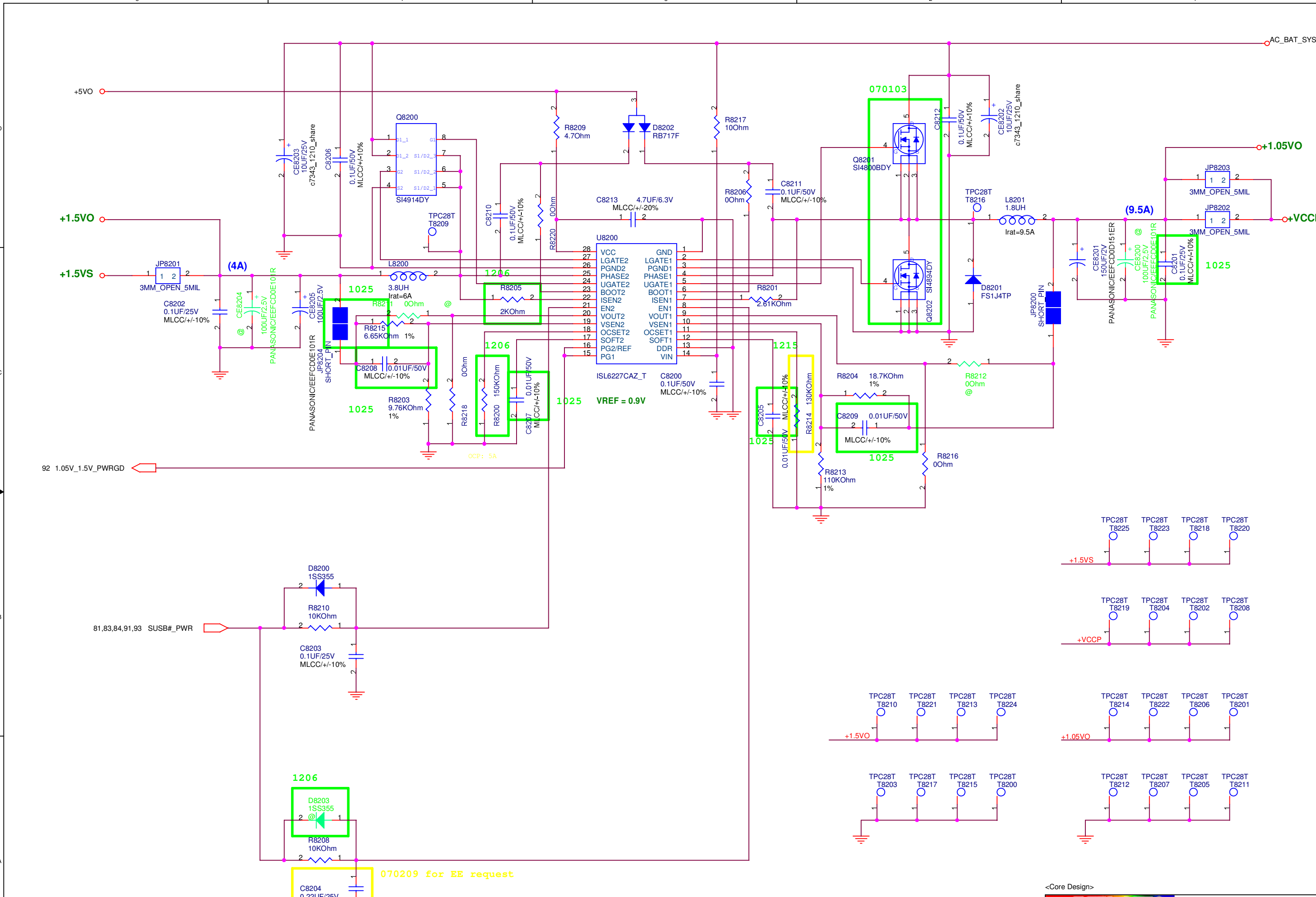

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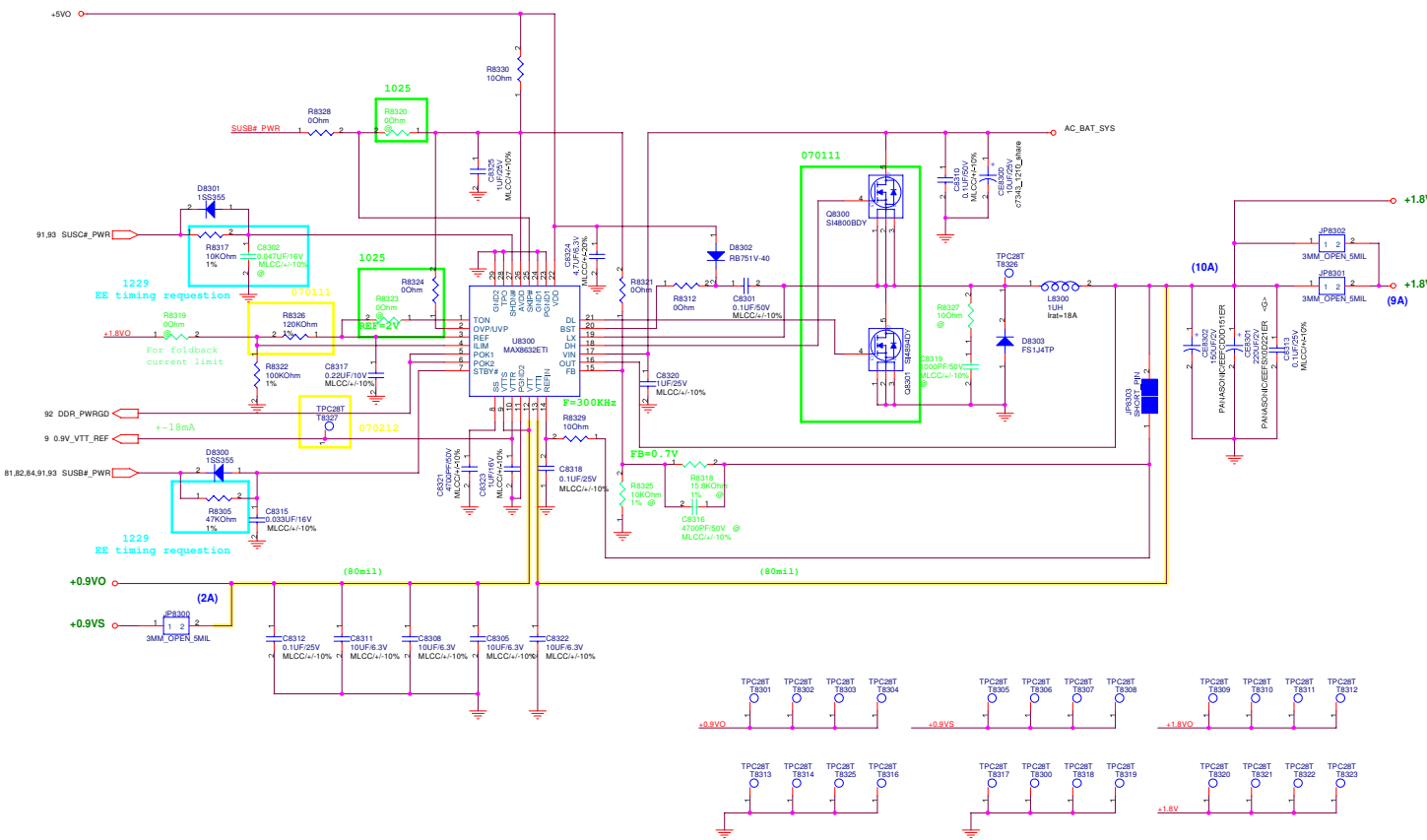
Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 82 of 94



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ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR & VTT

Engineer:

Size	Project Name	Rev
Custom	X51L	2.2

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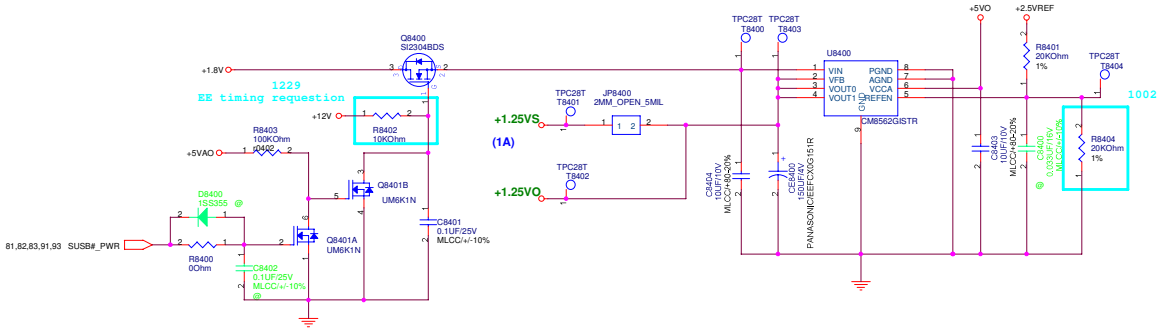
+1.25VS



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<OrgName>	Title : POWER_I/O_1.25VS	
	Engineer:	
Size: Custom	Project Name: X51L	Rev: 2.2
Date: Wednesday, September 19, 2007	Sheet 84 of 94	

<Core Design>

Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
C	X51L	1.1

Date: Wednesday, September 19, 2007 Sheet 85 of 94

<Core Design>

Title : N/A

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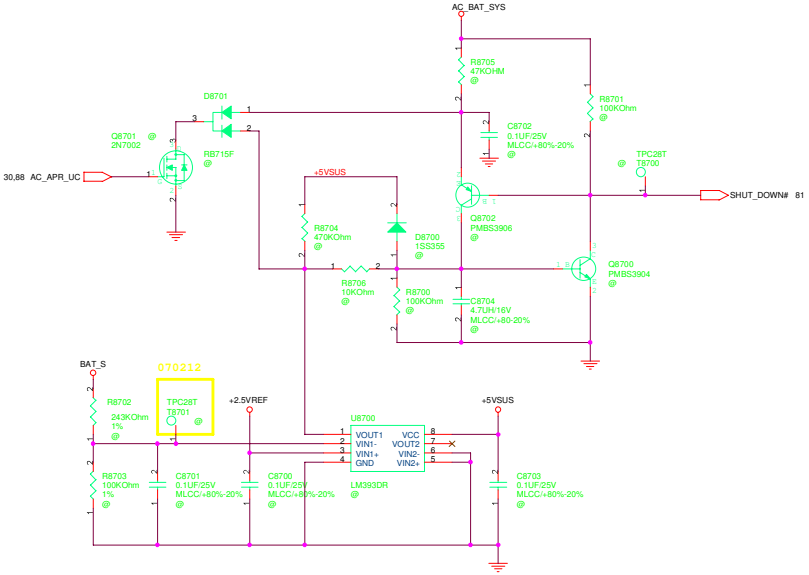
Engineer:

Size	Project Name	Rev
B	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 86 of 94

PIC only



<Core Design>

Title : POWER_SHUTDOWN#

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	X51L	2.2

Date: Wednesday, September 19, 2007 Sheet 87 of 94

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.020ohm
VCLS=3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R8805=20K,R8819=137K--->65W
=> R8805=20K,R8819=30K--->90W

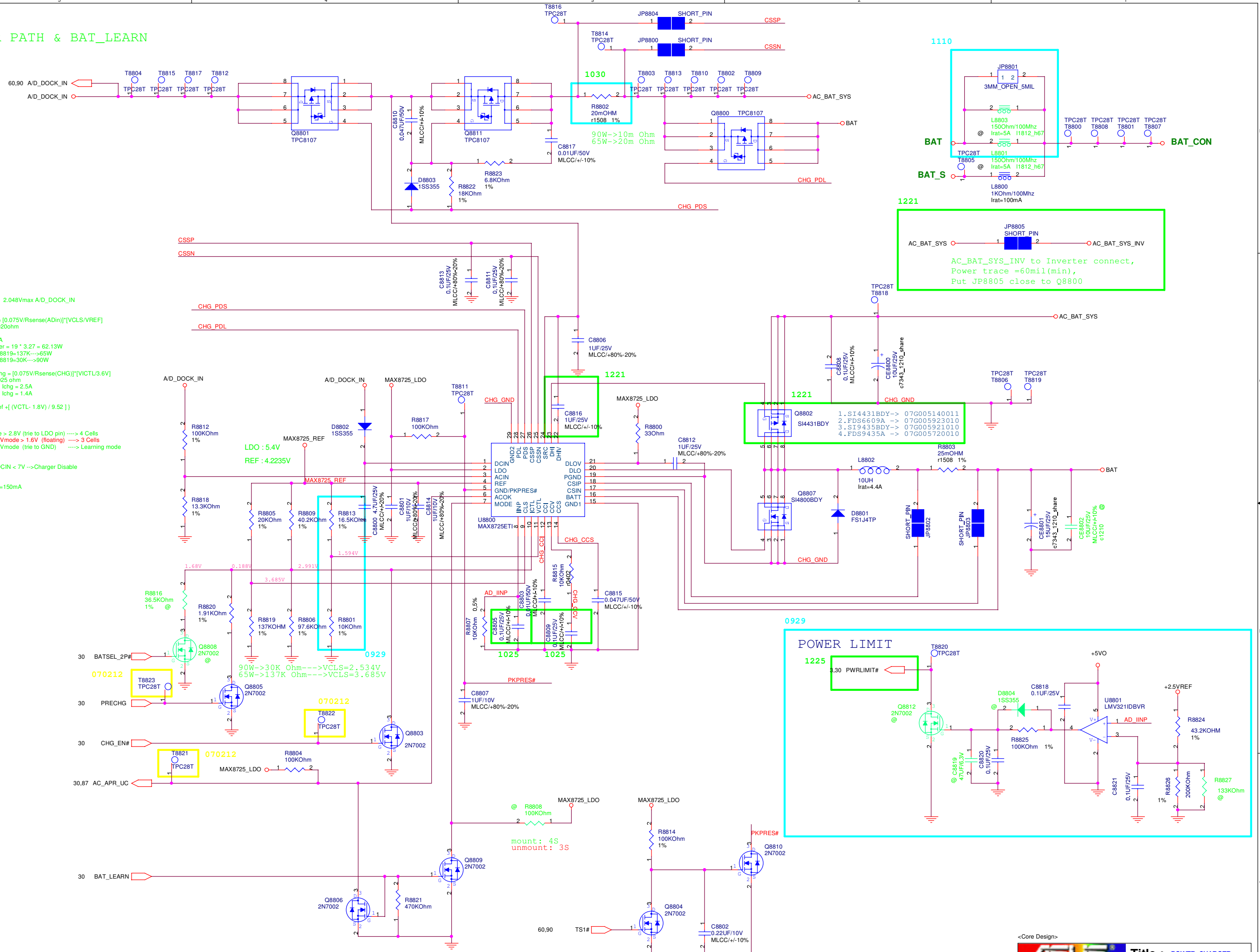
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL=3V => Ichg = 2.5A
VICTL=1.68V => Ichg = 1.4A

Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52])
VCTL=1.594V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin)----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA



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Title : N/A

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	X51L	1.1

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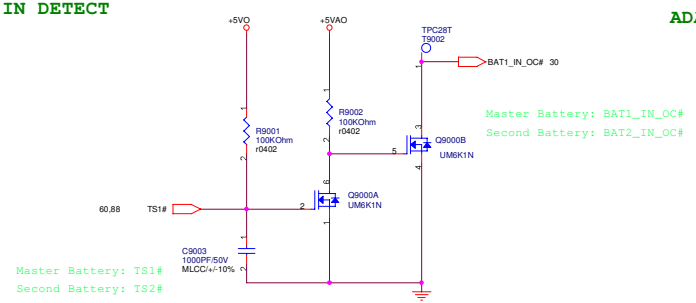
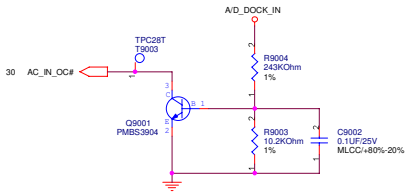
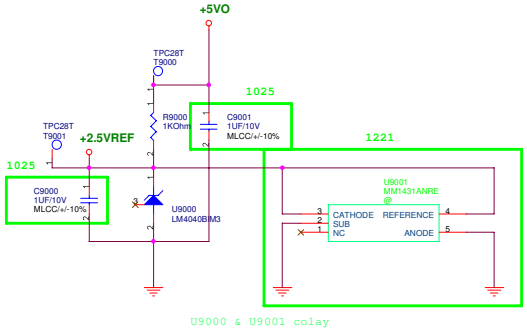
BATTERY IN DETECT



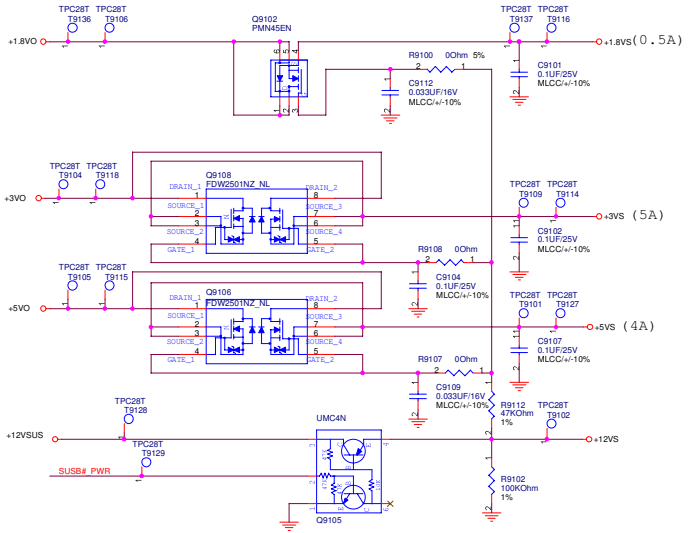
ADAPTER IN DETECT



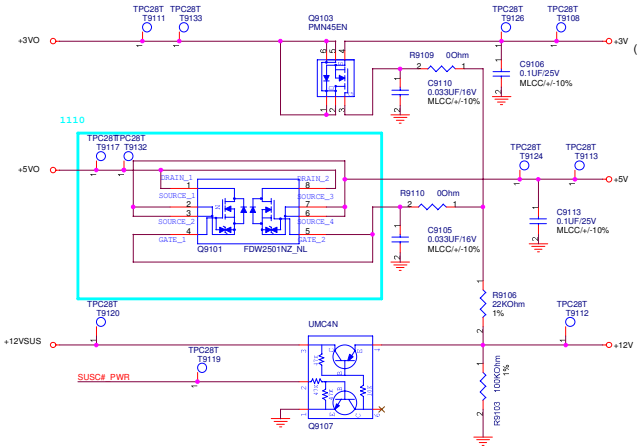
+2.5VREF

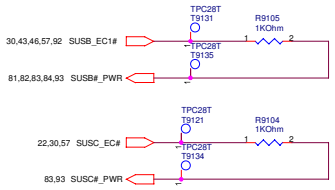


SUSB#_PWR POWER



SUSC#_PWR POWER





<Core Design>

Title : POWER_LOAD SWITCH

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	X51L	2.2

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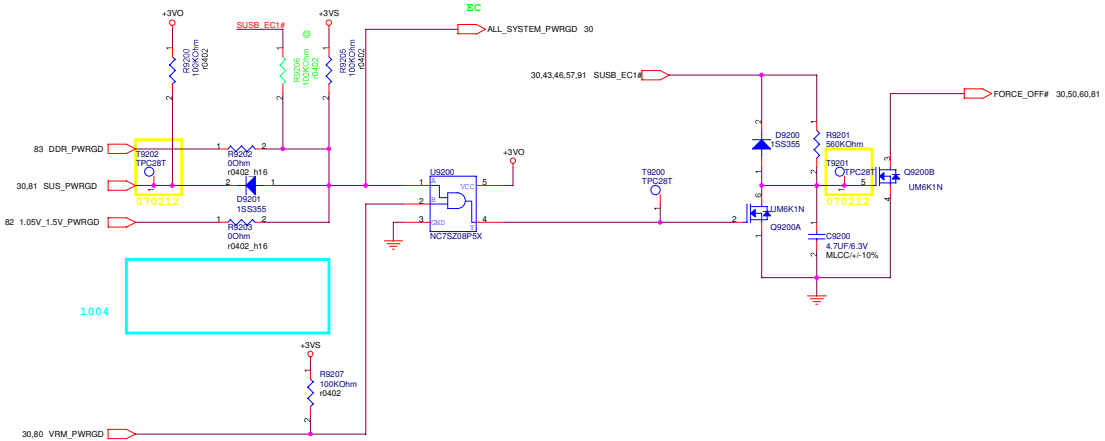
POWER GOOD DETECTER



<Core Design>

<OrgName>	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: X51L	Rev: 2.2
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AC_BAT_SYS — AC_BAT_SYS 60,80,81,82,83,87,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

+2.5VREF — +2.5VREF 84,87,88,90

+3VA — +3VA 20,22,30,46,50,57,81

+5VAO — +5VAO 81,84,90

+5VO — +5VO 81,82,83,84,88,90,91

+5VSUS — +5VSUS 23,32,81,87

+5V — +5V 15,32,46,52,56,57,65,91

+5VS — +5VS 23,24,32,36,37,38,45,50,51,56,57,80,91

+3VO — +3VO 81,91,92

+3VSUS — +3VSUS 21,22,23,30,33,37,43,81

+3V — +3V 21,22,35,40,41,44,53,57,61,62,64,65,91

+3VS — +3VS 3,7,8,11,12,15,18,22,23,24,29,30,32,33,36,40,42,43,45,46,50,51,53,57,62,63,64,66,80,91,92

+12VSUS — +12VSUS 81,91

+12V — +12V 37,42,52,61,84,91

+12VS — +12VS 46,91

+1.8VO — +1.8VO 83,91

+1.8V — +1.8V 7,8,9,11,14,15,83,84

+1.8VS — +1.8VS 18,66,91

+0.9VS — +0.9VS 9,83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,82

+VCCP — +VCCP 4,10,12,14,15,20,23,29,57,82

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 4,15,20,21,23,43,53,57,82

+VCORE — +VCORE 4,80

1004

+1.25VS — +1.25VS 11,15,23,84

FOR POWER TEST

070108

+3VA

JP9300 — SGL_JUMP — CPU_VRON_PWR 80

JP9301 — SGL_JUMP — SUSB#_PWR — SUSB#_PWR 81,82,83,84,91

JP9302 — SGL_JUMP — SUSC#_PWR — SUSC#_PWR 83,91

JP9303 — SGL_JUMP — VSUS_ON — VSUS_ON 30,43,81

<Core Design>

Title : POWER_SIGNAL

<OrgName>

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

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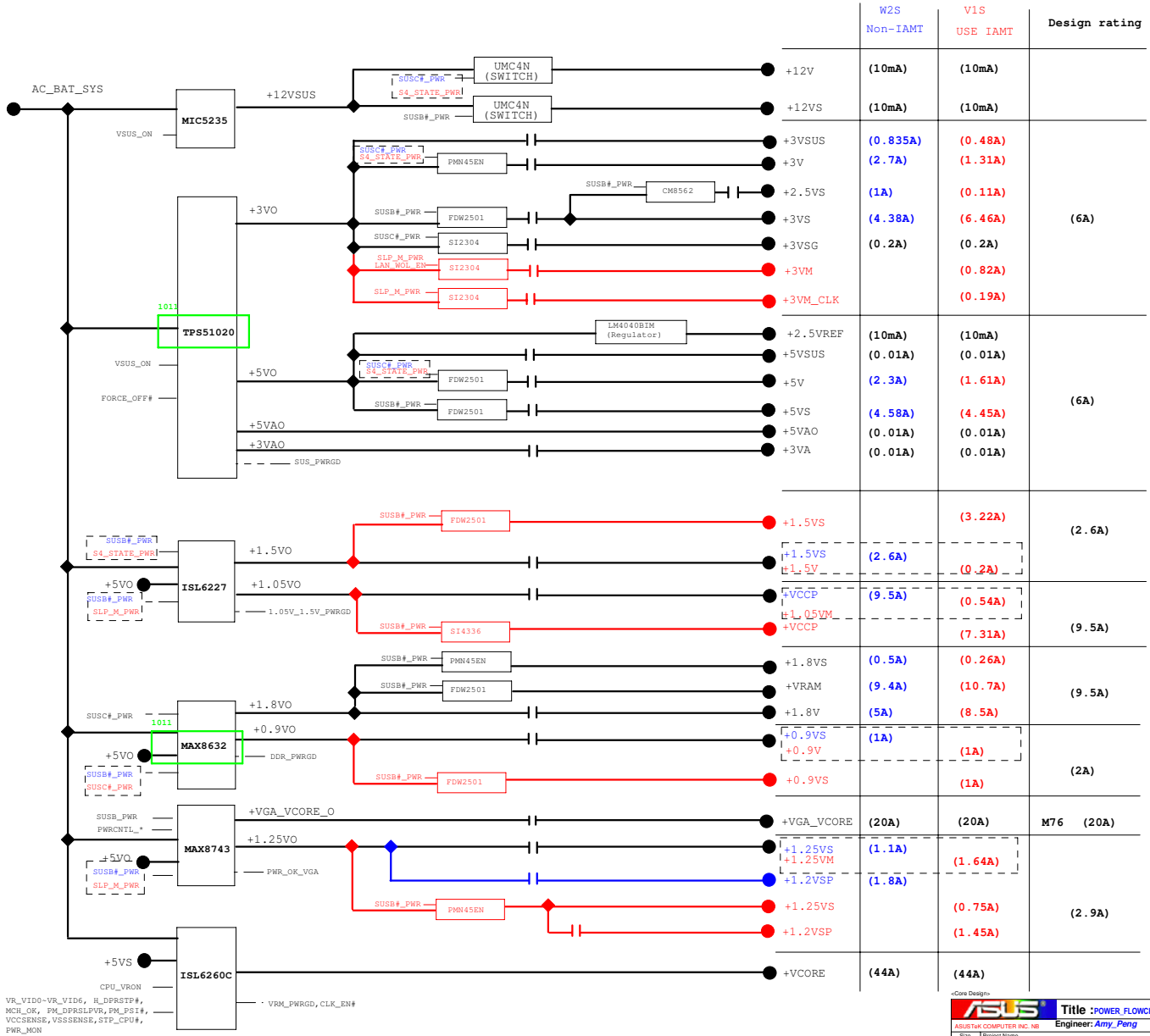

	W2S Non-IAMT	V1S USE IAMT	Design rating
+12V	(10mA)	(10mA)	
+12VS	(10mA)	(10mA)	
+3VSUS	(0.835A)	(0.48A)	
+3V	(2.7A)	(1.31A)	
+2.5VS	(1A)	(0.11A)	
+3VS	(4.38A)	(6.46A)	(6A)
+3VSG	(0.2A)	(0.2A)	
+3VM		(0.82A)	
+3VM_CLK		(0.19A)	
+2.5VREF	(10mA)	(10mA)	
+5VSUS	(0.01A)	(0.01A)	
+5V	(2.3A)	(1.61A)	
+5VS	(4.58A)	(4.45A)	(6A)
+5VAO	(0.01A)	(0.01A)	
+3VA	(0.01A)	(0.01A)	
+1.5VS		(3.22A)	(2.6A)
+1.5VS	(2.6A)		
+1.5V		(0.2A)	
+VCCP	(9.5A)	(0.54A)	
+1.05VM			
+VCCP		(7.31A)	(9.5A)
+1.8VS	(0.5A)	(0.26A)	
+VRAM	(9.4A)	(10.7A)	(9.5A)
+1.8V	(5A)	(8.5A)	
+0.9VS	(1A)		
+0.9V		(1A)	
+0.9VS		(1A)	(2A)
+VGA_VCORE	(20A)	(20A)	M76 (20A)
+1.25VS	(1.1A)		
+1.25VM		(1.64A)	
+1.2VSP	(1.8A)		
+1.25VS		(0.75A)	
+1.2VSP		(1.45A)	(2.9A)
+VCORE	(44A)	(44A)	

<Core Design>

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Amy_Peng

Size	Project Name	Rev
Custom	X51L	2.2

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