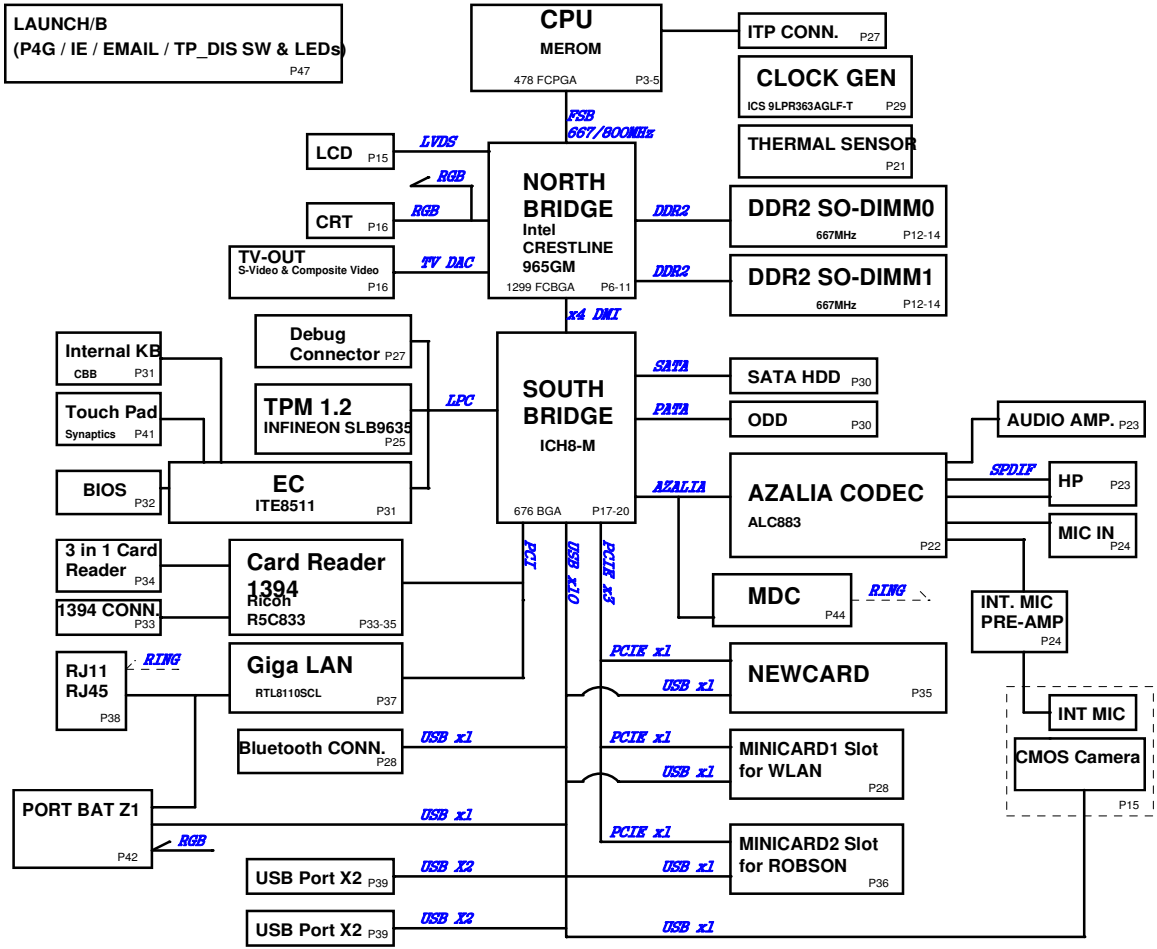
Z62E Block Diagram

Ver: 2.0G



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 八月 15, 2007 Sheet 1 of 59

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	1394
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	CARD
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
1394	AD17	0	INTA
CARD READER	AD17	0	INTB
LAN	AD23	2	INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

<Variant Name>

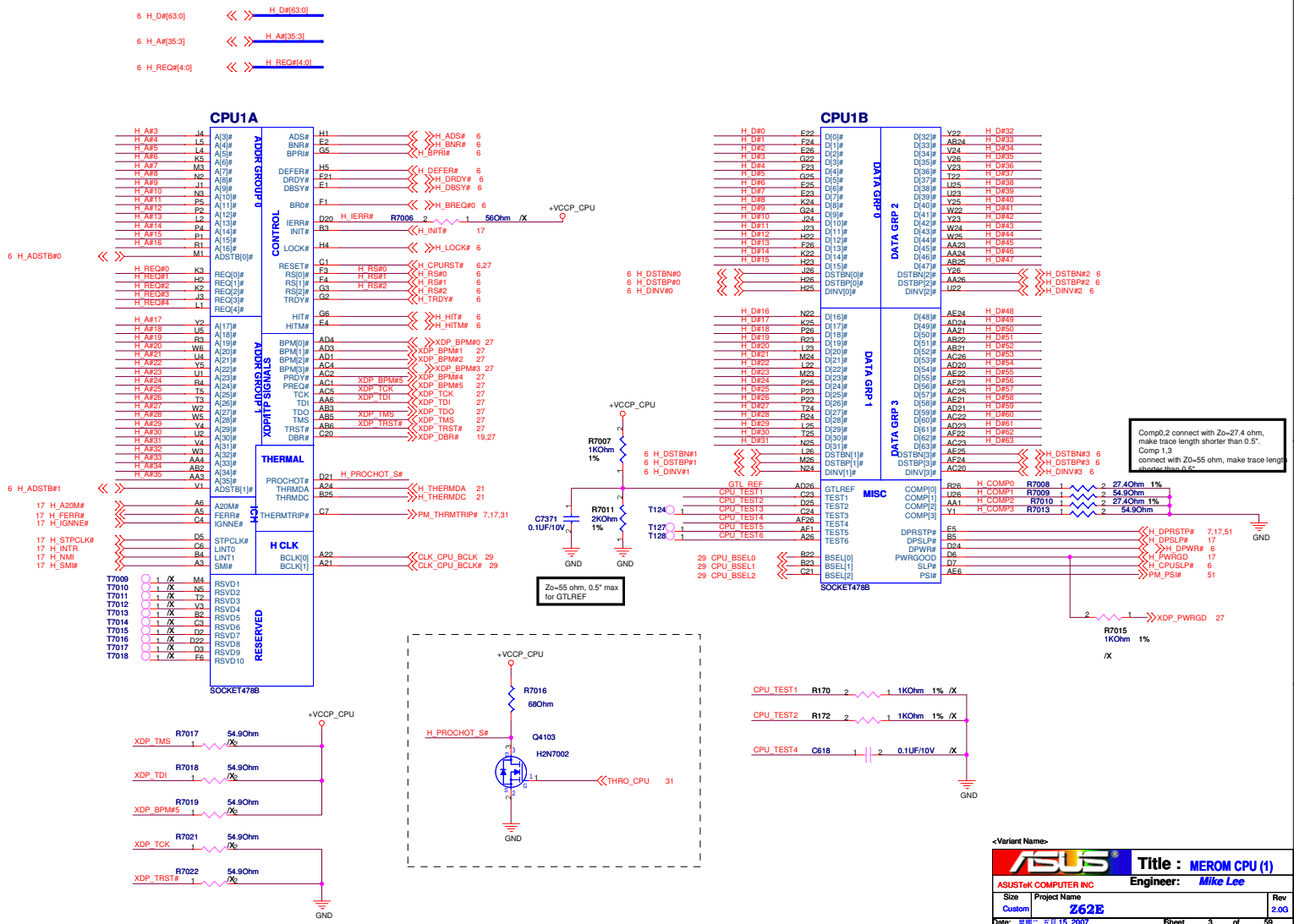
ASUSTeK Computer INC.

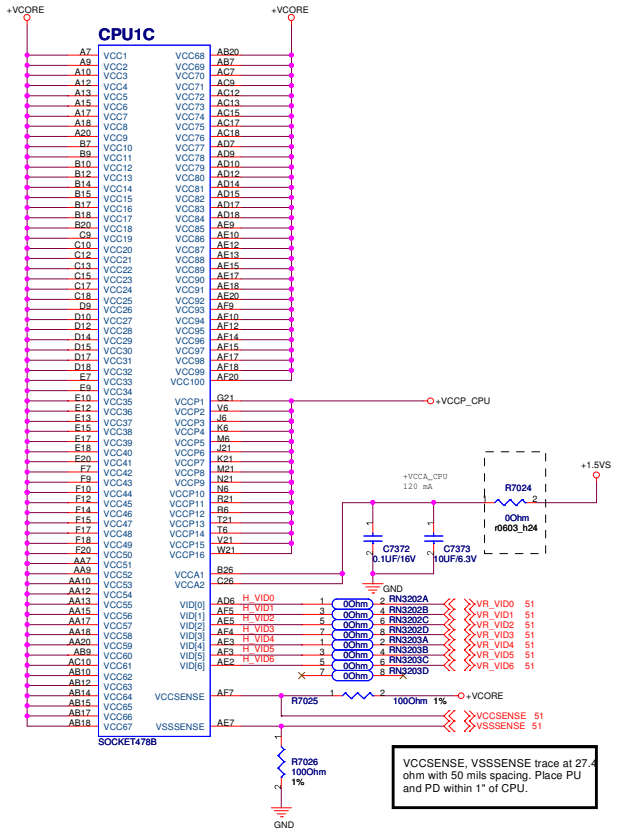
Title : System Setting

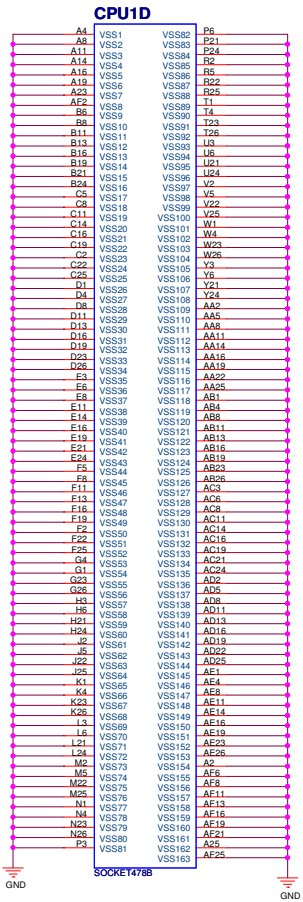
Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.0G

Date: 星期 一, 五月 15, 2007 Sheet 2 of 59


6 H_D#[63:0]
H_D#[63:0]
6 H_A#[35:3]
H_A#[35:3]
6 H_REQ#[4:0]
H_REQ#[4:0]
CPU1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
TCK
H CLK
RESERVED
SOCKET478B
CPU1B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
SOCKET478B
+VCCP_CPU
R7006 56Ohm /X
R7007 1KOhm 1%
R7011 2KOhm 1%
C7371 0.1UF/10V
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5"
R7008 27.4Ohm 1%
R7009 54.9Ohm
R7010 27.4Ohm 1%
R7013 54.9Ohm
R7015 1KOhm 1% /X
R7016 68Ohm
Q4103 H2N7002
R7017 54.9Ohm /X
R7018 54.9Ohm /X
R7019 54.9Ohm /X
R7021 54.9Ohm /X
R7022 54.9Ohm /X
R170 1KOhm 1% /X
R172 1KOhm 1% /X
C618 0.1UF/10V /X
GND
THRO_CPU 31
Title : MEROM CPU (1)
ASUSTeK COMPUTER INC
Engineer: Mike Lee
Size Custom
Project Name Z62E
Rev 2.0G
Date: 星期二, 五月 15, 2007
Sheet 3 of 59

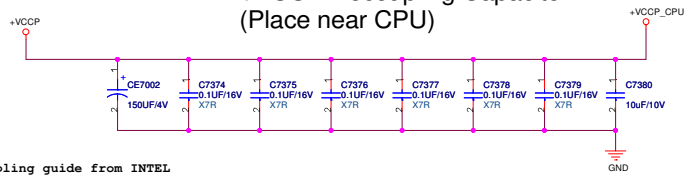




<Variant Name>

ASUSTeK COMPUTER INC	Title : MEROM CPU (2)	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z62E	Rev: 2.0G
Date: 星期二, 五月 15, 2007	Sheet 4 of 59	

+VCCP Decoupling Capacitor
(Place near CPU)



Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

<Variant Name>

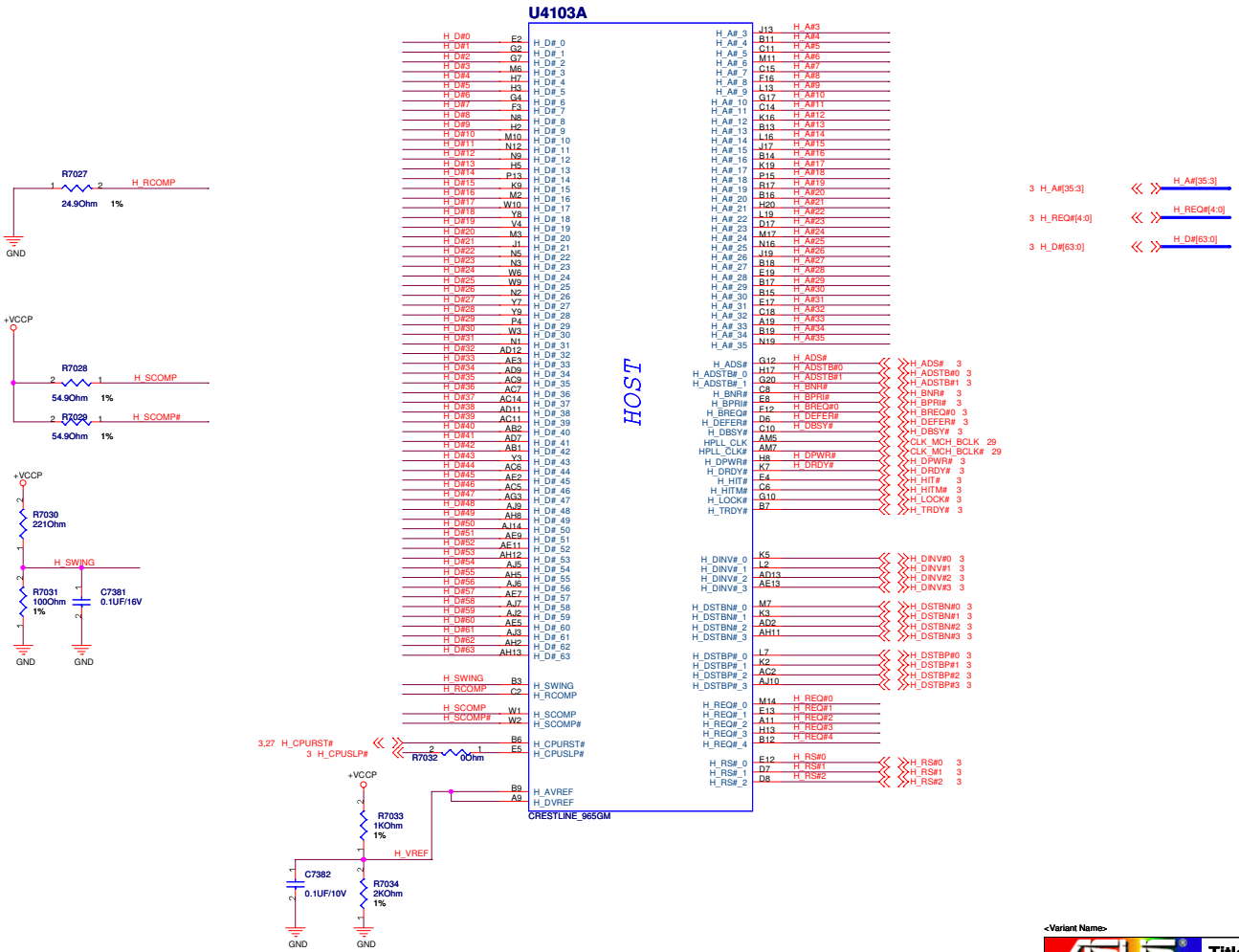
ASUSTek COMPUTER INC. NB1

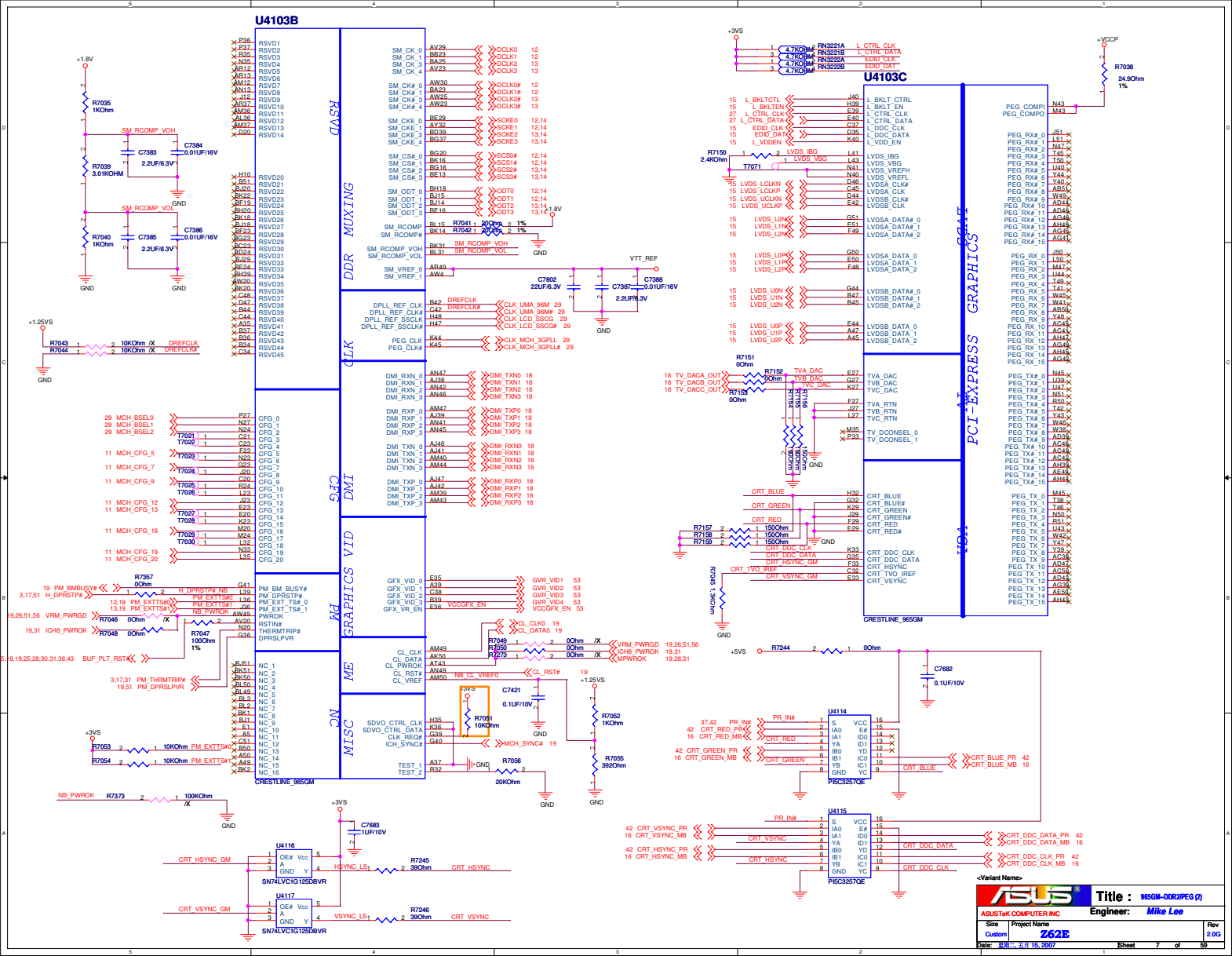
Title : CPU CAP and HOLES

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 5 of 59


U4103A
HOST
CRESTLINE_965GM
R7027
24.9Ohm 1%
H_RCOMP
GND
+VCCP
R7028
54.9Ohm 1%
H_SCOMP
R7029
54.9Ohm 1%
H_SCOMP#
R7030
221Ohm
H_SWING
R7031
100Ohm
1%
C7381
0.1UF/16V
R7032
0Ohm
3,27 H_CPURST#
3 H_CPUSLP#
R7033
1KOhm
1%
H_VREF
C7382
0.1UF/10V
R7034
2KOhm
1%
3 H_A#[35:3]
H_A#[35:3]
3 H_REQ#[4:0]
H_REQ#[4:0]
3 H_D#[63:0]
H_D#[63:0]


U4103B
RSVD
DDR MUXING
CLK
DMI
CRT
VID
GRAPHICS
PM
ME
MISC
CRESTLINE_965GM
U4103C
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_965GM
+1.8V
+1.25VS
+3VS
+5VS
+VCCP
VTT_REF
GND
R7035 1KOhm
R7039 3.01KOHM
R7040 1KOhm
SM_RCOMP_VOH
SM_RCOMP_VOL
C7383 2.2UF/6.3V
C7384 0.01UF/16V
C7385 2.2UF/6.3V
C7386 0.01UF/16V
R7043 10KOhm /X DREFCLK
R7044 10KOhm /X DREFCLK#
C7802 22UF/6.3V
C7387 2.2UF/6.3V
C7388 0.01UF/16V
R7041 200Ohm 1%
R7042 200Ohm 1%
R7357 0Ohm
R7046 0Ohm /X
R7047 100Ohm 1%
R7048 0Ohm
R7049 0Ohm /X
R7273 0Ohm /X
R7053 10KOhm PM_EXTTS#0
R7054 10KOhm PM_EXTTS#1
R7373 100KOhm /X
R7051 10KOhm
R7052 1KOhm
R7055 392Ohm
R7056 20KOhm
C7421 0.1UF/10V
C7689 1UF/10V
R7245 39Ohm
R7246 39Ohm
U4116 SN74LVC1G125DBVR
U4117 SN74LVC1G125DBVR
HSYNC_LS1
VSYNC_LS1
CRT_HSYNC_GM
CRT_VSYNC_GM
CRT_HSYNC
CRT_VSYNC
R7150 2.4KOhm
T7071
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
R7151 0Ohm
R7152 0Ohm
R7153 150Ohm
R7154 150Ohm
R7155 150Ohm
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL_0
TV_DCONSEL_1
R7157 150Ohm
R7158 150Ohm
R7159 150Ohm
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC_GM
CRT_TVO_IREF
CRT_VSYNC_GM
R7045 1.24KOhm
R7244 0Ohm
C7682 0.1UF/10V
U4114 P5C3257QE
U4115 P5C3257QE
PR_IN#
CRT_RED_PR
CRT_RED_MB
CRT_GREEN_PR
CRT_GREEN_MB
CRT_BLUE_PR
CRT_BLUE_MB
CRT_VSYNC_PR
CRT_VSYNC_MB
CRT_HSYNC_PR
CRT_HSYNC_MB
CRT_DDC_DATA_PR
CRT_DDC_DATA_MB
CRT_DDC_CLK_PR
CRT_DDC_CLK_MB
RN3221A 4.7KOhm
RN3221B 4.7KOhm
RN3222A 4.7KOhm
RN3222B 4.7KOhm
L_CTRL_CLK
L_CTRL_DATA
EDID_CLK
EDID_DAT
R7038 24.9Ohm 1%
<Variant Name>
Title : 965GM-DDR2/PEG (2)
Engineer: Mike Lee
ASUSTeK COMPUTER INC
Size: Custom
Project Name: Z62E
Rev: 2.0G
Date: 星期二, 五月 15, 2007
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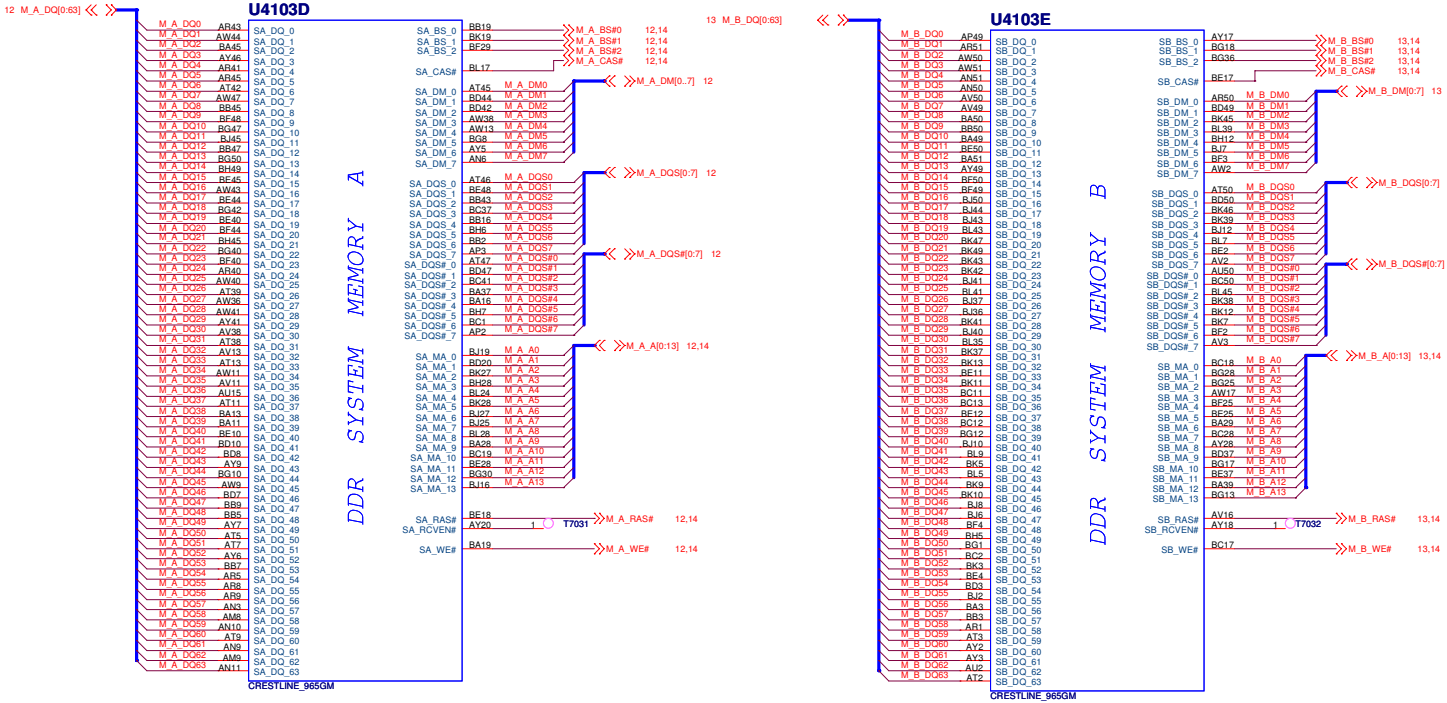


<Variant Name>

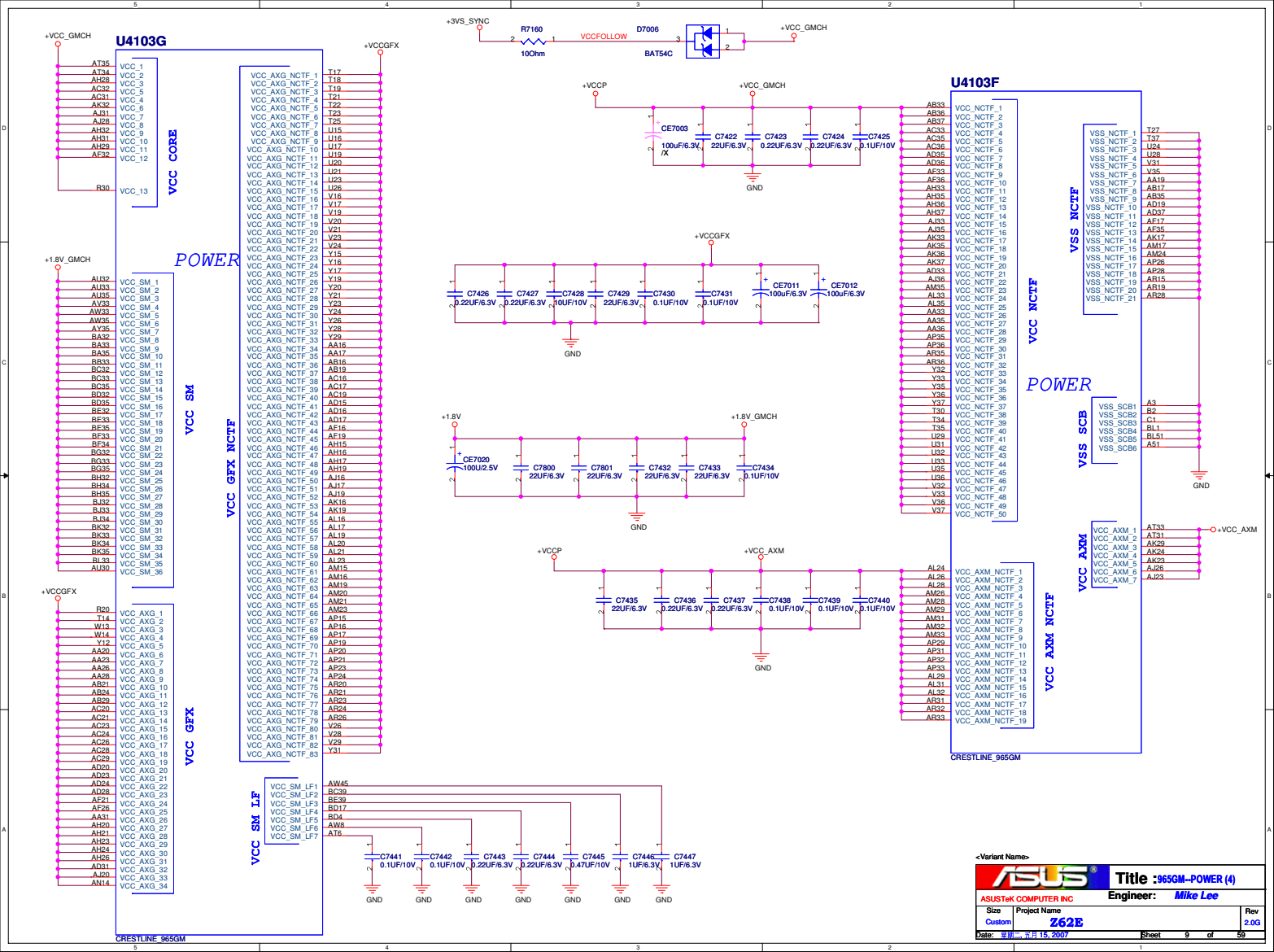
ASUSTeK COMPUTER INC

Title : 965GM--DDR2 bus (3)

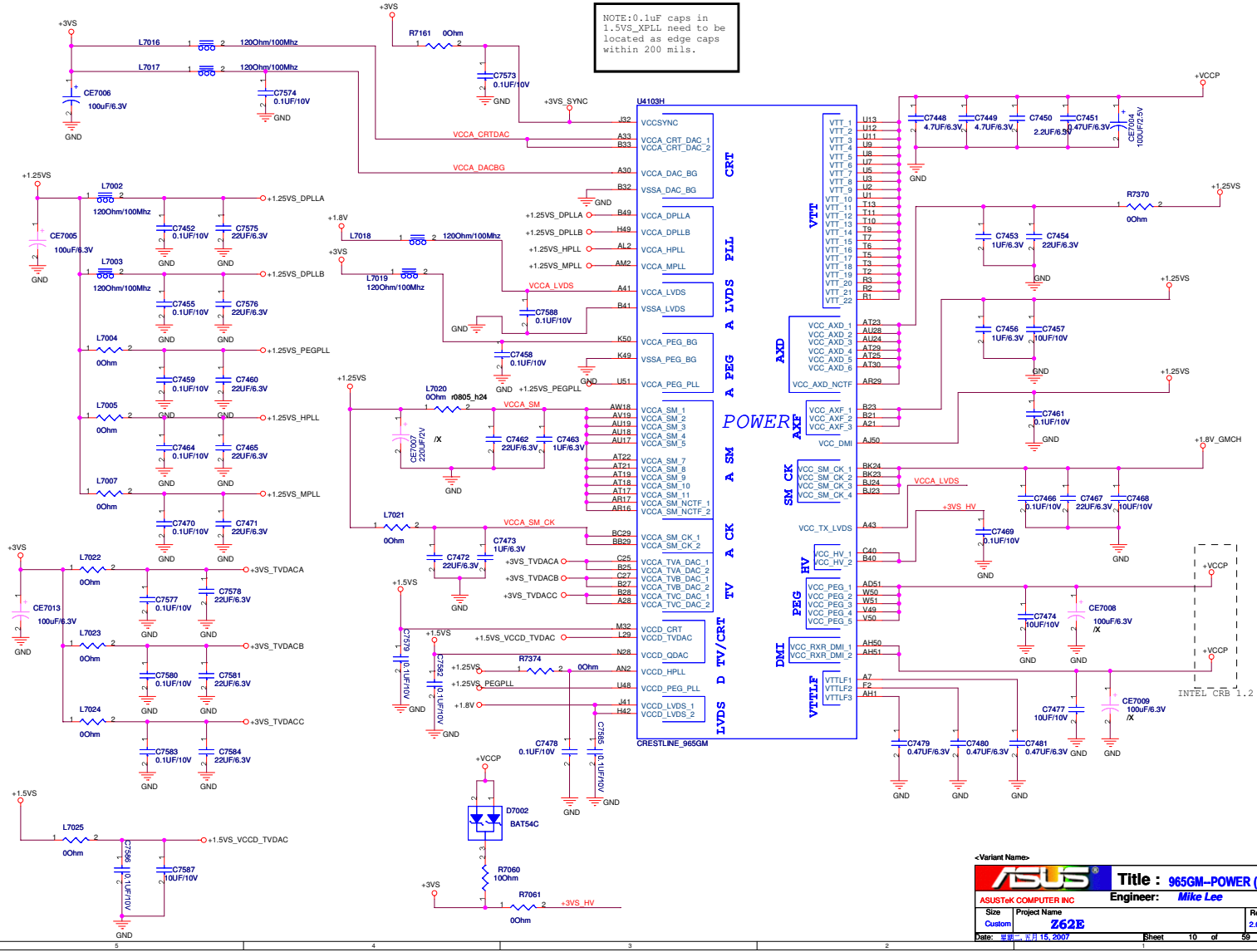
Engineer: Mike Lee

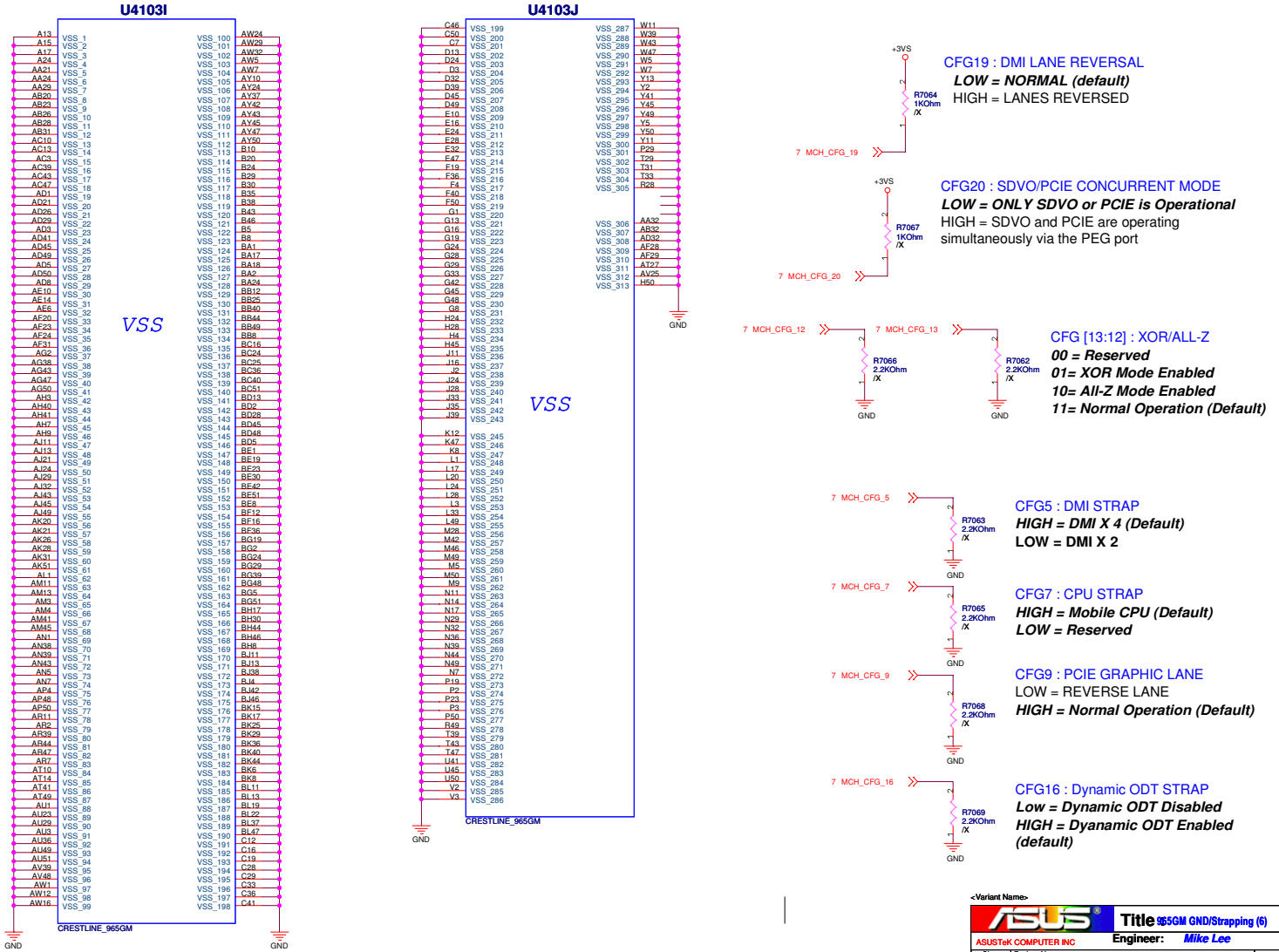
Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 8 of 59


U4103G
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_965GM
POWER
+VCC_GMCH
+VCCGFX
+1.8V_GMCH
+3VS_SYNC
R7160
10Ohm
VCCFOLLOW
D7006
BAT54C
U4103F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+VCCP
+VCC_AXM
+1.8V
CE7003
100uF/6.3V
/X
C7422
C7423
C7424
C7425
0.22UF/6.3V
0.1UF/10V
C7426
C7427
C7428
C7429
C7430
C7431
10UF/10V
22UF/6.3V
CE7011
CE7012
100uF/6.3V
CE7020
100U/2.5V
C7800
C7801
C7432
C7433
C7434
C7435
C7436
C7437
C7438
C7439
C7440
C7441
C7442
C7443
C7444
C7445
C7446
C7447
0.47UF/10V
1UF/6.3V
GND

<Variant Name>
ASUSTeK COMPUTER INC
Title :965GM--POWER (4)
Engineer: Mike Lee
Size: Custom
Project Name: Z62E
Rev: 2.0G
Date: 星期二, 五月 15, 2007
Sheet 9 of 59


NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
U4103H
CRESTLINE_965GM
POWER
CRT
PLL
LVDS
PEG
SM
CK
TV
HV
AXD
AXF
SM CK
PEG
DMI
VTT
VTTLF
LVDS
TV/CRT
VCCSYNC
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
VCCA_SM_10
VCCA_SM_11
VCCA_SM_NCTF_1
VCCA_SM_NCTF_2
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_TVA_DAC_1
VCCA_TVA_DAC_2
VCCA_TVB_DAC_1
VCCA_TVB_DAC_2
VCCA_TVC_DAC_1
VCCA_TVC_DAC_2
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS_1
VCCD_LVDS_2
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VCC_AXD_1
VCC_AXD_2
VCC_AXD_3
VCC_AXD_4
VCC_AXD_5
VCC_AXD_6
VCC_AXD_NCTF
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
VCC_DMI
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
VCC_TX_LVDS
VCC_HV_1
VCC_HV_2
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
VCC_RXR_DMI_1
VCC_RXR_DMI_2
VTTLF1
VTTLF2
VTTLF3
VCCA_CRTDAC
VCCA_DACBG
VCCA_LVDS
VCCA_SM
VCCA_SM_CK
+3VS_SYNC
+1.25VS_DPLLA
+1.25VS_DPLLB
+1.25VS_HPLL
+1.25VS_MPLL
+1.25VS_PEGPLL
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
+1.25VS_VCCD_TVDAC
+3VS_HV
+VCCP
INTEL CRB 1.2
Title : 965GM--POWER (5)
ASUSTeK COMPUTER INC
Engineer: Mike Lee
Size: Custom
Project Name: Z62E
Rev: 2.0G
Date: 星期二, 五月 15, 2007
Sheet 10 of 59
<Variant Name>
HIGH = LANES REVERSED



<Variant Name>

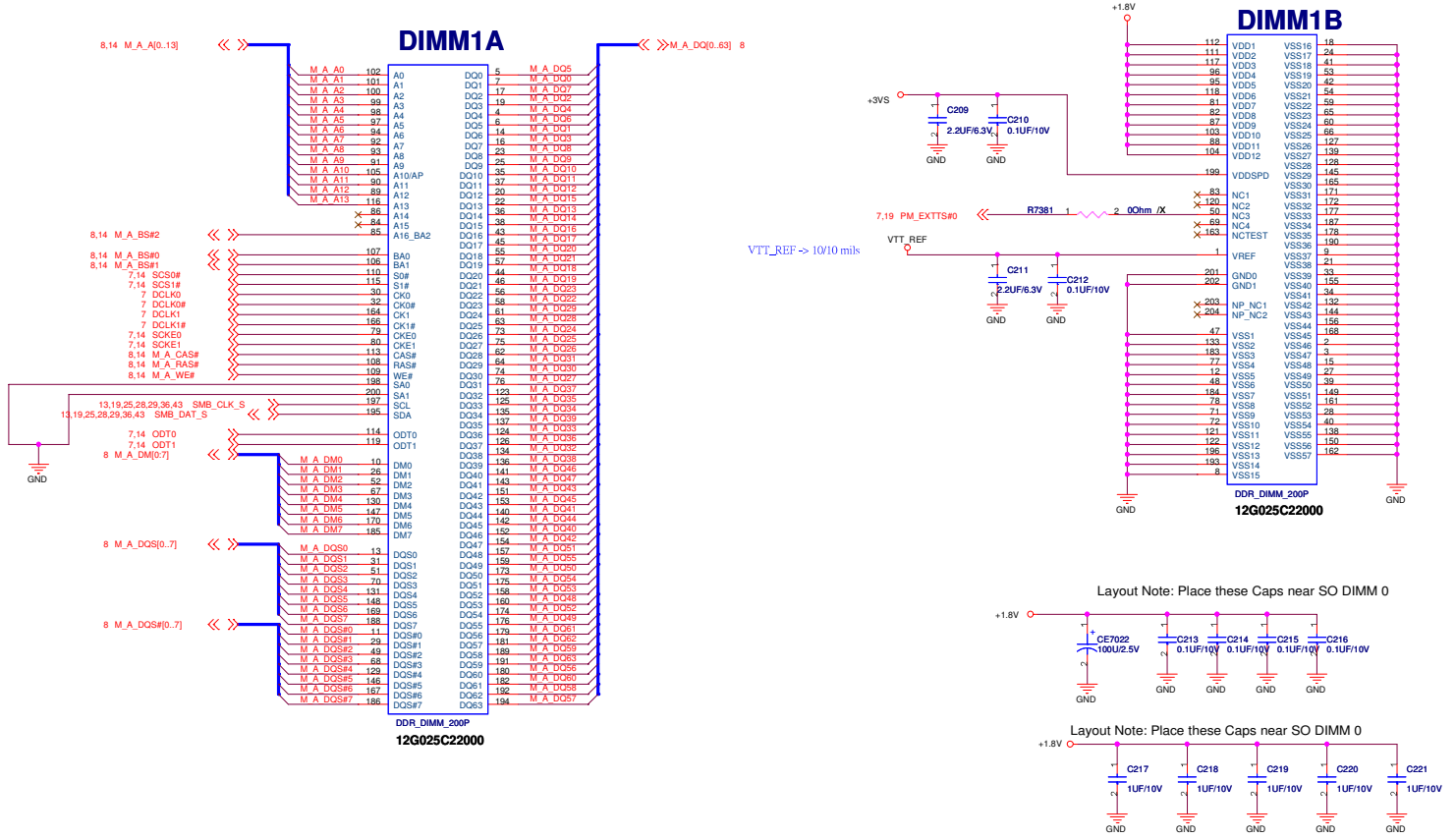
ASUSTeK COMPUTER INC

Title: 965GM GND/Strapping (6)

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 11 of 59



<Variant Name>

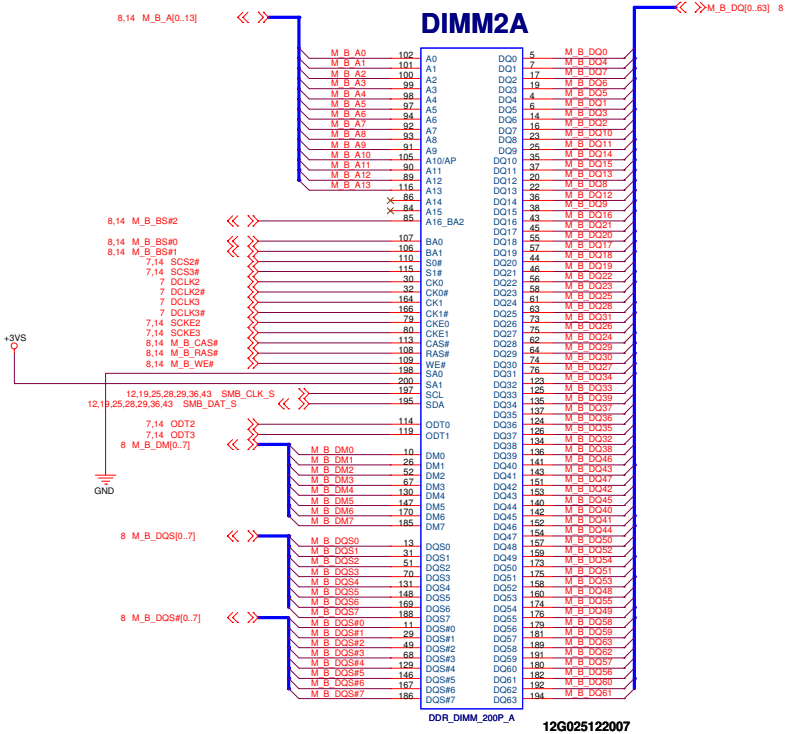
ASUSTeK COMPUTER INC

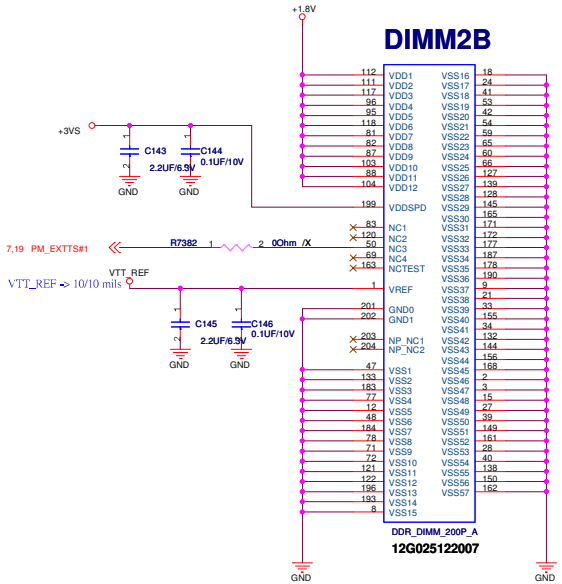
Title : DDR2 SO-DIMM(0)

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

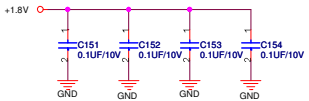
Date: 星期二, 五月 15, 2007 Sheet 12 of 59



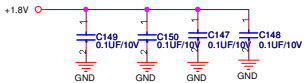


Layout Note: Place these Caps near SO DIMM 1

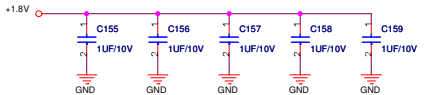
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these resistors near the GMCH



<Variant Name>

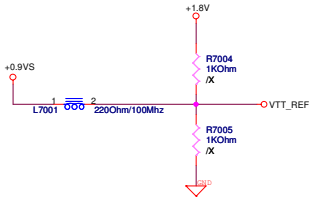
ASUSTeK COMPUTER INC

Title : DDR2_SO-DIMM(1)

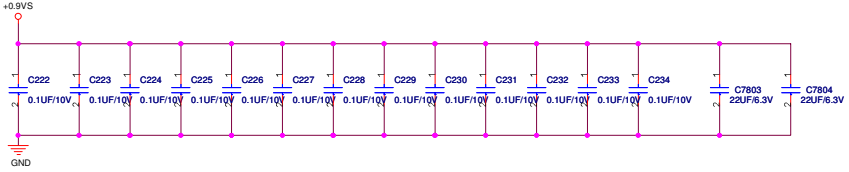
Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

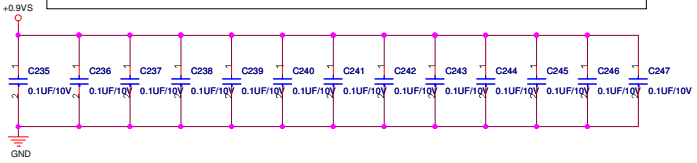
Date: 星期二, 五月 15, 2007 Sheet 13 of 59

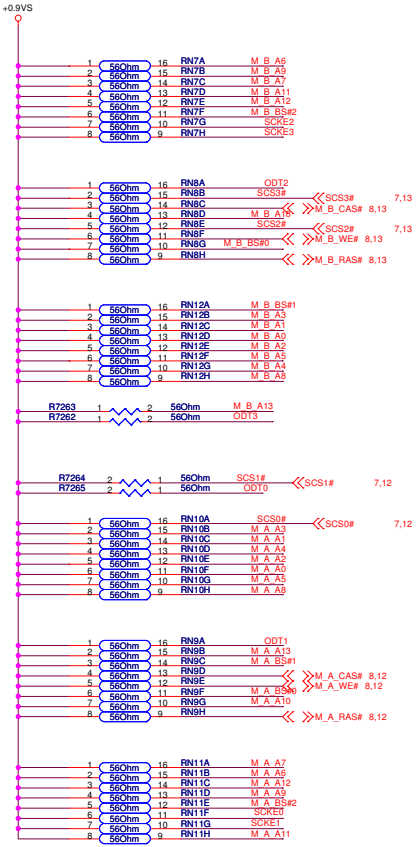


M_A_A[0..13] 8,12
M_A_BS#[0..2] 8,12
M_B_A[0..13] 8,13
M_B_BS#[0..2] 8,13
SCKE[0:3] 7,12,13
ODT[0:3] 7,12,13



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





<Variant Name>

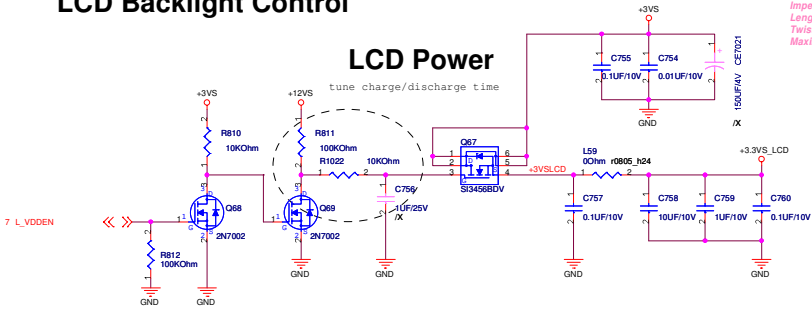
ASUSTeK COMPUTER INC	Title : DDR2 TERM	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z62E	Rev: 2.0G
Date: 星期二, 五月 15, 2007	Sheet 14 of 59	

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

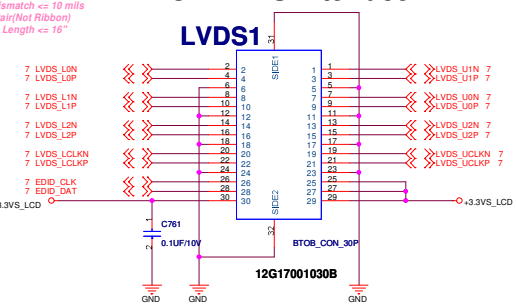
LCD Power

tune charge/discharge time

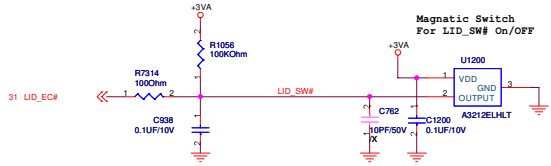


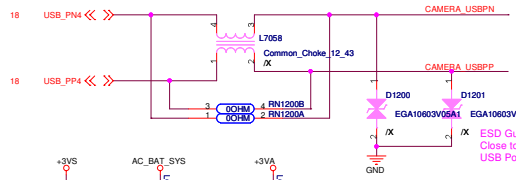
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

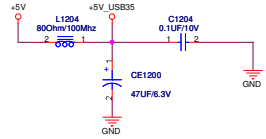
LCD LVDS Interface



LVDS NUT
H4042
L4E_1A
GND

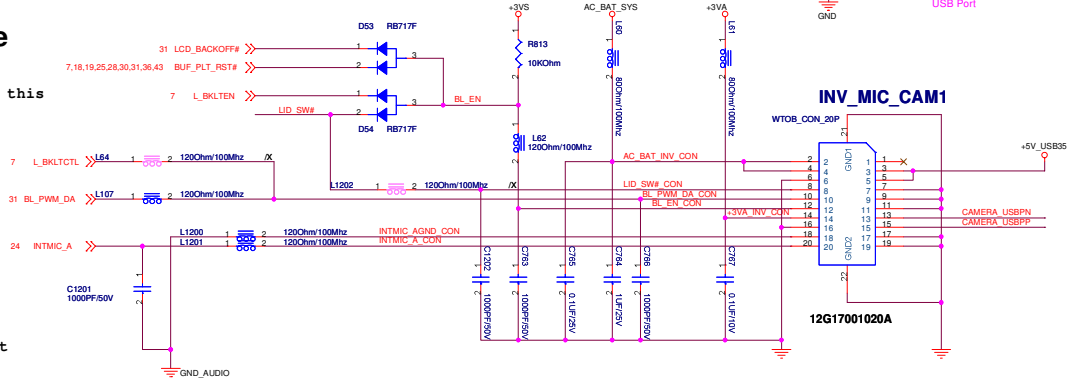






INVERTER Interface

BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



INVERTER NUT
H4039
L4E_1A
GND

BIOS
BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back light.

Inverter Board built in 14.1W LCD Panel

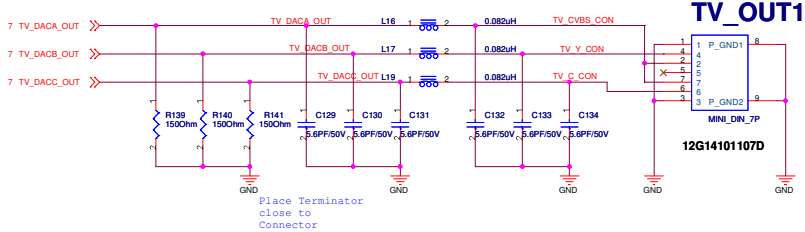
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 _ 五月 15, 2007	Sheet 15 of 59	

TV OUT

checklist suggests
150ohm/100MHz &
6pF

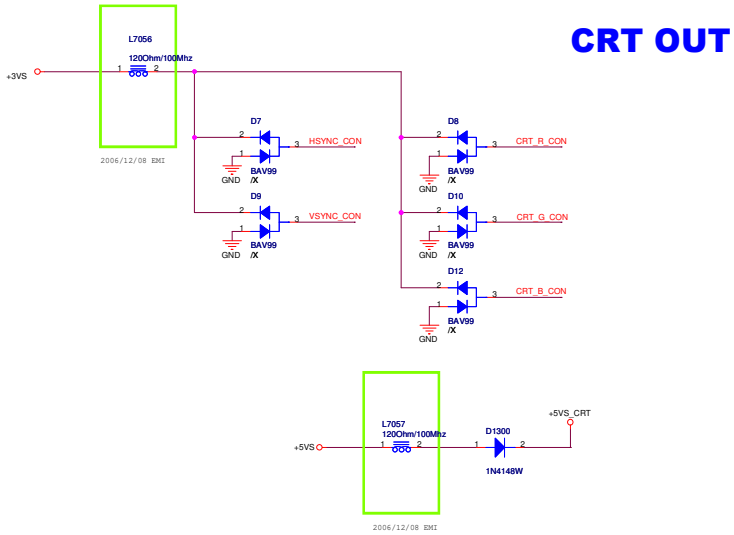


Place Terminator
close to
Connector

TV_OUT1

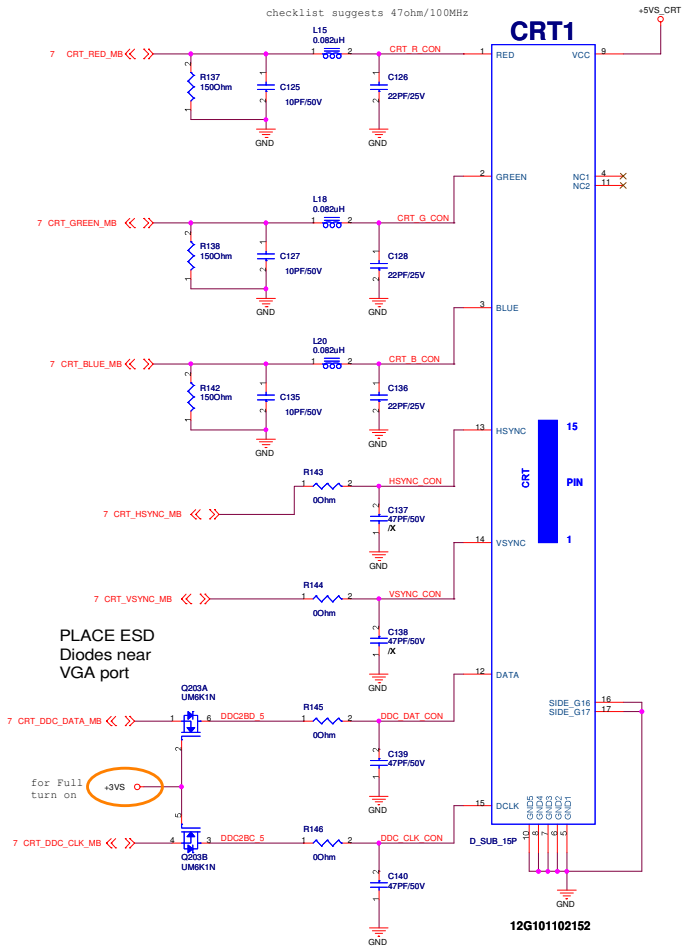
12G14101107D

CRT OUT

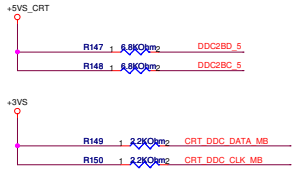


checklist suggests 47ohm/100MHz

CRT1



12G101102152



<Variant Name>

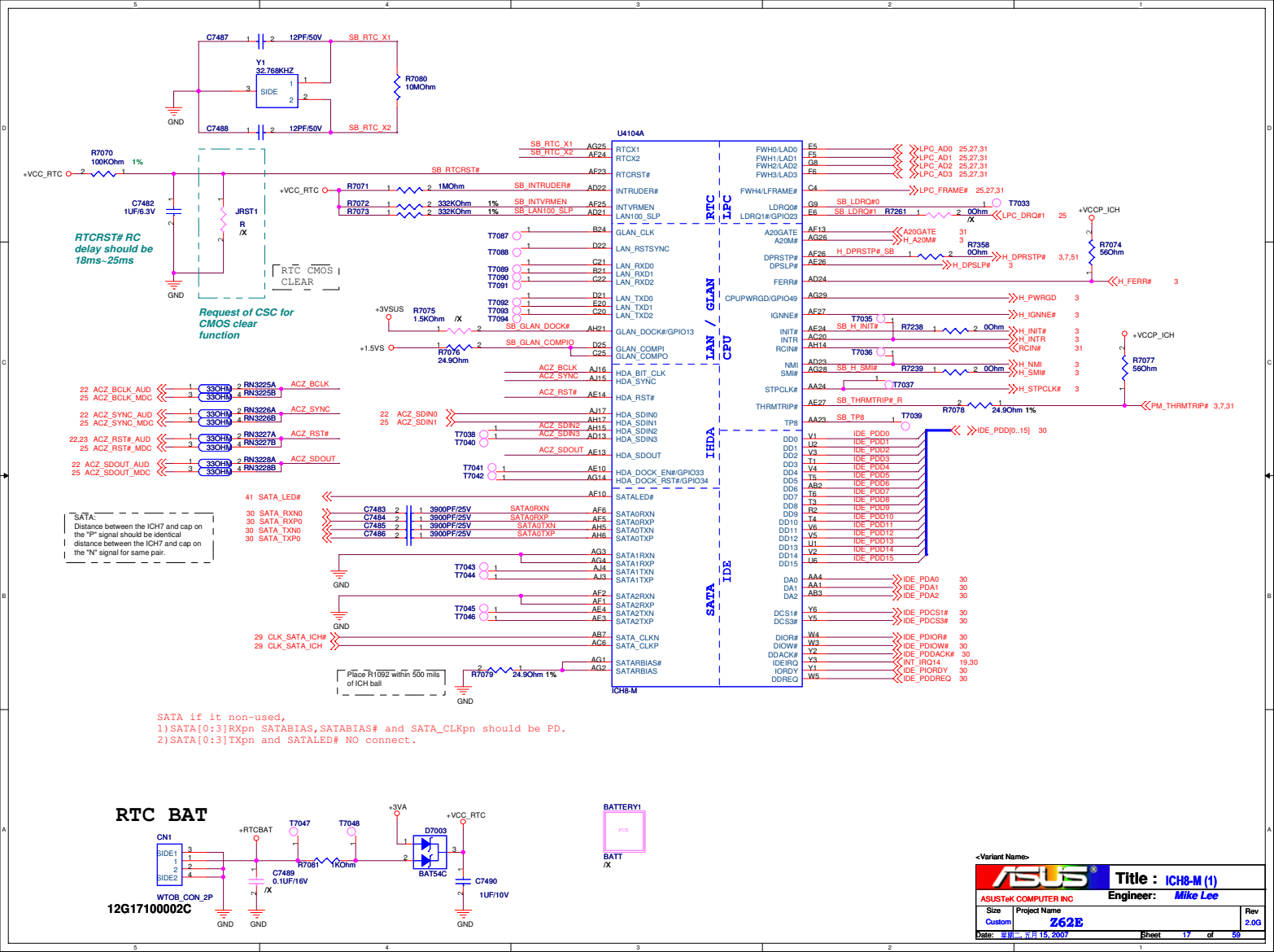
Title : CRT & TV OUT

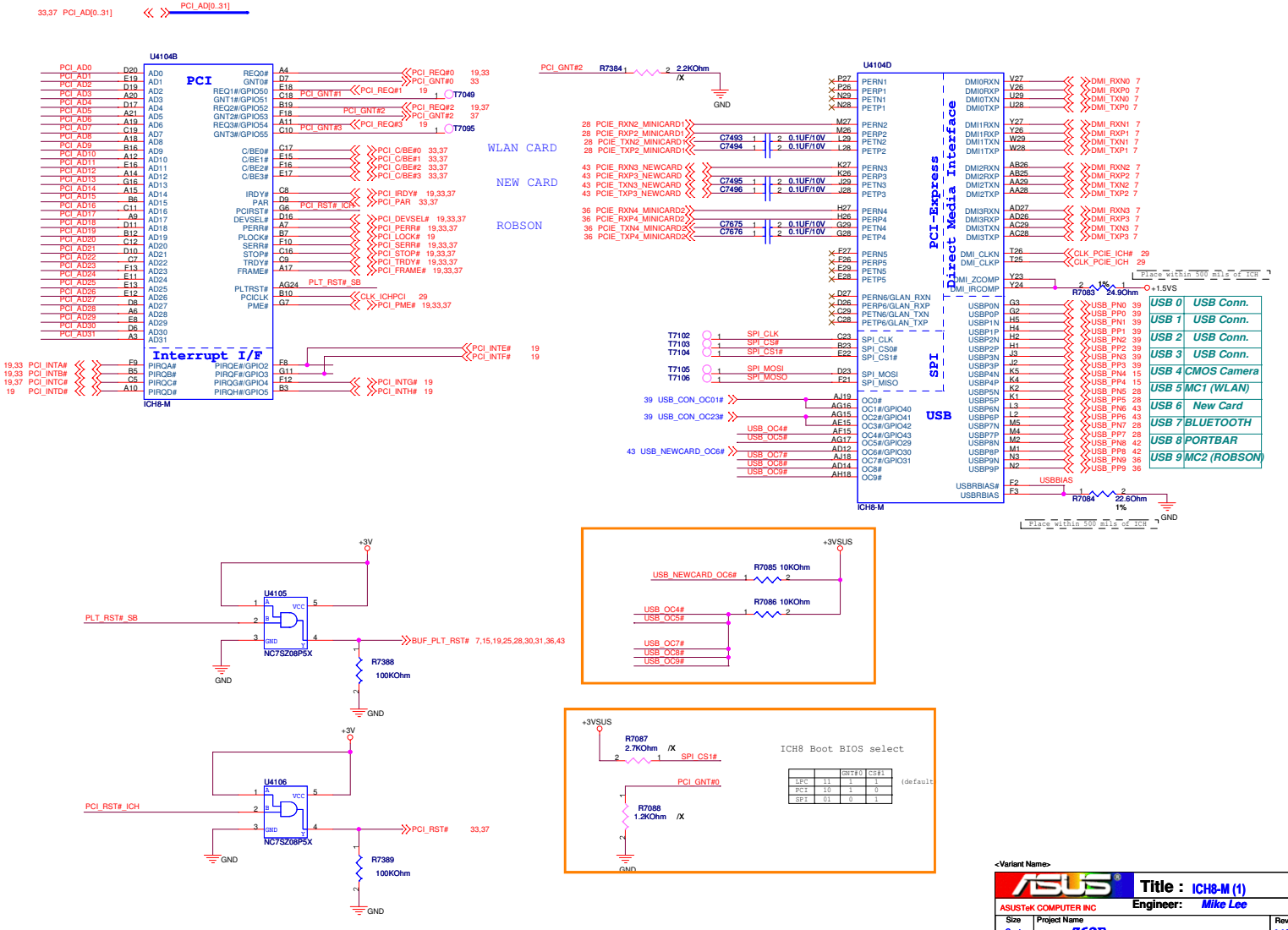
ASUSTeK COMPUTER INC

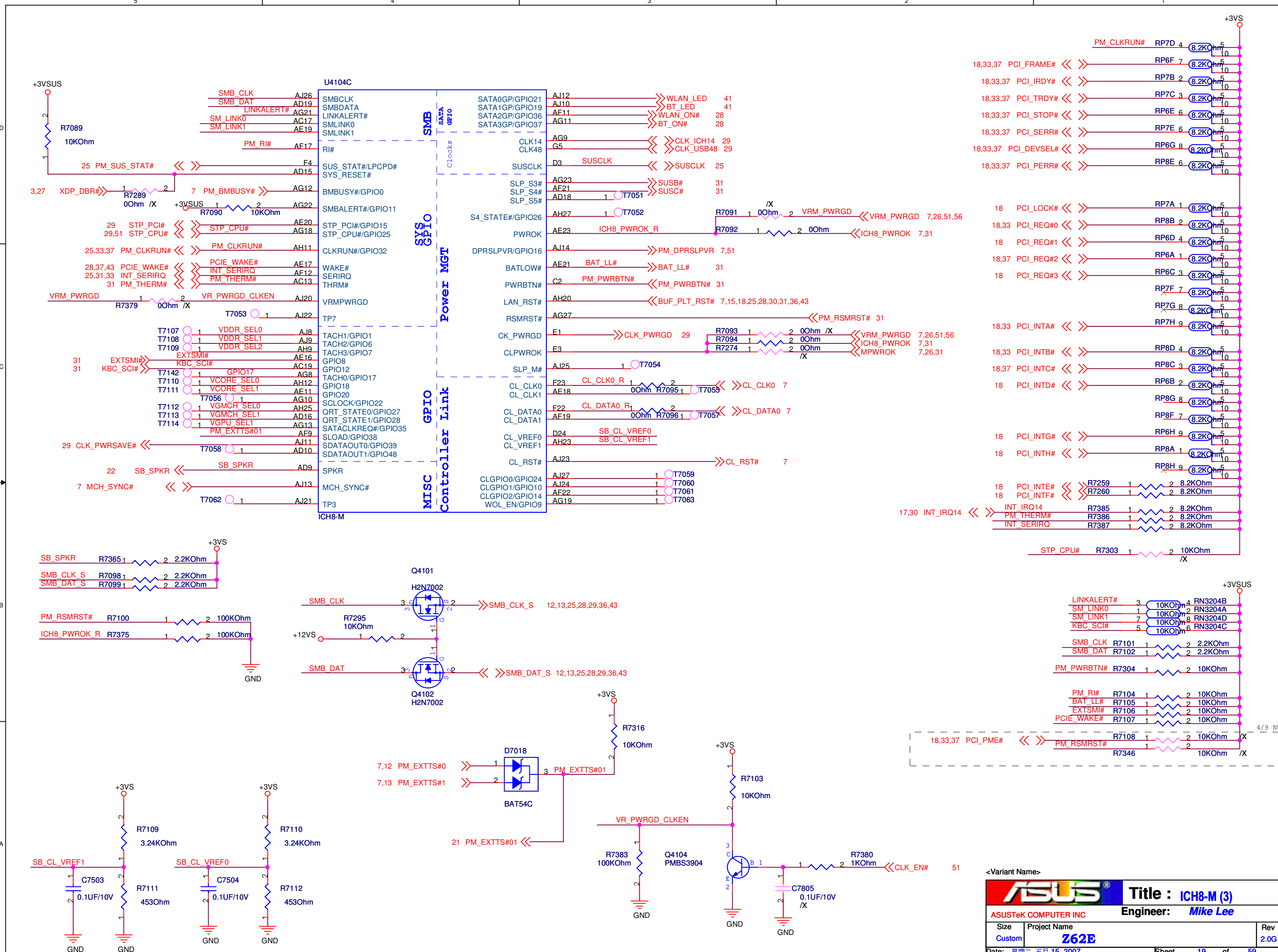
Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.0G

Date: 星期 _ 五月 15, 2007 Sheet 16 of 59


C7487 12PF/50V SB_RTC_X1
Y1 32.768KHZ SIDE
R7080 10MOhm
C7488 12PF/50V SB_RTC_X2
GND
U4104A
RTCX1 AG25
RTCX2 AF24
SB_RTC_X1
SB_RTC_X2
R7070 100KOhm 1%
+VCC_RTC
SB_RTCRST# AF23
RTCRST#
C7482 1UF/6.3V
JRST1
R /X
RTC CMOS CLEAR
RTCRST# RC delay should be 18ms~25ms
Request of CSC for CMOS clear function
R7071 1MOhm SB_INTRUDER# AD22
INTRUDER#
R7072 332KOhm 1% SB_INTVRMEN AF25
R7073 332KOhm 1% SB_LAN100_SLP AD21
INTVRMEN
LAN100_SLP
RTC
LPC
FWH0/LAD0 E5
FWH1/LAD1 F5
FWH2/LAD2 G8
FWH3/LAD3 F6
LPC_AD0 25,27,31
LPC_AD1 25,27,31
LPC_AD2 25,27,31
LPC_AD3 25,27,31
FWH4/LFRAME# C4
LPC_FRAME# 25,27,31
LDRQ0# G9 SB_LDRQ#0
LDRQ1#/GPIO23 E6 SB_LDRQ#1 R7261 0Ohm /X
T7033
LPC_DRQ#1 25
+VCCP_ICH
R7074 56Ohm
T7087 B24
T7088 D22
GLAN_CLK
LAN_RSTSYNC
T7089 C21
T7090 B21
T7091 C22
LAN_RXD0
LAN_RXD1
LAN_RXD2
T7092 D21
T7093 E20
T7094 C20
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN / CPU
+3VSUS R7075 1.5KOhm /X
SB_GLAN_DOCK# AH21
GLAN_DOCK#/GPIO13
+1.5VS R7076 24.9Ohm
SB_GLAN_COMPIO D25
C25
GLAN_COMPI
GLAN_COMPO
A20GATE AF13
A20M# AG26
A20GATE 31
H_A20M# 3
R7358 0Ohm
DPRSTP# AF26 H_DPRSTP#_SB
DPSLP# AE26
H_DPRSTP# 3,7,51
H_DPSLP# 3
FERR# AD24
H_FERR# 3
CPUPWRGD/GPIO49 AG29
H_PWRGD 3
IGNNE# AF27
T7035
H_IGNNE# 3
INIT# AE24 SB_H_INIT#
R7238 0Ohm
H_INIT# 3
INTR AC20
H_INTR 3
RCIN# AH14
RCIN# 31
T7036
NMI AD23
SMI# AG28 SB_H_SMI#
R7239 0Ohm
H_NMI 3
H_SMI# 3
STPCLK# AA24
T7037
H_STPCLK# 3
THRMTRIP# AE27 SB_THRMTRIP#_R
R7078 24.9Ohm 1%
PM_THRMTRIP# 3,7,31
TP8 AA23 SB_TP8
T7039
HDA_BIT_CLK AJ16
HDA_SYNC AJ15
HDA_RST# AE14
HDA_SDIN0 AJ17
HDA_SDIN1 AH17
HDA_SDIN2 AH15
HDA_SDIN3 AD13
HDA_SDOUT AE13
HDA_DOCK_EN#/GPIO33 AE10
HDA_DOCK_RST#/GPIO34 AG14
SATALED# AE10
IHDA
SATA
IDE
22 ACZ_BCLK_AUD 25 ACZ_BCLK_MDC
33OHM RN3225A RN3225B ACZ_BCLK
22 ACZ_SYNC_AUD 25 ACZ_SYNC_MDC
RN3226A RN3226B ACZ_SYNC
22,23 ACZ_RST#_AUD 25 ACZ_RST#_MDC
RN3227A RN3227B ACZ_RST#
22 ACZ_SDOUT_AUD 25 ACZ_SDOUT_MDC
RN3228A RN3228B ACZ_SDOUT
22 ACZ_SDIN0 25 ACZ_SDIN1
T7038 T7040
ACZ_SDIN2 ACZ_SDIN3
41 SATA_LED#
30 SATA_RXN0 30 SATA_RXP0 30 SATA_TXN0 30 SATA_TXP0
C7483 C7484 C7485 C7486 3900PF/25V
SATA0RXN SATA0RXP SATA0TXN SATA0TXP
SATA0RXN AF6
SATA0RXP AF5
SATA0TXN AH5
SATA0TXP AH6
SATA1RXN AG3
SATA1RXP AG4
SATA1TXN AJ4
SATA1TXP AJ3
T7043 T7044
SATA2RXN AF2
SATA2RXP AF1
SATA2TXN AE4
SATA2TXP AE3
T7045 T7046
29 CLK_SATA_ICH# 29 CLK_SATA_ICH
SATA_CLKN AB7
SATA_CLKP AC6
SATARBIAS# AG1
SATARBIAS AG2
Place R1092 within 500 mils of ICH ball
R7079 24.9Ohm 1%
SATA:
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.
ICH8-M
DD0 V1 IDE_PDD0
DD1 U2 IDE_PDD1
DD2 V3 IDE_PDD2
DD3 T1 IDE_PDD3
DD4 V4 IDE_PDD4
DD5 T5 IDE_PDD5
DD6 AB2 IDE_PDD6
DD7 T6 IDE_PDD7
DD8 T3 IDE_PDD8
DD9 R2 IDE_PDD9
DD10 T4 IDE_PDD10
DD11 V6 IDE_PDD11
DD12 V5 IDE_PDD12
DD13 U1 IDE_PDD13
DD14 V2 IDE_PDD14
DD15 U6 IDE_PDD15
IDE_PDD[0..15] 30
DA0 AA4 IDE_PDA0 30
DA1 AA1 IDE_PDA1 30
DA2 AB3 IDE_PDA2 30
DCS1# Y6 IDE_PDCS1# 30
DCS3# Y5 IDE_PDCS3# 30
DIOR# W4 IDE_PDIOR# 30
DIOW# W3 IDE_PDIOW# 30
DDACK# Y2 IDE_PDDACK# 30
IDEIRQ Y3 INT_IRQ14 19,30
IORDY Y1 IDE_PIORDY 30
DDREQ W5 IDE_PDDREQ 30
SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.
RTC BAT
CN1
SIDE1 SIDE2
WTOB_CON_2P
12G17100002C
+RTCBAT
C7489 0.1UF/16V /X
T7047 T7048
R7081 1KOhm
+3VA
D7003 BAT54C
+VCC_RTC
C7490 1UF/10V
GND
BATTERY1
BATT
/X
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICH8-M (1)
Engineer: Mike Lee
Size Custom
Project Name Z62E
Rev 2.0G
Date: 星期二, 五月 15, 2007
Sheet 17 of 59


33,37 PCI_AD[0..31]
PCI_AD[0..31]
U4104B
PCI
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
C/BE0# C/BE1# C/BE2# C/BE3#
IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PLTRST# PCICLK PME#
PCI_REQ#0 19,33
PCI_GNT#0 33
PCI_REQ#1 19
PCI_GNT#1
T7049
PCI_REQ#2 19,37
PCI_GNT#2 37
PCI_REQ#3 19
PCI_GNT#3
T7095
PCI_C/BE#0 33,37
PCI_C/BE#1 33,37
PCI_C/BE#2 33,37
PCI_C/BE#3 33,37
PCI_IRDY# 19,33,37
PCI_PAR 33,37
PCI_RST#_ICH
PCI_DEVSEL# 19,33,37
PCI_PERR# 19,33,37
PCI_LOCK# 19
PCI_SERR# 19,33,37
PCI_STOP# 19,33,37
PCI_TRDY# 19,33,37
PCI_FRAME# 19,33,37
PLT_RST#_SB
CLK_ICHPCI 29
PCI_PME# 19,33,37
WLAN CARD
NEW CARD
ROBSON
Interrupt I/F
PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
PCI_INTE# 19
PCI_INTF# 19
PCI_INTG# 19
PCI_INTH# 19
19,33 PCI_INTA#
19,33 PCI_INTB#
19,37 PCI_INTC#
19 PCI_INTD#
ICH8-M
PCI_GNT#2
R7384 2.2KOhm /X
GND
U4104D
PCI-Express
Direct Media Interface
PERN1 PERP1 PERN2 PERP2 PERN3 PERP3 PERN4 PERP4 PERN5 PERP5 PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP
DMI0RXN DMI0RXP DMI0TXN DMI0TXP DMI1RXN DMI1RXP DMI1TXN DMI1TXP DMI2RXN DMI2RXP DMI2TXN DMI2TXP DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_CLKN DMI_CLKP DMI_ZCOMP DMI_IRCOMP
DMI_RXN0 7
DMI_RXP0 7
DMI_TXN0 7
DMI_TXP0 7
DMI_RXN1 7
DMI_RXP1 7
DMI_TXN1 7
DMI_TXP1 7
DMI_RXN2 7
DMI_RXP2 7
DMI_TXN2 7
DMI_TXP2 7
DMI_RXN3 7
DMI_RXP3 7
DMI_TXN3 7
DMI_TXP3 7
CLK_PCIE_ICH# 29
CLK_PCIE_ICH 29
Place within 500 mils of ICH
R7083 24.9Ohm
+1.5VS
C7493 0.1UF/10V
C7494 0.1UF/10V
C7495 0.1UF/10V
C7496 0.1UF/10V
C7675 0.1UF/10V
C7676 0.1UF/10V
28 PCIE_RXN2_MINICARD1
28 PCIE_RXP2_MINICARD1
28 PCIE_TXN2_MINICARD1
28 PCIE_TXP2_MINICARD1
43 PCIE_RXN3_NEWCARD
43 PCIE_RXP3_NEWCARD
43 PCIE_TXN3_NEWCARD
43 PCIE_TXP3_NEWCARD
36 PCIE_RXN4_MINICARD2
36 PCIE_RXP4_MINICARD2
36 PCIE_TXN4_MINICARD2
36 PCIE_TXP4_MINICARD2
SPI
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO
T7102 SPI_CLK
T7103 SPI_CS#
T7104 SPI_CS1#
T7105 SPI_MOSI
T7106 SPI_MOSO
USB
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#
39 USB_CON_OC01#
39 USB_CON_OC23#
USB_OC4#
USB_OC5#
43 USB_NEWCARD_OC6#
USB_OC7#
USB_OC8#
USB_OC9#
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P
USB_PN0 39
USB_PP0 39
USB_PN1 39
USB_PP1 39
USB_PN2 39
USB_PP2 39
USB_PN3 39
USB_PP3 39
USB_PN4 15
USB_PP4 15
USB_PN5 28
USB_PP5 28
USB_PN6 43
USB_PP6 43
USB_PN7 28
USB_PP7 28
USB_PN8 42
USB_PP8 42
USB_PN9 36
USB_PP9 36
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 CMOS Camera
USB 5 MC1 (WLAN)
USB 6 New Card
USB 7 BLUETOOTH
USB 8 PORTBAR
USB 9 MC2 (ROBSON)
USBRBIAS# USBRBIAS
USBBIAS
R7084 22.6Ohm 1%
ICH8-M
+3V
U4105
NC7SZ08P5X
PLT_RST#_SB
BUF_PLT_RST# 7,15,19,25,28,30,31,36,43
R7388 100KOhm
GND
U4106
PCI_RST#_ICH
PCI_RST# 33,37
R7389 100KOhm
+3VSUS
R7085 10KOhm
R7086 10KOhm
USB_NEWCARD_OC6#
USB_OC4#
USB_OC5#
USB_OC7#
USB_OC8#
USB_OC9#
R7087 2.7KOhm /X
SPI_CS1#
PCI_GNT#0
R7088 1.2KOhm /X
ICH8 Boot BIOS select
GNT#0 CS#1
LPC 11 1 1
PCI 10 1 0
SPI 01 0 1
(default)
<Variant Name>
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: Mike Lee
Size Custom
Project Name Z62E
Rev 2.0G
Date: 星期二, 五月 15, 2007
Sheet 18 of 59



<Variant Name>

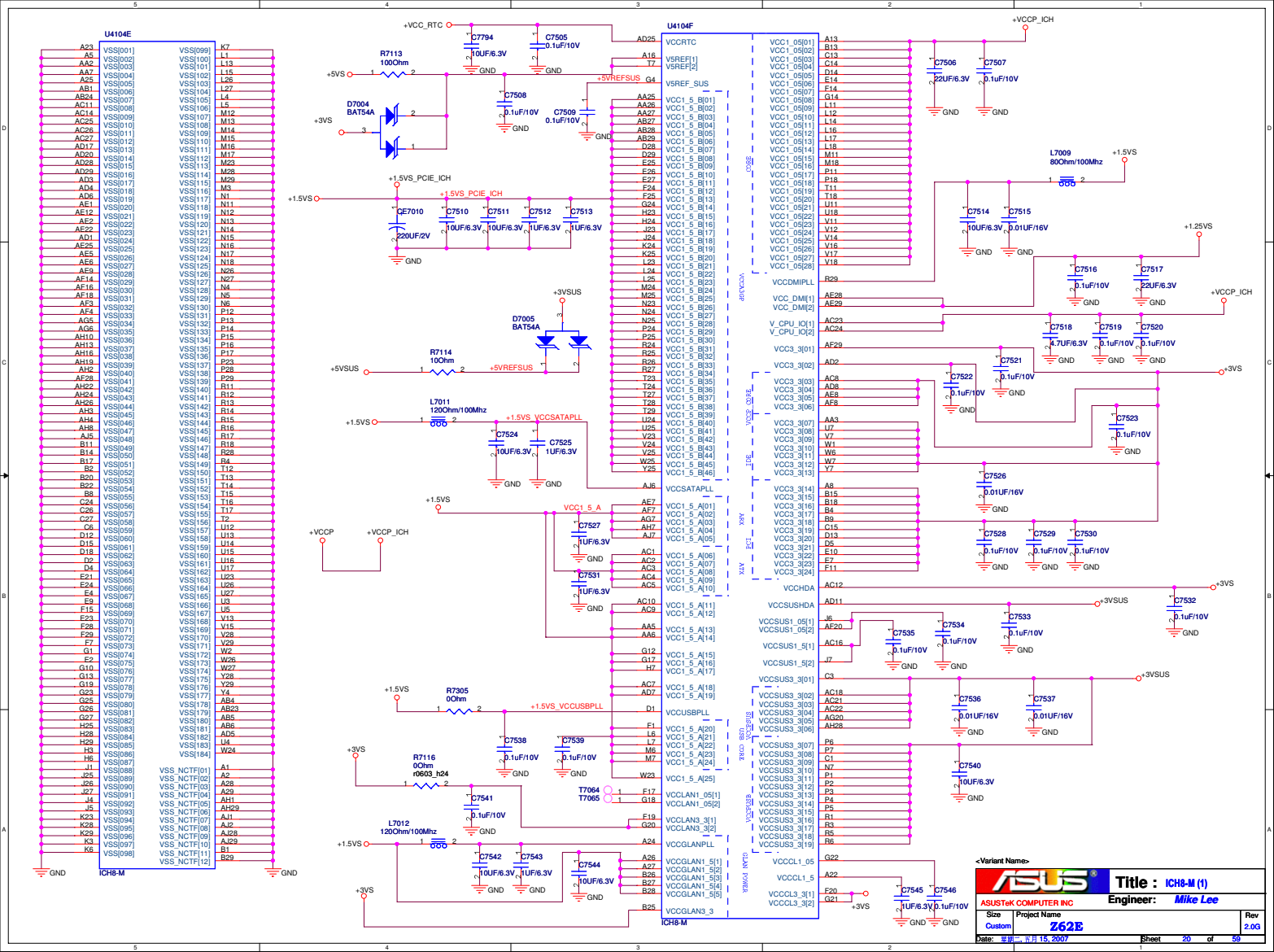
ASUSTeK COMPUTER INC

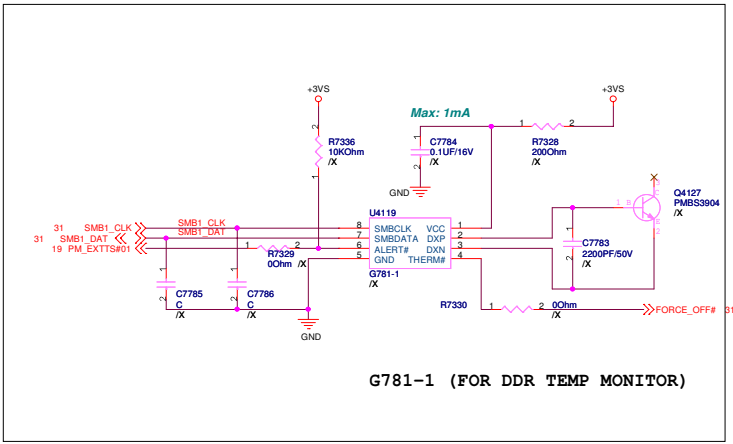
Title : ICH8-M (3)

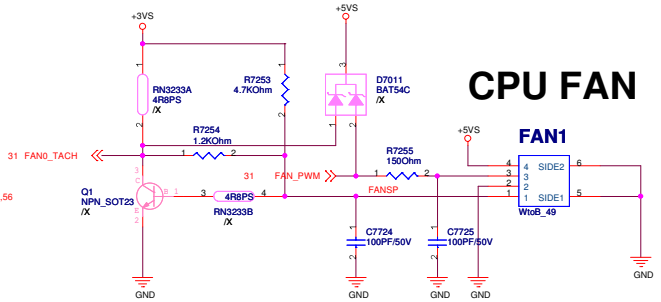
Engineer: *Mike Lee*

Size	Project Name	Rev
Custom	Z62E	2.0G

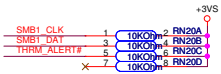
Date: 星期二, 五月 15, 2007 Sheet 19 of 59

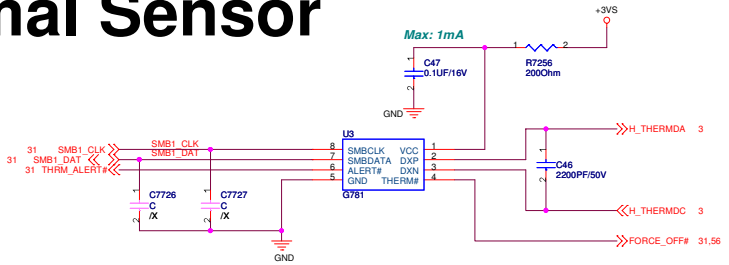

U4104E
ICH8-M
U4104F
ICH8-M
+VCC_RTC
C7794
10UF/6.3V
C7505
0.1uF/10V
R7113
100Ohm
+5VS
D7004
BAT54A
+3VS
C7508
0.1uF/10V
C7509
0.1uF/10V
+5VREFSUS
+1.5VS_PCIE_ICH
+1.5V
Q7010
220UF/2V
C7510
10UF/6.3V
C7511
10UF/6.3V
C7512
1UF/6.3V
C7513
1UF/6.3V
+3VSUS
D7005
BAT54A
R7114
10Ohm
+5VSUS
L7011
120Ohm/100Mhz
+1.5VS_VCCSATAPLL
C7524
10UF/6.3V
C7525
1UF/6.3V
+VCCP
+VCCP_ICH
VCC1_5_A
C7527
1UF/6.3V
C7531
1UF/6.3V
R7305
0Ohm
+1.5VS_VCCUSBPLL
C7538
0.1uF/10V
C7539
0.1uF/10V
R7116
0Ohm
r0603_h24
C7541
0.1uF/10V
L7012
120Ohm/100Mhz
C7542
10UF/6.3V
C7543
1UF/6.3V
C7544
10UF/6.3V
T7064
T7065
C7506
22UF/6.3V
C7507
0.1uF/10V
L7009
80Ohm/100Mhz
C7514
10UF/6.3V
C7515
0.01UF/16V
+1.25VS
C7516
0.1uF/10V
C7517
22UF/6.3V
C7518
4.7UF/6.3V
C7519
0.1uF/10V
C7520
0.1uF/10V
C7521
0.1uF/10V
C7522
0.1uF/10V
C7523
0.1uF/10V
C7526
0.01UF/16V
C7528
0.1uF/10V
C7529
0.1uF/10V
C7530
0.1uF/10V
C7532
0.1uF/10V
C7533
0.1uF/10V
C7534
0.1uF/10V
C7535
0.1uF/10V
C7536
0.01UF/16V
C7537
0.01UF/16V
C7540
10UF/6.3V
C7545
1UF/6.3V
C7546
0.1uF/10V
GND
<Variant Name>
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: Mike Lee
Size: Custom
Project Name: Z62E
Rev: 2.0G
Date: 星期二, 五月 15, 2007
Sheet 20 of 59





Thermal Sensor





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

<Variant Name>

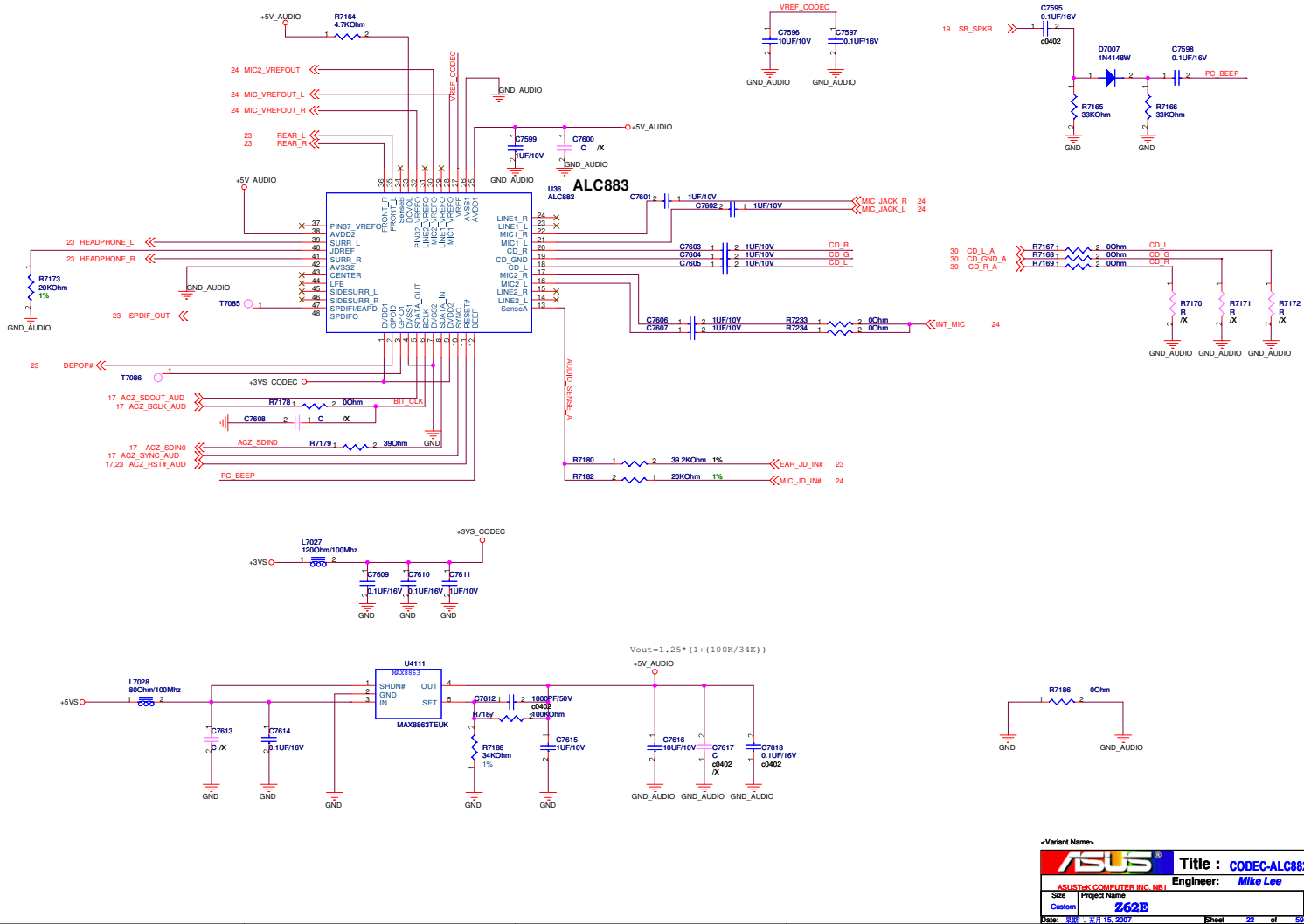
ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 21 of 59



<variant_name>

ASUSTeK COMPUTER INC. NBJ	Title : CODEC-ALC882		
	Engineer: Mike Lee		
Size: Custom	Project Name: 262E		Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 22 of 59		

SPEAKER CONN.

To Internal Speaker Connector

SPK_L_R1

SPEAKER is 4 ohm +- 15% / 2W /79 +- 3db (美星電子)
P/N:04-170003610

SPEAKER WILL BE CHANGE BY ME_061213

HEADPHONE JACK

HP_SPDIF1

	JACK REMOVE	JACK INSERTION	
		HEADPHONE	S/PDIF
PIN6	OPEN	LOW	OPEN
PIN7	HIGH	LOW	LOW

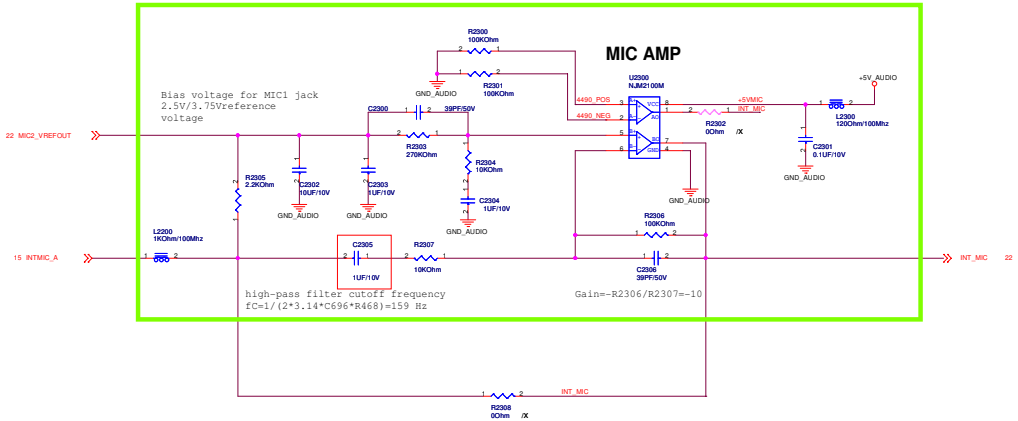
GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db

<variant_name>

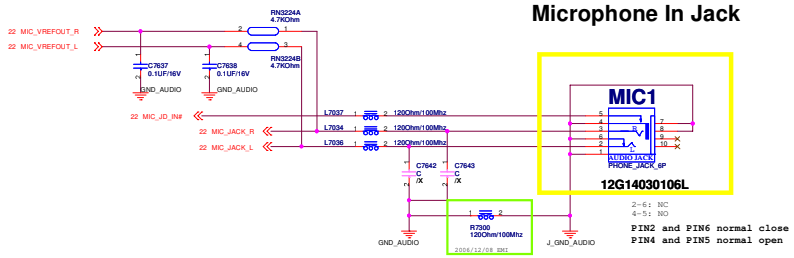
ASUSTeK COMPUTER INC. NB1 | Title : HP JCAK & AMP | Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.0G

Date: 星期 一 九月 15, 2007 | Sheet 23 of 59



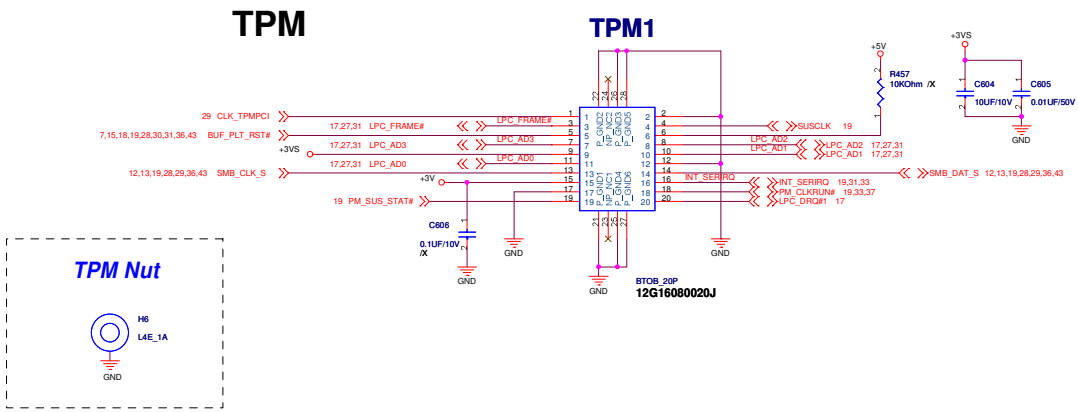
Microphone In Jack



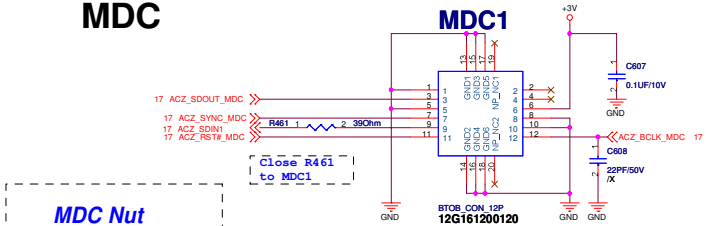
<Variant Name>

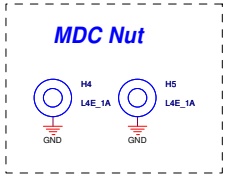
ASUSTeK COMPUTER INC. NB1	Title : MIC JACK & Pre-AMP	
	Engineer: Mike Lee	
Size: C	Project Name: Z62E	Rev: 2.0G
Date: Tuesday, January 15, 2007	Sheet 24 of 59	

TPM



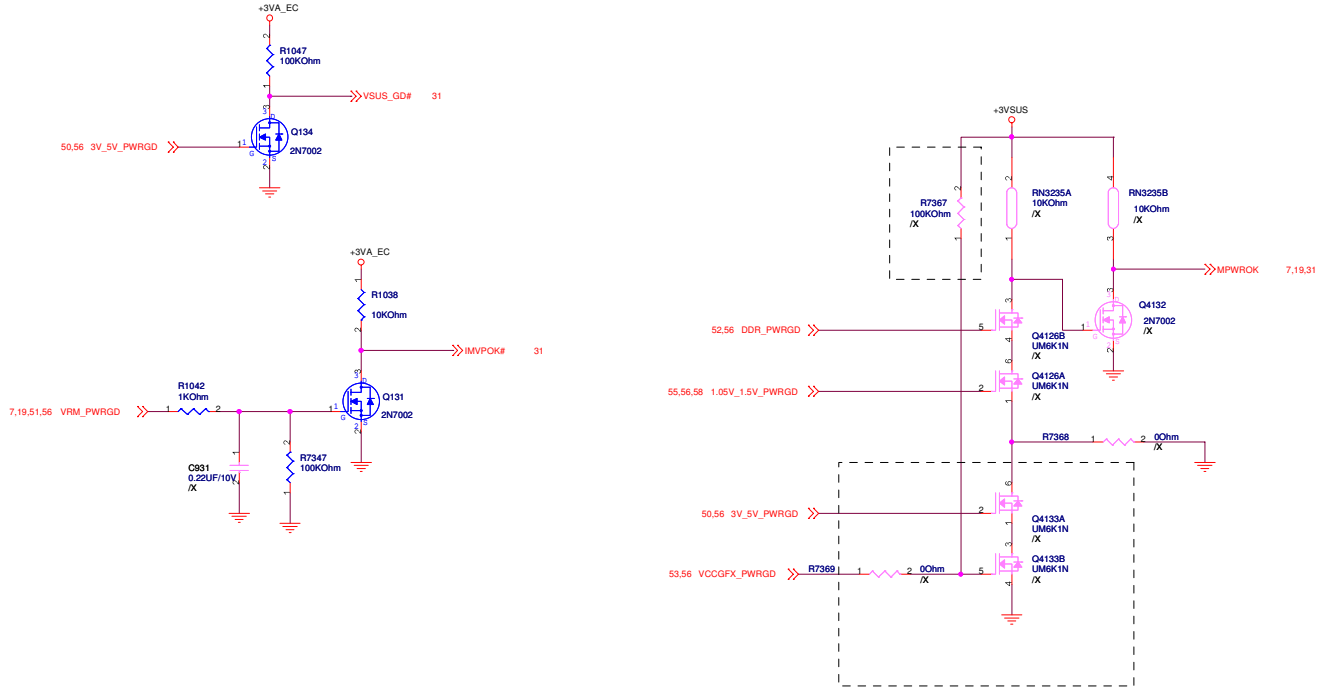
MDC





<variant_name>

ASUSTeK COMPUTER INC	Title : MODULE-TPM / MDC	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 25 of 59	



<Variant Name>

ASUSTeK COMPUTER INC

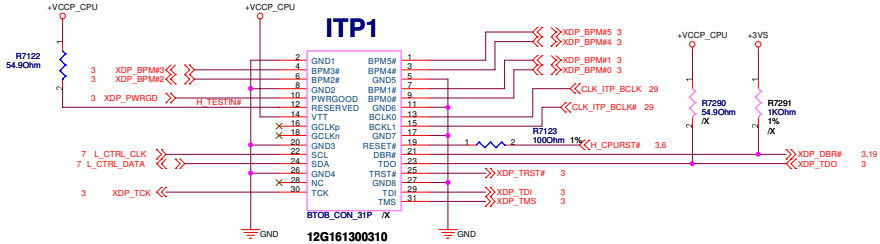
Title : POWER-ON SEQ.

Engineer: Mike Lee

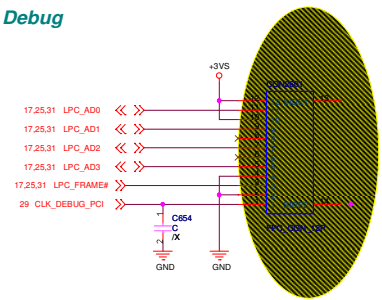
Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 26 of 59

ITP



For Debug



<Variant Name>

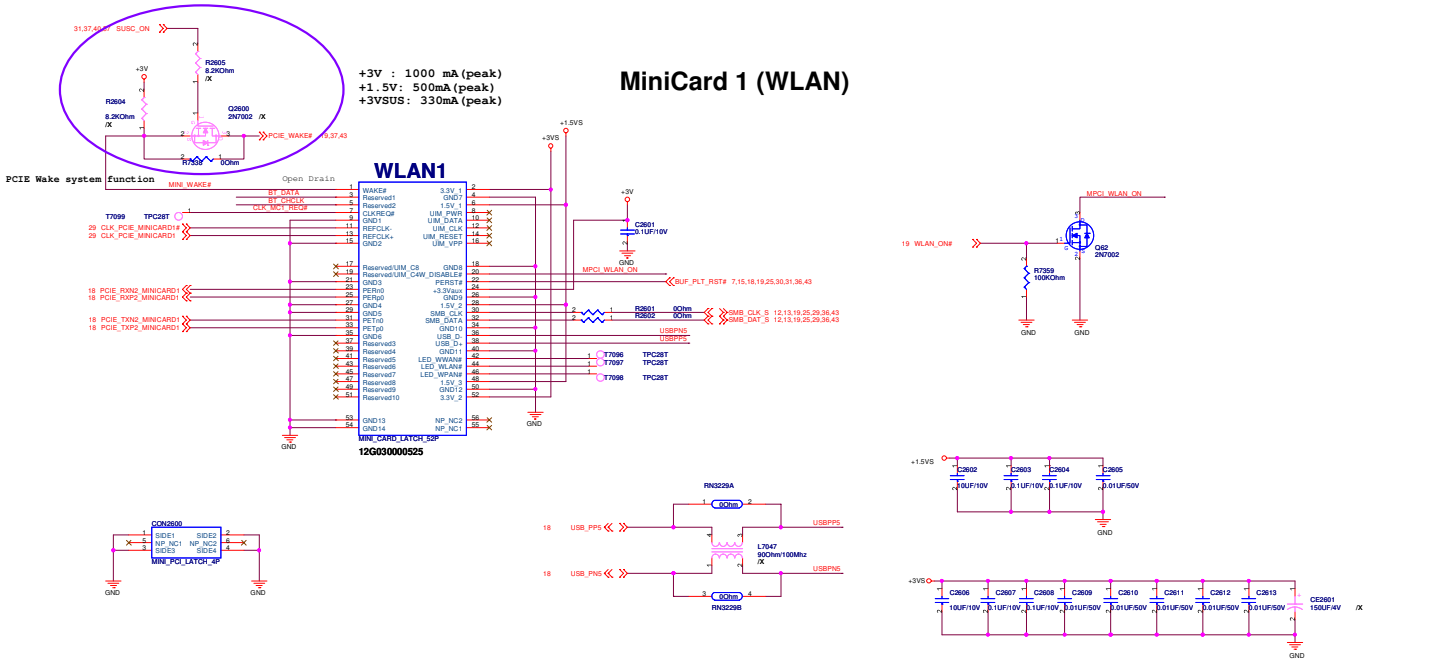
Title : ITP/Debug connector

ASUSTek Computer INC. Engineer: Mike Lee

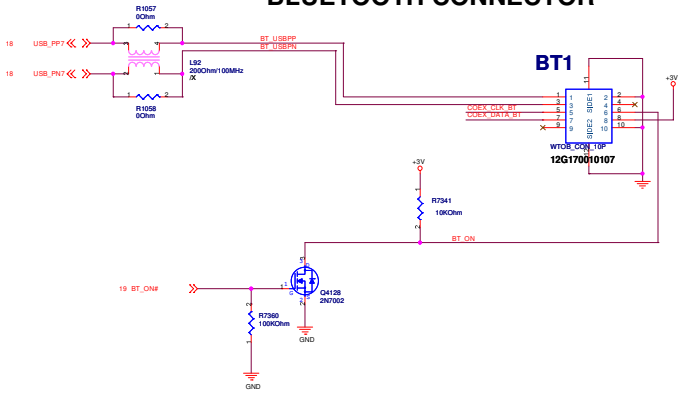
Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 九月 15, 2007 Sheet 27 of 59

MiniCard 1 (WLAN)



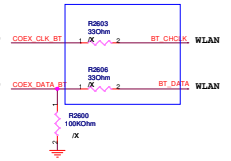
BLUETOOTH CONNECTOR



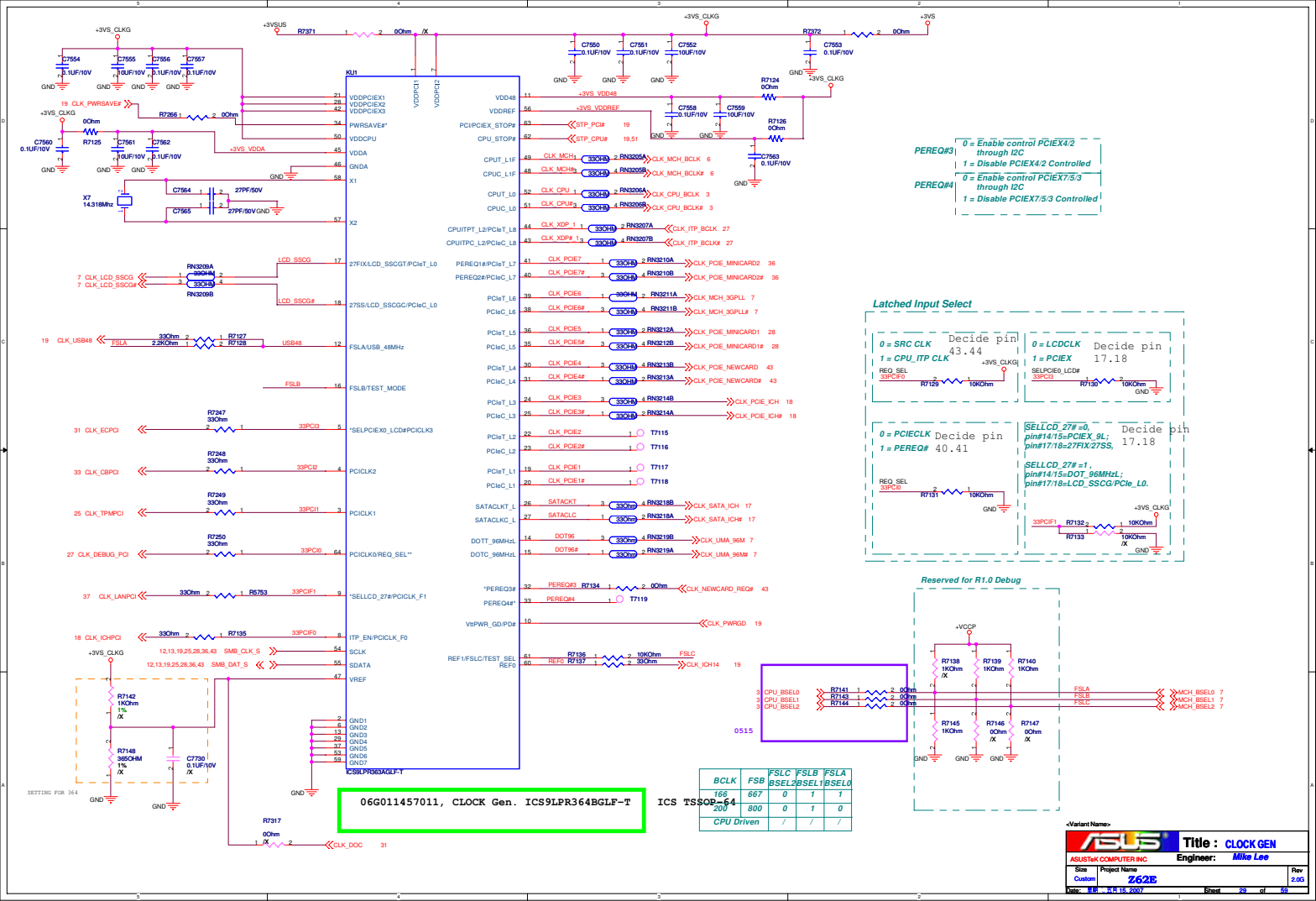
Check O/D output
or push pull

Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

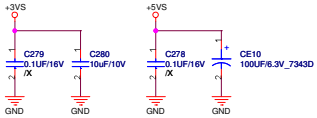
BT_ON 3.3V at
GPIO38

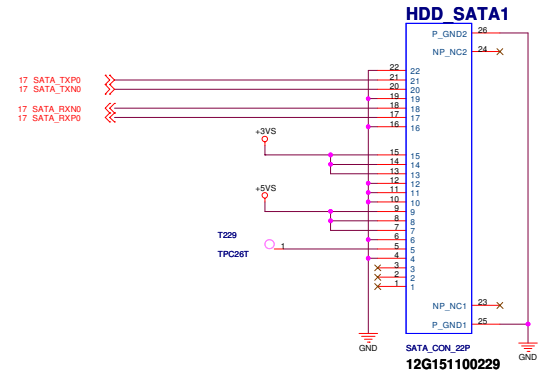


BT Module has no leakage, so
discard PMOS block circuits

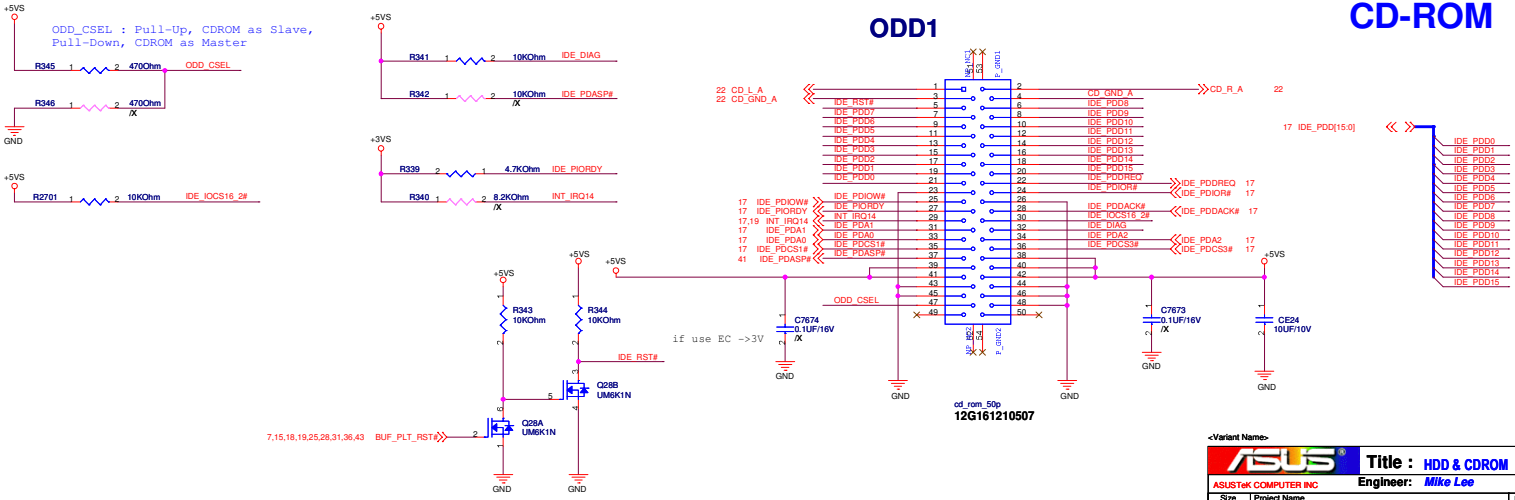

KU1
ICS9LPR363AGLF-T
06G011457011, CLOCK Gen. ICS9LPR364BGLF-T
ICS TSSOP-64
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
Reserved for R1.0 Debug
BCLK | FSB | FSLC BSEL2 | FSLB BSEL1 | FSLA BSEL0
166 | 667 | 0 | 1 | 1
200 | 800 | 0 | 1 | 0
CPU Driven | | / | / | /
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer: Mike Lee
Size: Custom
Project Name: Z62E
Rev: 2.0G
Date: 5 14, 2007
Sheet 29 of 59

SATA HDD Connector



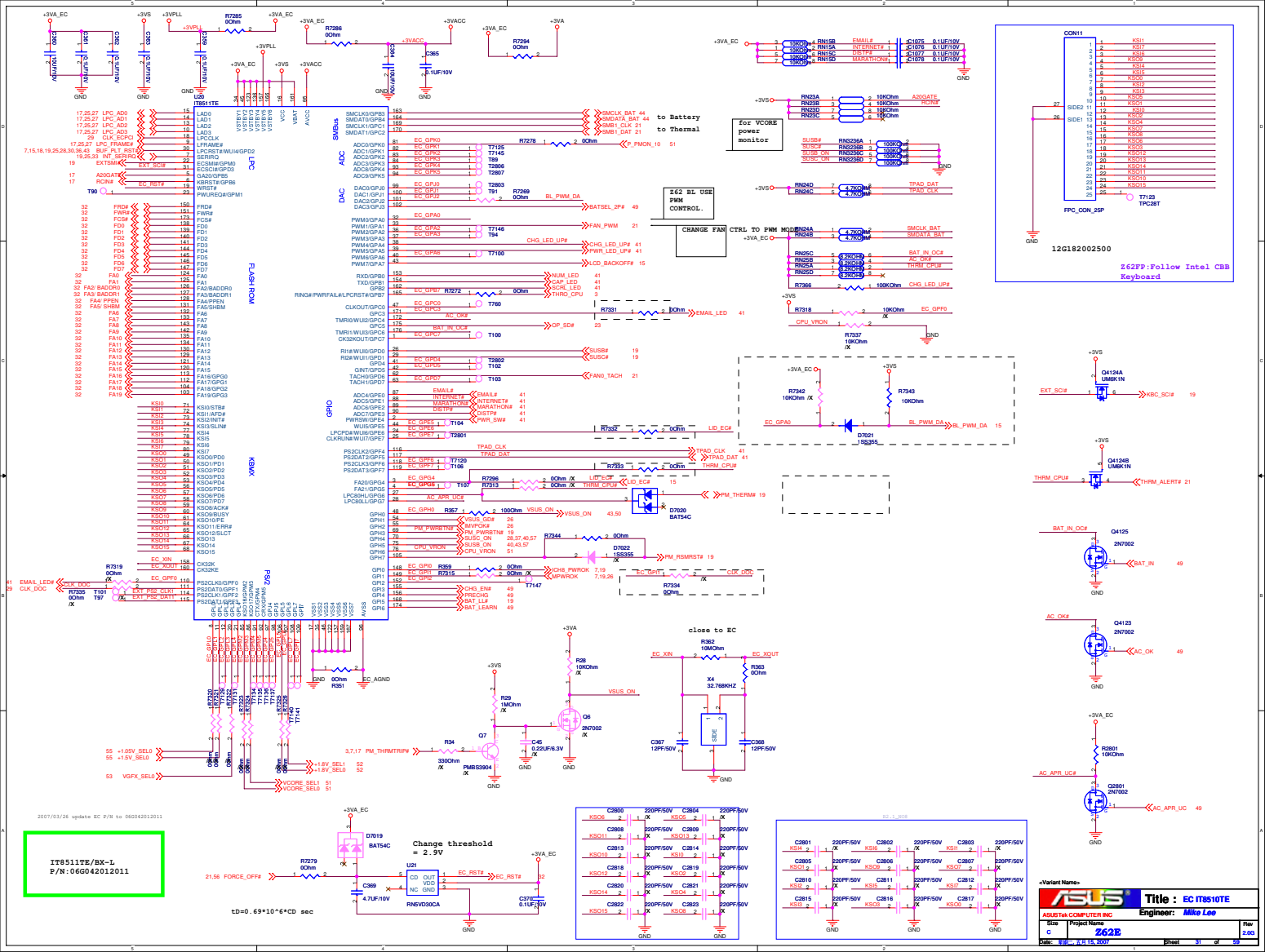


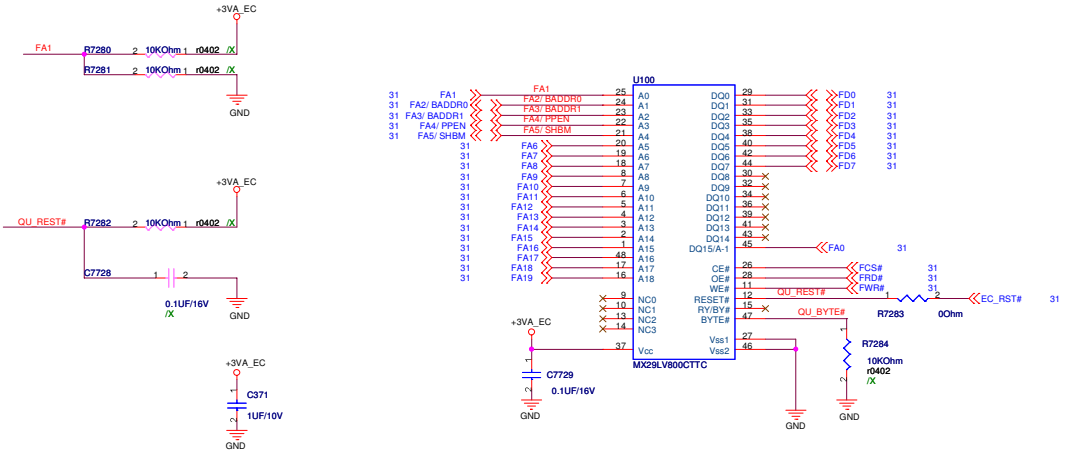
CD-ROM



<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 _ 五月 15, 2007	Sheet 30 of 59	


IT8511TE/BX-L
P/N:06G042012011
2007/03/26 update EC P/N to 06G042012011
Change threshold = 2.9V
tD=0.69*10^6*CD sec
Z62 BL USE PWM CONTROL.
CHANGE FAN CTRL TO PWM MODE
for VCORE power monitor
close to EC
Z62FP:Follow Intel CBB Keyboard
12G182002500
FPC_CON_25P
Title : EC IT8510TE
Engineer: Mike Lee
ASUSTeK COMPUTER INC
Project Name Z62E
Date: Wednesday, March 15, 2007
Sheet 31 of 59



BIOS:05G001204043

ISA ROM

EC Hardware Strapping

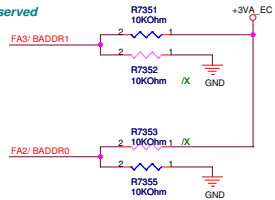
[FA3/ BADDR1 : FA2/ BADDR0]

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

01: PNPCNG Access Register Pair Are 004Eh and 004Fh

10: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved



Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

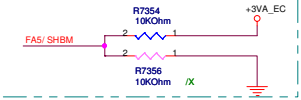
0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



<Variant Name>

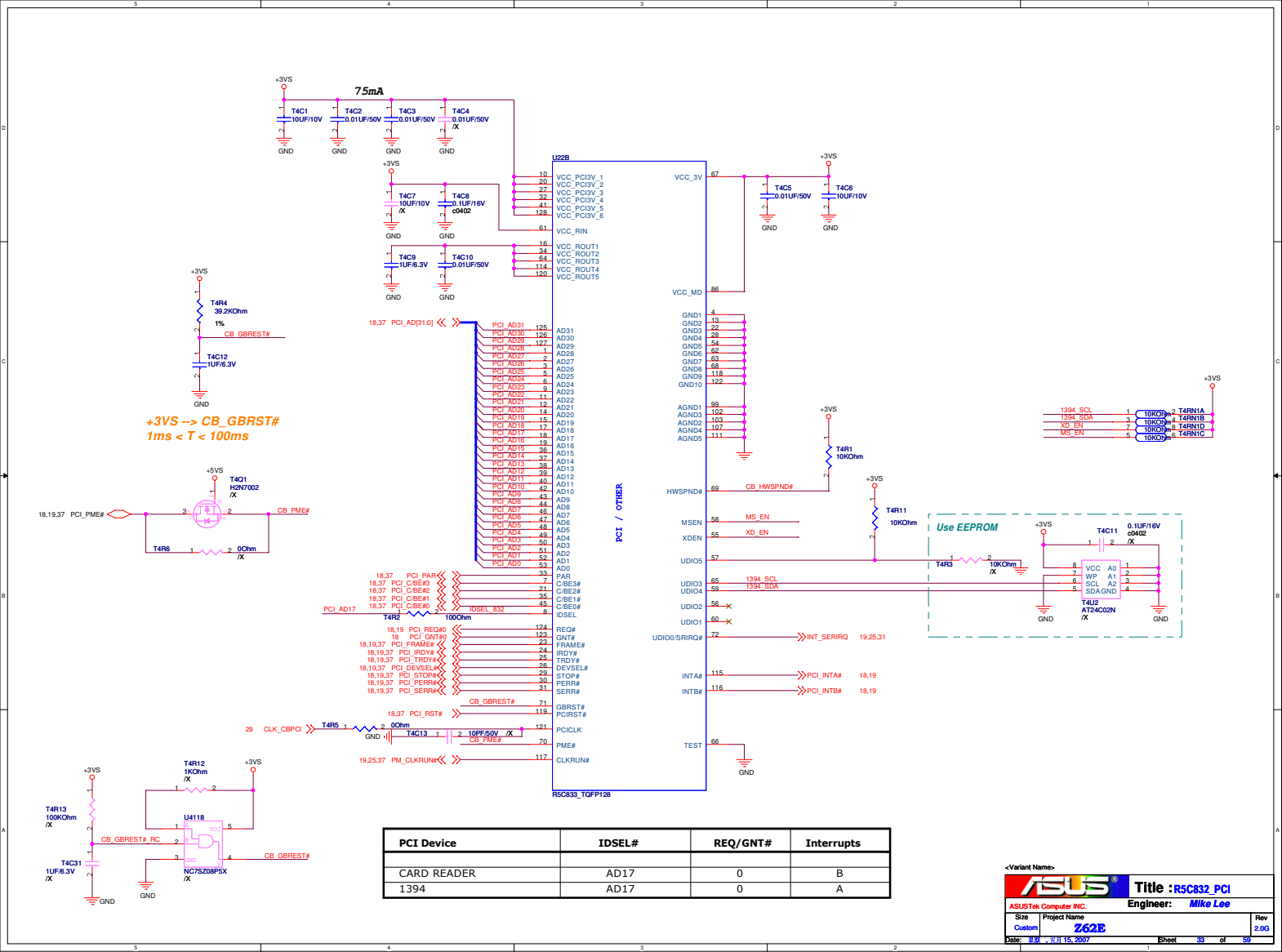
ASUSTek COMPUTER INC

Title : EC IT8510TE(2/2) & ROM

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 32 of 59



PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A

<Variant Name>

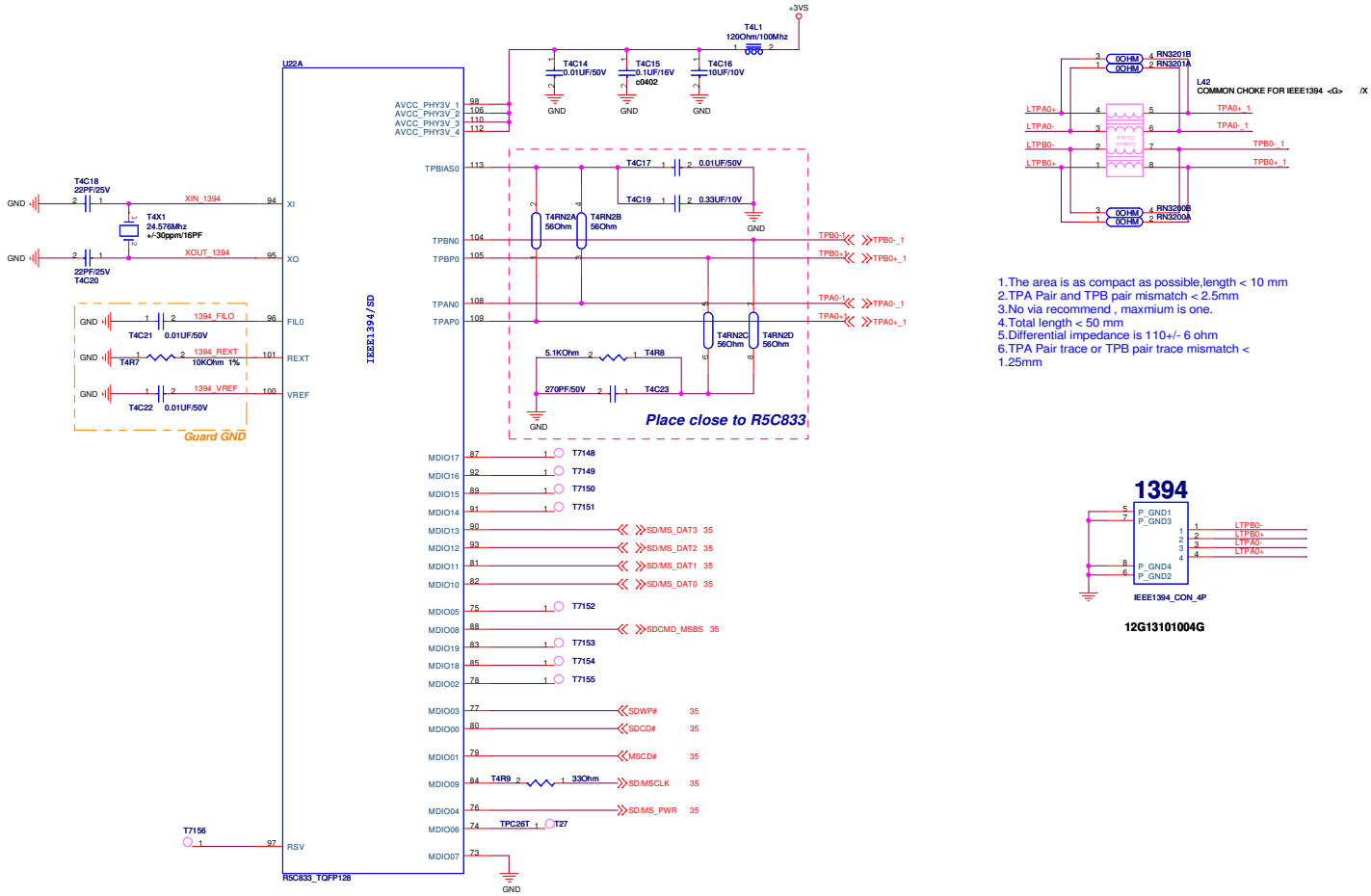
ASUSTek Computer INC.

Title : R5C832_PCI

Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.0G

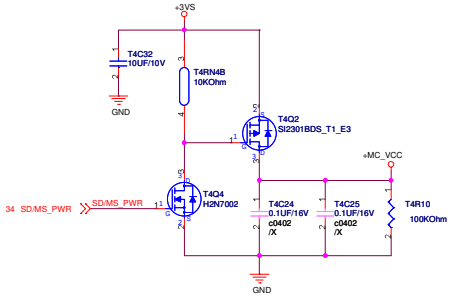
Date: 星期 _ 五月 15, 2007 Sheet 33 of 59



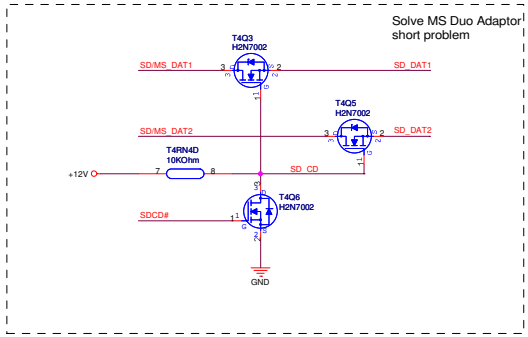
1.The area is as compact as possible,length < 10 mm
2.TPA Pair and TPB pair mismatch < 2.5mm
3.No via recommend , maxmium is one.
4.Total length < 50 mm
5.Differential impedance is 110+/- 6 ohm
6.TPA Pair trace or TPB pair trace mismatch < 1.25mm

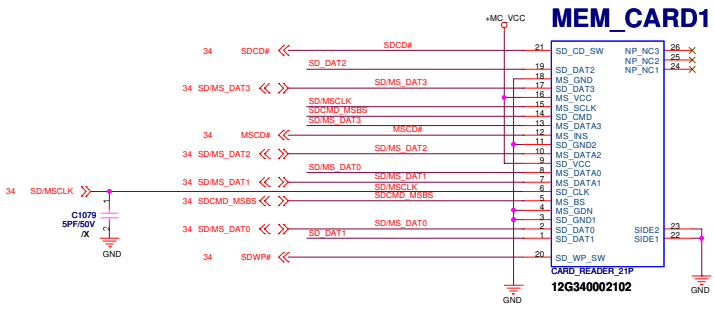
<Variant Name>

Title : R5C832_1394/SD		
ASUSTek Computer INC.	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 34 of 59	



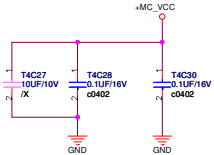
Card Reader Power Switcher

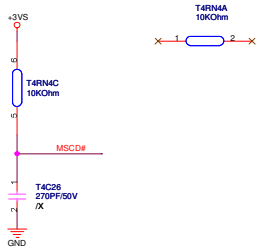




12G340002102

Layout: SHIELD GND

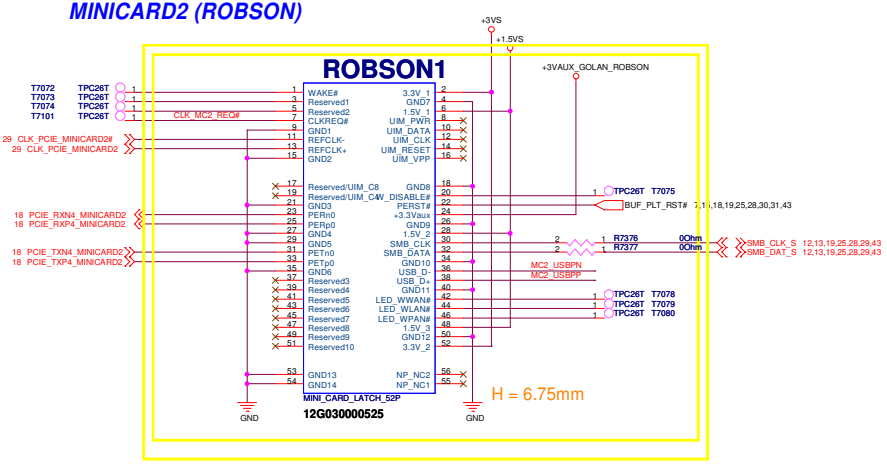




<variant_name>

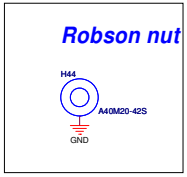
ASUSTek Computer INC.	Title: 3 in 1 Card Reader	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z62E	Rev: 2.0G
Date: 星期二, 五月 15, 2007	Sheet 35 of 59	

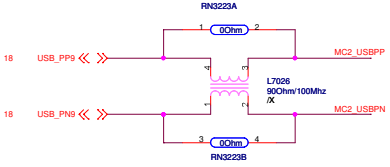
MINICARD2 (ROBSON)

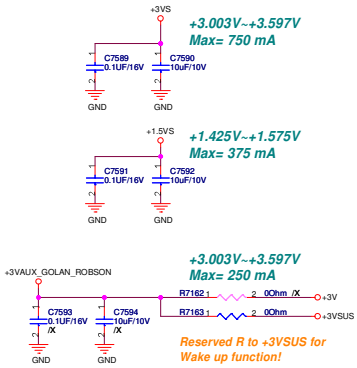


2007/1/15 change
ROBSON conn.

Robson nut







<Variant Name>

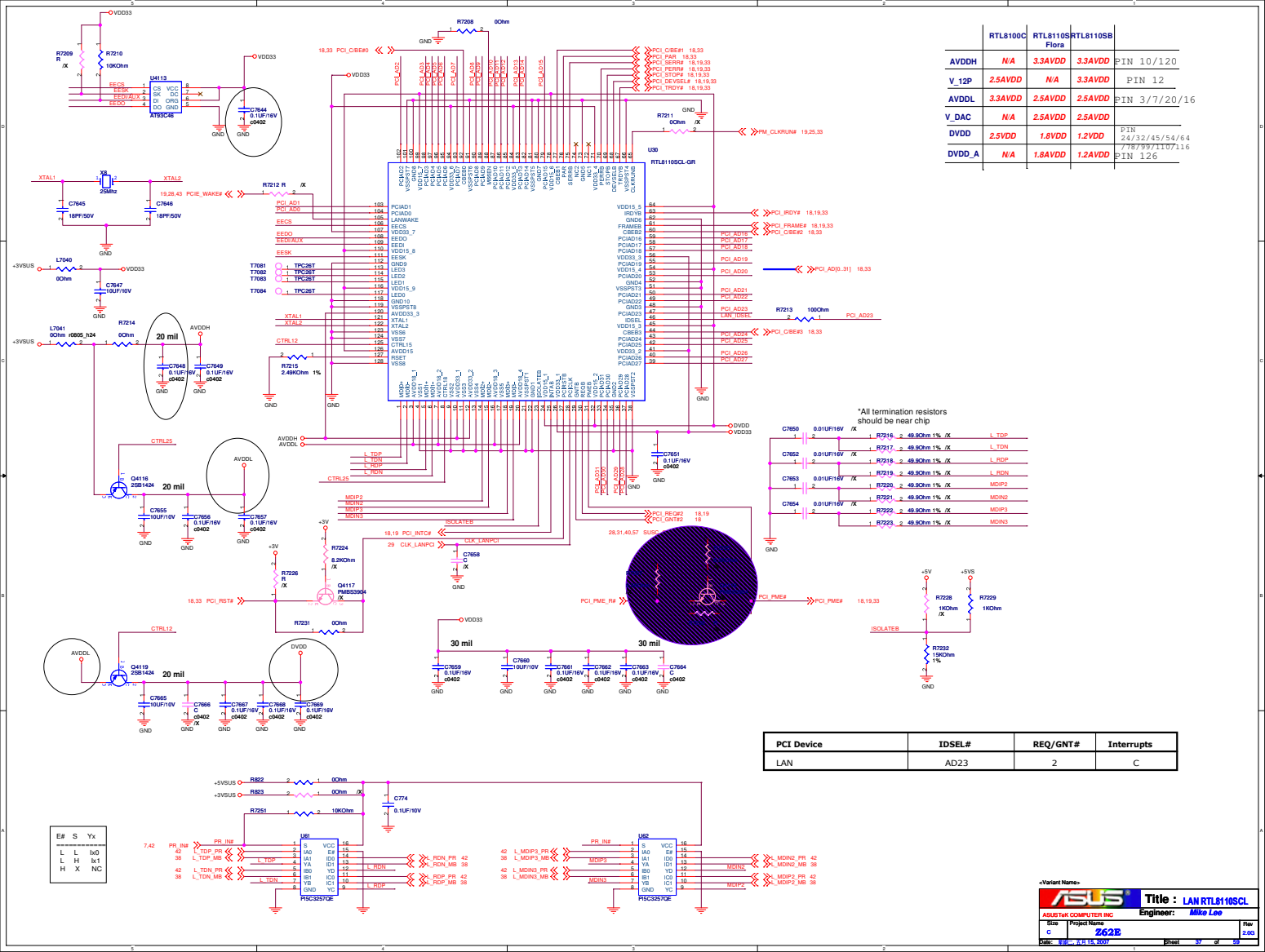
Title : MINICARD for 3G CARD

ASUSTek Computer INC.

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期一, 十月 15, 2007 Sheet 36 of 59



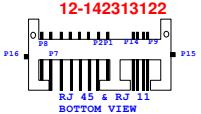
	RTL8100C	RTL8110S/SB Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 77/87/97/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	2	C

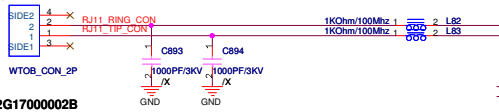
E#	S	Yx
L	L	Ix0
L	H	Ix1
H	X	NC

LAN PORT

12-142313122

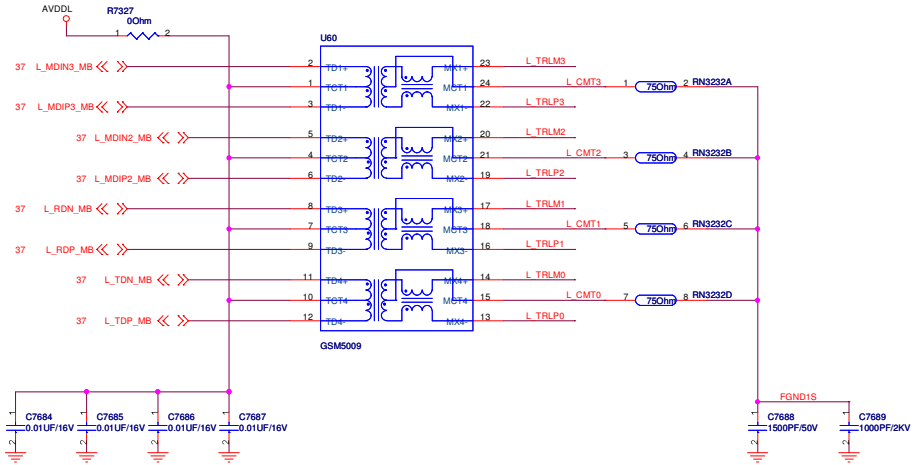


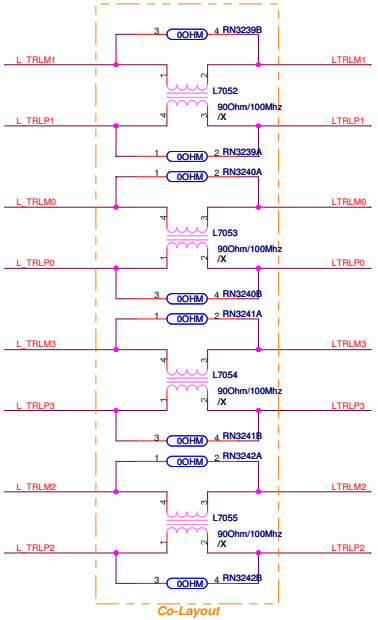
RING1



12G17000002B

12G142111120





<Variant Name>

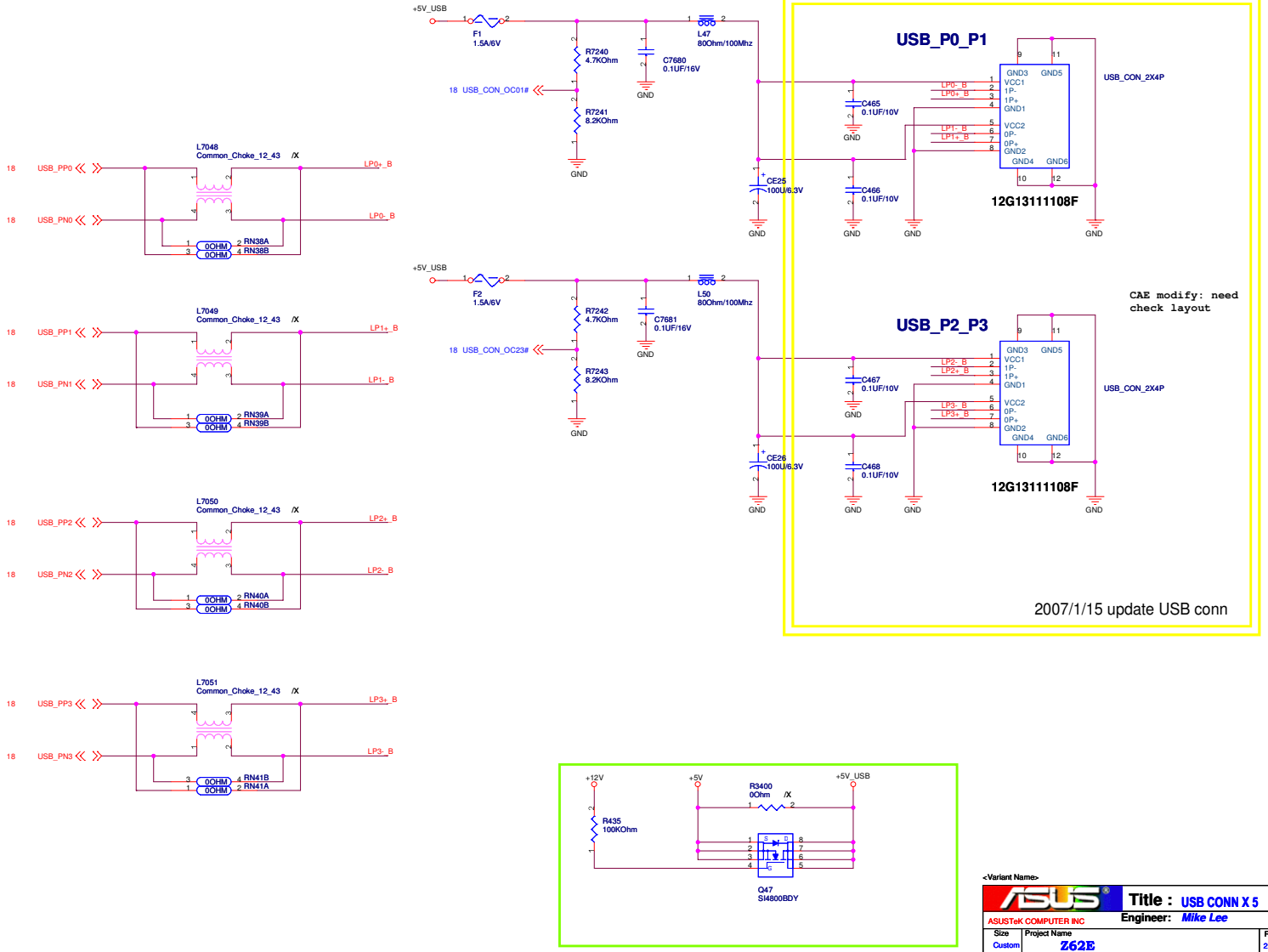
ASUSTeK COMPUTER INC

Title : RJ11+45

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 38 of 59



<Variant Name>

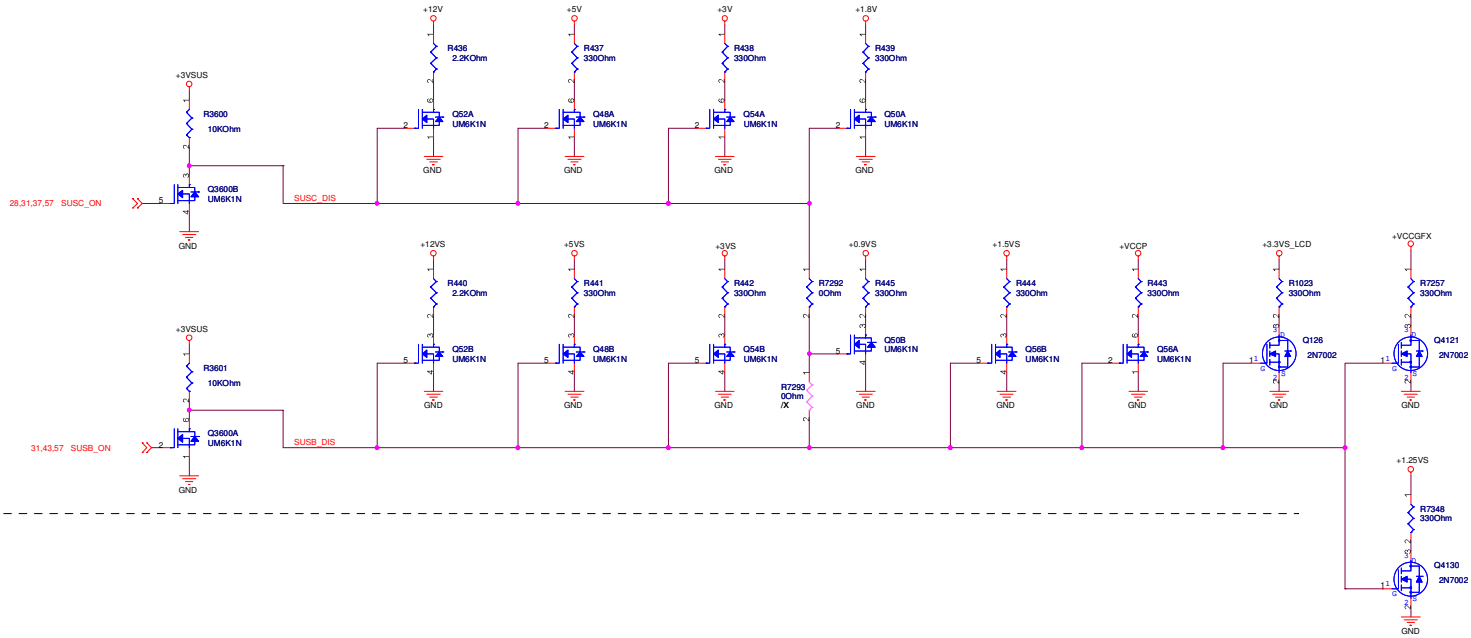
ASUSTeK COMPUTER INC

Title : USB CONN X 5

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 39 of 59



<Variant Name>

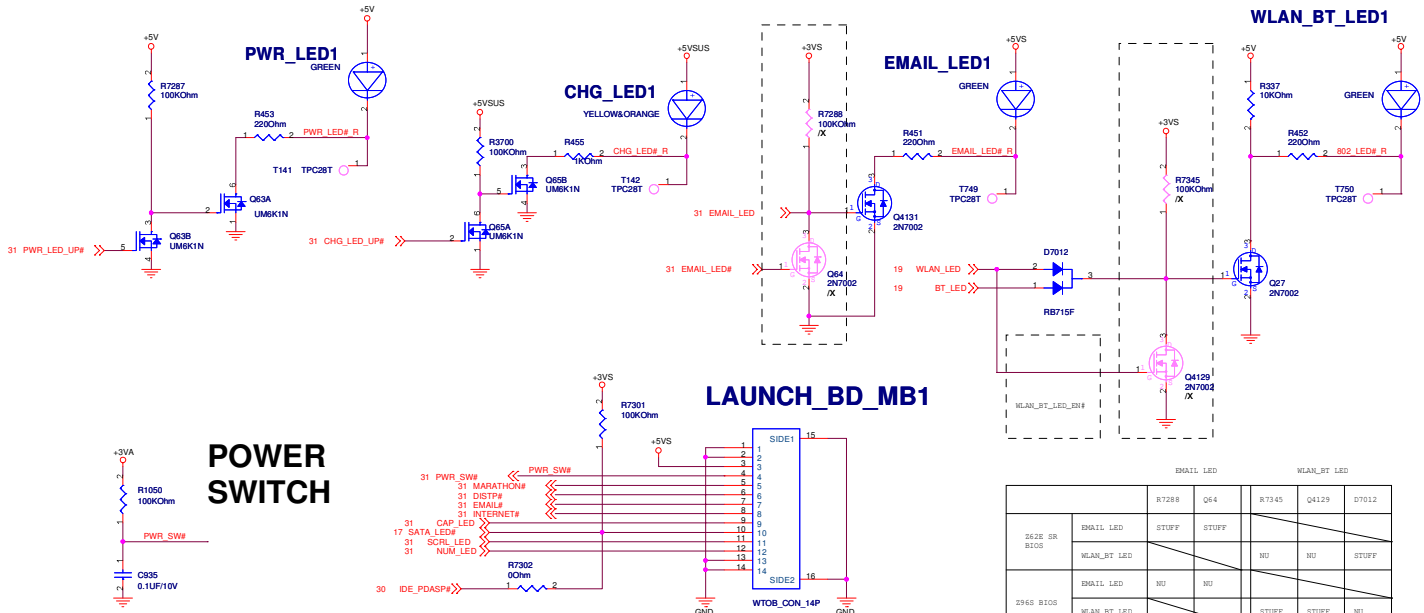
ASUSTeK COMPUTER INC

Title : Discharge Circuit

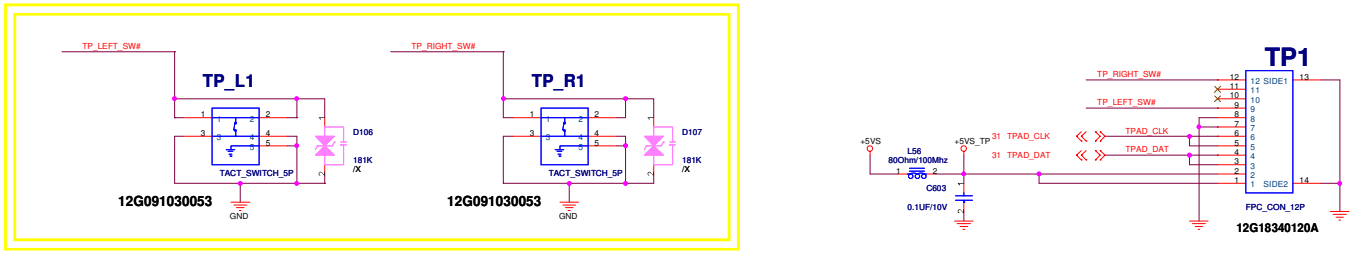
Engineer: Mike Lee

Size	Project Name	Rev
Custom	262E	2.0G

Date: 星期 一, 五月 15, 2007 Sheet 40 of 59



		EMAIL LED		WLAN_BT LED		
		R7288	Q64	R7345	Q4129	D7012
Z62E SR BIOS	EMAIL LED	STUFF	STUFF			
	WLAN_BT LED			NU	NU	STUFF
Z96S BIOS	EMAIL LED	NU	NU			
	WLAN_BT LED			STUFF	STUFF	NU



2007/1/15 change SW

TOUCH PAD SWITCH

Touch pad Definition

1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

Z62F: pin1 reversal

<Variant Name>

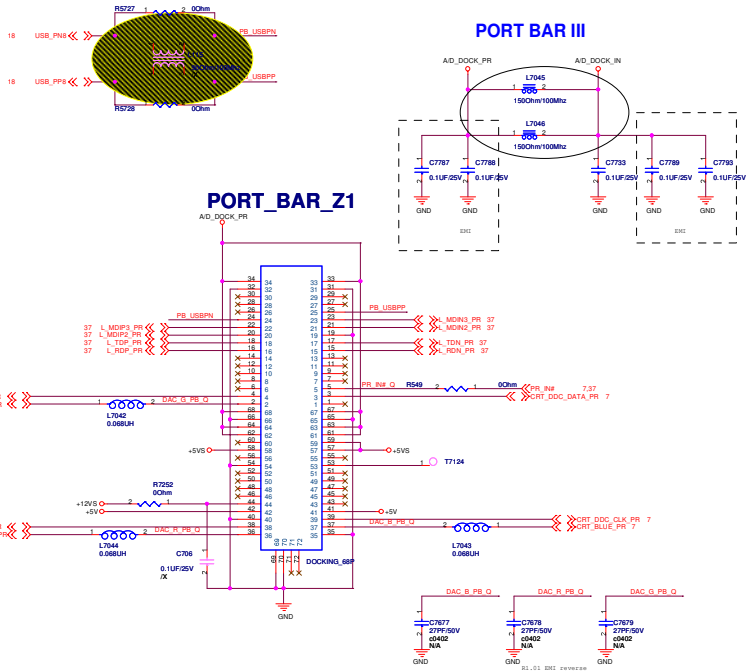
Title : LED/SW/TouchPad

ASUSTeK COMPUTER INC

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

Date: 星期 _ 三月 15, 2007 Sheet 41 of 59



<Variant Name>

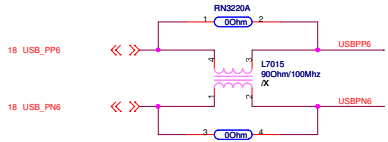
ASUSTeK COMPUTER INC

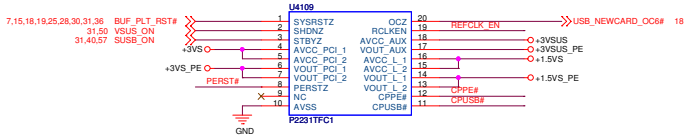
Title : PORT BAR 3 Conn.

Engineer: Mike Lee

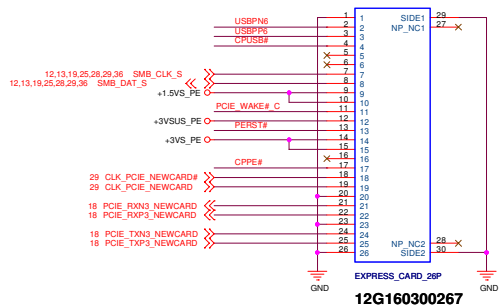
Size	Project Name	Rev
C	Z62E	2.0G

Date: 日 8月 15, 2007 Sheet 42 of 59



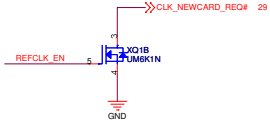


ExpressCard Header

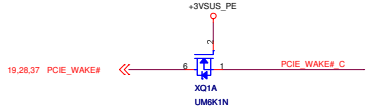


12G160300267

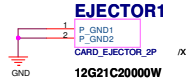
NEWCARD CLK Request



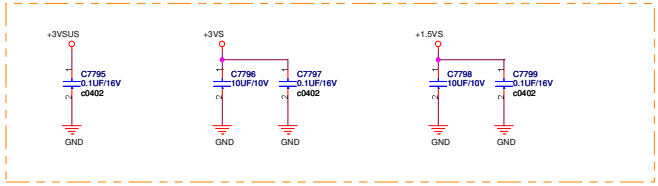
NEWCARD Wake#

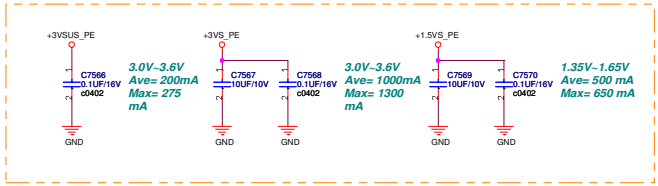


NewCard Ejector



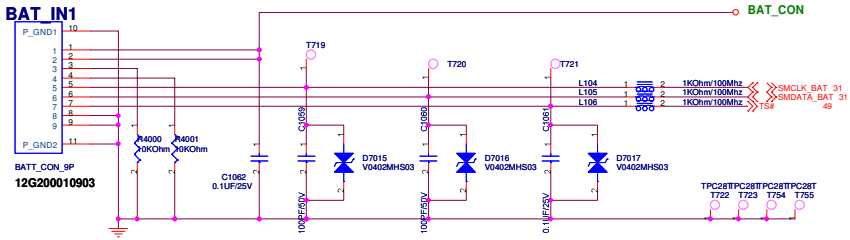
12G21C20000W

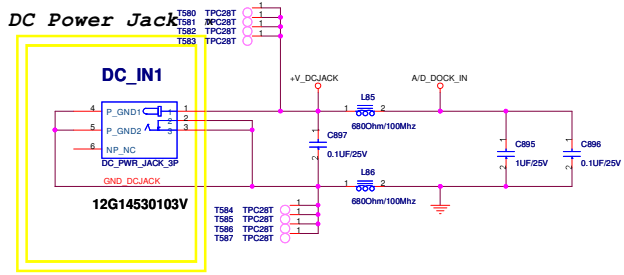




<Variant Name>

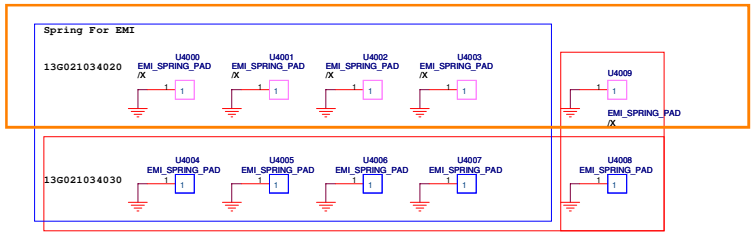
ASUSTek Computer INC.	Title : ExpressCARD	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 43 of 59	





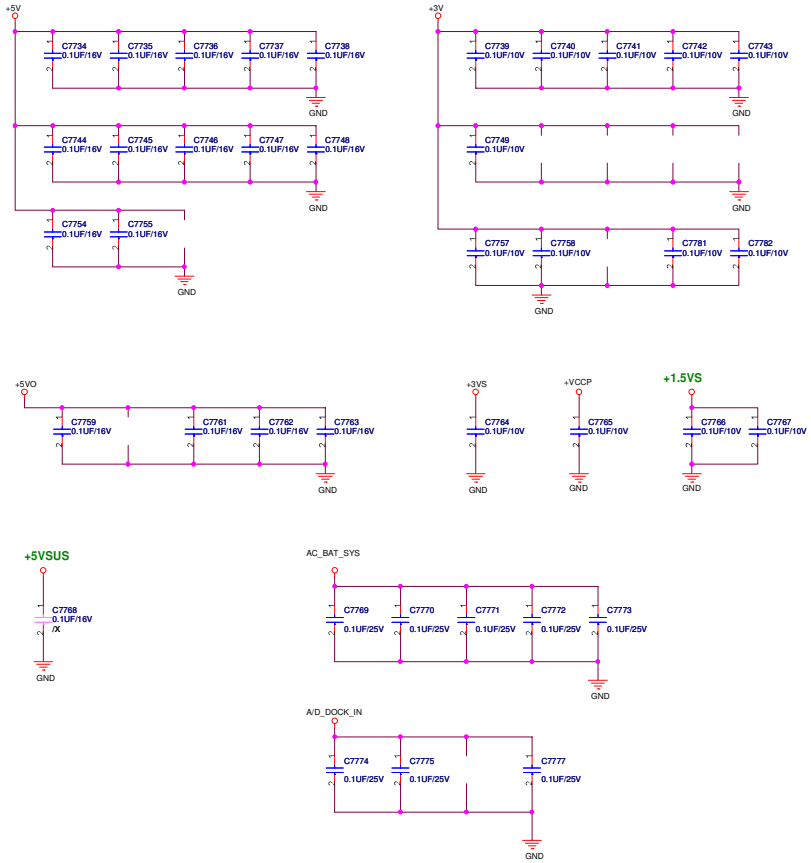
2007/1/15 change
DCIN jack

2007/04/01 13G021034020 SPRING --> NU



<Variant Name>

ASUSTeK COMPUTER INC	Title : DC/BATT IN	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 44 of 59	



<Variant Name>

ASUSTek Computer INC.

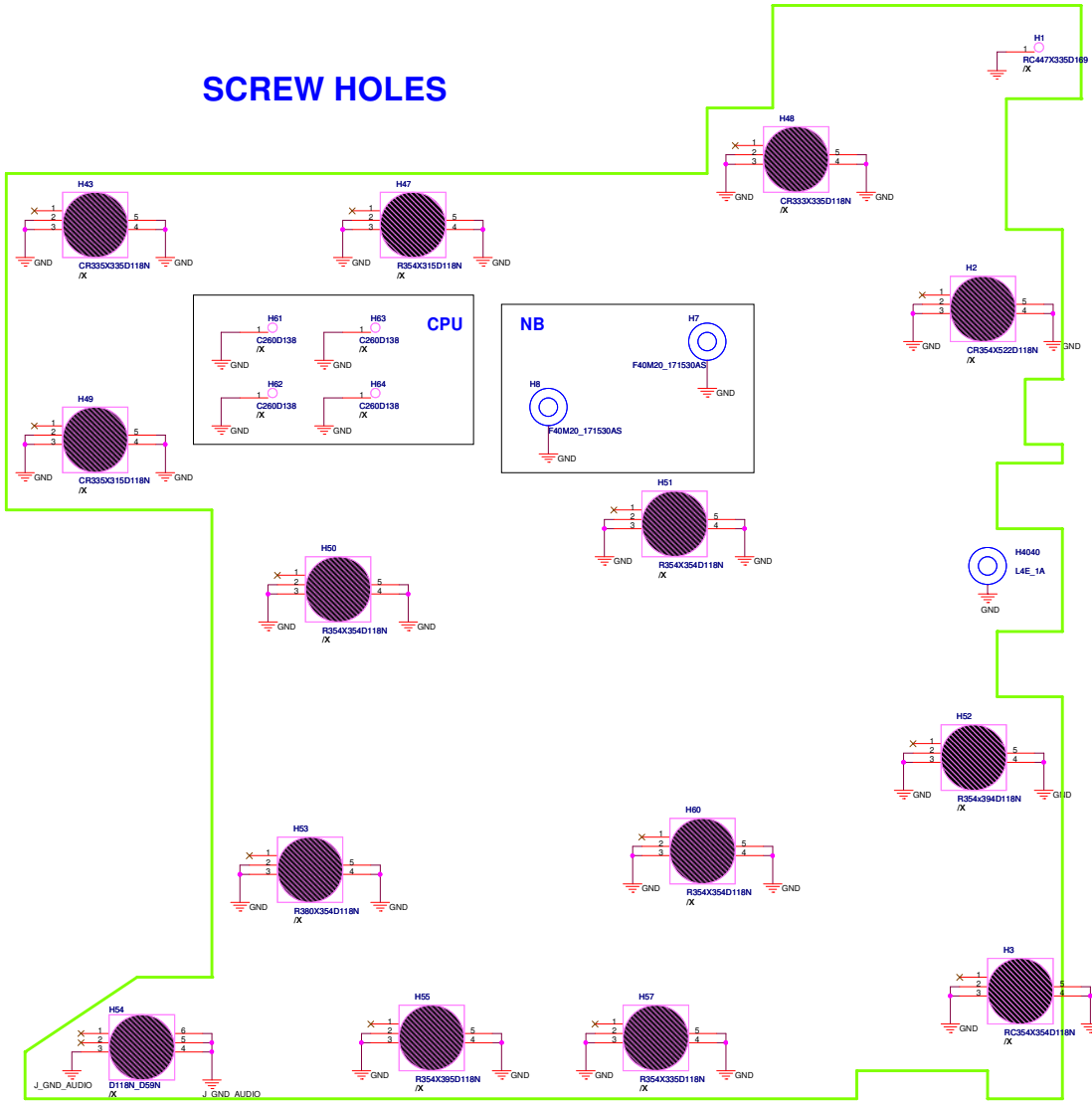
Title : STITCHING CAP

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

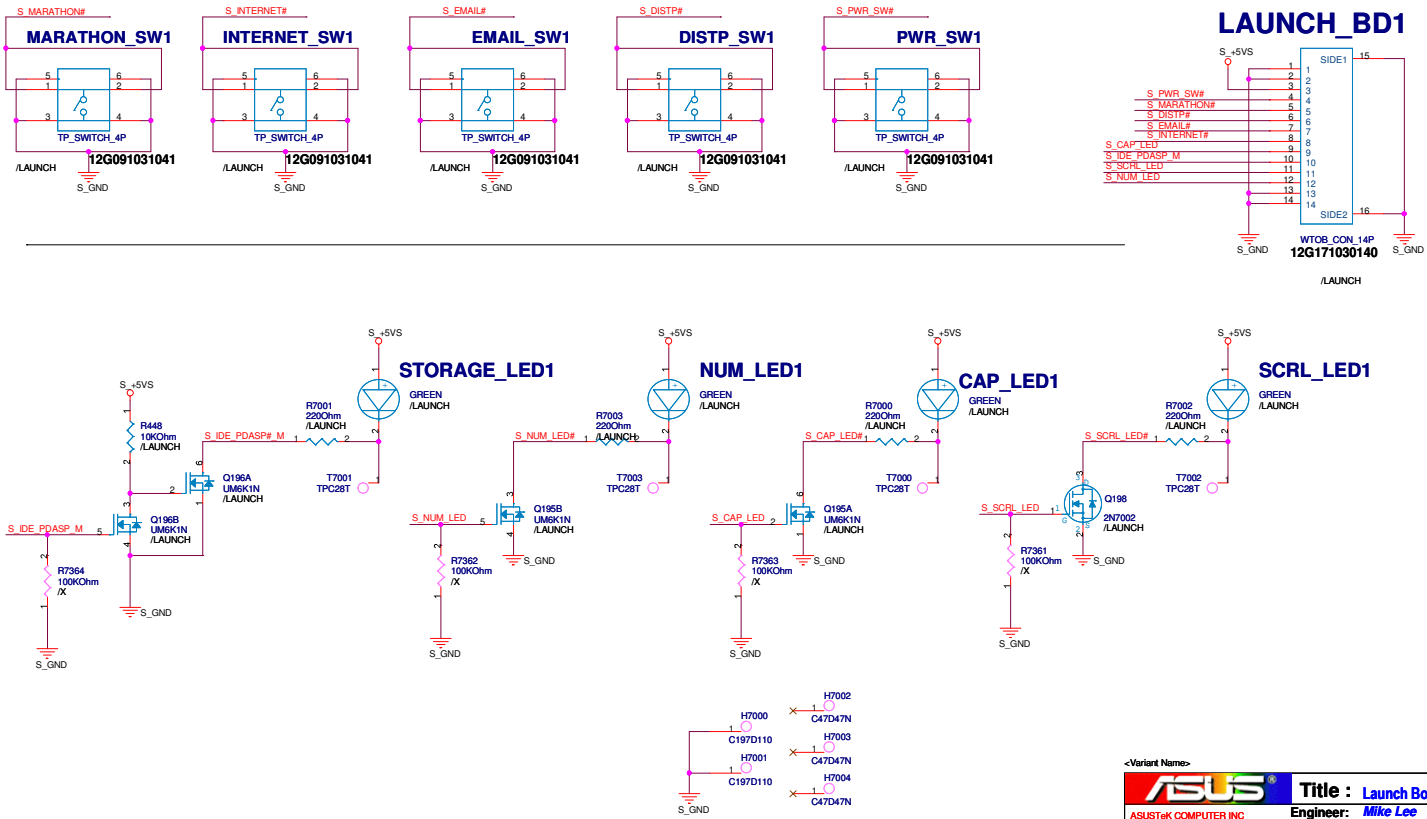
Date: 星期二, 九月 15, 2007 Sheet 45 of 59

SCREW HOLES



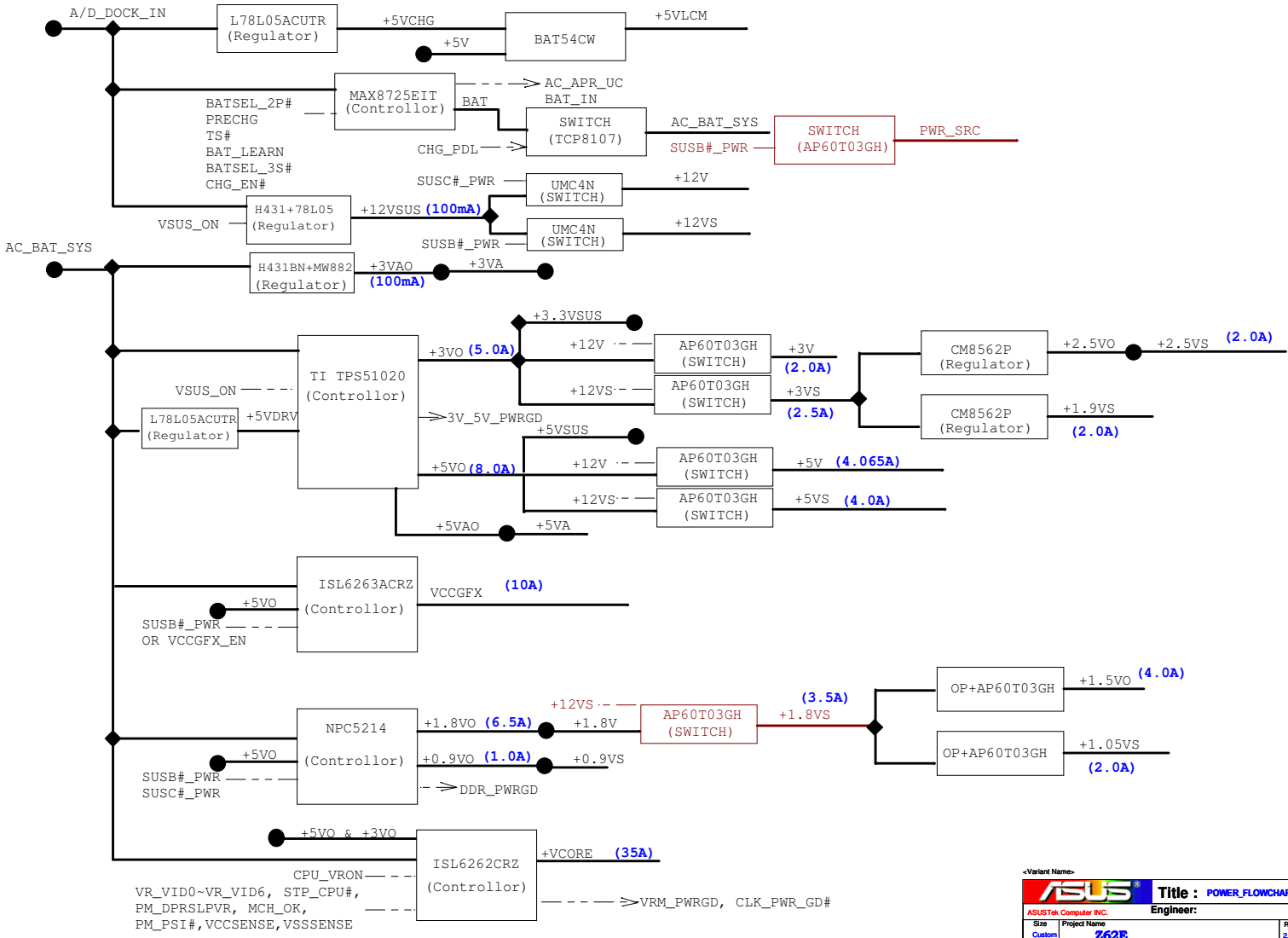
<Variant Name>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Mike Lee	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 _ 五月 15, 2007	Sheet 46 of 59	



<Variant Name>

ASUSTeK COMPUTER INC	Title : Launch Board	
	Engineer: Mike Lee	
Size: B	Project Name: Z62E	Rev: 2.0G
Date: 星期一, 五月 15, 2007	Sheet 47 of 59	


A/D_DOCK_IN
L78L05ACUTR (Regulator)
+5VCHG
+5V
BAT54CW
+5VLCM
MAX8725EIT (Controllor)
AC_APR_UC
BAT_IN
BAT
BATSEL_2P#
PRECHG
TS#
BAT_LEARN
BATSEL_3S#
CHG_EN#
SWITCH (TCP8107)
AC_BAT_SYS
CHG_PDL
SUSB#_PWR
SWITCH (AP60T03GH)
PWR_SRC
SUSC#_PWR
UMC4N (SWITCH)
+12V
H431+78L05 (Regulator)
VSUS_ON
+12VSUS (100mA)
UMC4N (SWITCH)
+12VS
SUSB#_PWR
AC_BAT_SYS
H431BN+MW882 (Regulator)
+3VAO (100mA)
+3VA
+3.3VSUS
TI TPS51020 (Controllor)
+3VO (5.0A)
+12V
AP60T03GH (SWITCH)
+3V (2.0A)
CM8562P (Regulator)
+2.5VO
+2.5VS (2.0A)
VSUS_ON
+12VS
AP60T03GH (SWITCH)
+3VS (2.5A)
CM8562P (Regulator)
+1.9VS (2.0A)
L78L05ACUTR (Regulator)
+5VDRV
3V_5V_PWRGD
+5VSUS
+5VO (8.0A)
+12V
AP60T03GH (SWITCH)
+5V (4.065A)
+12VS
AP60T03GH (SWITCH)
+5VS (4.0A)
+5VAO
+5VA
ISL6263ACRZ (Controllor)
VCCGFX (10A)
+5VO
SUSB#_PWR
OR VCCGFX_EN
NPC5214 (Controllor)
+1.8VO (6.5A)
+1.8V
+12VS
AP60T03GH (SWITCH)
(3.5A)
+1.8VS
OP+AP60T03GH
+1.5VO (4.0A)
+5VO
+0.9VO (1.0A)
+0.9VS
SUSB#_PWR
SUSC#_PWR
DDR_PWRGD
OP+AP60T03GH
+1.05VS (2.0A)
+5VO & +3VO
ISL6262CRZ (Controllor)
+VCORE (35A)
CPU_VRON
VR_VID0~VR_VID6, STP_CPU#,
PM_DPRSLPVR, MCH_OK,
PM_PSI#,VCCSENSE,VSSSENSE
VRM_PWRGD, CLK_PWR_GD#
<Variant Name>
Title : POWER_FLOWCHART
ASUSTek Computer INC.
Engineer:
Size
Custom
Project Name
262E
Rev
2.0G
Date:
Sheet 48 of 59

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

Adaptor Max. Current :

PR5708=20K PR5714 = 178K; Iilimit = 4.5A; 81W

PR5708=27K PR5714 = 47K; Iilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

VictI = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; VictI = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; VictI = 2.111V

=> Icharge = 2.9329A

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

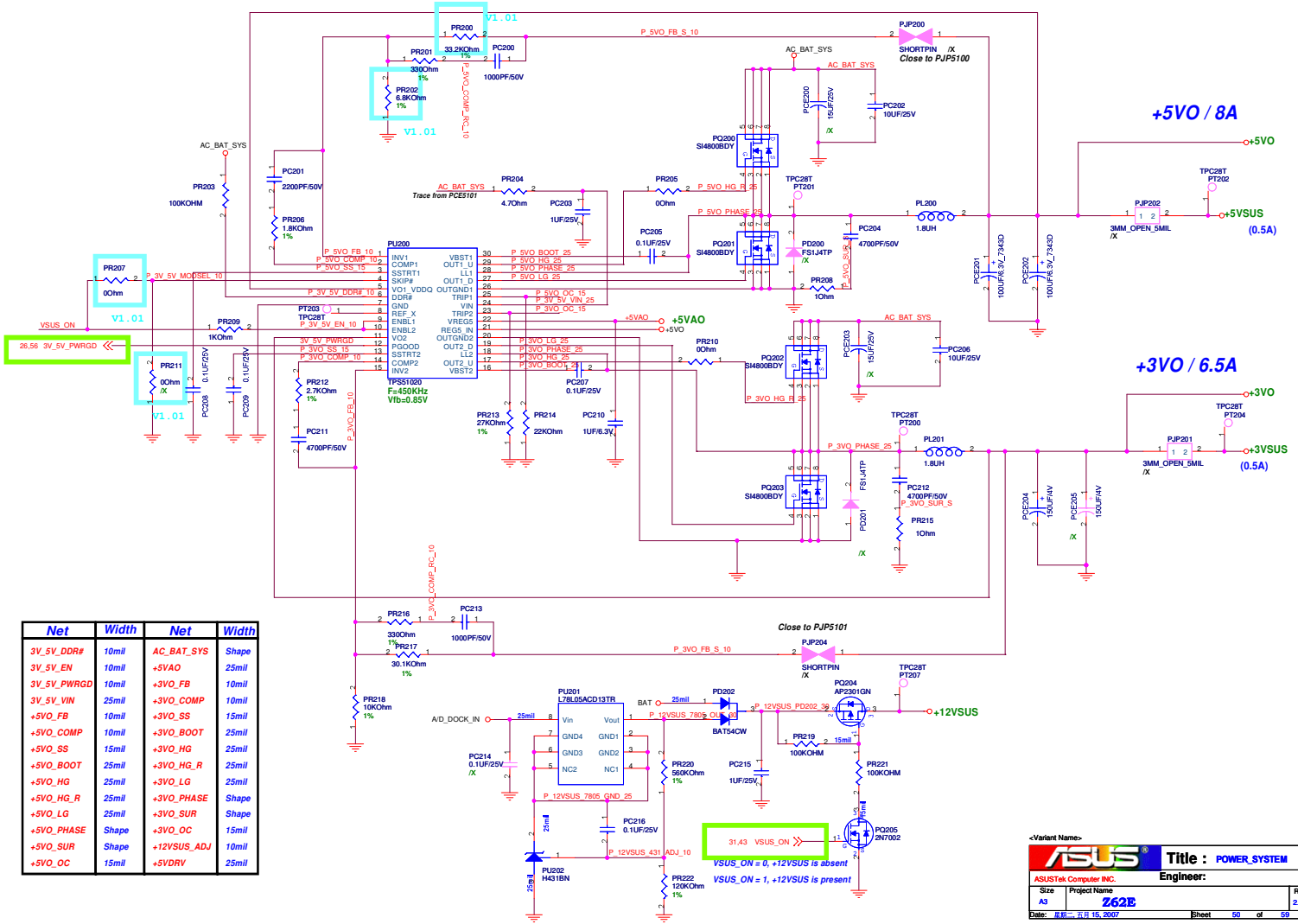
POWER PATH & BAT_LEARN

Battery Voltage

MXM AC_OK internal has 10K OHM pull down

BAT_IN_OC# = 1; Battery absence

BAT_IN_OC# = 0; Battery Plug-in



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

<Variant Name>
Title : POWER_SYSTEM
ASUSTek Computer INC.
Engineer:
Size: A3
Project Name: Z62E
Rev: 2.0G
Date: 星期二, 六月 15, 2007
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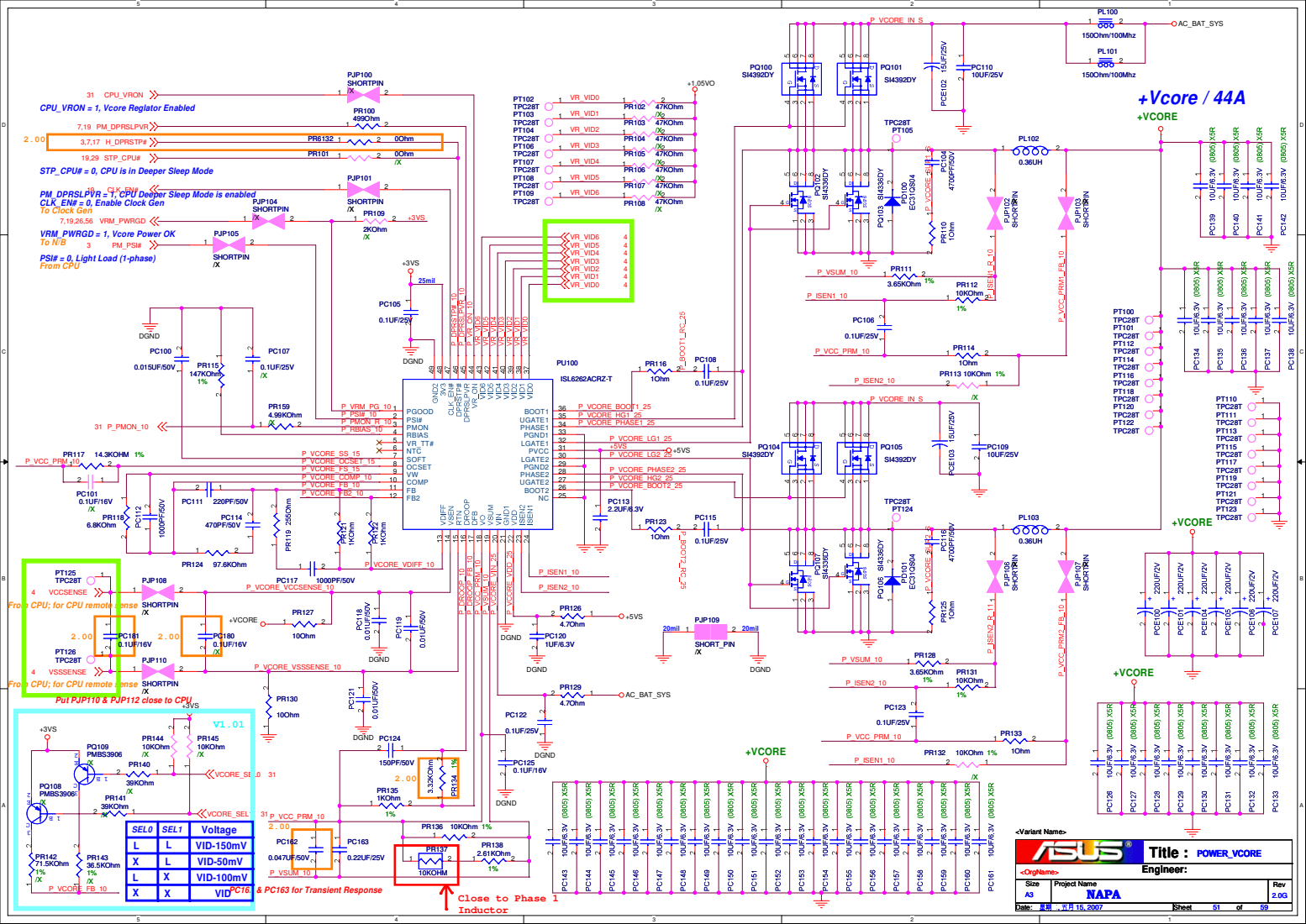
+Vcore / 44A
CPU_VRON = 1, Vcore Regulator Enabled
STP_CPU# = 0, CPU is in Deeper Sleep Mode
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
CLK_EN# = 0, Enable Clock Gen
VRM_PWRGD = 1, Vcore Power OK
PSI# = 0, Light Load (1-phase)
Put PJP110 & PJP112 close to CPU
PC161 & PC163 for Transient Response
Close to Phase 1 Inductor
SEL0 SEL1 Voltage
L L VID-150mV
X L VID-50mV
L X VID-100mV
X X VID
Title : POWER_VCORE
Engineer:
NAPA
Date: 五月 15, 2007
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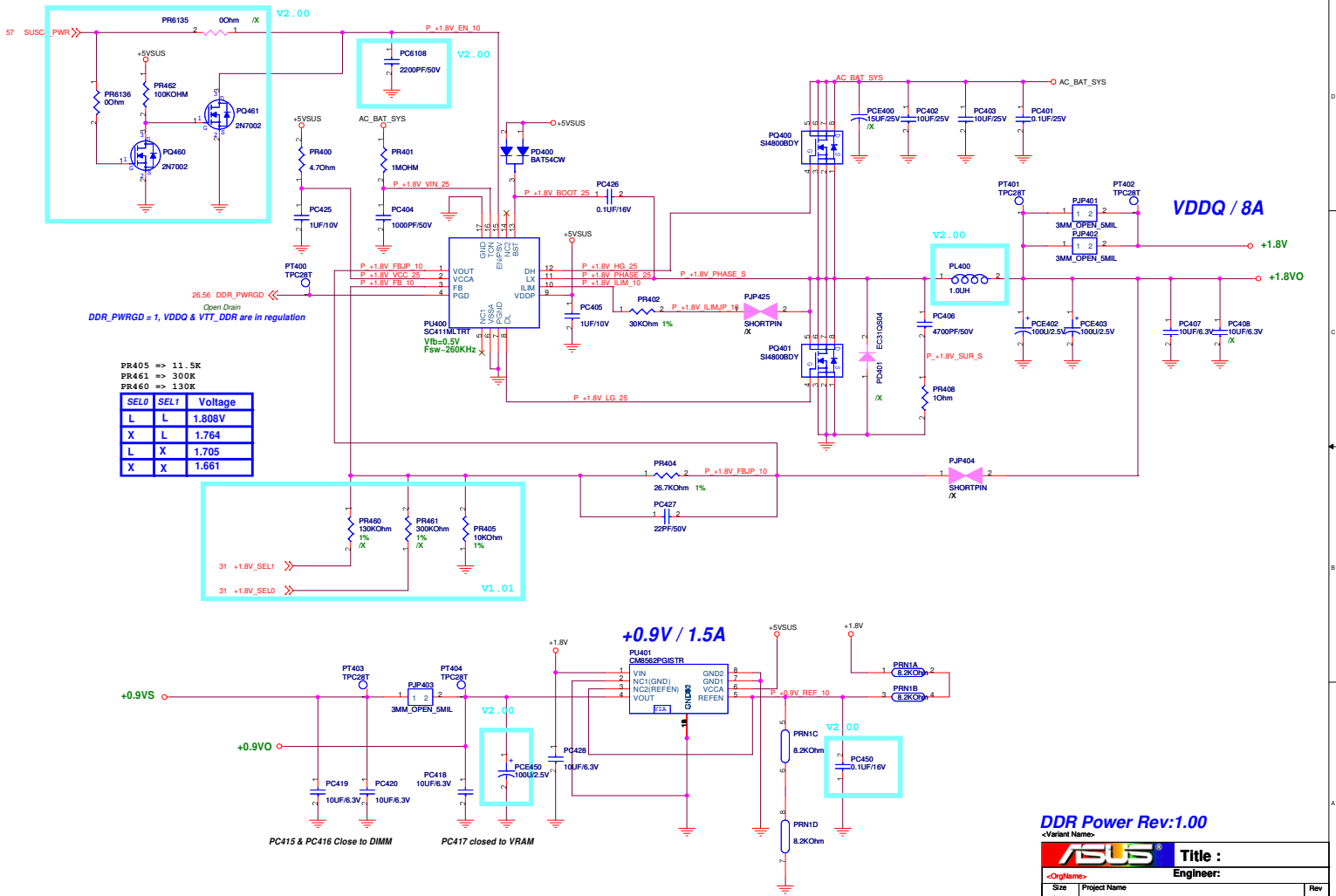

V2.00
57 SUSC_PWR
PR6135 0Ohm /X
+5VSUS
PR6136 0Ohm
PR462 100KOHM
PQ461 2N7002
PQ460 2N7002
P_+1.8V_EN_10
PC6108 2200PF/50V
V2.00
AC_BAT_SYS
PR400 4.7Ohm
PR401 1MOHM
PC425 1UF/10V
PC404 1000PF/50V
P_+1.8V_VIN_25
PD400 BAT54CW
PC426 0.1UF/16V
P_+1.8V_BOOT_25
PC400 SI4800BDY
PCE400 15UF/25V /X
PC402 10UF/25V
PC403 10UF/25V
PC401 0.1UF/25V
PT401 TPC28T
PT402 TPC28T
PJP401 3MM_OPEN_5MIL
PJP402 3MM_OPEN_5MIL
VDDQ / 8A
+1.8V
+1.8VO
PT400 TPC28T
26,56 DDR_PWRGD
Open Drain
DDR_PWRGD = 1, VDDQ & VTT_DDR are in regulation
P_+1.8V_FBJP_10
P_+1.8V_VCC_25
P_+1.8V_FB_10
PU400 SC411MLTRT
Vfb=0.5V
Fsw=260KHz
P_+1.8V_HG_25
P_+1.8V_PHASE_25
P_+1.8V_ILIM_10
P_+1.8V_PHASE_S
PC405 1UF/10V
PR402 30KOhm 1%
P_+1.8V_ILIMJP_10
PJP425 SHORTPIN /X
PQ401 SI4800BDY
EC31QS04
PD401 /X
PL400 1.0UH
PC406 4700PF/50V
P_+1.8V_SUR_S
PR408 10hm
PCE402 100U/2.5V
PCE403 100U/2.5V
PC407 10UF/6.3V
PC408 10UF/6.3V /X
P_+1.8V_LG_25
PR404 26.7KOhm 1%
PJP404 SHORTPIN /X
PC427 22PF/50V
PR460 130KOhm 1% /X
PR461 300KOhm 1% /X
PR405 10KOhm 1%
31 +1.8V_SEL1
31 +1.8V_SEL0
V1.01
PR405 => 11.5K
PR461 => 300K
PR460 => 130K
SEL0 SEL1 Voltage
L L 1.808V
X L 1.764
L X 1.705
X X 1.661
+0.9V / 1.5A
PU401 CM8562PGISTR
VIN
NC1(GND)
NC2(REFEN)
VOUT
GND2
GND1
VCCA
REFEN
+0.9VS
+0.9VO
PT403 TPC28T
PT404 TPC28T
PJP403 3MM_OPEN_5MIL
PC419 10UF/6.3V
PC420 10UF/6.3V
PC418 10UF/6.3V
PCE450 100U/2.5V
PC428 10UF/6.3V
P_+0.9V_REF_10
PRN1A 8.2KOhm
PRN1B 8.2KOhm
PRN1C 8.2KOhm
PRN1D 8.2KOhm
PC450 0.1UF/16V
PC415 & PC416 Close to DIMM
PC417 closed to VRAM
DDR Power Rev:1.00
<Variant Name>
Title :
Engineer:
<OrgName>
Size A3
Project Name
Rev 2.0G
Date: 日 10 , 月 15, 2007
Sheet 52 of 59

VID Set Rule :

Implemet Intel 965GM --> PR535 ~PR539

Implemet ATi M72S --> PR502, PR504 ->1.03V

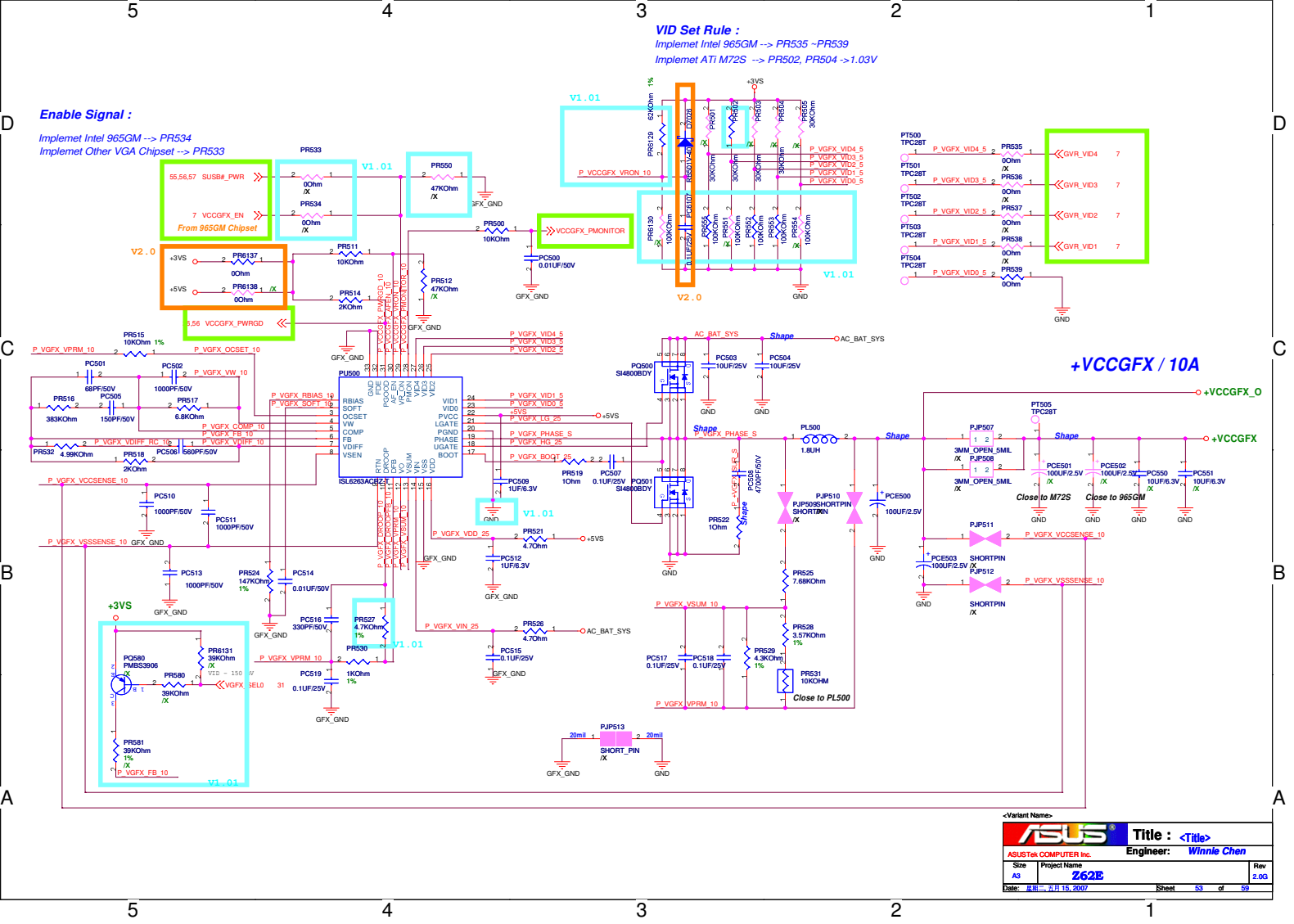
Enable Signal :

Implemet Intel 965GM --> PR534

Implemet Other VGA Chipset --> PR533

From 965GM Chipset

+VCCGFX / 10A



<Variant Name>

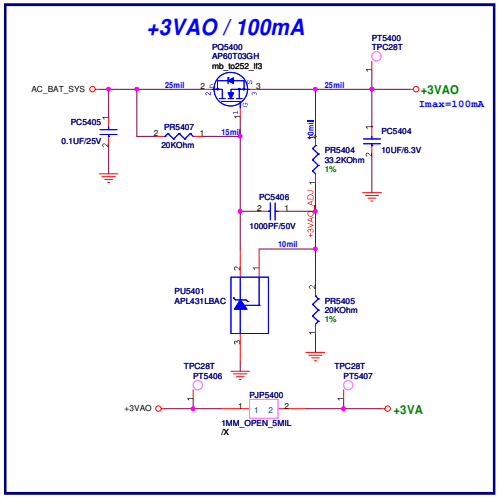
ASUSTek COMPUTER Inc.

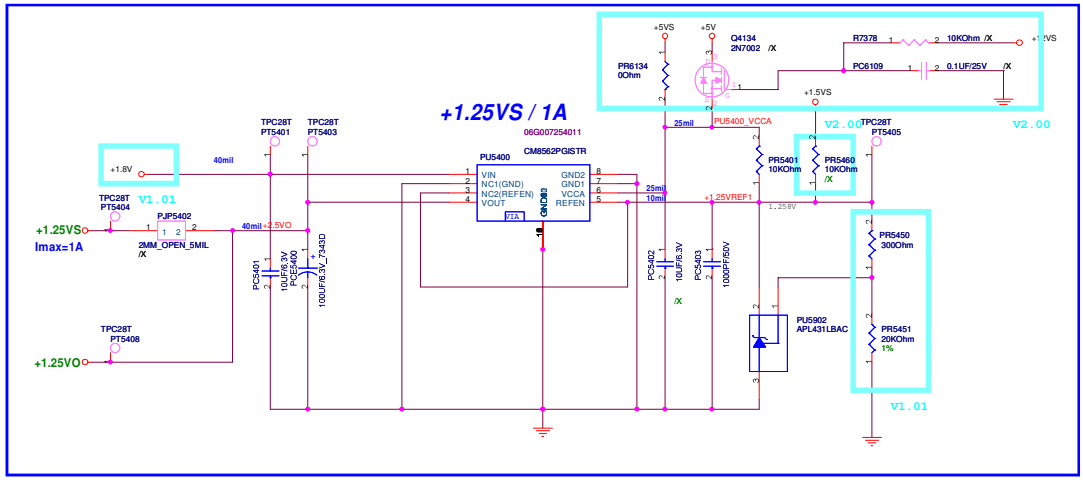
Title : <Title>

Engineer: Winnie Chen

Size	Project Name	Rev
A3	262E	2.0G

Date: 星期二, 五月 15, 2007 Sheet 53 of 59





<Variant Name>

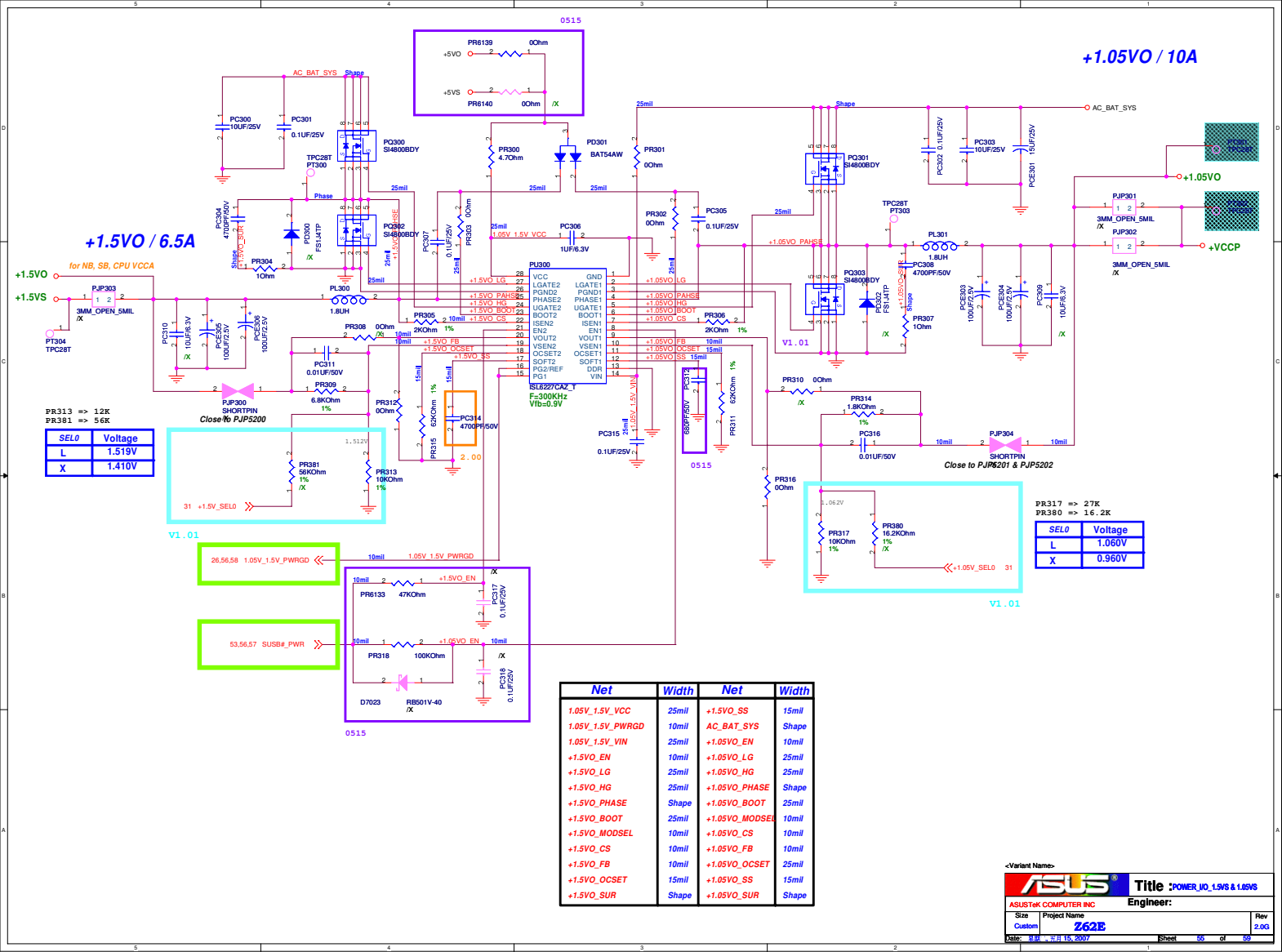
ASUSTek Computer INC.

Title : POWER_I/O_+3VA & +2.5V

Engineer:

Size	Project Name	Rev
Custom	Z84J	2.0G

Date: 星期 一, 五月 15, 2007 Sheet 54 of 59


+1.05VO / 10A
+1.5VO / 6.5A
for NB, SB, CPU VCCA
+1.5VO
+1.5VS
+1.05VO
+VCCP
AC_BAT_SYS
PR6139 0Ohm
PR6140 0Ohm /X
PC300 10UF/25V
PC301 0.1UF/25V
PQ300 SI4800BDY
PQ301 SI4800BDY
PQ302 SI4800BDY
PQ303 SI4800BDY
PD300 FSL4TP
PD301 BAT54AW
PR300 4.7Ohm
PR301 0Ohm
PR302 0Ohm
PC305 0.1UF/25V
PC306 1UF/6.3V
PC307 0.1UF/25V
PR303 0Ohm
PC302 0.1UF/25V
PC303 10UF/25V
PCE301 15UF/25V
PL301 1.8UH
PC308 4700PF/50V
PR307 1Ohm
PCE303 100UF/2.5V
PCE304 100UF/2.5V
PC309 10UF/6.3V
PJP301 3MM_OPEN_5MIL /X
PJP302 3MM_OPEN_5MIL /X
PJP303 3MM_OPEN_5MIL /X
PR304 1Ohm
PL300 1.8UH
PC304 4700PF/50V
PC310 10UF/6.3V
PCE305 100UF/2.5V
PCE306 100UF/2.5V
PR305 2KOhm 1%
PR306 2KOhm 1%
PR308 0Ohm /X
PC311 0.01UF/50V
PR309 6.8KOhm 1%
PJP300 SHORTPIN
Close to PJP5200
PR312 0Ohm
PR315 62KOhm 1%
PC314 4700PF/50V
PR310 0Ohm /X
PR314 1.8KOhm 1%
PC316 0.01UF/50V
PJP304 SHORTPIN
Close to PJP5201 & PJP5202
PR316 0Ohm
PC312 680PF/50V
PR311 62KOhm 1%
PC315 0.1UF/25V
PU300 ISL8227CAZ_T
F=300KHz
Vfb=0.9V
VCC GND
LGATE2 LGATE1
PGND2 PGND1
PHASE2 PHASE1
UGATE2 UGATE1
BOOT2 BOOT1
ISEN2 ISEN1
EN2 EN1
VOUT2 VOUT1
VSEN2 VSEN1
OCSET2 OCSET1
SOFT2 SOFT1
PG2/REF DDR
PG1 VIN
+1.05VO_LG
+1.05VO_PAHSE
+1.05VO_HG
+1.05VO_BOOT
+1.05VO_CS
+1.05VO_FB
+1.05VO_OCSET
+1.05VO_SS
1.05V_1.5V_VIN
TPC28T PT300
TPC28T PT303
TPC28T PT304
PR313 => 12K
PR381 => 56K
SEL0 Voltage
L 1.519V
X 1.410V
PR381 56KOhm 1% /X
PR313 10KOhm 1%
1.512V
31 +1.5V_SEL0
V1.01
PR317 => 27K
PR380 => 16.2K
SEL0 Voltage
L 1.060V
X 0.960V
PR317 10KOhm 1%
PR380 16.2KOhm 1% /X
1.062V
+1.05V_SEL0 31
V1.01
26,56,58 1.05V_1.5V_PWRGD
1.05V_1.5V_PWRGD
PR6133 47KOhm
PC317 0.1UF/25V
53,56,57 SUSB#_PWR
PR318 100KOhm
PC318 0.1UF/25V
D7023 RB501V-40 /X
0515
0515
Net Width Net Width
1.05V_1.5V_VCC 25mil +1.5VO_SS 15mil
1.05V_1.5V_PWRGD 10mil AC_BAT_SYS Shape
1.05V_1.5V_VIN 25mil +1.05VO_EN 10mil
+1.5VO_EN 10mil +1.05VO_LG 25mil
+1.5VO_LG 25mil +1.05VO_HG 25mil
+1.5VO_HG 25mil +1.05VO_PHASE Shape
+1.5VO_PHASE Shape +1.05VO_BOOT 25mil
+1.5VO_BOOT 25mil +1.05VO_MODSEL 10mil
+1.5VO_MODSEL 10mil +1.05VO_CS 10mil
+1.5VO_CS 10mil +1.05VO_FB 10mil
+1.5VO_FB 10mil +1.05VO_OCSET 25mil
+1.5VO_OCSET 15mil +1.05VO_SS 15mil
+1.5VO_SUR Shape +1.05VO_SUR Shape
<Variant Name>
Title :POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name 262E
Rev 2.0G
Date: 星期 一, 五月 15, 2007
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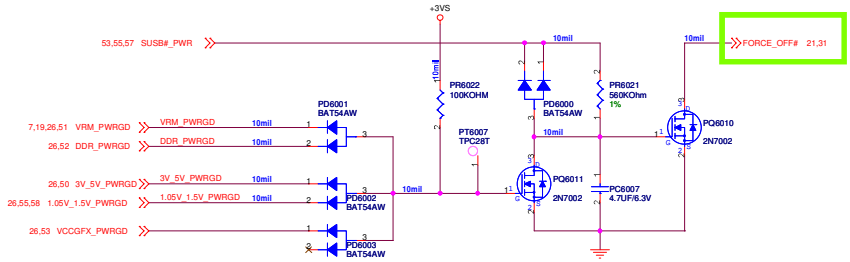
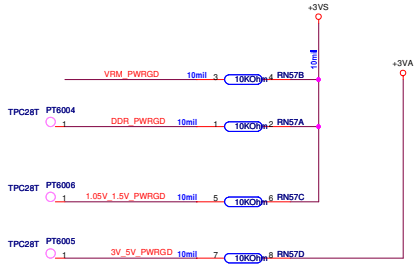
Power Good Detecter

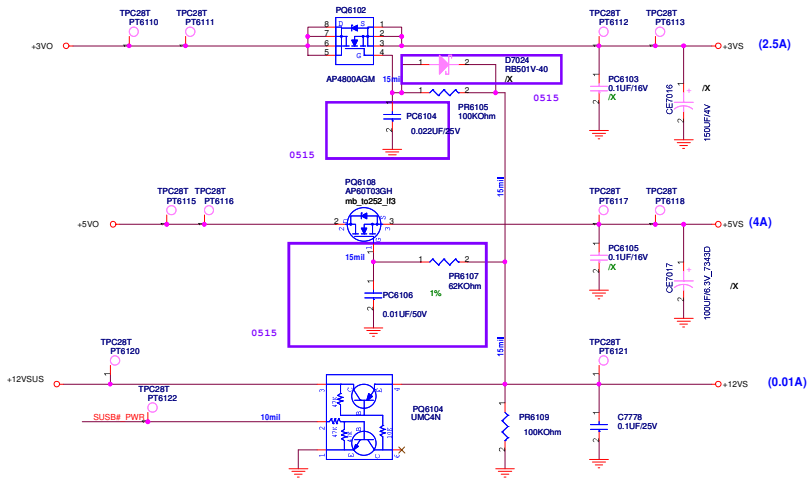




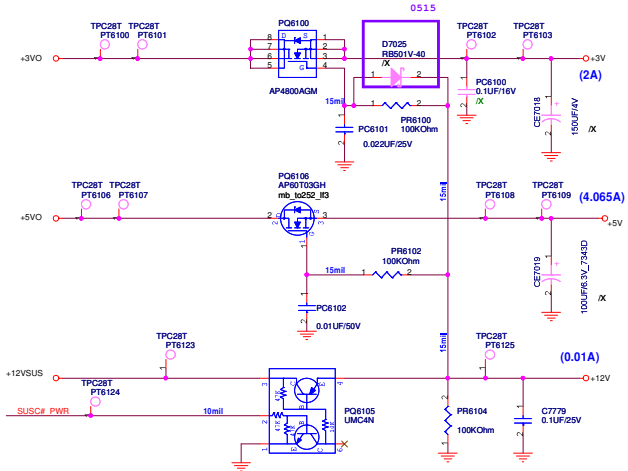
<Variant Name>

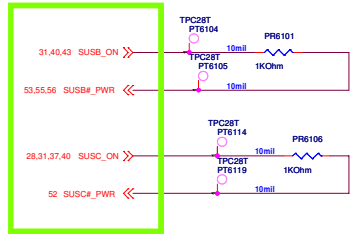
ASUSTek Computer INC.	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: 262E	Rev: 2.0G
Date: 星期 一, 五月 15, 2007	Sheet 58 of 59	

SUSB#_PWR POWER



SUSC#_PWR POWER





<variant_name>

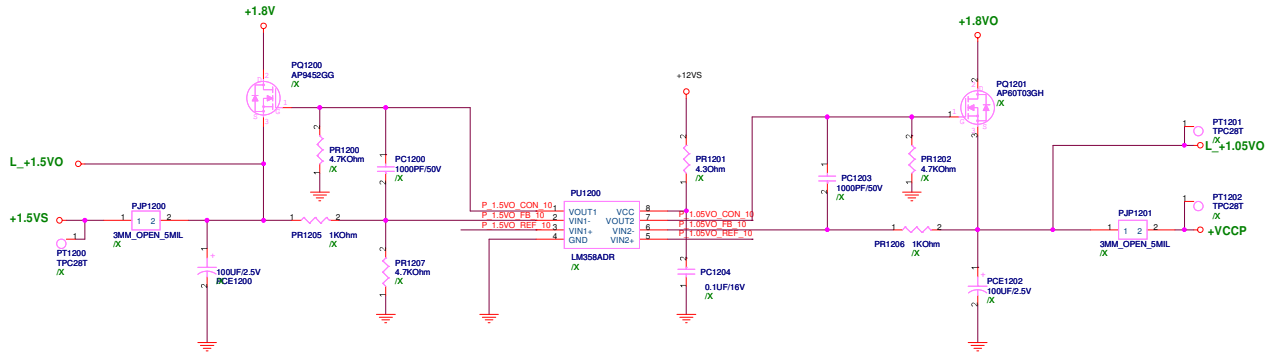
ASUSTek Computer INC.

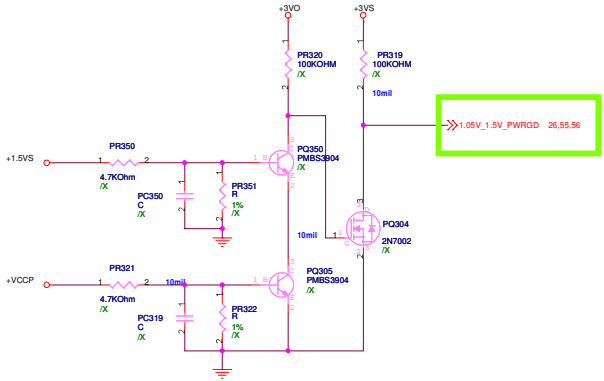
Title : POWER_LOAD SWITCH

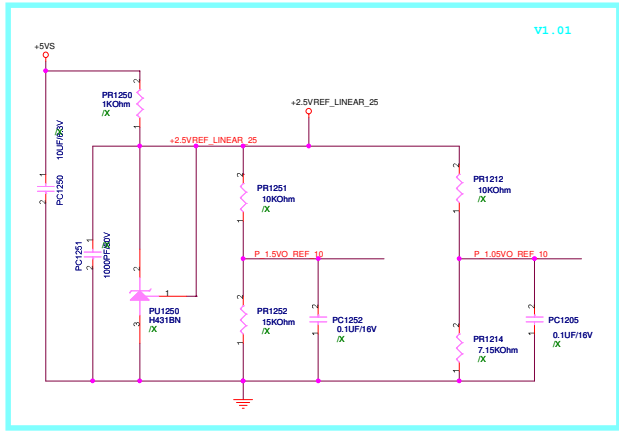
Engineer:

Size	Project Name	Rev
Custom	262E	2.0G

Date: 星期 二月 15, 2007 Sheet 57 of 59







<variant_name>

<OrgName>	Title : POWER_I/O_DDR & VTT	
	Engineer:	
Size: Custom	Project Name: 298S	Rev: 2.0G
Date: 星期 二 月 15, 2007	Sheet 58 of 59	

2007/05/15 Follow EN-0035869 to modify circuit.

<Variant Name>

Title : History(1)

ASUSTek COMPUTER INC

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z62E	2.0G

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