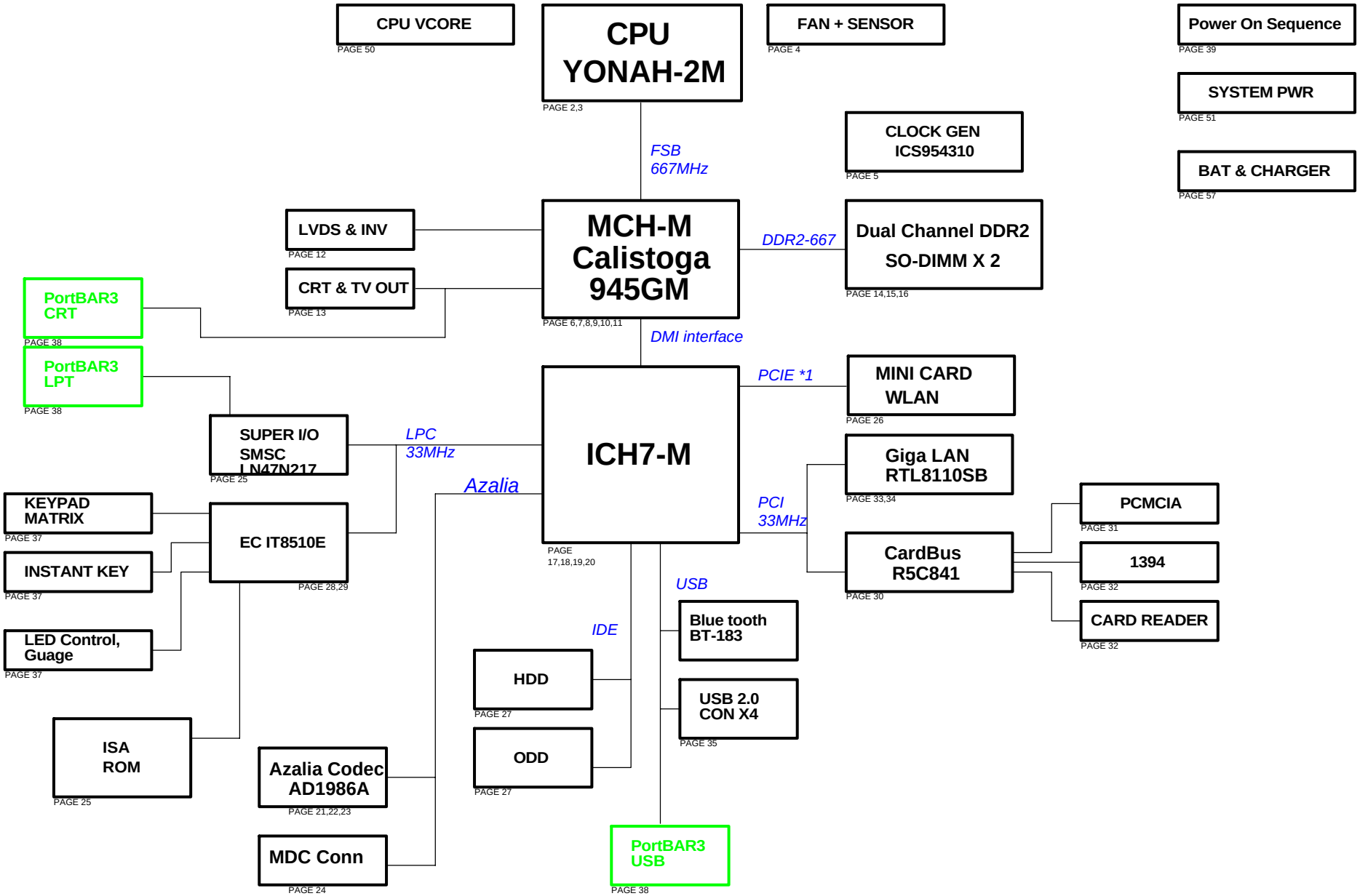
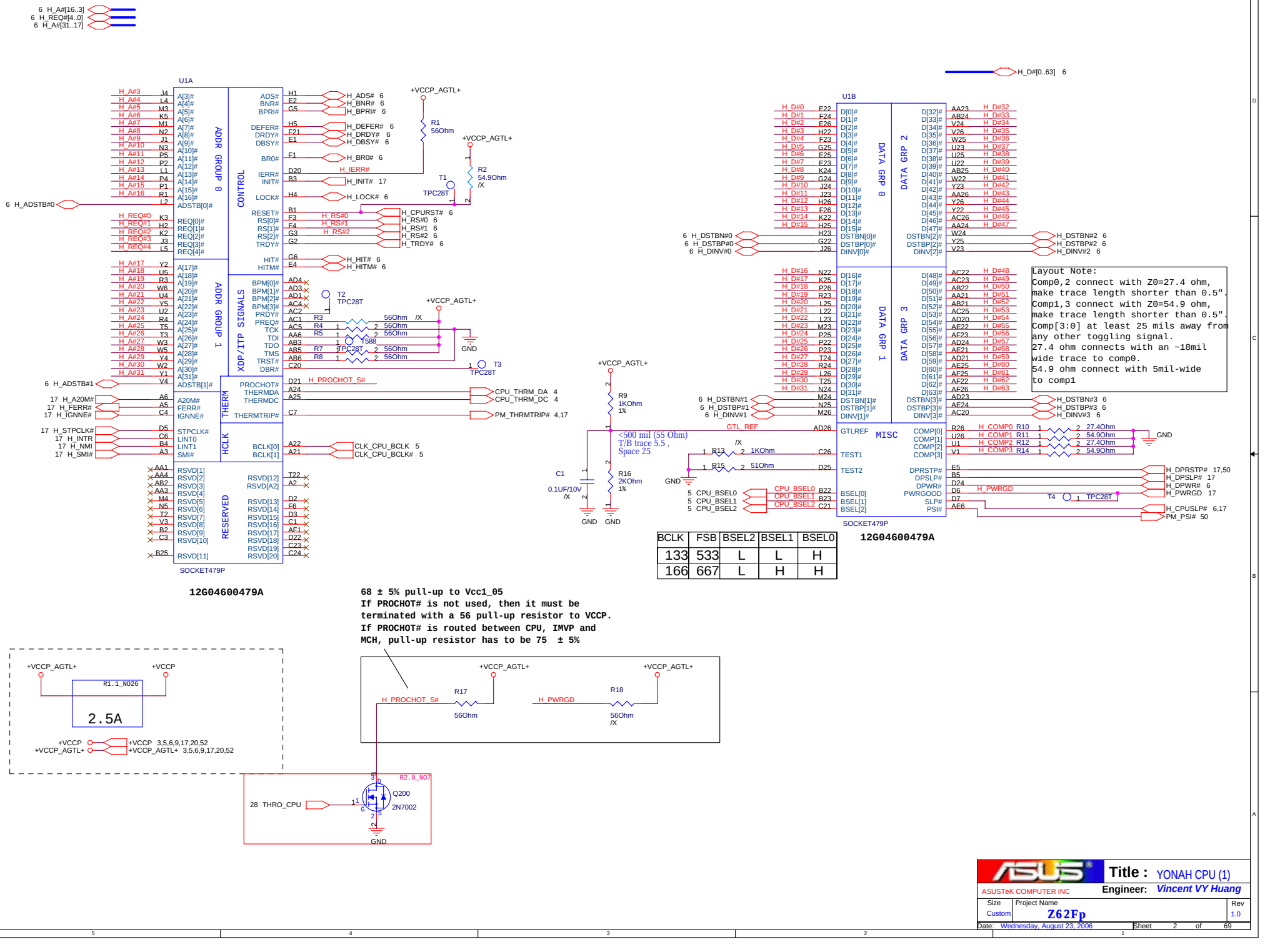
Z62FM Block Diagram



Title : BLOCK DIAGRAM		
ASUSTeK COMPUTER INC	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 1 of 69	



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Title : YONAH CPU (1)

ASUSTeK COMPUTER INC Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 2 of 69

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP_AGTL+ → +VCCP_AGTL+ 2,5,6,9,17,20,52

+VCORE, +1.5VS → +VCORE 50, +1.5VS 9,10,20,26,36,52

U1C

+VCORE

SOCKET479P

12G04600479A

+VCCP_AGTL+

+VCCA_CPU

RN1A 0Ohm

H_VID0 H_VID1 H_VID2 H_VID3 H_VID4 H_VID5 H_VID6

RN2D RN2C RN2B RN2A RN1D RN1C RN1B 0Ohm

VR_VID0 50, VR_VID1 50, VR_VID2 50, VR_VID3 50, VR_VID4 50, VR_VID5 50, VR_VID6 50

VCCSENSE, VSSSENSE

R19 100Ohm

VCCSENSE 50, VSSSENSE 50

R20 100Ohm

GND

VCCSENCE/VSSSENCE need to be routed as 27.4ohm

Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

Place pull-up/down resisters within 1 inch of CPU.

U1D

SOCKET479P

12G04600479A

Vcc Core Decoupling Caps
Place these on bottom side.

+VCORE

Place these caps on North side Secondary

CE1 330UF/2V_7343D /X

Place these caps on North side Secondary

C2 C3 C4 C5 C6 C7 C8 C9 10UF/6.3V /X

Place these caps on North side Primary

C12 C13 C14 C15 C16 10UF/6.3V /X

Place these caps on South side Primary

C18 C19 C20 C21 C22 10UF/6.3V /X

Place these caps on South side Secondary

C24 C25 C26 C27 C28 C29 C30 C31 10UF/6.3V /X

Place these caps on South side Secondary

CE4 330UF/2V_7343D /X

checklist suggests 0.1uF X5R

checklist suggests 10uF POSCAP

Close to B26 (VCCA)

+VCCA_CPU 120mA / 20mil

+VCCA_PROC

C41 10UF/10V C40 0.01UF/10V

GND

+1.5VS → +VCCA_CPU

0.12A

+VCCP_AGTL+

CE54 100UF/2.5V

C34 C35 C36 C37 C38 C39 0.1UF/10V

+V1.05S (VCCP_CPU) Decoupling Capacitor (Place near CPU)

ASUSTeK COMPUTER INC

Title : Yonah CPU (2)

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 3 of 69

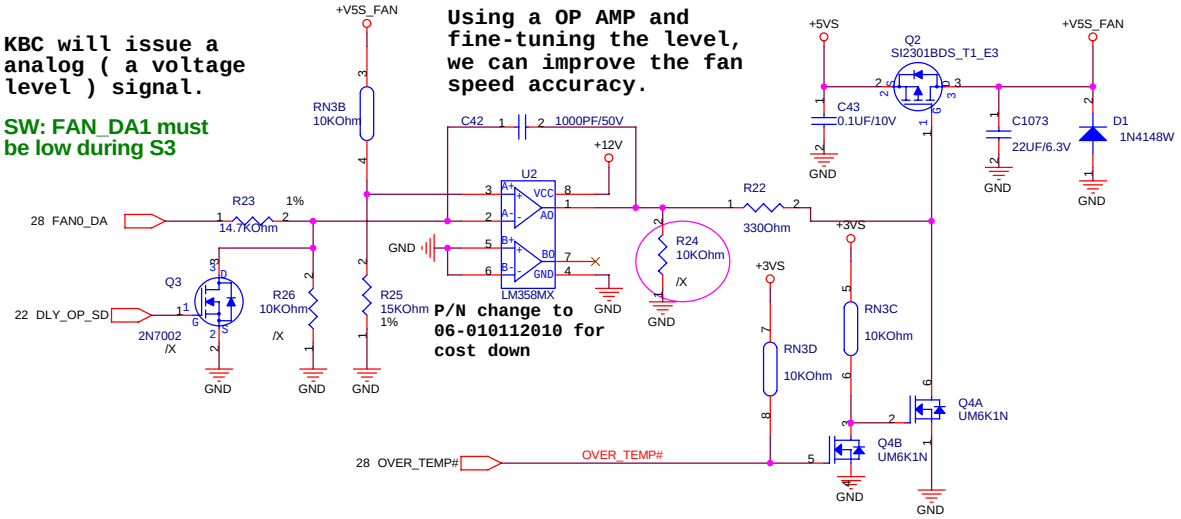
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

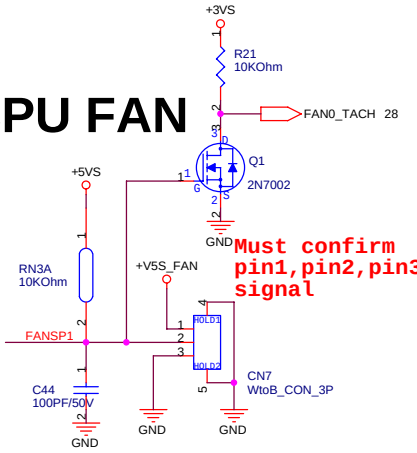
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

P/N change to 06-010112010 for cost down



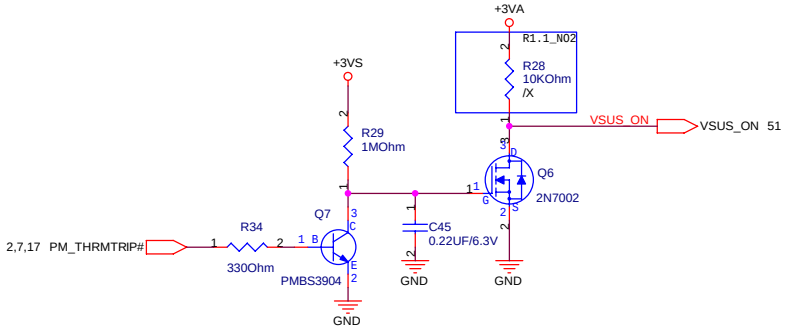
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

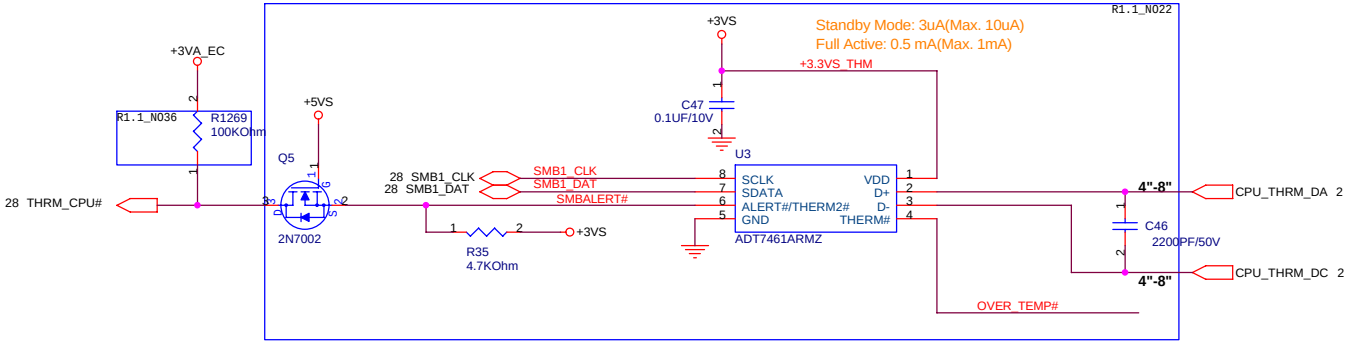
CPU FAN



+VCORE	+VCORE 3,50
+12V	+12V 35,36,61
+5VS	+5VS 13,19,20,21,22,27,36,37,38,50,61
+3VS	+3VS 5,7,9,11,12,13,14,15,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61
+3VA	+3VA 12,20,22,24,25,28,29,39,54,59,63

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTeK COMPUTER INC	Title : THER-SENSOR,FAN	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 4 of 69	

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	None

		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ +VCCP_AGTL+ 2,3,6,9,17,20,52

+3VS +3VS 4,7,9,11,12,13,14,15,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61

PLACE termination close to source IC

Pin34 is PWRSAVE#

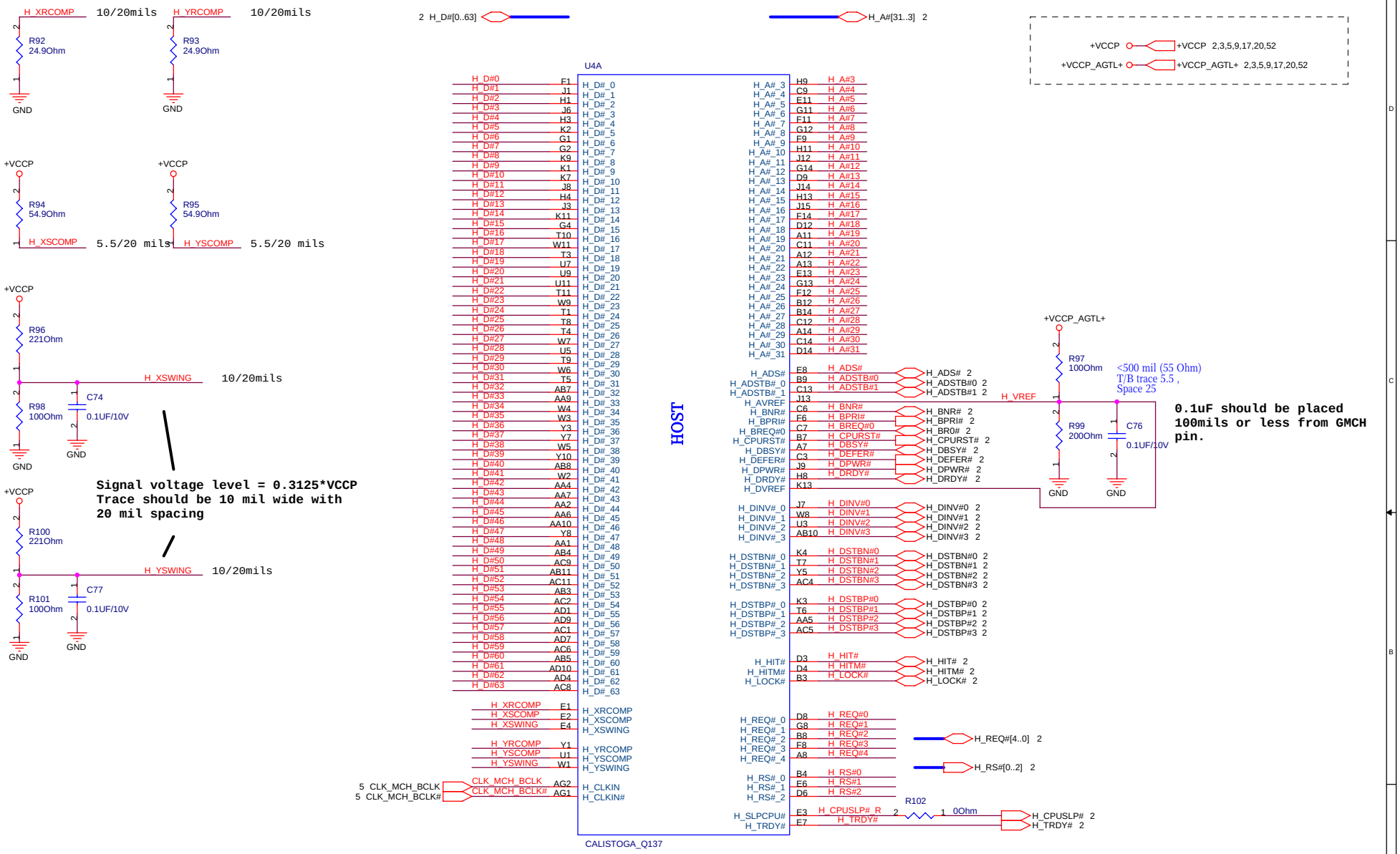
IC1 — ICS954310BGLFT

R1.1_N046

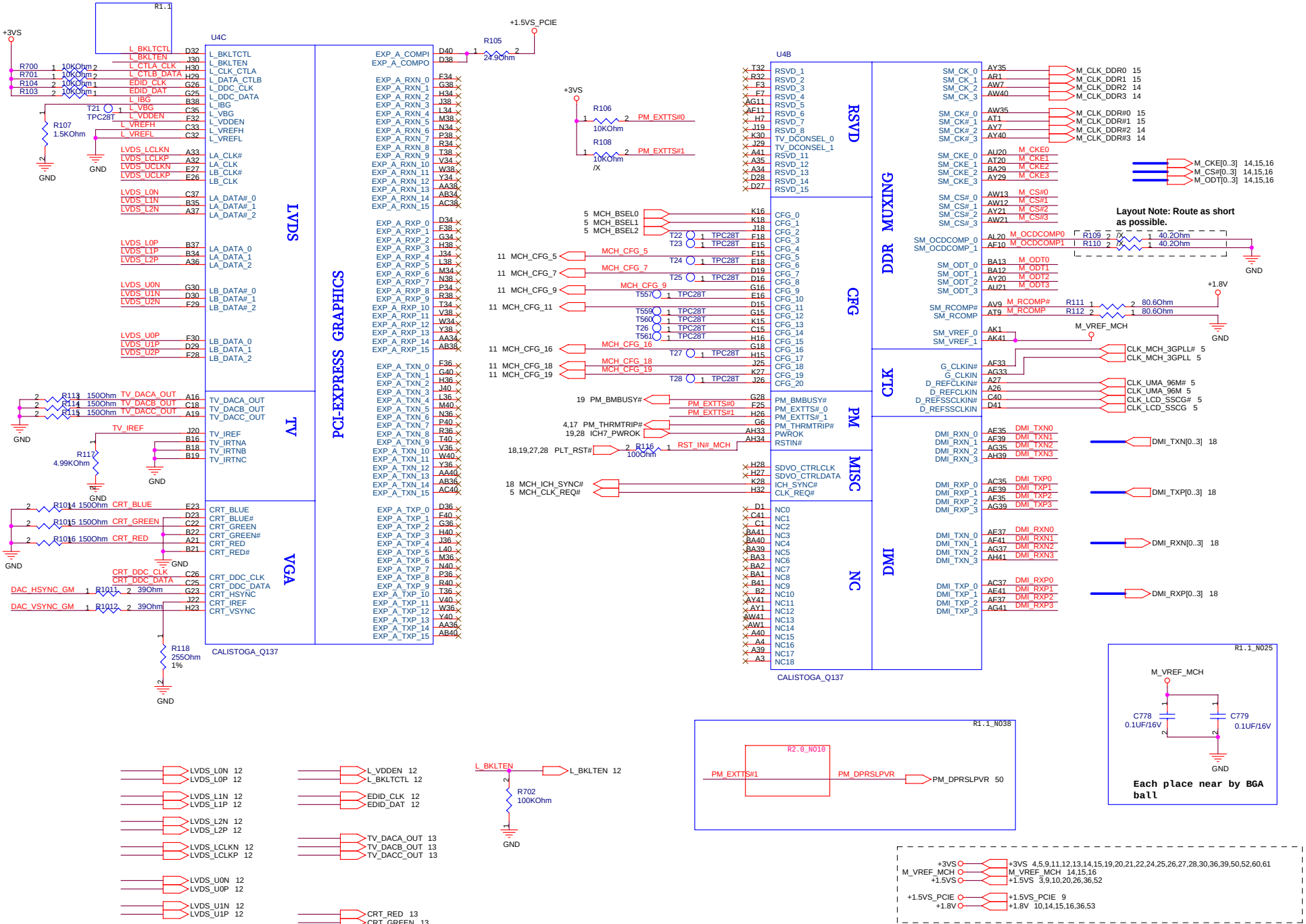
R70,R77,R79,R83 change to 39ohm

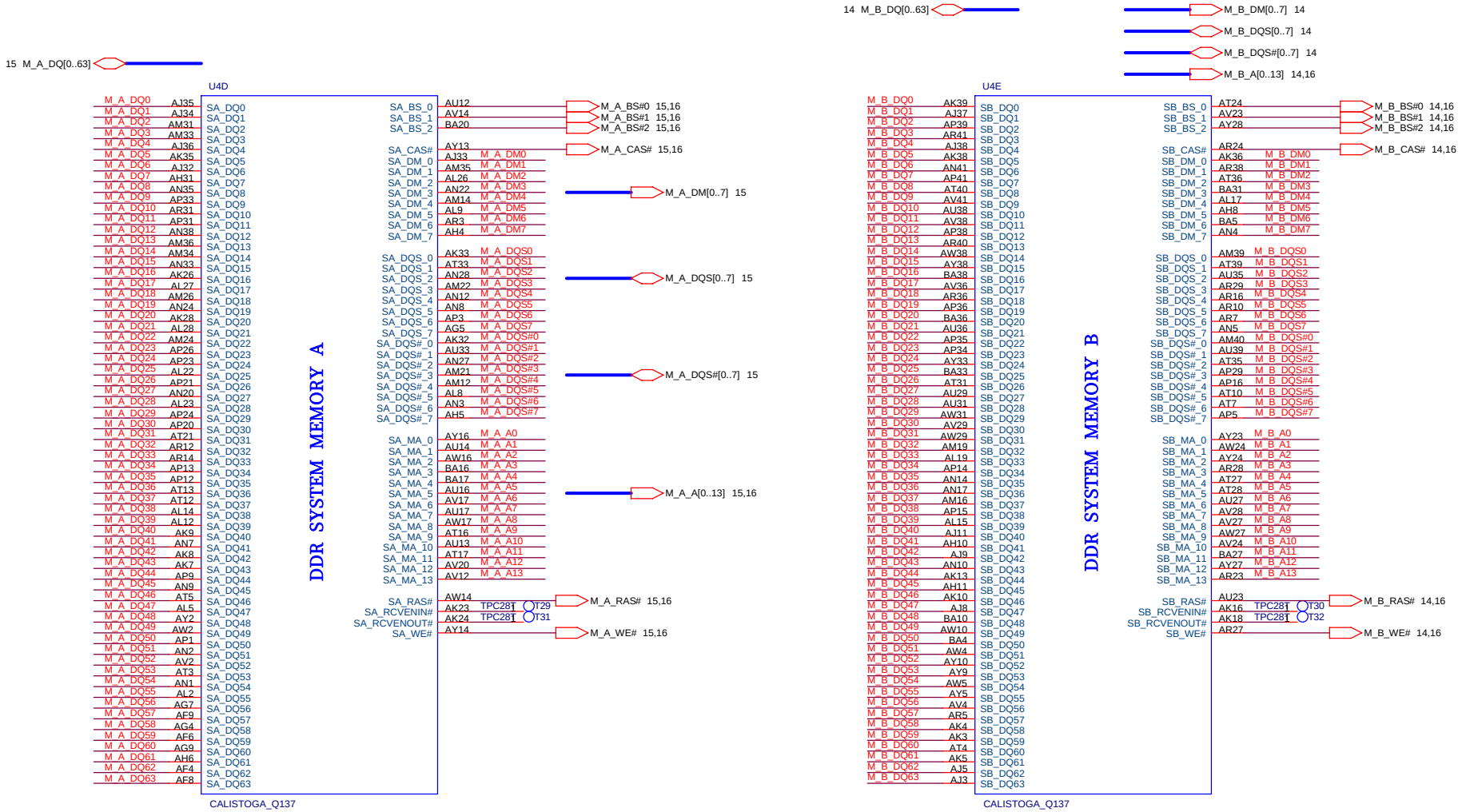
internal pull high

Title :	CLOCK GEN		
ASUSTeK COMPUTER INC		Engineer:	Vincent VY Huang
Size	Project Name		Rev
Custom	Z62Fp		1.0
Date:	Wednesday, August 23, 2006	Sheet	5 of 69



ASUSTeK COMPUTER INC	Title : Calistoga MCH (1)		
	Engineer: Vincent VY Huang		
Size: Custom	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 6 of 69		


U4C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
U4B
RSVD
CFG
PM
MISC
NC
DMI
DDR MUXING
CLK
Layout Note: Route as short as possible.
Each place near by BGA ball
Title : Calistoga PCI-E (2)
ASUSTeK COMPUTER INC
Engineer: Vincent VY Huang
Size: Custom
Project Name: Z62Fp
Rev: 1.0
Date: Wednesday, August 23, 2006
Sheet 7 of 69



ASUSTeK COMPUTER INC	Title : Calistoga DDR2 (3)		
	Engineer: Vincent VY Huang		
Size: Custom	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 8 of 69		

VCCA_3GBG

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

+1.05VS 3500 mA
+1.5VS 5500mA

where VCCD_HMPLL 150 mA?

+VCCP_AGTL+ 2,3,5,6,17,20,52
+VCCP_GMCH 10
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61
+2.5VS 13,36,54
+1.5VS 3,10,20,26,36,52

+VCCP
+VCCP_GMCH
3MM_OPEN_5MIL /X JP28
3MM_OPEN_5MIL /X JP29
R1.1_N05

PLACE IN CAVITY
C79 4.7UF/10V
C80 2.2UF/6.3V
GND

PLACE ON THE EDGE
800 mA
+VCCP_AGTL+
C81 0.22UF/6.3V
CE8 330UF/2V_7343D /X
R1.1_N040
GND

+2.5VS
C900 0.1UF/10V
C898 0.01UF/25V
C899 0.1UF/10V
C901 0.1UF/10V
C91 0.1UF/10V
C92 4.7UF/10V
VCC_SYNC, near GMCH
VCCA_LVDS 10 mA
VCCA_3GBG 2 mA
VCCTX_LVDS 60 mA
D77 BAT54C
R1026 10Ohm
+VCCP_GMCH
L87 120Ohm/100Mhz
+2.5VS_CRTDAC
70 mA
VCCA_CRTDAC
C902 0.022UF/25V
C903 0.1UF/10V

+1.5VS
L88 120Ohm/100Mhz
VCC3G
+1.5VS_PCIE
1500 mA
C955 0.1UF/10V
C904 10UF/10V
C905 10UF/10V

+1.5VS_3GPLL
L90 30Ohm/100Mhz
VCCA3GPLL
C82 0.1UF/10V
C83 10UF/10V

+1.5VS_VCCAUX
R1.1_N037
VCCAUX
Place filter components close to GMCH
CE50 10UF/10V
C912 0.1UF/10V

L3 30Ohm/100Mhz
+1.5VS_DPLLA
VCCA_DPLLA 50 mA
CE10 470UF/2.5V /X
C916 0.1UF/10V

L4 30Ohm/100Mhz
+1.5VS_DPLLB
VCCA_DPLLB 50 mA
CE13 470UF/2.5V /X
C919 0.1UF/10V

L5 120Ohm/100Mhz
+1.5VS_HPLL
VCCA_HPLL 45 mA
C920 22UF/6.3V
C85 0.1UF/10V

L6 120Ohm/100Mhz
+1.5VS_MPLL
VCCA_MPLL 45 mA
C921 22UF/6.3V
C87 0.1UF/10V

+1.5VS
VCCD_LVDS 20 mA
C95 0.1UF/10V
C96 10UF/10V

+1.5VS
VCCD_TVDAC 24 mA
C84 0.022UF/25V
C909 0.1UF/10V

+1.5VS
VCCDQ_TVDAC
C86 0.022UF/25V
C913 0.1UF/10V

U4H
CALISTOGA_Q137

H22	VCCSYNC	
C30	VCC_TXLVDS0	
B30	VCC_TXLVDS1	
A30	VCC_TXLVDS2	
AJ41	VCC3G0	
AB41	VCC3G1	
Y41	VCC3G2	
V41	VCC3G3	
R41	VCC3G4	
N41	VCC3G5	
L41	VCC3G6	
AC33	VCCA_3GPLL	
G41	VCCA_3GBG	
H41	VSSA_3GBG	
F21	VCCA_CRTDAC0	
F21	VCCA_CRTDAC1	
G21	VSSA_CRTDAC	
B26	VCCA_DPLLA	
C39	VCCA_DPLLB	
AF1	VCCA_HPLL	
A38	VCCA_LVDS	
B39	VSSA_LVDS	
AF2	VCCA_MPLL	
H20	VCCA_TVBG	
G20	VSSA_TVBG	
E19	VCCA_TVDACA0	
F19	VCCA_TVDACA1	
C20	VCCA_TVDACB0	
D20	VCCA_TVDACB1	
E20	VCCA_TVDACC0	
F20	VCCA_TVDACC1	
AH1	VCCD_HMPLL0	
AH2	VCCD_HMPLL1	
A28	VCCD_LVDS0	
B28	VCCD_LVDS1	
C28	VCCD_LVDS2	
D21	VCCD_TVDAC	
A23	VCC_HV0	
B23	VCC_HV1	
B25	VCC_HV2	
H19	VCCD_QTVDAC	
AK31	VCCAUX0	
AF31	VCCAUX1	
AE31	VCCAUX2	
AC31	VCCAUX3	
AL30	VCCAUX4	
AK30	VCCAUX5	
AJ30	VCCAUX6	
AH30	VCCAUX7	
AG30	VCCAUX8	
AF30	VCCAUX9	
AE30	VCCAUX10	
AD30	VCCAUX11	
AC30	VCCAUX12	
AG29	VCCAUX13	
AF29	VCCAUX14	
AE29	VCCAUX15	
AD29	VCCAUX16	
AC29	VCCAUX17	
AG28	VCCAUX18	
AF28	VCCAUX19	
AE28	VCCAUX20	
AH22	VCCAUX21	
AJ21	VCCAUX22	
AH21	VCCAUX23	
AJ20	VCCAUX24	
AH20	VCCAUX25	
AH19	VCCAUX26	
P19	VCCAUX27	
P16	VCCAUX28	
AH15	VCCAUX29	
P15	VCCAUX30	
AH14	VCCAUX31	
AG14	VCCAUX32	
AF14	VCCAUX33	
AE14	VCCAUX34	
Y14	VCCAUX35	
AF13	VCCAUX36	
AE13	VCCAUX37	
AF12	VCCAUX38	
AE12	VCCAUX39	
AD12	VCCAUX40	

AC14	VTT_0
AB14	VTT_1
W14	VTT_2
V14	VTT_3
T14	VTT_4
R14	VTT_5
P14	VTT_6
N14	VTT_7
M14	VTT_8
L14	VTT_9
AD13	VTT_10
AC13	VTT_11
AB13	VTT_12
AA13	VTT_13
Y13	VTT_14
W13	VTT_15
V13	VTT_16
U13	VTT_17
T13	VTT_18
R13	VTT_19
N13	VTT_20
M13	VTT_21
L13	VTT_22
AB12	VTT_23
AA12	VTT_24
Y12	VTT_25
W12	VTT_26
V12	VTT_27
U12	VTT_28
T12	VTT_29
R12	VTT_30
P12	VTT_31
N12	VTT_32
M12	VTT_33
L12	VTT_34
R11	VTT_35
P11	VTT_36
N11	VTT_37
M11	VTT_38
R10	VTT_39
P10	VTT_40
N10	VTT_41
M10	VTT_42
P9	VTT_43
N9	VTT_44
M9	VTT_45
R8	VTT_46
P8	VTT_47
N8	VTT_48
M8	VTT_49
P7	VTT_50
N7	VTT_51
M7	VTT_52
R6	VTT_53
P6	VTT_54
M6	VTT_55
A6	VTT_56
R5	VTT_57
P5	VTT_58
N5	VTT_59
M5	VTT_60
P4	VTT_61
N4	VTT_62
M4	VTT_63
R3	VTT_64
P3	VTT_65
N3	VTT_66
M3	VTT_67
R2	VTT_68
P2	VTT_69
M2	VTT_70
D2	VTT_71
AB1	VTT_72
R1	VTT_73
P1	VTT_74
N1	VTT_75
M1	VTT_76

POWER

+VCCP_AGTL+
VTTLF_CAP3
C88 0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C89 0.47UF/16V
C90 0.22UF/6.3V

+3VS
VCCHV 40 mA
C93 10UF/10V
C94 0.1UF/10V

+3VS
D78 BAT54C
R1027 10Ohm
+1.5VS
L89 180Ohm/100Mhz
C906 10UF/10V

+3.3VS_TVBG
VCCA_TVBG
C907 0.022UF/25V
C908 0.1UF/10V

+3.3VS_TVDACA
VCCA_TVDACA
C910 0.022UF/25V
C911 0.1UF/10V

+3.3VS_TVDACB
VCCA_TVDACB
C914 0.022UF/25V
C915 0.1UF/10V

+3.3VS_TVDACC
VCCA_TVDACC
C917 0.022UF/25V
C918 0.1UF/10V
all 120 mA

R2.0_N012
+1.5VS
C956 0.1UF/10V
C957 0.1UF/10V
C958 0.1UF/10V
C959 0.1UF/10V

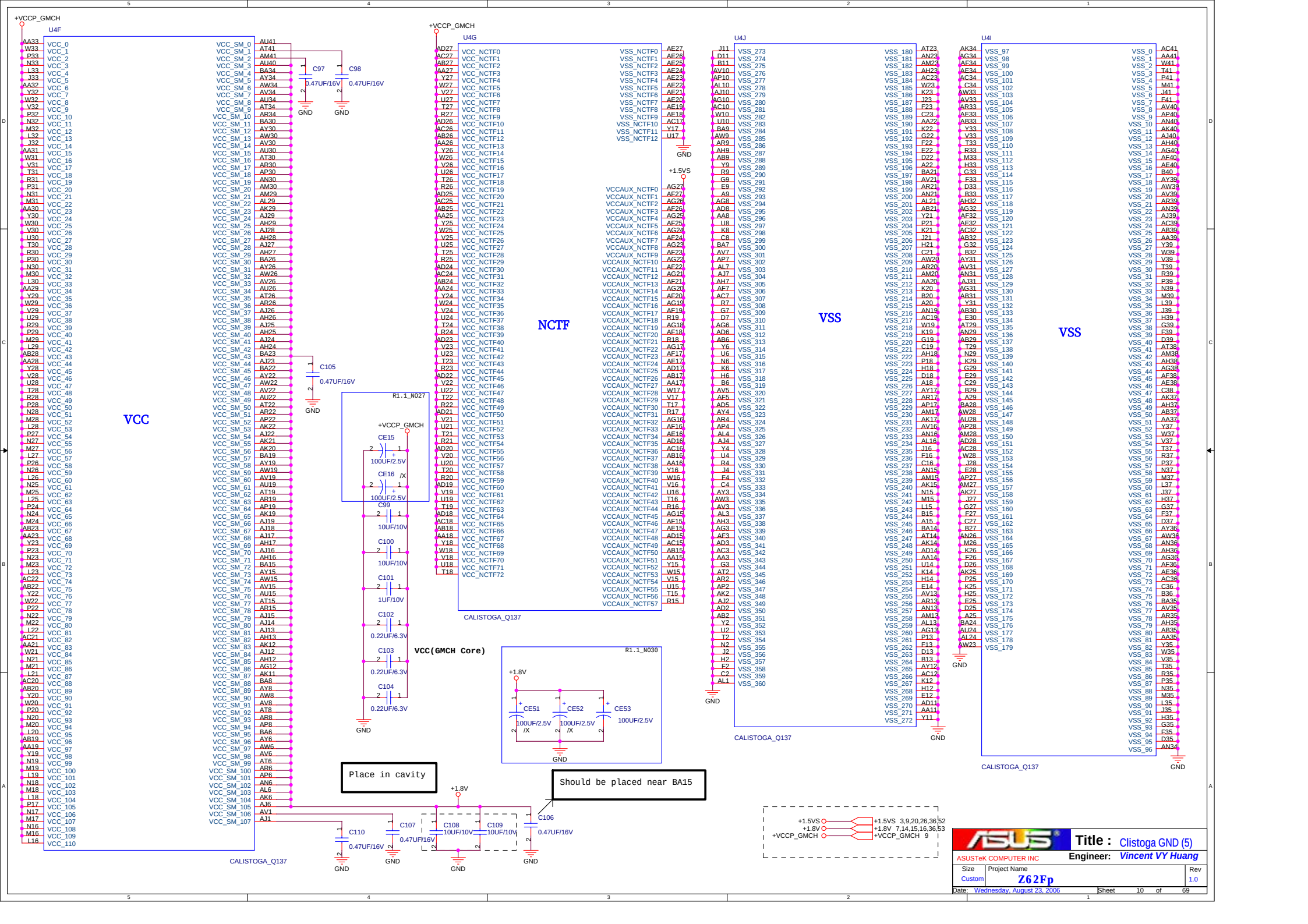
NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

ASUSTeK COMPUTER INC

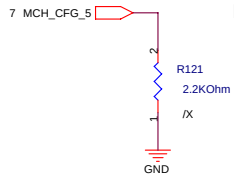
Title : Calistoga Power (4)
Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 9 of 69

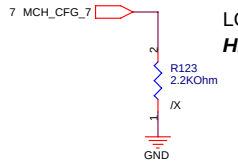

U4F
VCC
CALISTOGA_Q137
U4G
NCTF
CALISTOGA_Q137
U4J
VSS
CALISTOGA_Q137
U4I
VSS
CALISTOGA_Q137
VCC(GMCH Core)
Place in cavity
Should be placed near BA15
Title : Clistoga GND (5)
ASUSTeK COMPUTER INC
Engineer: Vincent VY Huang
Size Custom
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 10 of 69

CFG5 : DMI X2 Select



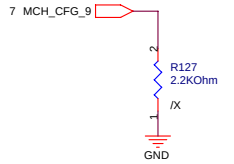
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP



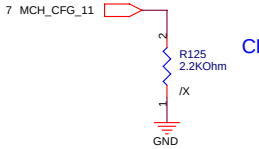
LOW = Reserved
HIGH = Mobility CPU (Default)

CFG9 : PCIE GRAPHIC LANE

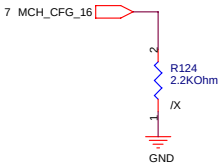


LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)

CFG11 : Reserved but need to be pull low

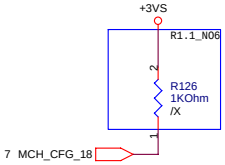


CFG16 : FSB DYNAMIC ODT



LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

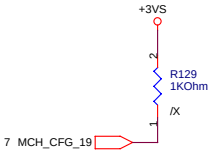
CFG18 : GMCH Core Voltage Level



LOW = 1.05V (Default)
HIGH = 1.5V

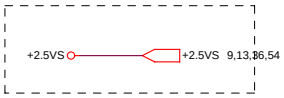
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG19 : DMI LANE REVERSAL



LOW = NORMAL
HIGH = LANES REVERSED

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



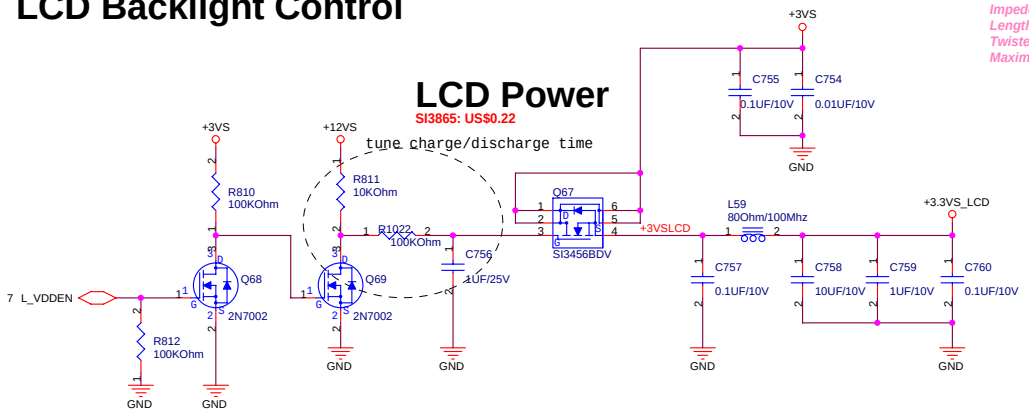
ASUSTeK COMPUTER INC
Title : Calistoga Strapping
Engineer: Vincent VY Huang
Size: Custom | Project Name: Z62Fp | Rev: 1.0
Date: Wednesday, August 23, 2006 | Sheet 11 of 69

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

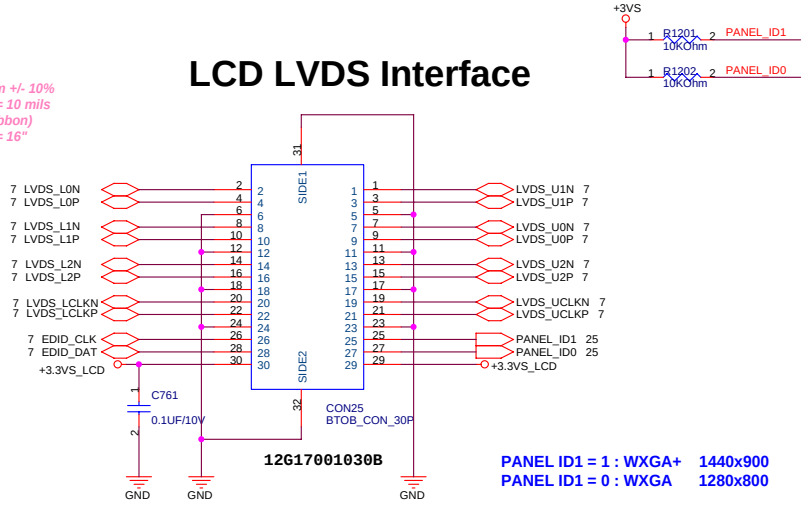
LCD Power

SI3865: US$0.22



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface



12G17001030B

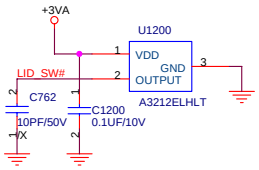
PANEL ID1 = 1 : WXGA+ 1440x900
PANEL ID1 = 0 : WXGA 1280x800

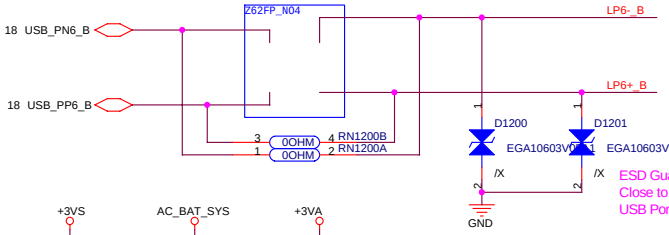
PANEL ID0 RESERVE FOR VENDOR

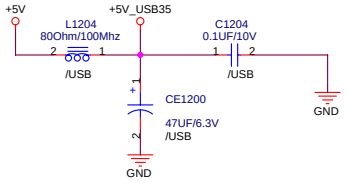
INVERTER Interface

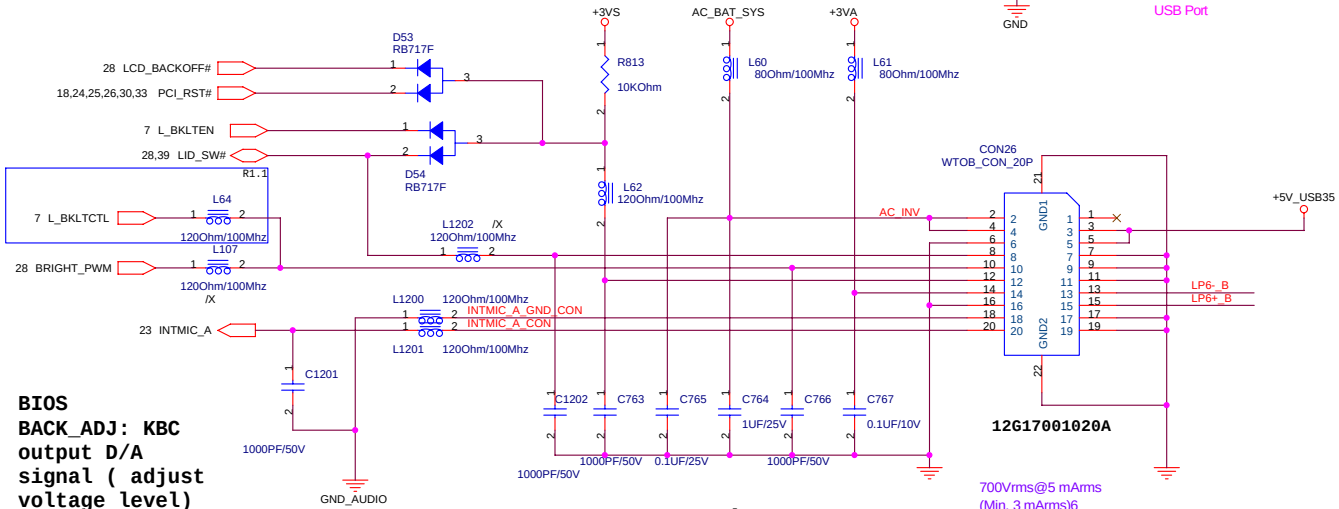
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

Magnatic Switch For LID_SW# On/OFF









12G17001020A

700Vrms@5 mArms (Min. 3 mArms)6 mArms(Max. 6.5 mArms)

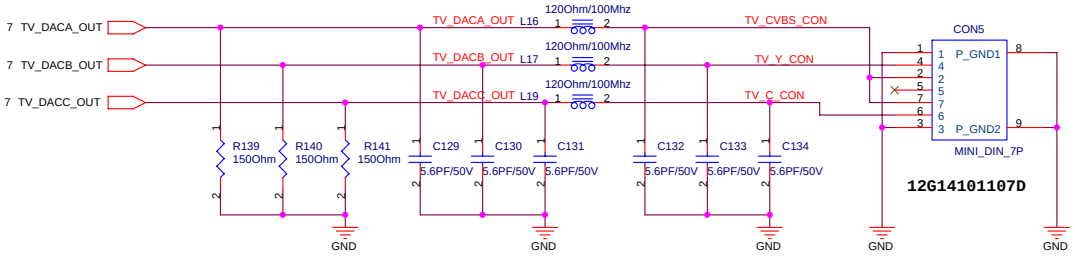
BIOS
BACK_ADJ: KBC output D/A signal (adjust voltage level) to adjust Back light.

Inverter Board built in 14.1W LCD Panel

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 12 of 69	

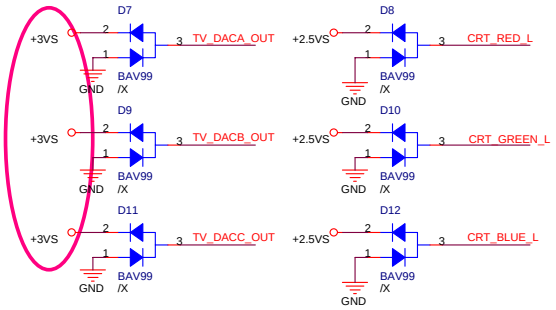
TV OUT

checklist suggests
150ohm/100MHz & 6pF



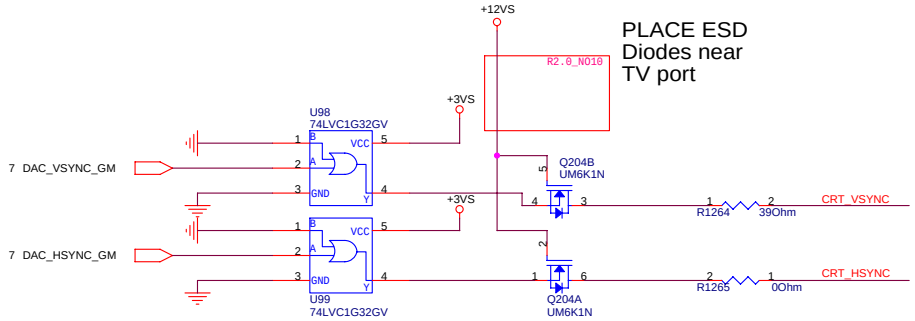
12G14101107D

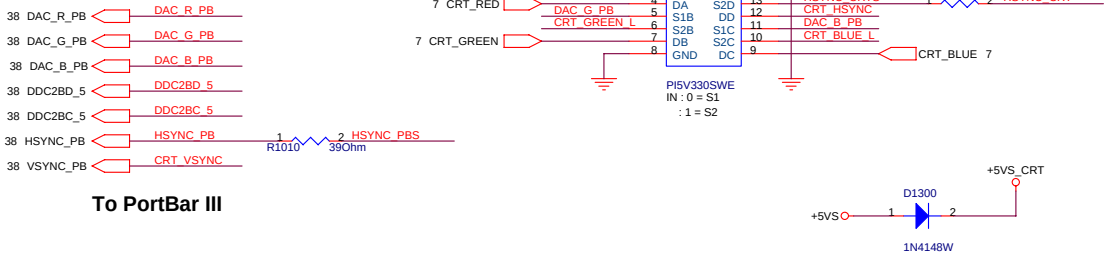
Place Terminator
close to
Connector



PLACE ESD
Diodes near
TV port

PLACE ESD
Diodes near
VGA port

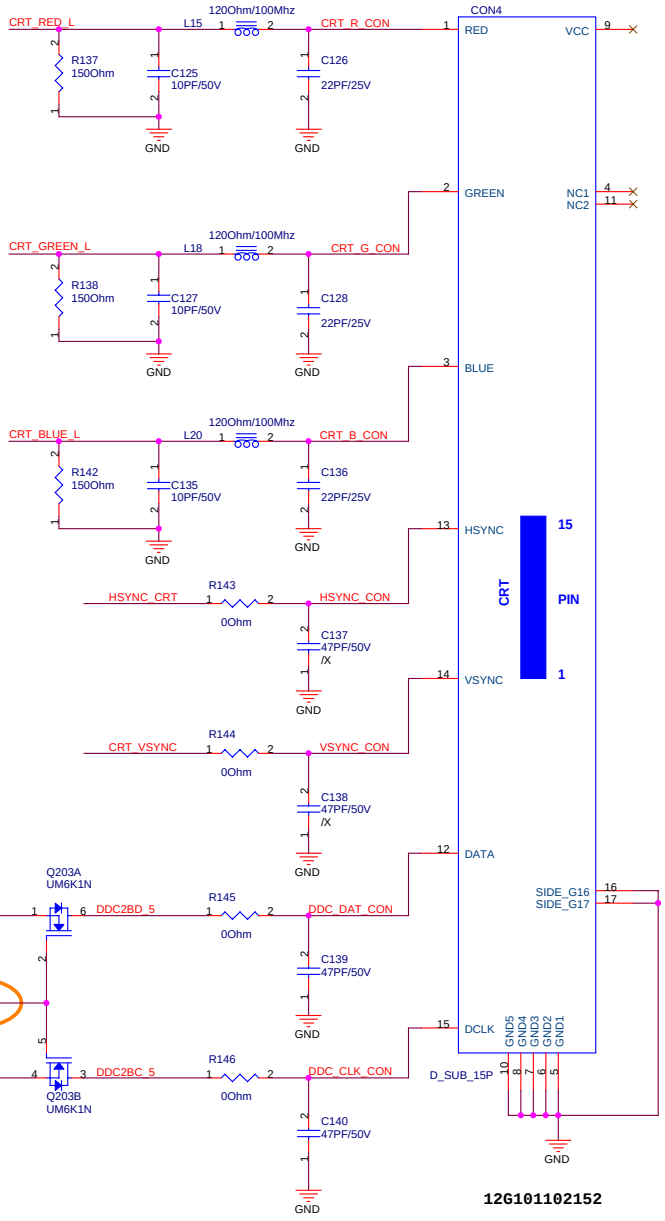




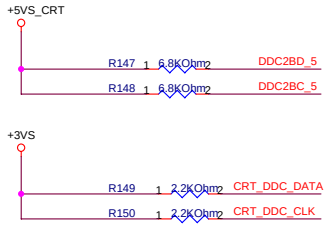
To PortBar III

CRT OUT

checklist suggests 47ohm/100MHz



12G101102152



ASUSTeK COMPUTER INC

Title : CRT & TV OUT

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 13 of 69

NO STUFF *

M_CLK_DDR3

PLACE NEAR SO-DIMM_0

M_CLK_DDR#3

M_CLK_DDR2

PLACE NEAR SO-DIMM_0

M_CLK_DDR#2

8,16 M_B_A[0..13]

M_VREF_DIMM1 — M_VREF_DIMM1 7,15,16
+1.8V — +1.8V 7,10,15,16,36,53
+3VS — +3VS 4,5,7,9,11,12,13,15,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61

M_B_DQ[0..63] 8

U5A

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10/AP
M_B_A11 90 A11
M_B_A12 89 A12
M_B_A13 116 A13
86 A14
84 A15
85 A16_BA2

8,16 M_B_BS#2
8,16 M_B_BS#0 107 BA0
8,16 M_B_BS#1 106 BA1
7,16 M_CS#2 110 S0#
7,16 M_CS#3 115 S1#
7 M_CLK_DDR2 30 CK0
7 M_CLK_DDR#2 32 CK0#
7 M_CLK_DDR3 164 CK1
7 M_CLK_DDR#3 166 CK1#
7,16 M_CKE2 79 CKE0
7,16 M_CKE3 80 CKE1
8,16 M_B_CAS# 113 CAS#
8,16 M_B_RAS# 108 RAS#
8,16 M_B_WE# 109 WE#
198 SA0
200 SA1
5,15,19,24,26 SMB_CLK_S 197 SCL
5,15,19,24,26 SMB_DAT_S 195 SDA

+3VS
SMBus address A2h
GND
R1.1_N033

7,16 M_ODT2 114 ODT0
7,16 M_ODT3 119 ODT1

For Data Swap

M_B_DM7 10 DM0
M_B_DM6 26 DM1
M_B_DM5 52 DM2
M_B_DM4 67 DM3
M_B_DM3 130 DM4
M_B_DM2 147 DM5
M_B_DM1 170 DM6
M_B_DM0 185 DM7

M_B_DQS7 13 DQS0
M_B_DQS6 31 DQS1
M_B_DQS5 51 DQS2
M_B_DQS4 70 DQS3
M_B_DQS3 131 DQS4
M_B_DQS2 148 DQS5
M_B_DQS1 169 DQS6
M_B_DQS0 188 DQS7
M_B_DQS#7 11 DQS#0
M_B_DQS#6 29 DQS#1
M_B_DQS#5 49 DQS#2
M_B_DQS#4 68 DQS#3
M_B_DQS#3 129 DQS#4
M_B_DQS#2 146 DQS#5
M_B_DQS#1 167 DQS#6
M_B_DQS#0 186 DQS#7

DQ0 5 M_B_DQ58
DQ1 7 M_B_DQ63
DQ2 17 M_B_DQ56
DQ3 19 M_B_DQ60
DQ4 4 M_B_DQ62
DQ5 6 M_B_DQ61
DQ6 14 M_B_DQ57
DQ7 16 M_B_DQ59
DQ8 23 M_B_DQ50
DQ9 25 M_B_DQ55
DQ10 35 M_B_DQ49
DQ11 37 M_B_DQ53
DQ12 20 M_B_DQ51
DQ13 22 M_B_DQ54
DQ14 36 M_B_DQ52
DQ15 38 M_B_DQ48
DQ16 43 M_B_DQ43
DQ17 45 M_B_DQ41
DQ18 55 M_B_DQ40
DQ19 57 M_B_DQ46
DQ20 44 M_B_DQ42
DQ21 46 M_B_DQ47
DQ22 56 M_B_DQ45
DQ23 58 M_B_DQ44
DQ24 61 M_B_DQ34
DQ25 63 M_B_DQ38
DQ26 73 M_B_DQ32
DQ27 75 M_B_DQ36
DQ28 62 M_B_DQ35
DQ29 64 M_B_DQ39
DQ30 74 M_B_DQ37
DQ31 76 M_B_DQ33
DQ32 123 M_B_DQ27
DQ33 125 M_B_DQ30
DQ34 135 M_B_DQ28
DQ35 137 M_B_DQ29
DQ36 124 M_B_DQ31
DQ37 126 M_B_DQ26
DQ38 134 M_B_DQ25
DQ39 136 M_B_DQ24
DQ40 141 M_B_DQ18
DQ41 143 M_B_DQ19
DQ42 151 M_B_DQ20
DQ43 153 M_B_DQ16
DQ44 140 M_B_DQ22
DQ45 142 M_B_DQ23
DQ46 152 M_B_DQ21
DQ47 154 M_B_DQ17
DQ48 157 M_B_DQ9
DQ49 159 M_B_DQ15
DQ50 173 M_B_DQ10
DQ51 175 M_B_DQ8
DQ52 158 M_B_DQ14
DQ53 160 M_B_DQ11
DQ54 174 M_B_DQ13
DQ55 176 M_B_DQ12
DQ56 179 M_B_DQ6
DQ57 181 M_B_DQ7
DQ58 189 M_B_DQ4
DQ59 191 M_B_DQ1
DQ60 180 M_B_DQ2
DQ61 182 M_B_DQ3
DQ62 192 M_B_DQ5
DQ63 194 M_B_DQ0

Group7 Group6 Group5 Group4 Group3 Group2 Group1 Group0

DDR_DIMM_200P_A

12G025122007

8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

VREF -> 10/10 mils
M_VREF_DIMM1

U5B

+1.8V

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199

VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163
VREF 1
GND0 201
GND1 202
NP_NC1 203
NP_NC2 204
VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8

+3VS
C143 2.2UF/6.3V
C144 0.1UF/10V
C145 2.2UF/6.3V
C146 0.1UF/10V
GND

DDR_DIMM_200P_A

12G025122007

Layout Note: Place these Caps near SO DIMM 1

Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V
C151 0.1UF/10V
C152 0.1UF/10V
C153 0.1UF/10V
C154 0.1UF/10V
GND

Layout Note: Place these resistors near the GMCH

Layout Note: Place these Caps near SO DIMM 1

+1.8V
C149 0.1UF/10V
C150 0.1UF/10V
C147 0.1UF/10V
C148 0.1UF/10V
GND

+1.8V
C155 2.2UF/6.3V
C156 2.2UF/6.3V
C157 2.2UF/6.3V
C158 2.2UF/6.3V
C159 2.2UF/6.3V
GND

ASUSTeK COMPUTER INC

Title : DDR2_SO-DIMM(1)

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 14 of 69

8,16 M_A_A[0..13]

8 M_A_DM[0..7]

8 M_A_DQS[0..7]

8 M_A_DQS#[0..7]

M_A_DQ[0..63] 8

+1.8V +1.8V 7,10,14,16,36,53

+3VS +3VS 4,5,7,9,11,12,13,14,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61

M_VREF_DIMM0 M_VREF_DIMM0 7,14,16

NO STUFF *

M_CLK_DDR0

PLACE NEAR SO-DIMM_1

M_CLK_DDR#0

M_CLK_DDR1

PLACE NEAR SO-DIMM_1

M_CLK_DDR#1

U8A

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
86 A14
84 A15
8,16 M_A_BS#2 85 A16_BA2

8,16 M_A_BS#0 107 BA0
8,16 M_A_BS#1 106 BA1
7,16 M_CS#0 110 S0#
7,16 M_CS#1 115 S1#
7 M_CLK_DDR1 30 CK0
7 M_CLK_DDR#1 32 CK0#
7 M_CLK_DDR0 164 CK1
7 M_CLK_DDR#0 166 CK1#
7,16 M_CKE0 79 CKE0
7,16 M_CKE1 80 CKE1
8,16 M_A_CAS# 113 CAS#
8,16 M_A_RAS# 108 RAS#
8,16 M_A_WE# 109 WE#
198 SA0
200 SA1
5,14,19,24,26 SMB_CLK_S 197 SCL
5,14,19,24,26 SMB_DAT_S 195 SDA

R1.1_N033
7,16 M_ODT0 114 ODT0
7,16 M_ODT1 119 ODT1

SMBus address A0h

GND GND

For Data Swap

M_A_DM7 10 DM0
M_A_DM6 26 DM1
M_A_DM5 52 DM2
M_A_DM4 67 DM3
M_A_DM3 130 DM4
M_A_DM2 147 DM5
M_A_DM1 170 DM6
M_A_DM0 185 DM7

M_A_DQS7 13 DQS0
M_A_DQS6 31 DQS1
M_A_DQS5 51 DQS2
M_A_DQS4 70 DQS3
M_A_DQS3 131 DQS4
M_A_DQS2 148 DQS5
M_A_DQS1 169 DQS6
M_A_DQS0 188 DQS7
M_A_DQS#7 11 DQS#0
M_A_DQS#6 29 DQS#1
M_A_DQS#5 49 DQS#2
M_A_DQS#4 68 DQS#3
M_A_DQS#3 129 DQS#4
M_A_DQS#2 146 DQS#5
M_A_DQS#1 167 DQS#6
M_A_DQS#0 186 DQS#7

M_A_DQ63 5 DQ0
M_A_DQ59 7 DQ1
M_A_DQ57 17 DQ2
M_A_DQ60 19 DQ3
M_A_DQ58 4 DQ4
M_A_DQ62 6 DQ5
M_A_DQ61 14 DQ6
M_A_DQ56 16 DQ7
M_A_DQ55 23 DQ8
M_A_DQ51 25 DQ9
M_A_DQ52 35 DQ10
M_A_DQ53 37 DQ11
M_A_DQ54 20 DQ12
M_A_DQ50 22 DQ13
M_A_DQ49 36 DQ14
M_A_DQ48 38 DQ15
M_A_DQ43 43 DQ16
M_A_DQ41 45 DQ17
M_A_DQ42 55 DQ18
M_A_DQ40 57 DQ19
M_A_DQ46 44 DQ20
M_A_DQ47 46 DQ21
M_A_DQ44 56 DQ22
M_A_DQ45 58 DQ23
M_A_DQ32 61 DQ24
M_A_DQ35 63 DQ25
M_A_DQ36 73 DQ26
M_A_DQ37 75 DQ27
M_A_DQ39 62 DQ28
M_A_DQ38 64 DQ29
M_A_DQ33 74 DQ30
M_A_DQ34 76 DQ31
M_A_DQ31 123 DQ32
M_A_DQ26 125 DQ33
M_A_DQ24 135 DQ34
M_A_DQ25 137 DQ35
M_A_DQ27 124 DQ36
M_A_DQ30 126 DQ37
M_A_DQ29 134 DQ38
M_A_DQ28 136 DQ39
M_A_DQ22 141 DQ40
M_A_DQ19 143 DQ41
M_A_DQ21 151 DQ42
M_A_DQ20 153 DQ43
M_A_DQ18 140 DQ44
M_A_DQ23 142 DQ45
M_A_DQ16 152 DQ46
M_A_DQ17 154 DQ47
M_A_DQ11 157 DQ48
M_A_DQ9 159 DQ49
M_A_DQ14 173 DQ50
M_A_DQ8 175 DQ51
M_A_DQ10 158 DQ52
M_A_DQ15 160 DQ53
M_A_DQ12 174 DQ54
M_A_DQ13 176 DQ55
M_A_DQ2 179 DQ56
M_A_DQ3 181 DQ57
M_A_DQ5 189 DQ58
M_A_DQ1 191 DQ59
M_A_DQ7 180 DQ60
M_A_DQ6 182 DQ61
M_A_DQ4 192 DQ62
M_A_DQ0 194 DQ63

Group7 Group6 Group5 Group4 Group3 Group2 Group1 Group0

DDR_DIMM_200P

12G025C22000

GMCH=====>SODIMM1=>SODIMM0

+1.8V

U8B

VDD1 112
VDD2 111
VDD3 117
VDD4 96
VDD5 95
VDD6 118
VDD7 81
VDD8 82
VDD9 87
VDD10 103
VDD11 88
VDD12 104
VDDSPD 199

NC1 83
NC2 120
NC3 50
NC4 69
NCTEST 163

VREF 1

GND0 201
GND1 202

NP_NC1 203
NP_NC2 204

VSS1 47
VSS2 133
VSS3 183
VSS4 77
VSS5 12
VSS6 48
VSS7 184
VSS8 78
VSS9 71
VSS10 72
VSS11 121
VSS12 122
VSS13 196
VSS14 193
VSS15 8

VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR_DIMM_200P

+3VS

C209 2.2UF/6.3V
C210 0.1UF/10V

VREF -> 10/10 mils
M_VREF_DIMM0

C211 2.2UF/6.3V
C212 0.1UF/10V

GND GND GND GND GND GND

12G025C22000

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C213 0.1UF/10V
C214 0.1UF/10V
C215 0.1UF/10V
C216 0.1UF/10V

GND GND GND GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C217 2.2UF/6.3V
C218 2.2UF/6.3V
C219 2.2UF/6.3V
C220 2.2UF/6.3V
C221 2.2UF/6.3V

GND GND GND GND GND

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM(0)

Engineer: Vincent VY Huang

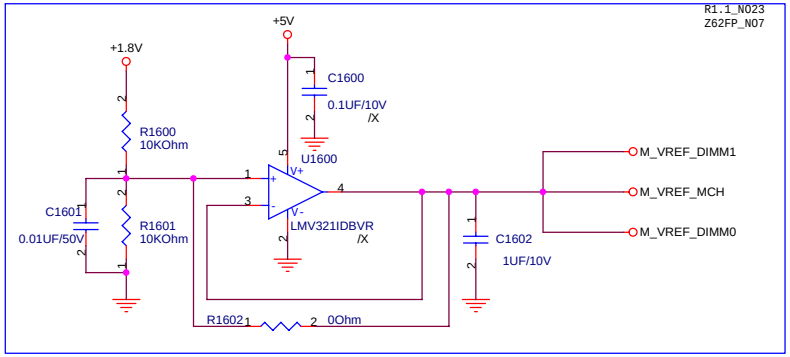
Size	Project Name	Rev
Custom	Z62Fp	1.0

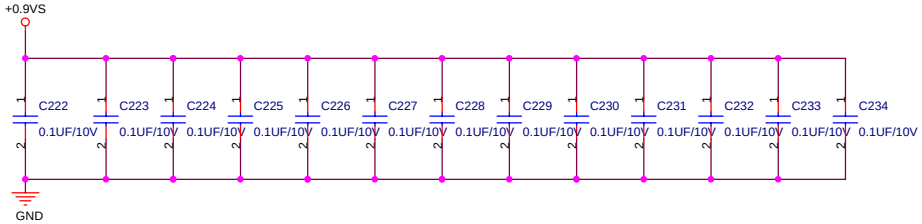
Date: Wednesday, August 23, 2006 Sheet 15 of 69

M_VREF_DIMM0
M_VREF_DIMM1
M_VREF_MCH
+0.9VS

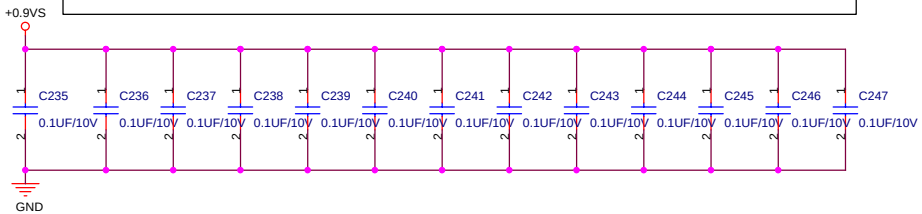
M_VREF_DIMM0 7,14,15
M_VREF_DIMM1 7,14,15
M_VREF_MCH 7,14,15
+0.9VS 36,53

R1.1_N023
Z62FP_N07





Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



M_A_A[0..13] 8,15
M_A_BS#[0..2] 8,15
M_A_CAS# 8,15
M_A_RAS# 8,15
M_A_WE# 8,15

M_B_A[0..13] 8,14
M_B_BS#[0..2] 8,14
M_B_CAS# 8,14
M_B_RAS# 8,14
M_B_WE# 8,14

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

+0.9VS

NEED TO SWAP

1	56Ohm	16	RN7A	M_B_A10
2	56Ohm	15	RN7B	M_B_A3
3	56Ohm	14	RN7C	M_B_A8
4	56Ohm	13	RN7D	M_B_A12
5	56Ohm	12	RN7E	M_B_BS#2
6	56Ohm	11	RN7F	M_B_A0
7	56Ohm	10	RN7G	M_CKE2
8	56Ohm	9	RN7H	M_CKE3

1	56Ohm	16	RN8A	M_B_BS#1
2	56Ohm	15	RN8B	M_B_A1
3	56Ohm	14	RN8C	M_B_A0
4	56Ohm	13	RN8D	M_B_A2
5	56Ohm	12	RN8E	M_B_A4
6	56Ohm	11	RN8F	M_B_A6
7	56Ohm	10	RN8G	M_B_A7
8	56Ohm	9	RN8H	M_B_A11

1	56Ohm	16	RN9A	M_B_CAS#
2	56Ohm	15	RN9B	M_B_WE#
3	56Ohm	14	RN9C	M_B_A5
4	56Ohm	13	RN9D	M_B_BS#0
5	56Ohm	12	RN9E	M_B_A13
6	56Ohm	11	RN9F	M_ODT2
7	56Ohm	10	RN9G	M_CS#2
8	56Ohm	9	RN9H	M_B_RAS#

1	56Ohm	2	RN14A	
3	56Ohm	4	RN14B	
5	56Ohm	6	RN14C	M_ODT3
7	56Ohm	8	RN14D	M_CS#3

1	56Ohm	16	RN10A	M_CKE0
2	56Ohm	15	RN10B	
3	56Ohm	14	RN10C	
4	56Ohm	13	RN10D	M_A_BS#2
5	56Ohm	12	RN10E	M_A_A12
6	56Ohm	11	RN10F	M_A_A9
7	56Ohm	10	RN10G	M_A_A8
8	56Ohm	9	RN10H	M_A_A5

1	56Ohm	16	RN11A	M_A_A3
2	56Ohm	15	RN11B	M_A_A1
3	56Ohm	14	RN11C	M_A_A2
4	56Ohm	13	RN11D	M_A_A0
5	56Ohm	12	RN11E	M_A_A6
6	56Ohm	11	RN11F	M_A_A7
7	56Ohm	10	RN11G	M_A_A4
8	56Ohm	9	RN11H	M_A_A11

1	56Ohm	16	RN12A	M_A_RAS#
2	56Ohm	15	RN12B	M_A_BS#1
3	56Ohm	14	RN12C	M_A_A13
4	56Ohm	13	RN12D	M_A_A10
5	56Ohm	12	RN12E	M_A_BS#0
6	56Ohm	11	RN12F	M_A_WE#
7	56Ohm	10	RN12G	M_A_CAS#
8	56Ohm	9	RN12H	M_CS#1

1	56Ohm	2	RN13A	M_ODT1
3	56Ohm	4	RN13B	M_CKE1
5	56Ohm	6	RN13C	M_CS#0
7	56Ohm	8	RN13D	M_ODT0

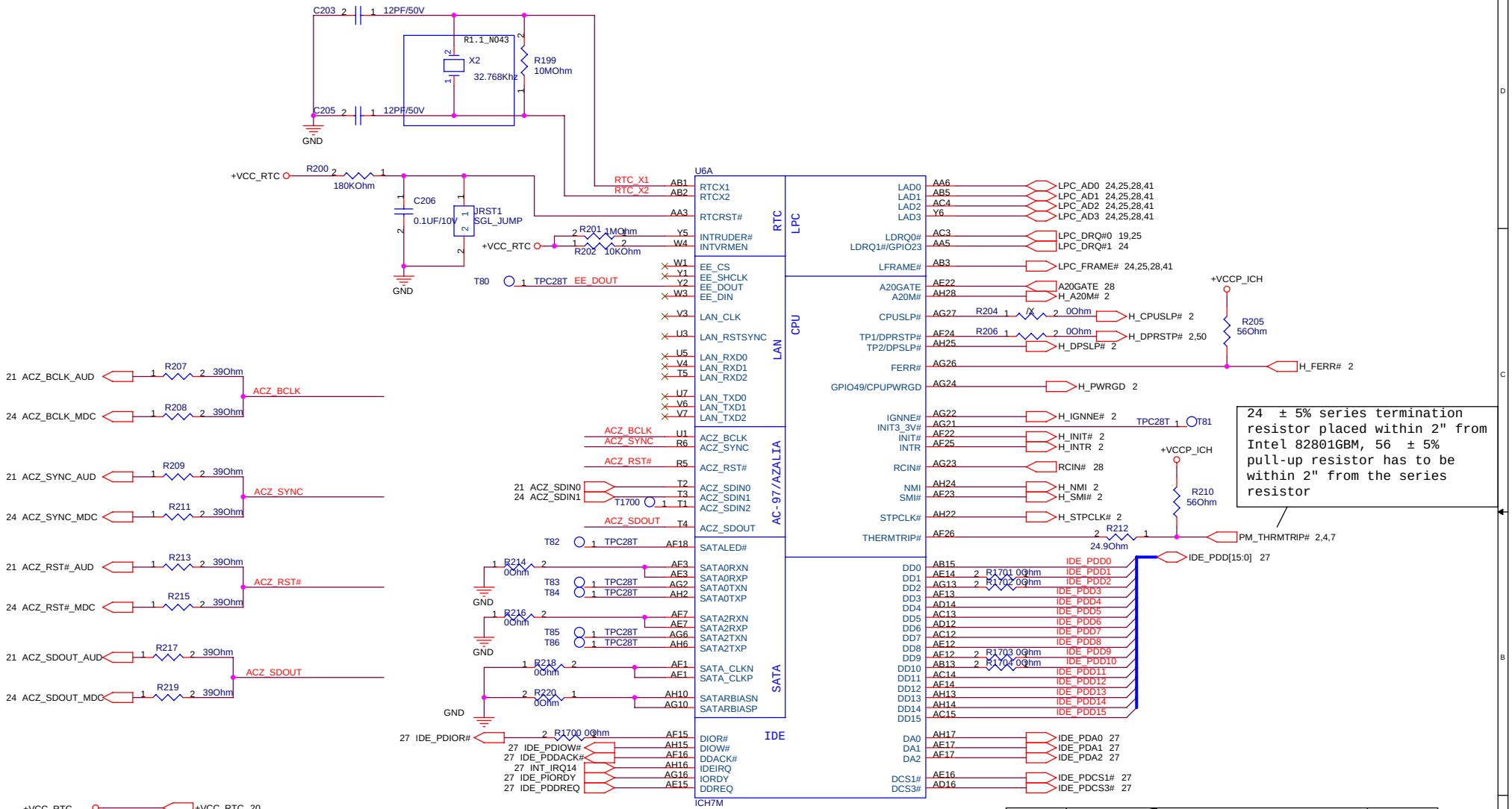
ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 16 of 69



24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor

+VCC_RTC +VCC_RTC 20
+VCCP_ICH +VCCP_ICH 2,3,5,6,9,20,52
+1.5VS_PCIE_ICH +1.5VS_PCIE_ICH 18,20
+3VA +3VA 4,12,20,22,24,25,28,29,39,54,59,63
+3VS +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,24,25,26,27,28,30,36,39,50,52,60,61
+5VS +5VS 4,13,19,20,21,22,27,36,37,38,50,61
+1.5VS +1.5VS 3,9,10,20,26,36,52
+VCCP +VCCP 2,3,5,6,9,20,52

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUSTeK COMPUTER INC

Title : ICH7-M (1/4)

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 17 of 69

DEVICE	IDSEL	REQ/GNT	INT
LAN	AD23	REQ2#/GNT2#	INT A#
CARDBUS	AD17	REQ1#/GNT1#	INT B#, INT C#, INT D#

Internal					
SM Bus	INTB#	EIP	INTA#	PCIE6	INTB#
SATA	INTB#	U3P	INTD#	PCIE5	INTA#
PATA	INTA#	U2P	INTC#	PCIE4	INTD#
AC97 Modem	INTB#	U1P	INTB#	PCIE3	INTC#
		U0P	INTA#	PCIE2	INTB#
AC97 Audio	INTA#	HD Audio	INTA#	PCIE1	INTA#

		GNT#5	GNT#4
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

Do not connect to reset on PCI slots or PCI down devices.

Pull-ups must be placed within 500 mils from Intel 82801GBM pins

ASUSTeK COMPUTER INC		Title : ICH7-M (2/4)	
		Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006		Sheet 18 of 69	

GPIO:
[0,6,7,16:23,32:39,48] - 3.3V core,
[1:5] - 5V core,
[8:15,24:31] - 3.3V resume,
[40:47] - N/A
[49] - V_CPU_IO

0 needs to check power plane again

For PCI compliance, SMBus signals should be routed to either all or none of the PCI slots in a chassis.
These signals should not be connected to SMLINK

U6C

SMB_CLK C22 SMBCLK
SMB_DAT B22 SMBDATA
LINKALERT# A26 LINKALERT#
SM_LINK0 B25 SMLINK0
SM_LINK1 A25 SMLINK1
SMB

RING# A28 RI#

SPKR A19 SPKR
SUS_STAT# A27 SUS_STAT#
A22 SYS_RST#

7 PM_BMBUSY# AB18 GPIO0/BM_BUSY#

3VSUS B23 SMBALERT#/GPIO11

5 STP_PCI# AC20 GPIO18/STPPCI#
5,50 STP_CPU# AF21 GPIO20/STPCPU#

PCB_ID2 A21 GPIO26

37 BT_LED_EN# B21 GPIO27
E23 GPIO28

24,30,33 PM_CLKRUN# AG18 GPIO32/CLKRUN#

26 BT_ON AC19 GPIO33/AZ_DOCK_EN#
26 WLAN_ON# U2 GPIO34/AZ_DOCK_RST#

26 SB_WAKE# F20 WAKE#
24,25,28,30 INT_SERIRQ AH21 SERIRQ
28 PM_THERM# AE20 THRM#

39 IMVPOK R160 0Ohm VRMPWRGD AD22 VRMPWRGD

T46 TPC28T AC21 GPIO6
RF_OFF_SW# AC18 GPIO7
E21 GPIO8
GPIO

28 EXTSMI#

ICH7M

GPIO21/SATA0GP AE19 2 R154 100Ohm GND TPC28T T41
GPIO19/SATA1GP AH18
GPIO36/SATA2GP AH19 2 R155 100Ohm GND
GPIO37/SATA3GP AE19 TPC28T T38
SATA GPIO

CLK14 AC1 CLK_ICH14 5
CLK48 B2 CLK_USB48 5
SUSCLK C20 TPC28T 1 T39
Clocks

C193 10PF/50V /X
GND

SLP_S3# B24 PM_SUSB# 28
SLP_S4# D23 PM_SUSC# 28
SLP_S5# F22 TPC28T T40
R2.0_NO10

PWROK AA4 ICH7_PWROK 7,28

GPIO16/DPRSLPVR AC22 PM_DPRSLPVR 50

TP0/BATLOW# C21 PM_BATLOW#

PWRBTN# C23 PM_PWRBTN# 28

R158 10KOhm
GND

LAN_RST# C19 PLT_RST# 7,18,27,28

RSMRST# Y4 PM_RSMRST# 28

R159 10KOhm
GND

SYS GPIO
Power MGT

GPIO9 E20 SATA_DET#0
GPIO10 A20 TPC28T T43
GPIO12 F19 KB_SCI# 28
GPIO13 E19 SIO_SMI# 25
GPIO14 R4 PWRLED_1HZ
GPIO15 F22 TPC28T T44
GPIO24 R3 802_LED_EN# 37
GPIO25 D20 CB_SD# 30
GPIO35 AD21 TPC28T T47
GPIO38 AD20 PCB_ID0
GPIO39 AE20 PCB_ID1

checklist suggests +3V
R2.0_NO3
21 SPKR_SB
+3V R156 1 2 10KOhm
3VSUS R157 1 2 10KOhm

If ICH7M embedded Lan controller was used, "LAN_RST#" should be connected to "RSMRST#"

+3VS

18,30,33 PCI_FRAME# PCI_FRAME# RP1A 1 8.2KOHM 5 10
18,30,33 PCI_IRDY# PCI_IRDY# RP1B 2 8.2KOHM 5 10
18,30,33 PCI_TRDY# PCI_TRDY# RP1C 3 8.2KOHM 5 10
18,30,33 PCI_STOP# PCI_STOP# RP1D 4 8.2KOHM 5 10
18,30,33 PCI_SERR# PCI_SERR# RP1E 6 8.2KOHM 5 10
18,30,33 PCI_DEVSEL# PCI_DEVSEL# RP1F 7 8.2KOHM 5 10
18,30,33 PCI_PERR# PCI_PERR# RP1G 8 8.2KOHM 5 10
18 PCI_LOCK# PCI_LOCK# RP1H 9 8.2KOHM 5 10

18,33 PCI_INTA# PCI_INTA# RP2A 1 8.2KOHM 5 10
18,30 PCI_INTB# PCI_INTB# RP2B 2 8.2KOHM 5 10
18,30 PCI_INTC# PCI_INTC# RP2C 3 8.2KOHM 5 10
18,30 PCI_INTD# PCI_INTD# RP2D 4 8.2KOHM 5 10
18 PCI_INTE# PCI_INTE# RP2E 6 8.2KOHM 5 10
18 PCI_INTF# PCI_INTF# RP2F 7 8.2KOHM 5 10
18 PCI_INTG# PCI_INTG# RP2G 8 8.2KOHM 5 10
18 PCI_INTH# PCI_INTH# RP2H 9 8.2KOHM 5 10

18 PCI_REQ#0 PCI_REQ#0 RP3A 1 8.2KOHM 5 10
18 PCI_REQ#1 PCI_REQ#1 RP3B 2 8.2KOHM 5 10
18 PCI_REQ#2 PCI_REQ#2 RP3C 3 8.2KOHM 5 10
18 PCI_REQ#3 PCI_REQ#3 RP3D 4 8.2KOHM 5 10
18 PCI_REQ#5 PCI_REQ#5 RP3E 6 8.2KOHM 5 10
18 PCI_REQ#4 PCI_REQ#4 RP3F 7 8.2KOHM 5 10
PM_CLKRUN# RP3G 8 8.2KOHM 5 10
PM_THERM# RP3H 9 8.2KOHM 5 10

INT_SERIRQ R163 2 10KOhm
STP_PCI# R164 2 10KOhm /X
STP_CPU# R167 2 10KOhm /X
17 LPC_DRQ#0 R170 2 8.2KOHm /X
SMB_CLK_S R172 2.2KOhm
SMB_DAT_S R174 2.2KOhm

+5VS
5,14,15,24,26 SMB_CLK_S Q16 2N7002 SMB_CLK
5,14,15,24,26 SMB_DAT_S Q17 2N7002 SMB_DAT

ICH7_PWROK Q15 2N7002 /X VRMPWRGD
R161 10KOhm /X
GND

PM_BATLOW# D16 1N4148W BAT_LL# 28

checklist suggests +3V
+3VSUS
RING# R162 8.2KOhm
RN4A 10KOhm
SM_LINK1 RN4B 10KOhm
LINKALERT# RN4C 10KOhm
SM_LINK0 RN4D 10KOhm
SMB_CLK R166 2.2KOhm
SMB_DAT R169 2.2KOhm
PM_BATLOW# R171 8.2KOhm
SUS_STAT# R173 4.7KOhm /X
18,33 PME# R176 /X 10KOhm

RF_OFF_SW# R165 8.2KOhm
PWRLED_1HZ R168 8.2KOhm

PCB_VID3 : PROJECT CODE

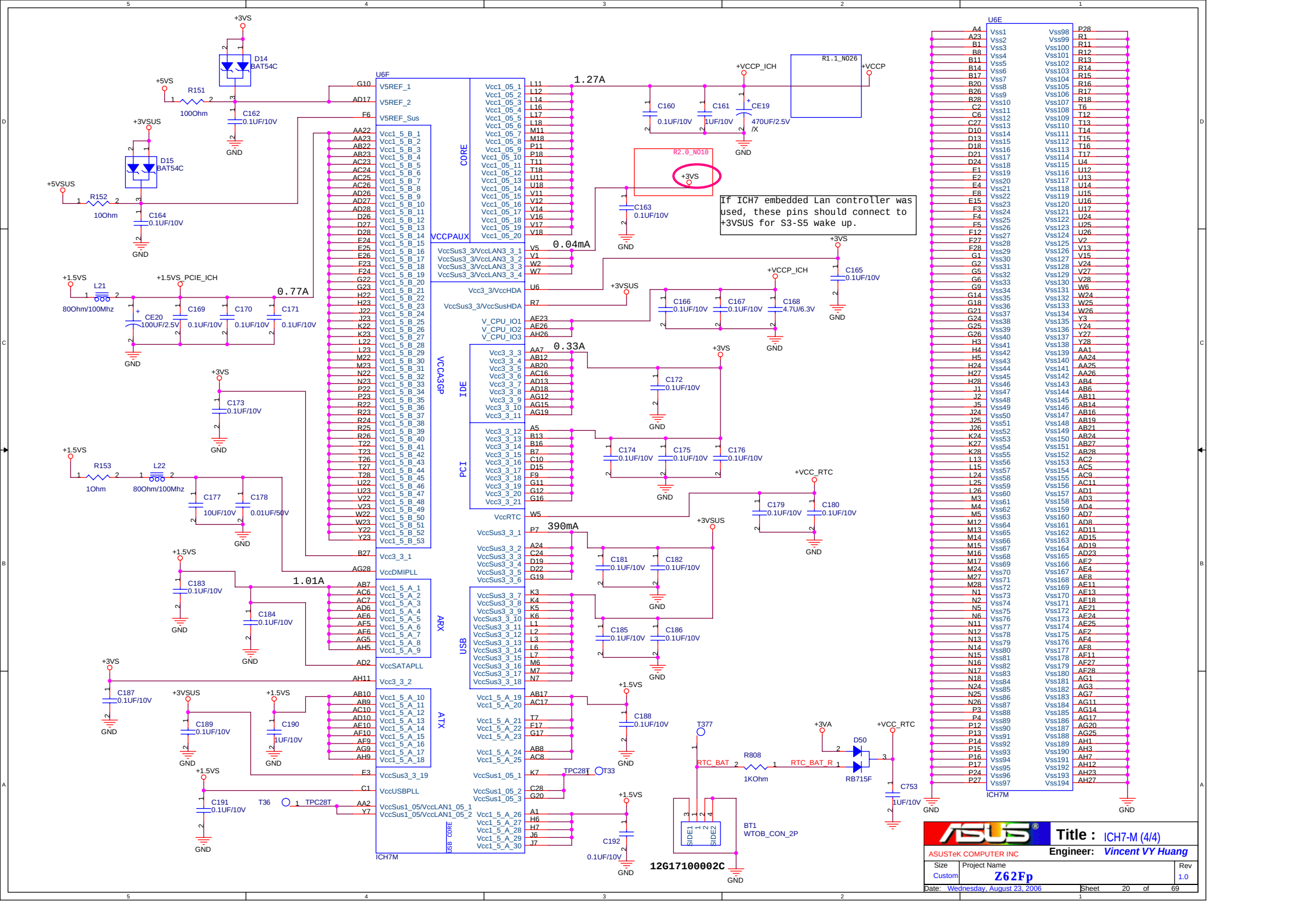
PCB_VID	0	1	2
MB V1.0	0	0	0

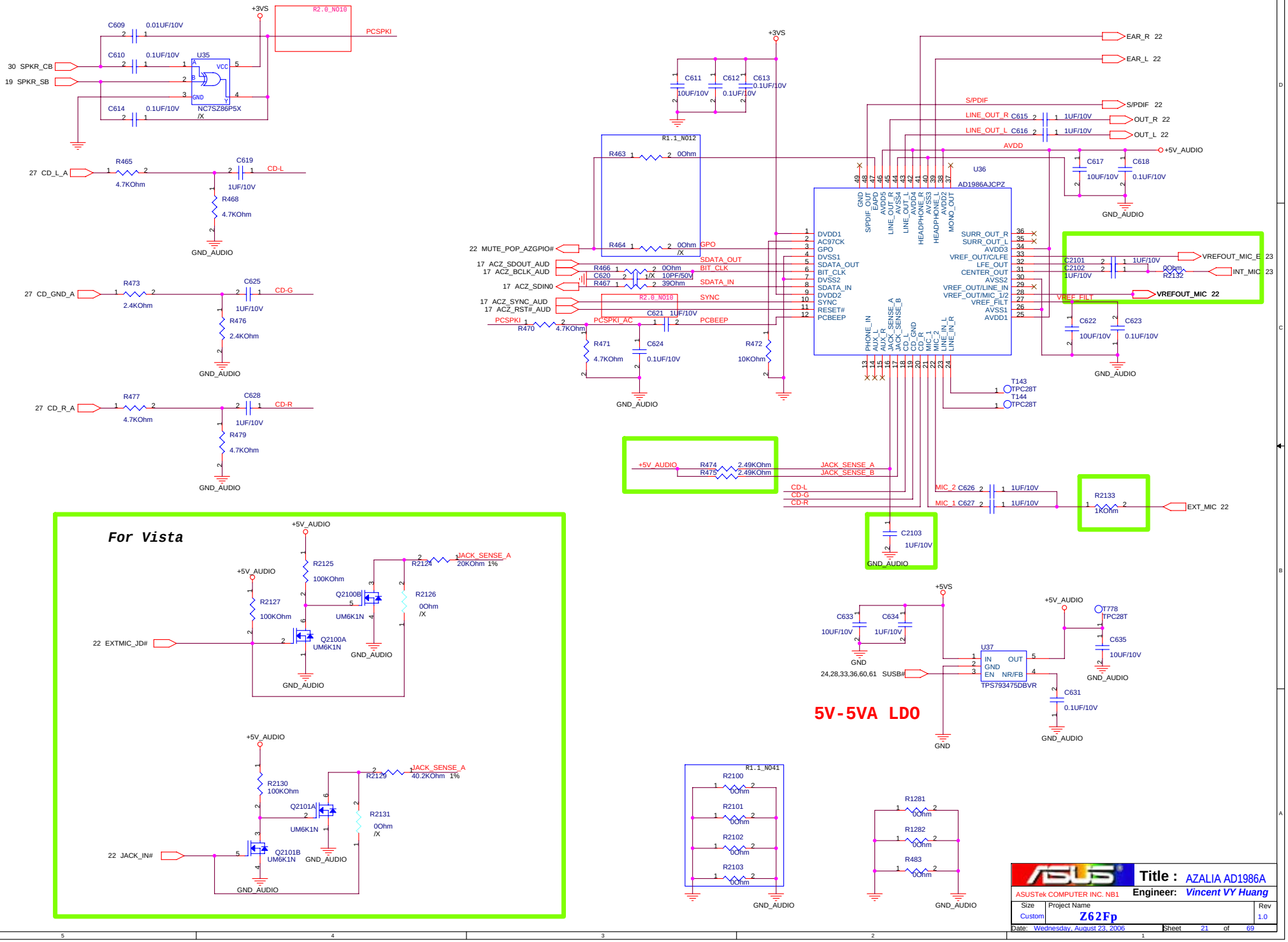
+3VSUS
R182 8.2KOhm /X
R183 8.2KOhm /X
R184 8.2KOhm /X
PCB_ID0
PCB_ID1
PCB_ID2
R190 8.2KOhm
R191 8.2KOhm
R192 8.2KOhm
GND

internal pull up
SATA_DET#0 R175 8.2KOhm
KB_SCI# R177 10KOhm
SIO_SMI# R179 8.2KOhm
802_LED_EN# R180 8.2KOhm
CB_SD# R181 8.2KOhm /X
BT_LED_EN# R185 8.2KOhm
BT_ON R187 8.2KOhm
WLAN_ON# R189 8.2KOhm
GND

internal pull down
PM_DPRSLPVR R186 100KOhm /X
PM_RSMRST# R188 10KOhm
GND

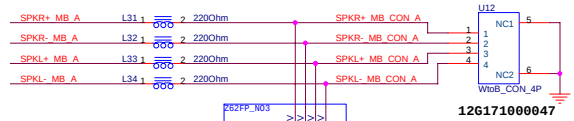
ASUSTeK COMPUTER INC
Title : ICH7-M (3/4)
Engineer: Vincent VY Huang
Size: Custom
Project Name: Z62Fp
Rev: 1.0
Date: Wednesday, August 23, 2006
Sheet 19 of 69


U6F
U6E
ICH7M
D14 BAT54C
D15 BAT54C
R151 100Ohm
R152 10Ohm
R153 1Ohm
L21 80Ohm/100Mhz
L22 80Ohm/100Mhz
R1.1_N026
R2.0_N010
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
1.27A
0.04mA
0.77A
0.33A
1.01A
390mA
12G17100002C
Title : ICH7-M (4/4)
ASUSTeK COMPUTER INC
Engineer: Vincent VY Huang
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 20 of 69



Title : AZALIA AD1986A		
ASUSTek COMPUTER INC. NB1	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 21 of 69	

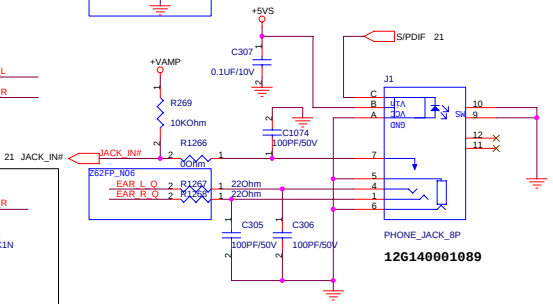
SPEAKER CONN.



12G171000047

SPEAKER is 4 ohm +- 15% / 2W /79 +- 3db (美星電子)
P/N:04-170003610

HEADPHONE JACK

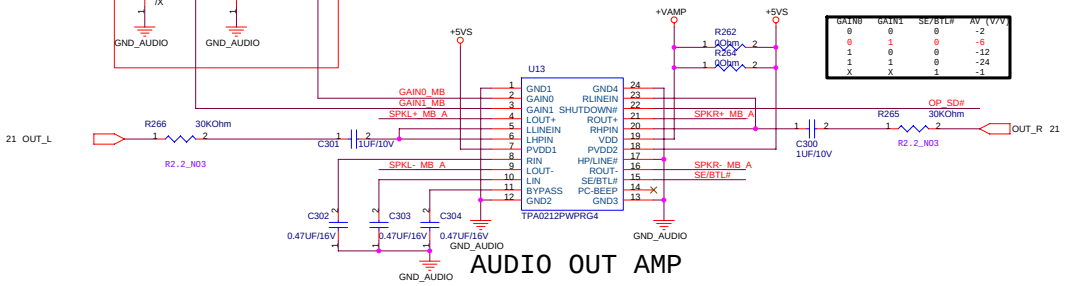


12G140001089

21 EAR_L
21 EAR_R
EAR_L
EAR_R

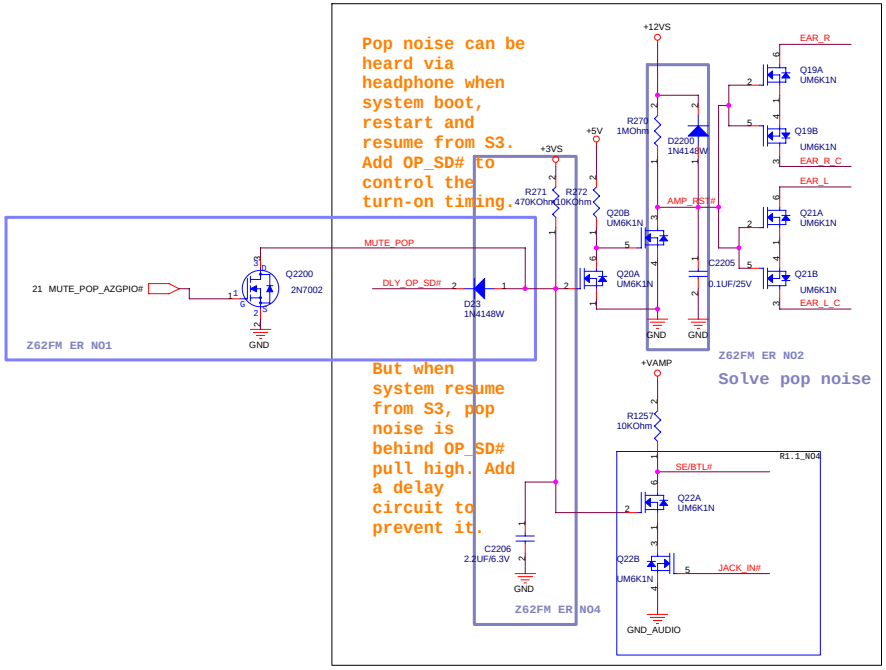
21 JACK_IN#

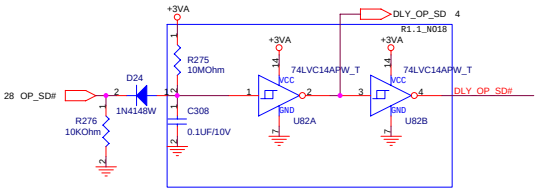
AUDIO OUT AMP



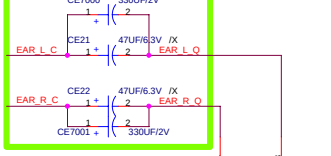
GAIN0	GAIN1	SE/BTL#	AV (V/V)
0	0	0	-2
0	1	0	-6
1	0	0	-12
1	1	0	-24
X	X	1	-1

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.





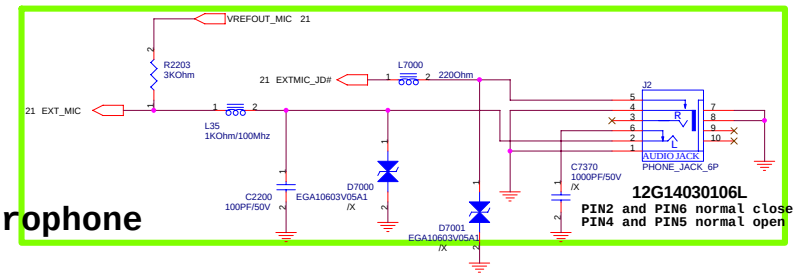
Colay:
330 uF for Vista



$$f(\text{highpass}) = \frac{1}{2*3.14*R*C} = \frac{1}{\text{---------}} = 73$$

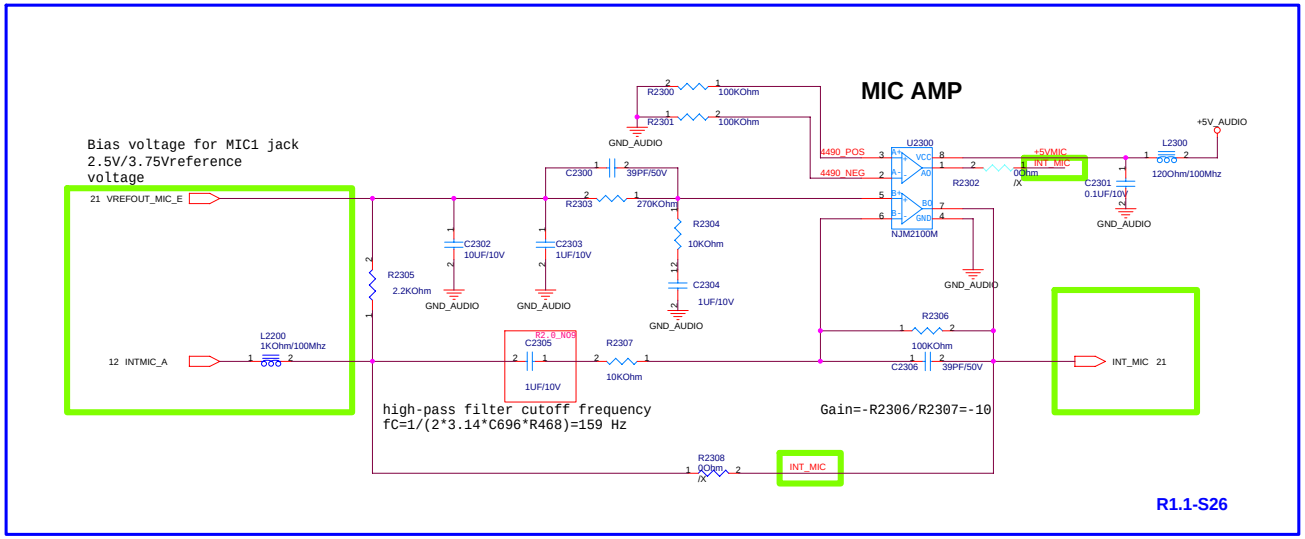
R=32 Ohm for Headphone, so C=68uF But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.

External Microphone

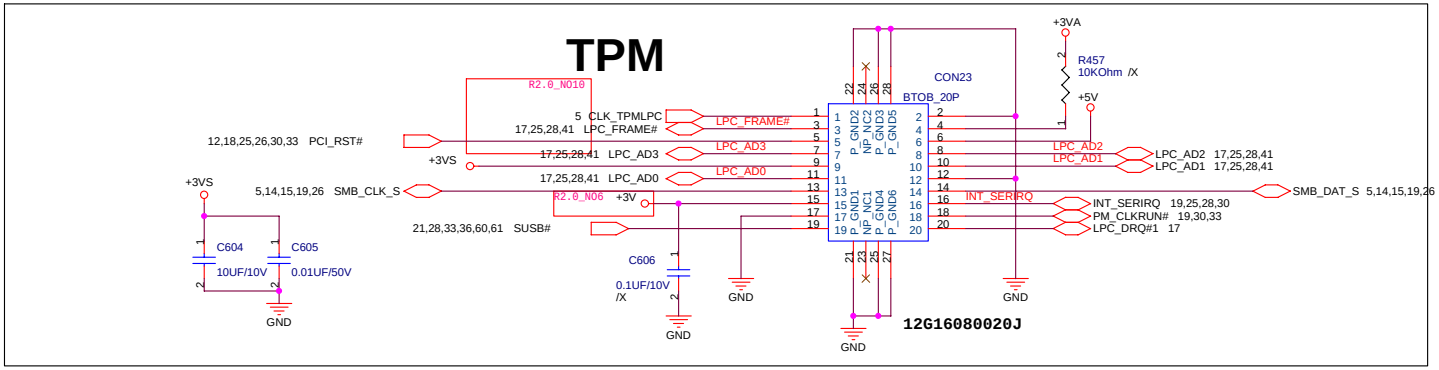


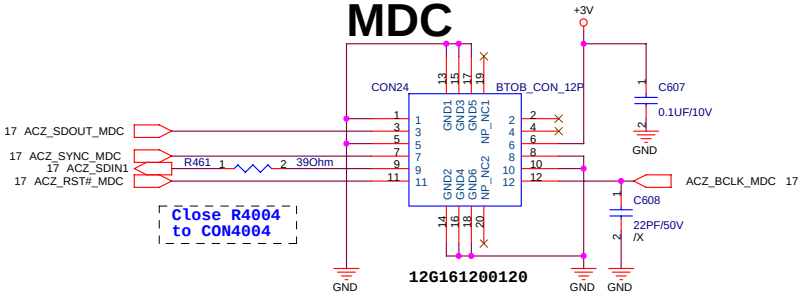
12G14030106L
PIN2 and PIN6 normal close
PIN4 and PIN5 normal open

ASUSTek COMPUTER INC. NB1	Title : AUDIO AMP	
	Engineer: Vincent VY Huang	
Size: C	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 22 of 69	



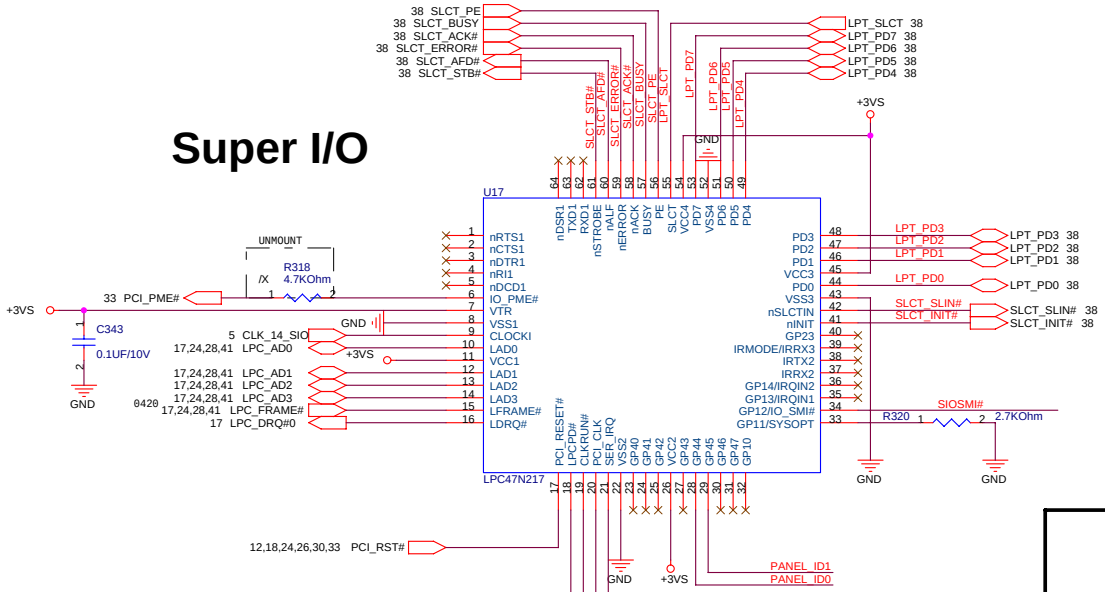
ASUSTek COMPUTER INC. NB1	Title : MIC Pre-AMP		
	Engineer: Vincent VY Huang		
Size: C	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 23 of 69		

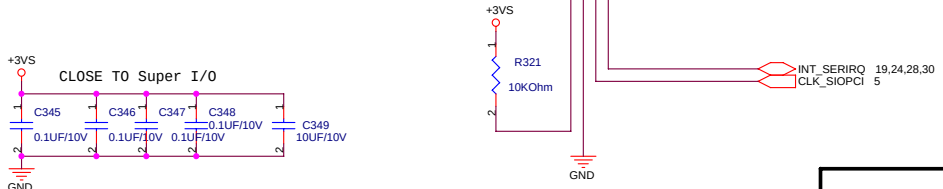


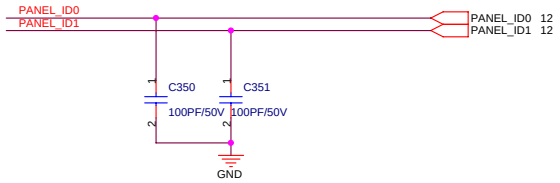


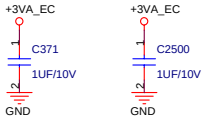
ASUSTeK COMPUTER INC	Title : MODULE-TPM/MDC	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 24 of 69	

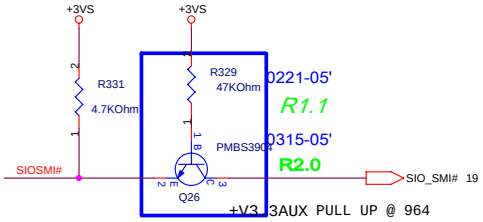
Super I/O







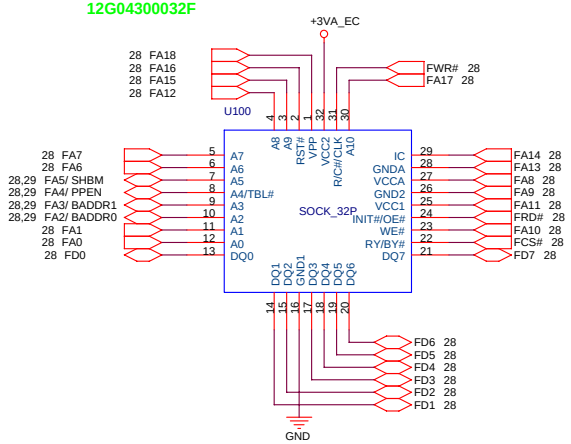




SST-PLCC32 4Mbits Flash ROM
PN:05G001014110(+3.3V)

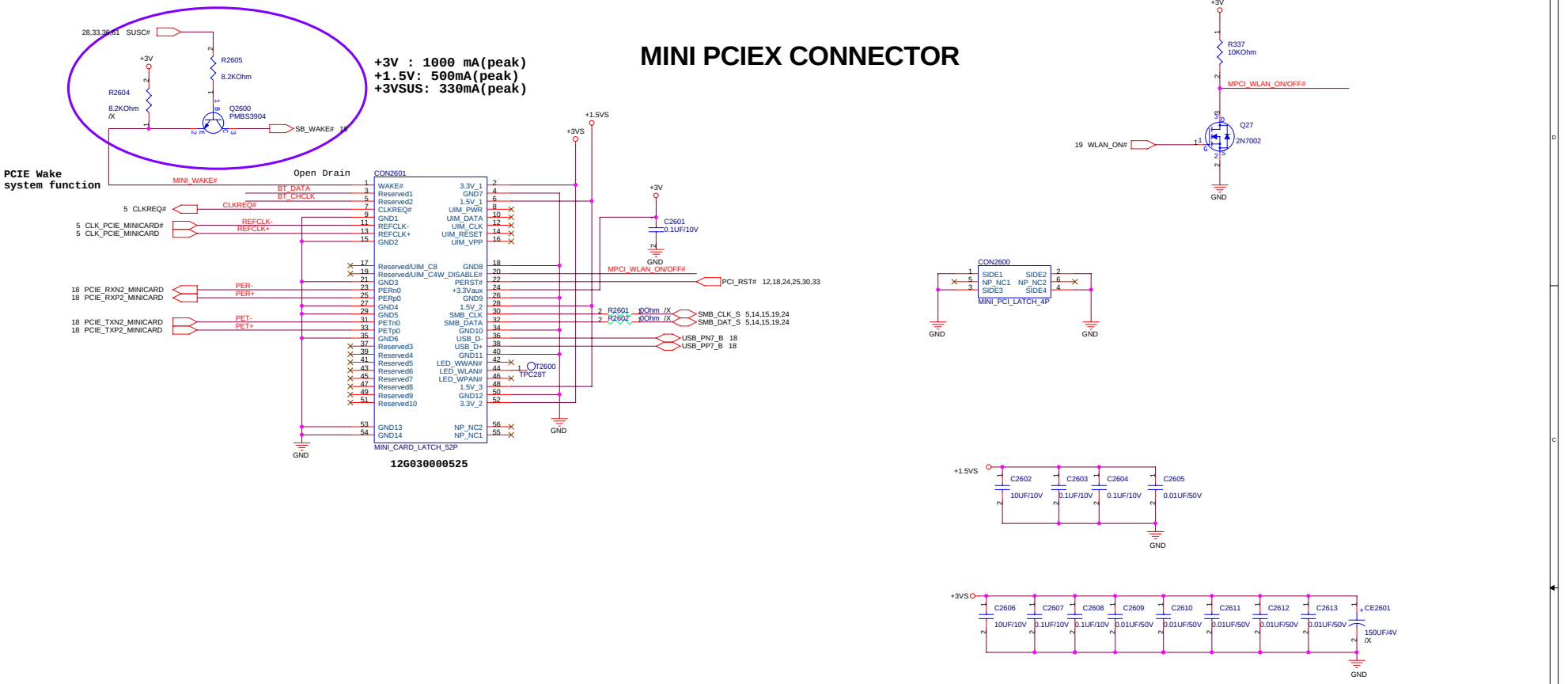
ISA ROM

PLCC32 Socket PN:
12G04300032F

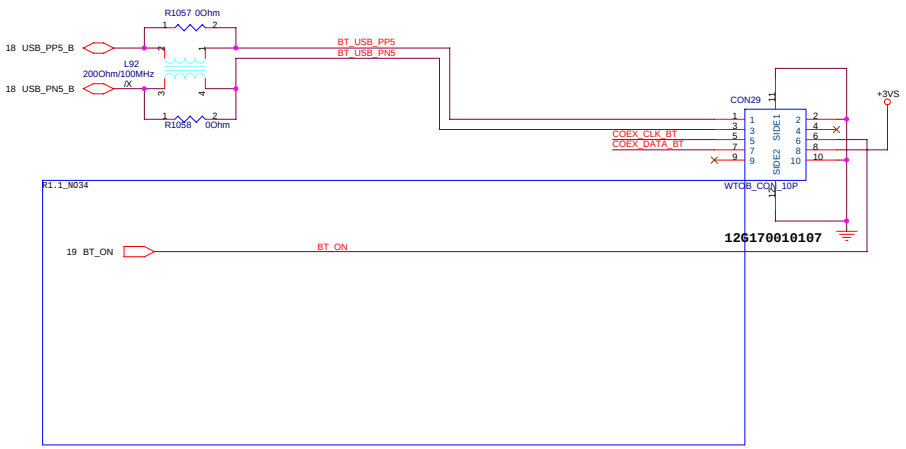


ASUSTeK COMPUTER INC	Title : SUPER I/O & ROM	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 25 of 69	

MINI PCIEX CONNECTOR



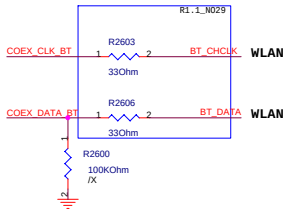
BLUETOOTH CONNECTOR



Check O/D output or push pull

Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

BT_ON 3.3V at GPIO38



BT Module has no leakage, so discard PMOS block circuits

ASUSTeK COMPUTER INC	Title : MINI PCIEX (TV) & BT Conn	
	Engineer: Vincent VY Huang	
Size: C	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 26 of 69	

HDD_CSEL : Pull-Down HDD as Master

R338 1 2 470Ohm HDD_CSEL
GND

+3VS
R339 2 1 4.7KOhm IDE_PIORDY
R340 1 2 8.2KOhm INT_IRQ14

+5VS
R341 1 2 10KOhm IDE_DIAG
R1.1_N035
R342 1 2 10KOhm IDE_PDASP#
/X
R2700 1 2 10KOhm IDE_IOCS16#

17 IDE_PDD[15:0]
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15

+5VS
R343 10KOhm
+5VS
R344 10KOhm
IDE_RST#
Q28B UM6K1N
Q28A UM6K1N
7,18,19,28 PLT_RST#
GND
GND

if use EC ->3V

CON9
IDE_RST#
IDE_PDD7
IDE_PDD8
IDE_PDD6
IDE_PDD9
IDE_PDD5
IDE_PDD10
IDE_PDD4
IDE_PDD11
IDE_PDD3
IDE_PDD12
IDE_PDD2
IDE_PDD13
IDE_PDD1
IDE_PDD14
IDE_PDD0
IDE_PDD15
48
NP_NC2
46
NP_NC1
45
47
HDD_CON_44P

17 IDE_PDDREQ
17 IDE_PDIOW#
17 IDE_PDIOR#
17 IDE_PIORDY
17 IDE_PDDACK#
17 INT_IRQ14
17 IDE_PDA1
17 IDE_PDA0
17 IDE_PDA2
17 IDE_PDCS1#
17 IDE_PDCS3#
37 IDE_PDASP#

IDE_PIORDY
HDD_CSEL
INT_IRQ14
IDE_IOCS16#
IDE_DIAG
IDE_PDASP#

+5VS
CE23 10UF/10V
GND
GND

12G16150044T

For Z62F, HDD placement is reversed, so the pin define swapped.
In normal case, reset pin should be connected to pin1 instead of pin 44

HDD

CD-ROM

+5VS
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master
R345 1 2 470Ohm ODD_CSEL
R346 1 2 470Ohm
/X
GND

+5VS
R2701 1 2 10KOhm IDE_IOCS16_2#

CON10
NP_NC1
51
53
P_GND1
P_cd_rom_50p
NP_NC2
52
54
P_GND2
R2.1_N03

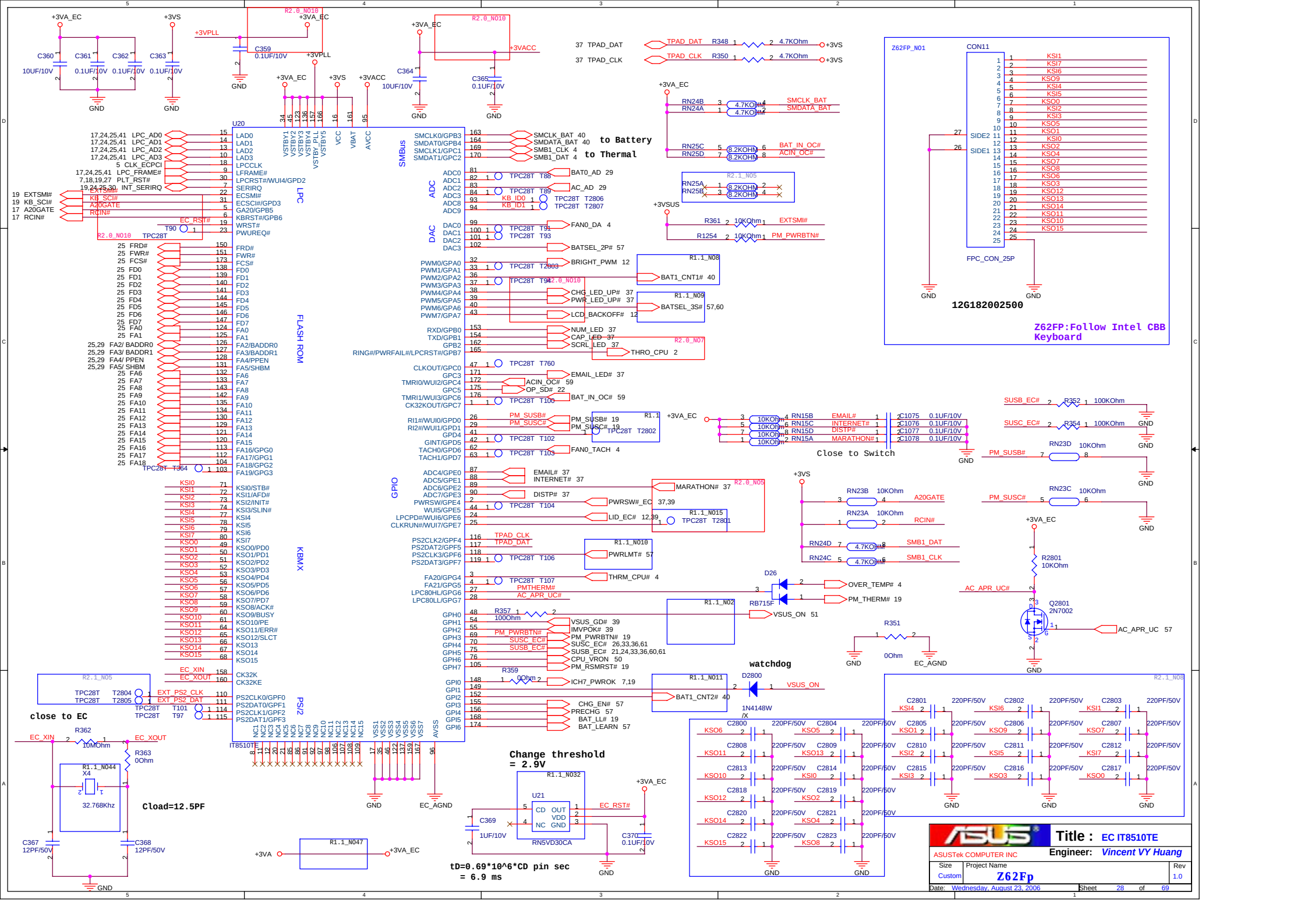
21 CD_L_A
21 CD_GND_A
CD_GND_A
CD_R_A 21

IDE_RST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0
IDE_PDIOW#
IDE_PIORDY
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDASP#
ODD_CSEL
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDREQ
IDE_PDIOR#
IDE_PDDACK#
IDE_IOCS16_2#
IDE_DIAG
IDE_PDA2
IDE_PDCS3#

+5VS
+5VS
CE24 10UF/10V
GND
GND
GND

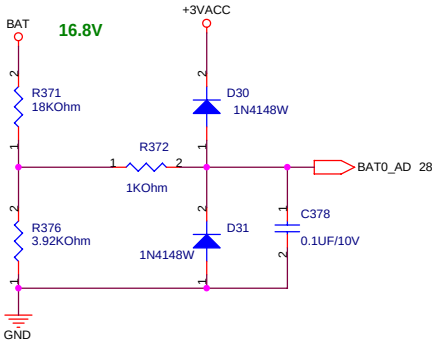
12G161210507

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 27 of 69	

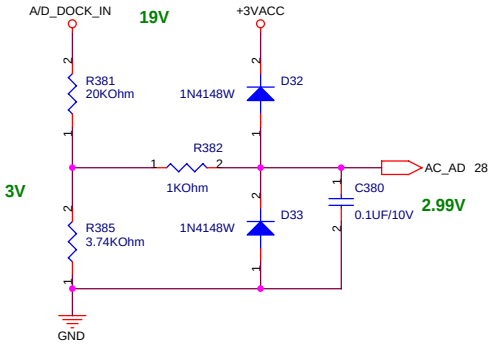

U20
IT8510TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
close to EC
Cload=12.5PF
Change threshold
= 2.9V
tD=0.69*10^6*CD pin sec
= 6.9 ms
watchdog
Close to Switch
Z62FP_N01
CON11
FPC_CON_25P
12G182002500
Z62FP:Follow Intel CBB
Keyboard
Title : EC IT8510TE
ASUSTek COMPUTER INC
Engineer: Vincent VY Huang
Project Name
Z62Fp
Size
Custom
Rev
1.0
Date: Wednesday, August 23, 2006
Sheet 28 of 69

EC ADC

Battery

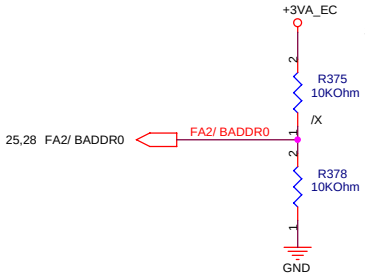


Adaptor

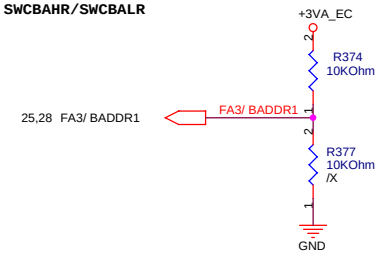


EC Hardware Strap

strap value sampled after
VSTBY power up reset

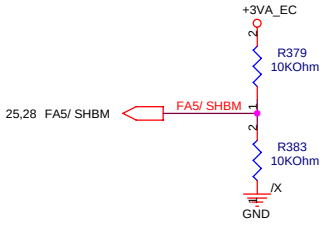


PNPCFG base address set by
SWCBAHR/SWCBALR

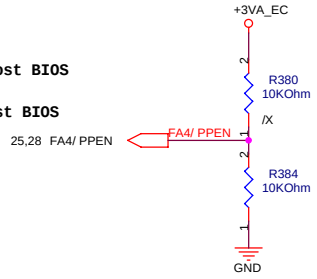


BADDR[1:0]
No pull up:
The register pair to access PNPCFG is
002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is
004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is
determined by EC domain registers
SWCBALR and SWCBAHR.

Share Memory

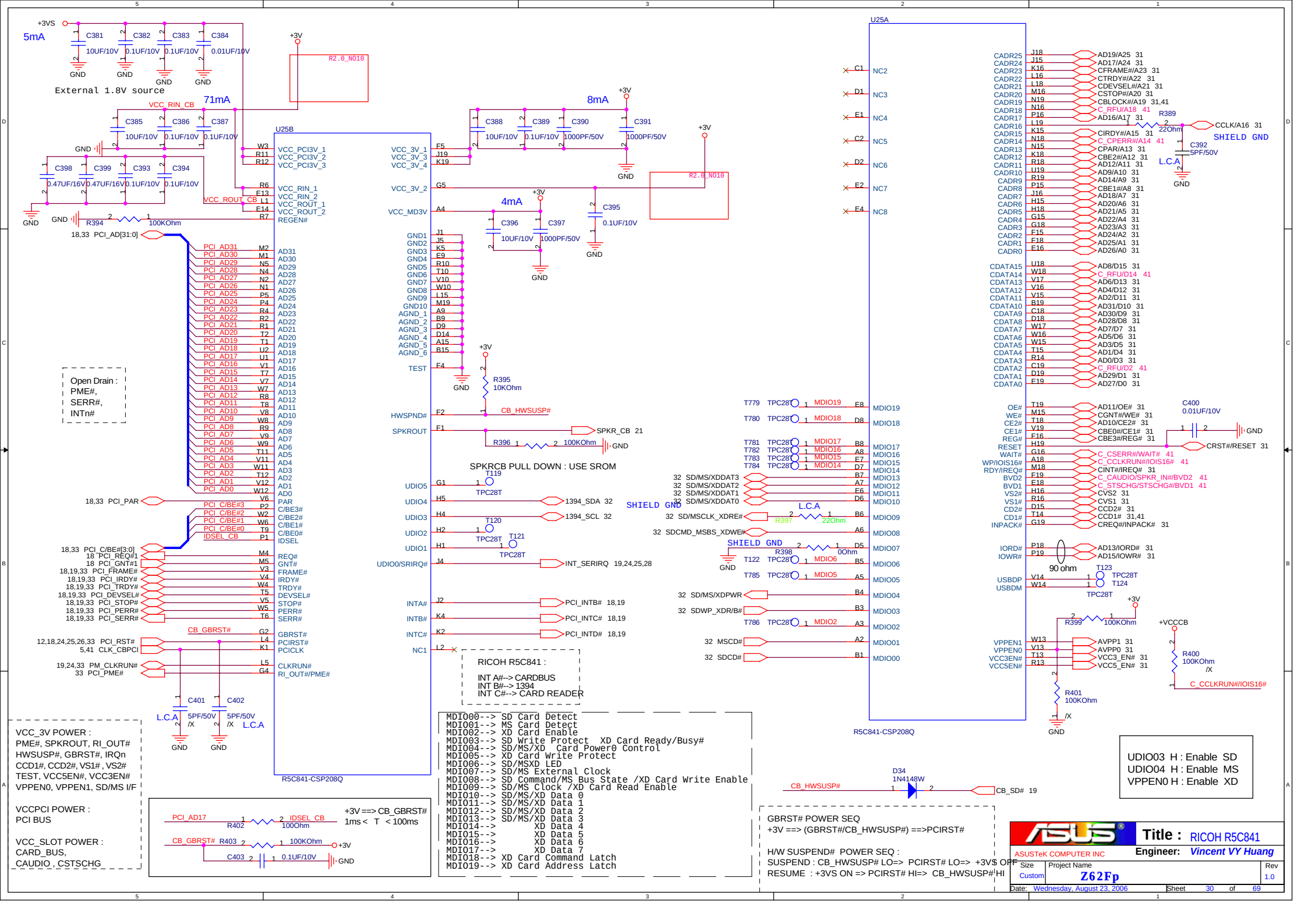


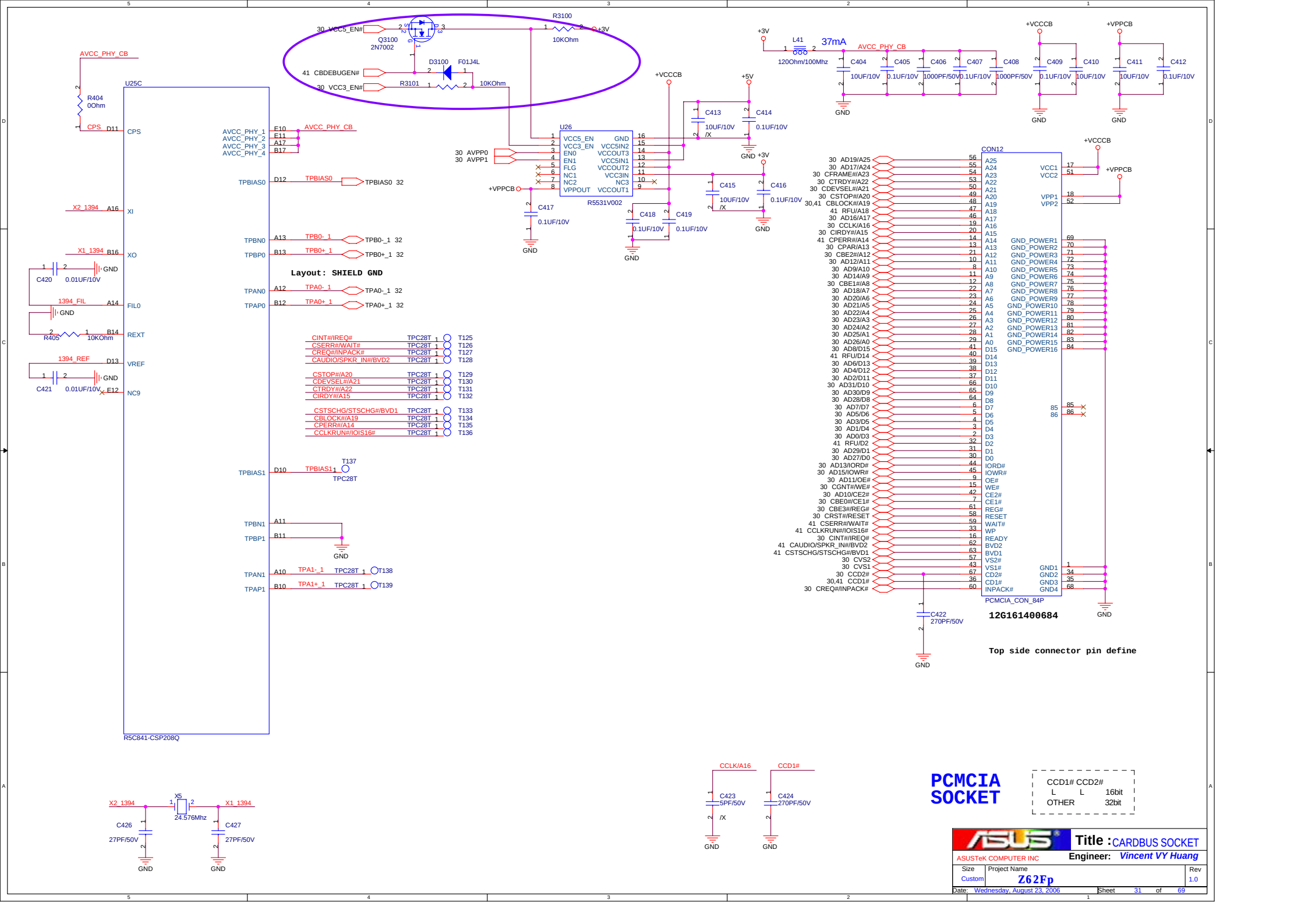
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

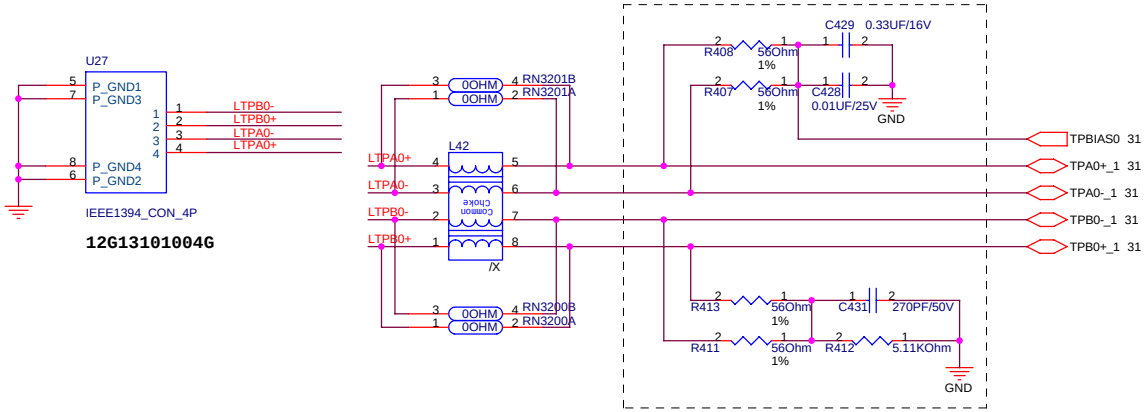


PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched
to parallel port interface for
in-system programming.

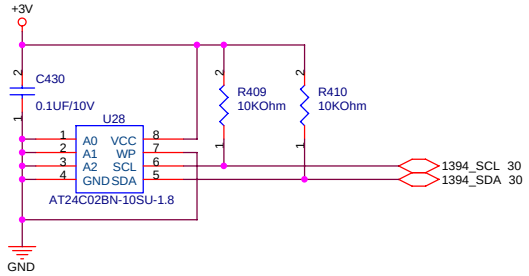
ASUSTek COMPUTER INC	Title : EC IT8510TE(2/2)	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 29 of 69	

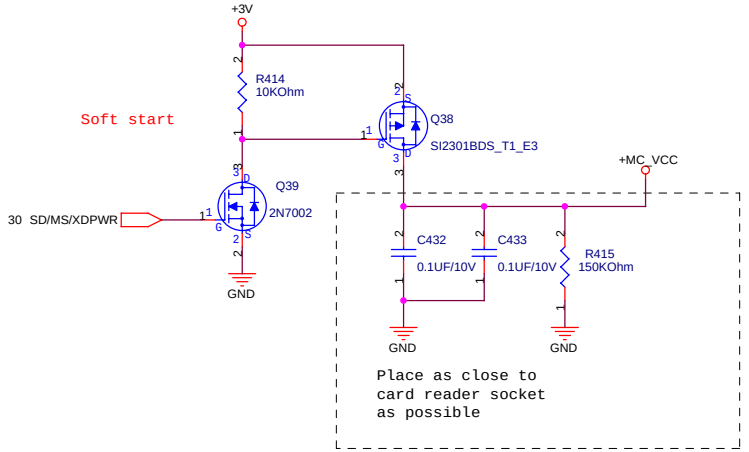

+3VS
5mA
C381 10UF/10V
C382 0.1UF/10V
C383 0.1UF/10V
C384 0.01UF/10V
GND
External 1.8V source
VCC_RIN_CB
71mA
C385 10UF/10V
C386 0.1UF/10V
C387 0.1UF/10V
C398 0.47UF/16V
C399 0.47UF/16V
C393 0.1UF/10V
C394 0.1UF/10V
R394 100KOhm
VCC_ROUT_CB
R2.0_N010
+3V
U25B
W3 VCC_PCI3V_1
R11 VCC_PCI3V_2
R12 VCC_PCI3V_3
R6 VCC_RIN_1
E13 VCC_RIN_2
L1 VCC_ROUT_1
E14 VCC_ROUT_2
R7 REGEN#
18,33 PCI_AD[31:0]
PCI_AD31 M2 AD31
PCI_AD30 M1 AD30
PCI_AD29 N5 AD29
PCI_AD28 N4 AD28
PCI_AD27 N2 AD27
PCI_AD26 N1 AD26
PCI_AD25 P5 AD25
PCI_AD24 P4 AD24
PCI_AD23 R4 AD23
PCI_AD22 R2 AD22
PCI_AD21 R1 AD21
PCI_AD20 T2 AD20
PCI_AD19 T1 AD19
PCI_AD18 U2 AD18
PCI_AD17 U1 AD17
PCI_AD16 V1 AD16
PCI_AD15 T7 AD15
PCI_AD14 V7 AD14
PCI_AD13 W7 AD13
PCI_AD12 R8 AD12
PCI_AD11 T8 AD11
PCI_AD10 V8 AD10
PCI_AD9 W8 AD9
PCI_AD8 R9 AD8
PCI_AD7 V9 AD7
PCI_AD6 W9 AD6
PCI_AD5 T11 AD5
PCI_AD4 V11 AD4
PCI_AD3 W11 AD3
PCI_AD2 T12 AD2
PCI_AD1 V12 AD1
PCI_AD0 W12 AD0
Open Drain : PME#, SERR#, INTn#
18,33 PCI_PAR V6 PAR
PCI_C/BE#3 P2 C/BE3#
PCI_C/BE#2 W2 C/BE2#
PCI_C/BE#1 W6 C/BE1#
PCI_C/BE#0 T9 C/BE0#
IDSEL_CB P1 IDSEL
18,33 PCI_C/BE#[3:0]
18 PCI_REQ#1 M4 REQ#
18 PCI_GNT#1 M5 GNT#
18,19,33 PCI_FRAME# V3 FRAME#
18,19,33 PCI_IRDY# V4 IRDY#
18,19,33 PCI_TRDY# W4 TRDY#
18,19,33 PCI_DEVSEL# T5 DEVSEL#
18,19,33 PCI_STOP# V5 STOP#
18,19,33 PCI_PERR# W5 PERR#
18,19,33 PCI_SERR# T6 SERR#
CB_GBRST# G2 GBRST#
12,18,24,25,26,33 PCI_RST# L4 PCIRST#
5,41 CLK_CBPCI K1 PCICLK
19,24,33 PM_CLKRUN# L5 CLKRUN#
33 PCI_PME# G4 RI_OUT#/PME#
C401 5PF/50V /X
C402 5PF/50V /X
L.C.A
GND
R5C841-CSP208Q
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCI_AD17
R402 IDSEL_CB 100Ohm
+3V ==> CB_GBRST#
1ms < T < 100ms
CB_GBRST# R403 100KOhm +3V
C403 0.1UF/10V GND
8mA
C388 10UF/10V
C389 0.1UF/10V
C390 1000PF/50V
C391 1000PF/50V
VCC_3V_1
VCC_3V_3
VCC_3V_4
VCC_3V_2
VCC_MD3V
4mA
C396 10UF/10V
C397 1000PF/50V
C395 0.1UF/10V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
R395 10KOhm
HWSPND# CB_HWSUSP#
SPKROUT SPKR_CB 21
R396 100KOhm
SPKRCB PULL DOWN : USE SROM
UDIO5 T119 TPC28T
UDIO4 1394_SDA 32
UDIO3 1394_SCL 32
UDIO2 T120 TPC28T
UDIO1 T121 TPC28T
UDIO0/SRIRQ# INT_SERIRQ 19,24,25,28
INTA# PCI_INTB# 18,19
INTB# PCI_INTC# 18,19
INTC# PCI_INTD# 18,19
NC1
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
U25A
C1 NC2
D1 NC3
E1 NC4
C2 NC5
D2 NC6
E2 NC7
E4 NC8
R5C841-CSP208Q
T779 TPC28T MDIO19 E8 MDIO19
T780 TPC28T MDIO18 D8 MDIO18
T781 TPC28T MDIO17 B8 MDIO17
T782 TPC28T MDIO16 A8 MDIO16
T783 TPC28T MDIO15 E7 MDIO15
T784 TPC28T MDIO14 D7 MDIO14
32 SD/MS/XDDAT3 B7 MDIO13
32 SD/MS/XDDAT2 A7 MDIO12
32 SD/MS/XDDAT1 E6 MDIO11
32 SD/MS/XDDAT0 D6 MDIO10
SHIELD GND
32 SD/MSCLK_XDRE# L.C.A R397 22Ohm B6 MDIO09
32 SDCMD_MSBS_XDWE# A6 MDIO08
SHIELD GND R398 0Ohm D5 MDIO07
T122 TPC28T MDIO6 B5 MDIO06
T785 TPC28T MDIO5 A5 MDIO05
32 SD/MS/XDPWR B4 MDIO04
32 SDWP_XDR/B# B3 MDIO03
T786 TPC28T MDIO2 A3 MDIO02
32 MSCD# A2 MDIO01
32 SDCD# B1 MDIO00
CADR25 J18 AD19/A25 31
CADR24 J15 AD17/A24 31
CADR23 K16 CFRAME#/A23 31
CADR22 L16 CTRDY#/A22 31
CADR21 L18 CDEVSEL#/A21 31
CADR20 M16 CSTOP#/A20 31
CADR19 N19 CBLOCK#/A19 31,41
CADR18 N16 C_RFU/A18 41
CADR17 P16 AD16/A17 31
CADR16 L19
R389 22Ohm
CCLK/A16 31
SHIELD GND
C392 5PF/50V
L.C.A
CADR15 K15 CIRDY#/A15 31
CADR14 N18 C_CPERR#/A14 41
CADR13 N15 CPAR/A13 31
CADR12 K18 CBE2#/A12 31
CADR11 R18 AD12/A11 31
CADR10 U19 AD9/A10 31
CADR9 R19 AD14/A9 31
CADR8 P15 CBE1#/A8 31
CADR7 J16 AD18/A7 31
CADR6 H15 AD20/A6 31
CADR5 H18 AD21/A5 31
CADR4 G15 AD22/A4 31
CADR3 G18 AD23/A3 31
CADR2 F15 AD24/A2 31
CADR1 F18 AD25/A1 31
CADR0 E16 AD26/A0 31
CDATA15 U18 AD8/D15 31
CDATA14 W18 C_RFU/D14 41
CDATA13 V17 AD6/D13 31
CDATA12 V16 AD4/D12 31
CDATA11 V15 AD2/D11 31
CDATA10 B19 AD31/D10 31
CDATA9 C18 AD30/D9 31
CDATA8 D18 AD28/D8 31
CDATA7 W17 AD7/D7 31
CDATA6 W16 AD5/D6 31
CDATA5 W15 AD3/D5 31
CDATA4 T15 AD1/D4 31
CDATA3 R14 AD0/D3 31
CDATA2 C19 C_RFU/D2 41
CDATA1 D19 AD29/D1 31
CDATA0 E19 AD27/D0 31
OE# T19 AD11/OE# 31
WE# M15 CGNT#/WE# 31
CE2# T18 AD10/CE2# 31
CE1# V19 CBE0#/CE1# 31
REG# F16 CBE3#/REG# 31
C400 0.01UF/10V
GND
RESET H19 CRST#/RESET 31
WAIT# G16 C_CSERR#/WAIT# 41
WP/IOIS16# A18 C_CCLKRUN#/IOIS16# 41
RDY/IREQ# M18 CINT#/IREQ# 31
BVD2 F19 C_CAUDIO/SPKR_IN#/BVD2 41
BVD1 E18 C_STSCHG/STSCHG#/BVD1 41
VS2# H16 CVS2 31
VS1# R16 CVS1 31
CD2# D15 CCD2# 31
CD1# T14 CCD1# 31,41
INPACK# G19 CREQ#/INPACK# 31
IORD# P18 AD13/IORD# 31
IOWR# P19 AD15/IOWR# 31
90 ohm
USBDP V14 T123 TPC28T
USBDM W14 T124 TPC28T
+3V
R399 100KOhm
+VCCCB
R400 100KOhm /X
C_CCLKRUN#/IOIS16#
VPPEN1 W13 AVPP1 31
VPPEN0 V13 AVPP0 31
VCC3EN# T13 VCC3_EN# 31
VCC5EN# R13 VCC5_EN# 31
R401 100KOhm /X
GND
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
CB_HWSUSP# D34 1N4148W CB_SD# 19
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3V$ OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Vincent VY Huang
Size Custom
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 30 of 69

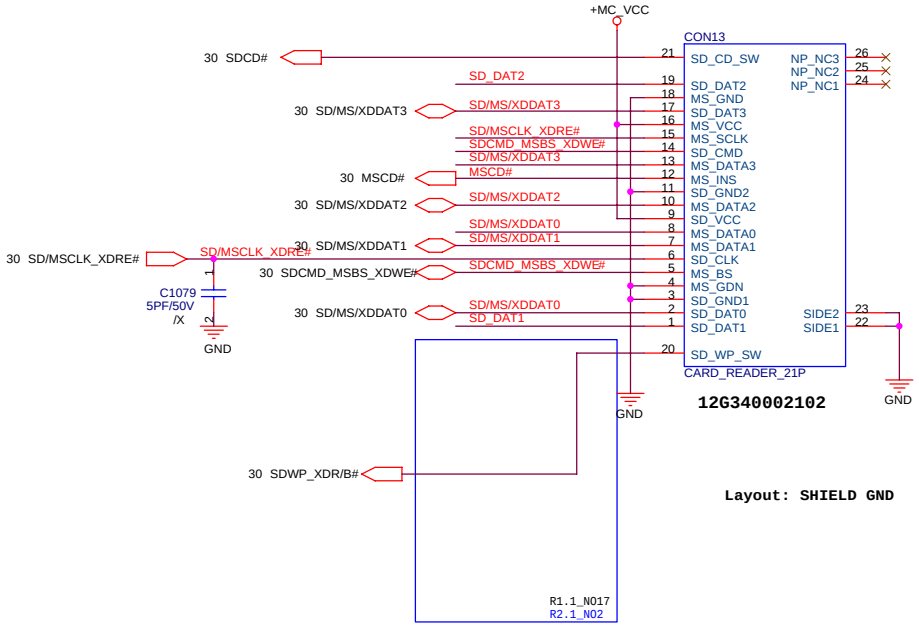

U25C
R5C841-CSP208Q
Layout: SHIELD GND
Top side connector pin define
PCMCIA SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Vincent VY Huang
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 31 of 69



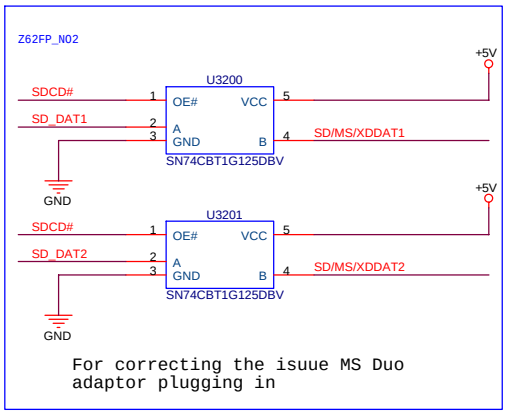
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm



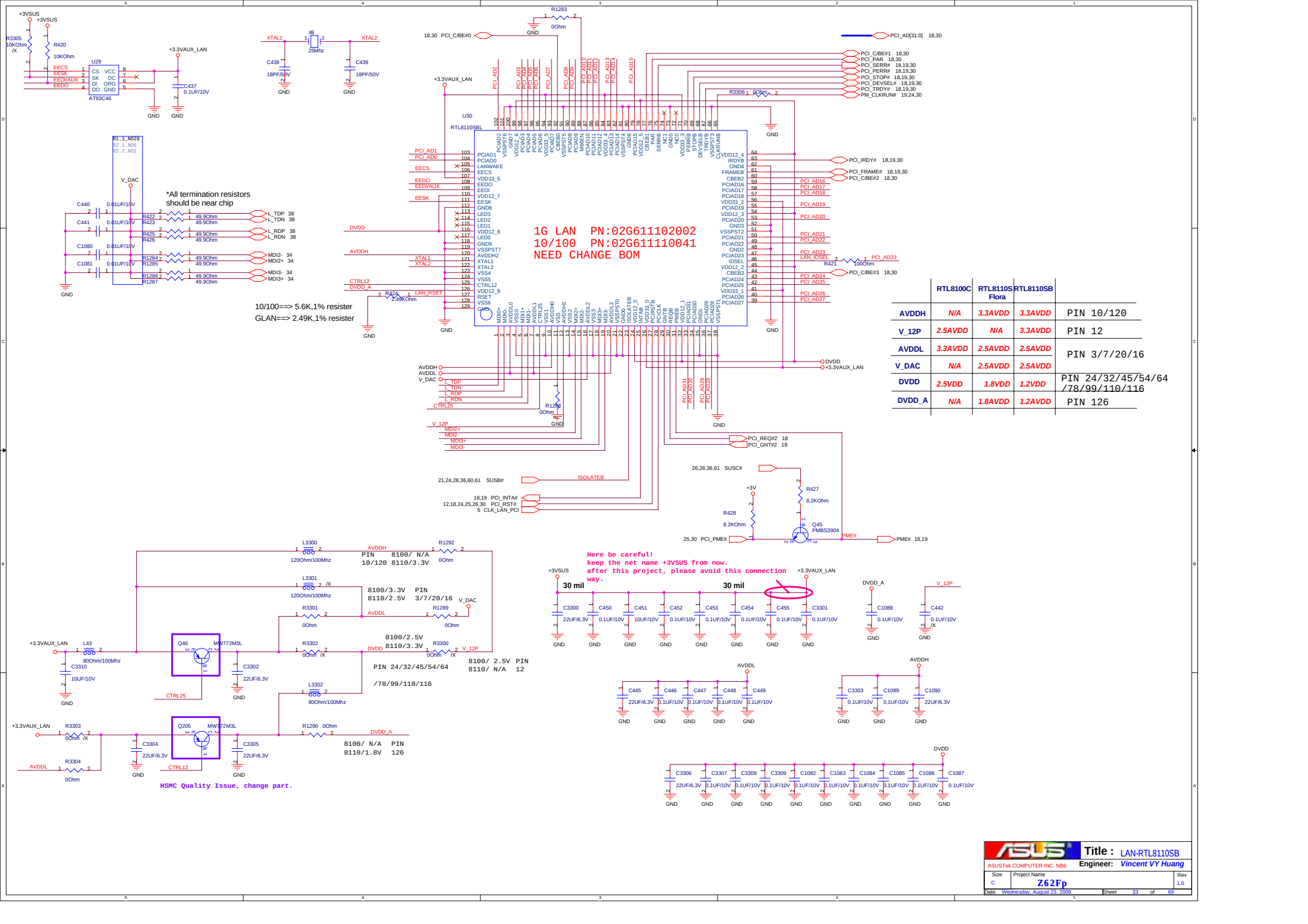




Layout: SHIELD GND



ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 32 of 69	

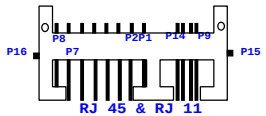


	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

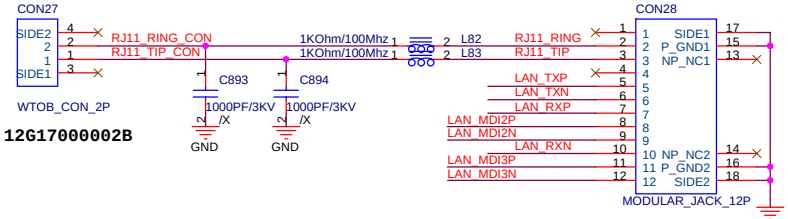
Title :	LAN-RTL8110SB	
ASUSTek COMPUTER INC. NB6	Engineer:	Vincent VY Huang
Size: C	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 33 of 69	

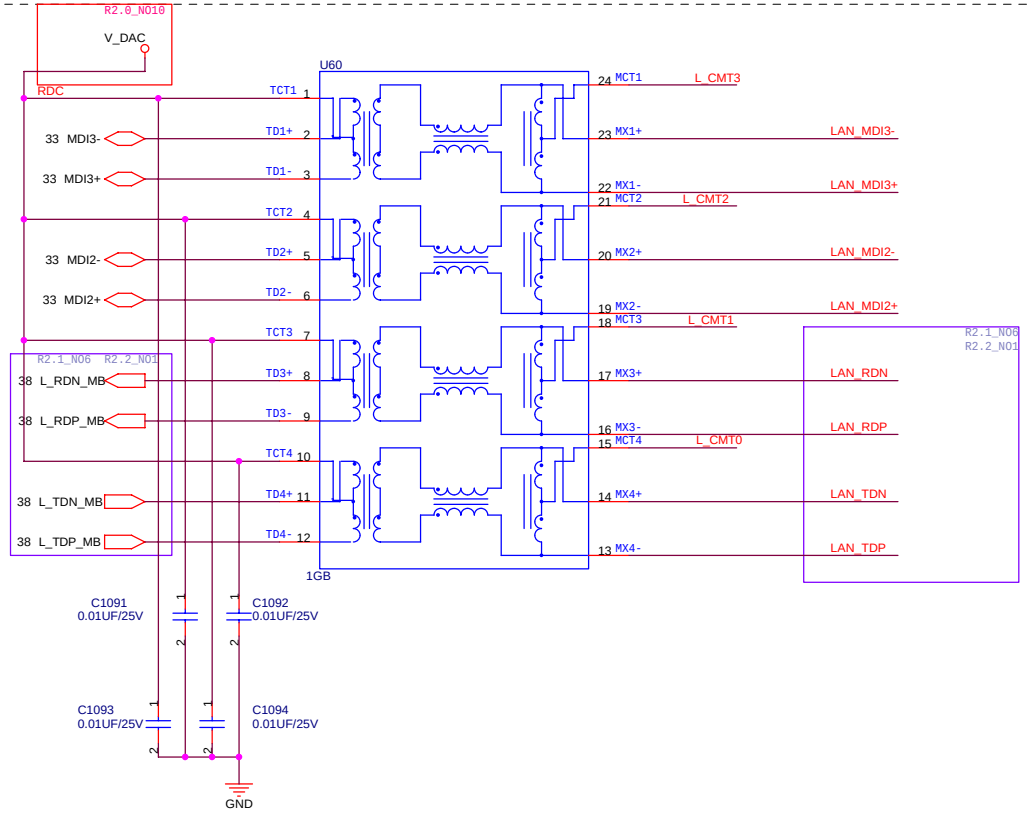
LAN PORT

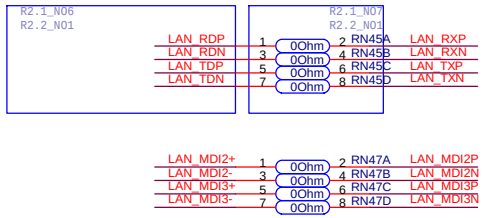
12-142313122

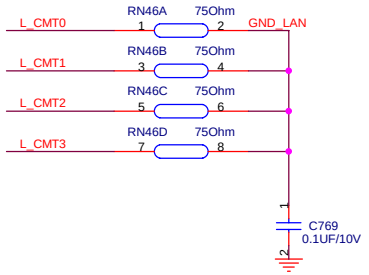


RJ 45 & RJ 11
BOTTOM VIEW









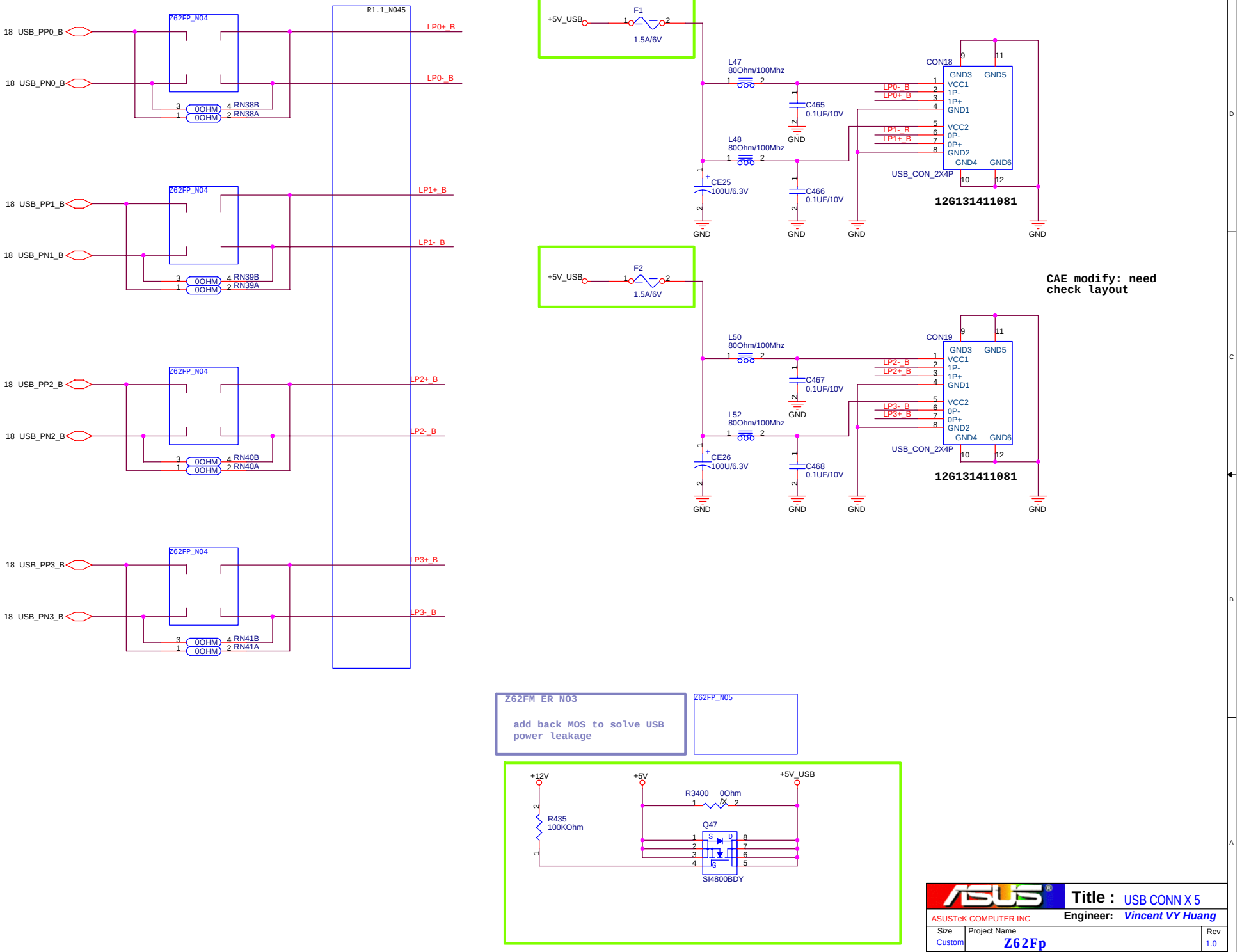
ASUSTeK COMPUTER INC

Title : RJ11+45

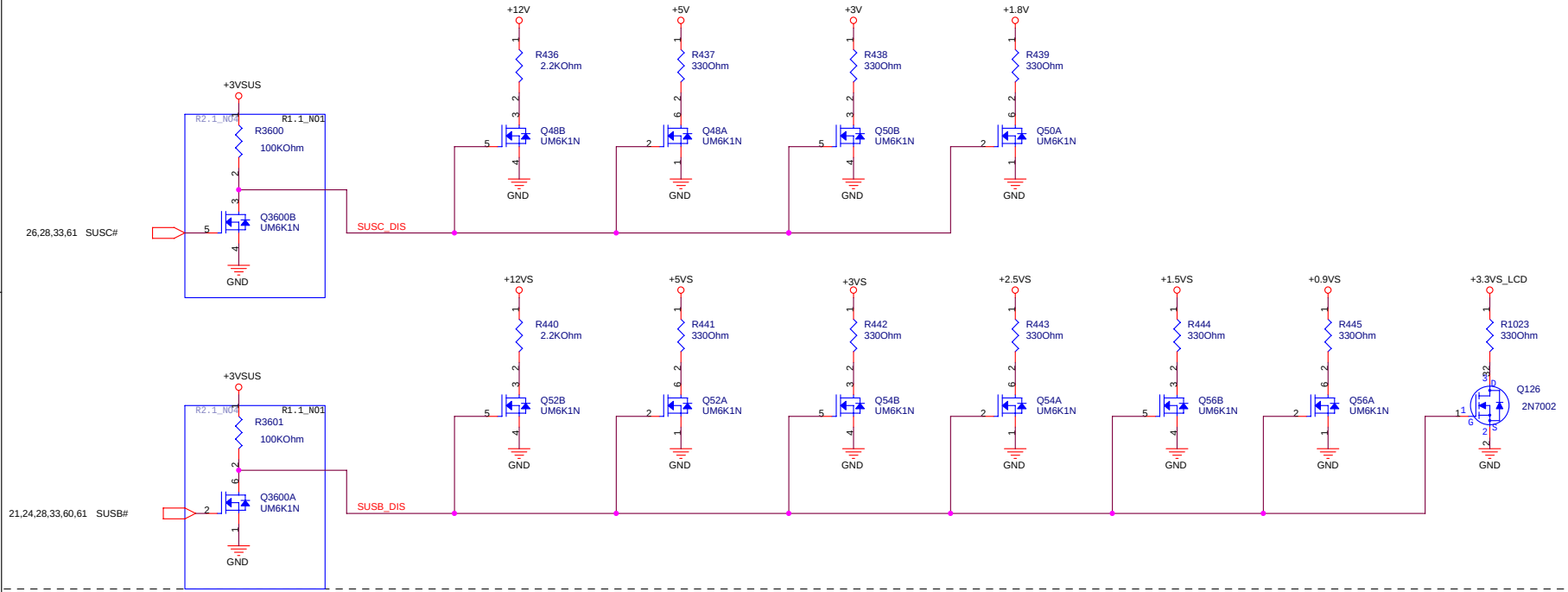
Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

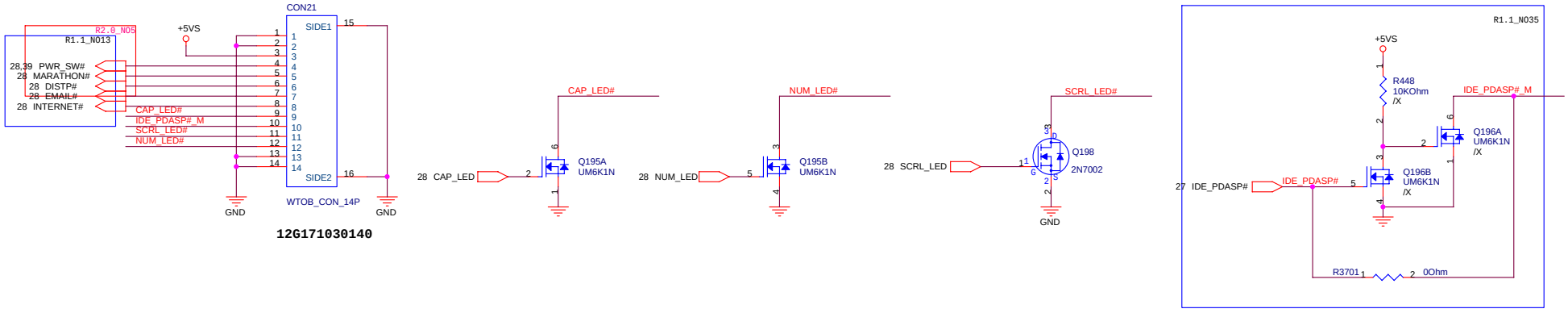
Date: Wednesday, August 23, 2006 Sheet 34 of 69

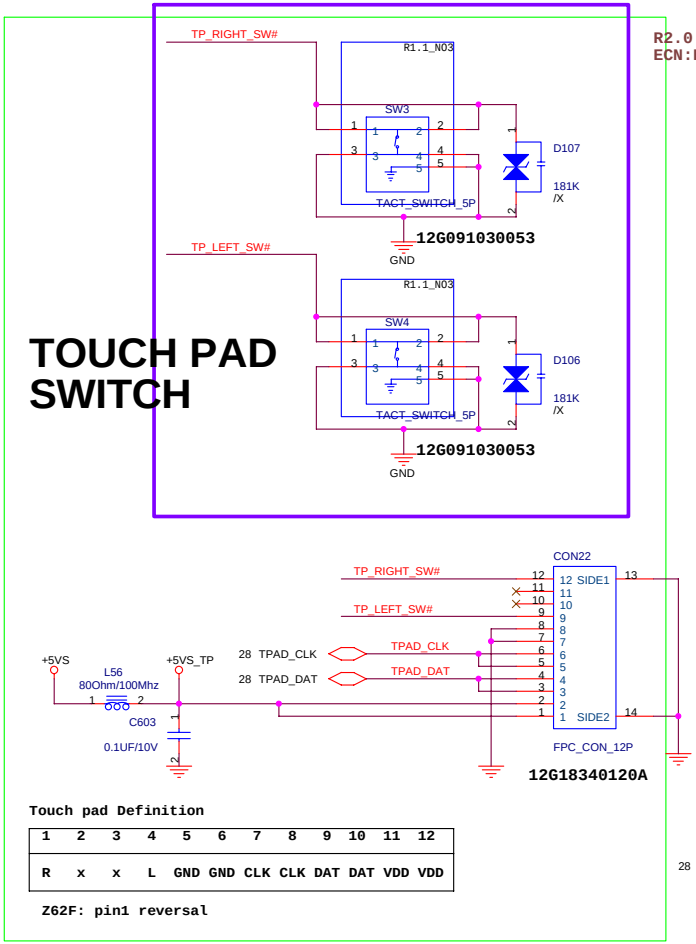


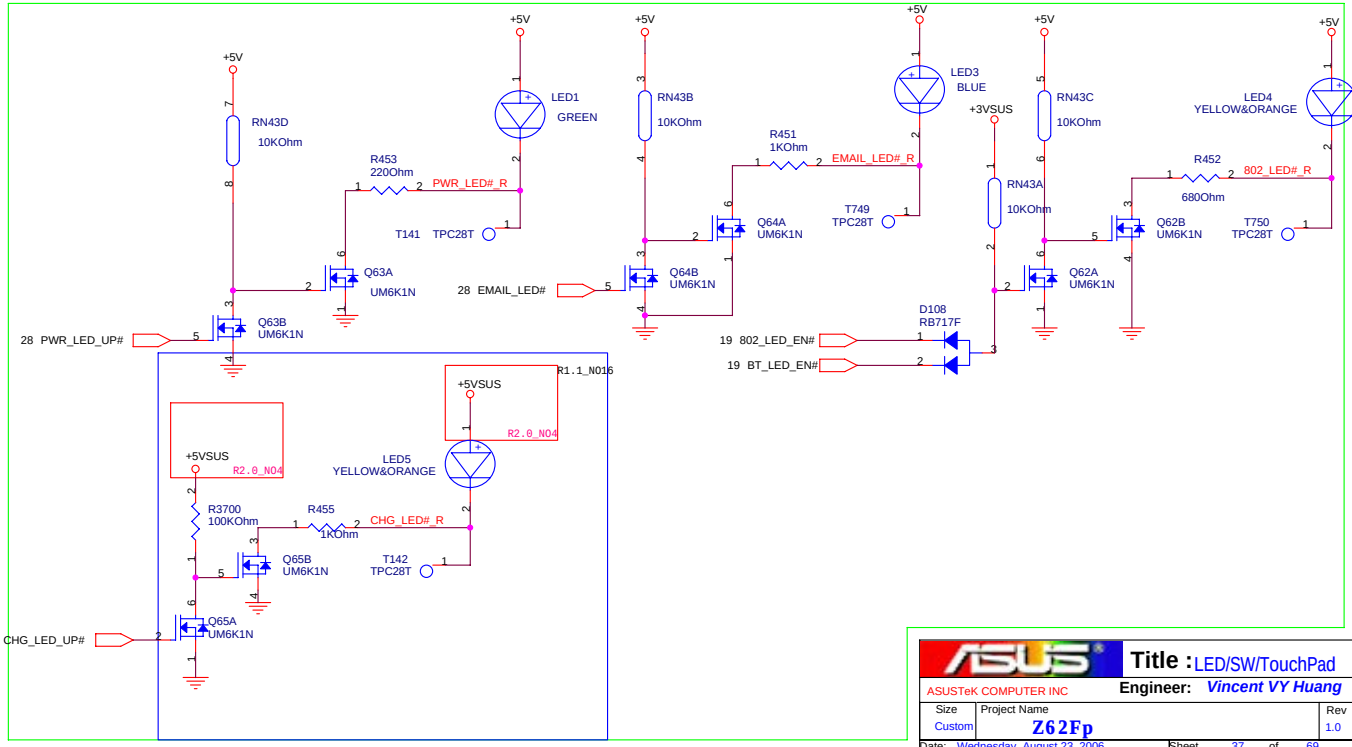
ASUSTeK COMPUTER INC	Title : USB CONN X 5	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 35 of 69	



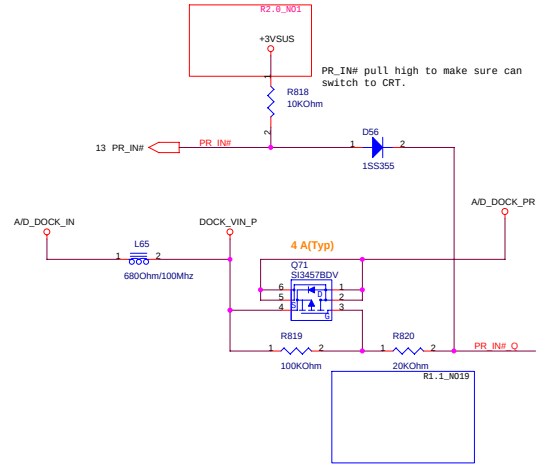
ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 36 of 69	



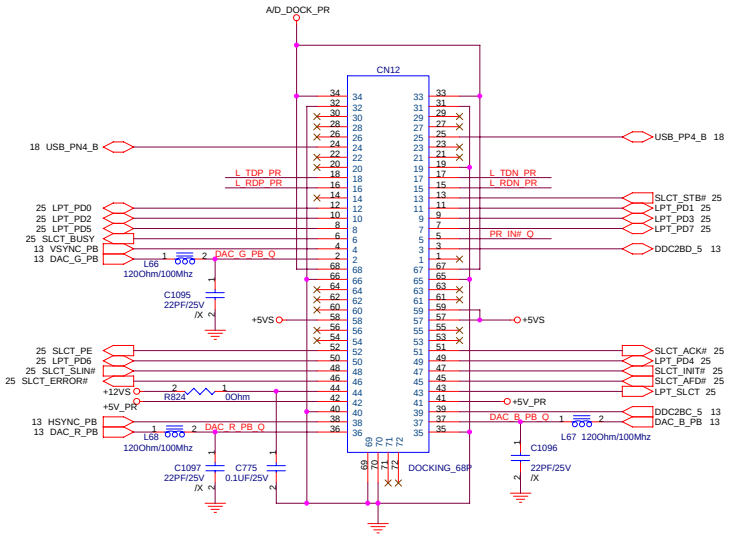




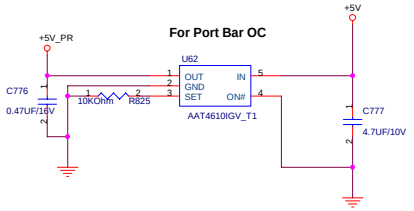
Title :	LED/SW/TouchPad
ASUSTeK COMPUTER INC	Engineer: Vincent VY Huang
Size: Custom	Project Name: Z62Fp
Rev:	1.0
Date:	Wednesday, August 23, 2006
Sheet	37 of 69

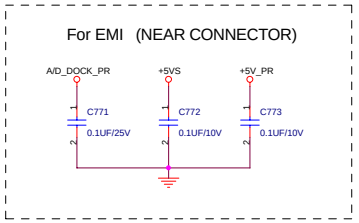


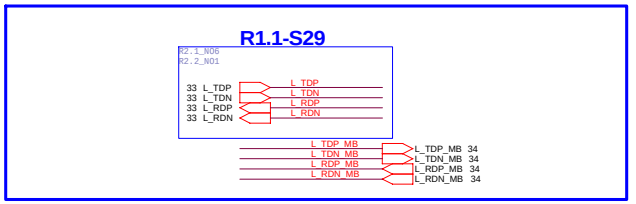
PORT BAR III CONN.

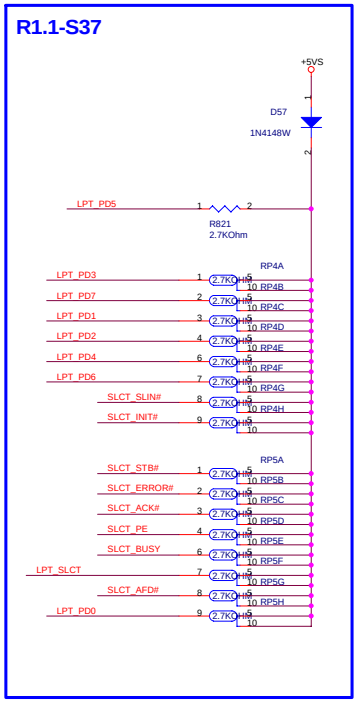


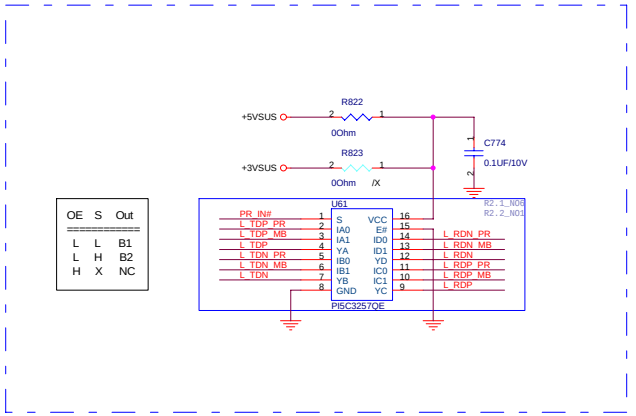
12G190006810

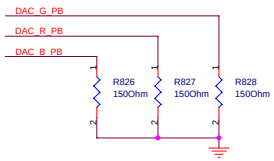




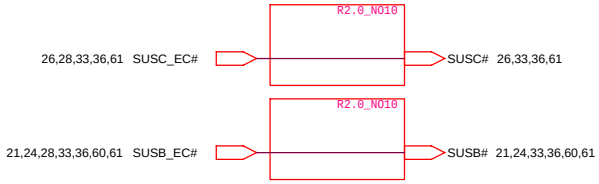


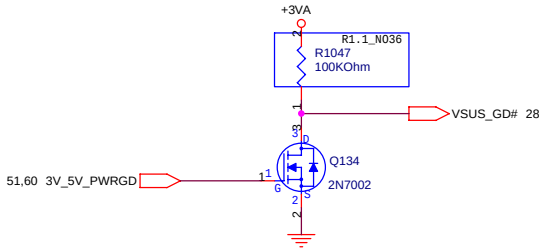




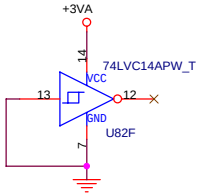


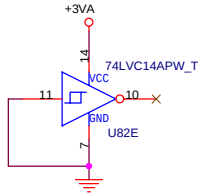
ASUSTeK COMPUTER INC	Title : PORT BAR 3 Conn.	
	Engineer: Vincent VY Huang	
Size: C	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 38 of 69	

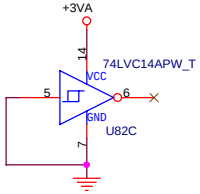


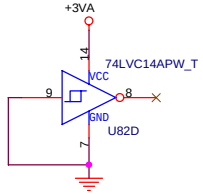


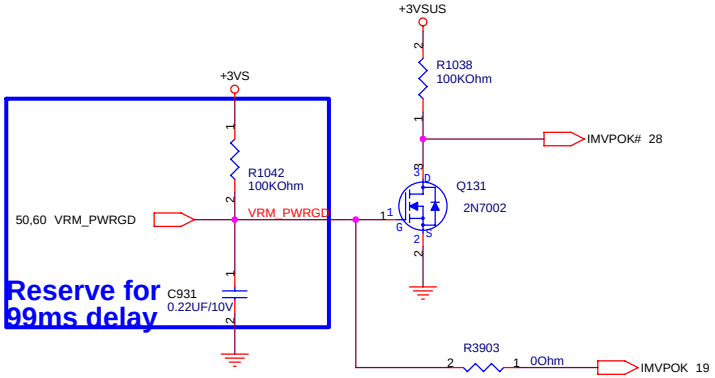
To Discharge circuits

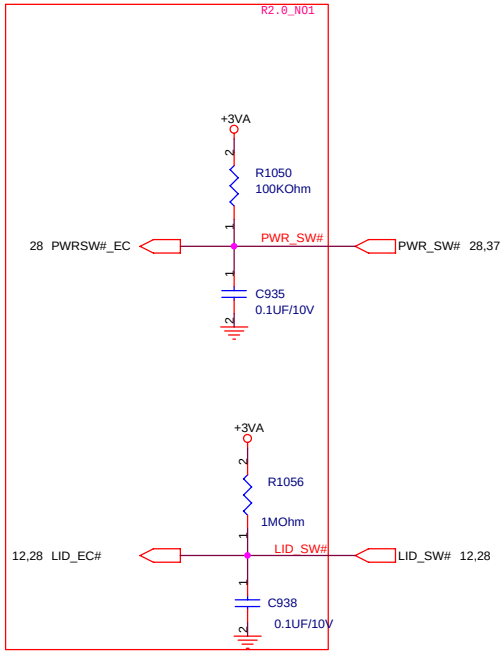






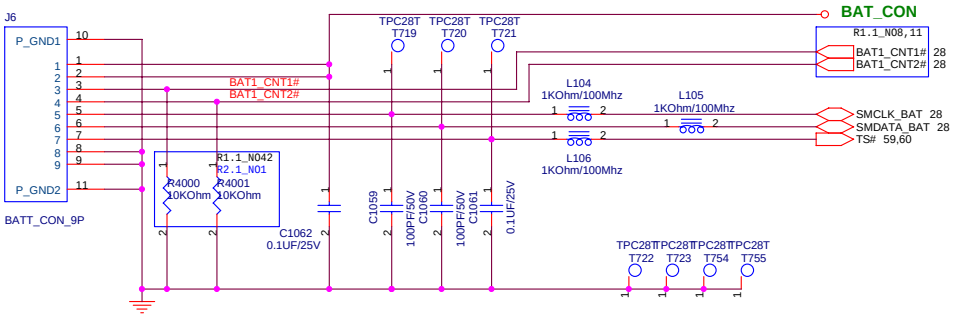




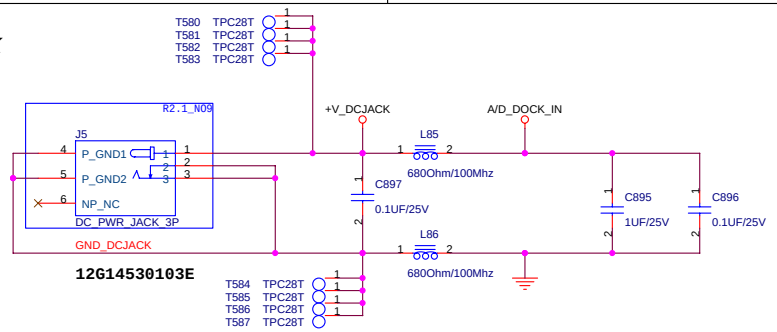


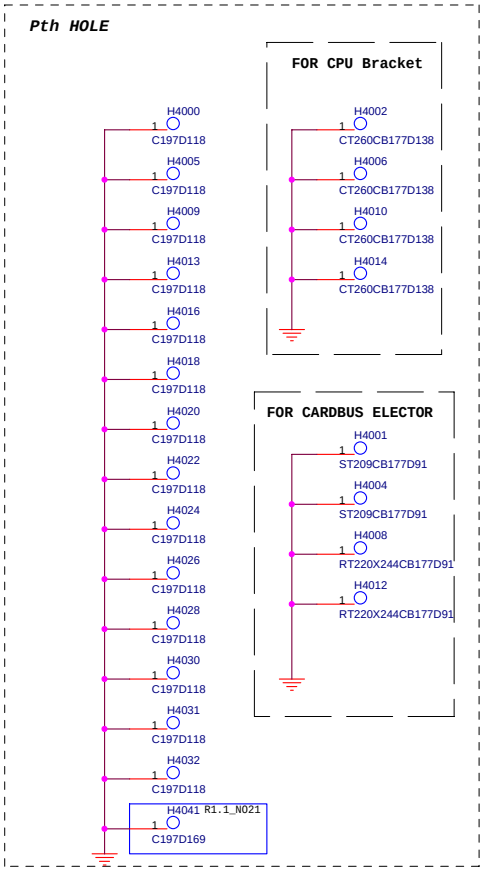
POWER SWITCH

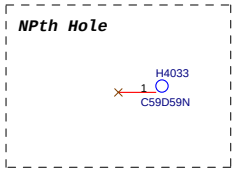
ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 39 of 69	

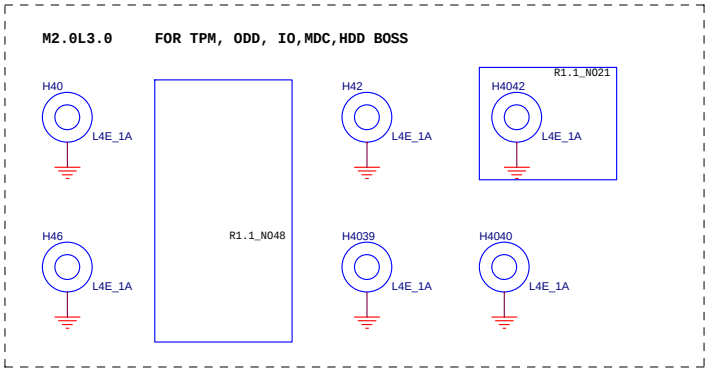


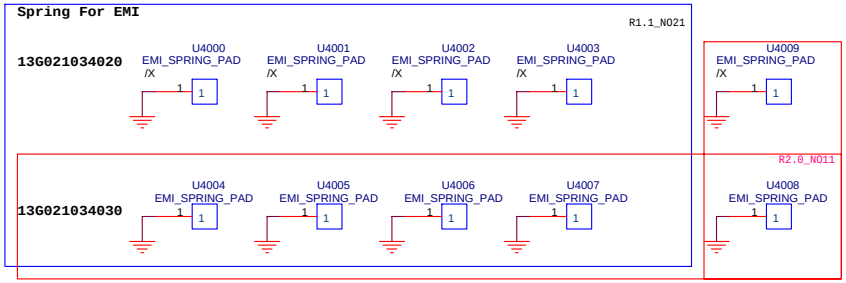
DC Power Jack











ASUSTeK COMPUTER INC

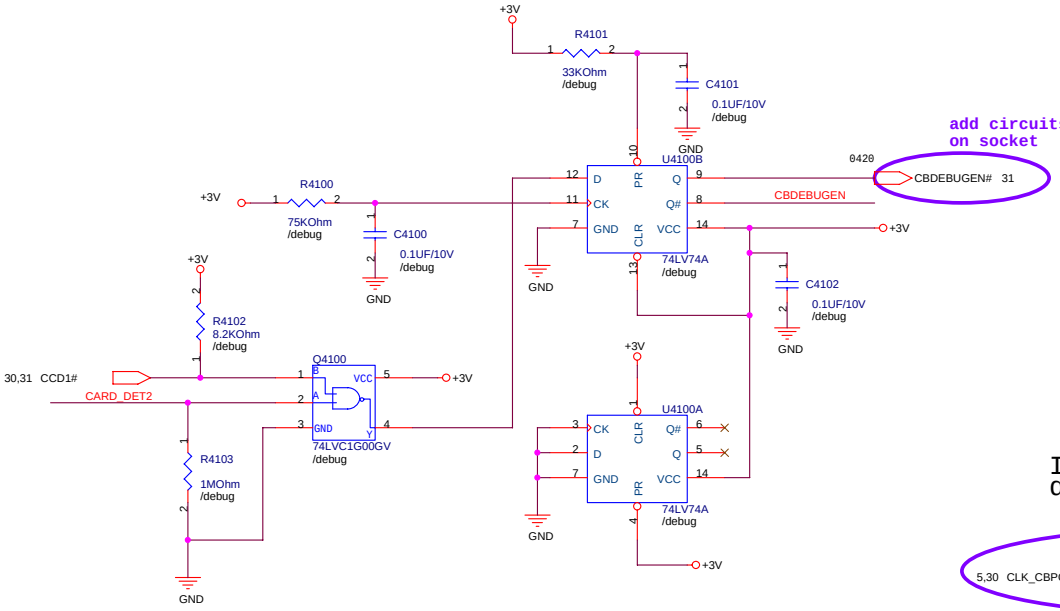
Title : DC/ BATT IN & Screw Hole

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

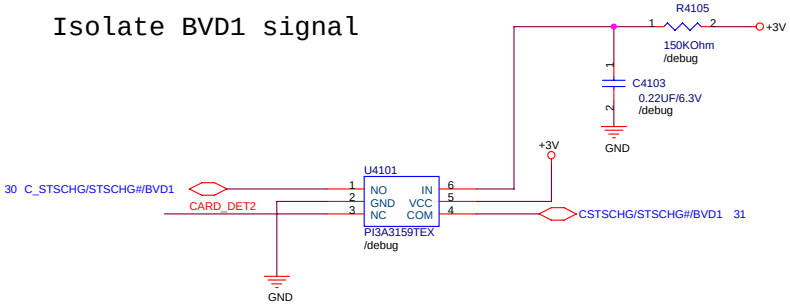
Date: Wednesday, August 23, 2006 Sheet 40 of 69

PCMCIA DEBUG PORT



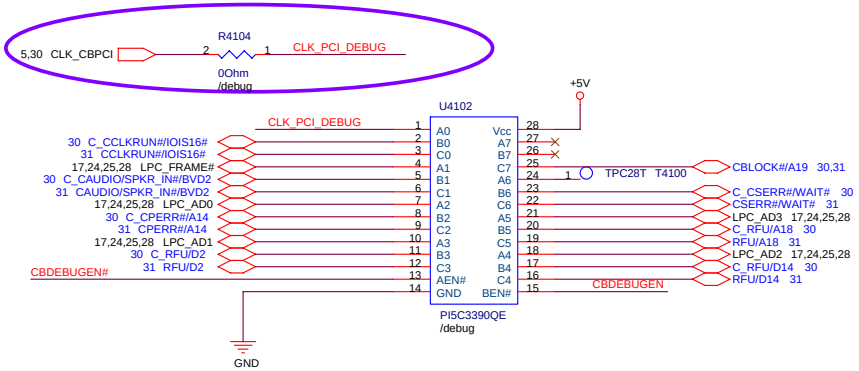
RC value may need to tuned for each product.

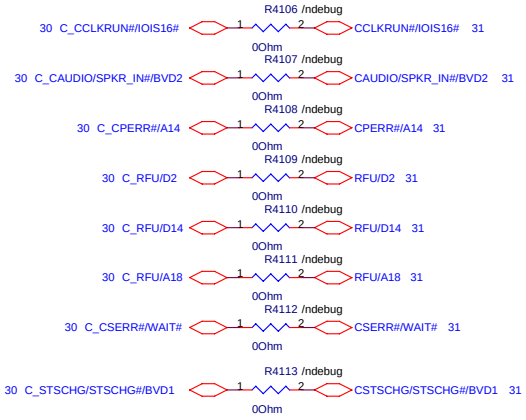
Isolate BVD1 signal



When +3V on, select BVD1 to CARD_DET2 for RC delay time

Isolate card bus control and slot signal when debug card plug in





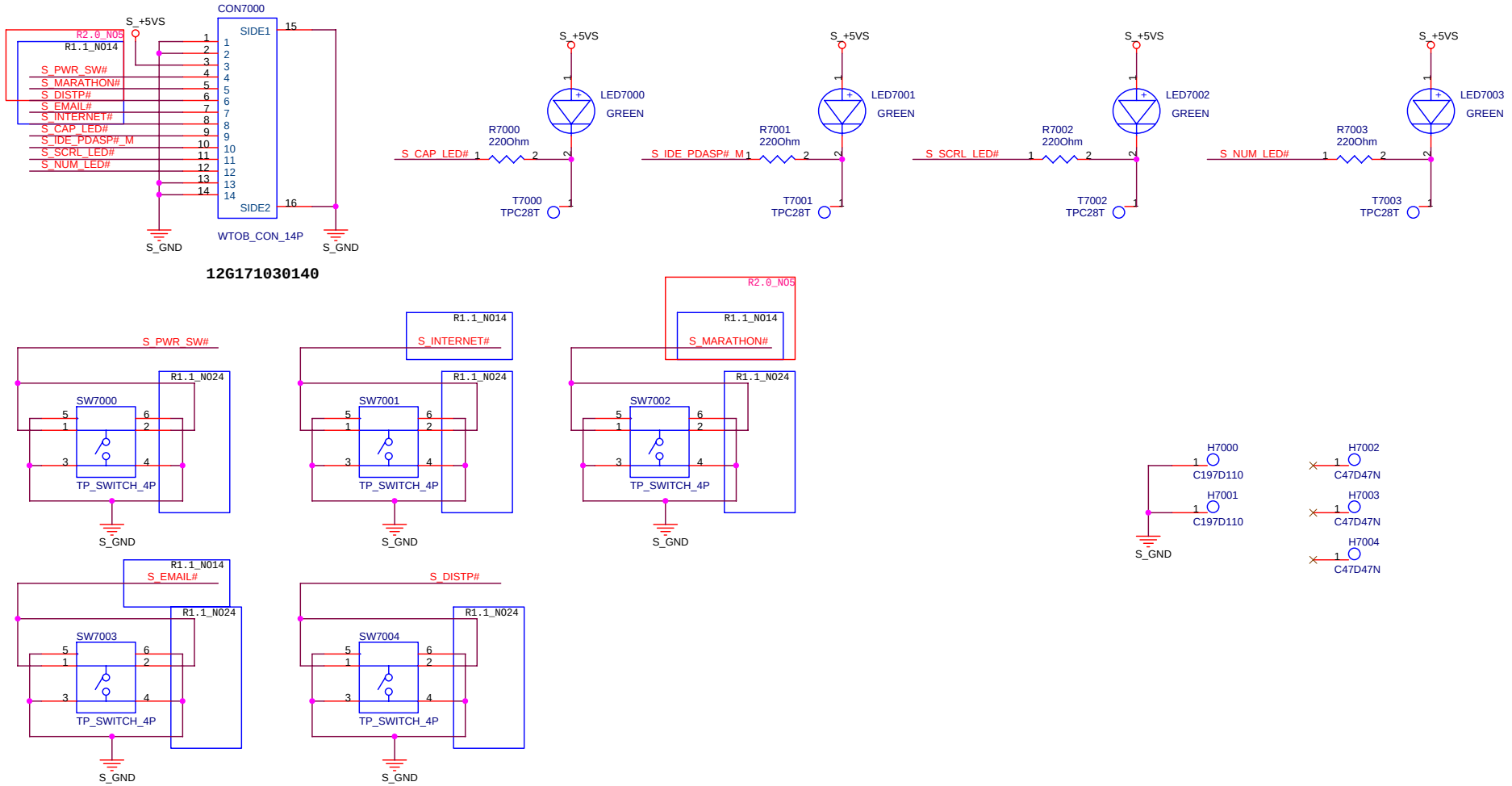
ASUSTeK COMPUTER INC

Title : PCMCIA Debug

Engineer: Vincent VY Huang

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 41 of 69



ASUSTeK COMPUTER INC	Title : Launch Board	
	Engineer: Vincent VY Huang	
Size: B	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 42 of 69	

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	43 of 69

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	44 of 69

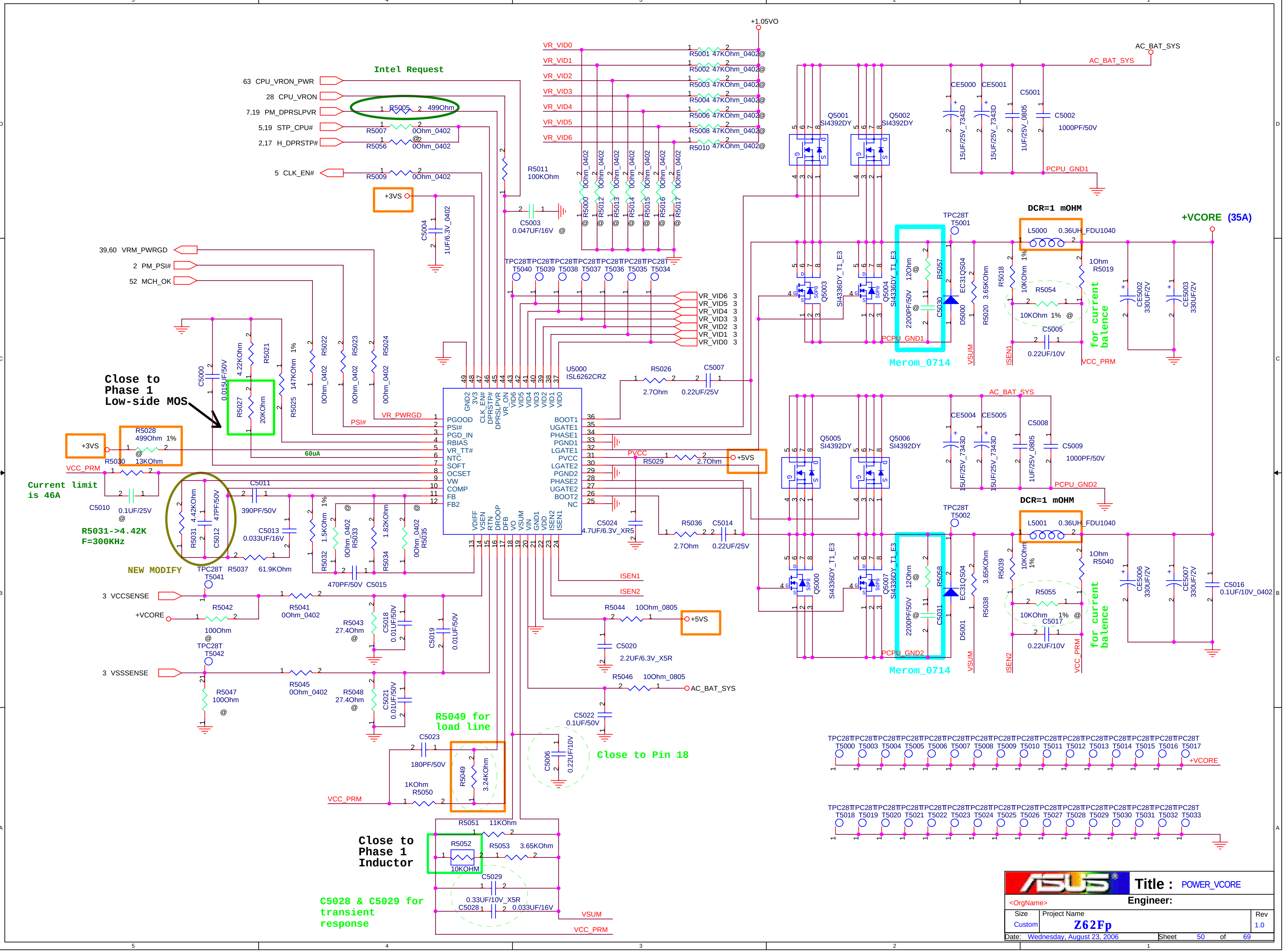
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	45 of 69

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	46 of 69

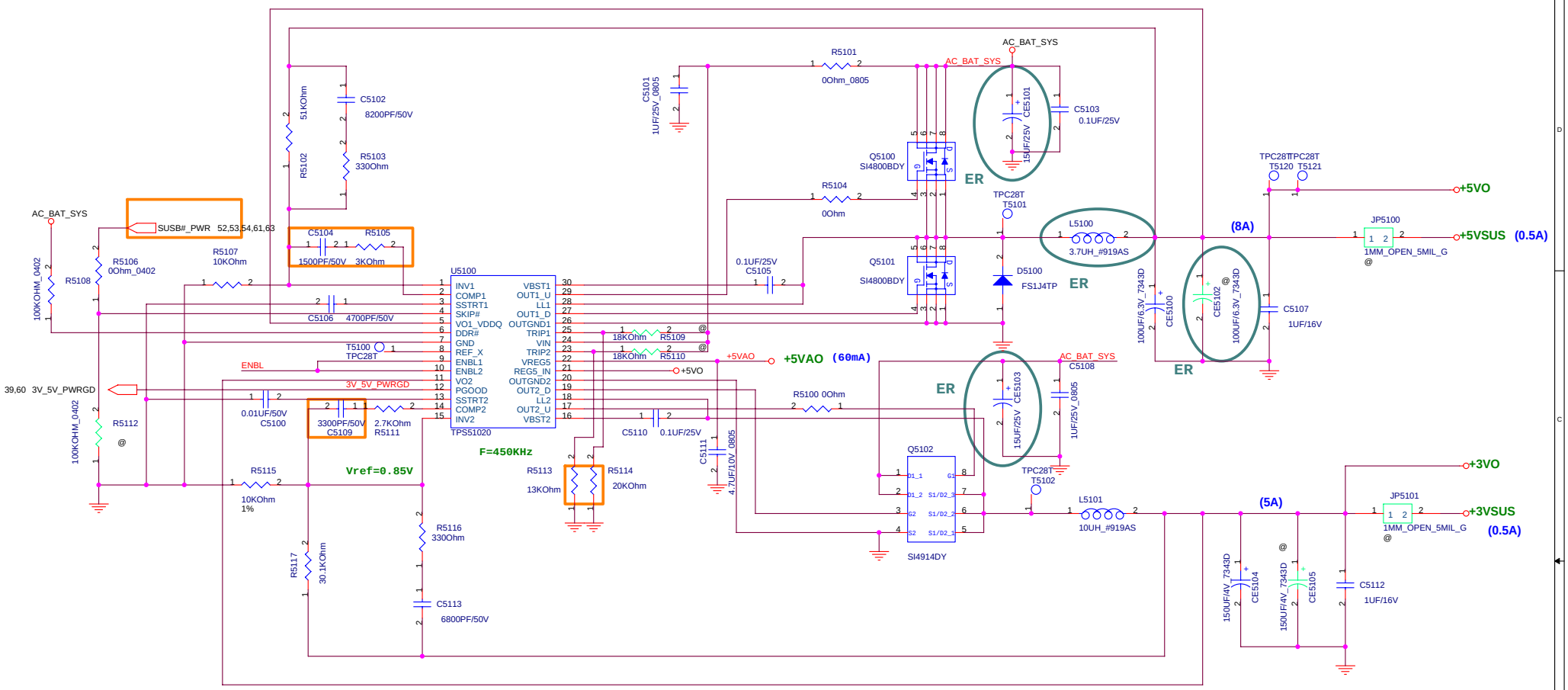
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	47 of 69

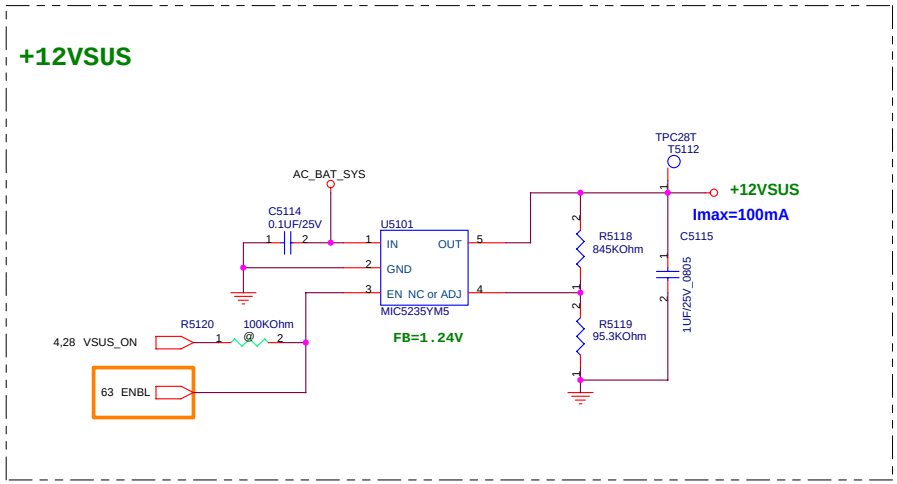
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	48 of 69

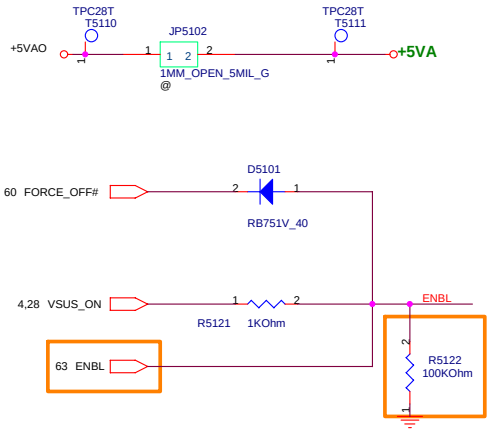
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Wednesday, August 23, 2006
Sheet	49 of 69

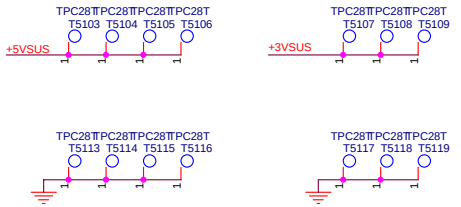


Intel Request
63 CPU_VRON_PWR
28 CPU_VRON
7,19 PM_DPRSLPVR
5,19 STP_CPU#
2,17 H_DPRSTP#
5 CLK_EN#
39,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
+1.05VO
R5001 47KOhm_0402@
R5002 47KOhm_0402@
R5003 47KOhm_0402@
R5004 47KOhm_0402@
R5006 47KOhm_0402@
R5008 47KOhm_0402@
R5010 47KOhm_0402@
R5005 499Ohm
R5007 0Ohm_0402
R5056 0Ohm_0402
R5009 0Ohm_0402
R5011 100KOhm
C5003 0.047UF/16V
C5004 1UF/6.3V_0402
+3VS
U5000 ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VR_PWRGD
PSI#
60uA
Close to Phase 1 Low-side MOS
Current limit is 46A
R5031->4.42K F=300KHz
NEW MODIFY
R5028 499Ohm 1%
R5030 13KOhm
VCC_PRM
C5010 0.1UF/25V
C5011 390PF/50V
C5013 0.033UF/16V
R5037 61.9KOhm
C5015 470PF/50V
3 VCCSENSE
+VCORE
3 VSSSENSE
R5042 100Ohm
R5041 0Ohm_0402
R5043 27.4Ohm
R5045 0Ohm_0402
R5047 100Ohm
R5048 27.4Ohm
R5049 for load line
R5049 3.24KOhm
R5050 1KOhm
C5023 180PF/50V
C5006 0.22UF/10V
Close to Pin 18
R5051 11KOhm
R5052 10KOHM
R5053 3.65KOhm
C5029 0.33UF/10V_X5R
C5028 0.033UF/16V
Close to Phase 1 Inductor
C5028 & C5029 for transient response
VSUM
VCC_PRM
ISEN1
ISEN2
R5044 10Ohm_0805
+5VS
C5020 2.2UF/6.3V_X5R
R5046 10Ohm_0805
AC_BAT_SYS
C5022 0.1UF/50V
R5026 2.7Ohm
C5007 0.22UF/25V
R5029 2.7Ohm
PVCC
R5036 2.7Ohm
C5014 0.22UF/25V
C5024 4.7UF/6.3V_X5R
Q5001 SI4392DY
Q5002 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5005 SI4392DY
Q5006 SI4392DY
Q5000 SI4336DY_T1_E3
Q5007 SI4336DY_T1_E3
CE5000 15UF/25V_7343D
CE5001 15UF/25V_7343D
C5001 1UF/25V_0805
C5002 1000PF/50V
PCPU_GND1
PCPU_GND2
DCR=1 mOHM
L5000 0.36UH_FDU1040
L5001 0.36UH_FDU1040
+VCORE (35A)
R5057 12Ohm
C5030 2200PF/50V
D5000 EC31QS04
D5001 EC31QS04
Merom_0714
R5018 10KOhm 1%
R5019 1Ohm
R5020 3.65KOhm
R5054 10KOhm 1%
C5005 0.22UF/10V
for current balence
CE5002 330UF/2V
CE5003 330UF/2V
CE5004
CE5005
C5008
C5009 1000PF/50V
R5058 12Ohm
C5031 2200PF/50V
R5038 3.65KOhm
R5039 10KOhm 1%
R5040 1Ohm
R5055 10KOhm 1%
C5017 0.22UF/10V
CE5006 330UF/2V
CE5007 330UF/2V
C5016 0.1UF/10V_0402
TPC28T
Title : POWER_VCORE
Engineer:
<OrgName>
Size Custom
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 50 of 69

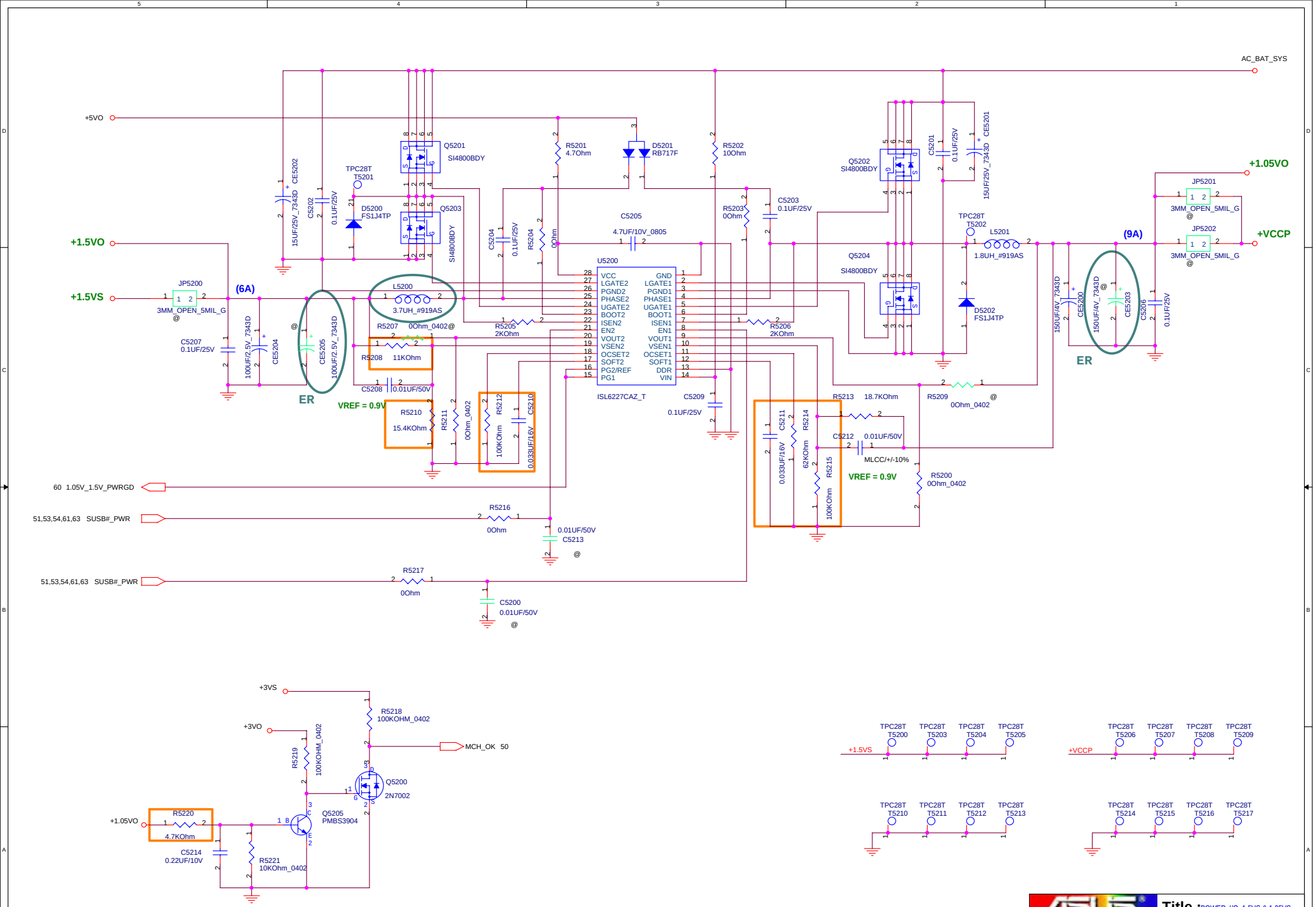


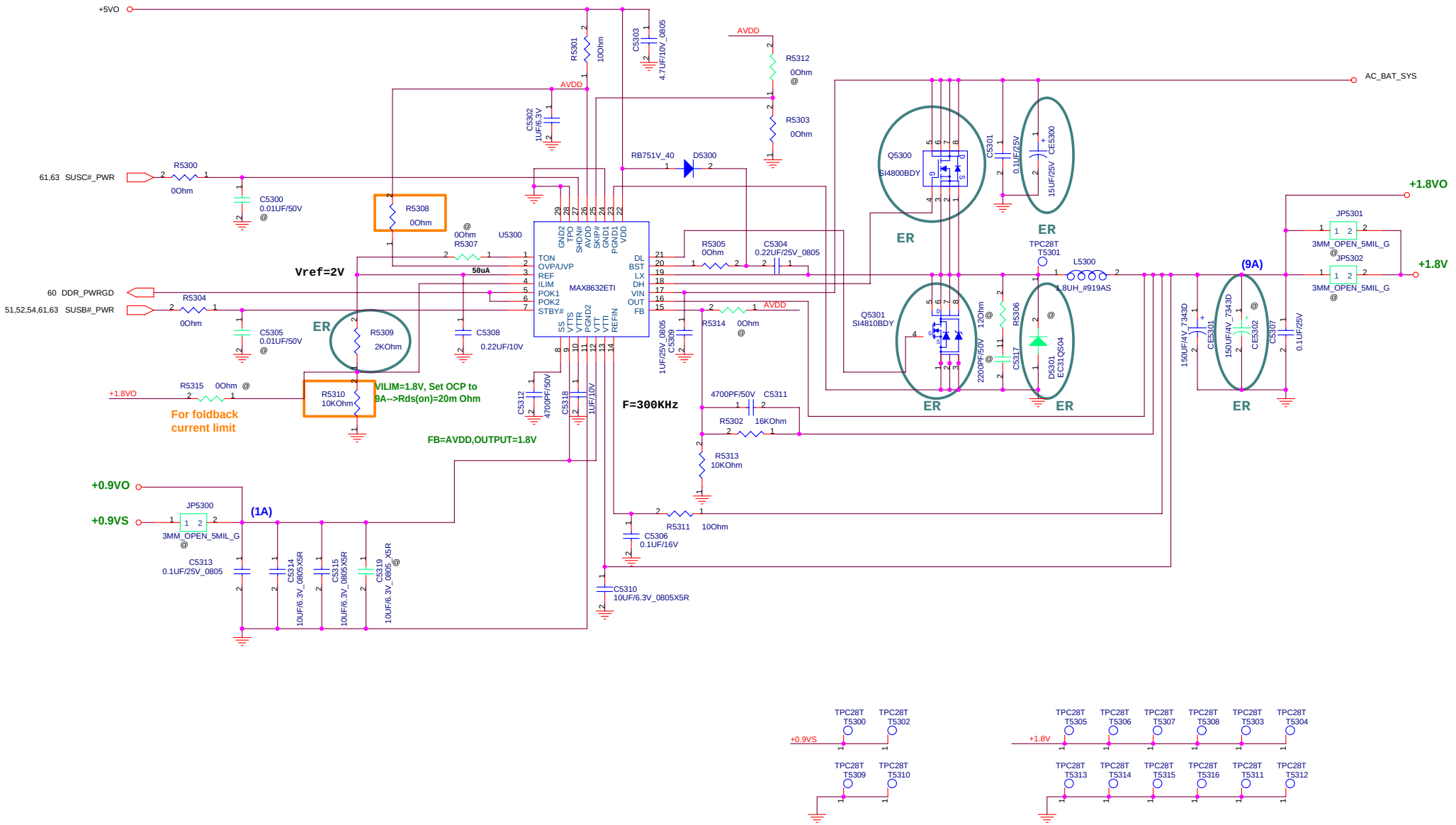






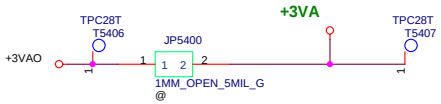
ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 51 of 69	

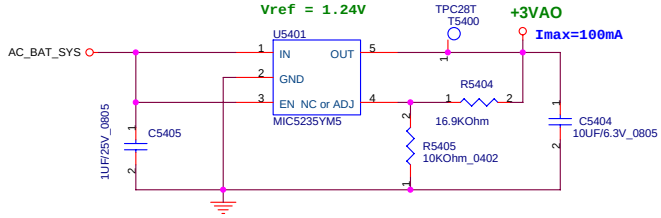

AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
(6A)
(9A)
JP5200
3MM_OPEN_5MIL_G
JP5201
JP5202
L5200
3.7UH_#919AS
L5201
1.8UH_#919AS
Q5201
SI4800BDY
Q5202
SI4800BDY
Q5203
SI4800BDY
Q5204
SI4800BDY
D5200
FS1J4TP
D5201
RB717F
D5202
FS1J4TP
U5200
ISL6227CAZ_T
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
R5200 0Ohm_0402
R5201 4.7Ohm
R5202 10Ohm
R5203 0Ohm
R5204 0Ohm
R5205 2KOhm
R5206 2KOhm
R5207 0Ohm_0402@
R5208 11KOhm
R5209 0Ohm_0402 @
R5210 15.4KOhm
R5211 0Ohm_0402
R5212 100KOhm
R5213 18.7KOhm
R5214 62KOhm
R5215 100KOhm
R5216 0Ohm
R5217 0Ohm
C5200 0.01UF/50V @
C5201 0.1UF/25V
C5202 0.1UF/25V
C5203 0.1UF/25V
C5204 0.1UF/25V
C5205 4.7UF/10V_0805
C5206 0.1UF/25V
C5207 0.1UF/25V
C5208 0.01UF/50V
C5209 0.1UF/25V
C5210 0.033UF/16V
C5211 0.033UF/16V
C5212 0.01UF/50V
MLCC/+/-10%
C5213 0.01UF/50V @
CE5200 150UF/4V_7343D
CE5201 15UF/25V_7343D
CE5202 15UF/25V_7343D
CE5203 150UF/4V_7343D @
CE5204 100UF/2.5V_7343D
CE5205 100UF/2.5V_7343D
TPC28T T5201
TPC28T T5202
ER
VREF = 0.9V
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
51,53,54,61,63 SUSB#_PWR
+3VS
+3VO
+1.05VO
R5218 100KOHM_0402
R5219 100KOHM_0402
R5220 4.7KOhm
R5221 10KOhm_0402
C5214 0.22UF/10V
Q5200 2N7002
Q5205 PMBS3904
MCH_OK 50
TPC28T T5200
TPC28T T5203
TPC28T T5204
TPC28T T5205
TPC28T T5206
TPC28T T5207
TPC28T T5208
TPC28T T5209
TPC28T T5210
TPC28T T5211
TPC28T T5212
TPC28T T5213
TPC28T T5214
TPC28T T5215
TPC28T T5216
TPC28T T5217
Title : POWER_I/O_1.5VS & 1.05VS
<OrgName>
Engineer:
Size Custom
Project Name Z62Fp
Rev 1.0
Date: Wednesday, August 23, 2006
Sheet 52 of 69



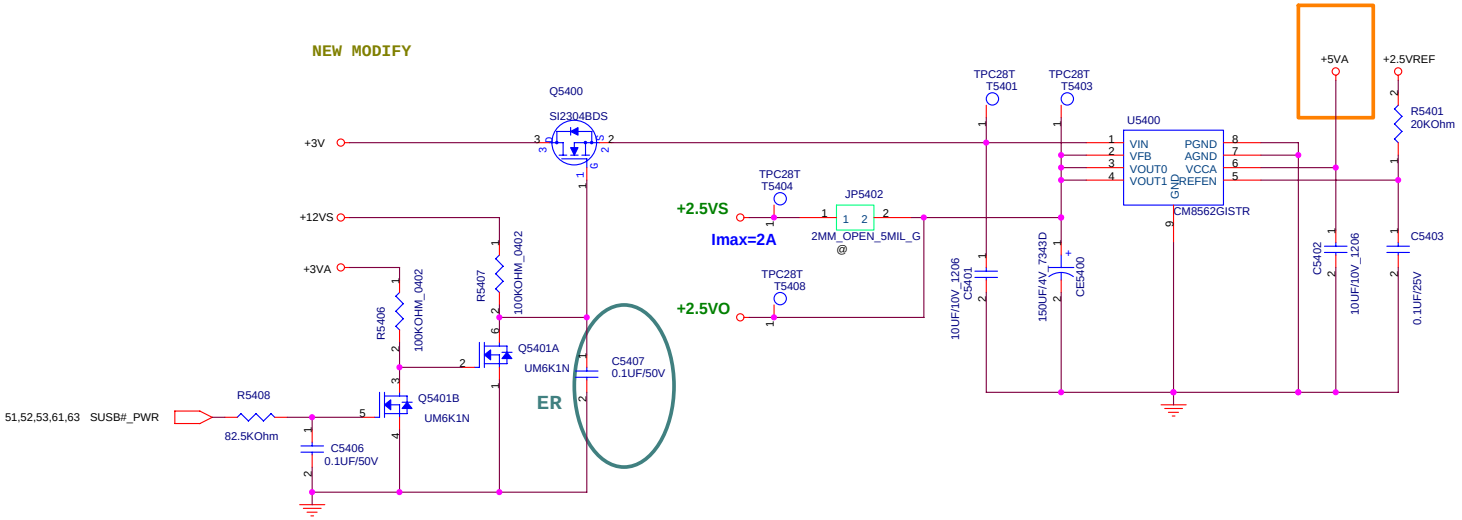
Title :	POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 53 of 69	

+3VA0





+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 54 of 69	

Title :	POWER_VGA_CORE & RAM
<OrgName>	Engineer:
Size: Custom	Project Name: Z62Fp
Rev: 1.0	
Date: Wednesday, August 23, 2006	Sheet 55 of 69

Title :	POWER_VGA_+1.2VSP
<OrgName>	Engineer:
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 56 of 69

TOTAL POWER=65W/19V -->3.42A

For open/short test

BATSEL_2P# = "H" (1P)			
BAT cpapcity	R5712	VICTL(V)	ICHG(A)
2000mAH	41.2K	1.8976	1.39
2200mAH	52.3K	2.0989	1.537
2400mAH	66.5K	2.2918	1.679
2600mAH	86.6K	2.4871	1.822

Vref = 4.096V
VLDO = 5.4V

Vbatt = Cell * { 4V +[0.4 X (VCTL/REFIN)] }
VCTL= LDO
=> Vbatt = 4.2V X CELLS

Vf=0.37(max & If=1mA)

VICTL= 2.269V

14.16V

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A

CHG_EN#	AC_APR_UC	SWITCH
H	H	OFF
H	L	ON
L	H	ON
L	L	ON

CELL pin : (trie to REFIN pin) ----> 4 Cells
(floating) ----> 3 Cells

3S2P/3P/4P

POWER_LIMIT CIRCUIT

VICHG=ICHG x RS x G x R-->58W

PRE_CHARGE CIRCUIT
Pre-charge voltage 10V@3S

Vref = 1.25V

Vf=0.41Vmax / If=0.5A

ER

Title : POWER_CHARGER			
<OrgName>	Engineer:		
Size: C	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 57 of 69		

Title : POWER_PIC

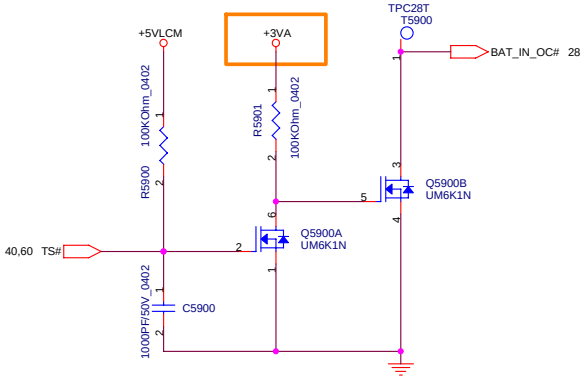
<OrgName>

Engineer:

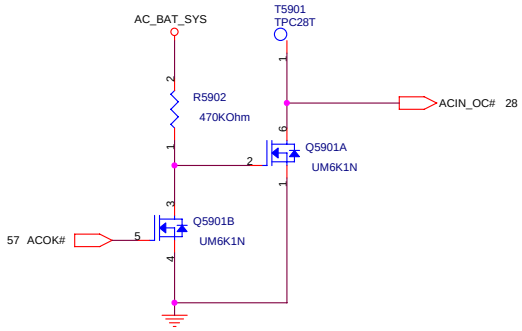
Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 58 of 69

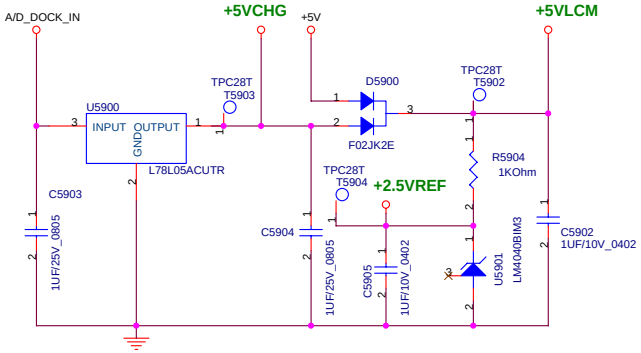
BATTERY IN DETECT



ADAPTER IN DETECT

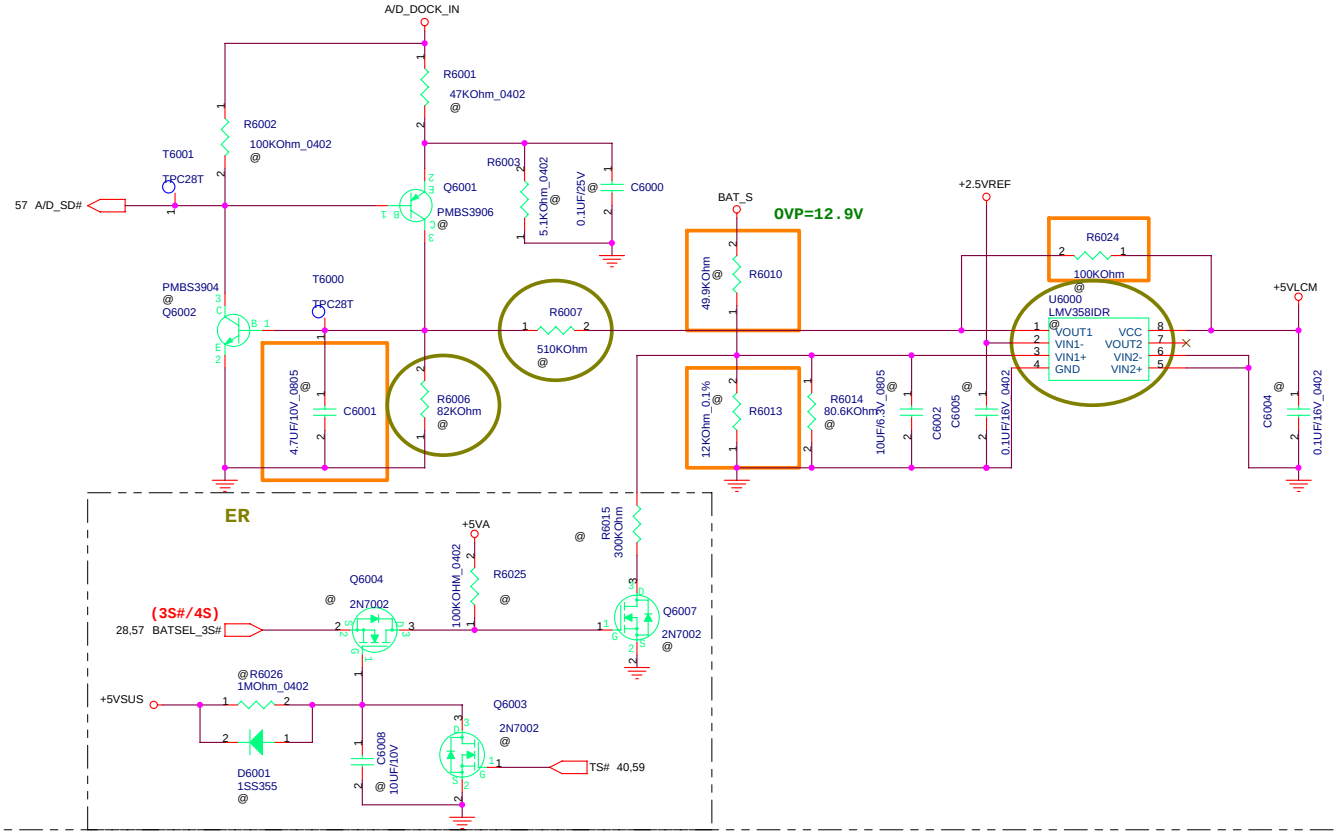


+5VLCM, +5VCHG & +2.5VREF

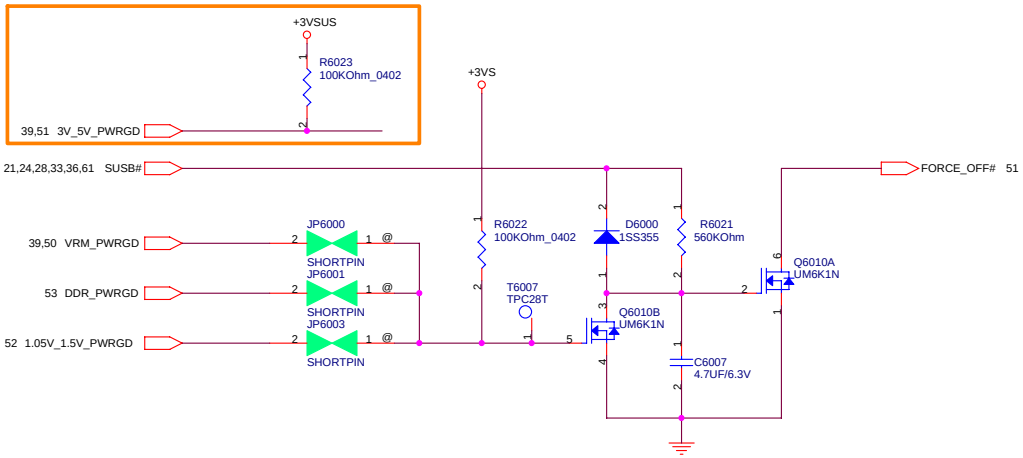


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 59 of 69	

BATTERY A/D_SD# (OVP)



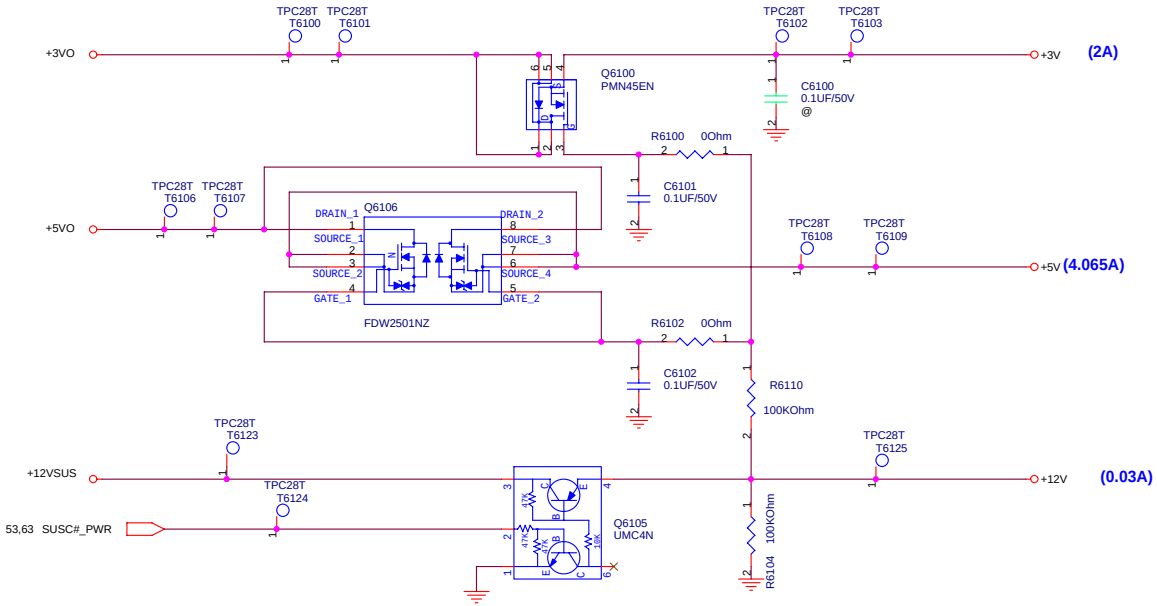
POWER GOOD DETECTER

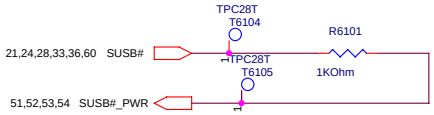


TPC28T T6003 — VRM_PWRGD
TPC28T T6004 — DDR_PWRGD
TPC28T T6005 — 3V_5V_PWRGD
TPC28T T6006 — 1.05V_1.5V_PWRGD

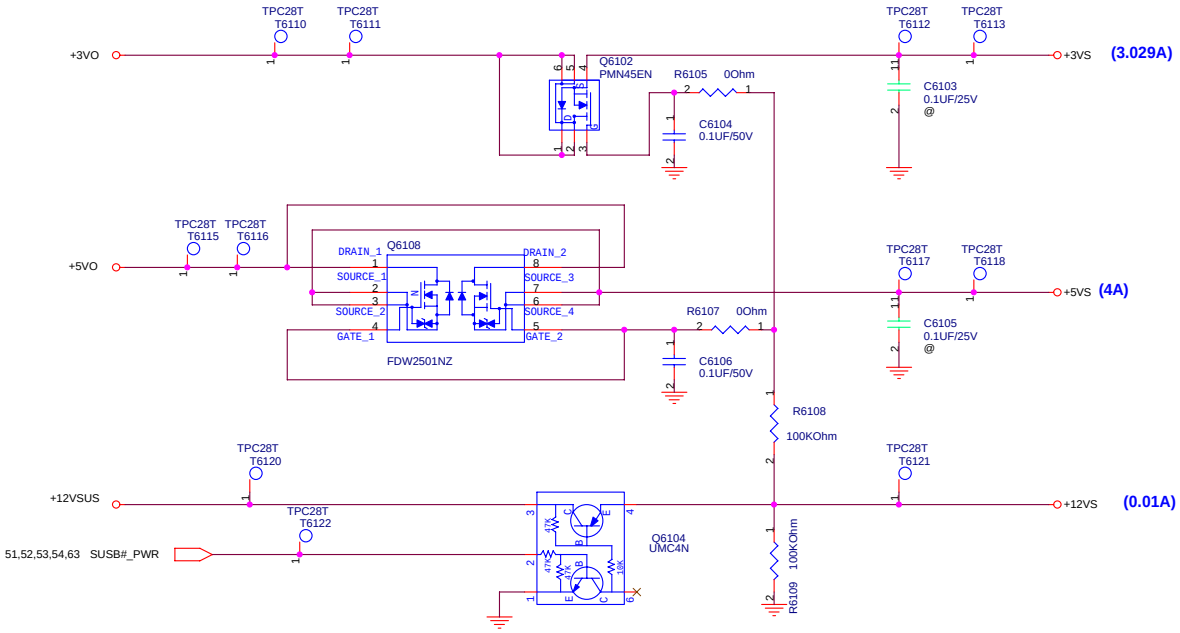
Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 60 of 69	

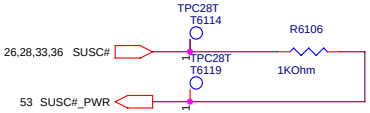
SUSC#_PWR POWER



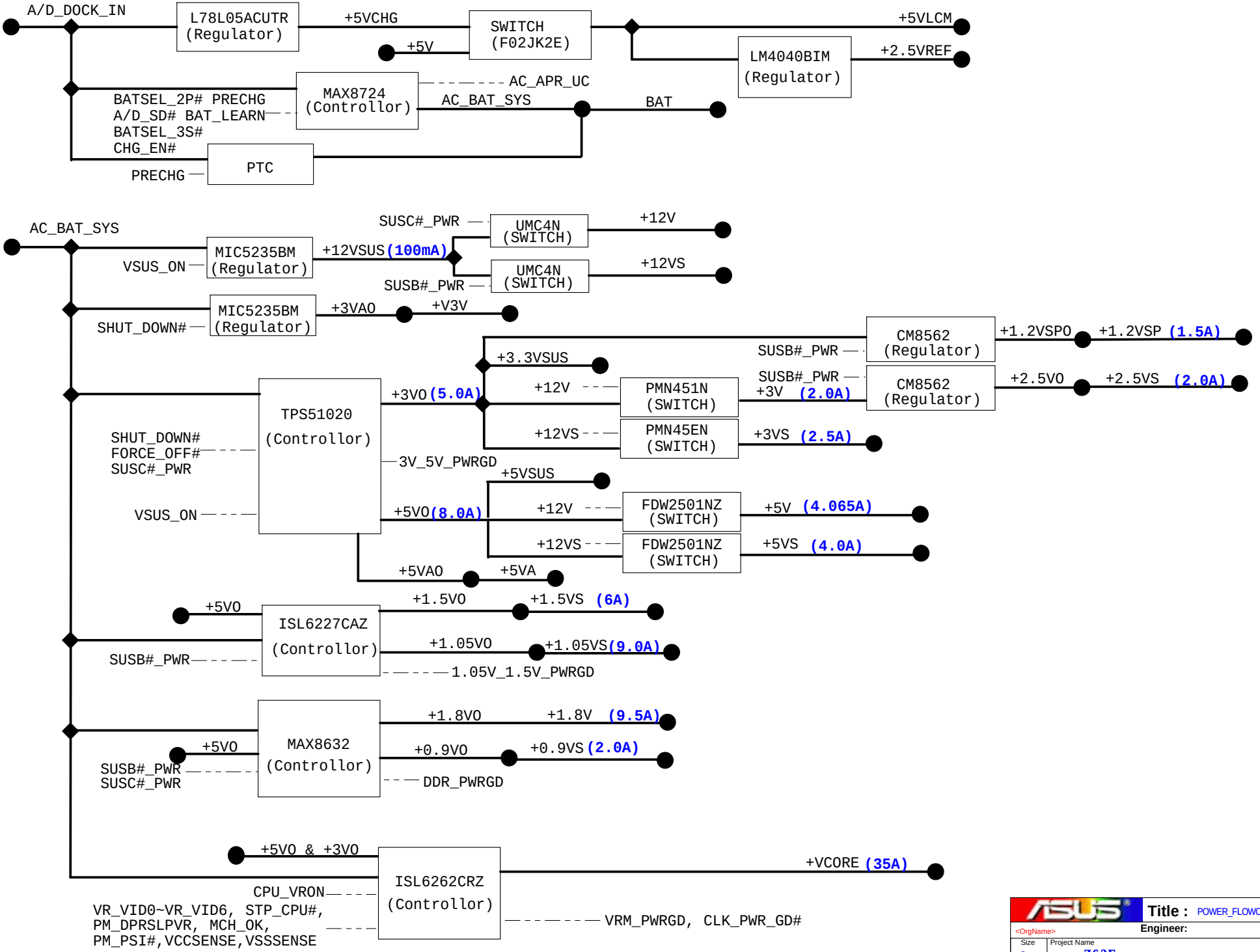


SUSB#_PWR POWER

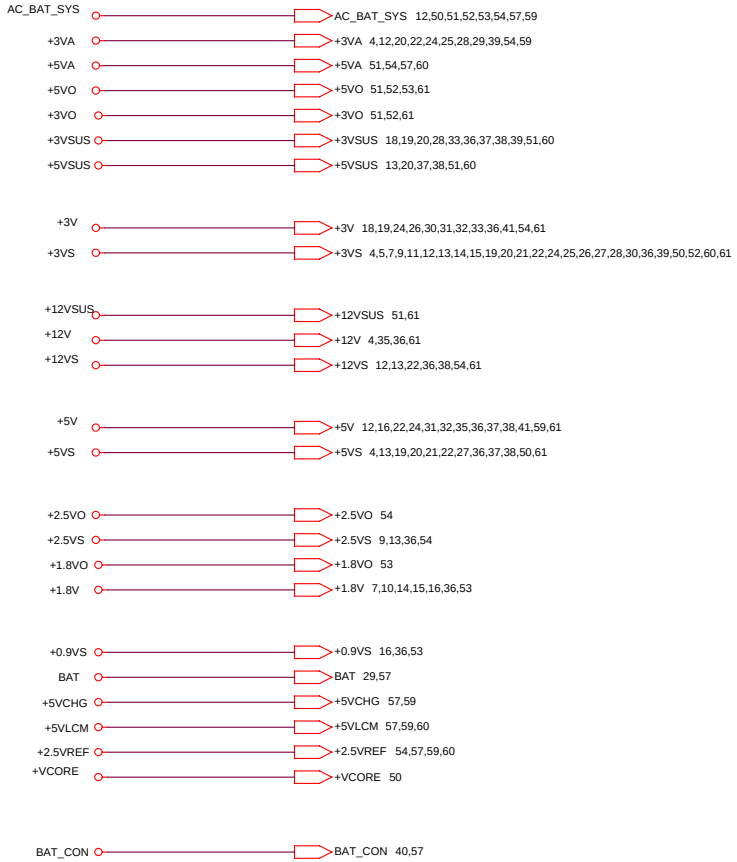




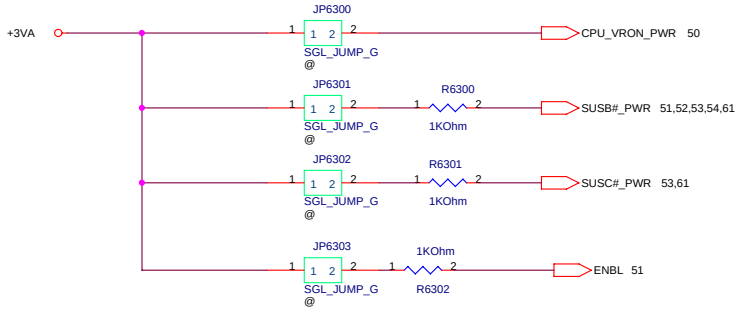
Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 61 of 69	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 62 of 69	



FOR POWER TEST



Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 63 of 69	

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date

R2.0

Item	Before	After	Reason	Owner	Date

ASUS

Title : POWER_HISTORY

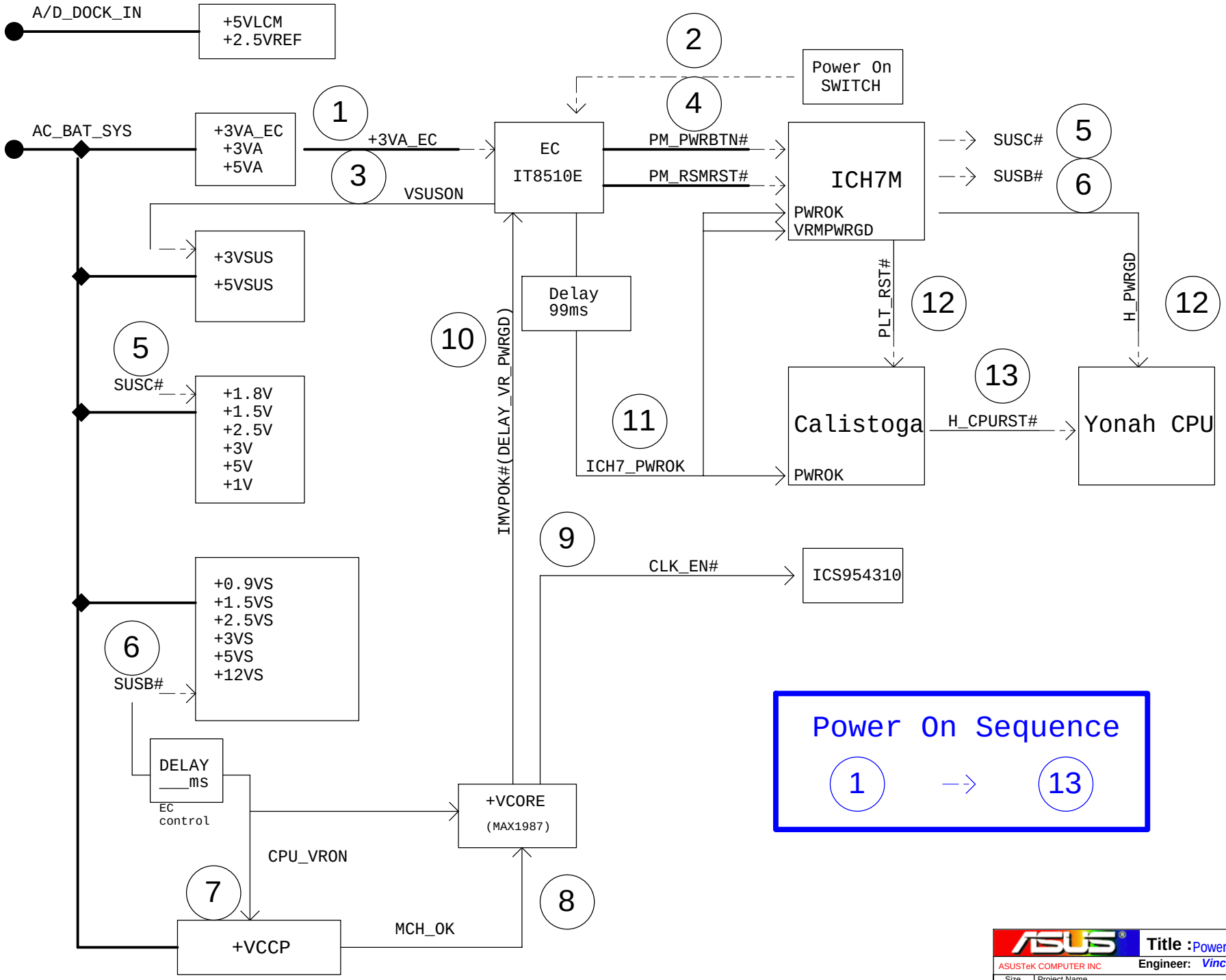
<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z62Fp	1.0

Date: Wednesday, August 23, 2006 Sheet 64 of 69

Title :	History
ASUSTek Computer INC. NB1	Engineer: *Vincent VY Huang*
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 65 of 69



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Vincent VY Huang		
Size: Custom	Project Name: Z62Fp		Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 66 of 69		

REVISION LIST

R1.0 2005/08/23

R1.1 2005/09/23

NO1 Page36 : Add R3600,R3601,Q3600 to correct Discharge circuit logic
NO2 Page4 : Unmount R28, Page28 : Delete D2801 ==>to correct VSUS_ON power sequence
NO3 Page37: Exchange SW3 and SW4 for proper click function
NO4 Page22: Change Q22 nets to correct JACK_IN# to disable internal Speaker
NO5 Page9: Change JP29 nets to increase +VCCP supply to GMCH
NO6 Page11: Set R126 to unmount component for correct strapping
NO7 Page28: Connect CHG_FULL_LED# to GPA1 for LED indication
NO8 Page28: Connect BAT1_CNT1# to GPA2 for LIBP battery control
NO9 Page28: Move BATSEL_3S# from GPI2 to GPA6 for default pull-up pin requirement
NO10 Page28: Add PWR_LMT# at GPF6 for power team requirement
NO11 Page28: Connect BAT1_CNT2# to GPI2 for LIBP battery control
NO12 Page21: Unmount R464 and Mount R463 for proper driver setting to control mute
NO13 Page37: Re-assign Launch board connector pin define for correct function button
NO14 Page42: Re-assign Launch board pin define for correct function button
NO15 Page28: Add EXPLORER# instant key due to SPEC change
NO16 Page37: Delete Q3700,R1255, Change LED5 to single color to remove charge full LED function. Connect power to +5VCHG avoid faulty GPIO control.
NO17 Page32: Add Q3200 and R3200 to invert SD_WP signal
NO18 Page22: Delete U34, and use U82 parts to instead. And also connect the power to +3VA
NO19 Page38: Delete R1258, D105 for redundant component
NO20 Page33: Connect V_DAC bias to GLAN terminator RC
NO21 Page40: Add EMI Springs x 8, Drill196 hole x 1, Stand off x1
NO22 Page4: Delete unmount component R1025, mount C46, C47, Q5, R35, U3
NO23 Page16: Delete L23, Add R1600,R1601,C1600,C1601,C1602,U1600, Reserve R1602 for bypass VREF
NO24 Page42: Delete Unmount component D7000,D7001,D7002,D7003,D7004
NO25 Page7: Add C778,C779 to stable memory VREF on GMCH side
NO26 Page20, Page2: Delete JP4, JP1
NO27 Page10 : CE15 change to 470uF low ESR cap, CE16 change to unmount component
NO28 Page28 : Change CON11 to up-contact component for ME part change.
NO29 Page26 : Change R2603,R2606 to 33 ohm 0603 part to avoid overshoot/undershoot
NO30 Page10 : Change CE51,CE52,CE53 to 470uF for height limitation by ME.
NO31 Page : Change U1, U4, U6's PCB footprint to meet Lead free BGA PAD rules
NO32 Page28 : Change U21 to 3.0V threashold reset IC for sourcer synchronize
NO33 Page14,15 : Change M_ODT[0..3]# to make correct rank ODT function
NO34 Page26 : Delete R1059,R1060,R1061,Q141,Q142,C939,C940,L93 for BT part reduce
NO35 Page27,37 : Change R342,R448,Q196 to unmount component, Add R3701 to bypass the circuits
NO36 Page39 : Change R1047,R1269 to 100K ohm to reduced power consumption
NO37 Page9 : Delete L91, Change CE50 to 10uF 0805 capacitor
NO38 Page7 : Add R703 to support C4E Fast exist latency
NO39 Page22: Change the HP mute circuits to behind decoupling capacitors
NO40 Page9: Change the CE8 to Common 330uF part use
NO41 Pag21: Add R2100,R2101,R2102,R2103 ohm resistor for EMI solution
NO42 Pag40: Add R4000,R4001 unmount part to reserve pull low
NO43 Pag17: Change X2 to ROHS compliant parts
NO44 Pag28: Change X4 to ROHS compliant parts
NO45 Pag35: Delete D37,D38,D39,D40,D41,D42,D43,D44 for Moat fine tune requested by EMI
NO46 Pag5: Change R70,R77,R79,R83 to 39ohm for fine tune clocks
NO47 Pag28: Delete JP7 and short +3VA_EC to +3VA
NO48 Pag40: Delete H41, H47 to sync ME drawing
NO49 Pag22: Change J2 connector by ID/ME's request

R2.0 2005/11/29

NO1 Page38 : R818 pin1 connect to +3VSUS to solve S4 WOL fail issue
Page13 : U80 pin16 connect to +5VSUS to solve S4 WOL fail issue
NO2 Page39 : Delete Q135, R1051, R1054, D82, D84, C934 for reduce component
NO3 Page19 : R156 pin1 change to +3V to meet Check list
NO4 Page37 : R3700 and LED5 change to connect +5VSUS to solve Battery low blinking indication no function issue.
NO5 Page28,37,42 : Delete EXPLORER# key and add back P4G instant key for PM's request
NO6 Page24 : Change TPM's power supply to +3V to avoid S5 leakage current
NO7 Page2, 28 : Add Q200 to support THRO_CPU function on to PROCHOT#.
NO8 Page22 : Add R2201, R2202 to reserve set high gain of AMP
NO9 Page23 : Change C2305 to 1uF for cutoff frequency fine tune
NO10 Reduce 0ohm resister=>R703, R1263, R195, R1900, R1901, R2000, R462, R469, R458, R2800, R347, R349, R387, R391, R1293, R3900, R3901
NO11 Page40 : Change U4004,U4005,U4006,U4007 and add U4008 and U4009 to match EMI Spring modify requirement
NO12 Page9: Add C956, C957, C958, C959 for EMI's request
NO13 Page7: Set R108 to unmount component
Page28: Set D2800 to unmount component

R2.1 2005/12/20

NO1 Page40 : Mount R4000 and R4001 to make CNT1 and CNT2 have pull down source
NO2 Page32 : Delete R3200 and Q3200 for SD_WP proper functionality
NO3 Page27 : Disconnect CON10's pin53 and pin54 from GND connection(NPTH)
NO4 Page36 : Change R3600 and R3601 to 100Kohm for power saving
NO5 Page28 : Disconnect RN25 part A & B for internal Pull up enabled and Add TP2804,TP2805
NO6 Page33 : Remove V_DAC connection of termination resistor
Page34 : Change Ethernet Switch connection to behind Transformer
Page38 : Change Ethernet Switch connection to behind Transformer
NO7 Page34 : Swap RN45's Pin 1 and Pin3 for layout
NO8 Page28 : Add C2800~2823 for EMI solution
NO9 Page40 : Change J5 connector requested by power team for burning issue.
NO10 Page22 : Change U82 to 06G004267010 to avoid use IBM's specified material.

R2.2 2006/01/16

NO1 Page33 : Recover V_DAC connection of termination resistor
Page34 : Change Ethernet Switch connection to before Transformer
Page38 : Change Ethernet Switch connection to before Transformer
NO2 Page17 : Add R1700~R1704 for EMI reserve
NO3 Page22 : Change R265,R266 to 30Kohm to meet Speaker's SPEC

Z62FP 2006/02/21

NO1
Page28: Delete R353,R355
Page28: Change CON11 to Intel CBB keyboard

NO2
Page32: Add U3200,U3201 to isolate 3 in 1 card signals

NO3
Page22: Delete CN1, instead by C2201~C2204

NO4
Page12,35: Delete Colay component: L1203, L46, L49, L51, L53

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1
MINIPCI(TV)	PCI_REQ#0

IDSEL

MINIPCI	PCI_AD19
CB&1394	PCI_AD17
10/100	PCI_AD16
MINIPCI(TV)	PCI_AD18

ASUSTeK COMPUTER INC
Title : Revision List
Engineer: Vincent VY Huang
Size: Custom | Project Name: Z62Fp | Rev: 1.0
Date: Wednesday, August 23, 2006 | Sheet 67 of 69

REVISION LIST

R2.0 2006/03/29

- NO5 Page35 : Add JP3500 for Cost down USB power swtich
- NO6 Page22 : Change R1267, R1268 to 22ohm to avoid micro sound
- NO7 Page16 : Change C1600, U1600 to unmount component, R1602 to mounted component
- NO8 Page32 : Add RN3200, RN3201 to 1394 co-lay and set L42 to unmount component
- NO9 Page3 : Cost down 22uF to 10uF MLCCs, unmount CE1, CE4
  CE54 change to use 100uF
- NO10 Page9 : Unmount CE8 for cost down
- NO11 Page10 : Change CE15, CE16, CE51, CE52, CE53 to 100uF for cost down
- NO12 Page20 : Unmount CE19, Change CE20 to 100uF for cost down
- NO13 Page26 : Unmount CE2601 for cost down
- NO14 Page22 : Mount C1074 to enhance ESD protection
- NO15 Page : Change Jumpers symbol which have 潤濕點
- NO16 Page17: Change R1700, R1701, R1702, R1703, R1704 component size 0402 to 0603
- NO16 Page35: Change Q47 component optional "/x"

ASUSTeK COMPUTER INC	Title : Revision List	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 68 of 69	

REVISION LIST

R2.1 2006/07/19 (for vista)

NO1 Page21 : Add C2101,C2102,C2103
Add R2124,R2125,R2127,R2129,R2130,R2132,R2133
Add Q2100(Q2100A,Q2100B),Q2101(Q2101A,Q2101B)
Change R474,R475 (2.2KOhm) to (2.49KOhm)
Add R2126,R2131 (unmount)
for Vista Jack sense feature

NO2 Page22 : Add Dual-lay mount CE7000,CE7001(CE21,CE22 unmount) Meet Vista Audio Bandwidth requirement
Change MIC JACK J2 (12G14030105N to 12G14030106L)
Add R2203,L7000
Add D7000,D7001,C7370 (unmount)
Move location to bottom side L35,C2200 (original top side)

NO3 Page23 : Move location to top side L2200 (original bottom side)

NO4 Page37 : Move location to bottom side D106 (original top side--unmount)

NO5 Page50 : Add C5030,C5031,R5057,R5058(Power circuit--unmount) For EMI solution

NO5 Page57 : Rotate R5704 90-degree(Power circuit) Avoid assembly short problem

Z62FM R2.0 2006/08/16

ER NO1: Page22 mute circuits inverted for vista default driver (Add Q2200)

ER NO2: Page22 solve external pop noise, +12VS delay, add C2205 and D2200, and change R270 to 1M ohm

ER NO3: Page35, solve external USB power leakage (Add Q47 mount)
JP3500 (unmount) change to R3400 (unmount)

ER NO4: Page22 solve internal pop noise, Change R271 to 470K Ohm, Add C2206=2.2uF

ASUSTeK COMPUTER INC	Title : Revision List	
	Engineer: Vincent VY Huang	
Size: Custom	Project Name: Z62Fp	Rev: 1.0
Date: Wednesday, August 23, 2006	Sheet 69 of 69	