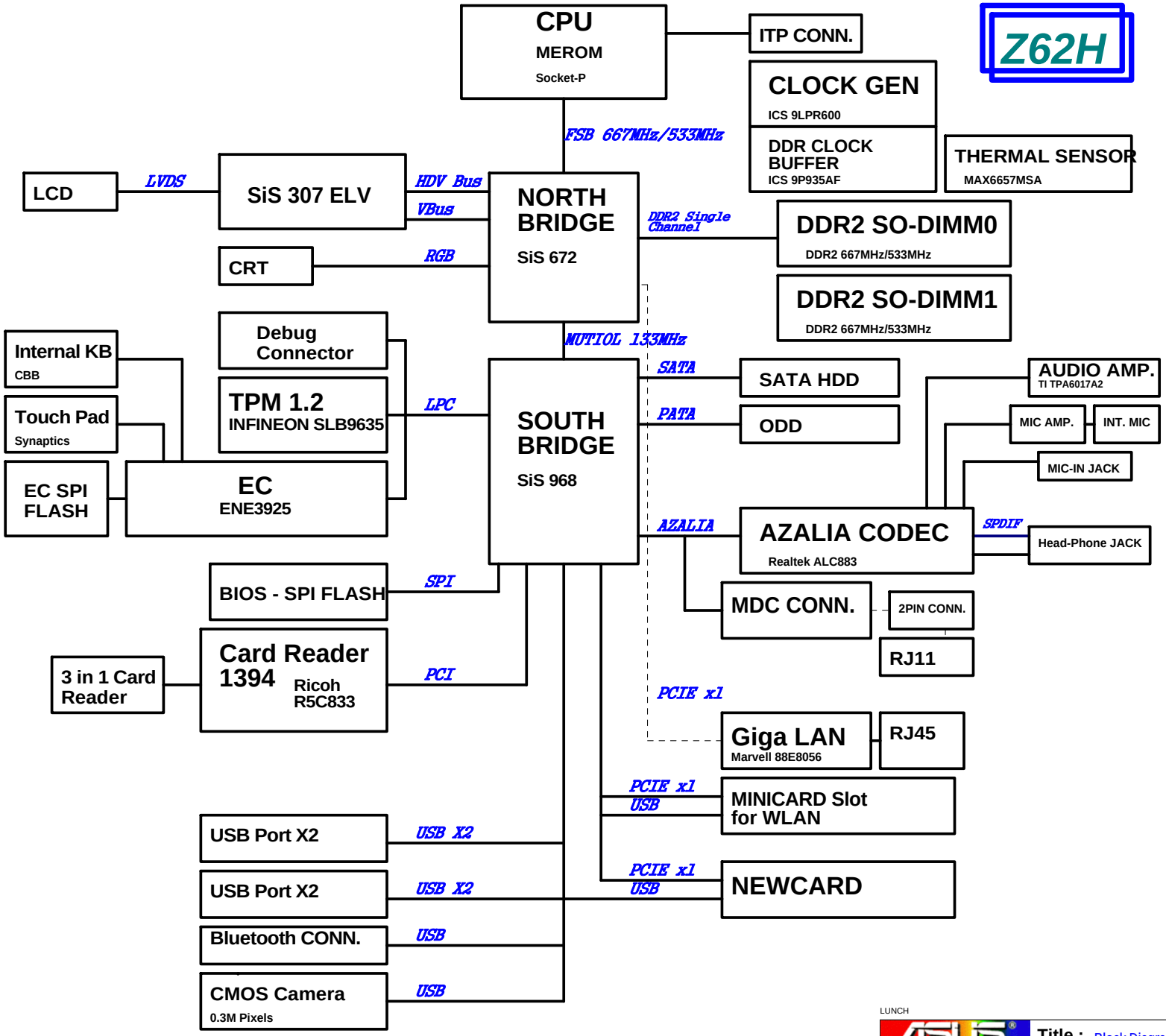


LUNCH

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 1 of 63	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

LUNCH

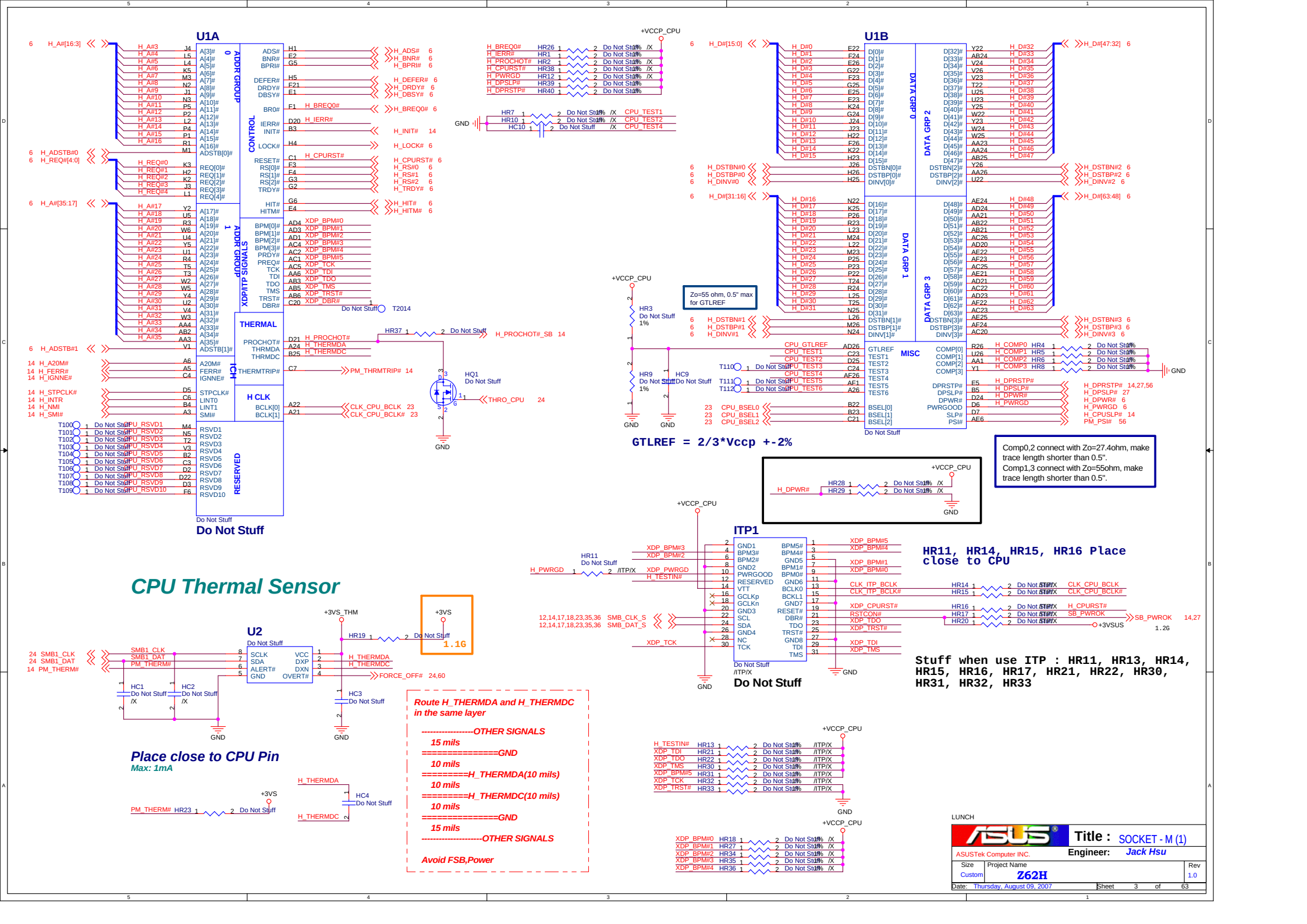
ASUSTek Computer INC.

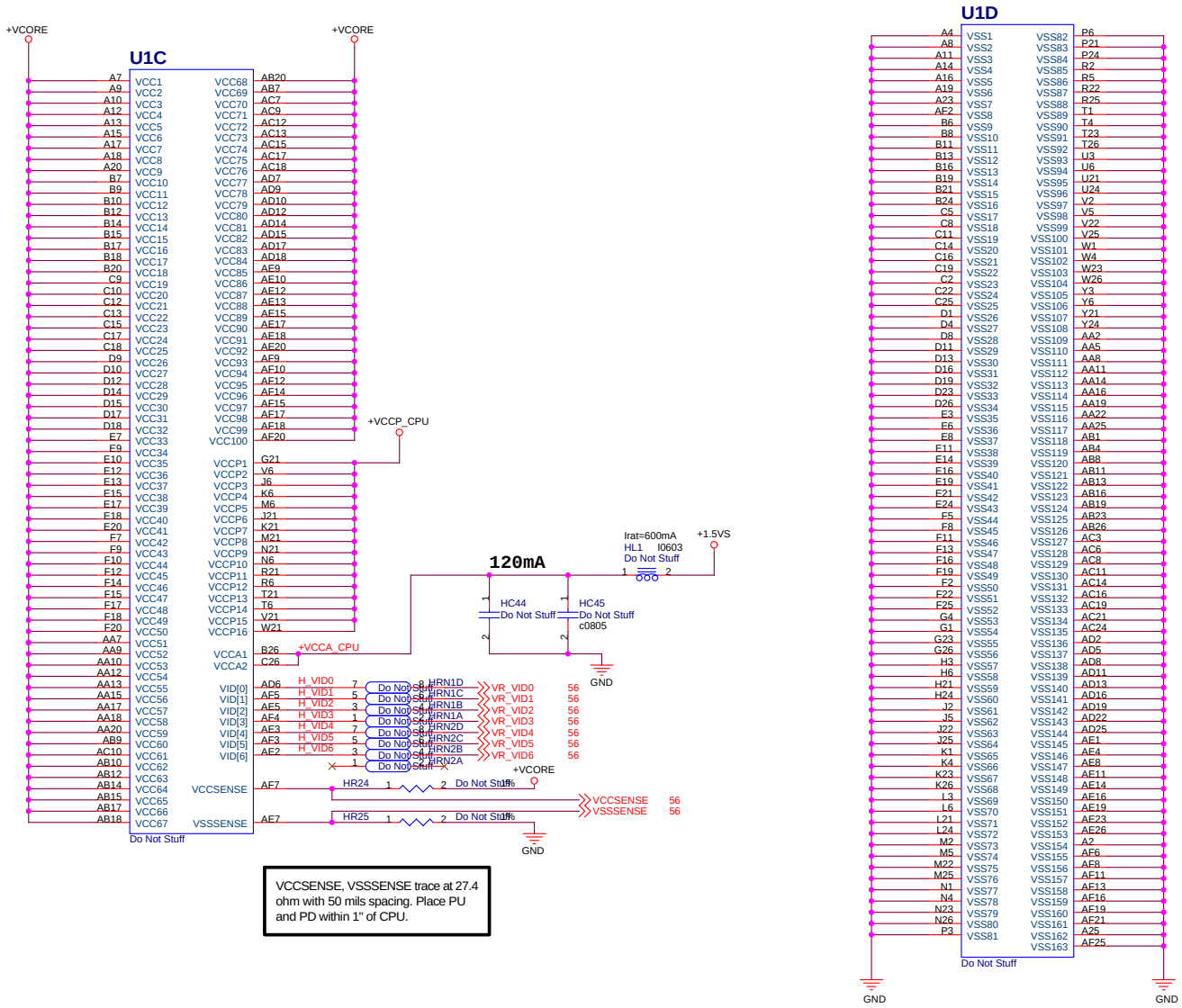
Title : System Setting

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 2 of 63

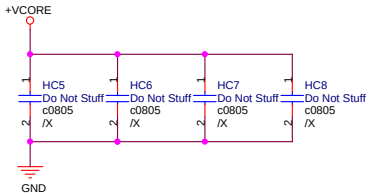

U1A
U1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Do Not Stuff
GTLREF = 2/3*Vccp +-2%
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5".
CPU Thermal Sensor
U2
ITP1
HR11, HR14, HR15, HR16 Place close to CPU
Stuff when use ITP : HR11, HR13, HR14, HR15, HR16, HR17, HR21, HR22, HR30, HR31, HR32, HR33
Place close to CPU Pin
Max: 1mA
Route H_THERMDA and H_THERMDC in the same layer
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS
Avoid FSB,Power
LUNCH
Title : SOCKET - M (1)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size: Custom
Project Name: Z62H
Rev: 1.0
Date: Thursday, August 09, 2007
Sheet 3 of 63

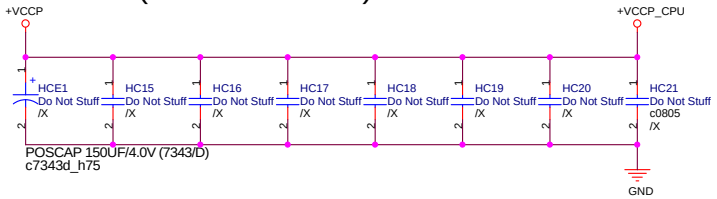


LUNCH

ASUSTek Computer INC.	Title : SOCKET - M (2)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 4 of 63	

+VCCP Decoupling Capacitor (Place near CPU)





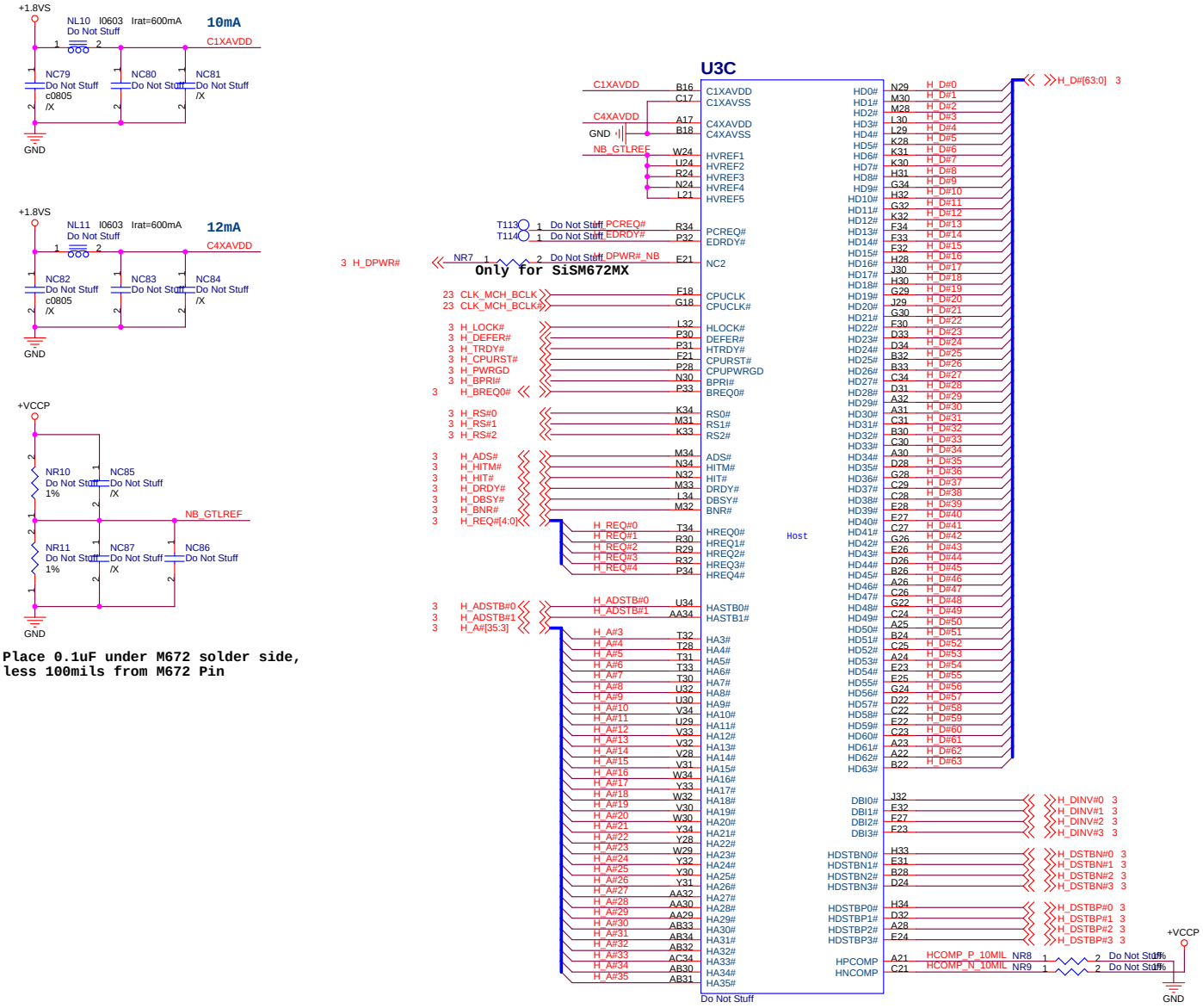
Non-Stuff

Decoupling guide from INTEL
44A for Merom

VCORE 22uF/10V * 32pcs, 330uF/2V * 6pcs
VCCP 0.1uF * 6pcs, 150uF * 1pcs

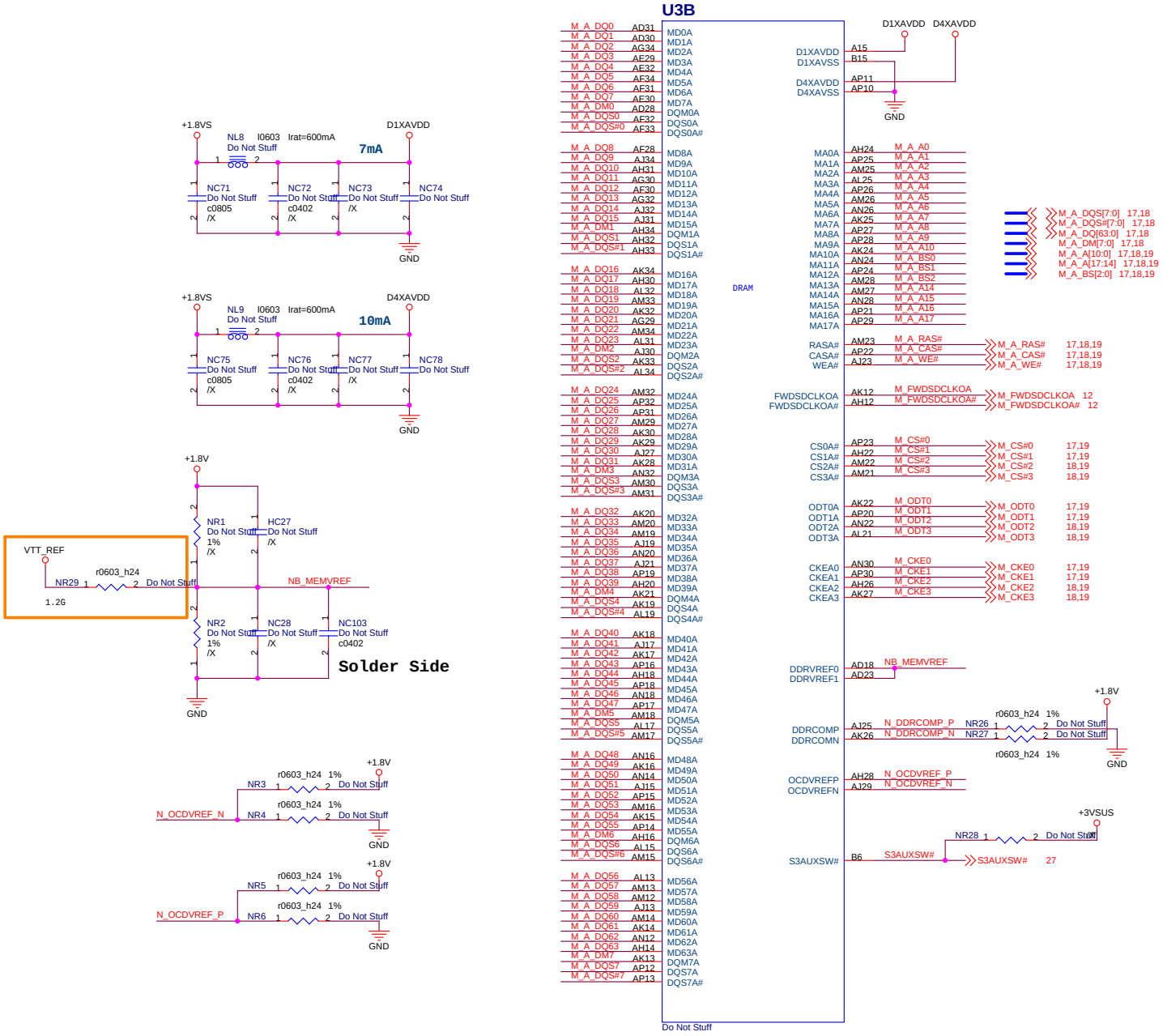
LUNCH

ASUSTek Computer INC.	Title : CPU CAP	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 5 of 63	



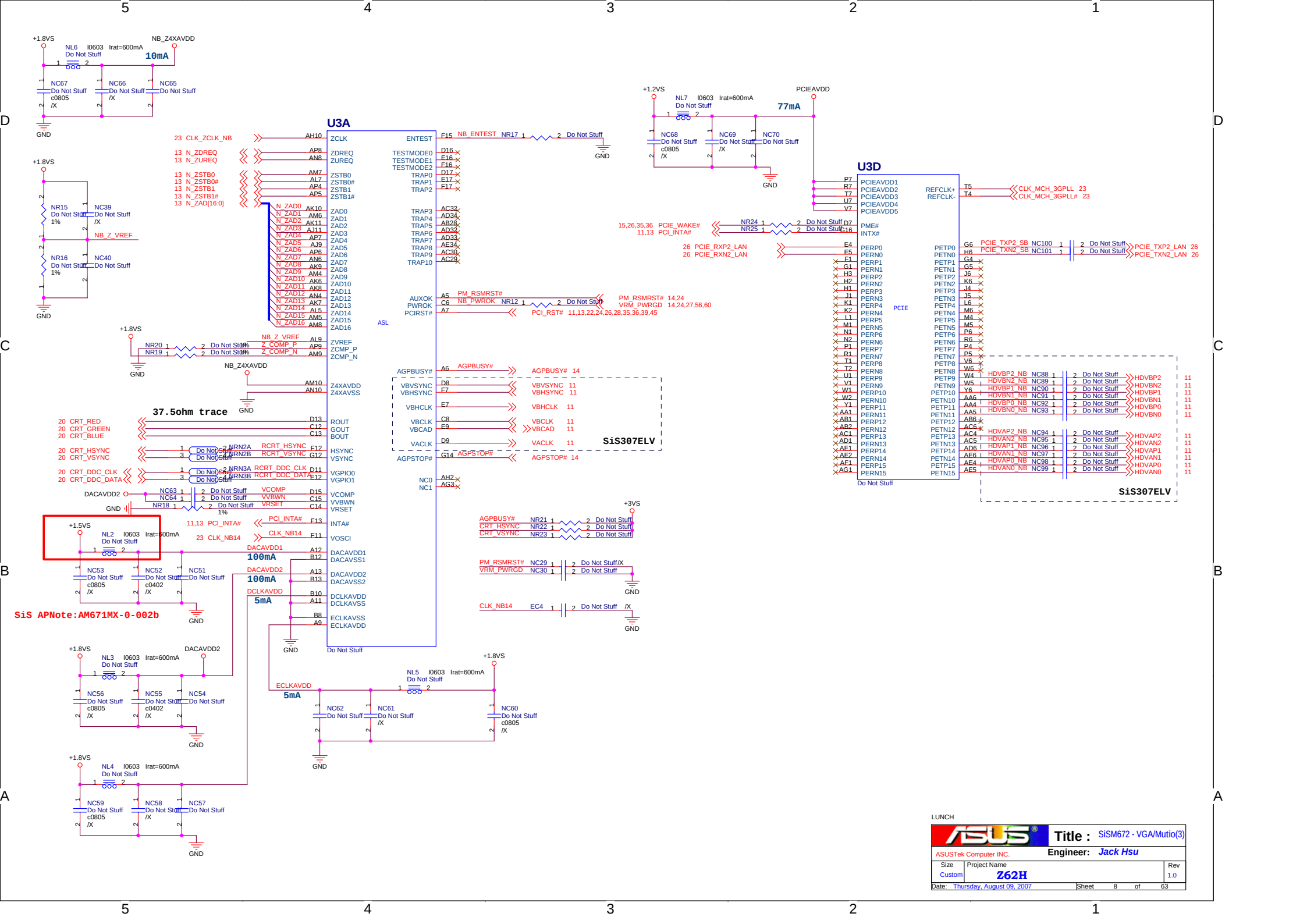
LUNCH

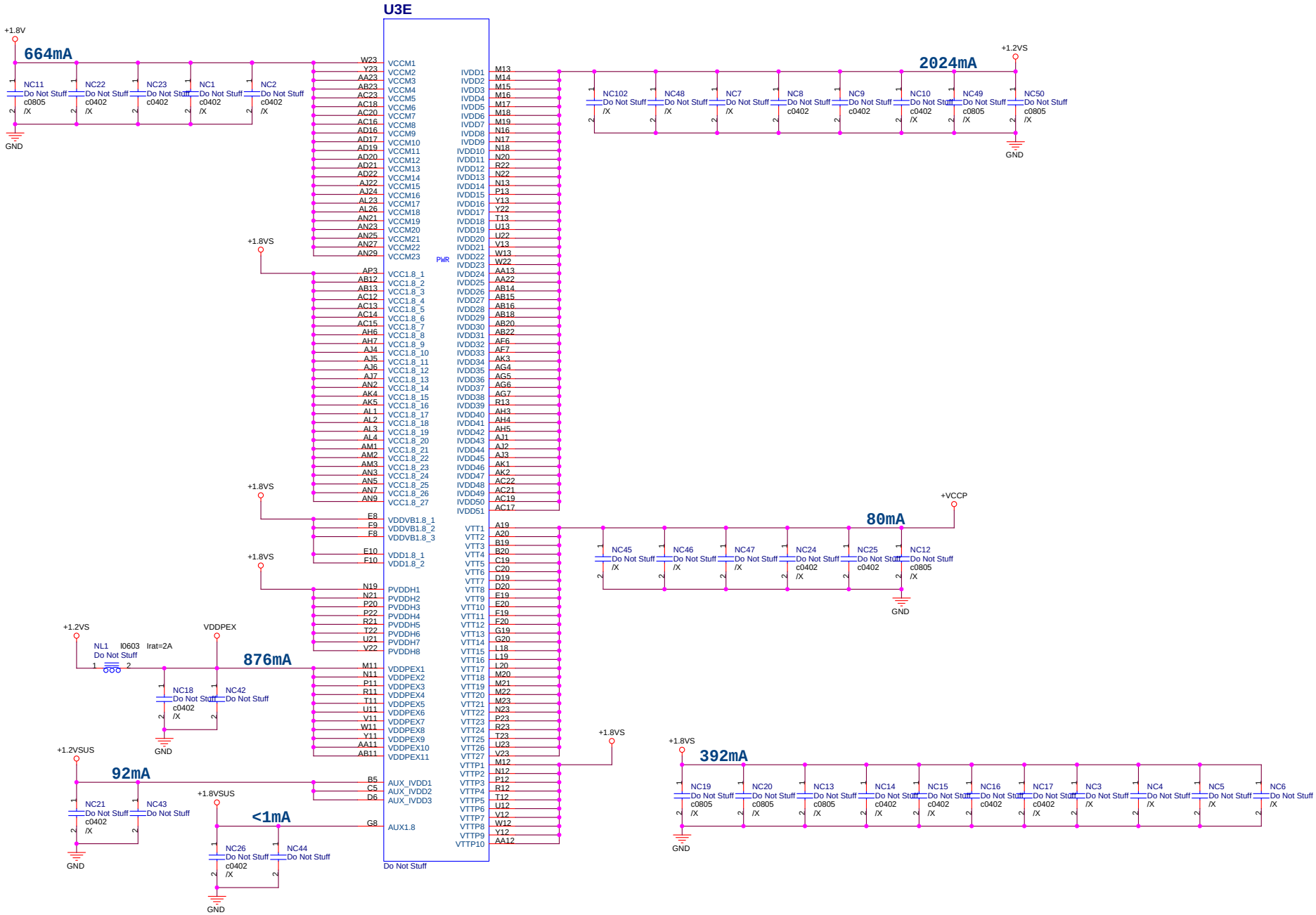
ASUSTek Computer INC.	Title : SiSM672 - HOST(1)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 6 of 63	



LUNCH

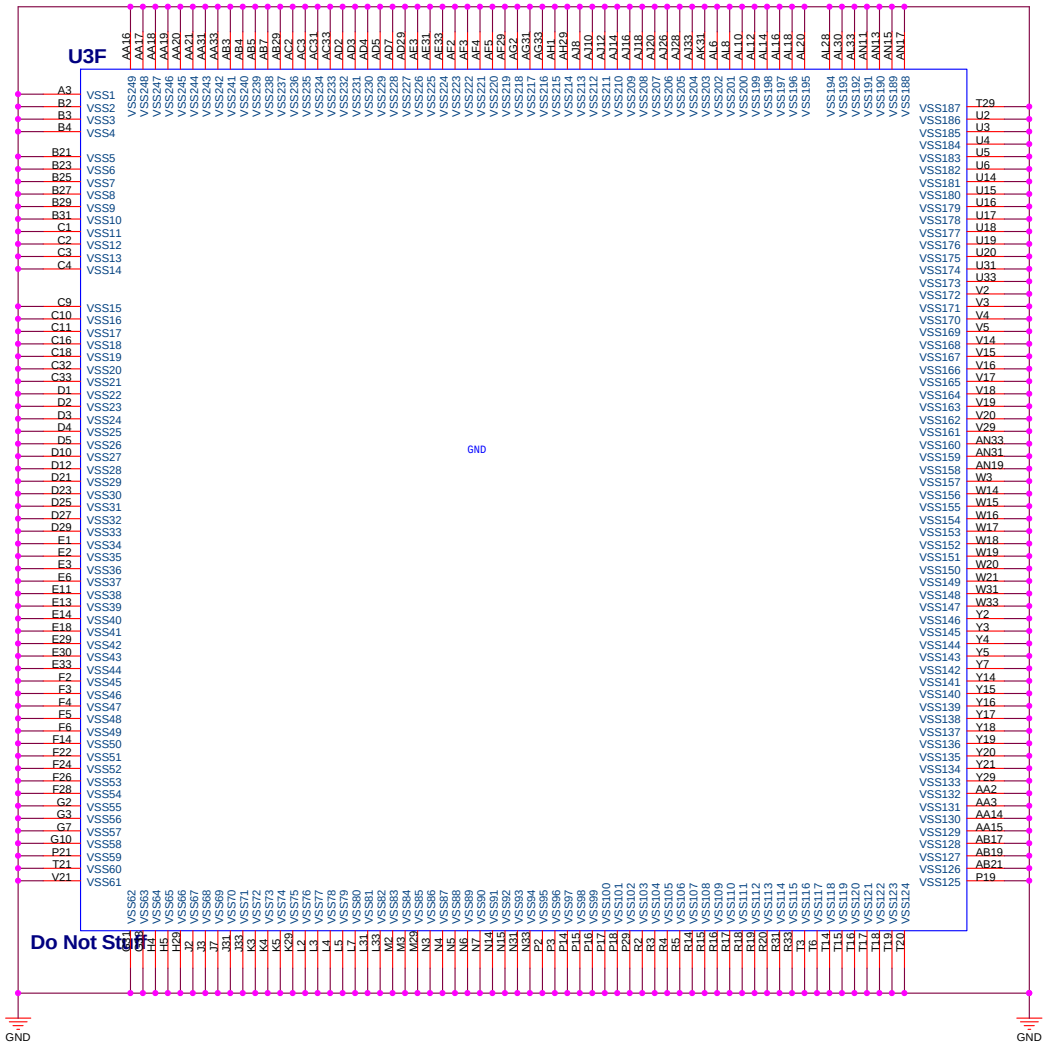
ASUSTek Computer INC.	Title : SiSM672 - DDR2(2)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 7 of 63	


U3A
U3D
SiS307ELV
SiS307ELV
37.5ohm trace
SiS APNote:AM671MX-0-002b
10mA
77mA
100mA
100mA
5mA
5mA
LUNCH
Title : SiSM672 - VGA/Mutio(3)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 8 of 63



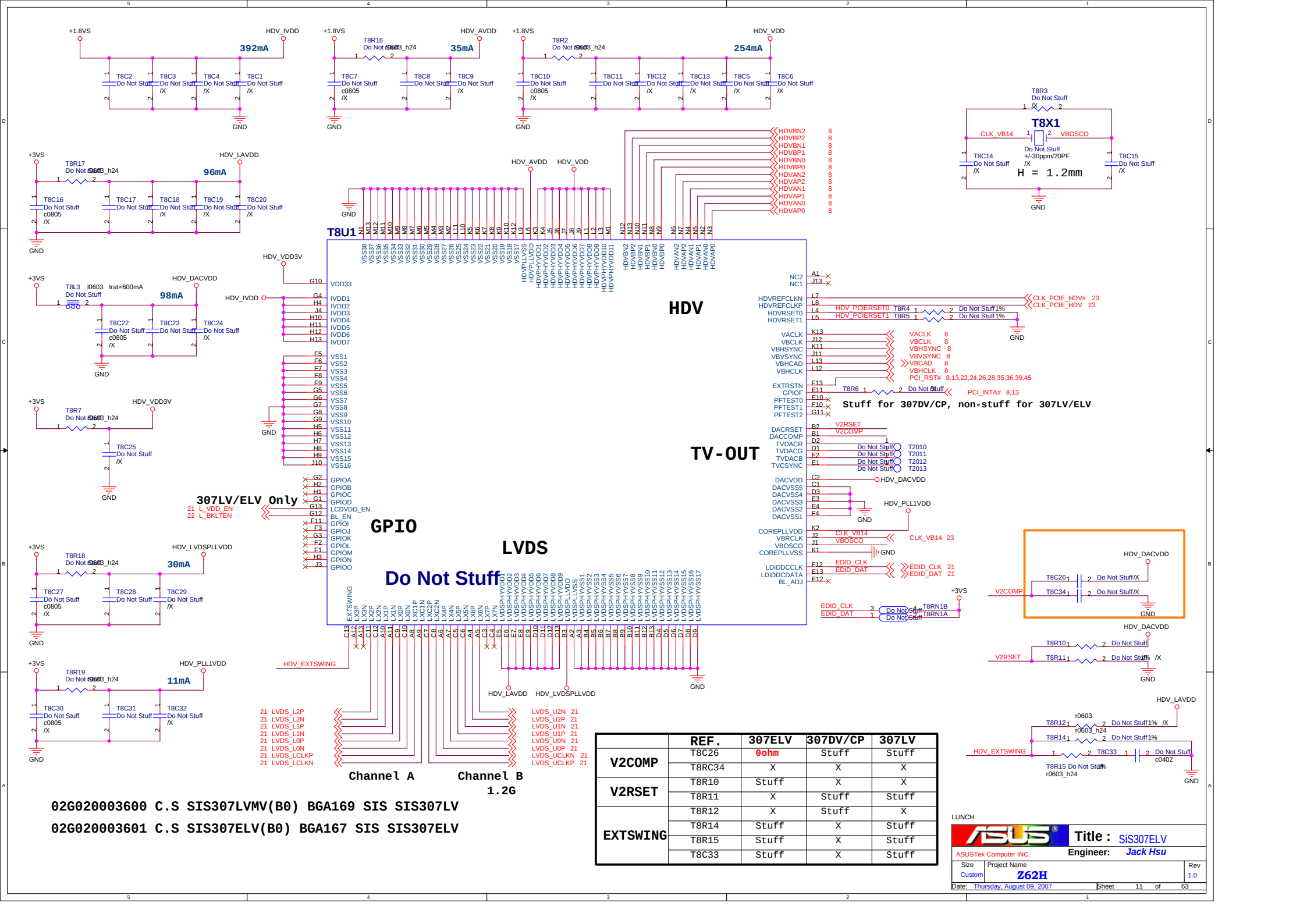
LUNCH

ASUSTek Computer INC.	Title : SiSM672 - POWER(4)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 9 of 63	



LUNCH

ASUSTek Computer INC.	Title : SiSM672 - GND(5)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 10 of 63	



	REF.	307ELV	307DV/CP	307LV
V2COMP	T8C26	0ohm	Stuff	Stuff
	T8RC34	X	X	X
V2RSET	T8R10	Stuff	X	X
	T8R11	X	Stuff	Stuff
EXTSWING	T8R12	X	Stuff	X
	T8R14	Stuff	X	Stuff
	T8R15	Stuff	X	Stuff
	T8C33	Stuff	X	Stuff

02G020003600 C.S SIS307LVMV(B0) BGA169 SIS SIS307LV

02G020003601 C.S SIS307ELV(B0) BGA167 SIS SIS307ELV

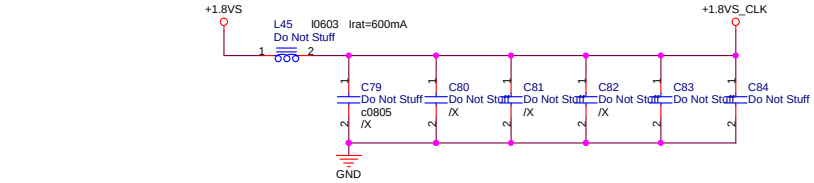
LUNCH

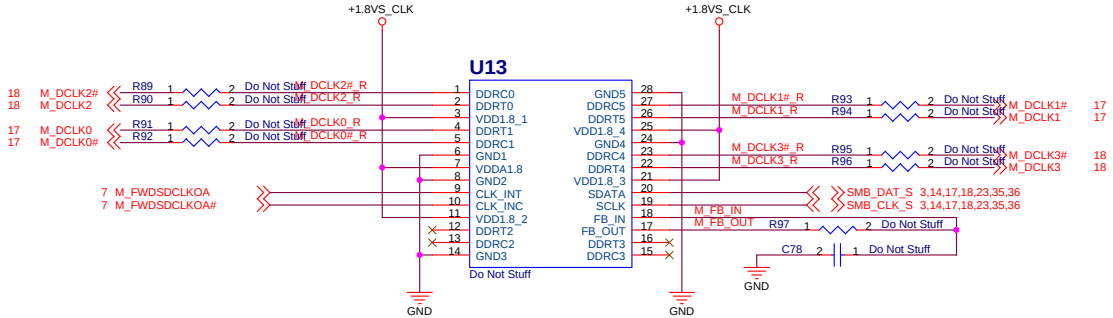
Title : SiS307ELV

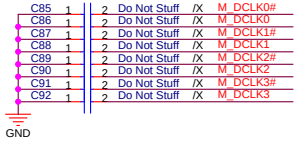
ASUSTek Computer INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 11 of 63

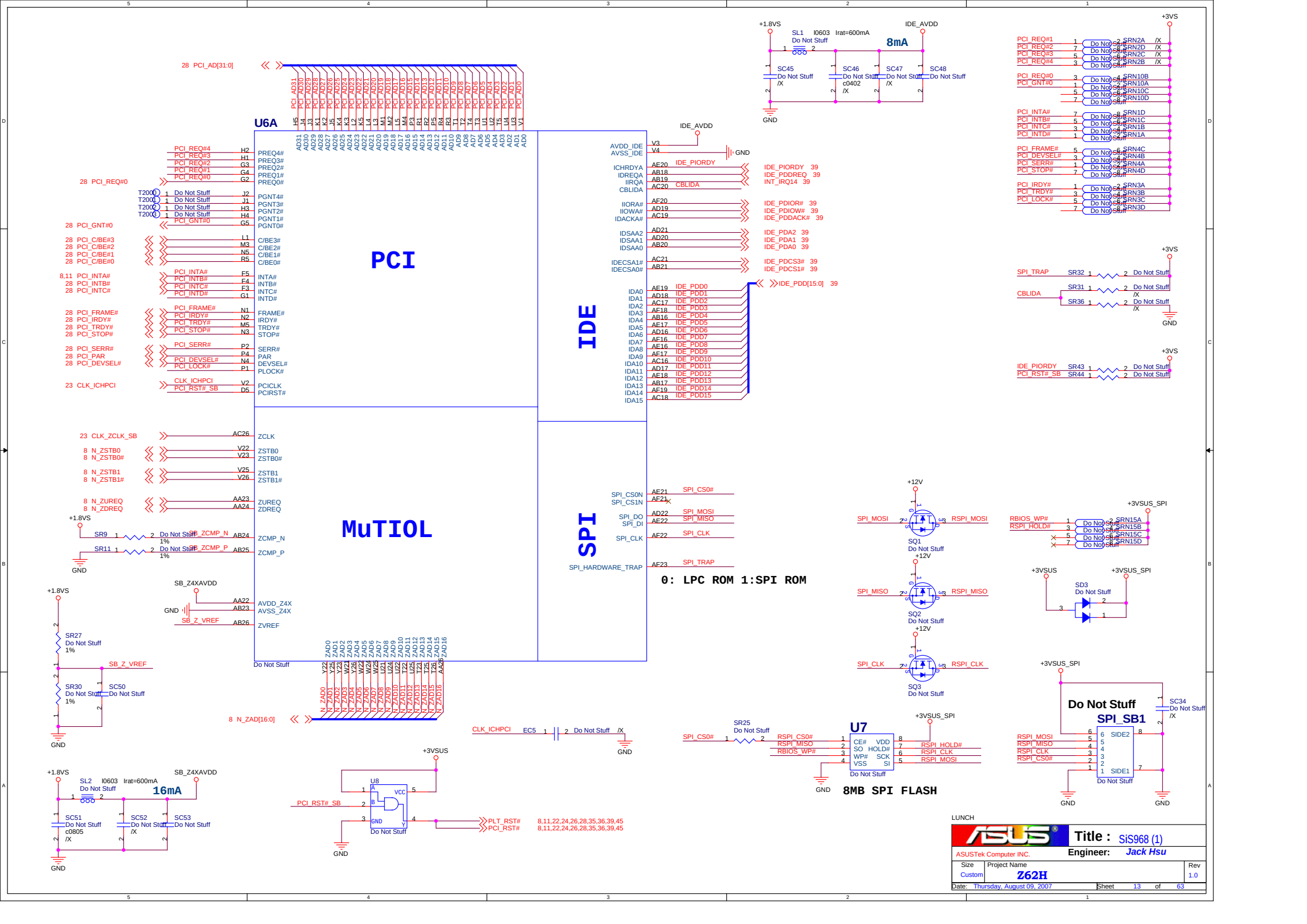






LUNCH

ASUSTek Computer INC.	Title : DDR2 CLOCK BUFFER	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 12 of 63	


U6A
PCI
IDE
SPI
MuTIOL
28 PCI_AD[31:0]
PCI_REQ#4
PCI_REQ#3
PCI_REQ#2
PCI_REQ#1
PCI_REQ#0
28 PCI_REQ#0
PCI_GNT#0
28 PCI_GNT#0
28 PCI_C/BE#3
28 PCI_C/BE#2
28 PCI_C/BE#1
28 PCI_C/BE#0
8,11 PCI_INTA#
28 PCI_INTB#
28 PCI_INTC#
PCI_INTD#
28 PCI_FRAME#
28 PCI_IRDY#
28 PCI_TRDY#
28 PCI_STOP#
28 PCI_SERR#
28 PCI_PAR
28 PCI_DEVSEL#
PCI_LOCK#
23 CLK_ICHPCI
PCI_RST#_SB
IDE_AVDD
IDE_PIORDY 39
IDE_PDDREQ 39
INT_IRQ14 39
IDE_PDIOR# 39
IDE_PDIOW# 39
IDE_PDDACK# 39
IDE_PDA2 39
IDE_PDA1 39
IDE_PDA0 39
IDE_PDCS3# 39
IDE_PDCS1# 39
IDE_PDD[15:0] 39
23 CLK_ZCLK_SB
8 N_ZSTB0
8 N_ZSTB0#
8 N_ZSTB1
8 N_ZSTB1#
8 N_ZUREQ
8 N_ZDREQ
SB_ZCMP_N
SB_ZCMP_P
SB_Z4XAVDD
SB_Z_VREF
Do Not Stuff
8 N_ZAD[16:0]
SPI_CS0#
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_TRAP
SPI_HARDWARE_TRAP
0: LPC ROM 1:SPI ROM
+1.8VS
+3VS
+3VSUS
+3VSUS_SPI
+12V
GND
SL1 l0603 Irat=600mA
8mA
SL2 l0603 Irat=600mA
16mA
IDE_AVDD
SC45 SC46 SC47 SC48
SR9 SR11 SR27 SR30 SR25
SC50 SC51 SC52 SC53
SC34 EC5
SQ1 SQ2 SQ3
SD3
U7
8MB SPI FLASH
U8
SPI_SB1
SRN2A SRN2D SRN2C SRN2B
SRN10B SRN10A SRN10C SRN10D
SRN1D SRN1C SRN1B SRN1A
SRN4C SRN4B SRN4A SRN4D
SRN3A SRN3B SRN3C SRN3D
SR32 SR31 SR36
SR43 SR44
SRN15A SRN15B SRN15C SRN15D
PLT_RST# 8,11,22,24,26,28,35,36,39,45
PCI_RST# 8,11,22,24,26,28,35,36,39,45
LUNCH
Title : SiS968 (1)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
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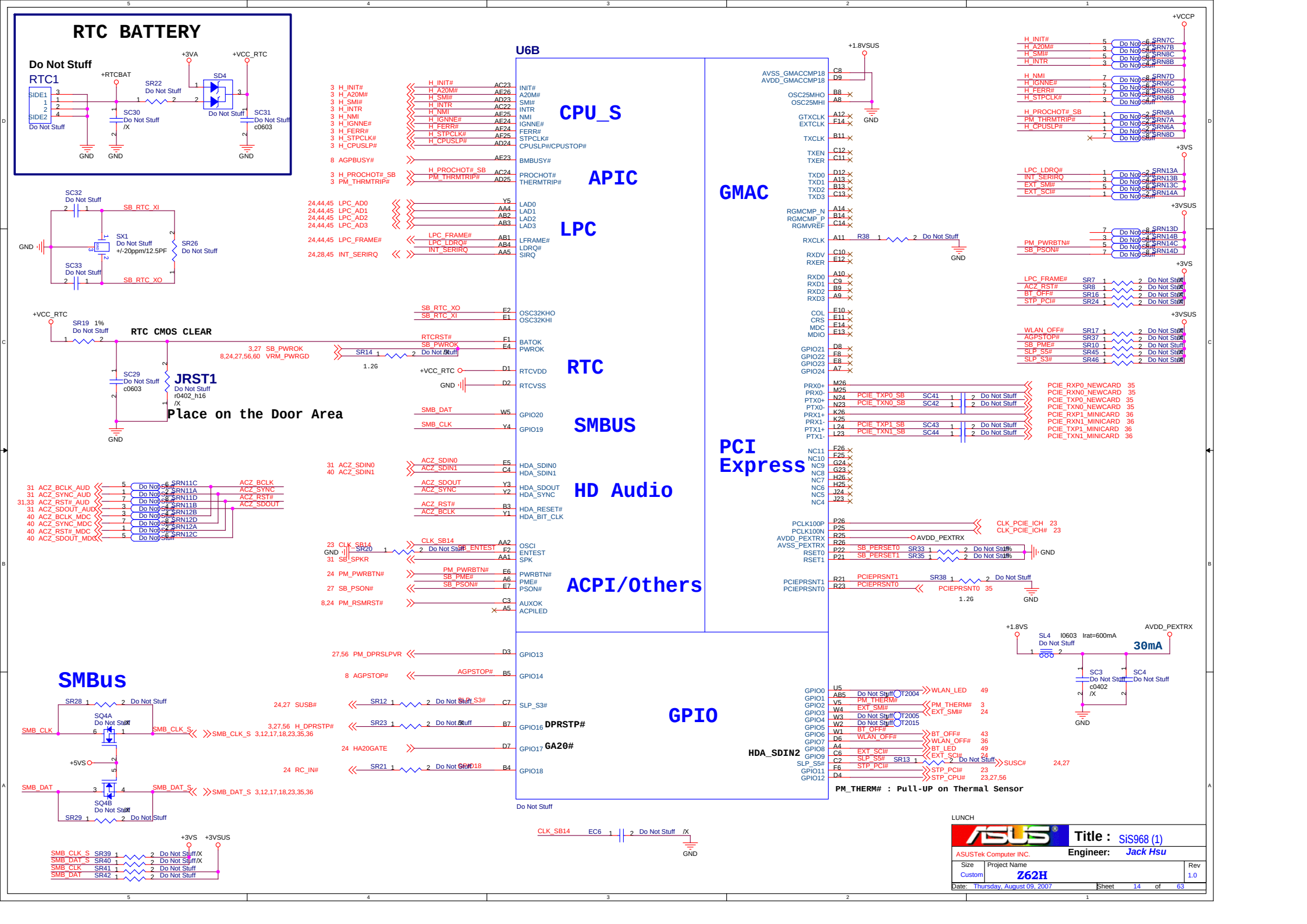

RTC BATTERY
Do Not Stuff
RTC1
SIDE1
SIDE2
+RTCBAT
+3VA
+VCC_RTC
SD4
SR22
SC30
SC31
GND
SC32
SC33
SX1
SR26
SB_RTC_XI
SB_RTC_XO
+VCC_RTC
SR19
RTC CMOS CLEAR
SC29
JRST1
Place on the Door Area
SMBus
SR28
SQ4A
SQ4B
SMB_CLK
SMB_DAT
SMB_CLK_S
SMB_DAT_S
+5VS
SR29
+3VS
+3VSUS
SR39
SR40
SR41
SR42
U6B
CPU_S
APIC
LPC
RTC
SMBUS
HD Audio
ACPI/Others
GPIO
GMAC
PCI Express
DPRSTP#
GA20#
HDA_SDIN2
PM_THERM# : Pull-UP on Thermal Sensor
+1.8VSUS
+VCCP
+1.8VS
AVDD_PEXTRX
SL4
30mA
SC3
SC4
LUNCH
Title : SiS968 (1)
ASUSTek Computer INC.
Engineer: Jack Hsu
Size
Custom
Project Name
Z62H
Rev
1.0
Date: Thursday, August 09, 2007
Sheet 14 of 63

USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth

U6C

USB

42 USB_PP0 — D26 UV0+
42 USB_PN0 — D25 UV0-
42 USB_PP1 — E24 UV1+
42 USB_PN1 — E23 UV1-
42 USB_PP2 — A20 UV2+
42 USB_PN2 — B20 UV2-
42 USB_PP3 — C19 UV3+
42 USB_PN3 — D19 UV3-
35 USB_PP4 — A18 UV4+
35 USB_PN4 — B18 UV4-
36 USB_PP5 — C17 UV5+
36 USB_PN5 — D17 UV5-
22 USB_PP6 — A16 UV6+
22 USB_PN6 — B16 UV6-
43 USB_PP7 — C15 UV7+
43 USB_PN7 — D15 UV7-

42 USB_OC#01 — A23 OC0#
— F21 OC1#
42 USB_OC#23 — A24 OC2#
— B24 OC3#
35 NEWCARD_OC#4 — C23 OC4#
USB_OC#5 — C24 OC5#
USB_OC#6 — A25 OC6#
USB_OC#7 — B23 OC7#

UVDD18 — E16 UVDD18_1, E18 UVDD18_2, F15 UVDD18_3, F16 UVDD18_4, J19 UVDD18_10, H18 UVDD18_8, H17 UVDD18_7, H16 UVDD18_6, H15 UVDD18_5, J15 UVDD18_9

UVDD33 — F22 UVDD33_1, F19 UVDD33_2, F17 UVDD33_3

OSC12MHI — A22 CLK_USB12 — CLK_USB12 23
OSC12MHO — B22 Do Not Stuff T2006
USBREF — F20 USBREF — SR34 1 2 Do Not Stuff 1%
AVDD_USBPLL18 — B26 USBPVDD18
AVSS_USBPLL18 — B25
AVDD_USBCMP18 — E21 USBCMPAVDD18
AVSS_USBCMP18 — E20
AVDD_USBCMP33 — D21 USBCMPAVDD33
AVSS_USBCMP33 — C21

GND

SATA

STX0+ — AC13 SATA_TXP0_ICH — SC38 2 1 Do Not Stuff — SATA_TXP0 39
STX0- — AD13 SATA_TXN0_ICH — SC37 2 1 Do Not Stuff — SATA_TXN0 39
SRX0+ — AE12 SATA_RXP0_ICH — SC36 2 1 Do Not Stuff — SATA_RXP0 39
SRX0- — AE12 SATA_RXN0_ICH — SC35 2 1 Do Not Stuff — SATA_RXN0 39
STX1+ — AC6
STX1- — AD6
SRX1+ — AF5
SRX1- — AE5

XIN — AE8 SATA_XIN — SR1 1 2 Do Not Stuff
XOUT — AF8 Do Not Stuff T2007
OD, Low Active
HDACT — AA3 — SATA_LED# 37
ISWITCHOPEN1 — AC1 ISW1 — SR2 1 2 Do Not Stuff
ISWITCHOPEN0 — AD1 ISW0 — SR3 1 2 Do Not Stuff

GND

AVDD_SATARX — AE14 AVDD_SATARX
AVDD_SATAPLL33 — AF15 AVSS_SATARX
AC9 AVDD_SATAPLL33_1
AD9 AVDD_SATAPLL33_2
AC8 AVSS_SATAPLL33_1
AD8 AVSS_SATAPLL33_2
SR6 1 2 Do Not Stuff 1% — GND
GND — SC5 2 1 Do Not Stuff — SATA_REXT — AF7 REXT

23 CLK_SATA_ICH — AE15 CLK100P
23 CLK_SATA_ICH# — AD15 CLK100N

Do Not Stuff

IPB_OUT0 — D22 Do Not Stuff T2008
IPB_OUT1 — C22 Do Not Stuff T2009
TRAP0 — E22 — SR5 1 2 Do Not Stuff /X — +3VSUS
ATRAP — D10 ATRAP — SR4 1 2 Do Not Stuff — GND
PCIEWAKE — E9 PCIE_WAKE# — PCIE_WAKE# 8,26,35,36

+3VSUS

USB_OC#5 — 5 — Do Not Stuff — SRN9C
USB_OC#6 — 7 — Do Not Stuff — SRN9D
USB_OC#7 — 3 — Do Not Stuff — SRN9B
PCIE_WAKE# — 1 — Do Not Stuff — SRN9A

CLK_USB12 — EC83 1 2 Do Not Stuff /X — GND

+1.8VSUS — SL5 I0603 Irat=600mA Do Not Stuff — USBPVDD18 — 7mA
SC54 Do Not Stuff /X — SC55 Do Not Stuff /X — SC56 Do Not Stuff
GND

+3VSUS — SL6 I0603 Irat=600mA Do Not Stuff — USBCMPAVDD33 — 8mA
SC57 Do Not Stuff /X — SC58 Do Not Stuff c0402 /X — SC59 Do Not Stuff /X — SC60 Do Not Stuff
GND

+3VSUS — SL7 I0603 Irat=600mA Do Not Stuff — UVDD33 — 8mA
SC61 Do Not Stuff /X — SC62 Do Not Stuff /X — SC63 Do Not Stuff
GND

+1.8VS — SL8 I0603 Irat=600mA Do Not Stuff — AVDD_SATARX — 6mA
SC64 Do Not Stuff /X — SC65 Do Not Stuff c0402 /X — SC66 Do Not Stuff /X — SC67 Do Not Stuff
GND

+1.8VSUS — SL9 I0603 Irat=600mA Do Not Stuff — USBCMPAVDD18 — 9mA
SC68 Do Not Stuff c0402 /X — SC69 Do Not Stuff /X — SC70 Do Not Stuff
GND

+1.8VSUS — SL10 I0603 Irat=600mA Do Not Stuff — UVDD18 — 284mA
SC71 Do Not Stuff c0402 — SC72 Do Not Stuff /X — SC73 Do Not Stuff /X — SC74 Do Not Stuff
GND

+3VS — SL11 I0603 Irat=600mA Do Not Stuff — AVDD_SATAPLL33 — 41mA
SC75 Do Not Stuff /X — SC76 Do Not Stuff c0402 — SC77 Do Not Stuff /X — SC78 Do Not Stuff /X — SC79 Do Not Stuff
GND

LUNCH

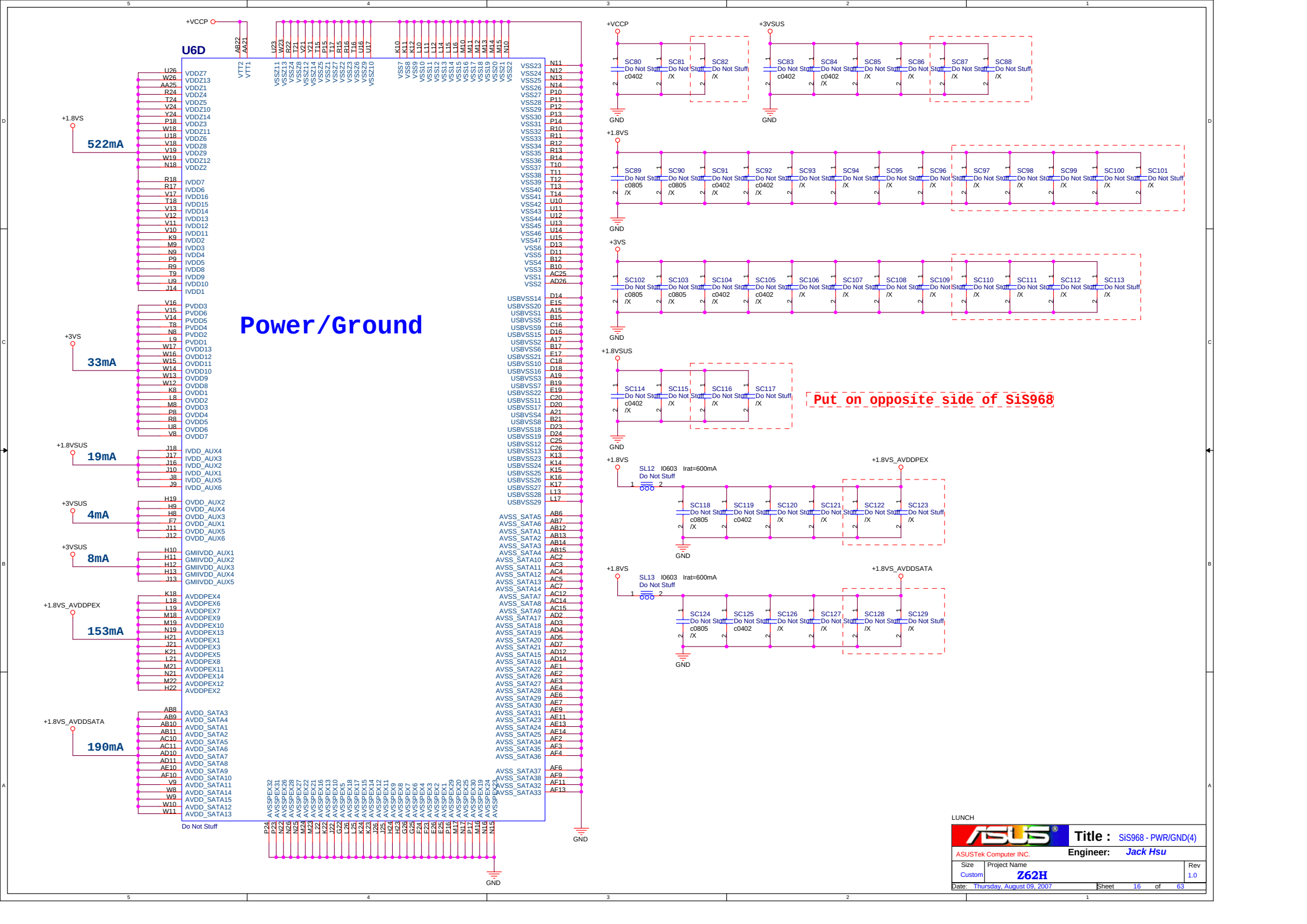
ASUSTek Computer INC.

Title : SiS968 (3)

Engineer: Jack Hsu

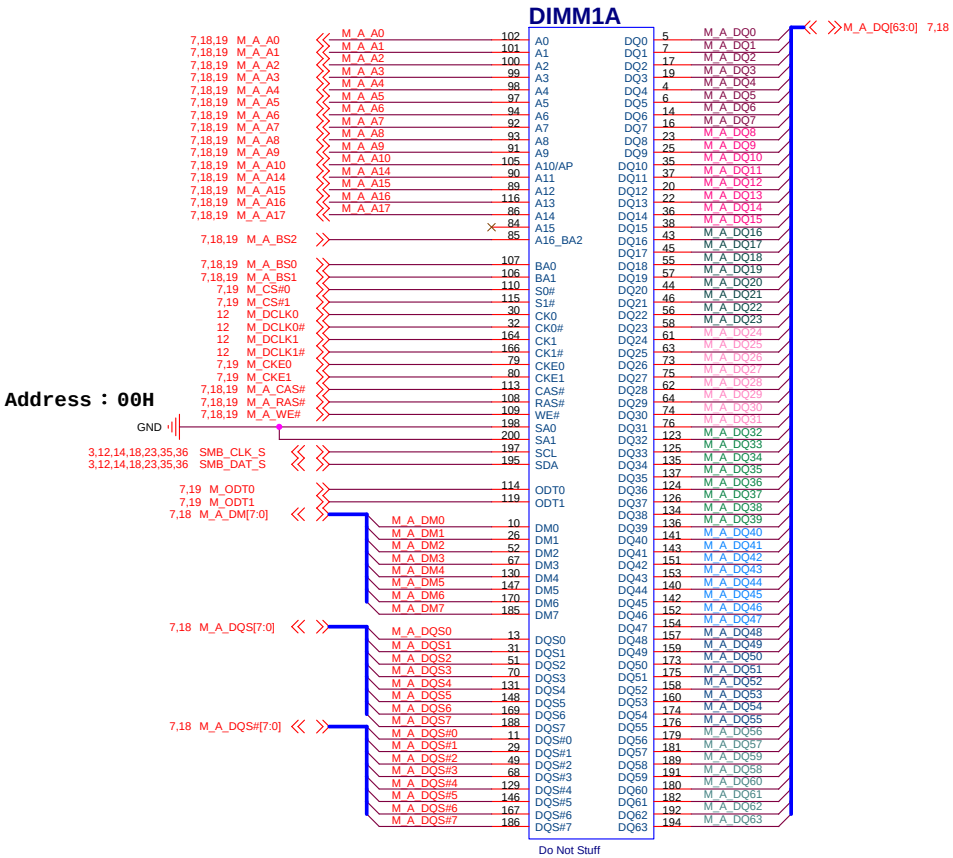
Size	Project Name	Rev
Custom	Z62H	1.0

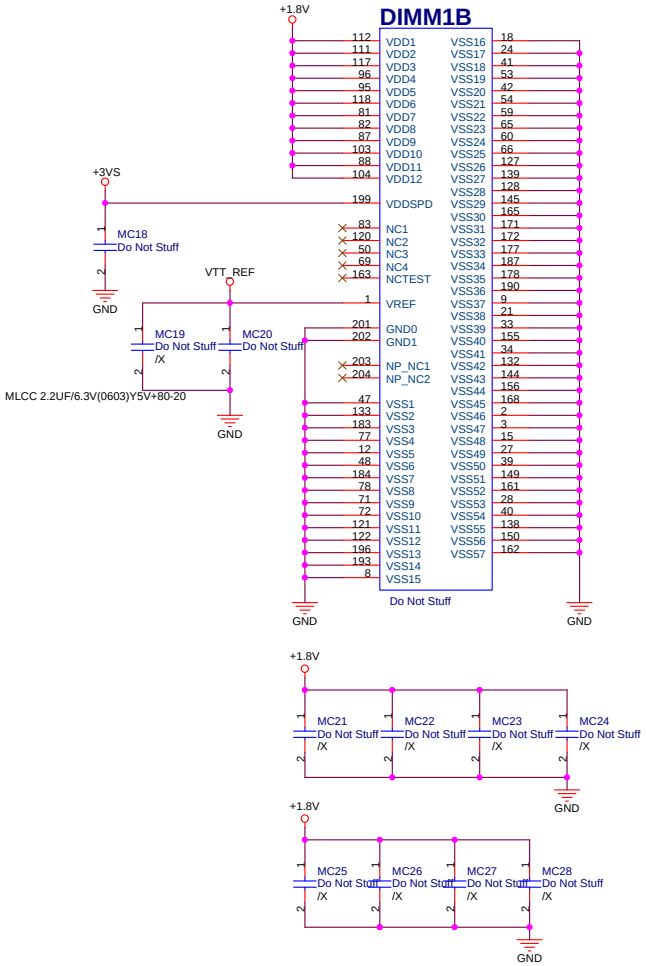
Date: Thursday, August 09, 2007 Sheet 15 of 63



LUNCH

ASUSTek Computer INC.	Title : SiS968 - PWR/GND(4)	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 16 of 63	





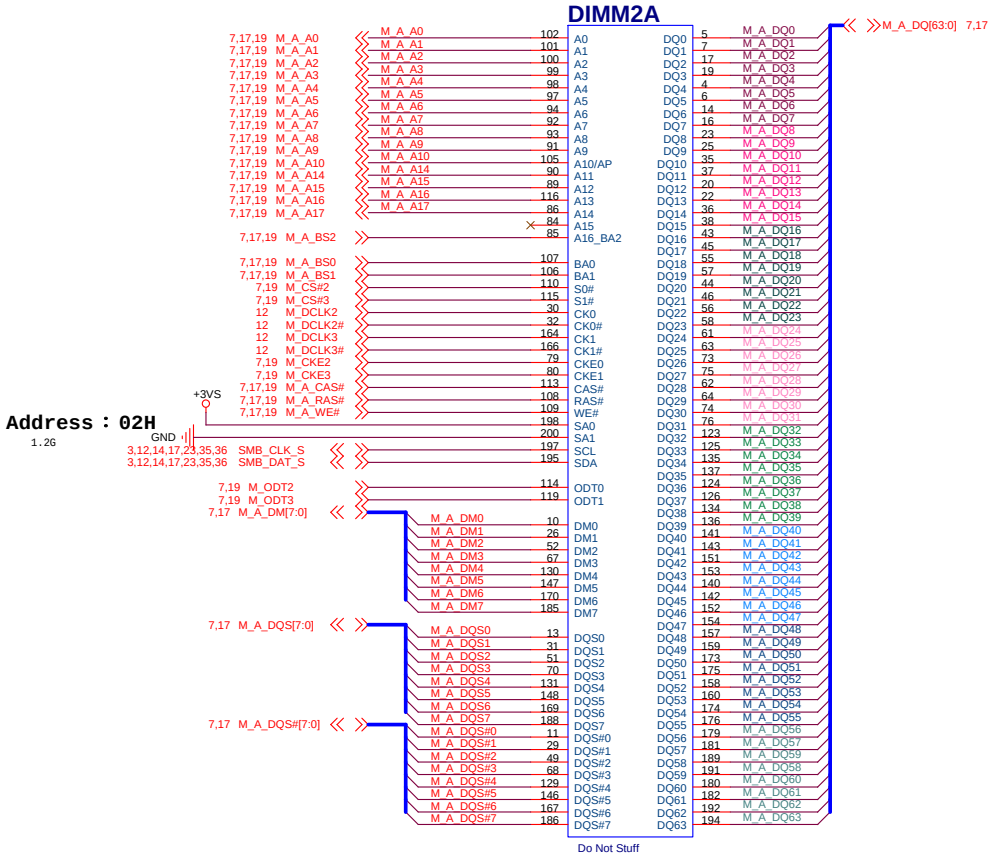
H=9.2mm Standard Type, 12G025C22000

Channel A, DIMM 0

Layout Note: Place these Caps near SO-DIMM0

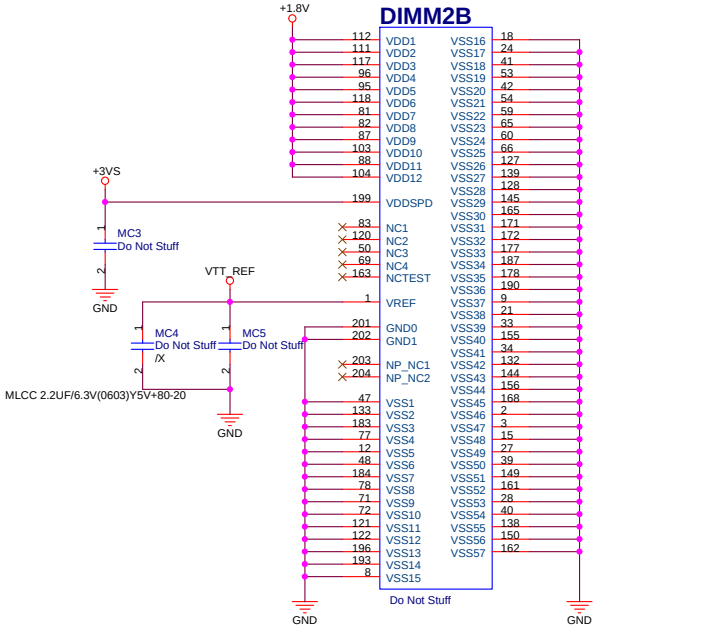
LUNCH

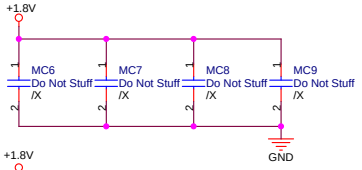
ASUSTek Computer INC.	Title : DDR SO-DIMM0	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 17 of 63	

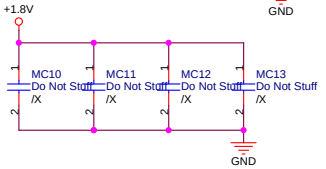


H=5.2mm Standard Type, 12G025122007

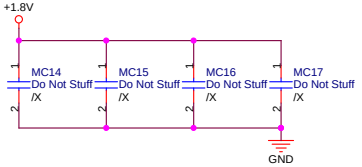
Channel A, DIMM 1







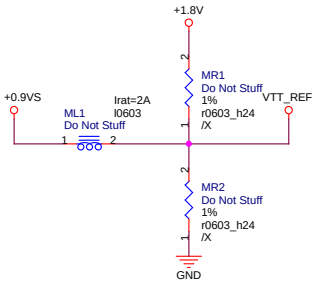
Layout Note: Place these Caps near SO-DIMM1

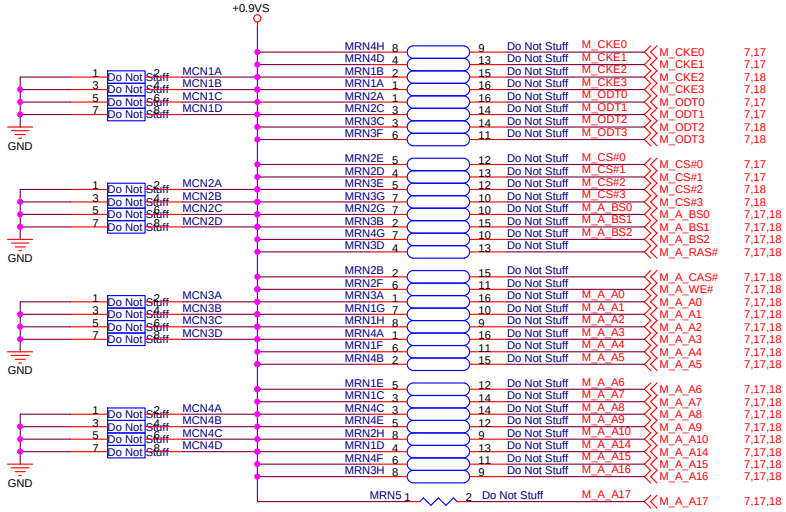


Layout Note: Place these High-Freq decoupling Caps near the GMCH

LUNCH

ASUSTek Computer INC.	Title : DDR SO-DIMM1	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 18 of 63	



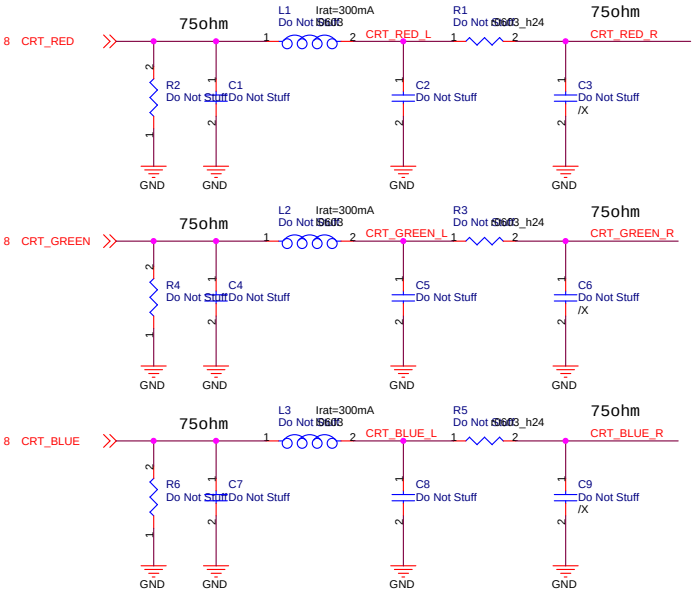


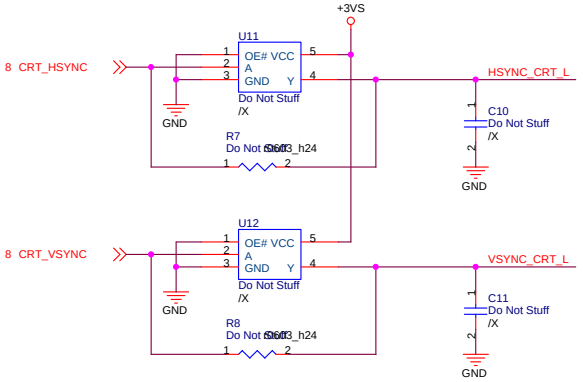
DDR2: Command, Control Signal need termination

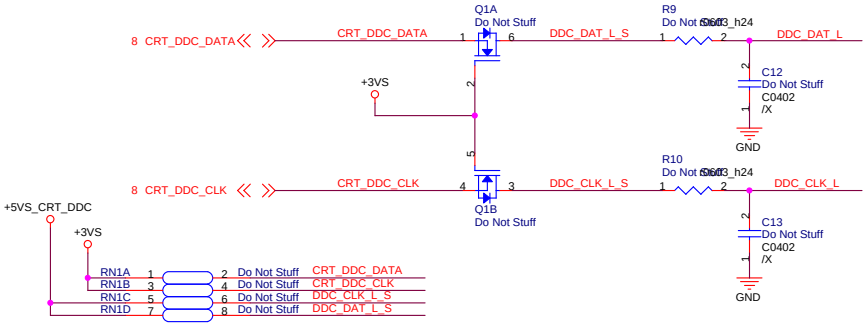
Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V

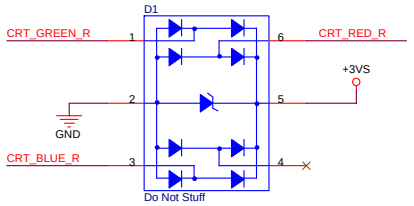
LUNCH

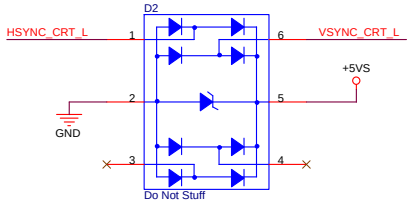
ASUSTek Computer INC.	Title : DDR2 Termination	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 19 of 63	





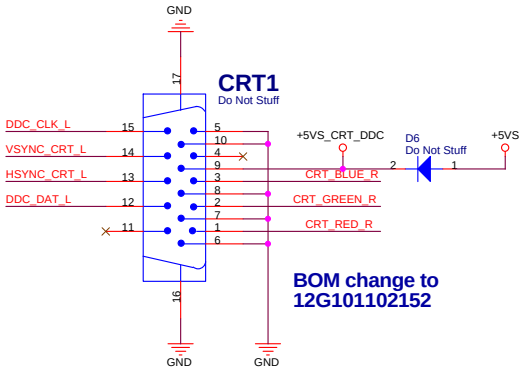






ESD Diodes

Place ESD Diodes near CRT Connector

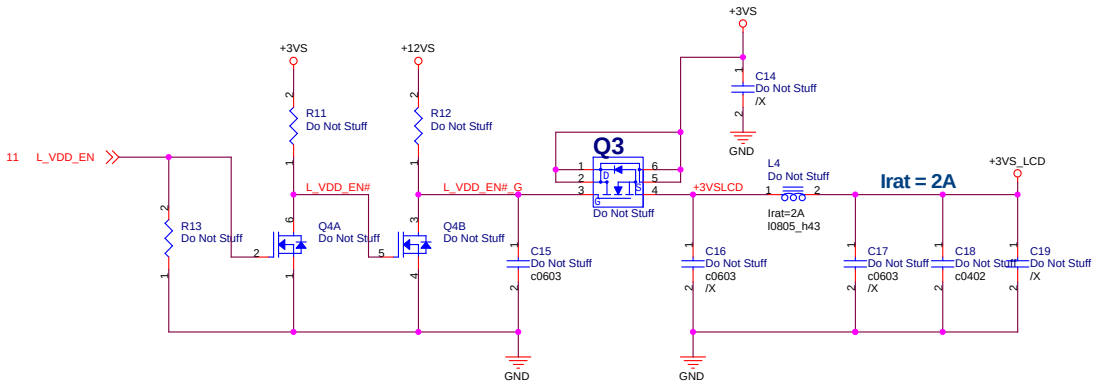


CRT Connector

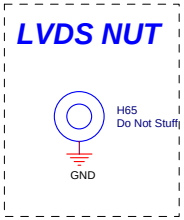
LUNCH

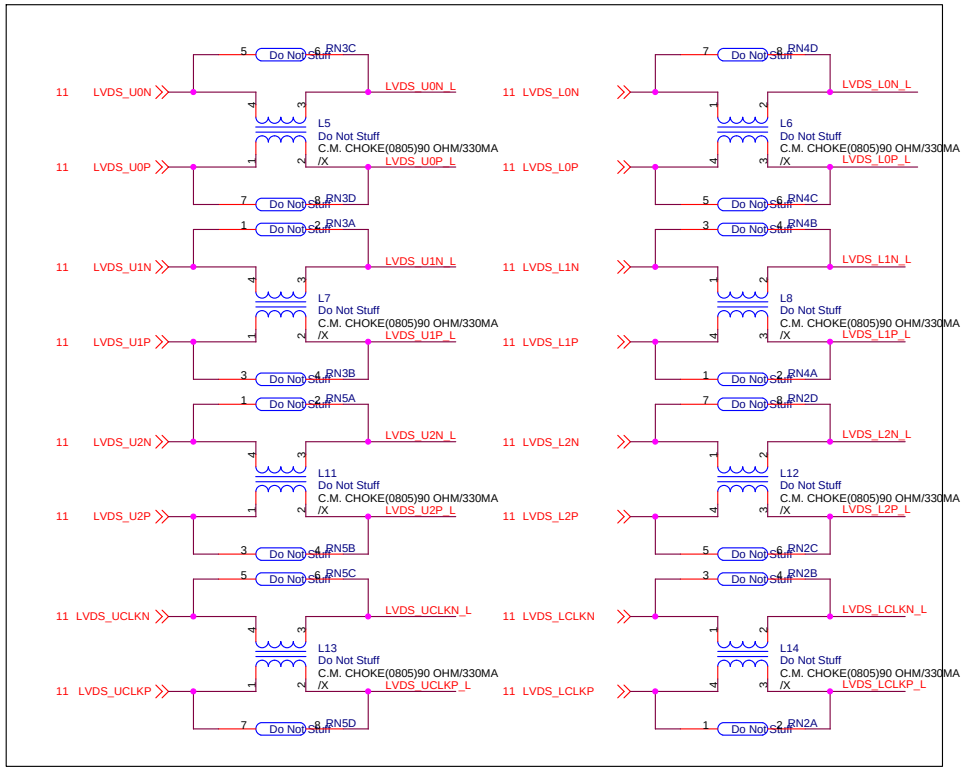
ASUSTek Computer INC.	Title : CRT Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 20 of 63	

LCD Power Switch

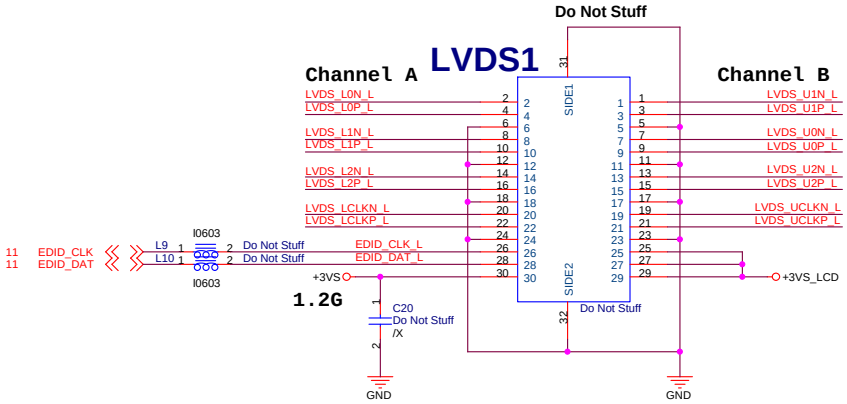


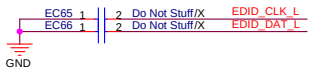
LVDS NUT





LVDS Connector





Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

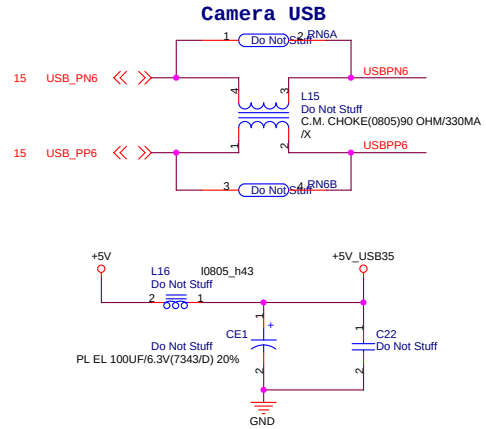
LUNCH

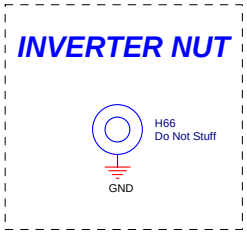
ASUSTek Computer INC.	Title : LVDS Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 21 of 63	

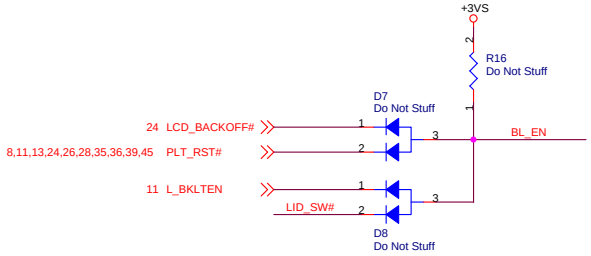
INVERTER Interface

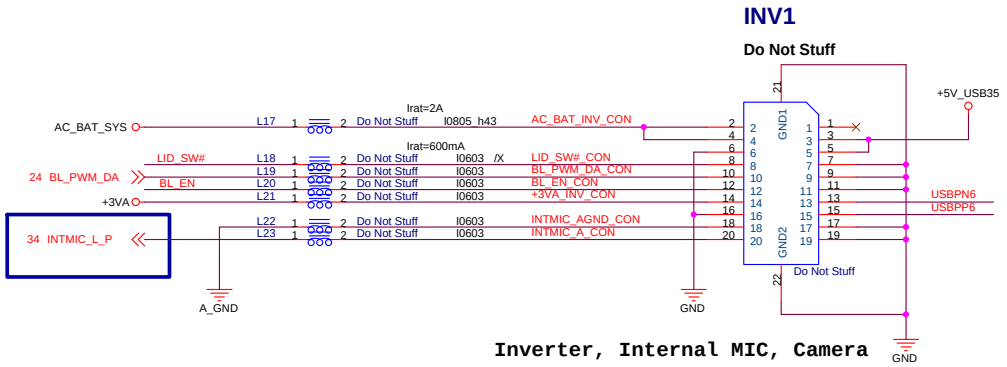
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back light.
Inverter Board built in 14.1W LCD Panel

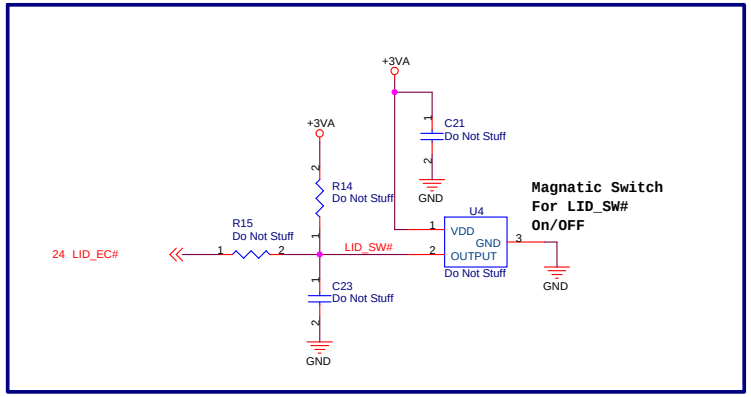


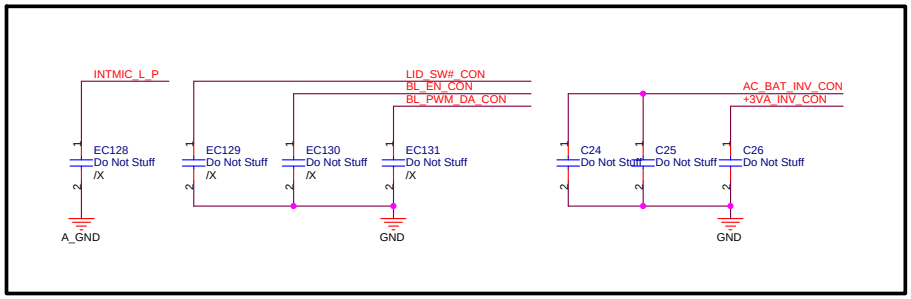






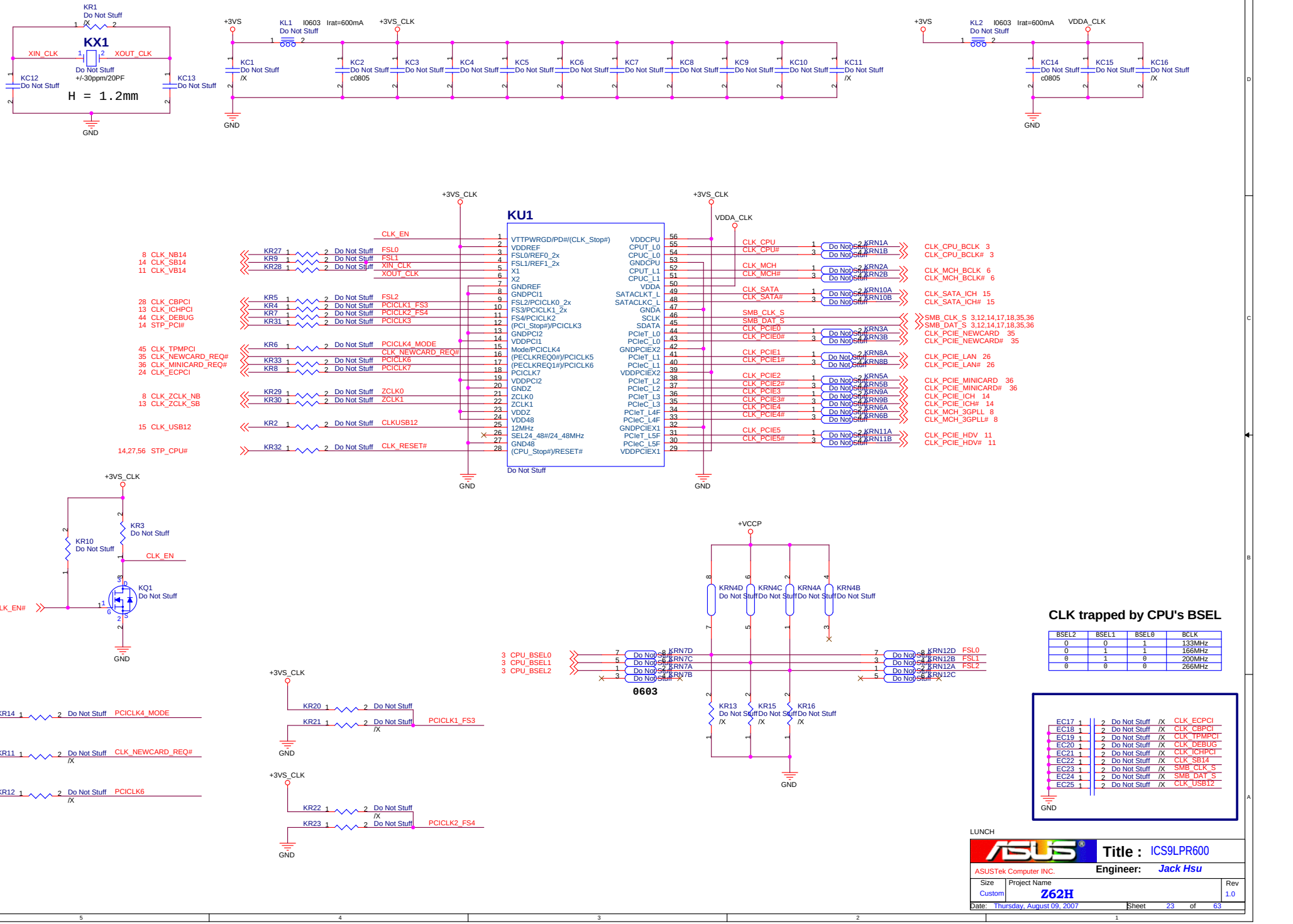
Inverter, Internal MIC, Camera





LUNCH

ASUSTek Computer INC.	Title : Inverter	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 22 of 63	



CLK trapped by CPU's BSEL

BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

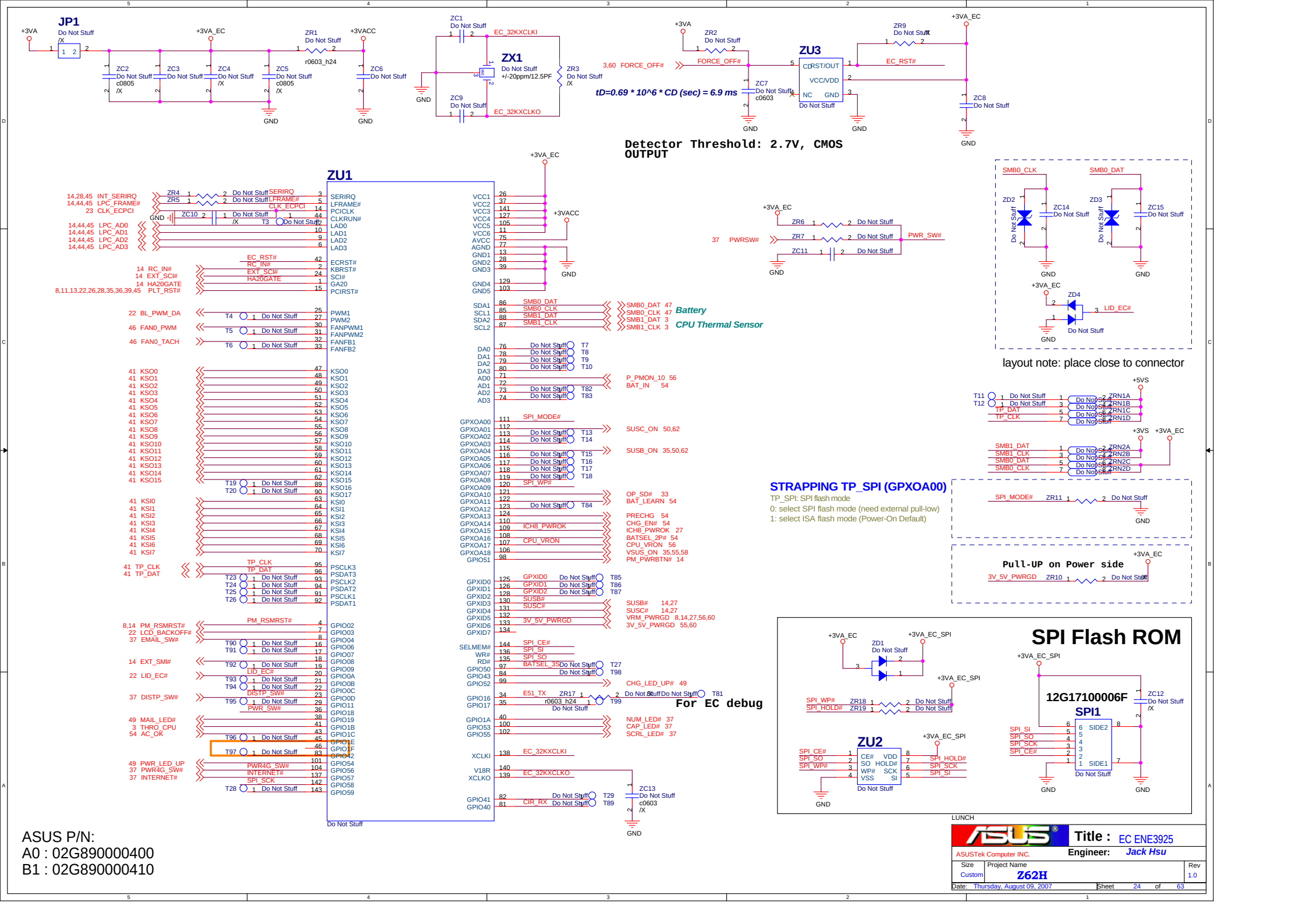
LUNCH

Title : ICS9LPR600

ASUSTek Computer INC. **Engineer:** *Jack Hsu*

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 23 of 63


JP1
Do Not Stuff
/X
+3VA
+3VA_EC
+3VACC
ZR1
Do Not Stuff
r0603_h24
ZC2
Do Not Stuff
c0805
/X
ZC3
Do Not Stuff
ZC4
Do Not Stuff
/X
ZC5
Do Not Stuff
c0805
/X
ZC6
Do Not Stuff
GND
ZC1
Do Not Stuff
EC_32KXCLKI
ZX1
Do Not Stuff
+/-20ppm/12.5PF
ZR3
Do Not Stuff
/X
EC_32KXCLKO
ZC9
Do Not Stuff
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
3,60 FORCE_OFF#
FORCE_OFF#
ZR2
Do Not Stuff
ZU3
CD RST/OUT
VCC/VDD
NC GND
Do Not Stuff
ZC7
Do Not Stuff
c0603
ZR9
Do Not Stuff
EC_RST#
ZC8
Do Not Stuff
Detector Threshold: 2.7V, CMOS OUTPUT
ZU1
SERIRQ
LFRAME#
PCICLK
CLKRUN#
LAD0
LAD1
LAD2
LAD3
ECRST#
KBRST#
SCI#
GA20
PCIRST#
PWM1
PWM2
FANPWM1
FANPWM2
FANFB1
FANFB2
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16
KSO17
KSI0
KSI1
KSI2
KSI3
KSI4
KSI5
KSI6
KSI7
PSCLK3
PSDAT3
PSCLK2
PSDAT2
PSCLK1
PSDAT1
GPIO02
GPIO03
GPIO04
GPIO06
GPIO07
GPIO08
GPIO09
GPIO0A
GPIO0B
GPIO0C
GPIO0D
GPIO11
GPIO18
GPIO19
GPIO1B
GPIO1C
GPIO1E
GPIO1F
GPIO42
GPIO54
GPIO56
GPIO57
GPIO58
GPIO59
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
AGND
GND1
GND2
GND3
GND4
GND5
SDA1
SCL1
SDA2
SCL2
DA0
DA1
DA2
DA3
AD0
AD1
AD2
AD3
GPXOA00
GPXOA01
GPXOA02
GPXOA03
GPXOA04
GPXOA05
GPXOA06
GPXOA07
GPXOA08
GPXOA09
GPXOA10
GPXOA11
GPXOA12
GPXOA13
GPXOA14
GPXOA15
GPXOA16
GPXOA17
GPXOA18
GPIO51
GPXID0
GPXID1
GPXID2
GPXID3
GPXID4
GPXID5
GPXID6
GPXID7
SELMEM#
WR#
RD#
GPIO50
GPIO43
GPIO52
GPIO16
GPIO17
GPIO1A
GPIO53
GPIO55
XCLKI
V18R
XCLKO
GPIO41
GPIO40
Do Not Stuff
+3VACC
GND
SMB0_DAT 47
SMB0_CLK 47
SMB1_DAT 3
SMB1_CLK 3
Battery
CPU Thermal Sensor
P_PMON_10 56
BAT_IN 54
SUSC_ON 50,62
SUSB_ON 35,50,62
OP_SD# 33
BAT_LEARN 54
PRECHG 54
CHG_EN# 54
ICH8_PWROK 27
BATSEL_2P# 54
CPU_VRON 56
VSUS_ON 35,55,58
PM_PWRBTN# 14
SUSB# 14,27
SUSC# 14,27
VRM_PWRGD 8,14,27,56,60
3V_5V_PWRGD 55,60
CHG_LED_UP# 49
NUM_LED# 37
CAP_LED# 37
SCRL_LED# 37
EC_32KXCLKI
EC_32KXCLKO
For EC debug
+3VA_EC
ZR6
ZR7
ZC11
37 PWRSW#
PWR_SW#
SMB0_CLK
SMB0_DAT
ZD2
ZD3
ZC14
ZC15
ZD4
LID_EC#
layout note: place close to connector
+5VS
+3VS
ZRN1A
ZRN1B
ZRN1C
ZRN1D
ZRN2A
ZRN2B
ZRN2C
ZRN2D
STRAPPING TP_SPI (GPXOA00)
TP_SPI: SPI flash mode
0: select SPI flash mode (need external pull-low)
1: select ISA flash mode (Power-On Default)
SPI_MODE#
ZR11
Pull-UP on Power side
3V_5V_PWRGD
ZR10
SPI Flash ROM
+3VA_EC_SPI
ZD1
SPI_WP#
SPI_HOLD#
ZR18
ZR19
ZU2
SPI_CE#
SPI_SO
SPI_WP#
CE# VDD
SO HOLD#
WP# SCK
VSS SI
SPI_HOLD#
SPI_SCK
SPI_SI
12G17100006F
SPI1
SIDE2
SIDE1
ZC12
LUNCH
ASUS P/N:
A0 : 02G890000400
B1 : 02G890000410
ASUSTek Computer INC.
Title : EC ENE3925
Engineer: Jack Hsu
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 24 of 63

LUNCH

Title : BLANK

ASUSTek Computer INC.

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 25 of 63

ASUS P/N:
A2:02G751006700
B0:02G751006710

+1.2VSUS_LAN **290mA**

T1C4 Do Not Stuff
T1C5 Do Not Stuff
T1C6 Do Not Stuff /X
T1C7 Do Not Stuff /X
GND

+1.8VSUS_LAN **150mA**

T1C8 Do Not Stuff
T1C9 Do Not Stuff
T1C10 Do Not Stuff /X
T1C11 Do Not Stuff /X
T1C12 Do Not Stuff /X
GND

+3VSUS **80mA**

T1C13 Do Not Stuff /X
T1C14 Do Not Stuff /X
T1C15 Do Not Stuff /X
T1C29 Do Not Stuff c0805
T1C30 Do Not Stuff c0805
GND

+3VS
T1C3 Do Not Stuff /X
GND

T1R1 Do Not Stuff /X
T1_XTALIN
T1X1 Do Not Stuff
T1_XTALOUT
T1C16 Do Not Stuff
T1C17 Do Not Stuff
GND

+1.2VSUS_LAN
+3VSUS
+3VS
LAN_EEDATA
LAN_EECLK
GND

T1U1 Do Not Stuff

48	VDD7		
47	VMAIN_AVBL		
46	TESTMODE		
45	VDDO_TTL3		
44	VDD6		
43	Reserved4		
42	CLKREQn		
41	VPD_DATA		
40	VDDO_TTL2		
39	VDD5		
38	VPD_CLK		
37	SPI_CLK		
36	SPI_CS		
35	SPI_DI		
34	SPI_DO		
33	VDD4		
49	TX_P	PCIE_RXP2_LAN_C	8 PCIE_RXP2_LAN
50	TX_N	PCIE_RXN2_LAN_C	8 PCIE_RXN2_LAN
51	NC2		
52	NC3		
53	RX_N	PCIE_TXN2_LAN	8 PCIE_TXN2_LAN
54	RX_P	PCIE_TXP2_LAN	8 PCIE_TXP2_LAN
55	REFCLKP		23 CLK_PCIE_LAN
56	REFCLKN		23 CLK_PCIE_LAN#
57	NC4		
58	VDD8		+1.2VSUS_LAN
59	LED_ACTn		
60	LED_LINK10/100n		
61	VDDO_TTL4		+3VSUS
62	LED_LINK1000n		
63	LED_DUPLEXn		
64	NC5		
65	GND		GND
32	NC1		
31	MDIN[3]	MDIN3	40
30	MDIP[3]	MDIP3	40
29	Reserved3		
28	AVDD4		
27	MDIN[2]	MDIN2	40
26	MDIP[2]	MDIP2	40
25	Reserved2		
24	Reserved1		
23	AVDD3		
22	AVDD2		
21	MDIN[1]	MDIN1	40
20	MDIP[1]	MDIP1	40
19	AVDD1		
18	MDIN[0]	MDIN0	40
17	MDIP[0]	MDIP0	40

T1C2 Do Not Stuff
T1C1 Do Not Stuff

+1.8VSUS_LAN

1	VDDO_TTL1		
2	VDD1		
3	CTRL12		
4	CTRL18		
5	PERSTn/TSTPT		
6	WAKEn		
7	VDD2		
8	AVDDH(3.3V)		
9	SWITCH_VAUX		
10	LOM_DISABLEn		
11	SWITCH_VCC		
12	VAUX_AVLBL		
13	VDD3		
14	XTALO		
15	XTALI		
16	RSET		

+1.2VSUS_LAN +3VSUS

Keep at least 25mils trace width

LAN_+1.2VSUS_CTRL_25MIL
LAN_+1.8VSUS_CTRL_25MIL

LAN_RSET
T1_XTALIN
T1_XTALOUT
8056_LAN_RST#

8,11,13,22,24,28,35,36,39,45 PLT_RST#
8,15,35,36 PCIE_WAKE#

T1U2
A0 VCC 8
A1 WP 7
A2 SCL 6
GND SDA 5
Do Not Stuff
LAN_EECLK
LAN_EEDATA
GND GND

T1C18 Do Not Stuff
T1C19 Do Not Stuff
T1C20 Do Not Stuff
T1C21 Do Not Stuff

T1R4	Do Not Stuff 1%	MDIP0
T1R5	Do Not Stuff 1%	MDIN0
T1R6	Do Not Stuff 1%	MDIP1
T1R7	Do Not Stuff 1%	MDIN1
T1R8	Do Not Stuff 1%	MDIP2
T1R9	Do Not Stuff 1%	MDIN2
T1R10	Do Not Stuff 1%	MDIP3
T1R11	Do Not Stuff 1%	MDIN3

GND

*All termination resistors should be near chip

+3VSUS
LAN_RSET
T1R12 Do Not Stuff 1%
T1R13 Do Not Stuff
T1R2 Do Not Stuff
T1R3 Do Not Stuff
LAN_EEDATA
LAN_EECLK
8056_LAN_RST#
T1C28 Do Not Stuff c0402
GND

+3VSUS
T1R16 Do Not Stuff
T1R17 Do Not Stuff
LAN_+1.2VSUS_CTRL_25MIL
T1Q1 Do Not Stuff
T1C23 Do Not Stuff
GND
+1.2VSUS_LAN
SHAPE
T1C22 Do Not Stuff /X
T1C24 Do Not Stuff c0805
GND GND

+3VSUS
T1R18 Do Not Stuff
T1R19 Do Not Stuff
LAN_+1.8VSUS_CTRL_25MIL
T1Q2 Do Not Stuff
T1C26 Do Not Stuff
GND
+1.8VSUS_LAN
SHAPE
T1C25 Do Not Stuff /X
T1C27 Do Not Stuff c0805
GND GND

LUNCH

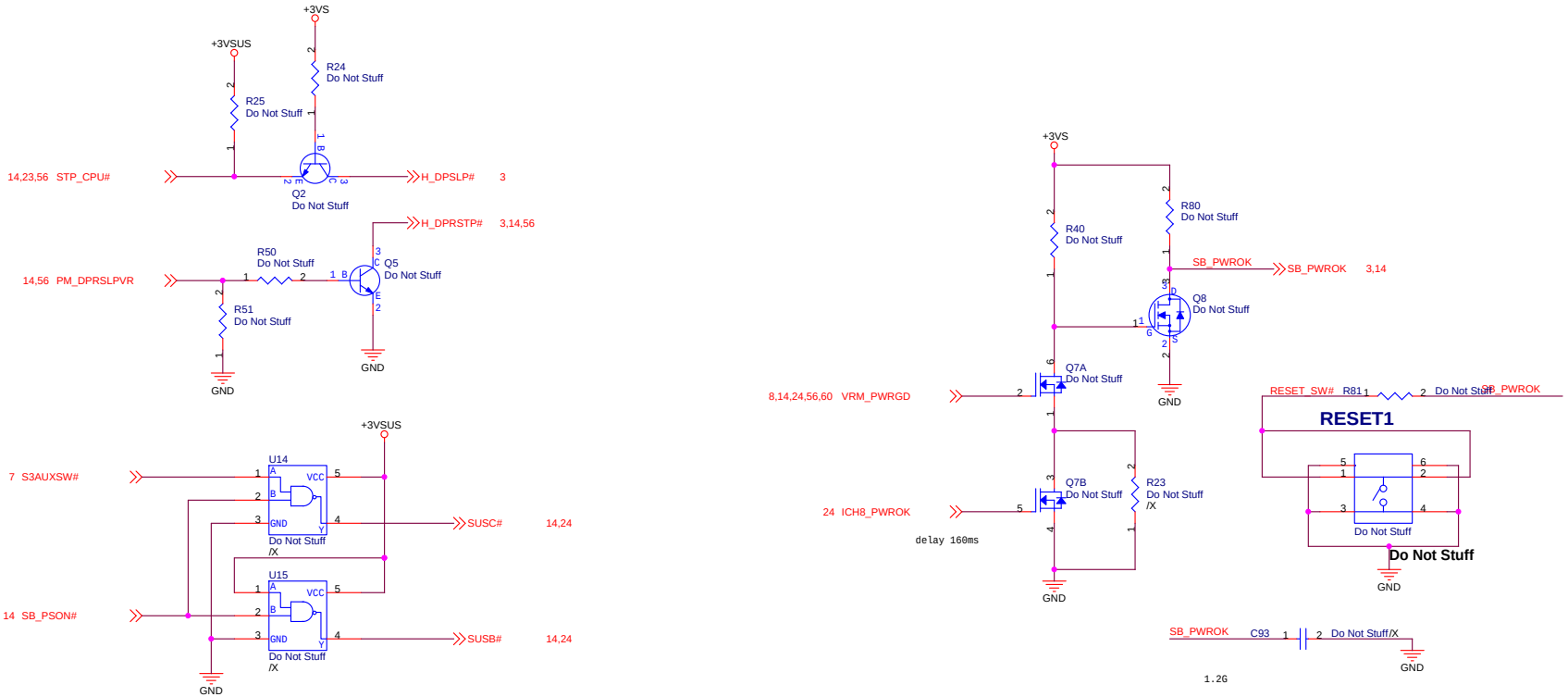
ASUSTek Computer INC.

Title : LAN Marvell 88E8056

Engineer: Jack Hsu

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Monday, August 13, 2007 Sheet 26 of 63



Power ON & OFF:

	S5 → S0 → S5		
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC#(S4)	0	1	0
SUSB#(S3)	0	1	0
Power Status	System	Main	System

Sleep & Wake up

	S0 → S3 → S0				
S3AUXSW#	1	0	0	0	1
SB_PSON#	0	0	1	0	0
SUSC#(S4)	1	1	1	1	1
SUSB#(S3)	1	1	0	1	1
Power Status	Main	Main	System, S4	Main	Main

LUNCH

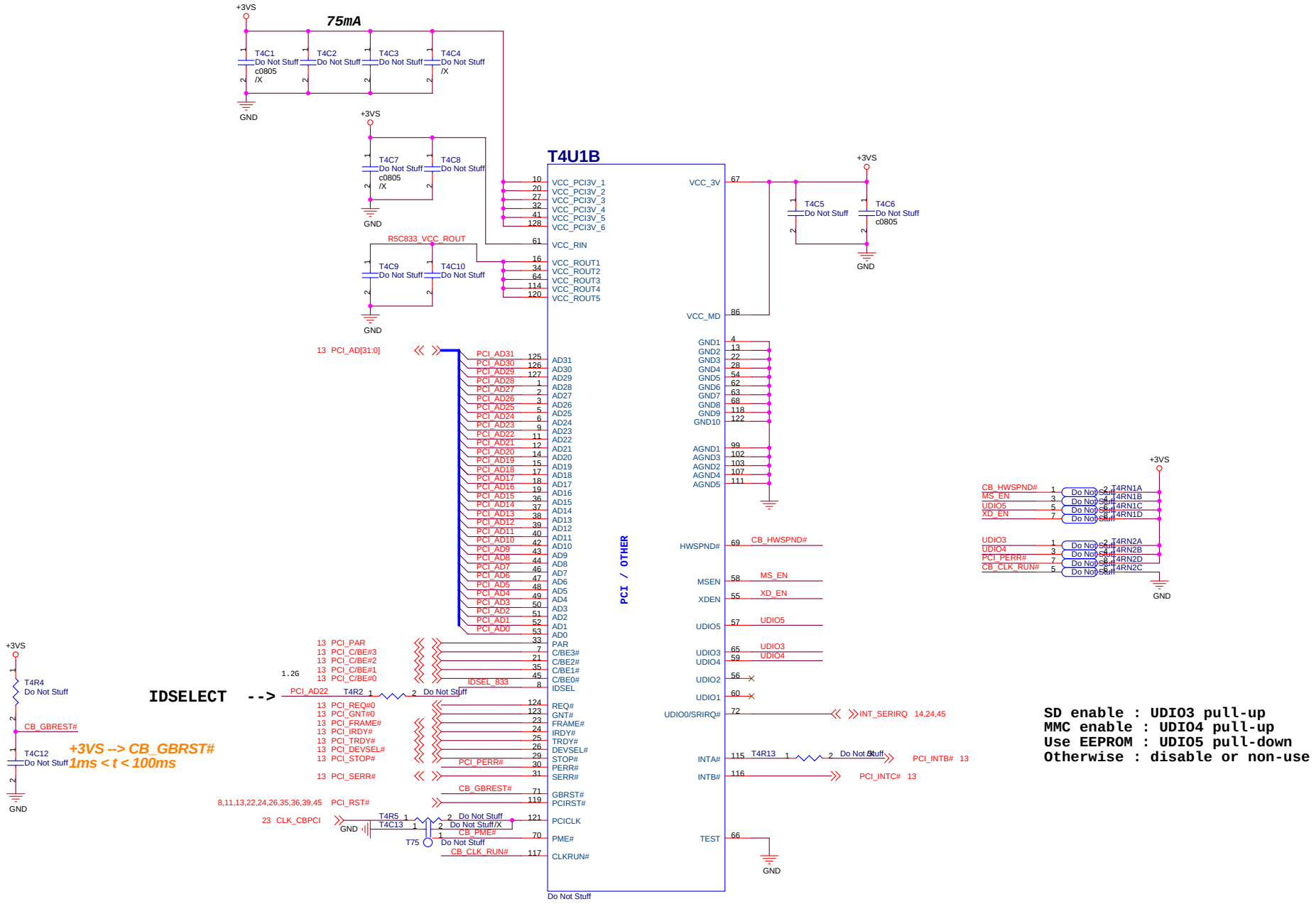
ASUSTek Computer INC.

Title : OTHER

Engineer: Jack Hsu

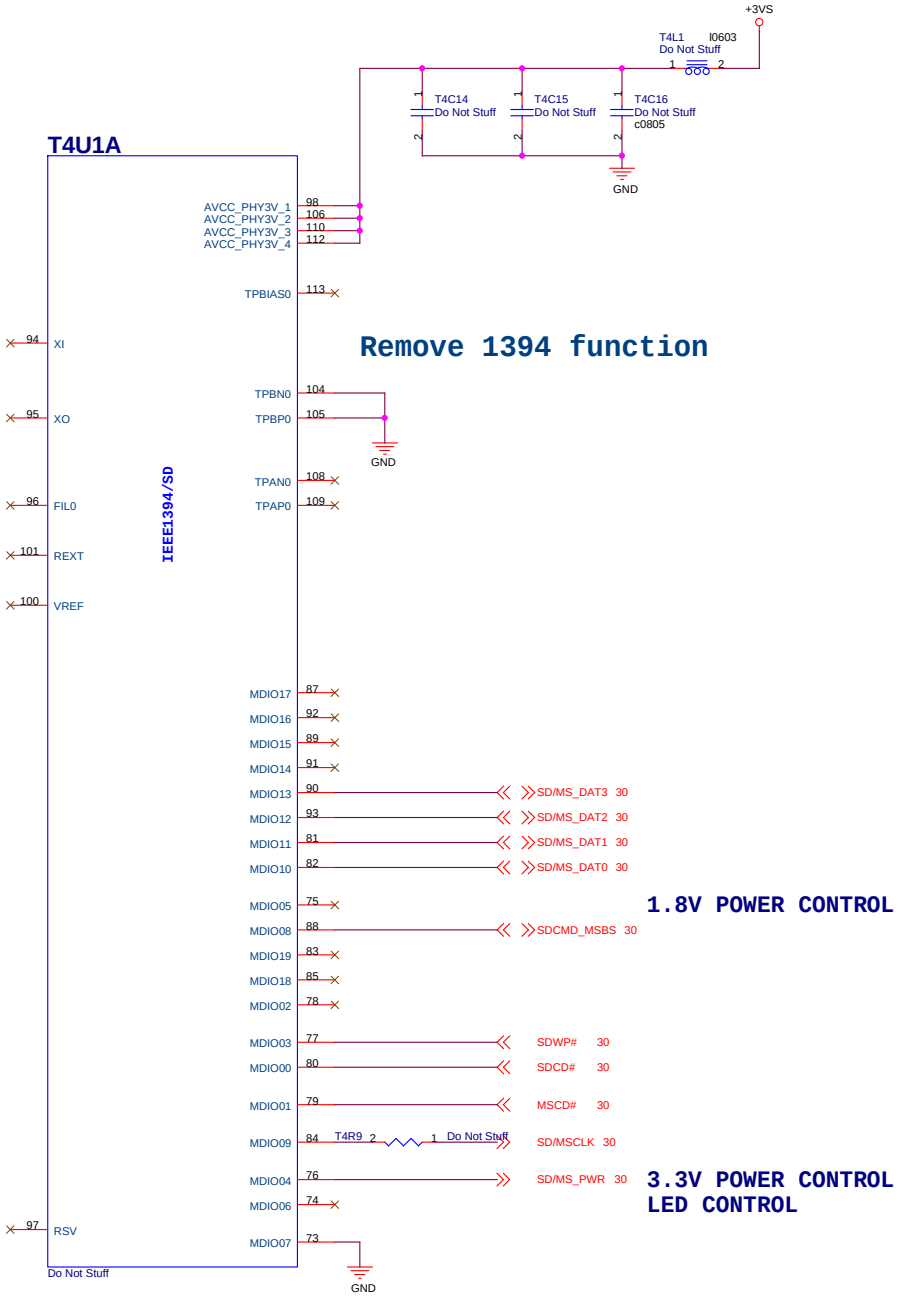
Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 27 of 63



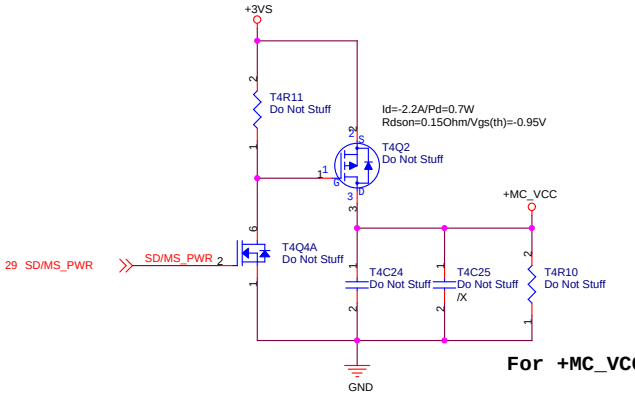
LUNCH

ASUSTek Computer INC.	Title : R5C833_PCI	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 28 of 63	



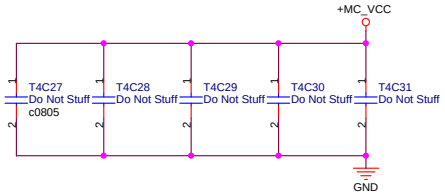
LUNCH

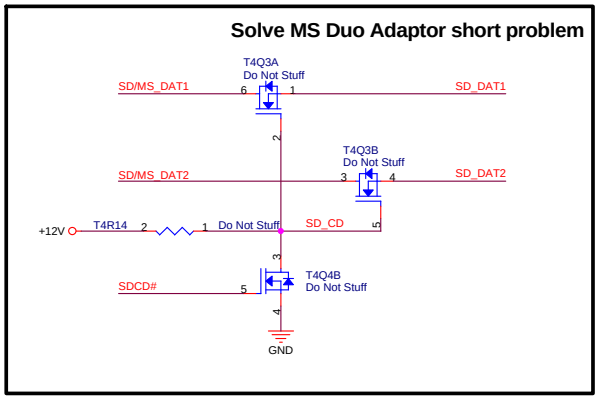
ASUSTek Computer INC.	Title : R5C833_1394/SD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 29 of 63	

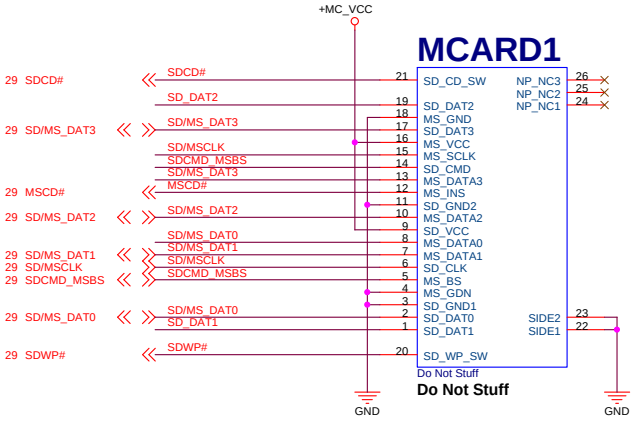


For +MC_VCC discharg

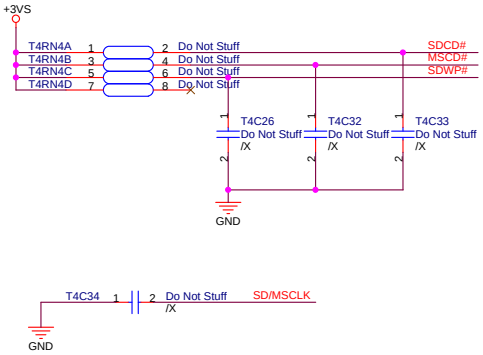
Card Reader Power Switcher





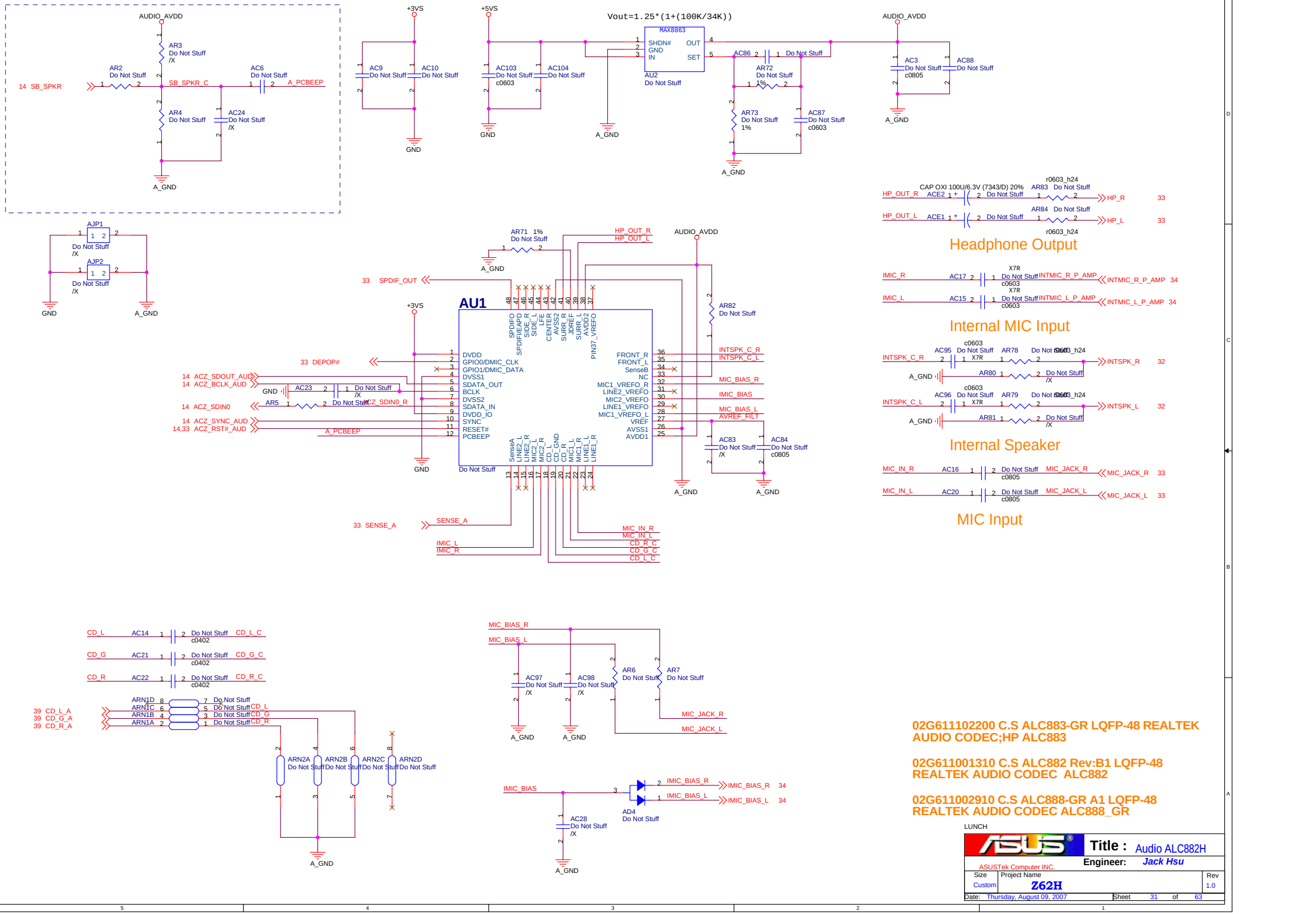


3 in 1 Card Reader



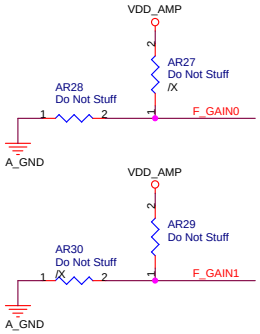
LUNCH

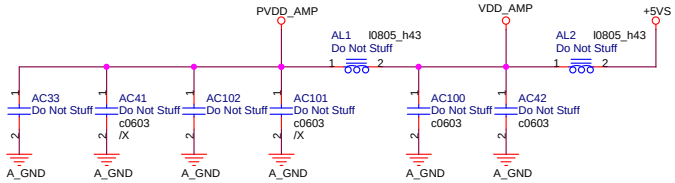
ASUSTek Computer INC.	Title : 3 in 1 Card Reader	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 30 of 63	

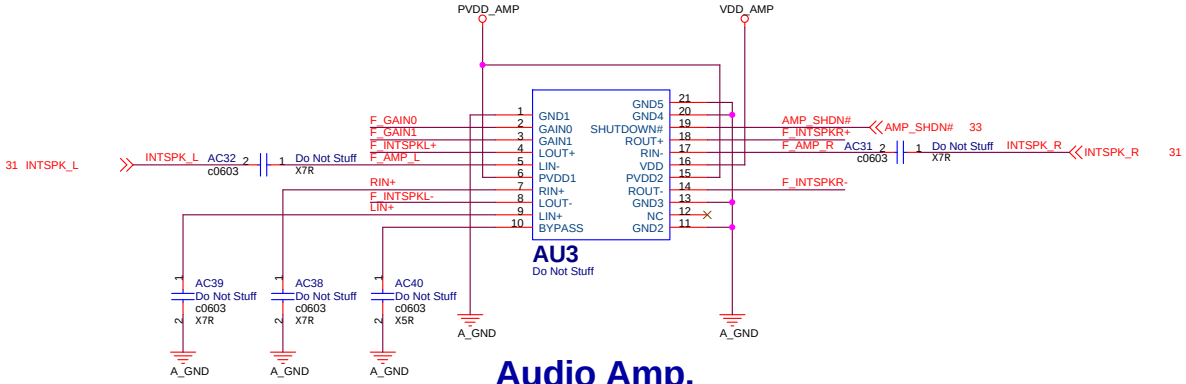

AUDIO_AVDD
AR3 Do Not Stuff /X
AR2 Do Not Stuff
AC6 Do Not Stuff
14 SB_SPKR
SB_SPKR_C
A_PCBEEP
AR4 Do Not Stuff
AC24 Do Not Stuff /X
A_GND
+3VS
AC9 Do Not Stuff
AC10 Do Not Stuff
GND
+5VS
AC103 Do Not Stuff c0603
AC104 Do Not Stuff
Vout=1.25*(1+(100K/34K))
MAX8863
SHDN#
GND
IN
OUT
SET
AU2 Do Not Stuff
AC86 Do Not Stuff
AR72 Do Not Stuff
AR73 Do Not Stuff 1%
AC87 Do Not Stuff c0603
AC3 Do Not Stuff c0805
AC88 Do Not Stuff
AJP1
AJP2
Do Not Stuff /X
AR71 1% Do Not Stuff
HP_OUT_R
HP_OUT_L
33 SPDIF_OUT
AU1
SPDIFO
SPDIFI/EAPD
SIDE_R
SIDE_L
LFE
CENTER
AVSS2
SURR_R
JDREF
SURR_L
AVDD2
PIN37_VREFO
DVDD
GPIO0/DMIC_CLK
GPIO1/DMIC_DATA
DVSS1
SDATA_OUT
BCLK
DVSS2
SDATA_IN
DVDD_IO
SYNC
RESET#
PCBEEP
FRONT_R
FRONT_L
SenseB
NC
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
LINE1_VREFO
MIC1_VREFO_L
VREF
AVSS1
AVDD1
SenseA
LINE2_R
LINE2_L
MIC2_R
MIC2_L
CD_GND
CD_R
CD_L
MIC1_R
MIC1_L
LINE1_R
LINE1_L
Do Not Stuff
AR82 Do Not Stuff
33 DEPOP#
14 ACZ_SDOUT_AUD
14 ACZ_BCLK_AUD
14 ACZ_SDIN0
14 ACZ_SYNC_AUD
14,33 ACZ_RST#_AUD
AC23 Do Not Stuff /X
AR5 Do Not Stuff
ACZ_SDIN0_R
INTSPK_C_R
INTSPK_C_L
MIC_BIAS_R
IMIC_BIAS
MIC_BIAS_L
AVREF_FILT
AC83 Do Not Stuff /X
AC84 Do Not Stuff c0805
33 SENSE_A
SENSE_A
IMIC_L
IMIC_R
MIC_IN_R
MIC_IN_L
CD_R_C
CD_G_C
CD_L_C
r0603_h24
CAP OXI 100U/6.3V (7343/D) 20%
ACE2
ACE1
AR83 Do Not Stuff
AR84 Do Not Stuff
HP_R
HP_L
33
Headphone Output
X7R
c0603
AC17
AC15
INTMIC_R_P_AMP
INTMIC_L_P_AMP
34
Internal MIC Input
AC95 Do Not Stuff
AR78 Do Not Stuff
AR80 Do Not Stuff /X
AC96 Do Not Stuff
AR79 Do Not Stuff
AR81 Do Not Stuff /X
INTSPK_R
INTSPK_L
32
Internal Speaker
AC16
AC20
MIC_JACK_R
MIC_JACK_L
MIC Input
CD_L
CD_G
CD_R
AC14 Do Not Stuff c0402
AC21 Do Not Stuff c0402
AC22 Do Not Stuff c0402
CD_L_C
CD_G_C
CD_R_C
39 CD_L_A
39 CD_G_A
39 CD_R_A
ARN1D
ARN1C
ARN1B
ARN1A
Do Not Stuff
ARN2A Do Not Stuff
ARN2B Do Not Stuff
ARN2C Do Not Stuff
ARN2D Do Not Stuff
AC97 Do Not Stuff /X
AC98 Do Not Stuff /X
AR6 Do Not Stuff
AR7 Do Not Stuff
IMIC_BIAS
IMIC_BIAS_R
IMIC_BIAS_L
AC28 Do Not Stuff /X
AD4 Do Not Stuff
34
02G611102200 C.S ALC883-GR LQFP-48 REALTEK AUDIO CODEC;HP ALC883
02G611001310 C.S ALC882 Rev:B1 LQFP-48 REALTEK AUDIO CODEC ALC882
02G611002910 C.S ALC888-GR A1 LQFP-48 REALTEK AUDIO CODEC ALC888_GR
LUNCH
Title : Audio ALC882H
Engineer: Jack Hsu
ASUSTek Computer INC.
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 31 of 63

GAIN Control

GAIN0	GAIN1	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



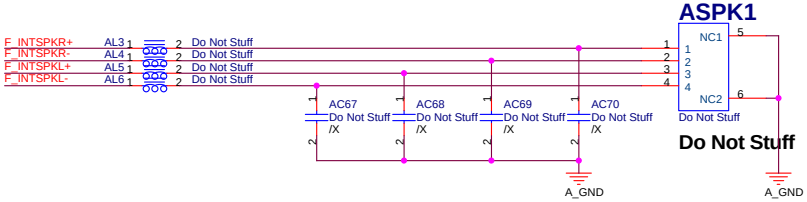




Audio Amp.
fc = 1kHz

12G171000047

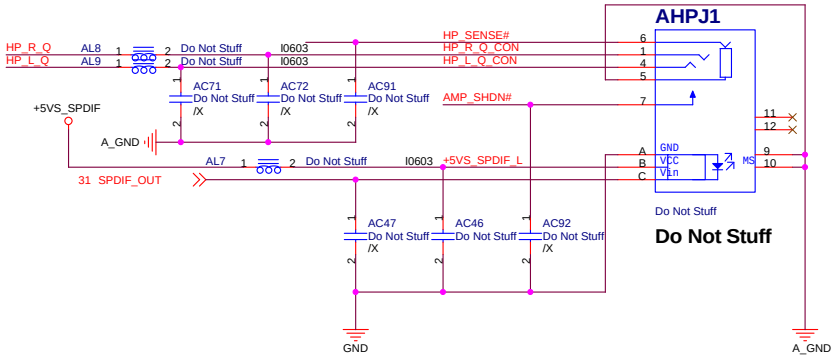
Internal Speaker Connector

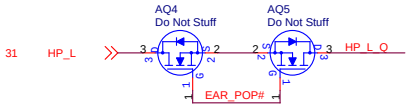


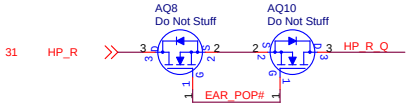
LUNCH

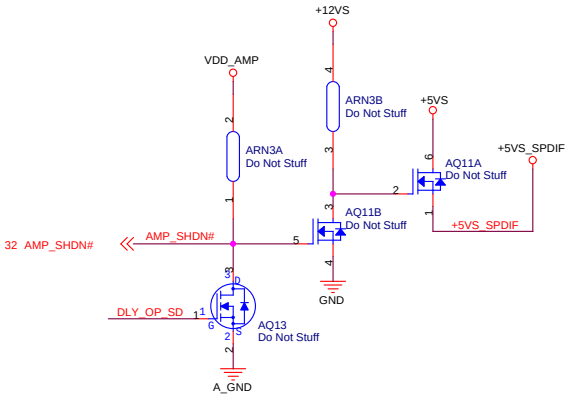
ASUSTek Computer INC.	Title : Audio Amp. & Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 32 of 63	

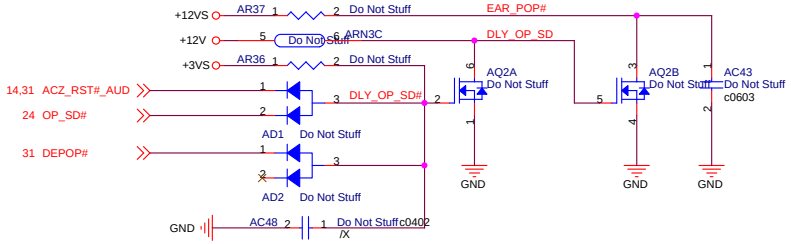
Headphone & S/PDIF Jack



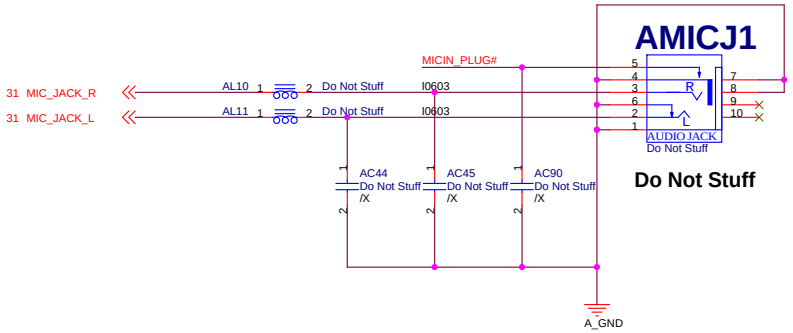








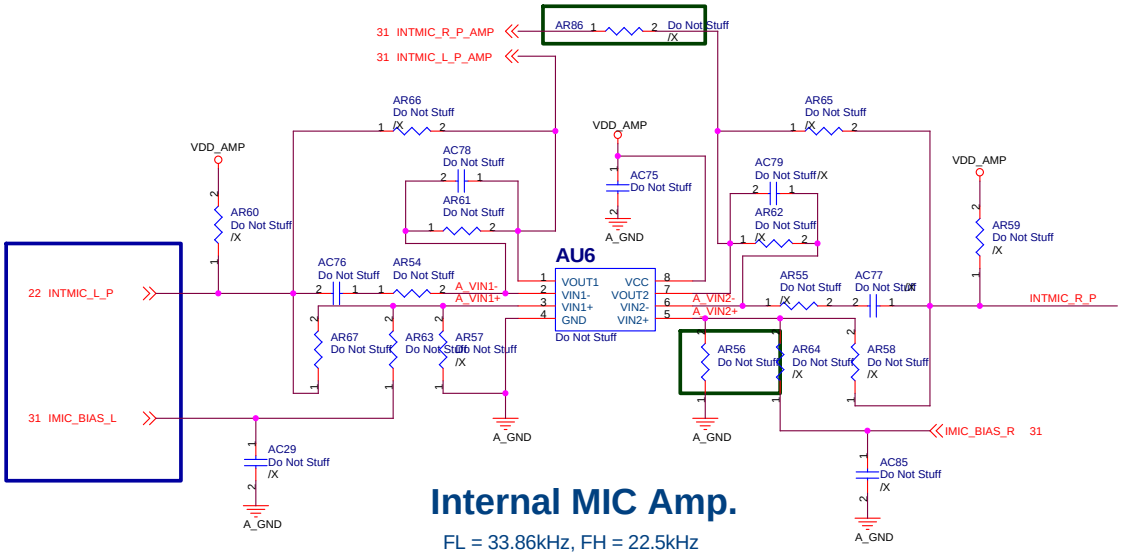
Microphone-In Jack



Jack Plug-in Detection

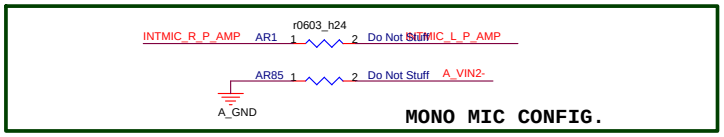
LUNCH

ASUSTek Computer INC.	Title : Audio JACK	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 33 of 63	



Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz



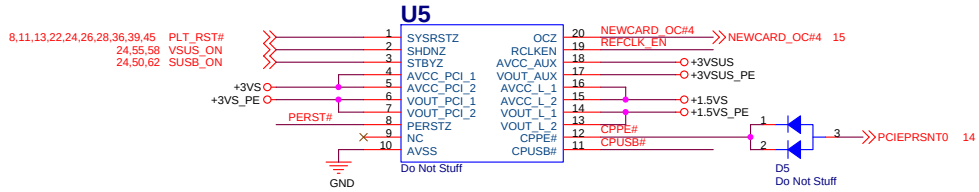
LUNCH

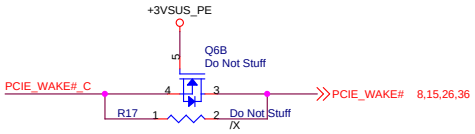
ASUSTek Computer INC.	Title : MIC PreAmp.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 34 of 63	

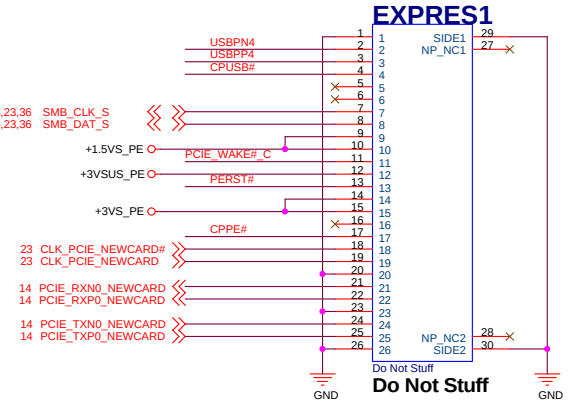
06G030057011 POWER SW. P2231TFC1 TSSOP-20 ENE P2231TFC1

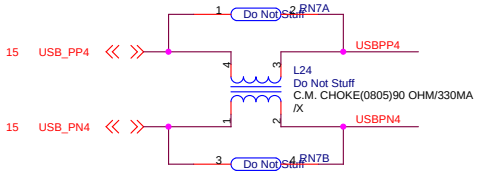
06G030057012 POWER SW. P2231TFC2 TSSOP-20 ENE P2231TFC2

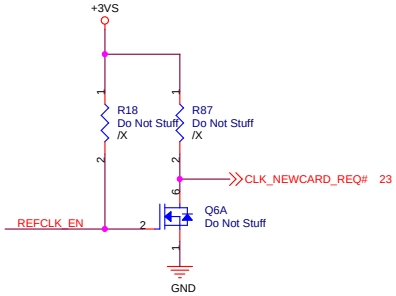
NewCard Header





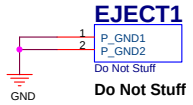


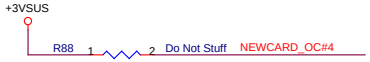


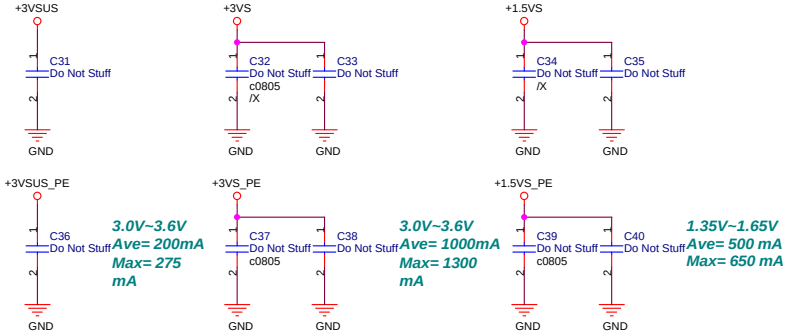


ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector

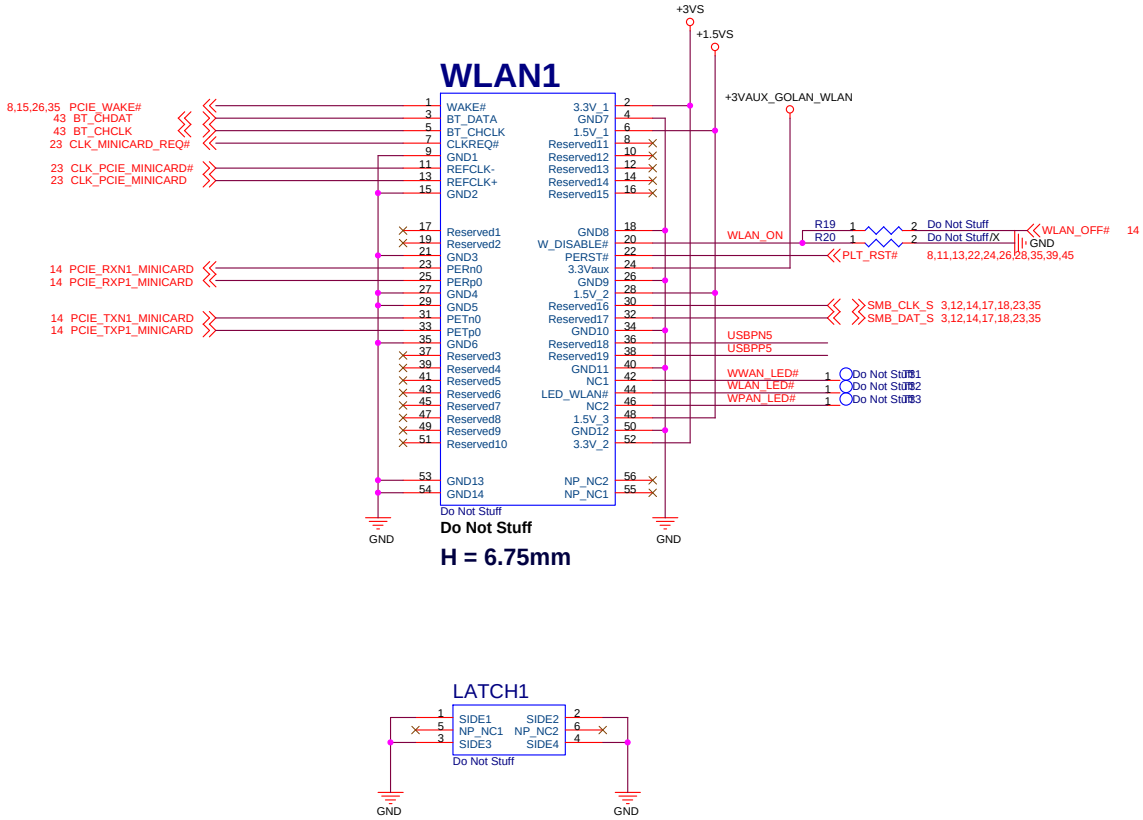


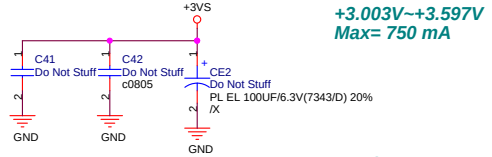




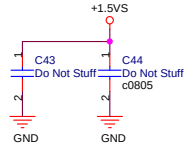
LUNCH

ASUSTek Computer INC.	Title : NEWCARD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 35 of 63	

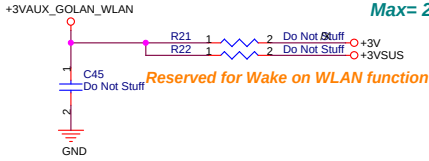




+3.003V~+3.597V
Max= 750 mA

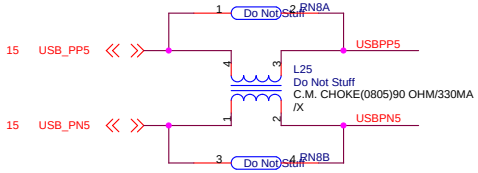


+1.425V~+1.575V
Max= 375 mA



+3.003V~+3.597V
Max= 250 mA

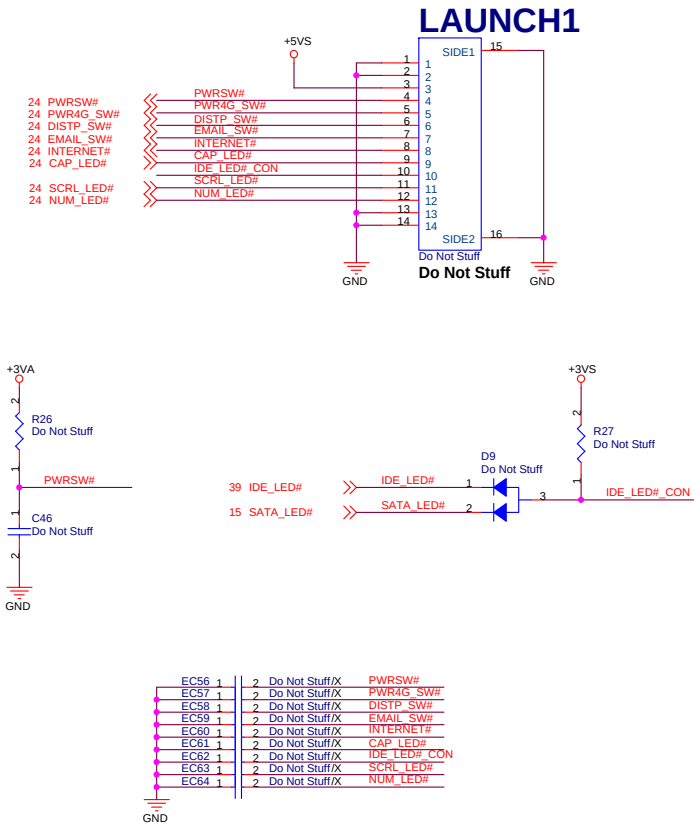
Reserved for Wake on WLAN function



LUNCH

ASUSTek Computer INC.	Title : MINICARD - WLAN	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 36 of 63	

LAUNCH BOARD Connector



LUNCH

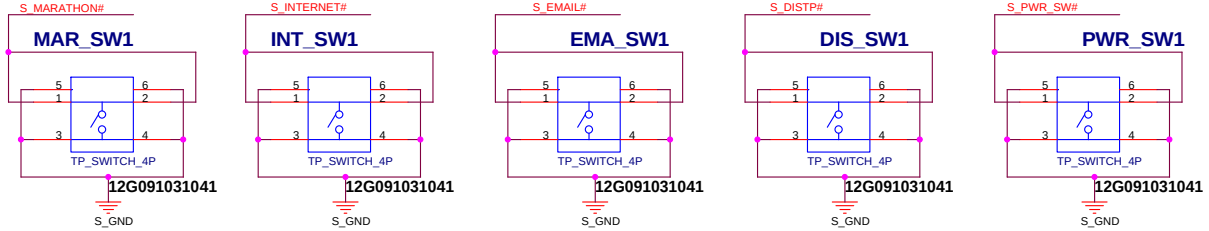
Title : LAUNCH_B Conn.

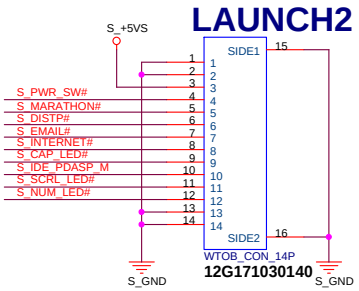
ASUSTek Computer INC.

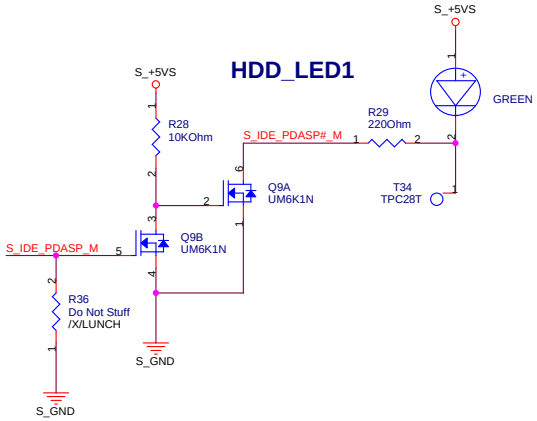
Engineer: Jack Hsu

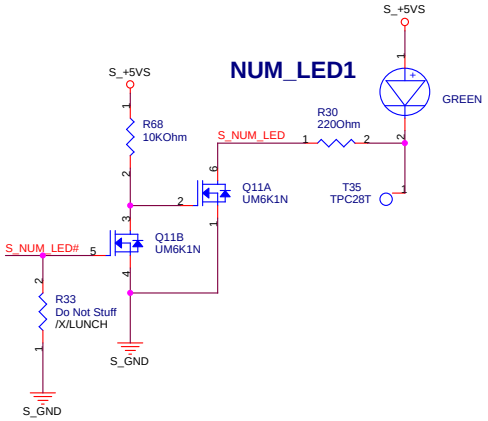
Size	Project Name	Rev
Custom	Z62H	1.0

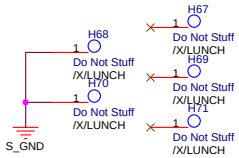
Date: Thursday, August 09, 2007 Sheet 37 of 63

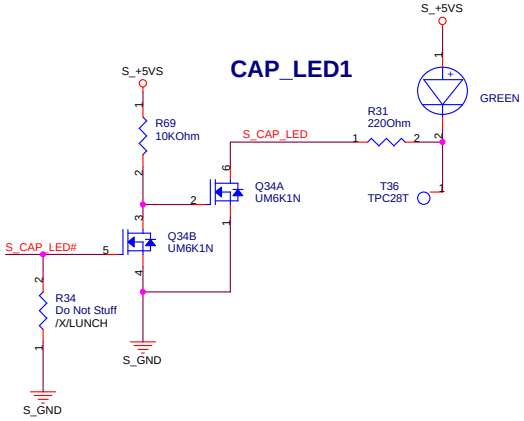


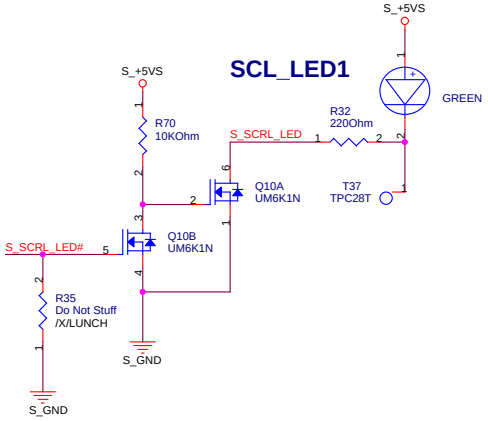












LUNCH

ASUSTek Computer INC.

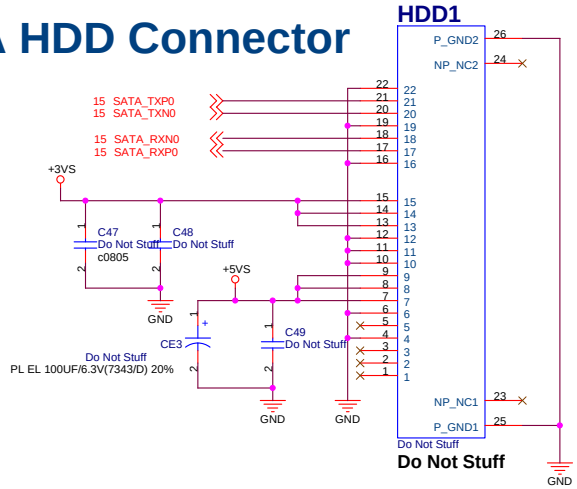
Title : LAUNCH BOARD

Engineer: Jack Hsu

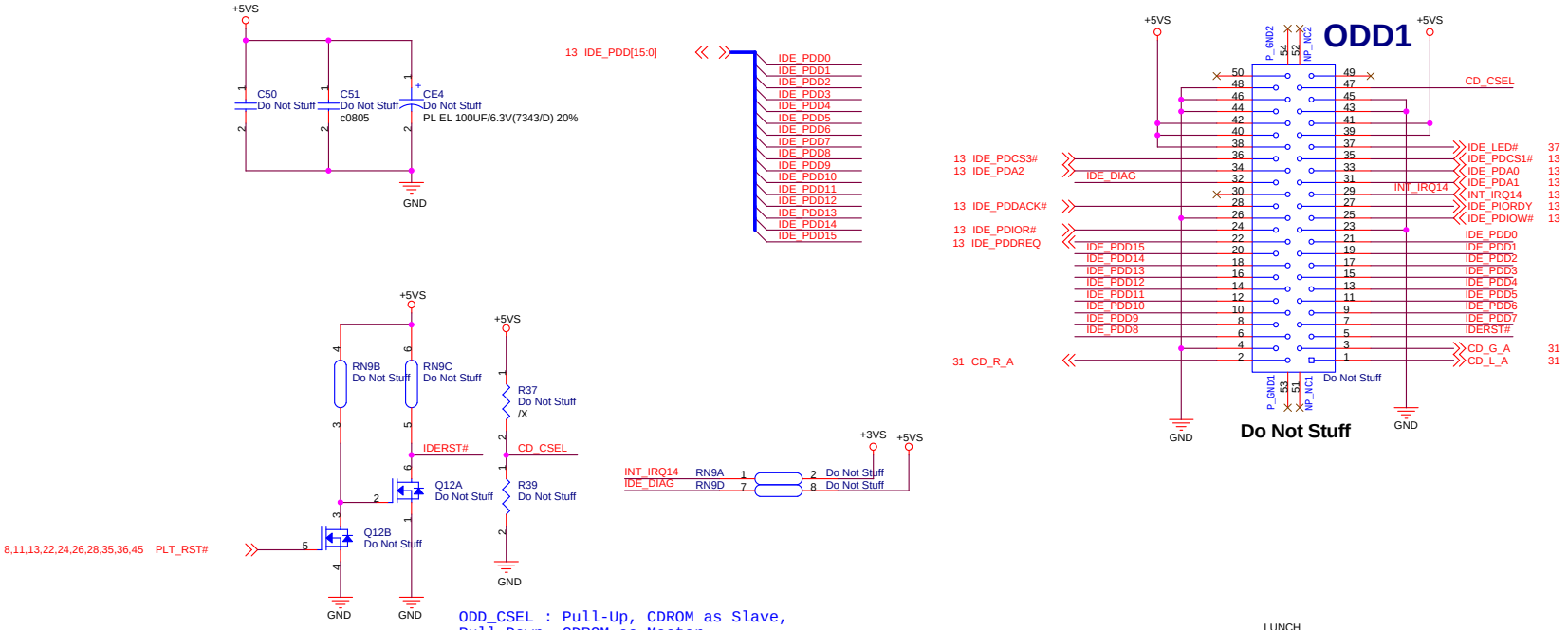
Size	Project Name	Rev
Custom	Z62H	1.0

Date: Monday, August 13, 2007 Sheet 38 of 63

SATA HDD Connector



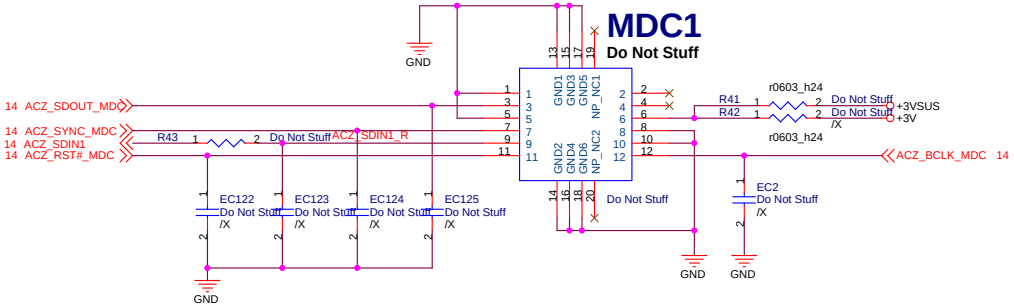
ODD Connector



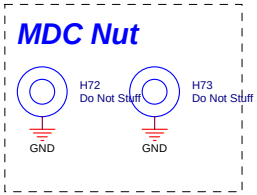
LUNCH

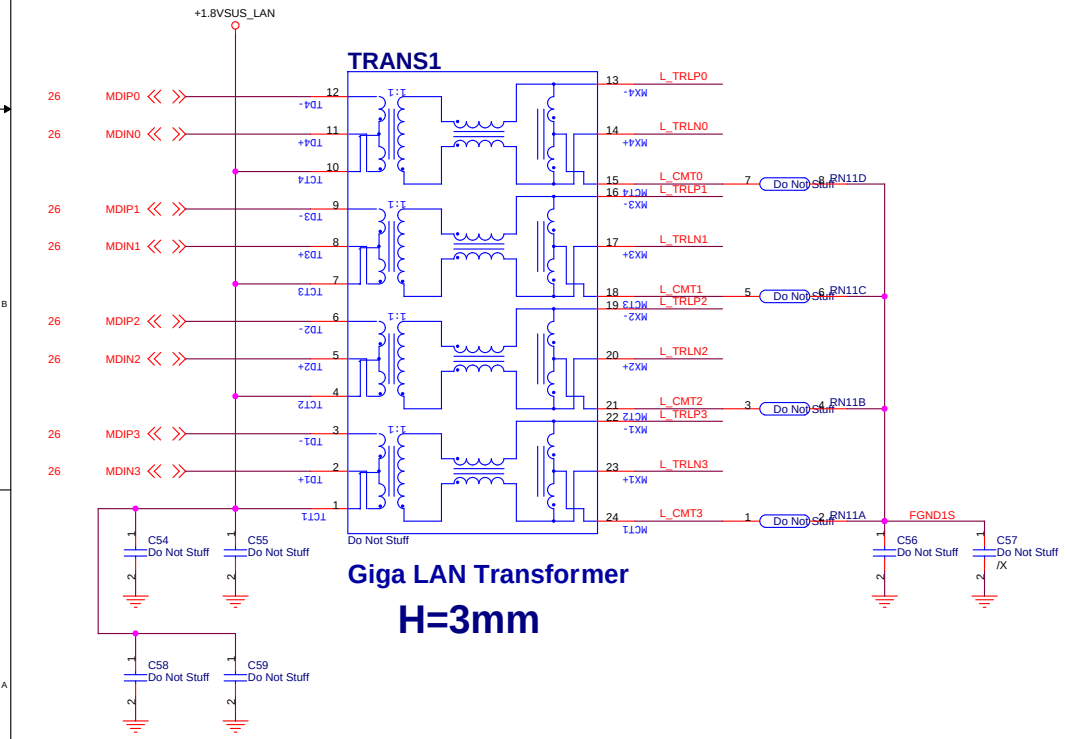
ASUSTek Computer INC.	Title : HDD & ODD	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 39 of 63	

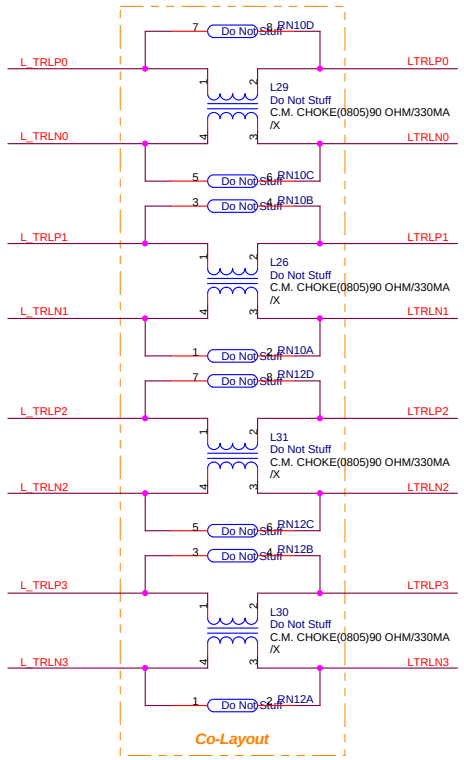
MDC Connector



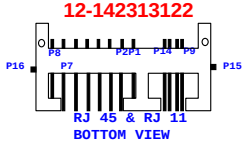
MDC Nut



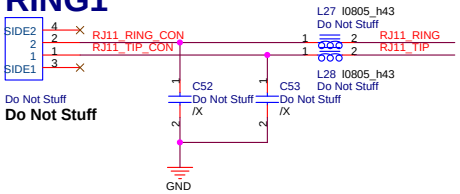




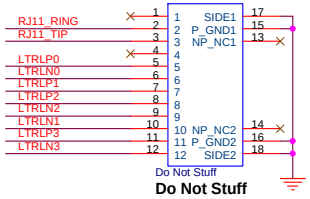
12-142313122



RING1



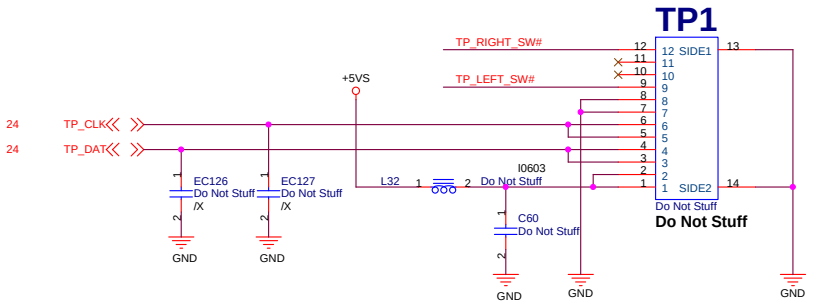
RJ45_11



LUNCH

ASUSTek Computer INC.	Title : MDC_RJ45_RJ11	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 40 of 63	

TouchPad Connector

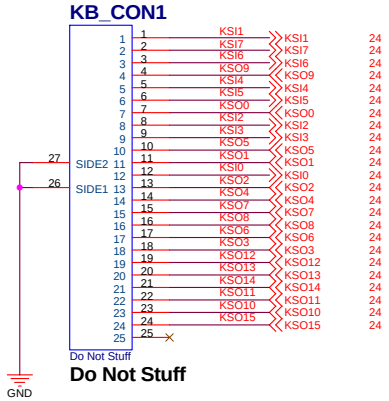


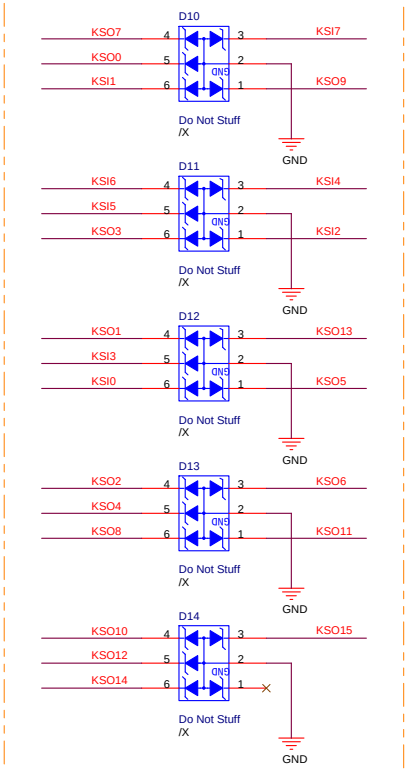
Touch pad Definition

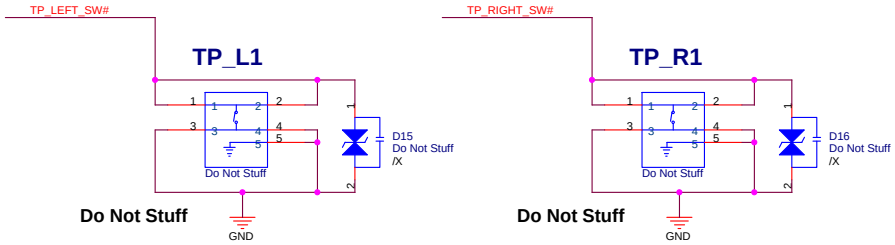
1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD

Z62F: pin1 reversal

Keyboard Connector





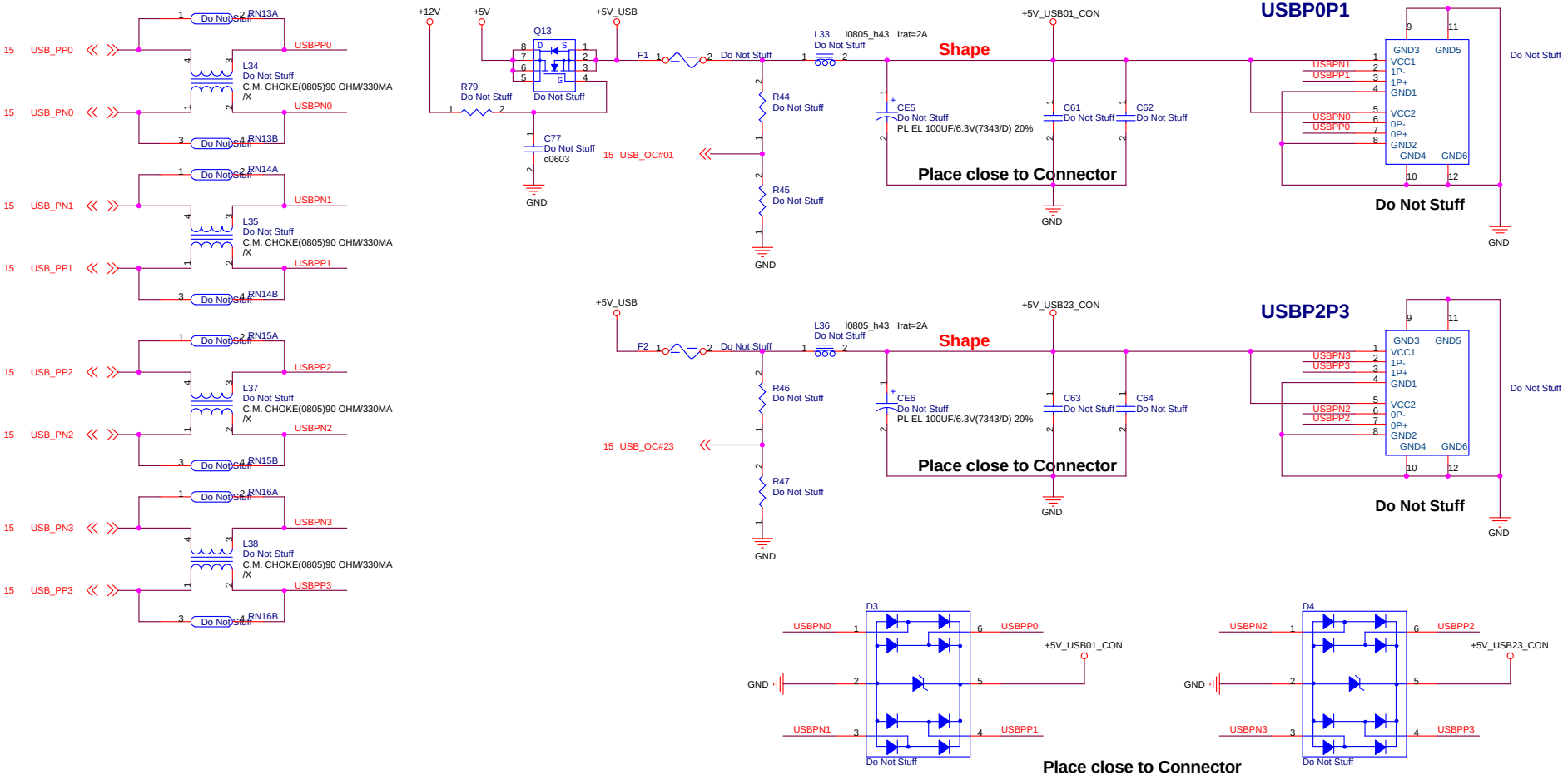


TOUCH PAD SWITCH

LUNCH

ASUSTek Computer INC.	Title : TP / KB Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 41 of 63	

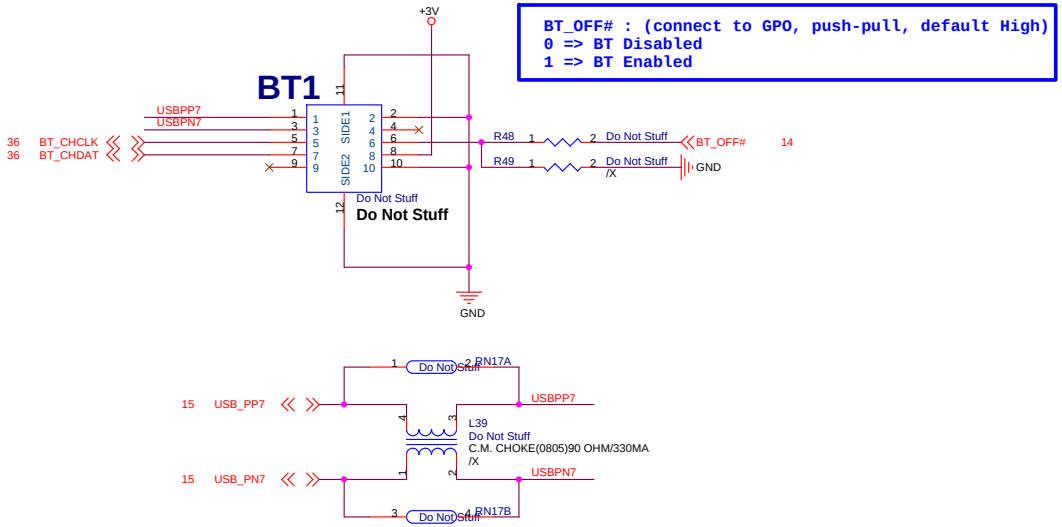
USB Power & OC Alert



LUNCH

ASUSTek Computer INC.	Title : USB Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 42 of 63	

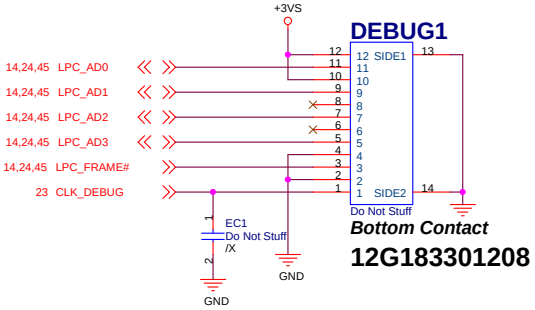
Bluetooth Connector



LUNCH

ASUSTek Computer INC.	Title : Bluetooth Conn.	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 43 of 63	

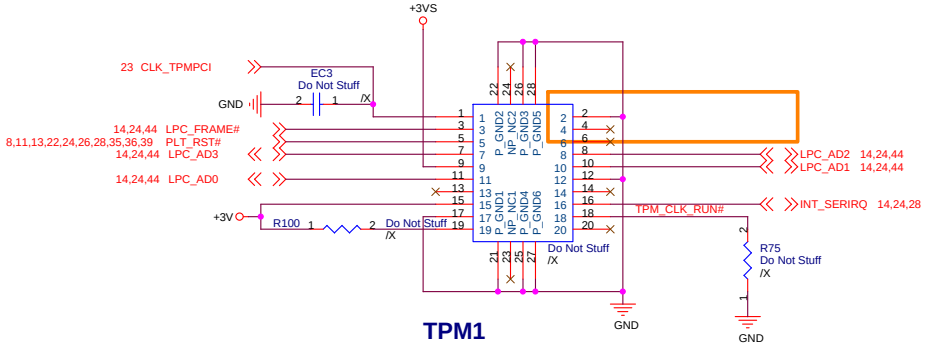
Debug Connector



LUNCH

ASUSTek Computer INC.	Title : Debug Port	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 44 of 63	

TPM Connector



TPM1

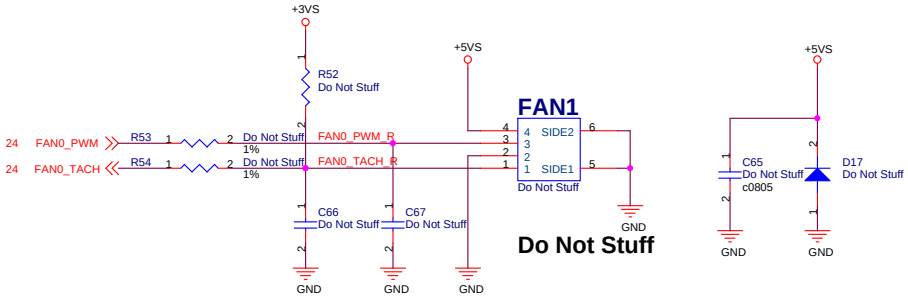
12G16080020J

Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
Removed!!

TPM Nut

LUNCH

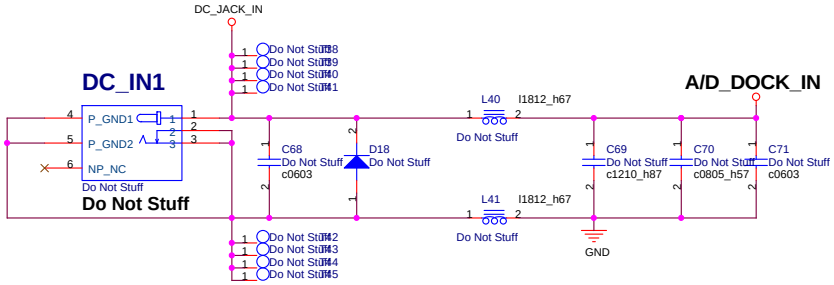
ASUSTek Computer INC.	Title : TPM Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 45 of 63	

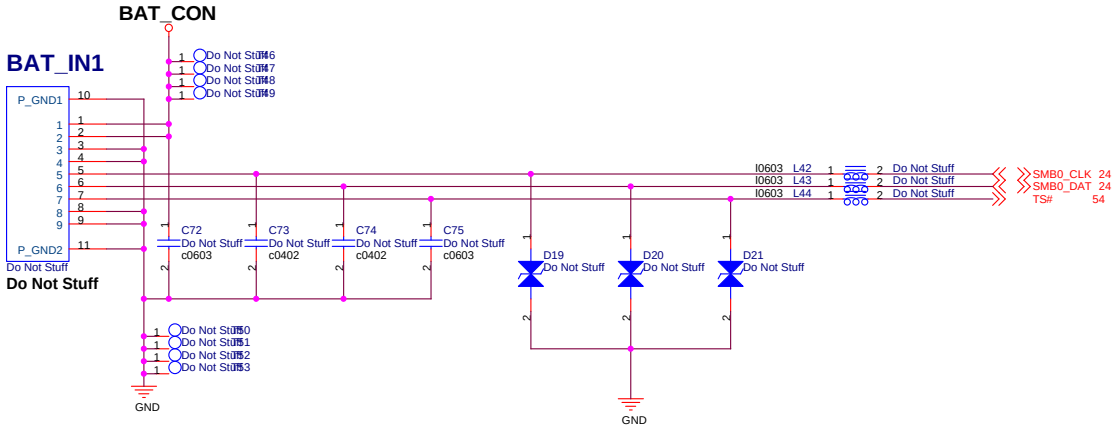


SYSTEM Fan Connector

LUNCH

ASUSTek Computer INC.	Title : Fan Connector	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 46 of 63	





LUNCH

ASUSTek Computer INC.	Title : DC-IN & BAT-IN	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 47 of 63	

LUNCH

Title : BLANK

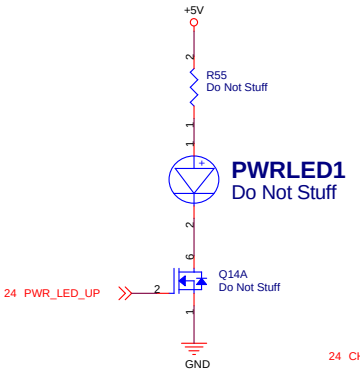
ASUSTek Computer INC.

Engineer: Jack Hsu

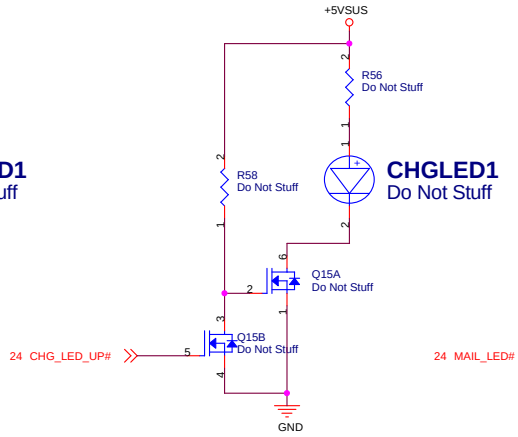
Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 48 of 63

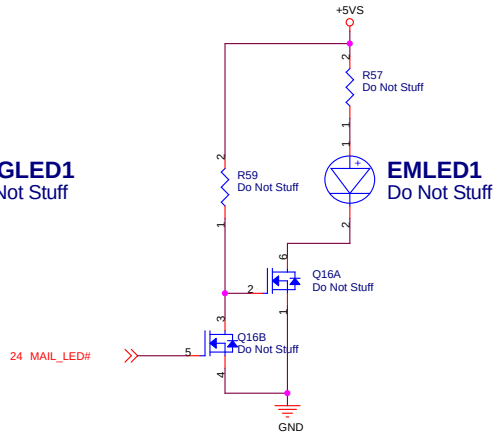
POWER LED



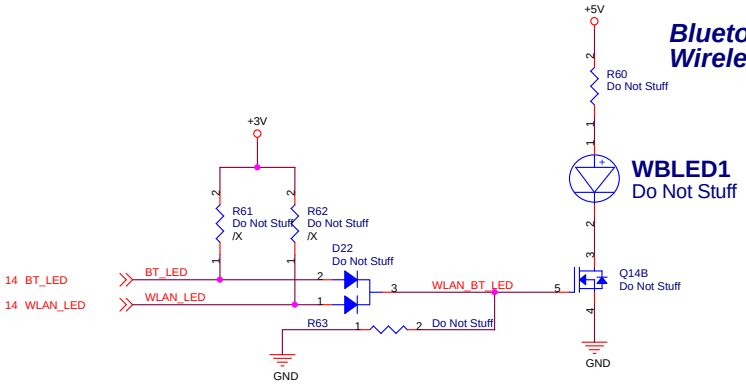
Battery Charge LED



Email LED

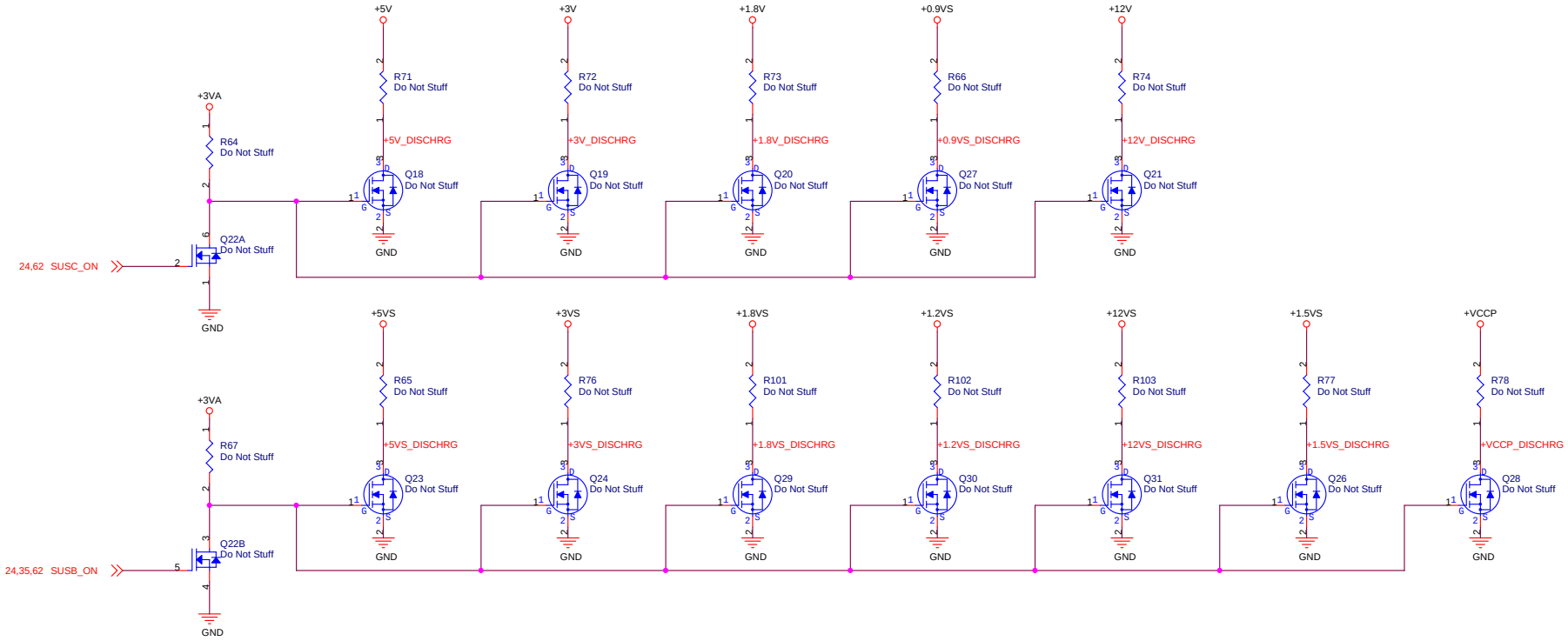


Bluetooth LED
Wireless LED



LUNCH

ASUSTek Computer INC.	Title : LED	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 49 of 63	



LUNCH

ASUSTek Computer INC.	Title : Discharger	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
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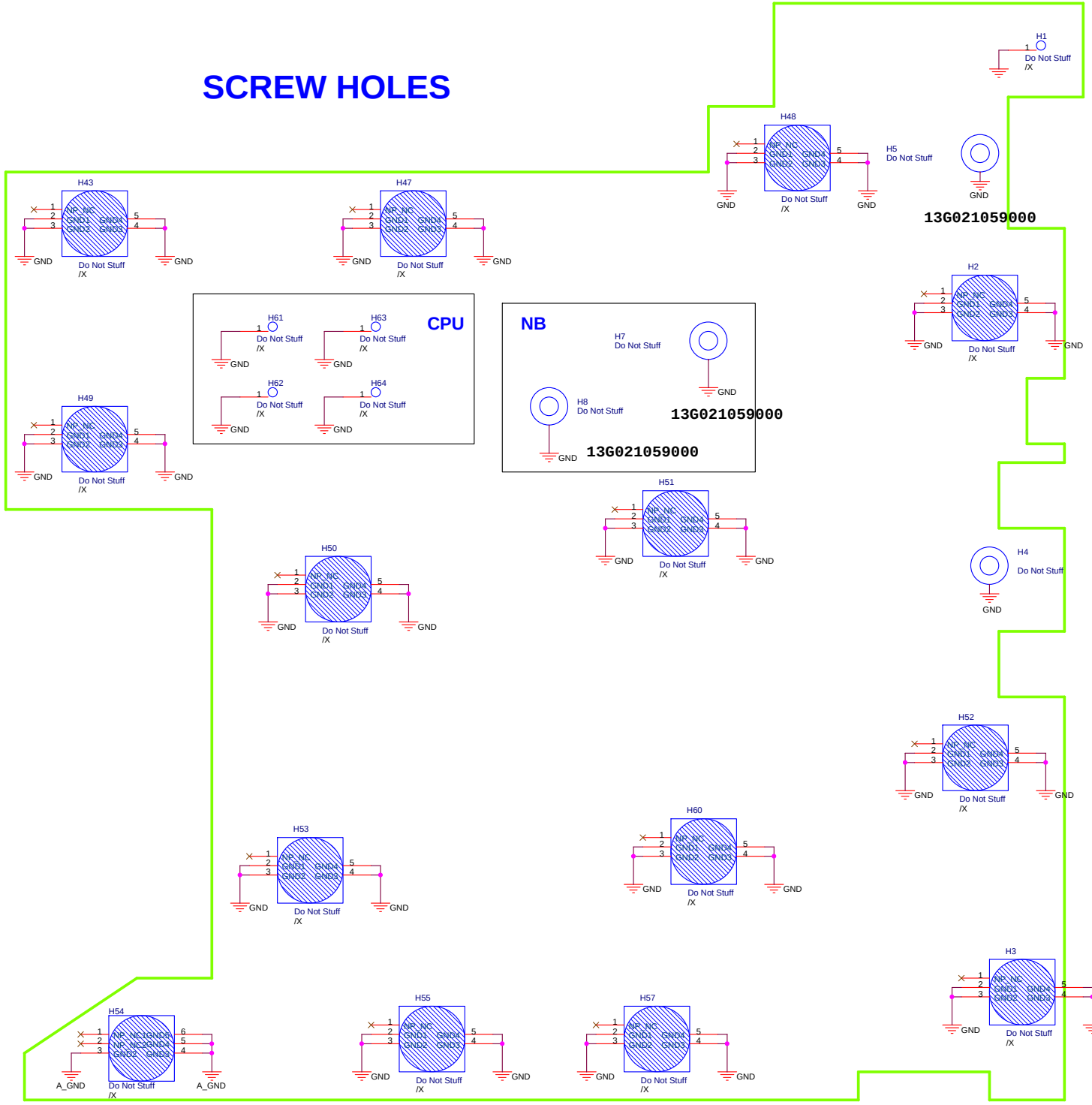
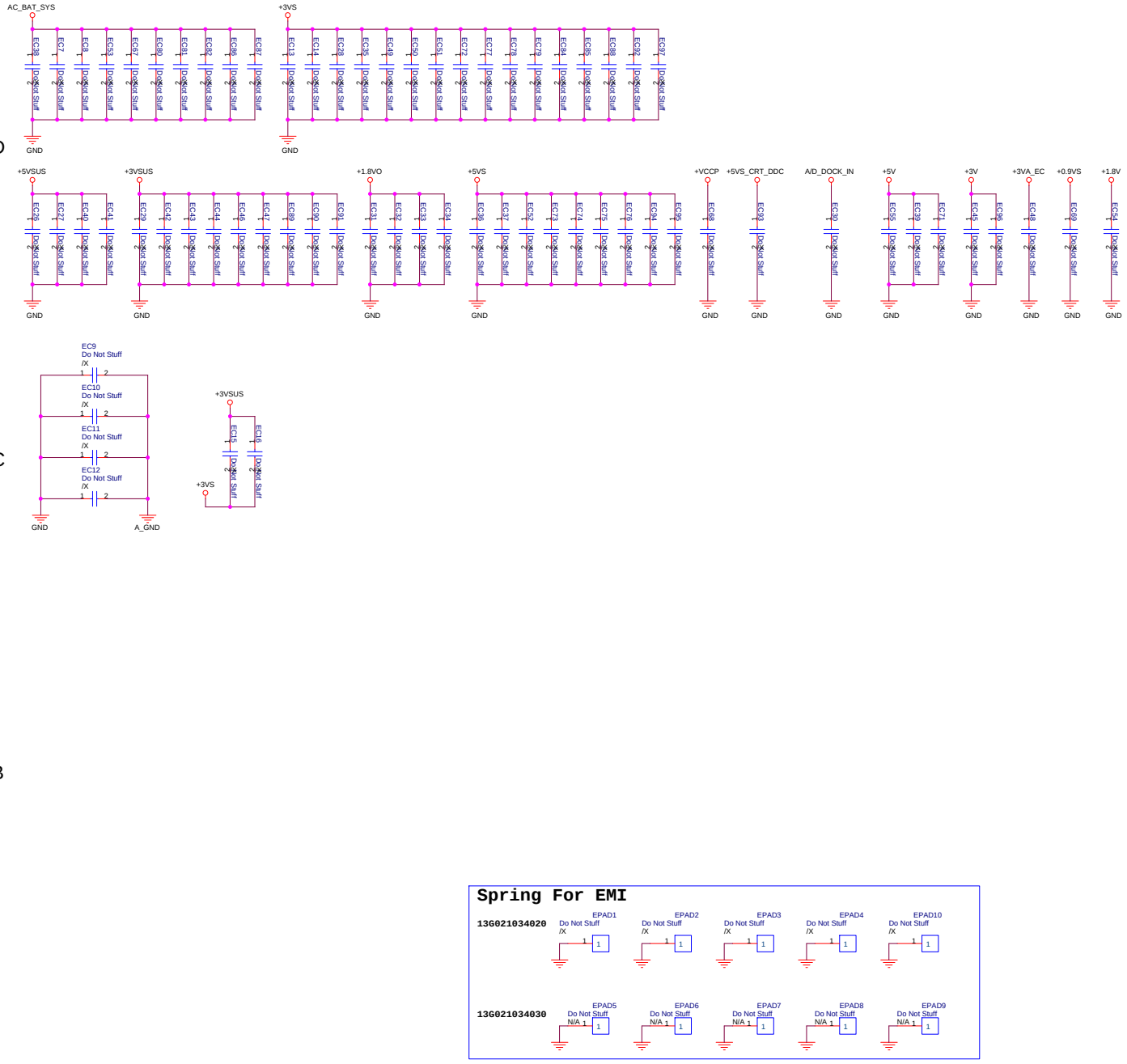
SCREW HOLES



LUNCH

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: Jack Hsu	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Thursday, August 09, 2007	Sheet 51 of 63	



Spring For EMI

136021034020

EPAD1 Do Not Stuff /X

EPAD2 Do Not Stuff /X

EPAD3 Do Not Stuff /X

EPAD4 Do Not Stuff /X

EPAD10 Do Not Stuff /X

136021034030

EPAD5 Do Not Stuff N/A

EPAD6 Do Not Stuff N/A

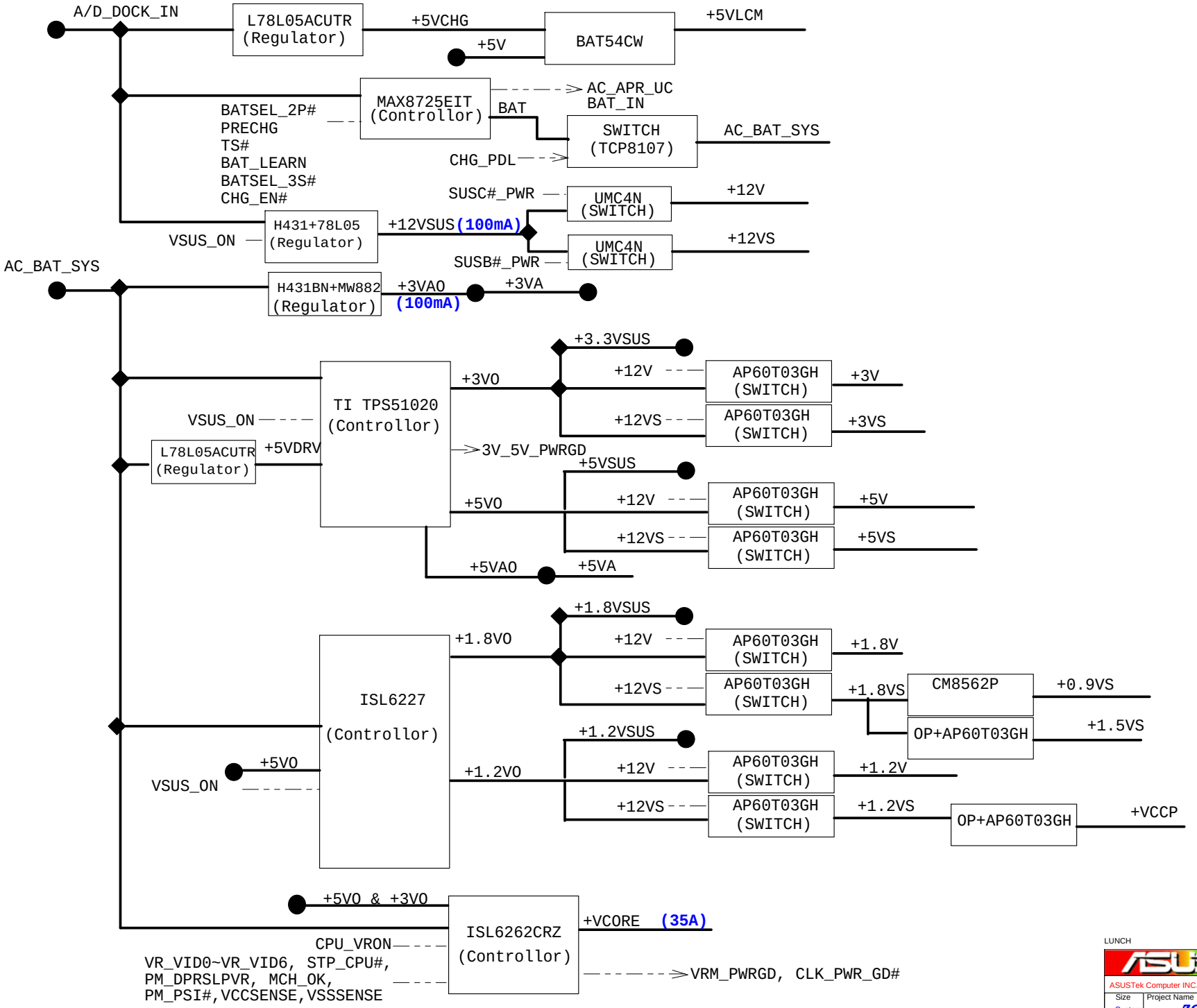
EPAD7 Do Not Stuff N/A

EPAD8 Do Not Stuff N/A

EPAD9 Do Not Stuff N/A

LUNCH

ASUSTek Computer INC.	Title : EMI CAP	
	Engineer: Jack Hsu	
Size: C	Project Name: Z62H	Rev: 1.0
Date: Friday, August 10, 2007	Sheet 52 of 63	



LUNCH

Title : POWER_FLOWCHART

ASUSTek Computer INC.

Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 53 of 63

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

Adaptor Max. Current :

PR5708=20K PR5714 = 178K; Ilimit = 4.5A; 81W

PR5708=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

Victl = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V

=> Icharge = 2.9329A

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

BATSEL_2P# = 1, 3 Cells

BATSEL_2P# = 0, 6 or 9 Cells

PRECHG = 1, Pre-Charging Mode

Charging Current = 156mA

CHG_EN# = 1, Charger Disabled

CHG_EN# = 0, Charger Enabled

AC_OK = 1, Adaptor is present

AC_OK = 0, Adaptor is absent

BAT_LEARN = 1, Battery discharges

BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

BAT_IN_OC# = 1; Battery absence

BAT_IN_OC# = 0; Battery Plug-in

TS# = 1; Battery absence

TS# = 0; Battery Plug-in

LUNCH

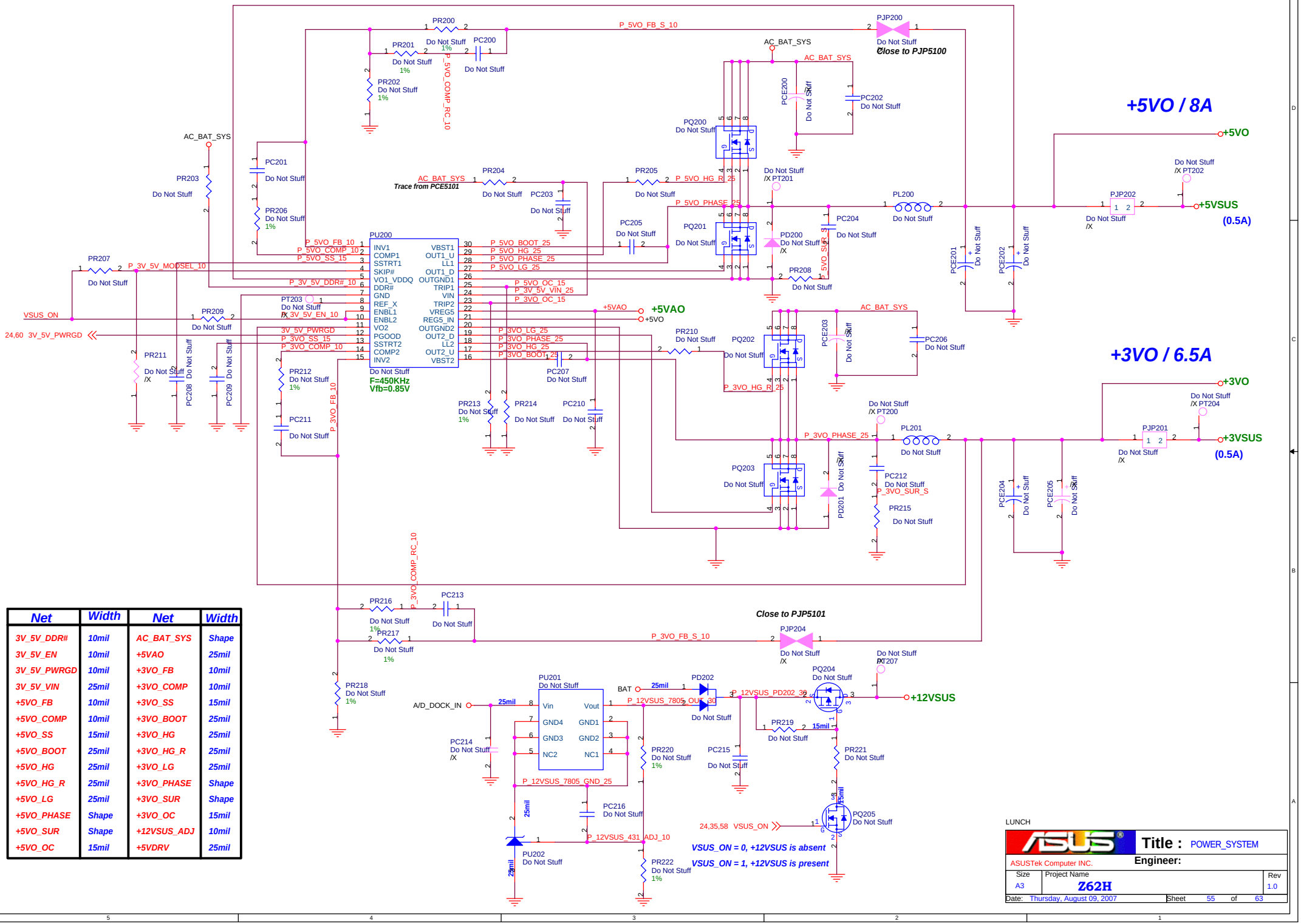
ASUSTek Computer INC.

Title : POWER_CHARGER

Engineer:

Size: C | Project Name: 262H | Rev: 1.0

Date: Thursday, August 09, 2007 | Sheet 54 of 63



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

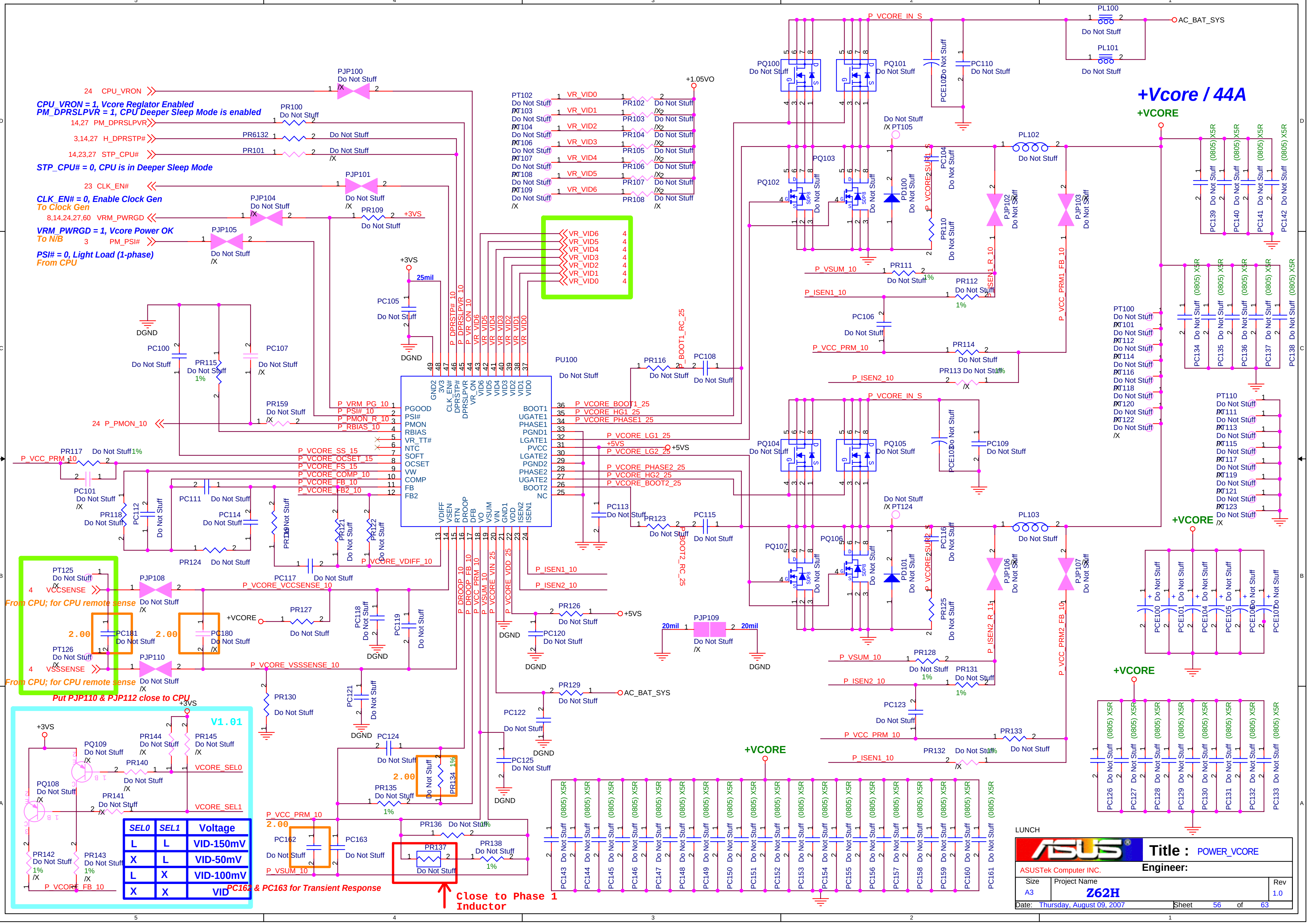
LUNCH

Title : POWER_SYSTEM

ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
A3	Z62H	1.0

Date: Thursday, August 09, 2007 Sheet 55 of 63



SEL0	SEL1	Voltage
L	L	VID-150mV
X	L	VID-50mV
L	X	VID-100mV
X	X	VID

ASUSTek Computer INC.

Title : POWER_VCORE

Engineer:

Size	Project Name	Rev
A3	Z62H	1.0

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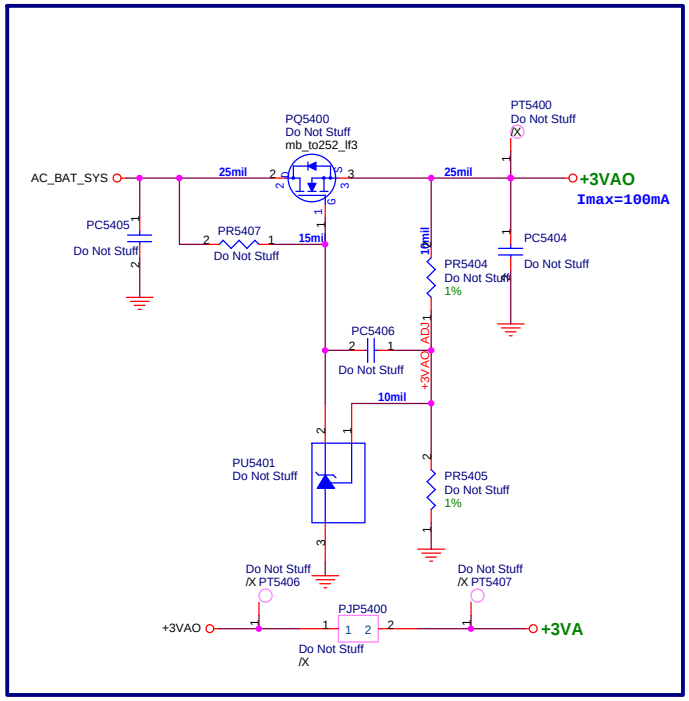
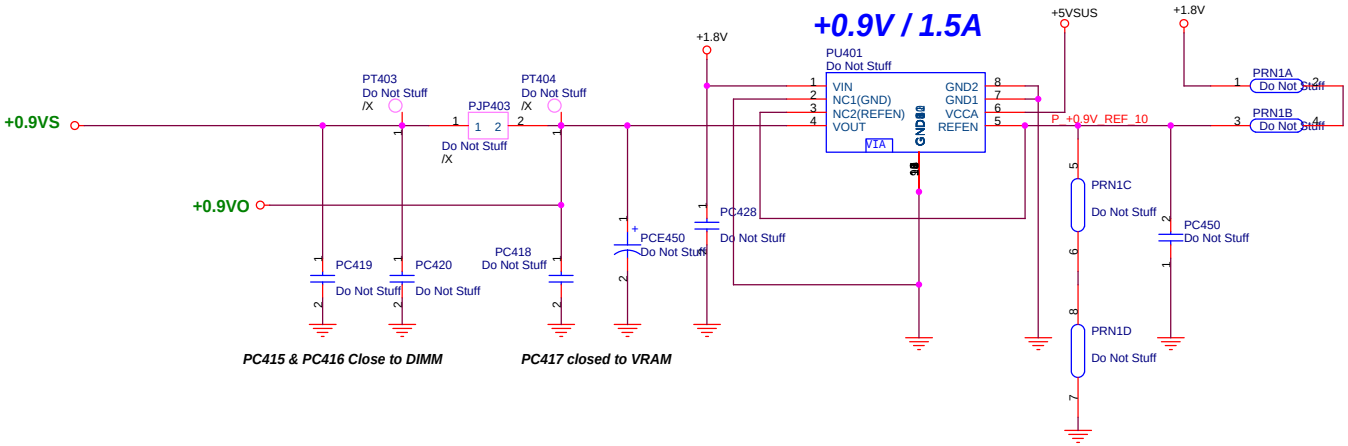
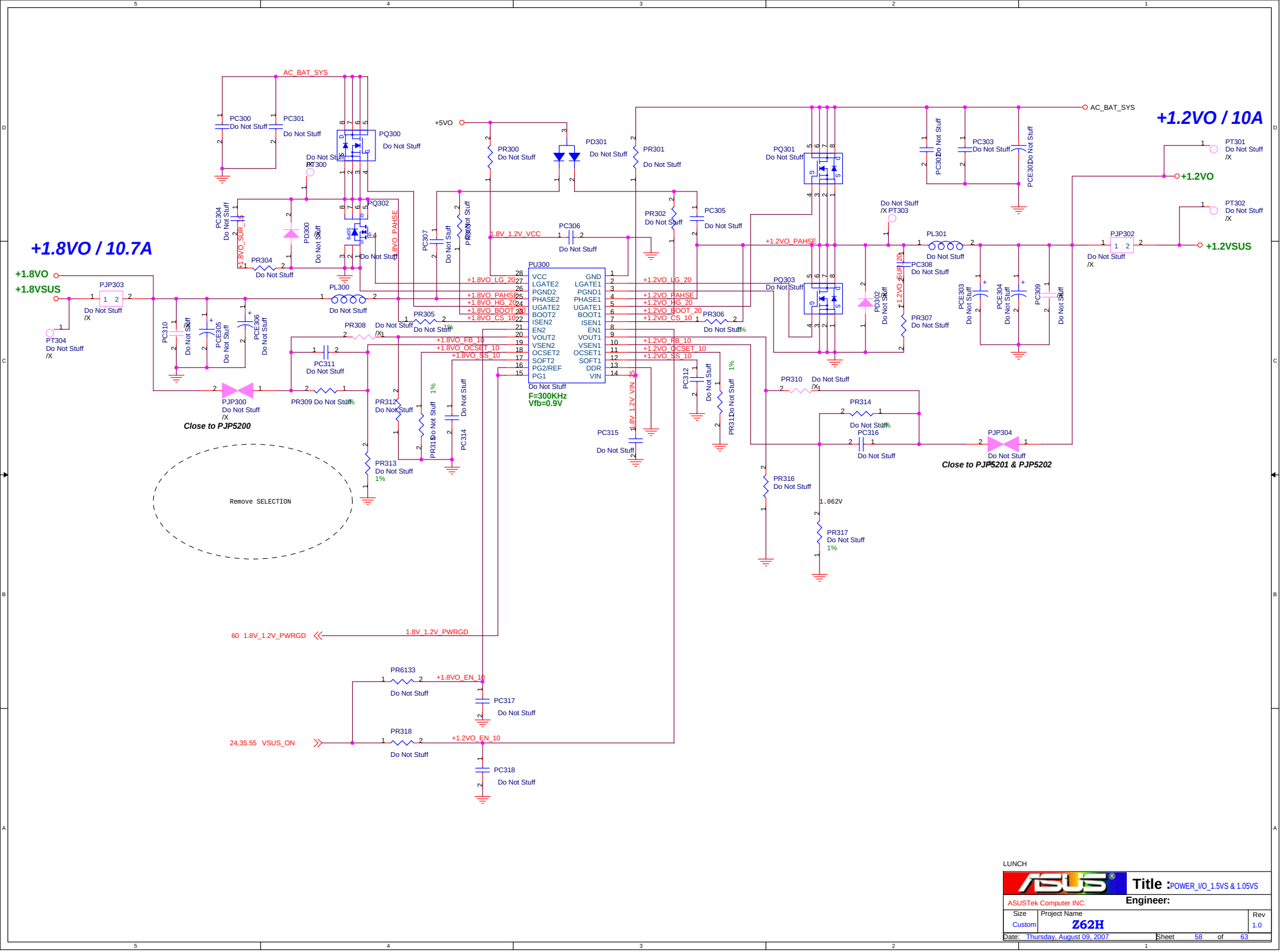


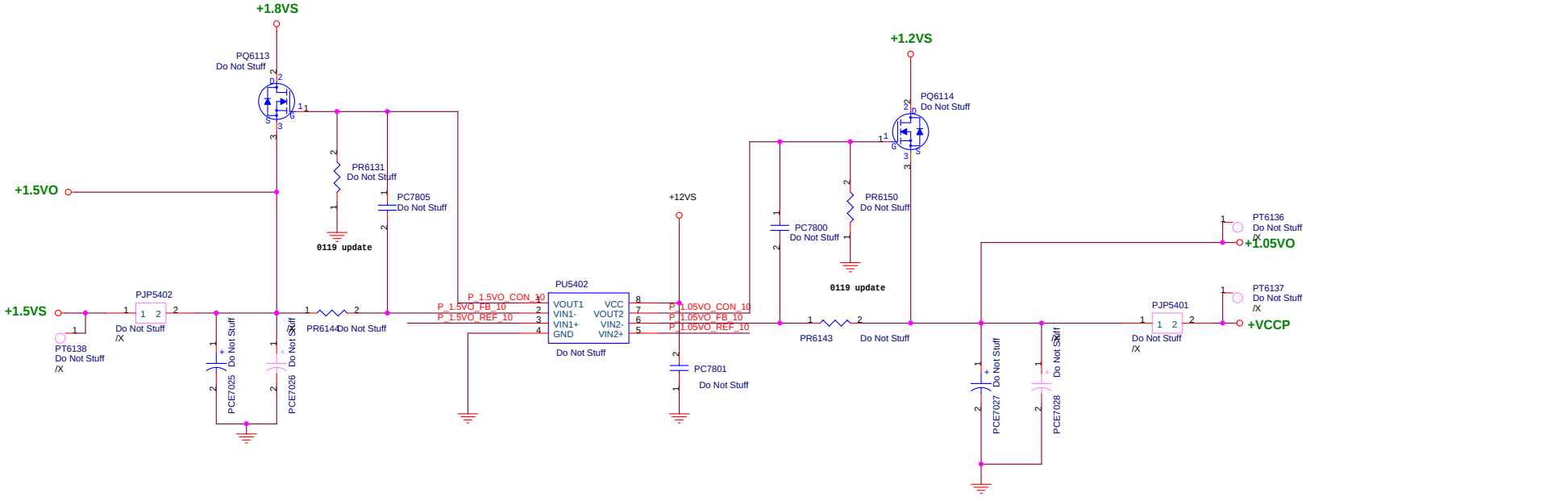


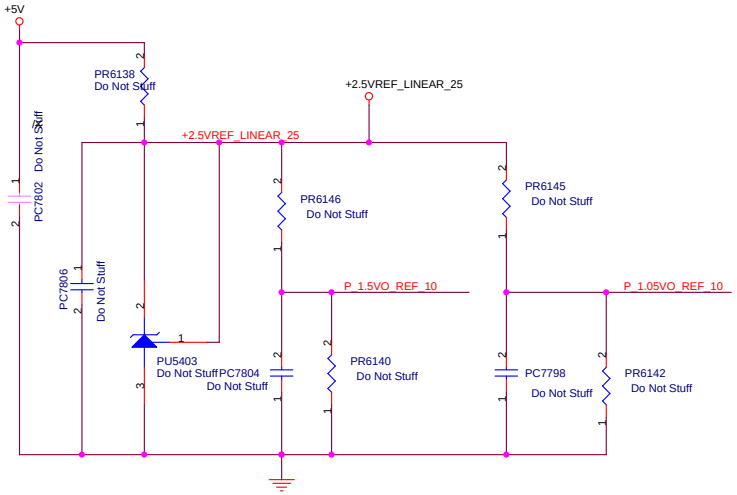
DDR Power Rev:1.00

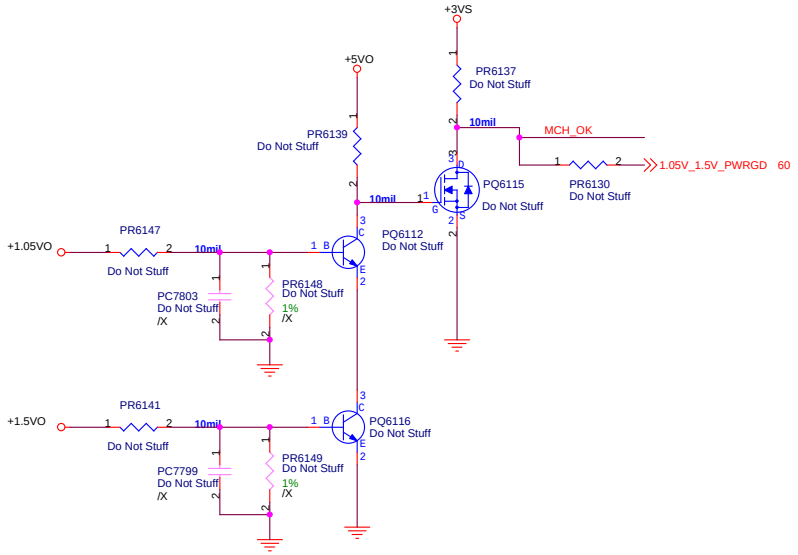
LUNCH

ASUSTek Computer INC.	Title :
	Engineer:
Size: A3	Project Name
Rev: 1.0	
Date: Thursday, August 09, 2007	Sheet 57 of 63


+1.8VO / 10.7A
+1.2VO / 10A
+1.8VO
+1.8VSUS
+1.2VO
+1.2VSUS
AC_BAT_SYS
+5VO
PU300
F=300KHz
Vfb=0.9V
Close to PJP5200
Close to PJP5201 & PJP5202
Remove SELECTION
1.062V
60 1.8V_1.2V_PWRGD
24,35,55 VSUS_ON
LUNCH
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTek Computer INC.
Engineer:
Size Custom
Project Name Z62H
Rev 1.0
Date: Thursday, August 09, 2007
Sheet 58 of 63







LUNCH

ASUSTek Computer INC.	Title : POWER_I/O_+3VA & +2.5V	
	Engineer:	
Size: Custom	Project Name: Z62H	Rev: 1.0
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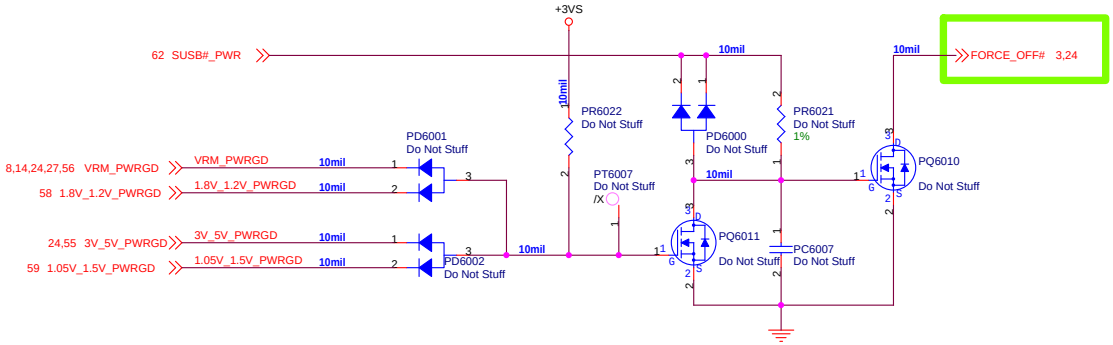
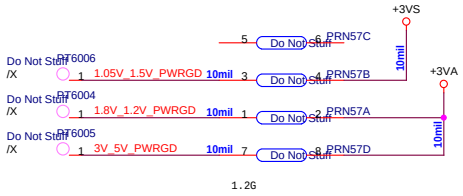
Power Good Detecter





1.26

LUNCH

ASUSTek Computer INC.	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: Z62H	Rev: 1.0
Date: Friday, August 10, 2007	Sheet 60 of 63	

LUNCH

ASUSTek Computer INC.	Title : POWER_BLANK	
	Engineer:	
Size: Custom	Project Name: Z62H	Rev: 1.0
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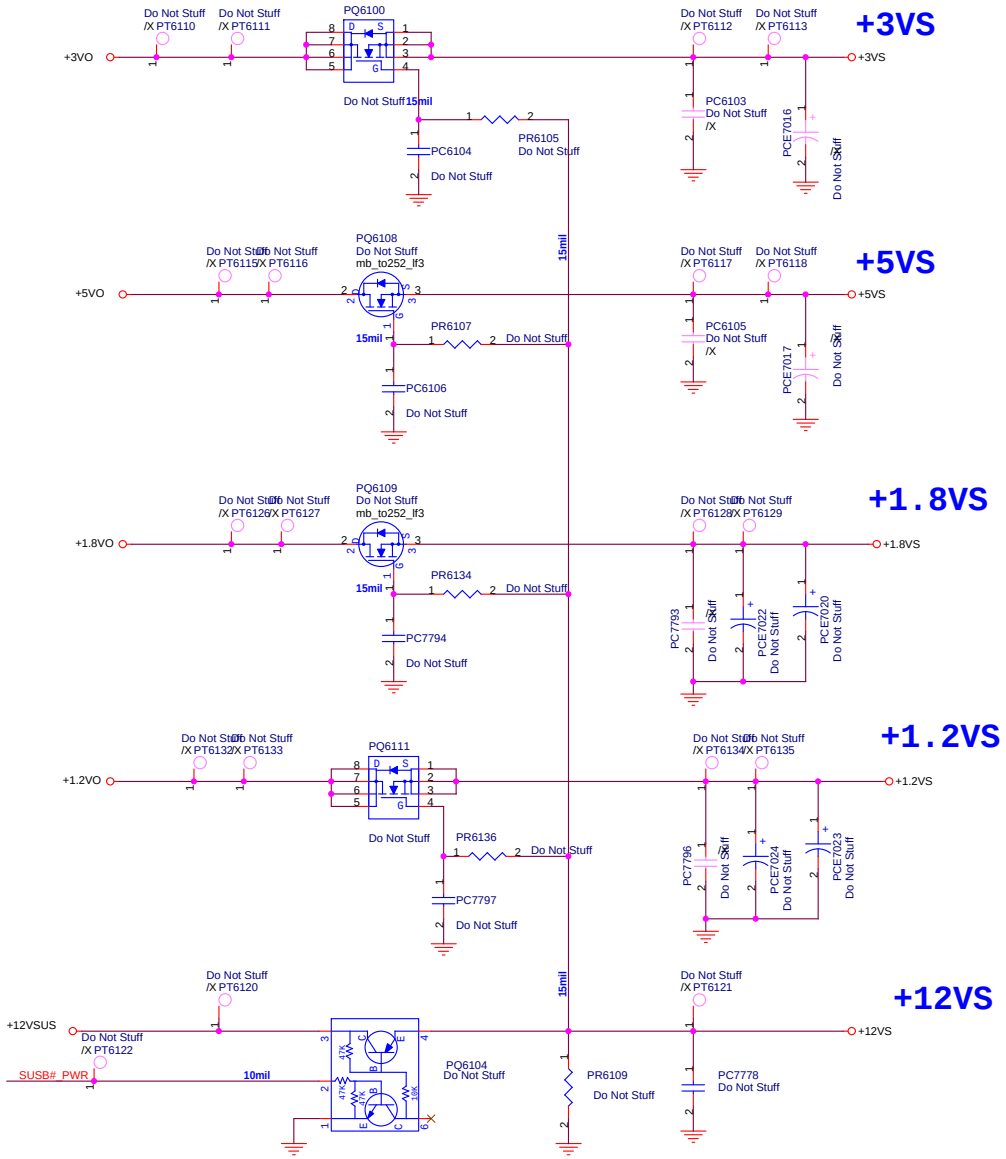
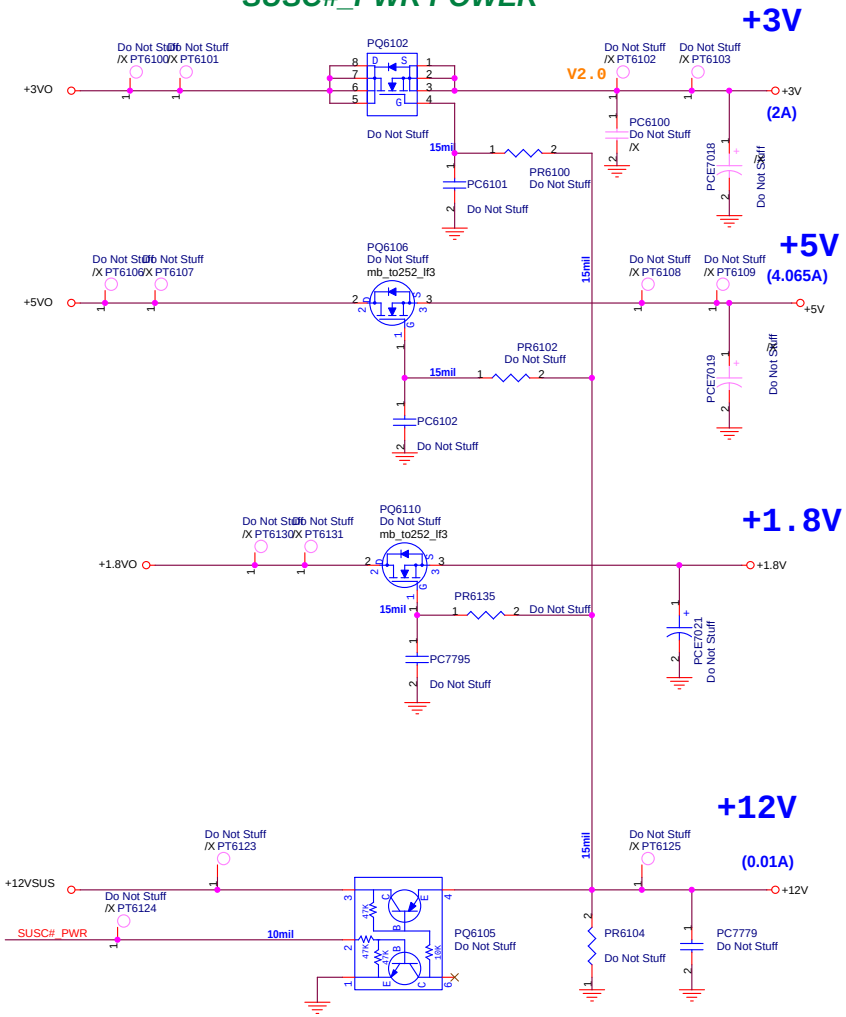
SUSB#_PWR POWER



SUSC#_PWR POWER



LUNCH

ASUSTek Computer INC.

Title : POWER_LOAD SWITCH

Engineer:

Size	Project Name	Rev
Custom	Z62H	1.0

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Rev	Date	Description
1.0	2007/02/14	1. Initial release.
1.1	2007/05/29	1. Change to SiSM672, SiS968, SiS307

Rev	Date	Description

LUNCH

ASUSTek Computer INC.

Title : History

Engineer: *Chihwan*

Size	Project Name	Rev
Custom	**Z62H**	1.0

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