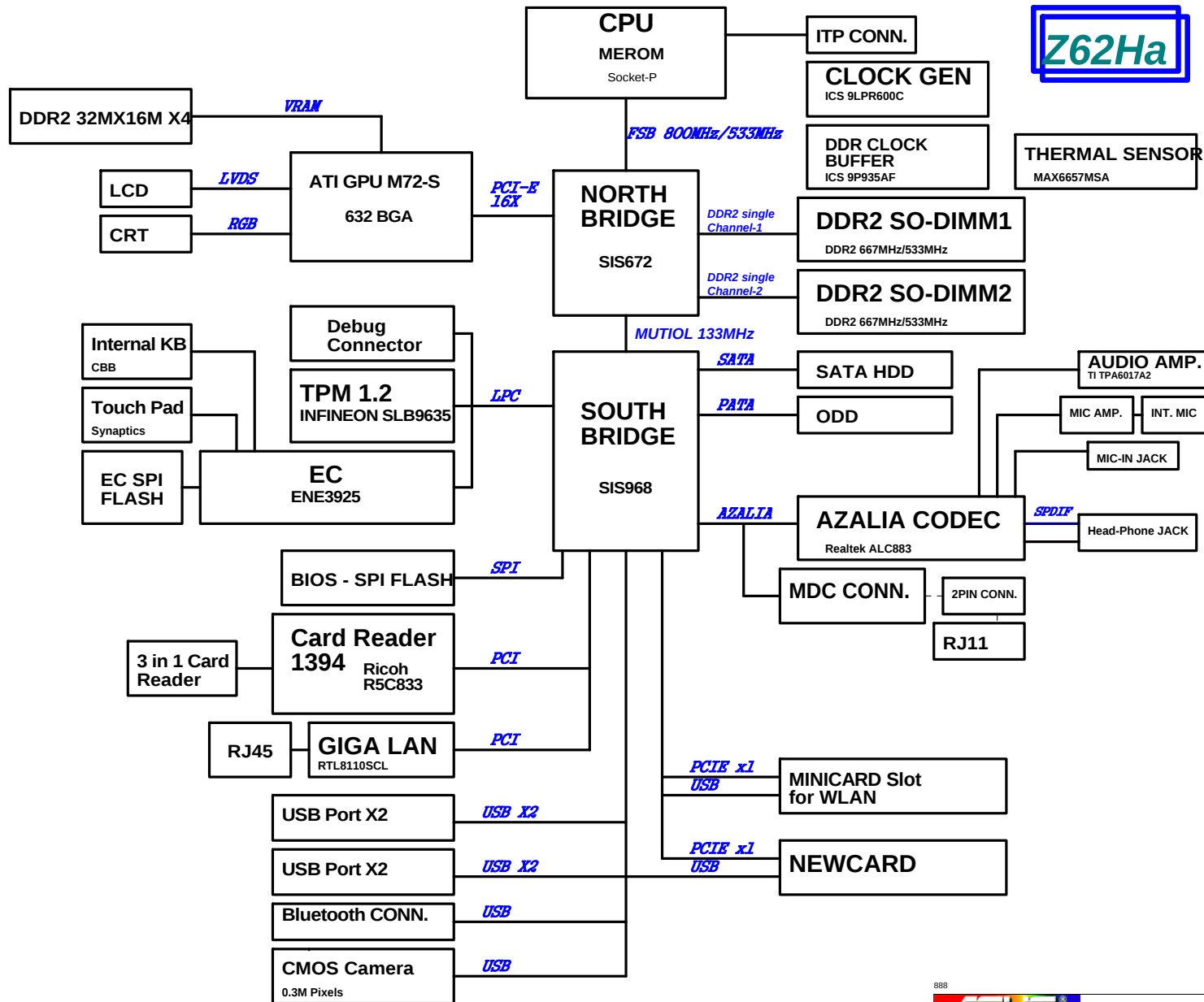




Z62Ha

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSERVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCR_L_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PLT_RST#	I
31	ECSCIN#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GP10	ICH7_PWROK	O
149	GP11	/	
152	GP12	MCHOK	I
155	GP13	CHG_EN#	O
156	GP14	PRECHG	O
168	GP15	BAT_LL#	O
174	GP16	BAT_LEARN	O

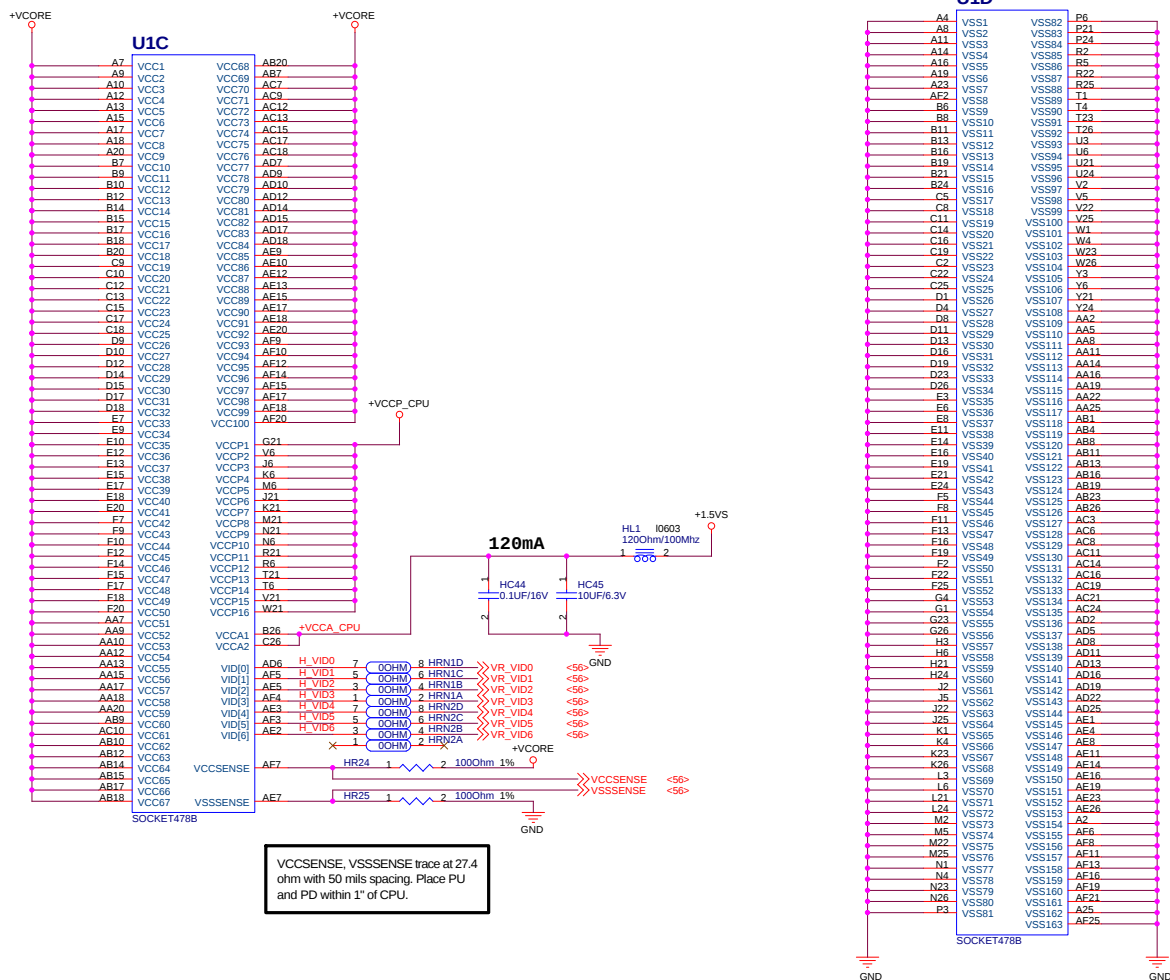
ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSPLVVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

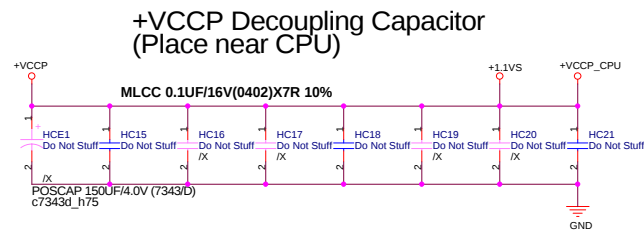
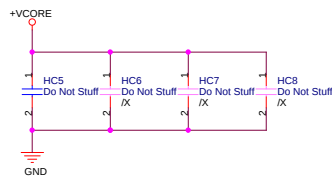
PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD22	0	INTB-->INTB
1394	AD22	0	INTA-->INTA
LAN	AD24	REQ#2/GNT#2	INTA-->INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

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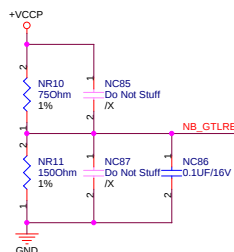
VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



Decoupling guide from INTEL 44A for Merom

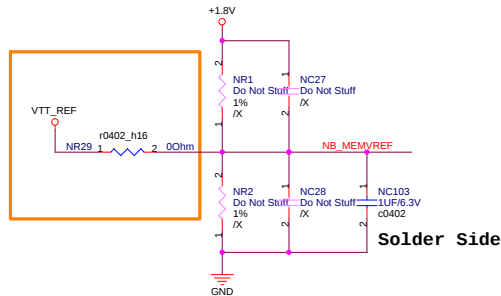
VCCORE 22uF/10V * 32pcs, 330uF/2V * 6pcs
VCCP 0.1uF * 6pcs, 150uF * 1pcs

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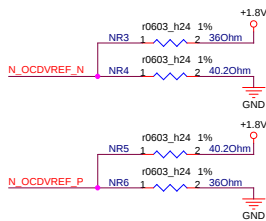


<3> H DPWR#

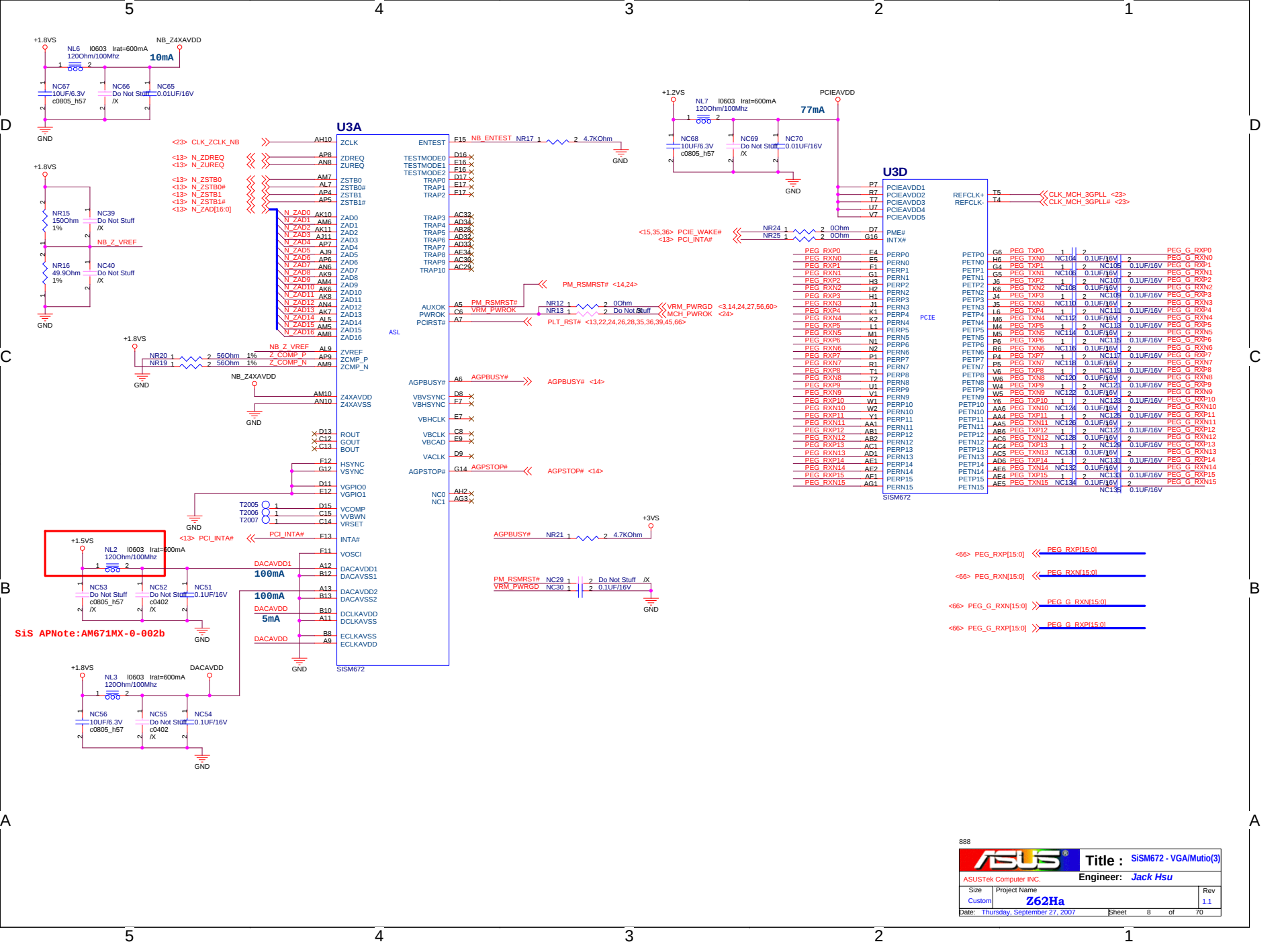


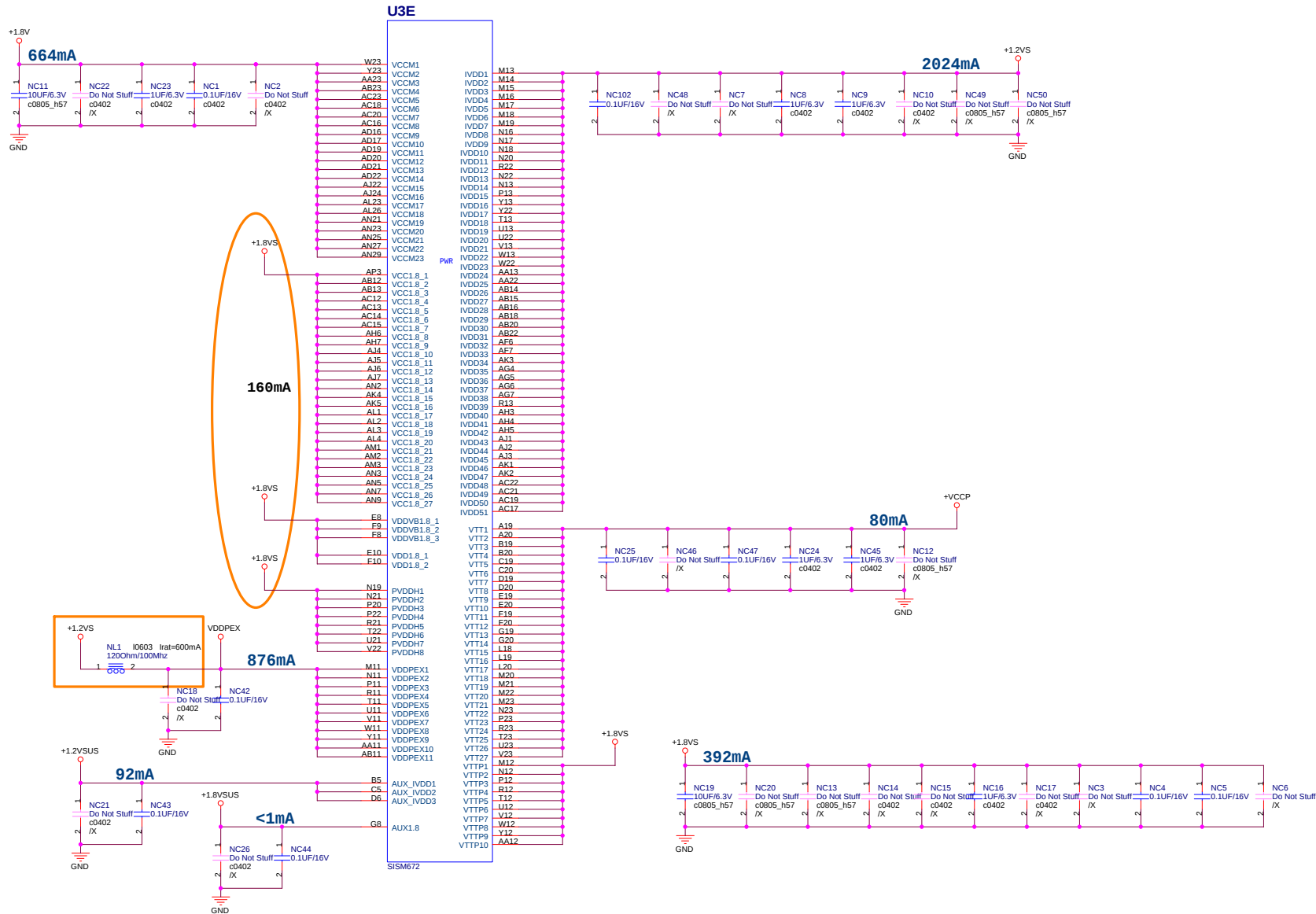


Solder Side

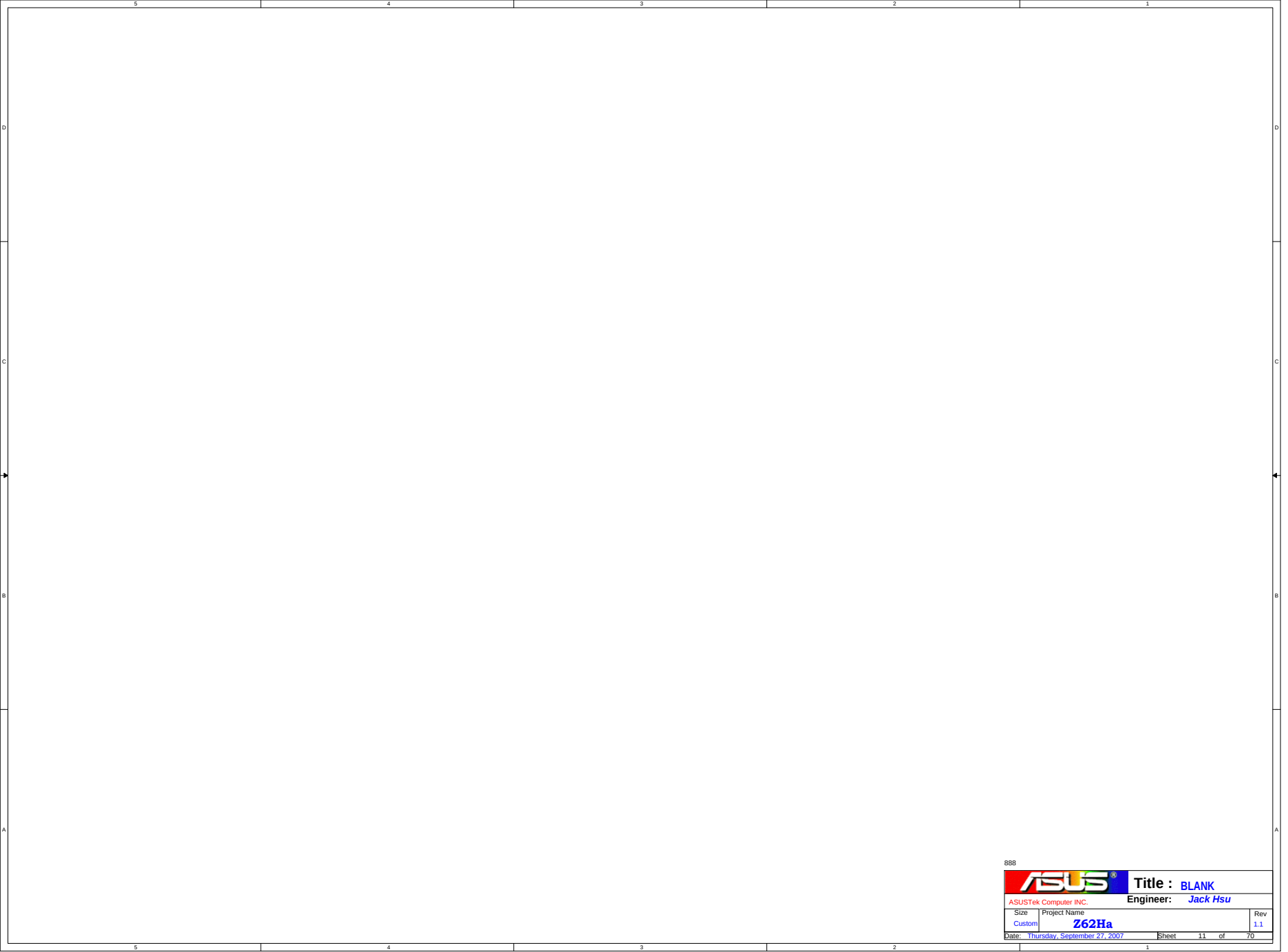
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SISM672



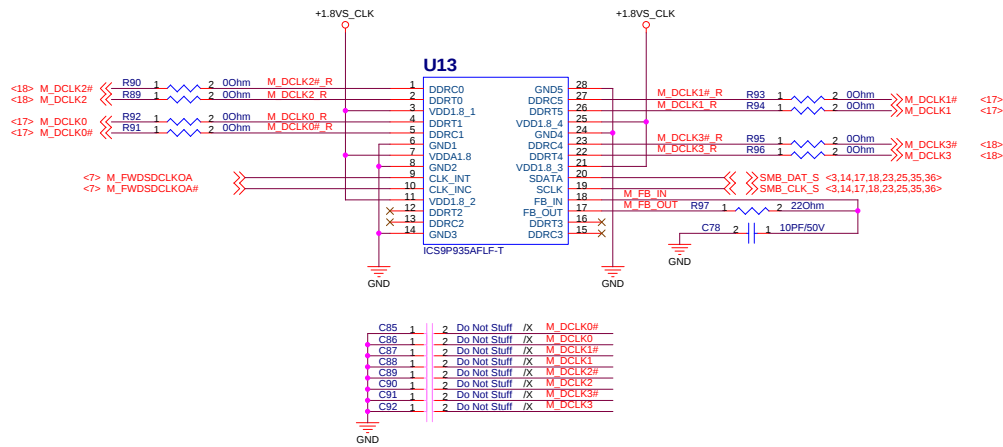
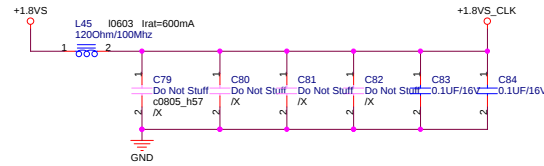


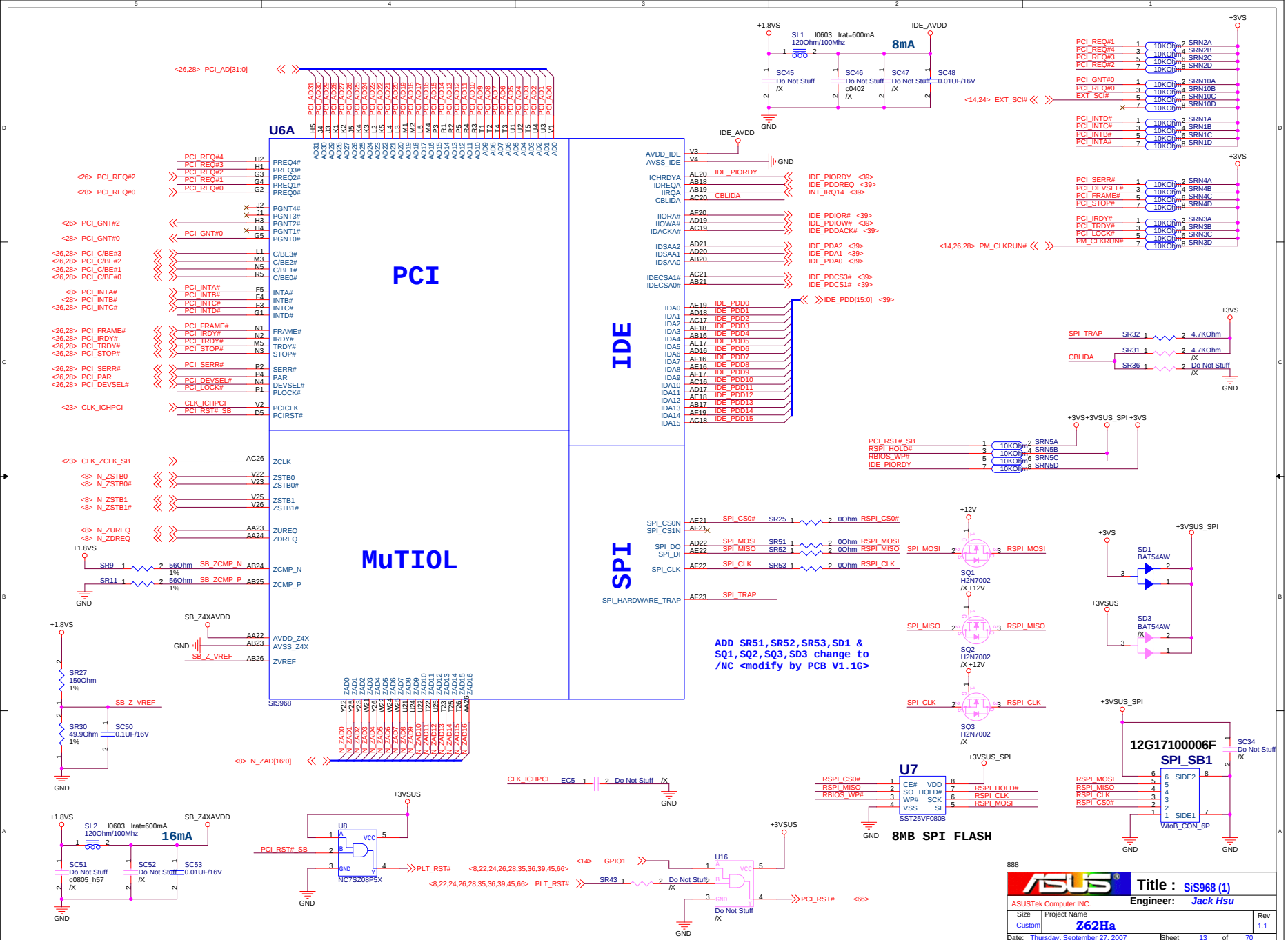
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		Title : BLANK	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007		Sheet	11 of 70

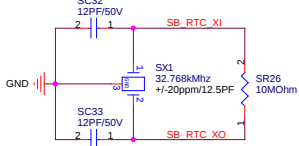
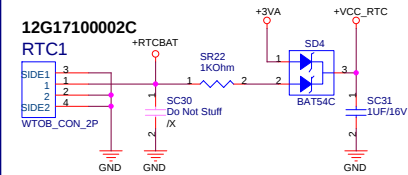




RTC BATTERY

12G17100002C

RTC1

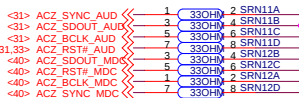


RTC CMOS CLEAR

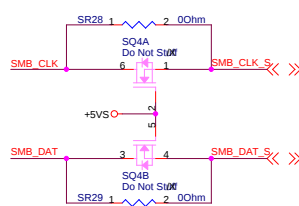
JRST1

Do Not Stuff

Place on the Door Area



SMBus



SMB_CLK, SMB_DAT from pull
+3VSUS change to +3VS
+modify by PCB V1.1G

U6B

CPU_S

APIC

LPC

RTC

SMBUS

HD Audio

ACPI/Others

GPIO

SIS968

GMAC

PCI Express

AVSS_GMACCMP18

AVDD_GMACCMP18

OSC25MH0

OSC25MH1

GTCLK

EXTCLK

TXEN

TXER

TXD0

TXD1

TXD2

TXD3

TXD4

TXD5

TXD6

TXD7

TXD8

TXD9

TXD10

TXD11

TXD12

TXD13

TXD14

TXD15

TXD16

TXD17

TXD18

TXD19

TXD20

TXD21

TXD22

TXD23

TXD24

TXD25

TXD26

TXD27

TXD28

TXD29

TXD30

TXD31

TXD32

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TXD38

TXD39

TXD40

TXD41

TXD42

TXD43

TXD44

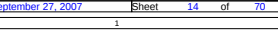
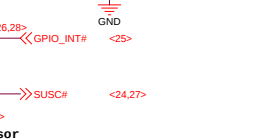
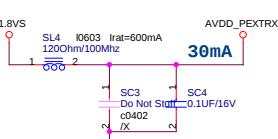
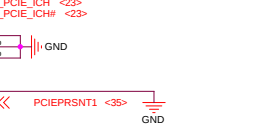
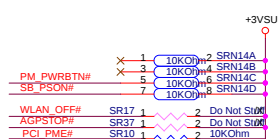
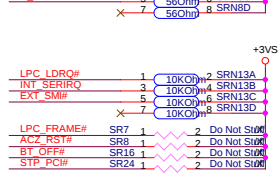
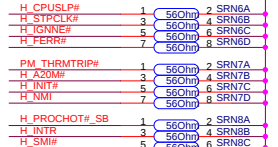
TXD45

TXD46

TXD47

TXD48

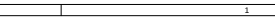
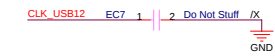
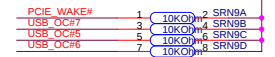
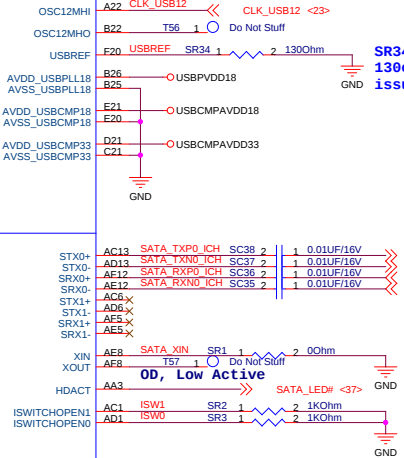
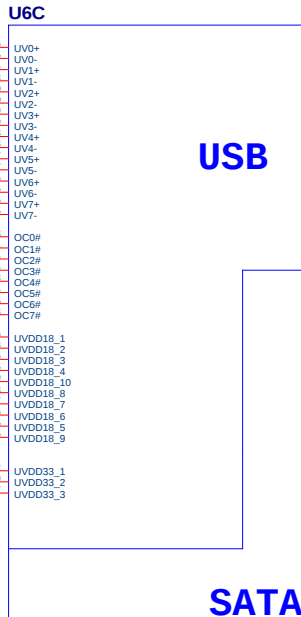
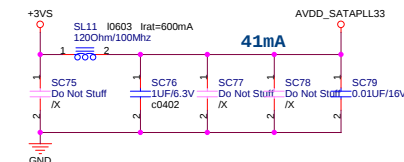
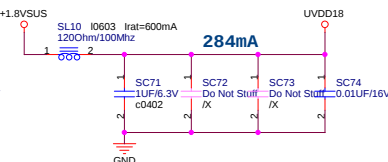
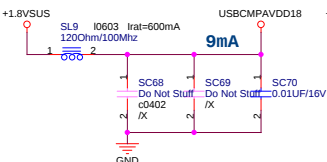
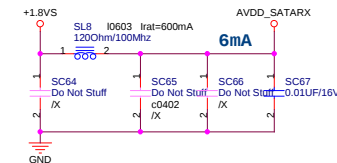
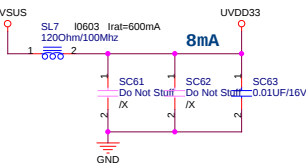
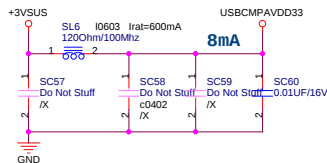
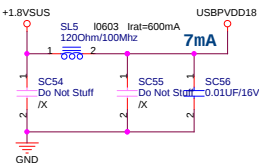
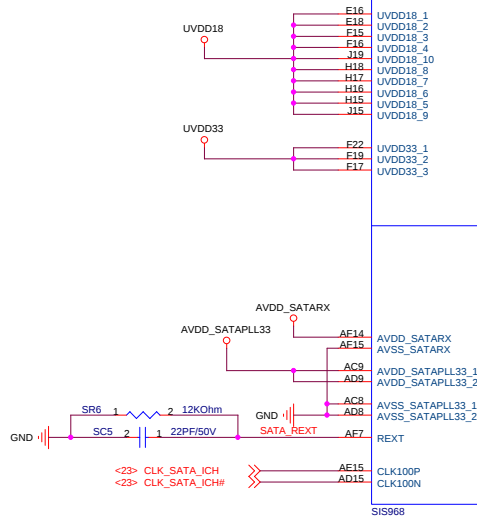
TXD49

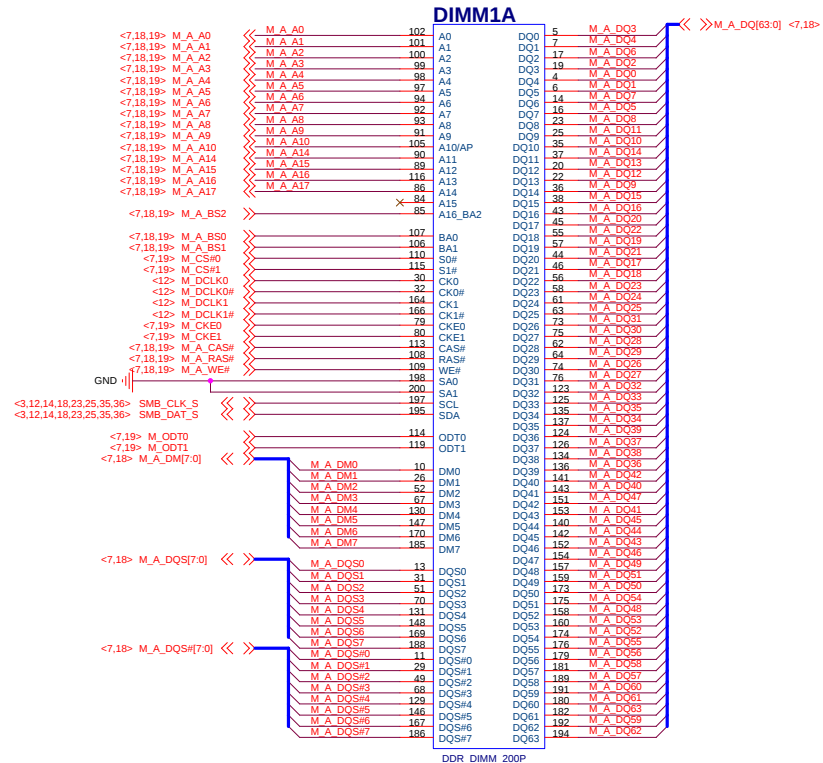


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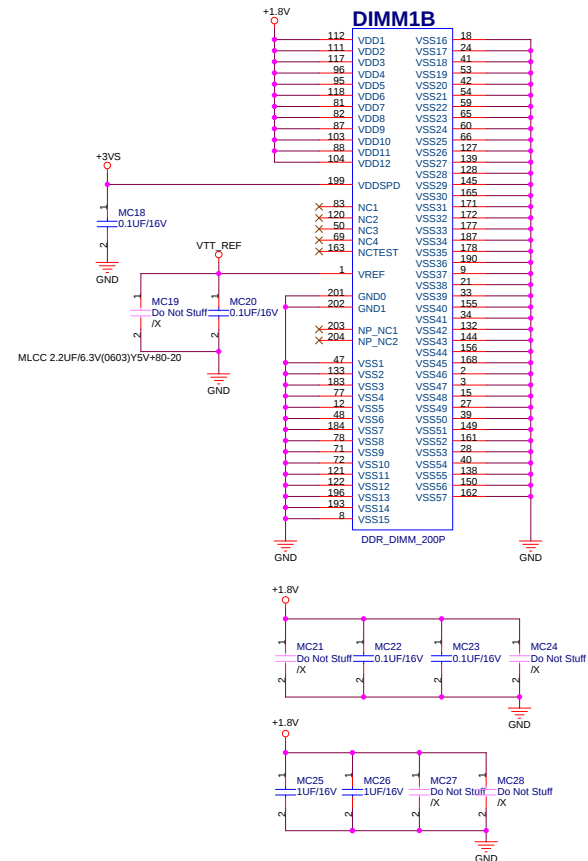
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB NEWCARD
USB 5	USB MINICARD
USB 6	CMOS Camera
USB 7	Bluetooth

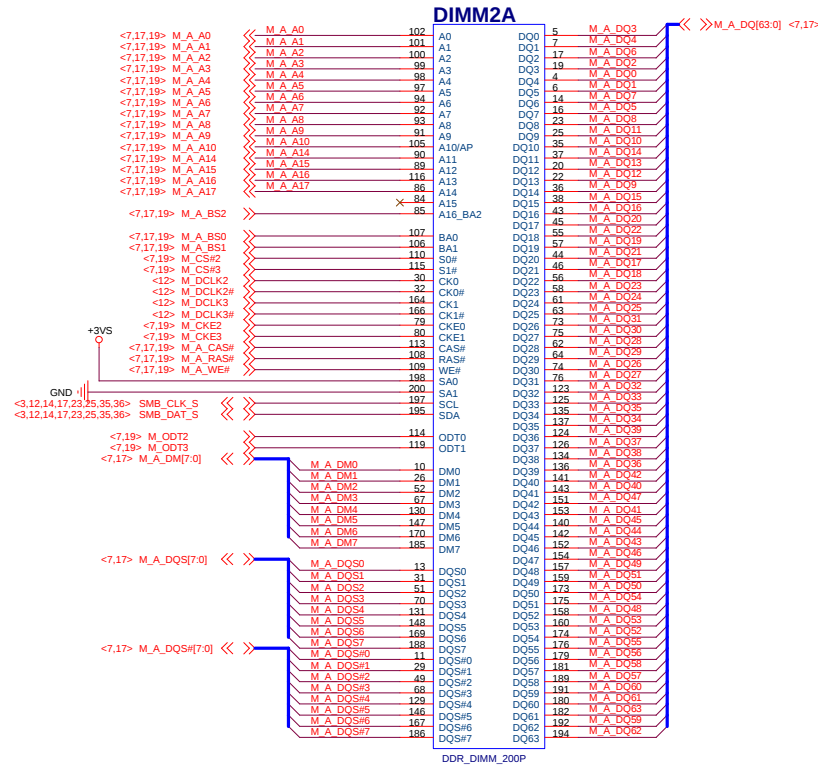
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 <35> NEWCARD_OC#4



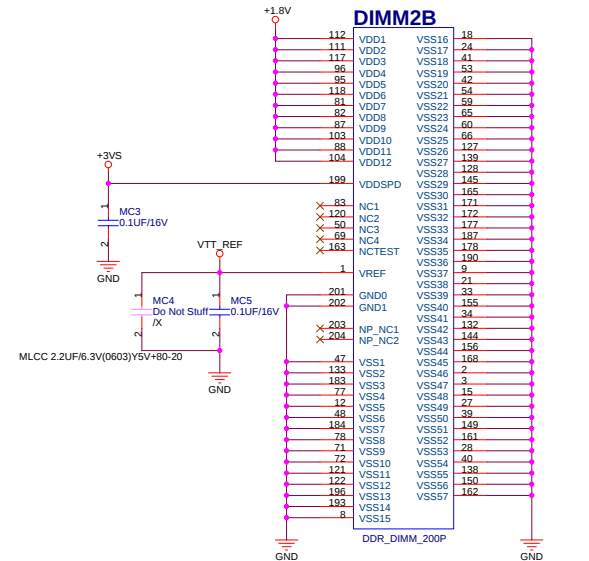


H=9.2mm Standard Type, 12G025C22000
Channel A, DIMM 0

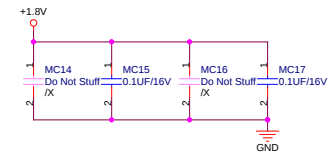




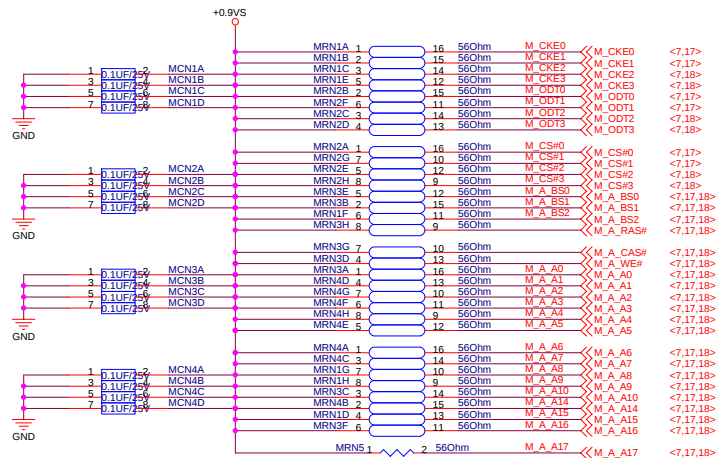
H=5.2mm Standard Type, 12G025122007
Channel A, DIMM 1



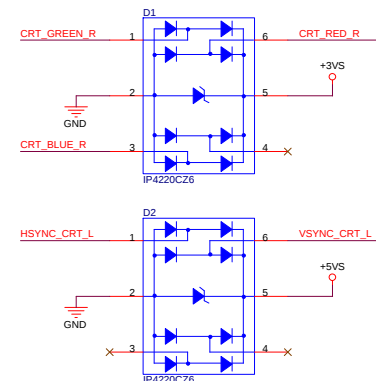
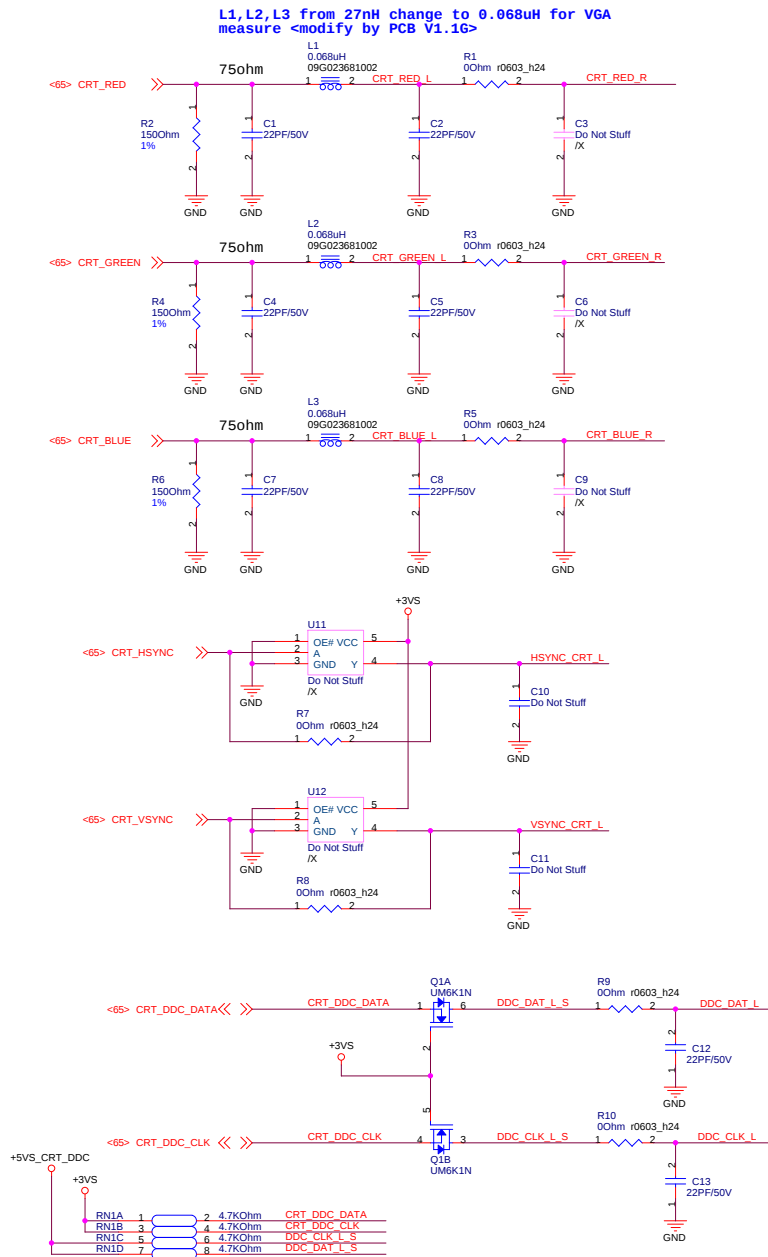
Layout Note: Place these Caps near SO-DIMM1



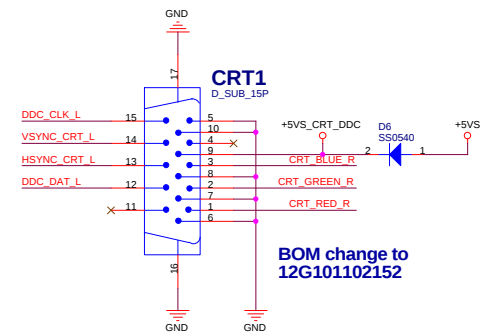
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout note: Place one cap close to every 2 pull-up resistors terminated to +0.9V



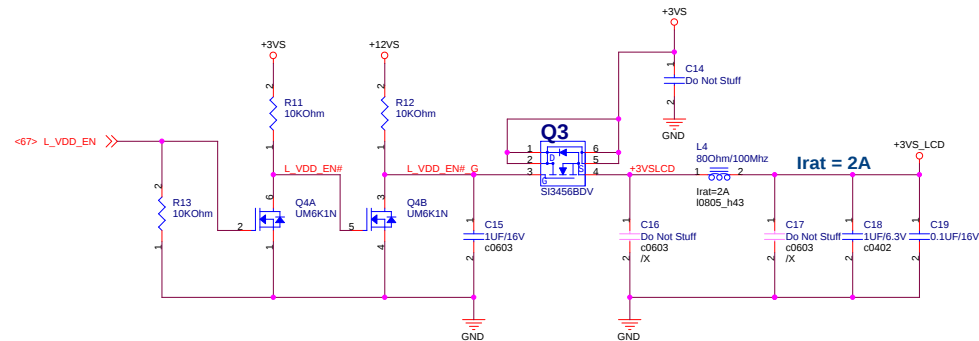
ESD Diodes
Place ESD Diodes near CRT Connector



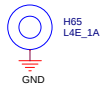
BOM change to
12G101102152

CRT Connector

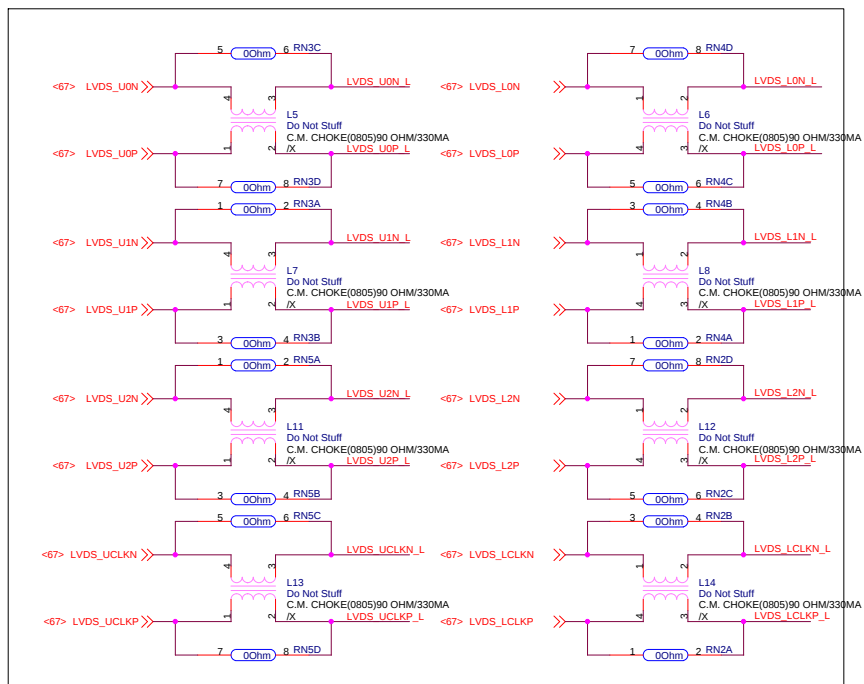
LCD Power Switch



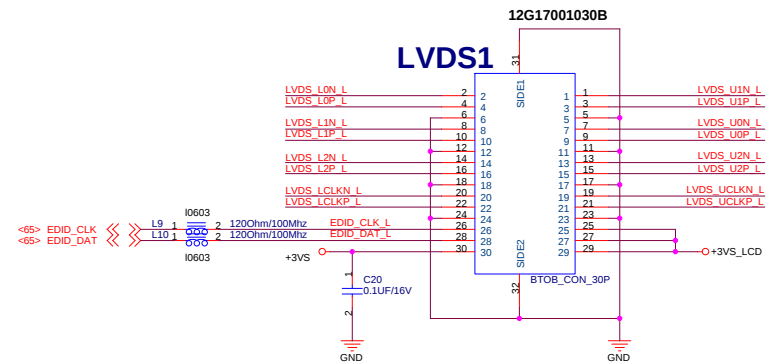
LVDS NUT



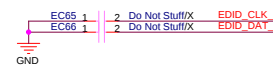
C14,C20 for EMI solution
<modify by PCB V1.1G>



LVDS Connector



Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

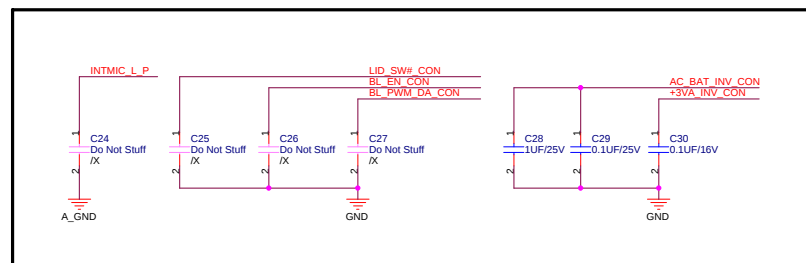
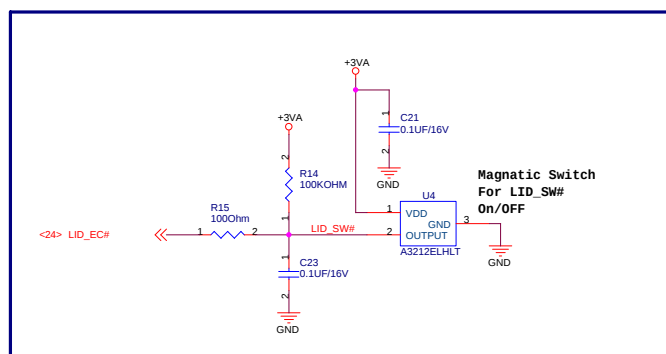
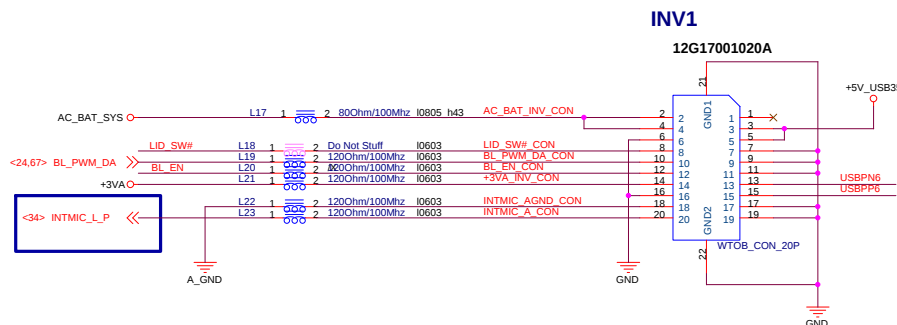
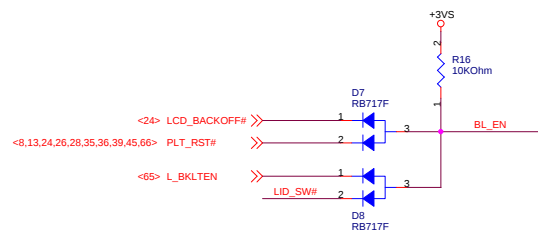
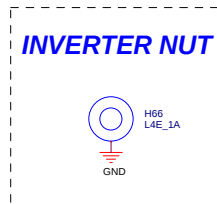
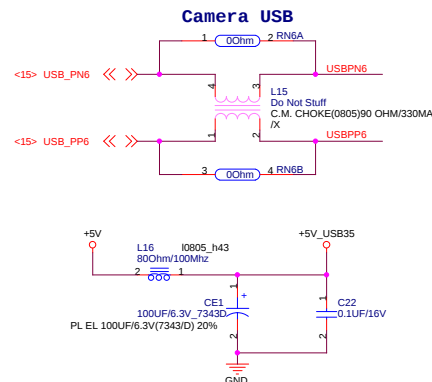


INVERTER Interface

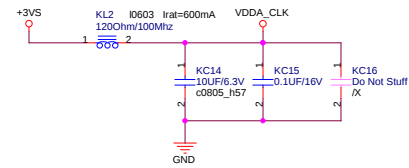
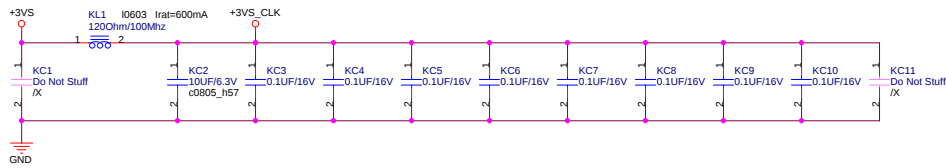
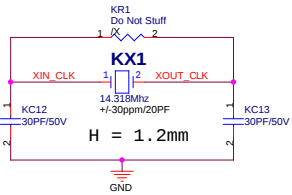
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

BIOS
BACK_ADJ: KBC output PWM signal (adjust pulse width) to adjust Back light.

Inverter Board built in 14.1W LCD Panel



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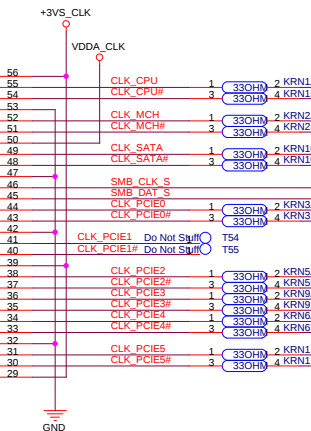
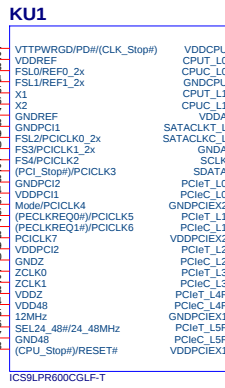
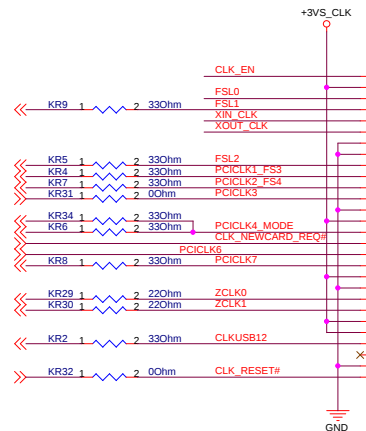
<14> CLK_SB14

<28> CLK_CBPIC1
<13> CLK_ICHPIC1
<26> CLK_LANPCI
<14> STP_PCI#
<44> CLK_DEBUG
<45> CLK_TPMPC1
<35> CLK_NEWCARD_REQ#
<36> CLK_MINICARD_REQ#
<24> CLK_ECPC1

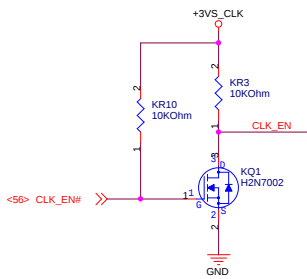
<8> CLK_ZCLK_NB
<13> CLK_ZCLK_SB

<15> CLK_USB12

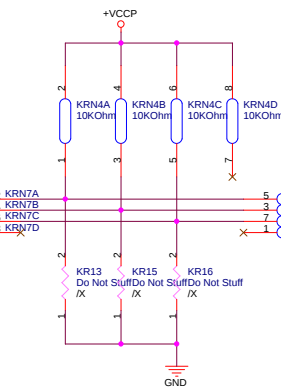
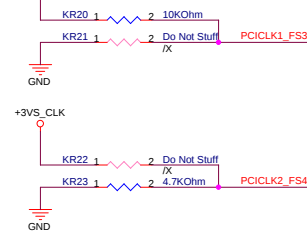
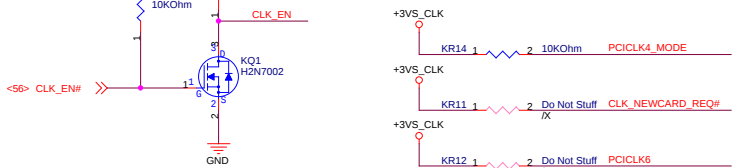
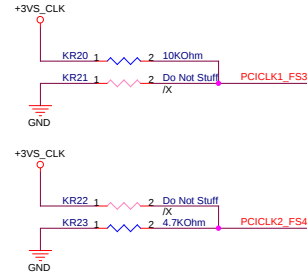
<14,27,56> STP_CPU#



CLK_CPU_BCLK <3>
CLK_CPU_BCLK# <3>
CLK_MCH_BCLK <6>
CLK_MCH_BCLK# <6>
CLK_SATA_ICH <15>
CLK_SATA_ICH# <15>
SMB_CLK_S <3,12,14,17,18,25,35,36>
SMB_DAT_S <3,12,14,17,18,25,35,36>
CLK_PCIE0 <35>
CLK_PCIE0# <35>
CLK_PCIE1 <35>
CLK_PCIE1# <35>
CLK_PCIE2 <35>
CLK_PCIE2# <35>
CLK_PCIE3 <35>
CLK_PCIE3# <35>
CLK_PCIE4 <35>
CLK_PCIE4# <35>
CLK_PCIE5 <35>
CLK_PCIE5# <35>



<56> CLK_EN#



<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

<3> CPU_BSEL0
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<3> CPU_BSEL0
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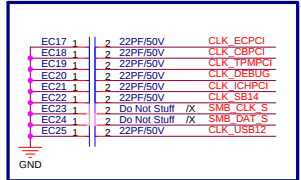
<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

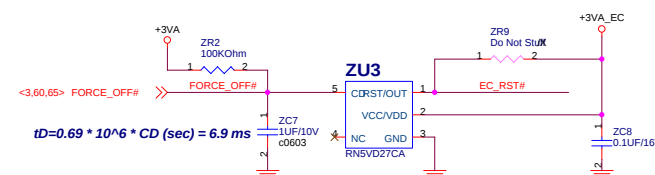
<3> CPU_BSEL0
<3> CPU_BSEL1
<3> CPU_BSEL2

CLK trapped by CPU's BSEL

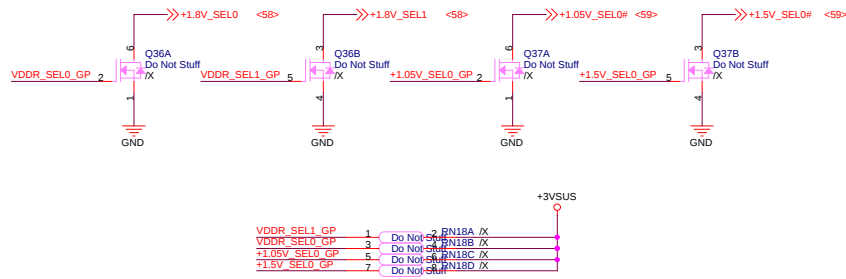
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

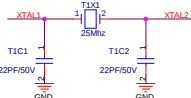
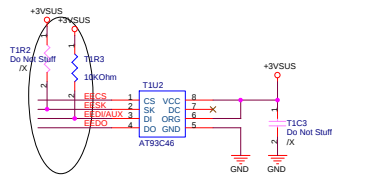


EC17 or EC22, EC25 for EMI solution<modify by PCB V1.1g>



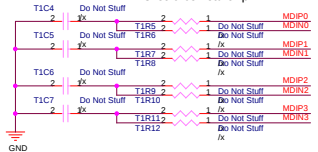
888					
	Title : <u>EC ENE3925</u>				
ASUSTek Computer INC.	Engineer: <u>Jack Hsu</u>				
<table border="1"> <tr> <td>Size</td> <td>Project Name</td> </tr> <tr> <td>Custom</td> <td>Z62Ha</td> </tr> </table>	Size	Project Name	Custom	Z62Ha	Re: <u>1.1</u>
Size	Project Name				
Custom	Z62Ha				
Date: <u>Thursday, September 27, 2007</u>	Sheet <u>24</u> of <u>70</u>				



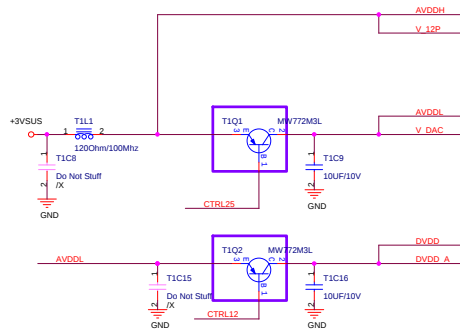


T1C1 & T1C2 from 18pF
change to 22pF
<modify by PCB V1.16>

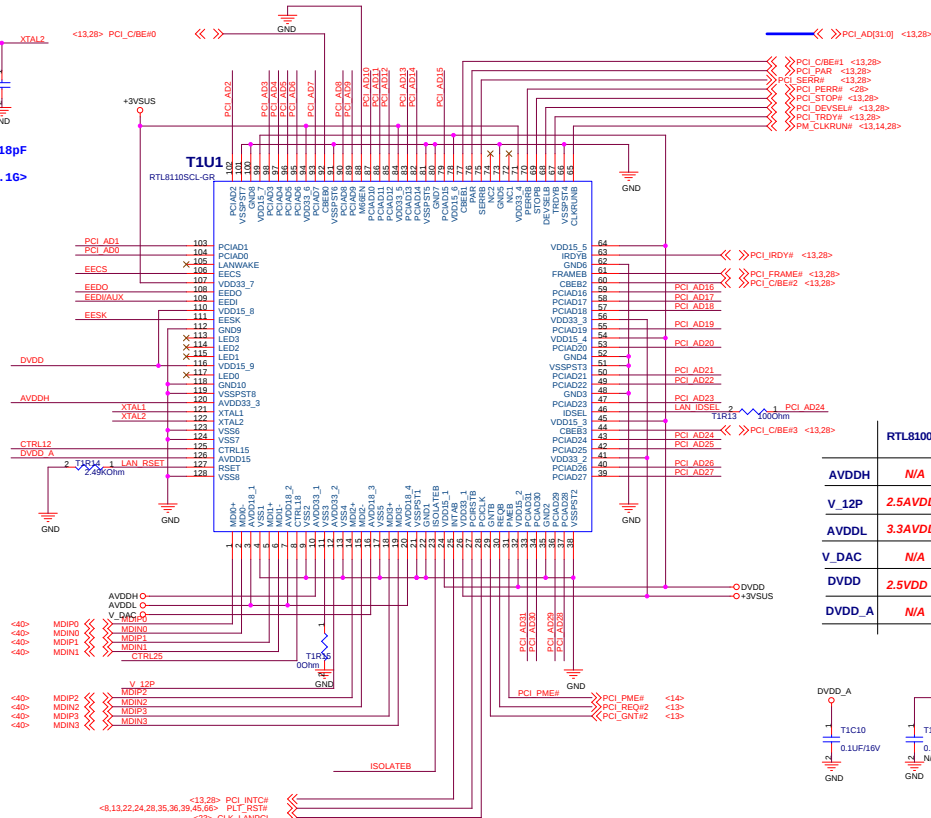
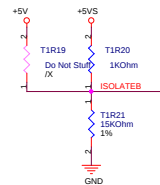
*All termination resistors
should be near chip



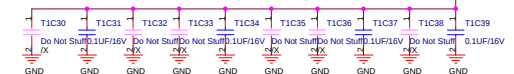
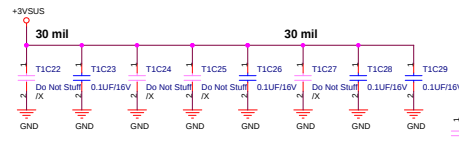
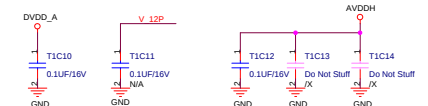
10/100==> 5.6K,1% resistor
GLAN==> 2.49K,1% resistor



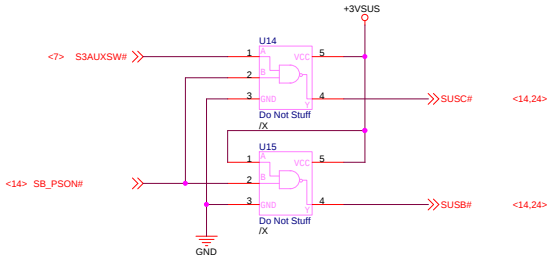
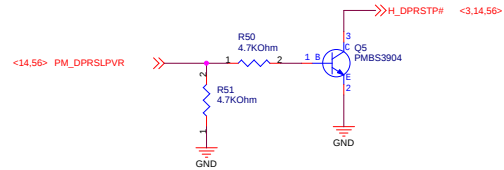
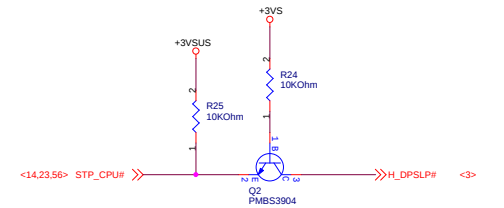
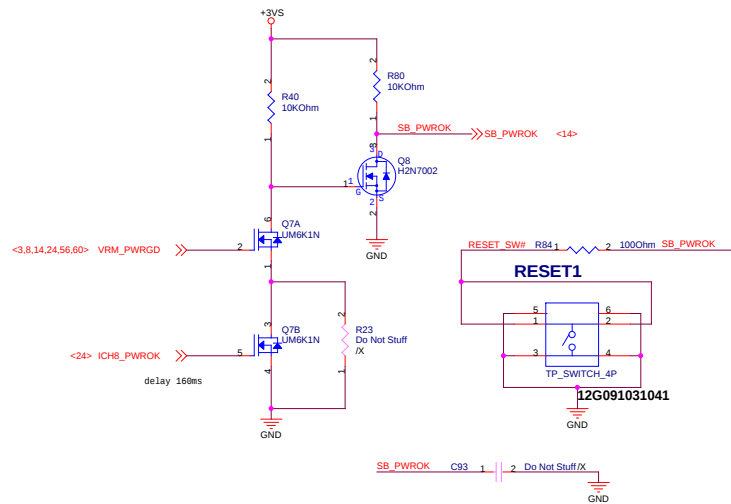
HSMC Quality Issue, change part.



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V 12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/116/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126



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Sleep & Wake up

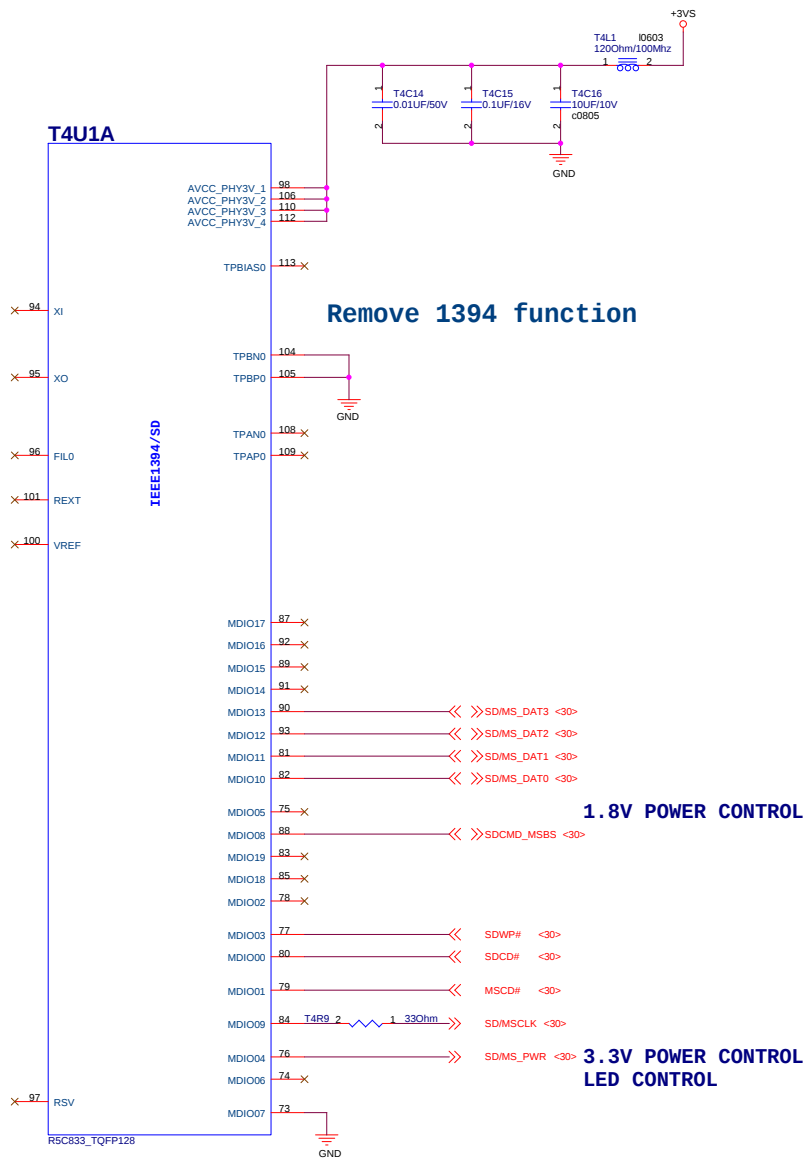
	S0 → S3 → S0				
S3AUXSW#	1	0	0	0	1
SB_PSON#	0	0	1	0	0
SUSC#(S4)	1	1	1	1	1
SUSB#(S3)	1	1	0	1	1
Power Status	Main	Main	System, S4	Main	Main

Power ON & OFF:

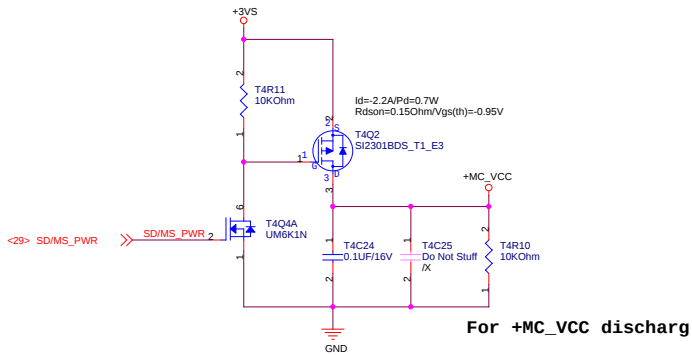
	S5 → S0 → S5		
S3AUXSW#	1	1	1
SB_PSON#	1	0	1
SUSC#(S4)	0	1	0
SUSB#(S3)	0	1	0
Power Status	System	Main	System

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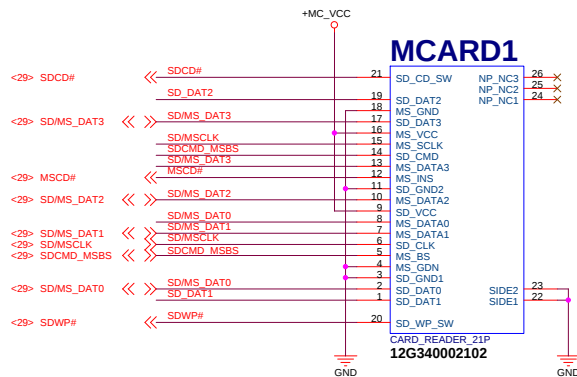
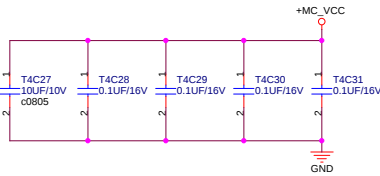
ASUS		Title : Other	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size Custom	Project Name Z62Ha	Rev 1.1	
Date: Thursday, September 27, 2007	Sheet 27 of 70		



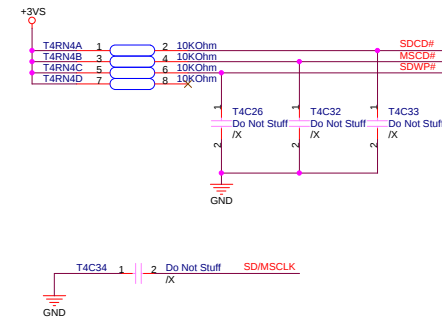
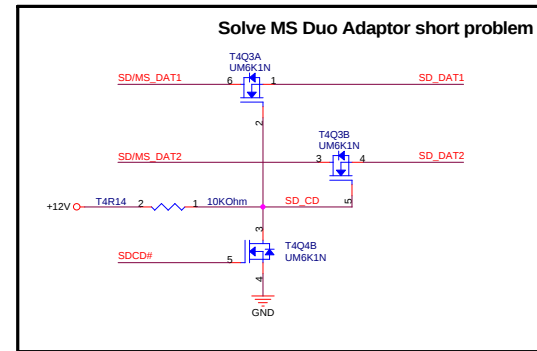
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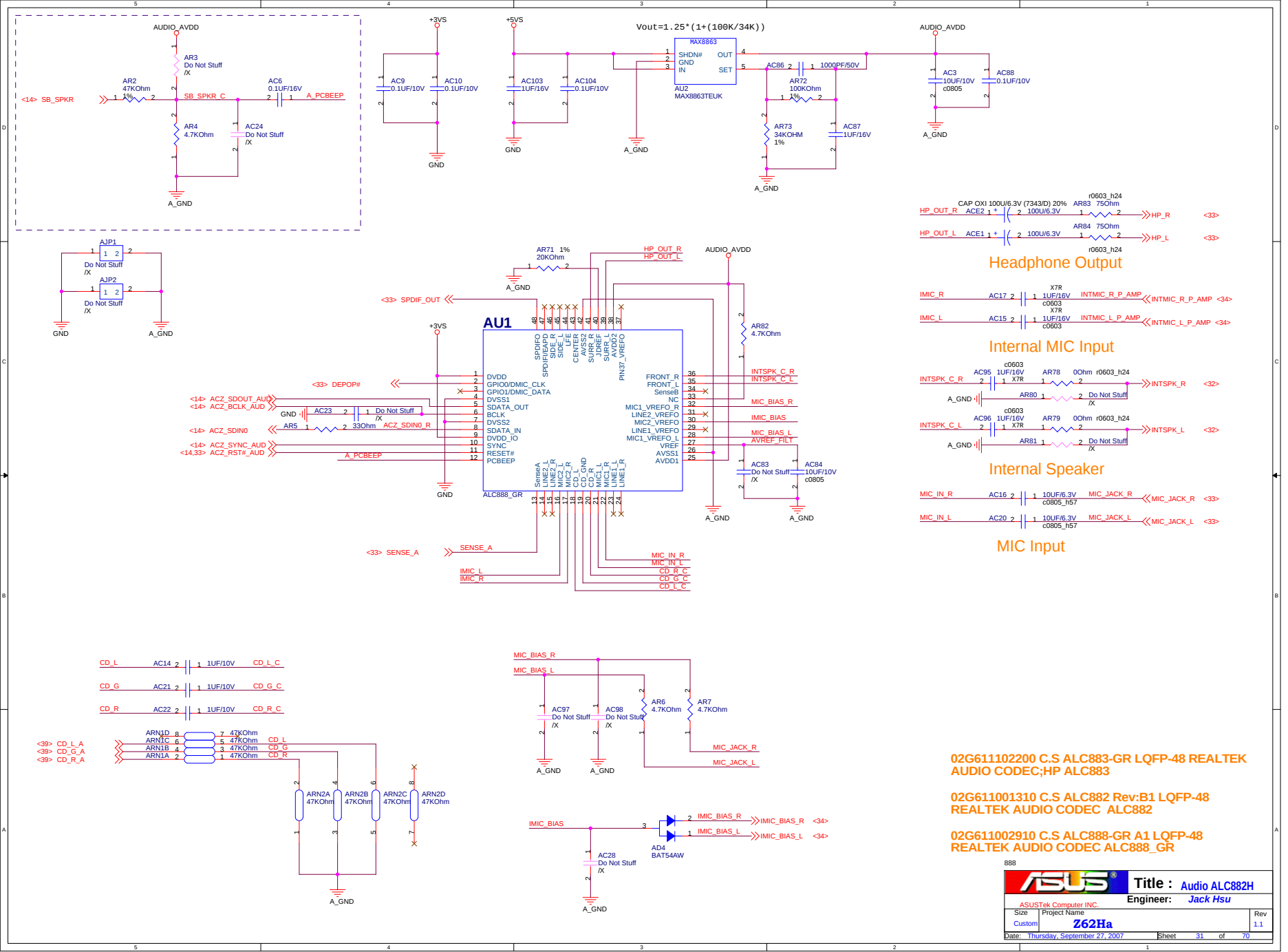


Card Reader Power Switcher



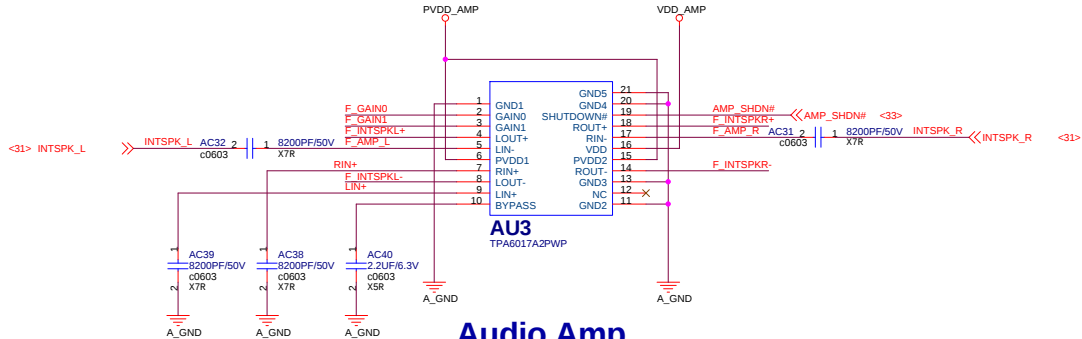
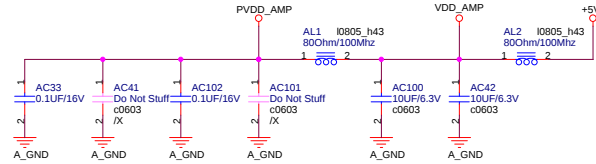
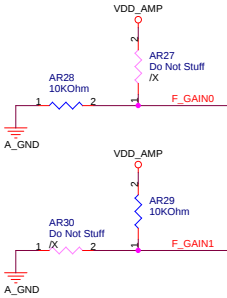
3 in 1 Card Reader





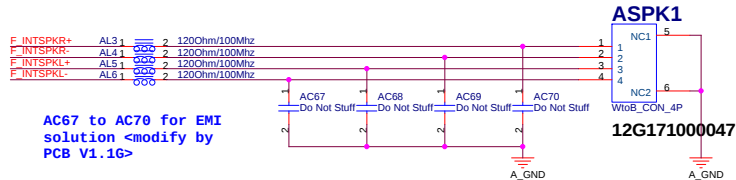
GAIN Control

GAIN0	GAIN1	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



Audio Amp.
fc = 1kHz

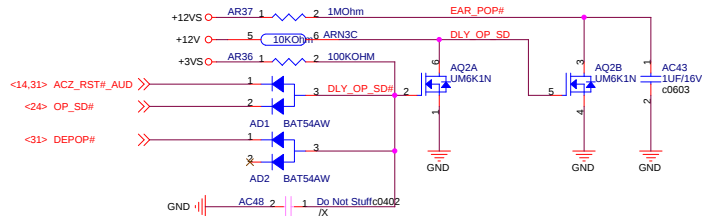
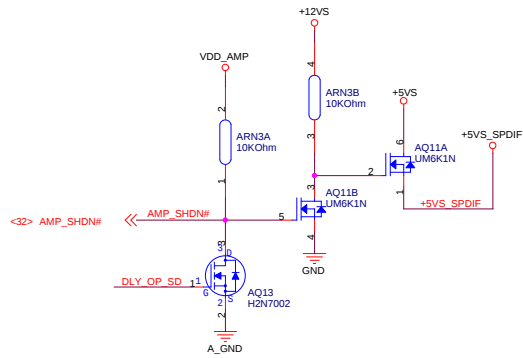
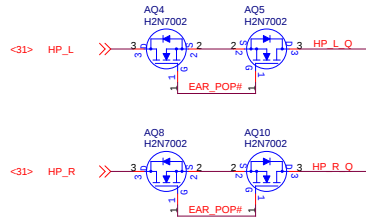
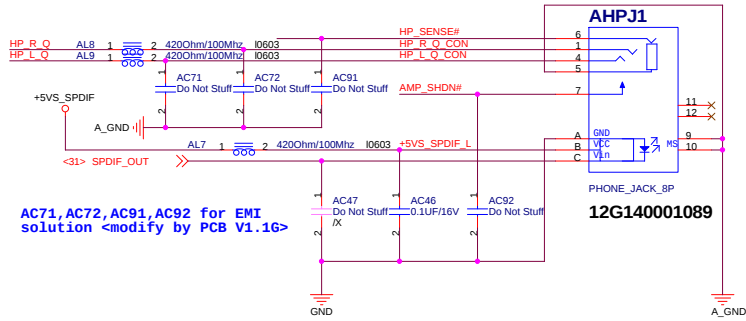
12G171000047
Internal Speaker Connector



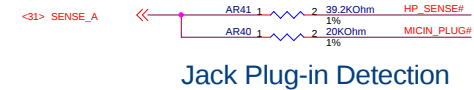
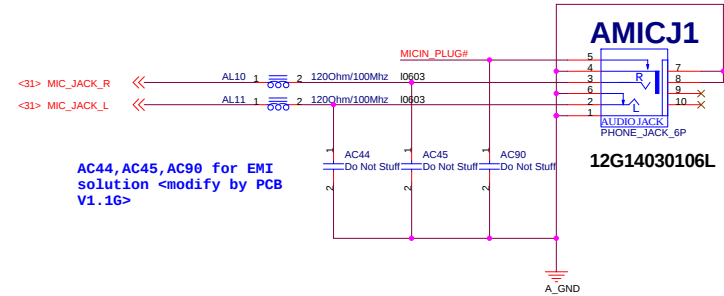
ASP K1

12G171000047

Headphone & S/PDIF Jack

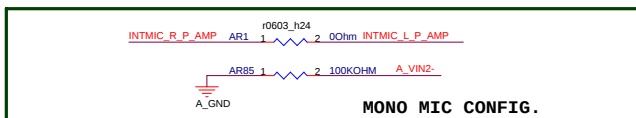
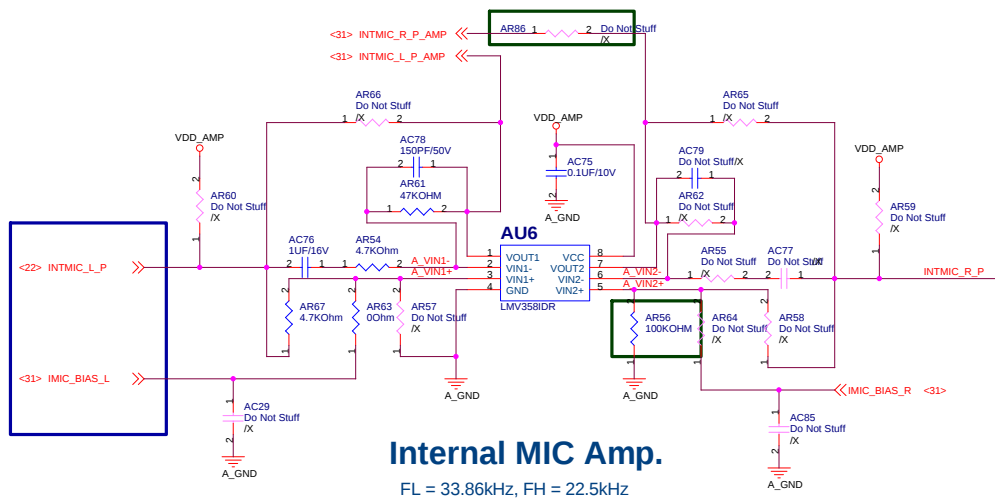


Microphone-In Jack



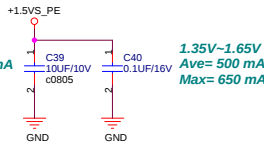
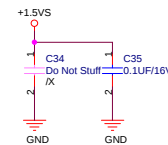
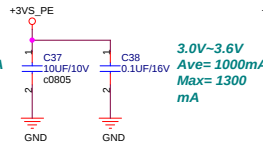
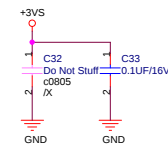
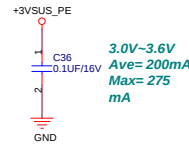
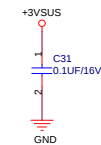
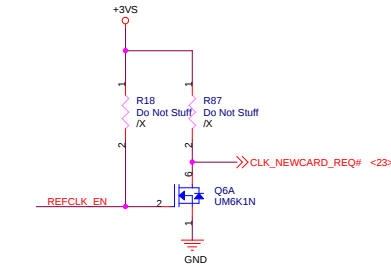
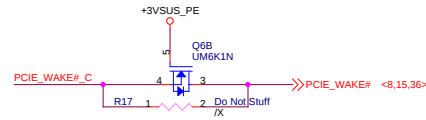
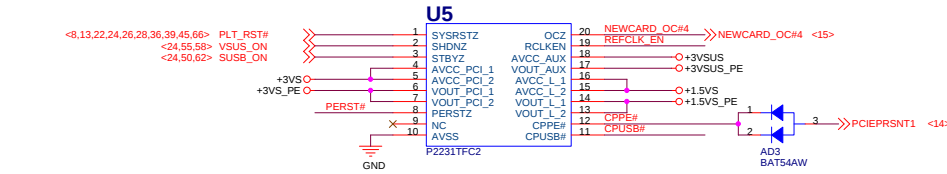
888

ASUS		Title : Audio JACK	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007	Sheet	33	of 70

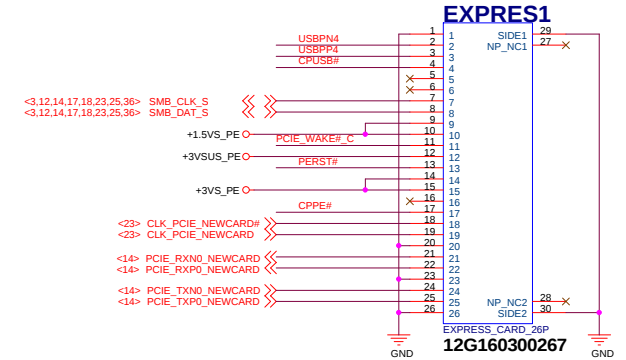


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06G030057011 POWER SW. P2231TFC1 TSS0P-20 ENE P2231TFC1
06G030057012 POWER SW. P2231TFC2 TSS0P-20 ENE P2231TFC2

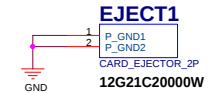


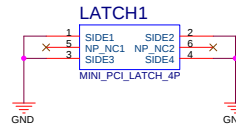
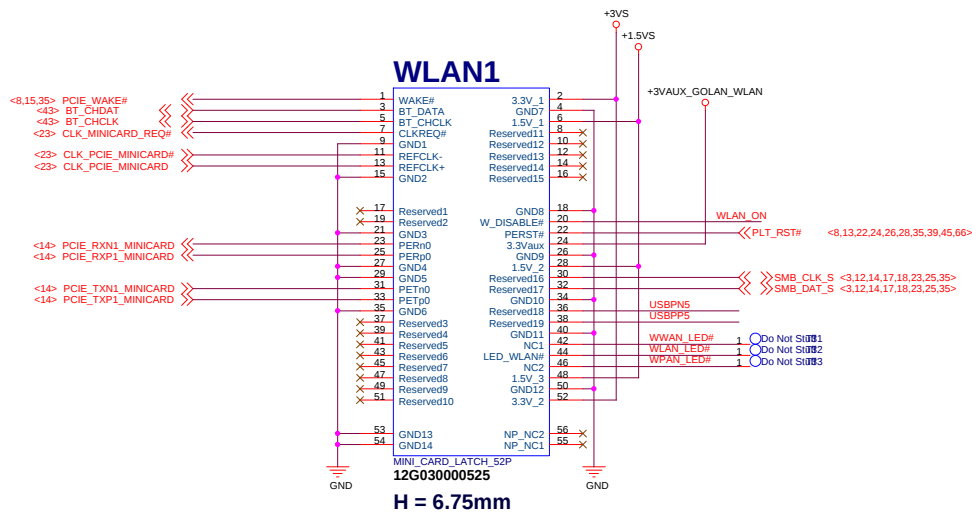
NewCard Header



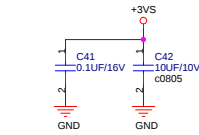
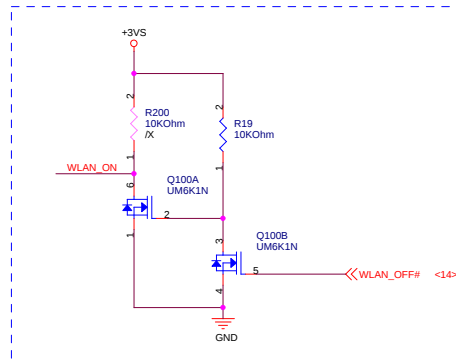
ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Ejector

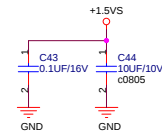




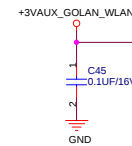
Add WLAN switch circuit <modify by PCB V1.16>



+3.003V~+3.597V
Max= 750 mA

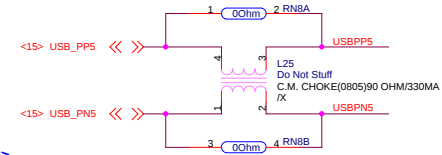


+1.425V~+1.575V
Max= 375 mA

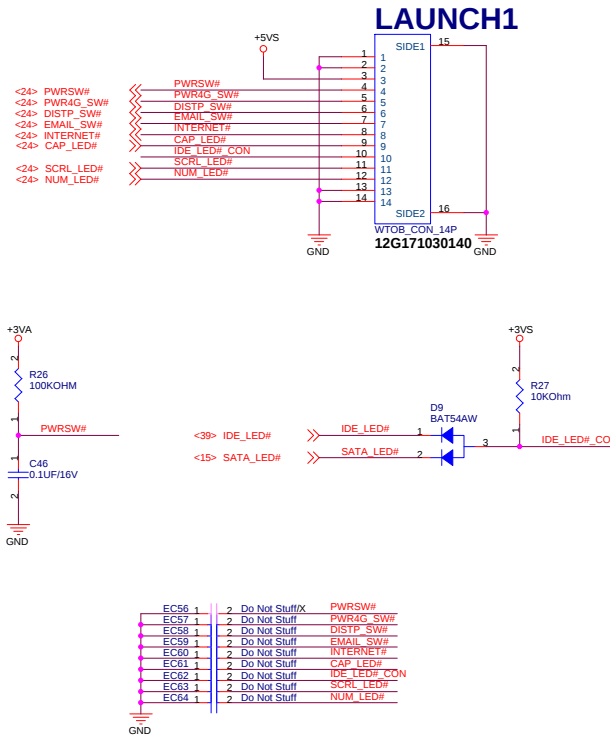


+3.003V~+3.597V
Max= 250 mA

Reserved for Wake on WLAN function



LAUNCH BOARD Connector



EC57 to EC64 for EMI solution
<modify by PCB V1.16>

5

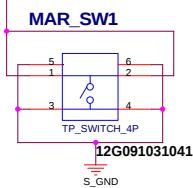
4

3

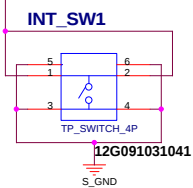
2

1

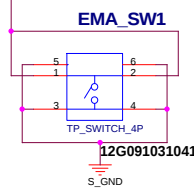
S_MARATHON#



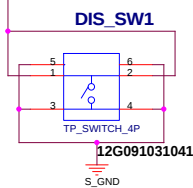
S_INTERNET#



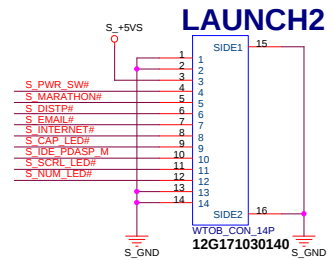
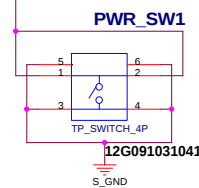
S_EMAIL#



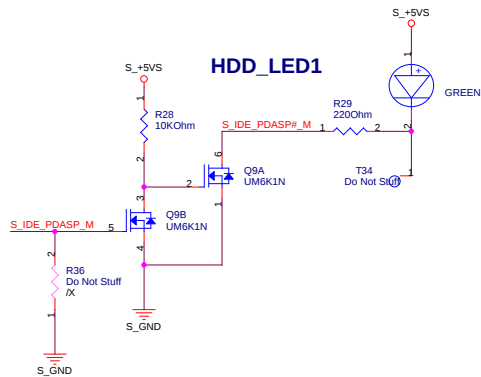
S_DISTP#



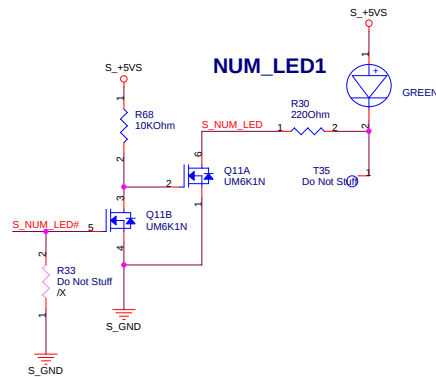
S_PWR_SW#



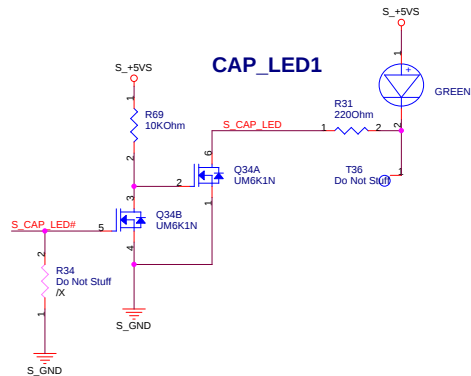
HDD_LED1



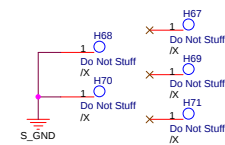
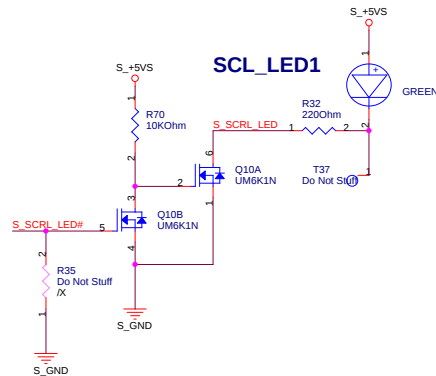
NUM_LED1



CAP_LED1



SCL_LED1



888

ASUS®			Title : LAUNCH BOARD	
ASUSTek Computer INC.			Engineer: Jack Hsu	
Size	Project Name		Rev	
Custom	Z62Ha		1.1	
Date: Thursday, September 27, 2007	Sheet		38	of 70

5

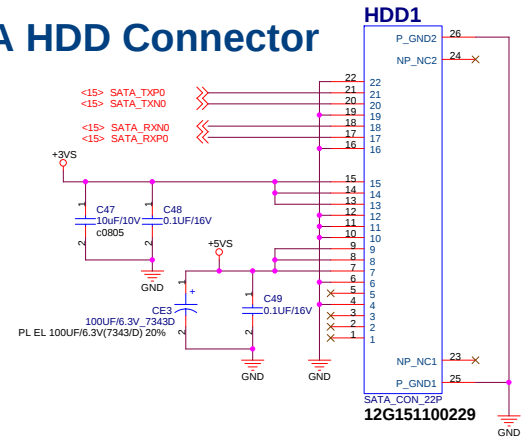
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3

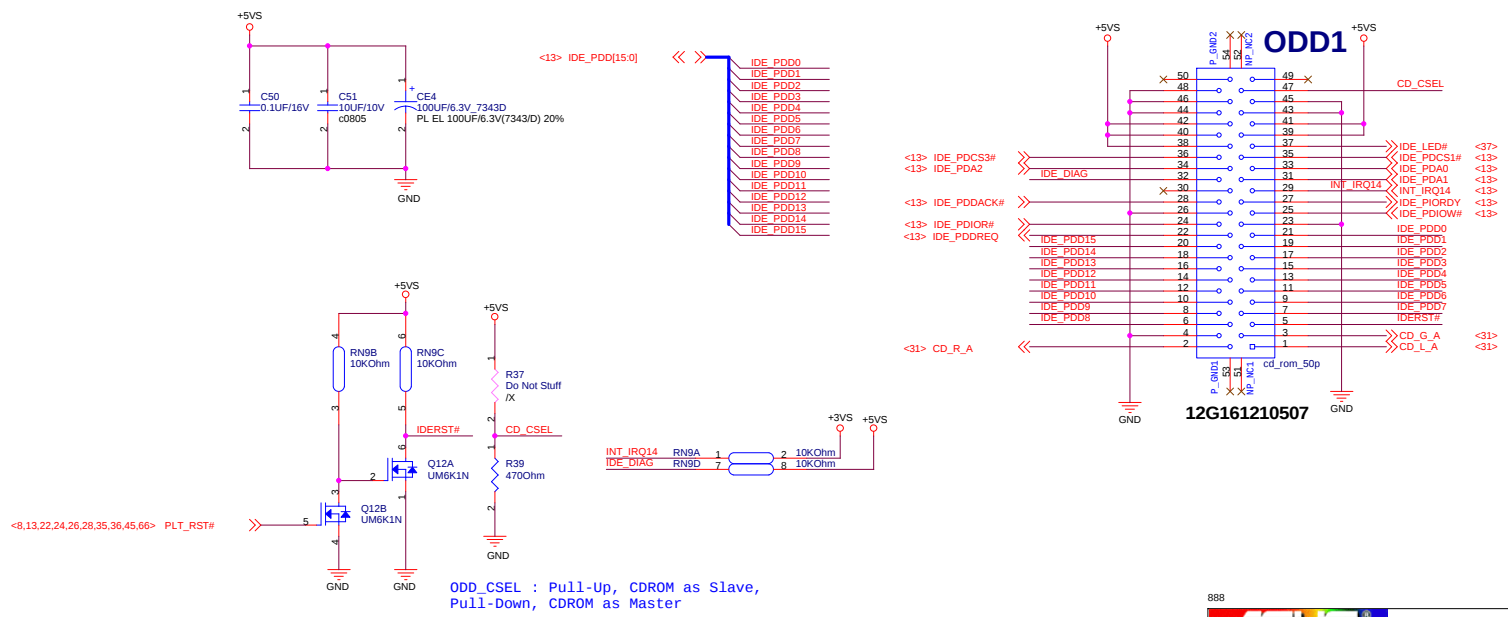
2

1

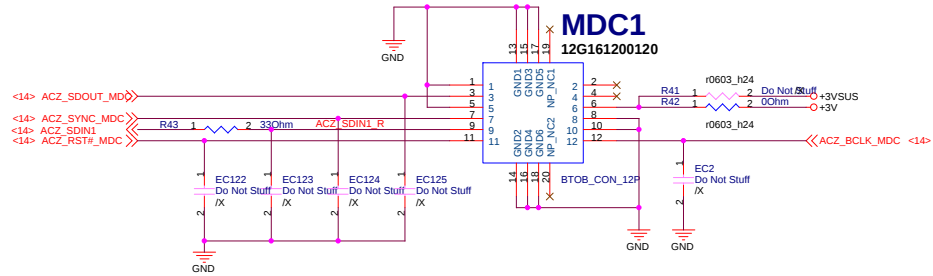
SATA HDD Connector



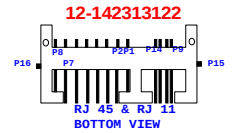
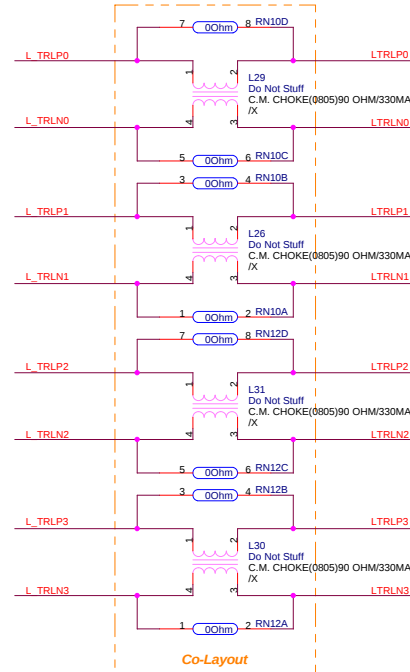
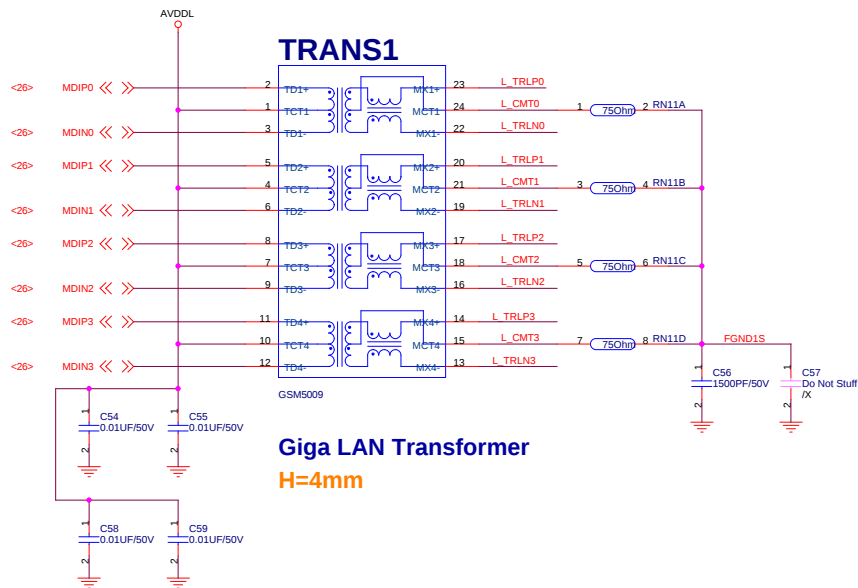
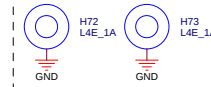
ODD Connector



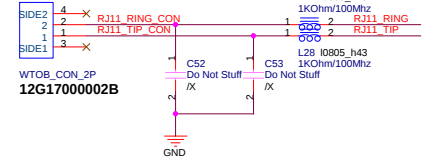
MDC Connector



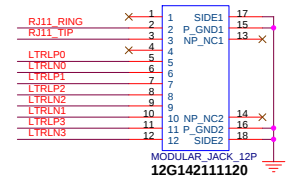
MDC Nut



RING1

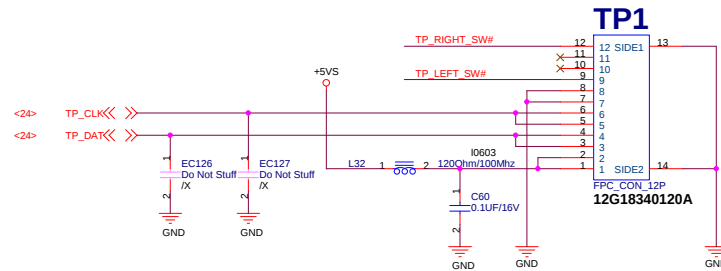


RJ45_11



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TouchPad Connector

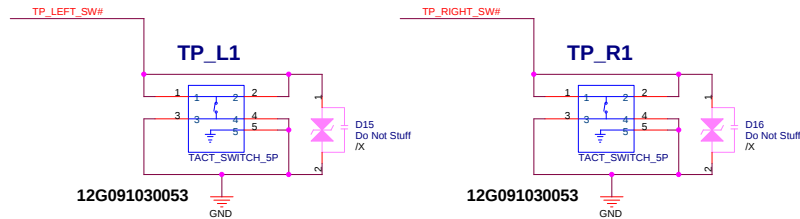
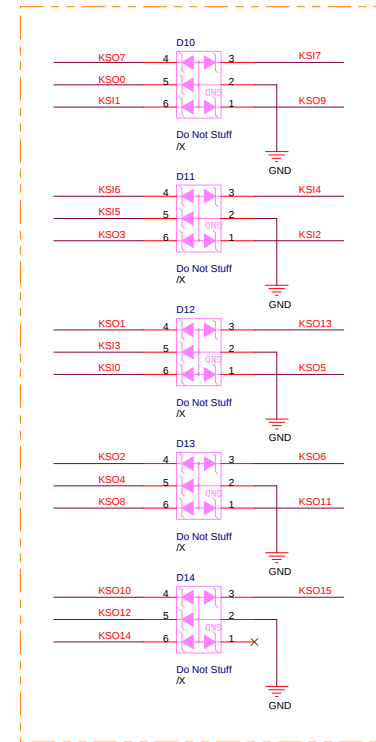
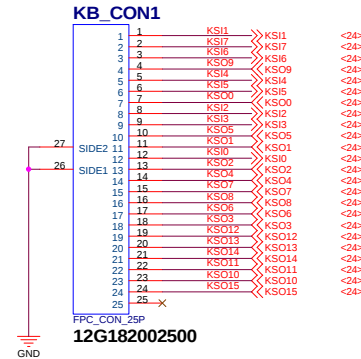


Touch pad Definition

	1	2	3	4	5	6	7	8	9	10	11	12
R	x	x	L	GND	GND	CLK	CLK	DAT	DAT	VDD	VDD	

Z62F: pin1 reversal

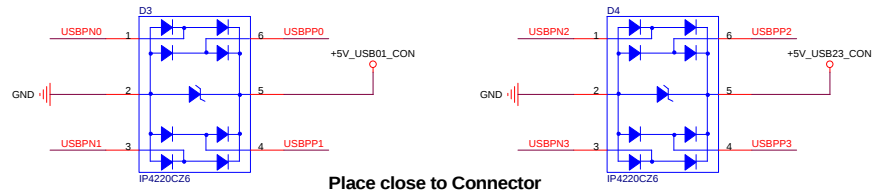
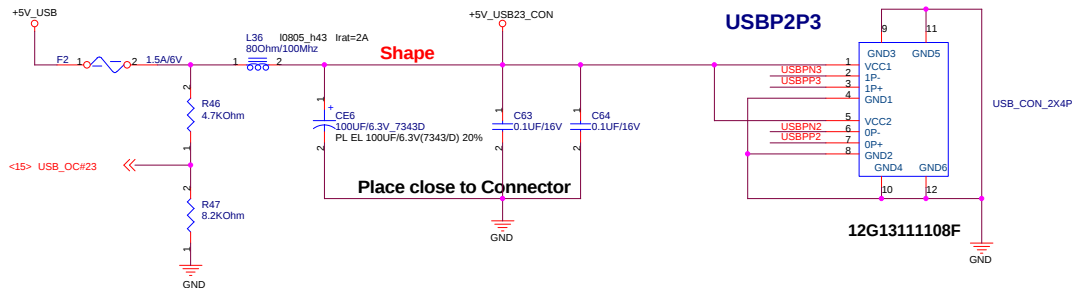
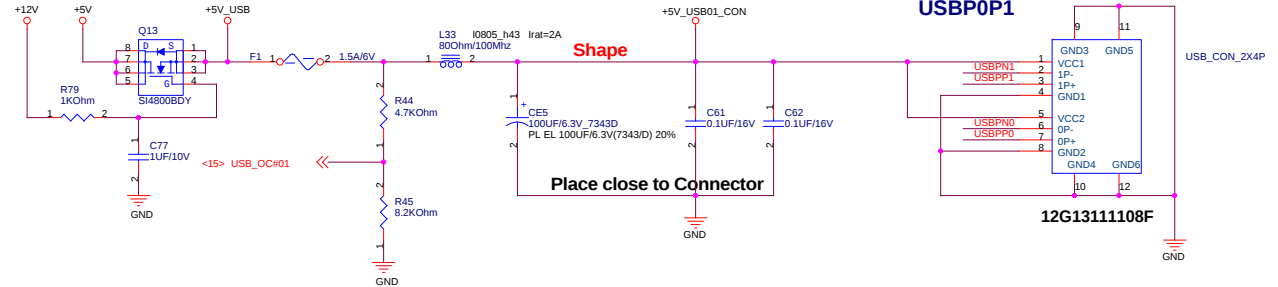
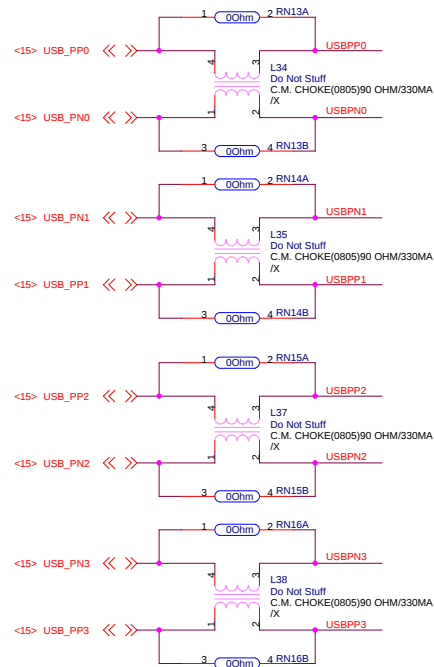
Keyboard Connector



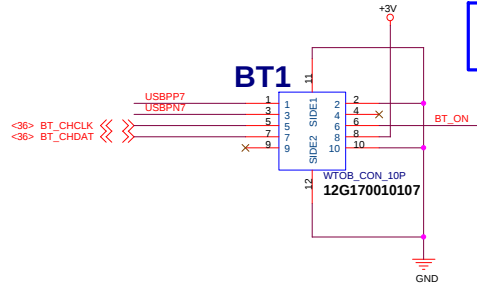
TOUCH PAD SWITCH

888

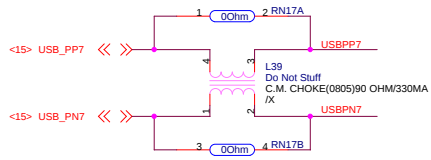
USB Power & OC Alert



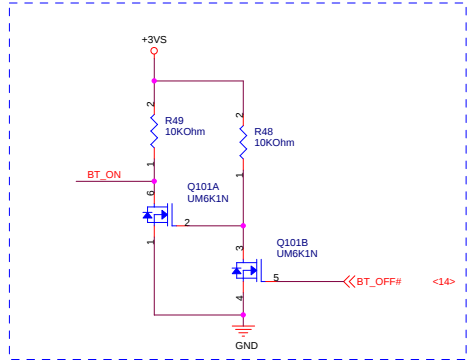
Bluetooth Connector



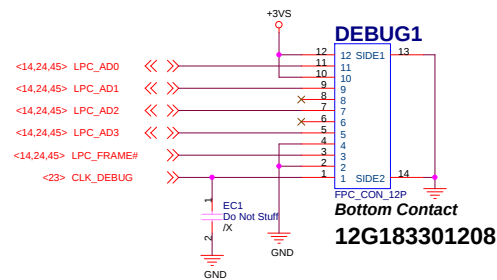
BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled



Add BT switch circuit <modify by PCB V1.16>

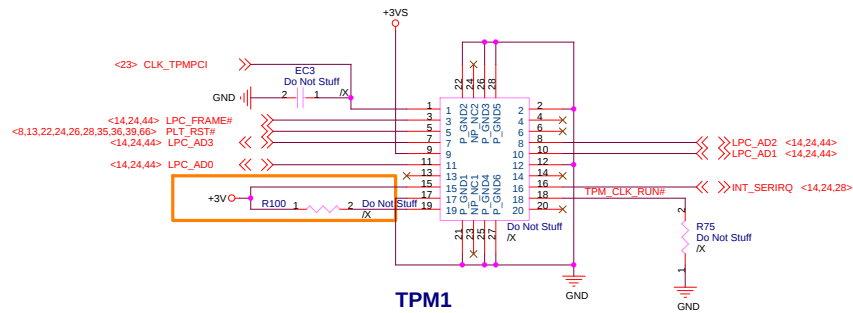


Debug Connector



888

TPM Connector



TPM1

12G16080020J

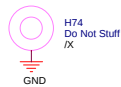
Pin 6: +3VA

Pin 13: SMB_CLK

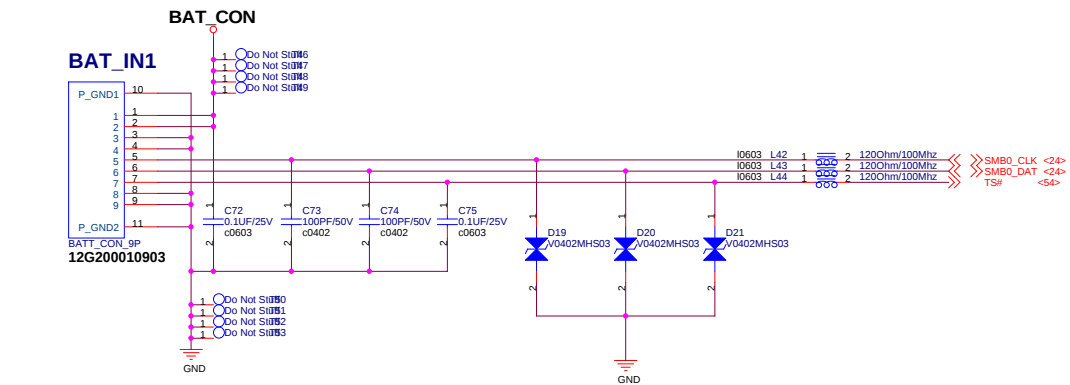
Pin 14: SMB_DAT

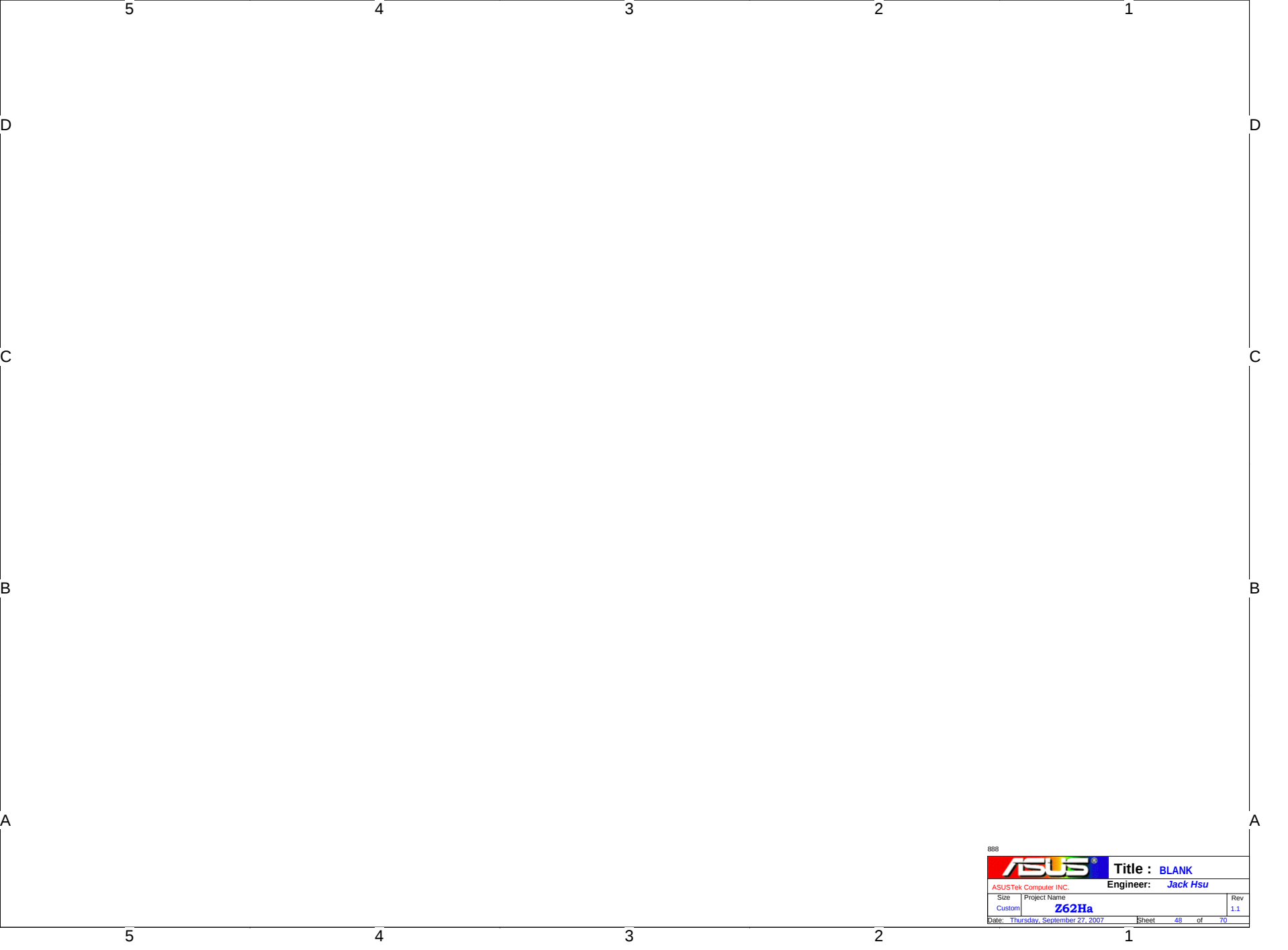
Removed!!

TPM Nut

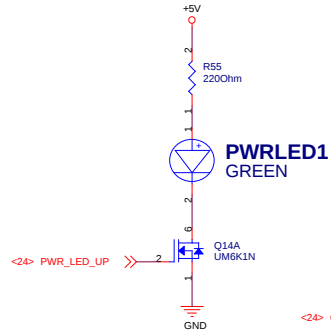


888

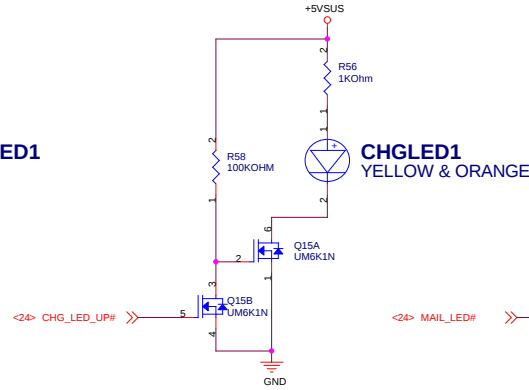




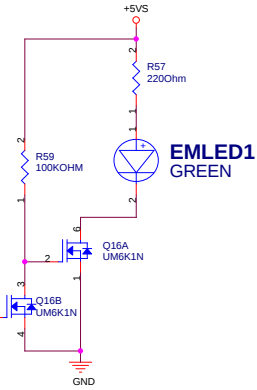
POWER LED



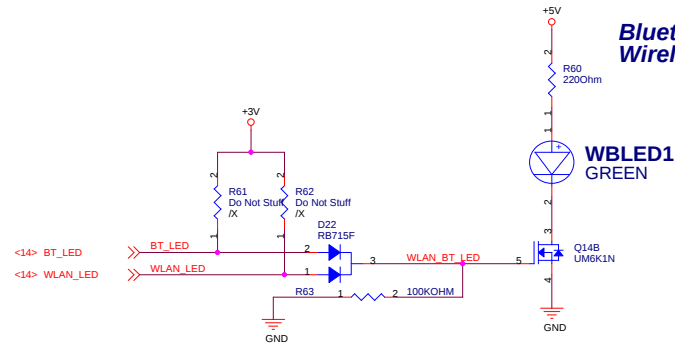
Battery Charge LED



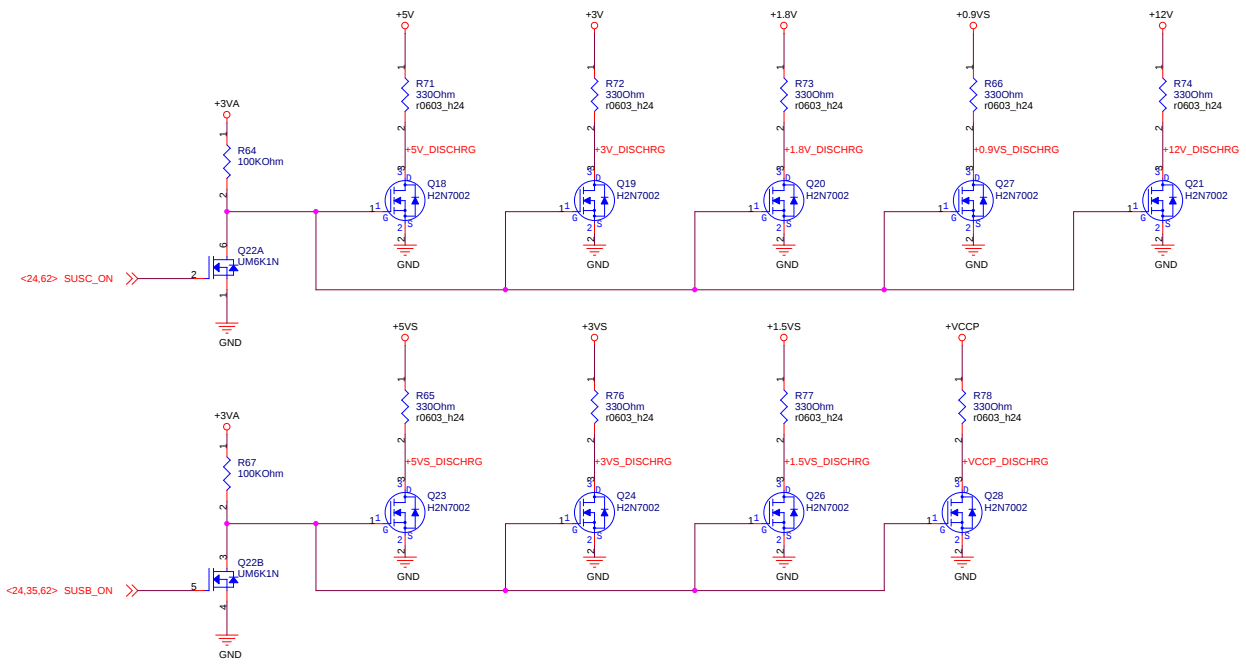
Email LED



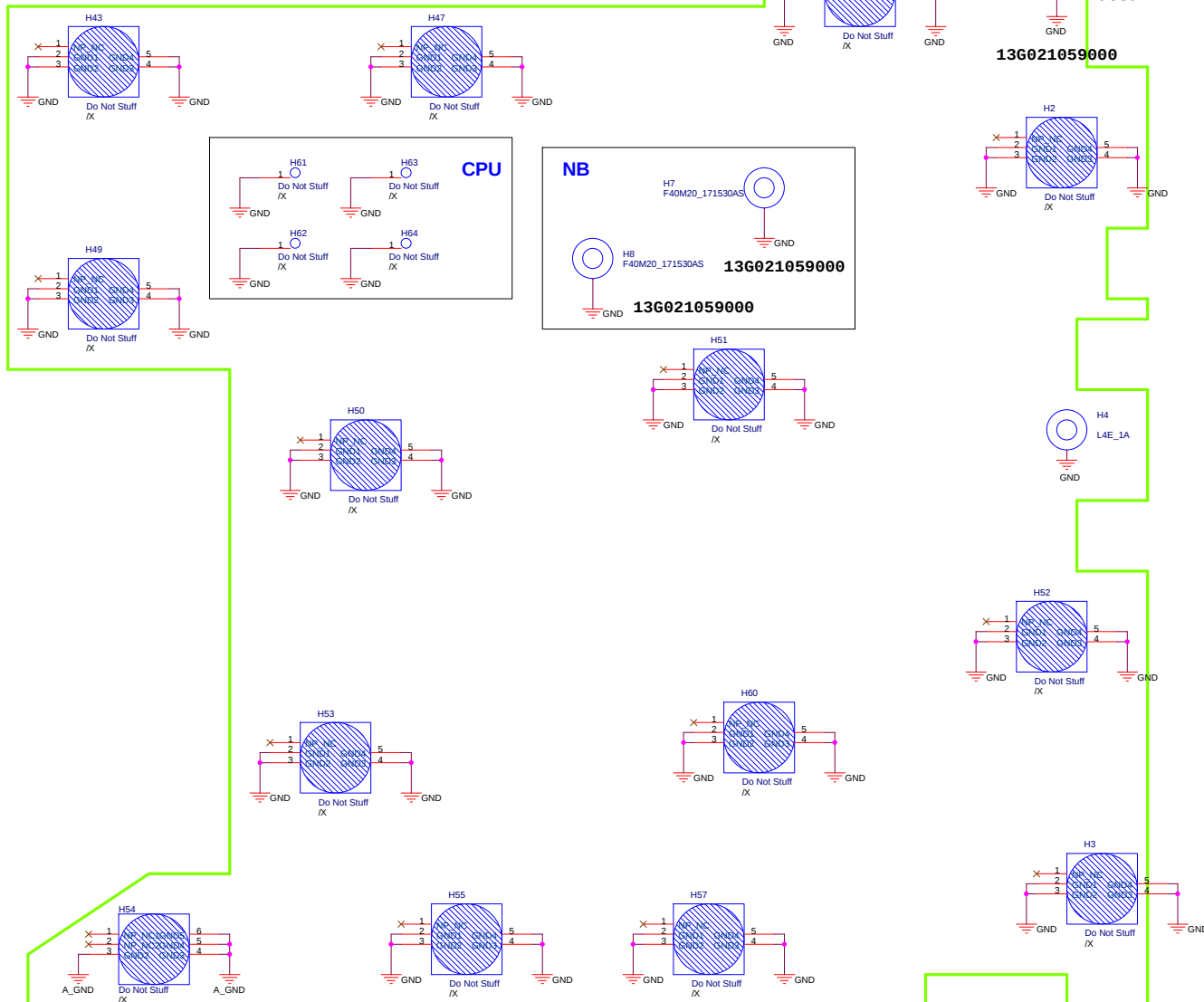
Bluetooth LED Wireless LED



888



SCREW HOLES



888

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4

3

2

1

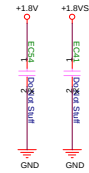
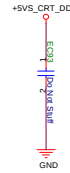
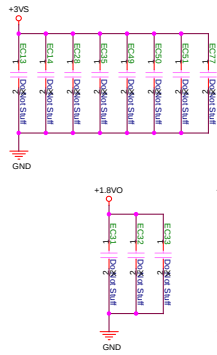
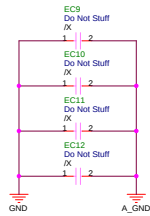
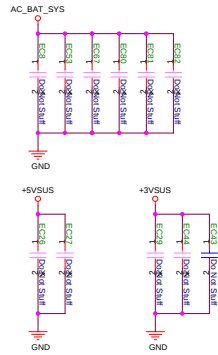
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4

3

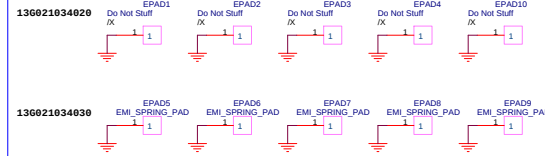
2

1



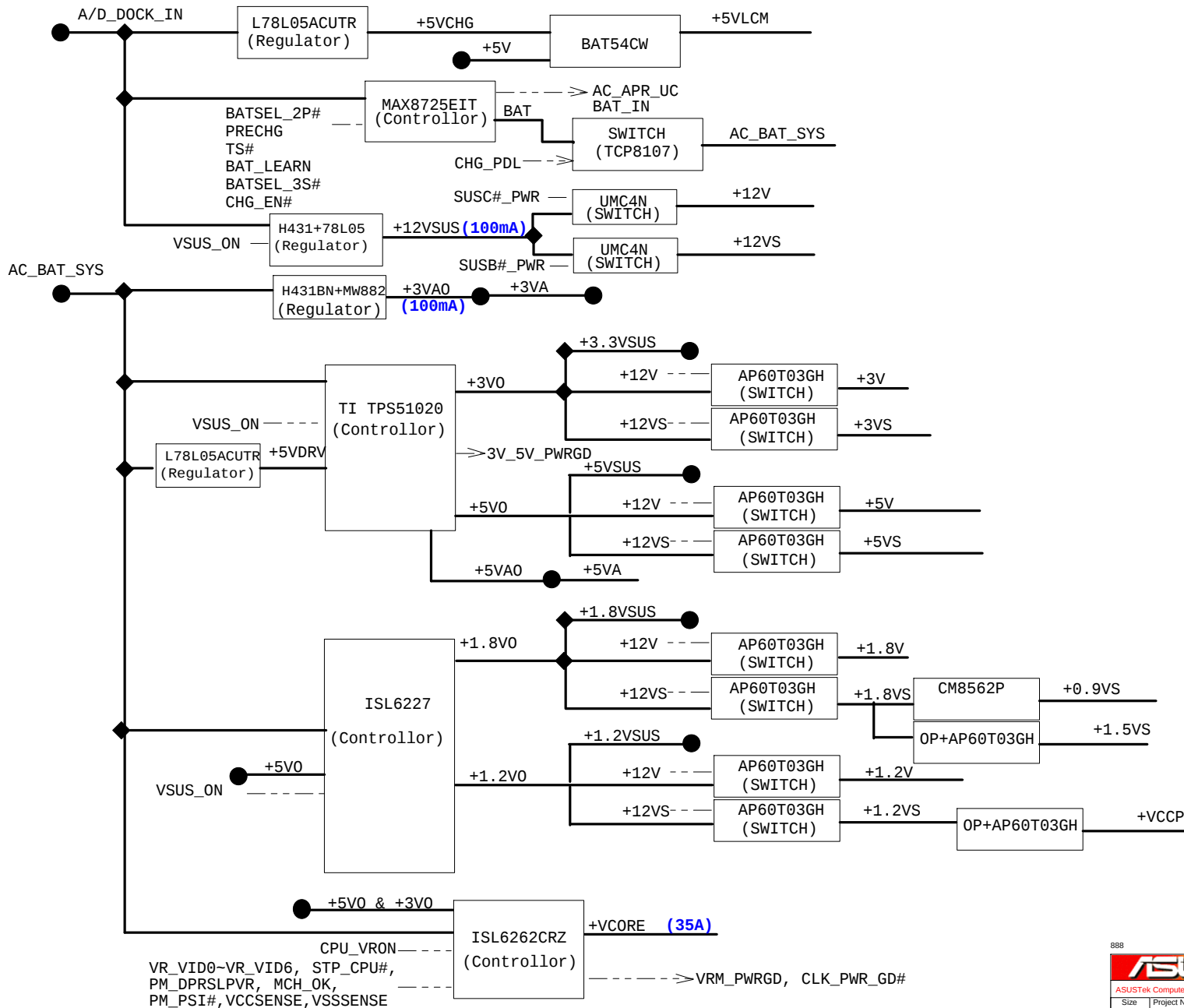
EC43, EC83 for EMI solution
<modify by PCB V1.16>

Spring For EMI



888

ASUS		Title : EMI CAP	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	Z62Ha	1.1	
Date: Thursday, September 27, 2007	Sheet	52	of 76



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AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter lin(max) = $[0.075V/R_{sense}(A_{lin})][V_{CLS}/V_{REF}]$
VCLS = 2.865V

Adaptor Max. Current :

PR5708=20K PR5714 = 178K; Ilimit = 4.5A; 81W
PR5708=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * [Vref + (VCTL - 1.8V) / 9.52]
VCTL = 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = $[0.075V/R_{sense}(CHG)][V_{CTL}/3.6V]$
Rsense(CHG) = 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA
Vctl = 0.107V ~ 0.109V

Battery Cell Selection :

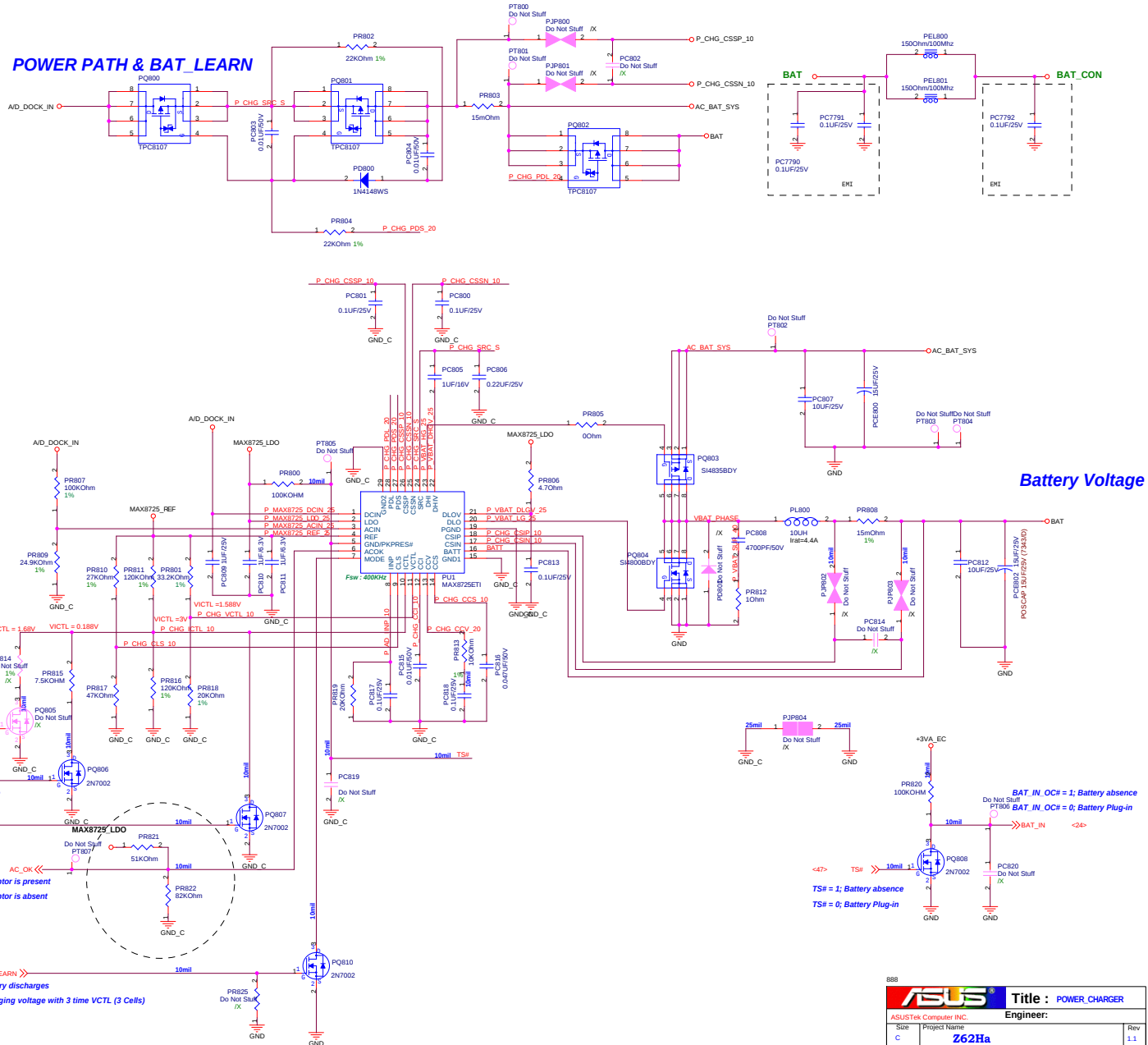
BATSEL_2P# = 1, 3 Cells; Vctl = 2.084V
=> Icharge = 1.6933A
BATSEL_2P# = 0, 6 or 9 Cells; Vctl = 2.111V
=> Icharge = 2.9329A

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

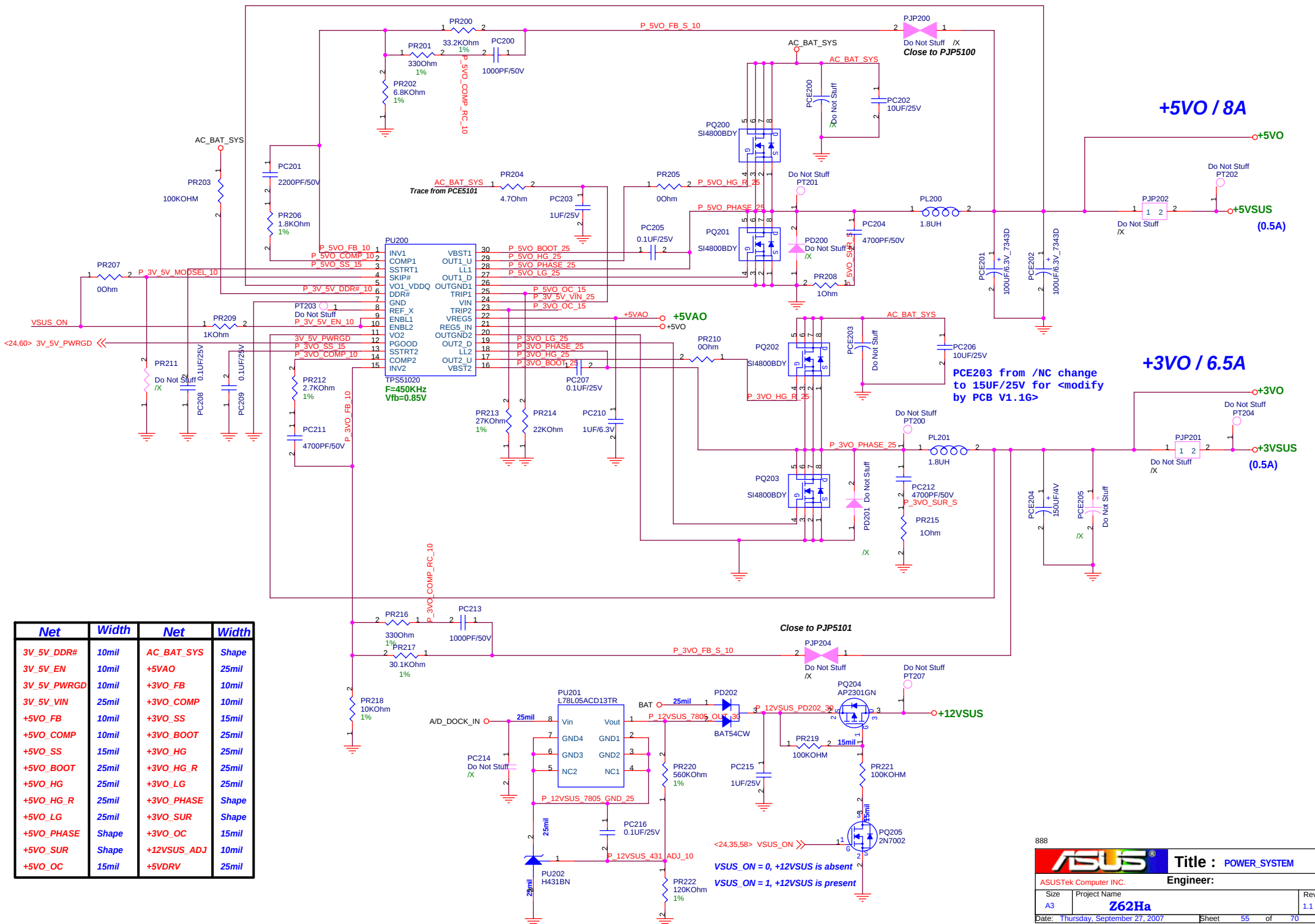
Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (try to GND) ----> Learning mode
VCTL < 0.8V or DCIN < 7V --> Charger Disable

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN



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Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_OC	15mil
+5VO_PHASE	Shape	+3VO_SUR	Shape
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

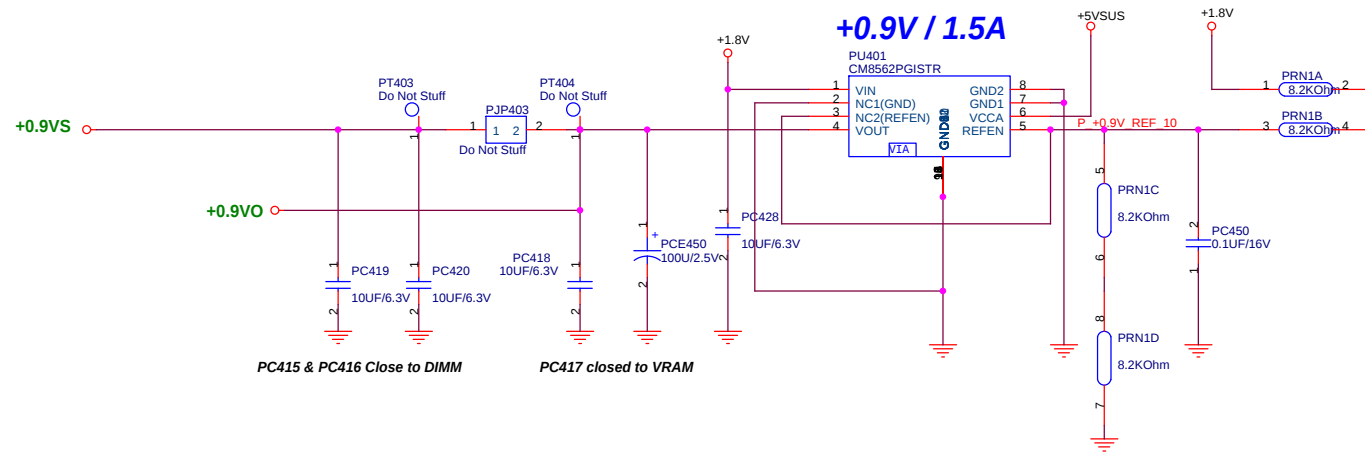
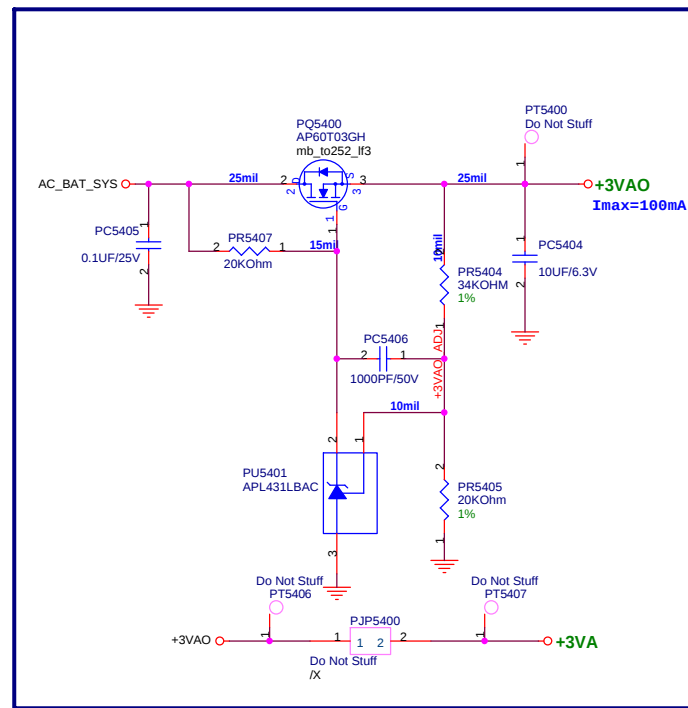
888

 **Title : POWER_SYSTEM**

ASUSTek Computer INC. **Engineer:**

Size	Project Name	Rev
A3	Z62Ha	1.1

Date: Thursday, September 27, 2007 Sheet 55 of 70



PC415 & PC416 Close to DIMM

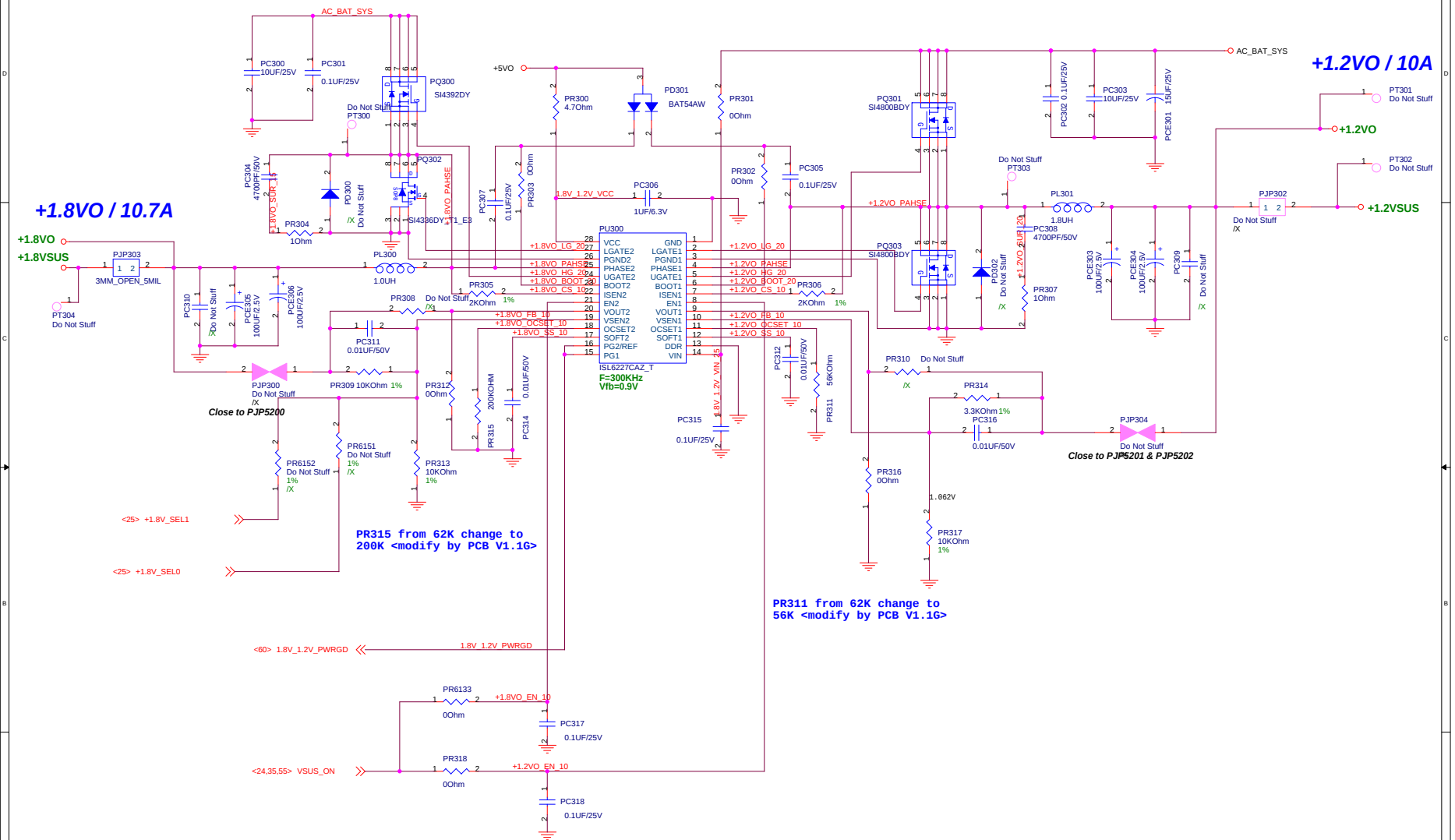
PC417 closed to VRAM

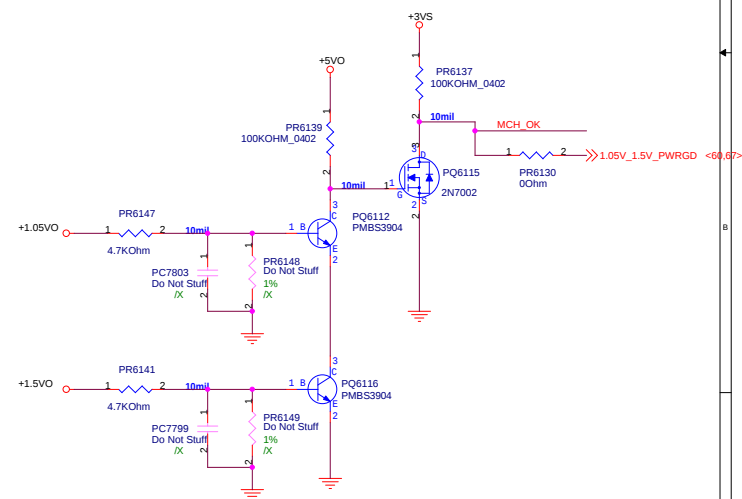
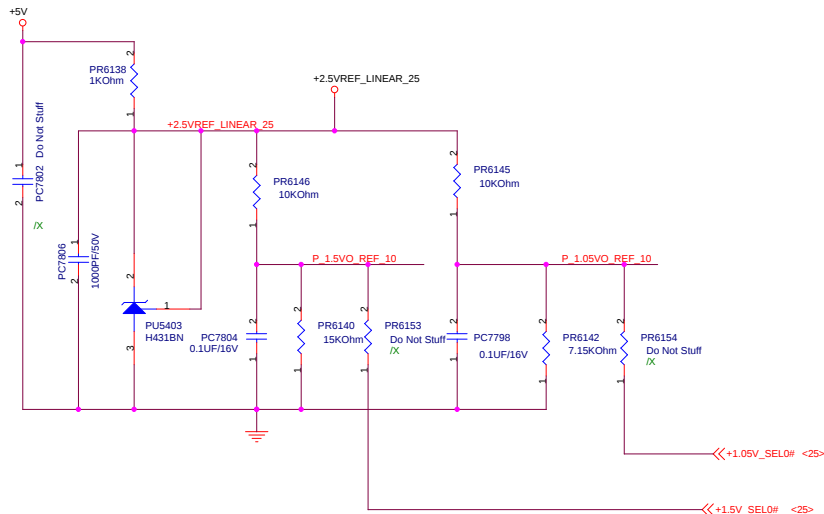
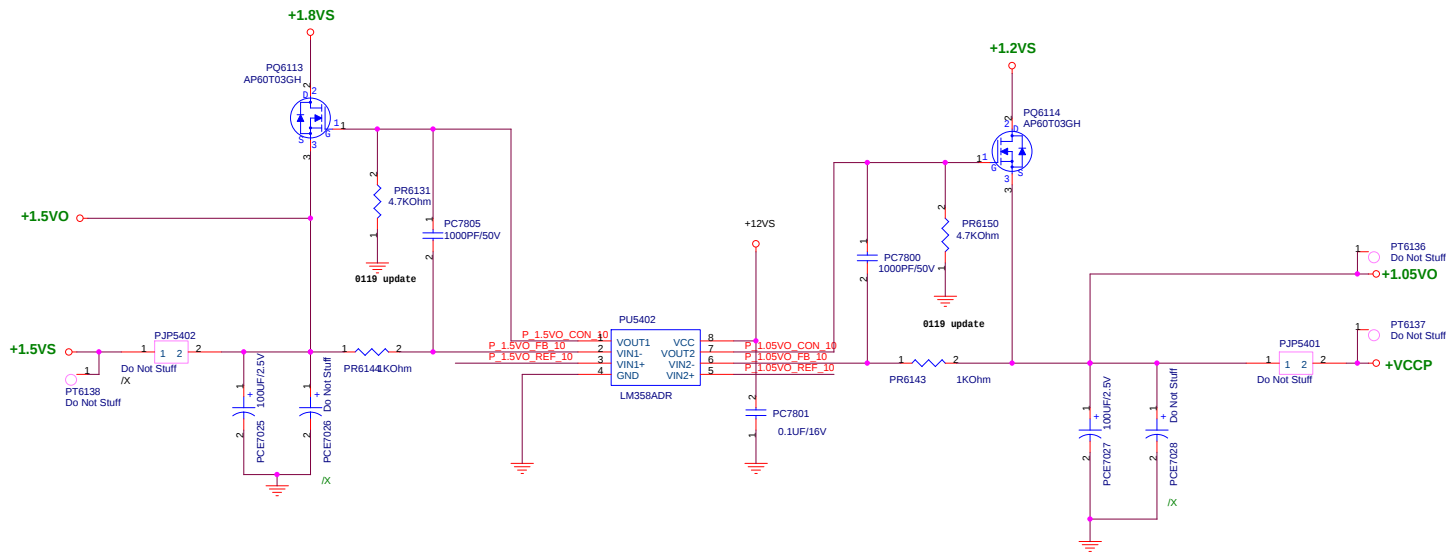
DDR Power Rev:1.00

888

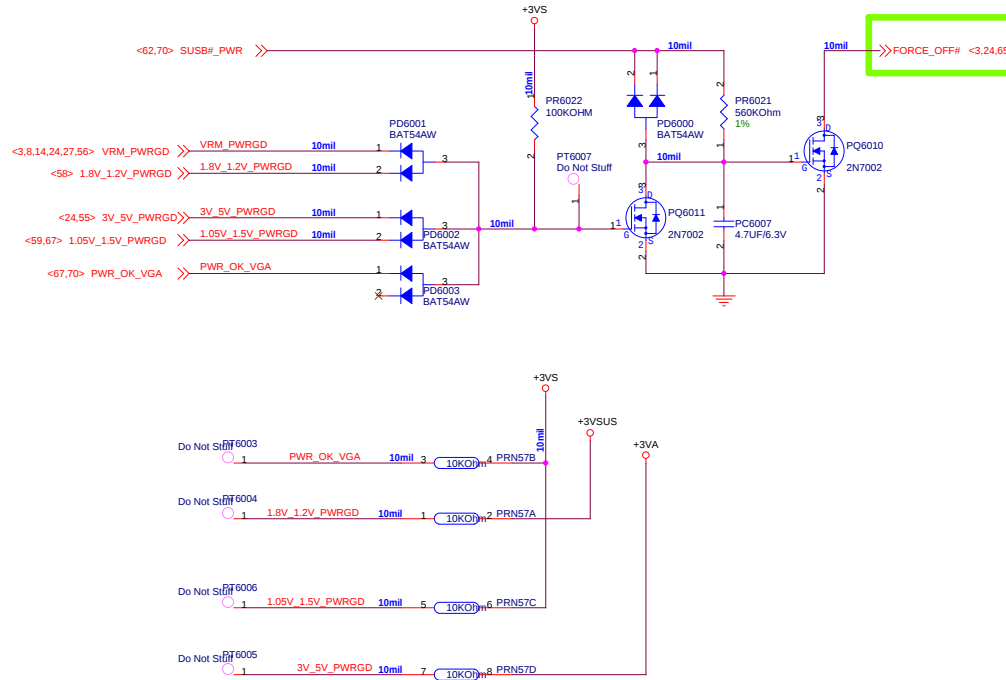
ASUS		Title :	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
A3		1.1	
Date: Thursday, September 27, 2007		Sheet 57 of 70	

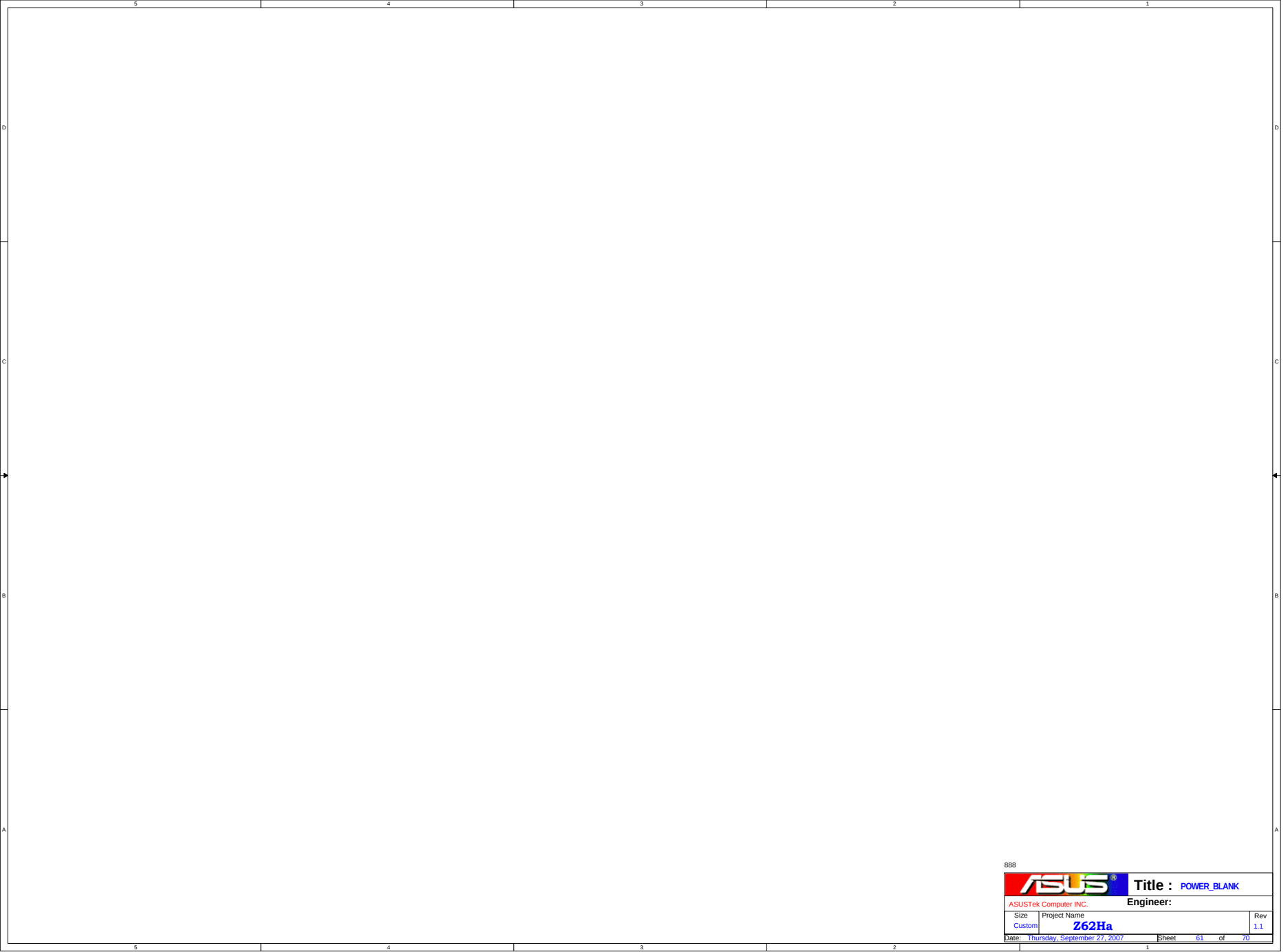
PR311 from 62K change to 200K <modify by PCB V1.1G>





Power Good Detector

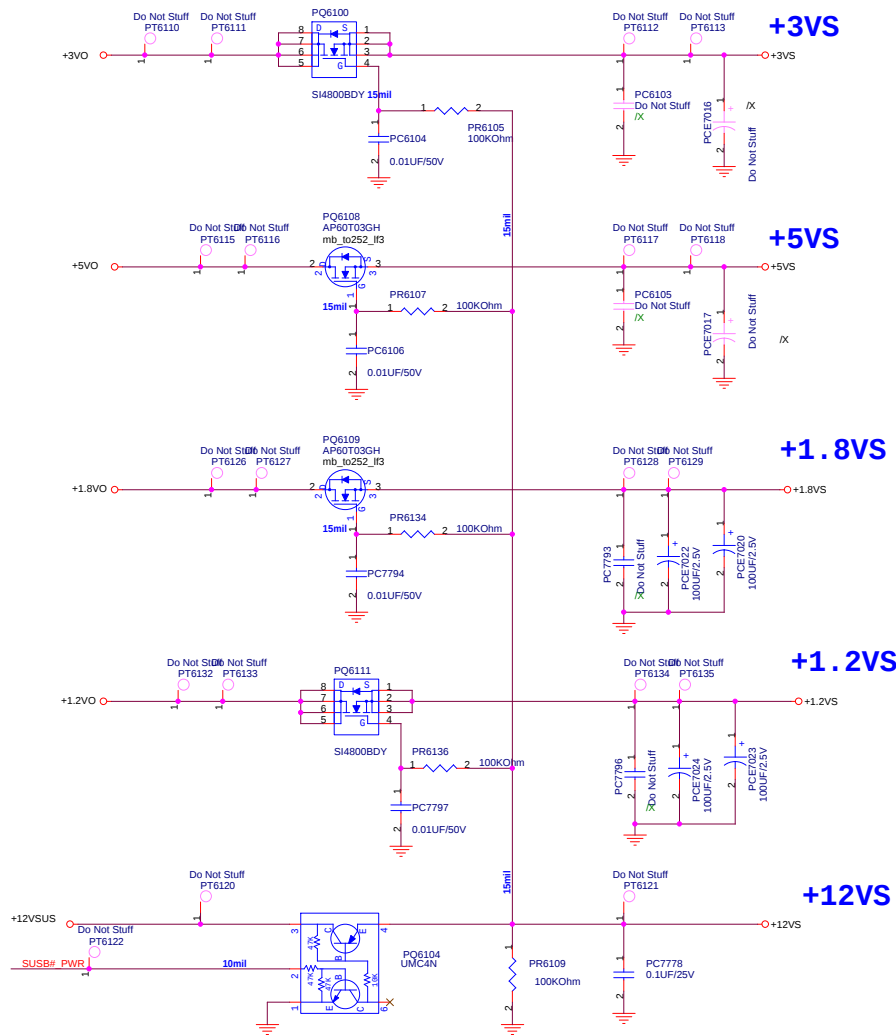




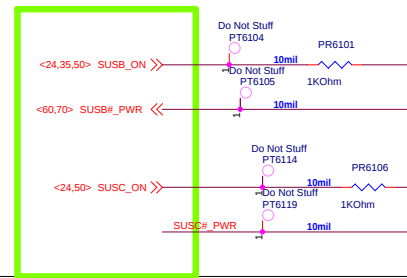
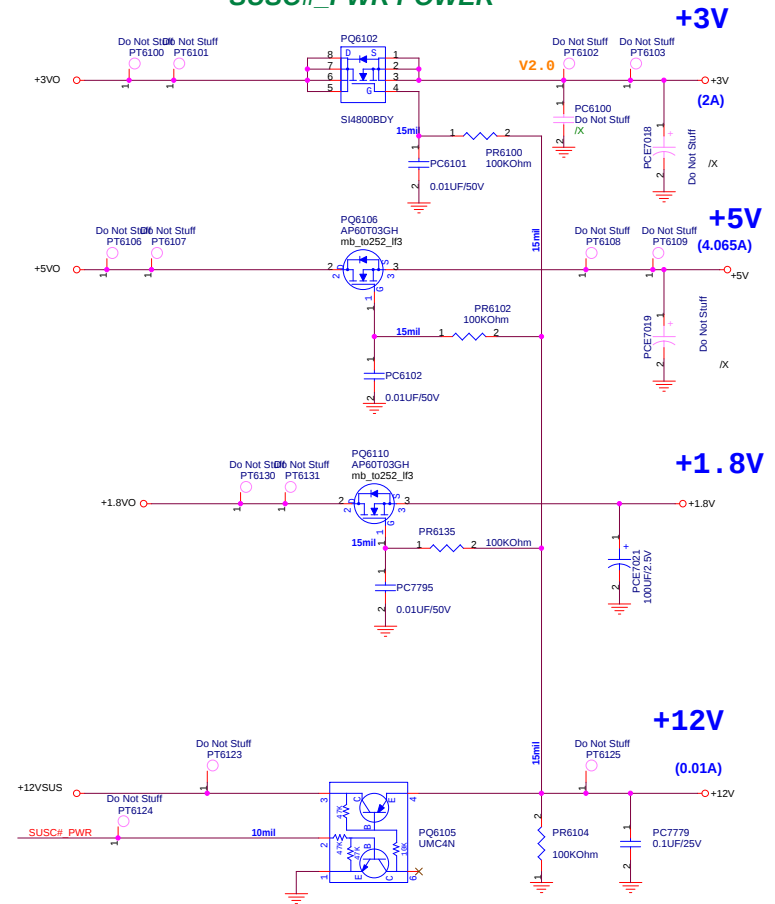
888

		Title : POWER_BLANK	
ASUSTek Computer INC.		Engineer:	
Size	Project Name		Rev
Custom	Z62Ha		1.1
Date: Thursday, September 27, 2007		Sheet 61 of 70	

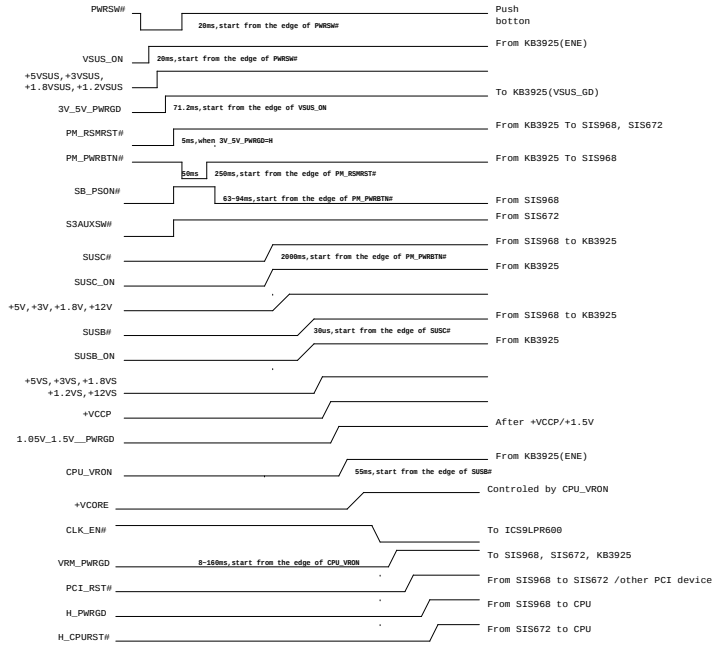
SUSB#_PWR POWER



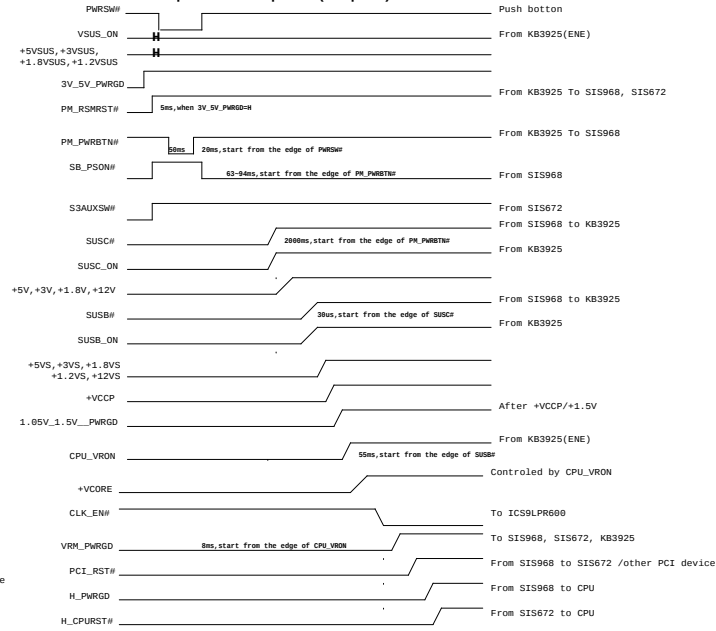
SUSC#_PWR POWER



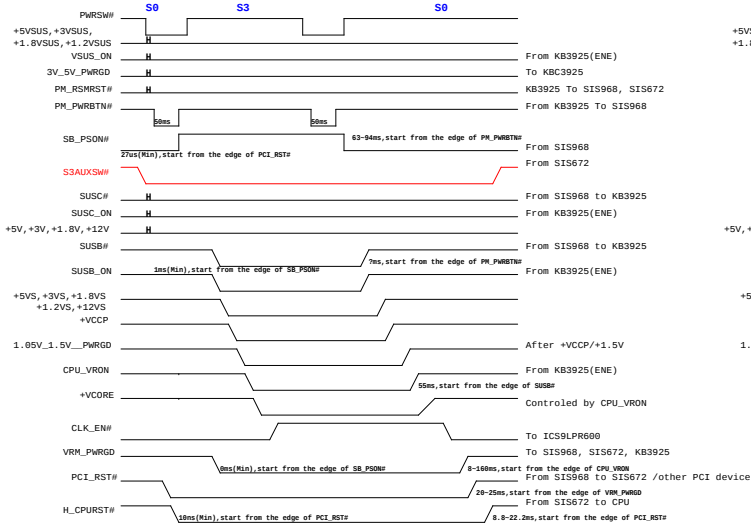
BATTERY ONLY POWER ON TIMING



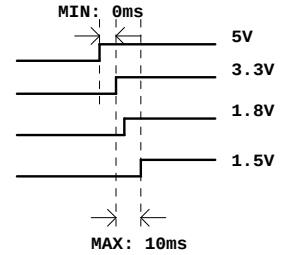
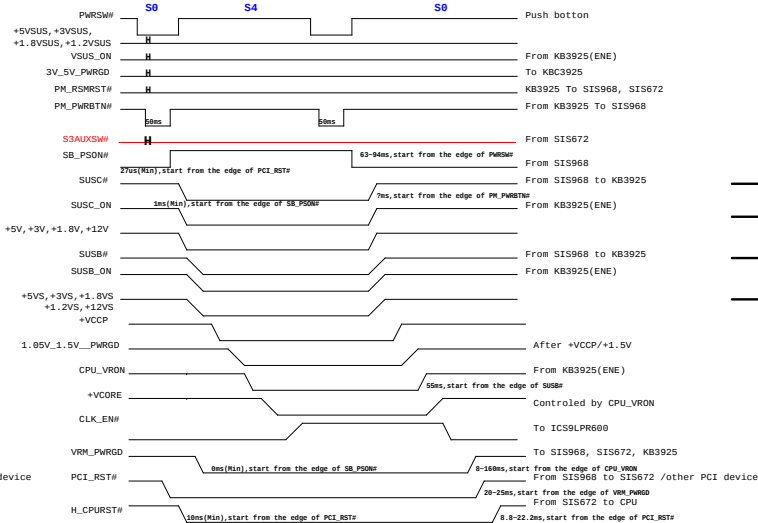
First time DCIN power on sequence (Adaptor)



Z62H S3 SUSPEND AND RESUME TIMING



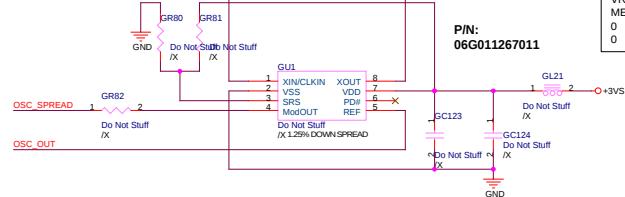
Z62H S4 SUSPEND AND RESUME TIMING



ADD GR26 10Mohm for
27HHz Un-Oscillate
<modify by PCB V1.1G>

GC120 & GC121 from 22pF
change to 18pF <modify
by PCB V1.1G>

OPTIONAL SPREAD SPECTRUM

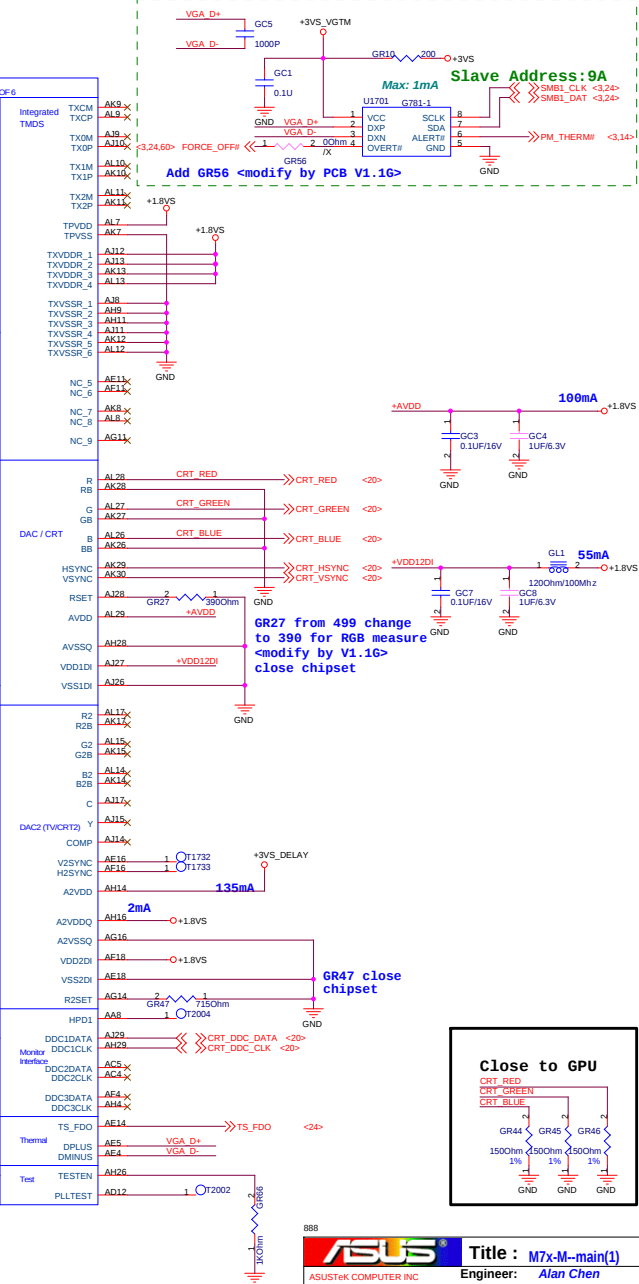
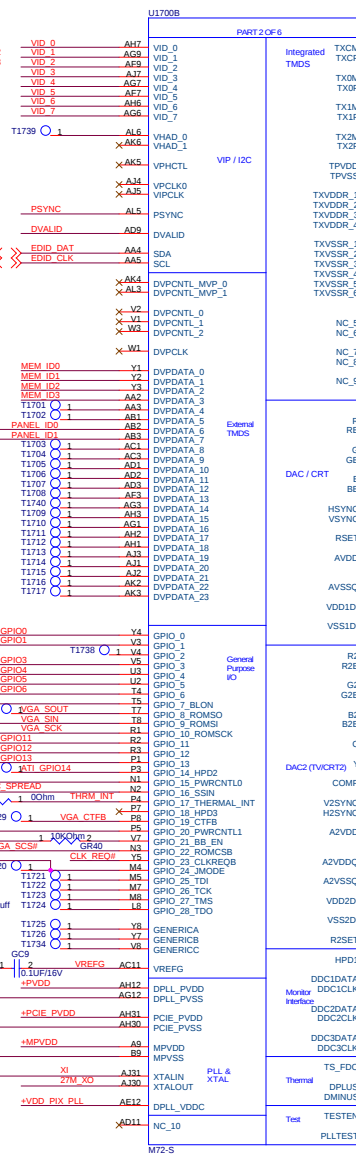
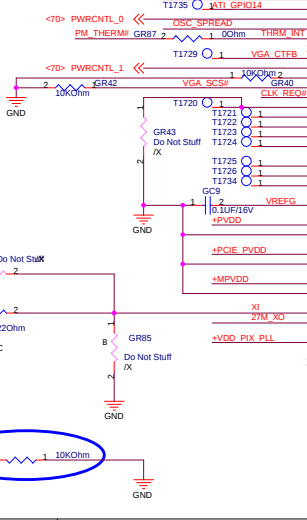
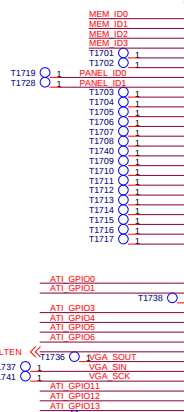
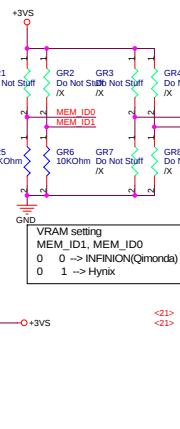
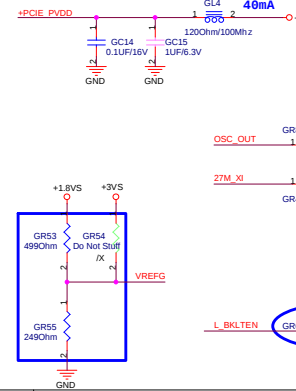
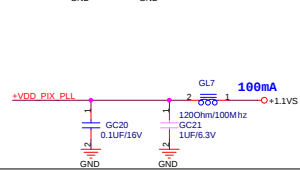
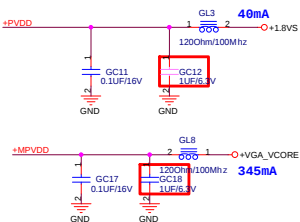


GPIO[0]: Tx Power Savings Enable	GPIO[1]: Tx De-emphasis Enable
0: 50% Tx output swing	0: Tx de-emphasis disabled
1: full Tx output swing (recommended)	1: Tx de-emphasis enable
(default 0, internal pull-down)	(default 0, internal pull-down)

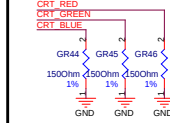
Pin	Description	M66N, M71M	M72N, M76N
V101	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
V103	ENABLE NO AUDIO	X	X
V105	64 BIT BAYS DISABLED	NA	0
P100	PCIe PMR Saving Mode	1	1
P101	PCIe TRANSMITTER DE-EMPHASIS ENABLED	1	1
P104	CEBUS SIGNALS NOT MIXED OUT	0	0
P106	(H671)BIAS CURRENT FOR PCIe PHY PLL	0	0
P107	(H671)BIAS CURRENT FOR PCIe PHY PLL	0	0
P108	(H673)BIAS CURRENT FOR PCIe PHY PLL	1	1
P108.22	(H672/18)BIAS CURRENT FOR PCIe PHY PLL	1	1
P108.22	ENABLE External BIOS ROM	NA	0
P101[13:1,0]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X	X
P59C	ONCHIE VIP ENABLE STRAPS	X	X
P59C	VGA ENABLED	NA	0

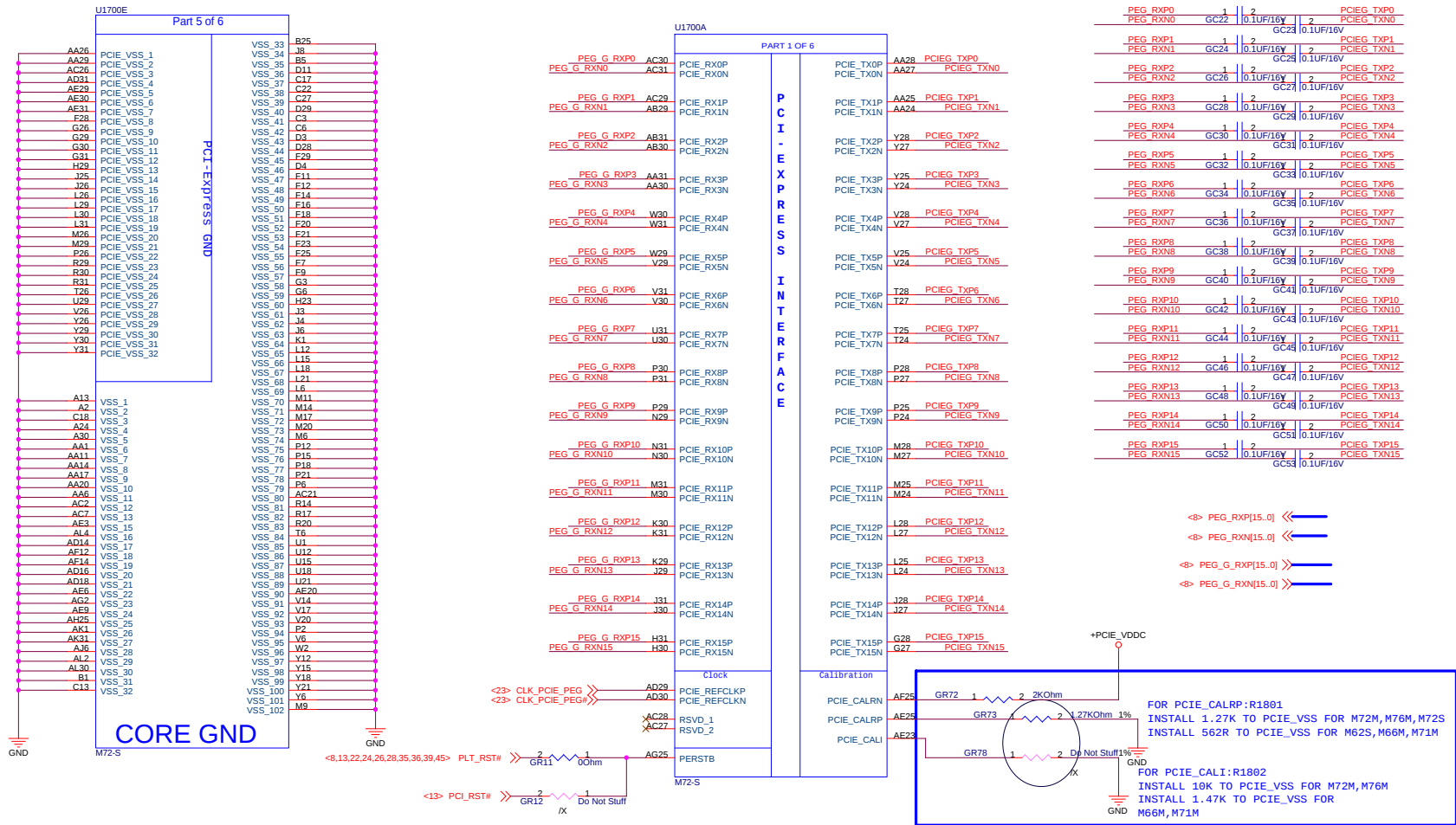
R1.1 Item 35

RECOMMENDED SETTINGS
@= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE



Close to GPU





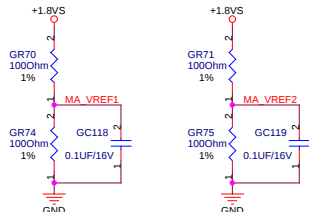
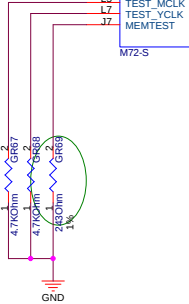
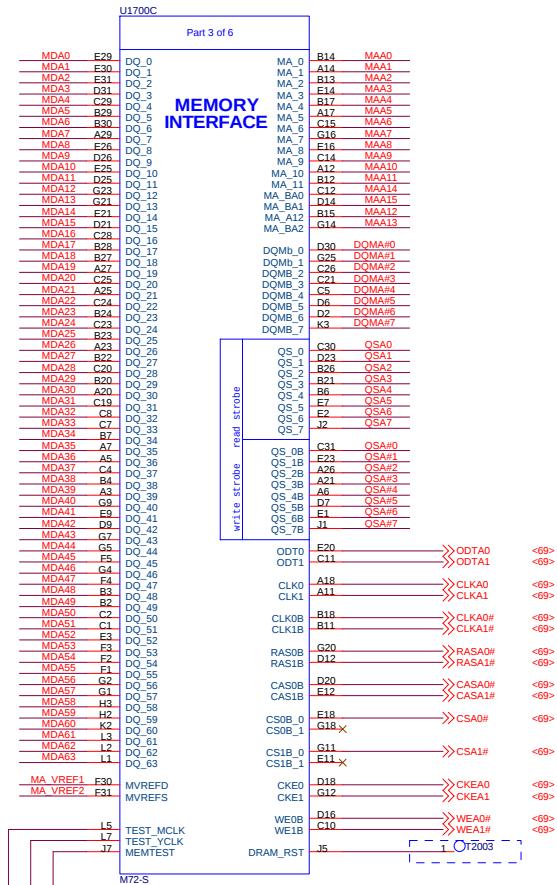
<69> MDA[63..0] << >> <69>

>> MAA[15..0] <69>

>> DQMA[7..0] <69>

<< QSA[7..0] <69>

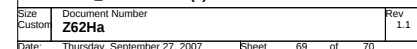
<< QSAH[7..0] <69>



M7REFD-S_A/B

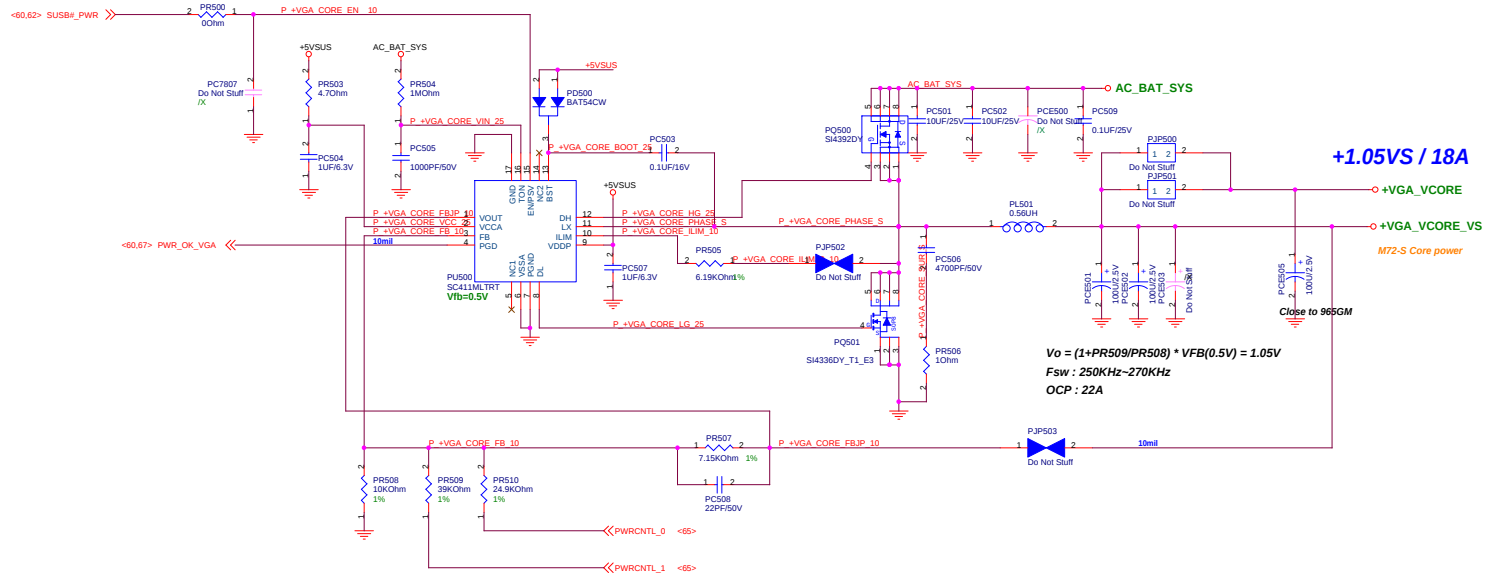
R	->1.8VS	R	->GND
GDDR2	100		100
GDDR3	40.2		100

888



Enable Signal :

Implemet Intel 965GM --> PR502
Implemet M72-S Chipset --> PR500



+1.05VS

VGMCH_SEL0	VGMCH_SEL1	Voltage
L	L	1.093V
X	L	1.001V
L	X	0.949V
X	X	0.857V

888

ASUSTek COMPUTER INC.

6-Fly_Ap0150_U-Tp_Rtl_Pchsw_Taipei_Taiwan_SOC

File

VGA_VCORE

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Document Number

Custom

Z52Ha

Date

Thursday, September 27, 2007

Sheet

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Rev

1.1