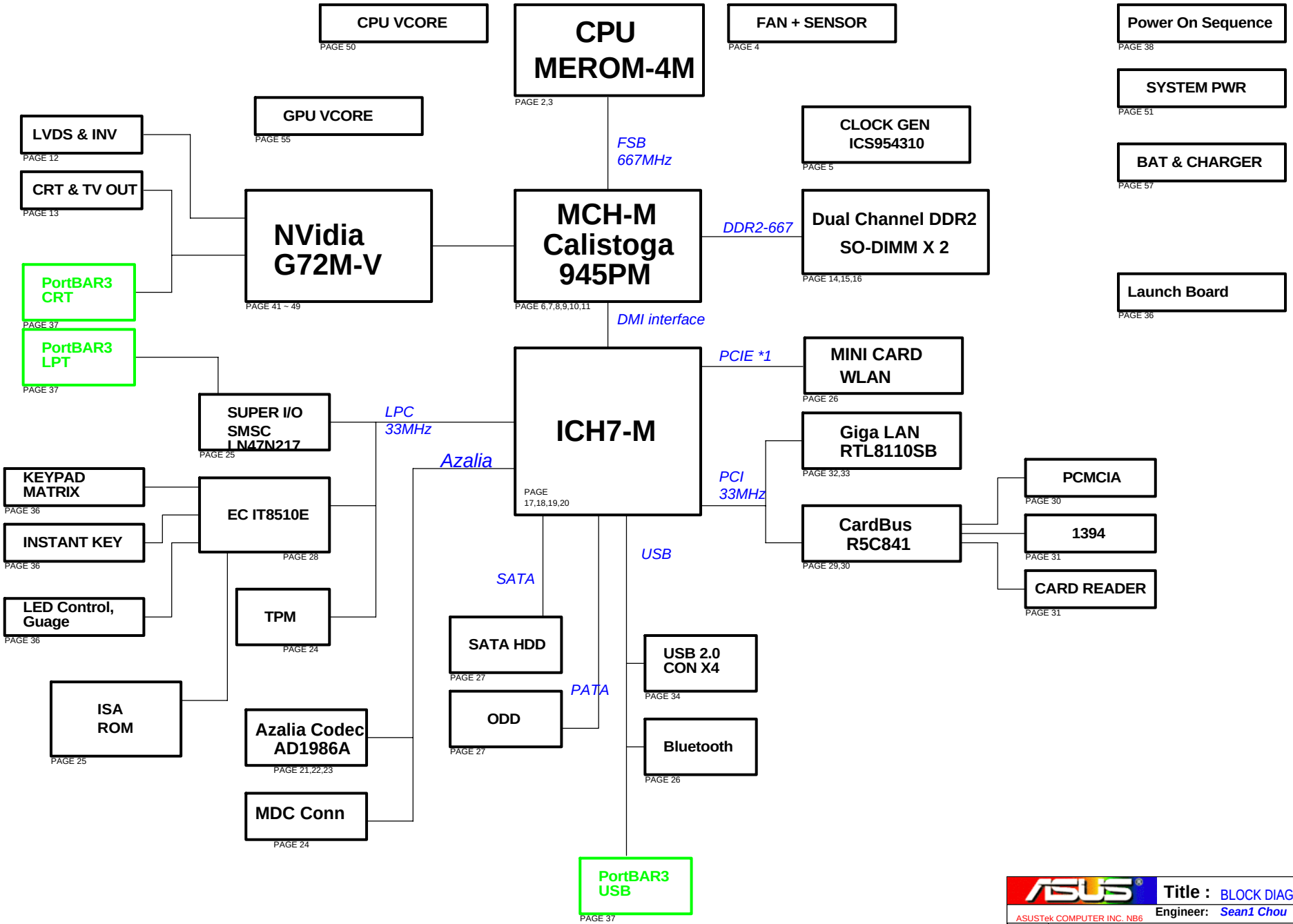
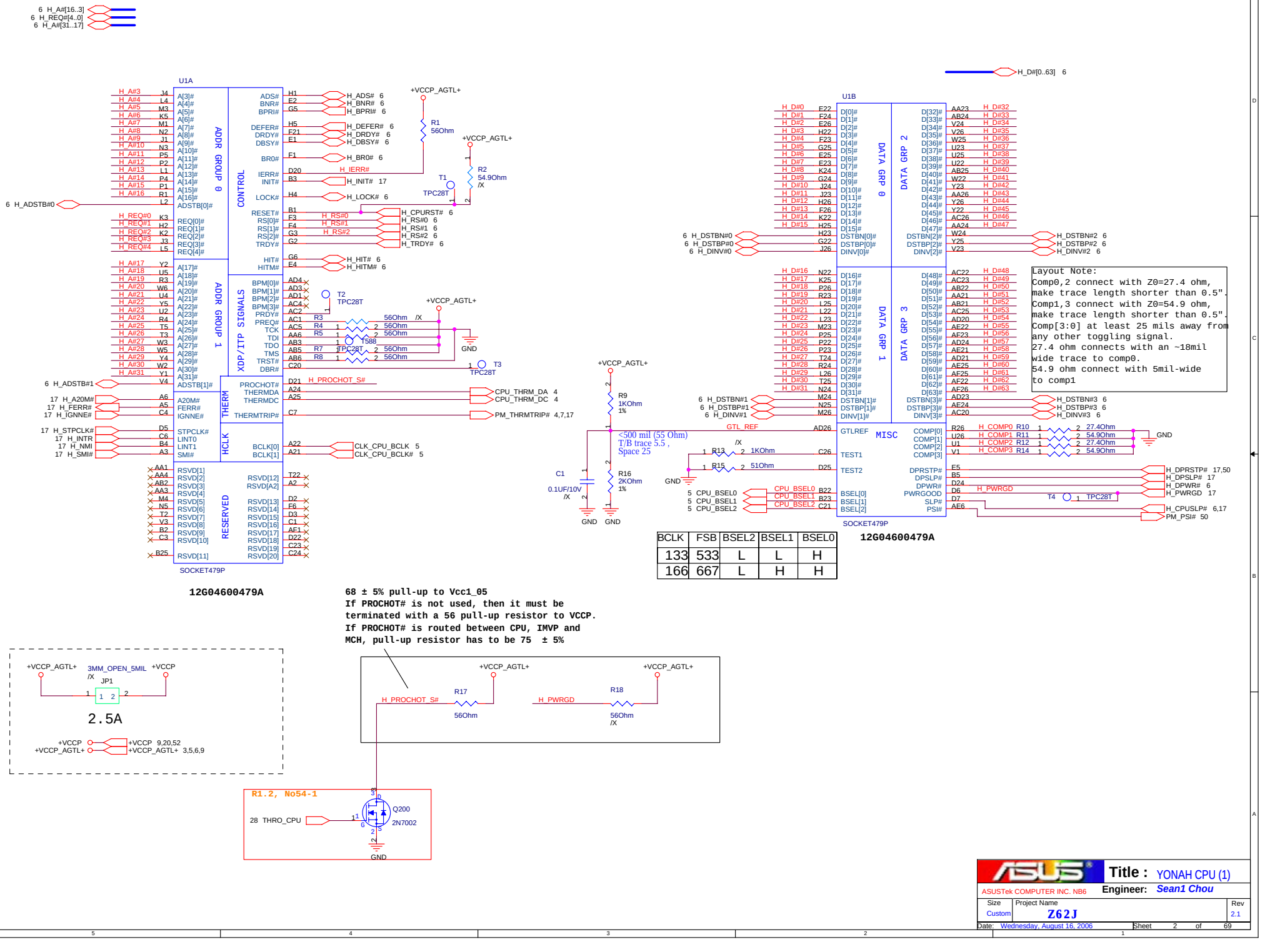
Z62JM Block Diagram



Title : BLOCK DIAGRAM		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 1 of 69	


6 H_A#[16..3]
6 H_REQ#[4..0]
6 H_A#[31..17]
U1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
6 H_ADSTB#0
6 H_ADSTB#1
+VCCP_AGTL+
R1 56Ohm
R2 54.9Ohm /X
T1 TPC28T
T2 TPC28T
T3 TPC28T
T588
H_IERR#
H_RS#0
H_RS#1
H_RS#2
H_CPURST# 6
H_RS#0 6
H_RS#1 6
H_RS#2 6
H_TRDY# 6
H_HIT# 6
H_HITM# 6
H_INIT# 17
H_LOCK# 6
H_ADS# 6
H_BNR# 6
H_BPRI# 6
H_DEFER# 6
H_DRDY# 6
H_DBSY# 6
H_BR0# 6
H_PROCHOT_S#
CPU_THRM_DA 4
CPU_THRM_DC 4
PM_THRMTRIP# 4,7,17
CLK_CPU_BCLK 5
CLK_CPU_BCLK# 5
56Ohm /X
SOCKET479P
12G04600479A
H_D#[0..63] 6
U1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0
6 H_DSTBN#1
6 H_DSTBP#1
6 H_DINV#1
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#2 6
H_DSTBN#3 6
H_DSTBP#3 6
H_DINV#3 6
GTL_REF
R9 1KOhm 1%
R16 2KOhm 1%
C1 0.1UF/10V /X
<500 mil (55 Ohm) T/B trace 5.5 , Space 25
R13 1KOhm /X
R15 51Ohm
5 CPU_BSEL0
5 CPU_BSEL1
5 CPU_BSEL2
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R10 27.4Ohm
R11 54.9Ohm
R12 27.4Ohm
R14 54.9Ohm
H_COMP0
H_COMP1
H_COMP2
H_COMP3
H_DPRSTP# 17,50
H_DPSLP# 17
H_DPWR# 6
H_PWRGD 17
H_CPUSLP# 6,17
PM_PSI# 50
T4 TPC28T
GND
Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 ± 5%
+VCCP_AGTL+
3MM_OPEN_5MIL /X
JP1
+VCCP
2.5A
+VCCP 9,20,52
+VCCP_AGTL+ 3,5,6,9
H_PROCHOT_S#
R17 56Ohm
H_PWRGD
R18 56Ohm /X
R1.2, No54-1
28 THRO_CPU
Q200 2N7002
GND
Title : YONAH CPU (1)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 2 of 69

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

U1C

SOCKET479P

12G04600479A

U1D

SOCKET479P

12G04600479A

+VCCP_AGTL+ 2,5,6,9

+VCORE 50

+1.5VS 7,9,20,26,35,52,56

R1.1,No43

unmount CE1,CE4

R2.1, No94-1

unmount CE54

C2~C31 22uF --> 10uF

Vcc Core Decoupling Caps
Place these on bottom side.

Place these caps on North side Secondary

CE1 470UF/2.5V /X

Place these caps on North side Secondary

C2 C3 C4 C5 C6 C7 C8 C9 10UF/6.3V

Place these caps on North side Primary

C12 C13 C14 C15 C16 10UF/6.3V

Place these caps on South side Primary

C18 C19 C20 C21 C22 10UF/6.3V

Place these caps on South side Secondary

C24 C25 C26 C27 C28 C29 C30 C31 10UF/6.3V

Place these caps on South side Secondary

CE4 470UF/2.5V /X

checklist suggests
0.1uF X5R

checklist suggests
10uF POSCAP

Close to B26 (VCCA)

+VCCA_CPU 120mA / 20mil

+VCCA_PROC

C41 10UF/10V C40 0.01UF/16V

+V1.05S (VCCP_CPU) Decoupling Capacitor (Place near CPU)

CE54 470UF/2.5V /X

C34 C35 C36 C37 C38 C39 0.1UF/10V

+1.5VS JP2 +VCCA_CPU

SHORT_PIN

0.12A

VCCSENCE/VSSSENCE need to be routed as 27.4ohm

Layout note:Route VCCSENSE and VSSSENSE trace at 27.4 ohm with 25 mils spacing mismatch and 18mils trace on 7mils spacing.

Place pull-up/down resisters within 1 inch of CPU.

Title : Yonah CPU (2)

ASUSTek COMPUTER INC. NB6 Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

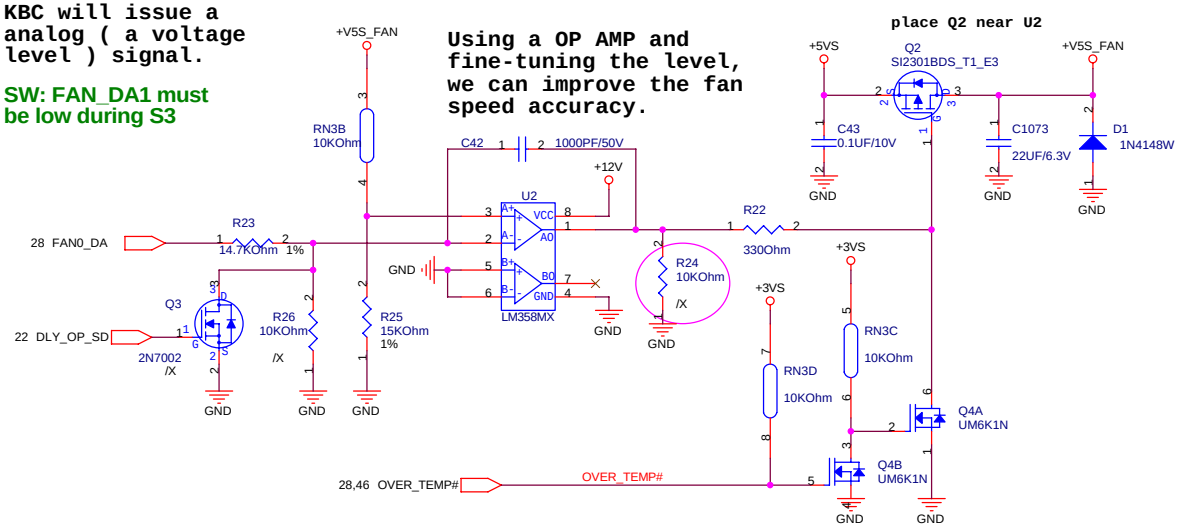
Date: Wednesday, August 16, 2006 Sheet 3 of 69

Fan Speed Control

KBC will issue a analog (a voltage level) signal.

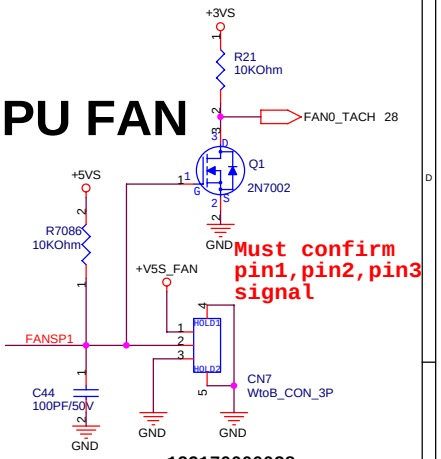
SW: FAN_DA1 must be low during S3

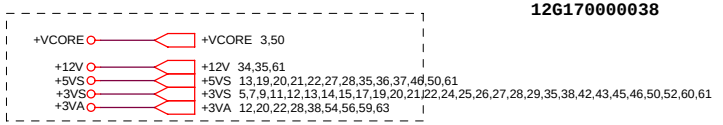
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



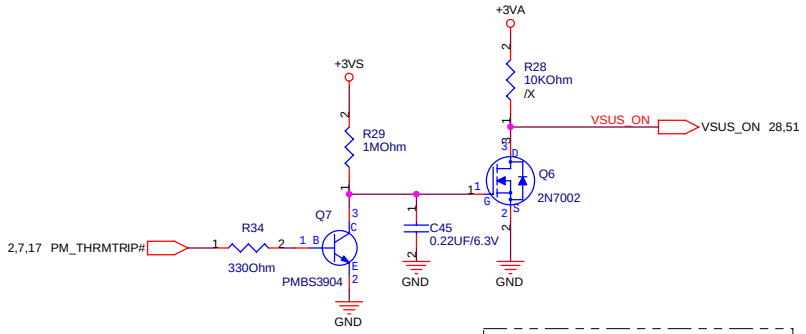
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

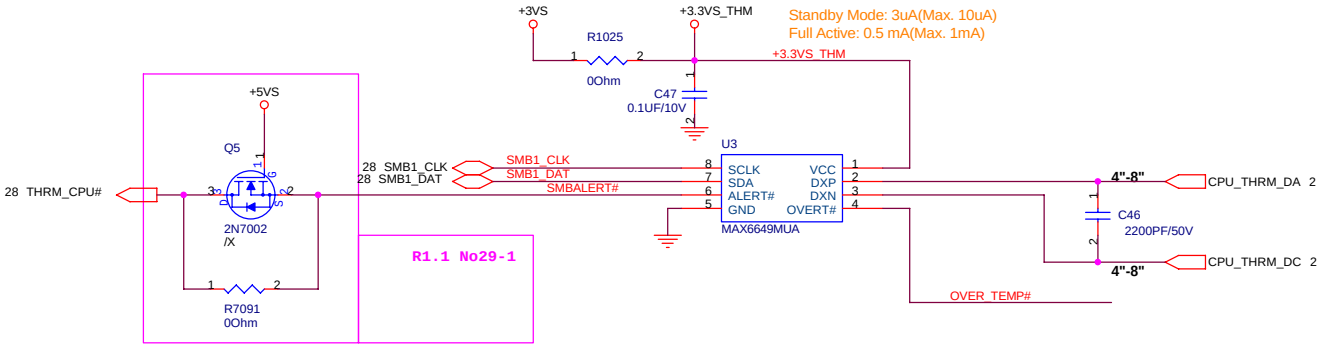
CPU FAN





U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSTek COMPUTER INC. NB6	Title : THER-SENSOR,FAN	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 4 of 69	

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD1(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	None

		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,6,9

+3VS → +3VS 4,7,9,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

PLACE termination close to source IC

Pin34 is PWRSAVE#

27MHz selected by SELPCIE0_LCD# and SELLCD_27#

internal pull high

PEREQ Register:
00100000 PCIE*3 is controlled <= check:PCIE*3 is controlled by CLKREQ#
00000010 PCIE*4 is controlled <= reserved only

R72 change to 39Ohm R1.1 No30-1

R77,R79,R83 change to 470hm.

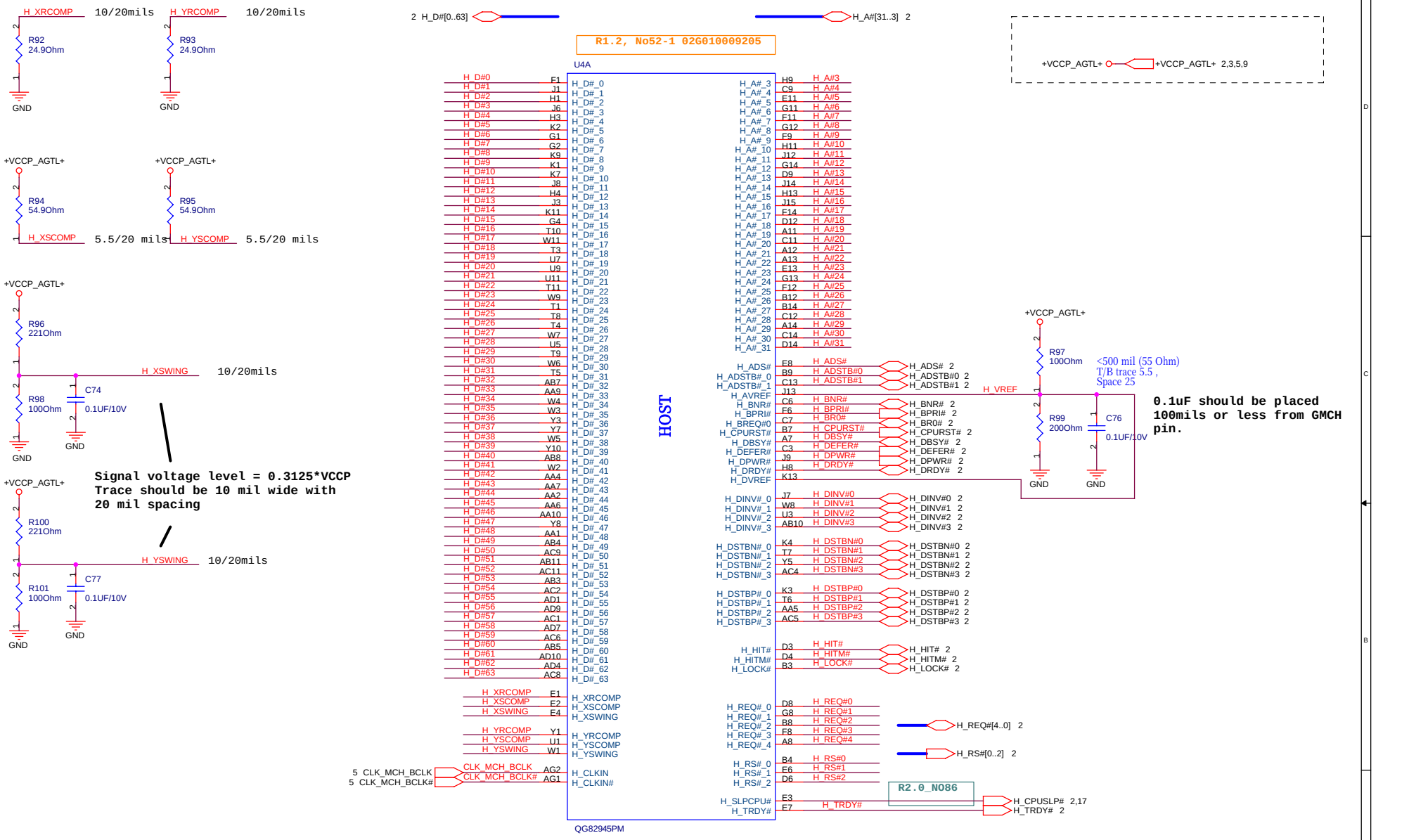
R81 change to 270hm

R1.2, No59

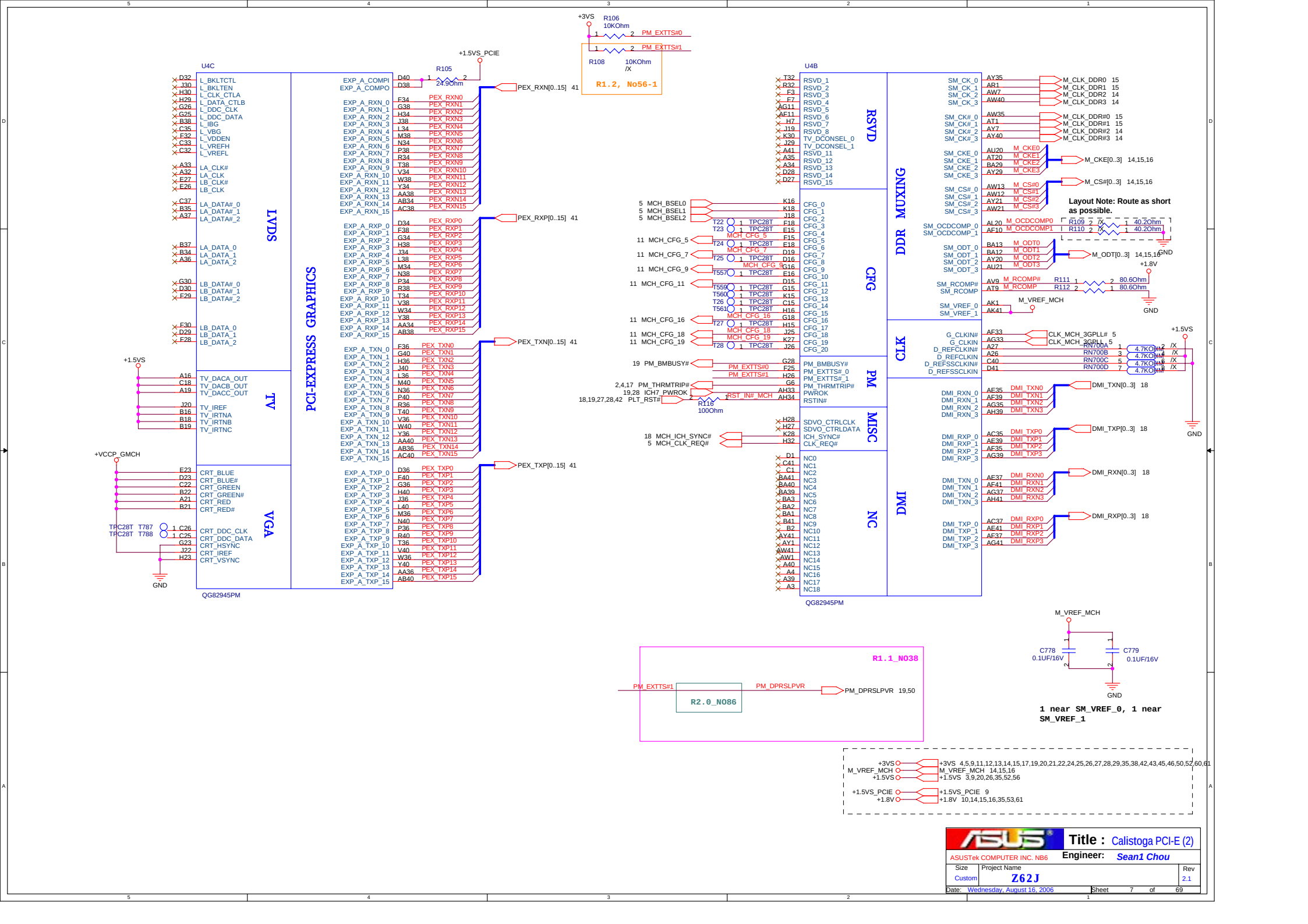
clock gen version change to ICS954310CGLFT

No2.1, No97

Title :	CLOCK GEN	
ASUSTek COMPUTER INC. NB6	Engineer:	Sean1 Chou
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 5 of 69	



ASUSTek COMPUTER INC. NB6	Title : Calistoga MCH (1)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 6 of 69	


U4C
L_BKLTCTL
L_BKLTEN
L_CLK_CTLA
L_DATA_CTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2
LVDS
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
VGA
PCI-EXPRESS GRAPHICS
EXP_A_COMPI
EXP_A_COMPO
EXP_A_RXN_0
EXP_A_RXN_1
EXP_A_RXN_2
EXP_A_RXN_3
EXP_A_RXN_4
EXP_A_RXN_5
EXP_A_RXN_6
EXP_A_RXN_7
EXP_A_RXN_8
EXP_A_RXN_9
EXP_A_RXN_10
EXP_A_RXN_11
EXP_A_RXN_12
EXP_A_RXN_13
EXP_A_RXN_14
EXP_A_RXN_15
EXP_A_RXP_0
EXP_A_RXP_1
EXP_A_RXP_2
EXP_A_RXP_3
EXP_A_RXP_4
EXP_A_RXP_5
EXP_A_RXP_6
EXP_A_RXP_7
EXP_A_RXP_8
EXP_A_RXP_9
EXP_A_RXP_10
EXP_A_RXP_11
EXP_A_RXP_12
EXP_A_RXP_13
EXP_A_RXP_14
EXP_A_RXP_15
EXP_A_TXN_0
EXP_A_TXN_1
EXP_A_TXN_2
EXP_A_TXN_3
EXP_A_TXN_4
EXP_A_TXN_5
EXP_A_TXN_6
EXP_A_TXN_7
EXP_A_TXN_8
EXP_A_TXN_9
EXP_A_TXN_10
EXP_A_TXN_11
EXP_A_TXN_12
EXP_A_TXN_13
EXP_A_TXN_14
EXP_A_TXN_15
EXP_A_TXP_0
EXP_A_TXP_1
EXP_A_TXP_2
EXP_A_TXP_3
EXP_A_TXP_4
EXP_A_TXP_5
EXP_A_TXP_6
EXP_A_TXP_7
EXP_A_TXP_8
EXP_A_TXP_9
EXP_A_TXP_10
EXP_A_TXP_11
EXP_A_TXP_12
EXP_A_TXP_13
EXP_A_TXP_14
EXP_A_TXP_15
QG82945PM
+1.5VS_PCIE
R105
24.9Ohm
PEX_RXN[0..15] 41
PEX_RXP[0..15] 41
PEX_TXN[0..15] 41
PEX_TXP[0..15] 41
+3VS
R106
10KOhm
PM_EXTTS#0
PM_EXTTS#1
R108
10KOhm
/X
R1.2, No56-1
U4B
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
TV_DCONSEL_0
TV_DCONSEL_1
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
CFG
PM_BMBUSY#
PM_EXTTS#_0
PM_EXTTS#_1
PM_THRMTRIP#
PWROK
RSTIN#
PM
SDVO_CTRLCLK
SDVO_CTRLDATA
ICH_SYNC#
CLK_REQ#
MISC
NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC
SM_CK_0
SM_CK_1
SM_CK_2
SM_CK_3
SM_CK#_0
SM_CK#_1
SM_CK#_2
SM_CK#_3
SM_CKE_0
SM_CKE_1
SM_CKE_2
SM_CKE_3
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_OCDCOMP_0
SM_OCDCOMP_1
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP#
SM_RCOMP
SM_VREF_0
SM_VREF_1
DDR MUXING
G_CLKIN#
G_CLKIN
D_REFCLKIN#
D_REFCLKIN
D_REFSSCLKIN#
D_REFSSCLKIN
CLK
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI
QG82945PM
Layout Note: Route as short as possible.
M_CLK_DDR0 15
M_CLK_DDR1 15
M_CLK_DDR2 14
M_CLK_DDR3 14
M_CKE[0..3] 14,15,16
M_CS#[0..3] 14,15,16
M_ODT[0..3] 14,15,16
M_OCDCOMP0
M_OCDCOMP1
40.2Ohm
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_RCOMP#
M_RCOMP
80.6Ohm
M_VREF_MCH
+1.8V
GND
CLK_MCH_3GPLL# 5
CLK_MCH_3GPLL 5
4.7KOhm
RN700A
RN700B
RN700C
RN700D
DMI_TXN[0..3] 18
DMI_TXP[0..3] 18
DMI_RXN[0..3] 18
DMI_RXP[0..3] 18
+1.5VS
+VCCP_GMCH
TPC28T T787
TPC28T T788
C26
C25
5 MCH_BSEL0
5 MCH_BSEL1
5 MCH_BSEL2
11 MCH_CFG_5
11 MCH_CFG_7
11 MCH_CFG_9
11 MCH_CFG_11
11 MCH_CFG_16
11 MCH_CFG_18
11 MCH_CFG_19
MCH_CFG_5
MCH_CFG_7
MCH_CFG_9
MCH_CFG_16
MCH_CFG_18
MCH_CFG_19
TPC28T
19 PM_BMBUSY#
2,4,17 PM_THRMTRIP#
19,28 ICH7_PWROK
18,19,27,28,42 PLT_RST#
RST_IN# MCH
R118
100Ohm
18 MCH_ICH_SYNC#
5 MCH_CLK_REQ#
R1.1_N038
PM_EXTTS#1
R2.0_N086
PM_DPRSLPVR
PM_DPRSLPVR 19,50
M_VREF_MCH
C778
0.1UF/16V
C779
0.1UF/16V
1 near SM_VREF_0, 1 near SM_VREF_1
+3VS 4,5,9,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61
M_VREF_MCH 14,15,16
+1.5VS 3,9,20,26,35,52,56
+1.5VS_PCIE 9
+1.8V 10,14,15,16,35,53,61
Title : Calistoga PCI-E (2)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
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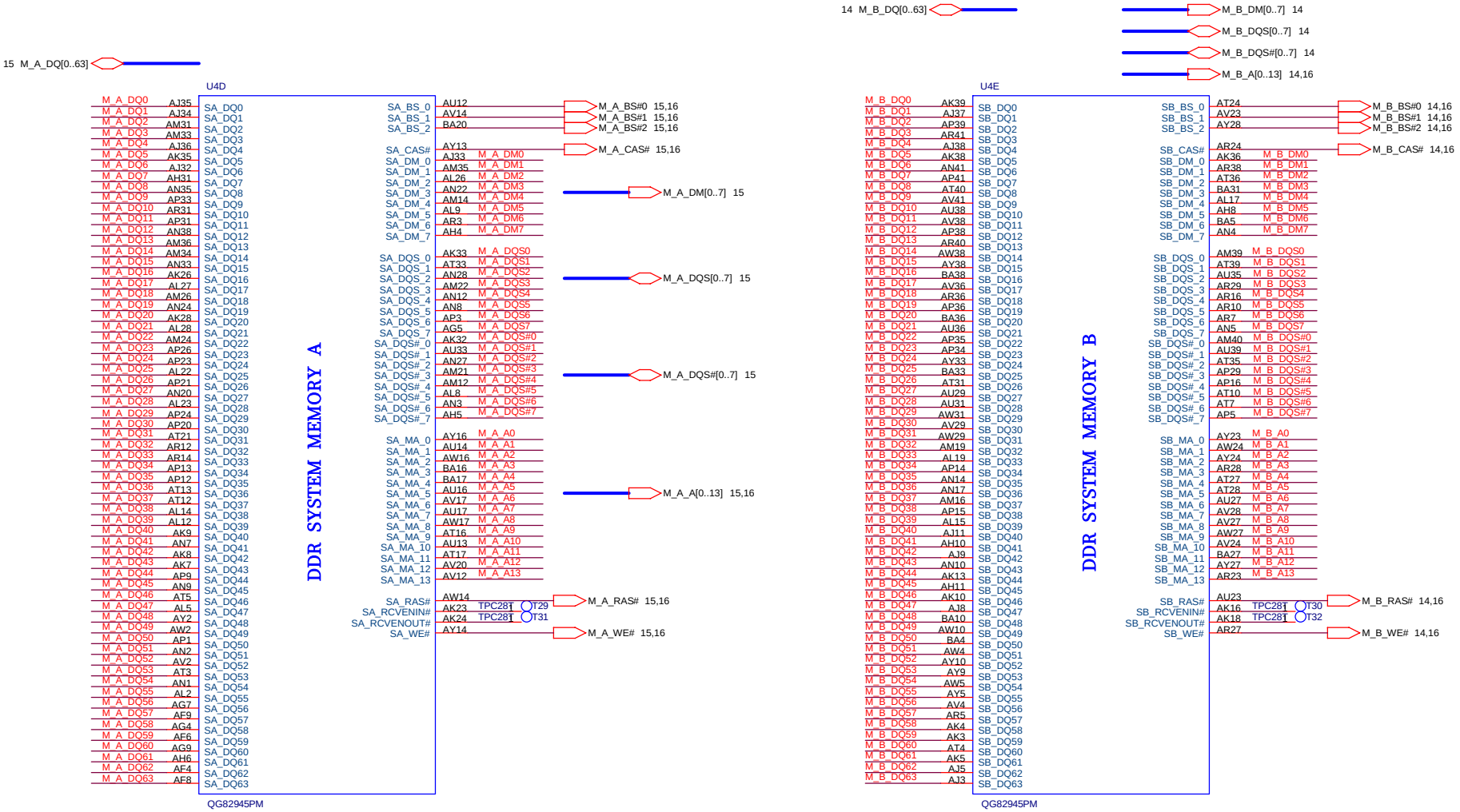


ASUSTek COMPUTER INC. NB6	Title : Calistoga DDR2 (3)		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 8 of 69		

VCCA_3GBG

NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

+VCCP — 3MM_OPEN_5MIL /X — JP28 — +VCCP_GMCH

Z62J use 1.05V

R2.1, No94 unmount CE8

+VCCP_AGTL+ 2,3,5,6 — +VCCP_GMCH 7,10 — +1.5VS_PCIE 7 — +3VS 4,5,7,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52 — +2.5VS 35,44,46,54 — +1.5VS 3,7,20,26,35,52,56

+2.5VS — C956 4.7UF/10V — C901 0.1UF/10V — GND

VCCA_3GBG ***2 mA***

D77 — R1026 10Ohm — BAT54C — +VCCP_GMCH

+1.5VS — L88 120Ohm/100Mhz — **VCC3G** — +1.5VS_PCIE — ***1500 mA***

C955 0.1UF/10V — C904 10UF/10V — C905 10UF/10V — GND

+1.5VS_3GPLL — L90 30Ohm/100Mhz — **VCCA3GPLL**

C82 0.1UF/10V — C83 10UF/10V — GND

+1.5VS_VCCAUX — L91 100Ohm/100Mhz — **VCCAUX**

CE50 470UF/2.5V — C912 0.1UF/10V — GND

Place filter components close to GMCH

+1.5VS_DPLLA — L3 30Ohm/100Mhz — **VCCA_DPLLA** ***50 mA***

CE10 470UF/2.5V /X — C916 0.1UF/10V — GND

+1.5VS_DPLLB — L4 30Ohm/100Mhz — **VCCA_DPLLB** ***50 mA***

CE13 470UF/2.5V /X — C919 0.1UF/10V — GND

+1.5VS_HPLL — L5 120Ohm/100Mhz — **VCCA_HPLL** ***45 mA***

C920 22UF/6.3V — C85 0.1UF/10V — GND

+1.5VS_MPLL — L6 120Ohm/100Mhz — **VCCA_MPLL** ***45 mA***

C921 22UF/6.3V — C87 0.1UF/10V — GND

+1.5VS — **VCCD_TVDAC** — C84 0.022UF/25V — C909 0.1UF/10V — ***24 mA***

+1.5VS — **VCCDQ_TVDAC** — C86 0.022UF/25V — C913 0.1UF/10V

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

U4H

+1.5VS_PCIE — H22 VCCSYNC

C30 VCC_TXLVDS0 — B30 VCC_TXLVDS1 — A30 VCC_TXLVDS2

AJ41 VCC3G0 — AB41 VCC3G1 — Y41 VCC3G2 — V41 VCC3G3 — R41 VCC3G4 — N41 VCC3G5 — L41 VCC3G6

+2.5VS — +1.5VS_3GPLL — AC33 VCCA_3GPLL — G41 VCCA_3GBG — H41 VSSA_3GBG

+VCCP_GMCH — F21 VCCA_CRTDAC0 — F21 VCCA_CRTDAC1 — G21 VSSA_CRTDAC

+1.5VS_DPLLA — B26 VCCA_DPLLA — +1.5VS_DPLLB — C39 VCCA_DPLLB — +1.5VS_HPLL — AF1 VCCA_HPLL

A38 VCCA_LVDS — B39 VSSA_LVDS

+1.5VS_MPLL — AF2 VCCA_MPLL

+1.5VS — H20 VCCA_TVBG — G20 VSSA_TVBG

+1.5VS — E19 VCCA_TVDACA0 — E19 VCCA_TVDACA1 — C20 VCCA_TVDACB0 — D20 VCCA_TVDACB1 — E20 VCCA_TVDACC0 — F20 VCCA_TVDACC1

+1.5VS — AH1 VCCD_HMPLL0 — AH2 VCCD_HMPLL1

A28 VCCD_LVDS0 — B28 VCCD_LVDS1 — C28 VCCD_LVDS2

+1.5VS — D21 VCCD_TVDAC

+3VS — A23 VCC_HV0 — B23 VCC_HV1 — B25 VCC_HV2

+1.5VS — H19 VCCD_QTVDAC

+1.5VS_VCCAUX — AK31 VCCAUX0 — AF31 VCCAUX1 — AE31 VCCAUX2 — AC31 VCCAUX3 — AL30 VCCAUX4 — AK30 VCCAUX5 — AJ30 VCCAUX6 — AH30 VCCAUX7 — AG30 VCCAUX8 — AE30 VCCAUX9 — AE30 VCCAUX10 — AD30 VCCAUX11 — AC30 VCCAUX12 — AG29 VCCAUX13 — AF29 VCCAUX14 — AE29 VCCAUX15 — AD29 VCCAUX16 — AC29 VCCAUX17 — AG28 VCCAUX18 — AF28 VCCAUX19 — AE28 VCCAUX20 — AH22 VCCAUX21 — AJ21 VCCAUX22 — AH21 VCCAUX23 — AJ20 VCCAUX24 — AH20 VCCAUX25 — AH19 VCCAUX26 — P19 VCCAUX27 — P16 VCCAUX28 — AH15 VCCAUX29 — P15 VCCAUX30 — AH14 VCCAUX31 — AG14 VCCAUX32 — AF14 VCCAUX33 — AE14 VCCAUX34 — Y14 VCCAUX35 — AF13 VCCAUX36 — AE13 VCCAUX37 — AF12 VCCAUX38 — AE12 VCCAUX39 — AD12 VCCAUX40

QG82945PM

POWER

+VCCP_AGTL+

VTT_0 AC14 — VTT_1 AB14 — VTT_2 W14 — VTT_3 V14 — VTT_4 T14 — VTT_5 R14 — VTT_6 P14 — VTT_7 N14 — VTT_8 M14 — VTT_9 L14

VTT_10 AD13 — VTT_11 AC13 — VTT_12 AB13 — VTT_13 AA13 — VTT_14 Y13 — VTT_15 W13 — VTT_16 V13 — VTT_17 U13 — VTT_18 T13 — VTT_19 R13 — VTT_20 N13 — VTT_21 M13 — VTT_22 L13 — VTT_23 AB12 — VTT_24 AA12 — VTT_25 Y12 — VTT_26 W12 — VTT_27 V12 — VTT_28 U12 — VTT_29 T12 — VTT_30 R12 — VTT_31 P12 — VTT_32 N12 — VTT_33 M12 — VTT_34 L12 — VTT_35 R11 — VTT_36 P11 — VTT_37 N11 — VTT_38 M11 — VTT_39 R10 — VTT_40 P10 — VTT_41 N10 — VTT_42 M10 — VTT_43 P9 — VTT_44 N9 — VTT_45 M9 — VTT_46 R8 — VTT_47 P8 — VTT_48 N8 — VTT_49 M8 — VTT_50 P7 — VTT_51 N7 — VTT_52 M7 — VTT_53 R6 — VTT_54 P6 — VTT_55 M6 — VTT_56 A6 — VTT_57 R5 — VTT_58 P5 — VTT_59 N5 — VTT_60 M5 — VTT_61 P4 — VTT_62 N4 — VTT_63 M4 — VTT_64 R3 — VTT_65 P3 — VTT_66 N3 — VTT_67 M3 — VTT_68 R2 — VTT_69 P2 — VTT_70 M2 — VTT_71 D2 — VTT_72 AB1 — VTT_73 R1 — VTT_74 P1 — VTT_75 N1 — VTT_76 M1

VTTLF_CAP3 — C88 0.47UF/16V — GND

VTTLF_CAP2 — VTTLF_CAP1 — C89 0.47UF/16V — C90 0.22UF/6.3V — GND

PLACE IN CAVITY

C79 4.7UF/10V — C80 2.2UF/6.3V — GND

PLACE ON THE EDGE

800 mA +VCCP_AGTL+

C81 0.22UF/6.3V — CE8 330UF/2V — GND

post- R2.1: No 101 mount 150uF

Z62JM ER NO4 mount 330uF

+3VS — **VCCHV** ***40 mA***

C93 10UF/10V — C94 0.1UF/10V — GND

+3VS — D78 — R1027 10Ohm — BAT54C — +1.5VS

LVDS disabled

	SDVO disabled	SDVO enabled
VCCD_LVDS	GND	1.5V
VCCA_LVDS	GND	GND
VCCTX_LVDS	GND	GND

TV-OUT disabled

VCCD_TVDAC	1.5V
VCCD_QTVDAC	1.5V
VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	1.5V
VCCA_TVBG	1.5V
TV_IREF	1.5V
TCDACAOUT,TCDACBOUT, TCDACCOUT,	1.5V
TV_IRTNA,TV_IRTNB,TV_IRTNC	1.5V
VSSA_TVBG	GND

CRT disabled

VCCA_CRTDAC	VCCP_GMCH
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,YSHYC	GND
RED,RED#,GREEN,GREEN#, BLUE,BLUE#	VCCP_GMCH

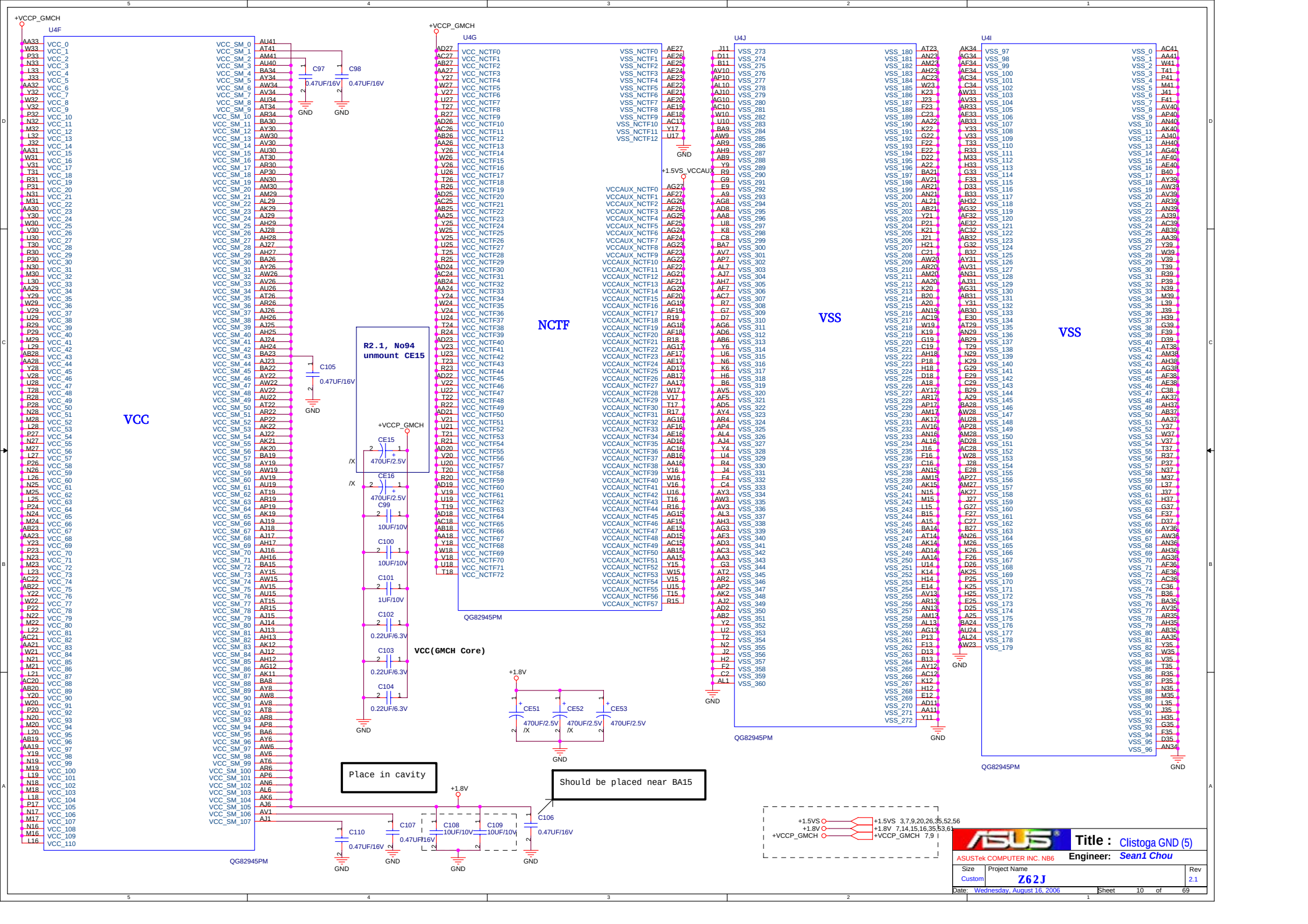
ASUSTek COMPUTER INC. NB6

Title : Calistoga Power (4)

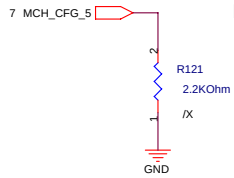
Engineer: *Sean1 Chou*

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 — Sheet 9 of 69

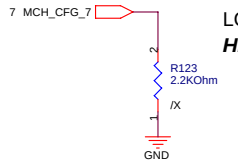

U4F
VCC
QG82945PM
U4G
NCTF
QG82945PM
U4J
VSS
QG82945PM
U4I
VSS
QG82945PM
+VCCP_GMCH
+1.5VS_VCCAUX
+1.8V
GND
R2.1, No94
unmount CE15
VCC(GMCH Core)
Place in cavity
Should be placed near BA15
+1.5VS 3,7,9,20,26,35,52,56
+1.8V 7,14,15,16,35,53,61
+VCCP_GMCH 7,9
Title : Clistoga GND (5)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 10 of 69

CFG5 : DMI X2 Select



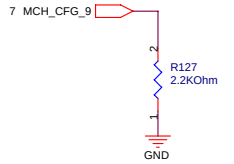
LOW = DMI X 2
HIGH = DMI X 4 (Default)

CFG7 : CPU STRAP



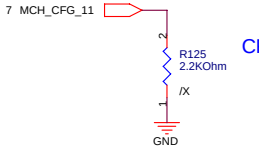
LOW = Reserved
HIGH = Mobility CPU (Default)

CFG9 : PCIE GRAPHIC LANE

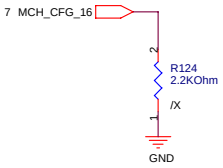


LOW = REVERSE LANES (Z62J default)
HIGH = NORMAL OPERATION

CFG11 : Reserved but need to be pull low

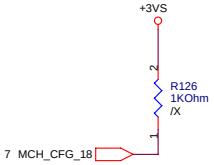


CFG16 : FSB DYNAMIC ODT



LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

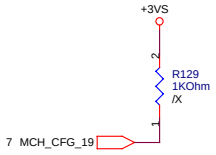
CFG18 : GMCH Core Voltage Level



LOW = 1.05V (Z62J default)
HIGH = 1.5V

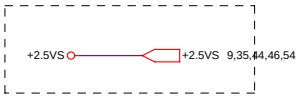
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG19 : DMI LANE REVERSAL



LOW = NORMAL
HIGH = LANES REVERSED

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



ASUSTek COMPUTER INC. NB6 **Engineer:** ***Sean1 Chou***

Title : Calistoga Strapping

Size	Project Name	Rev
Custom	Z62J	2.1

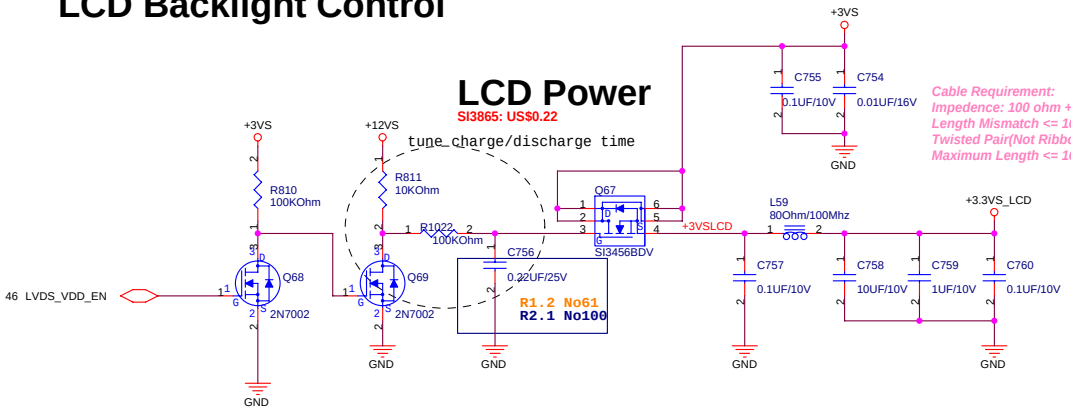
Date: Wednesday, August 16, 2006 Sheet 11 of 69

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

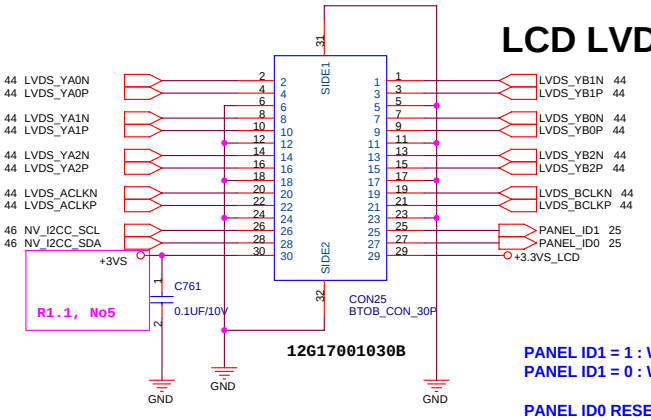
LCD Power

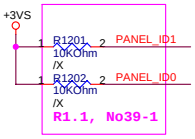
SI3865: US$0.22



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface





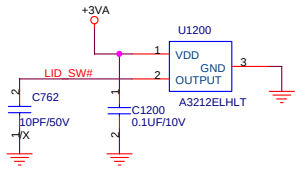
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

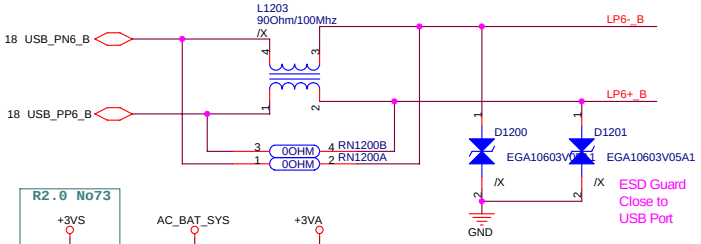
PANEL ID0 RESERVE FOR VENDOR

INVERTER Interface

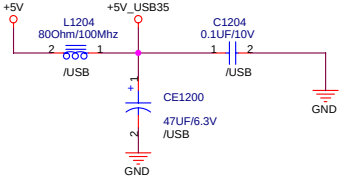
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

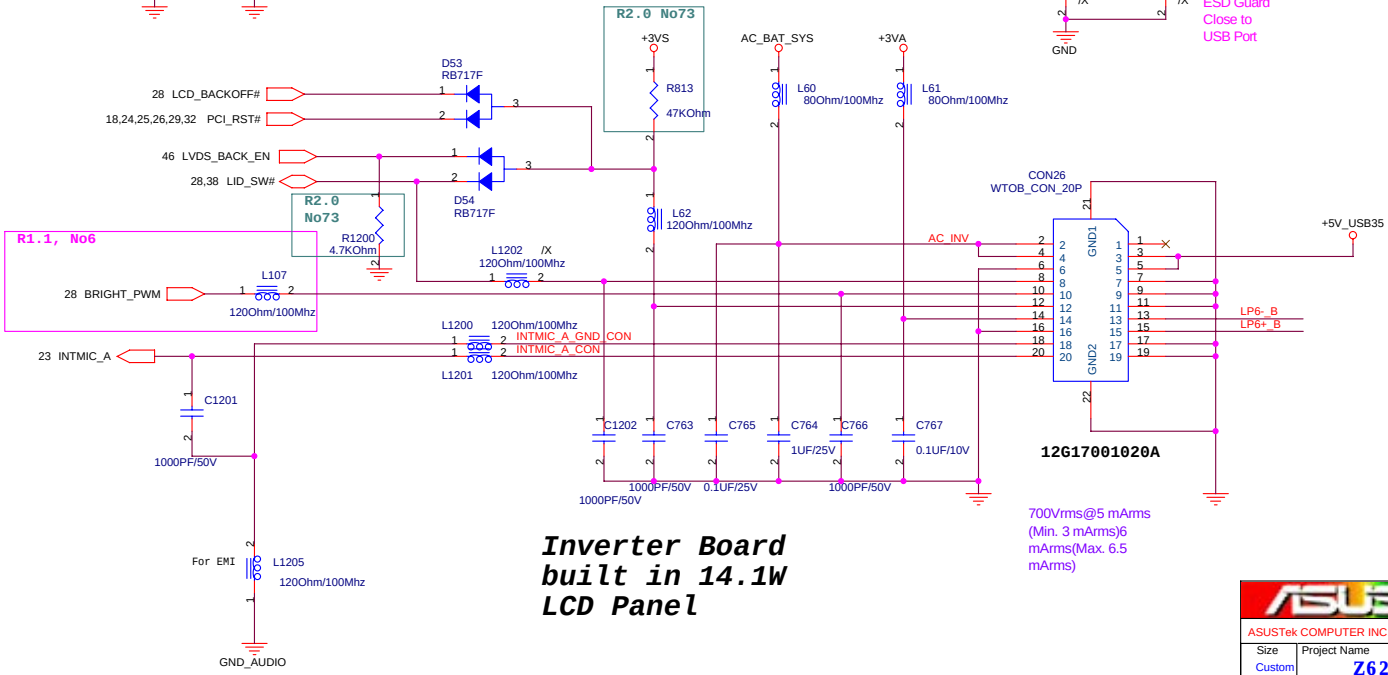
Magnatic Switch For LID_SW# On/OFF





ESD Guard Close to USB Port





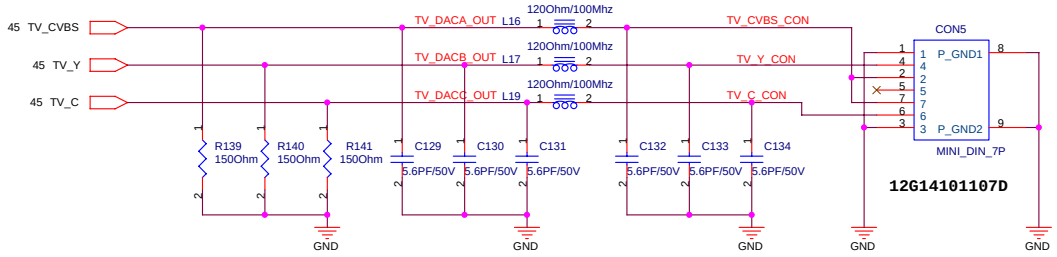
Inverter Board built in 14.1W LCD Panel

700Vrms@5 mArms
(Min. 3 mArms)6
mArms(Max. 6.5
mArms)

Title : LVDS & INVERTER		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 12 of 69	

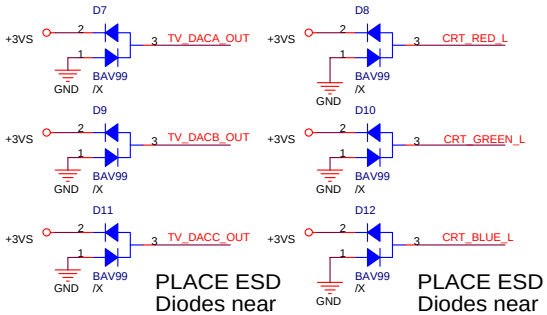
TV OUT

checklist suggests
150ohm/100MHz & 6pF



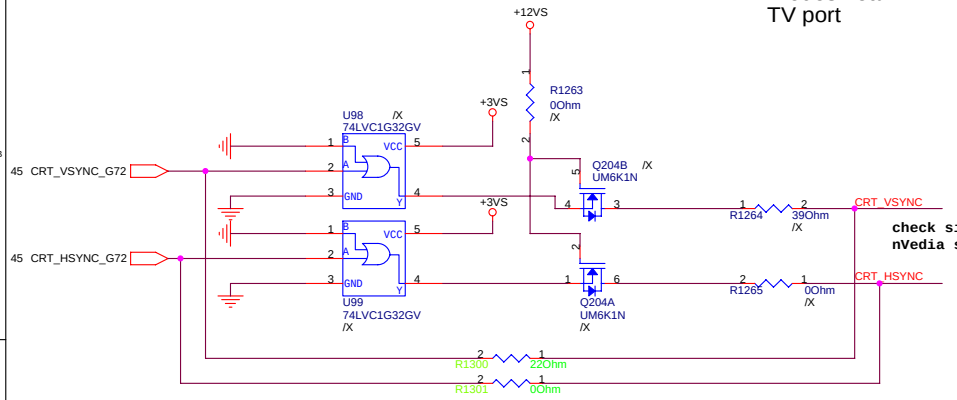
12G14101107D

Place Terminator
close to
Connector

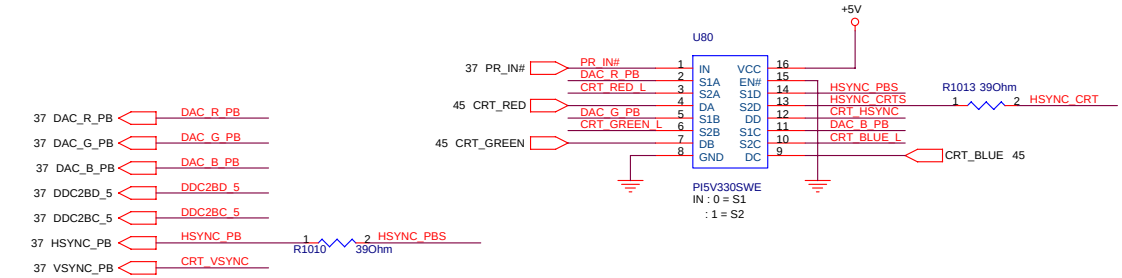


PLACE ESD
Diodes near
TV port

PLACE ESD
Diodes near
VGA port

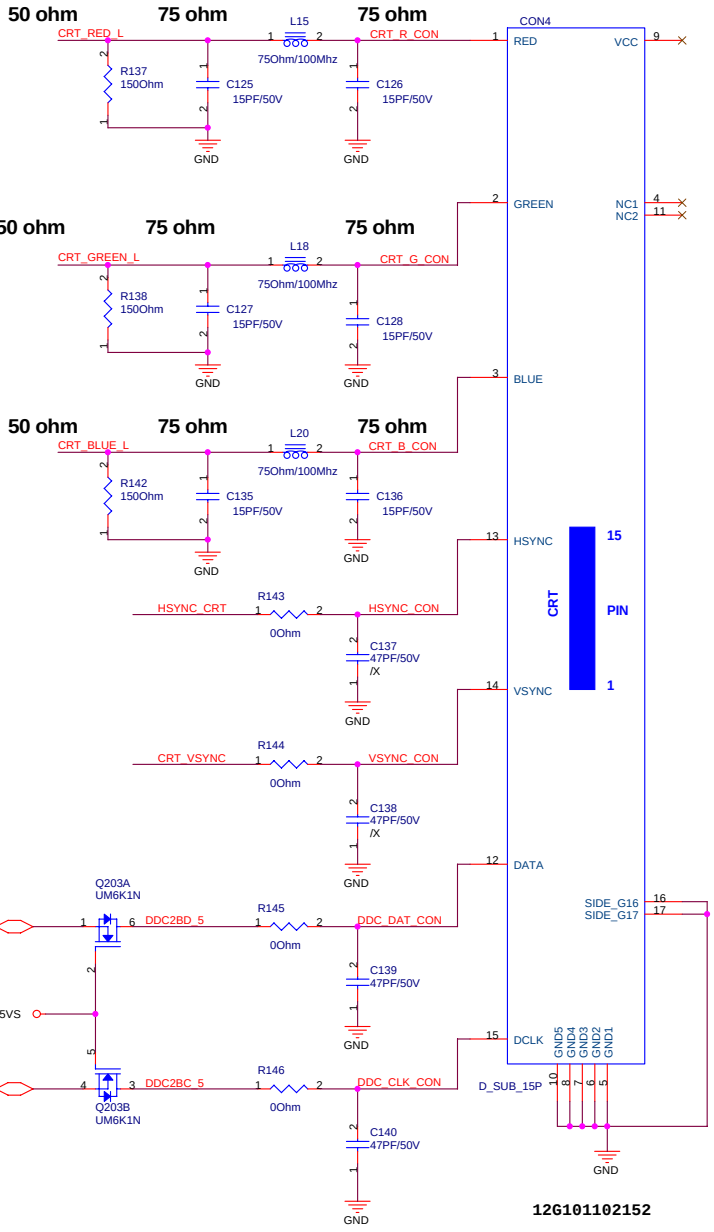


check signal integrity,
nVedia suggest 33ohm

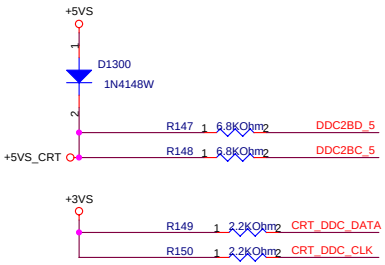


To PortBar III

checklist suggests 47ohm/100MHz



12G101102152



ASUSTek COMPUTER INC. NB6	Title : CRT & TV OUT		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 13 of 69		

NO STUFF *

M_CLK_DDR3

PLACE NEAR SO-DIMM_0

M_CLK_DDR#3

M_CLK_DDR2

PLACE NEAR SO-DIMM_0

M_CLK_DDR#2

8,16 M_B_A[0..13]

M_VREF_DIMM1 M_VREF_DIMM1 7,15,16
+1.8V 7,10,15,16,35,53,61
+3VS +3VS 4,5,7,9,11,12,13,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

M_B_DQ[0..63] 8

U5A

M_B_A0	102	A0	DQ0	5	M_B_DQ58
M_B_A1	101	A1	DQ1	7	M_B_DQ63
M_B_A2	100	A2	DQ2	17	M_B_DQ56
M_B_A3	99	A3	DQ3	19	M_B_DQ60
M_B_A4	98	A4	DQ4	4	M_B_DQ62
M_B_A5	97	A5	DQ5	6	M_B_DQ61
M_B_A6	94	A6	DQ6	14	M_B_DQ57
M_B_A7	92	A7	DQ7	16	M_B_DQ59
M_B_A8	93	A8	DQ8	23	M_B_DQ50
M_B_A9	91	A9	DQ9	25	M_B_DQ55
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ49
M_B_A11	90	A11	DQ11	37	M_B_DQ53
M_B_A12	89	A12	DQ12	20	M_B_DQ51
M_B_A13	116	A13	DQ13	22	M_B_DQ54
	86	A14	DQ14	36	M_B_DQ52
	84	A15	DQ15	38	M_B_DQ48
8,16 M_B_BS#2	85	A16_BA2	DQ16	43	M_B_DQ43
			DQ17	45	M_B_DQ41
8,16 M_B_BS#0	107	BA0	DQ18	55	M_B_DQ40
8,16 M_B_BS#1	106	BA1	DQ19	57	M_B_DQ46
7,16 M_CS#2	110	S0#	DQ20	44	M_B_DQ42
7,16 M_CS#3	115	S1#	DQ21	46	M_B_DQ47
7 M_CLK_DDR2	30	CK0	DQ22	56	M_B_DQ45
7 M_CLK_DDR#2	32	CK0#	DQ23	58	M_B_DQ44
7 M_CLK_DDR3	164	CK1	DQ24	61	M_B_DQ34
7 M_CLK_DDR#3	166	CK1#	DQ25	63	M_B_DQ38
7,16 M_CKE2	79	CKE0	DQ26	73	M_B_DQ32
7,16 M_CKE3	80	CKE1	DQ27	75	M_B_DQ36
8,16 M_B_CAS#	113	CAS#	DQ28	62	M_B_DQ35
8,16 M_B_RAS#	108	RAS#	DQ29	64	M_B_DQ39
8,16 M_B_WE#	109	WE#	DQ30	74	M_B_DQ37
	198	SA0	DQ31	76	M_B_DQ33
+3VS	200	SA1	DQ32	123	M_B_DQ27
5,15,19,24,26 SMB_CLK_S	197	SCL	DQ33	125	M_B_DQ30
5,15,19,24,26 SMB_DAT_S	195	SDA	DQ34	135	M_B_DQ28
			DQ35	137	M_B_DQ29
7,16 M_ODT2	114	ODT0	DQ36	124	M_B_DQ31
7,16 M_ODT3	119	ODT1	DQ37	126	M_B_DQ26
			DQ38	134	M_B_DQ25
M_B_DM7	10	DM0	DQ39	136	M_B_DQ24
M_B_DM6	26	DM1	DQ40	141	M_B_DQ18
M_B_DM5	52	DM2	DQ41	143	M_B_DQ19
M_B_DM4	67	DM3	DQ42	151	M_B_DQ20
M_B_DM3	130	DM4	DQ43	153	M_B_DQ16
M_B_DM2	147	DM5	DQ44	140	M_B_DQ22
M_B_DM1	170	DM6	DQ45	142	M_B_DQ23
M_B_DM0	185	DM7	DQ46	152	M_B_DQ21
			DQ47	154	M_B_DQ17
M_B_DQS7	13	DQS0	DQ48	157	M_B_DQ9
M_B_DQS6	31	DQS1	DQ49	159	M_B_DQ15
M_B_DQS5	51	DQS2	DQ50	173	M_B_DQ10
M_B_DQS4	70	DQS3	DQ51	175	M_B_DQ8
M_B_DQS3	131	DQS4	DQ52	158	M_B_DQ14
M_B_DQS2	148	DQS5	DQ53	160	M_B_DQ11
M_B_DQS1	169	DQS6	DQ54	174	M_B_DQ13
M_B_DQS0	188	DQS7	DQ55	176	M_B_DQ12
M_B_DQS#7	11	DQS#0	DQ56	179	M_B_DQ6
M_B_DQS#6	29	DQS#1	DQ57	181	M_B_DQ7
M_B_DQS#5	49	DQS#2	DQ58	189	M_B_DQ4
M_B_DQS#4	68	DQS#3	DQ59	191	M_B_DQ1
M_B_DQS#3	129	DQS#4	DQ60	180	M_B_DQ2
M_B_DQS#2	146	DQS#5	DQ61	182	M_B_DQ3
M_B_DQS#1	167	DQS#6	DQ62	192	M_B_DQ5
M_B_DQS#0	186	DQS#7	DQ63	194	M_B_DQ0

Group7 Group6 Group5 Group4 Group3 Group2 Group1 Group0

DDR_DIMM_200P_A

R1.1 No17

For Data Swap

12G025122007

8 M_B_DM[0..7]

8 M_B_DQS[0..7]

8 M_B_DQS#[0..7]

Layout Note: Place these High-Freq decoupling Caps near the GMCH

U5B

	112	VDD1	VSS16 18
	111	VDD2	VSS17 24
	117	VDD3	VSS18 41
	96	VDD4	VSS19 53
	95	VDD5	VSS20 42
	118	VDD6	VSS21 54
	81	VDD7	VSS22 59
	82	VDD8	VSS23 65
	87	VDD9	VSS24 60
	103	VDD10	VSS25 66
	88	VDD11	VSS26 127
	104	VDD12	VSS27 139
			VSS28 128
+3VS	199	VDDSPD	VSS29 145
			VSS30 165
	83	NC1	VSS31 171
	120	NC2	VSS32 172
	50	NC3	VSS33 177
	69	NC4	VSS34 187
	163	NCTEST	VSS35 178
			VSS36 190
M_VREF_DIMM1	1	VREF	VSS37 9
			VSS38 21
	201	GND0	VSS39 33
	202	GND1	VSS40 155
			VSS41 34
	203	NP_NC1	VSS42 132
	204	NP_NC2	VSS43 144
			VSS44 156
	47	VSS1	VSS45 168
	133	VSS2	VSS46 2
	183	VSS3	VSS47 3
	77	VSS4	VSS48 15
	12	VSS5	VSS49 27
	48	VSS6	VSS50 39
	184	VSS7	VSS51 149
	78	VSS8	VSS52 161
	71	VSS9	VSS53 28
	72	VSS10	VSS54 40
	121	VSS11	VSS55 138
	122	VSS12	VSS56 150
	196	VSS13	VSS57 162
	193	VSS14	
	8	VSS15	

DDR_DIMM_200P_A

12G025122007

C143 2.2UF/6.3V C144 0.1UF/10V C145 2.2UF/6.3V C146 0.1UF/10V

VREF -> 10/10 mils

Layout Note: Place these Caps near SO DIMM 1

Layout Note: Place these resistors near the GMCH

C151 0.1UF/10V C152 0.1UF/10V C153 0.1UF/10V C154 0.1UF/10V

Layout Note: Place these Caps near SO DIMM 1

C149 0.1UF/10V C150 0.1UF/10V C147 0.1UF/10V C148 0.1UF/10V

C155 2.2UF/6.3V C156 2.2UF/6.3V C157 2.2UF/6.3V C158 2.2UF/6.3V C159 2.2UF/6.3V

Title : DDR2_SO-DIMM(1)			
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 14 of 69		

8,16 M_A_A[0..13]

8 M_A_DM[0..7]

8 M_A_DQS[0..7]

8 M_A_DQS#[0..7]

M_A_DQ[0..63] 8

+1.8V +1.8V 7,10,14,16,35,53,61

+3VS +3VS 4,5,7,9,11,12,13,14,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

M_VREF_DIMM0 M_VREF_DIMM0 7,14,16

NO STUFF *

M_CLK_DDR0

PLACE NEAR SO-DIMM_1

M_CLK_DDR#0

M_CLK_DDR1

PLACE NEAR SO-DIMM_1

M_CLK_DDR#1

U8A

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
86 A14
84 A15
85 A16_BA2

8,16 M_A_BS#2

8,16 M_A_BS#0 107 BA0
8,16 M_A_BS#1 106 BA1
7,16 M_CS#0 110 S0#
7,16 M_CS#1 115 S1#
7 M_CLK_DDR1 30 CK0
7 M_CLK_DDR#1 32 CK0#
7 M_CLK_DDR0 164 CK1
7 M_CLK_DDR#0 166 CK1#
7,16 M_CKE0 79 CKE0
7,16 M_CKE1 80 CKE1
8,16 M_A_CAS# 113 CAS#
8,16 M_A_RAS# 108 RAS#
8,16 M_A_WE# 109 WE#
198 SA0
200 SA1
5,14,19,24,26 SMB_CLK_S 197 SCL
5,14,19,24,26 SMB_DAT_S 195 SDA

7,16 M_ODT0 114 ODT0
7,16 M_ODT1 119 ODT1

GND GND

R1.1 No17

M_A_DM7 10 DM0
M_A_DM6 26 DM1
M_A_DM5 52 DM2
M_A_DM4 67 DM3
M_A_DM3 130 DM4
M_A_DM2 147 DM5
M_A_DM1 170 DM6
M_A_DM0 185 DM7

M_A_DQS7 13 DQS0
M_A_DQS6 31 DQS1
M_A_DQS5 51 DQS2
M_A_DQS4 70 DQS3
M_A_DQS3 131 DQS4
M_A_DQS2 148 DQS5
M_A_DQS1 169 DQS6
M_A_DQS0 188 DQS7
M_A_DQS#7 11 DQS#0
M_A_DQS#6 29 DQS#1
M_A_DQS#5 49 DQS#2
M_A_DQS#4 68 DQS#3
M_A_DQS#3 129 DQS#4
M_A_DQS#2 146 DQS#5
M_A_DQS#1 167 DQS#6
M_A_DQS#0 186 DQS#7

DQ0 5 M_A_DQ63
DQ1 7 M_A_DQ59
DQ2 17 M_A_DQ57
DQ3 19 M_A_DQ60
DQ4 4 M_A_DQ58
DQ5 6 M_A_DQ62
DQ6 14 M_A_DQ61
DQ7 16 M_A_DQ56
DQ8 23 M_A_DQ55
DQ9 25 M_A_DQ51
DQ10 35 M_A_DQ52
DQ11 37 M_A_DQ53
DQ12 20 M_A_DQ54
DQ13 22 M_A_DQ50
DQ14 36 M_A_DQ49
DQ15 38 M_A_DQ48
DQ16 43 M_A_DQ43
DQ17 45 M_A_DQ41
DQ18 55 M_A_DQ42
DQ19 57 M_A_DQ40
DQ20 44 M_A_DQ46
DQ21 46 M_A_DQ47
DQ22 56 M_A_DQ44
DQ23 58 M_A_DQ45
DQ24 61 M_A_DQ32
DQ25 63 M_A_DQ35
DQ26 73 M_A_DQ36
DQ27 75 M_A_DQ37
DQ28 62 M_A_DQ39
DQ29 64 M_A_DQ38
DQ30 74 M_A_DQ33
DQ31 76 M_A_DQ34
DQ32 123 M_A_DQ31
DQ33 125 M_A_DQ26
DQ34 135 M_A_DQ24
DQ35 137 M_A_DQ25
DQ36 124 M_A_DQ27
DQ37 126 M_A_DQ30
DQ38 134 M_A_DQ29
DQ39 136 M_A_DQ28
DQ40 141 M_A_DQ22
DQ41 143 M_A_DQ19
DQ42 151 M_A_DQ21
DQ43 153 M_A_DQ20
DQ44 140 M_A_DQ18
DQ45 142 M_A_DQ23
DQ46 152 M_A_DQ16
DQ47 154 M_A_DQ17
DQ48 157 M_A_DQ11
DQ49 159 M_A_DQ9
DQ50 173 M_A_DQ14
DQ51 175 M_A_DQ8
DQ52 158 M_A_DQ10
DQ53 160 M_A_DQ15
DQ54 174 M_A_DQ12
DQ55 176 M_A_DQ13
DQ56 179 M_A_DQ2
DQ57 181 M_A_DQ3
DQ58 189 M_A_DQ5
DQ59 191 M_A_DQ1
DQ60 180 M_A_DQ7
DQ61 182 M_A_DQ6
DQ62 192 M_A_DQ4
DQ63 194 M_A_DQ0

Group7 Group6 Group5 Group4 Group3 Group2 Group1 Group0

DDR_DIMM_200P

For Data Swap

12G025C22000

U8B

+1.8V

+3VS

C209 2.2UF/6.3V
C210 0.1UF/10V
C211 2.2UF/6.3V
C212 0.1UF/10V

VREF -> 10/10 mils

M_VREF_DIMM0

GND

112 VDD1
111 VDD2
117 VDD3
96 VDD4
95 VDD5
118 VDD6
81 VDD7
82 VDD8
87 VDD9
103 VDD10
88 VDD11
104 VDD12
199 VDDSPD

83 NC1
120 NC2
50 NC3
69 NC4
163 NCTEST
1 VREF
201 GND0
202 GND1
203 NP_NC1
204 NP_NC2

47 VSS1
133 VSS2
183 VSS3
77 VSS4
12 VSS5
48 VSS6
184 VSS7
78 VSS8
71 VSS9
72 VSS10
121 VSS11
122 VSS12
196 VSS13
193 VSS14
8 VSS15

VSS16 18
VSS17 24
VSS18 41
VSS19 53
VSS20 42
VSS21 54
VSS22 59
VSS23 65
VSS24 60
VSS25 66
VSS26 127
VSS27 139
VSS28 128
VSS29 145
VSS30 165
VSS31 171
VSS32 172
VSS33 177
VSS34 187
VSS35 178
VSS36 190
VSS37 9
VSS38 21
VSS39 33
VSS40 155
VSS41 34
VSS42 132
VSS43 144
VSS44 156
VSS45 168
VSS46 2
VSS47 3
VSS48 15
VSS49 27
VSS50 39
VSS51 149
VSS52 161
VSS53 28
VSS54 40
VSS55 138
VSS56 150
VSS57 162

DDR_DIMM_200P

12G025C22000

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C213 0.1UF/10V
C214 0.1UF/10V
C215 0.1UF/10V
C216 0.1UF/10V

GND GND GND GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V

C217 2.2UF/6.3V
C218 2.2UF/6.3V
C219 2.2UF/6.3V
C220 2.2UF/6.3V
C221 2.2UF/6.3V

GND GND GND GND GND

GMCH=====>SODIMM1=>SODIMM0

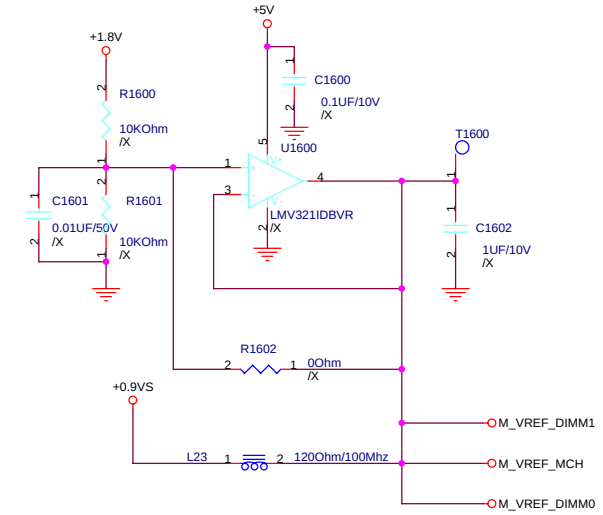
ASUSTek COMPUTER INC. NB6

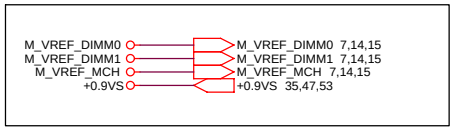
Title : DDR2 SO-DIMM(0)

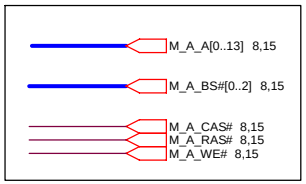
Engineer: Sean1 Chou

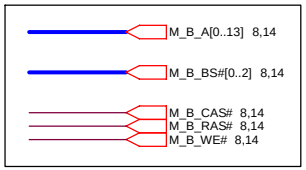
Size	Project Name	Rev
Custom	Z62J	2.1

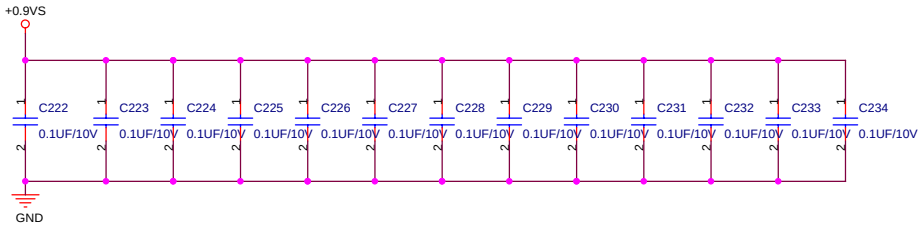
Date: Wednesday, August 16, 2006 Sheet 15 of 69



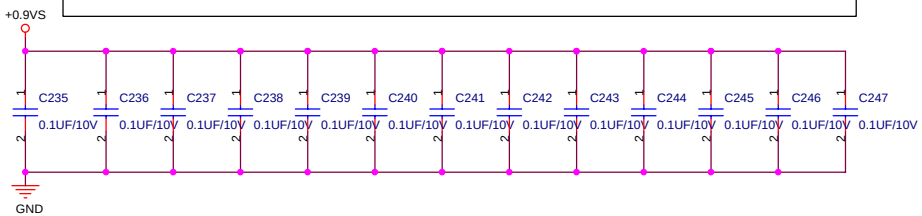


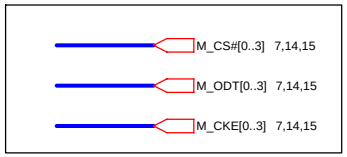


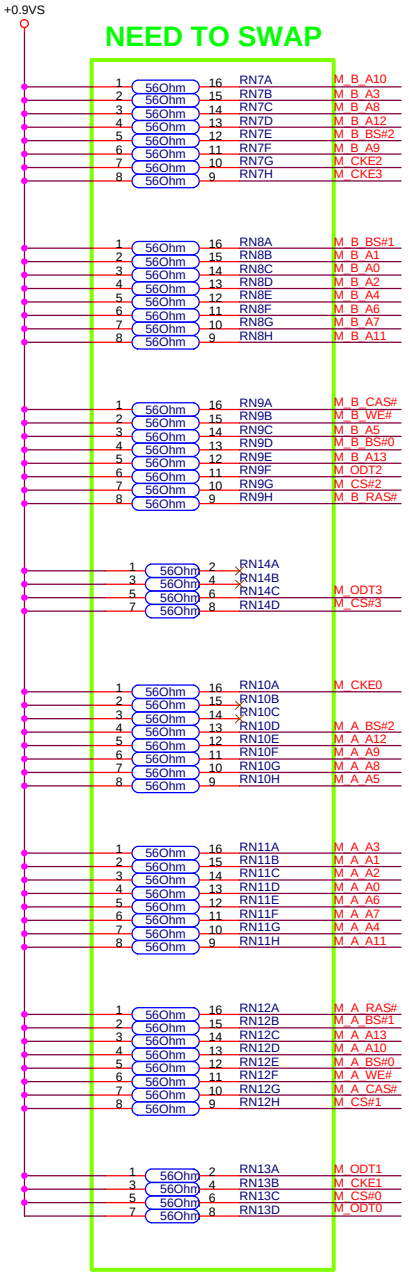




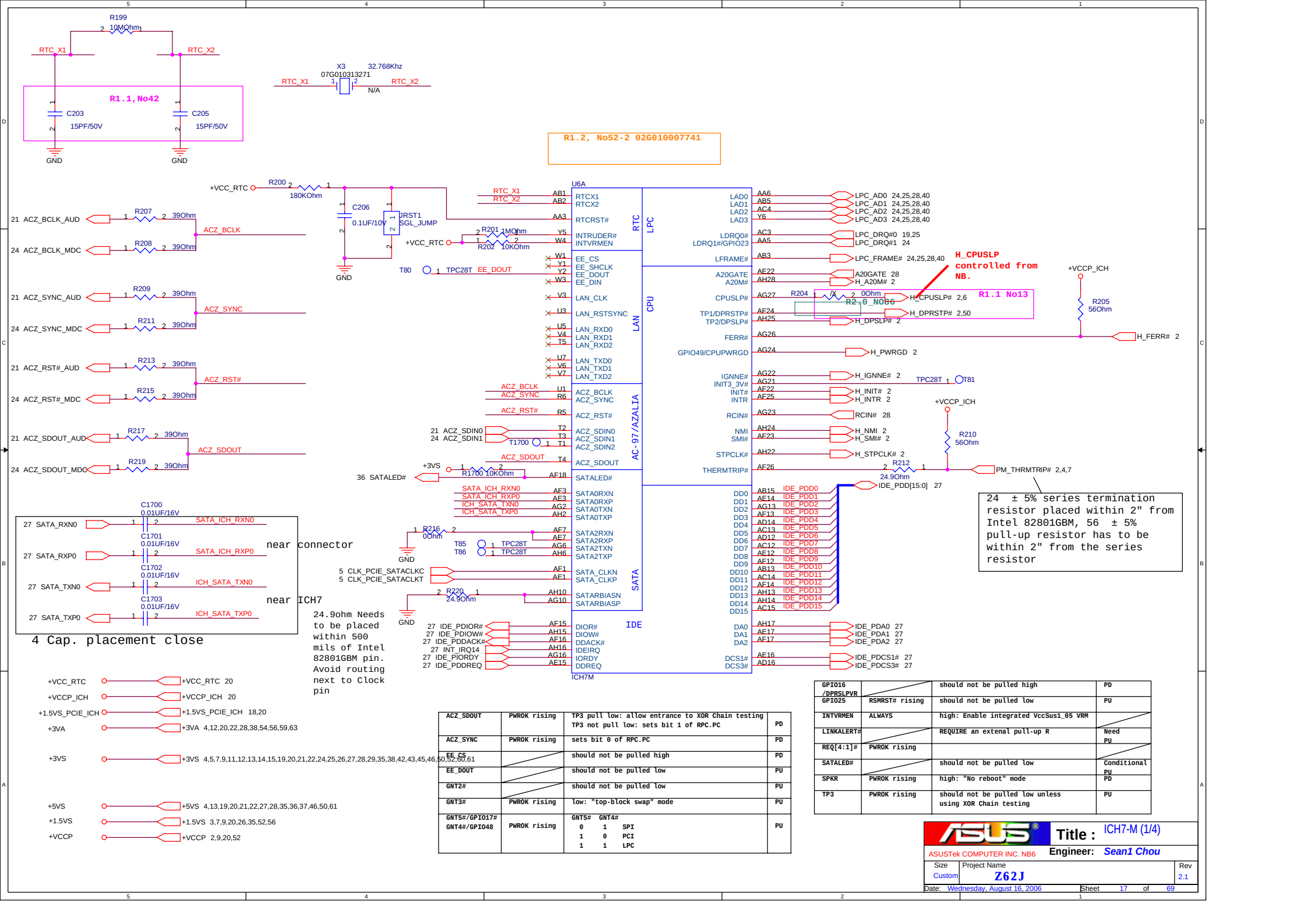
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS







ASUSTek COMPUTER INC. NB6	Title : DDR2 TERM	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 16 of 69	



ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUSTek COMPUTER INC. NB6

Title : ICH7-M (1/4)

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 17 of 69

DEVICE	IDSEL	REQ/GNT	INT
LAN	AD23	REQ2#/GNT2#	INT A#
CARDBUS	AD17	REQ1#/GNT1#	INT B#, INT C#, INT D#

Internal					
SM Bus	INTB#	EIP	INTA#	PCIE6	INTB#
SATA	INTB#	U3P	INTD#	PCIE5	INTA#
PATA	INTA#	U2P	INTC#	PCIE4	INTD#
AC97 Modem	INTB#	U1P	INTB#	PCIE3	INTC#
		U0P	INTA#	PCIE2	INTB#
AC97 Audio	INTA#	HD Audio	INTA#	PCIE1	INTA#

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

Do not connect to reset on PCI slots or PCI down devices.

Pull-ups must be placed within 500 mils from Intel 82801GBM pins

ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 18 of 69		

Title : ICH7-M (2/4)

GPIO:
[0,6,7,16:23,32:39,48] - 3.3V core,
[1:5] - 5V core,
[8:15,24:31] - 3.3V resume,
[40:47] - N/A
[49] - V_CPU_IO

0 needs to check power plane again

For PCI compliance, SMBus signals should be routed to either all or none of the PCI slots in a chassis.
These signals should not be connected to SMLINK

U6C

SMB_CLK C22 SMBCLK
SMB_DAT B22 SMBDATA
LINKALERT# A26 LINKALERT#
SM_LINK0 B25 SMLINK0
SM_LINK1 A25 SMLINK1
SMB

RING# A28 RI#

SPKR A19 SPKR
SUS_STAT# A27 SUS_STAT#
A22 SYS_RST#

7 PM_BMBUSY# AB18 GPIO0/BM_BUSY#

R157 1 2 10KOhm B23 SMBALERT#/GPIO11

5 STP_PCI# AC20 GPIO18/STPPCI#
5,50 STP_CPU# AF21 GPIO20/STPCPU#

PCB_ID2 A21 GPIO26

36 BT_LED_EN# B21 GPIO27
T42 1 TPC28T E23 GPIO28

24,29,32 PM_CLKRUN# AG18 GPIO32/CLKRUN#

26 BT_ON AC19 GPIO33/AZ_DOCK_EN#
26 WLAN_ON# U2 GPIO34/AZ_DOCK_RST#

+3VSUS 1 R1903 2 1KOhm

26 SB_WAKE# F20 WAKE#
24,25,28,29 INT_SERIRQ AH21 SERIRQ
28 PM_THERM# AE20 THERM#

38,50,60 IMVPOK AD22 VRMPWRGD
R2.0_NO86
T46 TPC28T

RF_OFF_SW# AC21
AC18
28 EXTSMI# E21
GPIO6
GPIO7
GPIO8

ICH7M

SYS GPIO

Clocks

CLK14 AC1 CLK14
CLK48 B2 CLK48
SUSCLK C20 SUSCLK

SLP_S3# B24 SLP_S3#
SLP_S4# D23 SLP_S4#
SLP_S5# F22 SLP_S5#
PWROK AA4 PWROK
GPIO16/DPRSLPVR AC22 GPIO16/DPRSLPVR
TP0/BATLOW# C21 TP0/BATLOW#
PWRBTN# C23 PWRBTN#

Power MGT

LAN_RST# C19 LAN_RST#
RSMRST# Y4 RSMRST#

GPIO9 E20
GPIO10 A20
GPIO12 F19
GPIO13 E19
GPIO14 R4
GPIO15 F22
GPIO24 R3
GPIO25 D20
GPIO35 AD21
GPIO38 AD20
GPIO39 AE20

SATA GPIO

GPIO21/SATA0GP AE19
GPIO19/SATA1GP AH18
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19

GPIO

AE19 2 R154 100Ohm GND TPC28T T41
AH19 2 R155 100Ohm GND TPC28T T38

CLK_ICH14 5
CLK_USB48 5
C193 10PF/50V /X

SUS_CLK 24
PM_SUSB# 28,32
PM_SUSC# 28
TPC28T T40
GND

ICH7_PWROK 7,28
R158 10KOhm
GND

PM_DPRSLPVR 7,50
PM_BATLOW#
PM_PWRBTN# 28

PLT_RST# 7,18,27,28,42

PM_RSMRST# 28

SATA_DET#0
R1904 1 0Ohm /X
NV_THERM# 46
R159 10KOhm
GND

KB_SCI# 28
SIO_SMI# 25
PWRLED_1HZ
T1900
TPC28T

TPC28T T44
802_LED_EN# 36
CB_SD# 29

TPC28T T47
PCB_ID0
PCB_ID1

If ICH7M embedded Lan controller was used, "LAN_RST#" should be connected to "RSMRST#"

GPIO 10 - Default GPI, 3.3V Resume

18,29,32 PCI_FRAME# RP1A 1 8.2KOHM 10
18,29,32 PCI_IRDY# RP1B 2 8.2KOHM 10
18,29,32 PCI_TRDY# RP1C 3 8.2KOHM 10
18,29,32 PCI_STOP# RP1D 4 8.2KOHM 10
18,29,32 PCI_SERR# RP1E 6 8.2KOHM 10
18,29,32 PCI_DEVSEL# RP1F 7 8.2KOHM 10
18,29,32 PCI_PERR# RP1G 8 8.2KOHM 10
18 PCI_LOCK# RP1H 9 8.2KOHM 10

18,32 PCI_INTA# RP2A 1 8.2KOHM 10
18,29 PCI_INTB# RP2B 2 8.2KOHM 10
18,29 PCI_INTC# RP2C 3 8.2KOHM 10
18,29 PCI_INTD# RP2D 4 8.2KOHM 10
18 PCI_INTE# RP2E 6 8.2KOHM 10
18 PCI_INTF# RP2F 7 8.2KOHM 10
18 PCI_INTG# RP2G 8 8.2KOHM 10
18 PCI_INTH# RP2H 9 8.2KOHM 10

18 PCI_REQ#0 RP3A 1 8.2KOHM 10
18,29 PCI_REQ#1 RP3B 2 8.2KOHM 10
18,32 PCI_REQ#2 RP3C 3 8.2KOHM 10
18 PCI_REQ#3 RP3D 4 8.2KOHM 10
18 PCI_REQ#5 RP3E 6 8.2KOHM 10
18 PCI_REQ#4 RP3F 7 8.2KOHM 10
PM_CLKRUN# RP3G 8 8.2KOHM 10
PM_THERM# RP3H 9 8.2KOHM 10

INT_SERIRQ R163 10KOhm
STP_PCI# R164 10KOhm /X
STP_CPU# R167 10KOhm /X
17,25 LPC_DRQ#0 R170 8.2KOhm /X
SMB_CLK_S R172 2.2KOhm
SMB_DAT_S R174 2.2KOhm

+5VS
5,14,15,24,26 SMB_CLK_S
Q16 2N7002
SMB_CLK

+5VS
5,14,15,24,26 SMB_DAT_S
Q17 2N7002
SMB_DAT

+5VS
ICH7_PWROK
Q15 2N7002 /X
VRMPWRGD
R161 10KOhm /X
GND

+3VS
RF_OFF_SW# R165 8.2KOhm

PM_BATLOW# D16 1N4148W BAT_LL# 28

checklist suggests +3V
+3VSUS
RING# R162 8.2KOhm
RN4A 10KOhm
SM_LINK1 RN4B 10KOhm
LINKALERT# RN4C 10KOhm
SM_LINK0 RN4D 10KOhm
SMB_CLK R166 2.2KOhm
SMB_DAT R169 2.2KOhm
PM_BATLOW# R171 8.2KOhm
SUS_STAT# R173 4.7KOhm /X
18,32 PME# R176 10KOhm /X

checklist suggests +3V
R1.2, No49
21 SPKR_SB
24 SUS_STAT#
R156 1 2 10KOhm
+3V
+3VSUS
R157 1 2 10KOhm

PCB_VID3 : PROJECT CODE

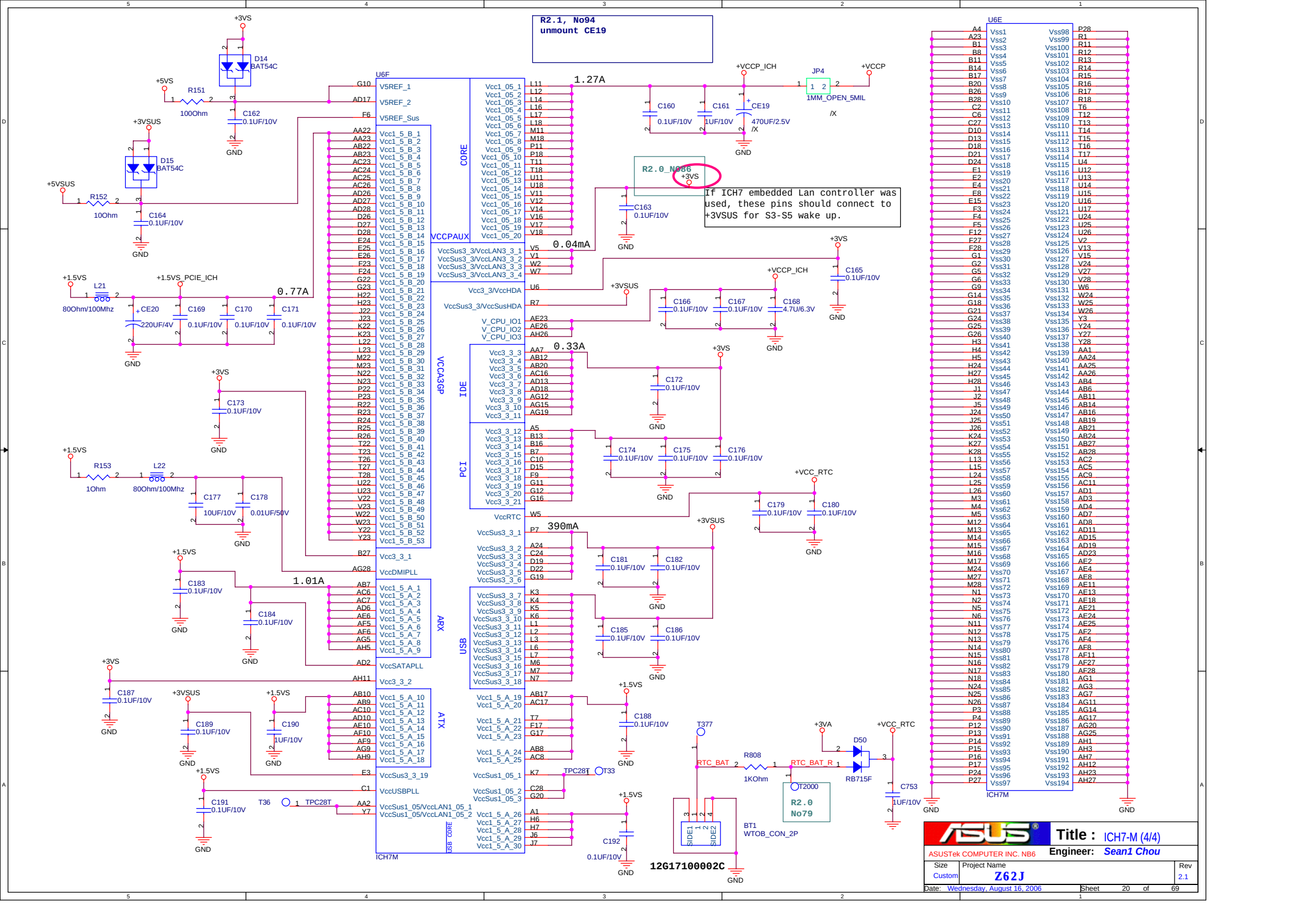
PCB_VID	0	1	2
MB V1.0	0	0	0
MB V1.1	0	0	1

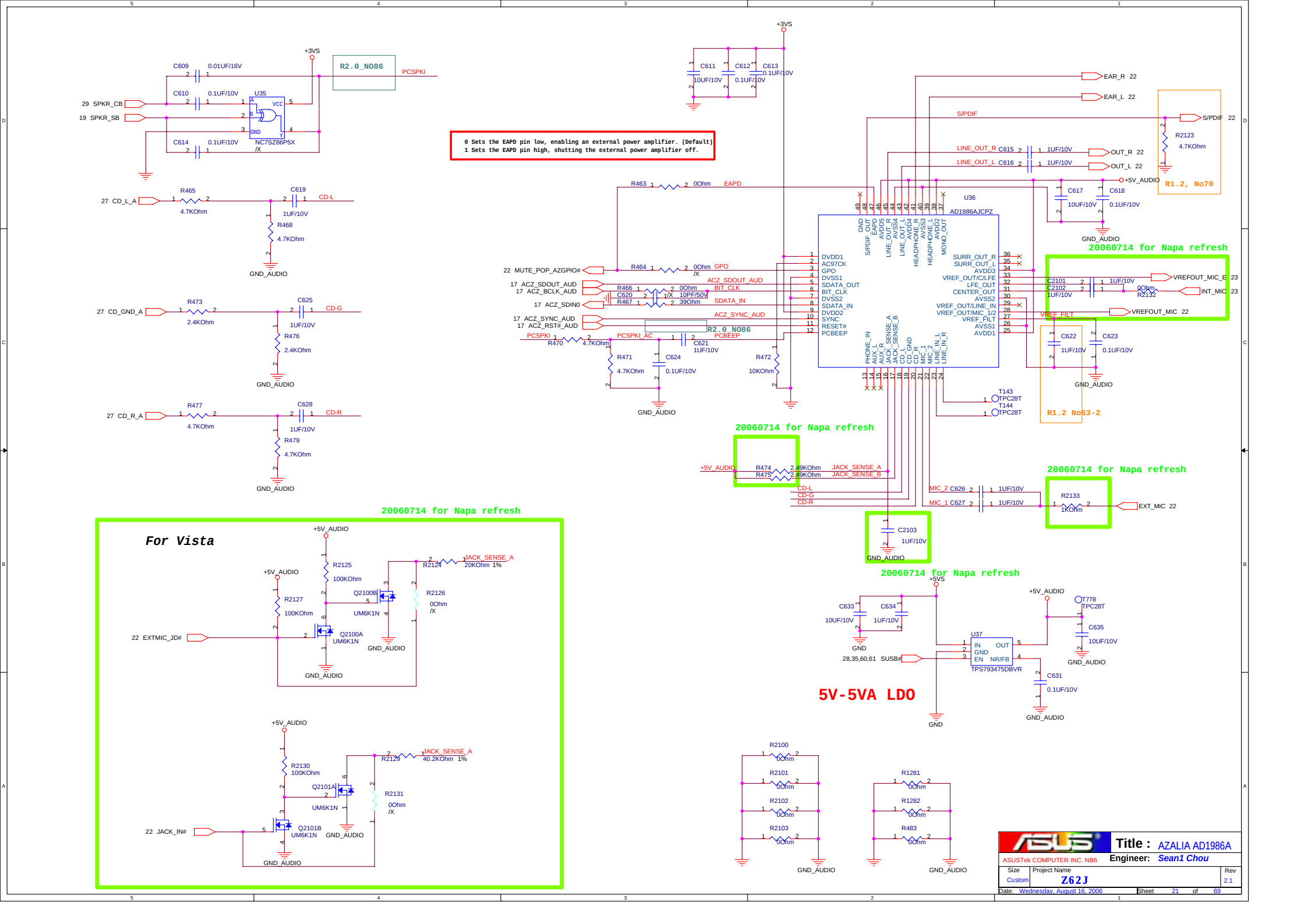
+3VSUS +3VSUS +3VSUS
R182 8.2KOhm /X
R183 8.2KOhm /X
R184 8.2KOhm
PCB_ID0
PCB_ID1
PCB_ID2
R190 8.2KOhm
R191 8.2KOhm
R192 8.2KOhm /X
GND
R1.1,No41

internal pull up
+3VSUS
SATA_DET#0 R175 8.2KOhm
KB_SCI# R177 10KOhm
SIO_SMI# R179 8.2KOhm
802_LED_EN# R180 8.2KOhm
CB_SD# R181 8.2KOhm /X
BT_LED_EN# R185 8.2KOhm
BT_ON R187 8.2KOhm
WLAN_ON# R189 8.2KOhm
GND

internal pull down
PM_DPRSLPVR R186 100KOhm /X
PM_RSMRST# R188 10KOhm
GND

ASUSTek COMPUTER INC. NB6
Title : ICH7-M (3/4)
Engineer: Sean1 Chou
Size: Custom
Project Name: Z62J
Rev: 2.1
Date: Wednesday, August 16, 2006
Sheet 19 of 69


R2.1, No94
unmount CE19
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
R2.0 No86
U6F
ICH7M
U6E
ICH7M
1.27A
0.04mA
0.33A
390mA
1.01A
0.77A
CORE
VCCPAUX
IDE
PCI
USB
ARX
ATX
VCCA3GP
USB CORE
D14 BAT54C
D15 BAT54C
R151 100Ohm
R152 10Ohm
R153 1Ohm
L21 80Ohm/100Mhz
L22 80Ohm/100Mhz
JP4 1MM_OPEN_5MIL
D50 RB715F
R808 1KOhm
BT1 WTOB_CON_2P
12G17100002C
Title : ICH7-M (4/4)
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 20 of 69


+3VS
C609 0.01UF/16V
C610 0.1UF/10V
C614 0.1UF/10V
U35
NC7SZ86P5X
/X
R2.0_NO86
PCSPKI
29 SPKR_CB
19 SPKR_SB
27 CD_L_A
R465 4.7KOhm
C619 1UF/10V
CD-L
R468 4.7KOhm
GND_AUDIO
27 CD_GND_A
R473 2.4KOhm
C625 1UF/10V
CD-G
R476 2.4KOhm
27 CD_R_A
R477 4.7KOhm
C628 1UF/10V
CD-R
R479 4.7KOhm
C611 10UF/10V
C612 0.1UF/10V
C613 0.1UF/10V
0 Sets the EAPD pin low, enabling an external power amplifier. (Default)
1 Sets the EAPD pin high, shutting the external power amplifier off.
R463 0Ohm EAPD
22 MUTE_POP_AZGPIO#
R464 0Ohm GPO
/X
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
R466 0Ohm
C620 10PF/50V
R467 39Ohm
BIT_CLK
17 ACZ_SDIN0
SDATA_IN
17 ACZ_SYNC_AUD
17 ACZ_RST#_AUD
ACZ_SYNC_AUD
R2.0_NO86
PCSPKI
R470 4.7KOhm
PCSPKI_AC
C621 1UF/10V
PCBEEP
R471 4.7KOhm
C624 0.1UF/10V
R472 10KOhm
U36
AD1986AJCPZ
DVDD1
AC97CK
GPO
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PCBEEP
GND
S/PDIF_OUT
EAPD
AVDD5
AUX_R
AVSS4
LINE_OUT_L
AVDD4
HEADPHONE_R
AVSS3
HEADPHONE_L
AVDD2
MONO_OUT
SURR_OUT_R
SURR_OUT_L
AVDD3
VREF_OUT/C/LFE
LFE_OUT
CENTER_OUT
AVSS2
VREF_OUT/LINE_IN
VREF_OUT/MIC_1/2
VREF_FILT
AVSS1
AVDD1
PHONE_IN
AUX_L
AUX_R
JACK_SENSE_A
JACK_SENSE_B
CD_L
CD_GND
CD_R
MIC_1
MIC_2
LINE_IN_L
LINE_IN_R
EAR_R 22
EAR_L 22
S/PDIF
S/PDIF 22
R2123 4.7KOhm
LINE_OUT_R C615 1UF/10V
LINE_OUT_L C616 1UF/10V
OUT_R 22
OUT_L 22
+5V_AUDIO
C617 10UF/10V
C618 0.1UF/10V
GND_AUDIO
R1.2, No70
20060714 for Napa refresh
C2101 1UF/10V
C2102 1UF/10V
0Ohm
R2132
VREFOUT_MIC_E 23
INT_MIC 23
VREFOUT_MIC 22
VREF_FILT
C622 1UF/10V
C623 0.1UF/10V
R1.2 No53-2
T143 TPC28T
T144 TPC28T
20060714 for Napa refresh
+5V_AUDIO
R474 2.49KOhm
R475 2.49KOhm
JACK_SENSE_A
JACK_SENSE_B
CD-L
CD-G
CD-R
MIC_2 C626 1UF/10V
MIC_1 C627 1UF/10V
R2133 1KOhm
EXT_MIC 22
20060714 for Napa refresh
C2103 1UF/10V
GND_AUDIO
20060714 for Napa refresh
+5VS
C633 10UF/10V
C634 1UF/10V
GND
28,35,60,61 SUSB#
U37
IN
GND
EN
OUT
NR/FB
TPS793475DBVR
+5V_AUDIO
T778 TPC28T
C635 10UF/10V
C631 0.1UF/10V
GND_AUDIO
5V-5VA LDO
20060714 for Napa refresh
For Vista
+5V_AUDIO
R2125 100KOhm
R2127 100KOhm
Q2100B UM6K1N
Q2100A UM6K1N
R2126 0Ohm /X
R2124 20KOhm 1%
JACK_SENSE_A
22 EXTMIC_JD#
GND_AUDIO
R2130 100KOhm
Q2101A UM6K1N
Q2101B UM6K1N
R2131 0Ohm /X
R2129 40.2KOhm 1%
22 JACK_IN#
R2100 0Ohm
R2101 0Ohm
R2102 0Ohm
R2103 0Ohm
R1281 0Ohm
R1282 0Ohm
R483 0Ohm
ASUSTek COMPUTER INC. NB6
Title : AZALIA AD1986A
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 21 of 69

SPEAKER CONN.

R1.1 No44
CHANGE P/N

SPKR+_MB_A — L31 220Ohm — SPKR+_MB_CON_A
SPKR-_MB_A — L32 220Ohm — SPKR-_MB_CON_A
SPKL+_MB_A — L33 220Ohm — SPKL+_MB_CON_A
SPKL-_MB_A — L34 220Ohm — SPKL-_MB_CON_A

U12 WtoB_CON_4P

C2201 150PF/50V /X
C2202 150PF/50V /X
C2203 150PF/50V /X
C2204 150PF/50V /X

R1.1 No37

12G171000047

SPEAKER is 4 ohm +- 15% / 2W /79 +- 3db (美星電子)
P/N:04-170003610

HEADPHONE JACK

21 EAR_L
21 EAR_R
21 JACK_IN#

+5VS
+VAMP
C307 0.1UF/10V
R269 10KOhm
R1266 0Ohm
C1074 100PF/50V /X
S/PDIF 21
J1
EAR_L_O — R1257 22Ohm
EAR_R_O — R1258 22Ohm
No2.1, No96
C305 100PF/50V
C306 100PF/50V
PHONE_JACK_8P

12G140001089

AUDIO OUT AMP

R1.2, No53

GAIN0	GAIN1	SE/BTL#	AV (V/V)
0	0	0	-2
0	1	0	-6
1	0	0	-12
1	1	0	-24
X	X	1	-1

+VAMP
R261 10KOhm
R263 0Ohm /X
R2201 10KOhm /X
R2202 0Ohm
GND_AUDIO

+5VS
C297 10UF/10V
C298 0.1UF/10V
+VAMP
C299 1UF/10V
Close to OP
GND_AUDIO

U13 TPA0212PWPRG4
GAIN0_MB
GAIN1_MB
SPKL+_MB_A
SPKL-_MB_A
SPKR+_MB_A
SPKR-_MB_A
SE/BTL#
OP_SD#
R262 0Ohm
R264 0Ohm
R266 30KOhm R2.0, No81
R265 30KOhm R2.0, No81
21 OUT_L
OUT_R 21
C301 1UF/10V
C300 1UF/10V
C302 0.47UF/16V
C303 0.47UF/16V
C304 0.47UF/16V

Vista UAA driver will set this pin low as default, so it needs inverted.

Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.

21 MUTE_POP_AZGPIO#
Q2200 2N7002
MUTE_POP
DLY_OP_SD#
D23 1N4148W
GND
Z62JM ER NO1

+12VS
+5V
+3VS
R270 1MOhm
D2200 1N4148W
R271 470KOhm
R272 10KOhm
AMP_RST#
Q20B UM6K1N
Q20A UM6K1N
C2205 0.1UF/25V
Q19A UM6K1N
Q19B UM6K1N
Q21A UM6K1N
Q21B UM6K1N
EAR_R
EAR_L
EAR_R_C
EAR_L_C
Z62JM ER NO2
Solve pop noise

But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.

+VAMP
R1257 10KOhm
SE/BTL#
Q22A UM6K1N
Q22B UM6K1N
JACK_IN#
C2206 2.2UF/6.3V
GND_AUDIO
Z62JM ER NO5

R1.1 No31

Colay:
330 uF for Vista

20060714 for Napa refresh

CE7000 330UF/6.3V
CE21 47UF/6.3V /X
CE22 47UF/6.3V /X
CE7001 330UF/6.3V
RN16A 1KOhm
RN16B 1KOhm

$$f(highpass) = \frac{1}{2*3.14*R*C} = 73$$

R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.

+3VA
28 OP_SD#
D24 1N4148W
R275 10MOhm
R276 10KOhm
C308 0.1UF/10V
U82A
U82B
SN74LV14APWR
DLY_OP_SD 4
DLY_OP_SD#

20060714 for Napa refresh

VREFOUT_MIC 21
21 EXT_MIC
21 EXTMIC_JD#
R2203 3KOhm
L7000 220Ohm
L35 1KOhm/100Mhz
J2 AUDIO JACK PHONE_JACK_6P
C2200 100PF/50V
D7000 EGA10603V05A1 /X
D7001 EGA10603V05A1 /X
C7370 1000PF/50V /X

12G14030106L
PIN2 and PIN6 normal close
PIN4 and PIN5 normal open

External Microphone

ASUSTek COMPUTER INC. NB6

Title : AUDIO AMP
Engineer: Sean1 Chou

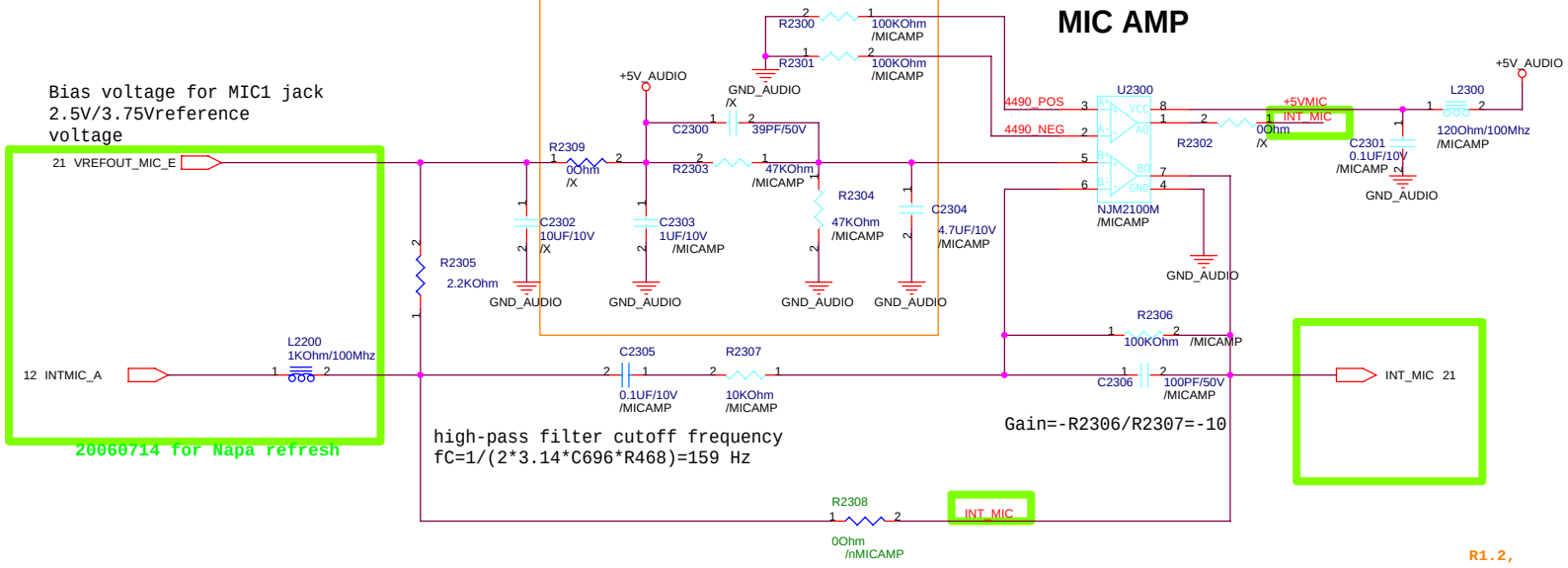
Size	Project Name	Rev
C	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 22 of 69

R1.2, No63

ADI suggests:
1. No install C2300
2. No install C2302
3. Ground bottom of R2304
4. Change R2303, R2304 to 47K. Change C2304 to 4.7uF
5. C2305 should be 0.1uF
6. Suggest using 100pF for C2306

MIC AMP

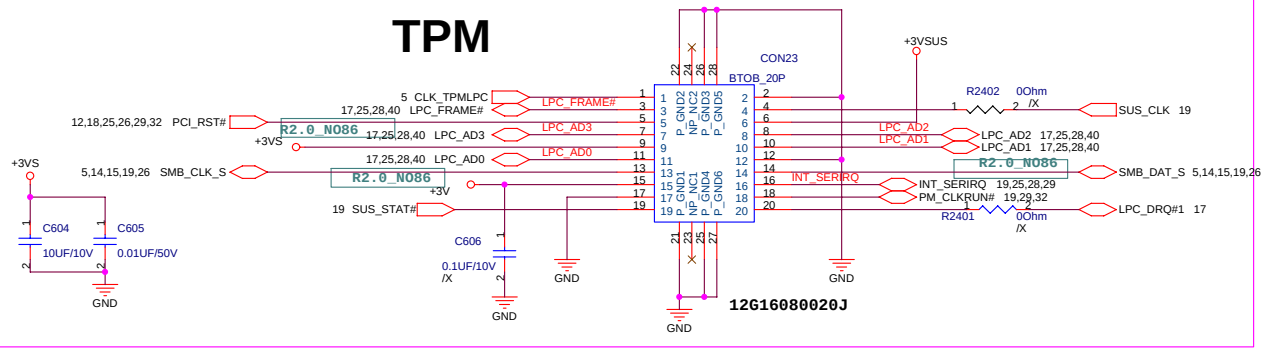


ASUSTek COMPUTER INC. NB6		Title : MIC Pre-AMP	
		Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006		Sheet 23 of 69	

TPM V1.2 Rev0.8

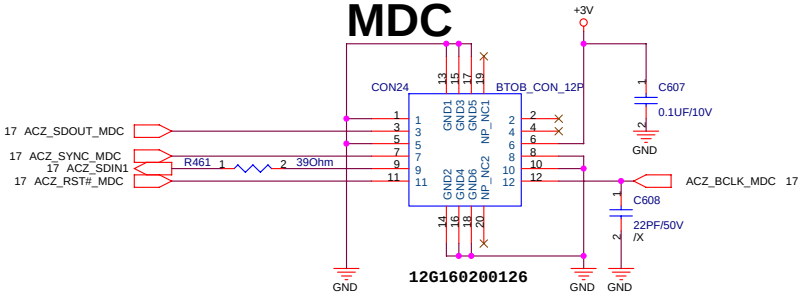
R1.1 No23

TPM



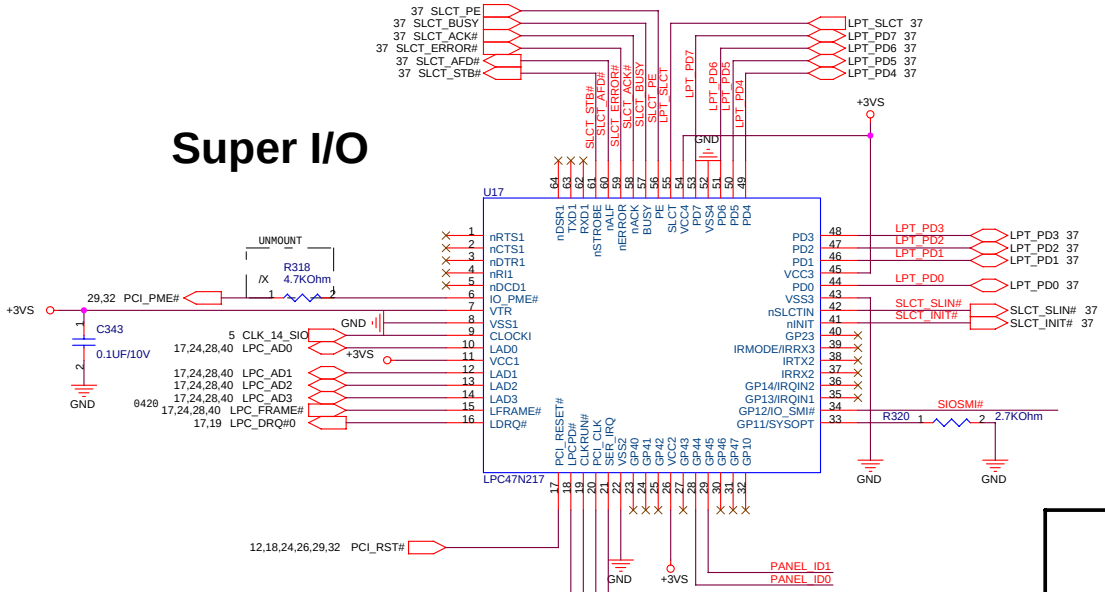
LPC CLK	Pin # 1	Pin # 2	GND
LPC_FRAME#	3	4	NC
RESET#	5	6	NC
LPC_AD3	7	8	LPC_AD2
+3VS	9	10	LPC_AD1
LPC_AD0	11	12	GND
NC	13	14	NC
+3V	15	16	SERIRQ
GND	17	18	CLKRUN#
LPC_PD#	19	20	NC

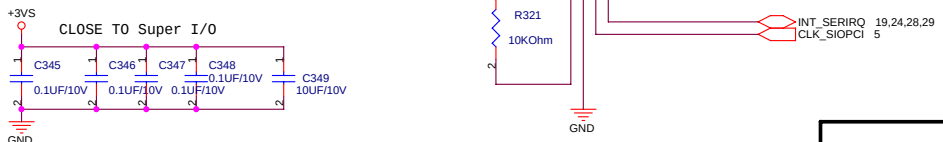
MDC

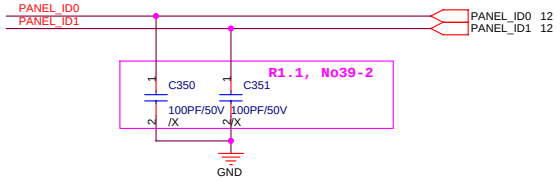


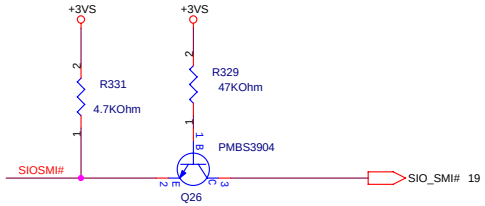
ASUSTek COMPUTER INC. NB6	Title : MODULE-TPM/MDC		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 24 of 69		

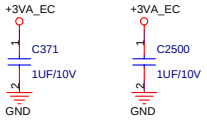
Super I/O







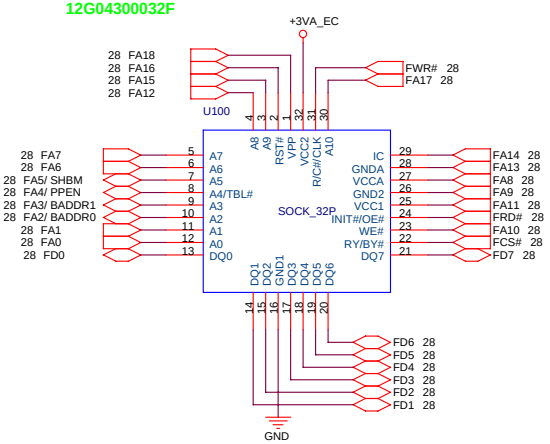




SST-PLCC32 4Mbits Flash ROM
PN:05G001014110(+3.3V)

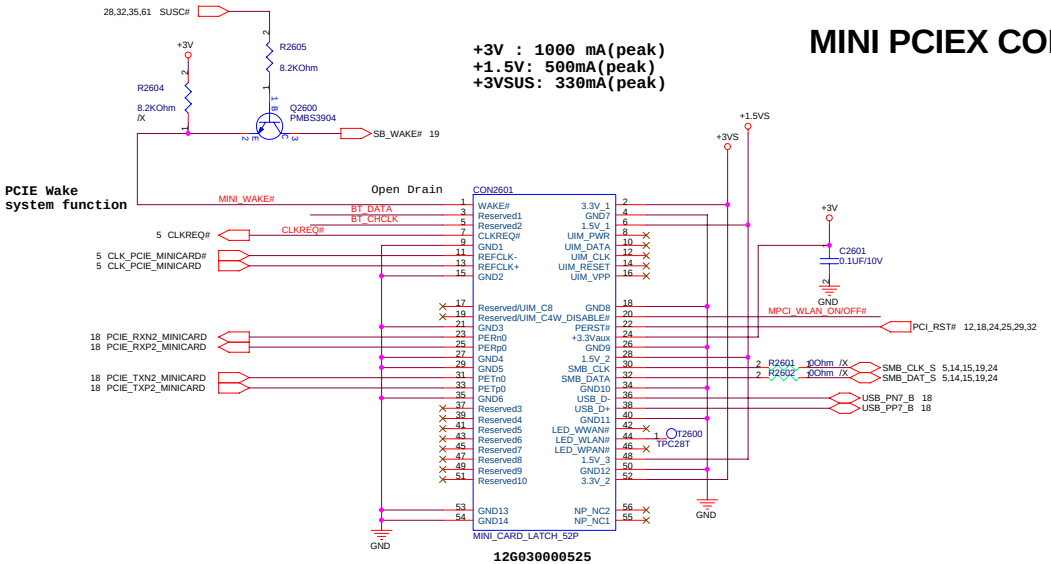
ISA ROM

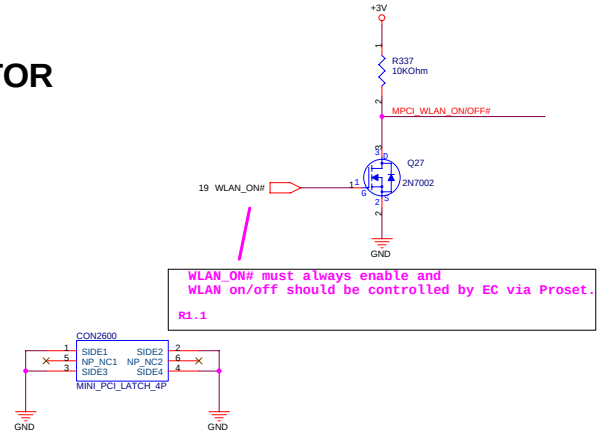
PLCC32 Socket PN:
12G04300032F

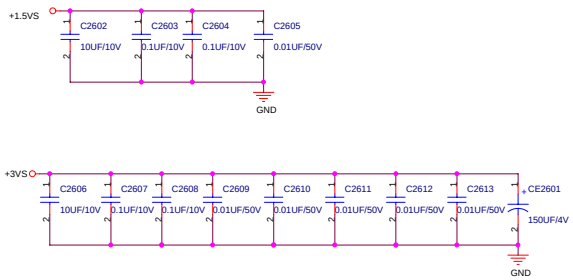


ASUSTek COMPUTER INC. NB6	Title : SUPER I/O & ROM	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 25 of 69	

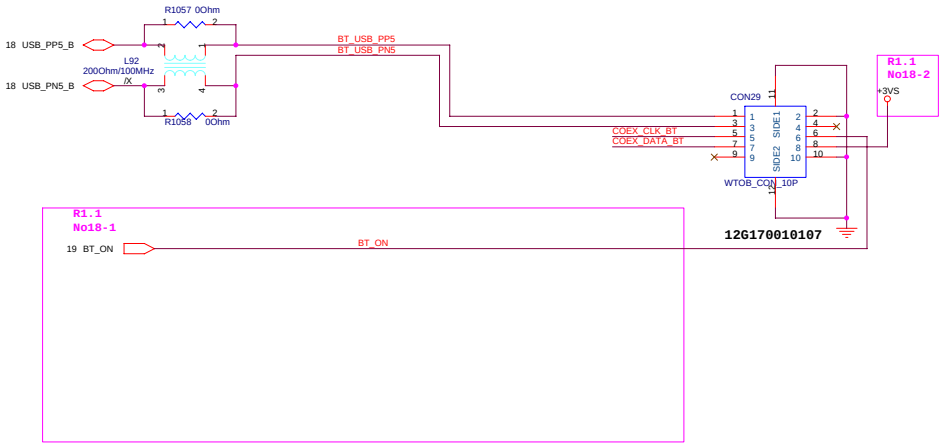
MINI PCIEX CONNECTOR



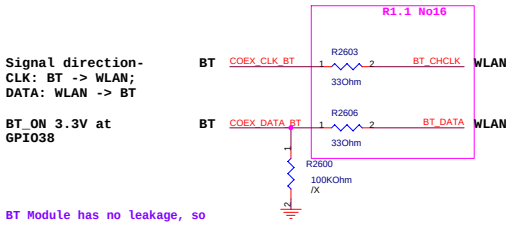




BLUETOOTH CONNECTOR



Check O/D output
or push pull



ASUSTek COMPUTER INC. NB6	Title : MINI PCIEX (TV) & BT Conn	
	Engineer: Sean1 Chou	
Size: C	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 26 of 69	

For Z62J, SATA HDD plug-in is reversed, so the pin definition is reversed.

+3VS
R339 2 1 4.7KOhm IDE_PIORDY
R340 1 2 8.2KOhm INT_IRQ14
+5VS
R341 1 2 10KOhm IDE_DIAG

+5VS
R343 10KOhm
R344 10KOhm
if use EC ->3V
IDE_RST#
Q28B UM6K1N
Q28A UM6K1N
7,18,19,28,42 PLT_RST#
GND GND

+5VS
CE2701 10UF/10V
CE2702 10UF/10V
C2700 4700PF/25V
C2701 4700PF/25V
GND

+3VS
CE2703 10UF/10V
C2702 4700PF/25V
GND

CON2700
P_GND2 26
NP_NC2 24
17 SATA_TXP0
17 SATA_TXN0
17 SATA_RXN0
17 SATA_RXP0
+3VS
+5VS
GND
NP_NC1 23
P_GND1 25
SATA_CON_22P
GND
126151100229

SATA HDD

CD-ROM

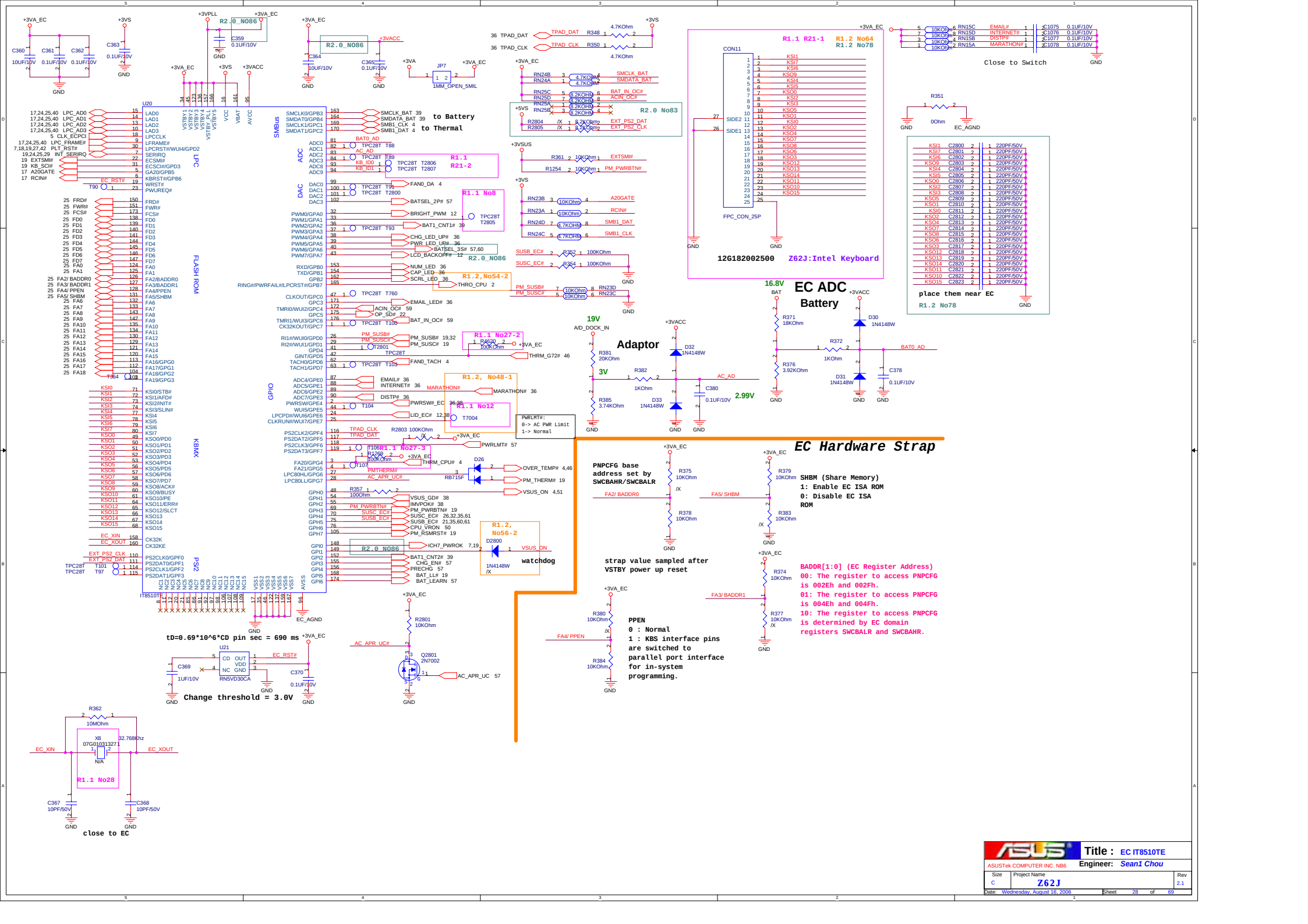
+5VS
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master
R345 1 2 470Ohm /X ODD_CSEL
R346 1 2 470Ohm
R2.1, No90
to set CDROM master
GND

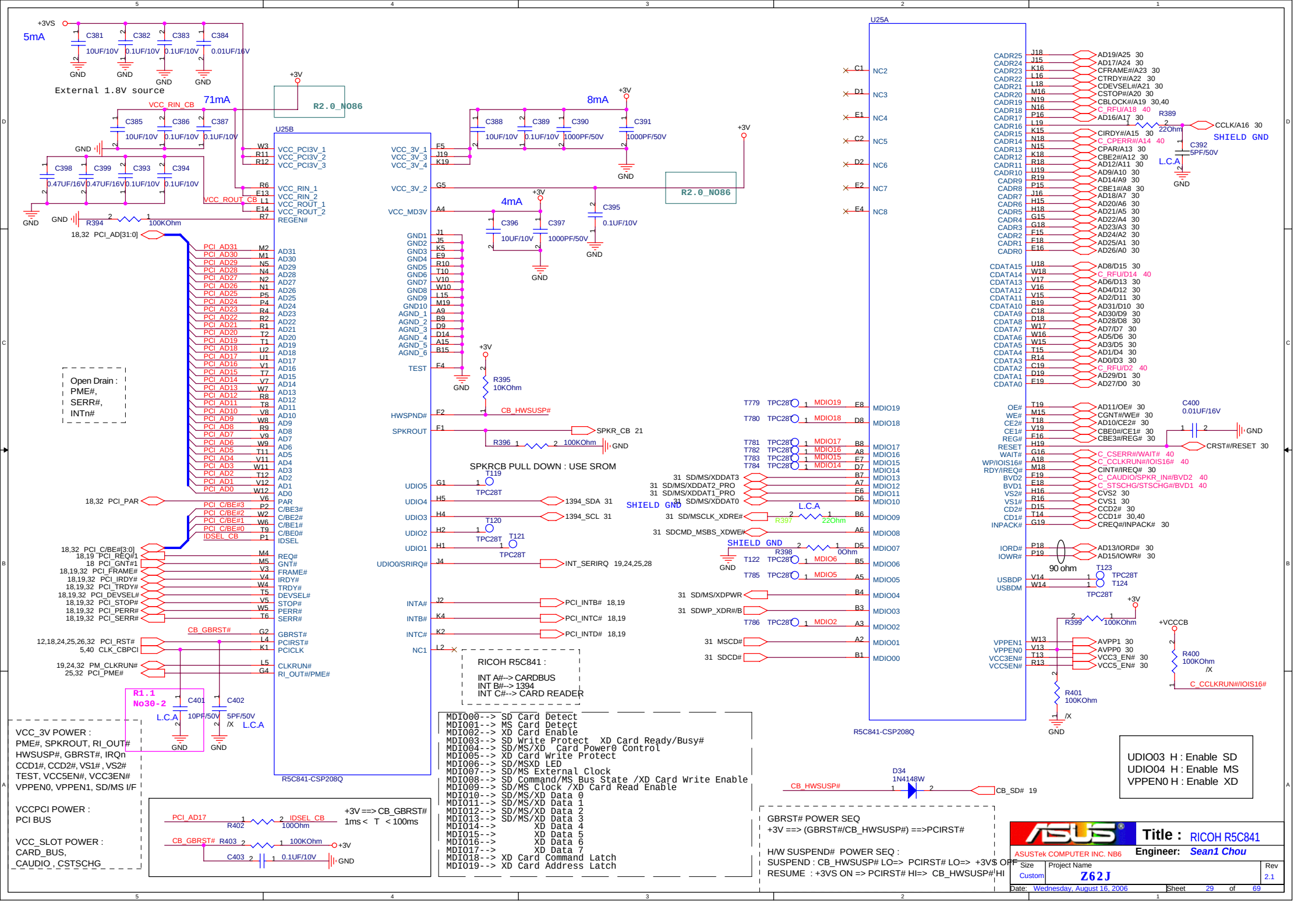
+5VS
R2701 1 2 10KOhm IDE_IOCS16_2#

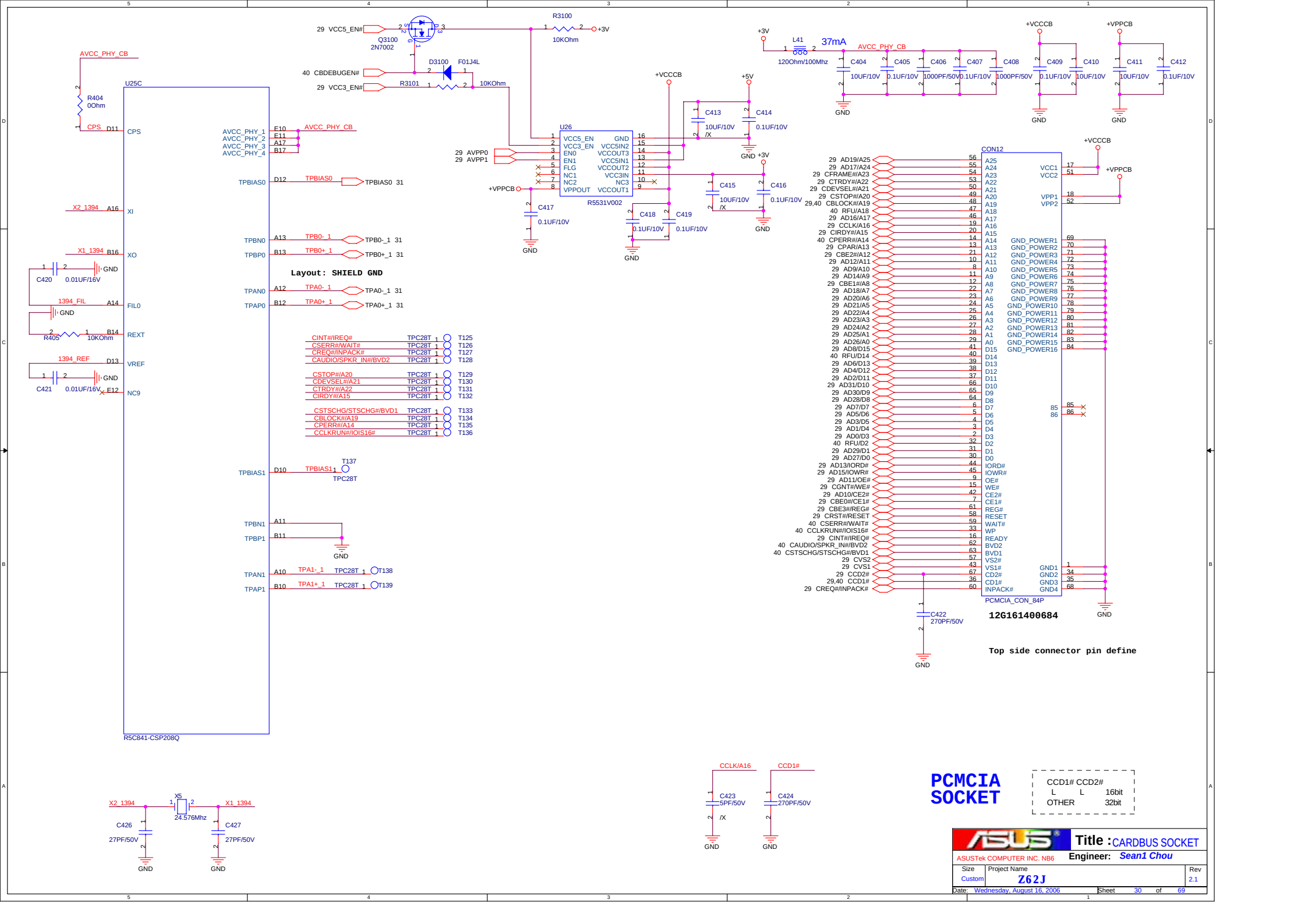
R1.1, No36
CON10
NP_NC1 51
NP_NC3 53
21 CD_L_A
21 CD_GND_A
CD_GND_A
CD_R_A 21
IDE_RST#
IDE_PDD7
IDE_PDD6
IDE_PDD5
IDE_PDD4
IDE_PDD3
IDE_PDD2
IDE_PDD1
IDE_PDD0
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDDREQ
IDE_PDIOR#
IDE_PDDREQ 17
IDE_PDIOR# 17
17 IDE_PDIOW#
17 IDE_PIORDY
17 INT_IRQ14
17 IDE_PDA1
17 IDE_PDA0
17 IDE_PDCS1#
IDE_PDIOW#
IDE_PIORDY
INT_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDDACK#
IDE_IOCS16_2#
IDE_DIAG
IDE_PDA2
IDE_PDCS3#
IDE_PDDACK# 17
IDE_PDA2 17
IDE_PDCS3# 17
TPC287
T2700
+5VS
+5VS
ODD_CSEL
NP_NC2 52
NP_NC4 54
cd_rom_50p
CE24 10UF/10V
GND GND GND
126161210507

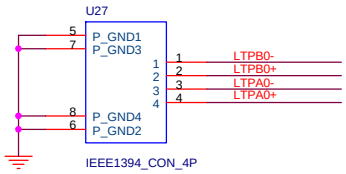
17 IDE_PDD[15:0]
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15

ASUSTek COMPUTER INC. NB6
Title : HDD & CDROM
Engineer: Sean1 Chou
Size: Custom
Project Name: Z62J
Rev: 2.1
Date: Wednesday, August 16, 2006
Sheet 27 of 69

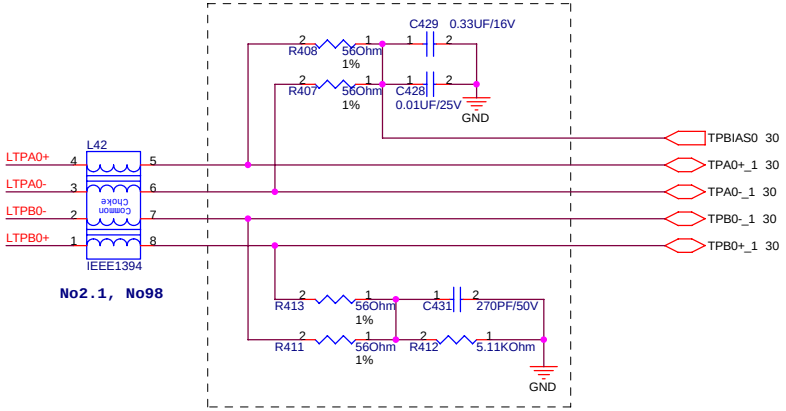

U20
IT8510TE
LPC
FLASH ROM
KBWK
PS/2
GPIO
SMBus
ADC
DAC
to Battery
to Thermal
R1.1 R21-1
R1.2 No64
R1.2 No78
12G182002500
Z62J:Intel Keyboard
Close to Switch
place them near EC
R1.2 No78
EC ADC
Battery
Adaptor
16.8V
19V
3V
2.99V
EC Hardware Strap
PNPCFG base address set by SWCBAHR/SWCBALR
SHBM (Share Memory)
1: Enable EC ISA ROM
0: Disable EC ISA ROM
strap value sampled after VSTBY power up reset
BADDR[1:0] (EC Register Address)
00: The register to access PNPCFG is 002Eh and 002Fh.
01: The register to access PNPCFG is 004Eh and 004Fh.
10: The register to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.
PPEN
0 : Normal
1 : KBS interface pins are switched to parallel port interface for in-system programming.
tD=0.69*10^6*CD pin sec = 690 ms
Change threshold = 3.0V
close to EC
watchdog
PWRLMT#:
0-> AC PWR Limit
1-> Normal
Title : EC IT8510TE
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Project Name Z62J
Size C
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 28 of 69


+3VS
5mA
C381 10UF/10V
C382 0.1UF/10V
C383 0.1UF/10V
C384 0.01UF/16V
GND
External 1.8V source
71mA
VCC_RIN_CB
C385 10UF/10V
C386 0.1UF/10V
C387 0.1UF/10V
C398 0.47UF/16V
C399 0.47UF/16V
C393 0.1UF/10V
C394 0.1UF/10V
R394 100KOhm
VCC_ROUT_CB
R2.0_N086
U25B
W3 VCC_PCI3V_1
R11 VCC_PCI3V_2
R12 VCC_PCI3V_3
R6 VCC_RIN_1
E13 VCC_RIN_2
L1 VCC_ROUT_1
E14 VCC_ROUT_2
R7 REGEN#
18,32 PCI_AD[31:0]
PCI_AD31 M2 AD31
PCI_AD30 M1 AD30
PCI_AD29 N5 AD29
PCI_AD28 N4 AD28
PCI_AD27 N2 AD27
PCI_AD26 N1 AD26
PCI_AD25 P5 AD25
PCI_AD24 P4 AD24
PCI_AD23 R4 AD23
PCI_AD22 R2 AD22
PCI_AD21 R1 AD21
PCI_AD20 T2 AD20
PCI_AD19 T1 AD19
PCI_AD18 U2 AD18
PCI_AD17 U1 AD17
PCI_AD16 V1 AD16
PCI_AD15 T7 AD15
PCI_AD14 V7 AD14
PCI_AD13 W7 AD13
PCI_AD12 R8 AD12
PCI_AD11 T8 AD11
PCI_AD10 V8 AD10
PCI_AD9 W8 AD9
PCI_AD8 R9 AD8
PCI_AD7 V9 AD7
PCI_AD6 W9 AD6
PCI_AD5 T11 AD5
PCI_AD4 V11 AD4
PCI_AD3 W11 AD3
PCI_AD2 T12 AD2
PCI_AD1 V12 AD1
PCI_AD0 W12 AD0
Open Drain : PME#, SERR#, INTn#
18,32 PCI_PAR V6 PAR
PCI_C/BE#3 P2 C/BE3#
PCI_C/BE#2 W2 C/BE2#
PCI_C/BE#1 W6 C/BE1#
PCI_C/BE#0 T9 C/BE0#
IDSEL_CB P1 IDSEL
18,32 PCI_C/BE#[3:0]
18,19 PCI_REQ#1 M4 REQ#
18 PCI_GNT#1 M5 GNT#
18,19,32 PCI_FRAME# V3 FRAME#
18,19,32 PCI_IRDY# V4 IRDY#
18,19,32 PCI_TRDY# W4 TRDY#
18,19,32 PCI_DEVSEL# T5 DEVSEL#
18,19,32 PCI_STOP# V5 STOP#
18,19,32 PCI_PERR# W5 PERR#
18,19,32 PCI_SERR# T6 SERR#
CB_GBRST# G2 GBRST#
12,18,24,25,26,32 PCI_RST# L4 PCIRST#
5,40 CLK_CBPCI K1 PCICLK
19,24,32 PM_CLKRUN# L5 CLKRUN#
25,32 PCI_PME# G4 RI_OUT#/PME#
R1.1 No30-2
C401 10PF/50V
C402 5PF/50V /X
L.C.A
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
R5C841-CSP208Q
PCI_AD17
R402 100Ohm
IDSEL_CB
+3V ==> CB_GBRST#
1ms < T < 100ms
CB_GBRST# R403 100KOhm
C403 0.1UF/10V
8mA
C388 10UF/10V
C389 0.1UF/10V
C390 1000PF/50V
C391 1000PF/50V
VCC_3V_1
VCC_3V_3
VCC_3V_4
VCC_3V_2
VCC_MD3V
4mA
C396 10UF/10V
C397 1000PF/50V
C395 0.1UF/10V
GND1 J1
GND2 J5
GND3 K5
GND4 E9
GND5 R10
GND6 T10
GND7 V10
GND8 W10
GND9 L15
GND10 M19
AGND_1 A9
AGND_2 B9
AGND_3 D9
AGND_4 D14
AGND_5 A15
AGND_6 B15
TEST F4
R395 10KOhm
HWSPND# F2
CB_HWSUSP#
SPKROUT F1
SPKR_CB 21
R396 100KOhm
SPKRCB PULL DOWN : USE SROM
UDIO5 G1 T119 TPC28T
UDIO4 H5 1394_SDA 31
UDIO3 H4 1394_SCL 31
UDIO2 H2 T120 TPC28T
UDIO1 H1 T121 TPC28T
UDIO0/SRIRQ# J4 INT_SERIRQ 19,24,25,28
INTA# J2 PCI_INTB# 18,19
INTB# K4 PCI_INTC# 18,19
INTC# K2 PCI_INTD# 18,19
NC1 L2
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
U25A
C1 NC2
D1 NC3
E1 NC4
C2 NC5
D2 NC6
E2 NC7
E4 NC8
R5C841-CSP208Q
T779 TPC28T MDIO19 E8 MDIO19
T780 TPC28T MDIO18 D8 MDIO18
T781 TPC28T MDIO17 B8 MDIO17
T782 TPC28T MDIO16 A8 MDIO16
T783 TPC28T MDIO15 E7 MDIO15
T784 TPC28T MDIO14 D7 MDIO14
31 SD/MS/XDDAT3 B7 MDIO13
31 SD/MS/XDDAT2_PRO A7 MDIO12
31 SD/MS/XDDAT1_PRO E6 MDIO11
31 SD/MS/XDDAT0 D6 MDIO10
SHIELD GND
L.C.A
31 SD/MSCLK_XDRE# R397 22Ohm B6 MDIO09
31 SDCMD_MSBS_XDWE# A6 MDIO08
SHIELD GND
R398 0Ohm
D5 MDIO07
T122 TPC28T MDIO6 B5 MDIO06
T785 TPC28T MDIO5 A5 MDIO05
31 SD/MS/XDPWR B4 MDIO04
31 SDWP_XDR#/B B3 MDIO03
T786 TPC28T MDIO2 A3 MDIO02
31 MSCD# A2 MDIO01
31 SDCD# B1 MDIO00
CADR25 J18 AD19/A25 30
CADR24 J15 AD17/A24 30
CADR23 K16 CFRAME#/A23 30
CADR22 L16 CTRDY#/A22 30
CADR21 L18 CDEVSEL#/A21 30
CADR20 M16 CSTOP#/A20 30
CADR19 N19 CBLOCK#/A19 30,40
CADR18 N16 C_RFU/A18 40
CADR17 P16 AD16/A17 30
R389 22Ohm
CCLK/A16 30
SHIELD GND
C392 5PF/50V
L.C.A
CADR16 L19
CADR15 K15 CIRDY#/A15 30
CADR14 N18 C_CPERR#/A14 40
CADR13 N15 CPAR/A13 30
CADR12 K18 CBE2#/A12 30
CADR11 R18 AD12/A11 30
CADR10 U19 AD9/A10 30
CADR9 R19 AD14/A9 30
CADR8 P15 CBE1#/A8 30
CADR7 J16 AD18/A7 30
CADR6 H15 AD20/A6 30
CADR5 H18 AD21/A5 30
CADR4 G15 AD22/A4 30
CADR3 G18 AD23/A3 30
CADR2 F15 AD24/A2 30
CADR1 F18 AD25/A1 30
CADR0 E16 AD26/A0 30
CDATA15 U18 AD8/D15 30
CDATA14 W18 C_RFU/D14 40
CDATA13 V17 AD6/D13 30
CDATA12 V16 AD4/D12 30
CDATA11 V15 AD2/D11 30
CDATA10 B19 AD31/D10 30
CDATA9 C18 AD30/D9 30
CDATA8 D18 AD28/D8 30
CDATA7 W17 AD7/D7 30
CDATA6 W16 AD5/D6 30
CDATA5 W15 AD3/D5 30
CDATA4 T15 AD1/D4 30
CDATA3 R14 AD0/D3 30
CDATA2 C19 C_RFU/D2 40
CDATA1 D19 AD29/D1 30
CDATA0 E19 AD27/D0 30
OE# T19 AD11/OE# 30
WE# M15 CGNT#/WE# 30
CE2# T18 AD10/CE2# 30
CE1# V19 CBE0#/CE1# 30
REG# F16 CBE3#/REG# 30
C400 0.01UF/16V
GND
RESET H19 CRST#/RESET 30
WAIT# G16 C_CSERR#/WAIT# 40
WP/IOIS16# A18 C_CCLKRUN#/IOIS16# 40
RDY/IREQ# M18 CINT#/IREQ# 30
BVD2 F19 C_CAUDIO/SPKR_IN#/BVD2 40
BVD1 E18 C_STSCHG/STSCHG#/BVD1 40
VS2# H16 CVS2 30
VS1# R16 CVS1 30
CD2# D15 CCD2# 30
CD1# T14 CCD1# 30,40
INPACK# G19 CREQ#/INPACK# 30
IORD# P18 AD13/IORD# 30
IOWR# P19 AD15/IOWR# 30
90 ohm
USBDP V14 T123 TPC28T
USBDM W14 T124 TPC28T
+3V
R399 100KOhm
+VCCCB
VPPEN1 W13 AVPP1 30
VPPEN0 V13 AVPP0 30
VCC3EN# T13 VCC3_EN# 30
VCC5EN# R13 VCC5_EN# 30
R400 100KOhm /X
C_CCLKRUN#/IOIS16#
R401 100KOhm /X
GND
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
CB_HWSUSP#
D34 1N4148W
CB_SD# 19
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3V$ OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
Title : RICOH R5C841
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size Custom
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 29 of 69


U25C
R5C841-CSP208Q
Layout: SHIELD GND
R5531V002
U26
CON12
PCMCIA_CON_84P
12G161400684
Top side connector pin define
PCMCIA SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Project Name Z62J
Rev 2.1
Date: Wednesday, August 16, 2006
Sheet 30 of 69

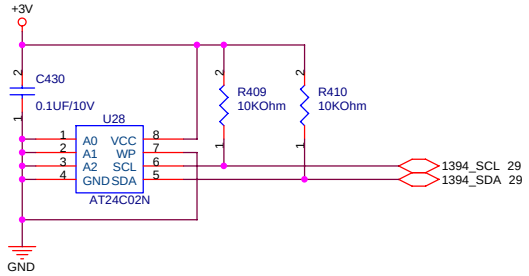


12G13101004G

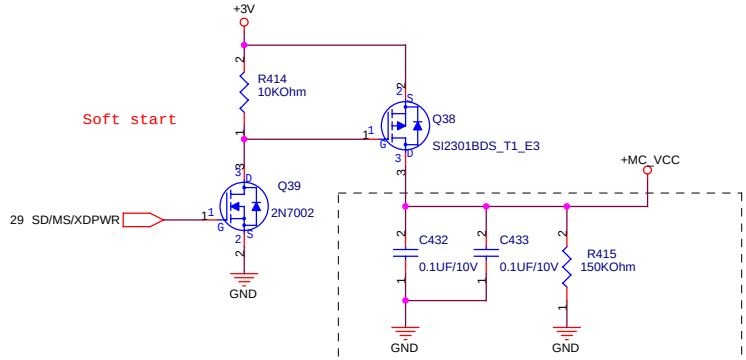


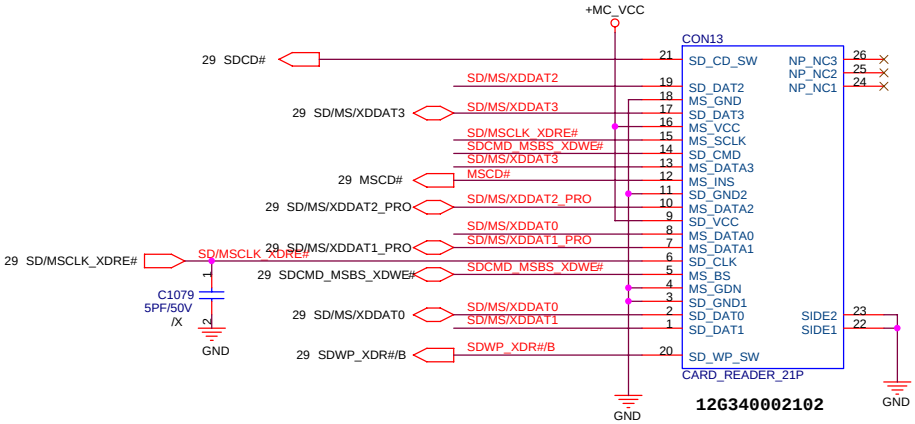
No2.1, No98

1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm



Soft start



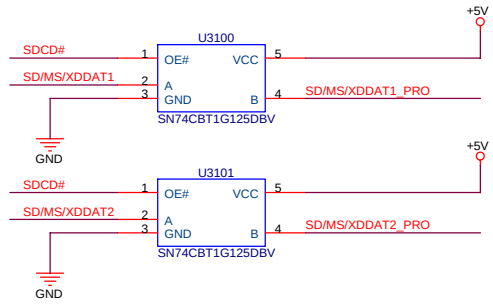


12G340002102

Layout: SHIELD GND

R1.1 No14

R2.0 No80



For correcting the isuue MS Duo adaptor plugging in

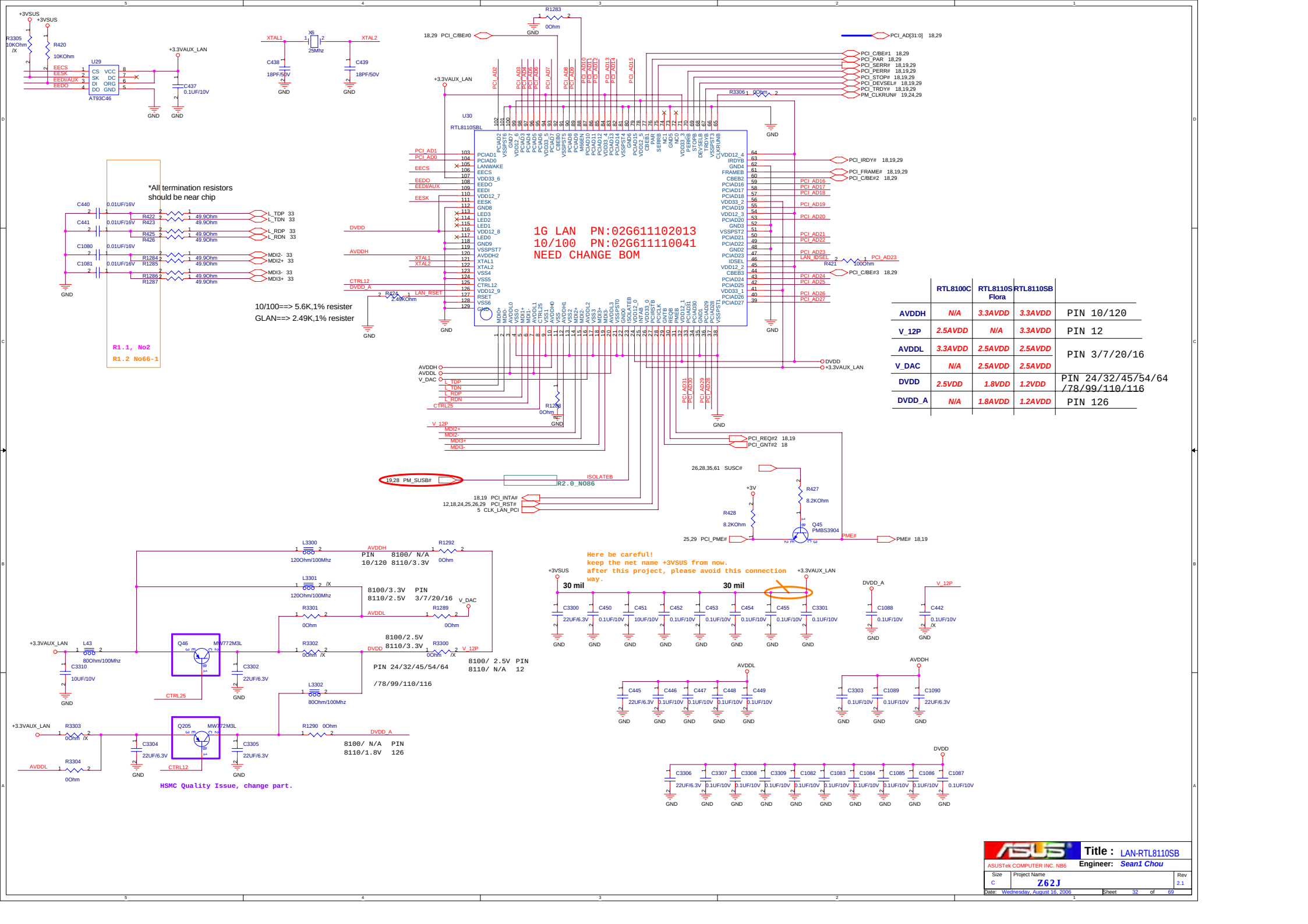
ASUSTek COMPUTER INC. NB6

Title : 1394 & 3 IN 1 CON

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 31 of 69



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

Title :	LAN-RTL8110SB		
ASUSTek COMPUTER INC. NB6	Engineer:	Sean1 Chou	
Size: C	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 32 of 69		

LAN PORT

CON27
SIDE2
SIDE1
WTOB_CON_2P
RJ11_RING_CON
RJ11_TIP_CON
1KOhm/100Mhz
C893 1000PF/3KV N/A GND
C894 1000PF/3KV N/A GND
L82 RJ11_RING
L83 RJ11_TIP
CON28
SIDE1
P_GND1
NP_NC1
NP_NC2
P_GND2
SIDE2
MODULAR_JACK_12P
LAN_TXP
LAN_TXN
LAN_RXP
LAN_RXN
LAN_MDI2P
LAN_MDI2N
LAN_MDI3P
LAN_MDI3N

12G17000002B

R2.1, No89

12G142111121

R1.1 CAE change footprint

R1.2 No66-3

TRANSFORMER 10/100MB
Dual Layout with GiGa Transformer.

U3300
L_RDN
L_RDP
RDC1
RDC2
L_TDN
L_TDP
RD+
RD-
RDCT
PTCT/TDCT
TD+
TD-
RX+
RX-
RXCT
TXCT
TX+
TX-
NC1
NC2
NC3
NC4
LAN_RDN
LAN_RDP
L_CMT1
L_CMT0
LAN_TDN
LAN_TDP
10/100MB
/X

L_RDP_MB 37
L_RDN_MB 37
L_TDP_MB 37
L_TDN_MB 37

R1293 unmount when using 10/100 LAN

AVDDL
R1293 0Ohm
U60
RDC
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
R3311 0Ohm
RDC1
TCT3
TD3+
TD3-
R3312 0Ohm
RDC2
TCT4
TD4+
TD4-
32 MDI3-
32 MDI3+
32 MDI2-
32 MDI2+
32 L_RDN
32 L_RDP
32 L_TDN
32 L_TDP
MCT1 L_CMT3
MX1+ LAN_MDI3-
MX1- LAN_MDI3+
MCT2 L_CMT2
MX2+ LAN_MDI2-
MX2- LAN_MDI2+
MCT3 L_CMT1
MX3+ LAN_RDN
MX3- LAN_RDP
MCT4 L_CMT0
MX4+ LAN_TDN
MX4- LAN_TDP
1GB

C1091 0.01UF/25V
C1092 0.01UF/25V
C1093 0.01UF/25V
C1094 0.01UF/25V
GND

L_RDP_MB 0Ohm RN45A LAN_RXP
L_RDN_MB 0Ohm RN45B LAN_RXN
L_TDP_MB 0Ohm RN45C LAN_TXP
L_TDN_MB 0Ohm RN45D LAN_TXN

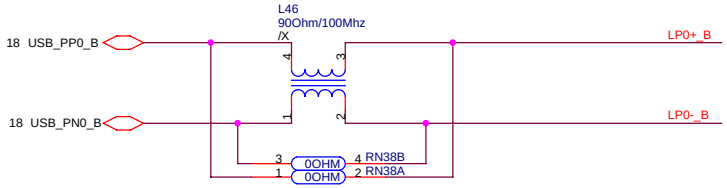
20060714 for Napa refresh

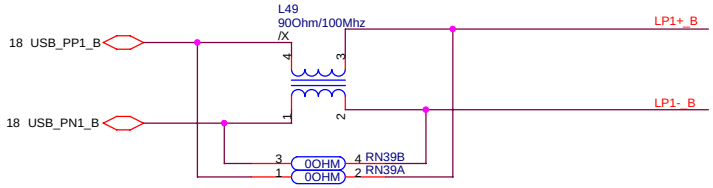
L_MDI2+_MB 0Ohm RN47A LAN_MDI2P
L_MDI2-_MB 0Ohm RN47B LAN_MDI2N
L_MDI3+_MB 0Ohm RN47C LAN_MDI3P
L_MDI3-_MB 0Ohm RN47D LAN_MDI3N

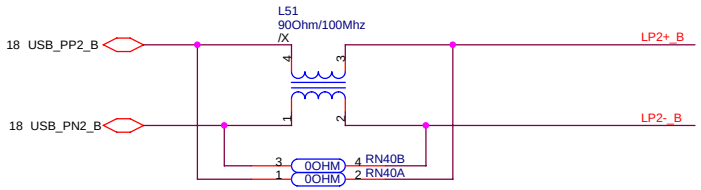
L_MDI3+_MB 37
L_MDI3-_MB 37
L_MDI2+_MB 37
L_MDI2-_MB 37

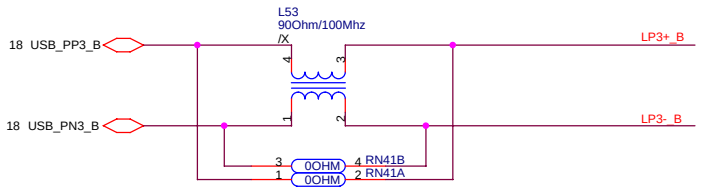
LAN_MDI3- R3307 75Ohm /X GND_LAN
LAN_MDI3+ R3308 75Ohm /X
LAN_MDI2- R3309 75Ohm /X
LAN_MDI2+ R3310 75Ohm /X
L_CMT0 RN46A 75Ohm
L_CMT1 RN46B 75Ohm
L_CMT2 RN46C 75Ohm
L_CMT3 RN46D 75Ohm
C769 0.1UF/10V

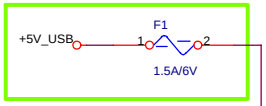
Title : RJ11+45		
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 33 of 69	

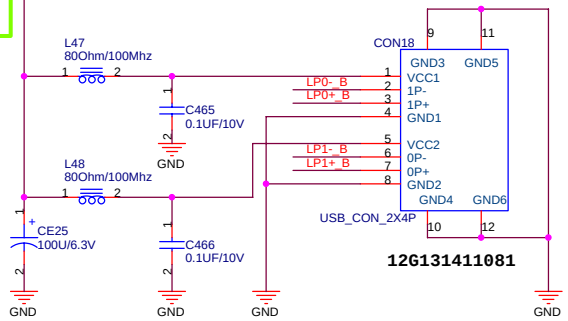


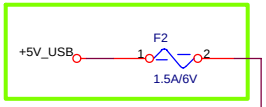


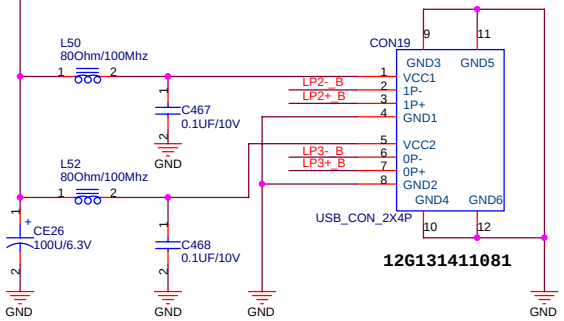










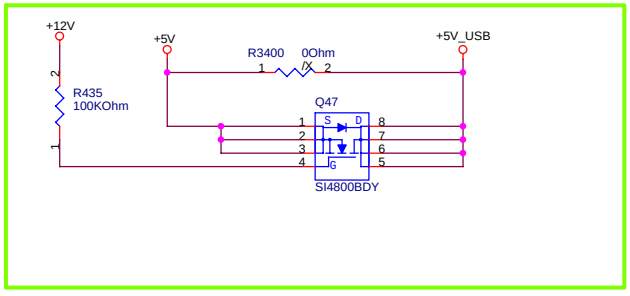


CAE modify: need check layout

Z62JM ER NO3

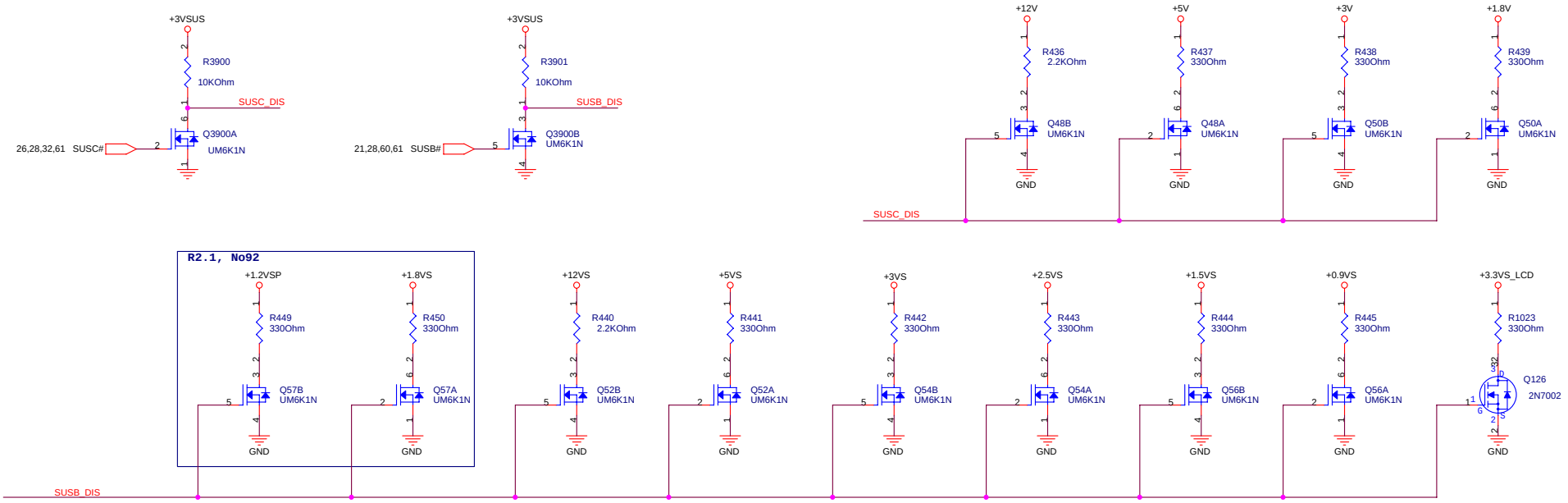
add back MOS to solve USB power leakage

R2.1, No93

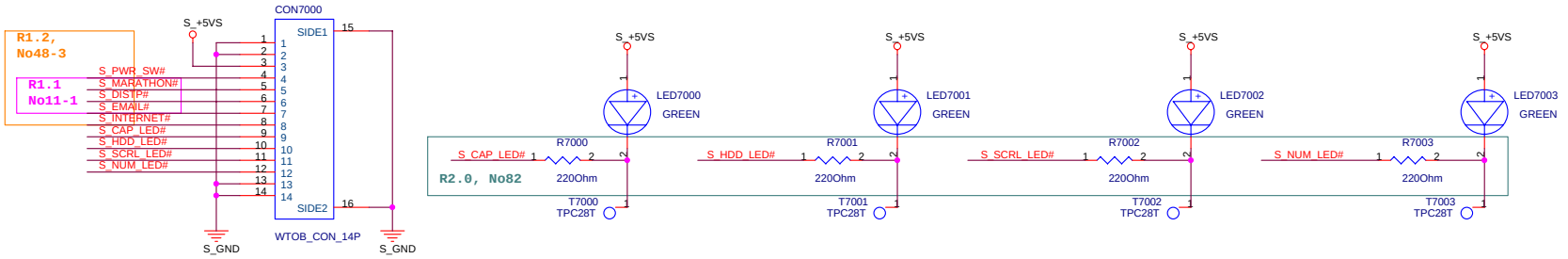


ASUSTek COMPUTER INC. NB6	Title : USB CONN X 5	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 34 of 69	

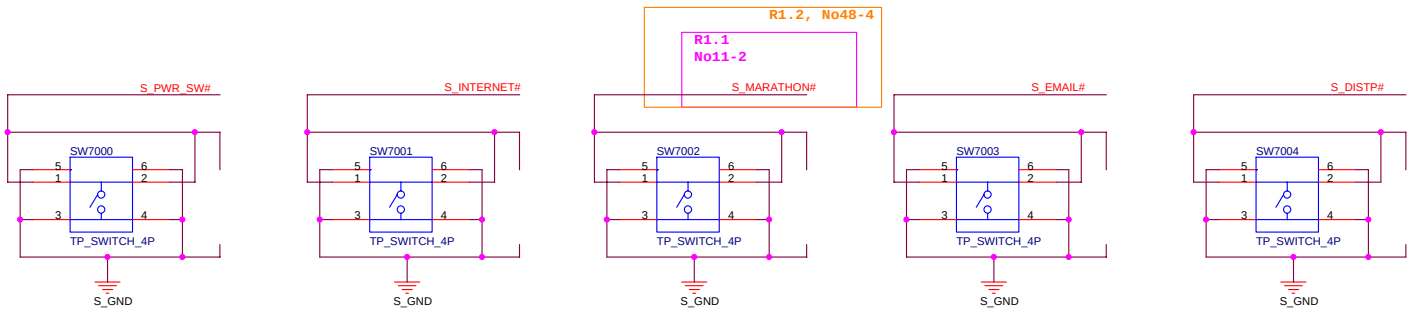
Discharge Circuit

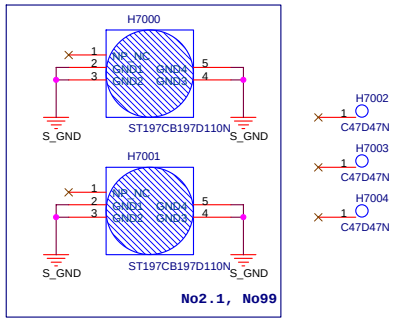


Launch Board

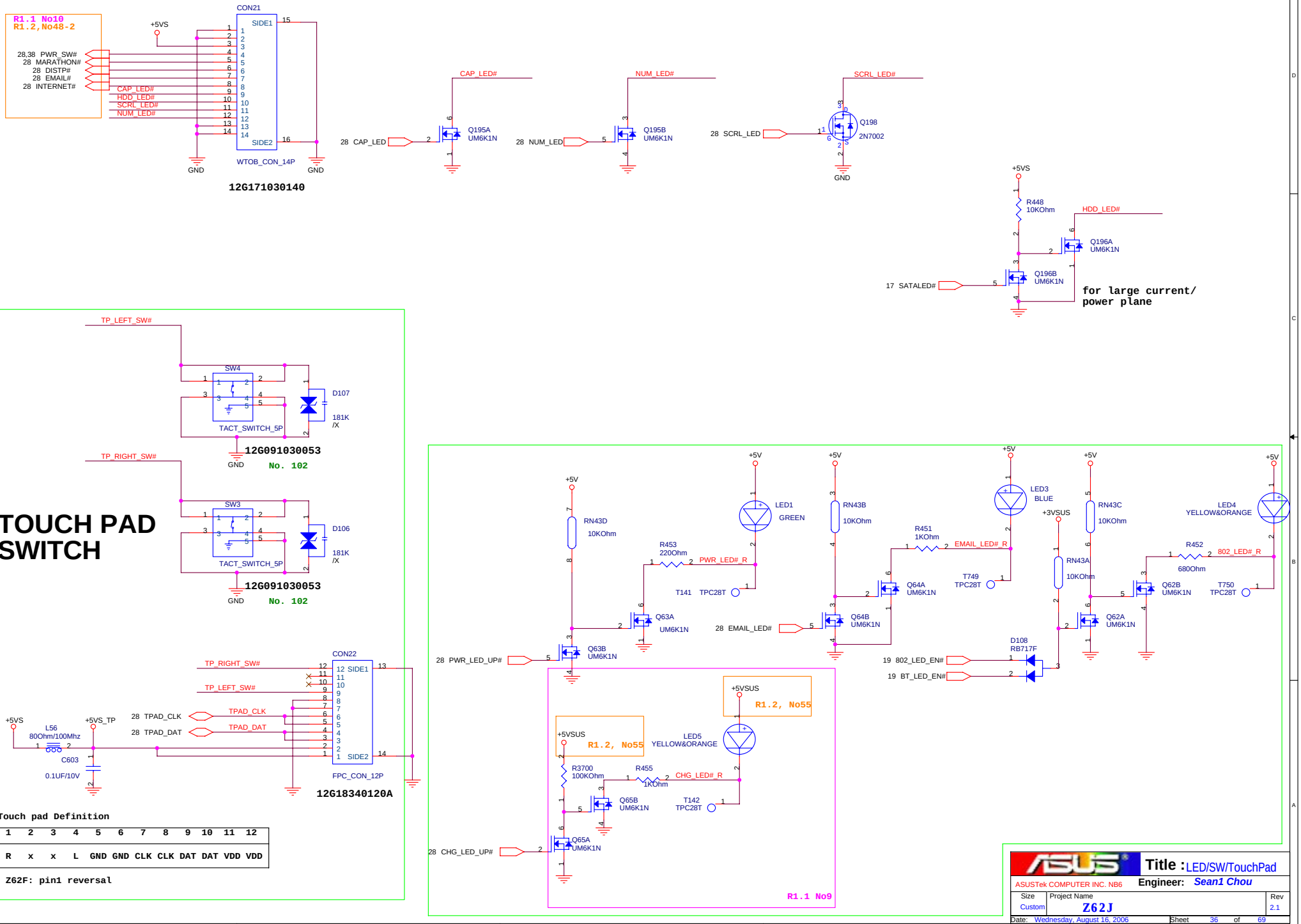


12G171030140





ASUSTek COMPUTER INC. NB6	Title : Discharge Circuit & Launch B	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 35 of 69	


R1.1 No10
R1.2,No48-2
28,38 PWR_SW#
28 MARATHON#
28 DISTP#
28 EMAIL#
28 INTERNET#
CAP_LED#
HDD_LED#
SCRL_LED#
NUM_LED#
+5VS
CON21
SIDE1
SIDE2
WTOB_CON_14P
GND
12G171030140
28 CAP_LED
Q195A
UM6K1N
28 NUM_LED
Q195B
UM6K1N
28 SCRL_LED
Q198
2N7002
17 SATALED#
R448
10KOhm
Q196A
UM6K1N
Q196B
UM6K1N
for large current/
power plane
TP_LEFT_SW#
TP_RIGHT_SW#
SW4
SW3
TACT_SWITCH_5P
D107
D106
181K
/X
12G091030053
No. 102
TOUCH PAD
SWITCH
CON22
FPC_CON_12P
12G18340120A
+5VS_TP
L56
80Ohm/100Mhz
C603
0.1UF/10V
28 TPAD_CLK
28 TPAD_DAT
TPAD_CLK
TPAD_DAT
Touch pad Definition
1 2 3 4 5 6 7 8 9 10 11 12
R x x L GND GND CLK CLK DAT DAT VDD VDD
Z62F: pin1 reversal
+5V
RN43D
10KOhm
LED1
GREEN
R453
220Ohm
PWR_LED#_R
T141 TPC28T
Q63A
UM6K1N
Q63B
UM6K1N
28 PWR_LED_UP#
RN43B
10KOhm
R451
1KOhm
EMAIL_LED#_R
T749
TPC28T
Q64A
UM6K1N
Q64B
UM6K1N
28 EMAIL_LED#
LED3
BLUE
+3VSUS
RN43C
10KOhm
RN43A
10KOhm
D108
RB717F
19 802_LED_EN#
19 BT_LED_EN#
LED4
YELLOW&ORANGE
R452
680Ohm
802_LED#_R
Q62B
UM6K1N
Q62A
UM6K1N
T750
TPC28T
+5VSUS
R1.2, No55
LED5
YELLOW&ORANGE
R3700
100KOhm
R455
1KOhm
CHG_LED#_R
Q65B
UM6K1N
Q65A
UM6K1N
T142
TPC28T
28 CHG_LED_UP#
R1.1 No9
Title : LED/SW/TouchPad
ASUSTek COMPUTER INC. NB6
Engineer: Sean1 Chou
Size
Custom
Project Name
Z62J
Rev
2.1
Date: Wednesday, August 16, 2006
Sheet 36 of 69

if we use +3V, PR_IN will be low when entering S4,S5, and then switch to PortBar (can not wake on on-board LAN)

R1.2,No45

+3VSUS

PR_IN# pull high to make sure can switch to CRT.

R818 10KOhm

13 PR_IN#

PR_IN#

D56 1SS355

A/D_DOCK_PR

A/D_DOCK_IN

DOCK_VIN_P

4 A(Typ)

L65 680Ohm/100Mhz

Q71 SI3457BDV

R819 100KOhm

R820 20KOhm

PR_IN# Q

For EMI (NEAR CONNECTOR)

A/D_DOCK_PR

+5VS

+5V_PR

C771 0.1UF/25V

C772 0.1UF/10V

C773 0.1UF/10V

PORT BAR III CONN.

L_MDI2-_MB
L_MDI2+_MB
L_MDI3+_MB
L_MDI3-_MB

L_MDI2-_MB 33
L_MDI2+_MB 33
L_MDI3+_MB 33
L_MDI3-_MB 33

L_TDP_MB
L_TDN_MB
L_RDP_MB
L_RDN_MB

L_TDP_MB 33
L_TDN_MB 33
L_RDP_MB 33
L_RDN_MB 33

A/D_DOCK_PR

CN12

18 USB_PN4_B

L_MDI3+_PR
L_MDI2+_PR
L_TDP_PR
L_RDP_PR

L_MDI3-_PR
L_MDI2-_PR
L_TDN_PR
L_RDN_PR

USB_PP4_B 18

25 LPT_PD0
25 LPT_PD2
25 LPT_PD5
25 SLCT_BUSY
13 VSYNC_PB
13 DAC_G_PB

L66 120Ohm/100Mhz

DAC_G_PB_Q

SLCT_STB# 25
LPT_PD1 25
LPT_PD3 25
LPT_PD7 25

PR_IN#_Q

DDC2BD_5 13

C1095 22PF/25V

+5VS

25 SLCT_PE
25 LPT_PD6
25 SLCT_SLIN#
25 SLCT_ERROR#

SLCT_ACK# 25
LPT_PD4 25
SLCT_INIT# 25
SLCT_AFD# 25
LPT_SLCT 25

+12VS

R824 0Ohm

+5V_PR

13 HSYNC_PB
13 DAC_R_PB

L68 120Ohm/100Mhz

DAC_R_PB_Q

DAC_B_PB_Q

DDC2BC_5 13
DAC_B_PB 13

L67 120Ohm/100Mhz

C1097 22PF/25V

C775 0.1UF/25V

DOCKING_68P

C1096 22PF/25V

12G190006810

+5VS

D57 1N4148W

LPT_PD5

R821 2.7KOhm

RP4A

LPT_PD3
LPT_PD7
LPT_PD1
LPT_PD2
LPT_PD4
LPT_PD6
SLCT_SLIN#
SLCT_INIT#

10 RP4B
10 RP4C
10 RP4D
10 RP4E
10 RP4F
10 RP4G
10 RP4H

RP5A

SLCT_STB#
SLCT_ERROR#
SLCT_ACK#
SLCT_PE
SLCT_BUSY
LPT_SLCT
SLCT_AFD#
LPT_PD0

10 RP5B
10 RP5C
10 RP5D
10 RP5E
10 RP5F
10 RP5G
10 RP5H

2.7KOhm

R1.2,No66-4
R1.2 No66-2
R2.0 No71
R2.0 No76
R2.0 No85

OE	S	Out
L	L	B1
L	H	B2
H	X	NC

20060714 for Napa refresh

33 LAN_MDI3-
33 LAN_MDI3+
33 LAN_MDI2-
33 LAN_MDI2+
33 LAN_TDP
33 LAN_TDN
33 LAN_RDP
33 LAN_RDN

LAN_MDI3-
LAN_MDI3+
LAN_MDI2-
LAN_MDI2+
LAN_TDP
LAN_TDN
LAN_RDP
LAN_RDN

R3704 0Ohm
R3701 0Ohm
R3702 0Ohm
R3703 0Ohm

L_MDI3-_MB
L_MDI3-_PR
L_MDI3+_MB
L_MDI3+_PR
L_MDI2-_PR
L_MDI2-_MB
L_MDI2+_PR
L_MDI2+_MB
L_TDP_MB
L_TDP_PR
L_TDN_MB
L_TDN_PR
L_RDP_PR
L_RDP_MB
L_RDN_PR
L_RDN_MB

R1.1 No32

C1095,C1096,C1097 mount

For Port Bar OC

+5V_PR

+5V

U62

OUT IN
GND
SET ON#

AAT4610AIGV

C776 0.47UF/16V

10KOhm R825

C777 4.7UF/10V

change P/N for buyer:06G030004040

DAC_G_PB
DAC_R_PB
DAC_B_PB

R826 150Ohm
R827 150Ohm
R828 150Ohm

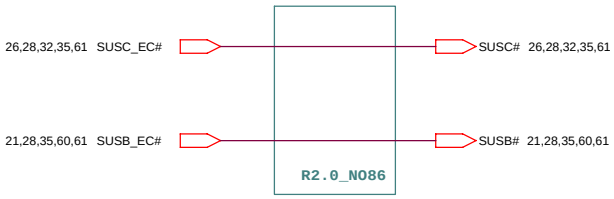
ASUSTek COMPUTER INC. NB6

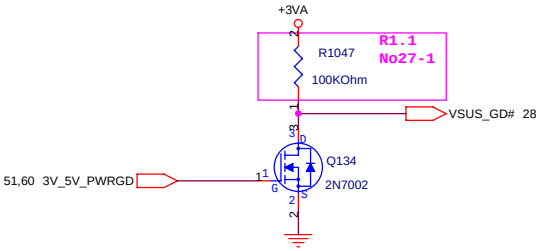
Title : PORT BAR 3 Conn.

Engineer: Sean1 Chou

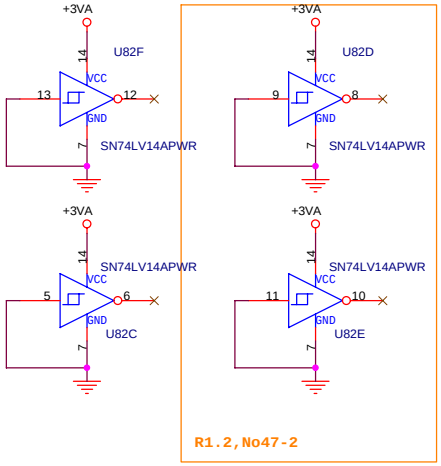
Size	Project Name	Rev
C	Z62J	2.1

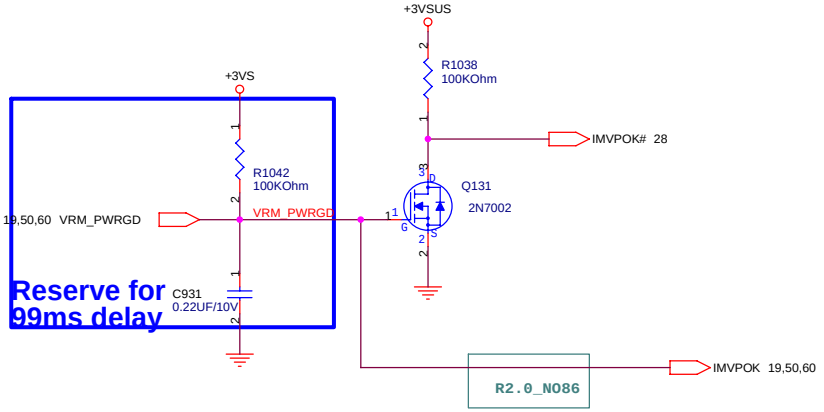
Date: Wednesday, August 16, 2006 Sheet 37 of 69



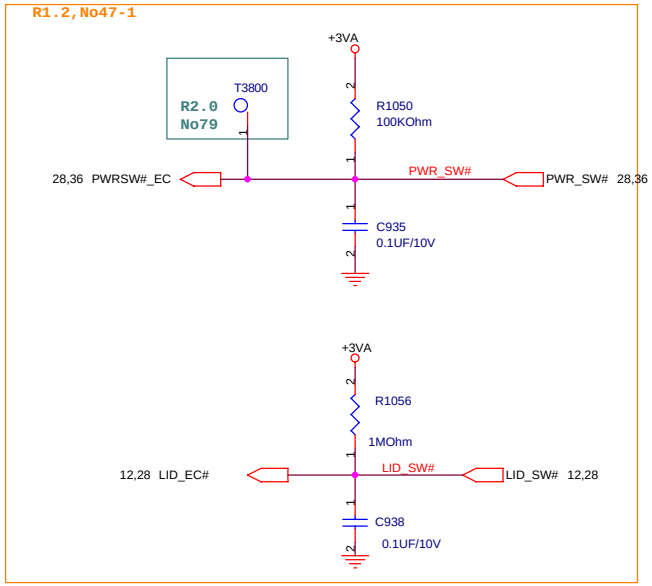


To Discharge circuits



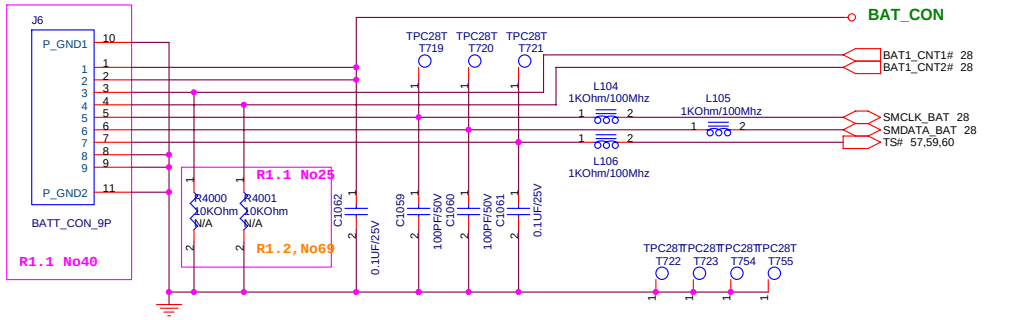


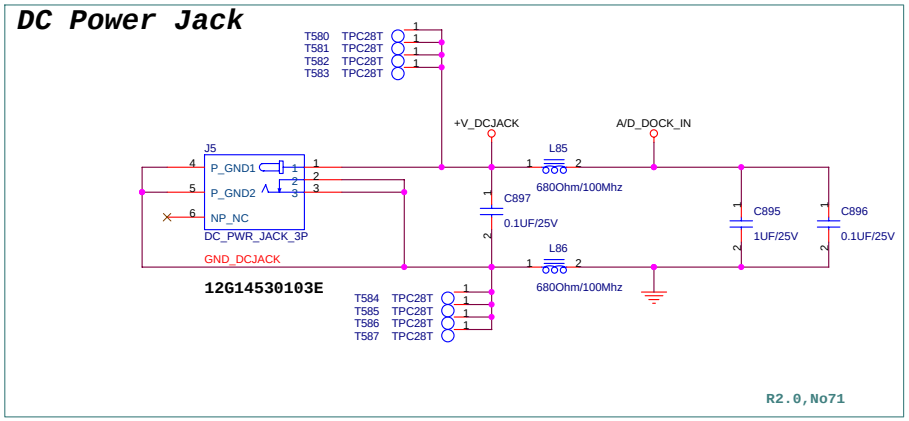
because of LID_SW# and PWR_SW# is connected to EC, we can simplify the circuits.

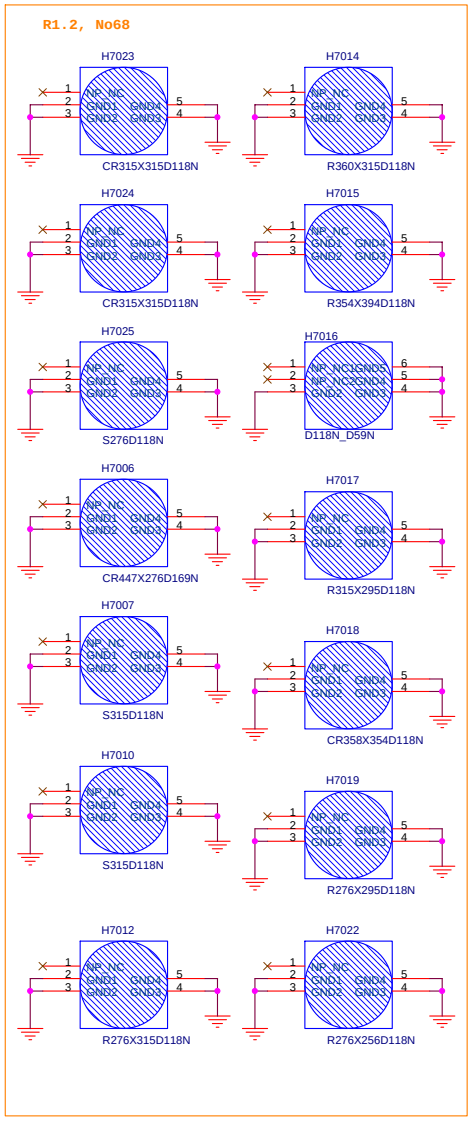


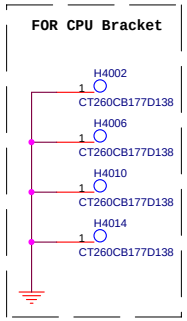
POWER SWITCH

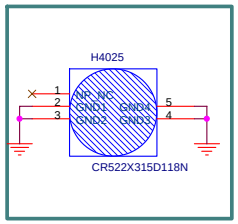
ASUSTek COMPUTER INC. NB6	Title : POWER-ON SEQ.	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 38 of 69	

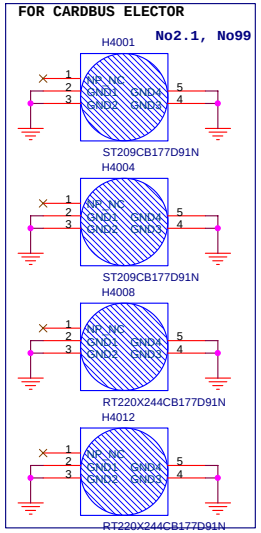


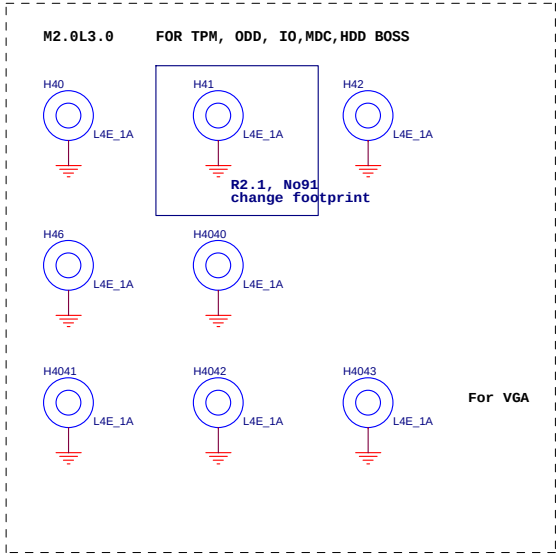


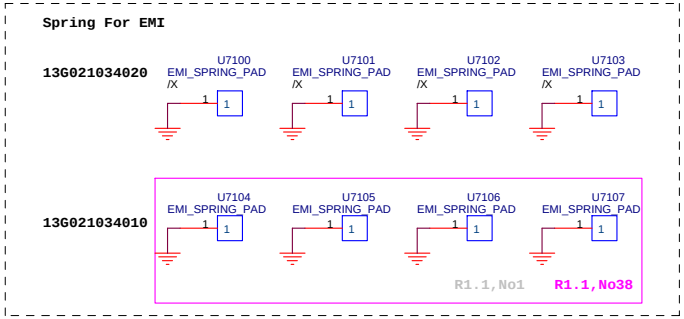


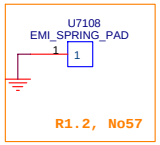






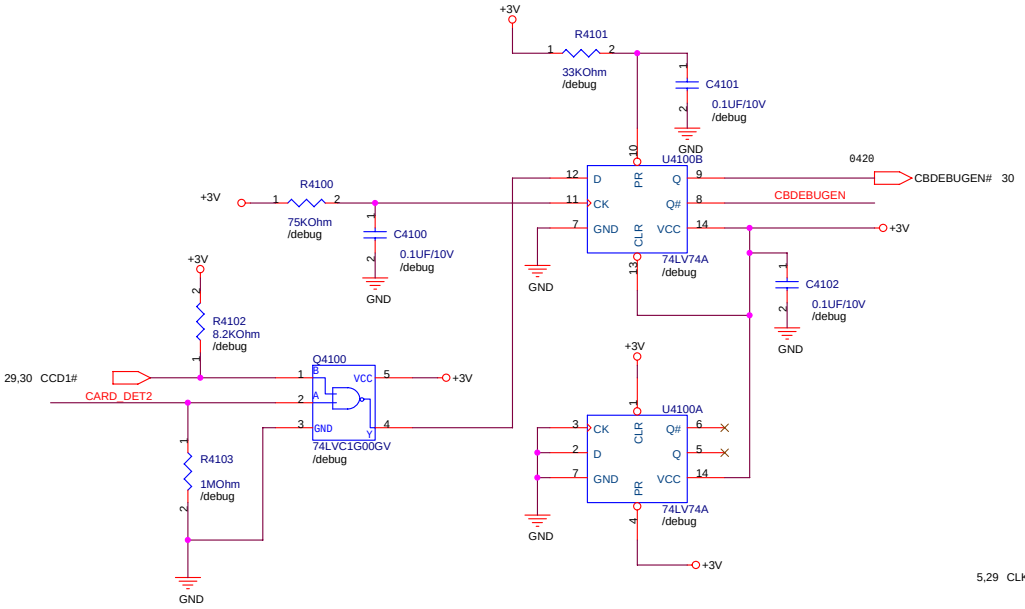






R1.2,No67

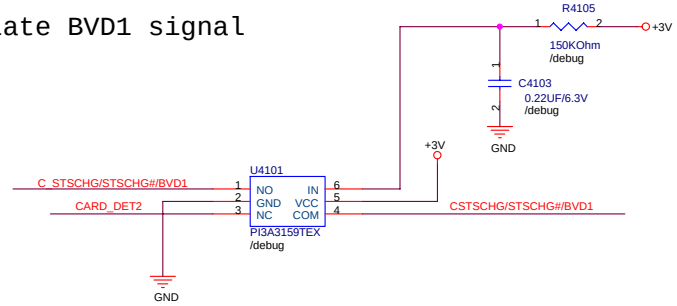
ASUSTek COMPUTER INC. NB6	Title : DC/ BATT IN & Screw Hole	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 39 of 69	



PCMCIA DEBUG PORT

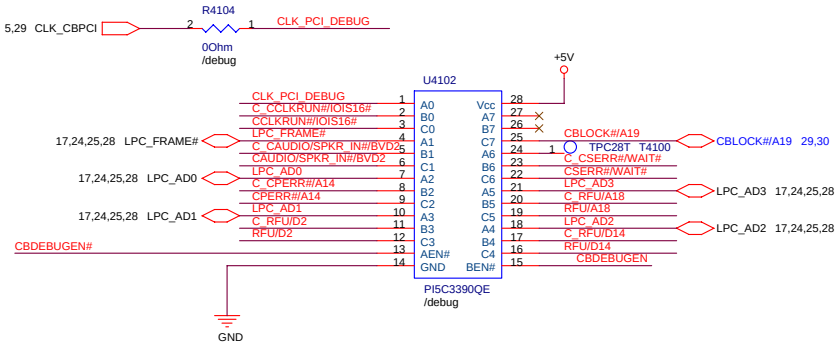
RC value may need to tuned for each product.

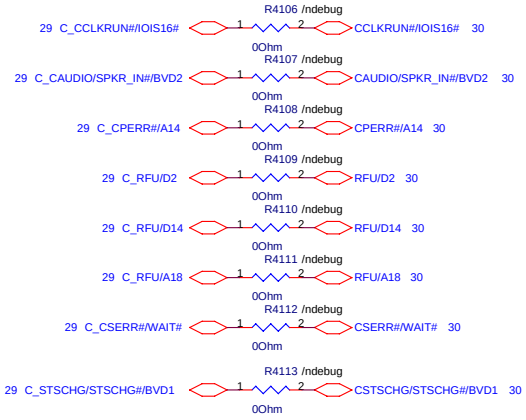
Isolate BVD1 signal



When +3V on, select BVD1 to CARD_DET2 for RC delay time

Isolate card bus control and slot signal when debug card plug in





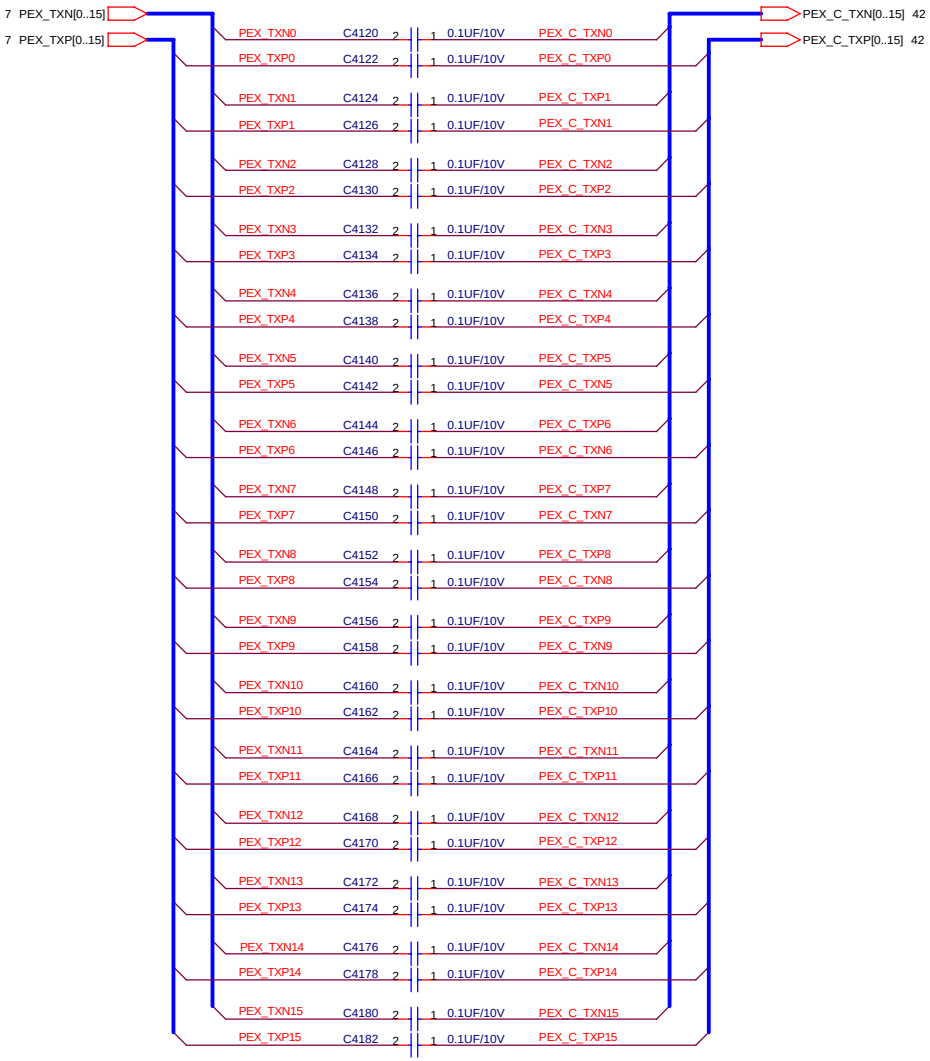
ASUSTek COMPUTER INC. NB6 **Engineer:** *Sean1 Chou*

Title : PCMCIA Debug

Size	Project Name	Rev
Custom	Z62J	2.1

Date: Wednesday, August 16, 2006 Sheet 40 of 69

PEX_C_TXN1,5,6,7,8,9 polarity reverse



PLACE these 0402 AC coupling caps close to 945PM.

PEX_RXN13 polarity reverse

PLACE these 0402 AC coupling caps close to G72M

ASUSTek COMPUTER INC. NB6	Title : PCIE AC COUPLE	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 41 of 69	

G72M-V

G72M-V need to change P/N: 02G190009303

U4200A

PCI-E I/F

R2.1_N087
R4202 0Ohm
7,18,19,27,28 PLT_RST#
no stuff
UNMOUNT R4203 200Ohm /X
C4200 0.1UF/10V /X
GND

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
5 CLK_G72
5 CLK_G72#
41 PEX_C_TXP[0..15]
41 PEX_C_TXN[0..15]
41 PEX_C_RXP[0..15]
41 PEX_C_RXN[0..15]

TW=5mils
TD=6/7mils
TW=5mils
PD=20mils
TW=5mils
TD=6/7mils
TW=5mils

PEX_IOVDD_0..5 — AD23 AF23 AF24 AF25 AG24 AG25
PEX_IOVDDQ_0..10 — AC16 AC17 AC21 AC22 AE18 AF21 AF22 AE12 AF18 AF21 AF22
VDD_0..19 — K16 K17 N13 N14 N16 N17 N19 N20 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19
VDD_20..37 — U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20
VDD_LP_0..5 — P20 T20 T23 U20 U23 W20
VDD33_0..12 — AC11 AC12 AC24 AD24 AE11 AE12 H7 J7 K7 L10 L7 L8 M10
PEX_PLLAVDD AF15
PEX_PLLDVDD AE15
PEX_PLLGND AE16
NC_0..4 — AM10 AM8 AM9 B32 J6

+1.2VSP
PEX_IOVDD
C4201 0.022UF/16V
C4202 0.022UF/16V
C4203 0.022UF/16V
C4204 4.7UF/6.3V
<< Place near balls
GND

+1.2VSP
PEX_IOVDDQ
Place Close to GPU
C4205 0.01UF/16V
C4206 0.01UF/16V
C4207 0.01UF/16V
C4208 0.01UF/16V
C4209 0.01UF/16V
C4210 0.022UF/25V
C4211 0.022UF/16V
C4212 4.7UF/6.3V
<< Place near balls
GND

+VGA_VCORE
TPC28T T4200
+1.2VSP
L4200 120Ohm/100Mhz
C4219 0.1UF/10V
C4225 4.7UF/6.3V
GND

+VGA_VCORE
C4213 4700PF/25V
C4214 0.01UF/16V
C4215 0.1UF/10V
C4216 0.022UF/16V
C4217 4.7UF/6.3V
C4218 0.022UF/16V
<< Place on bottom north of GPU
GND

C4220 4700PF/25V
C4221 0.01UF/16V
C4222 0.1UF/10V
C4223 0.022UF/16V
C4224 4.7UF/6.3V
<< Place on bottom east of GPU
GND

C4229 4700PF/25V
C4230 0.01UF/16V
C4226 0.022UF/16V
C4227 0.1UF/10V
C4228 4.7UF/6.3V
<< Place on bottom south of GPU
GND

C4231 4700PF/25V
C4232 0.01UF/16V
C4233 0.022UF/16V
C4234 0.1UF/10V
C4235 4.7UF/6.3V
<< Place on bottom west of GPU
GND

+VGA_VCORE
C4236 4700PF/25V
C4237 0.01UF/16V
C4238 0.022UF/16V
C4239 4.7UF/6.3V
C4240 0.1UF/10V
<< Place near balls
GND

+3VS
C4241 0.1UF/10V
C4242 4700PF/25V
C4243 0.022UF/16V
C4244 0.022UF/16V
C4245 1UF/10V
C4246 0.022UF/16V
<< Place near balls
GND

PEX_PLL_AVDD
C4247 0.1UF/10V
C4248 4700PF/25V
C4249 0.022UF/16V
C4250 0.022UF/16V
C4251 0.022UF/16V
<< Place near balls
GND

+1.2VSP
Place Near BGA
L4201 120Ohm/100Mhz
C4252 0.1UF/10V
C4253 0.01UF/16V
C4254 4.7UF/6.3V
<< Place near balls
GND

+1.2VSP
Place Near BGA
L4202 120Ohm/100Mhz
C4255 4700PF/25V
C4256 0.01UF/16V
C4257 4.7UF/6.3V
C4258 4.7UF/6.3V
<< Place near balls
GND

Title :	NV43M Main
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev: 2.1	
Date: Wednesday, August 16, 2006	Sheet 42 of 69

FOR MEMORY STRAPS

U4200E

G72M-V

STRAP

NC FOR NV44

MEMSTRAPSEL0
MEMSTRAPSEL1
MEMSTRAPSEL2
MEMSTRAPSEL3

RFU6
RFU7
RFU8
RFU9
RFU10
RFU11
RFU12

ROMCS* — NVROMCS — TPC28T T4300

ROM_SO — TPC28T T4301
ROM_SI — TPC28T T4302
ROM_SCLK — TPC28T T4303

I2CH_SCL — HDCPROMSCL — TPC28T T4304
I2CH_SDA — HDCPROMSDA — TPC28T T4305

BUFRST* — TPC28T T4306

STEREO — TPC28T T4307

SWAPRDY_A — SWAPRDY_A — TPC28T T4308

TESTMEMCLK — TESTMEMCLK — R4300 10KOhm
TESTMODE — TESTMODE — R4305 10KOhm

MCG0
MCG1

GND

FOR MEMORY STRAPS

+3VS

C4300 0.1UF/10V

PLACE CAPS & RES CLOSE TO GPU PINS

U4200K

G72M-V

MIOA_VDDQ_0
MIOA_VDDQ_1
MIOA_VDDQ_2
MIOA_VDDQ_3
MIOA_VDDQ_4

MIOACAL_PD_VDDQ — TPC28T T4309
MIOACAL_PU_GND — TPC28T T4310

MIOA_VREF

R4315 1KOhm /X

R4317 1KOhm /X

C4301 0.1UF/10V /X

GND

MIOAD0
MIOAD1
MIOAD2
MIOAD3
MIOAD4
MIOAD5
MIOAD6
MIOAD7
MIOAD8
MIOAD9
MIOAD10
MIOAD11

MIOAD0 — MIOAD1 — MIOAD2 — MIOAD3 — MIOAD4 — MIOAD5 — MIOAD6 — MIOAD8 — MIOAD9

/X 10KOhm R4328
/X 10KOhm R4329
/X 10KOhm R4330
/X 10KOhm R4331

+3VS

(for panel user ID)

MIOAD[2:5] : USER[0:3]

MIOAD7 : TVMODE0
MIOAD10 : TVMODE1

MIOA_HSYNC : GPU MCH share ref clk or not

MIOA_HSYNC
MIOA_VSYNC
MIOA_DE
MIOA_CTL3

R4316 2KOhm /X

GND

MIOAD1 — R4314 2KOhm — For System BIOS

STRAP= 0: System BIOS
STRAP= 1: Adapter BIOS

GND

MIOA_CLKOUT
MIOA_CLKOUT*
MIOA_CLKIN

MIOA_CLKIN — R4318 10KOhm /X

check: need mount or not

GND

FOR CRYSTAL / PCIE_ID STRAPS

+3VS

MIOB_VDDQ

C4302 0.1UF/10V

PLACE CAPS CLOSE TO GPU PINS

U4200N

G72M-V

MIOB_VDDQ_0
MIOB_VDDQ_1
MIOB_VDDQ_2
MIOB_VDDQ_3
MIOB_VDDQ_4

MIOBCAL_PD_VDDQ — TPC28T T4313
MIOBCAL_PU_GND — TPC28T T4314

MIOB_VREF

R4323 1KOhm /X

R4326 1KOhm /X

C4303 0.1UF/10V /X

GND

MIOBD0
MIOBD1
MIOBD2
MIOBD3
MIOBD4
MIOBD5
MIOBD6
MIOBD7
MIOBD8
MIOBD9
MIOBD10
MIOBD11
RFU13
RFU14
RFU15
RFU16
RFU17
RFU18
RFU19
RFU20

MIOBD0 — MIOBD1 — VIPD2 — TPC28T T4311
VIPD3 — VIPD4 — VIPD5 — VIPD6 — TPC28T T4312 — VIPD7
MIOBD8 — MIOBD9 — MIOBD11

MIOBD10 : ROMTYPE0

R4319 2KOhm /X

R4322 2KOhm

GND

MIOB_VSYNC
MIOB_HSYNC
MIOB_DE
MIOB_CTL3

MIOB_VSYNC : ROMTYPE1

MIOB_CLKOUT
MIOB_CLKOUT*
MIOB_CLKIN

MIOB_CLKIN — R4327 10KOhm /X

GND

3GIO PADCFG STRP

02 (0010) NV43/44M
04 (0100) G72

+3VS

R4301 2KOhm /X — MIOAD0

R4302 2KOhm — MIOAD6

R1.1, No3

R4308 2KOhm /X — MIOAD8

R4309 2KOhm /X — MIOAD9

MEM TYPE STRAP

R1.1, No34

G72:
RAM_CFG[3:0] Config FB Bus Width Definitions
0000 16Mx16 DDR2 64-bit Elpida
0001 16Mx16 DDR2 64-bit Samsung
0010 16Mx16 DDR2 64-bit Infineon
0011 16Mx16 DDR2 64-bit Hynix
0100 64-bit Reserved
0101 32Mx16 DDR2 64-bit Samsung
0110 32Mx16 DDR2 64-bit Infineon
0111 32Mx16 DDR2 64-bit Hynix

Samsung needs:
--> unmount R4304, R4307, mount R4306, R4303

MIOBD0 : RAMCFG0
MIOBD8 : RAMCFG2
MIOBD1 : RAMCFG1
MIOBD9 : RAMCFG3

+3VS

R4303 10KOhm N/A — MIOBD0

R4304 10KOhm /X — MIOBD1

R4307 10KOhm /X

R4306 10KOhm N/A

GND

R4310 10KOhm /X — MIOBD8

R4311 10KOhm /X — MIOBD9

R4312 10KOhm

R4313 10KOhm

GND

(PCI_DEVICE_ID)

MIOBD4 : PCI_DEVID0
MIOBD5 : PCI_DEVID1
MIOBD3 : PCI_DEVID2
MIOBD11 : PCI_DEVID3

NV43M - ID 0X0168
NV43M- V- ID 0X0167

+3VS

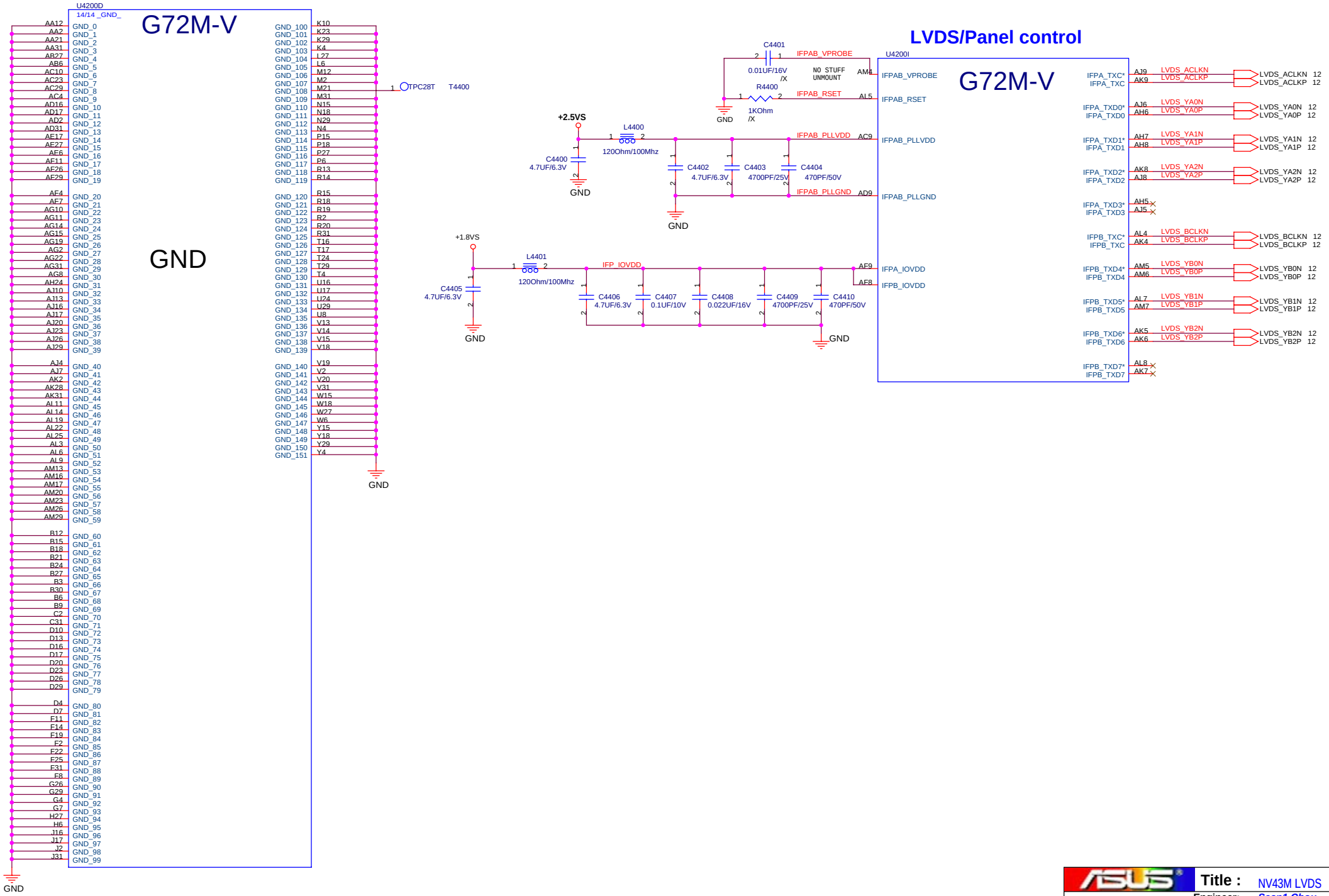
R4320 2KOhm — VIPD4

R4321 2KOhm — VIPD3

R4324 2KOhm — VIPD5

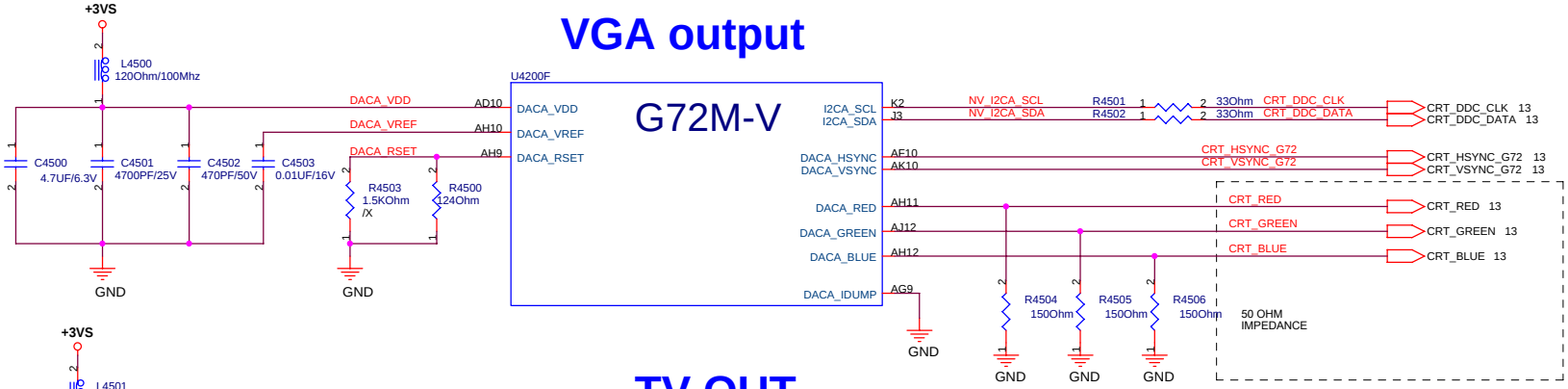
R4325 2KOhm /X — MIOBD11 — no stuff UNMOUNT

ASUSTek COMPUTER INC. NB6	Title : NV43 Strapping	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 43 of 69	

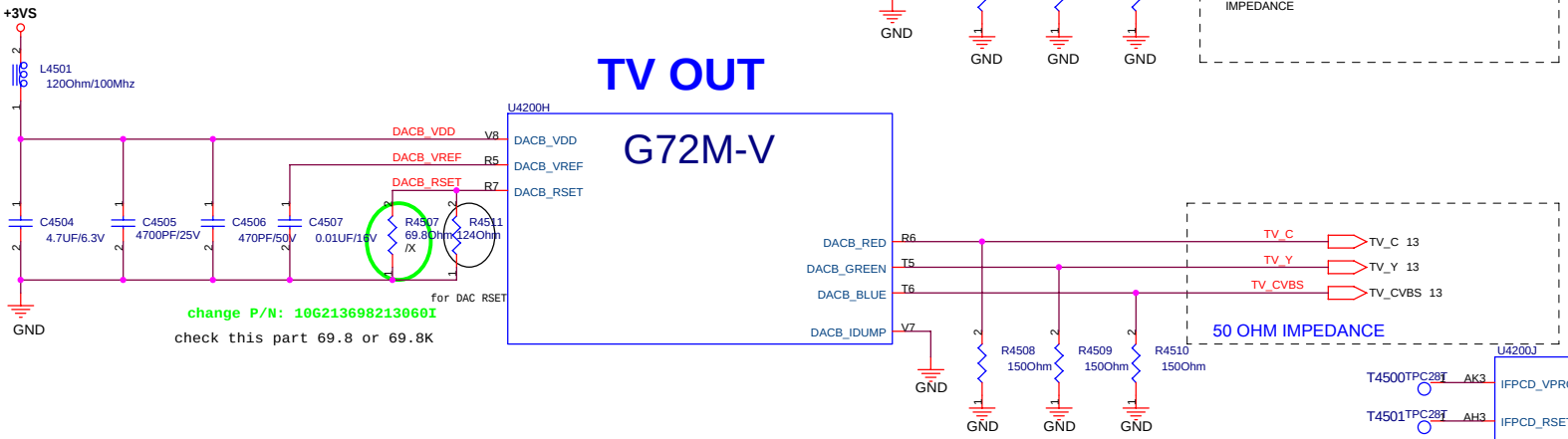


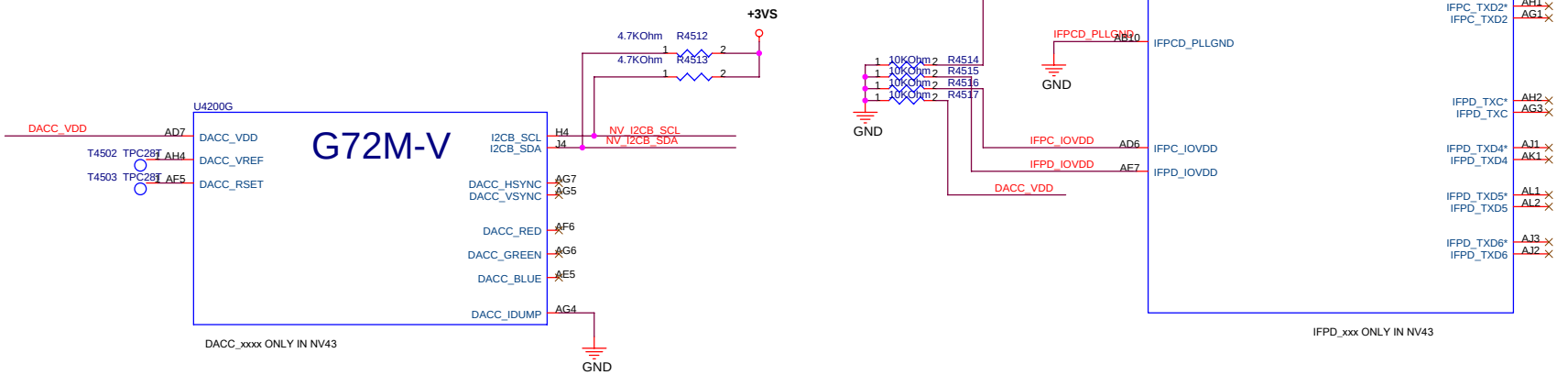
ASUSTek COMPUTER INC. NB6	Title : NV43M LVDS	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 44 of 69	

VGA output



TV OUT





<Variant Name>

ASUSTek COMPUTER INC. NB6	Title : MV43 VGA/TV Out	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 45 of 69	

XTAL/PLLVDD

PLLVDD-- 3.3V +/- 5% Imax= 25mA

DISP_PLLVDD-- 3.3V +/- 5% Imax=30mA

XTALIN is 1.2V tolerant
3.2V * 150 / (33+270+150) = 1.06

The following must be verified:
MIN Rise Time at XTALIN = 0.133 V/ns
using 10% - 90% with Vmax = 1.3V and
Vmin = -0.7V

R1.1 No35

R1.1 No33
R1.2, No58
R2.1, No88

Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

check: leakage current

R1.1 No29-2

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOT PLUG
1	IN	N/A	2ND DVI HOT PLUG
2	OUT	HIGH	BACKLIGHT BRIGHTNESS
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID0
6	OUT	HIGH	NVVDD VID1
7	OUT	HIGH	FBVDD VID0
8	IN	LOW	THERMAL SHUTDOWN
9	OUT	LOW	THERM ALERT

GPIO & JTAG

R2.0
No84

Title	NV Spread Spectrum
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev	2.1
Date: Wednesday, August 16, 2006	Sheet 46 of 69

G72M-V

VRAM I/F Channel A

U4200B

FBAD0	N27	FBAD0
FBAD1	M27	FBAD1
FBAD2	N28	FBAD2
FBAD3	L29	FBAD3
FBAD4	K27	FBAD4
FBAD5	K28	FBAD5
FBAD6	J29	FBAD6
FBAD7	J28	FBAD7
FBAD8	P30	FBAD8
FBAD9	N31	FBAD9
FBAD10	N30	FBAD10
FBAD11	N32	FBAD11
FBAD12	L31	FBAD12
FBAD13	L30	FBAD13
FBAD14	J30	FBAD14
FBAD15	L32	FBAD15
FBAD16	H30	FBAD16
FBAD17	K30	FBAD17
FBAD18	H31	FBAD18
FBAD19	E30	FBAD19
FBAD20	H32	FBAD20
FBAD21	E31	FBAD21
FBAD22	D30	FBAD22
FBAD23	E30	FBAD23
FBAD24	H28	FBAD24
FBAD25	H29	FBAD25
FBAD26	E29	FBAD26
FBAD27	J27	FBAD27
FBAD28	F27	FBAD28
FBAD29	E27	FBAD29
FBAD30	E28	FBAD30
FBAD31	F28	FBAD31
FBAD32	AD29	FBAD32
FBAD33	AE29	FBAD33
FBAD34	AD28	FBAD34
FBAD35	AC28	FBAD35
FBAD36	AB29	FBAD36
FBAD37	AA30	FBAD37
FBAD38	Y28	FBAD38
FBAD39	AB30	FBAD39
FBAD40	AM30	FBAD40
FBAD41	AF30	FBAD41
FBAD42	AJ31	FBAD42
FBAD43	AJ30	FBAD43
FBAD44	AJ32	FBAD44
FBAD45	AK29	FBAD45
FBAD46	AM31	FBAD46
FBAD47	AL30	FBAD47
FBAD48	AE32	FBAD48
FBAD49	AE30	FBAD49
FBAD50	AE31	FBAD50
FBAD51	AD30	FBAD51
FBAD52	AC31	FBAD52
FBAD53	AC32	FBAD53
FBAD54	AB32	FBAD54
FBAD55	AB31	FBAD55
FBAD56	AG27	FBAD56
FBAD57	AE28	FBAD57
FBAD58	AH28	FBAD58
FBAD59	AG28	FBAD59
FBAD60	AG29	FBAD60
FBAD61	AD27	FBAD61
FBAD62	AE27	FBAD62
FBAD63	AE28	FBAD63

49 FBAD[0..63] — FBAD[0..63]

FBADQM0	M29	FBADQM0
FBADQM1	M30	FBADQM1
FBADQM2	G30	FBADQM2
FBADQM3	F29	FBADQM3
FBADQM4	AA29	FBADQM4
FBADQM5	AK30	FBADQM5
FBADQM6	AC30	FBADQM6
FBADQM7	AG30	FBADQM7

49 FBADQM[0..7] — FBADQM[0..7]

FBAWDQS0	L28	FBADQS_WP0
FBAWDQS1	K31	FBADQS_WP1
FBAWDQS2	G32	FBADQS_WP2
FBAWDQS3	G28	FBADQS_WP3
FBAWDQS4	AB28	FBADQS_WP4
FBAWDQS5	AL32	FBADQS_WP5
FBAWDQS6	AE32	FBADQS_WP6
FBAWDQS7	AH30	FBADQS_WP7

49 FBAWDQS[0..7] — FBAWDQS[0..7]

FBARDQS0	M28	FBADQS_RN0
FBARDQS1	K32	FBADQS_RN1
FBARDQS2	G31	FBADQS_RN2
FBARDQS3	G27	FBADQS_RN3
FBARDQS4	AA28	FBADQS_RN4
FBARDQS5	AL31	FBADQS_RN5
FBARDQS6	AE31	FBADQS_RN6
FBARDQS7	AH29	FBADQS_RN7

49 FBARDQS[0..7] — FBARDQS[0..7]

NVFBA_VREF — E32 — FB_VREF1

+1.8VS

R4700 10KOhm 1% /X C4700 0.022UF/25V — NVFBA_VREF — R4701 10KOhm 1% C4718 0.022UF/25V

GND GND

+1.8VS

FBVDD_0	A12	
FBVDD_1	A15	
FBVDD_2	A18	
FBVDD_3	A21	
FBVDD_4	A24	
FBVDD_5	A27	
FBVDD_6	A3	
FBVDD_7	A30	
FBVDD_8	A6	
FBVDD_9	A9	
FBVDD_10	AA32	
FBVDD_11	AD32	
FBVDD_12	AG32	
FBVDD_13	AK32	
FBVDD_14	C32	
FBVDD_15	F32	
FBVDD_16	J32	
FBVDD_17	M32	
FBVDD_18	R32	
FBVDD_19	V32	

FBVDDQ_0	AA25	
FBVDDQ_1	AA26	
FBVDDQ_2	AB25	
FBVDDQ_3	AB26	
FBVDDQ_4	G11	
FBVDDQ_5	G12	
FBVDDQ_6	G15	
FBVDDQ_7	G18	
FBVDDQ_8	G21	
FBVDDQ_9	G22	
FBVDDQ_10	H11	
FBVDDQ_11	H12	
FBVDDQ_12	H15	
FBVDDQ_13	H18	
FBVDDQ_14	H21	
FBVDDQ_15	H22	
FBVDDQ_16	L25	
FBVDDQ_17	L26	
FBVDDQ_18	M25	
FBVDDQ_19	M26	
FBVDDQ_20	R25	
FBVDDQ_21	R26	
FBVDDQ_22	V25	
FBVDDQ_23	V26	

+1.8VS

C4701 4700PF/25V — C4702 0.022UF/25V — C4703 0.1UF/10V — C4704 0.1UF/10V — C4705 4700PF/25V — C4706 0.1UF/10V — C4707 4.7UF/6.3V — C4708 4.7UF/6.3V

GND

+1.8VS

C4709 0.022UF/25V — C4710 0.1UF/10V — C4711 4700PF/25V — C4712 0.022UF/25V — C4713 0.1UF/10V — C4714 0.1UF/10V — C4715 0.022UF/25V — C4716 0.1UF/10V — C4717 0.022UF/25V

GND

FBA_CMD0	P32	FBA_A3	FBA_A3 49
FBA_CMD1	U27	FBA_A0	FBA_A0 49
FBA_CMD2	P31	FBA_A2	FBA_A2 49
FBA_CMD3	U30	FBA_A1	FBA_A1 49
FBA_CMD4	Y31	FBE_A3	FBE_A3 49
FBA_CMD5	W32	FBE_A4	FBE_A4 49
FBA_CMD6	W31	FBE_A5	FBE_A5 49
FBA_CMD7	T32	FBA_CS1#	FBA_CS1# 49
FBA_CMD8	V27	FBA_CS0#	FBA_CS0# 49
FBA_CMD9	T28	FBA_WE#	FBA_WE# 49
FBA_CMD10	T31	FBA_BA0	FBA_BA0 49
FBA_CMD11	U32	FBA_CKE	FBA_CKE 49
FBA_CMD12	W29	FBA_RST	FBA_RST
FBA_CMD13	W30	FBE_A2	FBE_A2 49
FBA_CMD14	T27	FBA_A12	FBA_A12 49
FBA_CMD15	V28	FBA_RAS#	FBA_RAS# 49
FBA_CMD16	V30	FBA_A11	FBA_A11 49
FBA_CMD17	U31	FBA_A10	FBA_A10 49
FBA_CMD18	R27	FBA_BA1	FBA_BA1 49
FBA_CMD19	V29	FBA_A8	FBA_A8 49
FBA_CMD20	T30	FBA_A9	FBA_A9 49
FBA_CMD21	W28	FBA_A6	FBA_A6 49
FBA_CMD22	R29	FBA_A5	FBA_A5 49
FBA_CMD23	R30	FBA_A7	FBA_A7 49
FBA_CMD24	P29	FBA_A4	FBA_A4 49
FBA_CMD25	U28	FBA_CAS#	FBA_CAS# 49
FBA_CMD26	Y32		

(FBA_CMD26 ONLY IN NV44)

FBA_CLK0	P28	FBA_CLK0	FBA_CLK0 49
FBA_CLK0*	R28	FBA_CLK0#	FBA_CLK0# 49
FBA_CLK1	Y27	FBA_CLK1	FBA_CLK1 49
FBA_CLK1*	AA27	FBA_CLK1#	FBA_CLK1# 49

SWAPABLE

R1.2 No60

R2.0, No75

All unmount

+0.9VS

FBA_CS1#	1	2 RN4701A
FBA_A9	3	4 RN4701B
FBA_CAS#	1	2 RN4702A
FBA_A1	3	4 RN4702B
FBA_A8	1	2 RN4703A
FBA_A7	3	4 RN4703B
FBA_A10	1	2 RN4704A
FBA_BA0	3	4 RN4704B
FBE_A3	1	2 RN4705A
FBE_A2	3	4 RN4705B
FBA_A0	1	2 RN4706A
FBA_A6	3	4 RN4706B
FBE_A5	1	2 RN4708A
FBA_A11	3	4 RN4708B
FBA_CS0#	56Ohm /X	RN4705
FBE_A4	56Ohm /X	R4706
FBA_A12	56Ohm /X	R4707
FBA_RAS#	56Ohm /X	R4708
FBA_WE#	56Ohm /X	R4709
FBA_BA1	56Ohm /X	R4710
FBA_A2	/X1	
FBA_A5	3 56Ohm /X	4 RN4711B
FBA_A3	1 56Ohm /X	2 RN4712A
FBA_A4	3 56Ohm /X	4 RN4712B

Put termination at branch,close to VRAM

R2.0, No75

+0.9VS

C4722 0.1UF/25V /X — C4723 0.1UF/25V /X

GND

place at the start and the end of termination

+1.8VS

R7087 0Ohm — FBA_RST

R7088 10KOhm /X — FBA_ODT — FBA_ODT 49

R7089 0Ohm /X — NVFBA_DEBUG

RFU2 Y30

RFU3 AC26

FBA_DEBUG AC27

FBA_REFCLK D32 — NVFBA_REFCLK — TPC28T T4703

FBA_REFCLKN D31 — NVFBA_REFCLK# — TPC28T T4704

R7090 10KOhm

FBA_PLLVDD G23 — FBA_PLLVDD — TPC28T T4705 — GND

FBA_PLLAVDD G25 — FBA_PLLAVDD — L4700 120Ohm/100Mhz — +1.2VSP

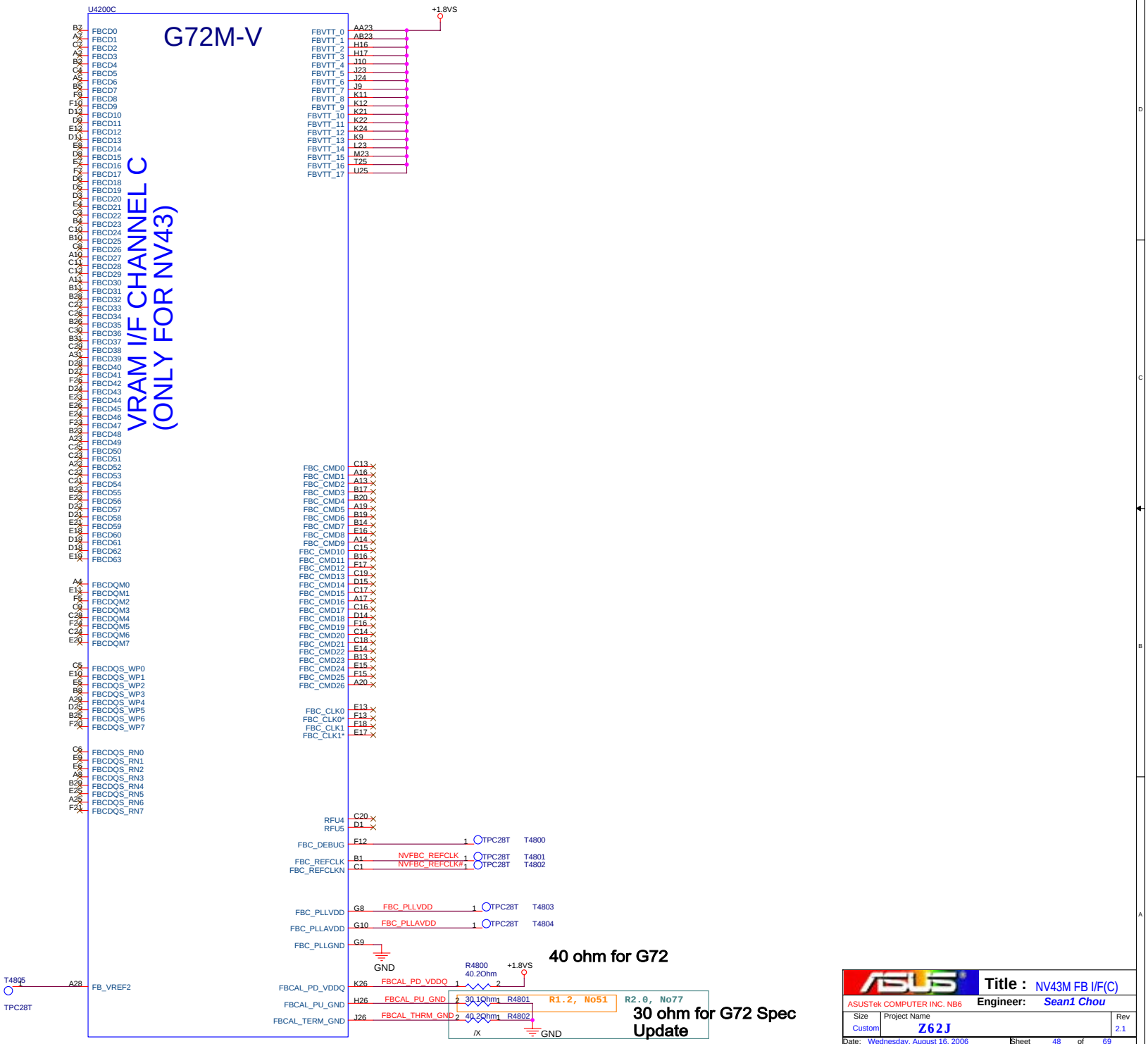
FBA_PLLGND G24

GND

C4719 470PF/50V — C4720 4700PF/25V — C4721 4.7UF/6.3V

GND

Title :	NV43M FB I/F(A)
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev: 2.1	
Date: Wednesday, August 16, 2006	Sheet 47 of 69



ASUSTek COMPUTER INC. NB6	Title : NV43M FB I/F(C)		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 48 of 69		

R1.2 No65

DDR2/16M*16-2.5 1.8V

03G151236011	INFINEON/HYB18T256161AFL-25
03G151236114	SAMSUNG/K4N56163QG-ZC25
03G151236210	HYNIX/HY5PS561621AFP-25

Swapable

Swapable

R1.1 R19

VRAM change P/N:
03G151236114

U4900 / U4901 / U4902 / U4903 — K4N56163QF-ZC25

Place near U4901

Place near U4903

VDD/VDDQ = 1.8V

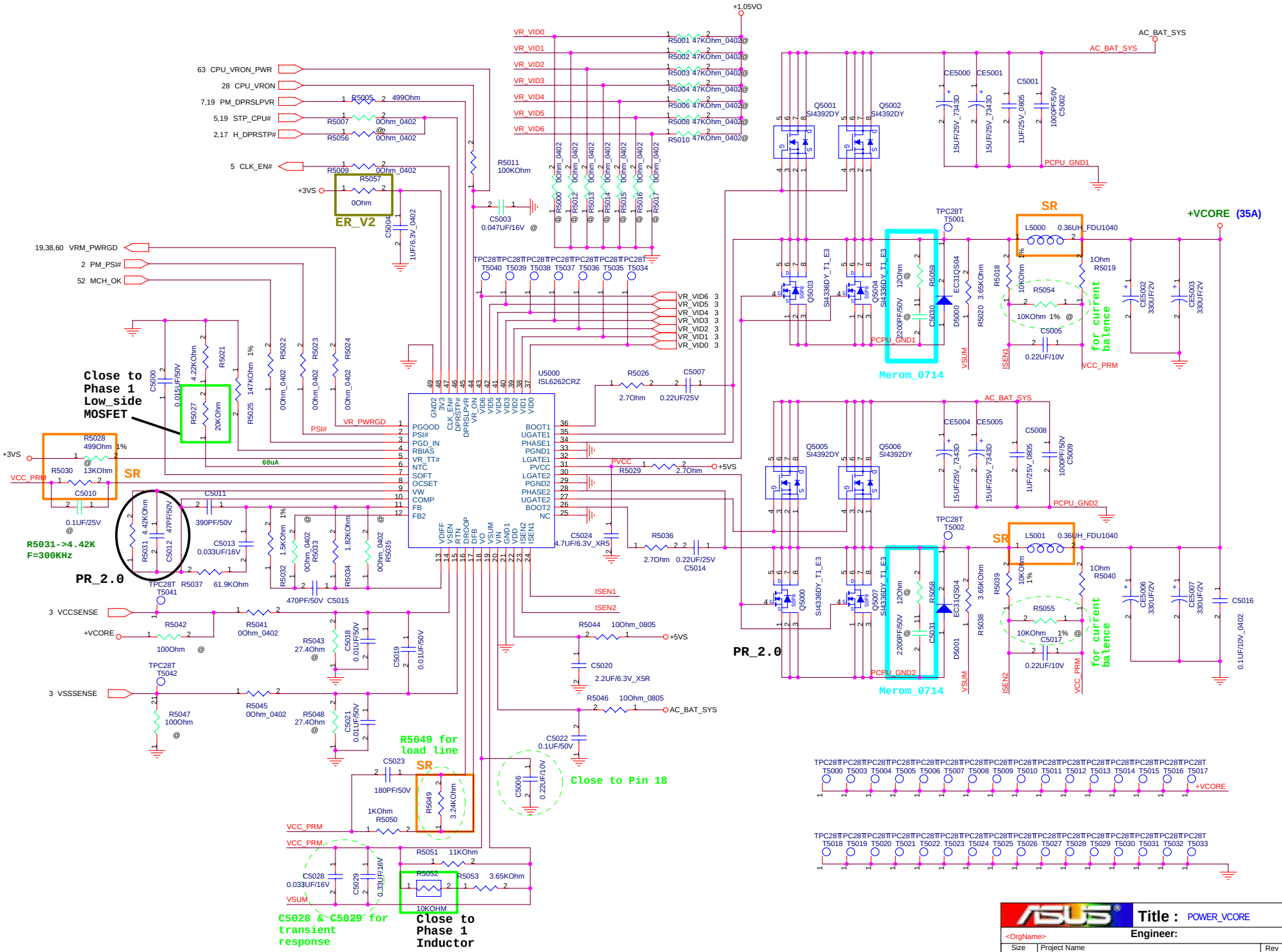
Place near right VRAM >>

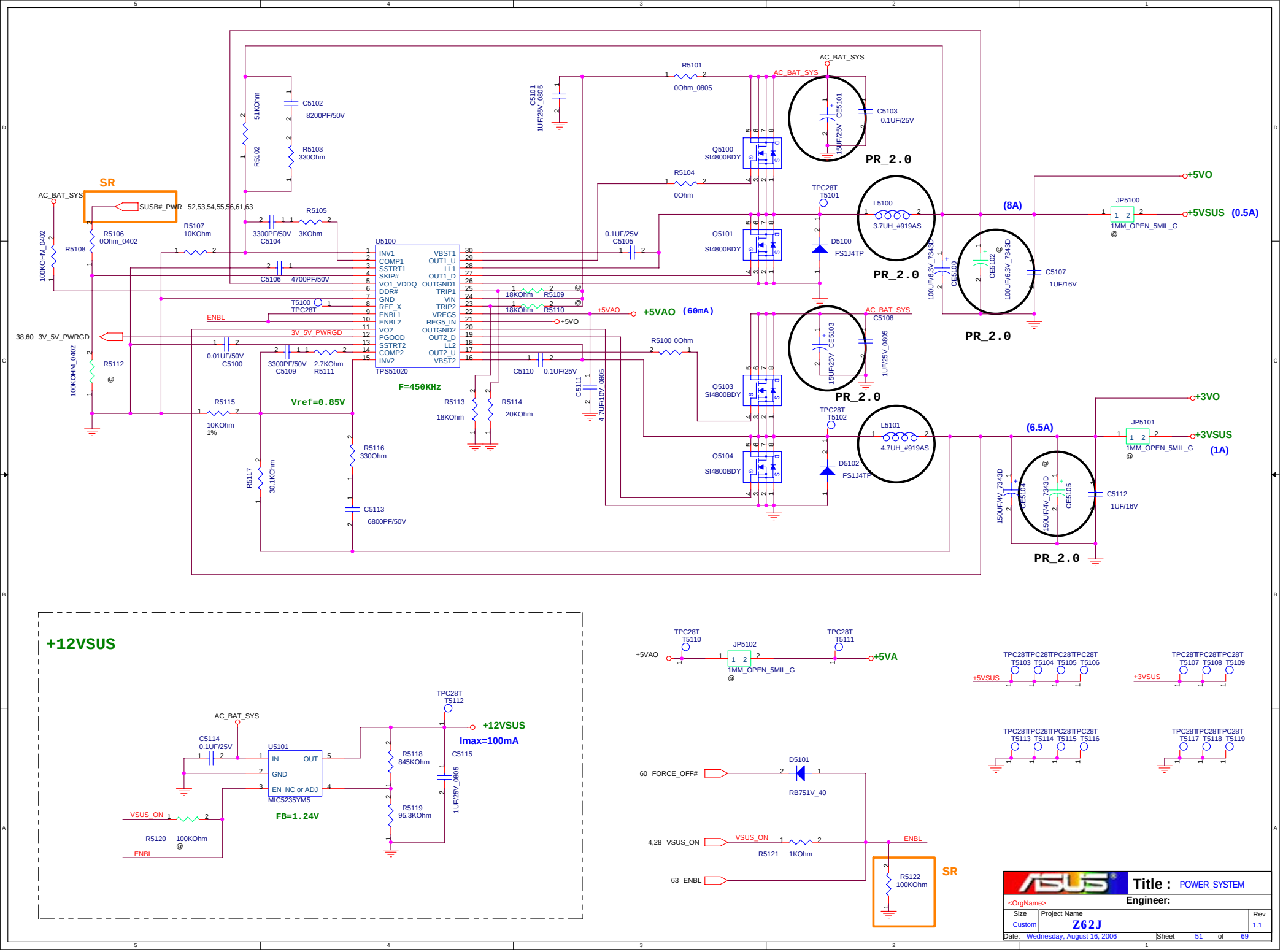
<< Place near left VRAM

VREF=0.4(FBVDDQ) FOR NV44

VREF=0.4(FBVDDQ) FOR NV44

Title :	NV43M VRAM(A)
ASUSTek COMPUTER INC. NB6	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J
Rev: 2.1	
Date: Wednesday, August 16, 2006	Sheet 49 of 69


+1.05VO
AC_BAT_SYS
+VCORE (35A)
Close to Phase 1 Low_side MOSFET
SR
PR_2.0
Merom_0714
for current balence
R5031->4.42K
F=300KHz
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
ER_V2
U5000 ISL6262CRZ
Title : POWER_VCORE
Engineer:
<OrgName>
Project Name Z62J
Size Custom
Rev 1.1
Date: Wednesday, August 16, 2006
Sheet 50 of 67



ASUS

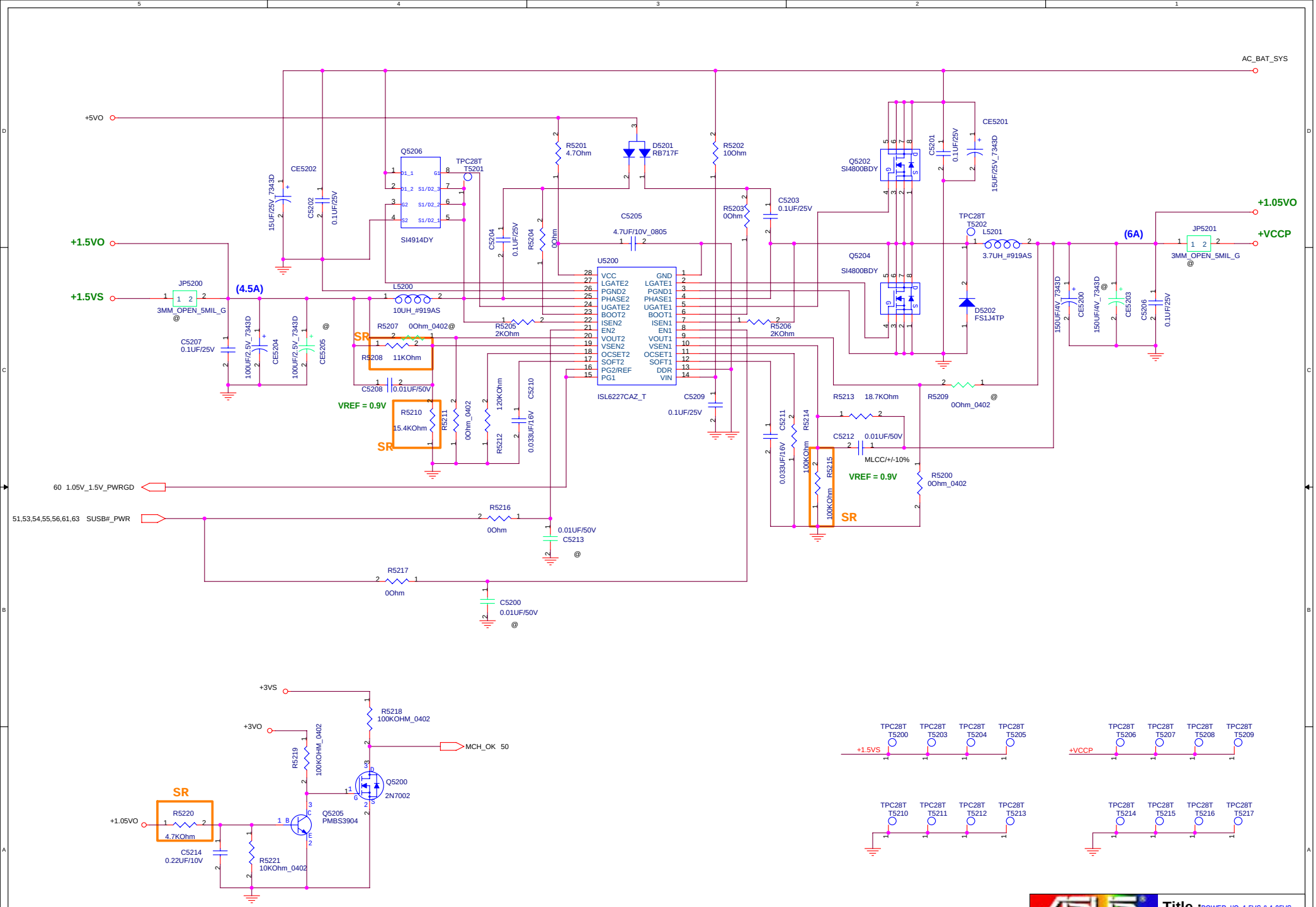
Title : POWER_SYSTEM

<OrgName>

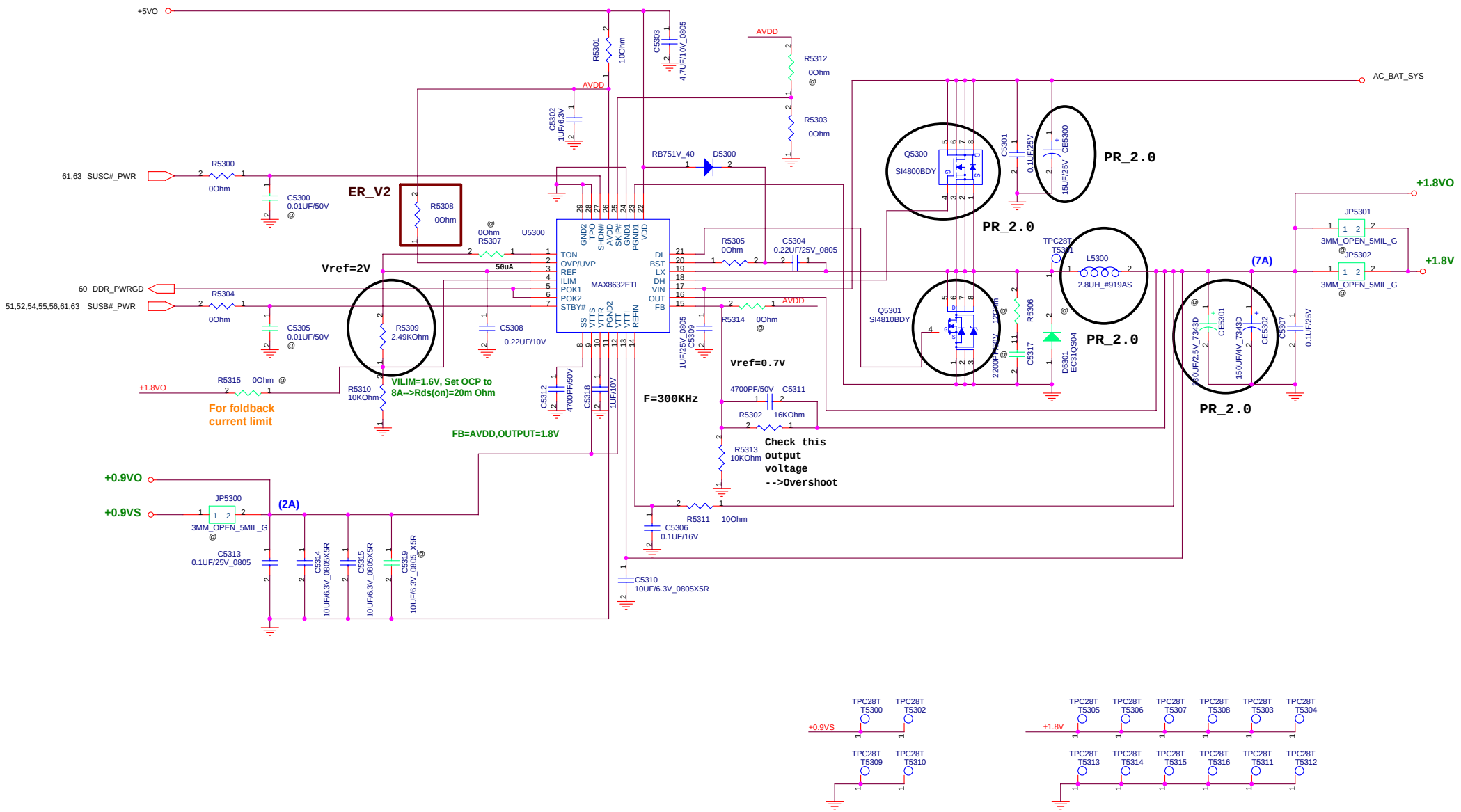
Engineer:

Size	Project Name	Rev
Custom	Z62J	1.1

Date: Wednesday, August 16, 2006 Sheet 51 of 69

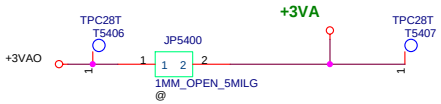


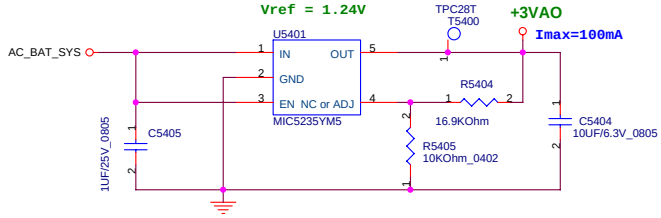
Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 52 of 69	



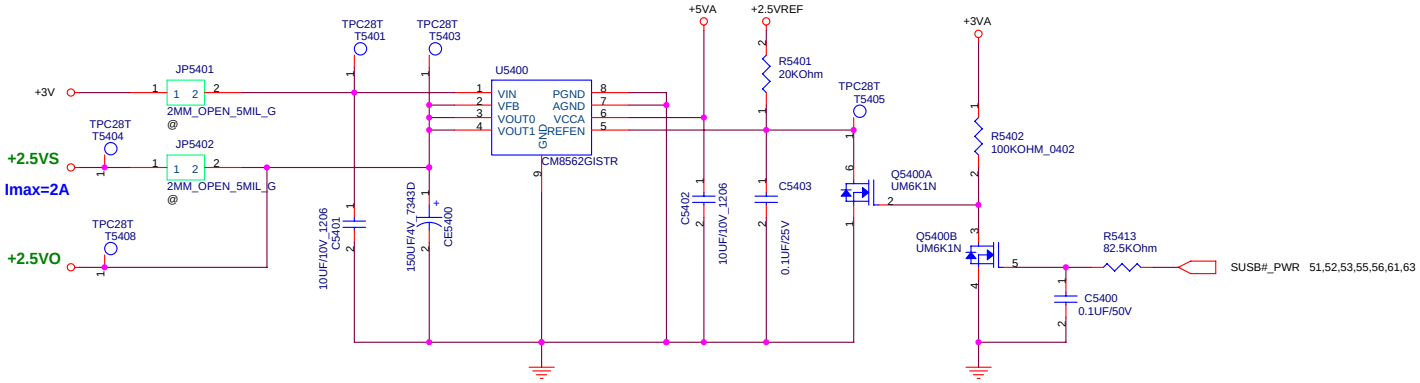
Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 53 of 69	

+3VA0

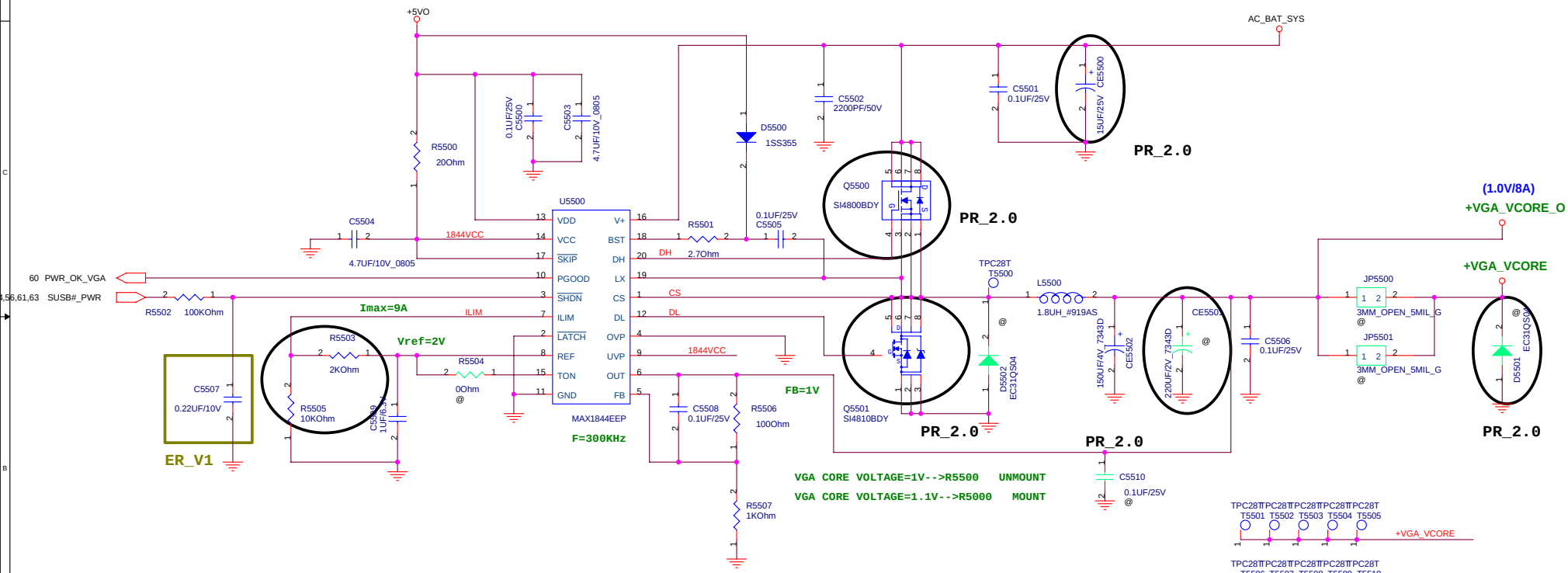




+2.5VS

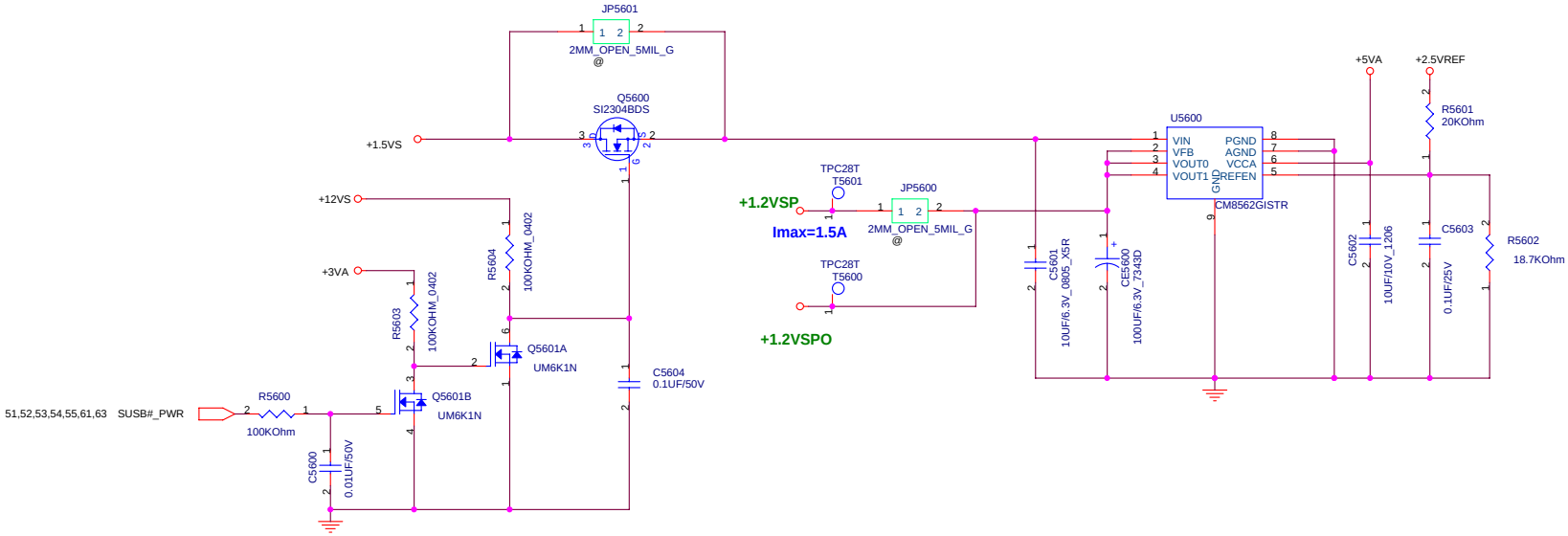


Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 54 of 69	

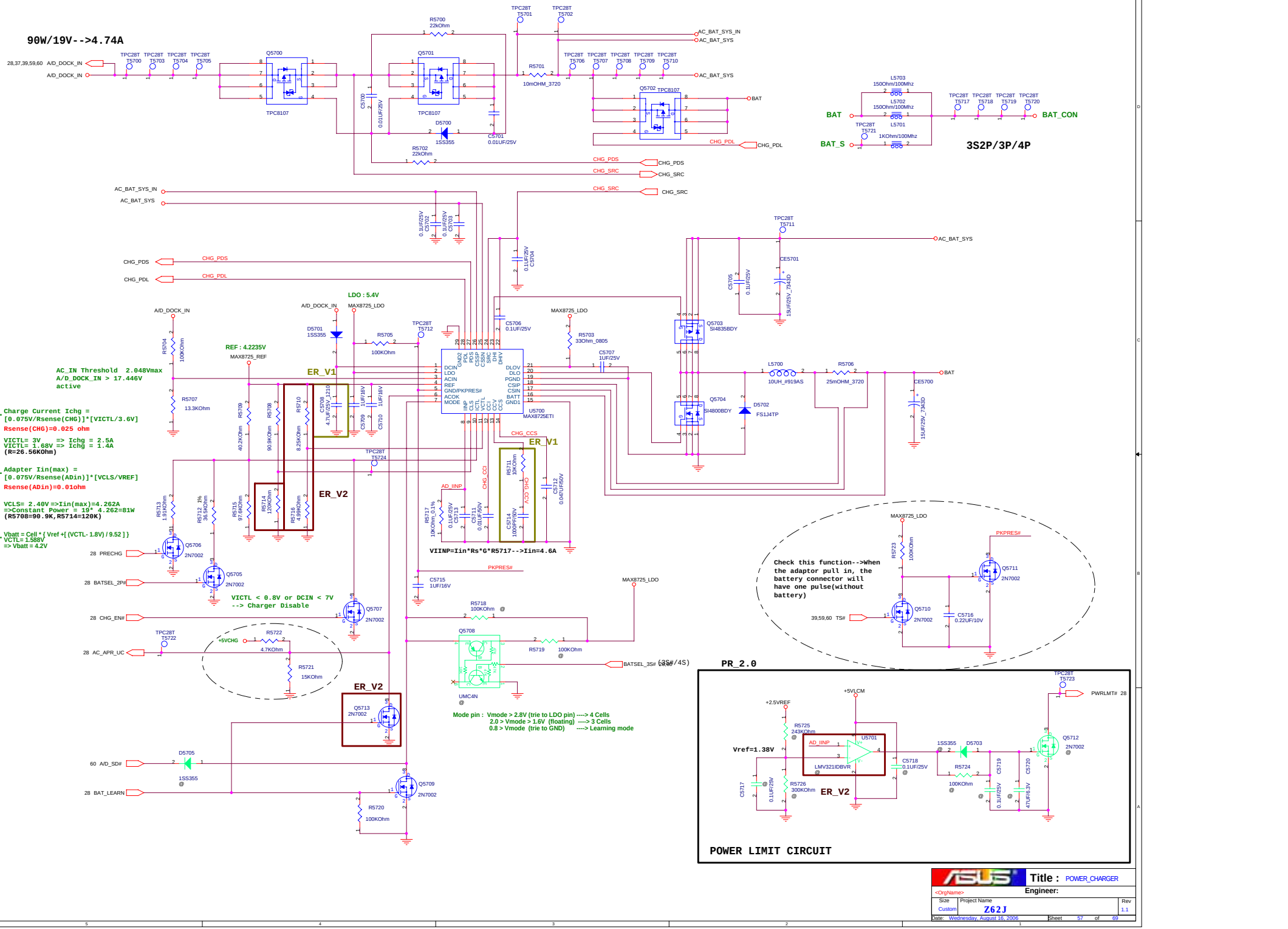


Title: POWER_VGA_CORE		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 55 of 69	

+1.2VSP



ASUS	Title : POWER_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 56 of 69	


90W/19V-->4.74A
AC_IN Threshold 2.048Vmax
A/D_DOCK_IN > 17.446V
active
1. Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
(R=26.56KOhm)
2. Adapter Iin(max) =
[0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.01ohm
VCLS= 2.40V=>Iin(max)=4.262A
=>Constant Power = 19* 4.262=81W
(R5708=90.9K,R5714=120K)
3. Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V
LDO : 5.4V
REF : 4.2235V
ER_V1
ER_V2
VICTL < 0.8V or DCIN < 7V
--> Charger Disable
VIINP=Iin*Rs*G*R5717-->Iin=4.6A
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
Check this function-->When the adaptor pull in, the battery connector will have one pulse(without battery)
3S2P/3P/4P
PR_2.0
POWER LIMIT CIRCUIT
Vref=1.38V
Title : POWER_CHARGER
Engineer:
Project Name Z62J
Rev 1.1
Date: Wednesday, August 16, 2006
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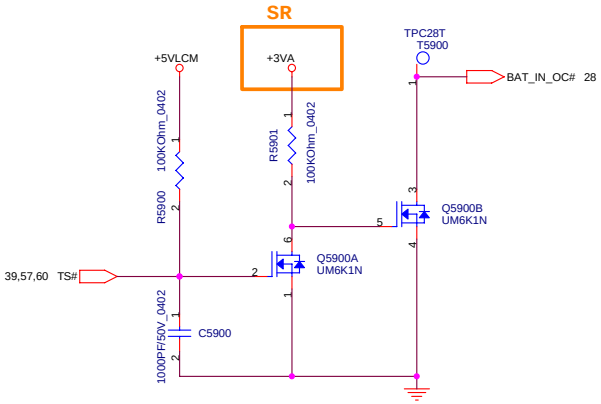
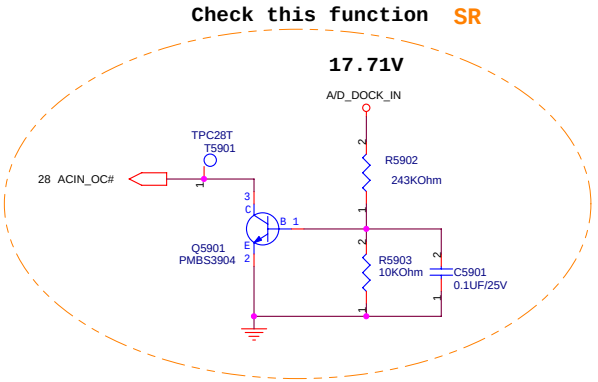
Title :	POWER_PIC
<OrgName>	Engineer:
Size: Custom	Project Name: Z62J
Rev: 1.1	
Date: Wednesday, August 16, 2006	Sheet 58 of 69

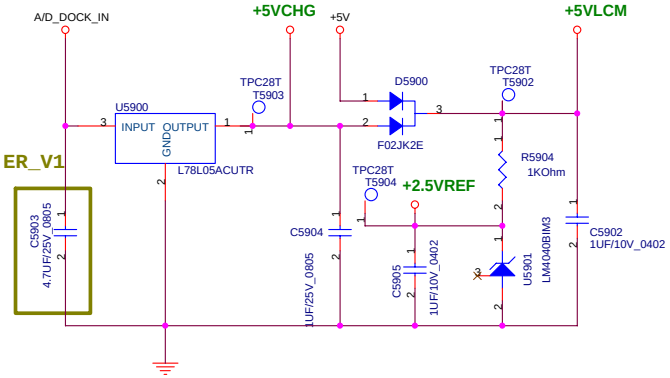
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



Title : POWER_DETECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
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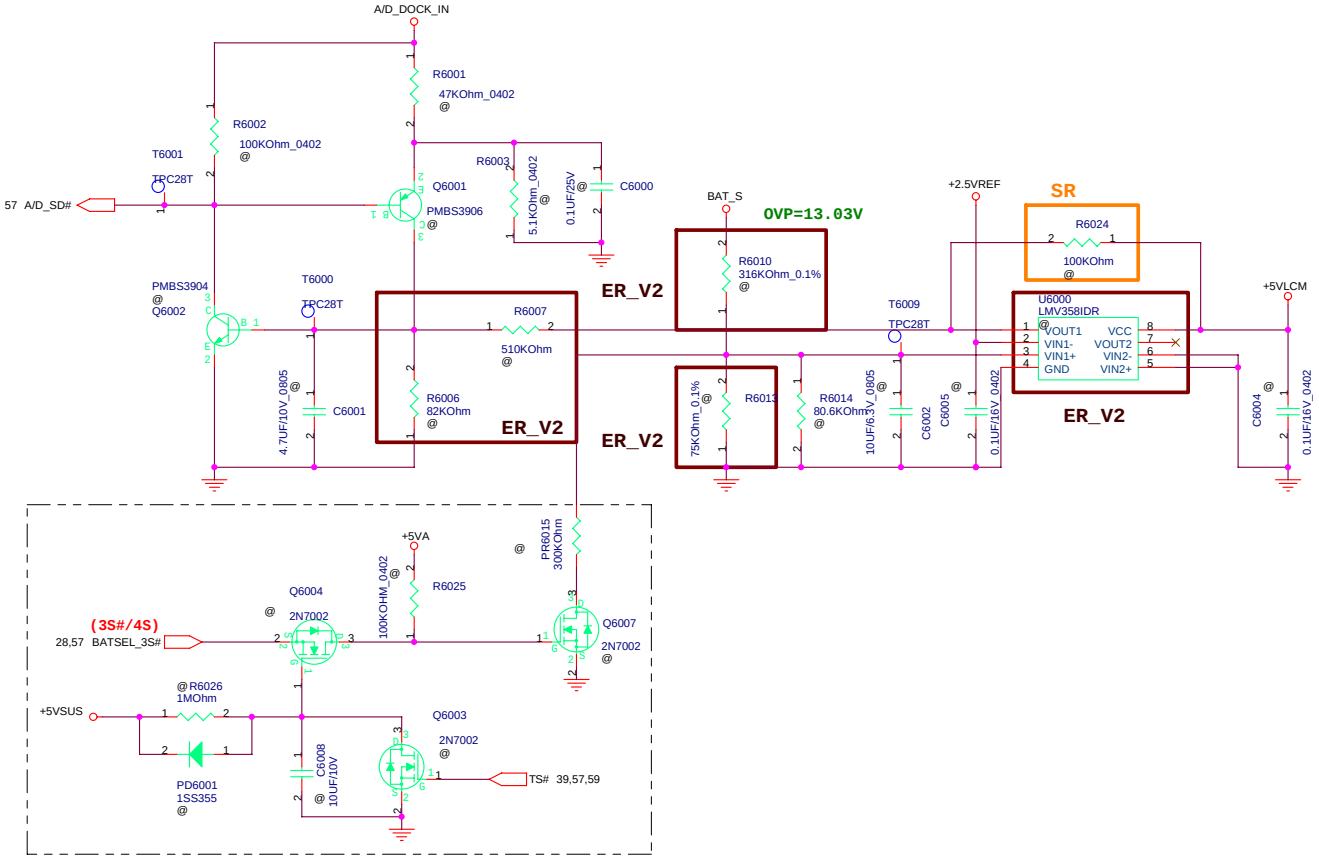
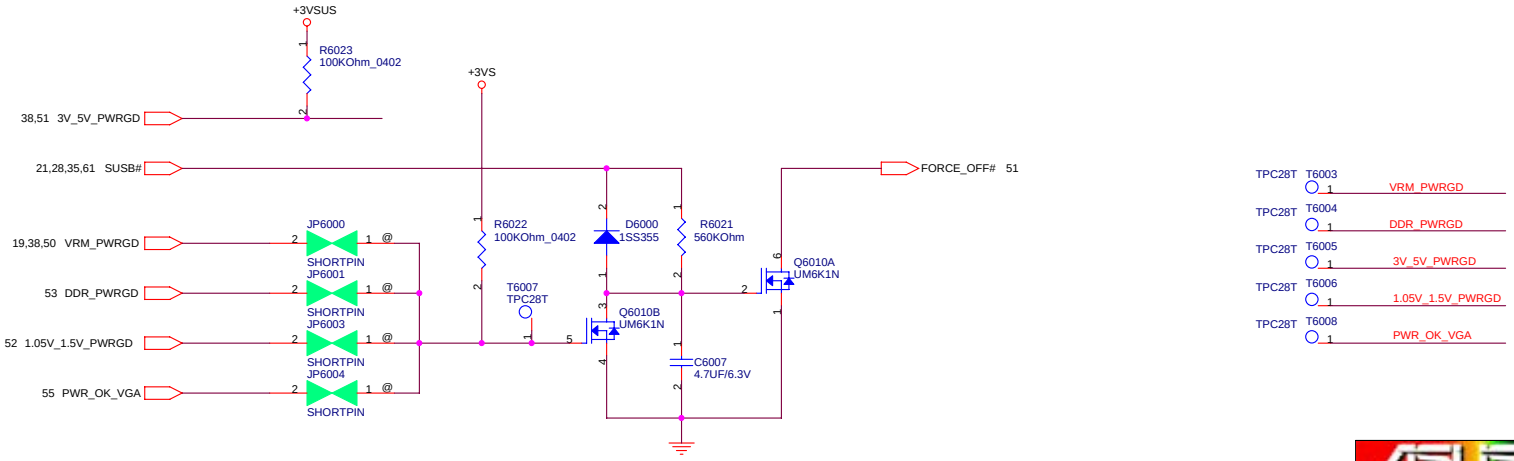
BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
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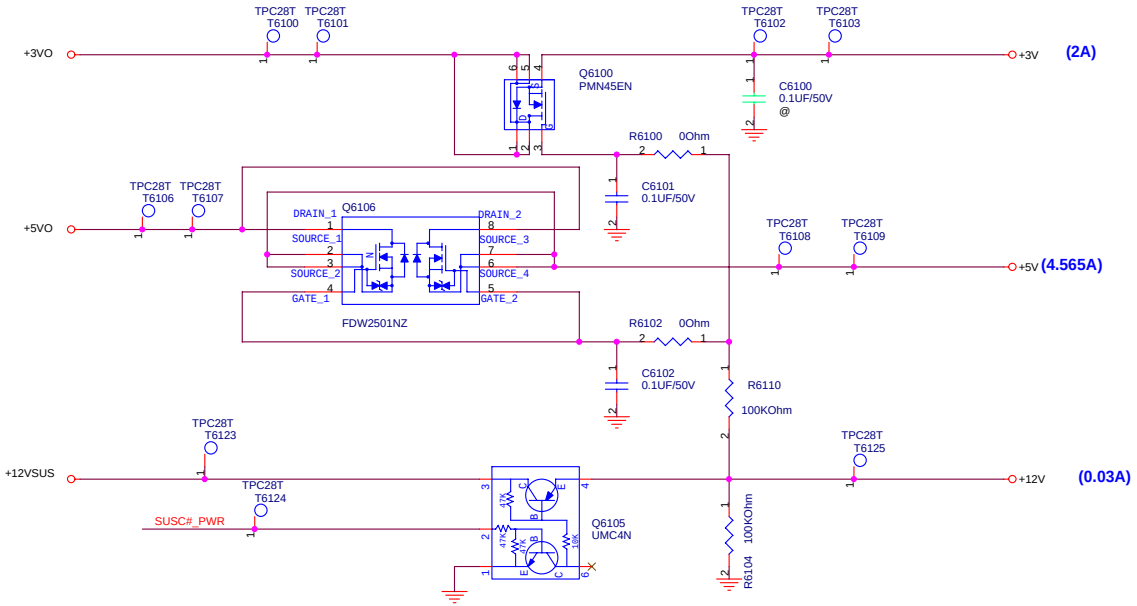
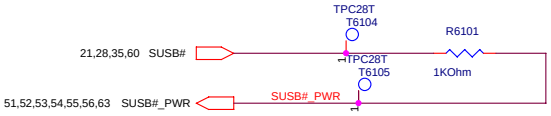
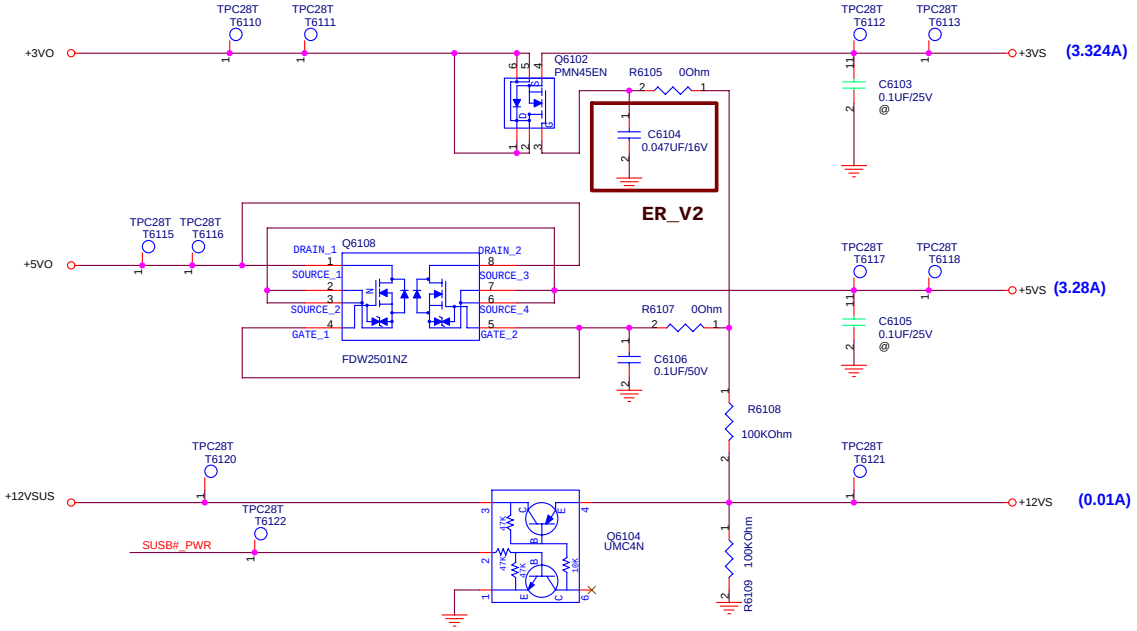
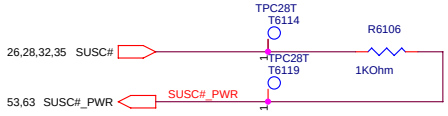
SUSC#_PWR POWER

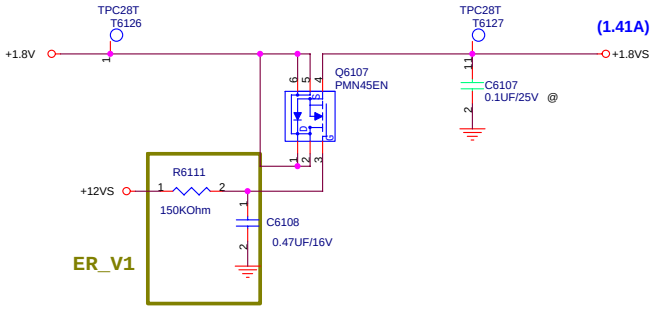




SUSB#_PWR POWER







ASUS

Title : POWER_LOAD SWITCH

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z62J	1.1

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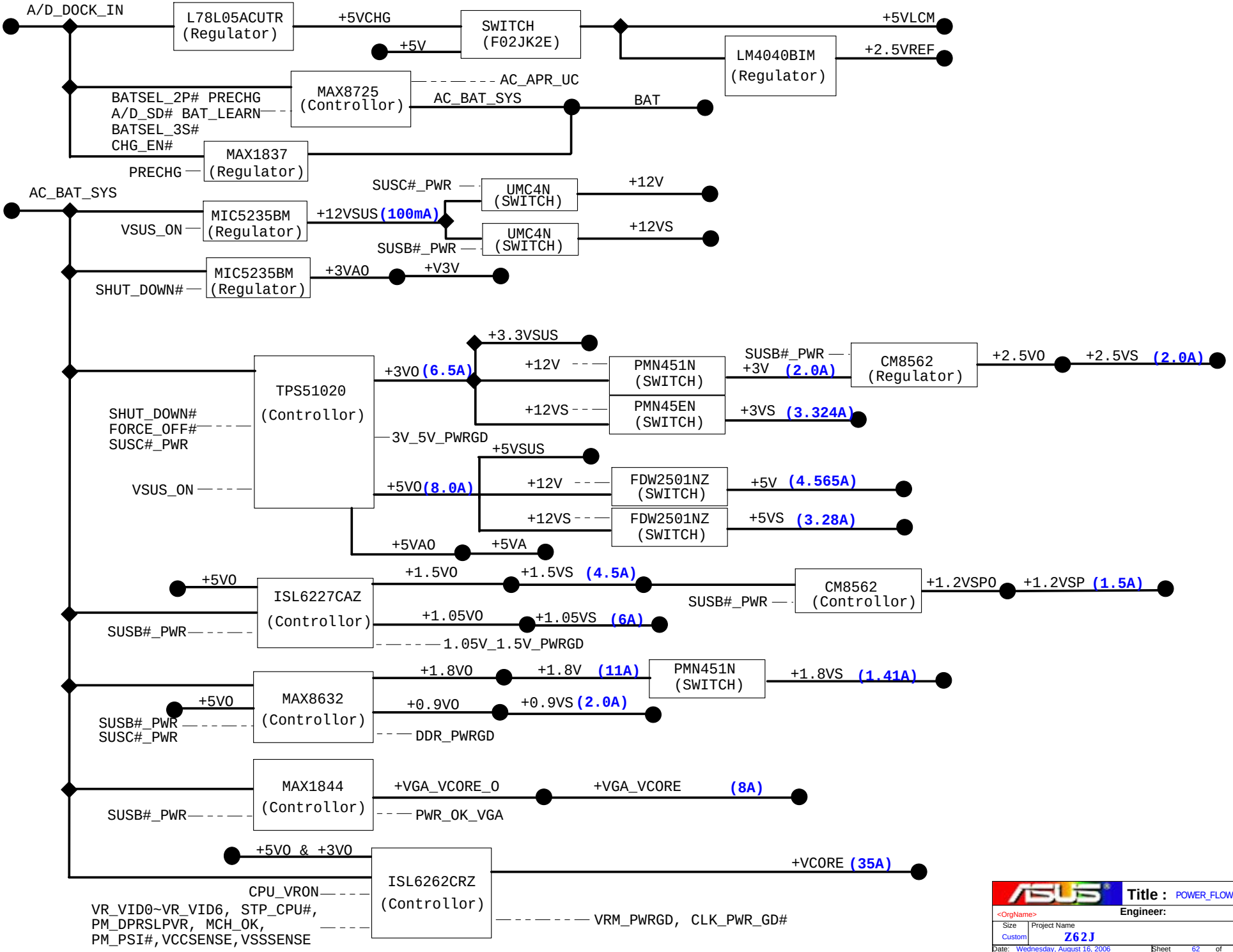


Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 62 of 69	

AC_BAT_SYS → AC_BAT_SYS 12,50,51,52,53,54,55,57

+3VA → +3VA 4,12,20,22,28,38,54,56,59

+5VA → +5VA 51,54,56,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,61

+3VSUS → +3VSUS 18,19,20,24,28,32,35,36,37,38,51,60

+5VSUS → +5VSUS 20,36,51,60

+3V → +3V 18,19,24,26,29,30,31,32,35,40,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,17,19,20,21,22,24,25,26,27,28,29,35,38,42,43,45,46,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,34,35,61

+12VS → +12VS 12,13,22,35,37,56,61

+5V → +5V 12,13,16,22,30,31,34,35,36,37,40,59,61

+5VS → +5VS 4,13,19,20,21,22,27,28,35,36,37,46,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,35,44,46,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,16,35,53,61

+1.8VS → +1.8VS 35,44,47,48,49,61

+0.9VS → +0.9VS 16,35,47,53

BAT → BAT 28,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 57,59,60

+2.5VREF → +2.5VREF 54,56,57,59,60

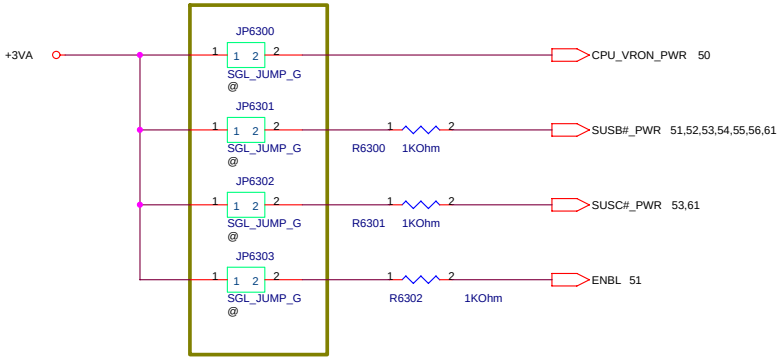
+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 39,57

+VGA_VCORE → +VGA_VCORE 42,55

+1.2VSP → +1.2VSP 35,42,47,56

FOR POWER TEST



ER_V1

Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z62J	Rev: 1.1
Date: Wednesday, August 16, 2006	Sheet 63 of 69	

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date

R2.0

Item	Before	After	Reason	Owner	Date

ASUS

Title : POWER_HISTORY

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z62J	2.0

Date: Wednesday, August 16, 2006 Sheet 64 of 69

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (TV)	AD18	0	H,G

Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A2)	DDR SOCKET2
ICH7-M	MINI_CARD		Wireless_LAN

ICH7-M GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 0	INPUT	PM_BMBUSY#				+3VS
GPIO 1		PCI_REQ#5				+3VS
GPIO 2		PCI_INTE#				+3VS
GPIO 3		PCI_INTF#				+3VS
GPIO 4		PCI_INTG#				+3VS
GPIO 5		PCI_INTH#				+3VS
GPIO 6						+3VS
GPIO 7	INPUT	RF_OFF_SW#	**LOW**			+3VS
GPIO 8	INPUT	EXTSMI#	LOW			+3VSUS
GPIO 9	INPUT	SATA_DET#0	**LOW**			+3VSUS
GPIO 10						+3VSUS
GPIO 11	INPUT	SMBALERT#				+3VSUS
GPIO 12	INPUT	KB_SCI#	**LOW**			+3VSUS
GPIO 13	INPUT	SIO_SMI#	LOW			+3VSUS
GPIO 14	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 15	OUTPUT	CB_SD#	**LOW**	HIGH	LOW	+3VSUS
GPIO 16		DPRSLPVR				+3VS
GPIO 17		GNT#5	PULL-DOWN:Boot BIOS destination select			+3VS
GPIO 18	OUTPUT	STP_PCI#				+3VS
GPIO 19	OUTPUT	PWRLED_1HZ	1 Hz	1 Hz	Off	+3VS
GPIO 20	OUTPUT	STP_CPU#				+3VS
GPIO 21		SATA0GP				+3VS
GPIO 22		REQ4#				+3VS
GPIO 23		LDRQ1#				+3VS
GPIO 24						+3VSUS
GPIO 25	OUTPUT	BT_LED_EN#	**LOW**	HIGH	Driven	+3VSUS
GPIO 26	INPUT	PCB_ID2	Default : 0			+3VSUS
GPIO 27	INPUT	PCB_ID1	Default : 0			+3VSUS
GPIO 28	INPUT	PCB_ID0	Default : 0			+3VSUS
GPIO 29		USB_OC5#				+3VSUS
GPIO 30		USB_OC6#				+3VSUS
GPIO 31		USB_OC7#				+3VSUS
GPIO 32	IN/OUTPUT	PM_CLKRUN#				+3VS
GPIO 33		AZ_DOCK_EN#				+3VSUS
GPIO 34		AZ_DOCK_RST#				+3VS
GPIO 35		SATACLKREQ#				+3VS
GPIO 36		SATA2GP				+3VS
GPIO 37						+3VS
GPIO 38	OUTPUT	BT_ON#	**LOW**	LOW	Off	+3VS
GPIO 39	OUTPUT	WLAN_ON#	**LOW**	LOW	Off	+3VS
GPIO 48		GNT#4	PULL-DOWN:Boot BIOS destination select			+3VS
GPIO 49	OUTPUT	H_PWRGD				+Vccp

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

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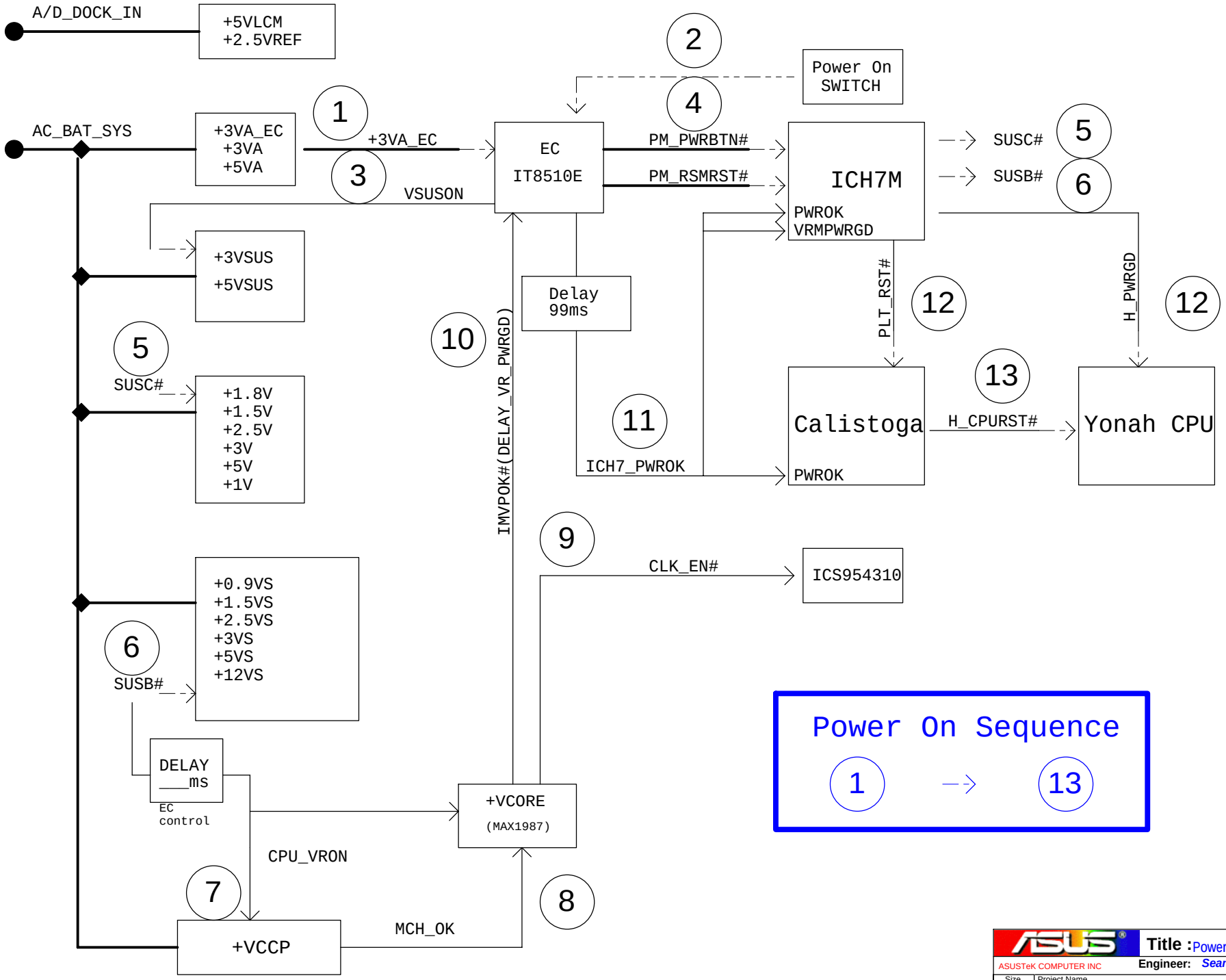
Title :	History
ASUSTek Computer INC. NB1	Engineer: Sean1 Chou
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 66 of 69



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Sean1 Chou		
Size: Custom	Project Name: Z62J		Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 67 of 69		

REVISION LIST

R1.0 2005/10/06

R1.1 2005/10/18

No 1:P39, EMI spring footprint modified

No 2:P32, Connect V_DAC bias to GLAN terminator RC: for PortBar bias issue

No 3:P43, unmount R4308 and mount R4302

No 4:P48, R4801 should change P/N to 30.1 Ohm

No 5:P12, connect the pin 30 of CON25 to +3VS

No 6:P12, mount L107 & delete L64 path; P46: add T4604

No 7:P27, ODD pin 53,54 NC

No 8:P28, delete GPA1 CHG_FULL_LED# - Bug 8

No 9:P36, Delete Q3600,R3600,R1255, Change LED5 to single color to remove charge full LED function. Connect power to +5VCHG avoid faulty GPIO control.

No10:P36, Re-assign Launch board connector pin define for correct function button

No11:P35, Re-assign Launch board pin define for correct function button

No12:P28, Add EXPLORER# instant key due to SPEC change

No13:P17, mount R206

No14:P31, delete SD_WP inverter(Q7000,R7083) - Bug 3, Bug4

No15:P23, Pre-Amp unmount - Bug 9

No16:P26, Change R2603,R2606 to 33 ohm 0603 part to avoid overshoot/undershoot

No17:P14,15, Change M_ODT[0..3]# to make correct rank ODT function

No18:P26, Delete R1059,R1060,R1061,Q141,Q142,C939,C940,L93 for BT part reduce

No19:P49, VRAM from 2 to 4

No20:P22, Change J2 connector by ID/ME's request

No21:P28, Change Con11 connector by Intel Request and redefine key matrix.

No22: Change U1's footprint to match Green Part rules. change U4,U6 part number for B0 QS samples.

No23: P24, TPM circuits modified.

No24: P7, Add R703 to support C4E Fast exist latency

No25: P39, Add R4000,R4001 unmount part to reserve pull low

No26:Green parts, JP4,7,5100,5101,5102,5400

No27: P28,38, Change R1047,R1269,R4620 to 100K ohm to reduce power consumption

No28: P28, change X8 to ROHS compliant parts.

No29: P4, P46, delete R35 & R4619; unmount Q5,Q4600; add R7091,R7092 because of no leakage current

No30: P5, P29, (1)mount C401 and change to 10pF (2) change R72 to 39ohm, (3)R77,R79,R83 change to 47Ohm. for fine clock, (4)R81 to 27Ohm

No31: P22, Change the HP mute circuits to behind decoupling capacitors for dispelling POP noise.

No32: P37, mount C1095,C1096,C1097 for EMI solution of PortBar3

No33: P46, unmount VGA thermal sensor circuits.

No34: P43, Memory strap modified

No35: P46, R4617 is changed from 300 ohm to 270 ohm to meet the 27FIX level.

No36: P27, Con10 symbol changed and pin 53,54 NC for NPTH

No37: P22, change CN1 to C2201~C2204

No38: P39, U7104~7107 change

No39: P12, P25, unmount R1201,R1202,C350,C351

No40: P39, J6 footprint changed

No41: P19, PCB_ID definition.

No42: P17, X3 capacitors change to 15 pF for accurate timing.

No43: P3, unmount CE1,CE4

No44: P22, change L31~L34 P/N

R1.2 2005/11/29

No45:P37, R818 pin1 connect to +3VSUS to solve S4 WOL fail issue

No46:P13, U80 pin16 connect to +5VSUS to solve S4 WOL fail issue

No47:P38,Delete Q135, R1051, R1054, D82, D84, C934 for reduce component

No48:P28,35,36, Delete EXPLORER# key and add back P4G instant key for PM's request

No49:P19, R156 pin1 change to +3V to meet Check list

No50:P23, mount Mic Pre-Amp for micphone volume & change C2305 to 1uF for cutoff freq. fine tune.

No51:P48, R4801 change to 40.2 Ohm for GDDR2 setting

No52: change U4 to 02G010009205, U6 to 02G010007741 for new P/N

No53: P22, add R2201,R2202 to reserve gain modification.

No54:P2,28, Add Q200 to support THRO_CPU function on to PROCHOT#.

No55:P36 : R3700 and LED5 change to connect +5VSUS to solve Battery low blinking indication no function issue.

No56:P7, Set R108 to unmount component
P28, Set D2800 to unmount component because EC do not support Watchdog

No57: P39, add U7108 for EMI spring requirement

No58: P46, add back thermal sensor

No59: P5, clock gen version changes to ICS954310CGLFT

No60: P47, add VGA termination for high speed.

No61: P12, change C756 to 0.1uF to meet LCD power sequence

No62: change all 11G232110316320 MLCC 0.01UF/10V (0402)X7R 10% to 11G232110311320 MLCC 0.01UF/16V (0402) X7R 10%

No63: P21,23, change Pre-Amp circuits because of ADI's suggest.

No64: P28, add 0 ohm at KB for EMI suggestion.

No65: P49, change VRAM from -28 to -25

No66: P32,33,37, modify LAN circuits for PortBar failure issue.

No67: P39, EMI spring footprint changed for indicating direction.

No68: P39, all screw holes except CPU bracket change to Npth.

No69: P39, R4000,R4001 mount for LIBP

No70: P21, SPDIF add a 4.7K ohm to GND

R2.0 2006/01/02

No71: P37, reserving a direct path instead of the PR/MB Lan switch.

No72: P39, changing DC Jack part and circuits for Power team's request

No73: P12, changing R813 to 47Kohm and adding R1200 for white display solution

No74: P37, updating L65 symbol and modifying all ports' properties, including power circuits

No75: P47, add two 0.1uF and unmount all the terminations

No76: P37, unmount switch ralative 3 components, and mount all 2R4P 0ohm

No77: P48, change R4801 to 30.1 OHM back from nVidia(No51)

No78: P28, use capacitors instead of KBC beads for cost down and EMI

No79: P20, 38, add test point T2000, T3800

No80: P31, add MS Duo protect circuits

No81: P22, Change R265,R266 to 30Kohm to meet Speaker's SPEC

No82: P35, change R7000~R7003 to 220 ohm to meet 5ma current

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1
MINIPCI(TV)	PCI_REQ#0

IDSEL

MINIPCI	PCI_AD19
CB&1394	PCI_AD17
10/100	PCI_AD16
MINIPCI(TV)	PCI_AD18

ASUSTeK COMPUTER INC

Title : Revision List

Engineer: Sean1 Chou

Size	Project Name	Rev
Custom	Z62J	2.1

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REVISION LIST (2)

No83: P28, add and reserve R2804, R2805
No84: P46, use GPIO9 to moniter temperture.
No85: P37, delete reseverd analog switch circuits.
No86: delete 0 Ohm:
R195,703,102,2000,462,469,2400,2403,458,2800,347,349,387,391,7084,7085,4202,3903,359,404,466,507,1259,3200,160,206

R2.1 2006/02/23
No87: P42, add 0 ohm back : R4202,R466,R507,R404.
No88: P46, unmount thermal sensor circuits
No89: P33, mount C893, C894 for PR EMI concern
No90: P27, unmount R345, mount R346 for setting CDROM master
No91: P39, H41 change footprint to PHI=6.9 for factory issue.
No92: P35, add +1.2VSP and +1.8VS discharge circuits
No93: P34, add R3400 and unmount R435 and Q47
No94: P2, unmount CE54, CE8, CE19, CE15 and change VCORE 22uF to 10uF
No95: P29,P42, U25 U4200 footpoint change to nb_
No96: P22, R1267, R1268 are from 0 ohm to 22 ohm to fix audio volume bar issue.
No97: P5, unmount R507
No98: P31, change L42 footprint for lower height
No99: P35,P39, H4001,4004,4008,4012,7000,7001 change to NPTH
No100: P12, change C756 to 0.22uF to reduce CMO power off garbage.

post R2.1 2006/05/03
No101: P9, add 150uF on CE8
No102: P36, TP switch change P/N

Z62JM R2.2
change some circuits for Vista and PortBar LAN

Z62JM R2.3 2006/08/09
ER NO1: P22 mute circuits inverted for vista default driver
ER NO2: P22 solve external pop noise, +12VS delay, add C2205 and D2200, and change R270 to 1M ohm
ER NO3: P34, solve external USB power leakage
ER NO4: P9, change 150uF to 330uF for CMOS data lost
ER NO5: P22 solve internal pop noise, R271=470K, C2206=2.2uF

ASUSTeK COMPUTER INC	Title : Revision List (2)	
	Engineer: Sean1 Chou	
Size: Custom	Project Name: Z62J	Rev: 2.1
Date: Wednesday, August 16, 2006	Sheet 69 of 69	