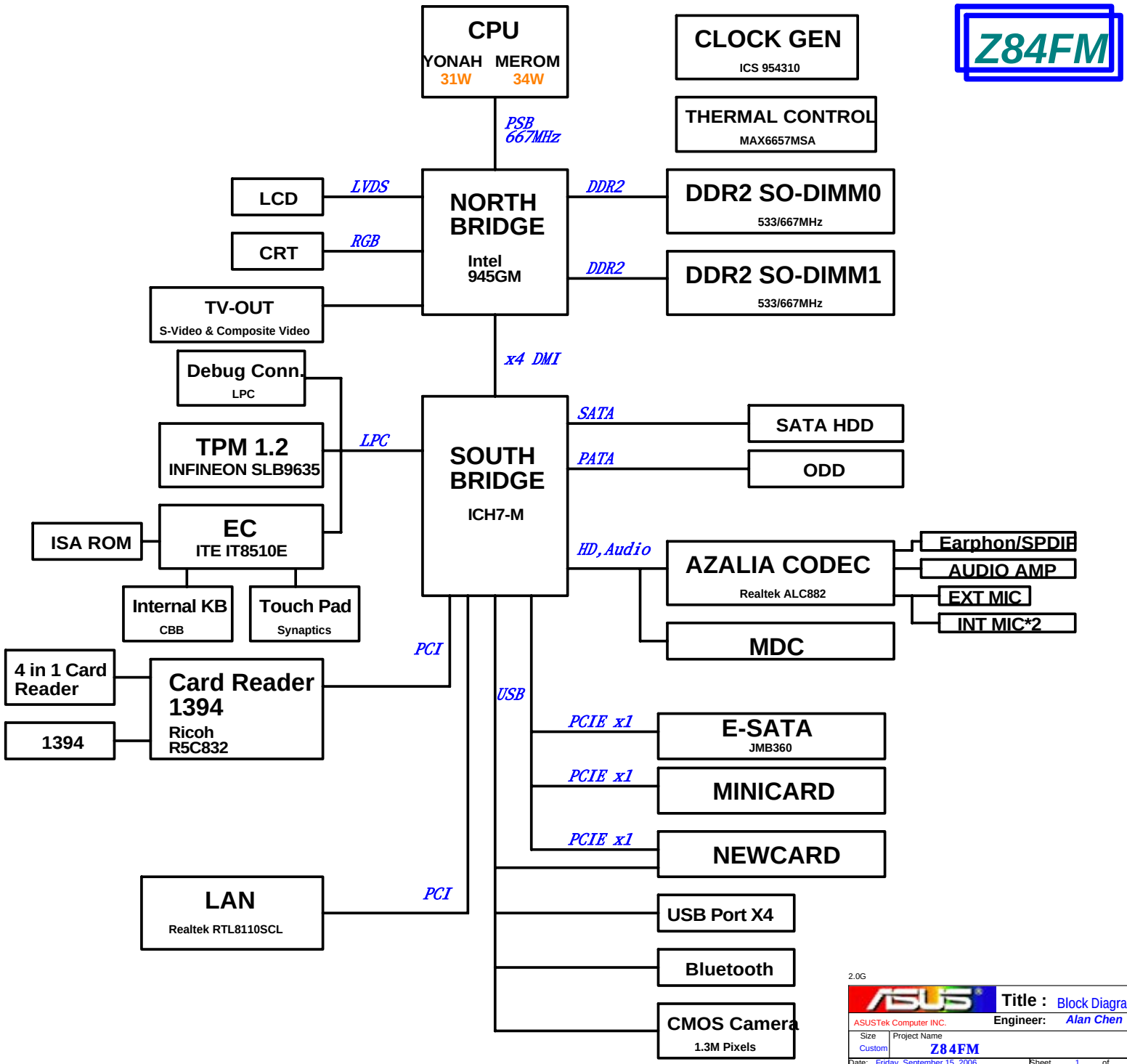


2.0G

Title : Block Diagram

ASUSTek Computer INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 1 of 57

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

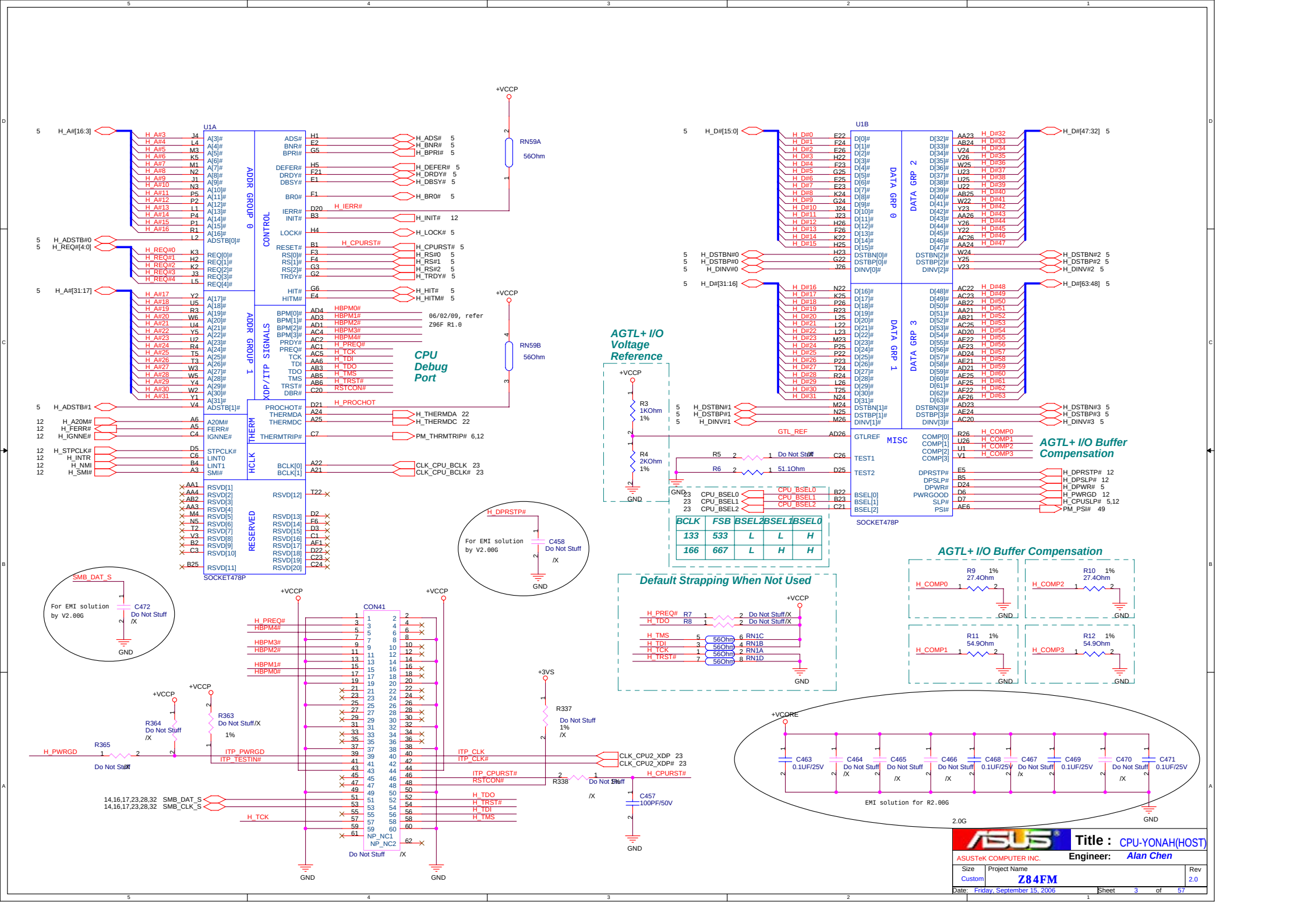
2.0G

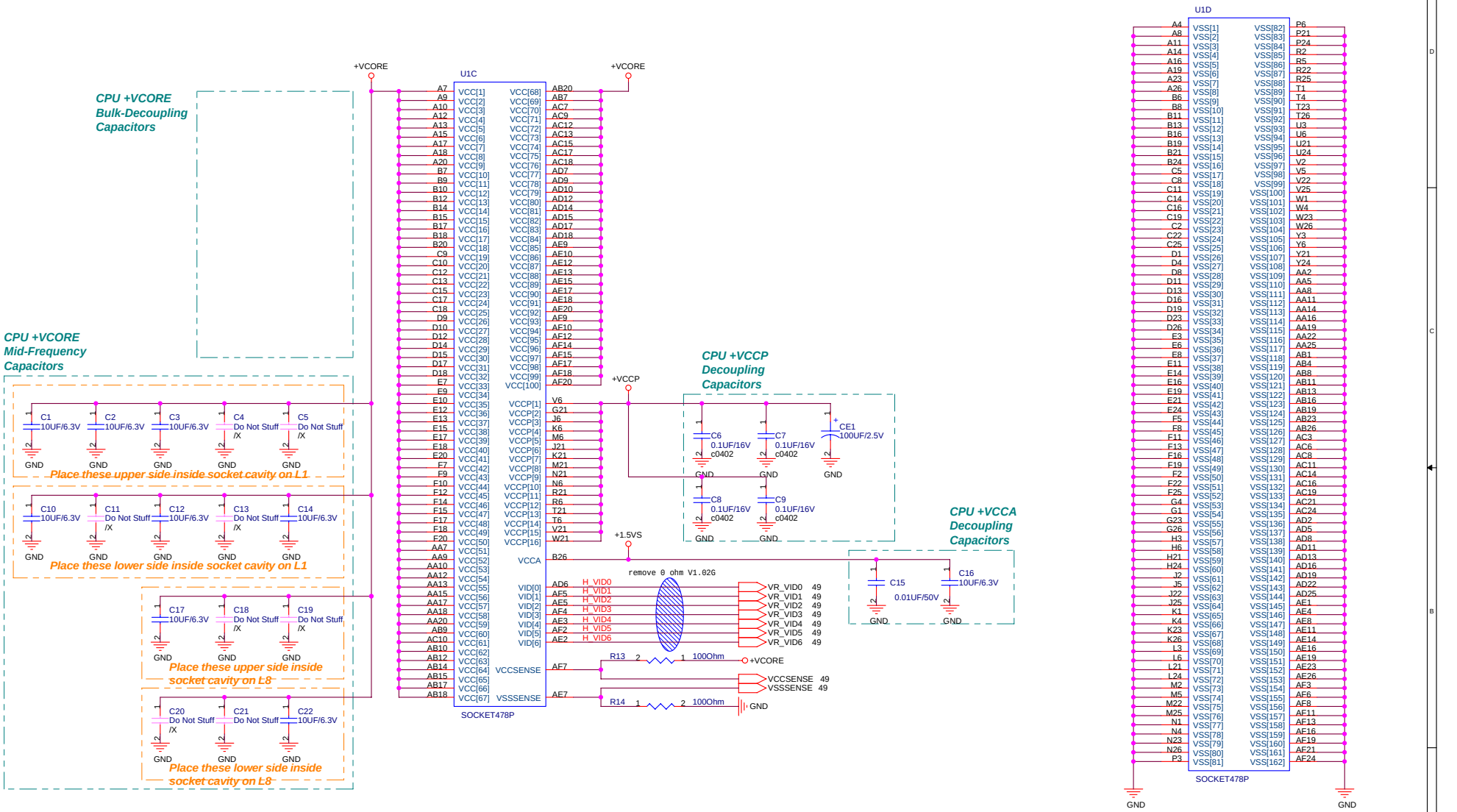
Title : <Title>

ASUSTek Computer INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 2 of 57

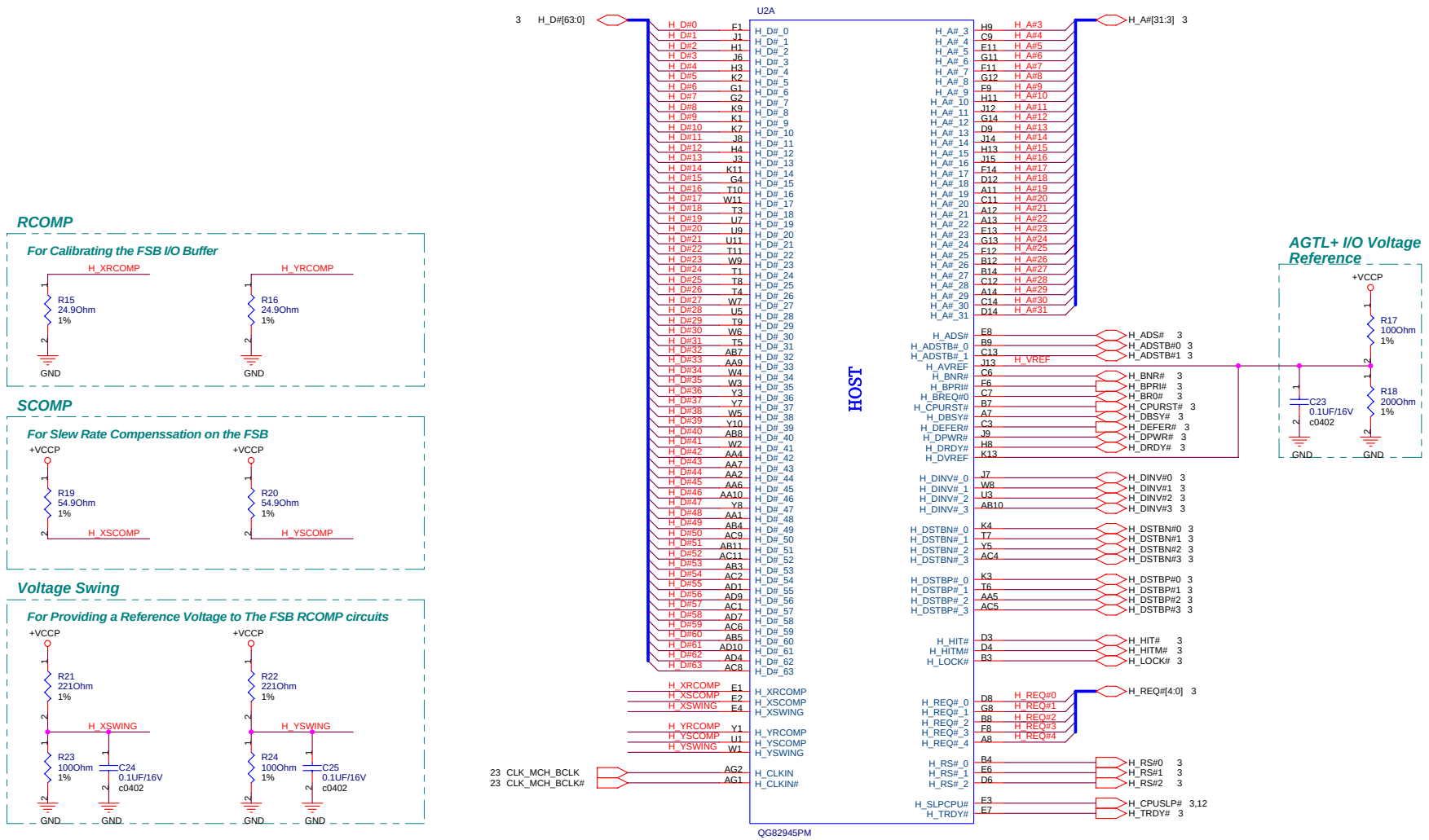

U1A
U1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478P
CPU Debug Port
AGTL+ I/O Voltage Reference
AGTL+ I/O Buffer Compensation
Default Strapping When Not Used
CON41
+VCCP
+VCORE
+3VS
GND
RN59A
56Ohm
RN59B
56Ohm
H_A#[16:3]
H_A#[31:17]
H_REQ#[4:0]
H_ADSTB#0
H_ADSTB#1
H_D#[15:0]
H_D#[31:16]
H_D#[47:32]
H_D#[63:48]
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR#
H_INIT#
H_LOCK#
H_CPURST#
H_RS#0
H_RS#1
H_RS#2
H_TRDY#
H_HIT#
H_HITM#
H_PREQ#
H_TCK
H_TDI
H_TDO
H_TMS
H_TRST#
RSTCON#
H_PROCHOT
H_THERMDA
H_THERMDC
PM_THRMTRIP# 6,12
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
CLK_CPU_BCLK 23
CLK_CPU_BCLK# 23
06/02/09, refer Z96F R1.0
GTL_REF
R3 1KOhm 1%
R4 2KOhm 1%
R5 Do Not Stuff/X
R6 51.1Ohm
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
133 | 533 | L | L | H
166 | 667 | L | H | H
H_COMP0
H_COMP1
H_COMP2
H_COMP3
R9 1% 27.4Ohm
R10 1% 27.4Ohm
R11 1% 54.9Ohm
R12 1% 54.9Ohm
H_DPRSTP# 12
H_DPSLP# 12
H_DPWR# 5
H_PWRGD 12
H_CPUSLP# 5,12
PM_PSI# 49
H_PREQ# R7 Do Not Stuff/X
H_TDO R8 Do Not Stuff/X
H_TMS 56Ohm RN1C
H_TDI 56Ohm RN1B
H_TCK 56Ohm RN1A
H_TRST# 56Ohm RN1D
SMB_DAT_S
SMB_CLK_S
C458 Do Not Stuff /X
C472 Do Not Stuff /X
R363 Do Not Stuff/X 1%
R364 Do Not Stuff /X
R365 Do Not Stuff /X
R337 Do Not Stuff 1% /X
R338 Do Not Stuff /X
C457 100PF/50V
C463 0.1UF/25V
C464 Do Not Stuff /X
C465 Do Not Stuff /X
C466 Do Not Stuff /X
C468 0.1UF/25V
C467 Do Not Stuff /X
C469 0.1UF/25V
C470 Do Not Stuff /X
C471 0.1UF/25V
EMI solution for R2.00G
2.0G
For EMI solution by V2.00G
ITP_PWRGD
ITP_TESTIN#
ITP_CLK
ITP_CLK#
ITP_CPURST#
RSTCON#
CLK_CPU2_XDP 23
CLK_CPU2_XDP# 23
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size: Custom
Project Name: Z84FM
Rev: 2.0
Date: Friday, September 15, 2006
Sheet 3 of 57



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

2.0G

ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 4 of 57	



2.0G

Title : NB-945GM(HOST)

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 5 of 57

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — 1 — R25 /X — 2 — Do Not Stuff — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — 1 — R26 /X — 2 — Do Not Stuff — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — 1 — R27 /X — 2 — Do Not Stuff — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — 1 — R30 — 2 — 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — 1 — R31 /X — 2 — Do Not Stuff — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — 1 — R34 /X — 2 — Do Not Stuff — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+2.5VS

MCH_CFG_18 — 1 — R35 /X — 2 — Do Not Stuff

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — 1 — R37 /X — 2 — Do Not Stuff — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

+2.5VS

MCH_CFG_19 — 1 — R38 /X — 2 — Do Not Stuff

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

U2B

RSVD: T32 RSVD_1, R32 RSVD_2, F3 RSVD_3, E7 RSVD_4, AG11 RSVD_5, AF11 RSVD_6, H7 RSVD_7, J19 RSVD_8, K30 TV_DCONSEL_0, J29 TV_DCONSEL_1, A41 RSVD_11, A35 RSVD_12, A34 RSVD_13, D28 RSVD_14, D27 RSVD_15

CFG: 23 MCH_BSEL0 → K16 CFG_0; 23 MCH_BSEL1 → K18 CFG_1; 23 MCH_BSEL2 → J18 CFG_2; F18 CFG_3, E15 CFG_4, F15 CFG_5 (MCH_CFG_5), E18 CFG_6, D19 CFG_7 (MCH_CFG_7), D16 CFG_8, G16 CFG_9 (MCH_CFG_9), E16 CFG_10 (MCH_CFG_10), D15 CFG_11 (MCH_CFG_11), G15 CFG_12, K15 CFG_13, C15 CFG_14, H16 CFG_15 (MCH_CFG_15), G18 CFG_16 (MCH_CFG_16), H15 CFG_17, J25 CFG_18 (MCH_CFG_18), K27 CFG_19 (MCH_CFG_19), J26 CFG_20

PM: +3VS; 1 T3 Do Not Stuff; 14 PM_BMBUSY# → G28 PM_BMBUSY#; R32 2 10KOhm 1 c0402 PM_EXTTS# 0 → F25 PM_EXTTS#_0; R33 2 10KOhm 1 c0402 PM_EXTTS# 1 → H26 PM_EXTTS#_1; 3,12 PM_THRMTRIP# → G6 PM_THRMTRIP#; 14,35,49,54 VRM_PWRGD → AH33 PWROK; 13,14,28,32 BUF_PLT_RST# — R36 1 — 2 100Ohm RST_IN_MCH# → AH34 RSTIN#

MISC: H28 SDVO_CTRLCLK, H27 SDVO_CTRLDATA, 13 MCH_ICH_SYNC# → K28 ICH_SYNC#, H32 CLK_REQ#

NC: D1, C41, C1, BA41, BA40, BA39, BA3, BA2, BA1, B41, B2, AY41, AY1, AW41, AW1, A40, A4, A39, A3 → NC0 … NC18

QG82945PM

DDR MUXING:

SM_CK_0 AY35, SM_CK_1 AR1, SM_CK_2 AW7, SM_CK_3 AW40 → M_CLK_DDR0 16, M_CLK_DDR1 16, M_CLK_DDR2 17, M_CLK_DDR3 17

SM_CK#_0 AW35, SM_CK#_1 AT1, SM_CK#_2 AY7, SM_CK#_3 AY40 → M_CLK_DDR#0 16, M_CLK_DDR#1 16, M_CLK_DDR#2 17, M_CLK_DDR#3 17

SM_CKE_0 AU20, SM_CKE_1 AT20, SM_CKE_2 BA29, SM_CKE_3 AY29 → M_CKE0 16,18, M_CKE1 16,18, M_CKE2 17,18, M_CKE3 17,18

SM_CS#_0 AW13, SM_CS#_1 AW12, SM_CS#_2 AY21, SM_CS#_3 AW21 → M_CS#0 16,18, M_CS#1 16,18, M_CS#2 17,18, M_CS#3 17,18

SM_OCDCOMP_0 AL20, SM_OCDCOMP_1 AF10

SM_ODT_0 BA13, SM_ODT_1 BA12, SM_ODT_2 AY20, SM_ODT_3 AU21 → M_ODT0 16,18, M_ODT1 16,18, M_ODT2 17,18, M_ODT3 17,18

+1.8V

SM_RCOMP# AV9 — R28 1 — 2 80.6Ohm 1%; SM_RCOMP AT9 — R29 1 — 2 80.6Ohm 1%

SM_VREF_0 AK1, SM_VREF_1 AK41 — M_VREF_MCH → M_VREF_MCH 16,17,18

GND

CLK:

G_CLKIN# AF33, G_CLKIN AG33, D_REFCLKIN# AG27, D_REFCLKIN A26, D_REFSSCLKIN# C40, D_REFSSCLKIN D41 → CLK_MCH_3GPLL# 23, CLK_MCH_3GPLL 23, CLK_UMA_96M# 23, CLK_UMA_96M 23, CLK_LCD_SSCG# 23, CLK_LCD_SSCG 23

DMI:

DMI_RXN_0 AE35, DMI_RXN_1 AE39, DMI_RXN_2 AG35, DMI_RXN_3 AH39 → DMI_TXN0, DMI_TXN1, DMI_TXN2, DMI_TXN3 → DMI_TXN[3:0] 13

DMI_RXP_0 AC35, DMI_RXP_1 AE39, DMI_RXP_2 AE35, DMI_RXP_3 AG39 → DMI_TXP0, DMI_TXP1, DMI_TXP2, DMI_TXP3 → DMI_TXP[0..3] 13

DMI_TXN_0 AE37, DMI_TXN_1 AE41, DMI_TXN_2 AG37, DMI_TXN_3 AH41 → DMI_RXN0, DMI_RXN1, DMI_RXN2, DMI_RXN3 → DMI_RXN[0..3] 13

DMI_TXP_0 AC37, DMI_TXP_1 AE41, DMI_TXP_2 AE37, DMI_TXP_3 AG41 → DMI_RXP0, DMI_RXP1, DMI_RXP2, DMI_RXP3 → DMI_RXP[0..3] 13

M_VREF_MCH — C26 0.1UF/16V c0402 — GND; C27 1UF/10V — GND

2.0G

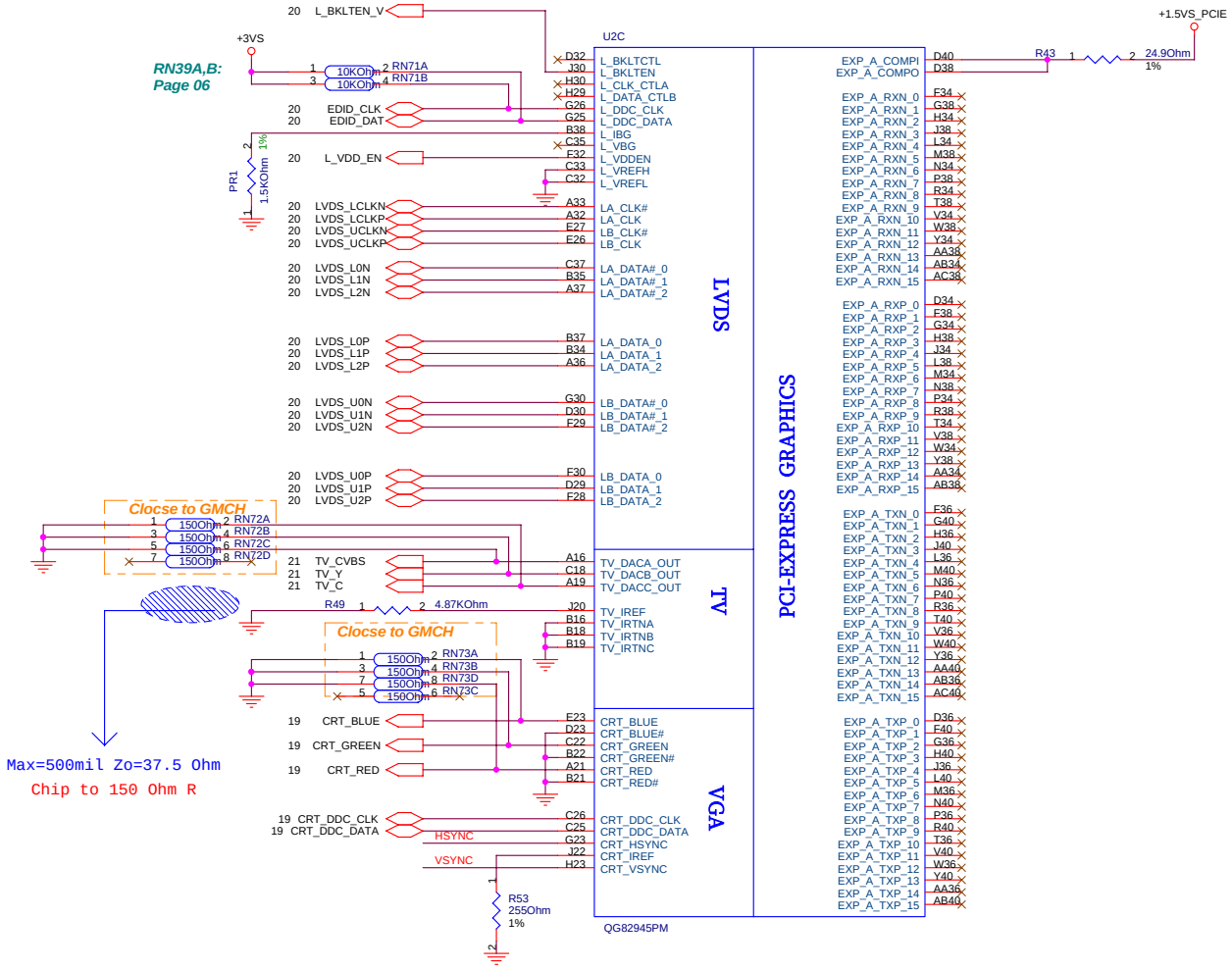
ASUSTeK COMPUTER INC.

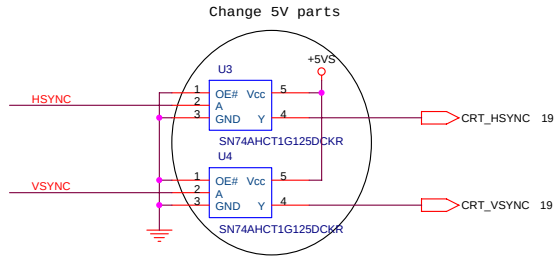
Title : NB-945GM(DMI & CFG)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

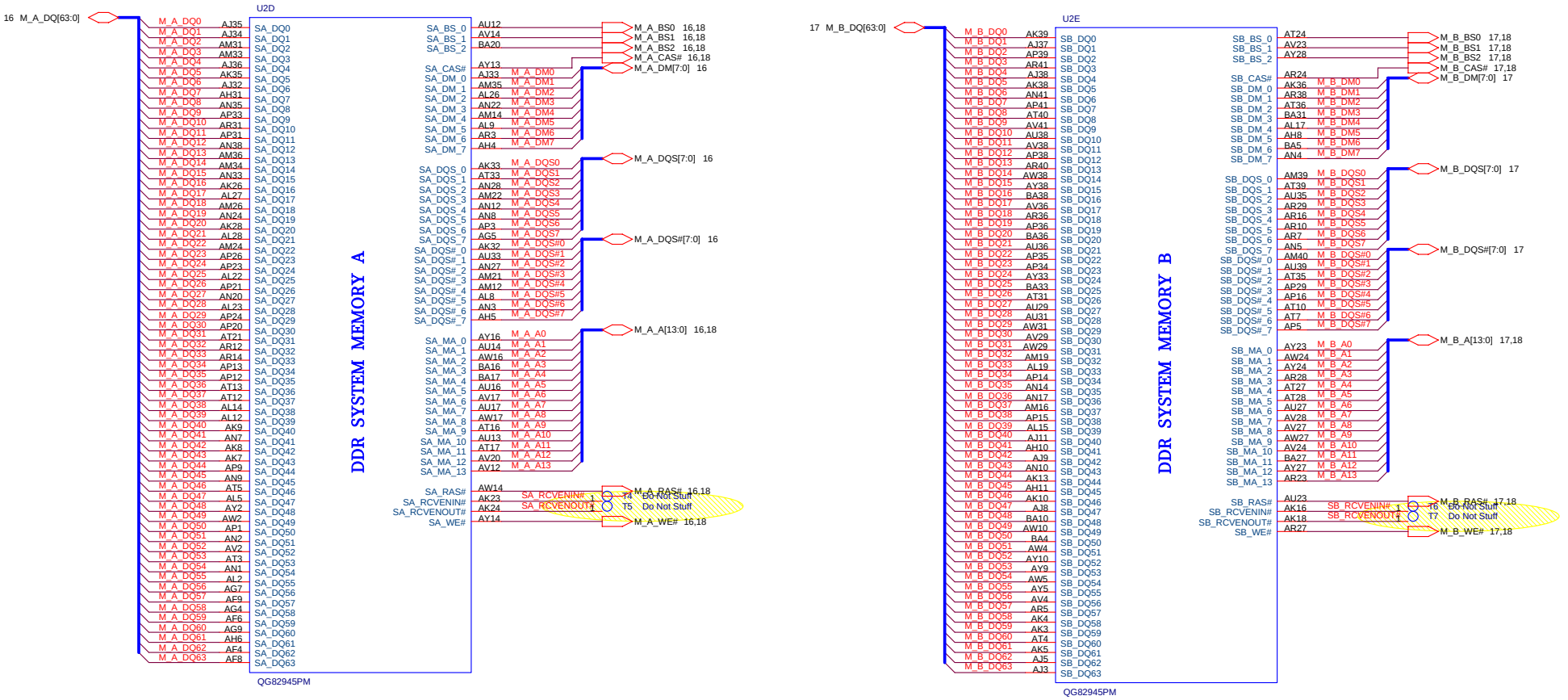
Date: Friday, September 15, 2006 Sheet 6 of 57





2.0G

ASUSTeK COMPUTER INC.	Title : NB_945GM(GRAPHIC)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 7 of 57	



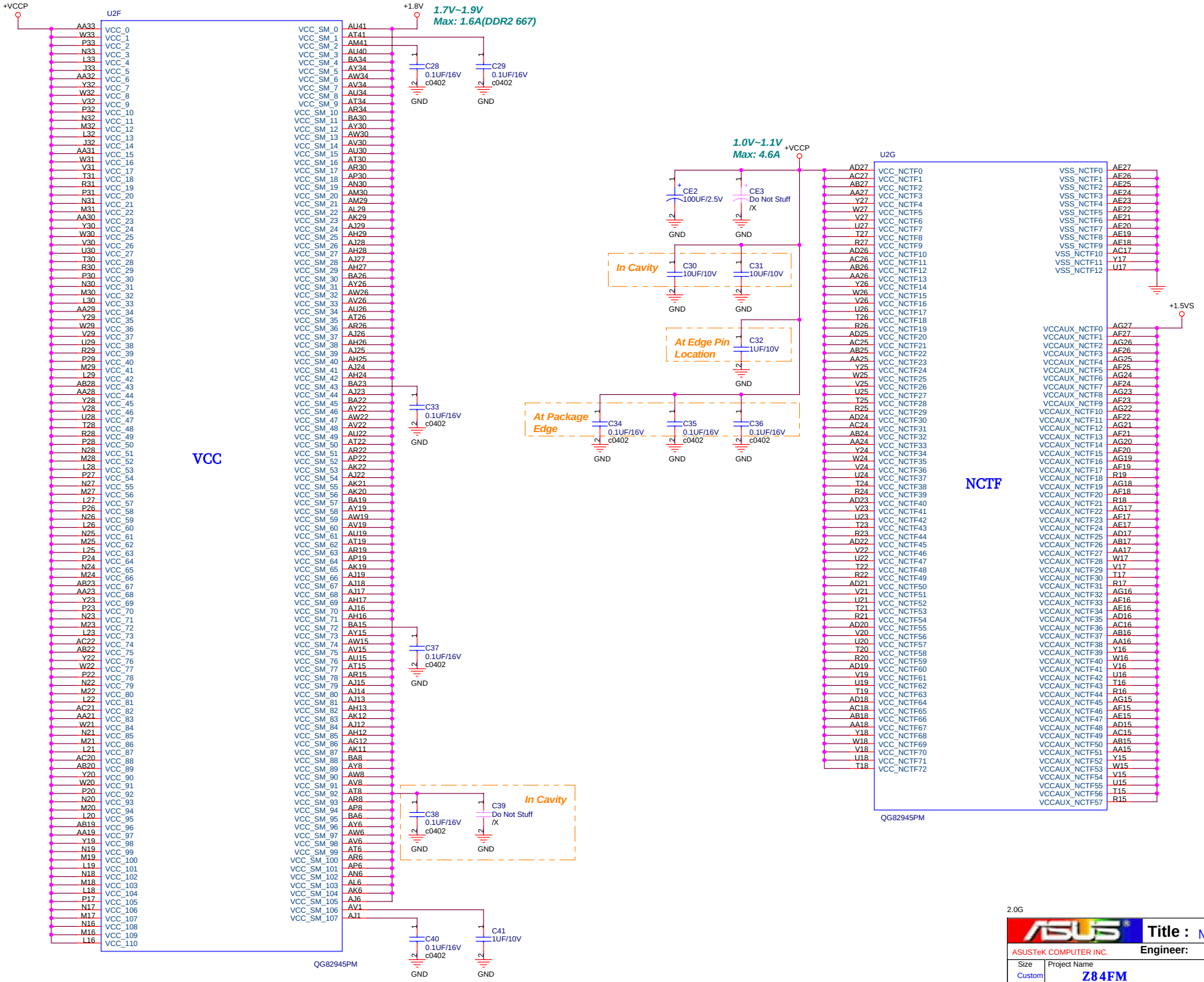
2.0G

Title : NB-945GM(DDR2)

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 8 of 57



2.0G

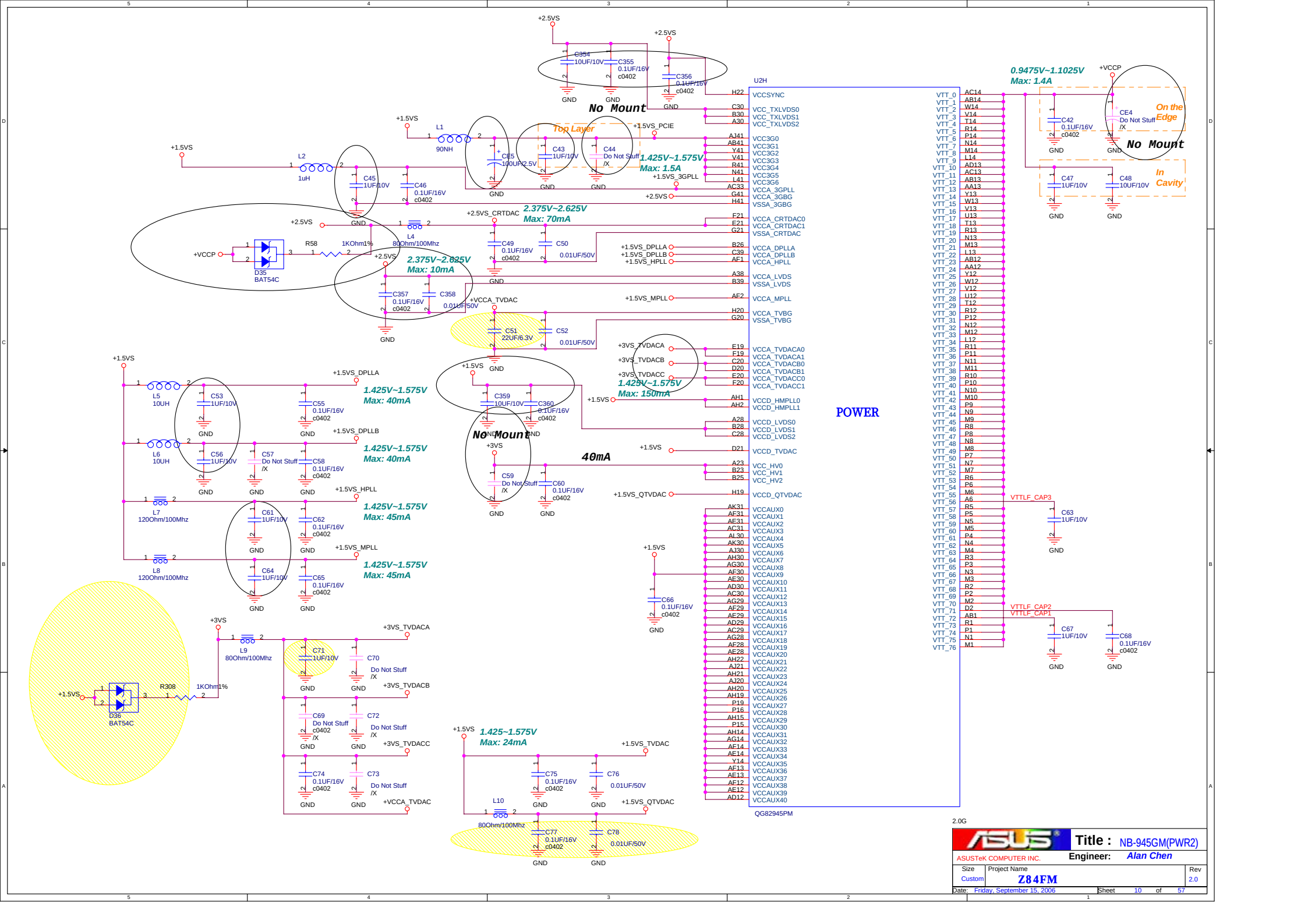
ASUSTeK COMPUTER INC.

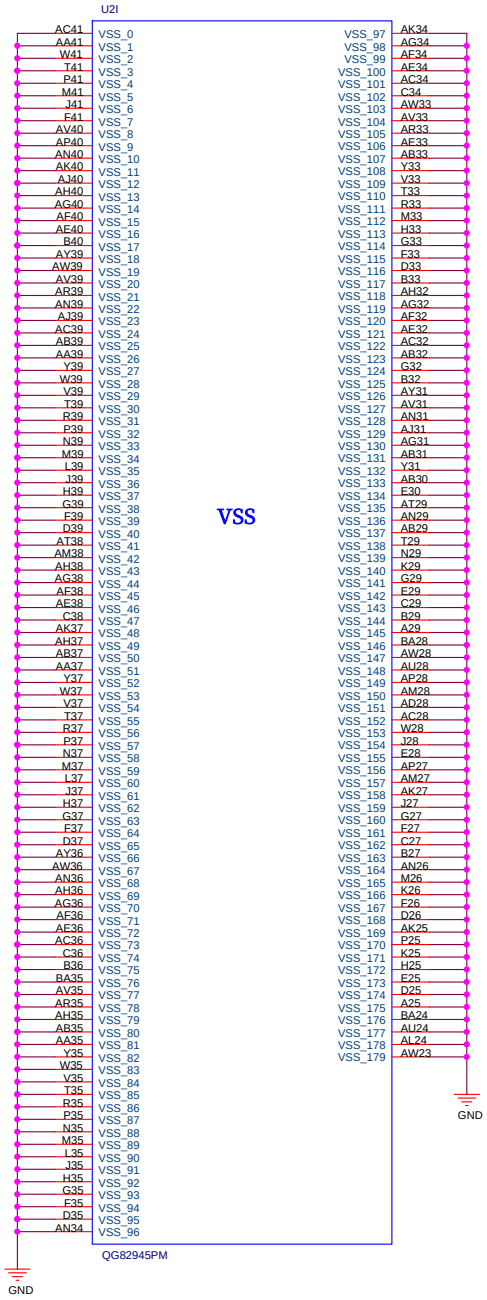
Title : NB-945GM(PWR)

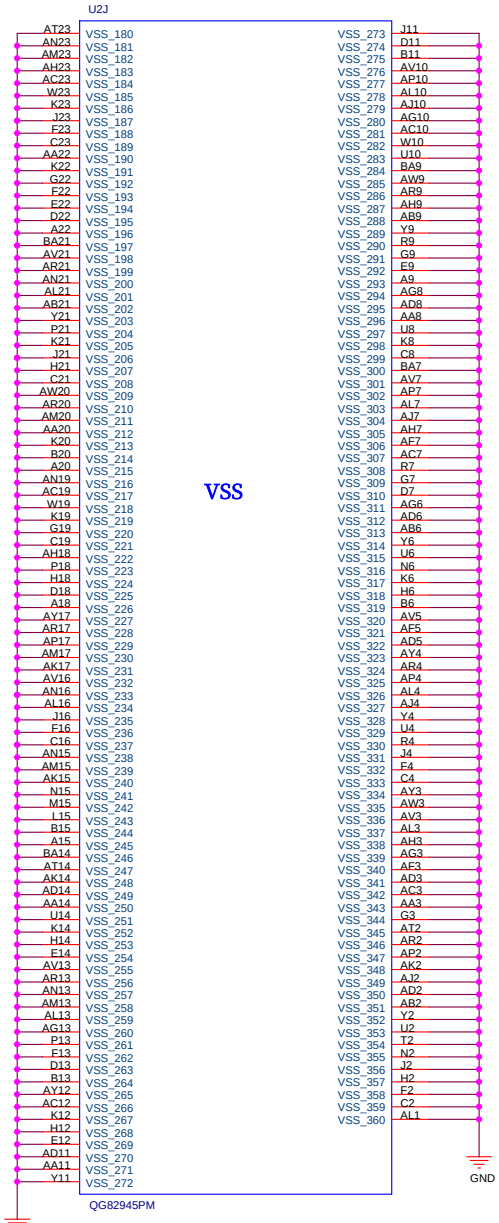
Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 9 of 57

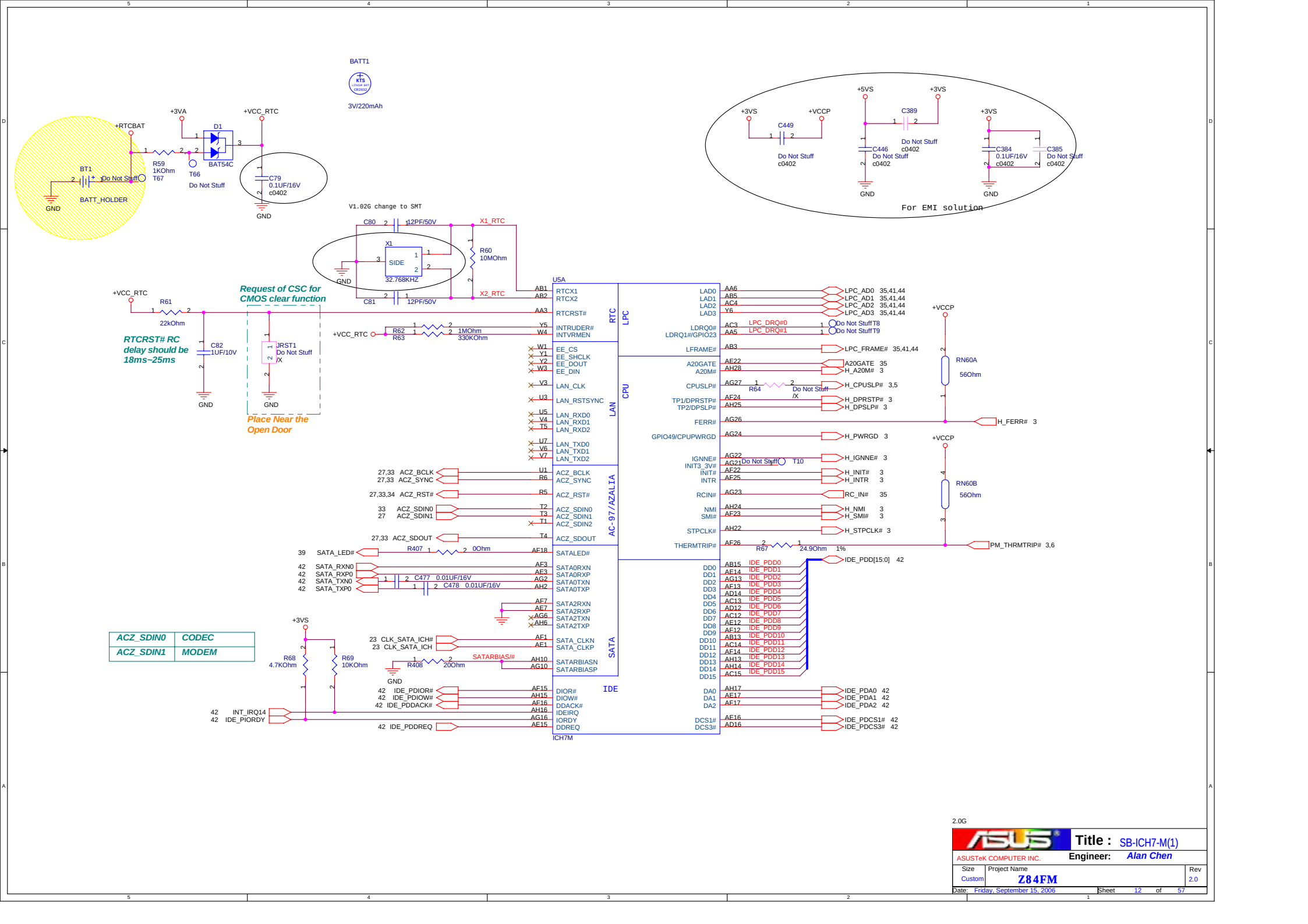

U2H
QG82945PM
POWER
No Mount
Top Layer
On the Edge
In Cavity
1.425V~1.575V
Max: 1.5A
0.9475V~1.1025V
Max: 1.4A
2.375V~2.625V
Max: 70mA
2.375V~2.625V
Max: 10mA
1.425V~1.575V
Max: 150mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425~1.575V
Max: 24mA
40mA
Title : NB-945GM(PWR2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size Custom
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 10 of 57

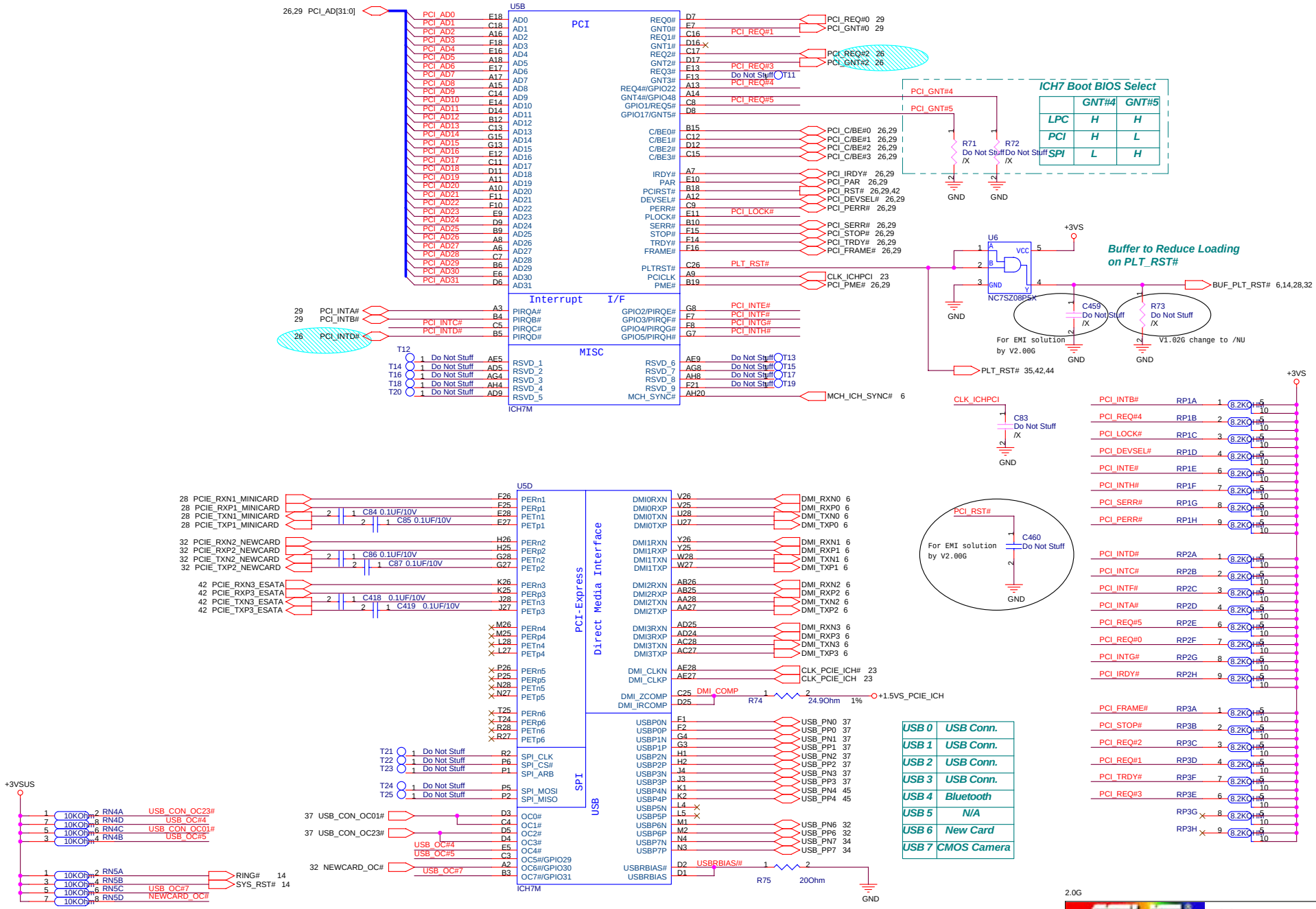


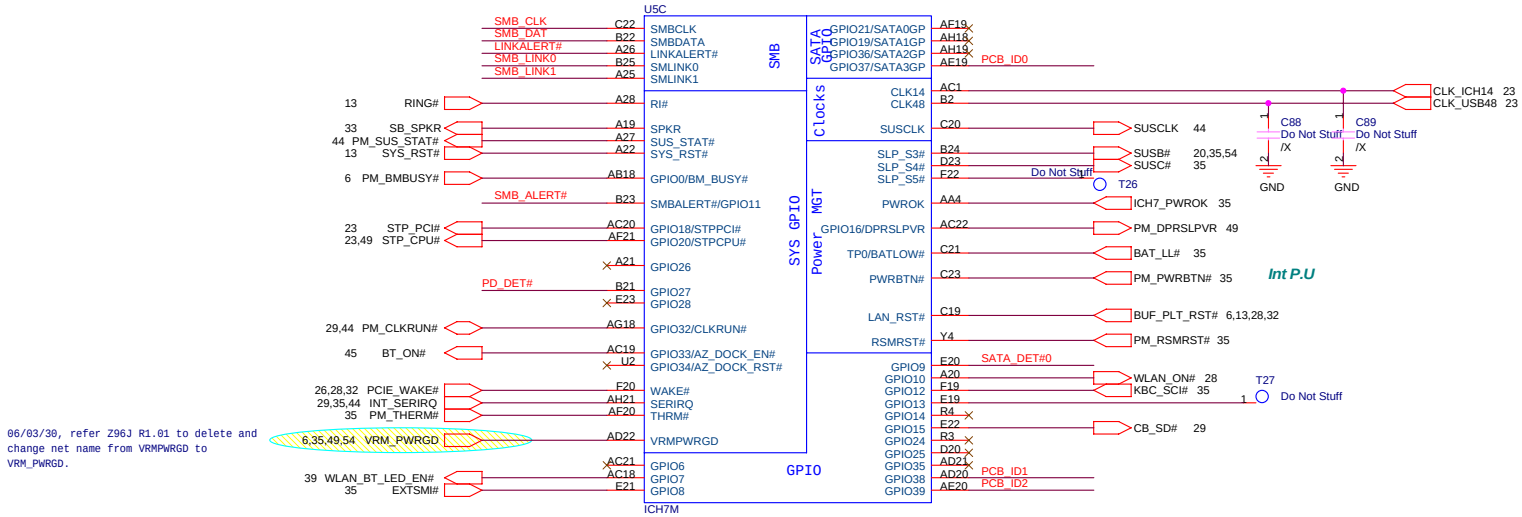


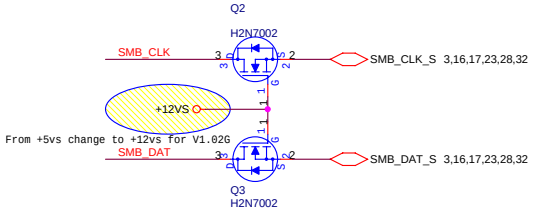
2.0G

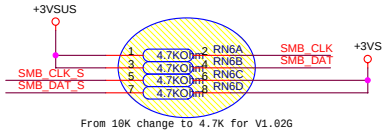
ASUSTeK COMPUTER INC.	Title : NB-945PM(GND)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 11 of 57	

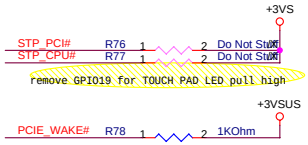

BATT1
3V/220mAh
+RTCBAT
+3VA
+VCC_RTC
D1
BAT54C
R59
1KOhm
T66
T67
Do Not Stuff
BT1
BATT_HOLDER
C79
0.1UF/16V
c0402
GND
+5VS
+3VS
+VCCP
C449
C389
C446
C384
0.1UF/16V
C385
For EMI solution
V1.02G change to SMT
C80
12PF/50V
X1
SIDE
32.768KHZ
C81
X1_RTC
X2_RTC
R60
10MOhm
Request of CSC for
CMOS clear function
R61
22kOhm
C82
1UF/10V
JRST1
RTCRST# RC
delay should be
18ms~25ms
Place Near the
Open Door
R62
R63
1MOhm
330KOhm
U5A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN
CPU
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
AC-97/AZALIA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
SATA
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE
ICH7M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
LPC_AD0 35,41,44
LPC_AD1 35,41,44
LPC_AD2 35,41,44
LPC_AD3 35,41,44
LPC_DRQ#0
LPC_DRQ#1
Do Not Stuff T8
Do Not Stuff T9
LPC_FRAME# 35,41,44
A20GATE 35
H_A20M# 3
H_CPUSLP# 3,5
R64
H_DPRSTP# 3
H_DPSLP# 3
H_FERR# 3
RN60A
56Ohm
H_PWRGD 3
H_IGNNE# 3
T10
H_INIT# 3
H_INTR 3
RC_IN# 35
H_NMI 3
H_SMI# 3
H_STPCLK# 3
R67
24.9Ohm 1%
PM_THRMTRIP# 3,6
RN60B
56Ohm
IDE_PDD[15:0] 42
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
IDE_PDA0 42
IDE_PDA1 42
IDE_PDA2 42
IDE_PDCS1# 42
IDE_PDCS3# 42
27,33 ACZ_BCLK
27,33 ACZ_SYNC
27,33,34 ACZ_RST#
33 ACZ_SDIN0
27 ACZ_SDIN1
27,33 ACZ_SDOUT
39 SATA_LED#
R407
0Ohm
42 SATA_RXN0
42 SATA_RXP0
42 SATA_TXN0
42 SATA_TXP0
C477 0.01UF/16V
C478 0.01UF/16V
23 CLK_SATA_ICH#
23 CLK_SATA_ICH
SATARBIAS#
R408
20Ohm
R68
4.7KOhm
R69
10KOhm
42 IDE_PDIOR#
42 IDE_PDIOW#
42 IDE_PDDACK#
42 INT_IRQ14
42 IDE_PIORDY
42 IDE_PDDREQ
ACZ_SDIN0 CODEC
ACZ_SDIN1 MODEM
2.0G
Title : SB-ICH7-M(1)
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size Custom
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 12 of 57

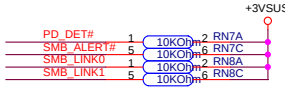

U5B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4
GNT#5
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
U6
NC7SZ08P5X
For EMI solution by V2.00G
V1.02G change to /NU
U5D
PCI-Express
Direct Media Interface
USB
SPI
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 N/A
USB 6 New Card
USB 7 CMOS Camera
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size Custom
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 13 of 57

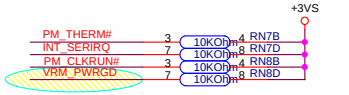


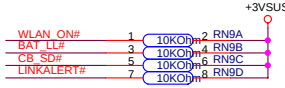


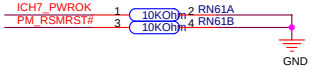


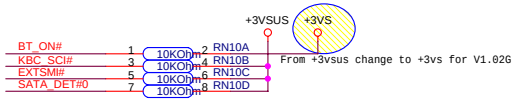


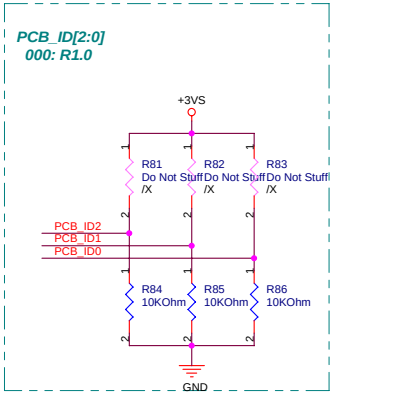






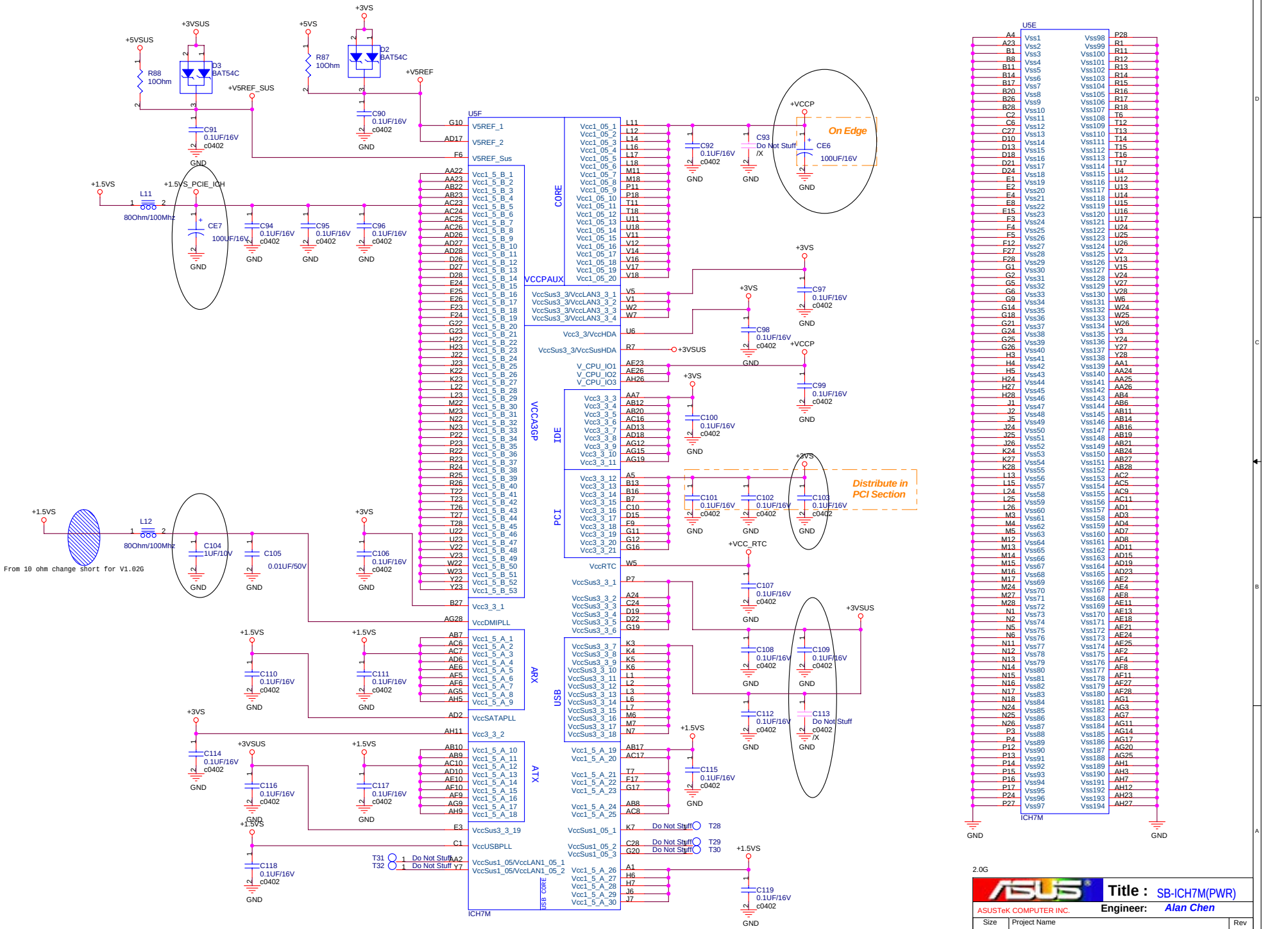






2.0G

ASUSTeK COMPUTER INC	Title : SB-ICH7M(3)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 14 of 57	

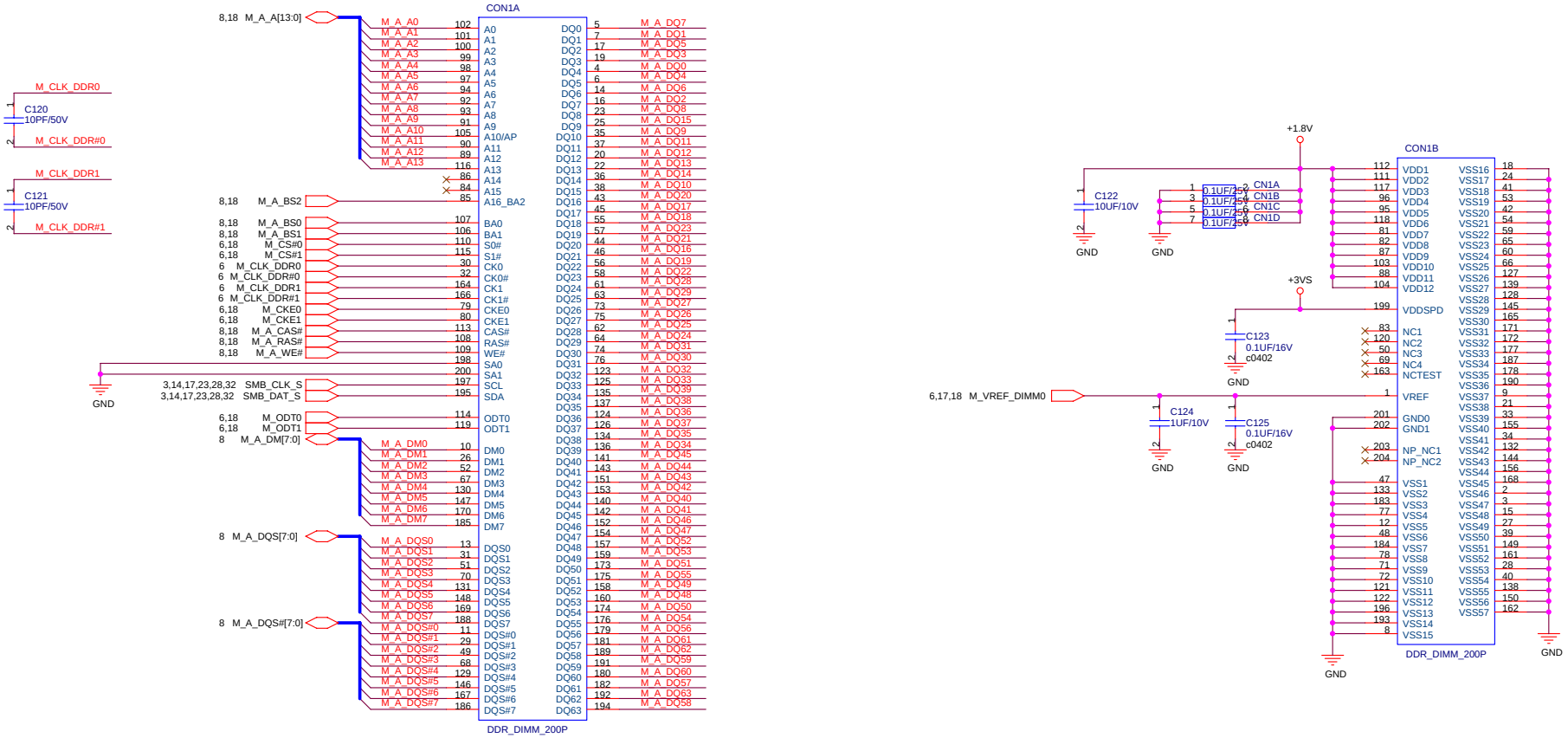


2.0G

ASUSTeK COMPUTER INC.	Title : SB-ICH7M(PWR)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 15 of 57	

M_A_DQ[63:0] 8

REV Type

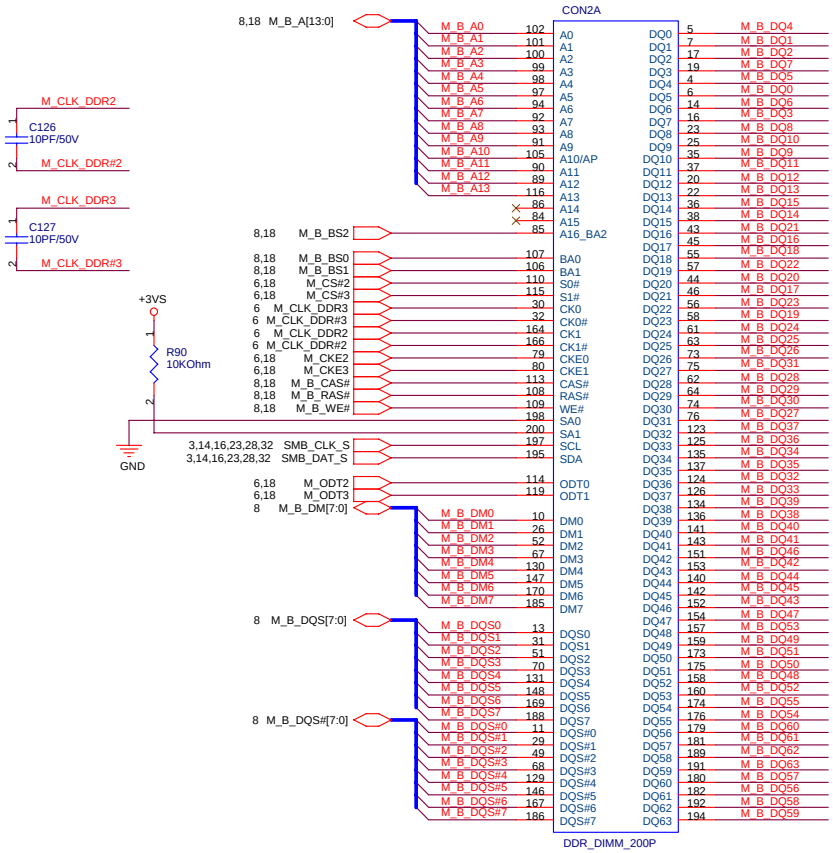


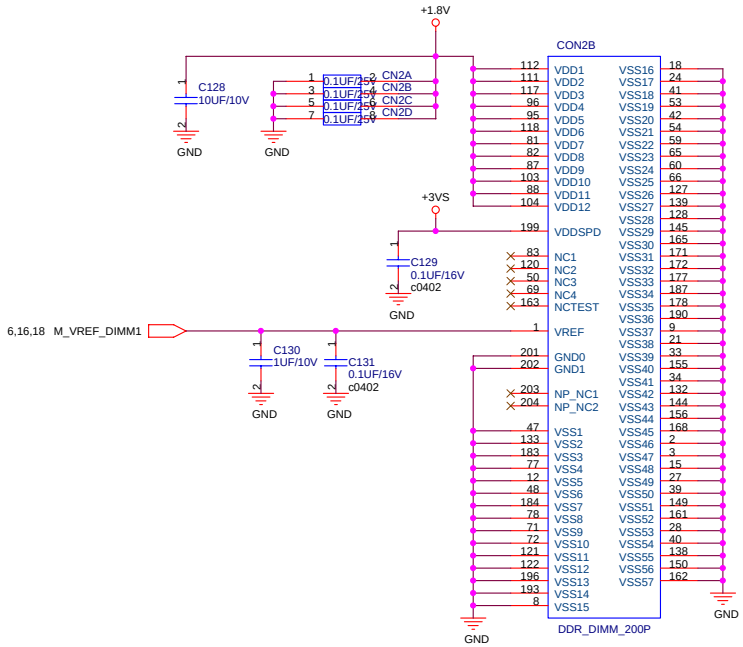
2.0G

ASUSTeK COMPUTER INC.	Title : DDR2 SO-DIMM0	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 16 of 57	

M_B_DQ[63:0] 8

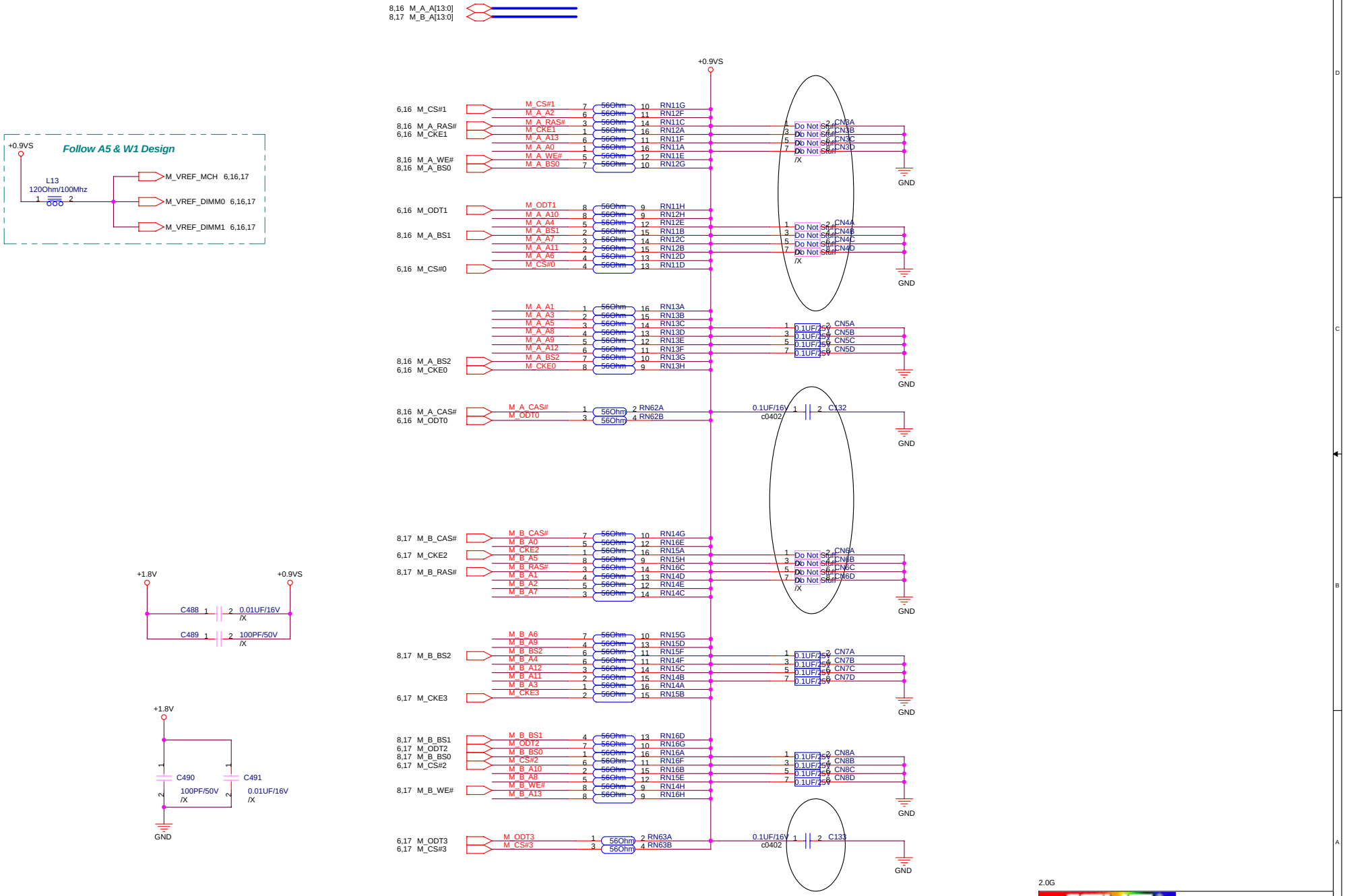
STD Type





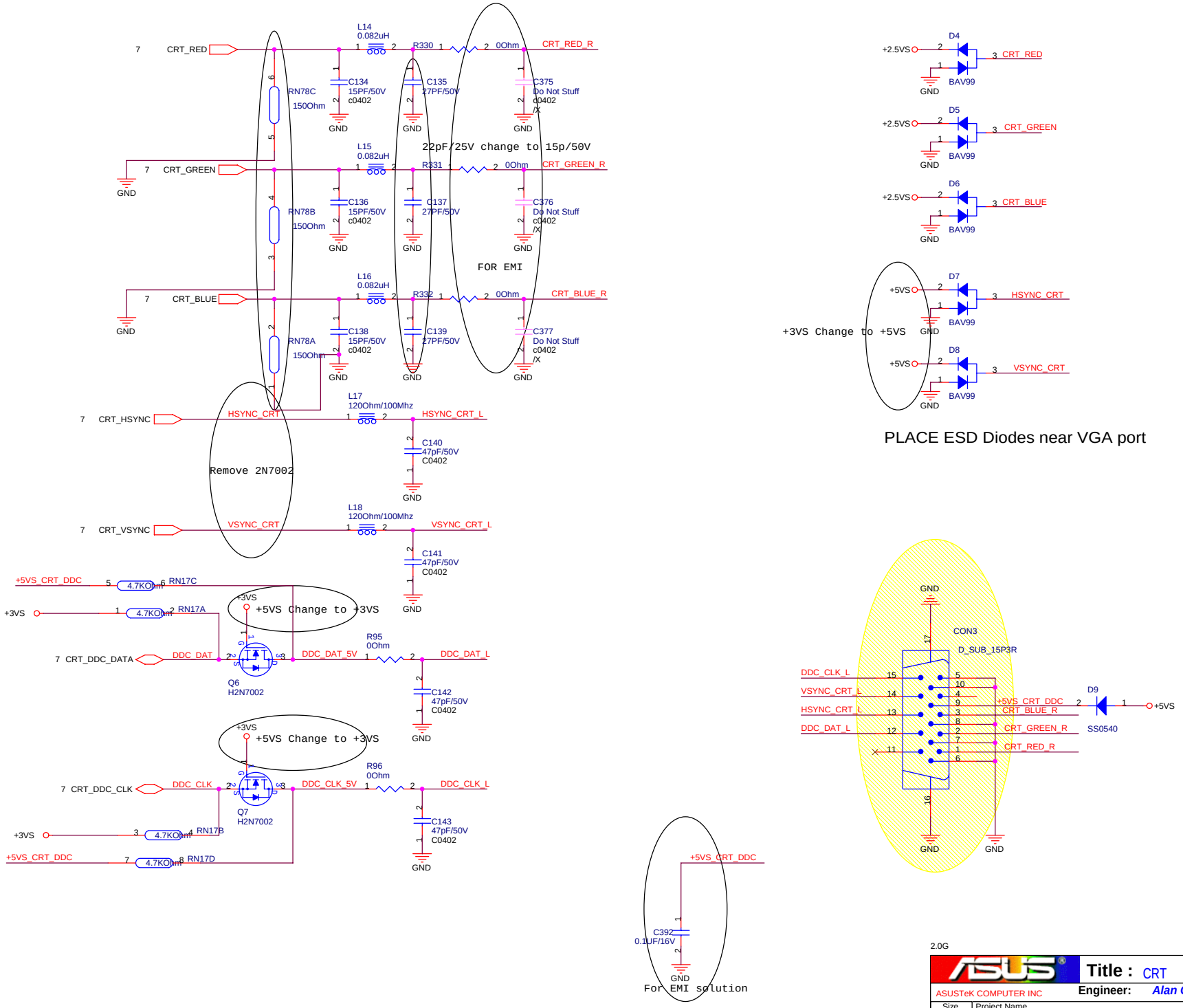
2.0G

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 17 of 57	



2.0G

ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 18 of 57	



PLACE ESD Diodes near VGA port

2.0G

ASUSTeK COMPUTER INC

Title : CRT

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 19 of 57

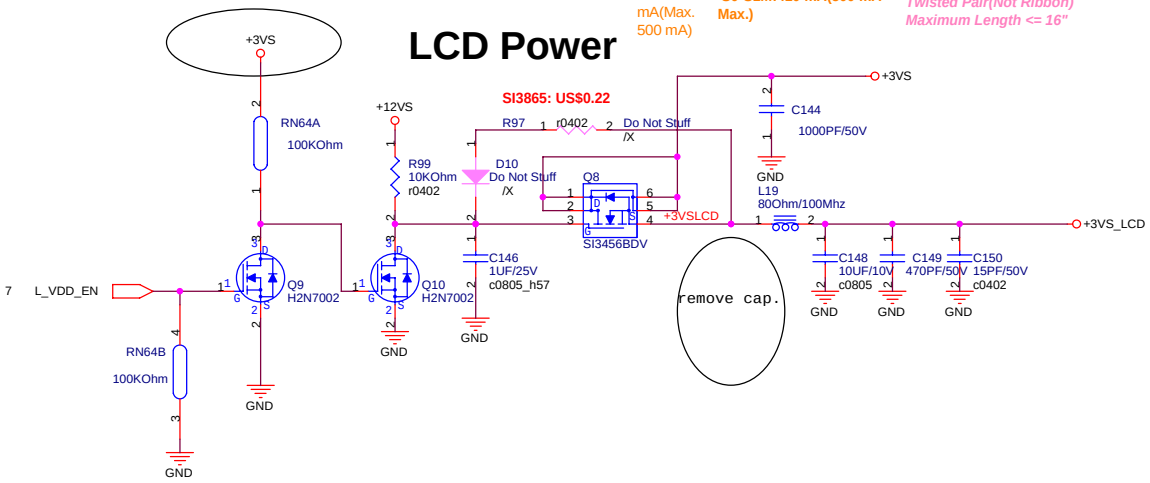
LCD Backlight Control

3V-3.6V
Full
Active:
410
mA(Max.
500 mA)

3-3.6V
S0-S1M:410 mA(500 mA Max.)

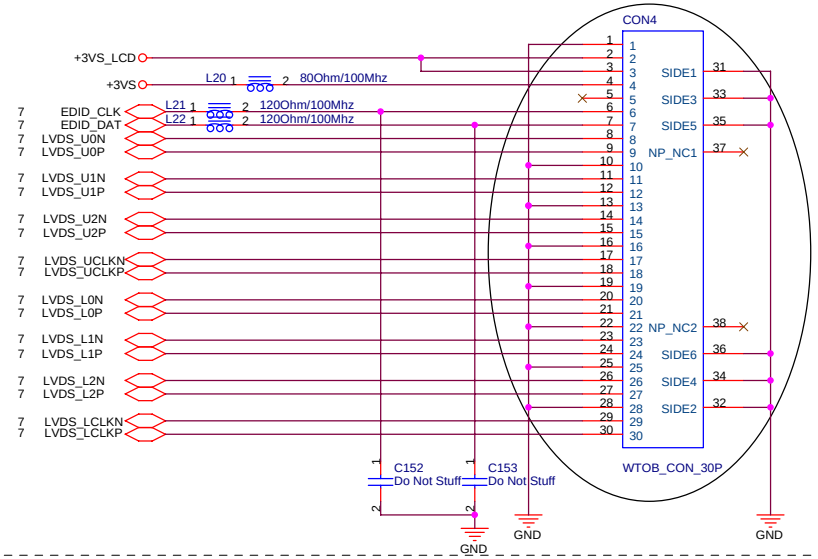
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power



LCD LVDS Interface

Updata pin define

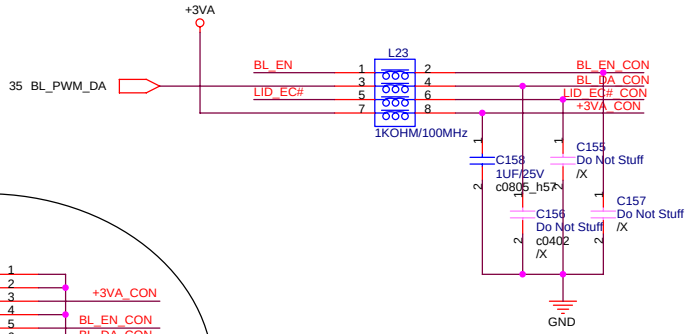


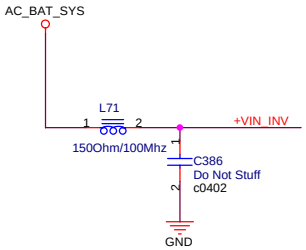
INVERTER Interface/Speaker CONN.

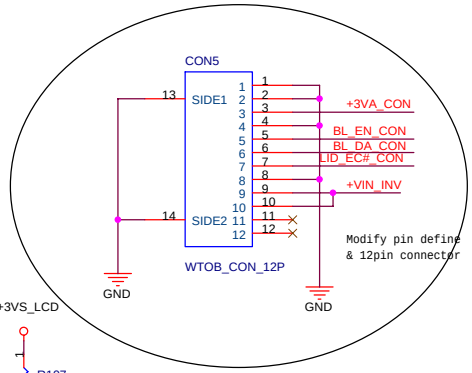
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

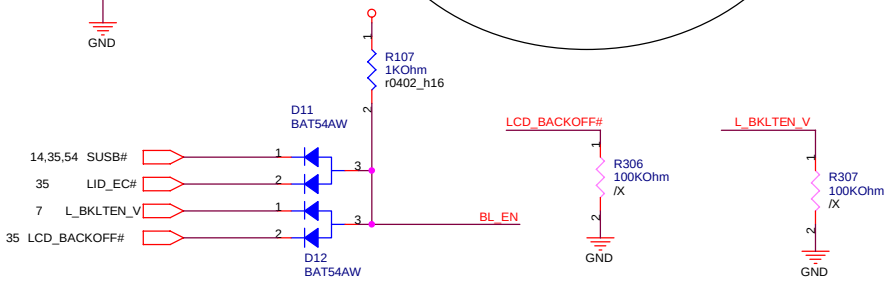
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR





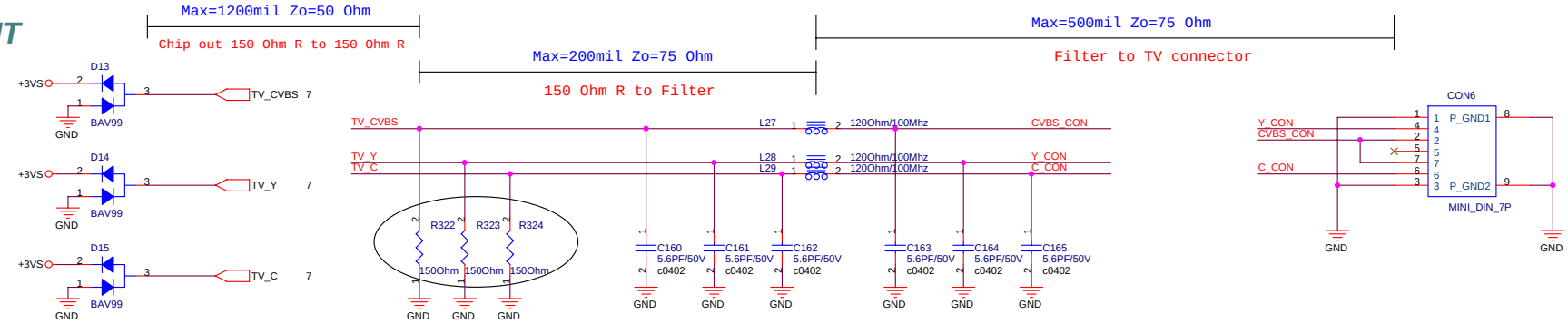




2.0G

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 20 of 57	

TV OUT

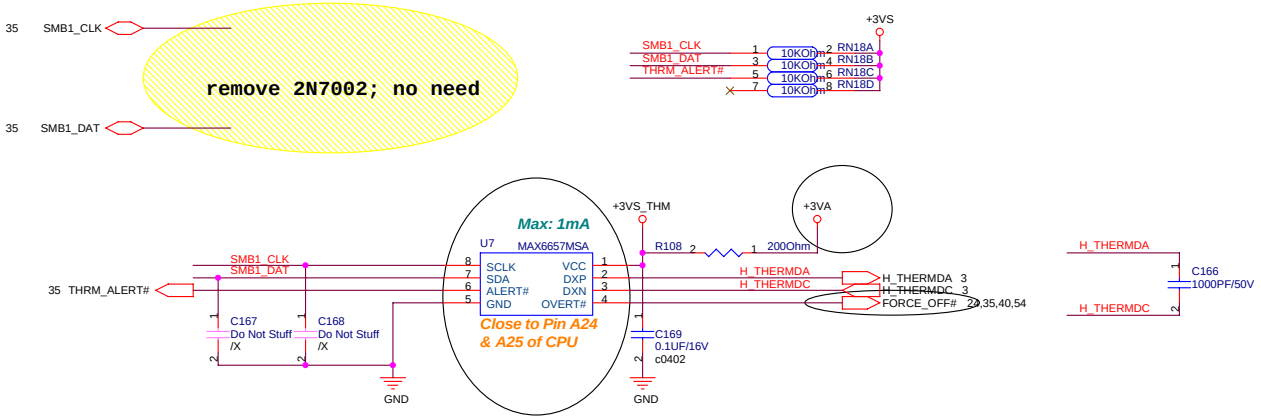


PLACE ESD
Diodes near
TV port

2.0G

ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 21 of 57	

Thermal Sensor

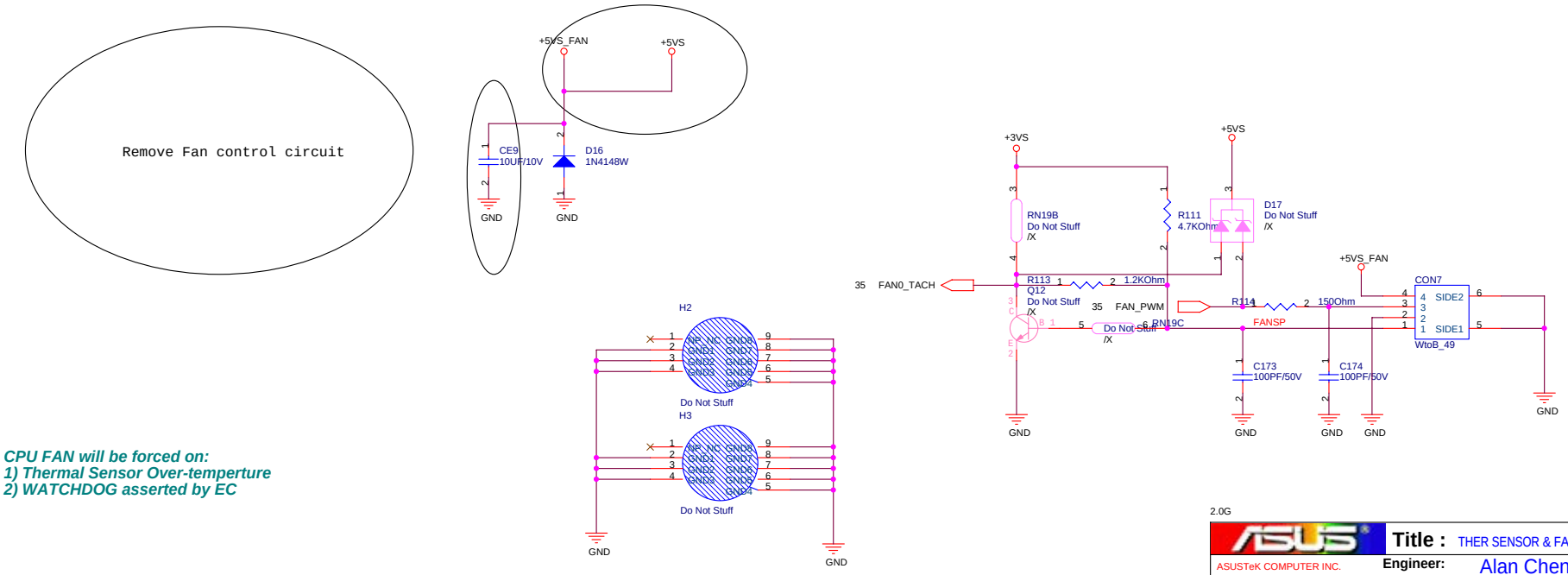


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

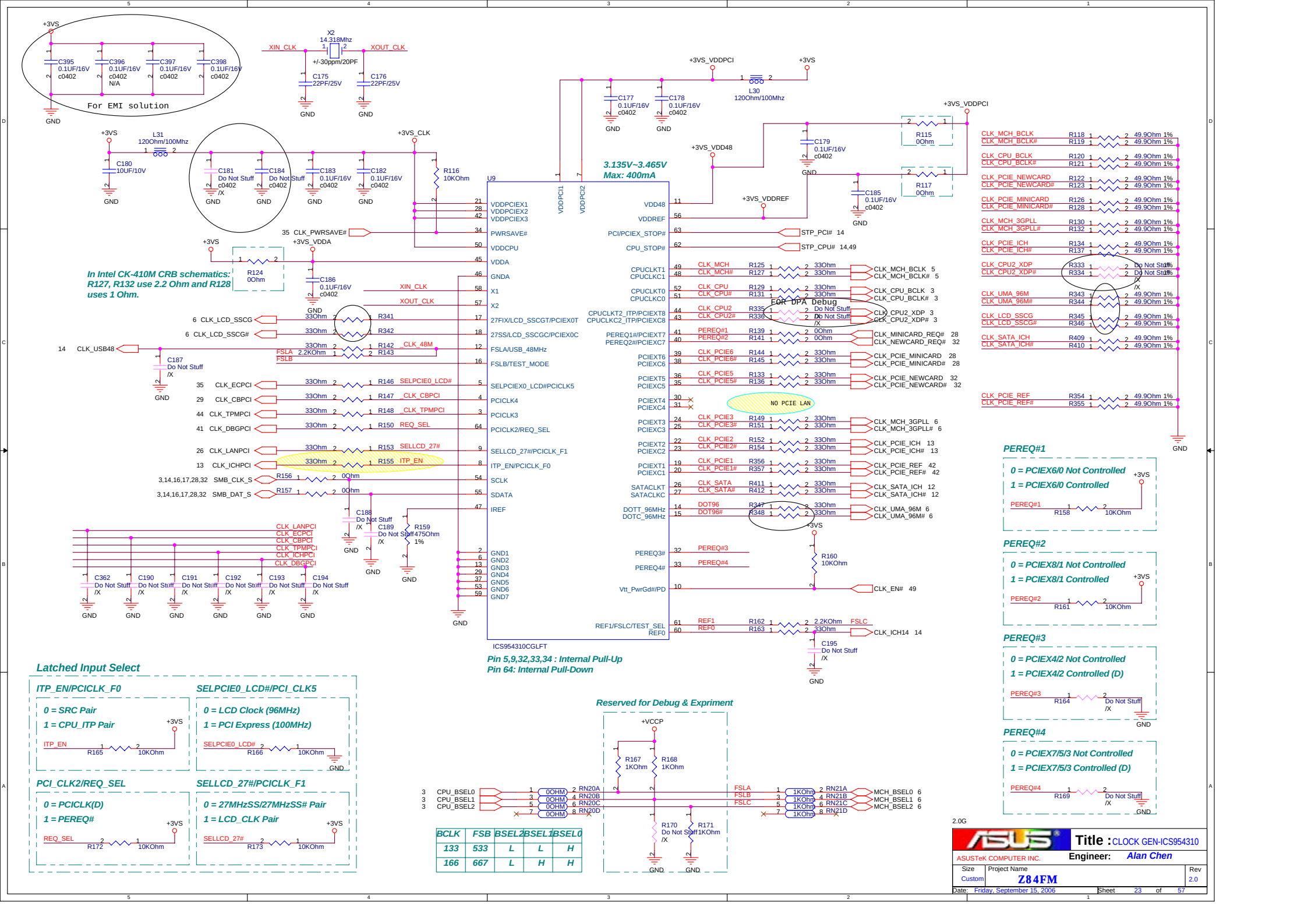
DC FAN Control

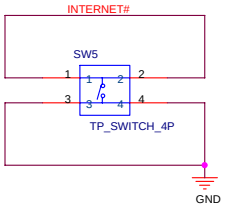


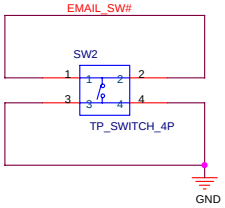
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

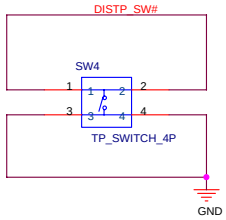
2.0G

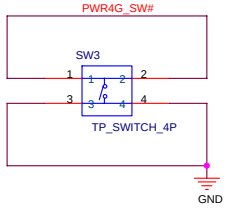
ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 22 of 57	


For EMI solution
X2
14.318Mhz
+/-30ppm/20PF
XIN_CLK
XOUT_CLK
C175 22PF/25V
C176 22PF/25V
L30 120Ohm/100Mhz
L31 120Ohm/100Mhz
3.135V~3.465V
Max: 400mA
U9
ICS954310CGLFT
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128 uses 1 Ohm.
FOR DPA Debug
NO PCIE LAN
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
Reserved for Debug & Expriment
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 23 of 57

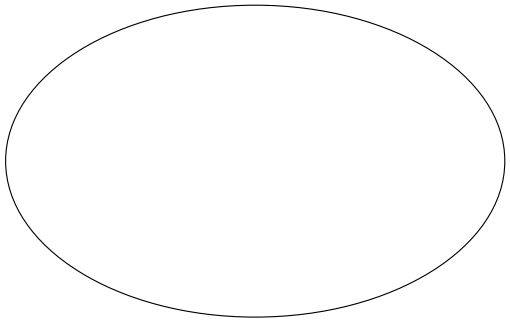


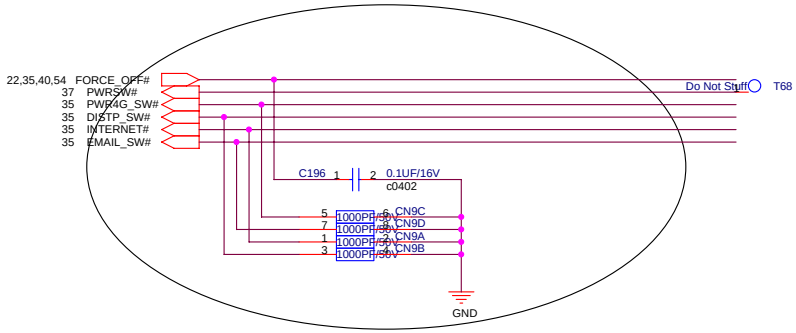


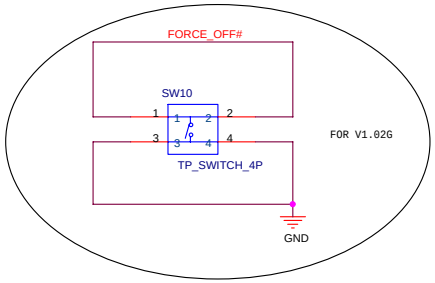


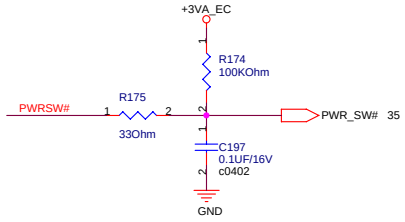


SHUT_DOWN#









2.0G

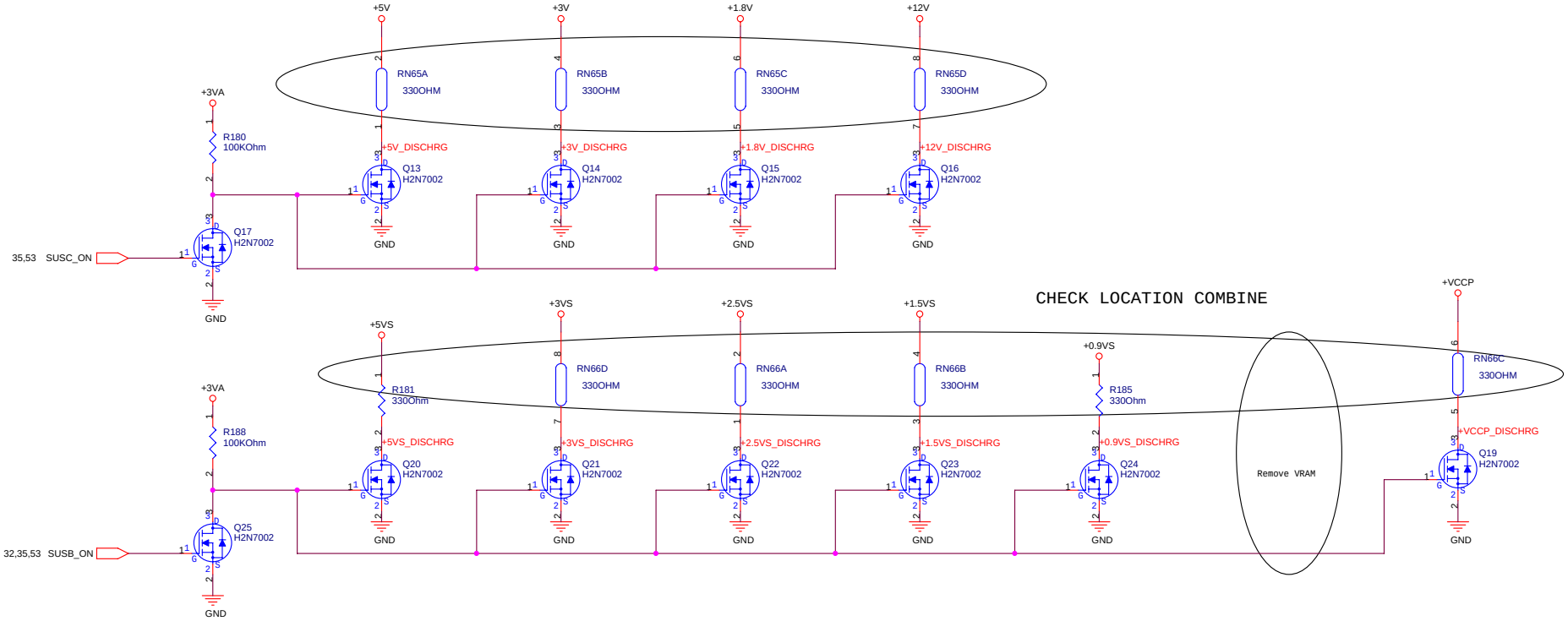
Title : Power on & Res Freq

ASUSTeK COMPUTER INC

Engineer: Alan Chen

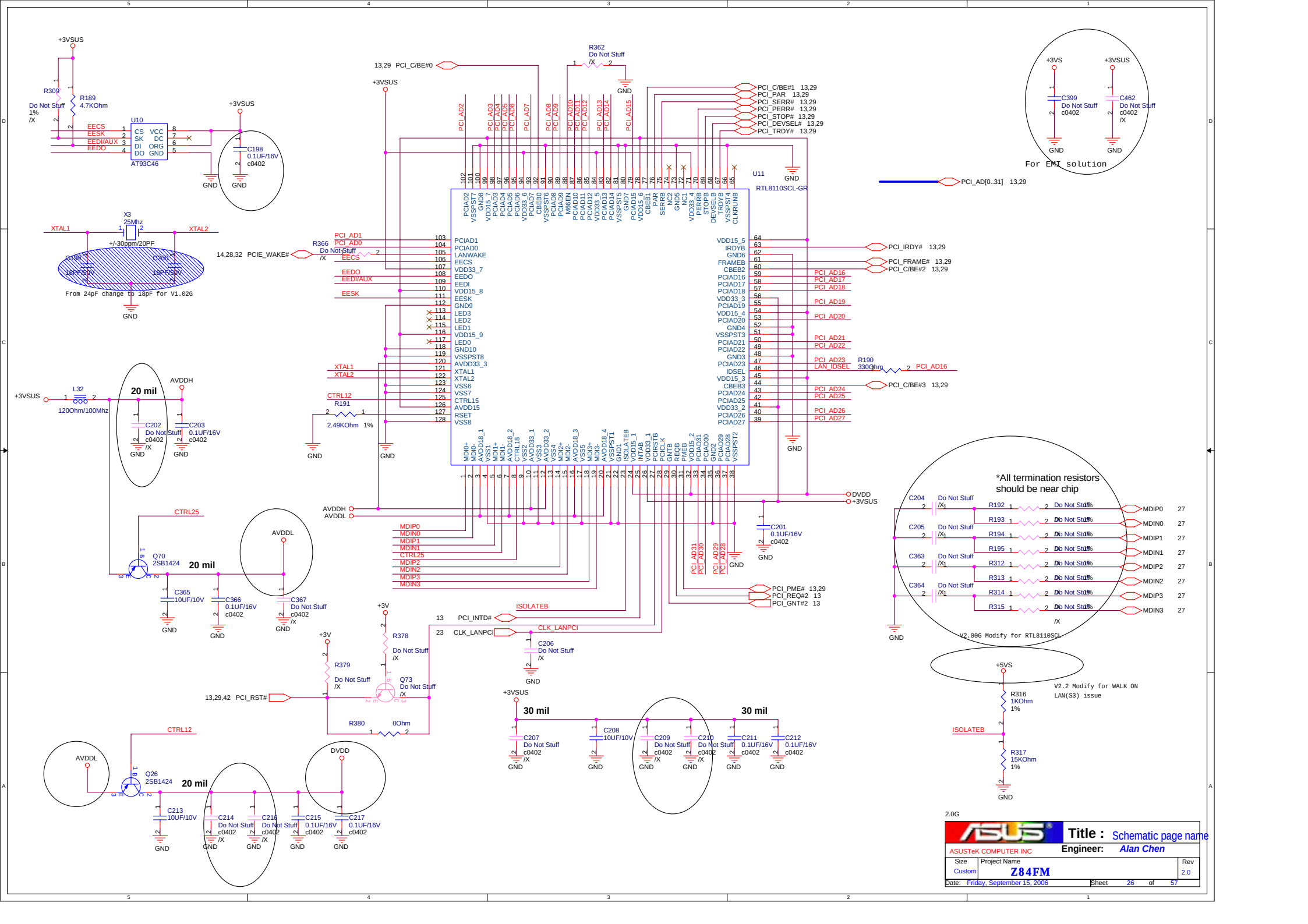
Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 24 of 57



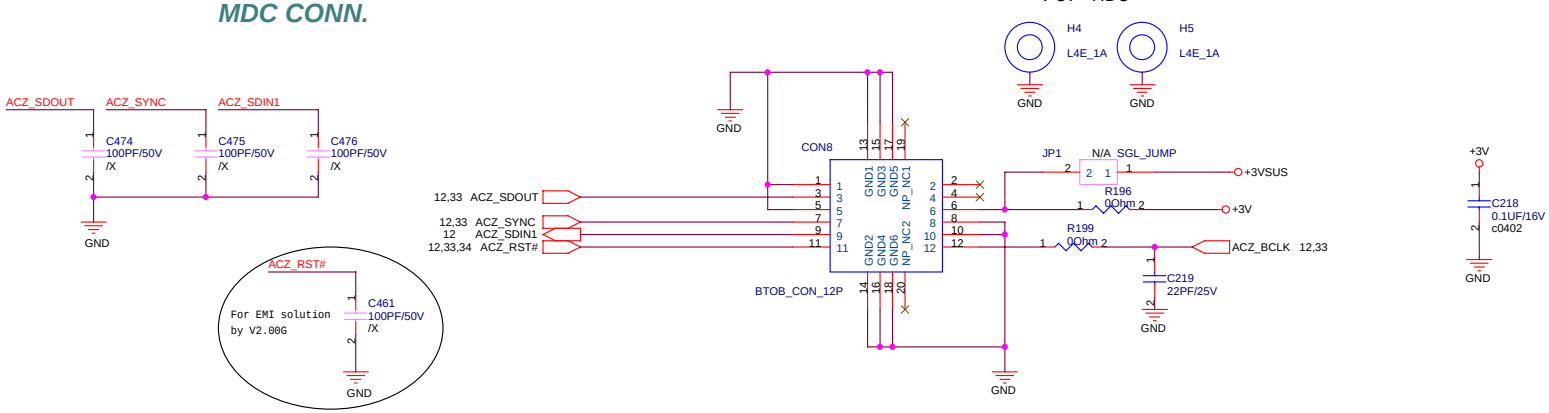
2.0G

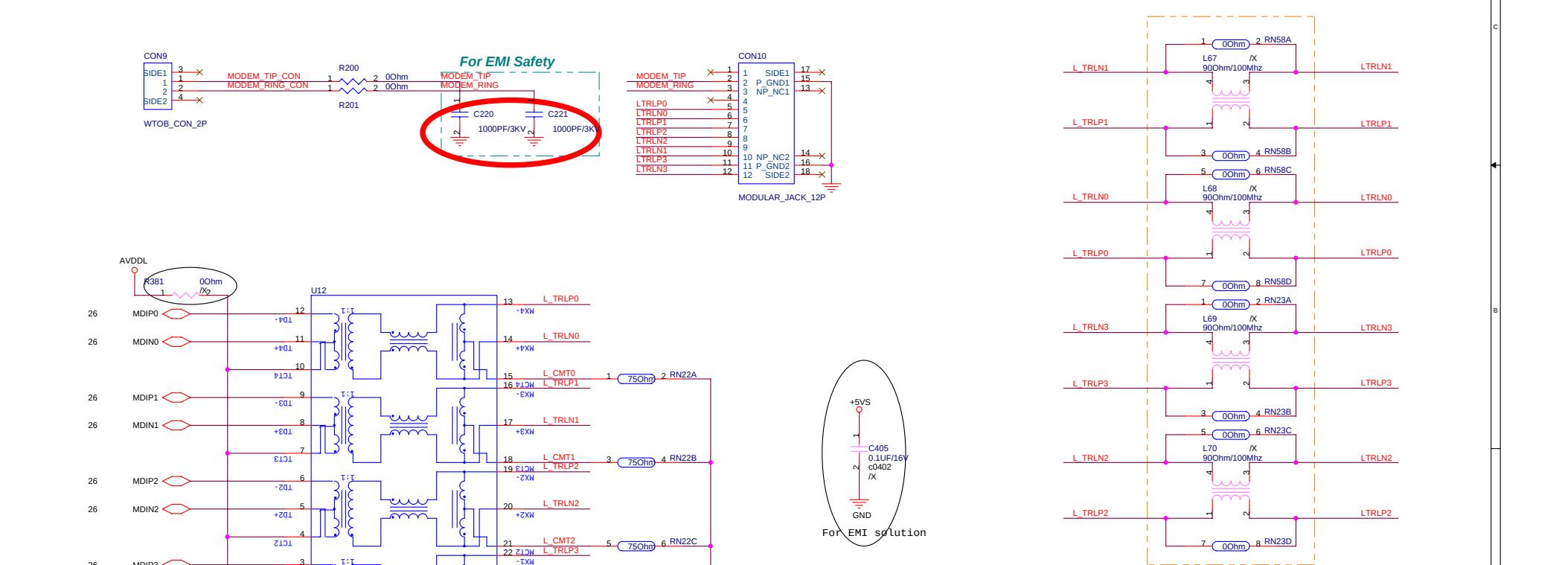
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 25 of 57	


+3VSUS
R309
Do Not Stuff
1%
/X
R189
4.7KOhm
U10
AT93C46
EECS
EESK
EEDI/AUX
EEDO
CS
SK
DI
DO
VCC
DC
ORG
GND
C198
0.1UF/16V
c0402
GND
X3
25Mhz
XTAL1
XTAL2
+/-30ppm/20PF
C199
C200
18PF/50V
From 24pF change to 18pF for V1.02G
13,29 PCI_C/BE#0
R362
Do Not Stuff
/X
U11
RTL8110SCL-GR
PCI_AD[0..31] 13,29
PCI_C/BE#1 13,29
PCI_PAR 13,29
PCI_SERR# 13,29
PCI_PERR# 13,29
PCI_STOP# 13,29
PCI_DEVSEL# 13,29
PCI_TRDY# 13,29
PCI_IRDY# 13,29
PCI_FRAME# 13,29
PCI_C/BE#2 13,29
PCI_C/BE#3 13,29
14,28,32 PCIE_WAKE#
R366
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
CTRL12
R191
2.49KOhm 1%
R190
330Ohm
LAN_IDSEL
L32
120Ohm/100Mhz
20 mil
AVDDH
C202
Do Not Stuff
C203
0.1UF/16V
AVDDL
CTRL25
Q70
2SB1424
C365
10UF/10V
C366
0.1UF/16V
C367
Do Not Stuff
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
DVDD
+3VSUS
C201
0.1UF/16V
PCI_PME# 13,29
PCI_REQ#2 13
PCI_GNT#2 13
13 PCI_INTD#
23 CLK_LANPCI
ISOLATEB
CLK_LANPCI
C206
Do Not Stuff
+3V
R378
Do Not Stuff
R379
Do Not Stuff
Q73
Do Not Stuff
13,29,42 PCI_RST#
R380
0Ohm
30 mil
C207
Do Not Stuff
C208
10UF/10V
C209
Do Not Stuff
C210
Do Not Stuff
C211
0.1UF/16V
C212
0.1UF/16V
Q26
2SB1424
C213
10UF/10V
C214
Do Not Stuff
C216
Do Not Stuff
C215
0.1UF/16V
C217
0.1UF/16V
+3VS
C399
Do Not Stuff
C462
Do Not Stuff
For EMI solution
*All termination resistors
should be near chip
C204
C205
C363
C364
R192
R193
R194
R195
R312
R313
R314
R315
MDIP0 27
MDIN0 27
MDIP1 27
MDIN1 27
MDIP2 27
MDIN2 27
MDIP3 27
MDIN3 27
V2.00G Modify for RTL8110SCL
+5VS
R316
1KOhm
R317
15KOhm
V2.2 Modify for WALK ON
LAN(S3) issue
2.0G
Title : Schematic page name
ASUSTeK COMPUTER INC
Engineer: Alan Chen
Size
Custom
Project Name
Z84FM
Rev
2.0
Date: Friday, September 15, 2006
Sheet 26 of 57

MDC CONN.

For MDC





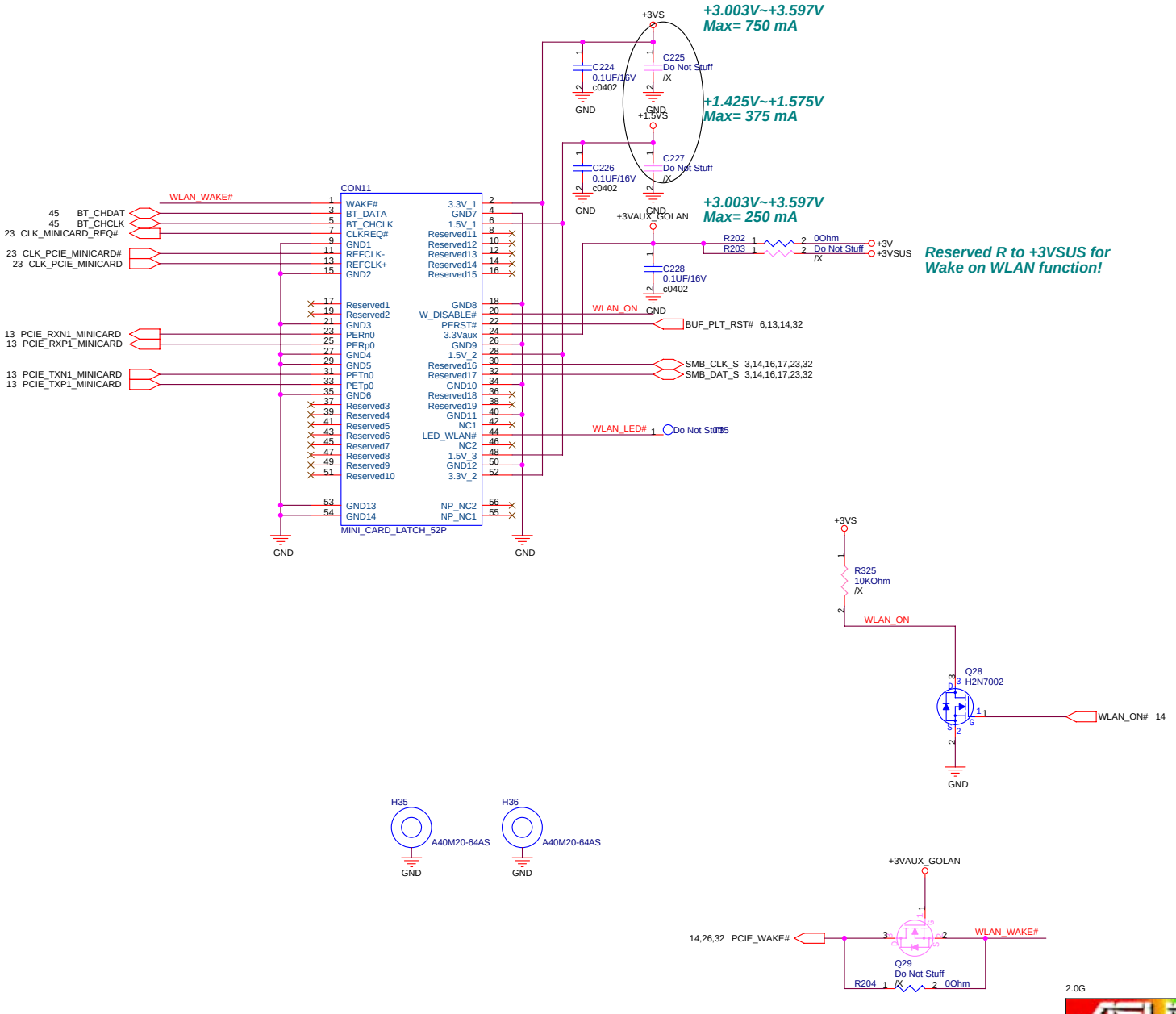
2.0G

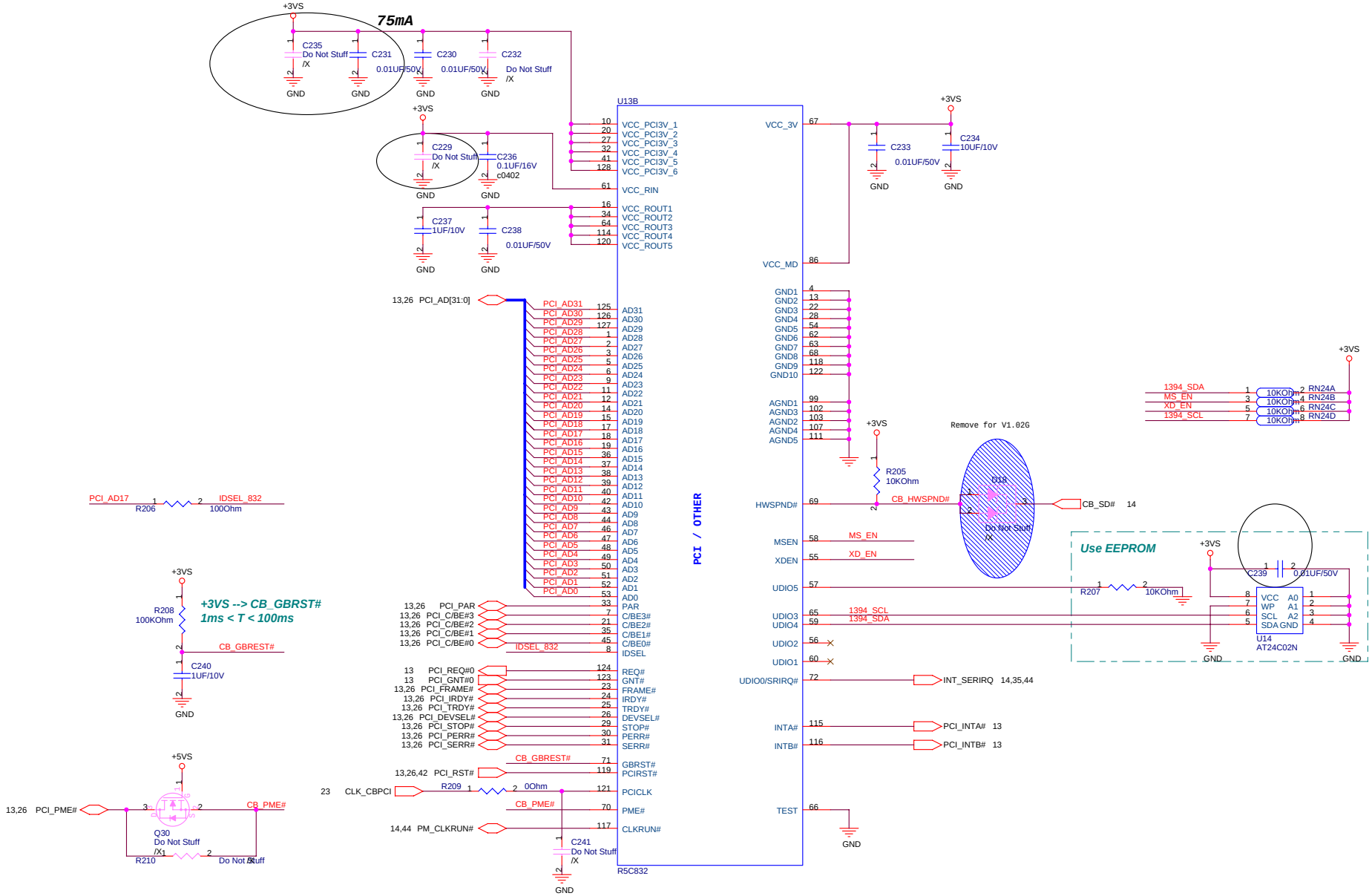
Title : RJ45&RJ11

ASUSTeK COMPUTER INC. Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 27 of 57


+3VS
+3.003V~+3.597V
Max= 750 mA
C224
0.1UF/16V
c0402
C225
Do Not Stuff
/X
GND
+1.5VS
+1.425V~+1.575V
Max= 375 mA
C226
0.1UF/16V
c0402
C227
Do Not Stuff
/X
+3VAUX_GOLAN
+3.003V~+3.597V
Max= 250 mA
R202 0Ohm
R203 Do Not Stuff
/X
+3V
+3VSUS
Reserved R to +3VSUS for
Wake on WLAN function!
C228
0.1UF/16V
c0402
CON11
MINI_CARD_LATCH_52P
WLAN_WAKE#
45 BT_CHDAT
45 BT_CHCLK
23 CLK_MINICARD_REQ#
23 CLK_PCIE_MINICARD#
23 CLK_PCIE_MINICARD
13 PCIE_RXN1_MINICARD
13 PCIE_RXP1_MINICARD
13 PCIE_TXN1_MINICARD
13 PCIE_TXP1_MINICARD
WLAN_ON
BUF_PLT_RST# 6,13,14,32
SMB_CLK_S 3,14,16,17,23,32
SMB_DAT_S 3,14,16,17,23,32
WLAN_LED#
Do Not Stuff
R325
10KOhm
/X
Q28
H2N7002
WLAN_ON# 14
H35
H36
A40M20-64AS
+3VAUX_GOLAN
14,26,32 PCIE_WAKE#
WLAN_WAKE#
Q29
Do Not Stuff
/X
R204 0Ohm
2.0G
Title : MINICARD
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size Custom
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 28 of 57



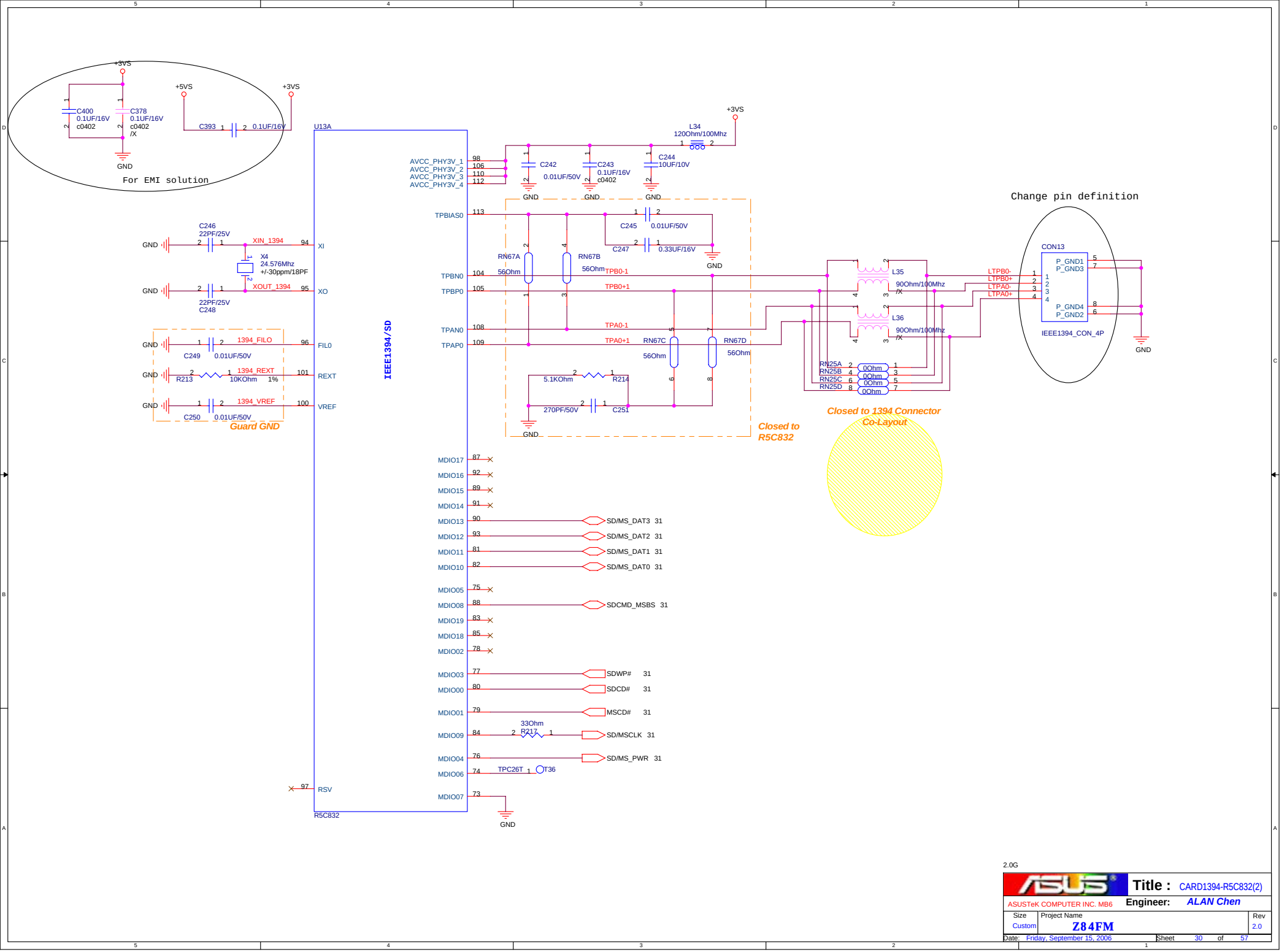
2.0G

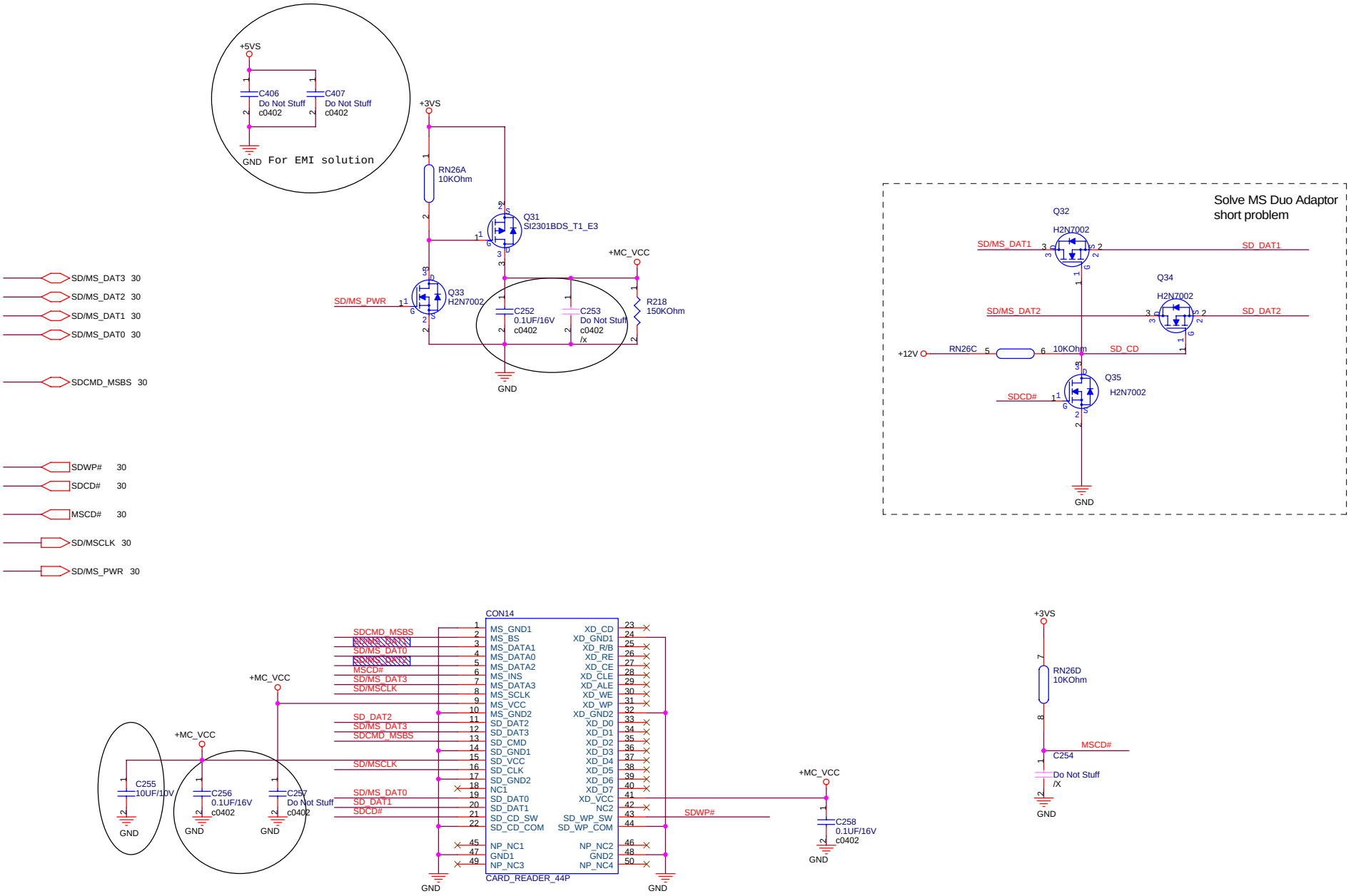
Title : CARD1394-R5C832(1)

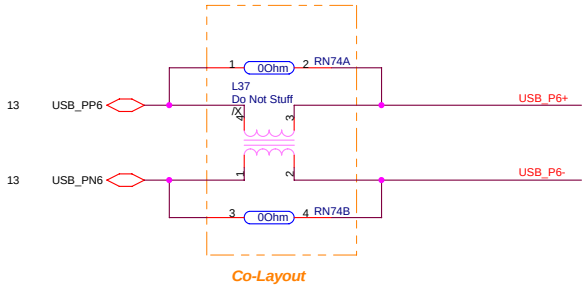
ASUSTeK COMPUTER INC. MB6 Engineer: ALAN Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

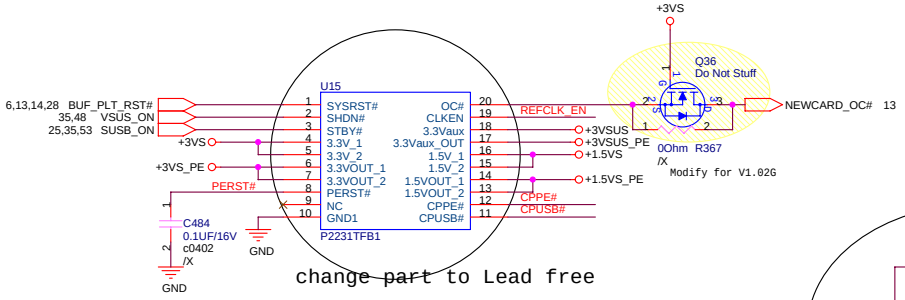
Date: Friday, September 15, 2006 Sheet 29 of 57


+3VS
+5VS
+3VS
C400 0.1UF/16V c0402
C378 0.1UF/16V c0402 /X
C393 0.1UF/16V
GND
For EMI solution
U13A
IEEE1394/SD
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
98
106
110
112
C242 0.01UF/50V
C243 0.1UF/16V c0402
C244 10UF/10V
L34 120Ohm/100Mhz
TPBIAS0
113
C245 0.01UF/50V
C247 0.33UF/16V
RN67A 56Ohm
RN67B 56Ohm
TPBN0
104
TPBP0
105
TPB0-1
TPB0+1
TPAN0
108
TPAP0
109
TPA0-1
TPA0+1
RN67C 56Ohm
RN67D 56Ohm
5.1KOhm R214
270PF/50V C251
C246 22PF/25V
XIN_1394
94
XI
X4 24.576Mhz +/-30ppm/18PF
XOUT_1394
95
XO
22PF/25V C248
1394_FILO
96
FIL0
C249 0.01UF/50V
1394_REXT
101
REXT
R213 10KOhm 1%
1394_VREF
100
VREF
C250 0.01UF/50V
Guard GND
RSV
97
R5C832
MDIO17 87
MDIO16 92
MDIO15 89
MDIO14 91
MDIO13 90
MDIO12 93
MDIO11 81
MDIO10 82
MDIO05 75
MDIO08 88
MDIO19 83
MDIO18 85
MDIO02 78
MDIO03 77
MDIO00 80
MDIO01 79
MDIO09 84
MDIO04 76
MDIO06 74
MDIO07 73
SD/MS_DAT3 31
SD/MS_DAT2 31
SD/MS_DAT1 31
SD/MS_DAT0 31
SDCMD_MSBS 31
SDWP# 31
SDCD# 31
MSCD# 31
33Ohm R217
SD/MSCLK 31
SD/MS_PWR 31
TPC26T T36
Closed to R5C832
L35 90Ohm/100Mhz /X
L36 90Ohm/100Mhz /X
RN25A 0Ohm
RN25B 0Ohm
RN25C 0Ohm
RN25D 0Ohm
Closed to 1394 Connector Co-Layout
Change pin definition
CON13
P_GND1
P_GND3
P_GND4
P_GND2
LTPB0-
LTPB0+
LTPA0-
LTPA0+
IEEE1394_CON_4P
GND
2.0G
Title : CARD1394-R5C832(2)
ASUSTeK COMPUTER INC. MB6
Engineer: ALAN Chen
Size Custom
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 30 of 57

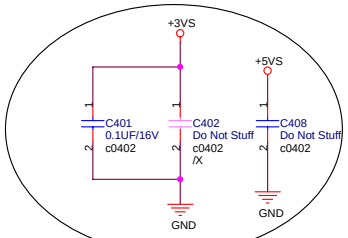

+5VS
C406
Do Not Stuff
c0402
C407
Do Not Stuff
c0402
GND
For EMI solution
+3VS
RN26A
10KOhm
Q31
SI2301BDS_T1_E3
+MC_VCC
SD/MS_PWR
Q33
H2N7002
C252
0.1UF/16V
c0402
C253
Do Not Stuff
c0402
/x
R218
150KOhm
GND
SD/MS_DAT3 30
SD/MS_DAT2 30
SD/MS_DAT1 30
SD/MS_DAT0 30
SDCMD_MSBS 30
SDWP# 30
SDCD# 30
MSCD# 30
SD/MSCLK 30
SD/MS_PWR 30
Solve MS Duo Adaptor
short problem
Q32
H2N7002
SD/MS_DAT1
SD_DAT1
Q34
H2N7002
SD/MS_DAT2
SD_DAT2
+12V
RN26C
10KOhm
SD_CD
Q35
H2N7002
SDCD#
GND
CON14
MS_GND1
MS_BS
MS_DATA1
MS_DATA0
MS_DATA2
MS_INS
MS_DATA3
MS_SCLK
MS_VCC
MS_GND2
SD_DAT2
SD_DAT3
SD_CMD
SD_GND1
SD_VCC
SD_CLK
SD_GND2
NC1
SD_DAT0
SD_DAT1
SD_CD_SW
SD_CD_COM
NP_NC1
GND1
NP_NC3
XD_CD
XD_GND1
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_GND2
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
XD_VCC
NC2
SD_WP_SW
SD_WP_COM
NP_NC2
GND2
NP_NC4
CARD_READER_44P
SDCMD_MSBS
SD/MS_DAT1
SD/MS_DAT0
SD/MS_DAT3
MSCD#
SD/MS_DAT3
SD/MSCLK
SD_DAT2
SD/MS_DAT3
SDCMD_MSBS
SD/MSCLK
SD/MS_DAT0
SD_DAT1
SDCD#
SDWP#
+MC_VCC
C255
10UF/10V
C256
0.1UF/16V
c0402
C257
Do Not Stuff
c0402
C258
0.1UF/16V
c0402
+3VS
RN26D
10KOhm
MSCD#
C254
Do Not Stuff
/X
2.0G
Title : 4 in 1 CARD READER
ASUSTeK COMPUTER INC
Engineer: ALAN CHEN
Size A3
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 31 of 57



Co-Layout



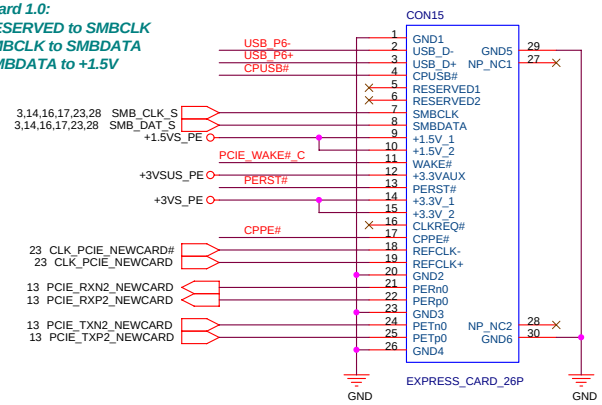
change part to Lead free

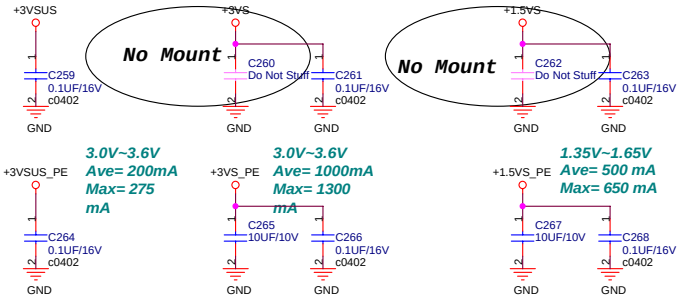


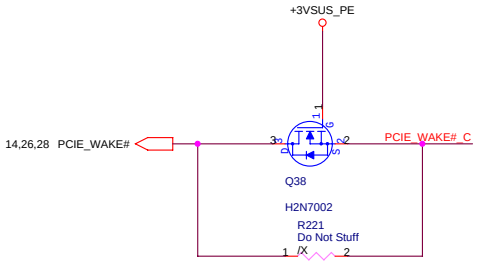
For EMI solution

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

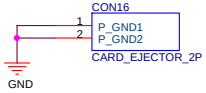
NewCard Header







NewCard Ejecter



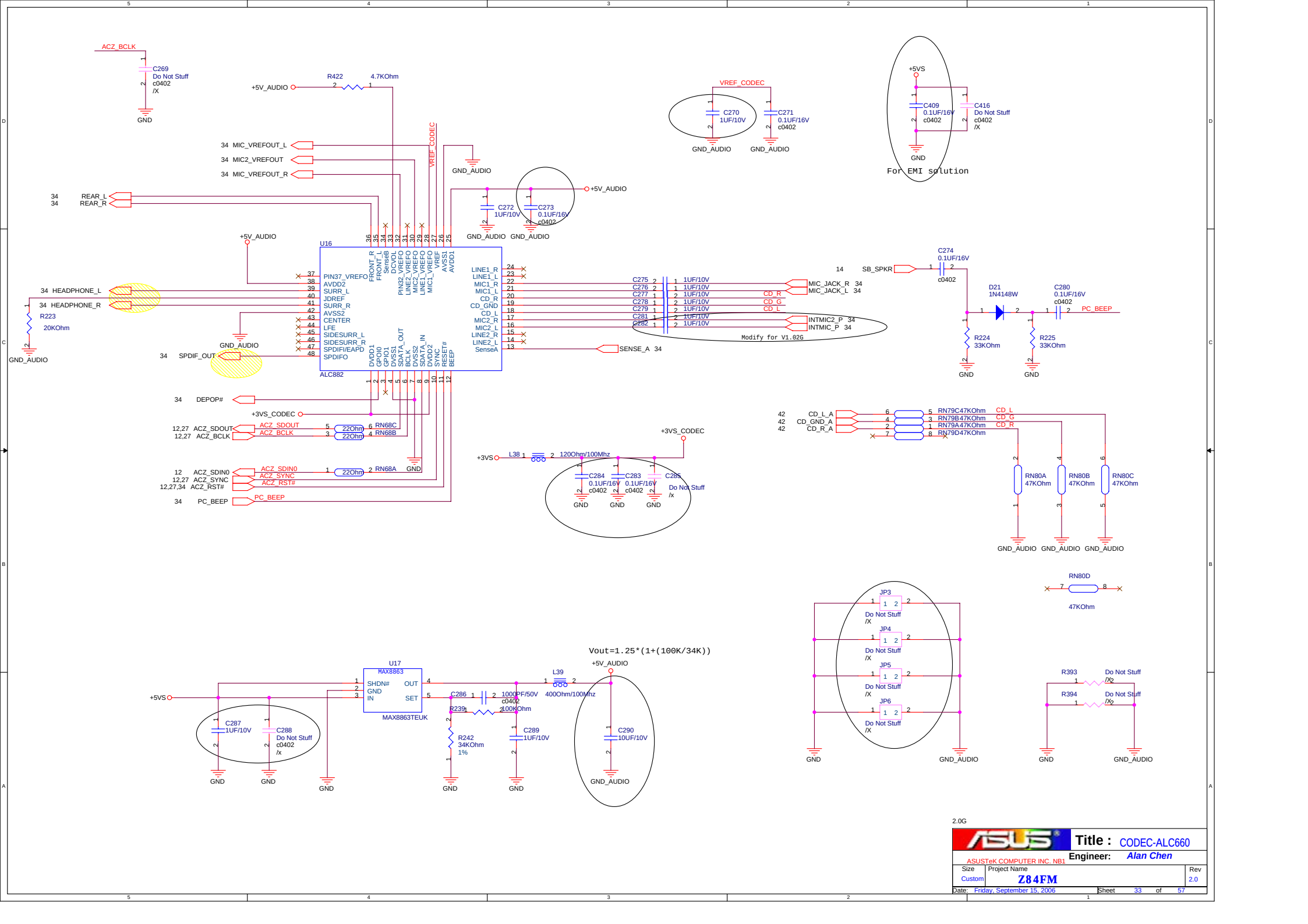
2.0G

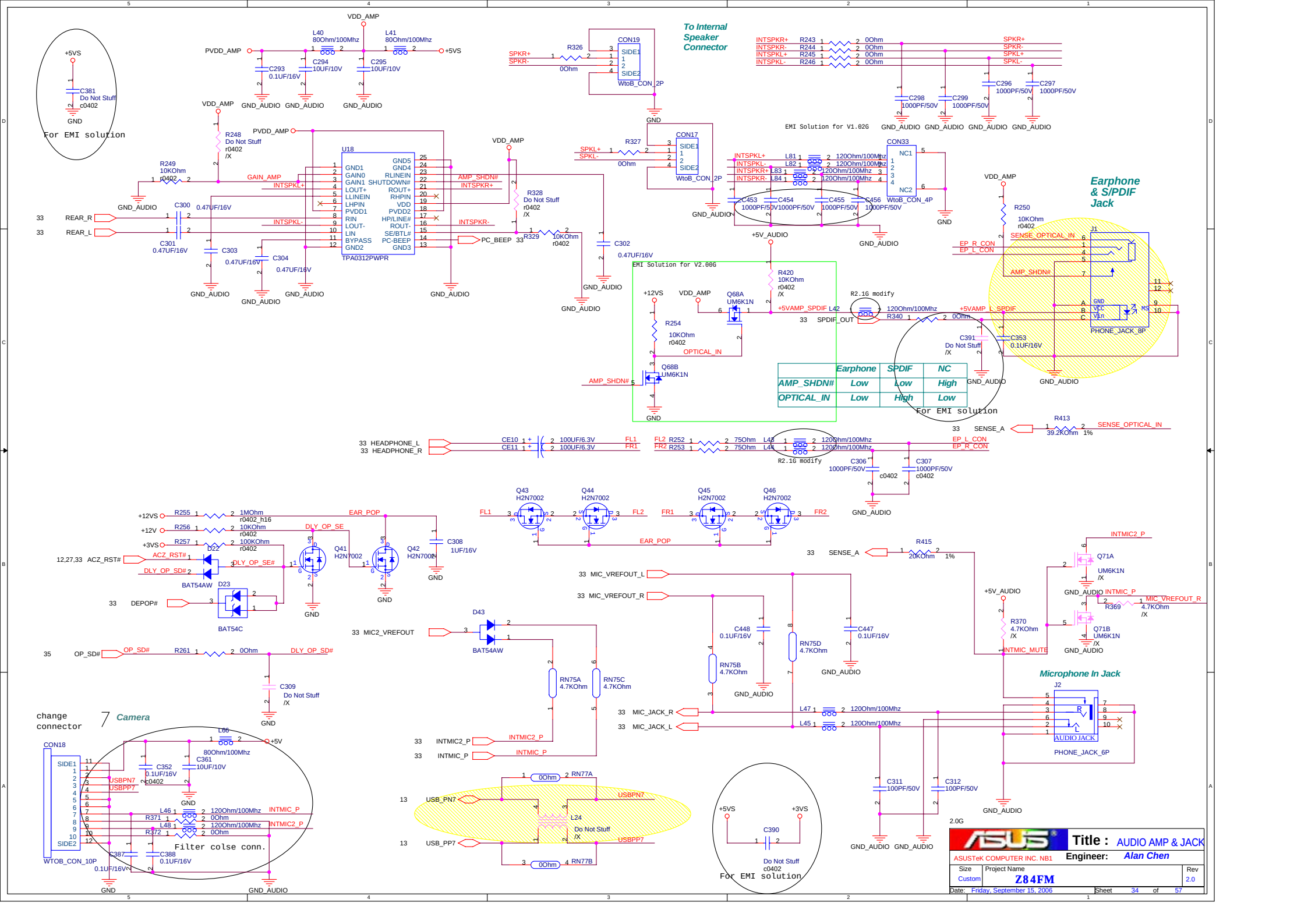
Title : NEWCARD

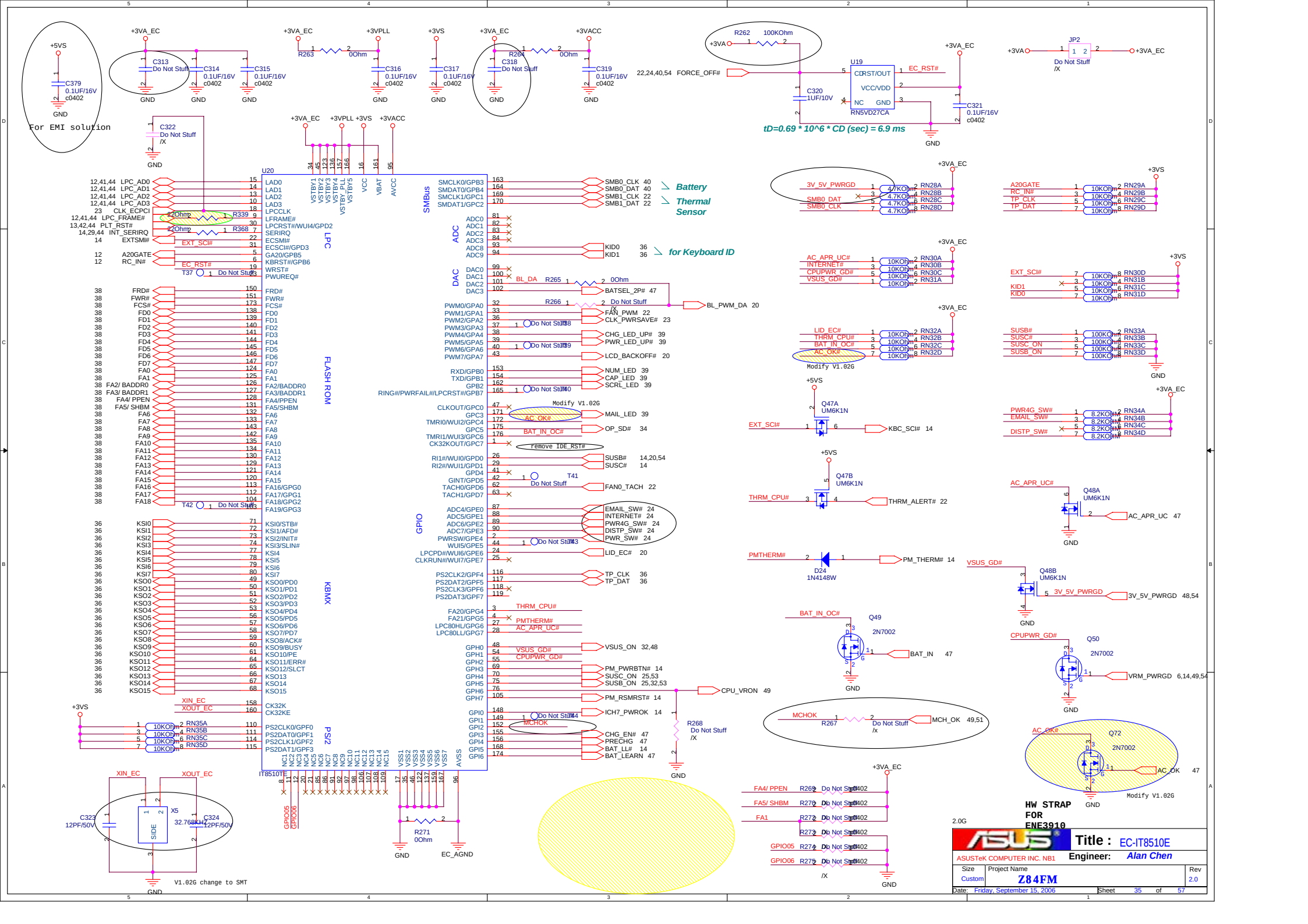
ASUSTeK COMPUTER INC. NB1 Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z84FM	2.0

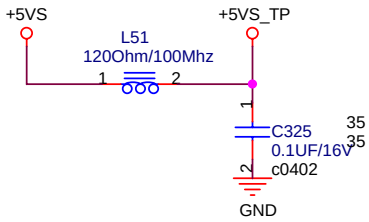
Date: Friday, September 15, 2006 Sheet 32 of 57

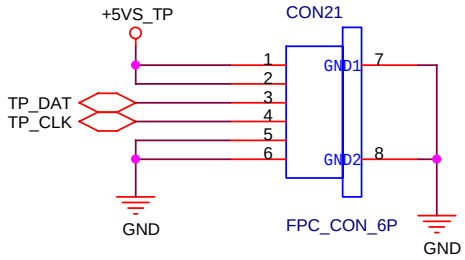

ACZ_BCLK
C269
Do Not Stuff
c0402
/X
GND
R422
4.7KOhm
+5V_AUDIO
34 MIC_VREFOUT_L
34 MIC2_VREFOUT
34 MIC_VREFOUT_R
VREF_CODEC
GND_AUDIO
34 REAR_L
34 REAR_R
C272
1UF/10V
C273
0.1UF/16V
c0402
GND_AUDIO GND_AUDIO
+5V_AUDIO
U16
ALC882
34 HEADPHONE_L
34 HEADPHONE_R
R223
20KOhm
GND_AUDIO
34 SPDIF_OUT
34 DEPOP#
+3VS_CODEC
12,27 ACZ_SDOUT
12,27 ACZ_BCLK
ACZ_SDOUT
ACZ_BCLK
22Ohm
RN68C
RN68B
12 ACZ_SDIN0
12,27 ACZ_SYNC
12,27,34 ACZ_RST#
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#
RN68A
GND
34 PC_BEEP
PC_BEEP
C275 C276 C277 C278 C279 C281 C282
1UF/10V
MIC_JACK_R 34
MIC_JACK_L 34
CD_R
CD_G
CD_L
INTMIC2_P 34
INTMIC_P 34
Modify for V1.02G
SENSE_A 34
VREF_CODEC
C270
1UF/10V
C271
0.1UF/16V
c0402
GND_AUDIO GND_AUDIO
+5VS
C409
0.1UF/16V
c0402
C416
Do Not Stuff
c0402
/X
GND
For EMI solution
14 SB_SPKR
C274
0.1UF/16V
c0402
D21
1N4148W
C280
0.1UF/16V
c0402
PC_BEEP
R224
33KOhm
R225
33KOhm
GND GND
+3VS
L38
120Ohm/100Mhz
C284
0.1UF/16V
c0402
C283
0.1UF/16V
c0402
C285
Do Not Stuff
/x
GND GND GND
+3VS_CODEC
42 CD_L_A
42 CD_GND_A
42 CD_R_A
RN79C47KOhm
RN79B47KOhm
RN79A47KOhm
RN79D47KOhm
CD_L
CD_G
CD_R
RN80A
47KOhm
RN80B
47KOhm
RN80C
47KOhm
GND_AUDIO GND_AUDIO GND_AUDIO
RN80D
47KOhm
JP3
JP4
JP5
JP6
Do Not Stuff
/X
GND
GND_AUDIO
R393
R394
Do Not Stuff
/X2
GND
GND_AUDIO
Vout=1.25*(1+(100K/34K))
U17
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
+5VS
C287
1UF/10V
C288
Do Not Stuff
c0402
/x
GND GND GND
C286
1000PF/50V
c0402
R239
100KOhm
R242
34KOhm
1%
C289
1UF/10V
GND GND
L39
400Ohm/100Mhz
+5V_AUDIO
C290
10UF/10V
GND_AUDIO
2.0G
Title : CODEC-ALC660
Engineer: Alan Chen
ASUSTeK COMPUTER INC. NB1
Size
Custom
Project Name
Z84FM
Rev
2.0
Date: Friday, September 15, 2006
Sheet 33 of 57


To Internal Speaker Connector
Earphone & S/PDIF Jack
Microphone In Jack
Camera
change connector
For EMI solution
EMI Solution for V1.02G
EMI Solution for V2.00G
Filter colse conn.
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chen
Project Name Z84FM
Rev 2.0
Date: Friday, September 15, 2006
Sheet 34 of 57

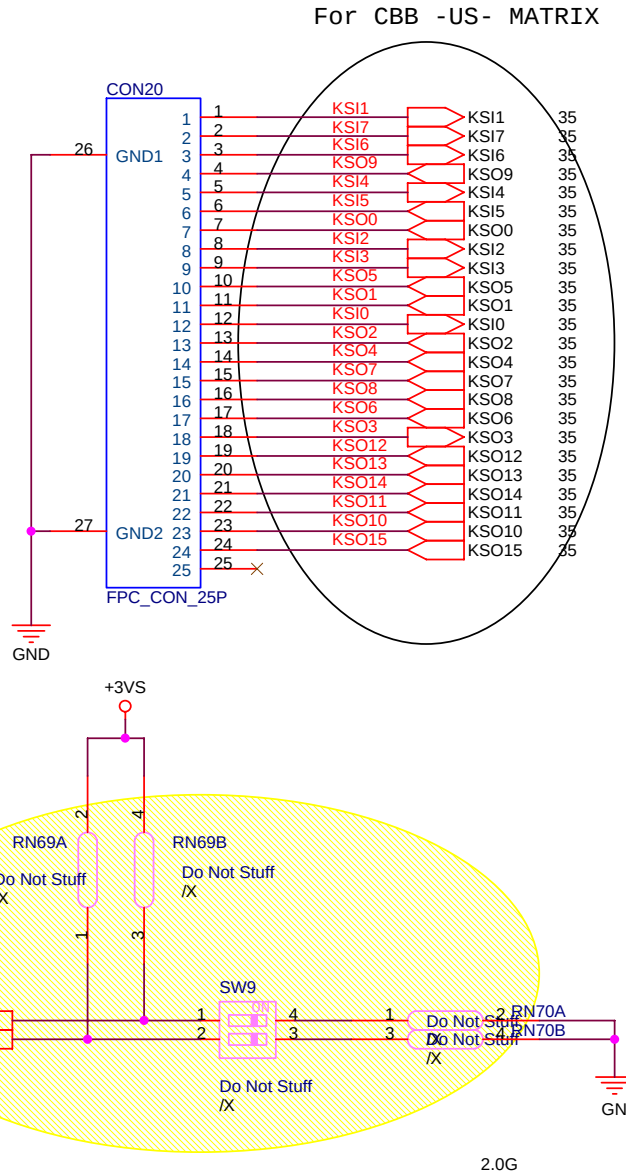

For EMI solution
U20
IT8510TE
LPC
FLASH ROM
KBMX
PS2
GPIO
SMBus
ADC
DAC
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
U19
RN5VD27CA
JP2
Do Not Stuff
/X
HW STRAP FOR ENE3910
2.0G
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chen
Project Name
Z84FM
Rev
2.0
Date: Friday, September 15, 2006
Sheet 35 of 57

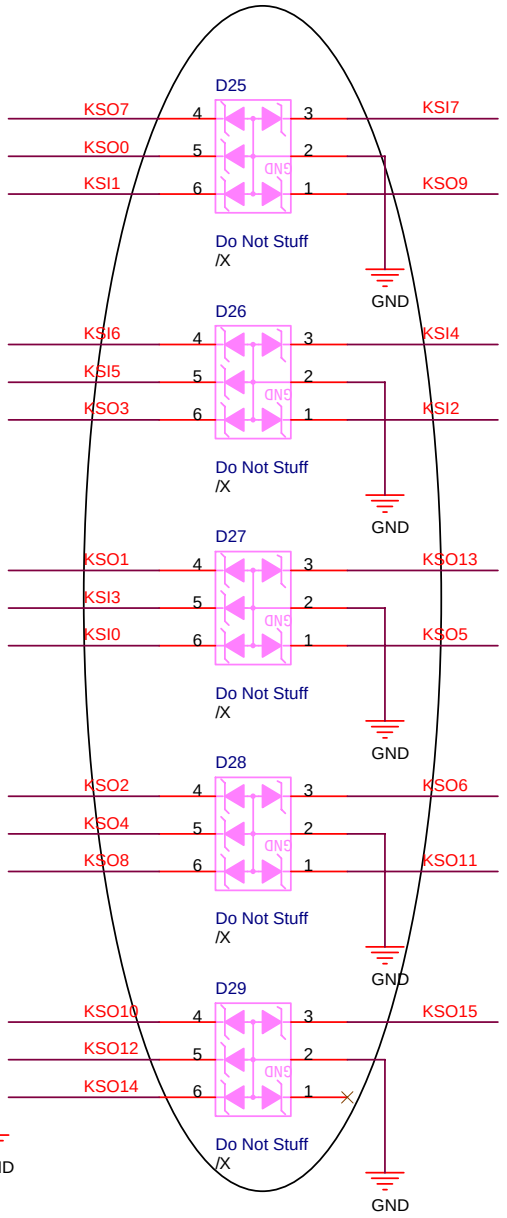
For Touch-Pad





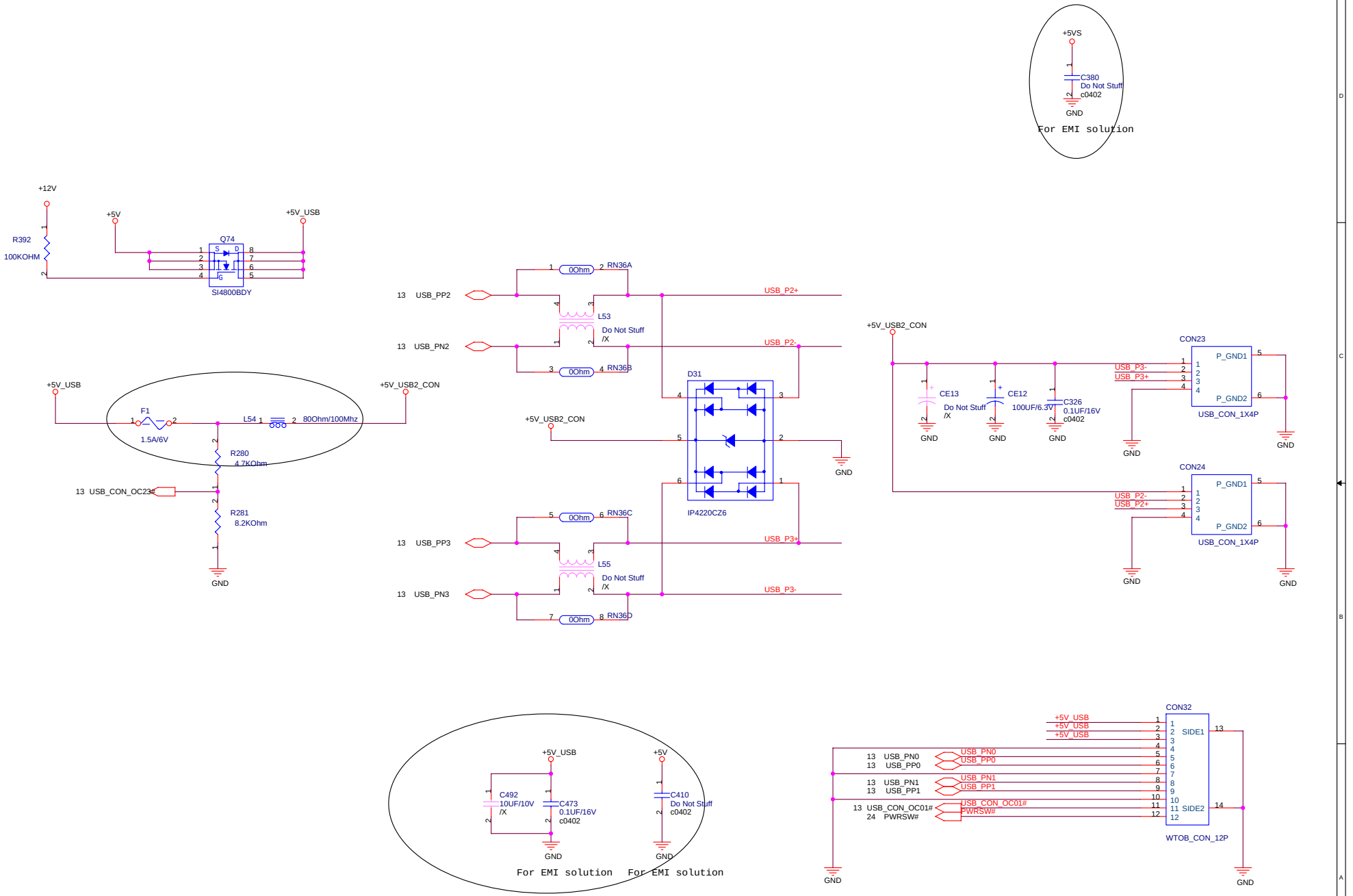
For Keyboard





2.0G

ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: ALAN CHEN	
Size: A4	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 36 of 57	



2.0G

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 37 of 57	

ISA ROM

EC Hardware Strapping

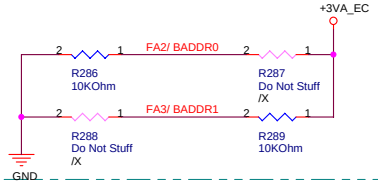
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

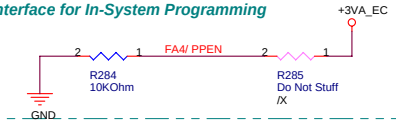


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

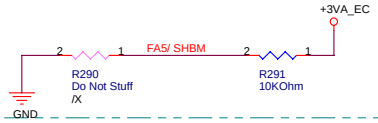
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

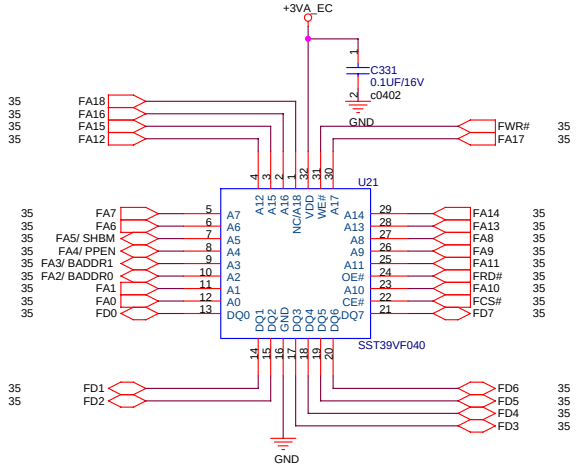


FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



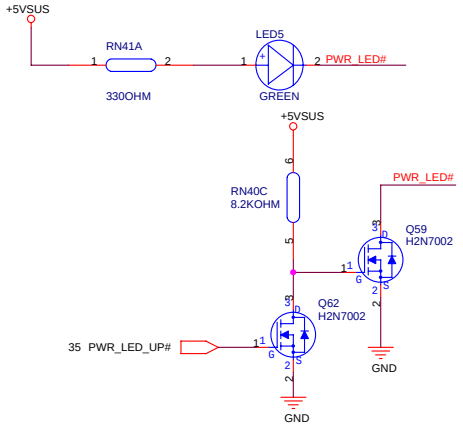


2.0G

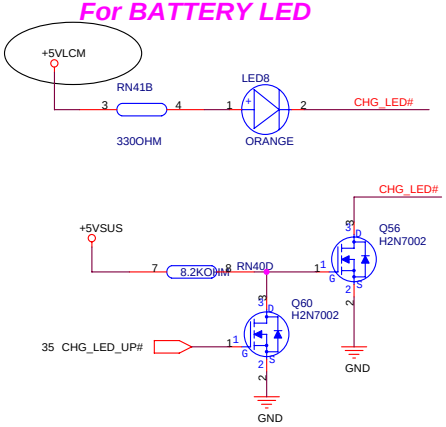
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 38 of 57	

For LED

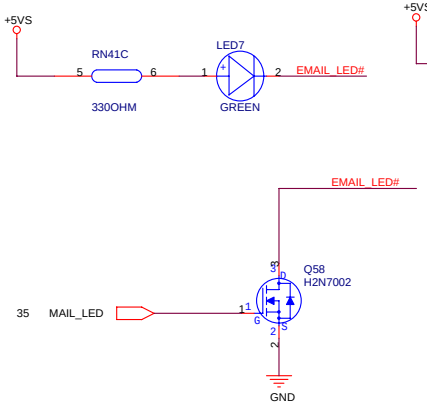
For POWER LED



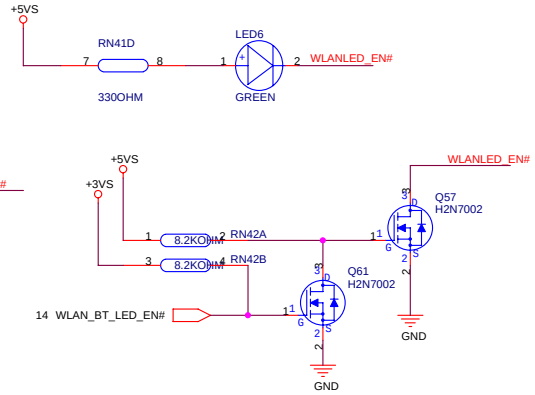
For BATTERY LED



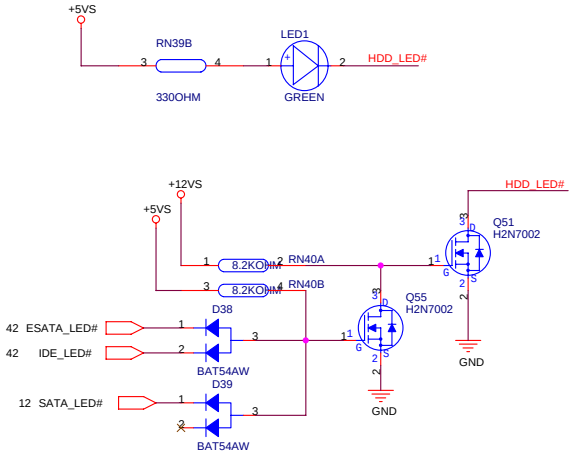
for EMIAL LED



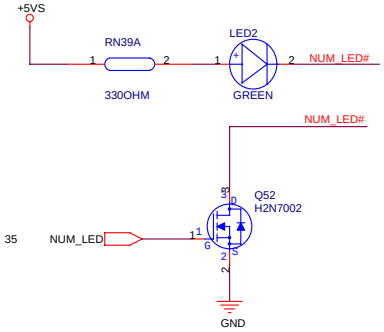
For WireLess LED



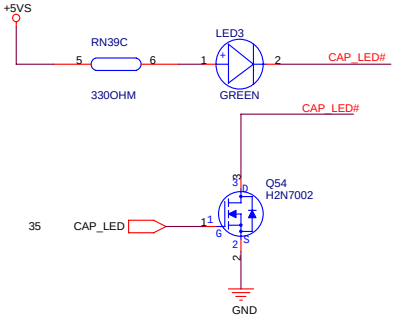
For ESATA/IDE LED



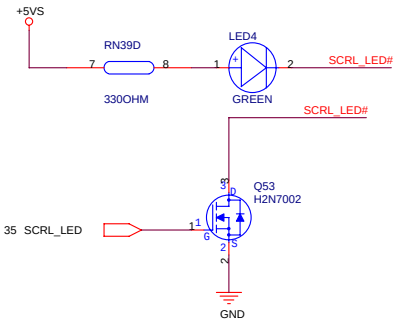
for Num Lock

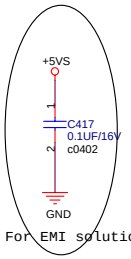


for Cap. Lock



for Scroll Lock



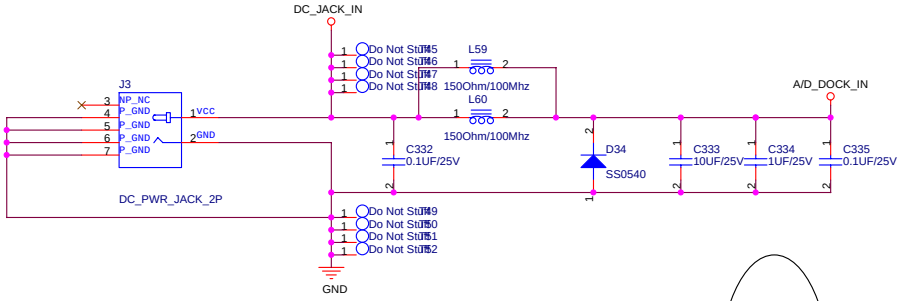


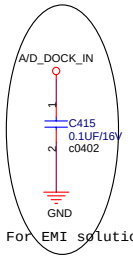
For EMI solution

2.0G

ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 39 of 57	

DC IN

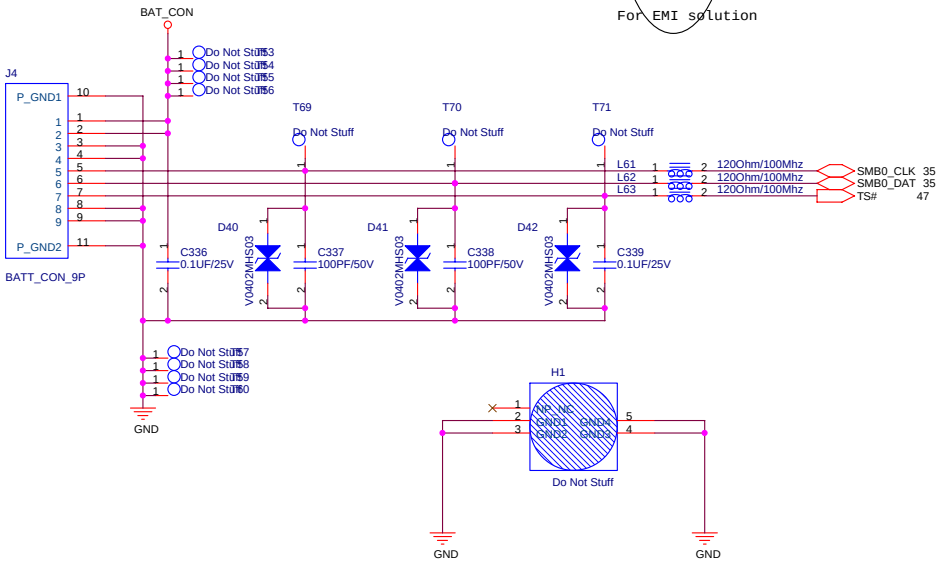




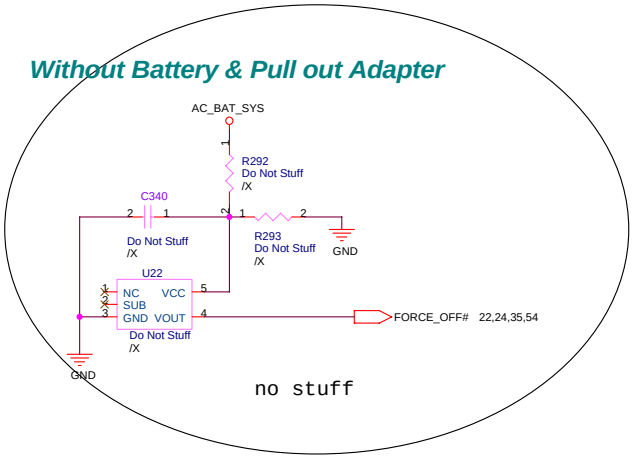
For EMI solution

remove AC DC detect; no need

BAT IN



Without Battery & Pull out Adapter

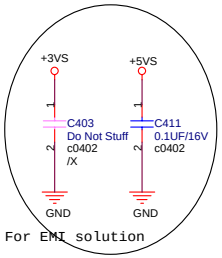


no stuff

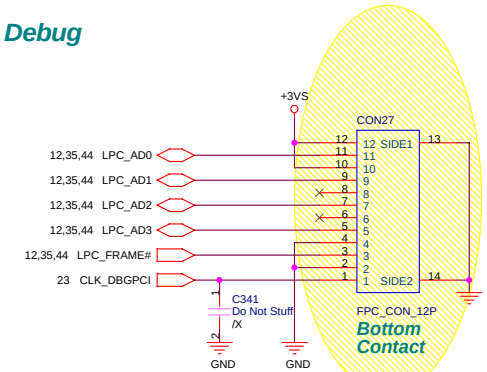
2.0G

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 40 of 57	

For Debug



For EMI solution



pin swap;by F3J

2.0G

ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 41 of 57	

HD_CSEL : Pull-Down, HDD as Master

ESATA & PATA HDD

ODD

Place near pin 16,32,44

Place near the PIN18

Place near pin 9, 21

Place near pin 4

Place near pin 1,33,41

Place near the PIN6

Normal type
High: Slave
Low : Master

For EMI solution

For EMI solution

Title :	SATA-HDD & ODD
ASUSTeK COMPUTER INC. NB1	Engineer: Alan Chen
Size: Custom	Project Name: Z84FM
Rev: 2.0	
Date: Friday, September 15, 2006	Sheet 42 of 57

FOR LEFT UNDER

FOR FAN

FOR RIGHT UP

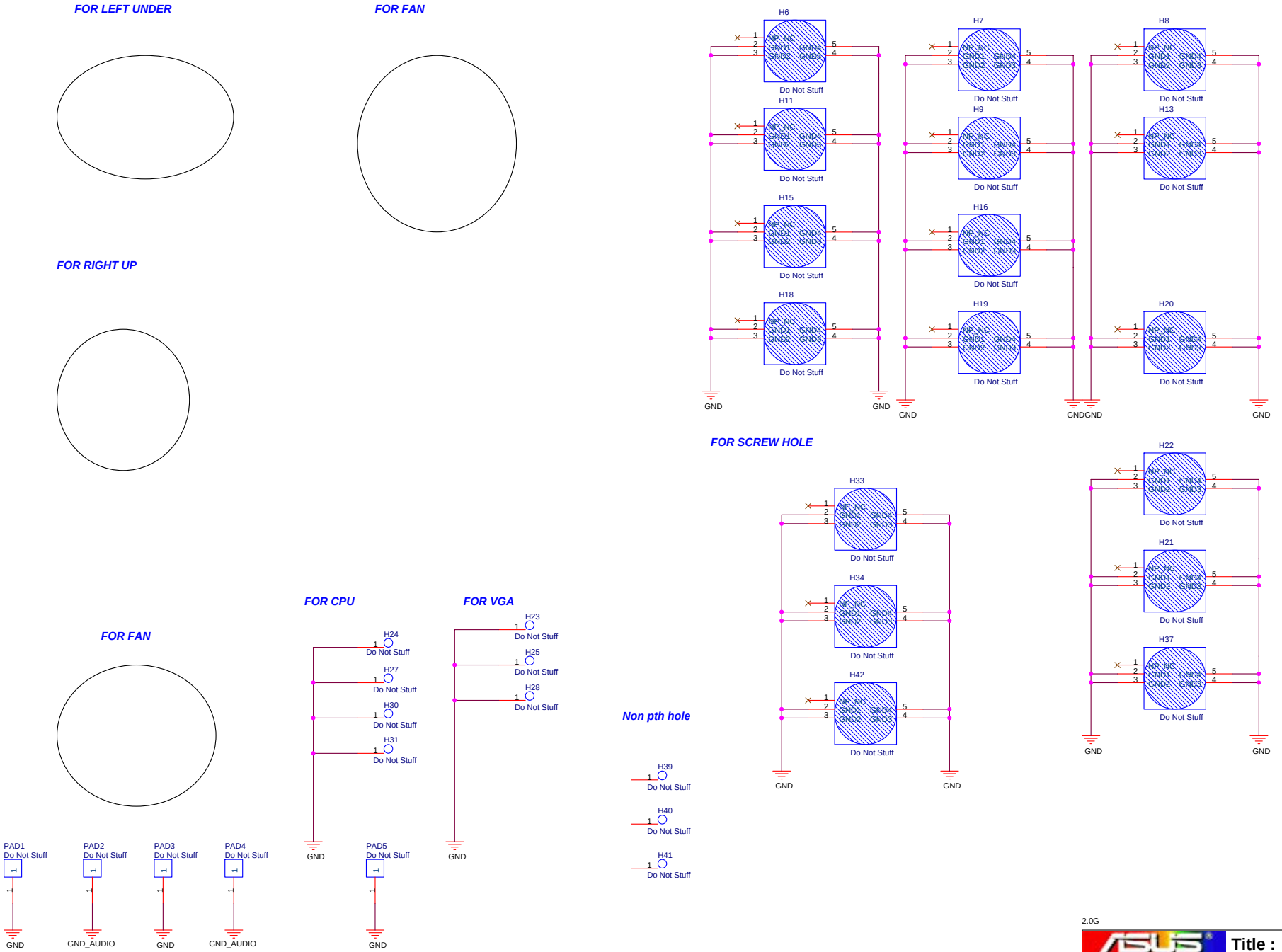
FOR FAN

FOR CPU

FOR VGA

Non pth hole

FOR SCREW HOLE



2.0G

Title : SREW HOLE

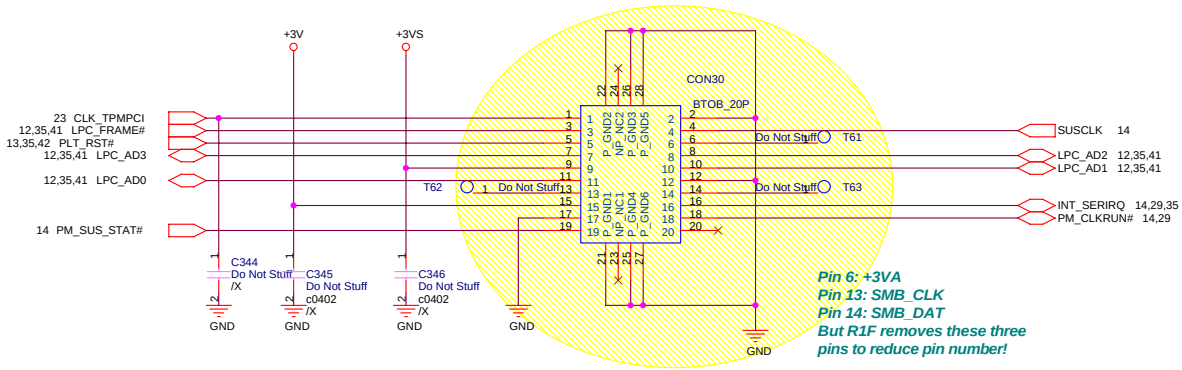
ASUSTeK COMPUTER INC

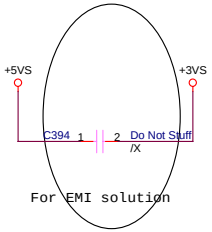
Engineer: ALan Chen

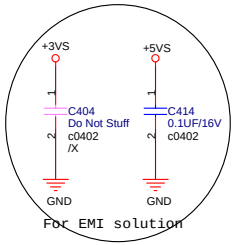
Size	Project Name	Rev
Custom	Z84FM	2.0

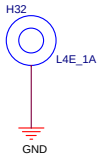
Date: Friday, September 15, 2006 Sheet 43 of 57

For TPM Module





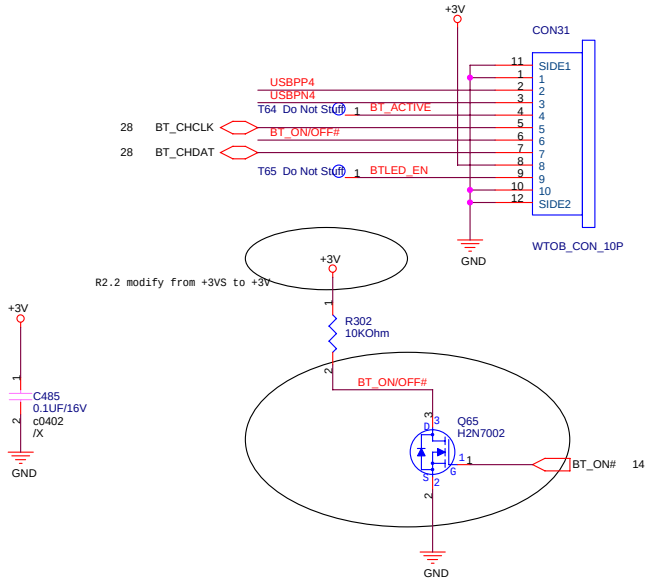


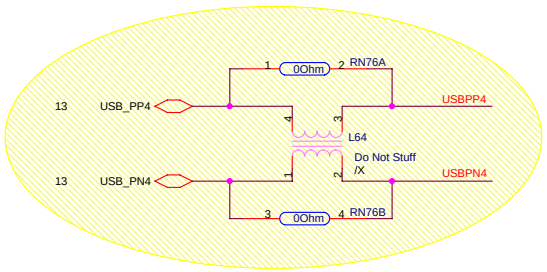


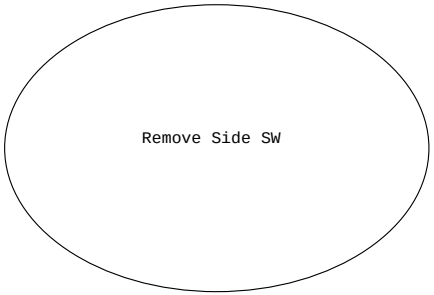
2.0G

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 44 of 57	

For Bluetooth

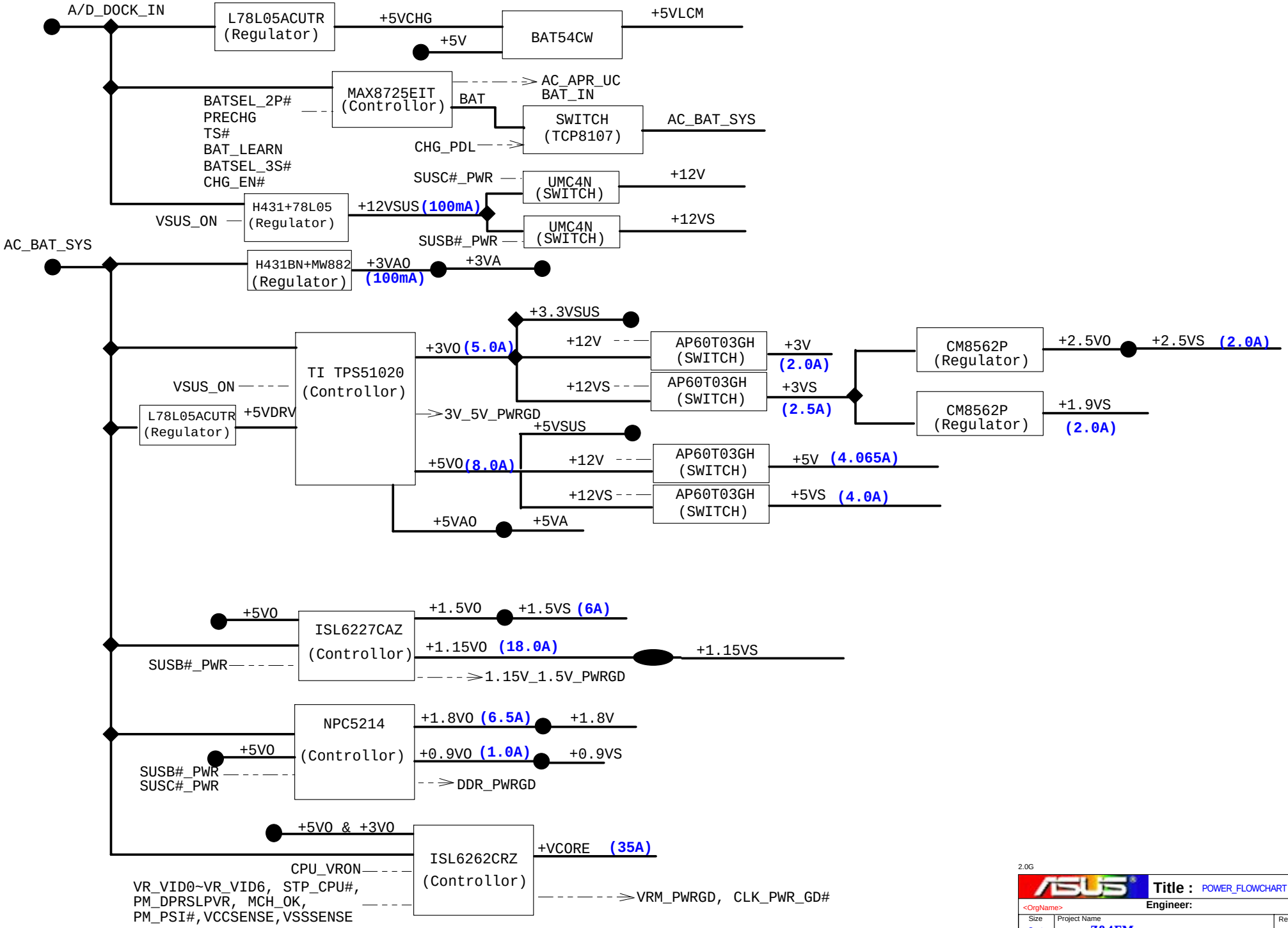






2.0G

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 45 of 57	



2.0G

Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 46 of 57

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]

VCLS= 2.865V

Adaptor Max. Current :

PR5718=20K PR5714 = 178K; Ilimit = 4.5A; 90W

PR5718=27K PR5714 = 47K; Ilimit = 3.175A; 60W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }

VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

Victl = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Victl = 2.084V

=> Icharge = 1.6933A

BATSEL_2P# = 0, 6 or 9 Cells; Victl = 2.111V

=> Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells

2.0 > Vmode > 1.6V (floating) ----> 3 Cells

0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

Rev2.0 power update

Rev1.2 power update

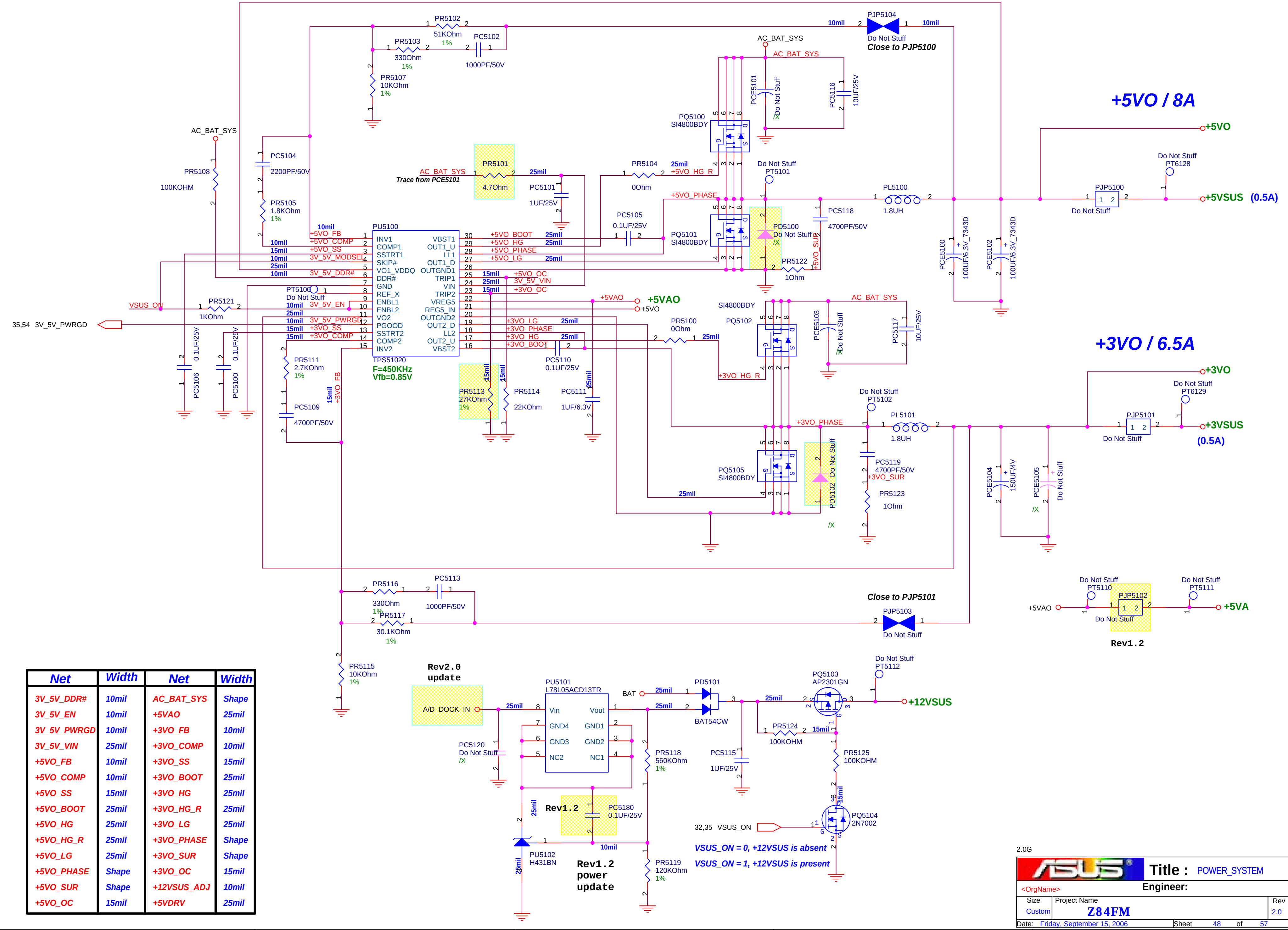
Title : POWER_CHARGER

Engineer:

<OrgName>

Size: C | Project Name: Z84FM | Rev: 2.0

Date: Friday, September 15, 2006 | Sheet 47 of 57



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

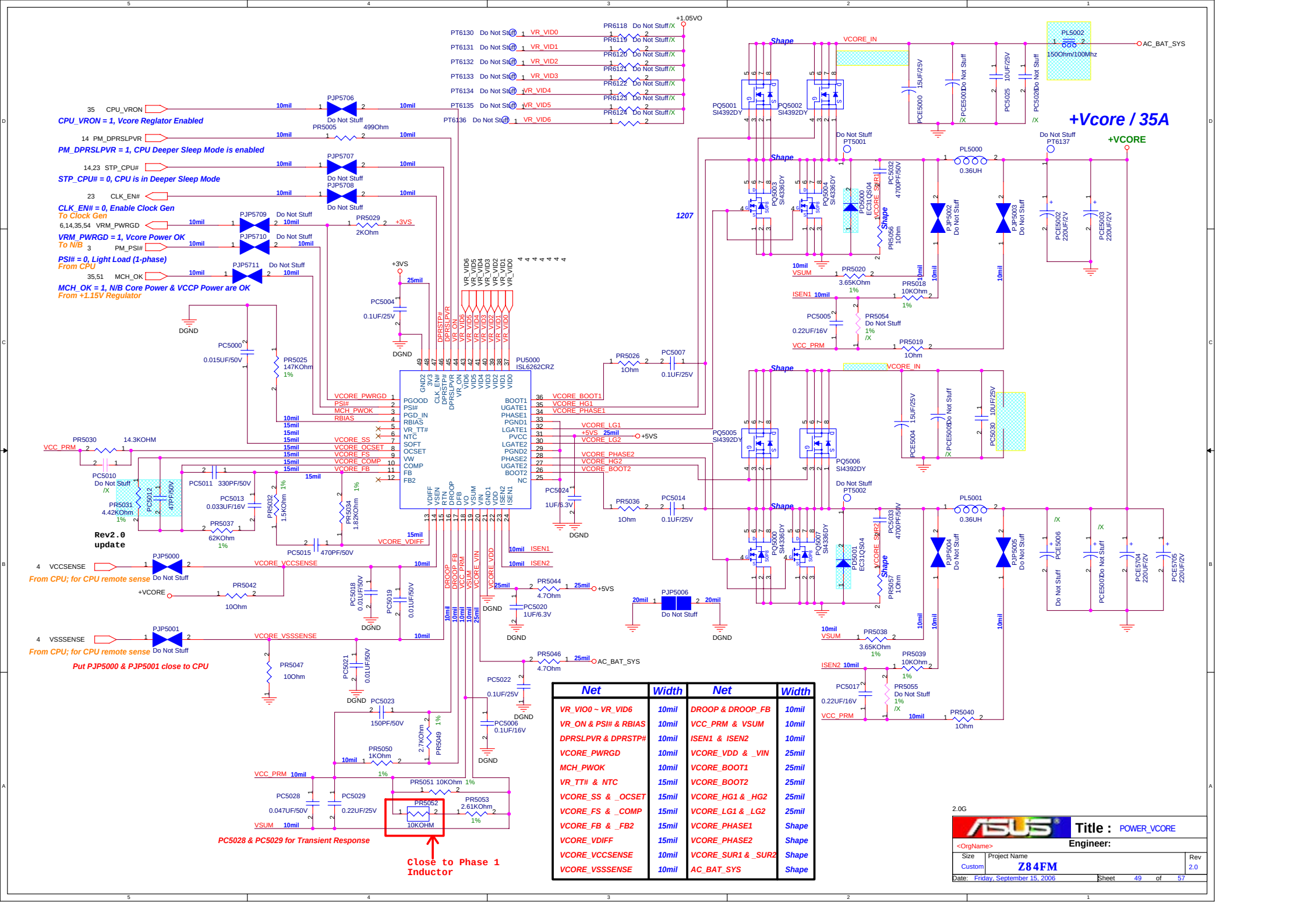
2.0G

Title : POWER_SYSTEM

<OrgName> Engineer:

Size: Custom | Project Name: Z84FM | Rev: 2.0

Date: Friday, September 15, 2006 | Sheet 48 of 57



Net	Width	Net	Width
VR_VID0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

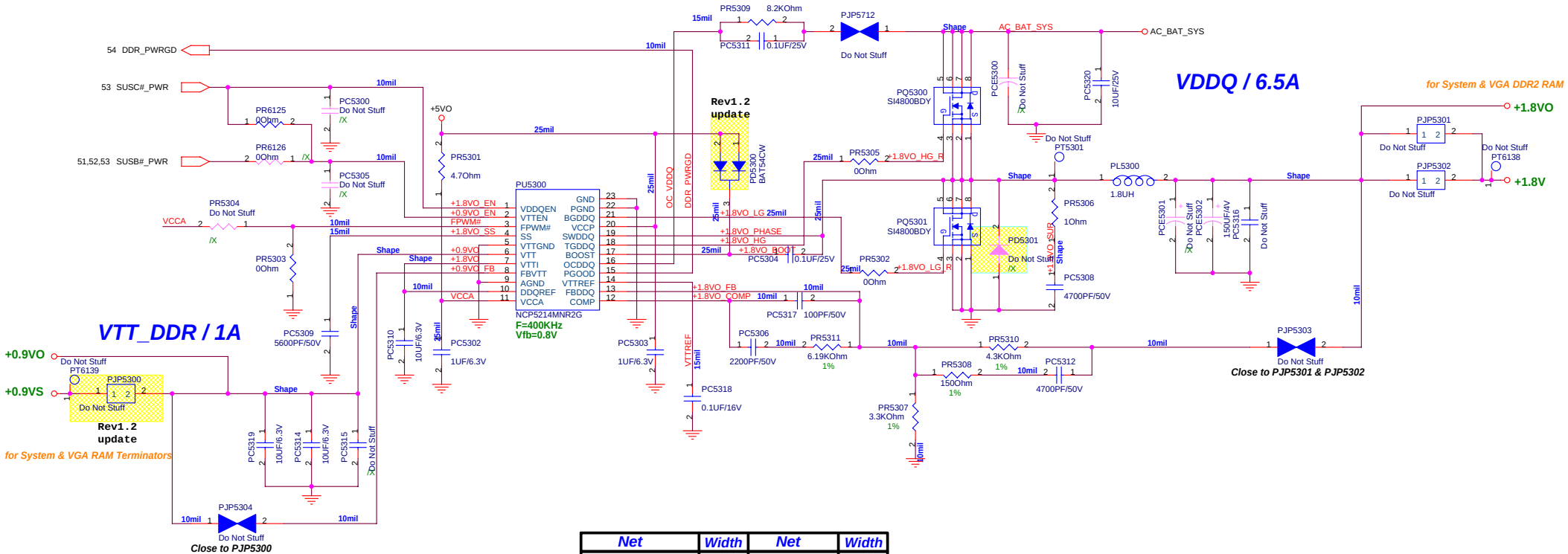
2.0G

Title : POWER_VCORE

<OrgName> Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 49 of 57



Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

2.0G

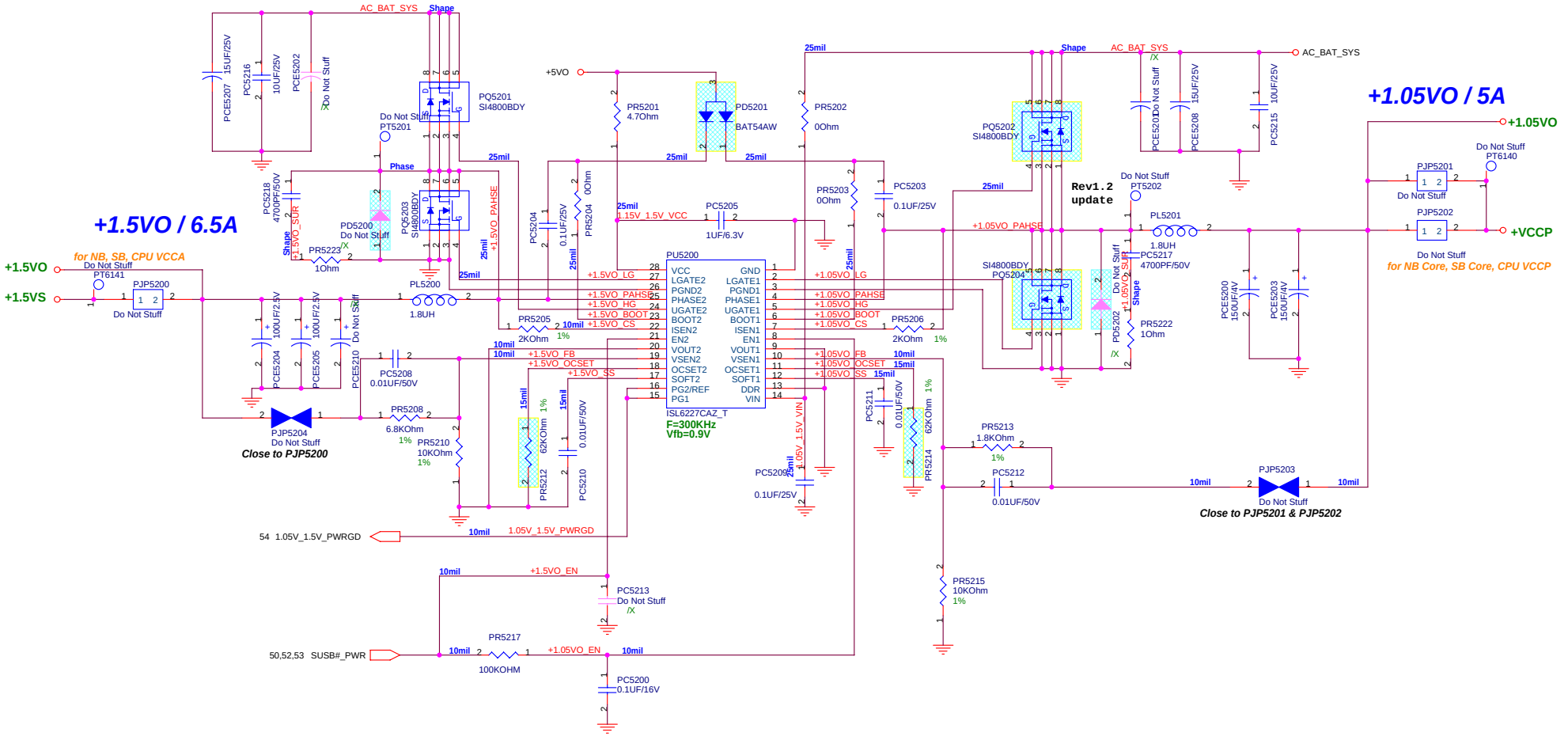
Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 50 of 57



Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

2.0G

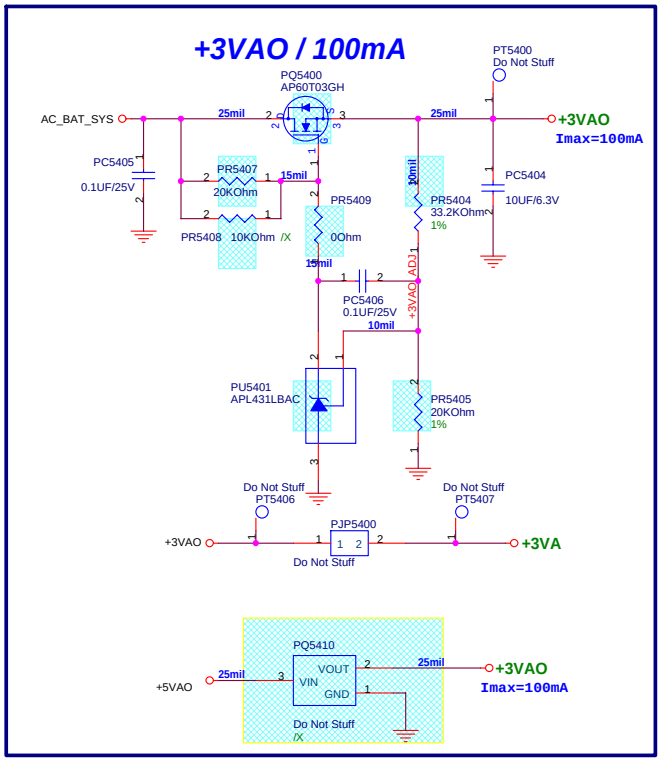
Title : POWER_I/O_1.5VS & 1.05VS

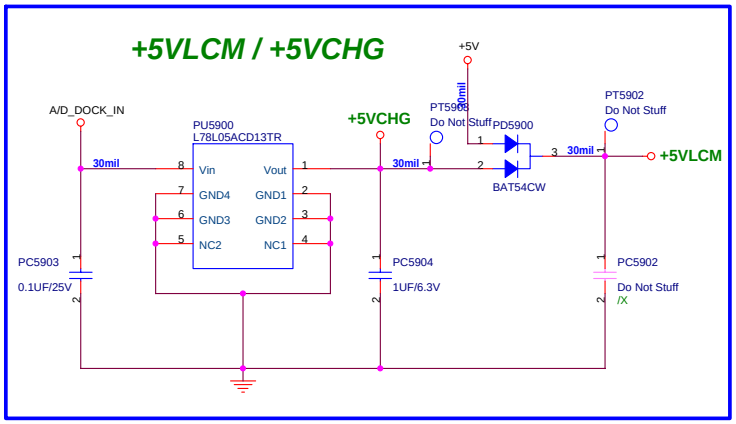
<OrgName>

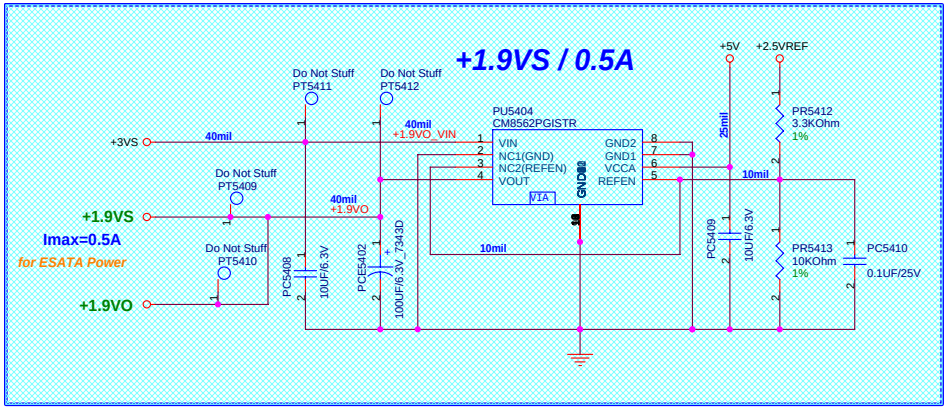
Engineer:

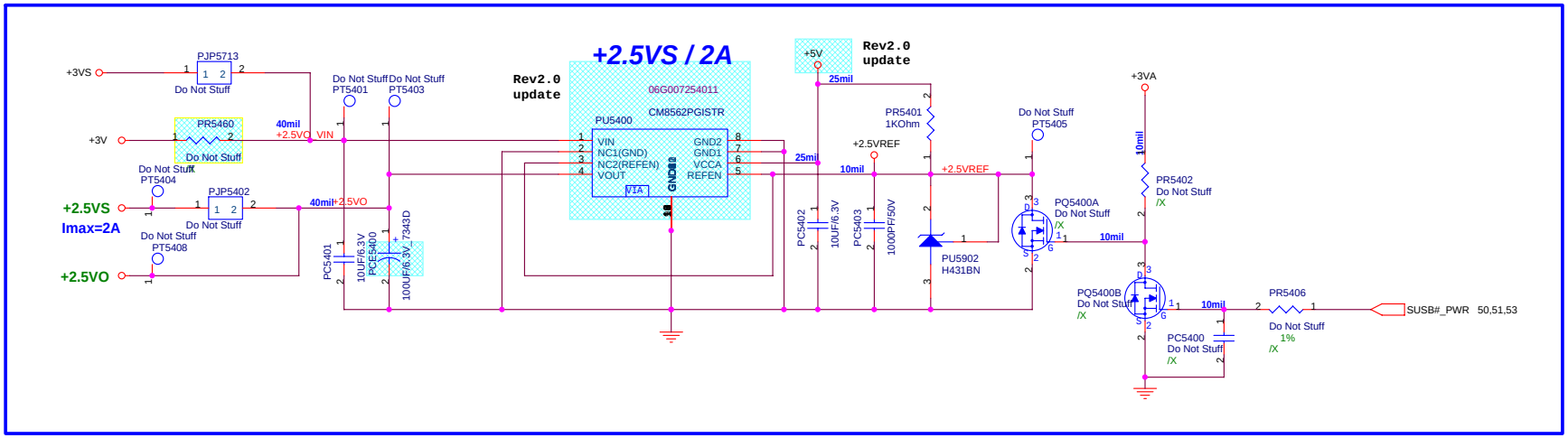
Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 51 of 57









2.0G

ASUS

Title : POWER_I/O_+3VA & +2.5V

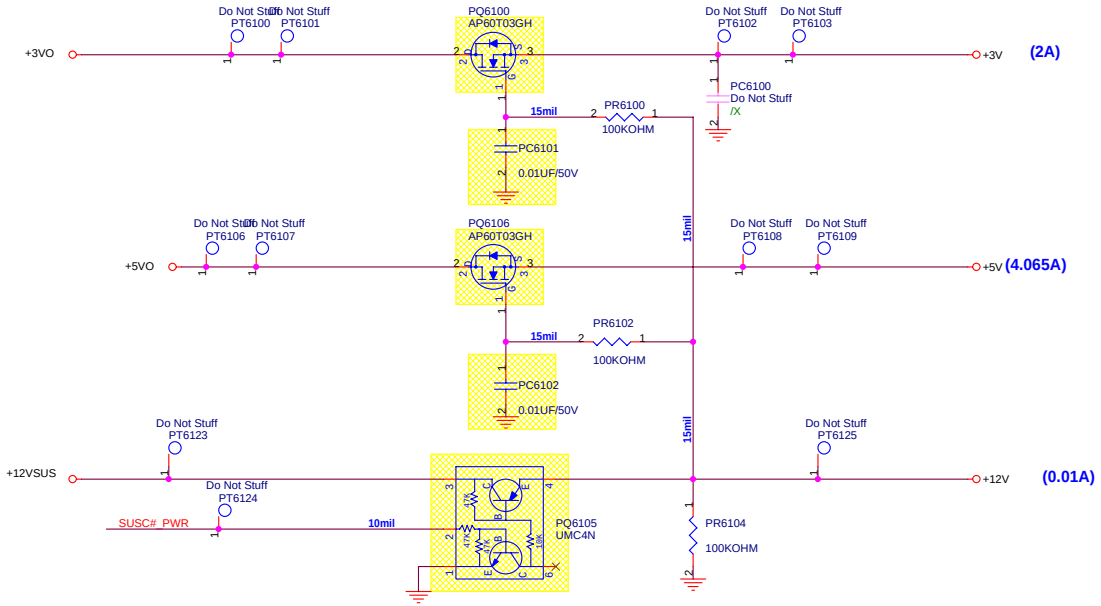
<OrgName>

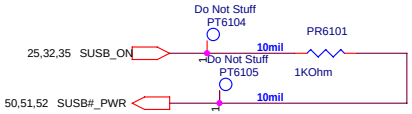
Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

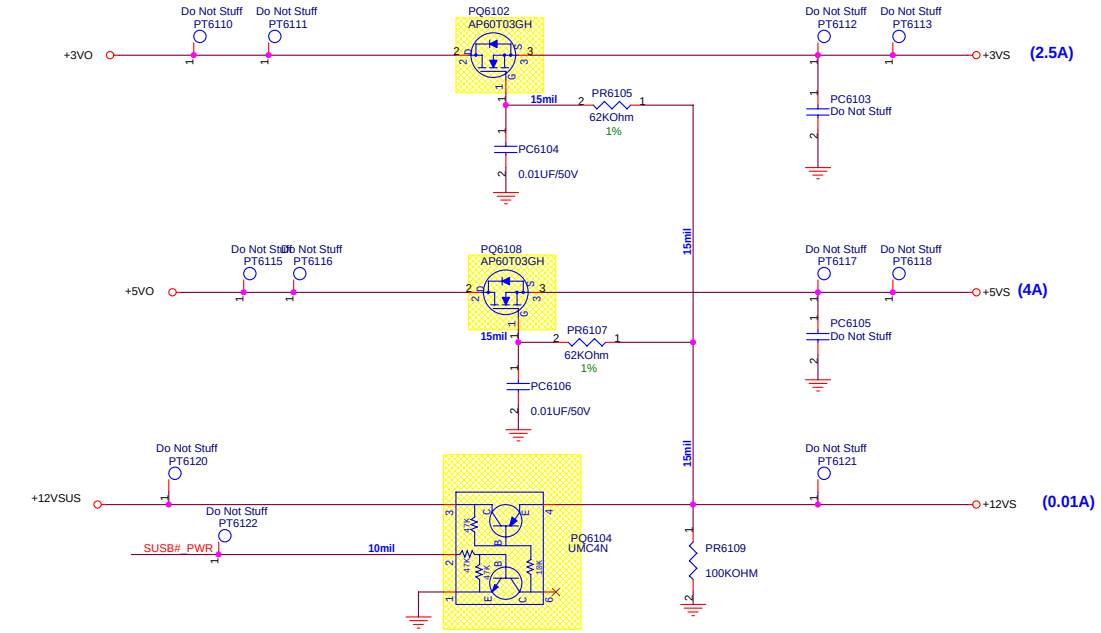
Date: Friday, September 15, 2006 Sheet 52 of 57

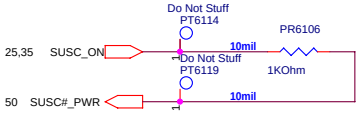
SUSC#_PWR POWER





SUSB#_PWR POWER

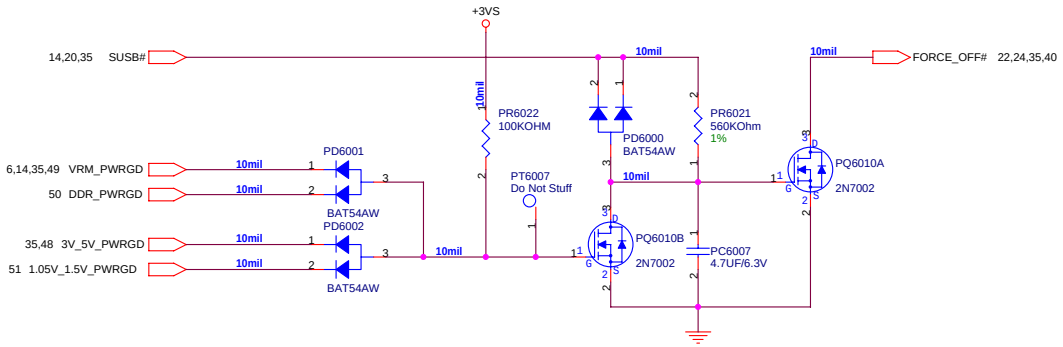


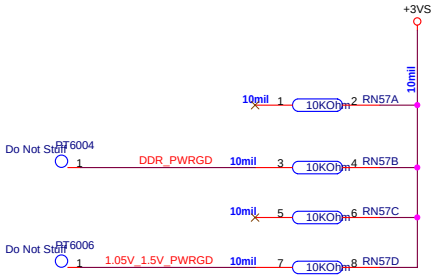


2.0G

Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 53 of 57	

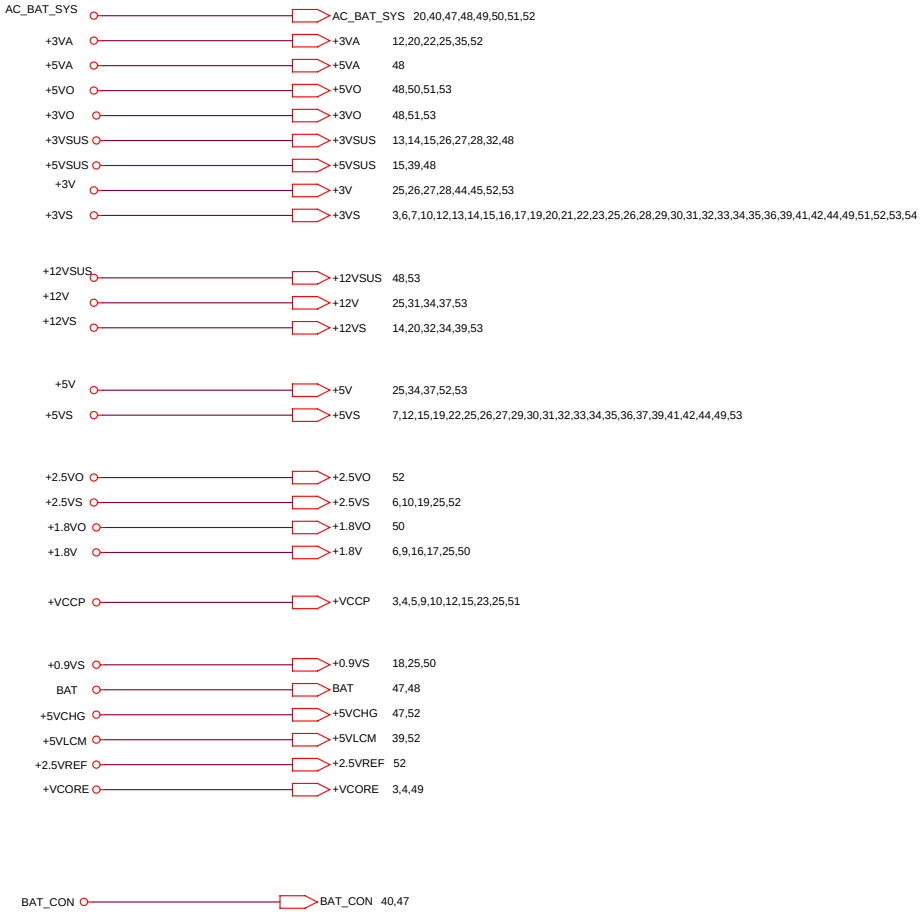
Power Good Detecter





2.0G

Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: Z84FM	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 54 of 57	



2.0G

Title : POWER_SIGNAL

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 55 of 57

Rev	Date	Description
1.0	08/04/06	Refer Z84F R2.2G
1.0	08/04/06	1. Change PATA to SATA<p42>
1.0	08/08/06	2.Modify Audio circuit for Jack-sense<P33 & P34>
1.0	08/08/06	3.Add D40,D41,D42 for Battery varistor<P40>
1.0	08/08/06	4.Modify inverter connector pin define<P20>
1.0	08/08/06	5.Change CON5 Connector from 10pin to 12pin <p20>
1.0	08/10/06	6.ADD PR6125,PR6126 for DDR&VTT on S3 issue<P50>
1.0	08/10/06	7.Change CON21 touch pad connector type<P36>
1.0	08/10/06	8.Change J2 connector type for Azalia <P34>
1.0	08/10/06	9.Add C484,C485,C486,C487 for EMI Solution<P32>
2.0	08/16/06	1.Add D43 and Del R422 for MIC2_VREFOUT issue<P33&P34>
2.0	09/11/06	2.R408 from 24.9 ohm change to 20 ohm for SATA eye-patten issue<P12>
2.0	09/12/06	3.PC5005, PC5017 from 0.1uF change to 0.22uF for Power solution<p49>
2.0	09/13/06	4.Add C488,C489,C490,C491,C492 and C493 for EMI solution<P42>
2.0	09/13/06	5.C481, C482 and C483 from /N change to load for EMI solution<P42>

Rev	Date	Description

2.0G

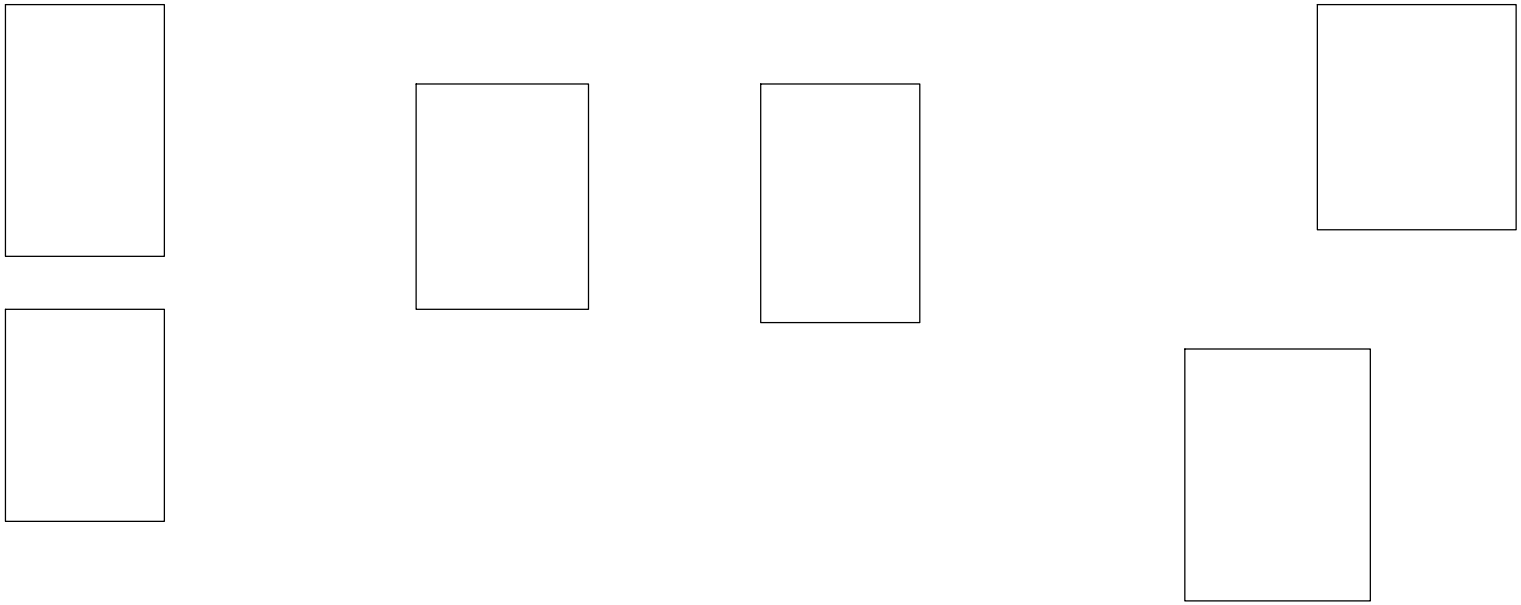
Title : History

ASUSTek COMPUTER INC

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z84FM	2.0

Date: Friday, September 15, 2006 Sheet 56 of 57



2.0G

ASUSTeK COMPUTER INC	Title : <Title>	
	Engineer: *Alan Chu*	
Size: A3	Project Name: **Z84FM**	Rev: 2.0
Date: Friday, September 15, 2006	Sheet 57 of 57	