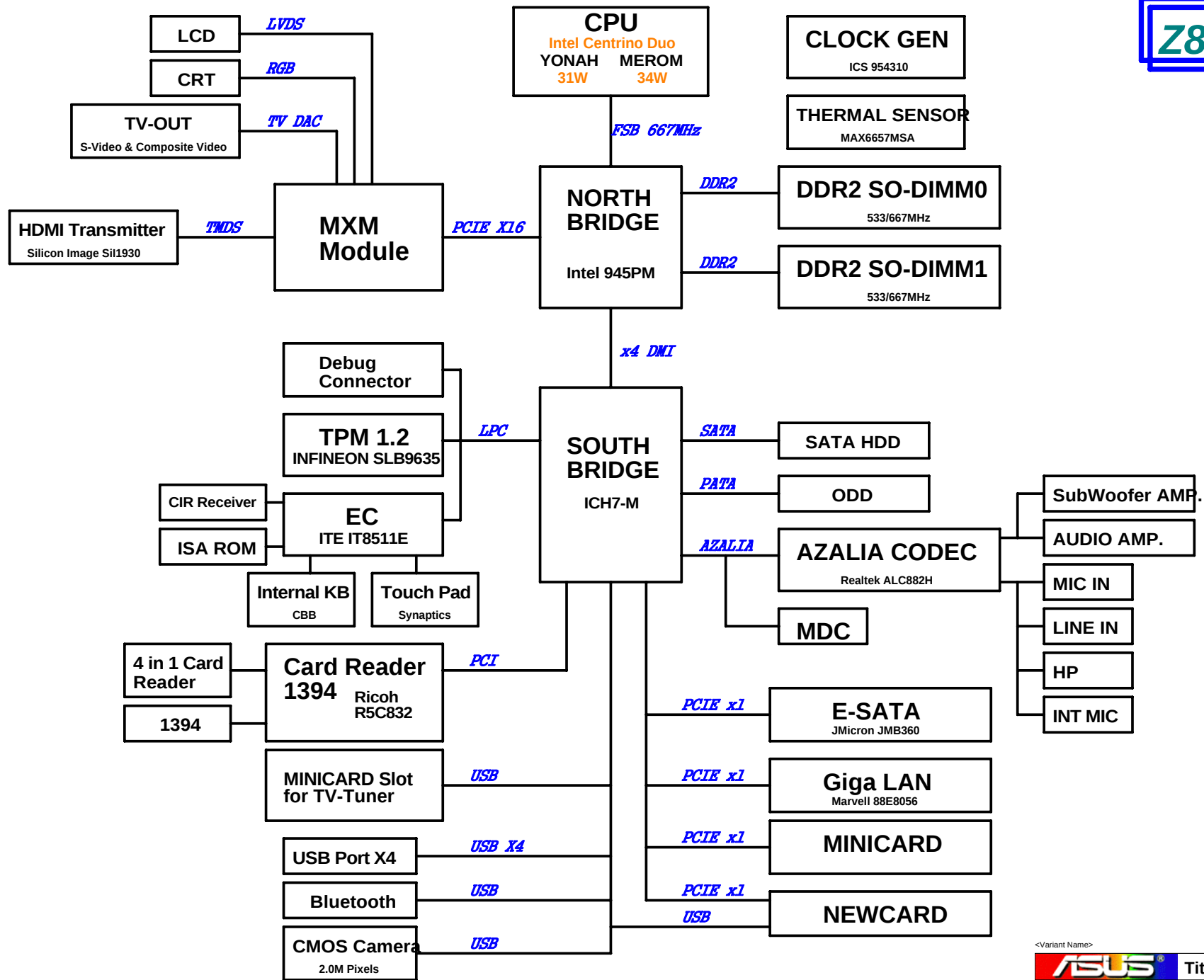




Z84J

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMR10/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4/GPD2	PLT_RST#	I
31	ECSC1#/GPD3	EXT_SC#	O
41	GPD4	/	
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	PWR4G_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWR5W/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I
115	PS2DAT1/GPF3	/	I
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

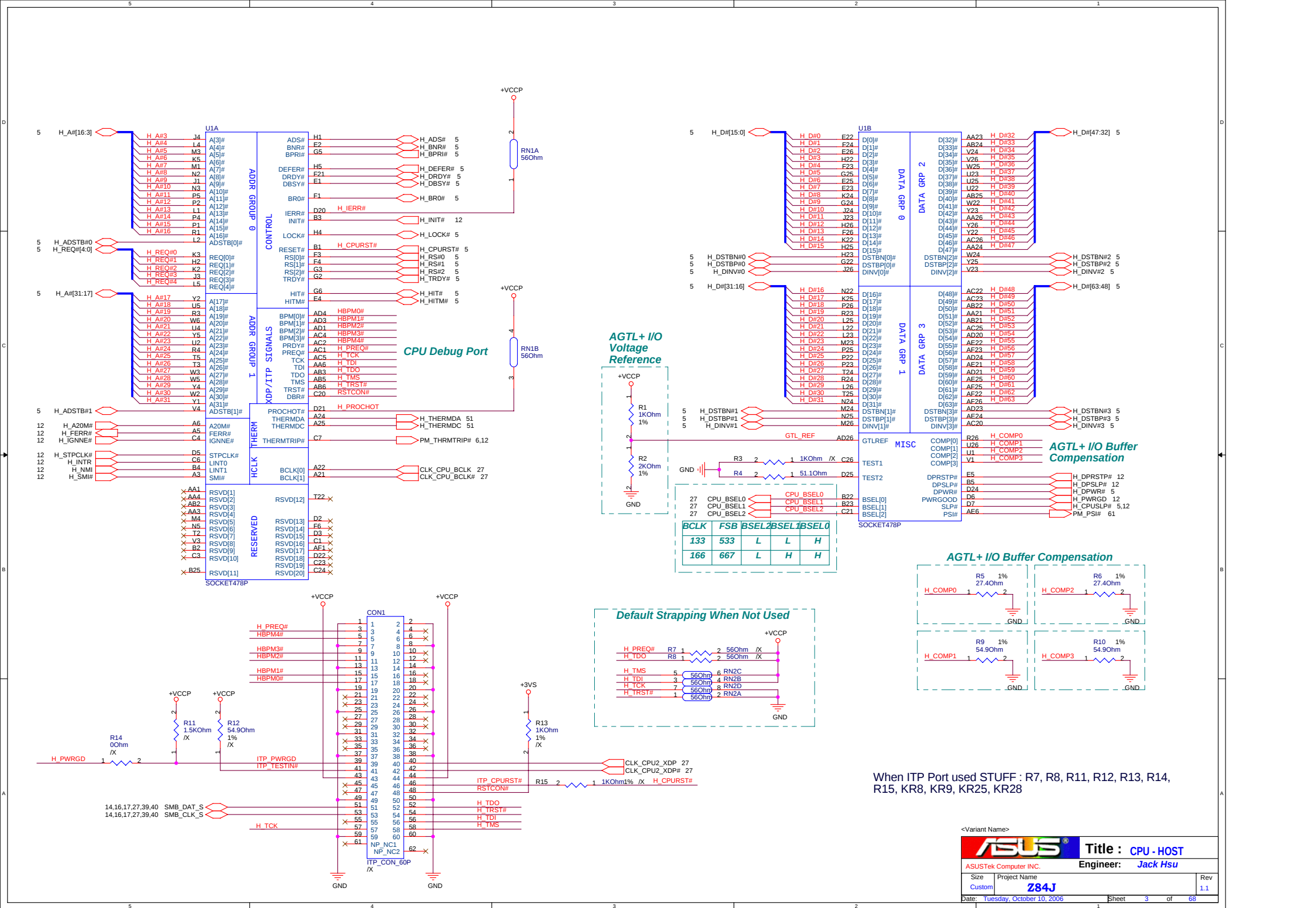
Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	I	V_CPU_IO	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	INTB-->INTB
1394	AD17	0	INTA-->INTA
LAN	AD16	REQ#2/GNT#2	INTA-->INTD

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

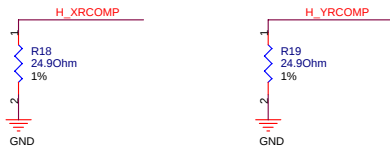
<Variant Name>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size Custom	Project Name 284J	Rev 1.1	
Date: Tuesday, October 10, 2006		Sheet	2 of 68



RCOMP

For Calibrating the FSB I/O Buffer



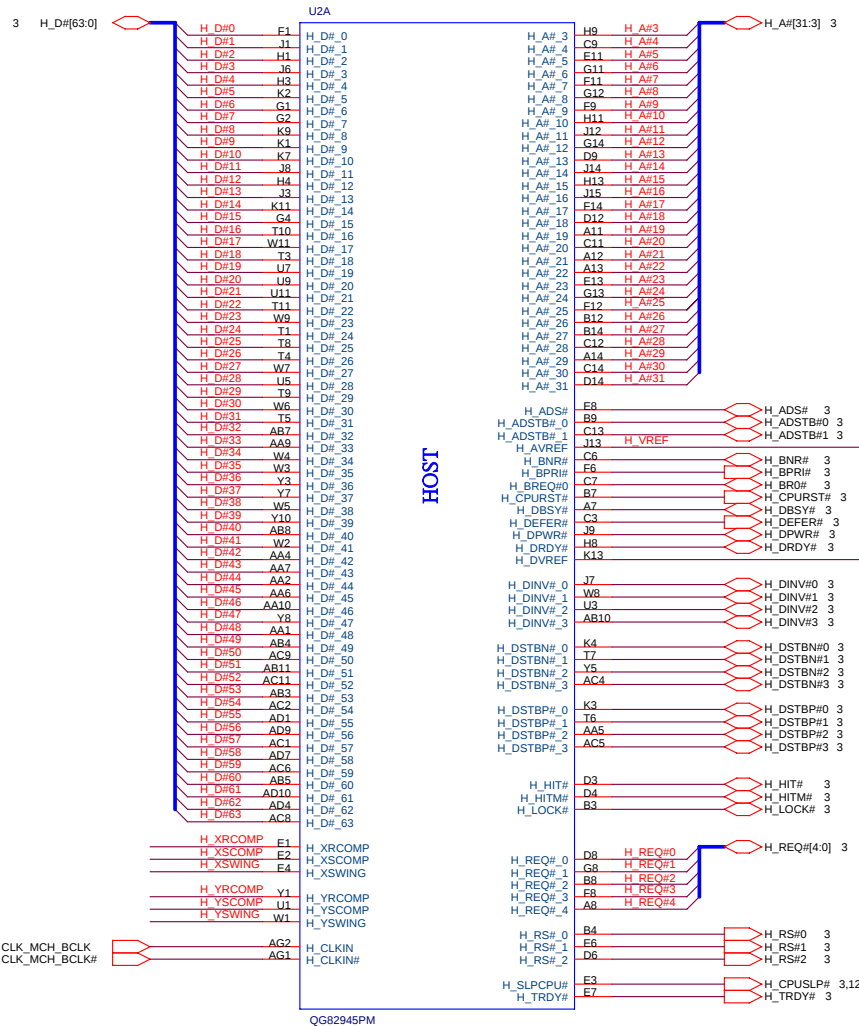
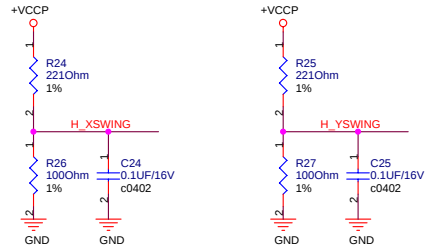
SCOMP

For Slew Rate Compensation on the FSB

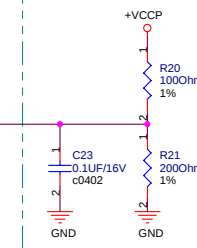


Voltage Swing

For Providing a Reference Voltage to the FSB RCOMP



AGTL+ I/O Voltage Reference



<Variant Name>



Title : NB_945PM_HOST

ASUSTek Computer INC.

Engineer: Jack Hsu

Size

Custom

Project Name

284J

Rev

1.1

Date: Tuesday, October 10, 2006

Sheet 5 of 68

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

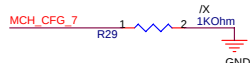


CFG[13:12] : GMCH Test Mode

- 00= Partial CLK Gating Disable
- 01 = XOR Mode Enable
- 10 = All Z Mode Enable
- 11 = Normal Operation (D)

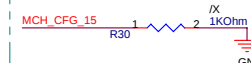
CFG7 : CPU Strap

0 = Desktop/Transpotable CPU
1 = Mobile CPU (D)



CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)



CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)



CFG18 : VCC Select

- 0 = 1.05V (D)
- 1 = 1.5V



CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)

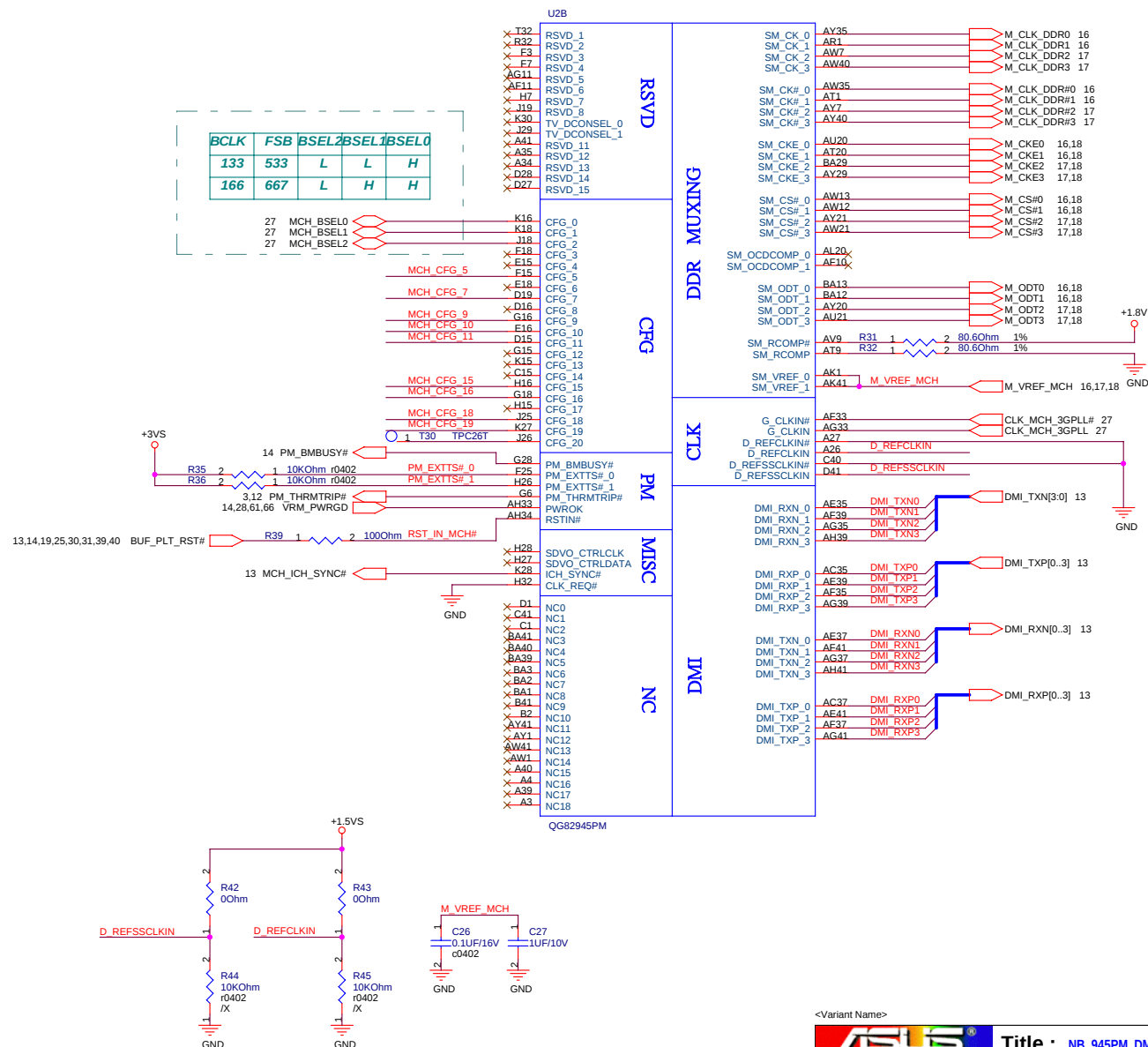


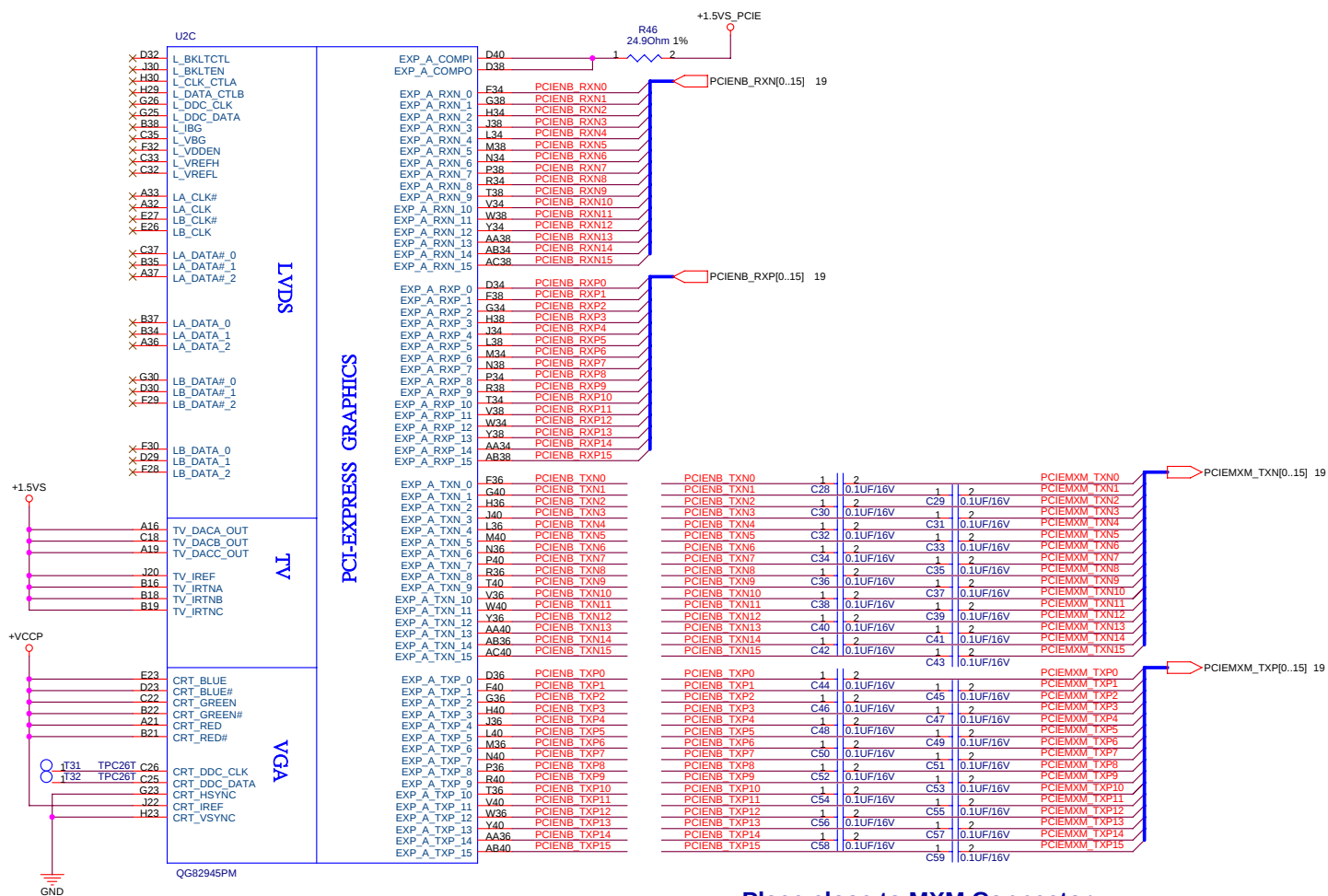
CFG19 : DMI Lane Reversal

- | 0 = Normal Operation (D)
- | 1 = Reverse Lane

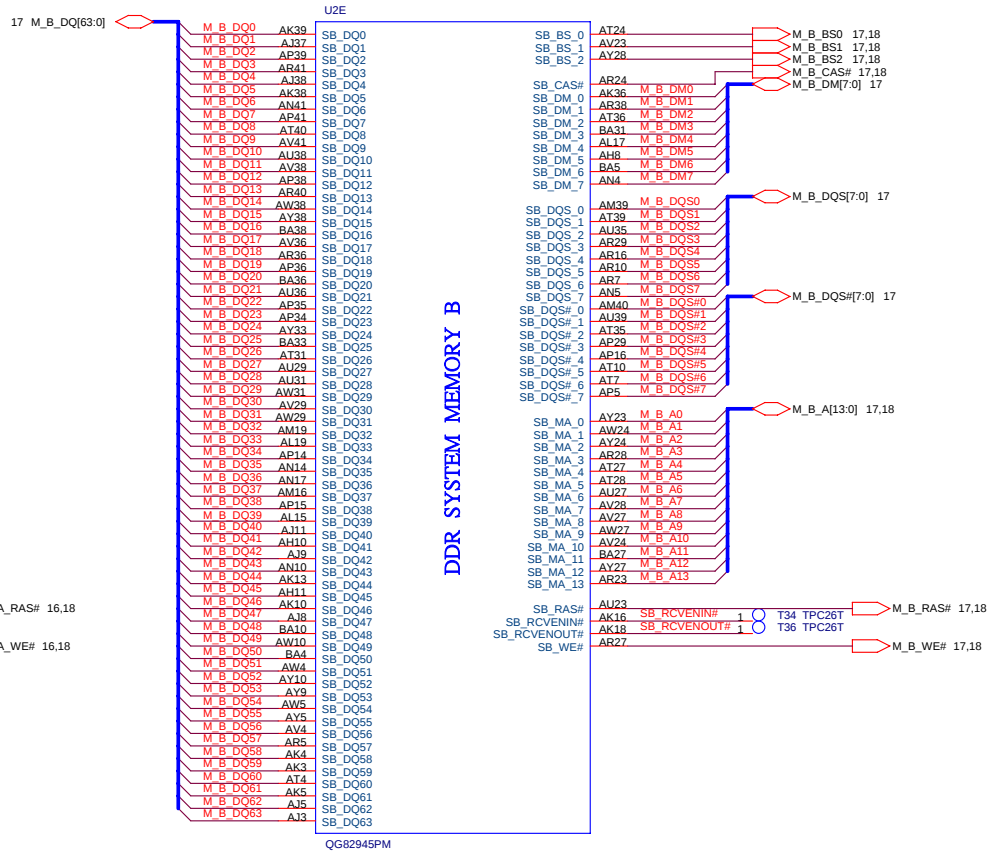


Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

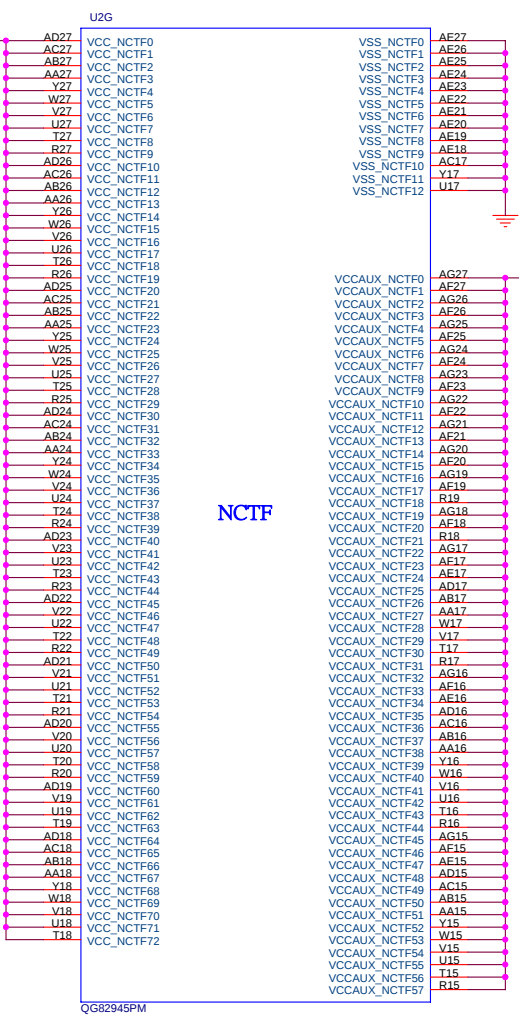
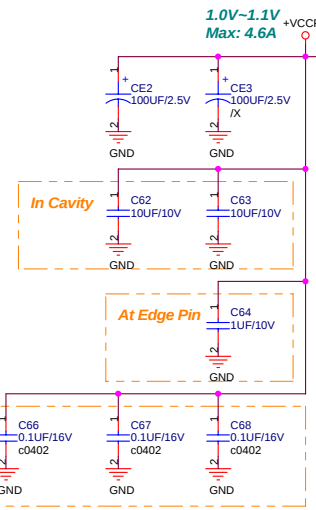
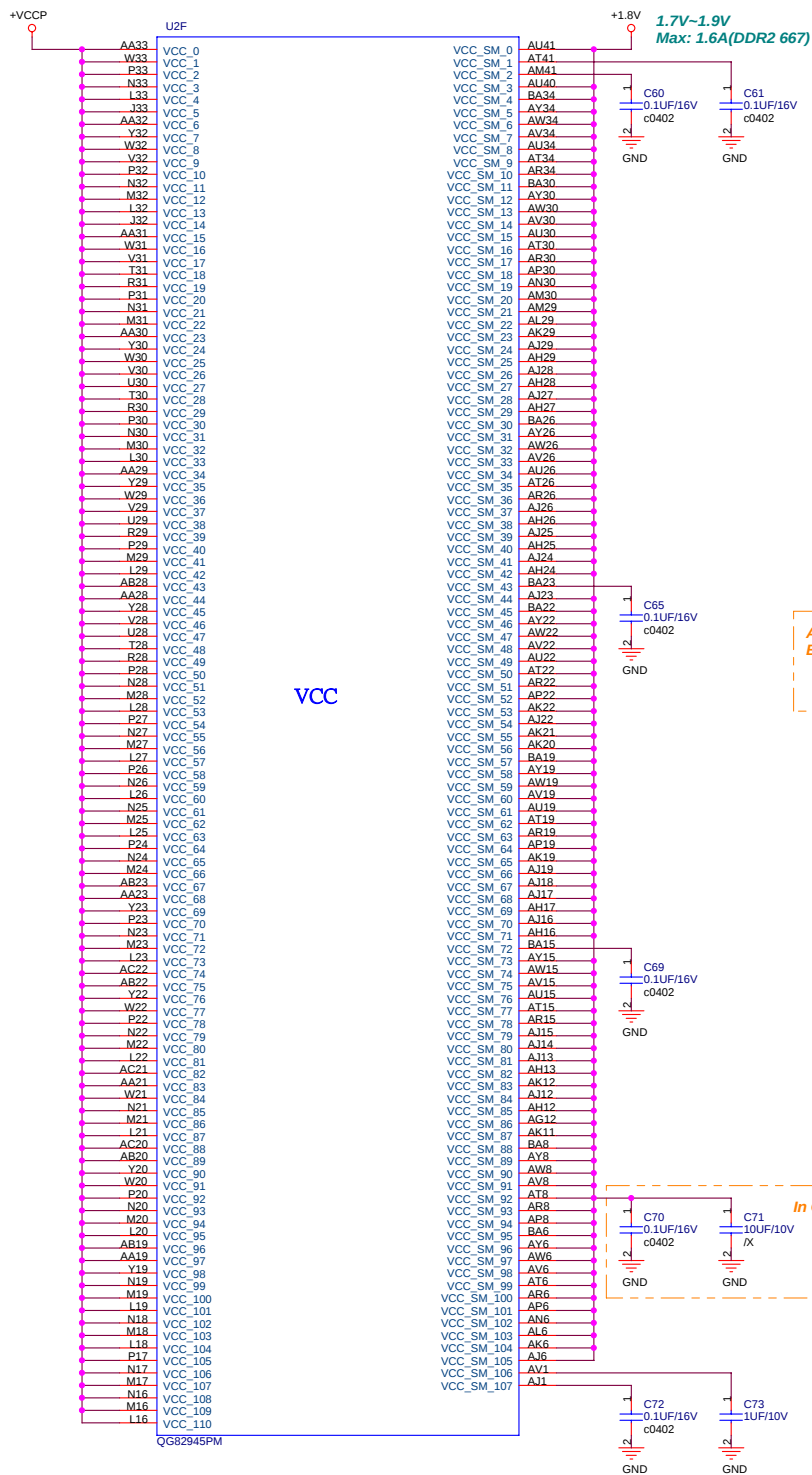


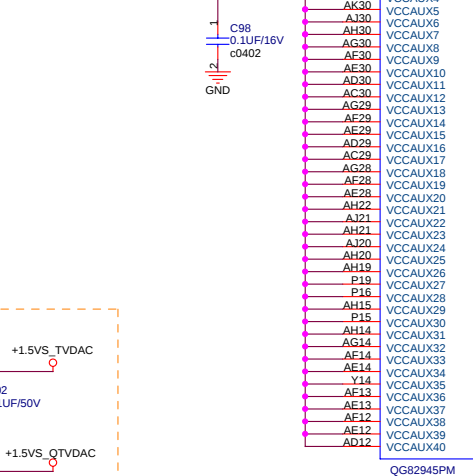
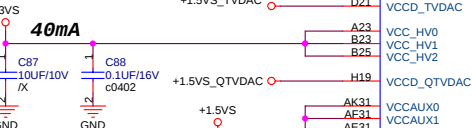
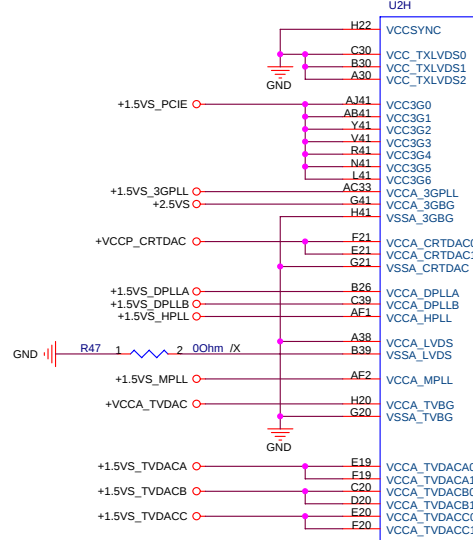
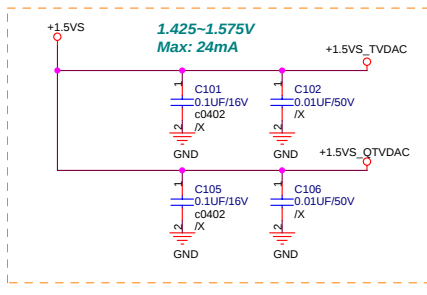
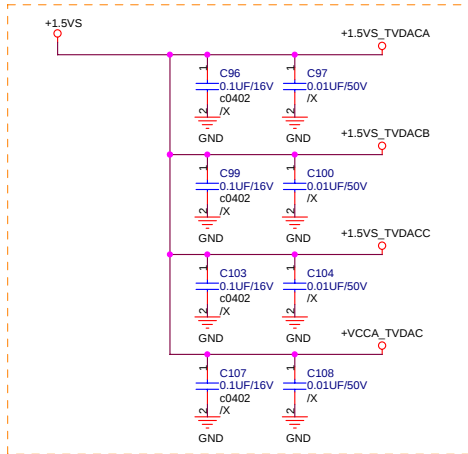
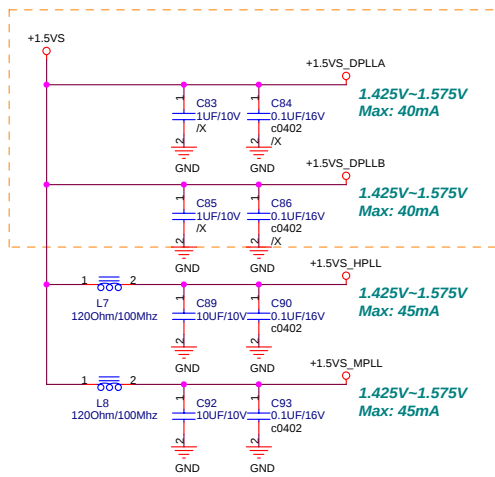
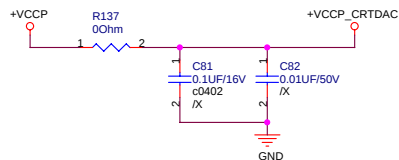
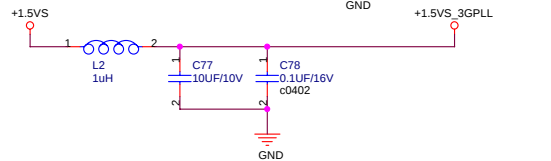
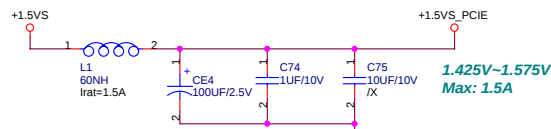


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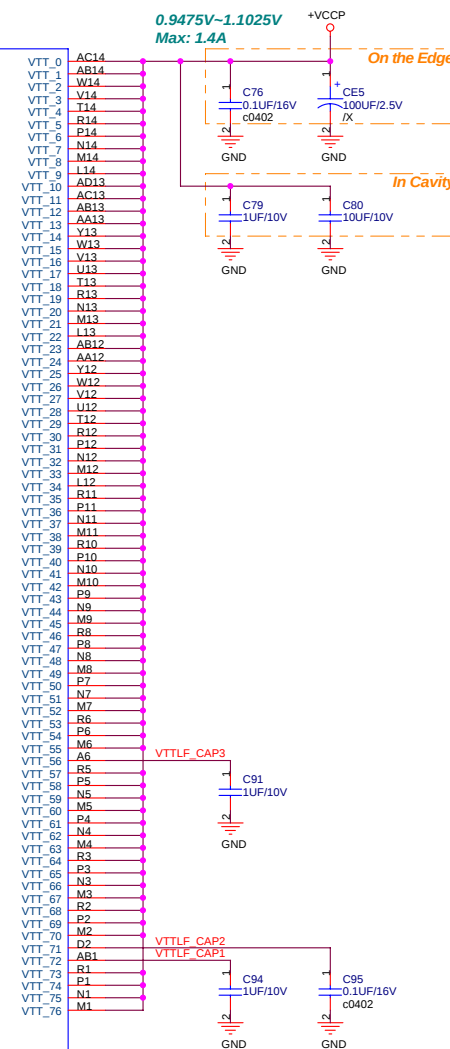
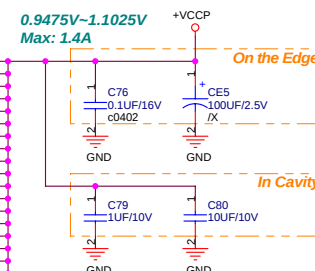


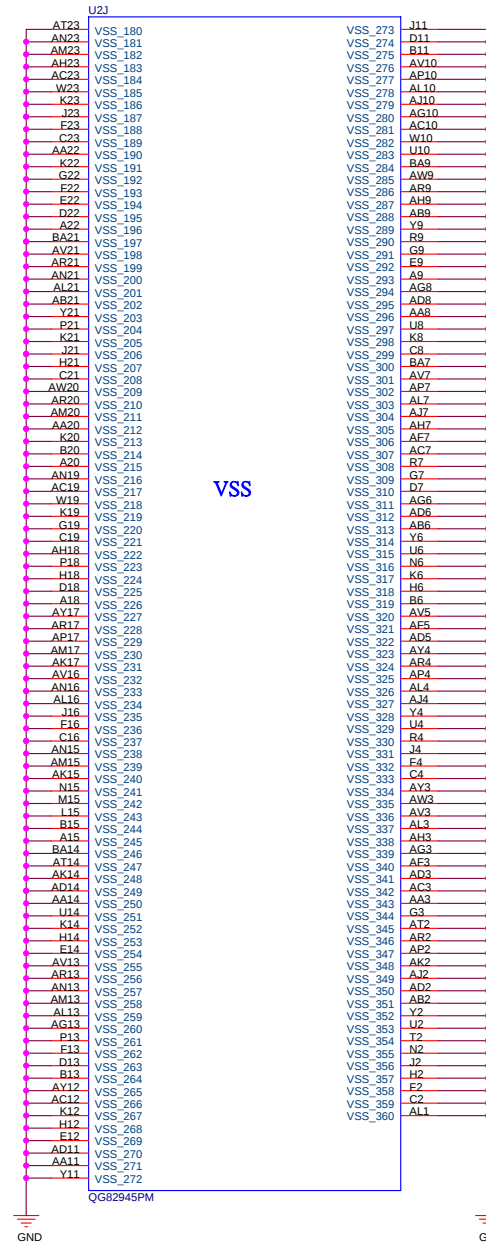
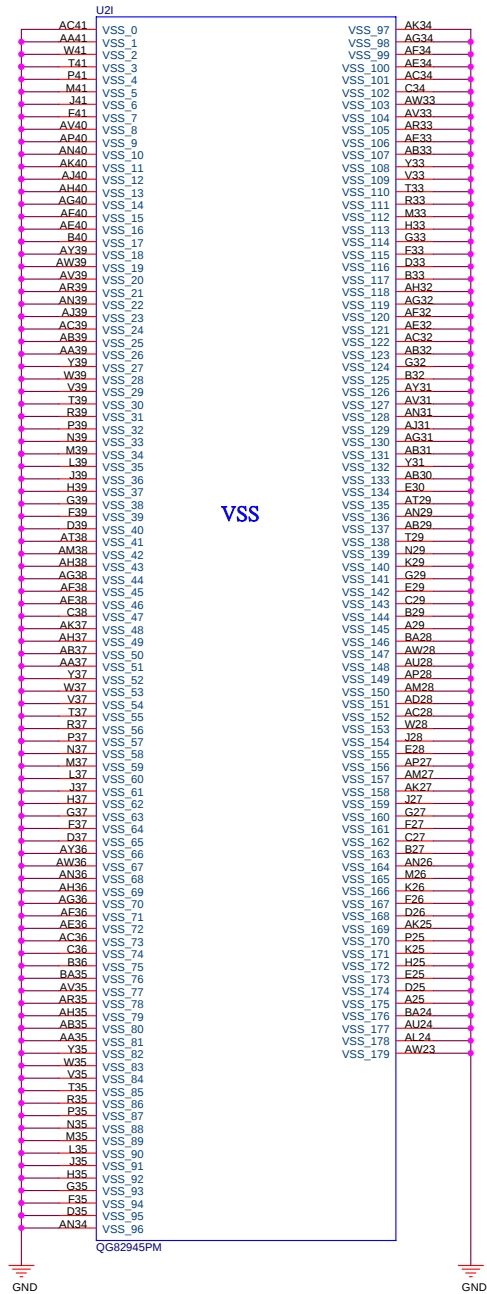
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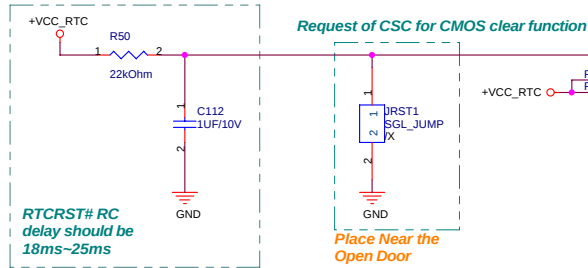
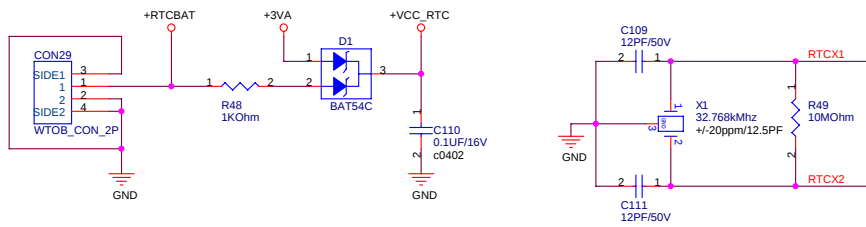
POWER



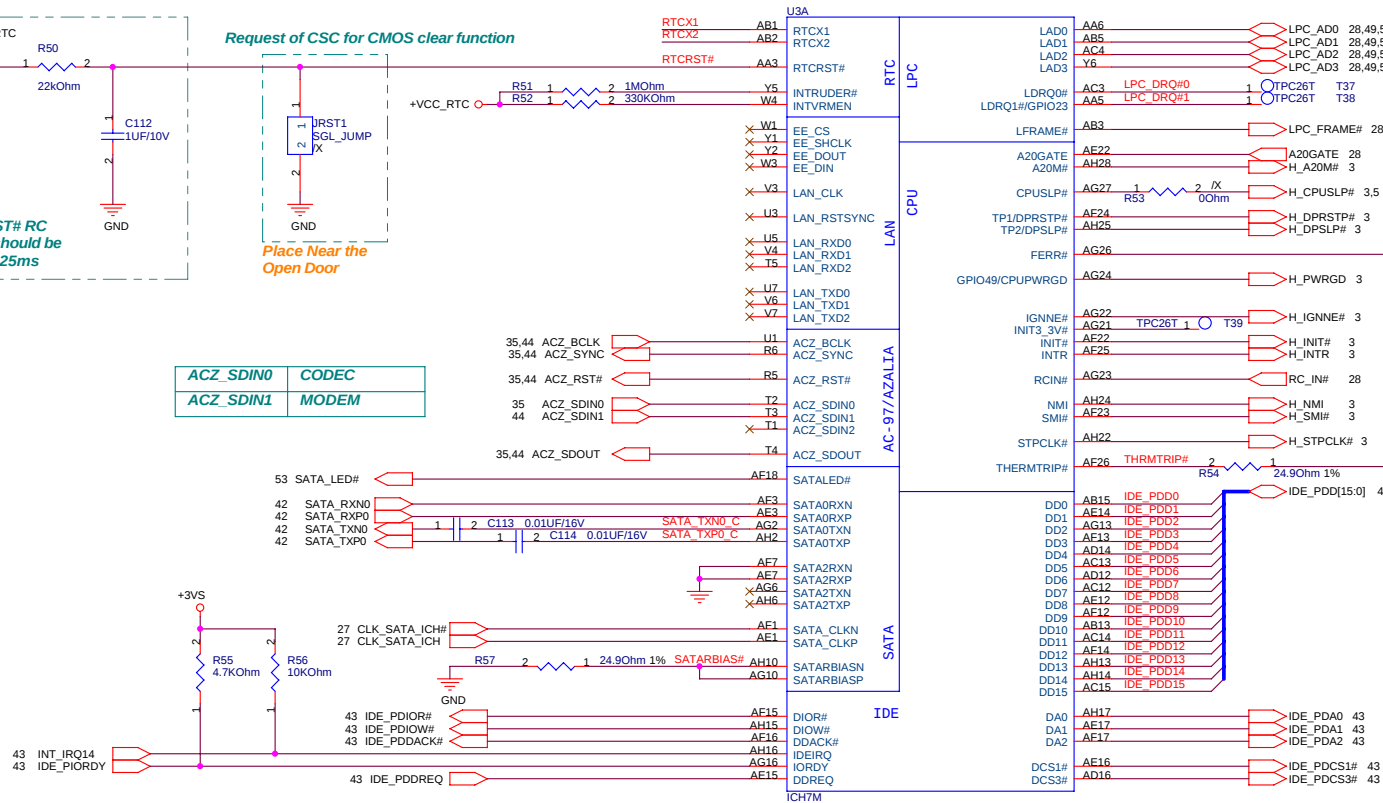


<Variant Name>

		Title : NB_945PM_GND	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date:	Tuesday, October 10, 2006	Sheet	11 of 68

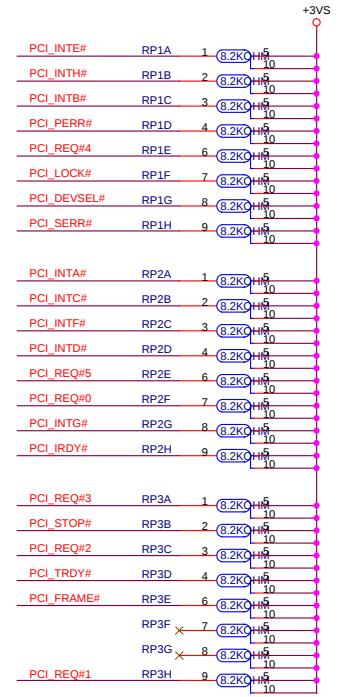
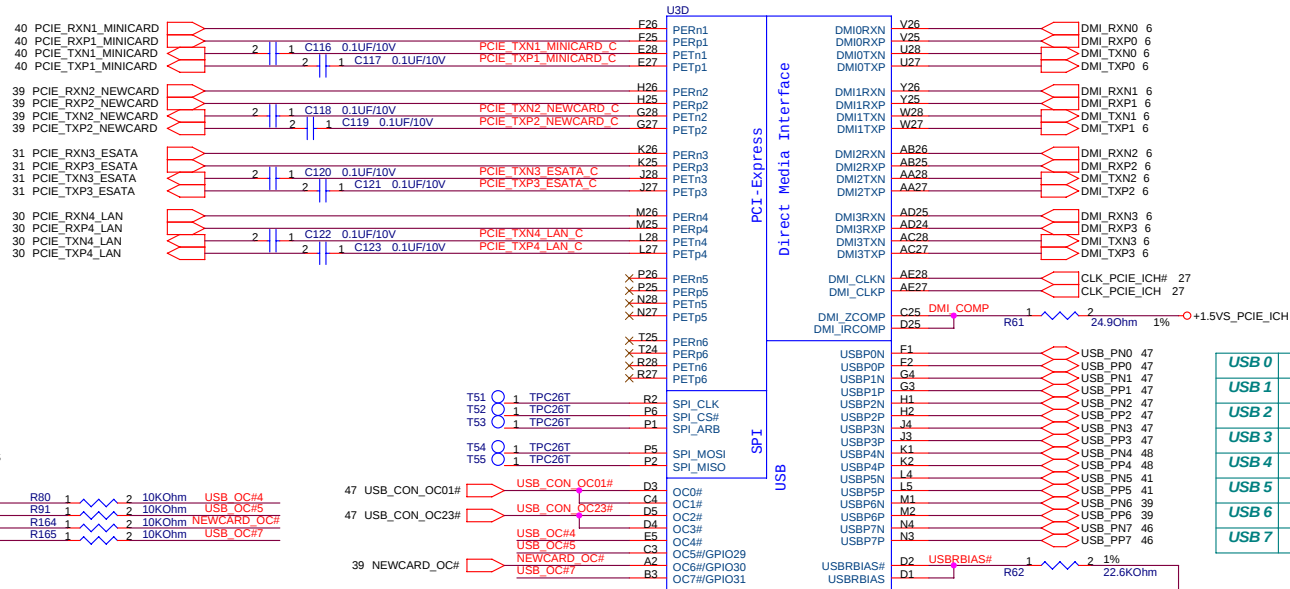
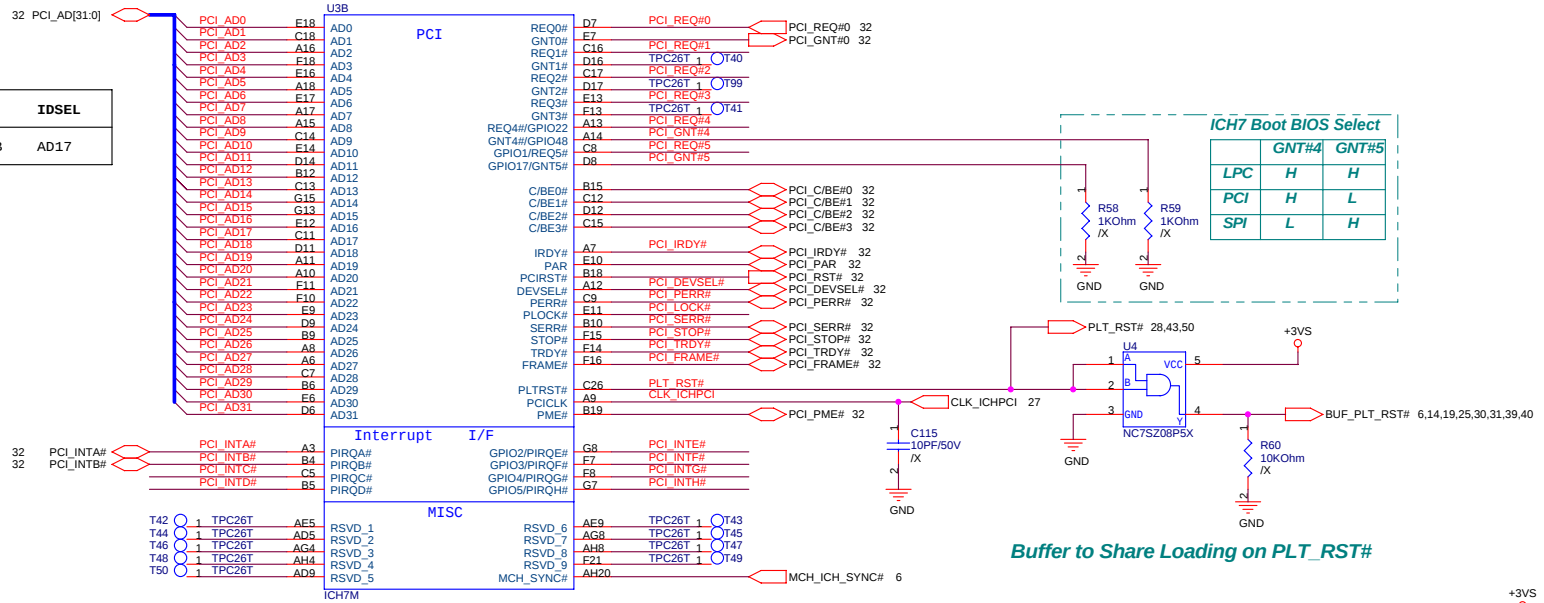


ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM

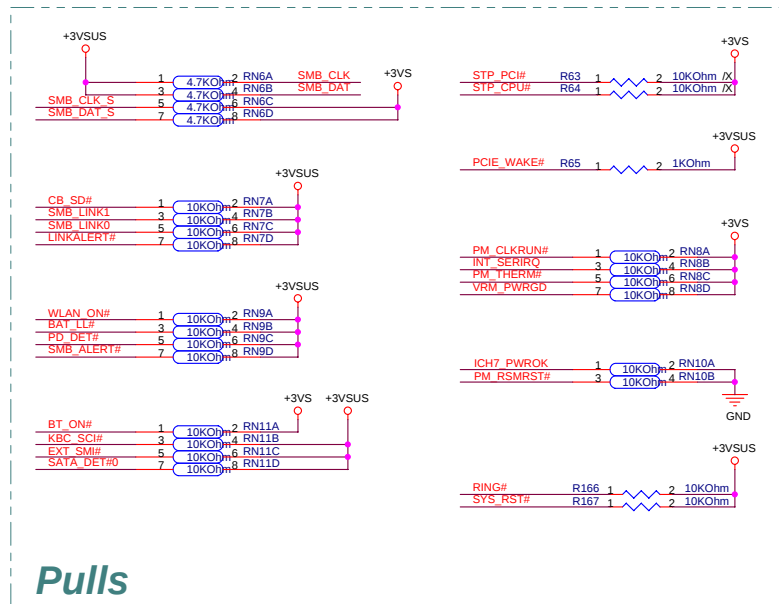
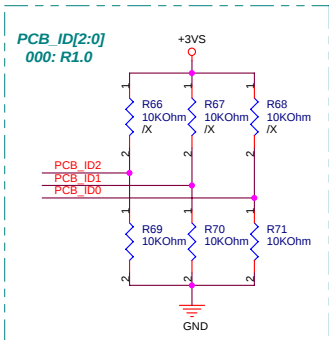
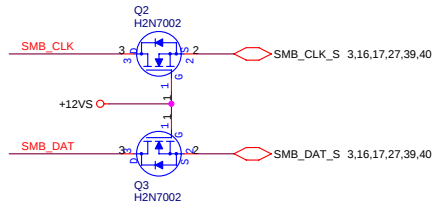
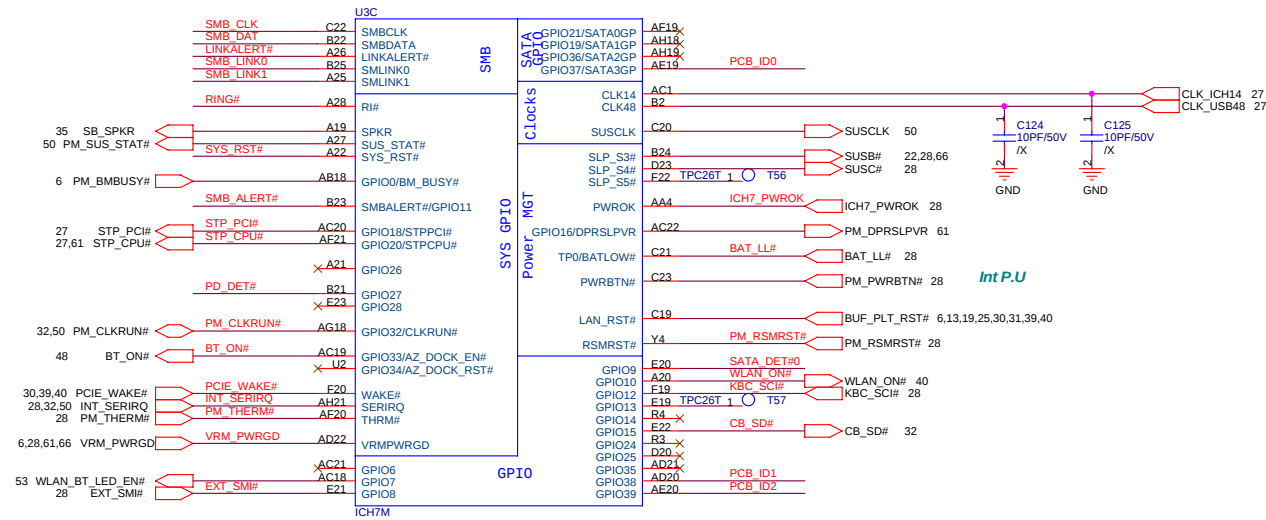


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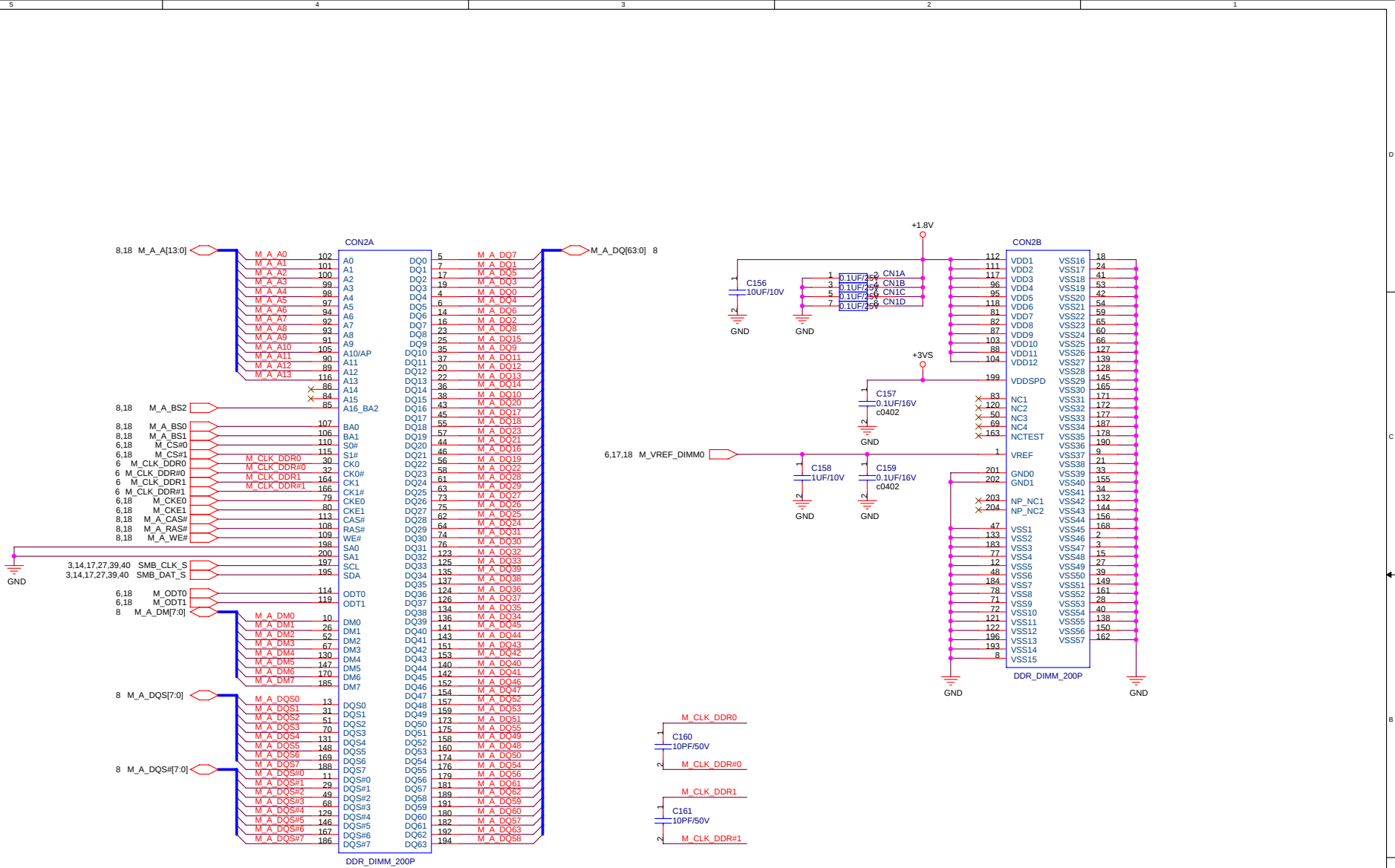
PCI Device	REQ?#	GNT?#	INT?#	IDSEL
R5C832	PCI_REQ#0	PCI_GNT#0	INTA, B	AD17



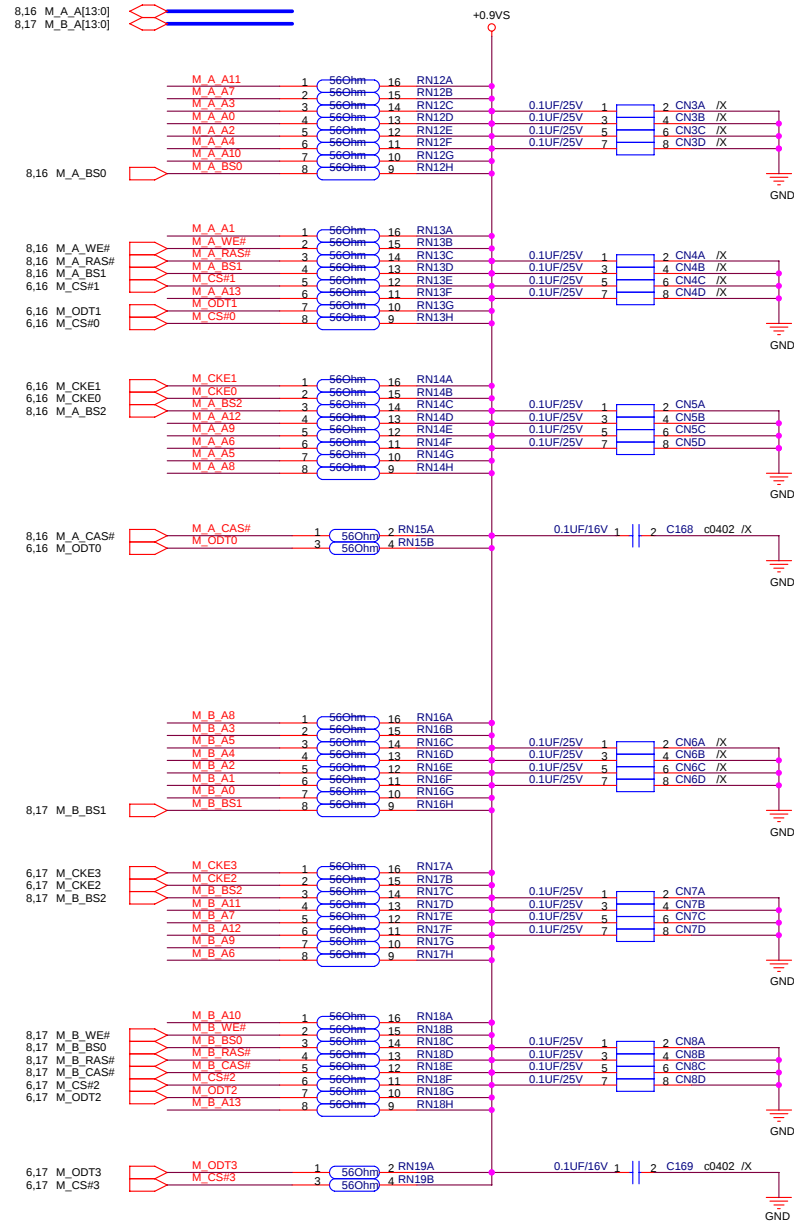
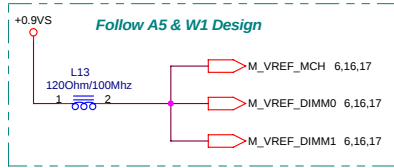
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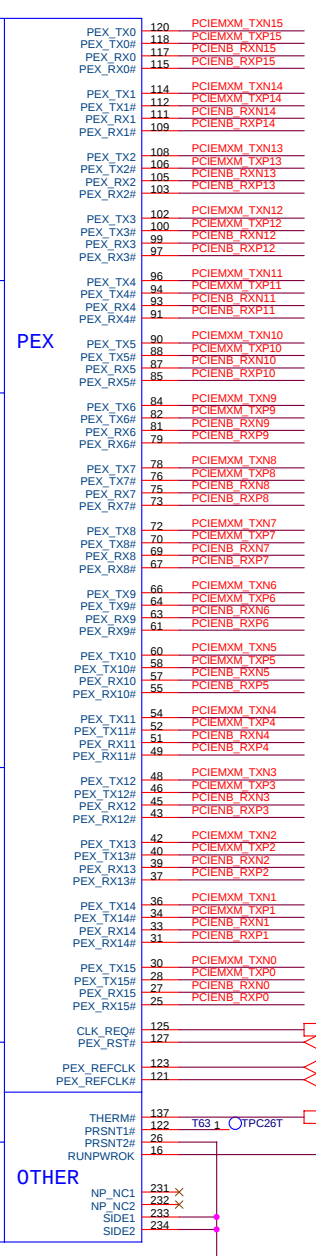
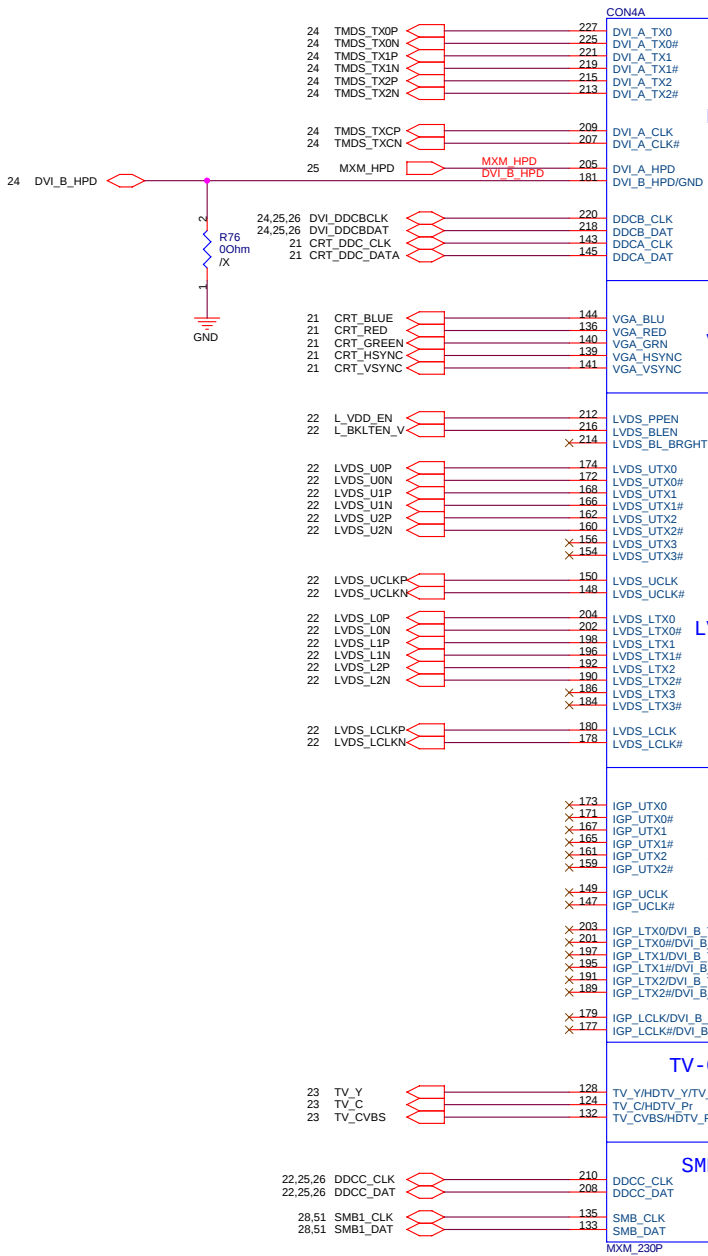
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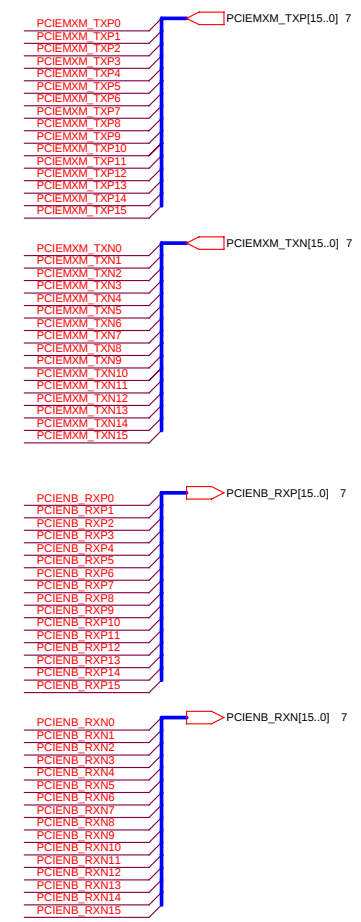
Standard Type SODIMM Connector H=9.2mm



<Variant Name>



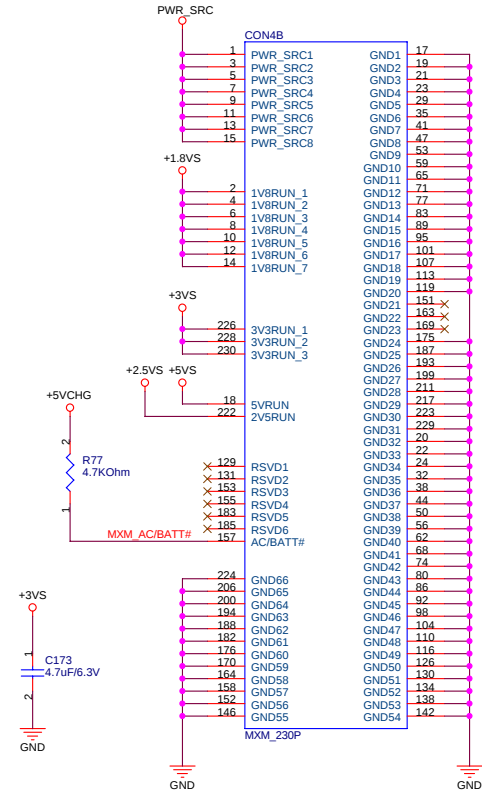
PCIE Lane Reversed



DDCA_CLK, DDCA_DAT,
DDCB_CLK, DDCB_DAT,
DDCC_CLK, DDCC_DAT,
Should have 2.2K PULL-UP to +3.3V on MXM Module

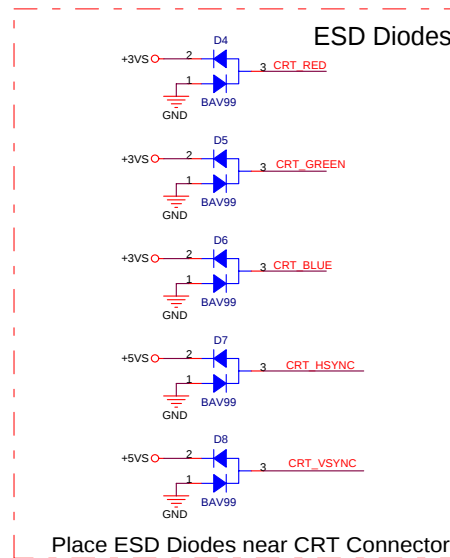
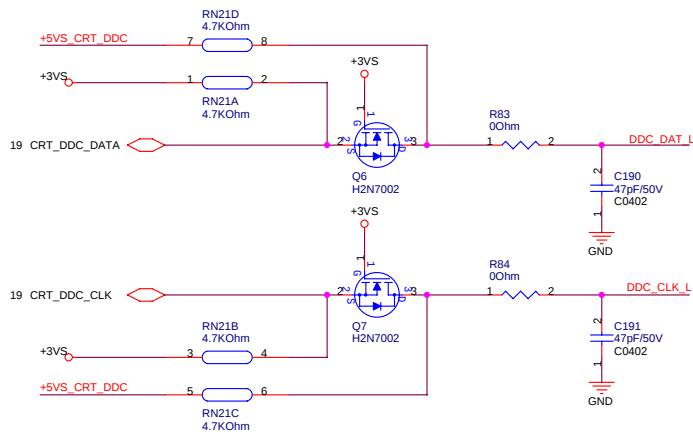
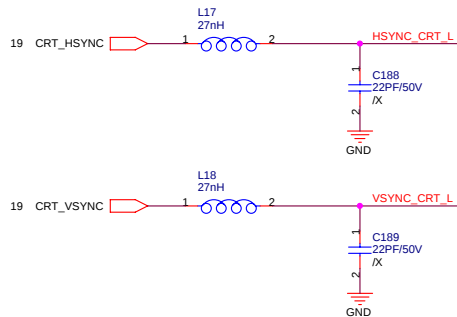
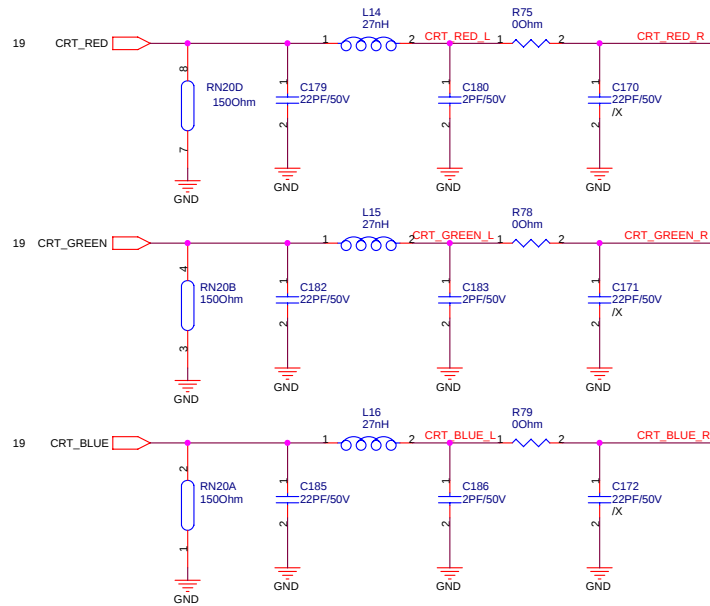
THERM# -- Open Collector Output, Active Low, 5V tolerant
CLK_REQ# -- Output, Open Drain, Active Low

MXM Connector Pin Definition

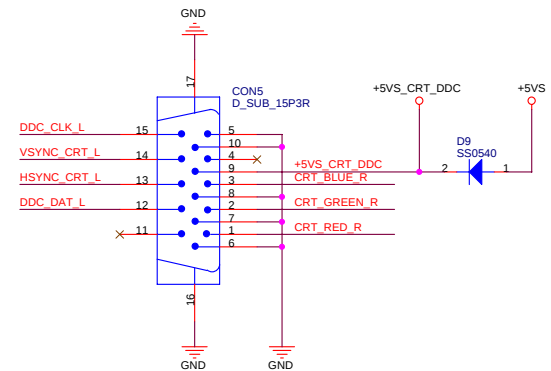


AC/BATT# : Input, 10K PULL-DOWN on Module.
0= nominal performance
1=high performance

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	PWR_SRC	2	1V8RUN	111	PEX_RX1	112	PEX_TX1#	221	DVI_A_TX1	222	2V5RUN
3	PWR_SRC	4	1V8RUN	113	GND	114	PEX_TX1	223	GND	224	GND
5	PWR_SRC	6	1V8RUN	115	PEX_RX0#	116	GND	225	DVI_A_TX0#	226	3V3RUN
7	PWR_SRC	8	1V8RUN	117	PEX_RX0	118	PEX_TX0#	227	DVI_A_TX0	228	3V3RUN
9	PWR_SRC	10	1V8RUN	119	GND	120	PEX_TX0	229	GND	230	3V3RUN
11	PWR_SRC	12	1V8RUN	121	PEX_REFCLK#	122	PRSNT1#				
13	PWR_SRC	14	1V8RUN	123	PEX_REFCLK	124	TV_C/HDTV_Pr				
15	PWR_SRC	16	RUNPWROK	125	CLK_REQ#	126	GND				
17	GND	18	5VRUN	127	PEX_RST#	128	TV_Y/HDTV_Y/TV_CVBS				
19	GND	20	GND	129	RSVD	130	GND				
21	GND	22	GND	131	RSVD	132	TV_CVBS/HDTV_Pb				
23	GND	24	GND	133	SMB_DAT	134	GND				
25	PEX_RX15#	26	PRSNT2#	135	SMB_CLK	136	VGA_RED				
27	PEX_RX15	28	PEX_TX15#	137	THERM#	138	GND				
29	GND	30	PEX_TX15	139	VGA_HSYNC	140	VGA_GRN				
31	PEX_RX14#	32	GND	141	VGA_VSYNC	142	GND				
33	PEX_RX14	34	PEX_TX14#	143	DDCA_CLK	144	VGA_BLU				
35	GND	36	PEX_TX14	145	DDCA_DAT	146	GND				
37	PEX_RX13#	38	GND	147	IGP	148	LVDS_UCLK#				
39	PEX_RX13	40	PEX_TX13#	149	IGP	150	LVDS_UCLK				
41	GND	42	PEX_TX13	151	IGP	152	GND				
43	PEX_RX12#	44	GND	153	RSVD	154	LVDS_UTX3#				
45	PEX_RX12	46	PEX_TX12#	155	RSVD	156	LVDS_UTX3				
47	GND	48	PEX_TX12	157	AC/BATT#	158	GND				
49	PEX_RX11#	50	GND	159	IGP	160	LVDS_UTX2#				
51	PEX_RX11	52	PEX_TX11#	161	IGP	162	LVDS_UTX2				
53	GND	54	PEX_TX11	163	IGP	164	GND				
55	PEX_RX10#	56	GND	165	IGP	166	LVDS_UTX1#				
57	PEX_RX10	58	PEX_TX10#	167	IGP	168	LVDS_UTX1				
59	GND	60	PEX_TX10	169	IGP	170	GND				
61	PEX_RX9#	62	GND	171	IGP	172	LVDS_UTX0#				
63	PEX_RX9	64	PEX_TX9#	173	IGP	174	LVDS_UTX0				
65	GND	66	PEX_TX9	175	GND	176	GND				
67	PEX_RX8#	68	GND	177	IGP/DVI_B_CLK#	178	LVDS_LCLK#				
69	PEX_RX8	70	PEX_TX8#	179	IGP/DVI_B_CLK	180	LVDS_LCLK				
71	GND	72	PEX_TX8	181	DVI_B_HPD/GND	182	GND				
73	PEX_RX7#	74	GND	183	RSVD	184	LVDS_LTX3#				
75	PEX_RX7	76	PEX_TX7#	185	RSVD	186	LVDS_LTX3				
77	GND	78	PEX_TX7	187	GND	188	GND				
79	PEX_RX6#	80	GND	189	IGP/DVI_B_TX2#	190	LVDS_LTX2#				
81	PEX_RX6	82	PEX_TX6#	191	IGP/DVI_B_TX2	192	LVDS_LTX2				
83	GND	84	PEX_TX6	193	GND	194	GND				
85	PEX_RX5#	86	GND	195	IGP/DVI_B_TX1#	196	LVDS_LTX1#				
87	PEX_RX5	88	PEX_TX5#	197	IGP/DVI_B_TX1	198	LVDS_LTX1				
89	GND	90	PEX_TX5	199	GND	200	GND				
91	PEX_RX4#	92	GND	201	IGP/DVI_B_TX0#	202	LVDS_LTX0#				
93	PEX_RX4	94	PEX_TX4#	203	IGP/DVI_B_TX0	204	LVDS_LTX0				
95	GND	96	PEX_TX4	205	DVI_A_HPD	206	GND				
97	PEX_RX3#	98	GND	207	DVI_A_CLK#	208	DDCC_DAT				
99	PEX_RX3	100	PEX_TX3#	209	DVI_A_CLK	210	DDCC_CLK				
101	GND	102	PEX_TX3	211	GND	212	LVDS_PPEN				
103	PEX_RX2#	104	GND	213	DVI_A_TX2#	214	LVDS_BL_BRGHT				
105	PEX_RX2	106	PEX_TX2#	215	DVI_A_TX2	216	LVDS_BLEN				
107	GND	108	PEX_TX2	217	GND	218	DDCB_DAT				
109	PEX_RX1#	110	GND	219	DVI_A_TX1#	220	DDCB_CLK				



Place ESD Diodes near CRT Connector



CRT Connector

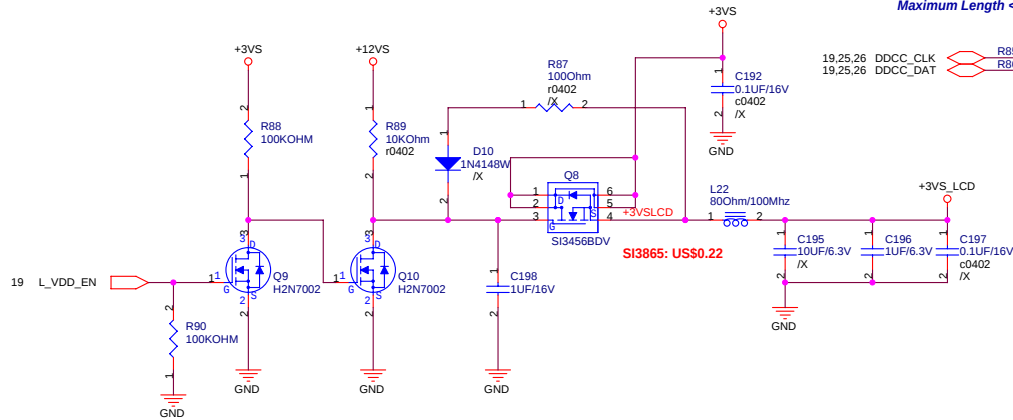
<Variant Name>

ASUS		Title : CRT Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Z84J	Rev 1.1
Custom			
Date: Tuesday, October 10, 2006		Sheet	21 of 68

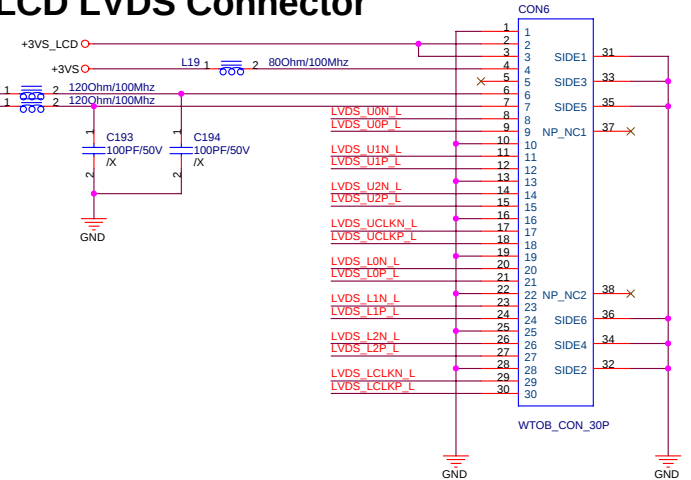
LCD Power

3-3.6V S0-S1M:410 mA(500 mA Max.)

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



LCD LVDS Connector



LCD Backlight Control

INVERTER Connector

BIOS

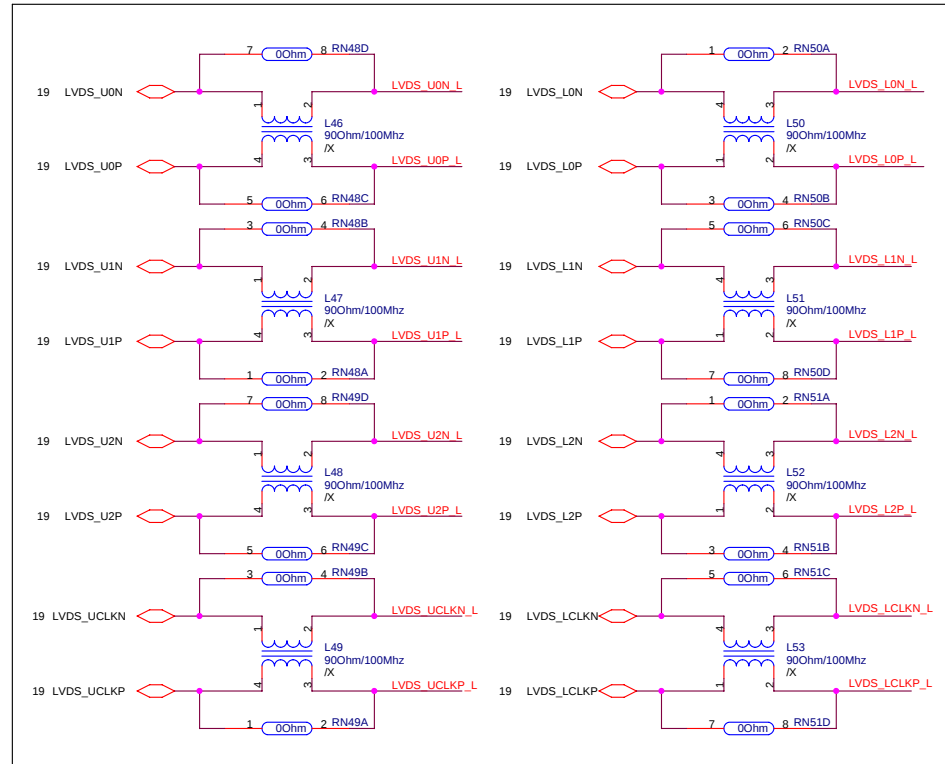
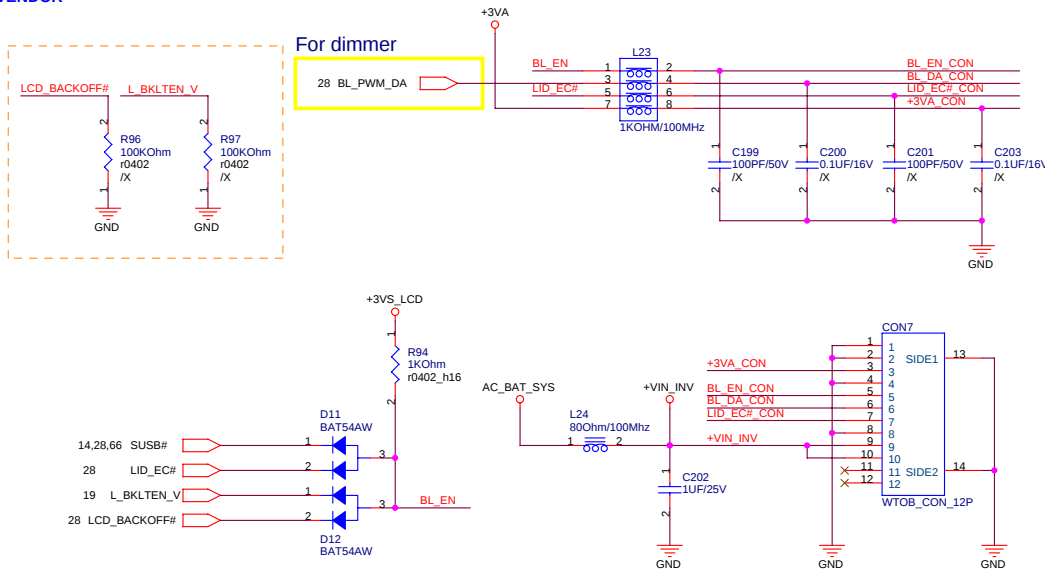
LCD_BACKOFF#:

When user push "Fn+F7" button,
BIOS active this pin to turn off
back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050

PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVED FOR VENDOR



<Variant Name>



Title : LVDS & Inverter Conn.

ASUSTek Computer INC.

Engineer: *Jack Hsu*

Size

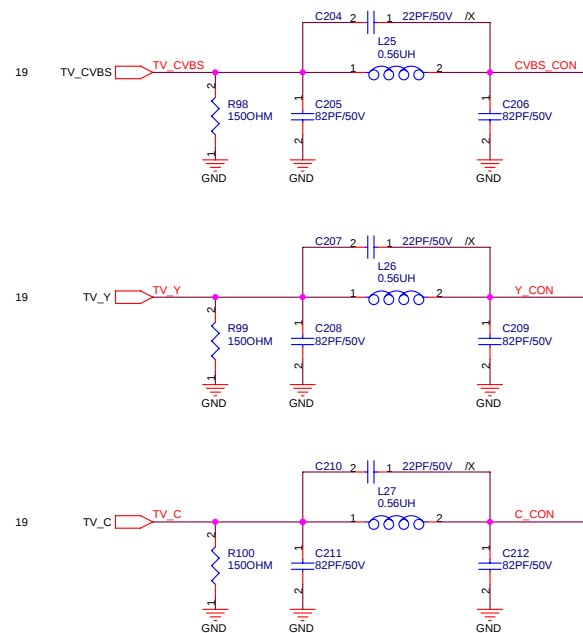
Product Name

284J

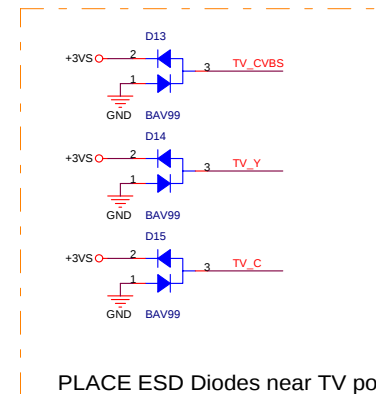
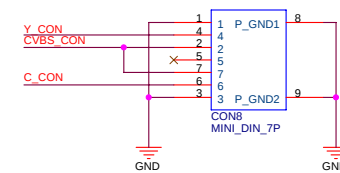
Date: Tuesday, October 10, 2006

Sheet 22 of 68

Rev



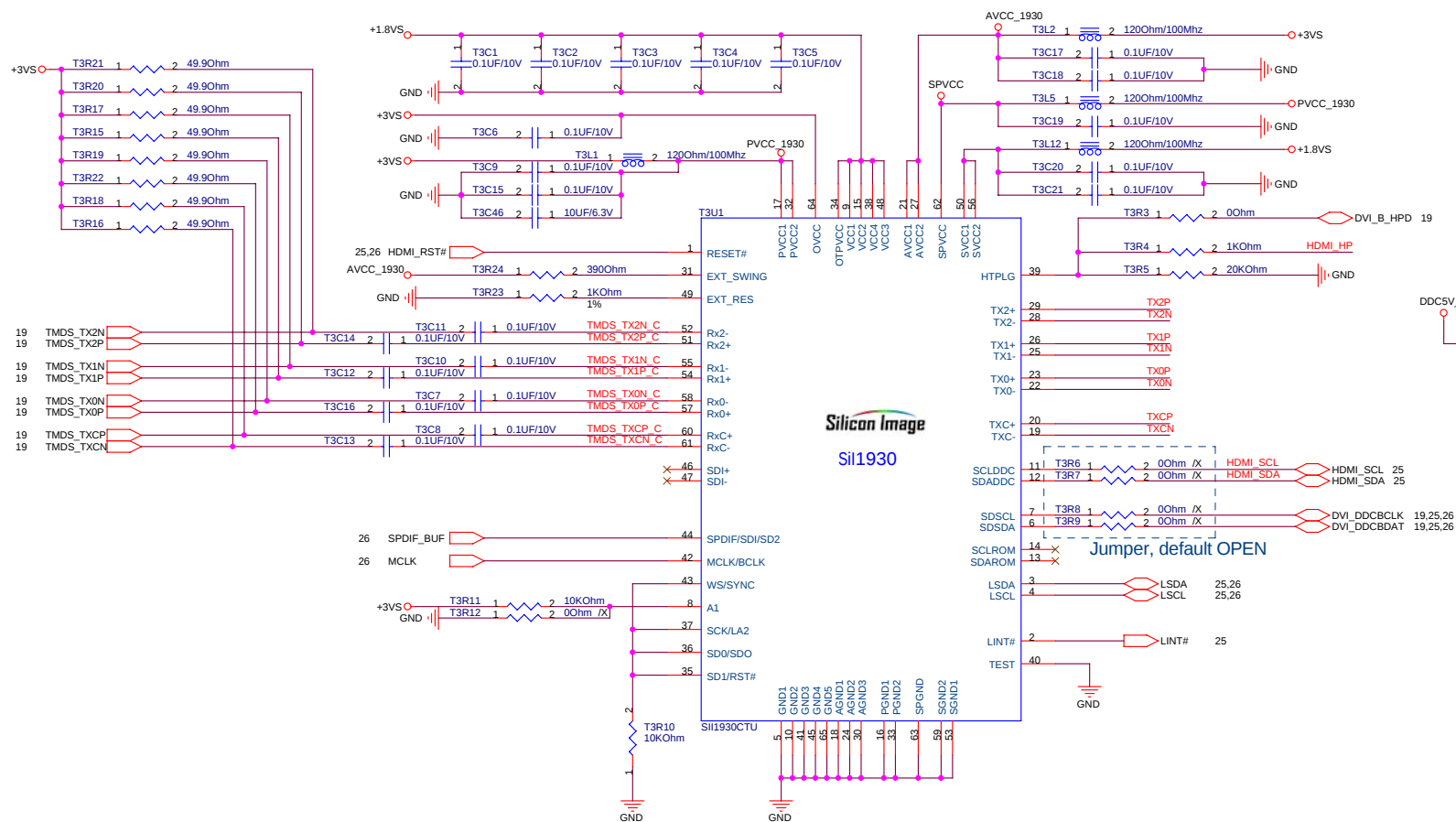
TV OUT Connector



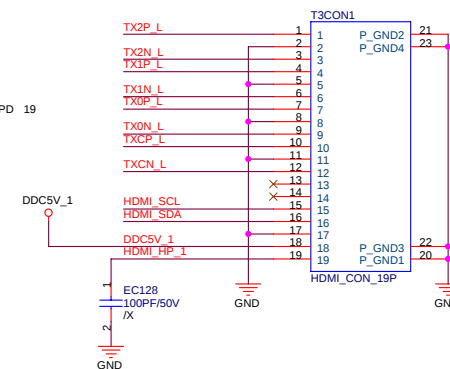
<Variant Name>

ASUS		Title : TV-OUT Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Z84J	Rev
Custom			
Date: Tuesday, October 10, 2006		Sheet	23 of 68

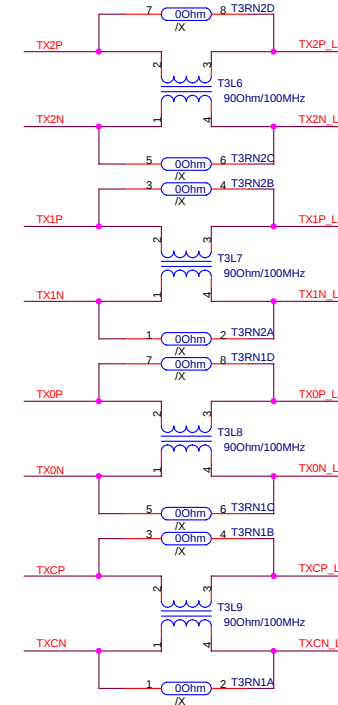
HDMI Transmitter



HDMI Connector

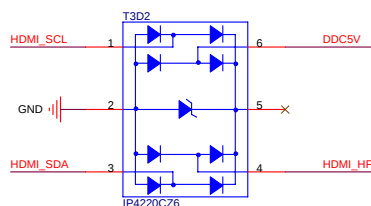


Choke : TDK ACM2012 preferred
ASUS P/N : 09G061054000



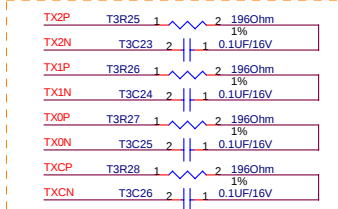
Si1930
1.8VS<380mA
3.3VS<110mA
5VS <55mA

Place Polarity caps close to the inductors



ESD Diode, Place close to Connector

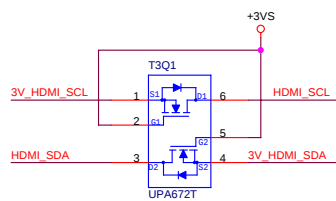
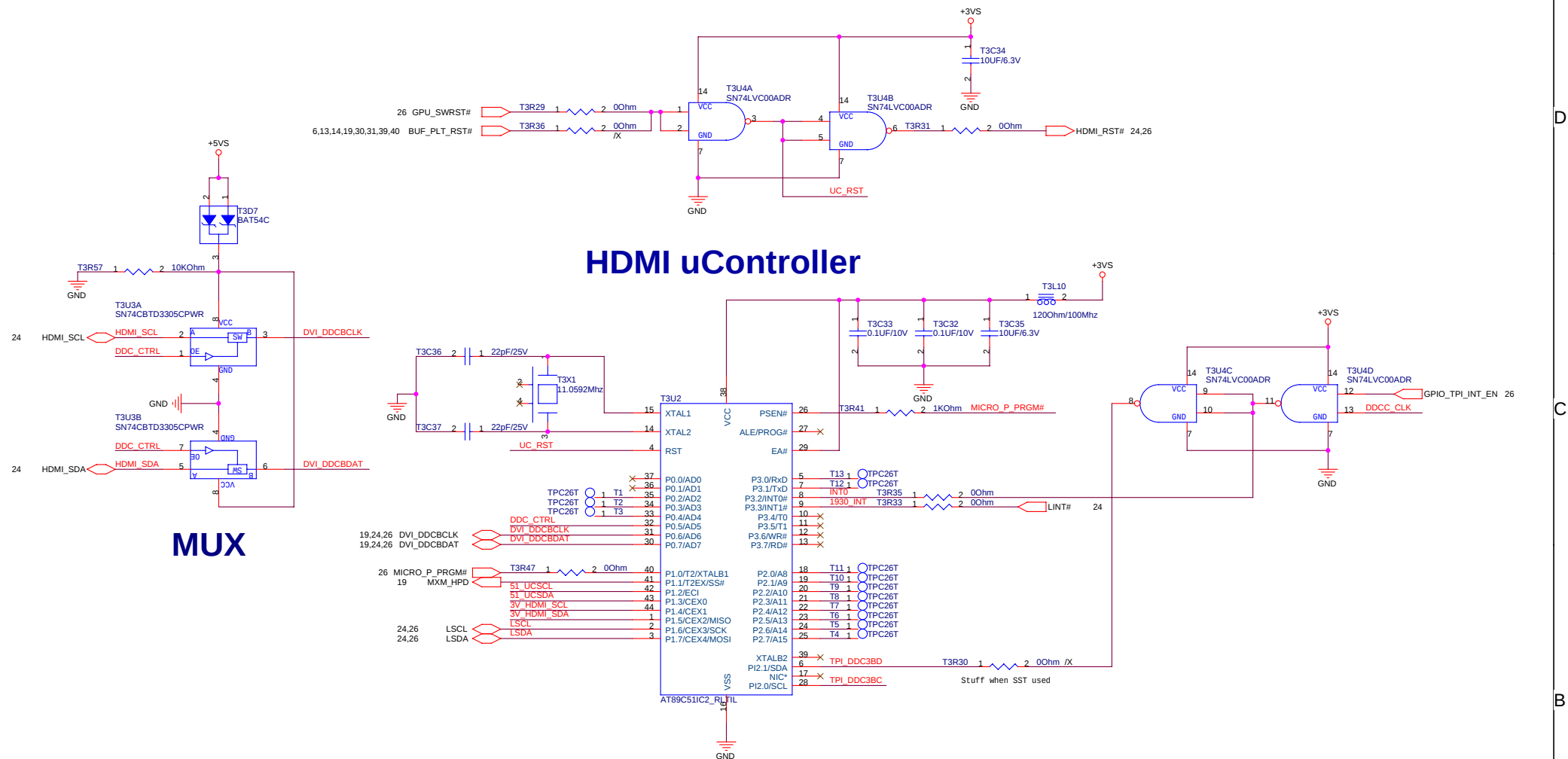
T3R25, T3R26, T3R27, T3R28 Must be 0603 package for Layout issue



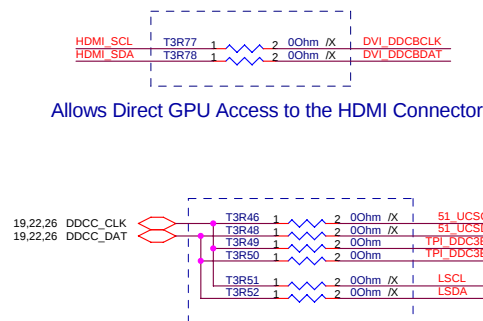
Source Termination, Place close to Transmitter
Refer to layout guide for detail placement

<Variant Name>

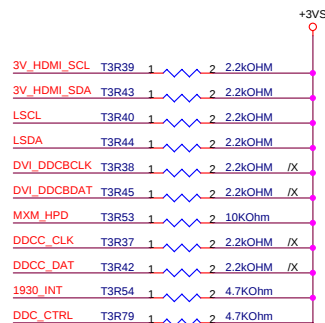
ASUS		Title : HDMI Si1930	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet 24 of 68	



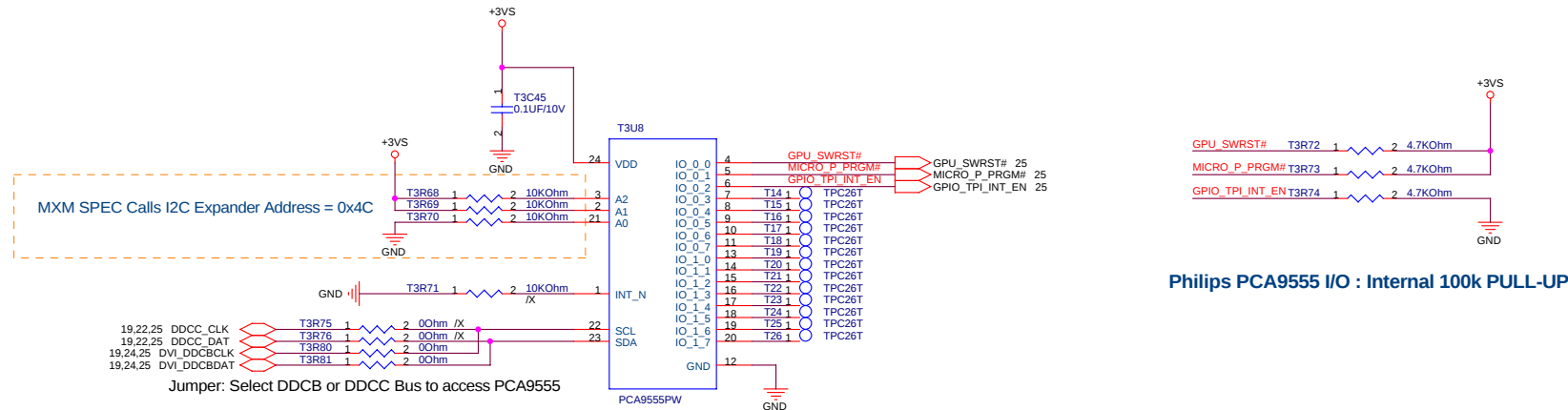
Level Shift



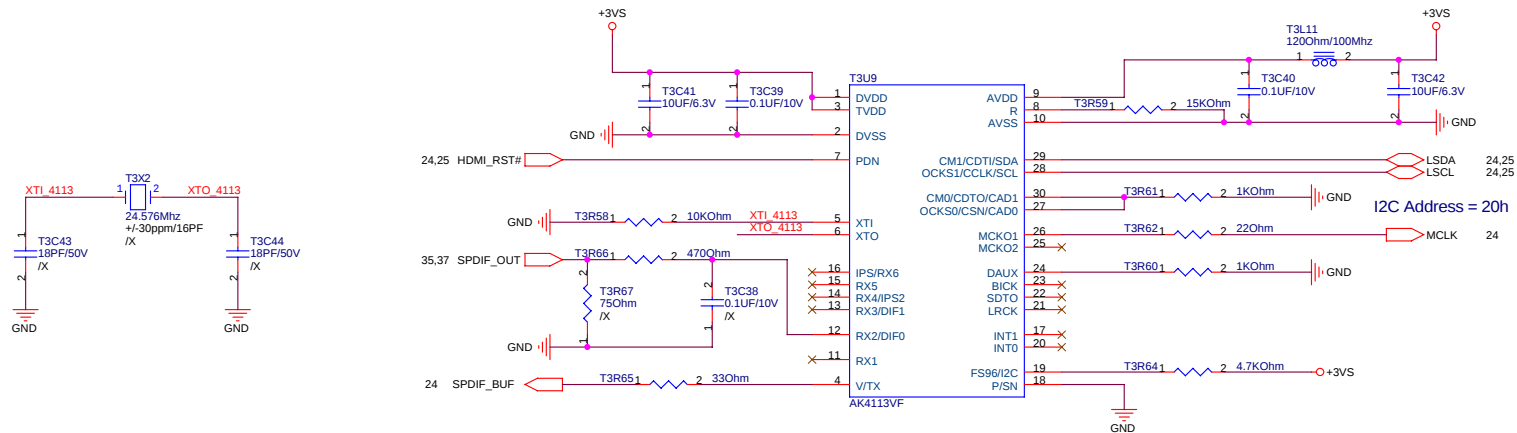
Jumper:
 Stuff T3R46, T3R48 Software I2C (SST)
 Stuff T3R49, T3R50 Hardware I2C (ATMEL)



I2C GPIO Controller

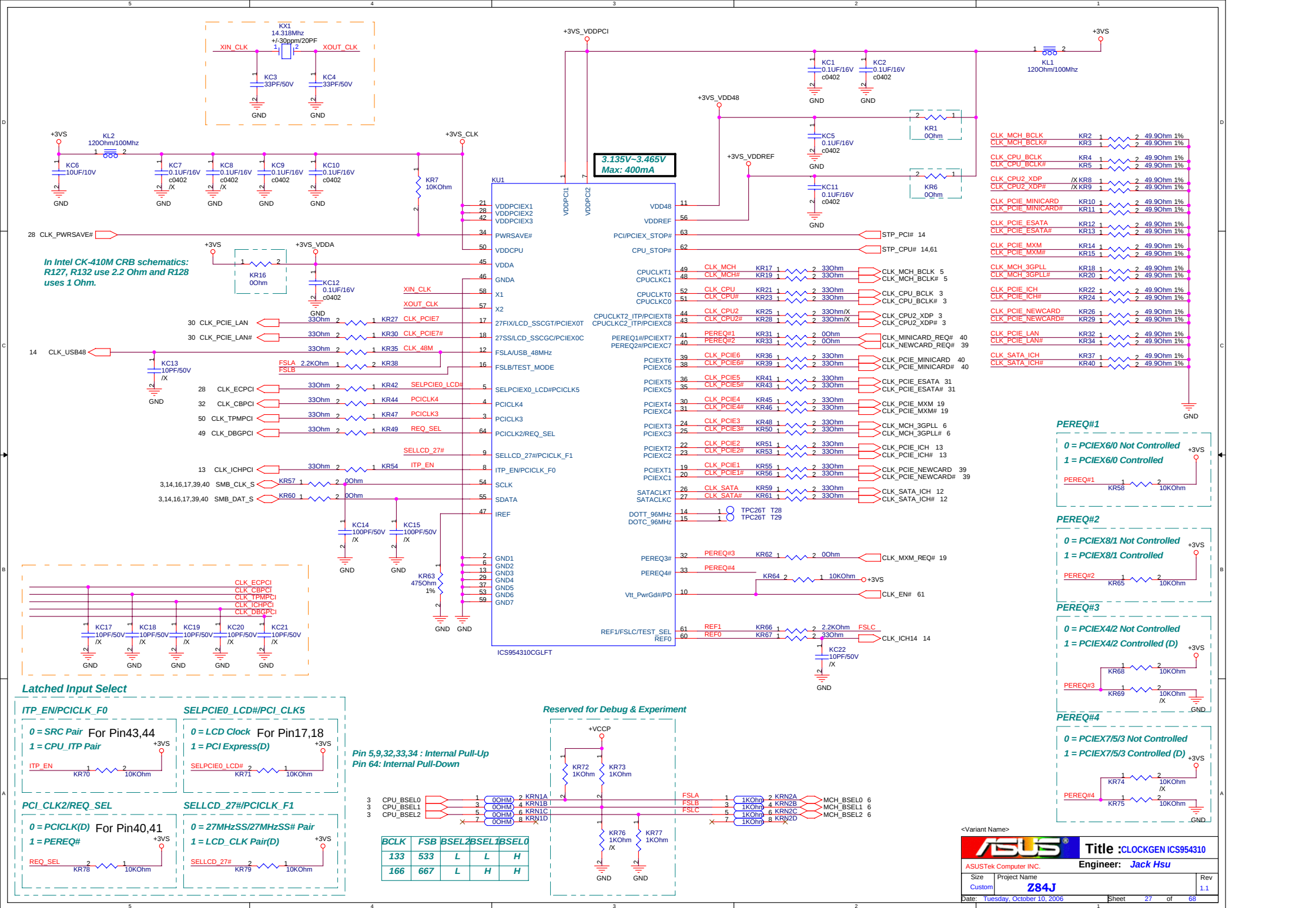


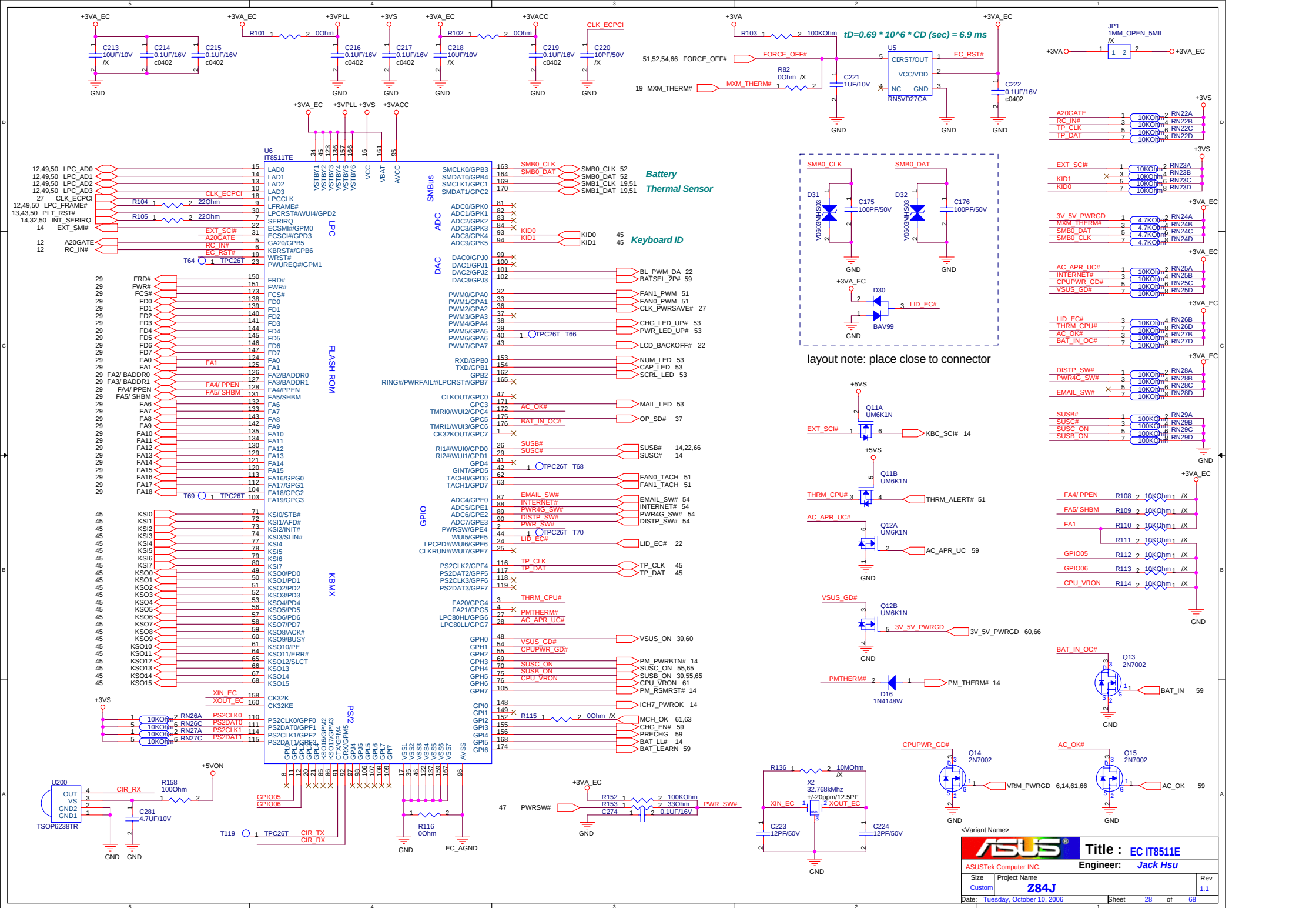
AK4113 Audio Codec



<Variant Name>

ASUS		Title : I2C EXP. & Codec	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet	26 of 68



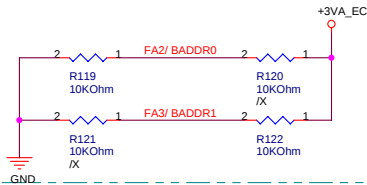


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

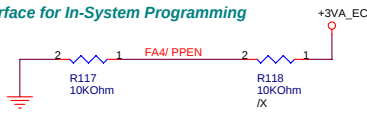
- 00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

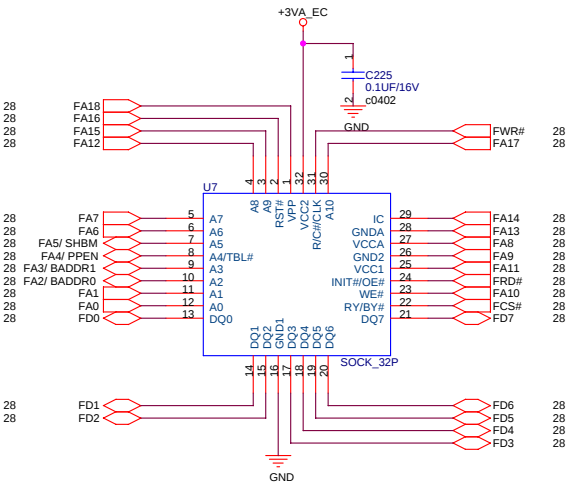
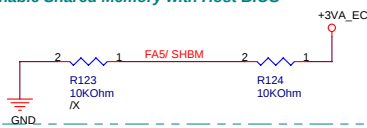
FA4/ PPEN

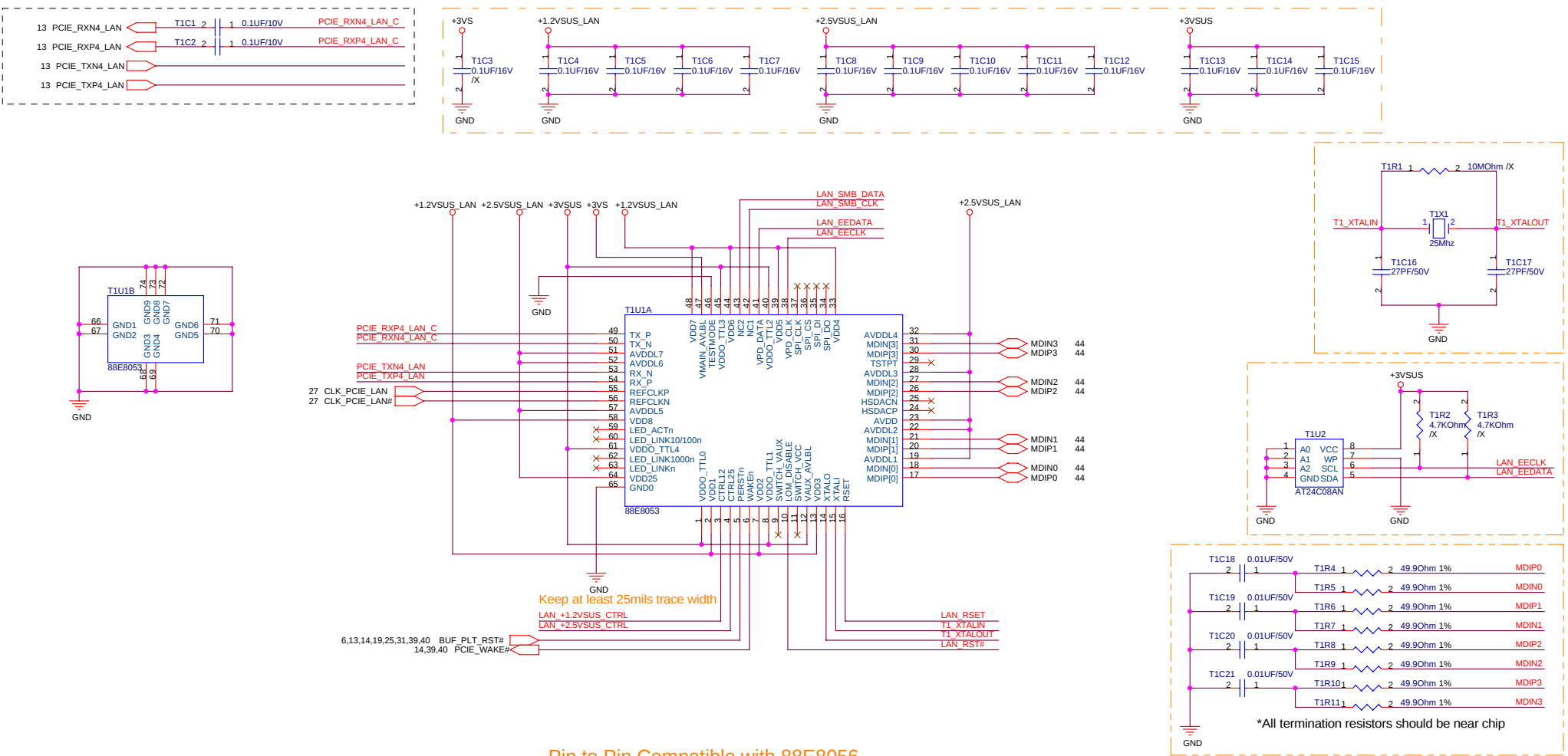
- 0: Normal
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



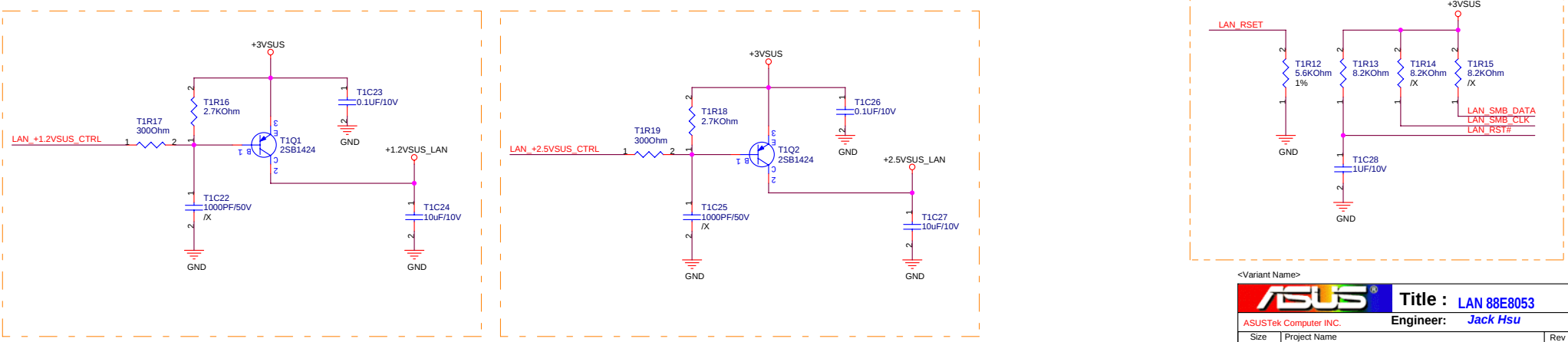
FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

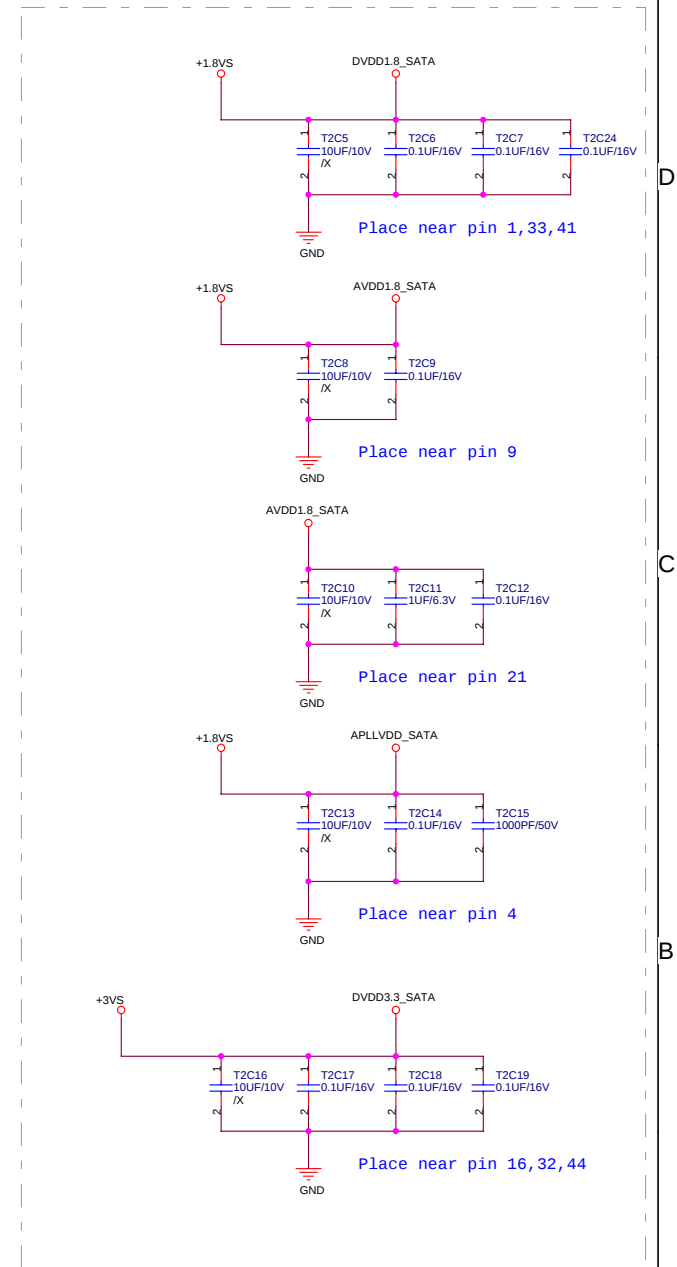
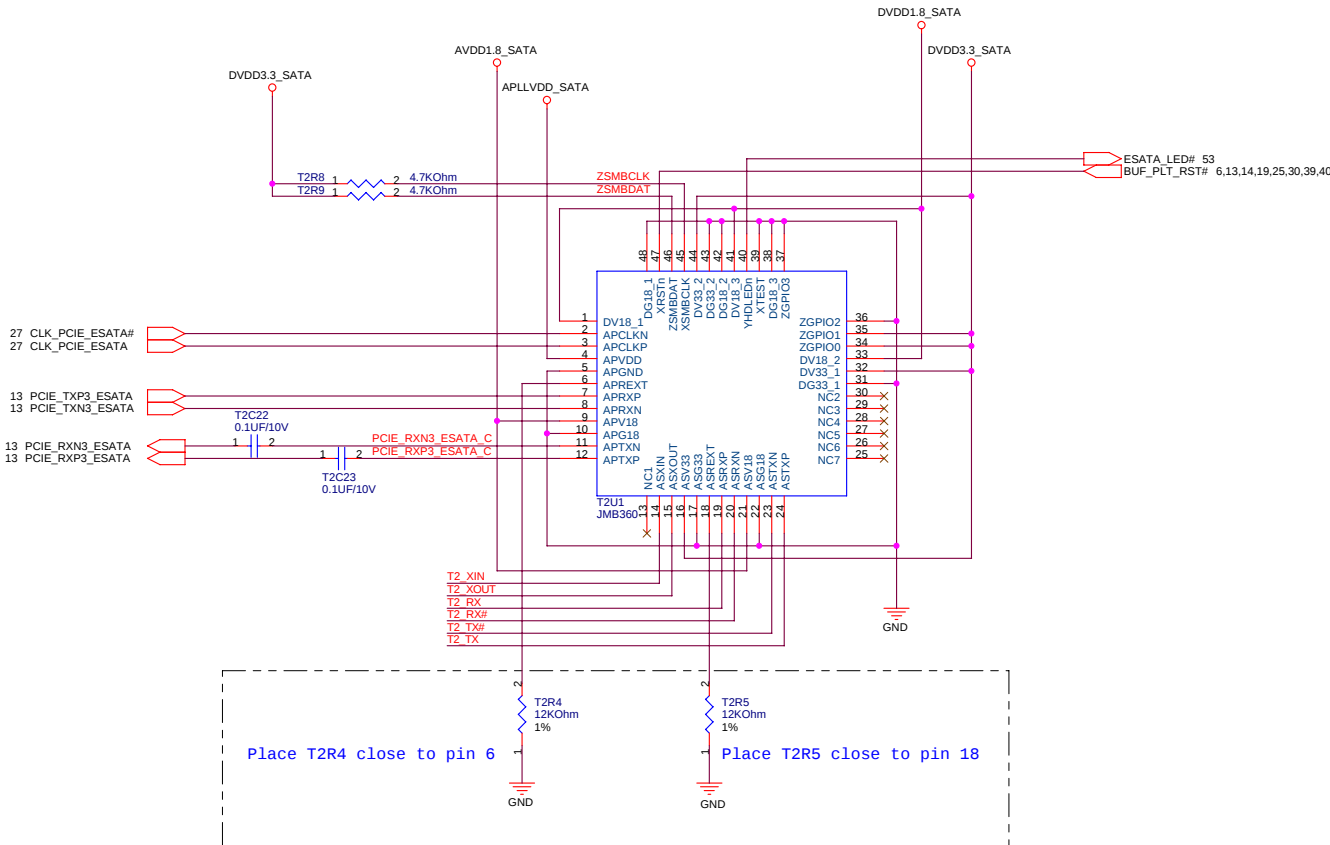
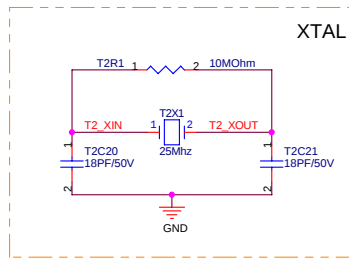
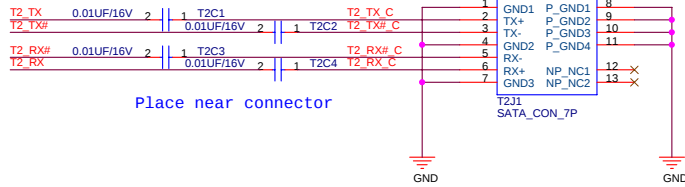




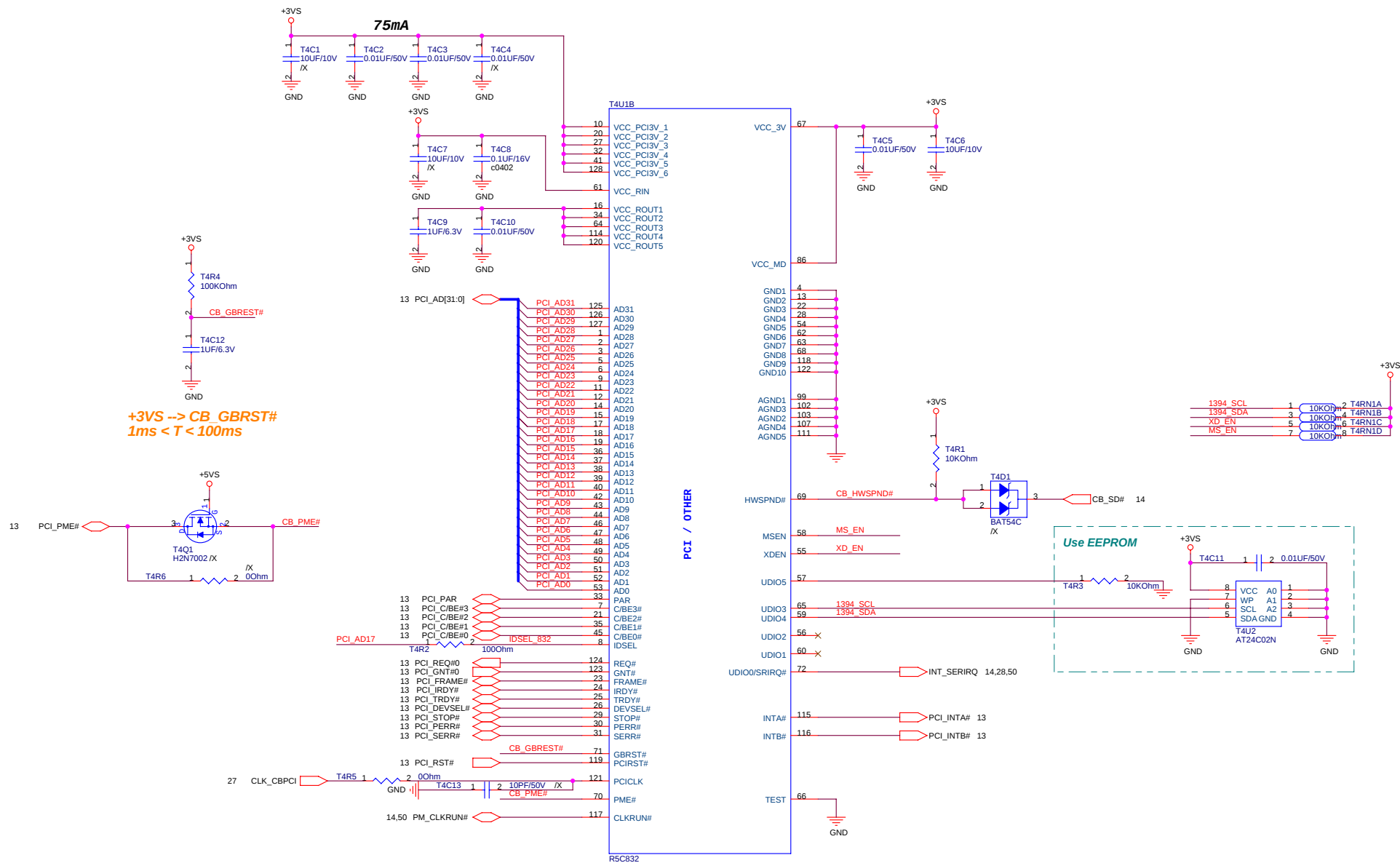
Pin to Pin Compatible with 88E8056
ASUS P/N: 02G751006700



ESATA Connector

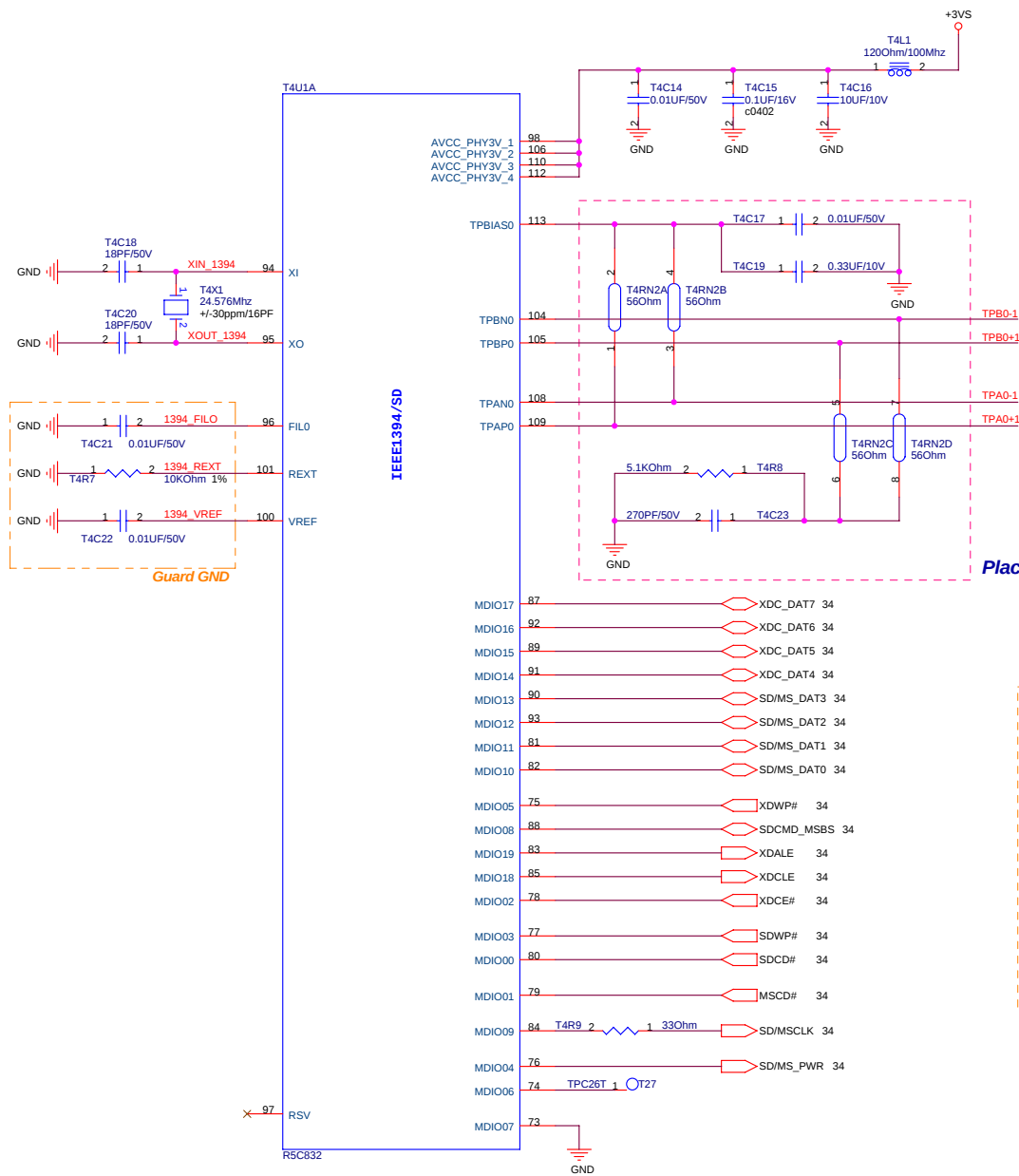


<Variant Name>

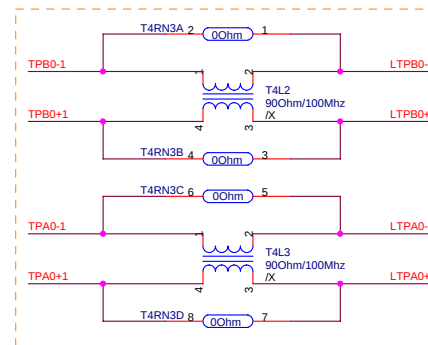


<Variant Name>

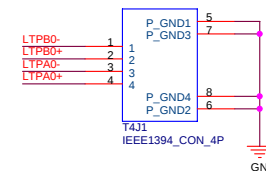
ASUS		Title :R5C832_PCI	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet	32 of 68



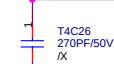
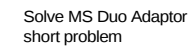
Place close to R5C832

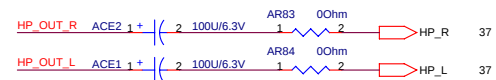
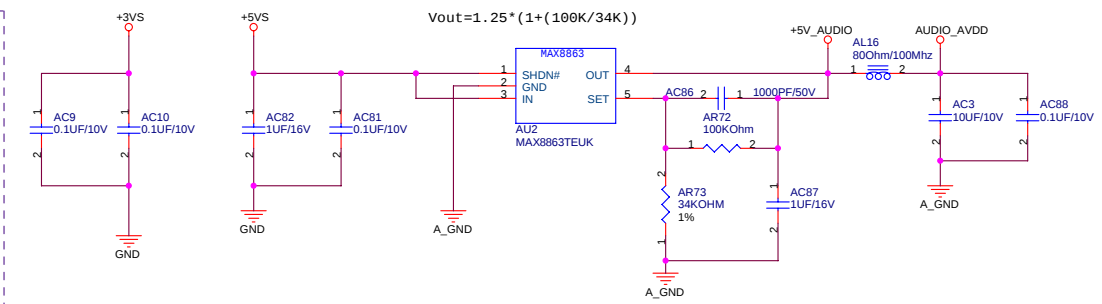
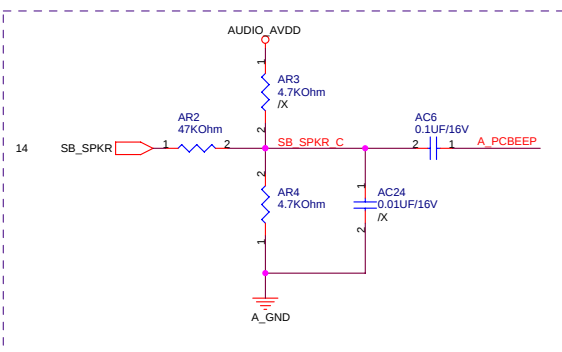


IEEE 1394 Connector

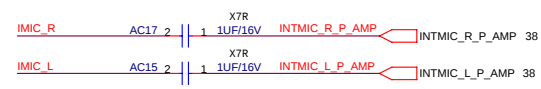


<Variant Name>

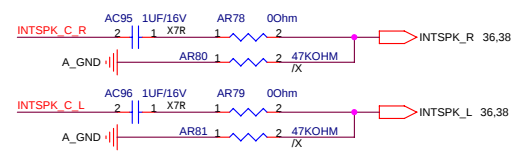




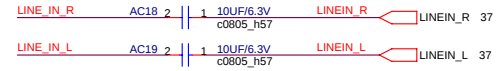
Headphone Output



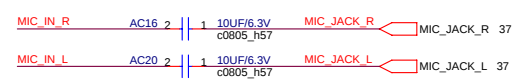
Internal MIC Input



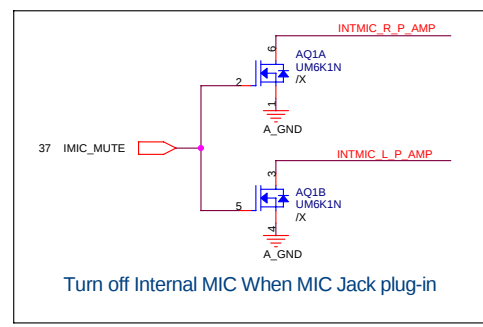
Internal Speaker, Subwoofer Output



Line-In Input

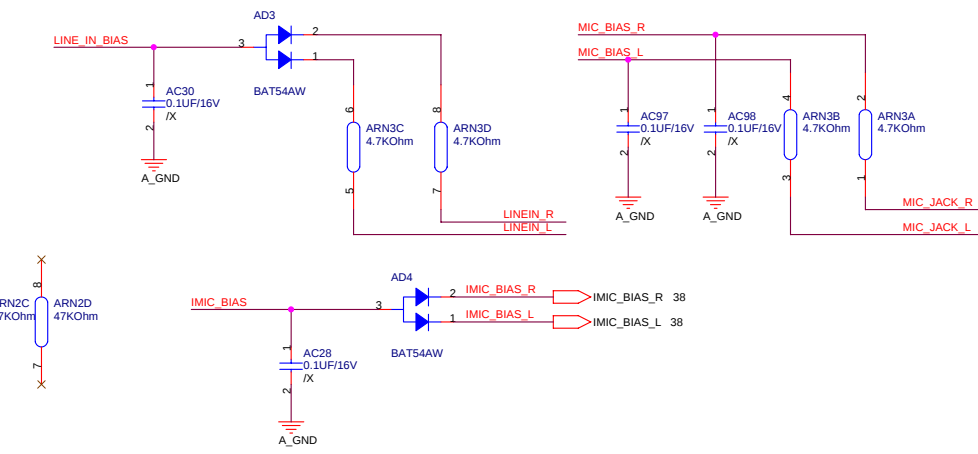
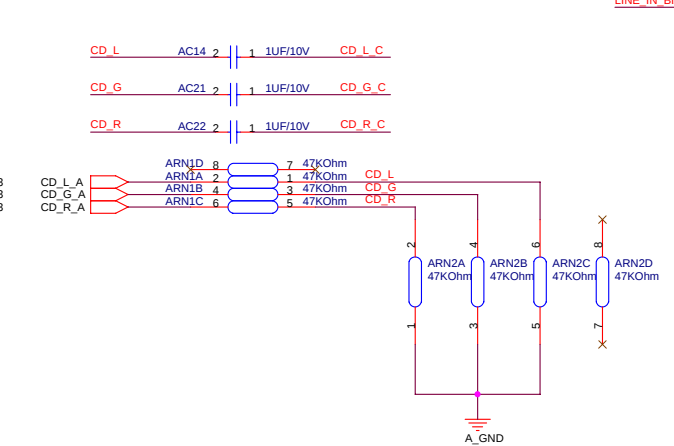


MIC Input



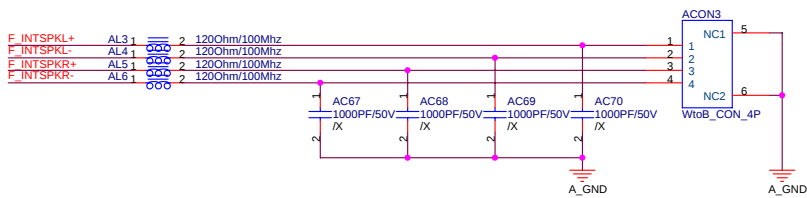
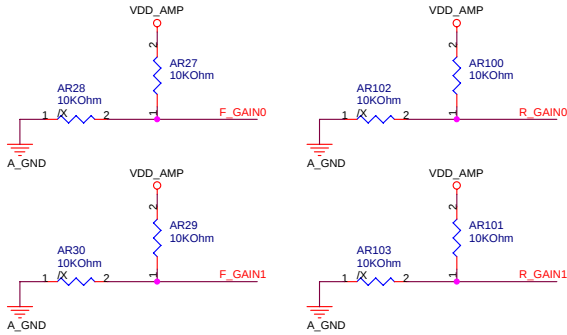
Turn off Internal MIC When MIC Jack plug-in

ASUS P/N: 02G611002900, 02G611002910

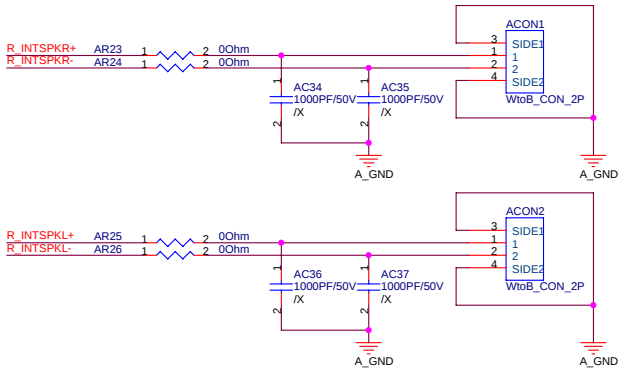


GAIN Control

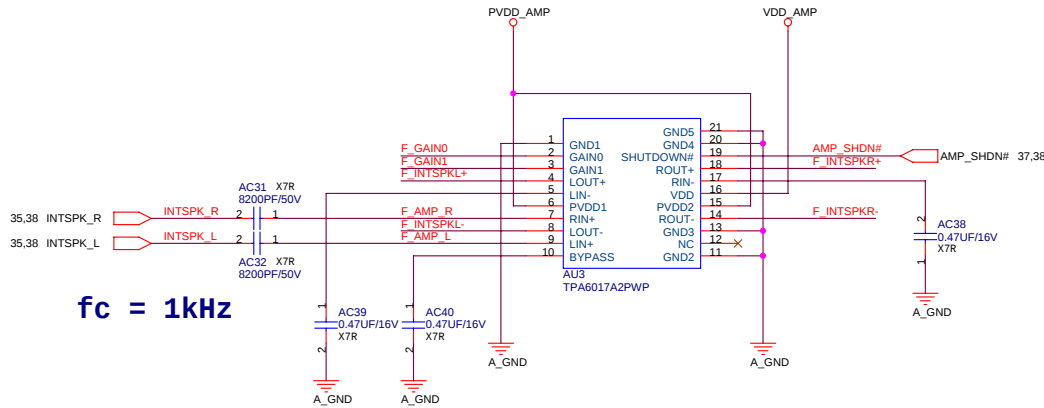
GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



FRONT Speaker Connector

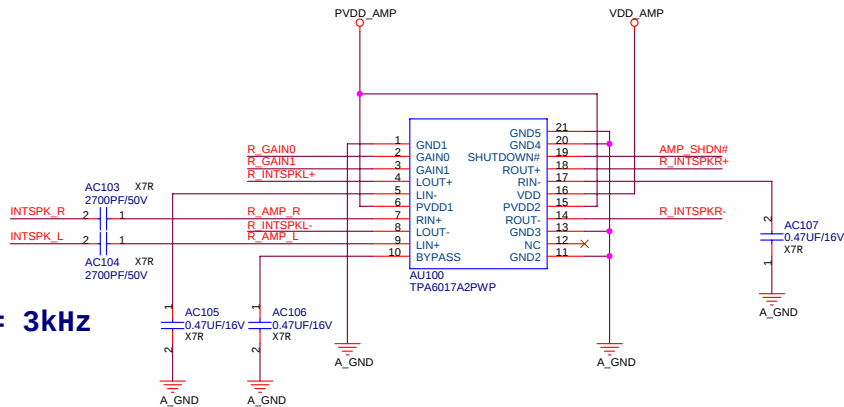


REAR Speaker Connector



fc = 1kHz

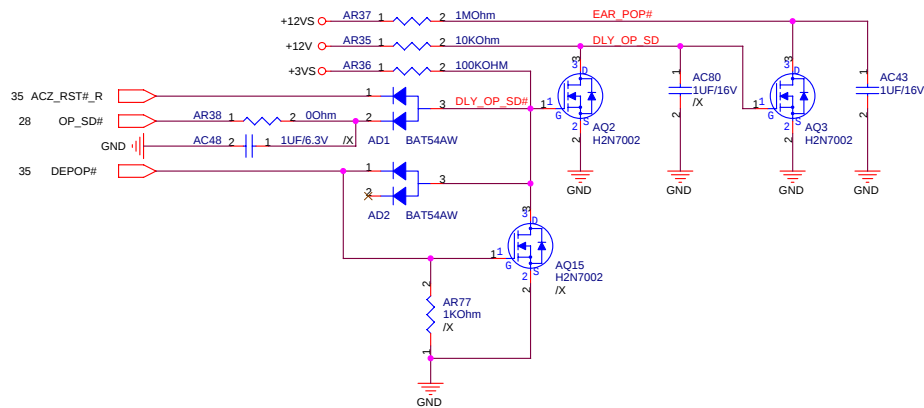
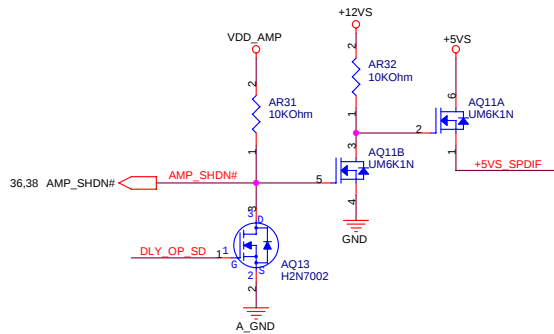
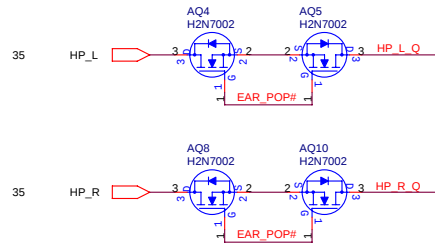
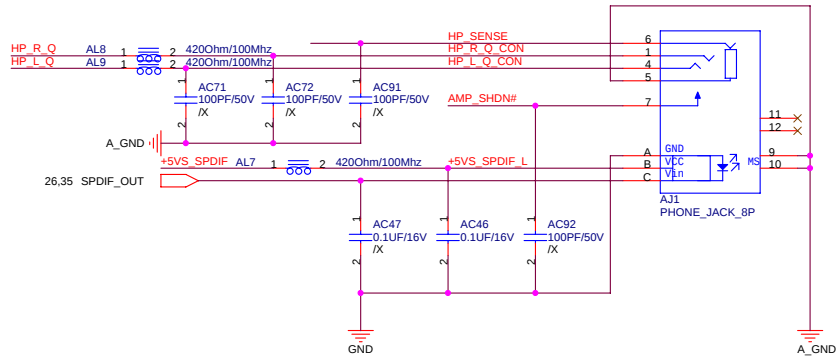
FRONT Audio Amp.



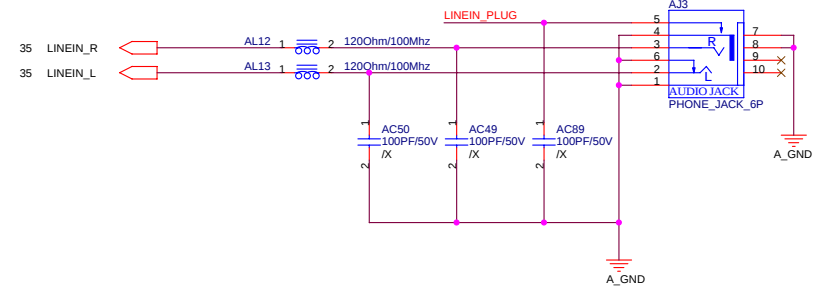
fc = 3kHz

REAR Audio Amp.

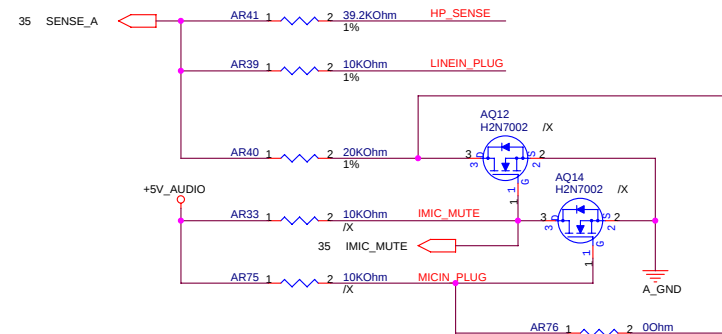
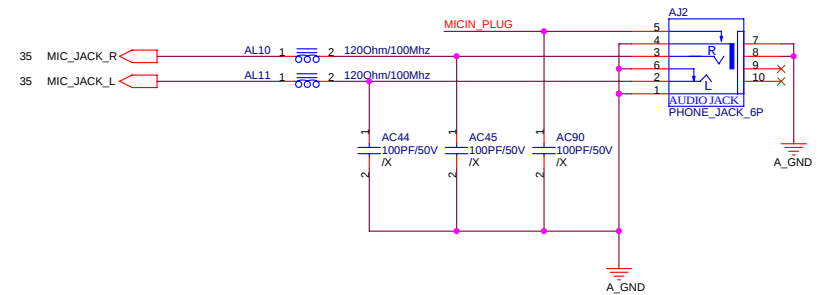
Headphone & S/PDIF Jack



Line-In Jack



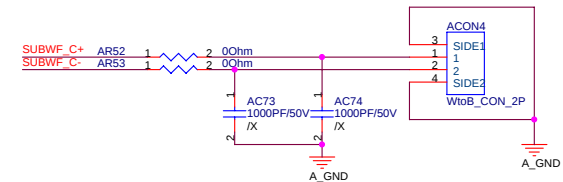
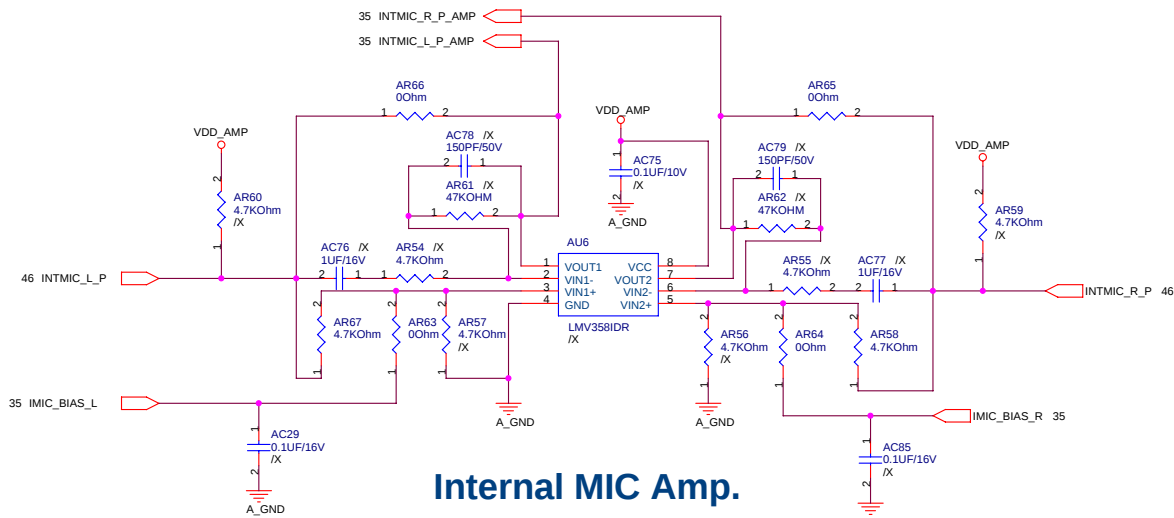
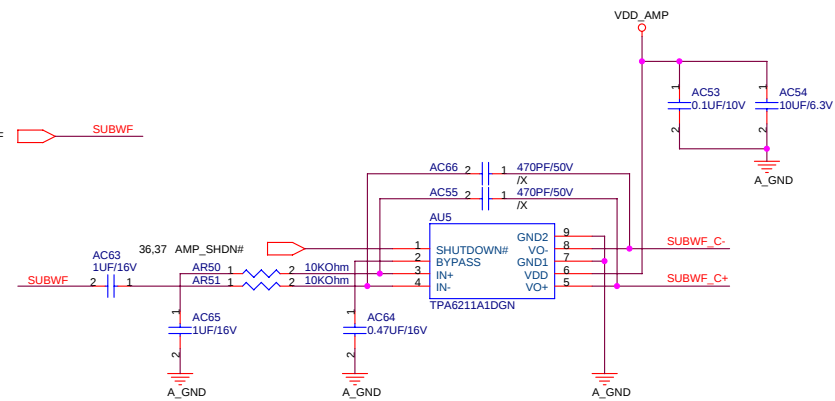
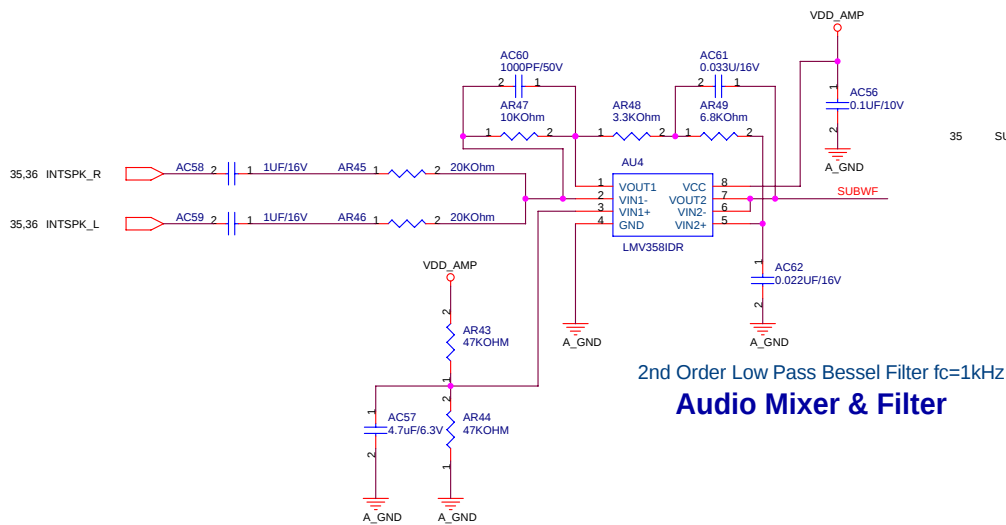
Microphone-In Jack



Jack Plug-in Detection

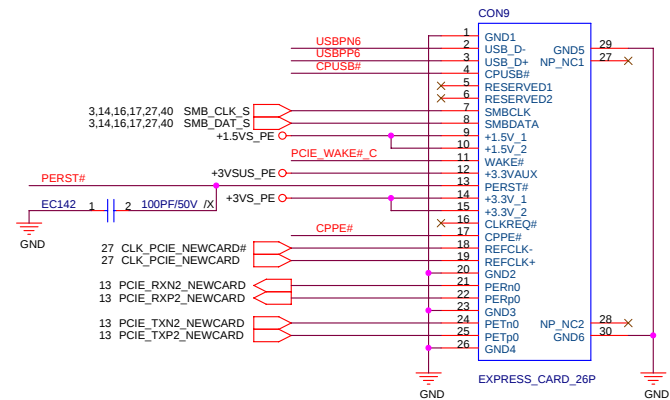
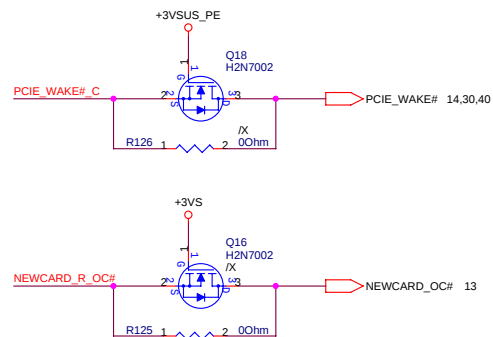
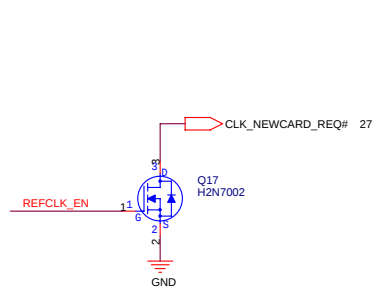
<Variant Name>

ASUS		Title : Audio JACK	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet	37 of 68

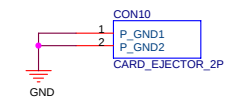


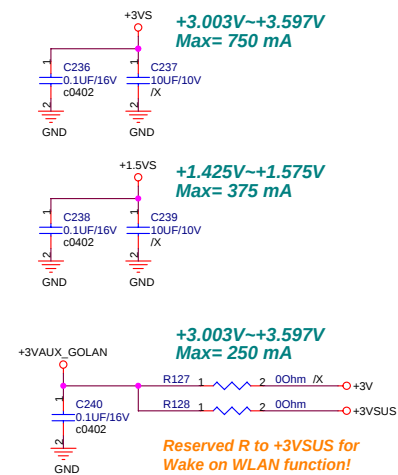
<Variant Name>

ASUS		Title : Subwoofer Amp.	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet 38 of 68	



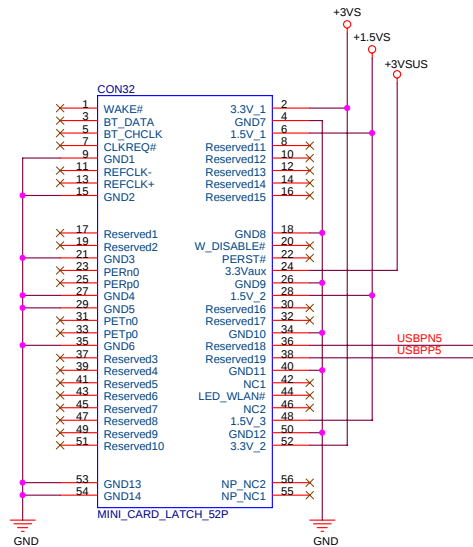
NewCard Ejector



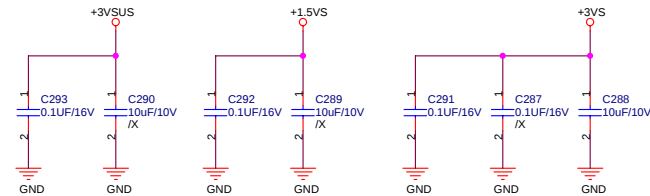
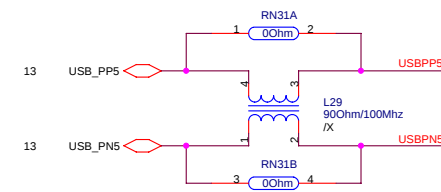


The schematic diagram illustrates the electrical connections for the WLAN module. It features two NPN transistors, Q19 and Q20, both of type HZLN7002. Transistor Q19 is used to drive the WLAN_ON signal. Its base is connected to a +3VS supply through a 10KOhm resistor (R129). The emitter of Q19 is connected to GND, and its collector is connected to the WLAN_ON# signal. Transistor Q20 is used to drive the WLAN_WAKE# signal. Its base is connected to a +3VAUX_GOLAN supply through a 10KOhm resistor (R130). The emitter of Q20 is connected to GND, and its collector is connected to the WLAN_WAKE# signal. The diagram also shows the connection of the WLAN module to the PCIE_WAKE# signal, which is connected to the base of Q20 through a 10KOhm resistor (R130).

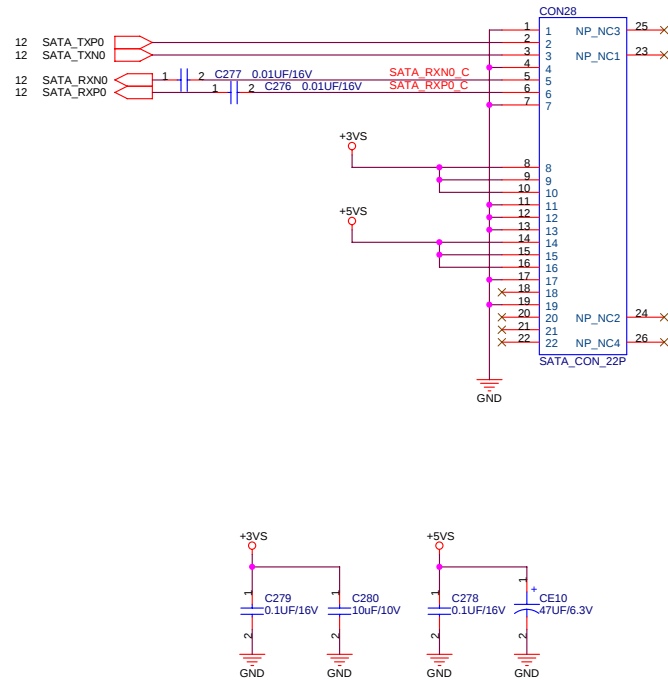
MINICARD For TV-Tuner



USB ONLY H = 6.75mm



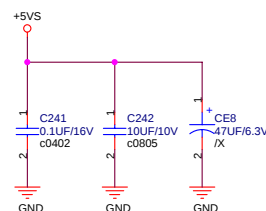
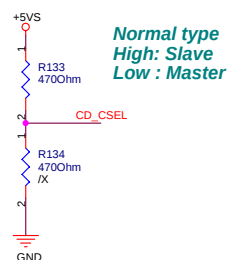
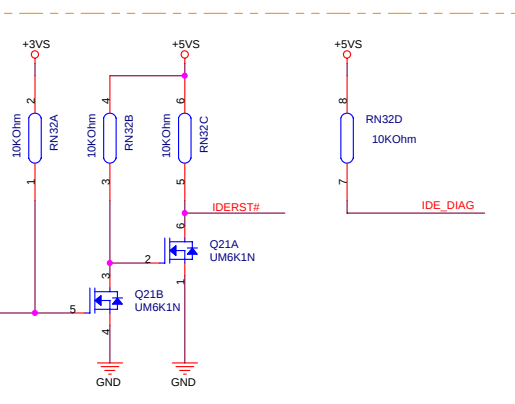
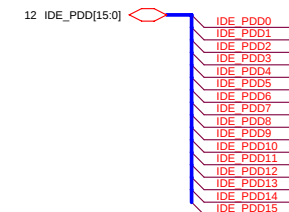
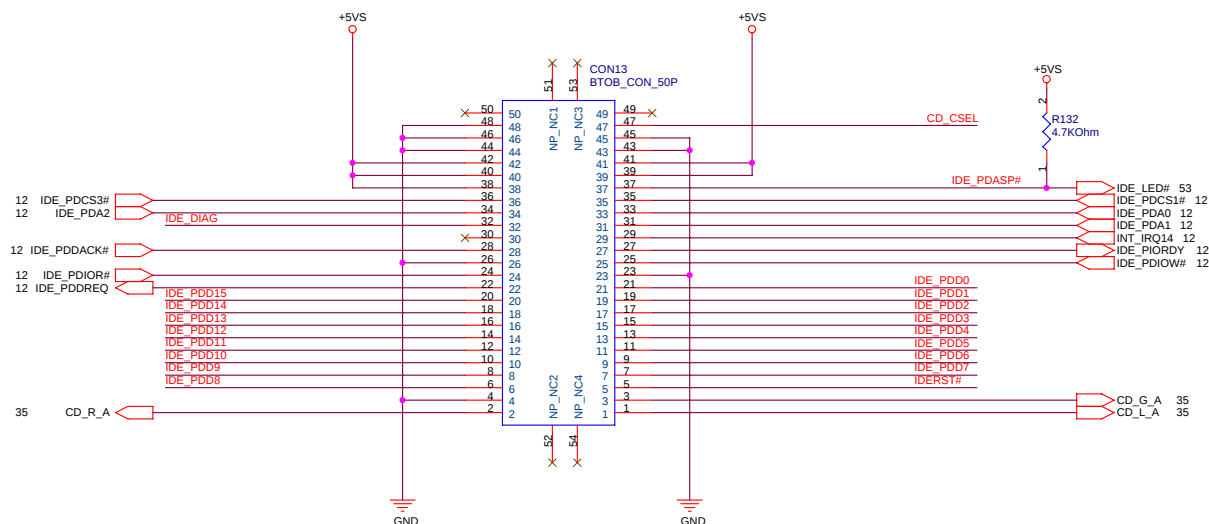
SATA HDD Connector



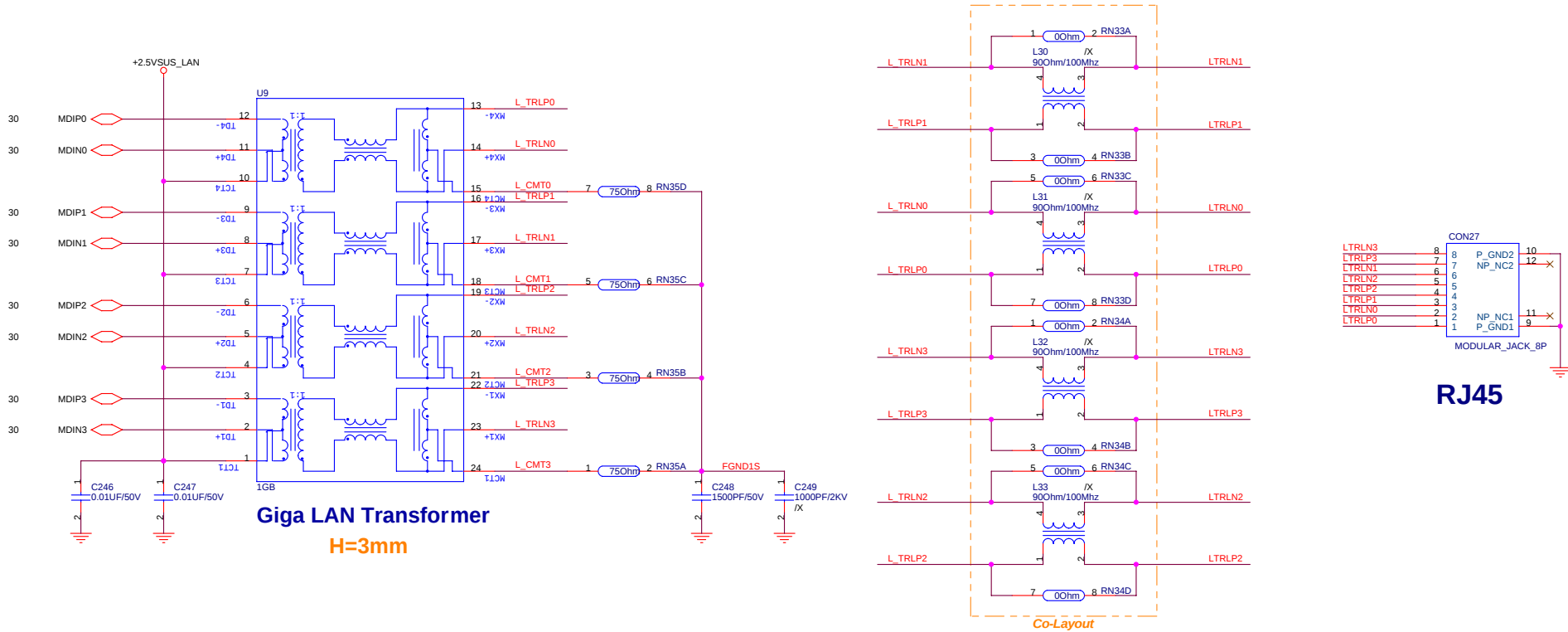
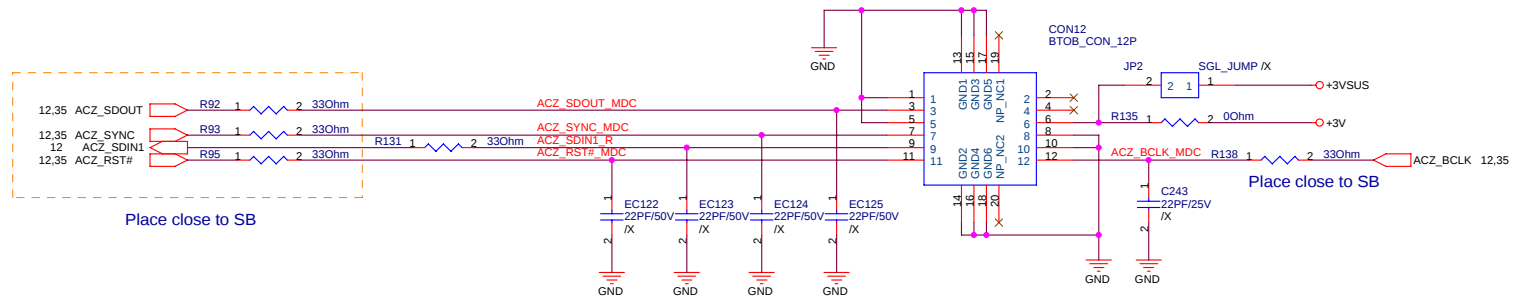
<Variant Name>

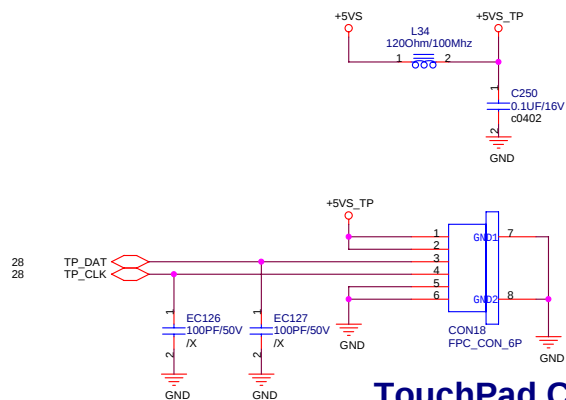
ASUS		Title : SATA HDD Conn.	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size Custom	Project Name Z84J		Rev 1.1
Date: Tuesday, October 10, 2006		Sheet 42 of 68	

ODD Connector

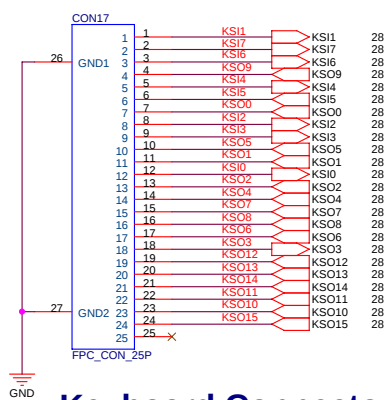


MDC Connector

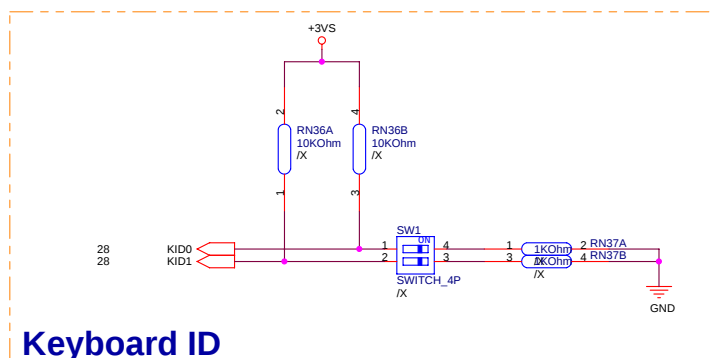




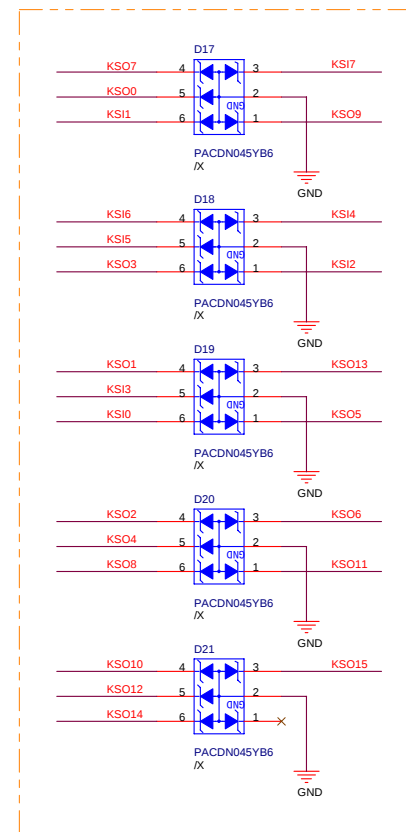
TouchPad Connector



Keyboard Connector

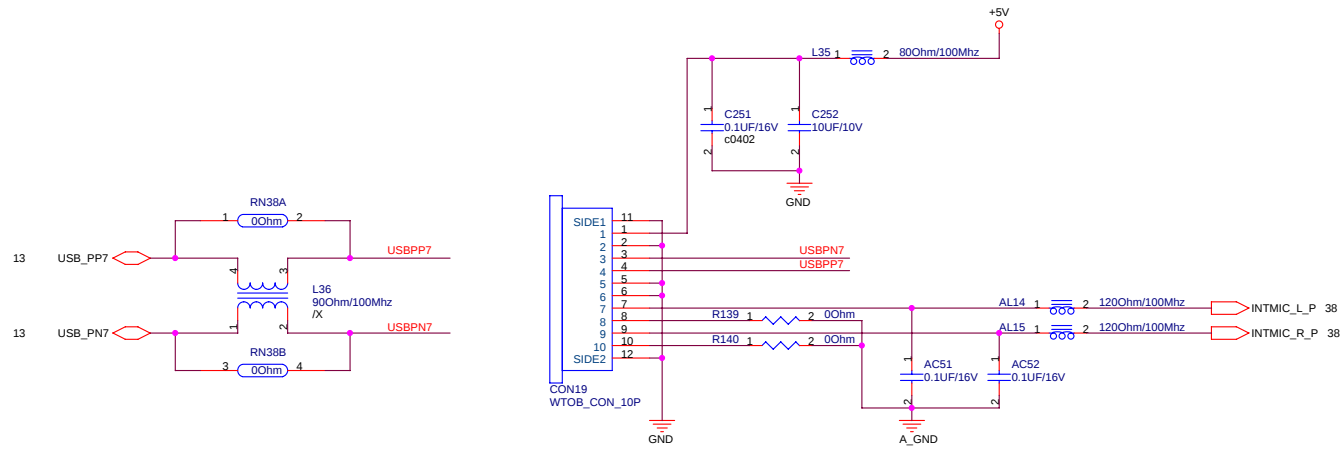


Keyboard ID



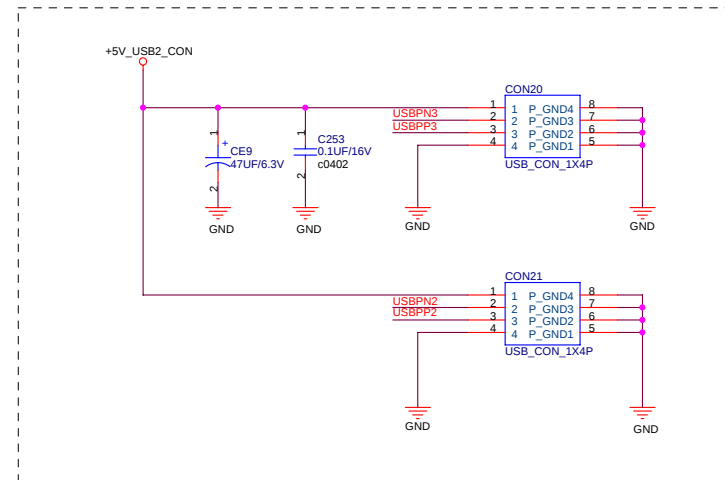
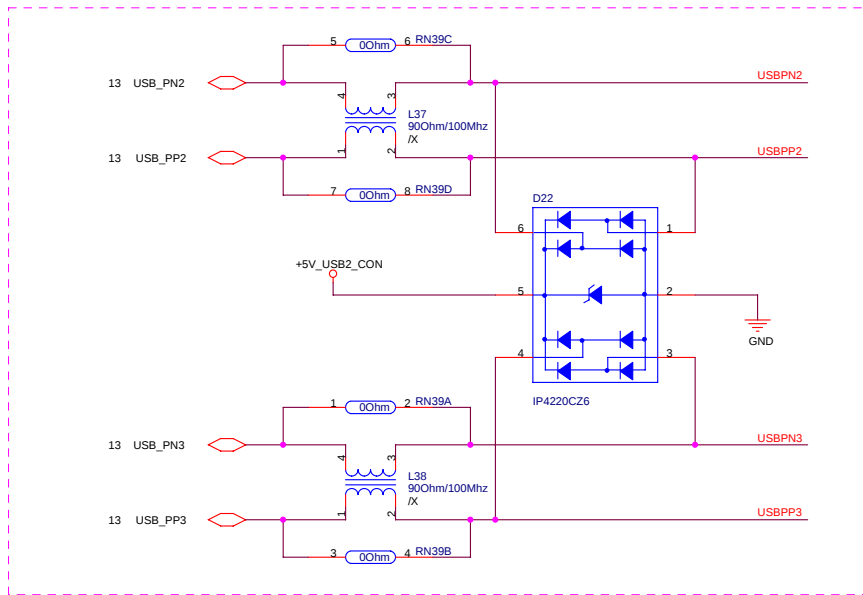
<Variant Name>

Camera & Internal MIC Connector

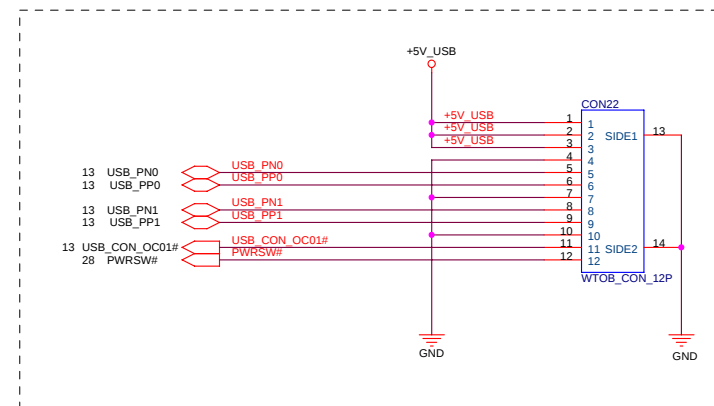


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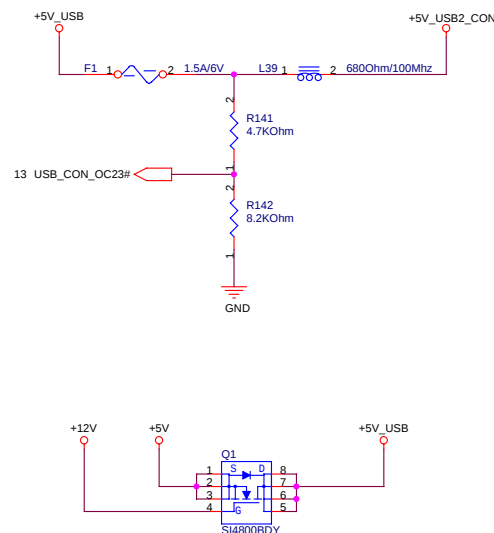
ASUS		Title : Camera Conn.	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z84J		1.1
Date: Tuesday, October 10, 2006		Sheet 46 of 68	



On-board USB Connector

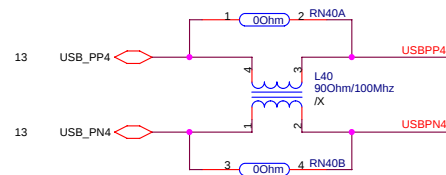
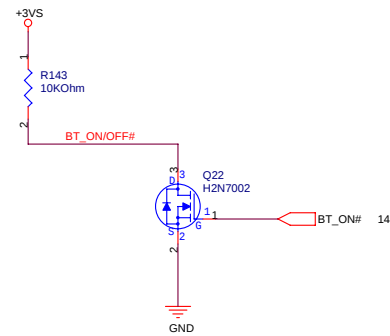
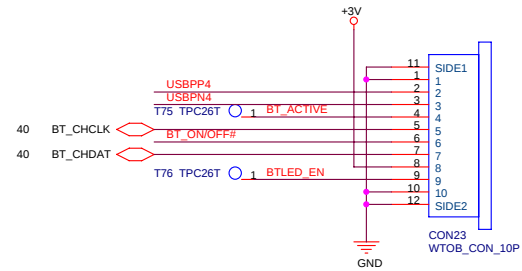


USB Daughter Board Connector



<Variant Name>

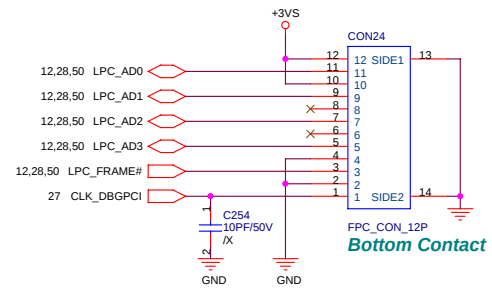
Bluetooth Connector



<Variant Name>

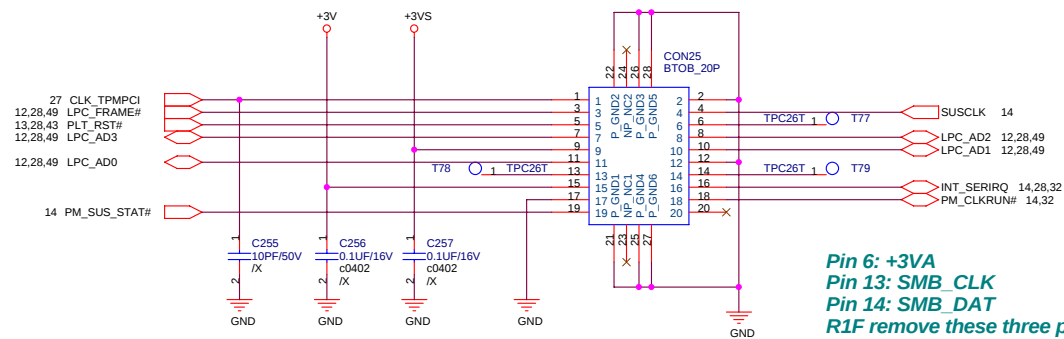
ASUS		Title : Bluetooth Conn.	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006	Sheet	48	of 68

Debug Connector



<Variant Name>

		Title : Debug Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name		Rev
Custom	Z84J		1.1
Date: Tuesday, October 10, 2006		Sheet 49 of 68	

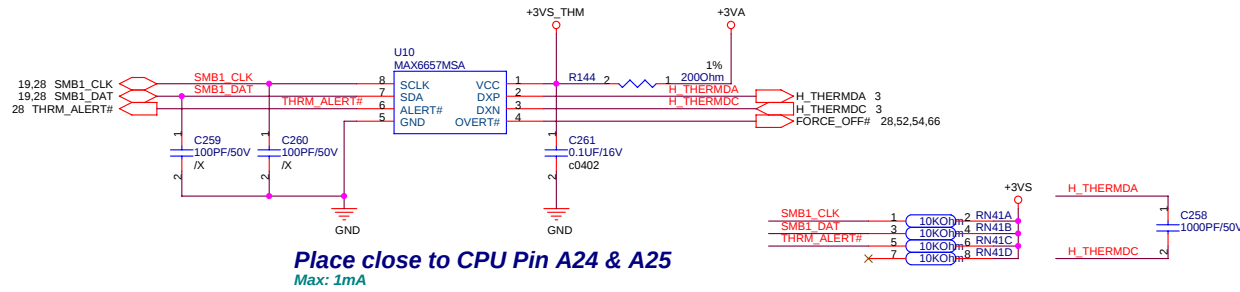


TPM Module Connector

<Variant Name>

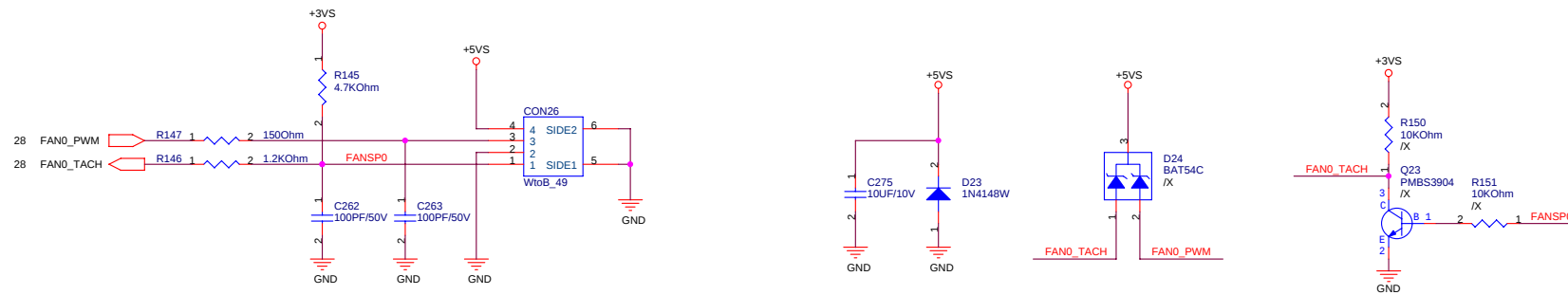
ASUS		Title : TPM Connector	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006	Sheet	50	of 68

CPU Thermal Sensor

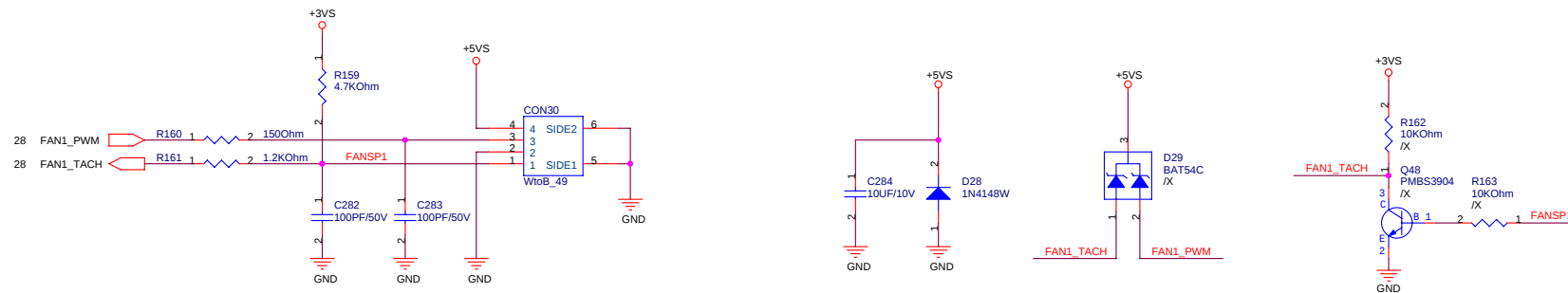


Route H_THERMDA and H_THERMDC in the same layer

OTHER SIGNALS
15 mils
GND
10 mils
H_THERMDA(10 mils)
10 mils
H_THERMDC(10 mils)
10 mils
GND
15 mils
OTHER SIGNALS
Avoid FSB,Power



System Fan Connector

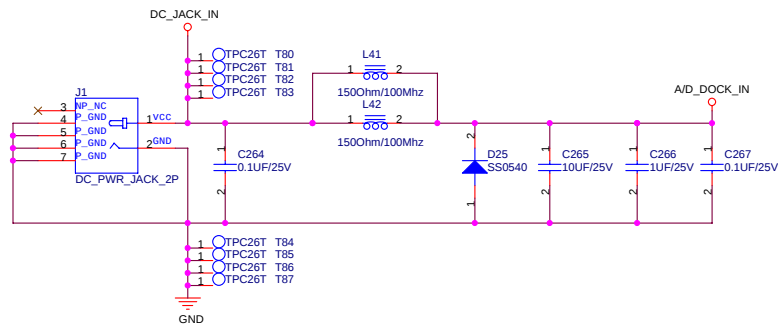


VGA Fan Connector

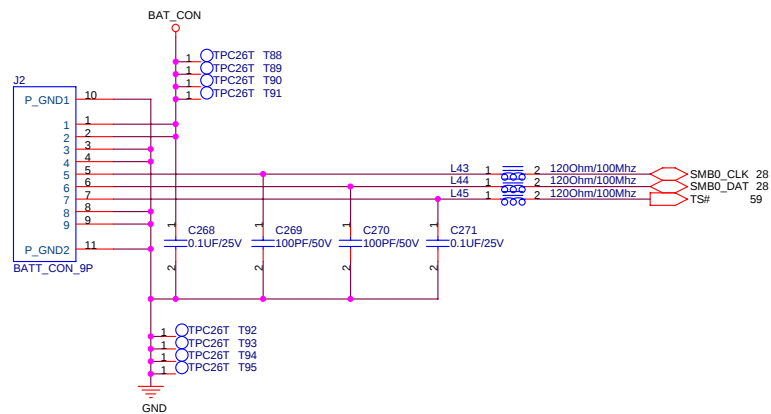
CPU FAN will be forced on:
1) Thermal Sensor Over-temperature
2) WATCHDOG asserted by EC

<Variant Name>

ASUS		Title : Thermal Sensor & Fan	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	284J	1.1	
Date: Tuesday, October 10, 2006	Sheet	51	of 68

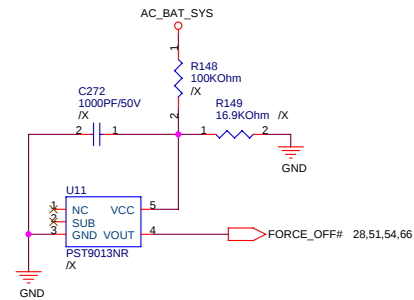


DC-IN Connector



BAT-IN Connector

System Power Loss

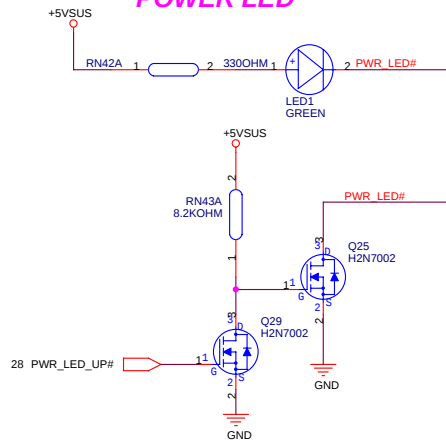


<Variant Name>

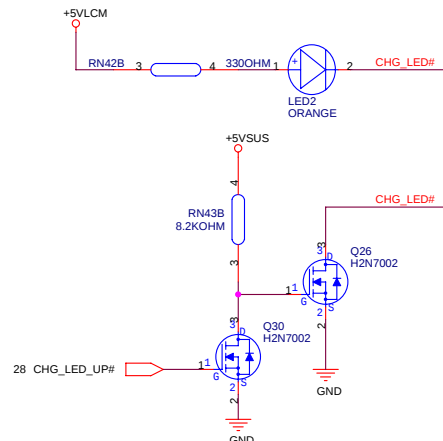
ASUS		Title : DC IN & BAT IN	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date: Tuesday, October 10, 2006		Sheet	52 of 68

LED

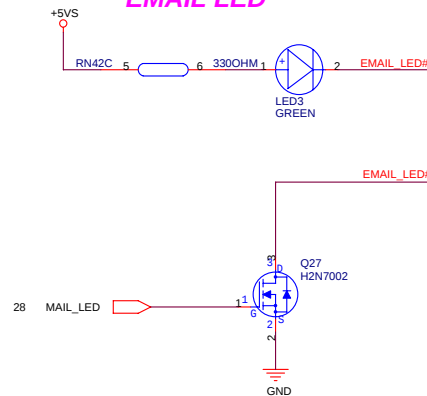
POWER LED



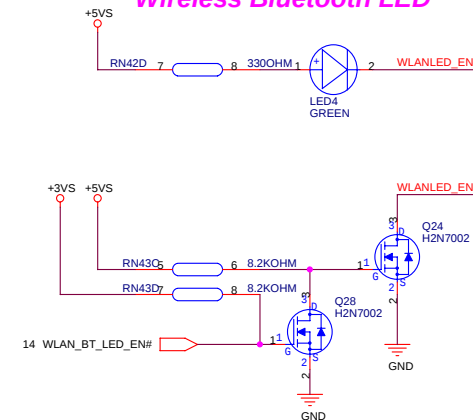
BATTERY CHARGE LED



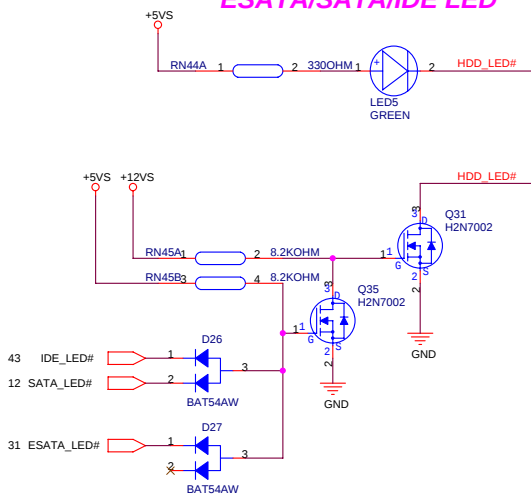
EMAIL LED



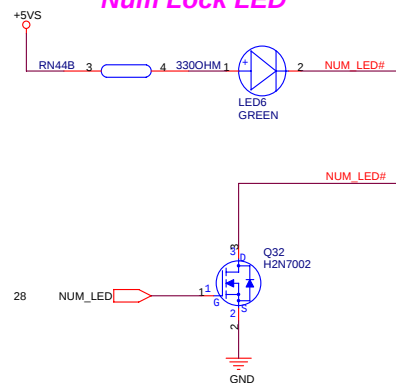
Wireless Bluetooth LED



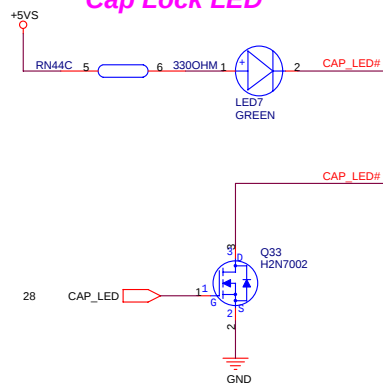
ESATA/SATA/IDE LED



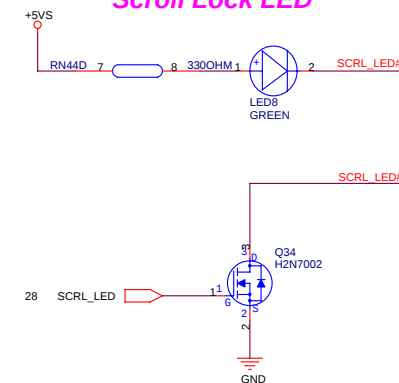
Num Lock LED



Cap Lock LED

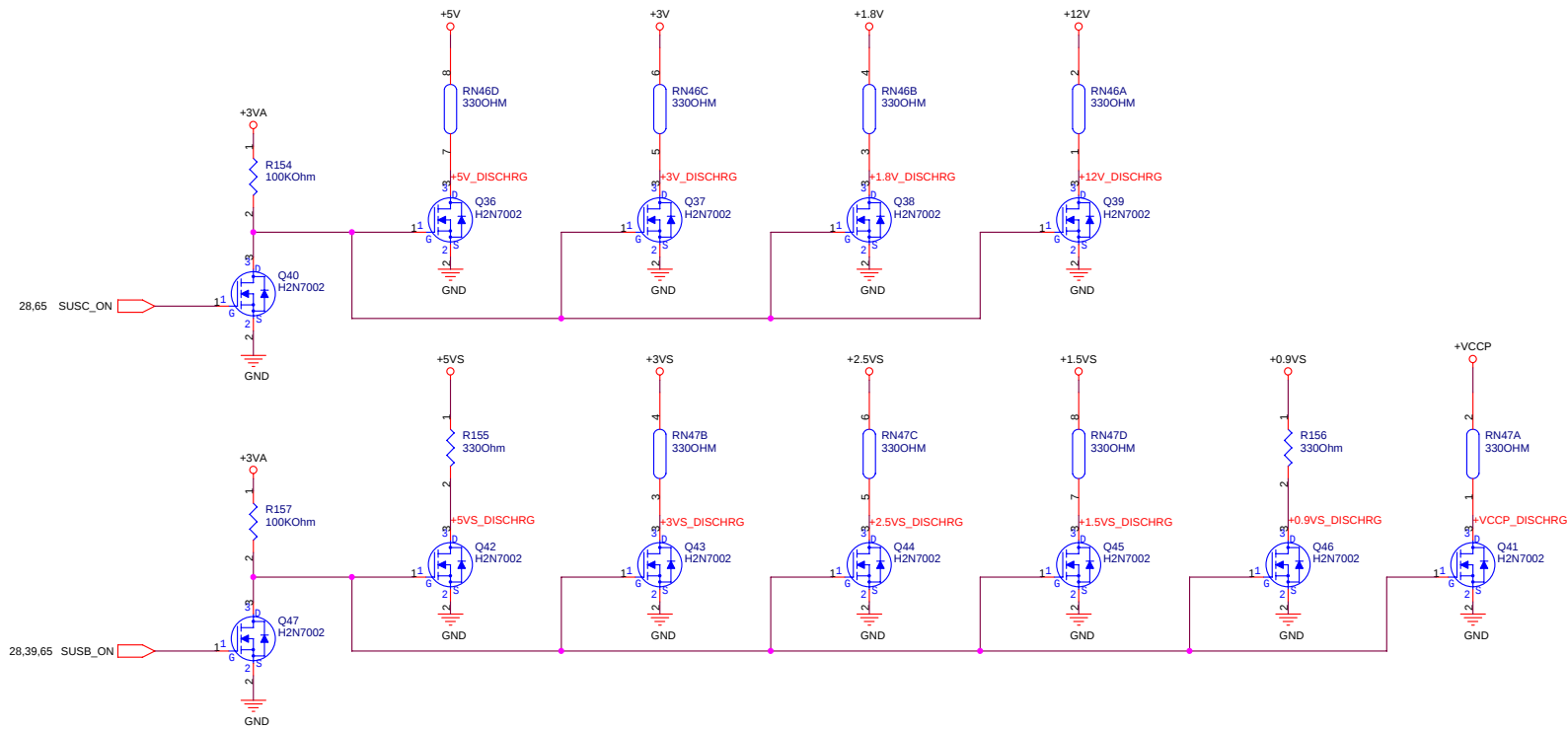


Scroll Lock LED



<Variant Name>

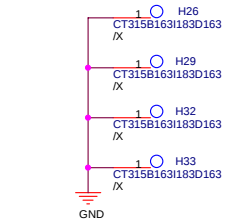
ASUS		Title : LED	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	284J	1.1	
Date: Tuesday, October 10, 2006		Sheet	53 of 68



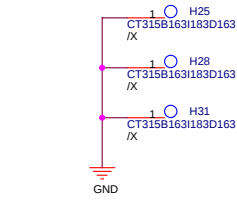
<Variant Name>

ASUS		Title : Discharger	
ASUSTek Computer INC.		Engineer: Jack Hsu	
Size	Project Name	Custom	Rev
Custom	Z84J		
Date: Tuesday, October 10, 2006		Sheet	55 of 68

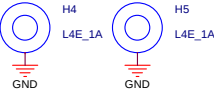
CPU Thermal Housing



North Bridge Thermal Housing



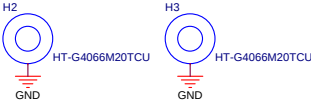
MDC Nut



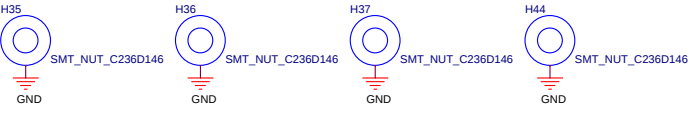
TPM Nut



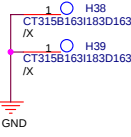
Mini Card Nut



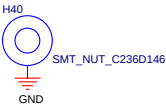
System Fan Nut



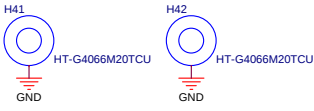
MXM



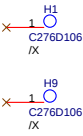
System Nut



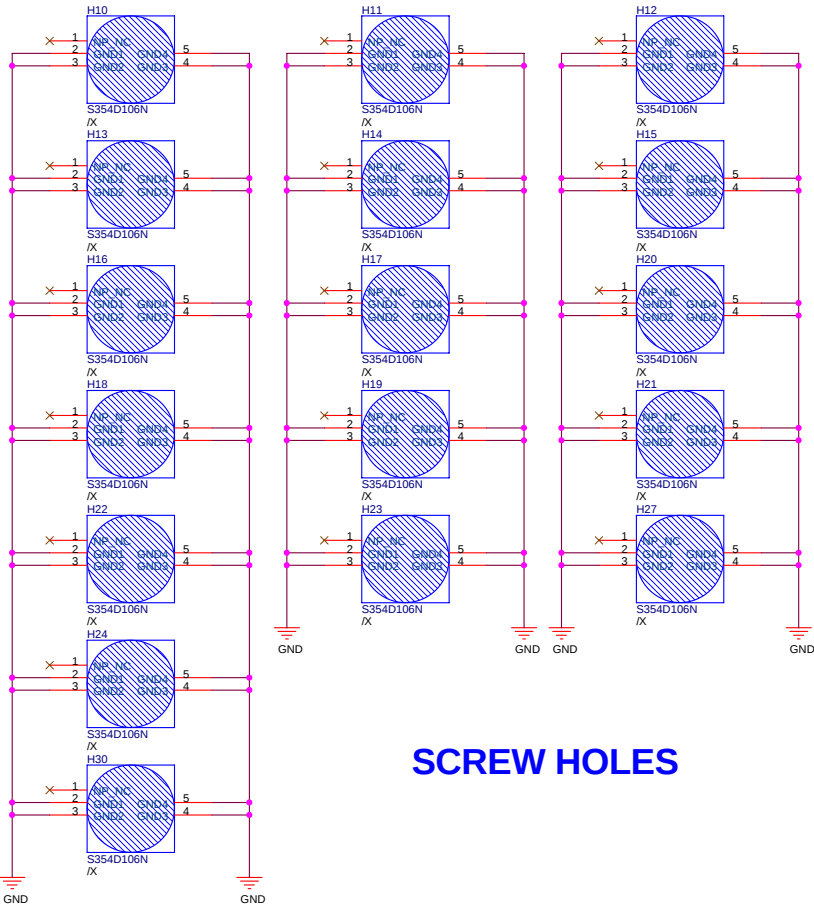
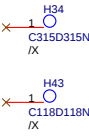
TV-Tuner Nut



PTH HOLE

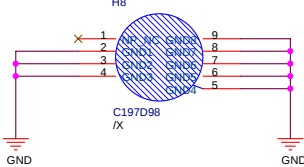


NPTH HOLE

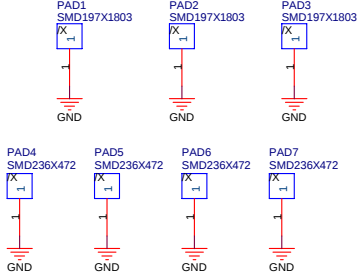


SCREW HOLES

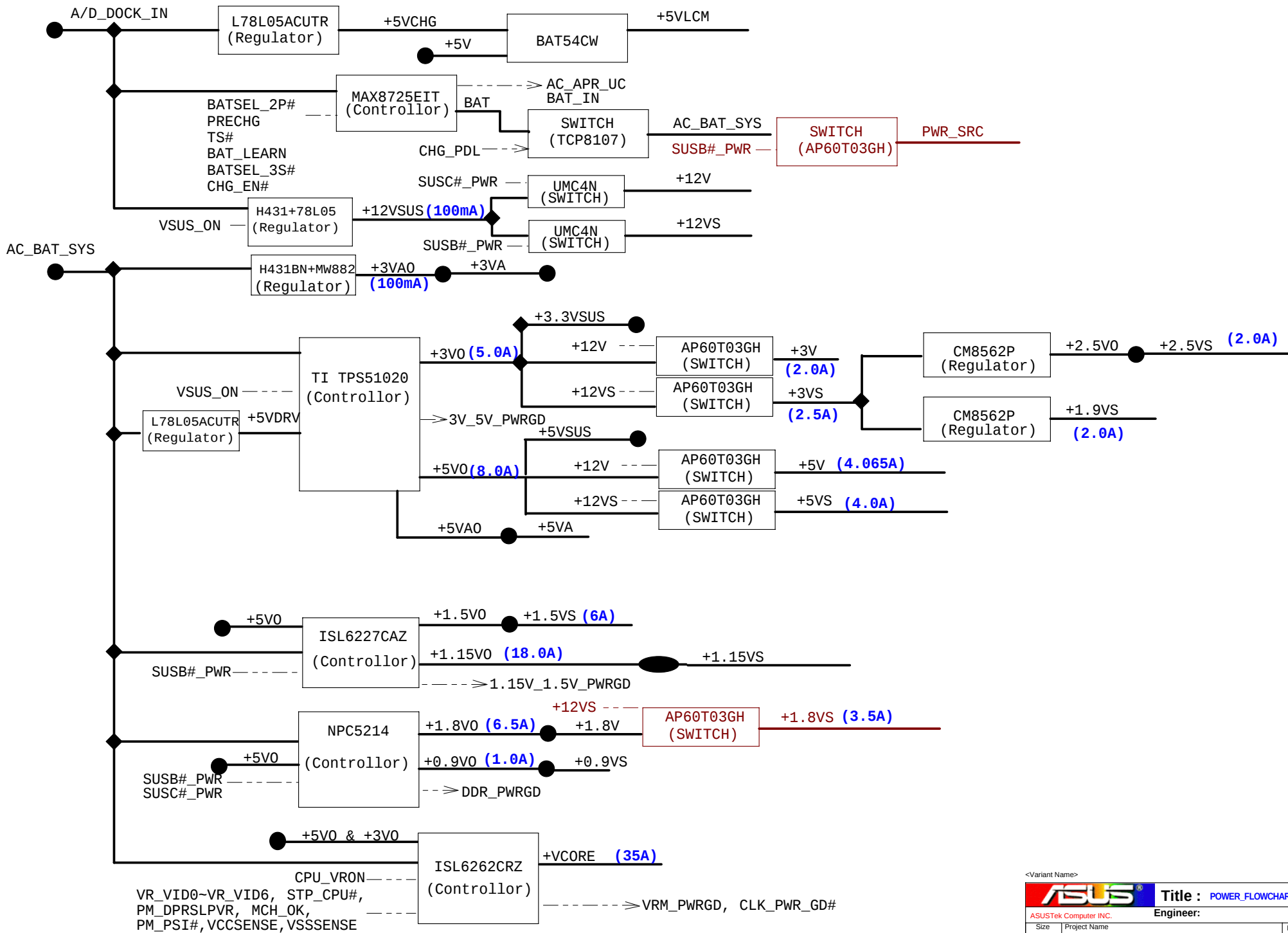
System Fan Screw hole



EMI PAD







AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter lin(max) = $[0.075V/R_{sense}(ADin)] \cdot [V_{CLS}/V_{REF}]$
 $V_{CLS} = 2.865V$

Adaptor Max. Current :

PR5708=20K PR5714 = 178K; I_{limit} = 4.5A; 81W
PR5708=27K PR5714 = 47K; I_{limit} = 3.175A; 60W

Setting the Charge Voltage

$$V_{batt} = Cell * \{ V_{ref} + [(V_{CTL} - 1.8V) / 9.52] \}$$

$$V_{CTL} = 1.588V \Rightarrow V_{batt} = 4.2V$$

Setting the Charge Current

Charge Current $I_{chg} = [0.075V/R_{sense}(CHG)] * [V_{ICTL}/3.6V]$
 $R_{sense}(CHG) = 15m\ \Omega$

Pre-Charging Mode :

Precharging current = 148 ~ 152mA

$$V_{ictl} = 0.107V \sim 0.109V$$

Battery Cell Selection :

BATSEL_2P# = 1, 3 Cells; Vct1 = 2.084V

$$\Rightarrow I_{charge} = 1.6933A$$

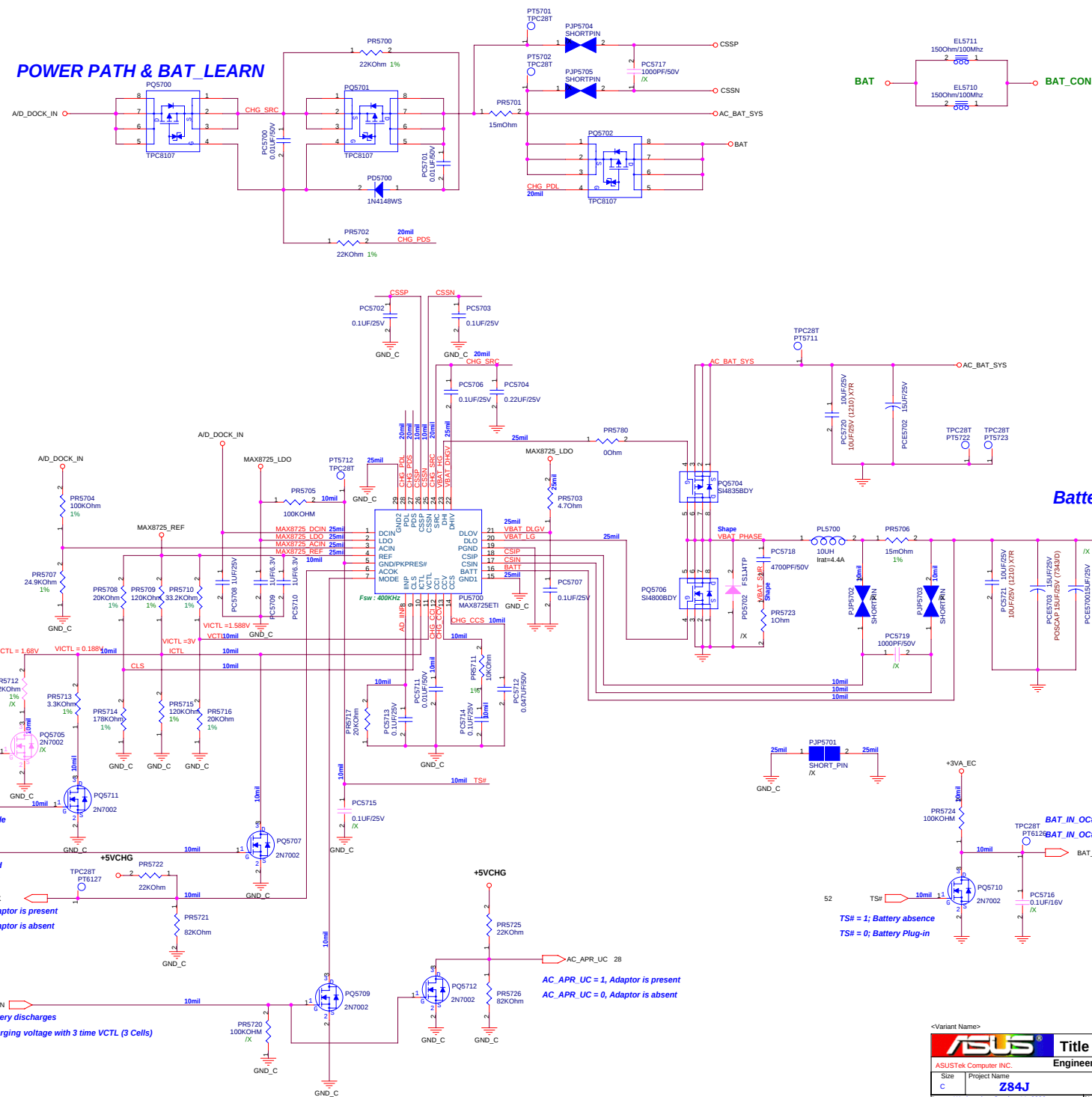
BATSEL 2P# = 0, 6 or 9 Cells: Victl = 2.111V

$$\Rightarrow I_{\text{charge}} = 2.9329 \text{ A}$$

PR5709=120K PR5715 = 120K; Icharge = 2.9329A

Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (try to GND) ----> Learning mode
VICTL < 0.8V or DCIN < 7V --> Charger Disable

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V



Battery Voltage

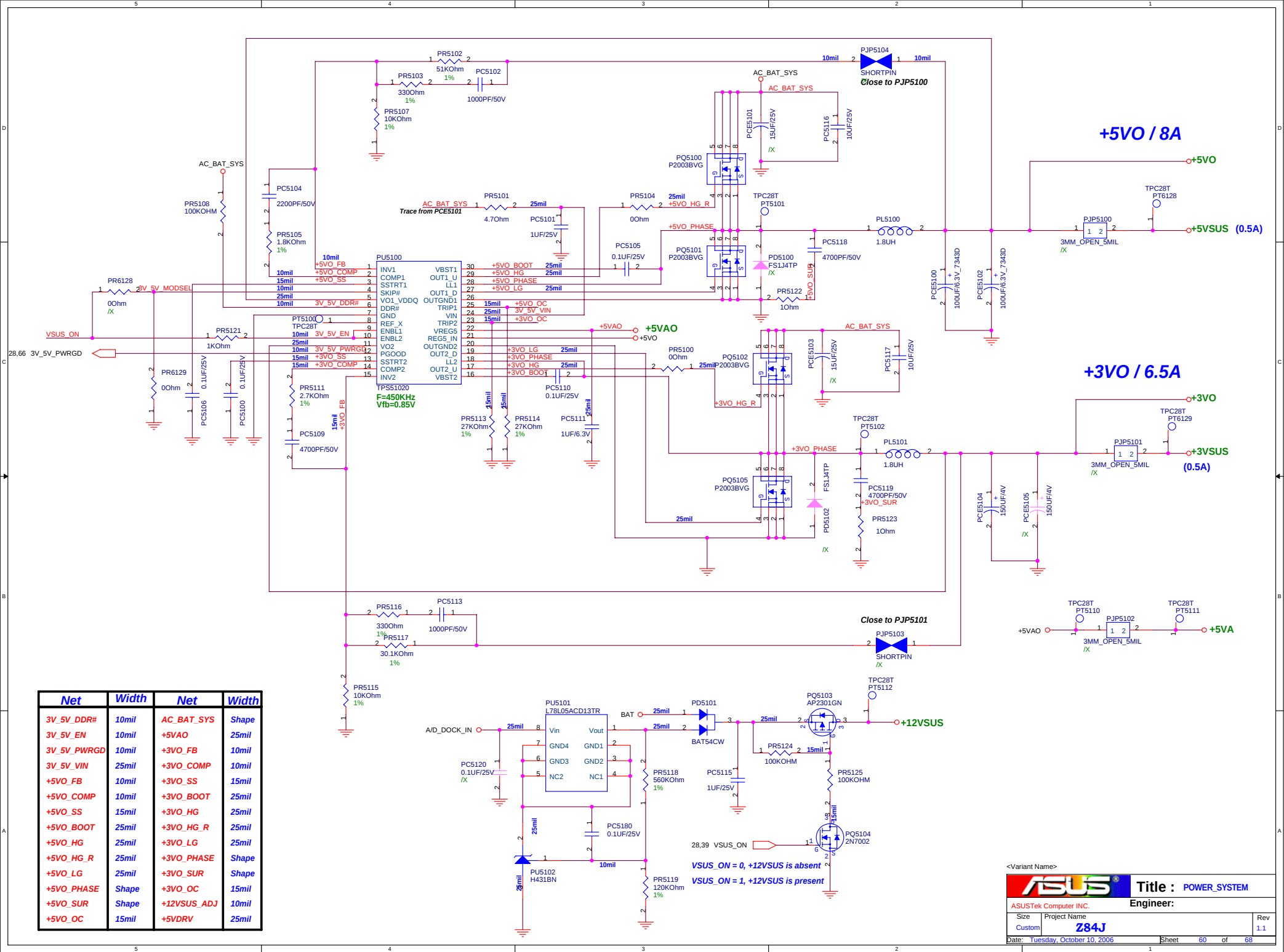
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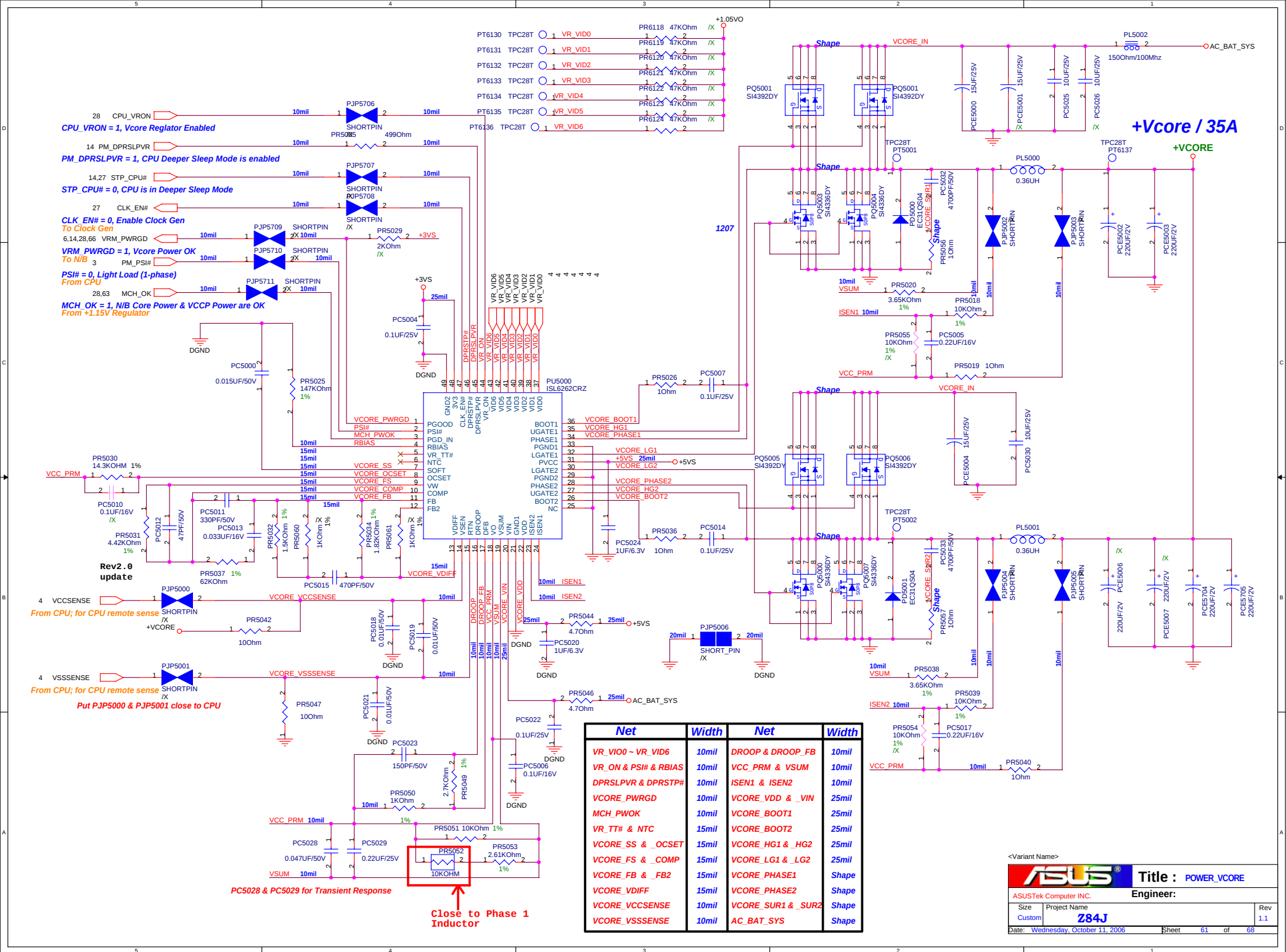


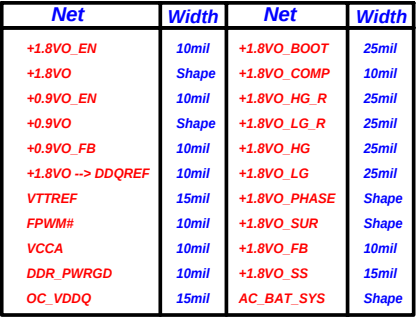
Title : POWER CHARGER

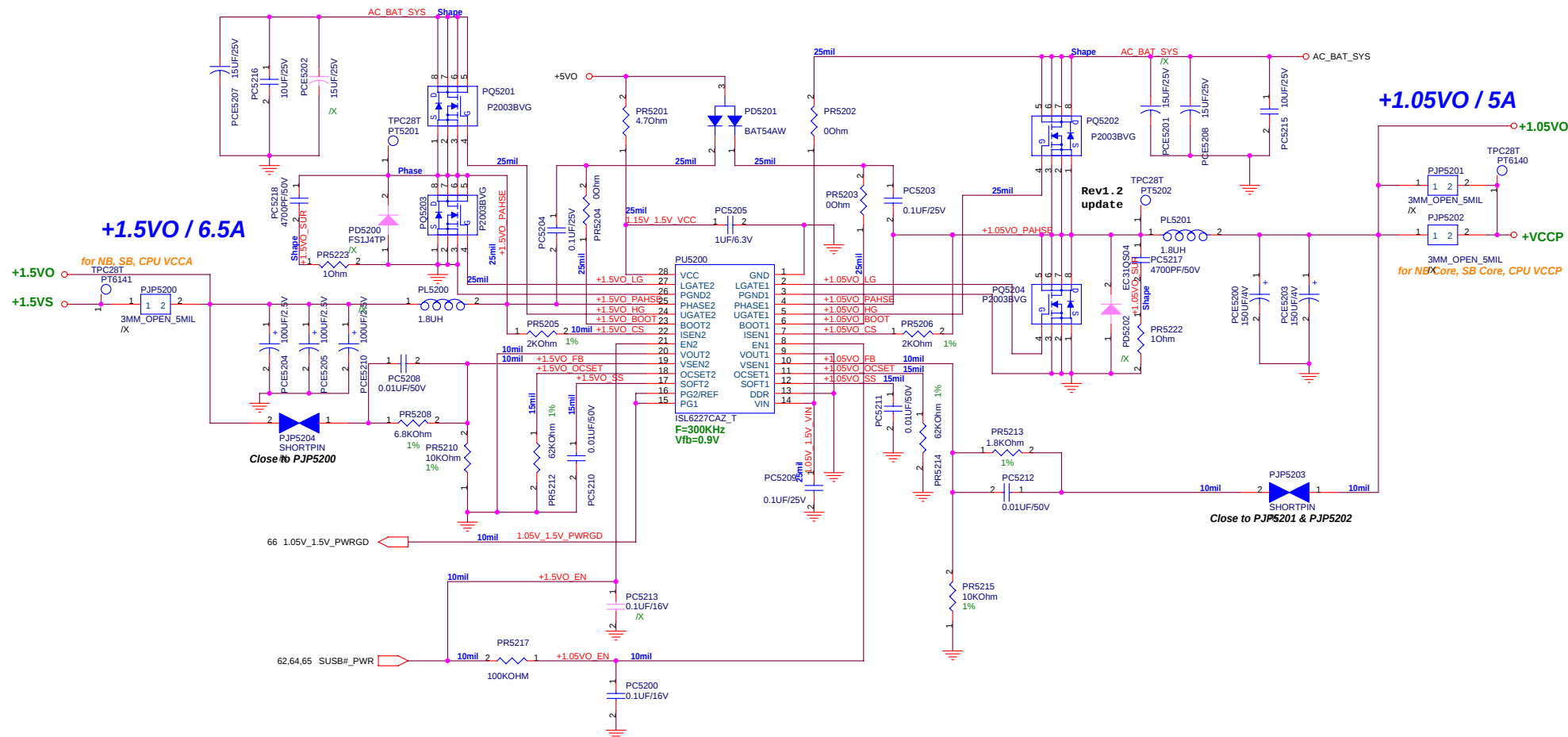
Engineer:

Size C	Project Name Z84J
Date: Wednesday, October 11, 2006	Sheet 59 of 68









+1.05VO / 5A

TPC28T
PT5202
3MM_OPEN_5MIL
PJP5202
3MM_OPEN_5MIL
for NB,Core, SB Core, CPU VCCP

+1.5VO / 6.5A

for NB, SB, CPU VCCA
TPC28T
PT5201
3MM_OPEN_5MIL
PJP5201
3MM_OPEN_5MIL
for NB,Core, SB Core, CPU VCCP

Close to PJP5202

Close to PJP5201 & PJP5202

Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

<Variant Name>



Title :POWER_I/O_1.5VS & 1.05VS

ASUSTek Computer INC.

Engineer:

Size

Project Name

Custom

Z84J

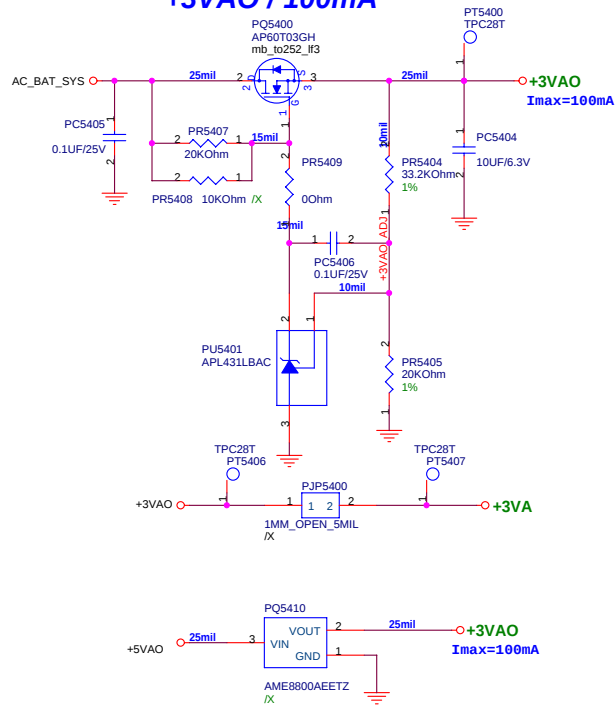
Rev

1.1

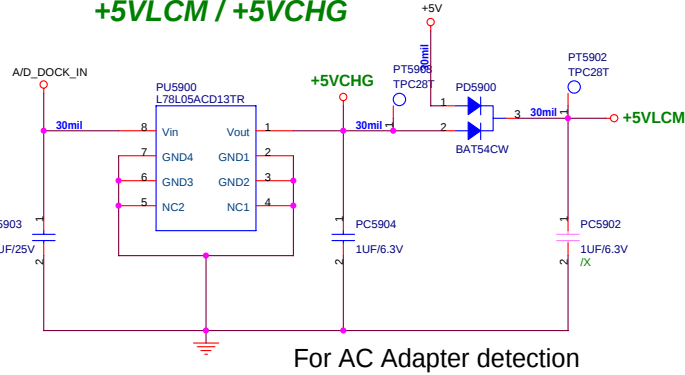
Date: Tuesday, October 10, 2006

Sheet 63 of 68

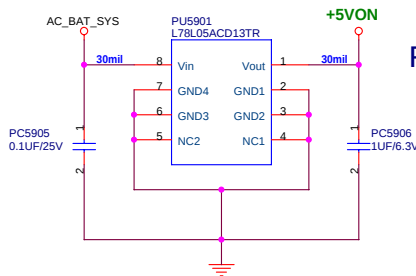
+3VAO / 100mA



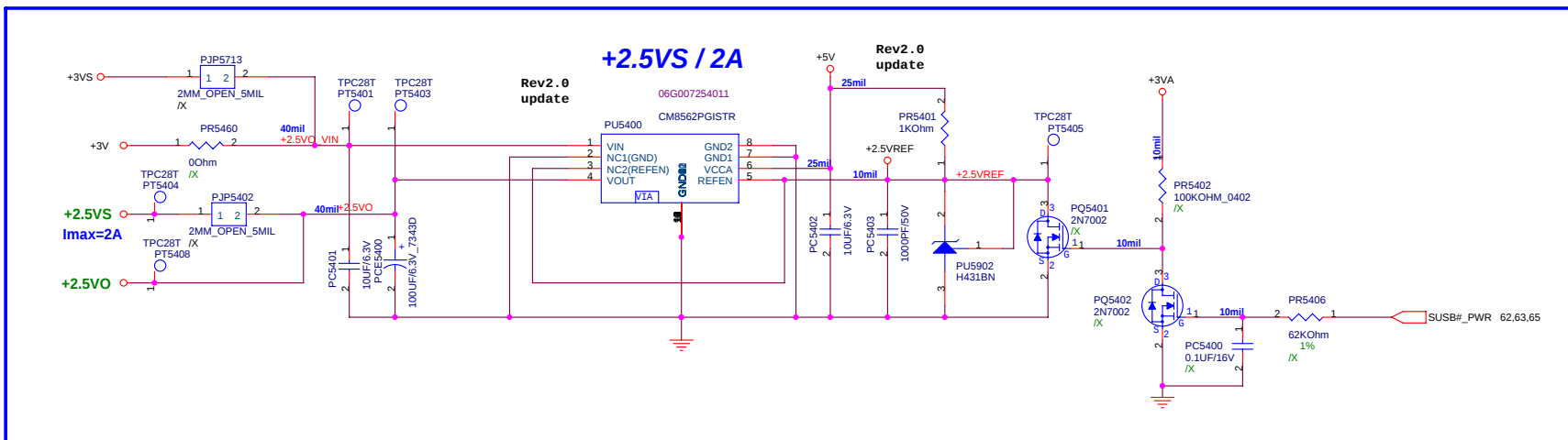
+5VLCM / +5VCHG



For CIR Power

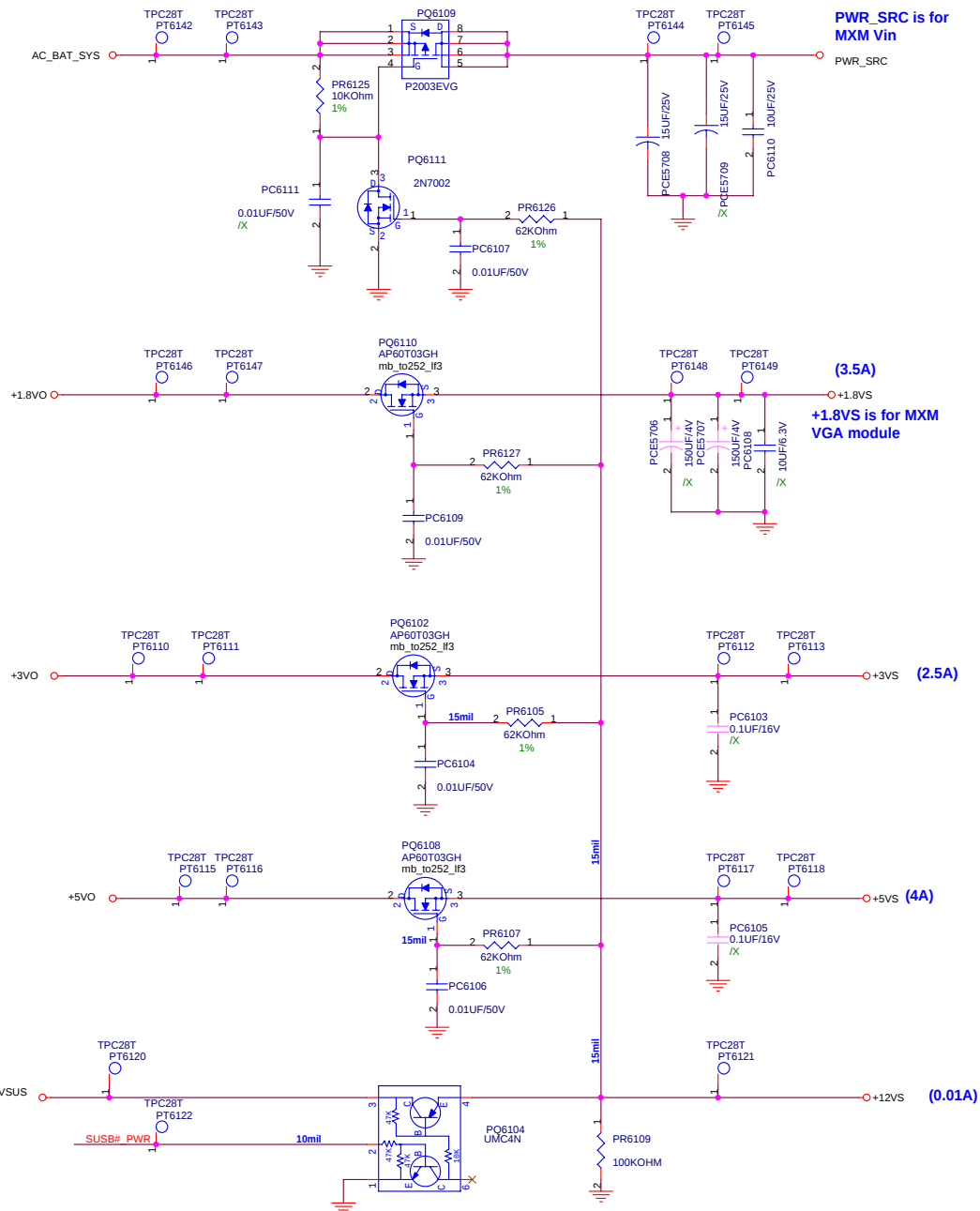


+2.5VS / 2A

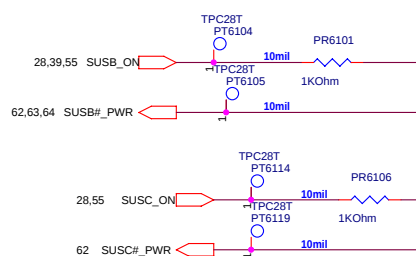
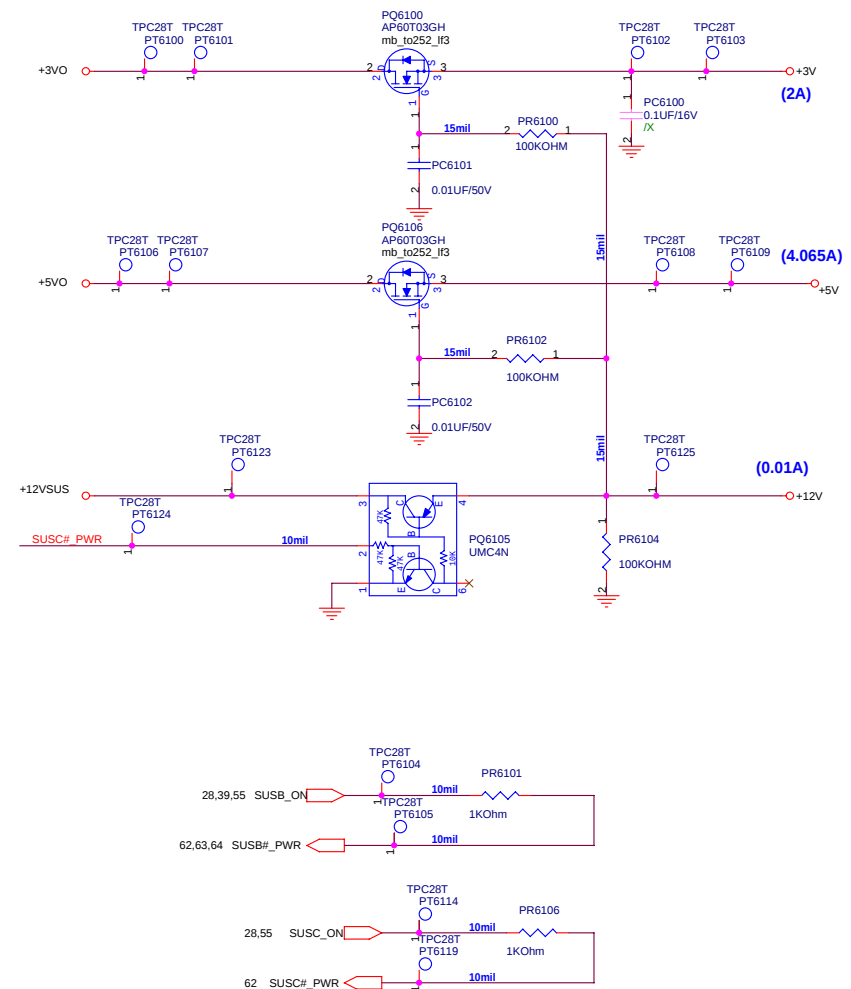


<Variant Name>

SUSB#_PWR POWER



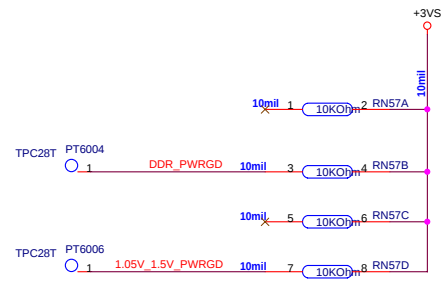
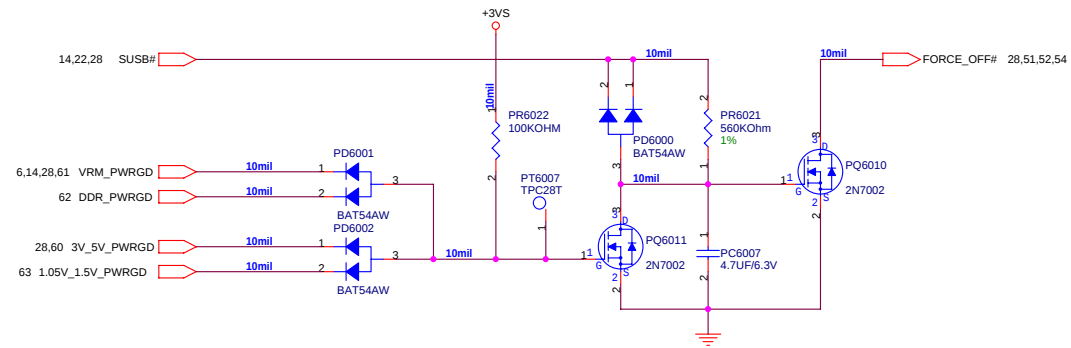
SUSC#_PWR POWER



<Variant Name>

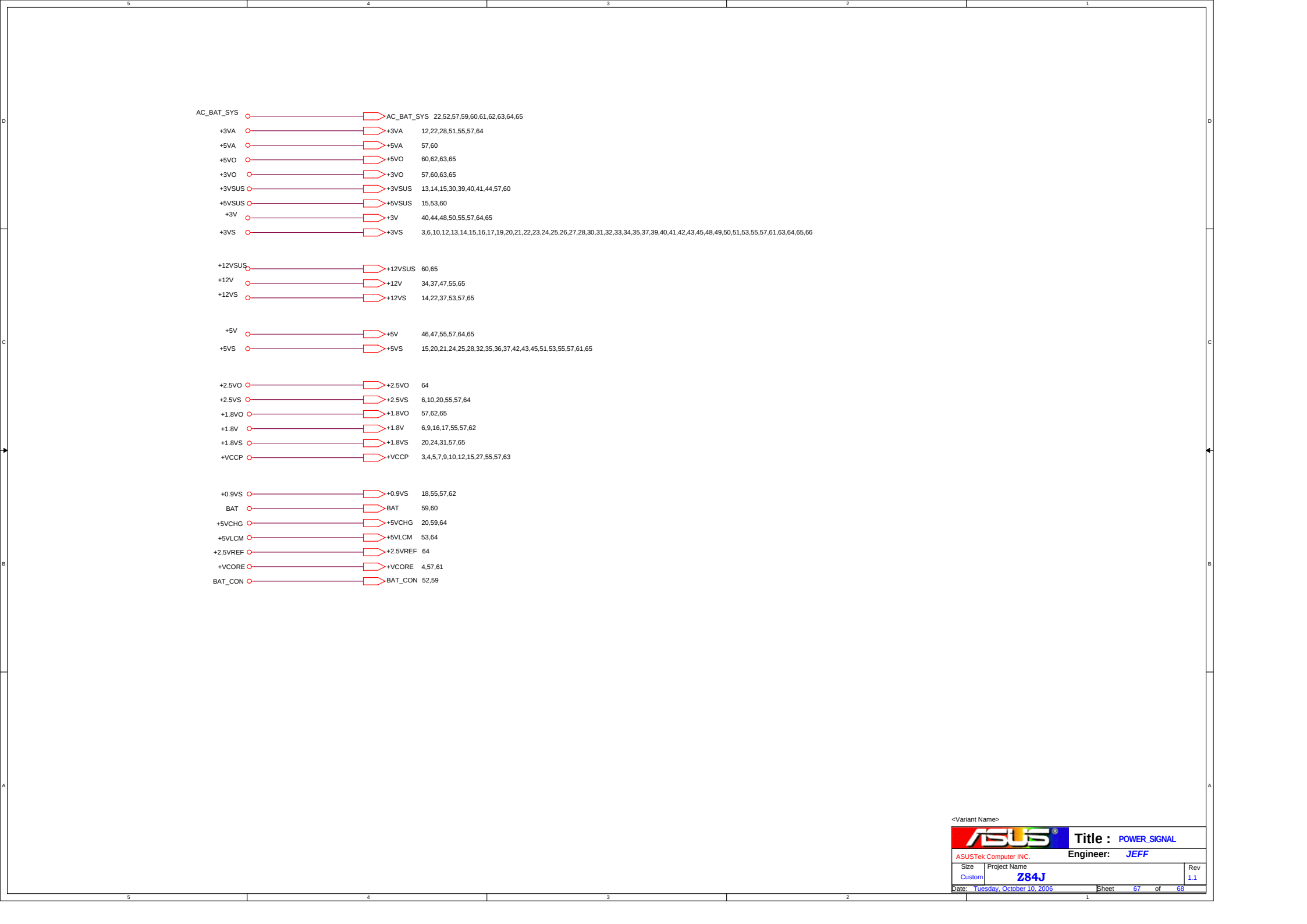
ASUS		Title : POWER_LOAD SWITCH	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date:	Tuesday, October 10, 2006	Sheet	65 of 68

Power Good Detector



<Variant Name>

ASUS		Title : POWER_PROTECT	
ASUSTek Computer INC.		Engineer:	
Size	Project Name	Rev	
Custom	Z84J	1.1	
Date:	Tuesday, October 10, 2006	Sheet	66 of 68



Rev	Date	Description
1.0	04/10/06	1. Initial release.(From Z84F)
1.1	08/08/06	1. Change Audio Codec from AD1988B to ALC888(Page 35) 2. Change AJ2, AJ3 to Azalia type 3. Correct RN2 Connection 4. Add PR5312, PR5313 to fix NANYA DIMM S3 fail issue(Page 62) 5. MXM_PWROK : remove R80(Page 19, Page 28) 6. PR5308 change to 1.2K 1% 0603(Page 62) 7. Change Inverter Connector type (12pin) & Pin define CON7(Page 22) 8. Remove : AR1, AR6, AR7, AR8, AR13, AR14, AR15, AR18, AR19, AR21, AR22, AR34, AC1, AC2, AC4, AC5, AC7, AC8, AC11, AC13, AC23, AC25, AC26, AC27, AU2, AQ6, AQ7, AQ9, AQ12 Add : AC81-AC85, AR71, ARN3, AD3, AD4, AL16
	08/10/06	1. Remove T100-T118(Page 41) 2. Add PU5901, PC5905, PC5906 for CIR Power(Page 64) 3. PR5308 change to 150K 1% 0603, PC5312 change to 1500PF 0603(Page 62) 4. Add PR5060, PR5061(Page 61) 5. PR5114 change to 27K 1% 0603(Page 60) 6. PR5722 change to 22K 1% 0603, Stuff PR5721(Page 59) 7. R77 change to 4.7K, Pull to +5VCHG for AC_OK(Page 20) 8. Change connection of L23, L24 9. Change CON18 P/N 10. Add D30, D31, D32, C175, C176, R136(Page 28)
	08/11/06	1. Add Audio Amp. AU100, AR100-AR103, AC100-AC107, non-stuff AC41(Page 36) 2. AC82 change to 1uF 0603, Add AU2, AC23, AC86, AC87, AR72, AR73, AJP1, AJP2, Remove AC12 3. Change MXM SMBus connection to EC, SMB1_CLK, SMB1_DAT(Page 28, Page19)
1.2	08/29/06	1. Change eSATA Controller from Sil3531 to JMB360(Page 31)

Rev	Date	Description