

Rev.1.1

CLOCK GEN.
ICS951417
17

Thermal Sensor
(MAX6657)
4

Yonah
Socket M
2,3 478 uFCPGA

HOST BUS
AGTL+
1.05V, 133/166MHZ

RC410ME
5,6,7,8 707 FCBGA

LVDS & INV
18/32

CRT
19

USB X1

USB X2
31

USB WLAN
32

CDROM
30

HDD
30

IDE BUS

SB450
564 BGA
10,11,12,13,14

A-link(X2)

USB2.0

PCI_BUS

CARDBUS
RICOH
R5C841
27

LAN
RTL8100CL
25/26

CARDBUS
1 SLOT
VCCA, VCCB
VPPA, VPPB 28

3 IN 1
CARD READER
29

DUAL DDR2 SO-DIMM
15,16
DDR2 400/533/667
Single channel

LPC, 33MHZ

Super I/O
47N217
24

IT8510E
22

TP

Printer

PortBAR
24

USB

INTERNAL KEYBOARD

ISA ROM
23

ALC660
20

MDC
26

AMP
21

JACK & MIC
26/20

CLOCK GEN.
ICS951417
17

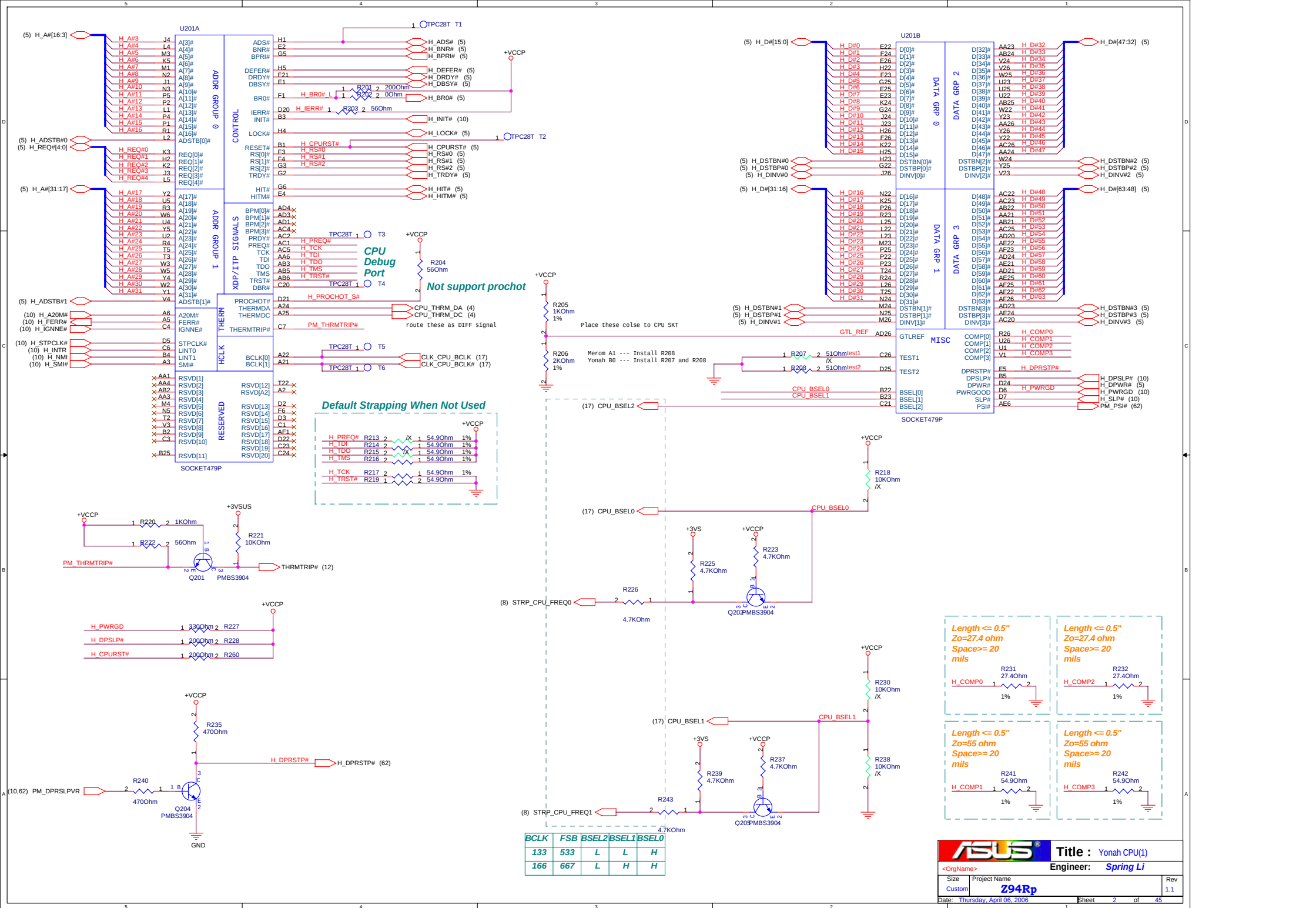
Thermal Sensor
(MAX6657)
4

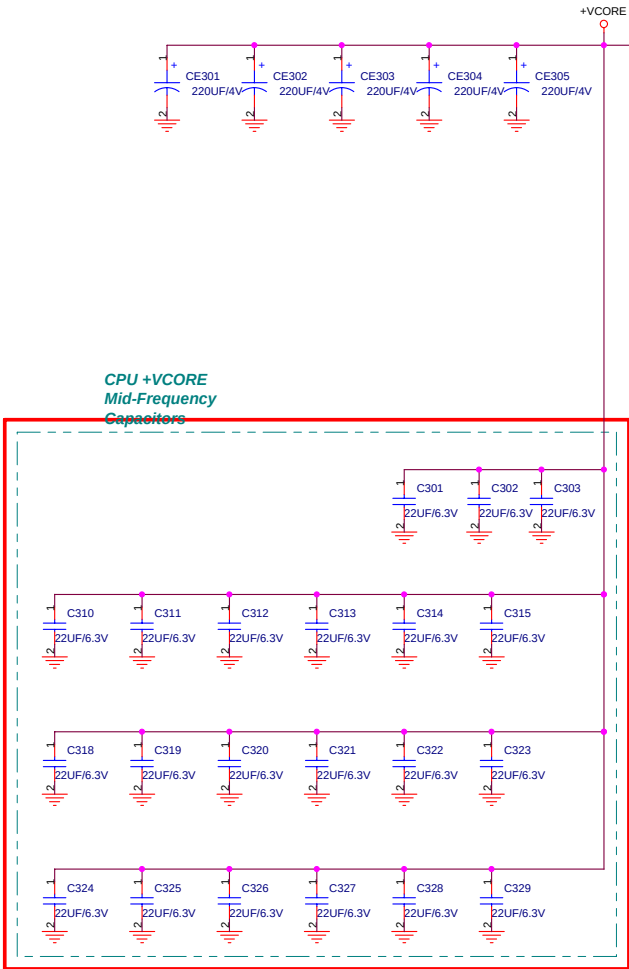
CRT
19

LAN

ASUS
ASUS-HD Server

Title : BLOCK DIAGRAM
Engineer: Spring Li

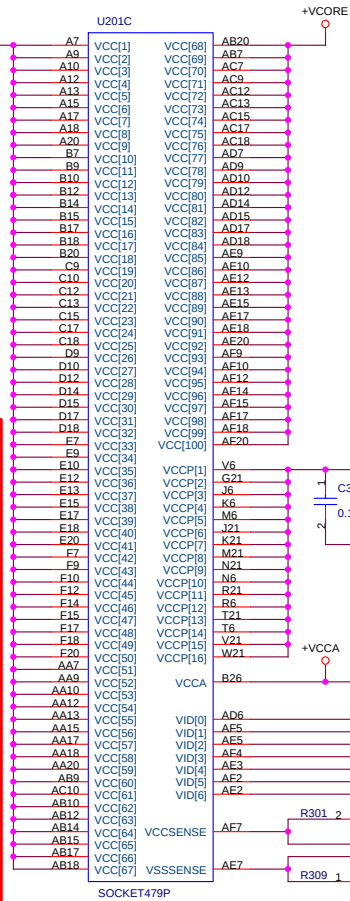




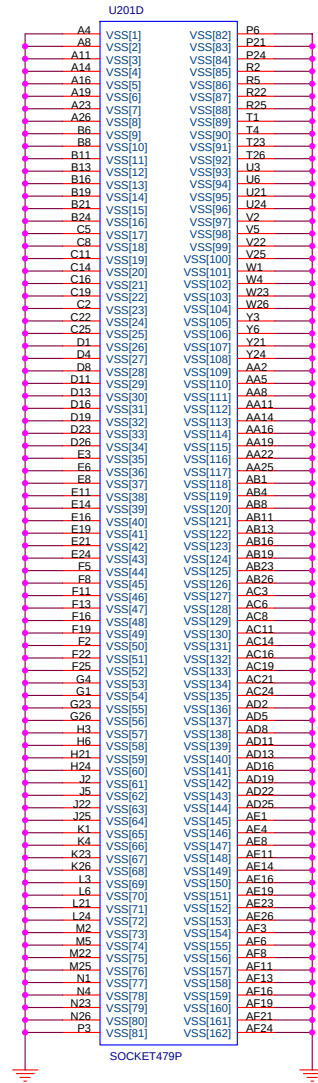
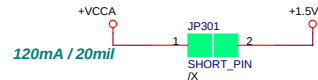
+VCCORE Low-Freq Capacitor
Intel: 330UF *6
ATI: 330UF *6
R1F: 330UF *4
A7J: 330UF *5

+VCCORE Mid-Frequency Capacitor
Intel: 22UF *32
ATI: 10UF *26
R1F: 22UF *16
A7J: 22UF*29 use 19
A6RF: 22UF*21 use 21

+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4
A7J: 220UF *1, 0.1UF *6
A6RF: 220UF *1, 0.1UF *6



Layout note : route VCCSENSE and VSSSENSE trace at 27.4 OHM with 25mil spacing mismatch and 18 mils trace on 7 mils spacing , please place the pull-up/down resistors within 1 inch of cpu

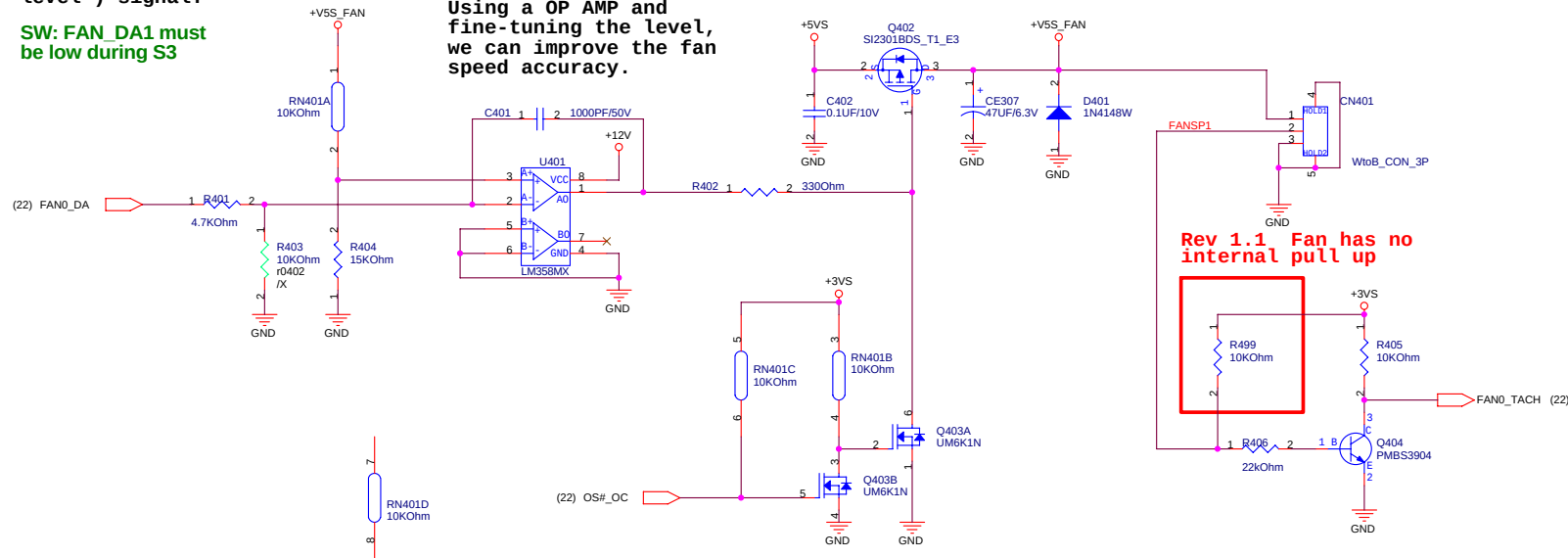


Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

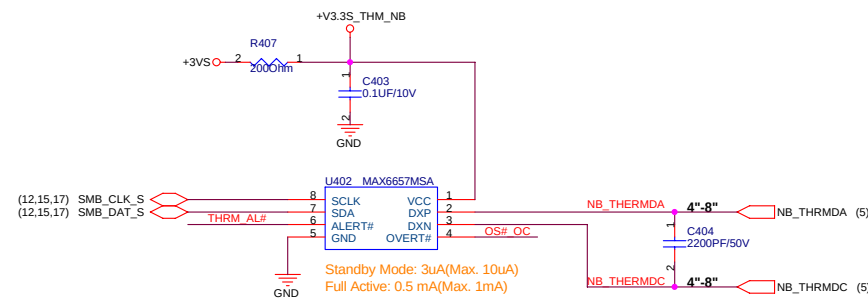


Route H_THERMDA and H_THERMDC on the same layer

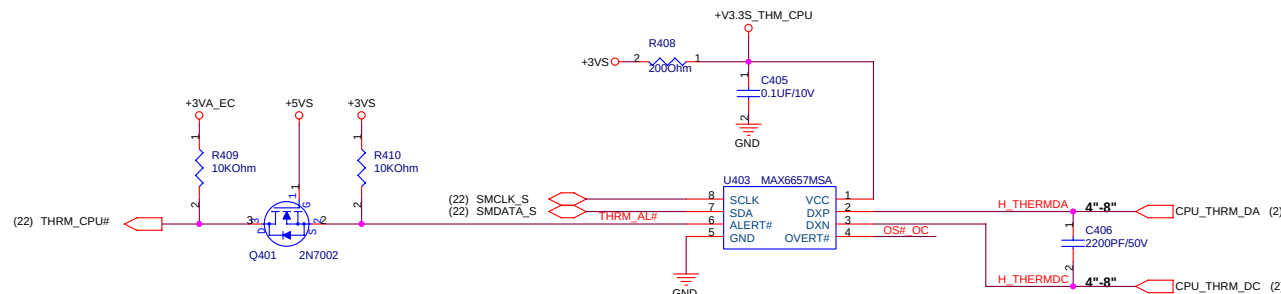
-----OTHER SIGNALS
12 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
12 mils
-----OTHER SIGNALS

Avoid BPSB,Power

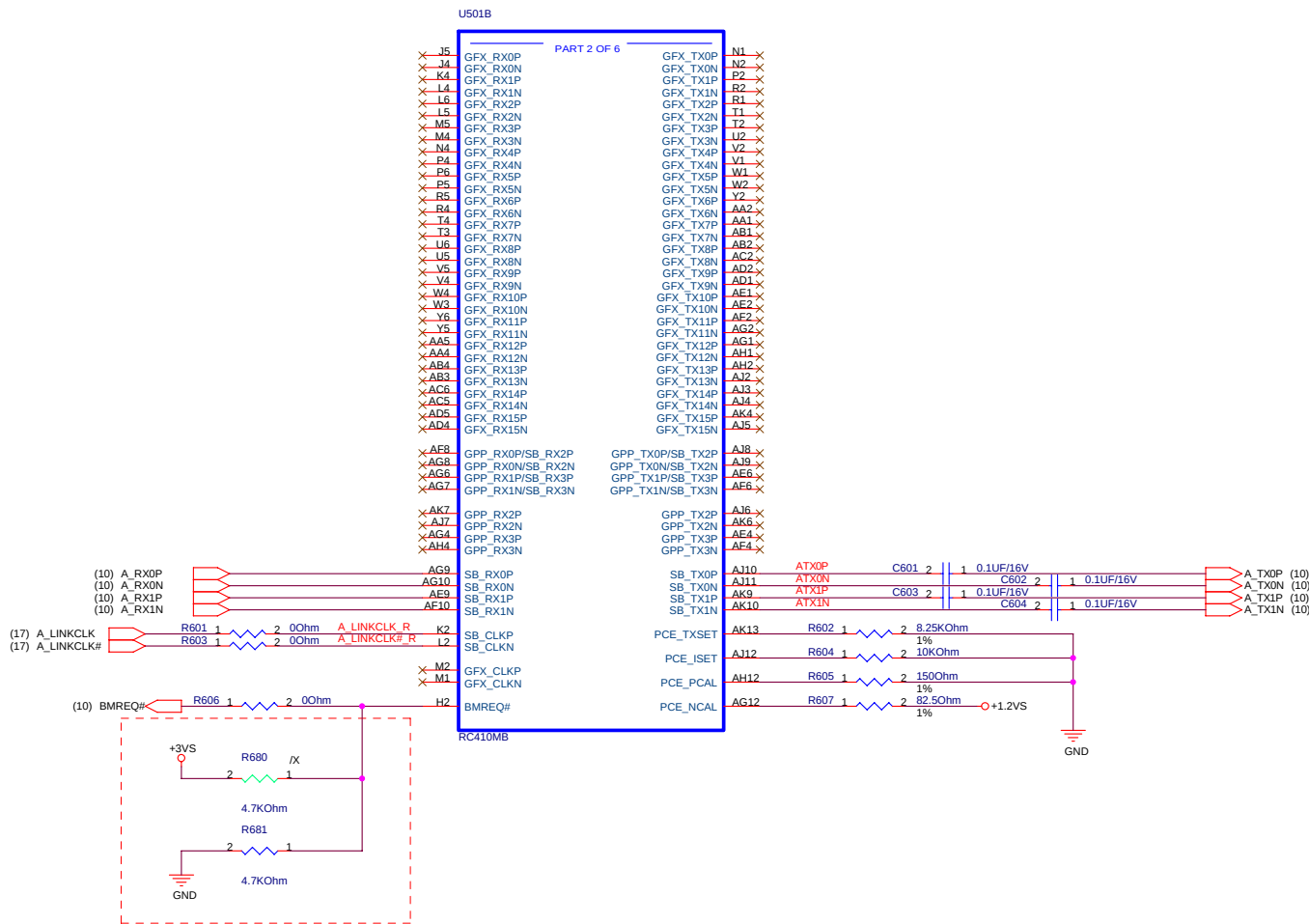
Rev 1.1 Fan has no internal pull up

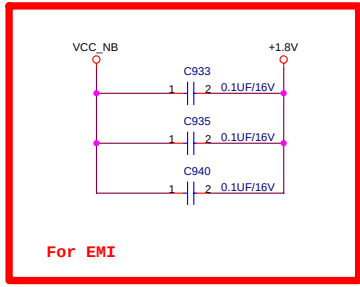
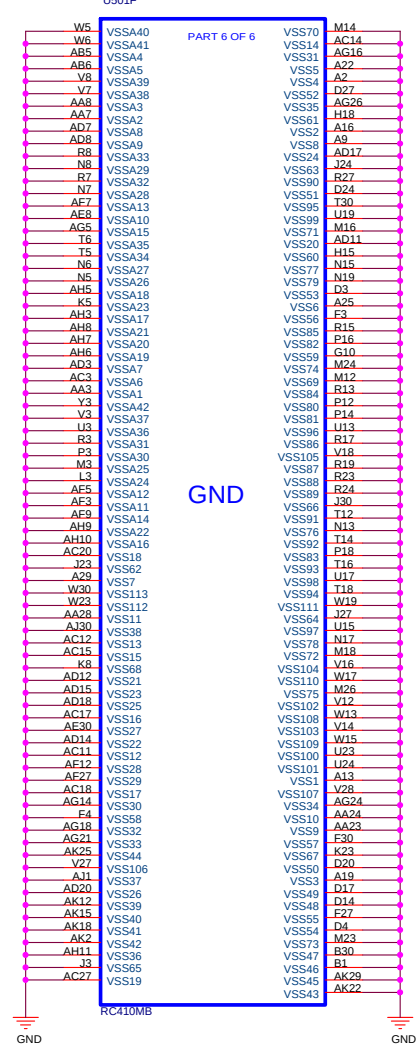
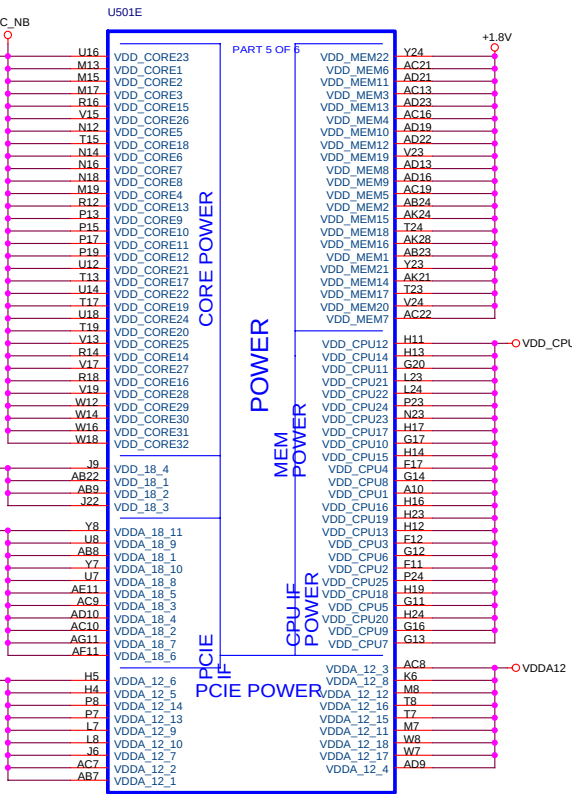
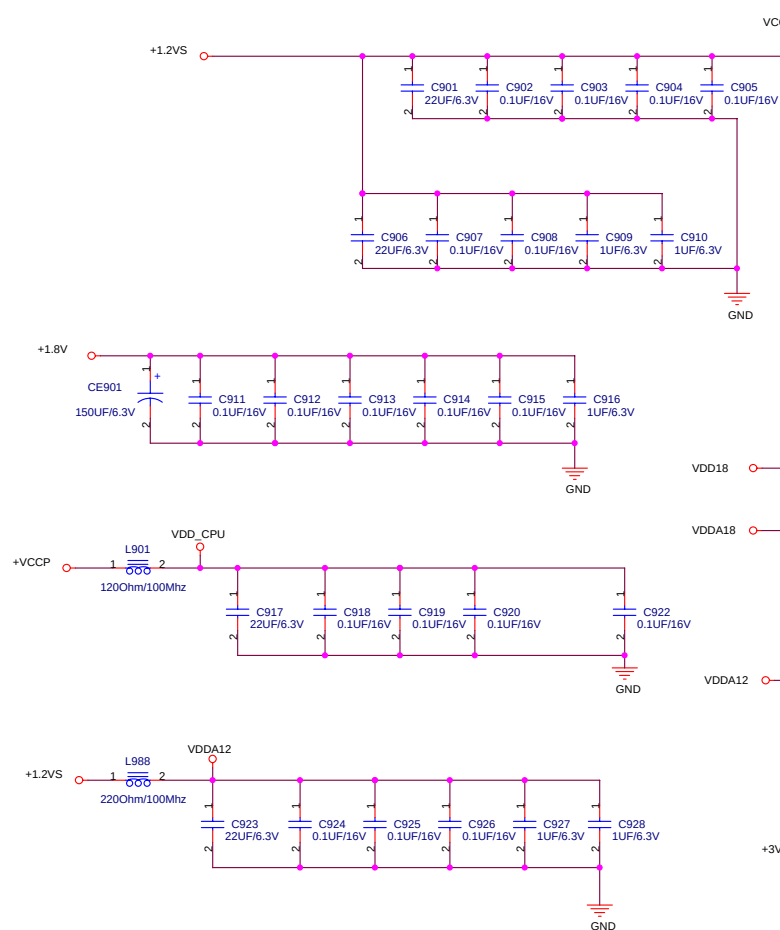


NB Detect

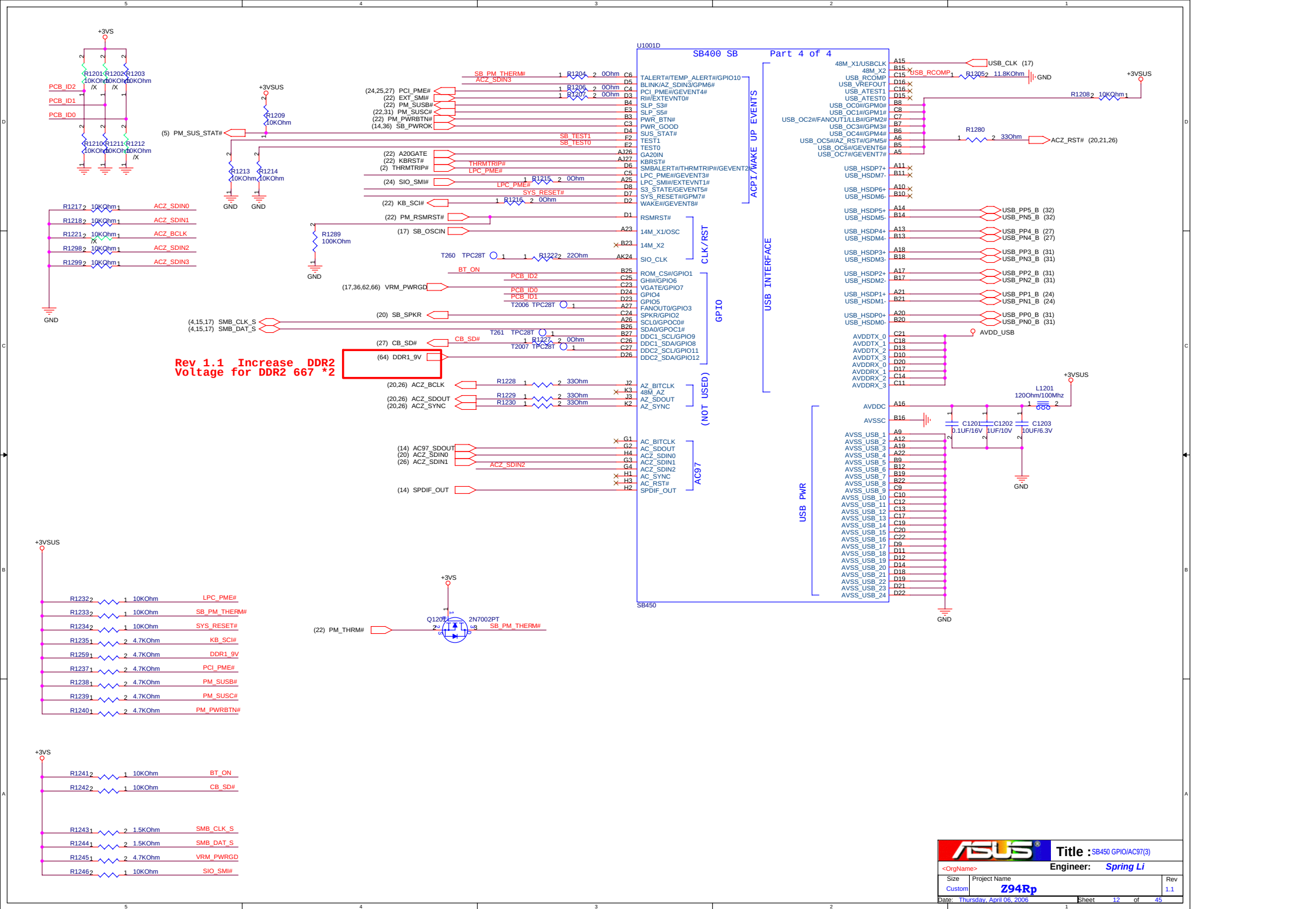


CPU Detect

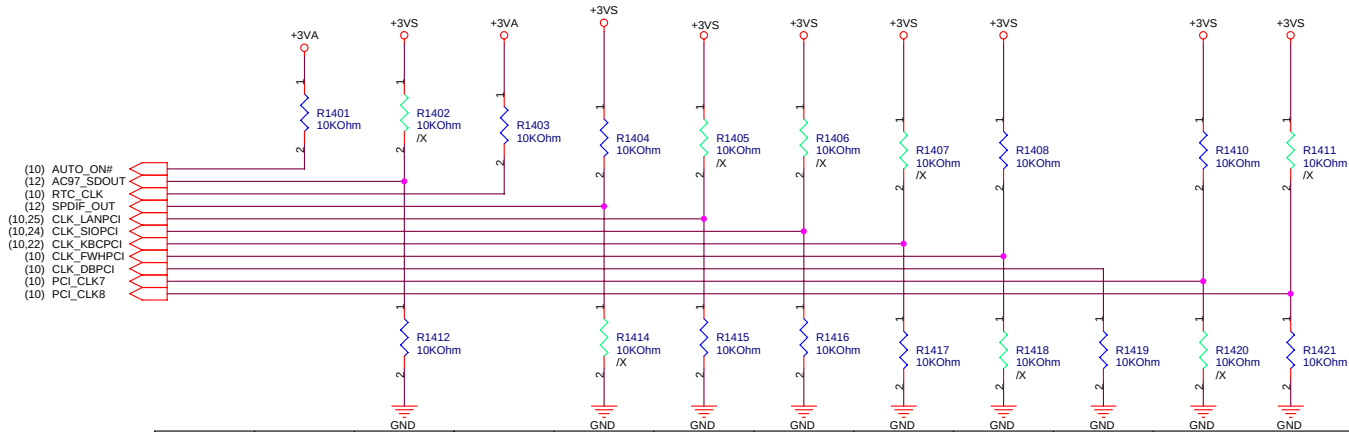








REQUIRED STRAPS



	AUTO_ON#	AC_SDOOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz		USB PHY PWRDOWN DISABLE	USE USB PLL		CPU I/F = K8	ROM TYPE H,H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz	SEE NOTE1	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	SEE NOTE2	CPU I/F = P4	H,L = LPC ROM I LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM	

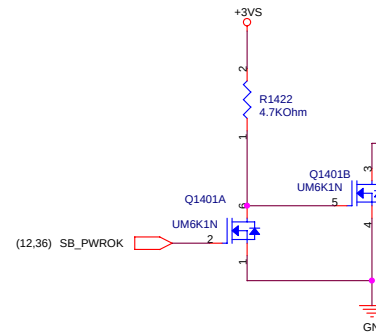
NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH

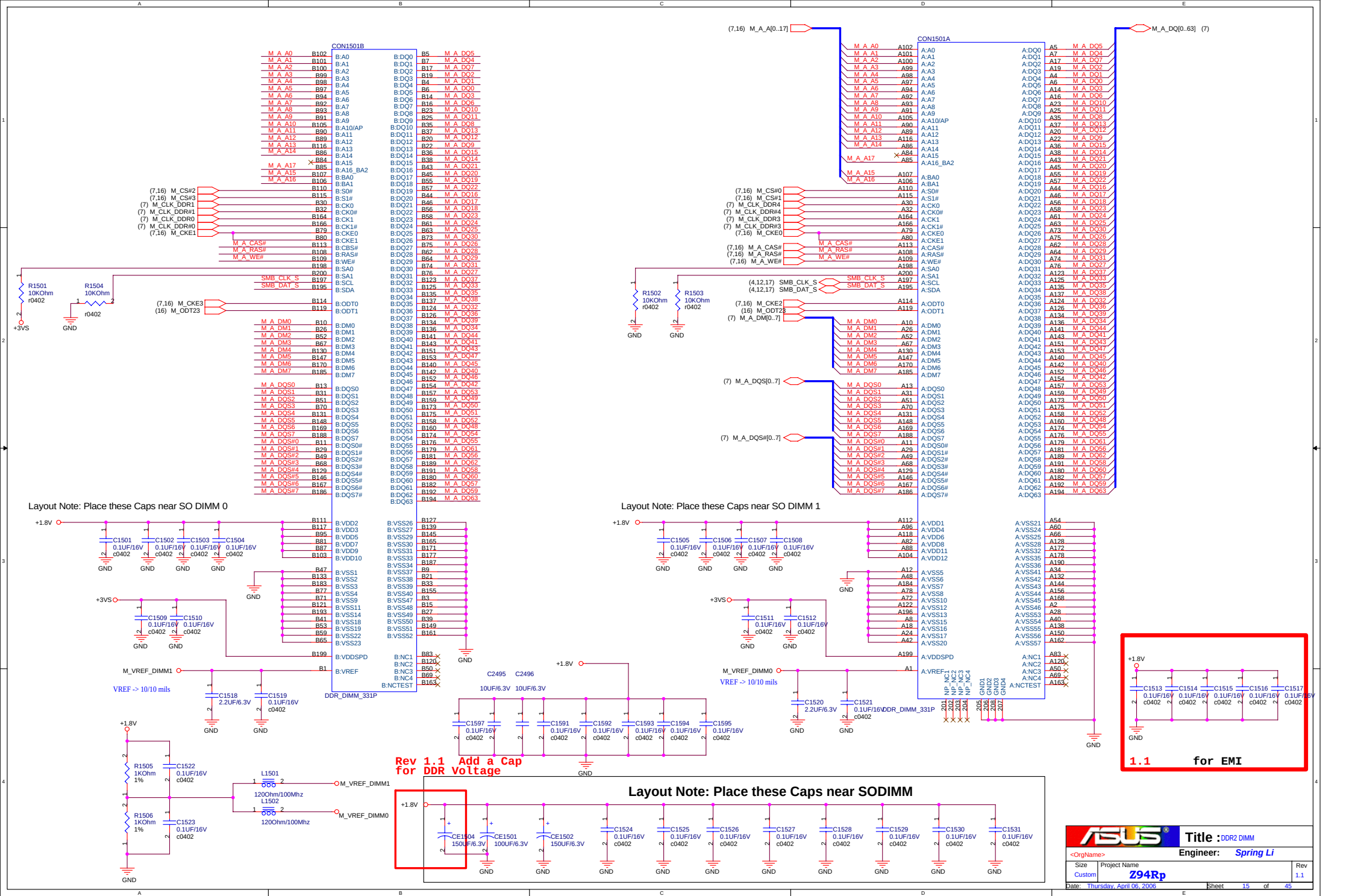


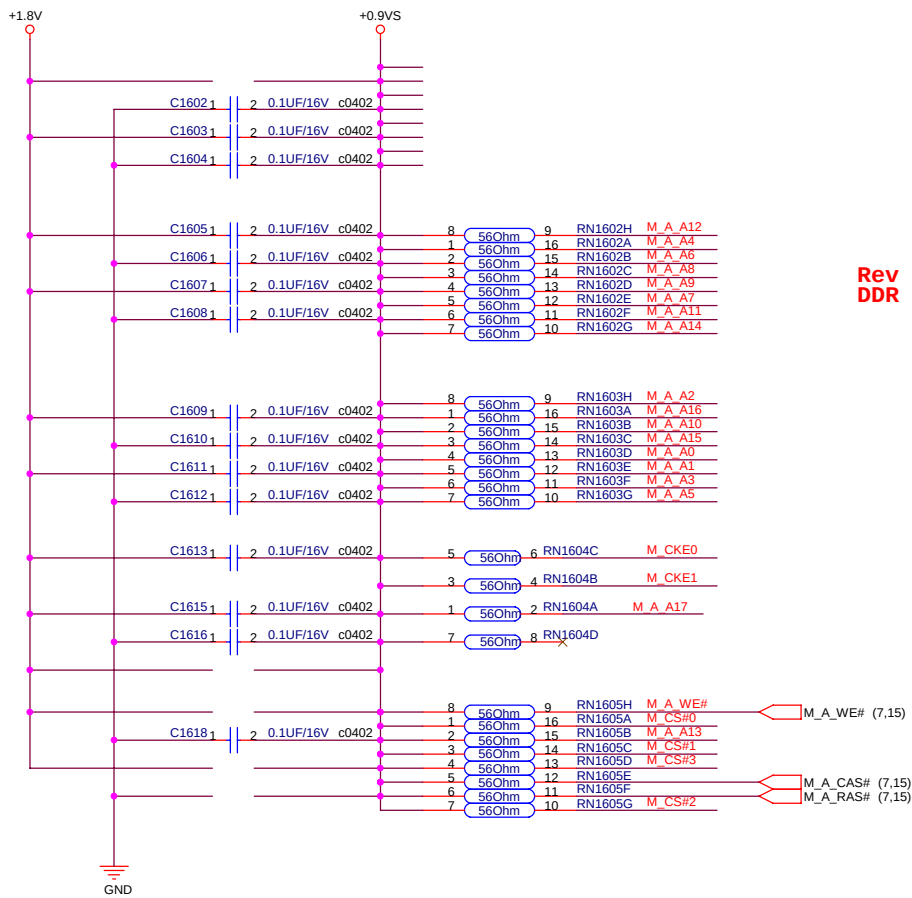
STRP_CPU_VOLTAGE: CPU VCC

0: MOBILE CPU
1: DESKTOP CPU

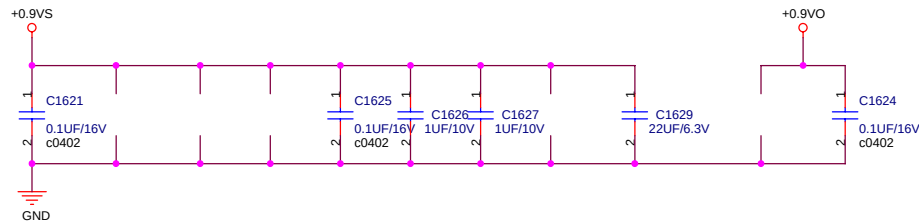
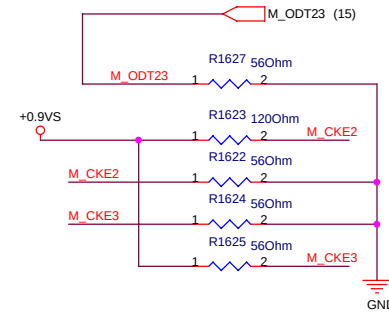
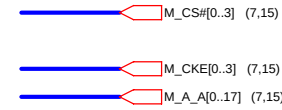
DEFAULT:0

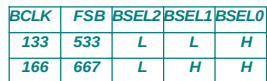
STRP_CPU_VOLTAGE (8)





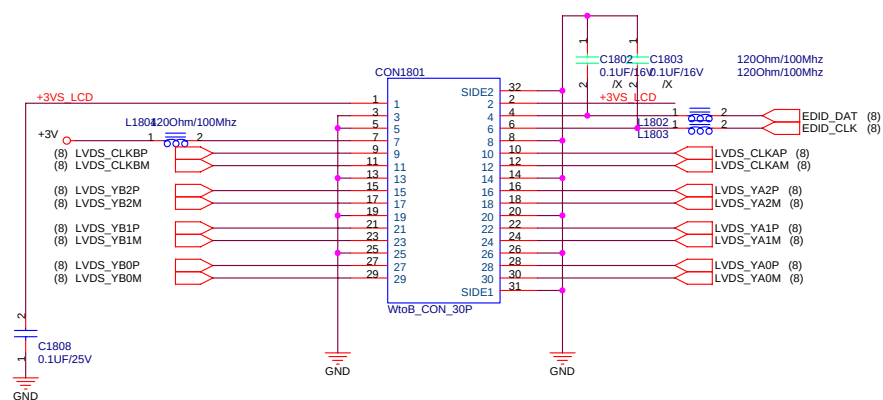
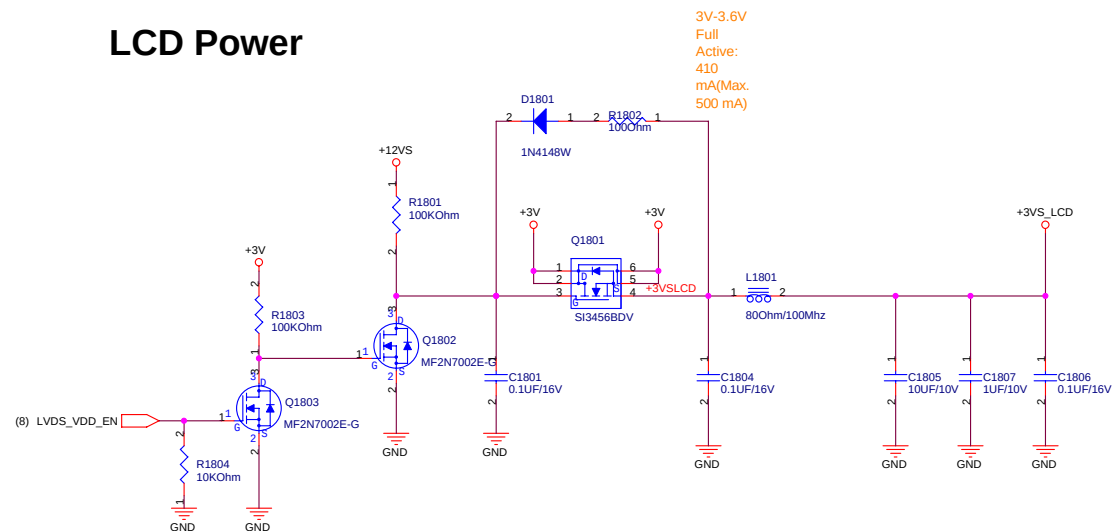
Rev 1.1 swap for
DDR Termination





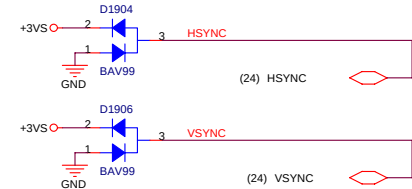
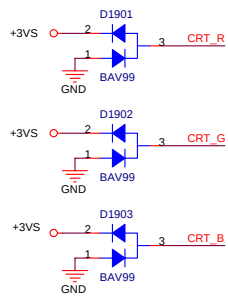
<i>BCLK</i>	<i>FSB</i>	<i>BSEL2</i>	<i>BSEL1</i>	<i>BSEL0</i>
133	533	<i>L</i>	<i>L</i>	<i>H</i>
166	667	<i>L</i>	<i>H</i>	<i>H</i>

LCD Power

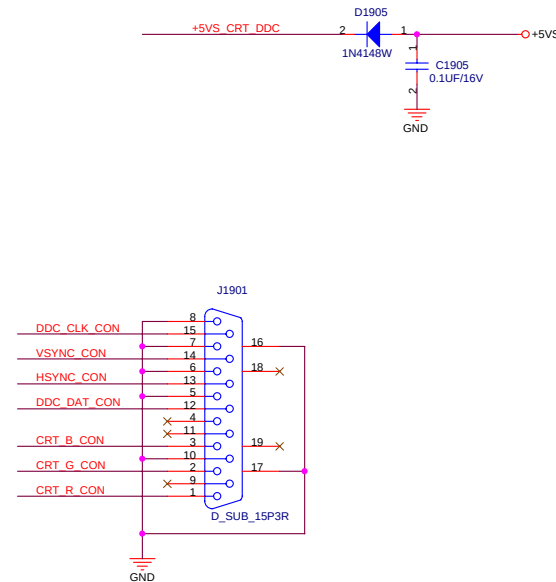
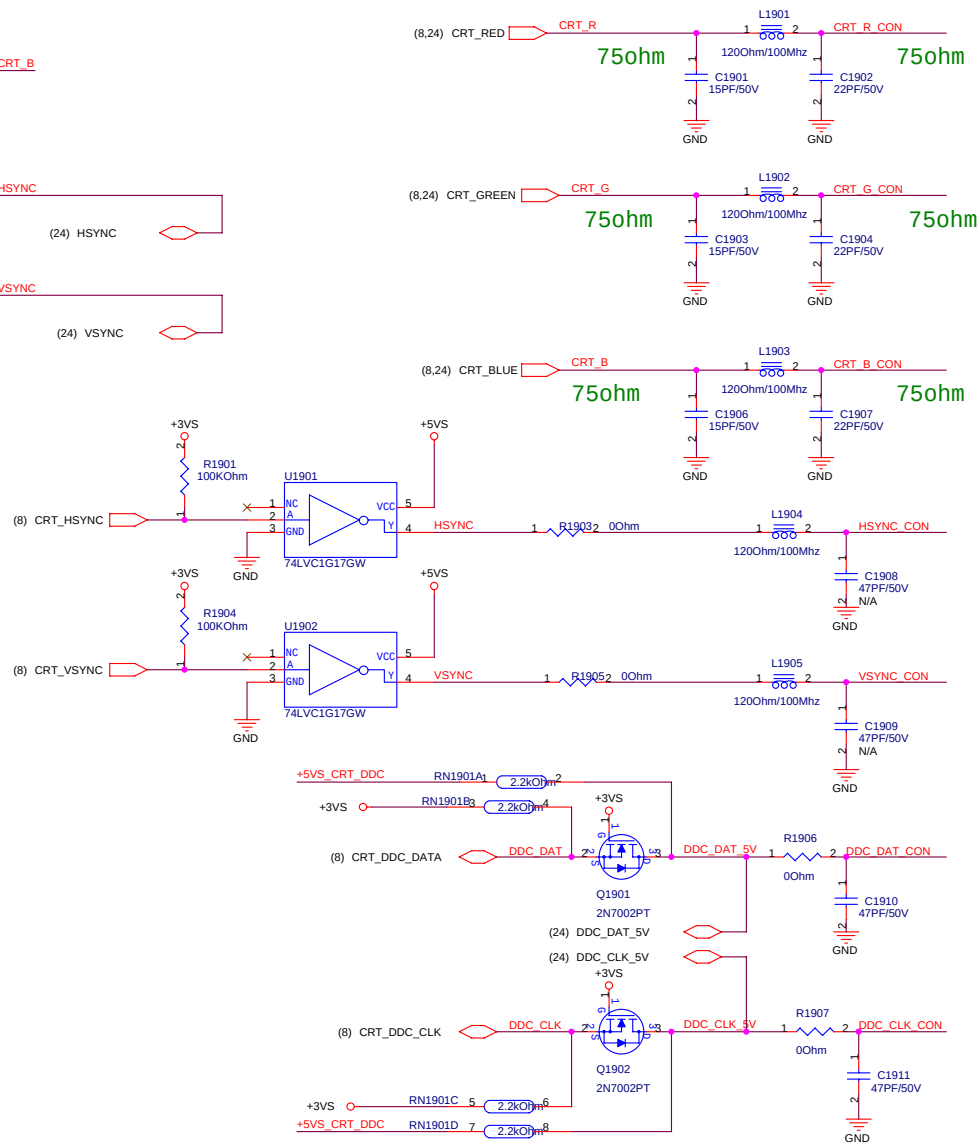


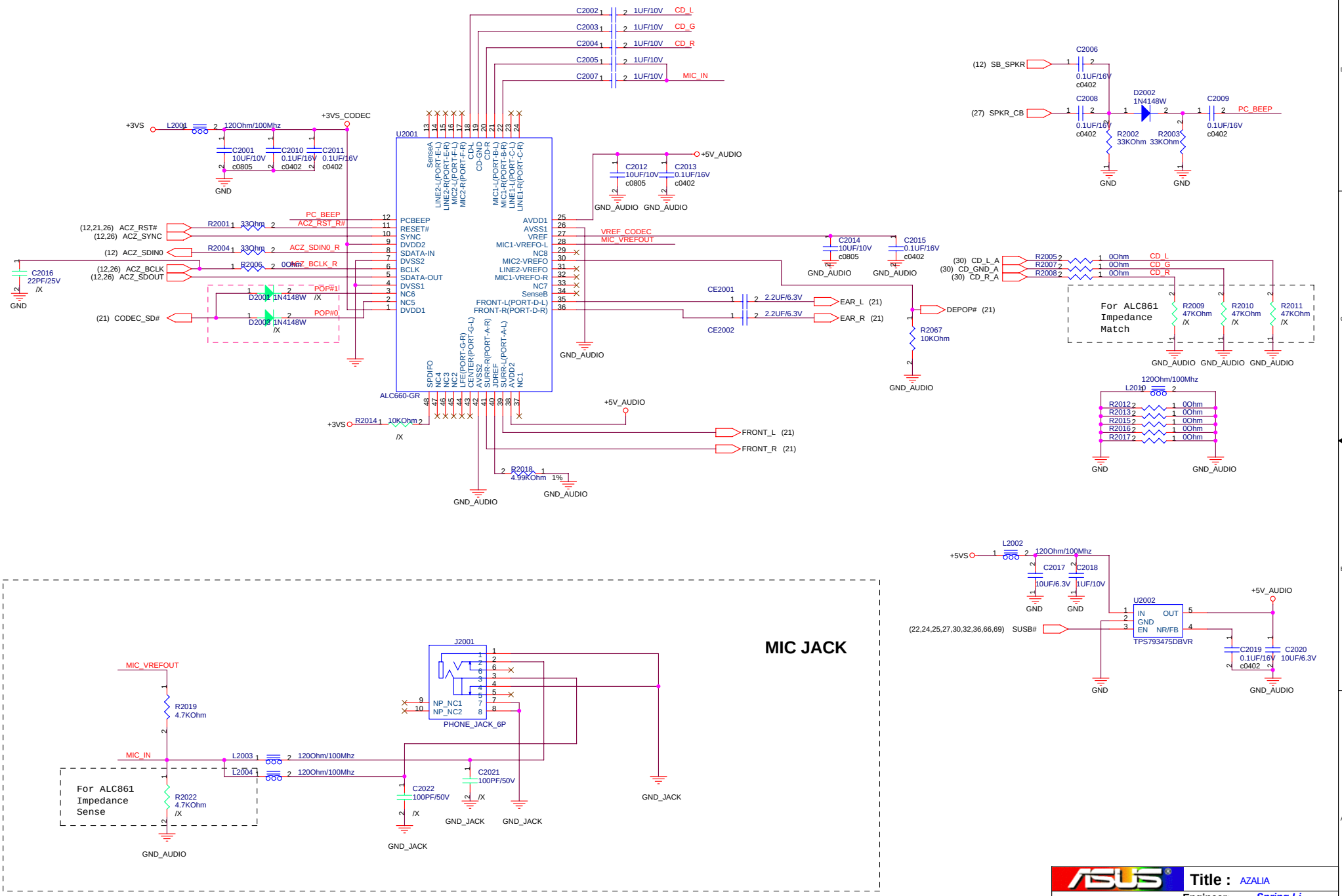
Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

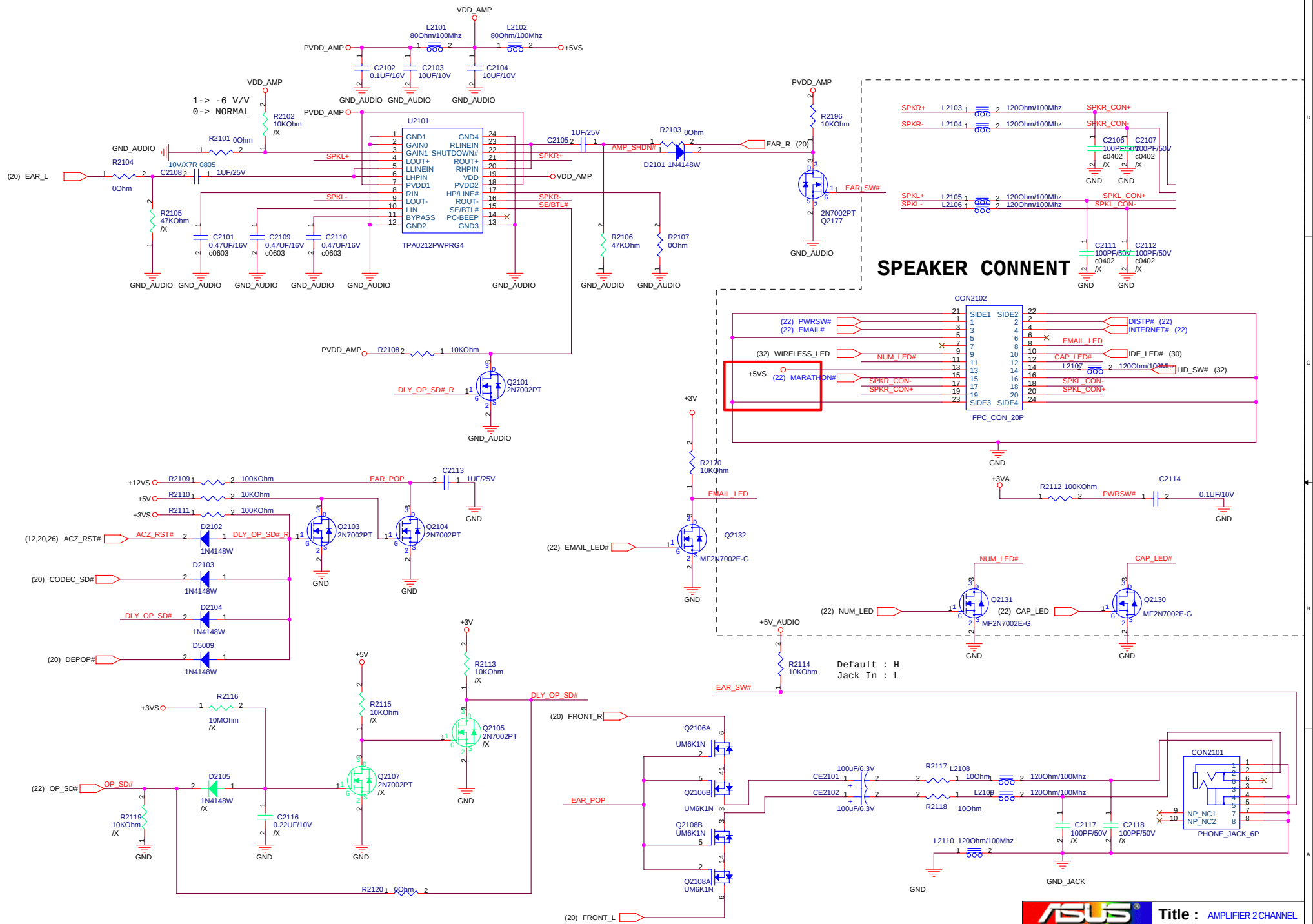
LCD LVDS Interface

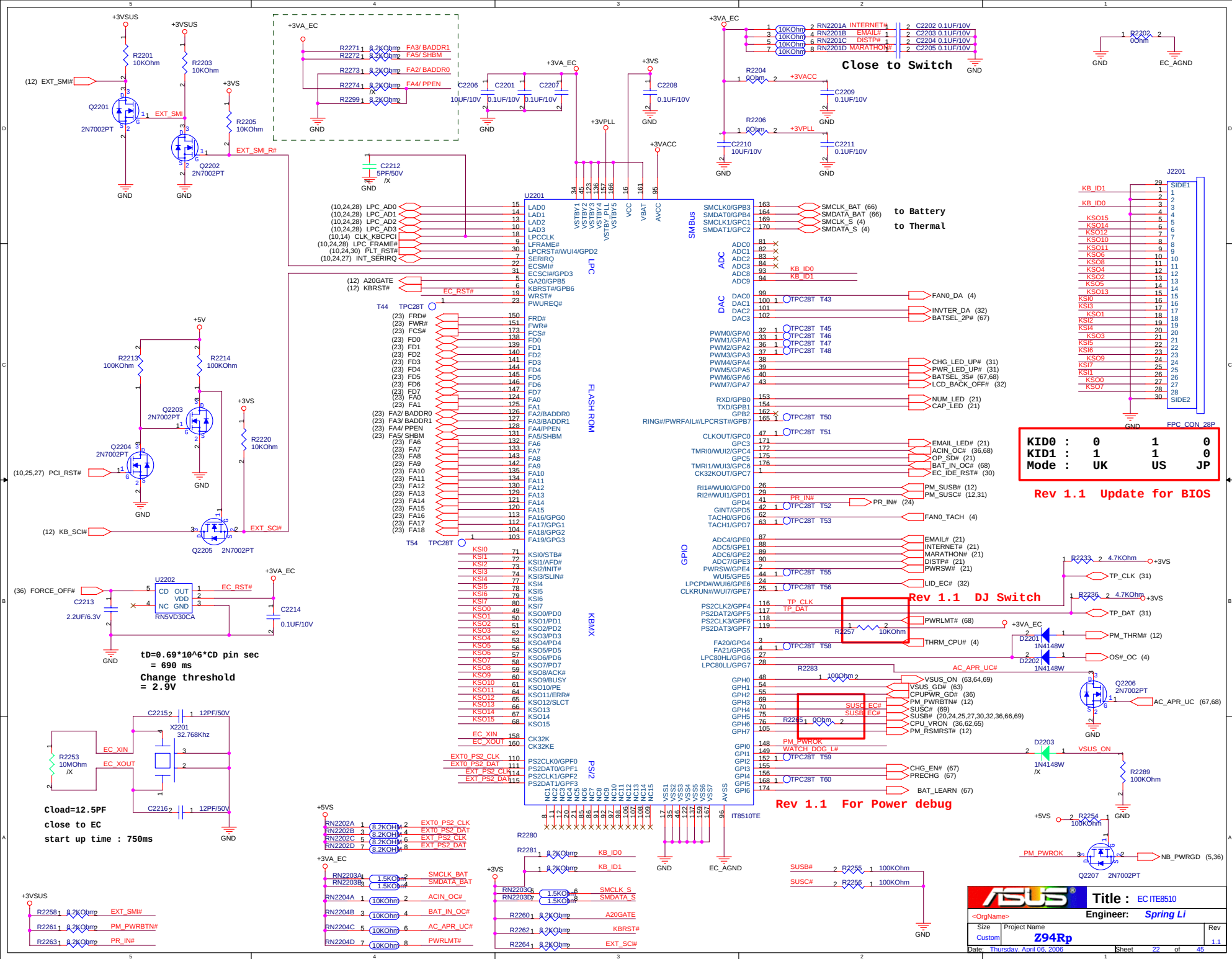


PLACE ESD
Diodes near
VGA port

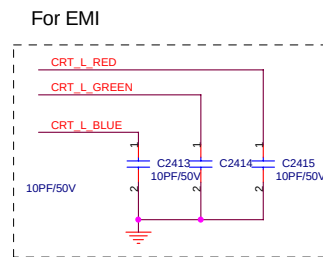
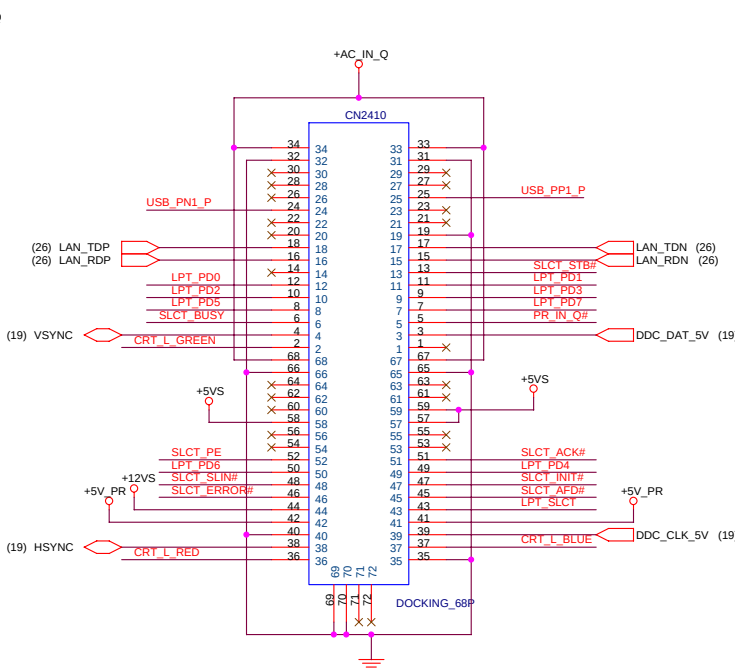
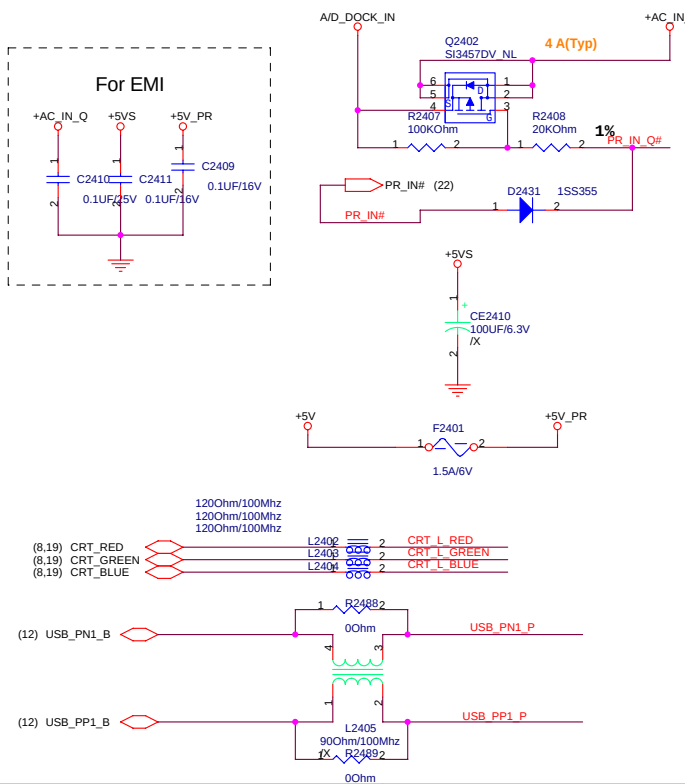
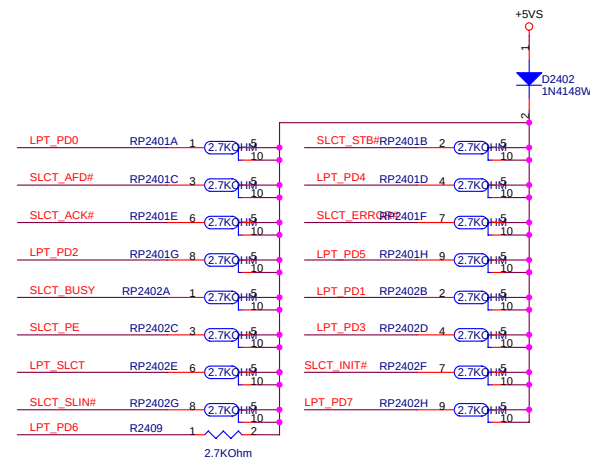
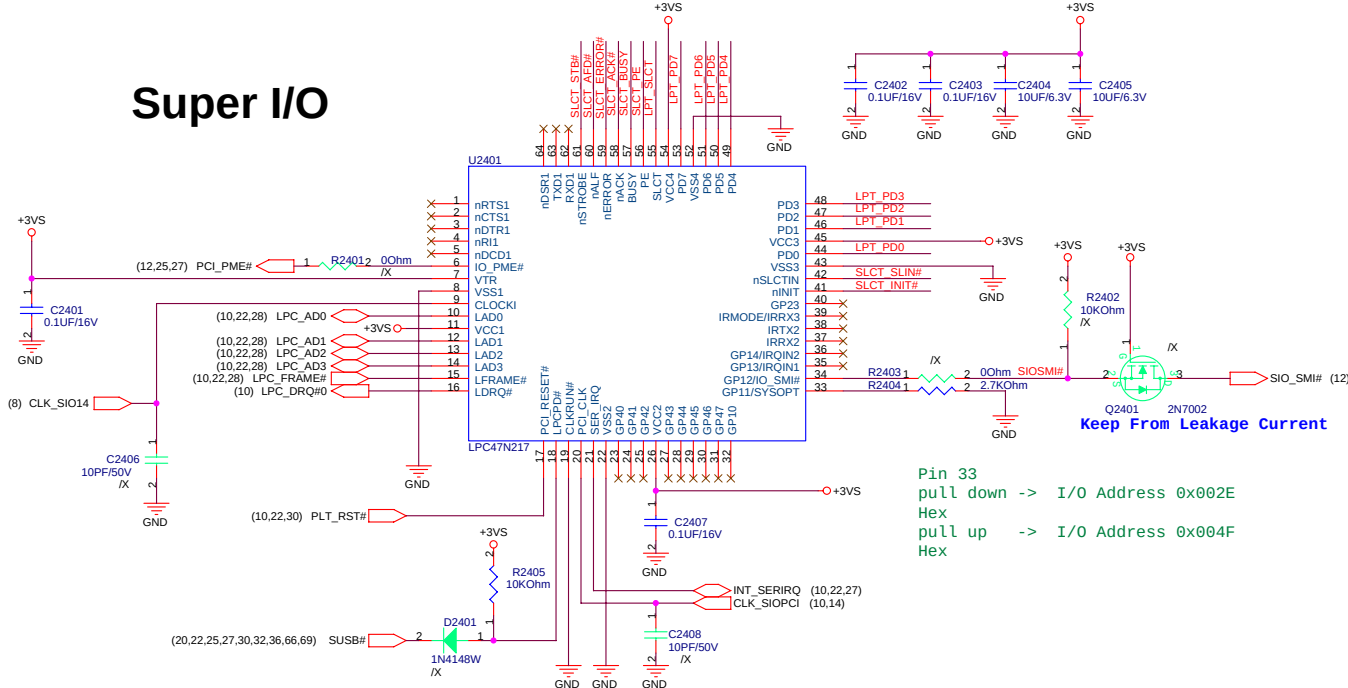


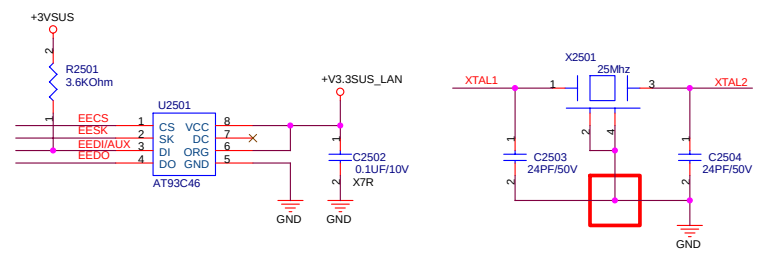




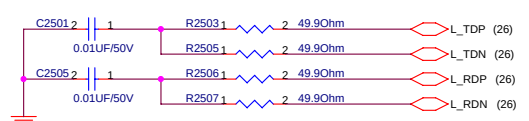


Super I/O

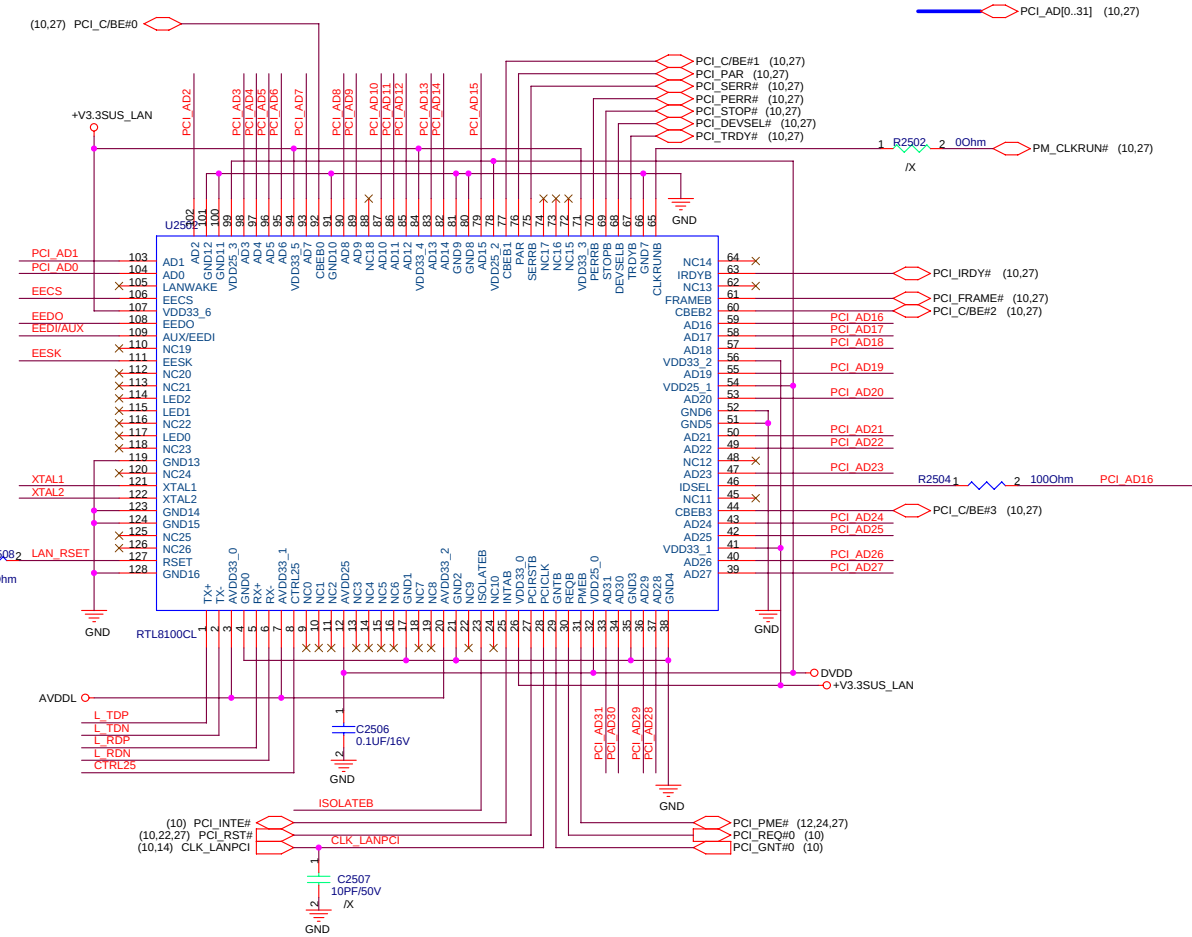
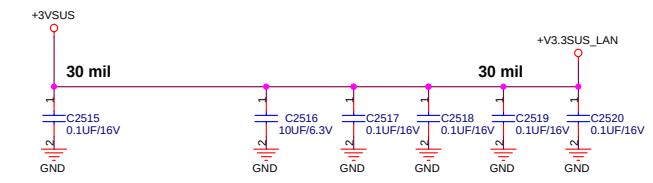
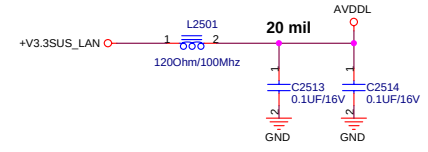
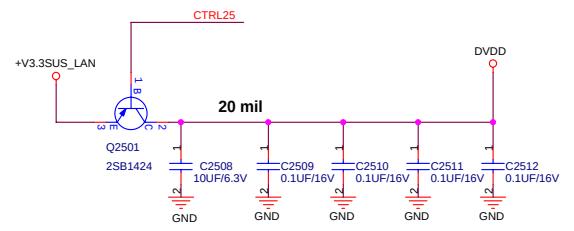
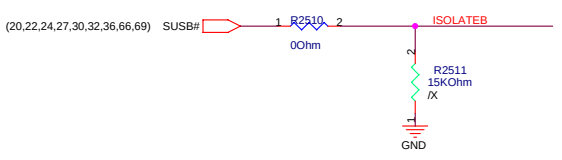


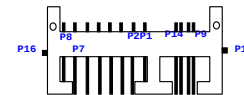
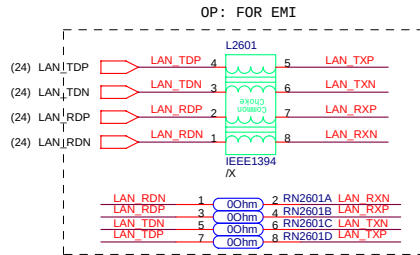
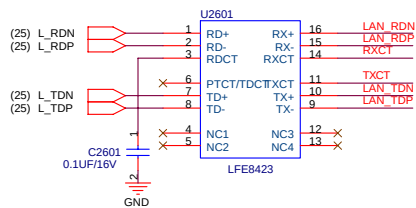


L_TDP, L_TDN termination resistors should be near chip



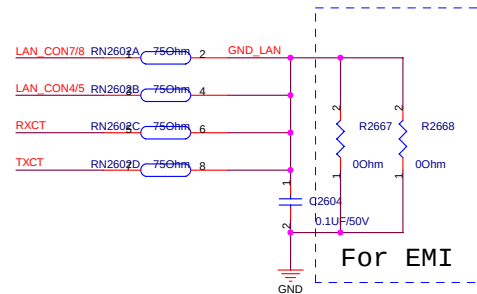
L_RDP, L_RDN termination resistors should be near transformer-U32



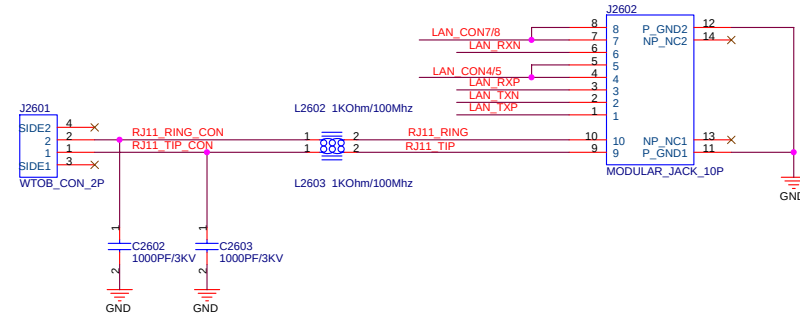


RJ 45 & RJ 11
BOTTOM VIEW

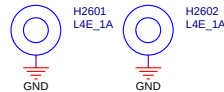
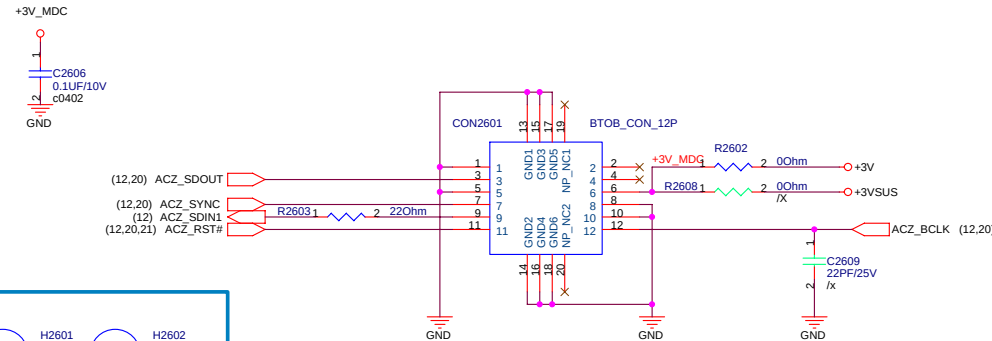
LAN PORT



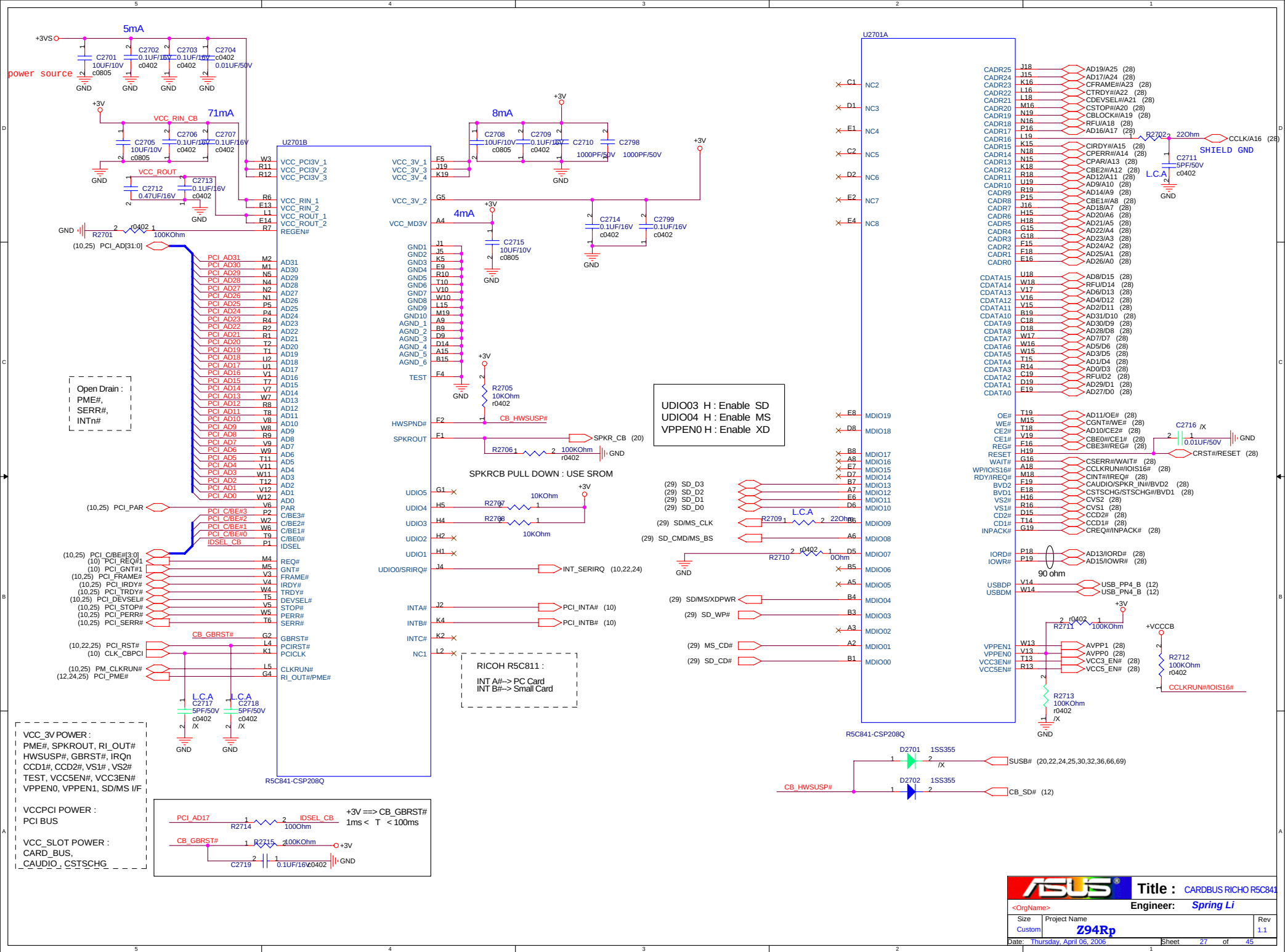
For EMI

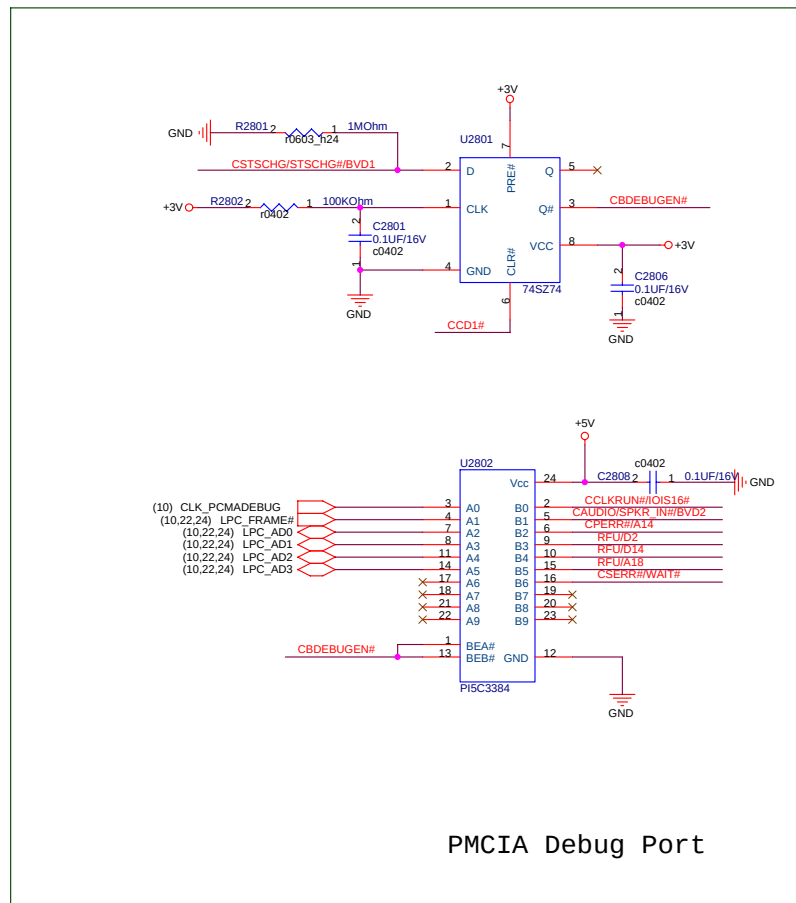


MDC

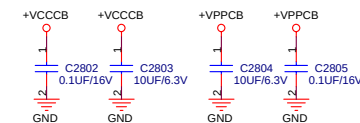
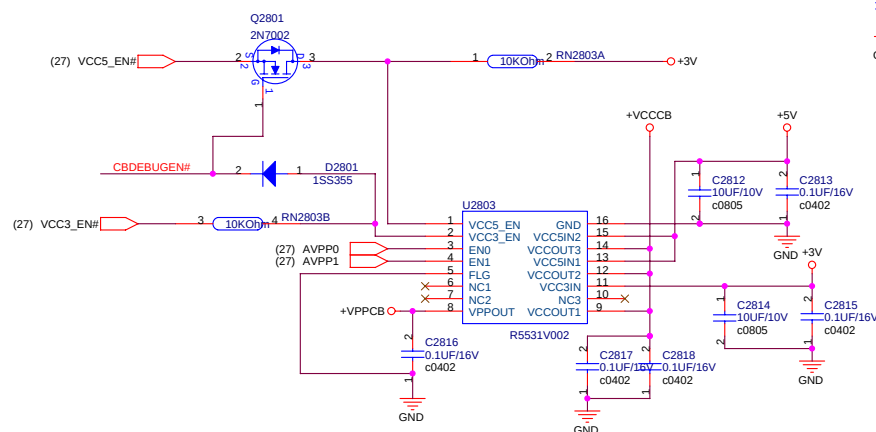


Must change to
13-N7510M270

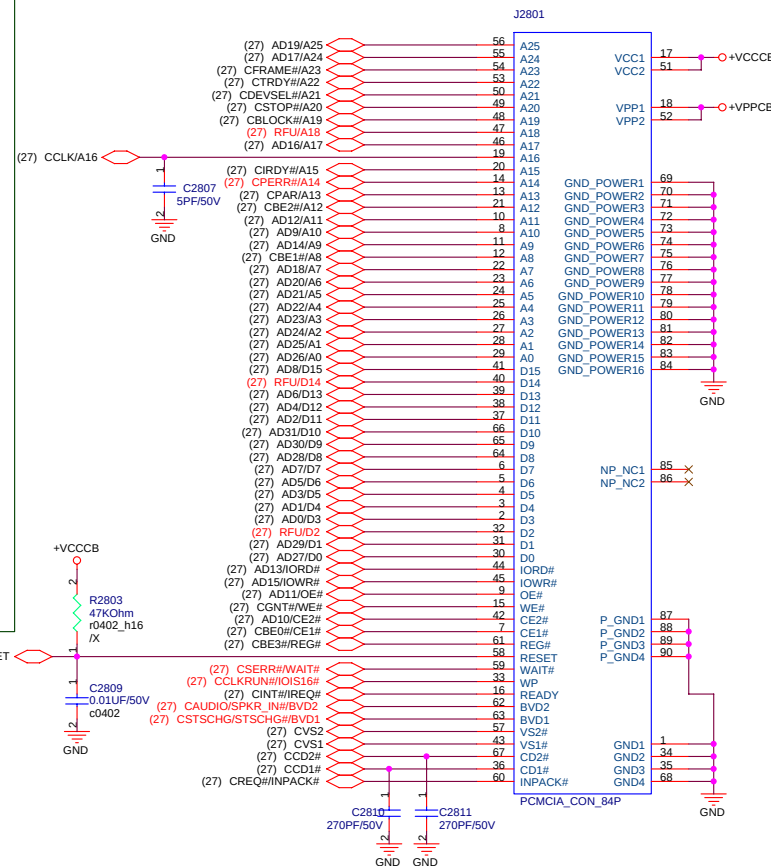




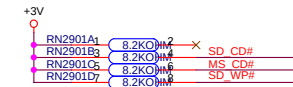
PMCIA Debug Port



PCMCIA Socket



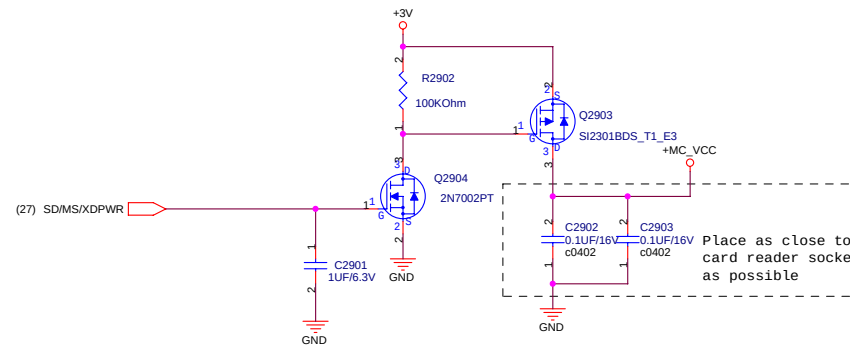
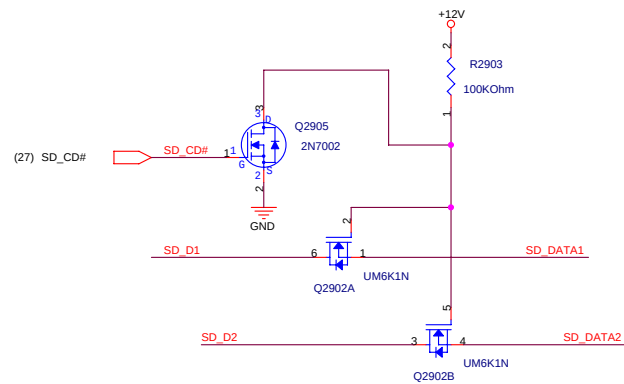
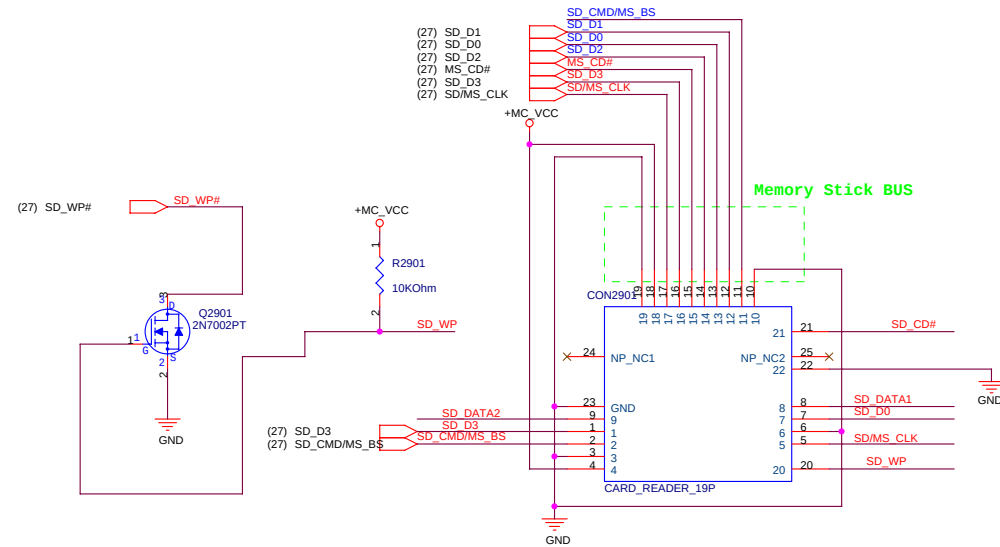
CCD1#	CCD2#
L	L
OTHER	16bit
	32bit

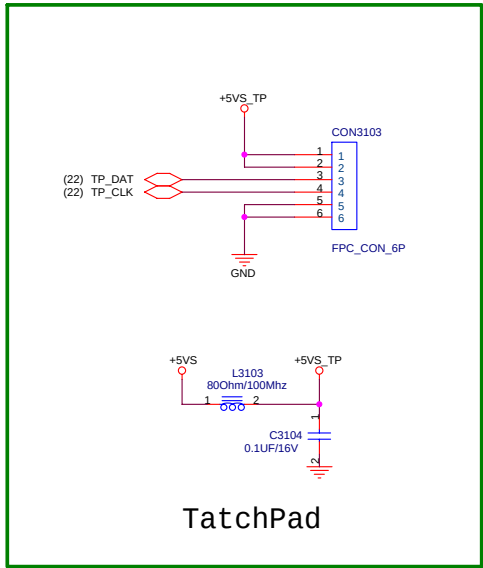
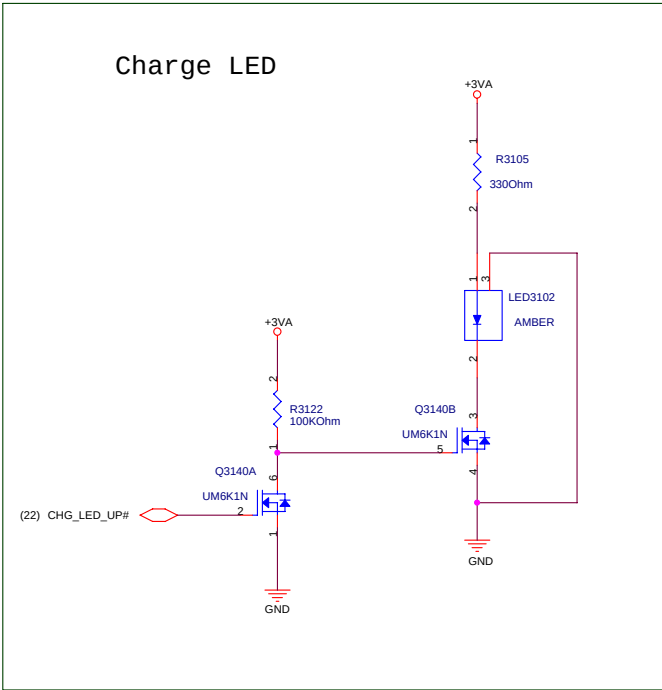
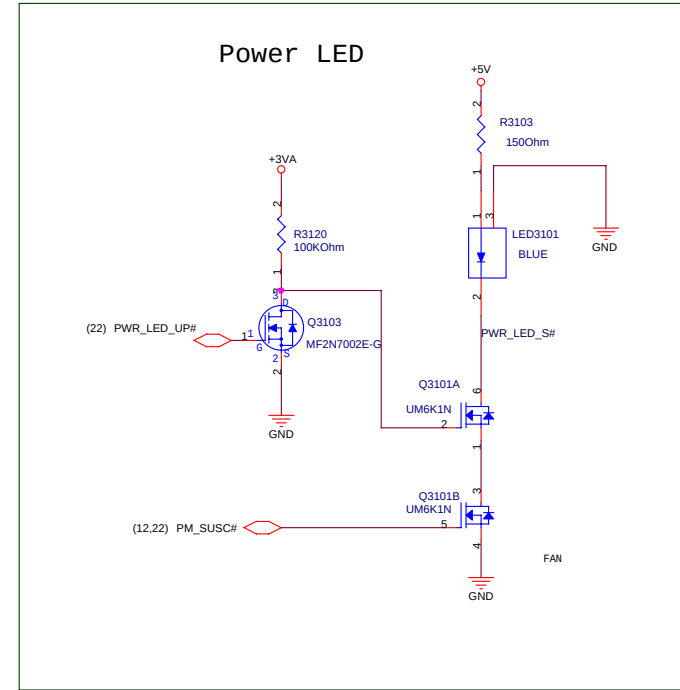
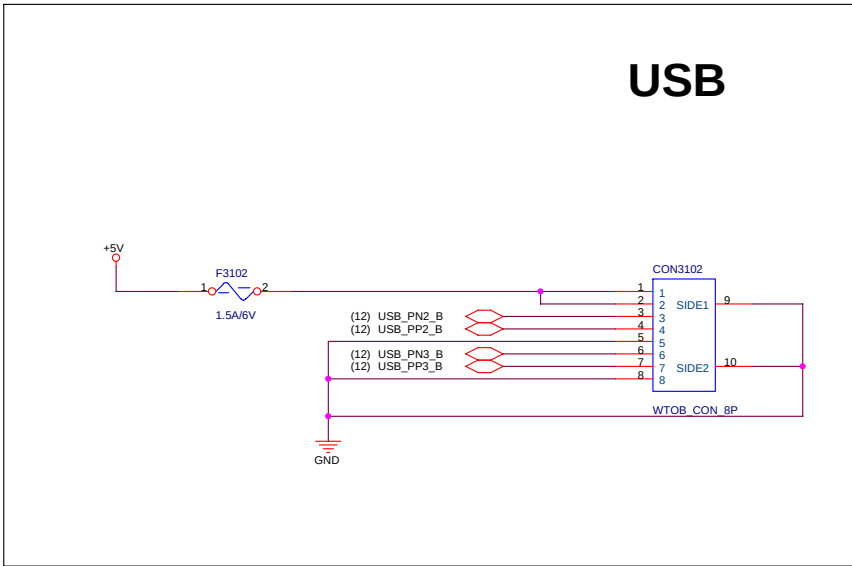
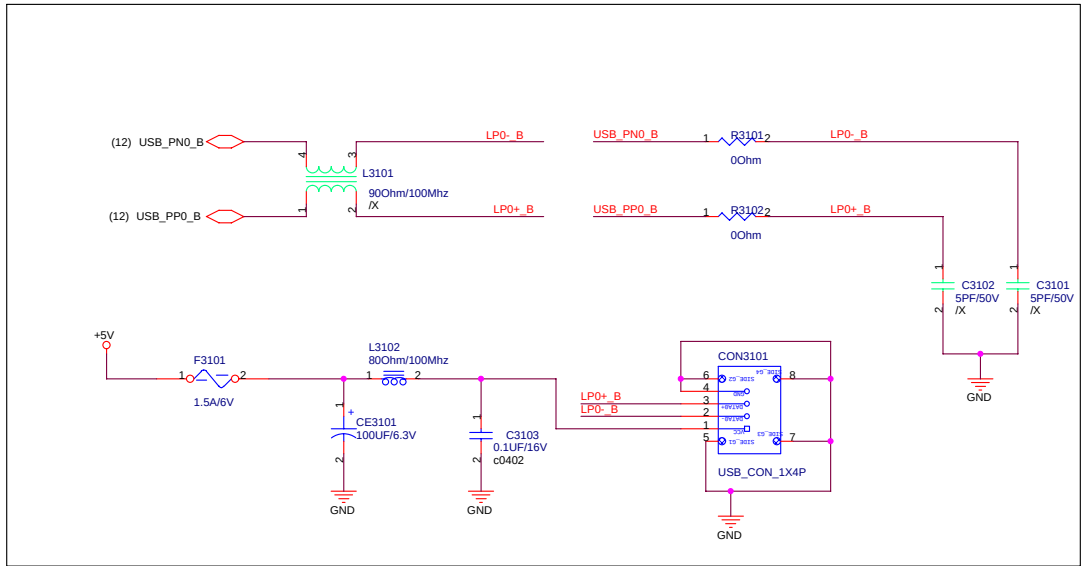


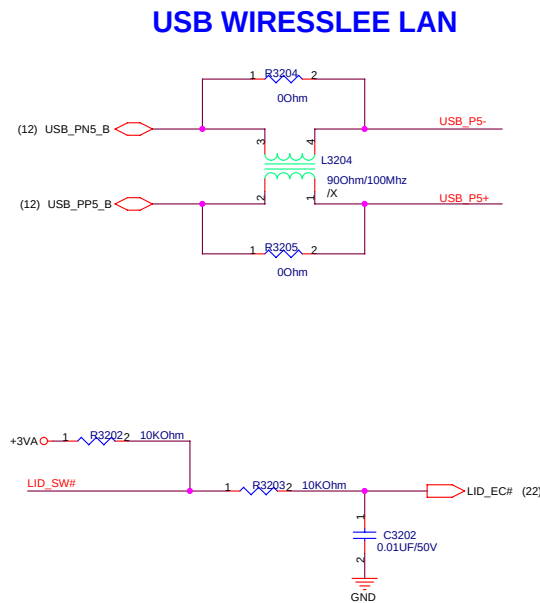
Memory Card Detect

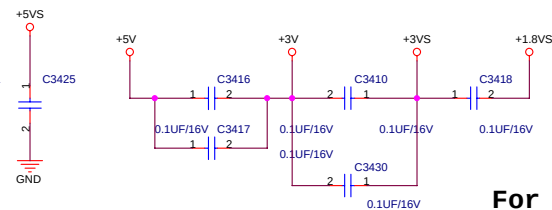
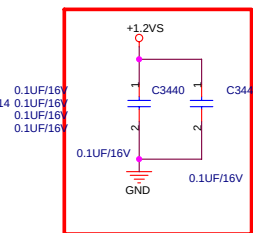
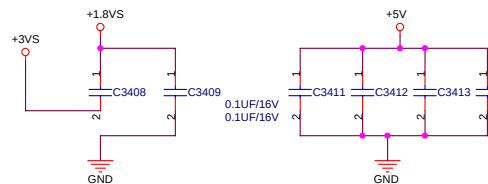
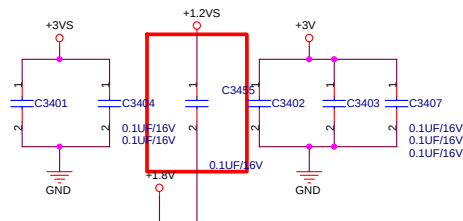
MS_CD#	SD_CD#	
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

MC_CD# : Memory Card Detect





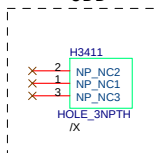




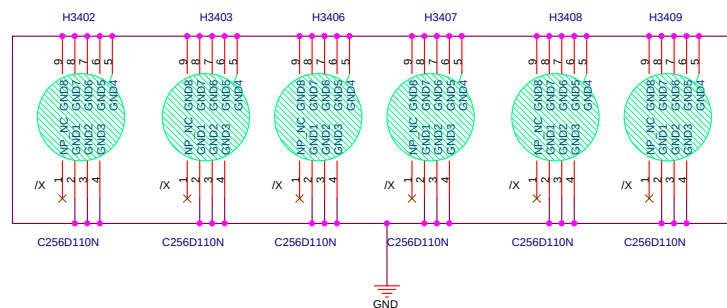
Rev 1.1 add for EMI

For EMI

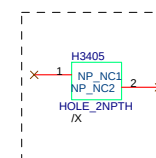
ODD



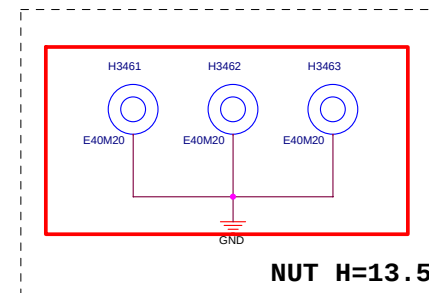
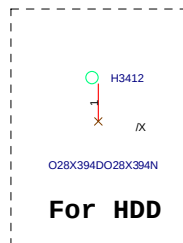
Hole no GND --- A



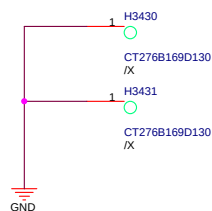
PAD Hole (2hole)--- E



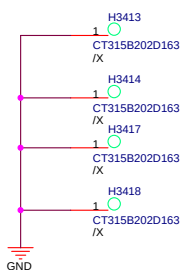
Oblong drill hole



NUT H=13.5

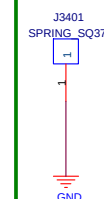
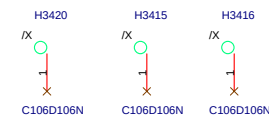


For mount NB Heatsink



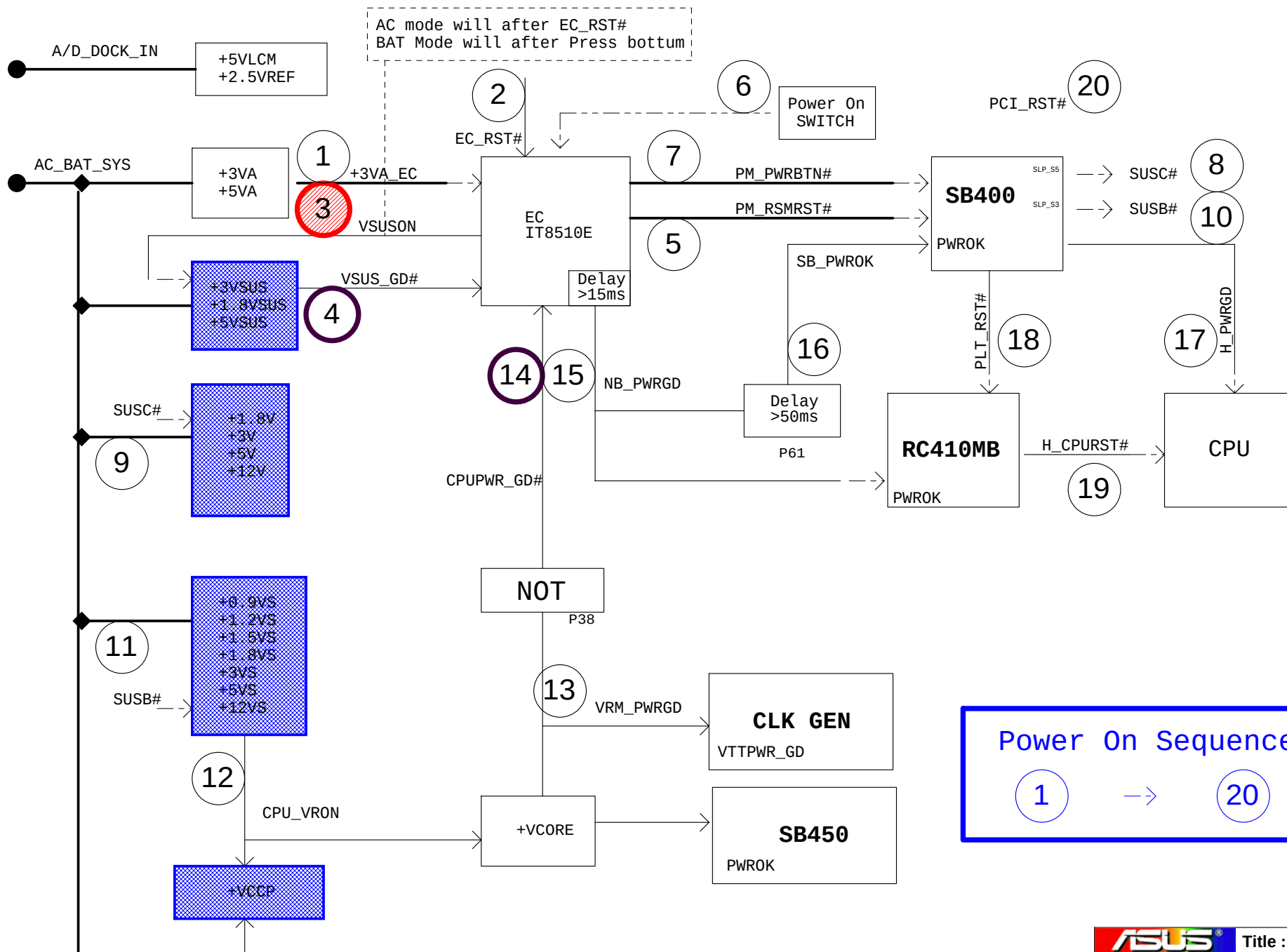
For mount CPU spring

MB HOLE



For EMI

PTH Hole



Power On Sequence

1 → 20

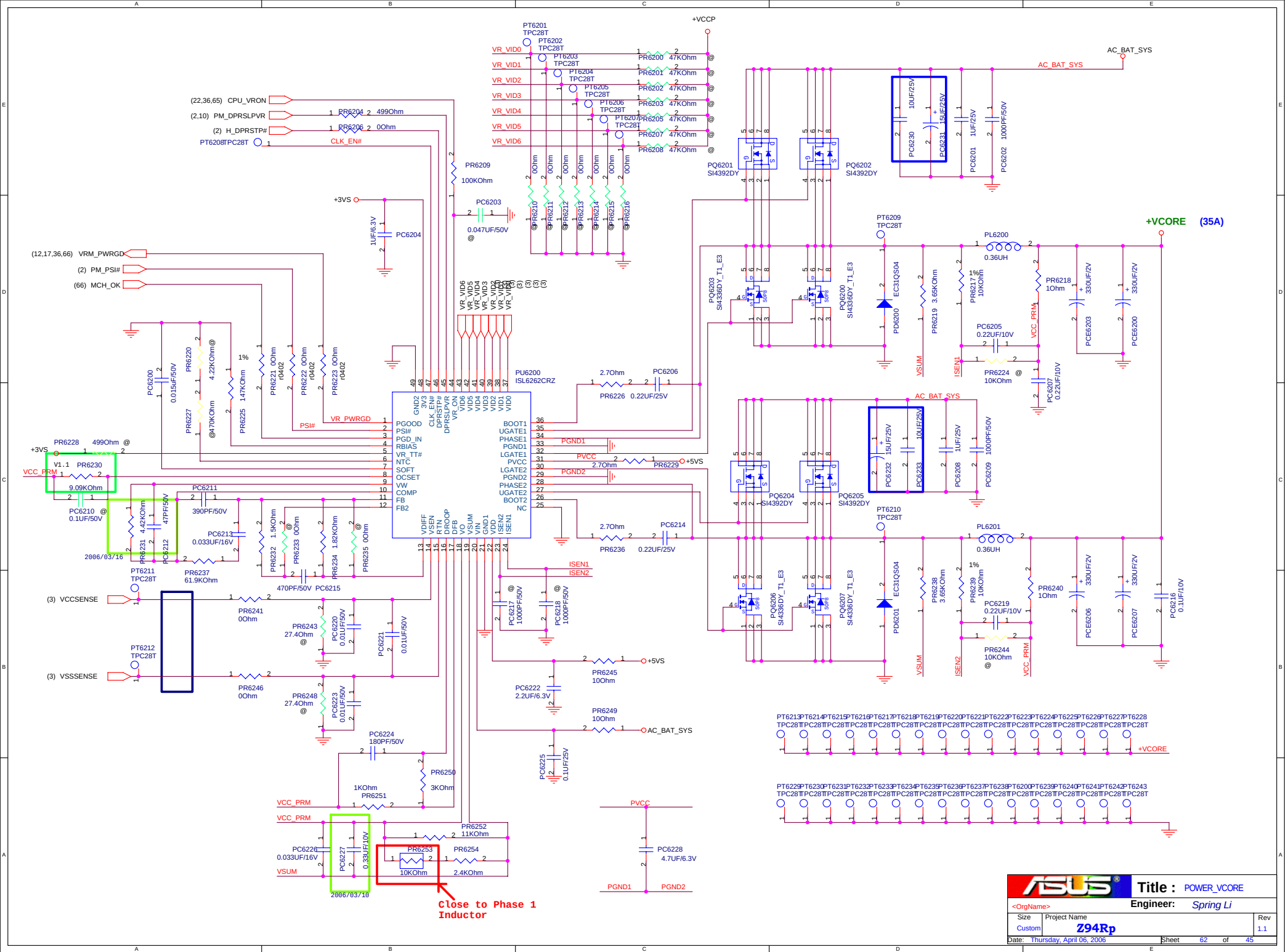
PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

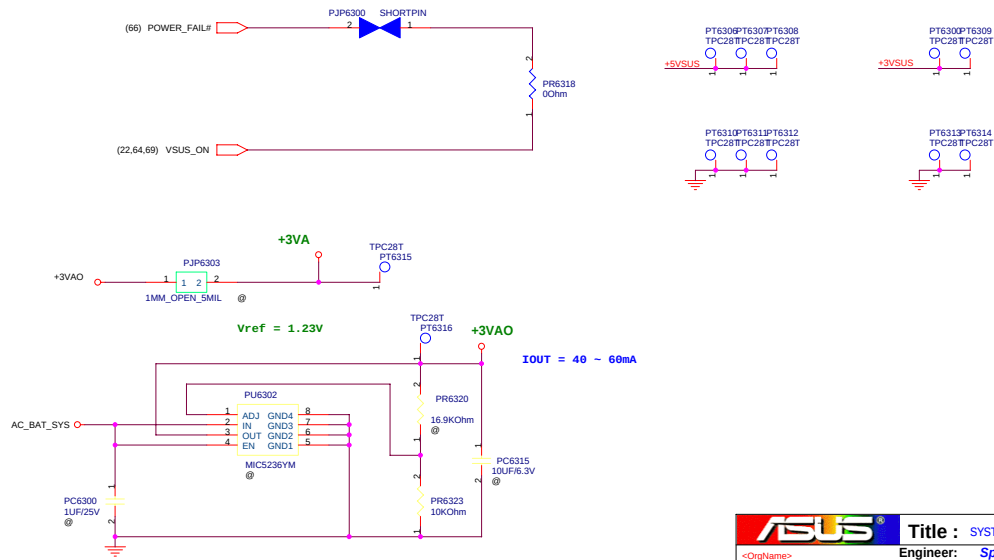
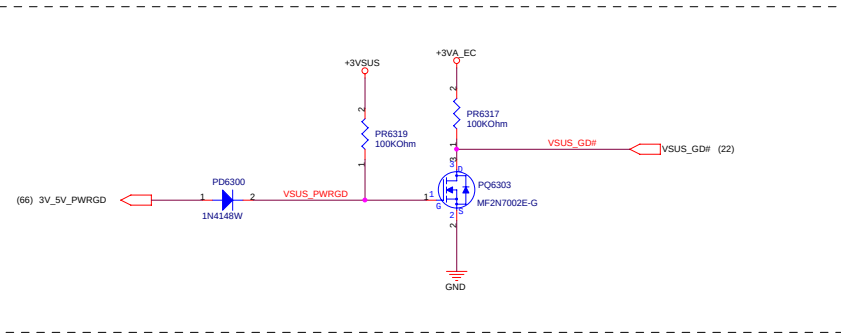
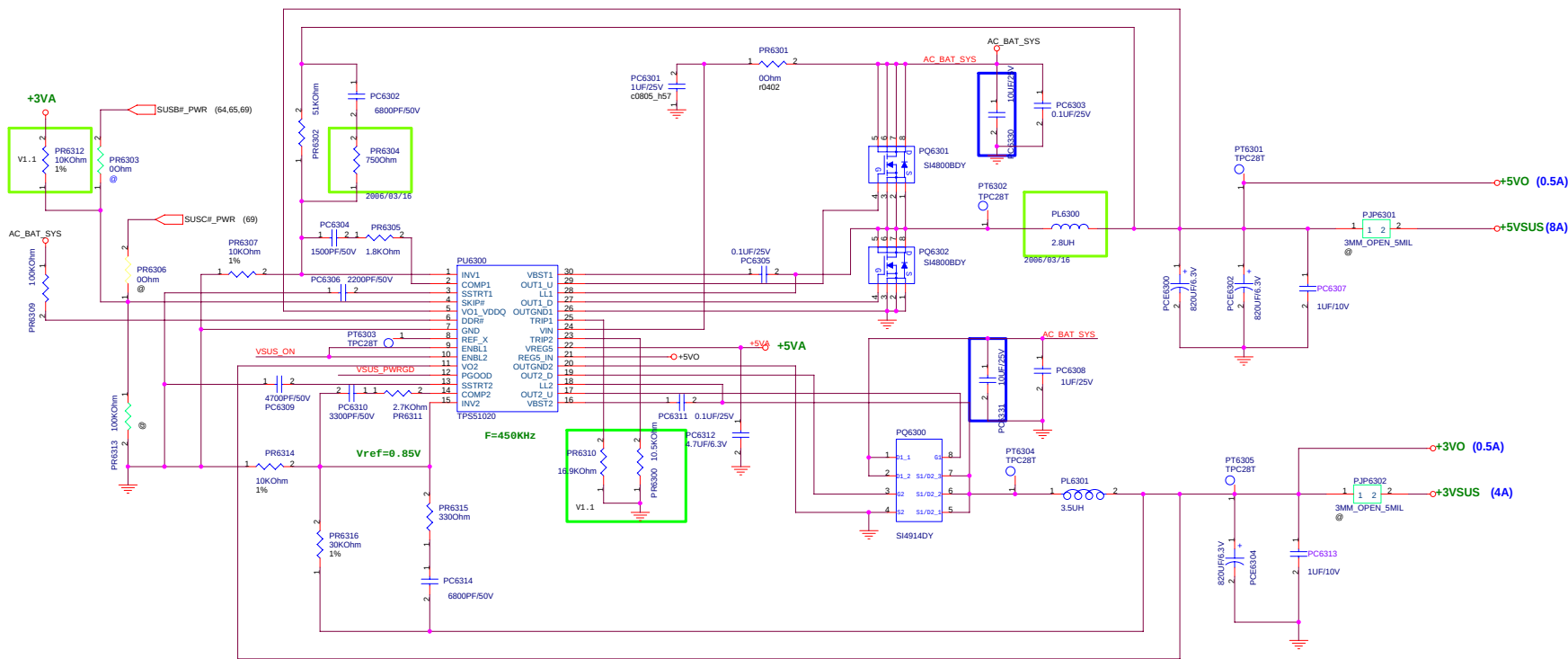
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

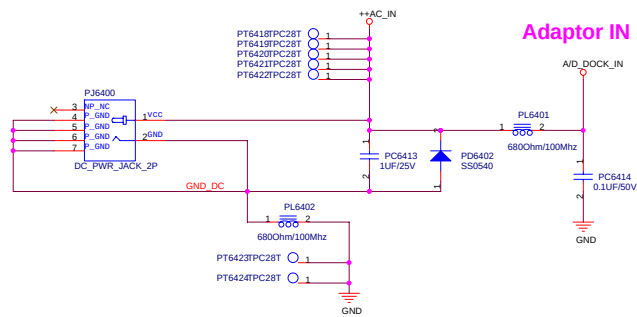
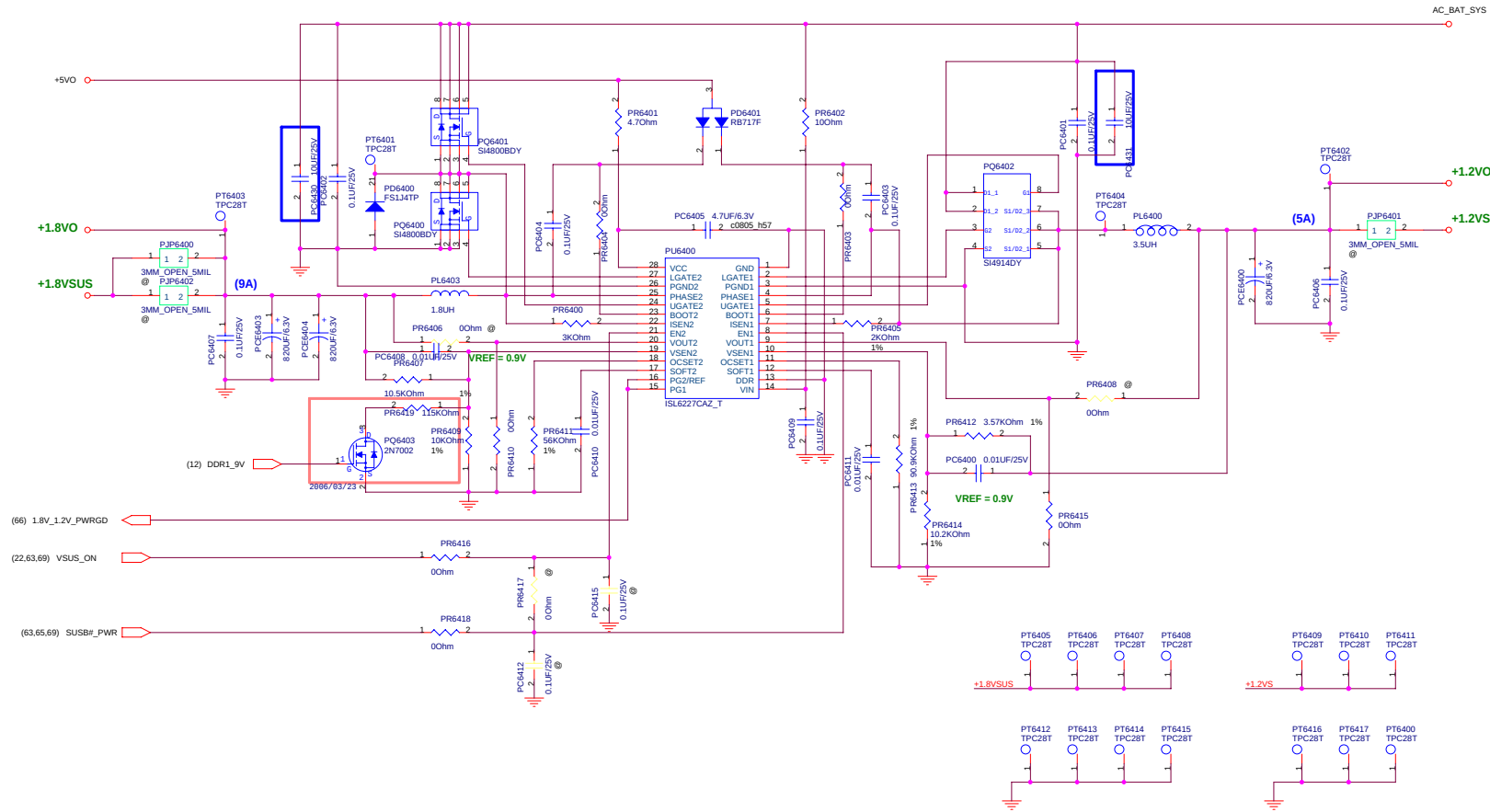
SB400 GPIO TABLE

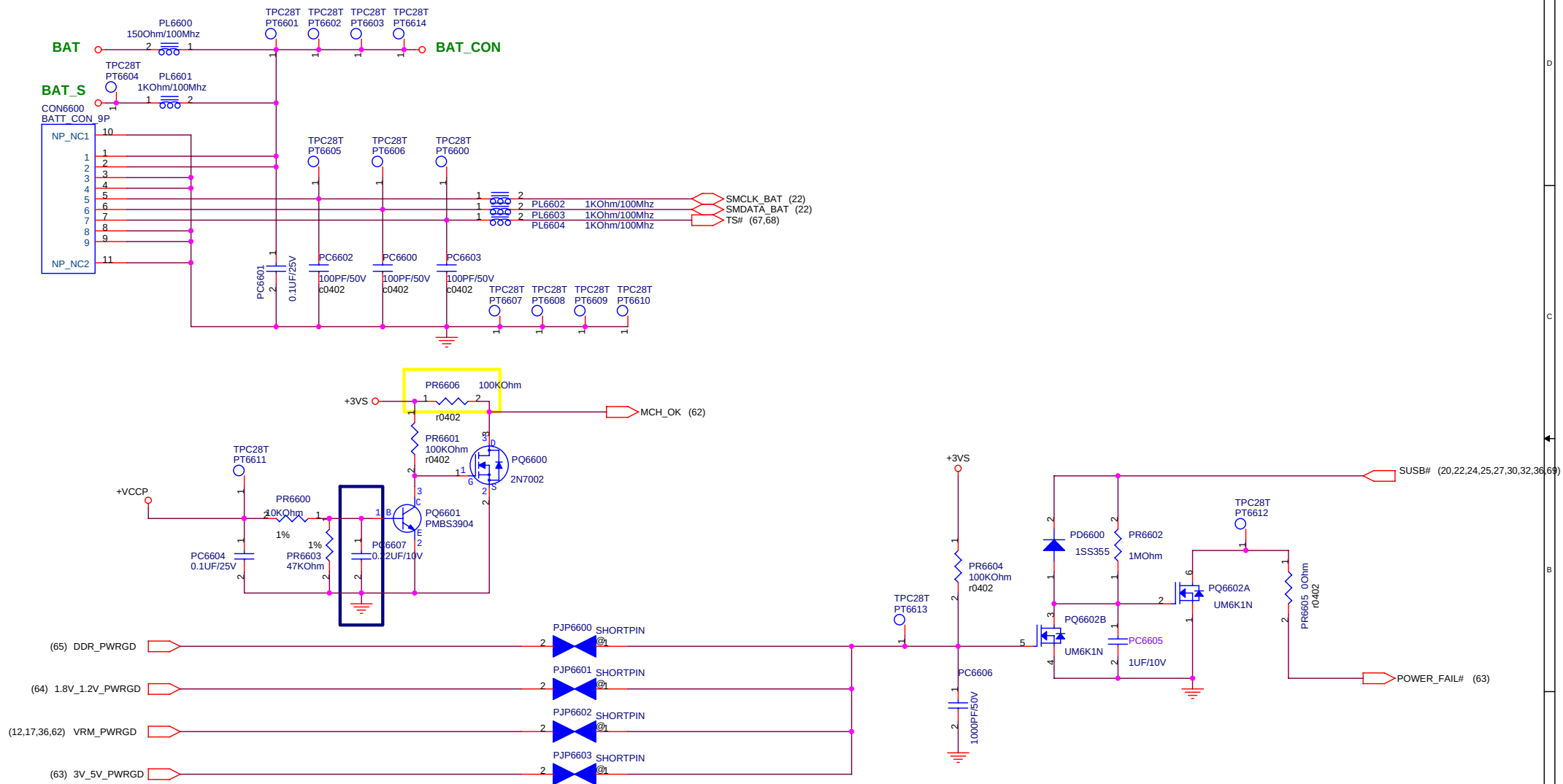
GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

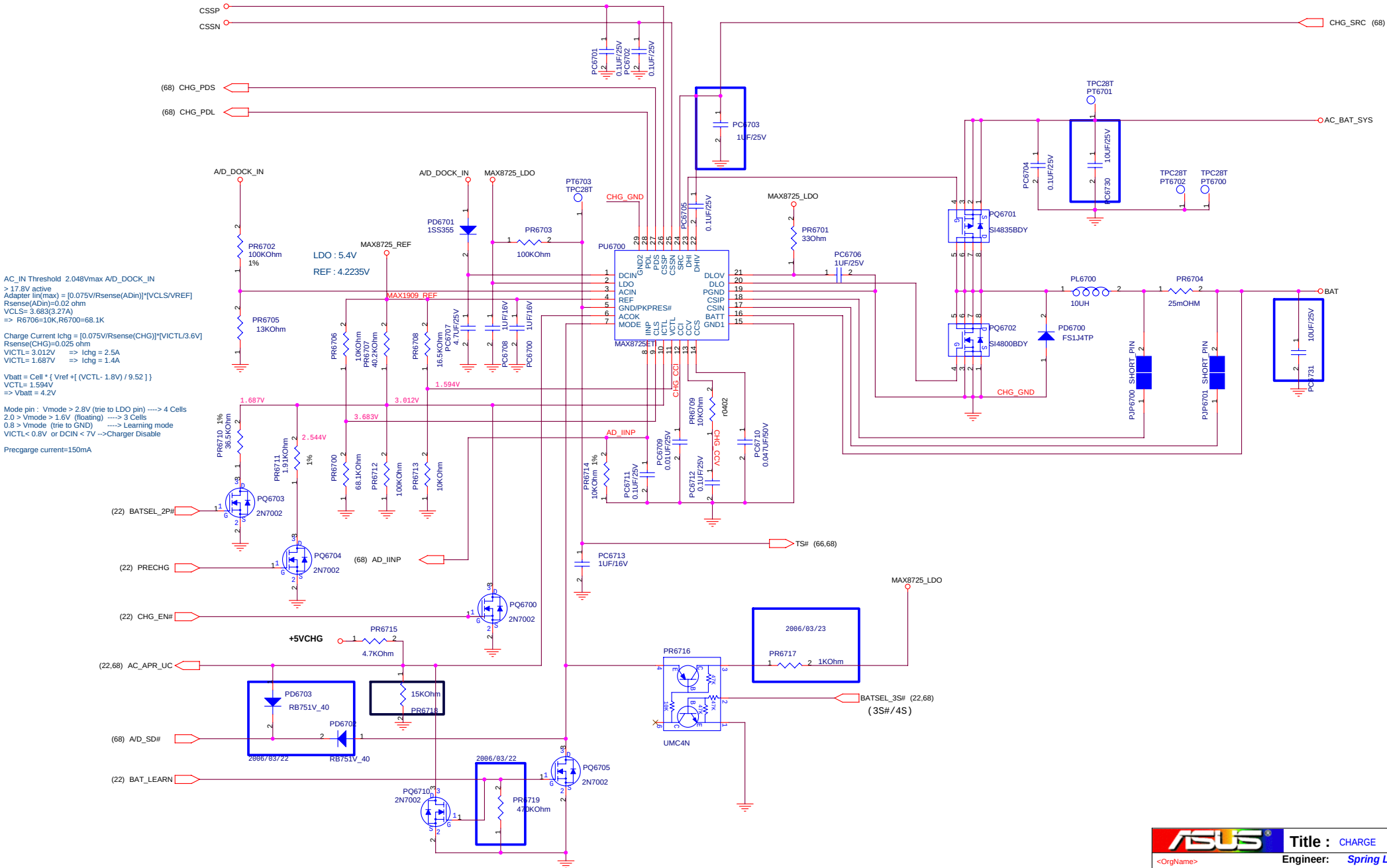
KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

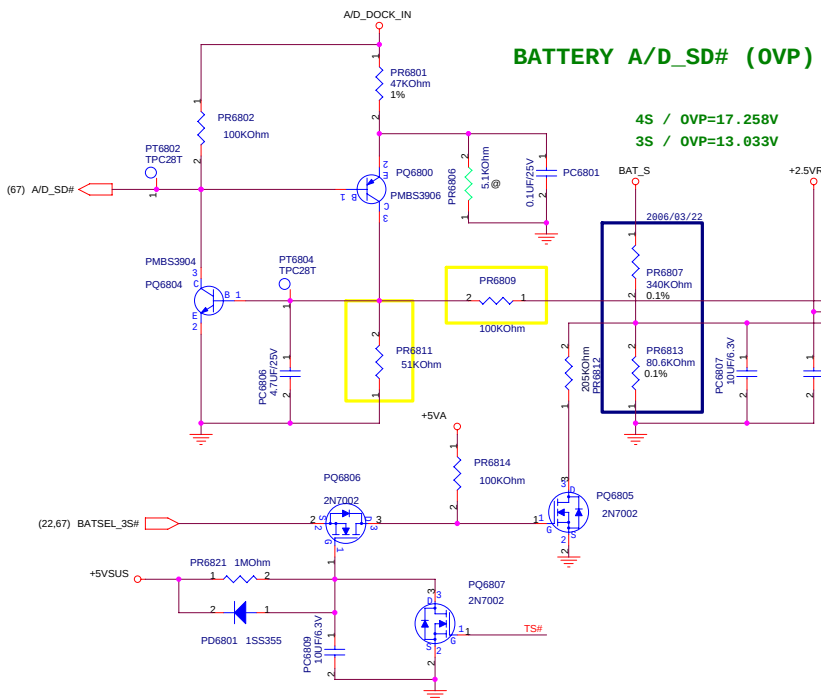




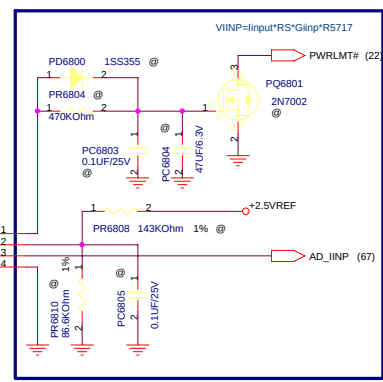




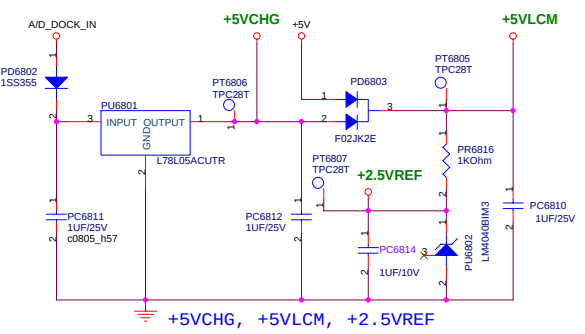
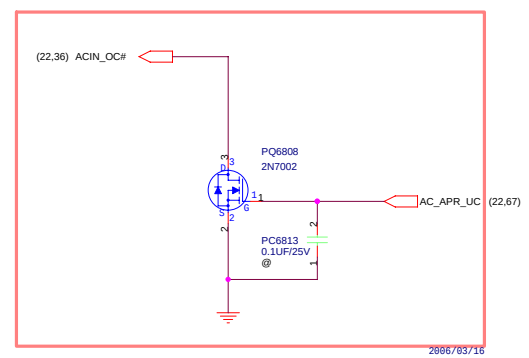
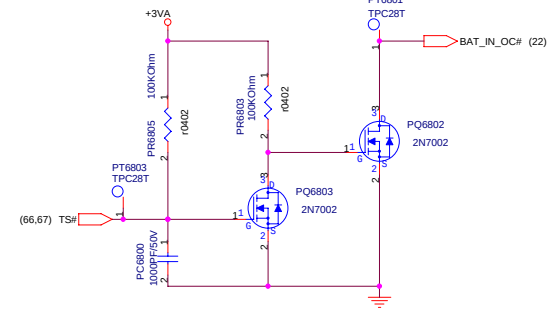




Power Limit Circuit



BATTERY IN DETECT



POWER PATH & BAT_LEARN

