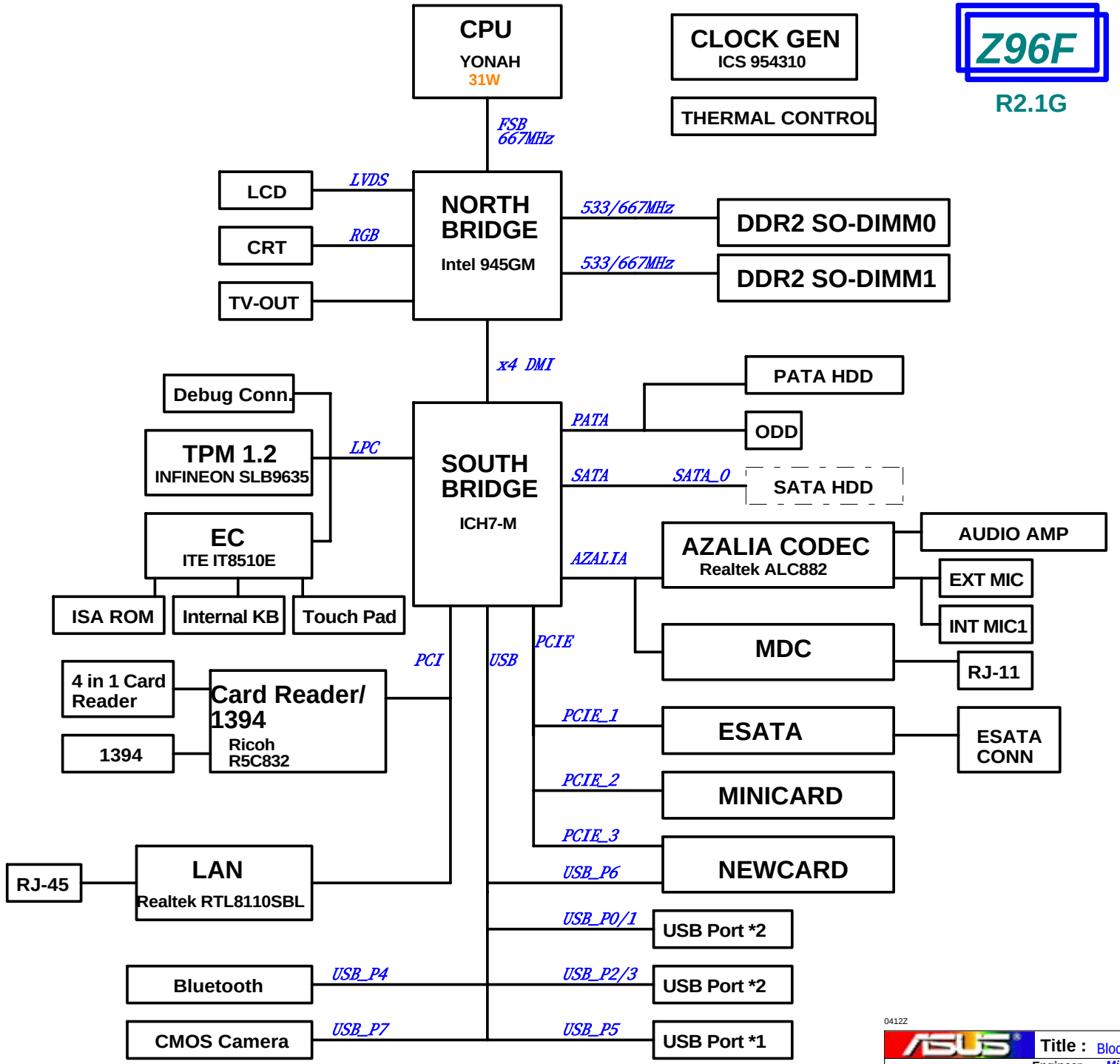


0412Z

Title : Block Diagram

ASUSTek Computer INC. Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 1 of 96

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O	H	GPI
37	PWM3/GPA3	/	I		GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	AC_OK#	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

06/01/23

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	01001100 (4C)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

0412Z

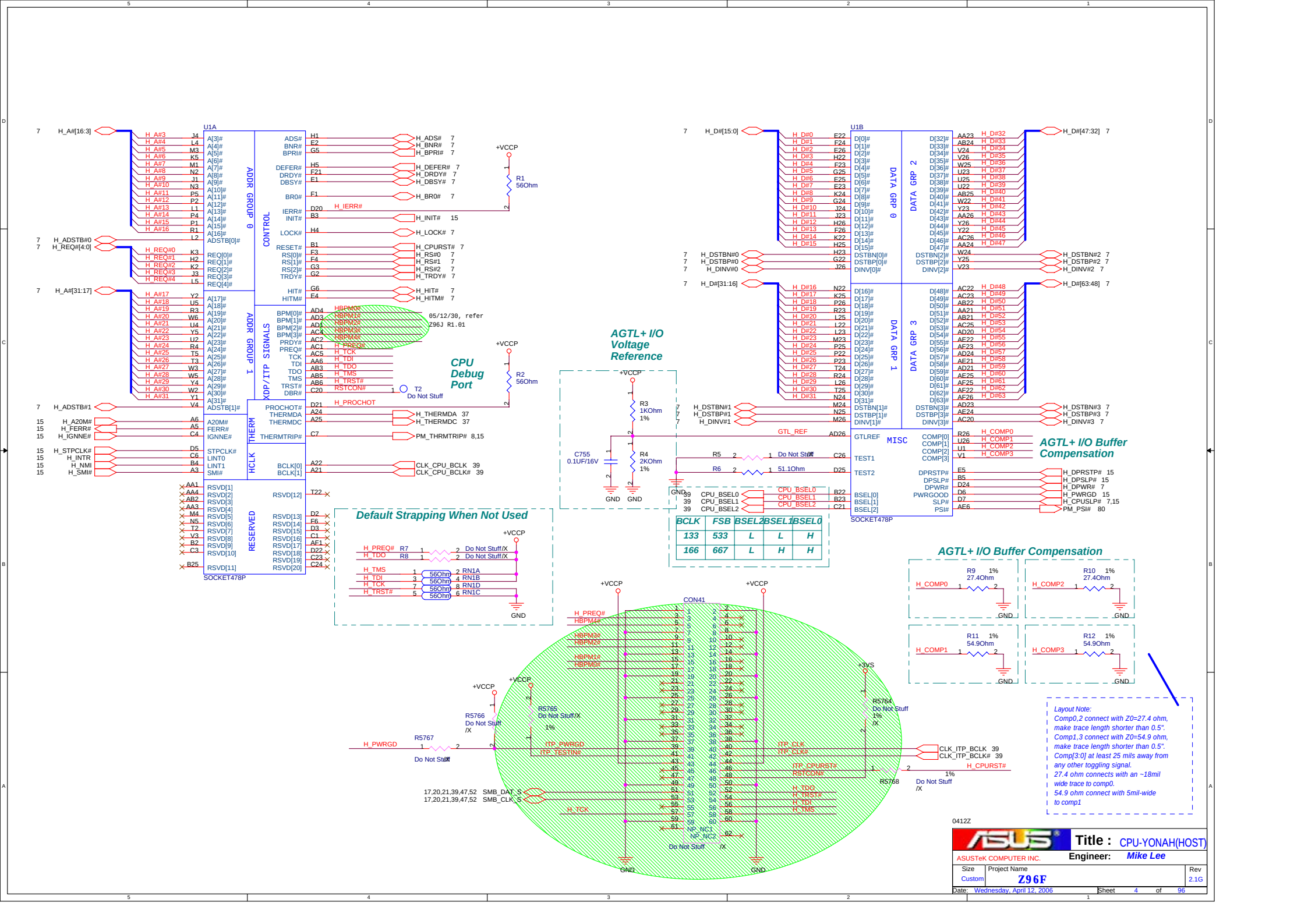
ASUSTek Computer INC.

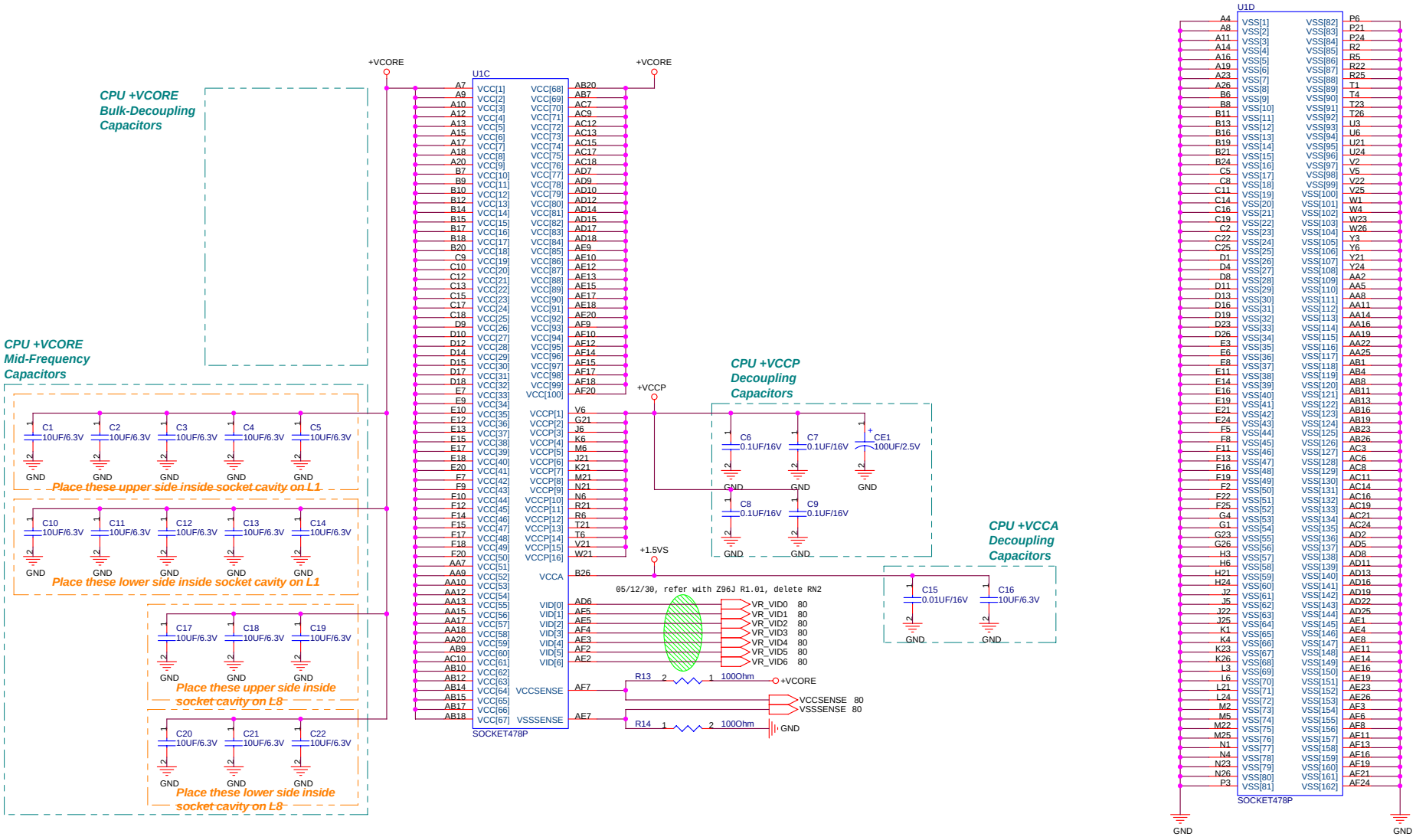
Title : <Title>

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 2 of 96


U1A
U1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478P
CPU Debug Port
AGTL+ I/O Voltage Reference
AGTL+ I/O Buffer Compensation
Default Strapping When Not Used
CON41
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
133 | 533 | L | L | H
166 | 667 | L | H | H
Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1
0412Z
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size: Custom
Project Name: Z96F
Rev: 2.1G
Date: Wednesday, April 12, 2006
Sheet 4 of 96



+VCORE Mid-Frequency Capacitor
- Intel: 22UF *32
- R1F: 10UF *16

+VCCP Decoupling Capacitor
- Intel: 270UF *1, 0.1UF *6
- R1F: 220UF *1, 0.1UF *4

0412Z

ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 5 of 96	

RCOMP

For Calibrating the FSB I/O Buffer

H_XRCOMP — R15 24.9Ohm 1% — GND

H_YRCOMP — R16 24.9Ohm 1% — GND

SCOMP

For Slew Rate Compenssation on the FSB

+VCCP — R19 54.9Ohm 1% — H_XSCOMP

+VCCP — R20 54.9Ohm 1% — H_YSCOMP

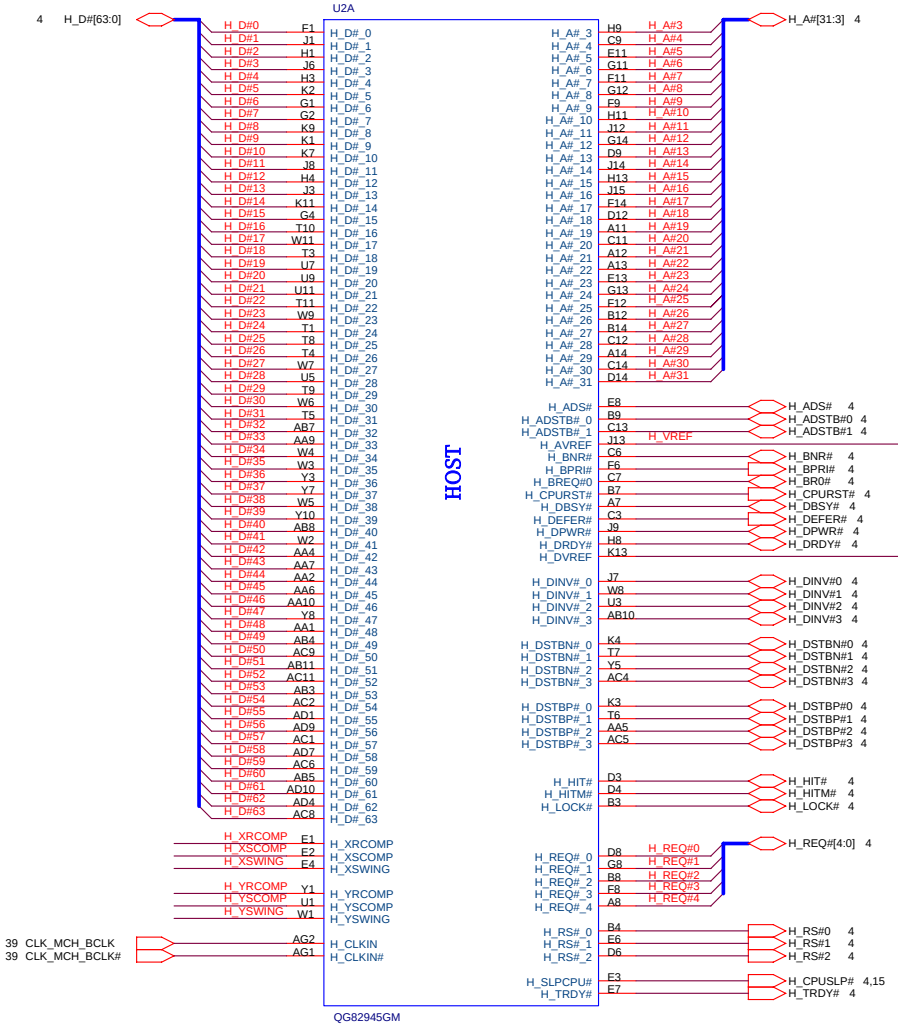
Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

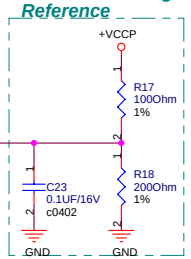
+VCCP — R21 221Ohm 1% — H_XSWING — R23 100Ohm 1% — C24 0.1UF/16V c0402 — GND GND

+VCCP — R22 221Ohm 1% — H_YSWING — R24 100Ohm 1% — C25 0.1UF/16V c0402 — GND GND

Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing



AGTL+ I/O Voltage Reference



Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

0412Z

ASUSTeK COMPUTER INC.

Title : NB-945GM(HOST)

Engineer: *Mike Lee*

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 7 of 96

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — 1 — R25 /X — 2 — Do Not Stuff — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — 1 — R26 /X — 2 — Do Not Stuff — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — 1 — R27 /X — 2 — Do Not Stuff — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — 1 — R30 /X — 2 — Do Not Stuff — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — 1 — R31 /X — 2 — Do Not Stuff — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — 1 — R34 /X — 2 — Do Not Stuff — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+2.5VS

MCH_CFG_18 — 1 — R35 /X — 2 — Do Not Stuff

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — 1 — R37 /X — 2 — Do Not Stuff — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

+2.5VS

MCH_CFG_19 — 1 — R38 /X — 2 — Do Not Stuff — GND

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

U2B

RSVD: RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 TV_DCONSEL_0 TV_DCONSEL_1 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15

CFG: CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM: PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 PM_THRMTRIP# PWROK RSTIN#

MISC: SDVO_CTRLCLK SDVO_CTRLDATA ICH_SYNC# CLK_REQ#

NC: NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

DDR MUXING: SM_CK_0 SM_CK_1 SM_CK_2 SM_CK_3 / SM_CK#_0 SM_CK#_1 SM_CK#_2 SM_CK#_3 / SM_CKE_0 SM_CKE_1 SM_CKE_2 SM_CKE_3 / SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 / SM_OCDCOMP_0 SM_OCDCOMP_1 / SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 / SM_RCOMP# SM_RCOMP / SM_VREF_0 SM_VREF_1

CLK: G_CLKIN# G_CLKIN D_REFCLKIN# D_REFCLKIN D_REFSSCLKIN# D_REFSSCLKIN

DMI: DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 / DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 / DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 / DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3

QG82945GM

39 MCH_BSEL0, 39 MCH_BSEL1, 39 MCH_BSEL2

+3VS — Do Not Stuff — T3

17 PM_BMBUSY#

R32 10KOhm r0402 PM_EXTTS#_0; R33 10KOhm r0402 PM_EXTTS#_1

4,15 PM_THRMTRIP#

17,59,80,90 VRM_PWRGD

16,17,47,52 BUF_PLT_RST# — R36 100Ohm — RST_IN_MCH#

16 MCH_ICH_SYNC#

R5794 0Ohm — GND

SM_CK_0 AY35; SM_CK_1 AR1; SM_CK_2 AW7; SM_CK_3 AW40 → M_CLK_DDR0 20, M_CLK_DDR1 20, M_CLK_DDR2 21, M_CLK_DDR3 21

SM_CK#_0 AW35; SM_CK#_1 AT1; SM_CK#_2 AY7; SM_CK#_3 AY40 → M_CLK_DDR#0 20, M_CLK_DDR#1 20, M_CLK_DDR#2 21, M_CLK_DDR#3 21

SM_CKE_0 AU20; SM_CKE_1 AT20; SM_CKE_2 BA29; SM_CKE_3 AY29 → M_CKE0 20,22; M_CKE1 20,22; M_CKE2 21,22; M_CKE3 21,22

SM_CS#_0 AW13; SM_CS#_1 AW12; SM_CS#_2 AY21; SM_CS#_3 AW21 → M_CS#0 20,22; M_CS#1 20,22; M_CS#2 21,22; M_CS#3 21,22

Layout Note: Route as short as possible

SM_OCDCOMP_0 AL20 — M_OCDCOMP0 — R5792 — Do Not Stuff/X

SM_OCDCOMP_1 AF10 — M_OCDCOMP1 — R5793 — Do Not Stuff/X — GND

SM_ODT_0 BA13; SM_ODT_1 BA12; SM_ODT_2 AY20; SM_ODT_3 AU21 → M_ODT0 20,22; M_ODT1 20,22; M_ODT2 21,22; M_ODT3 21,22

+1.8V

SM_RCOMP# AV9 — R28 80.6Ohm 1%; SM_RCOMP AT9 — R29 80.6Ohm 1% — GND

SM_VREF_0 AK1; SM_VREF_1 AK41 — M_VREF_MCH → M_VREF_MCH 20,21,22

G_CLKIN# AF33; G_CLKIN AG33; D_REFCLKIN# A27 CLK_UMA_96M#; D_REFCLKIN A26 CLK_UMA_96M; D_REFSSCLKIN# C40 CLK_LCD_SSCG#; D_REFSSCLKIN D41 CLK_LCD_SSCG

→ CLK_MCH_3GPLL# 39, CLK_MCH_3GPLL 39, CLK_UMA_96M# 39, CLK_UMA_96M 39, CLK_LCD_SSCG# 39, CLK_LCD_SSCG 39

DMI_RXN_0 AE35 DMI_TXN0; DMI_RXN_1 AE39 DMI_TXN1; DMI_RXN_2 AG35 DMI_TXN2; DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN[3:0] 16

DMI_RXP_0 AC35 DMI_TXP0; DMI_RXP_1 AE39 DMI_TXP1; DMI_RXP_2 AE35 DMI_TXP2; DMI_RXP_3 AG39 DMI_TXP3 → DMI_TXP[0..3] 16

DMI_TXN_0 AE37 DMI_RXN0; DMI_TXN_1 AE41 DMI_RXN1; DMI_TXN_2 AG37 DMI_RXN2; DMI_TXN_3 AH41 DMI_RXN3 → DMI_RXN[0..3] 16

DMI_TXP_0 AC37 DMI_RXP0; DMI_TXP_1 AE41 DMI_RXP1; DMI_TXP_2 AE37 DMI_RXP2; DMI_TXP_3 AG41 DMI_RXP3 → DMI_RXP[0..3] 16

M_VREF_MCH — C26 0.1UF/16V c0402 — GND; C27 1UF/10V — GND

R5798: 17,80 PM_DPRSLPVR — Do Not Stuff /X — PM_EXTTS#_1

0412Z

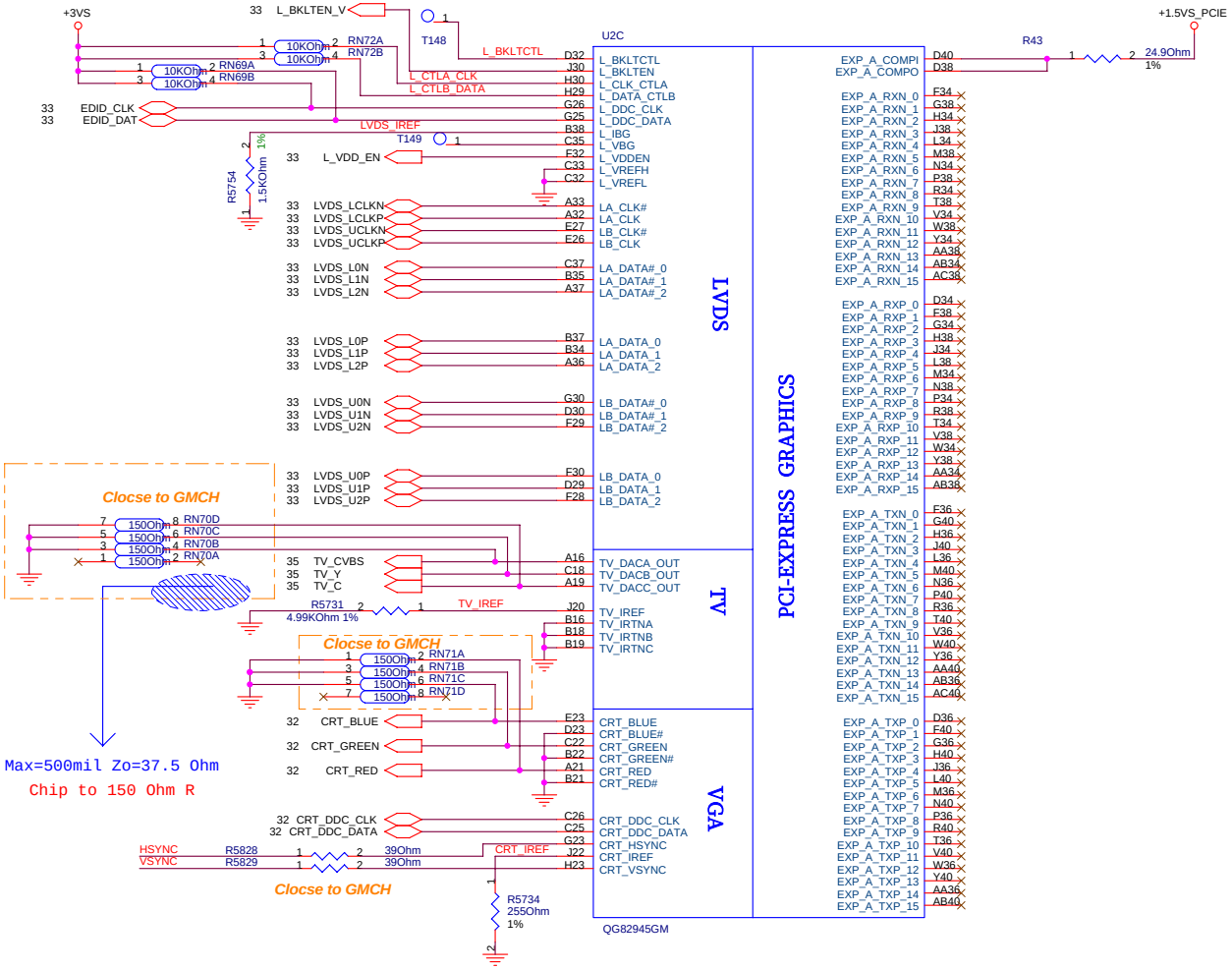
ASUSTeK COMPUTER INC.

Title : NB-945GM(DMI & CFG)

Engineer: Mike Lee

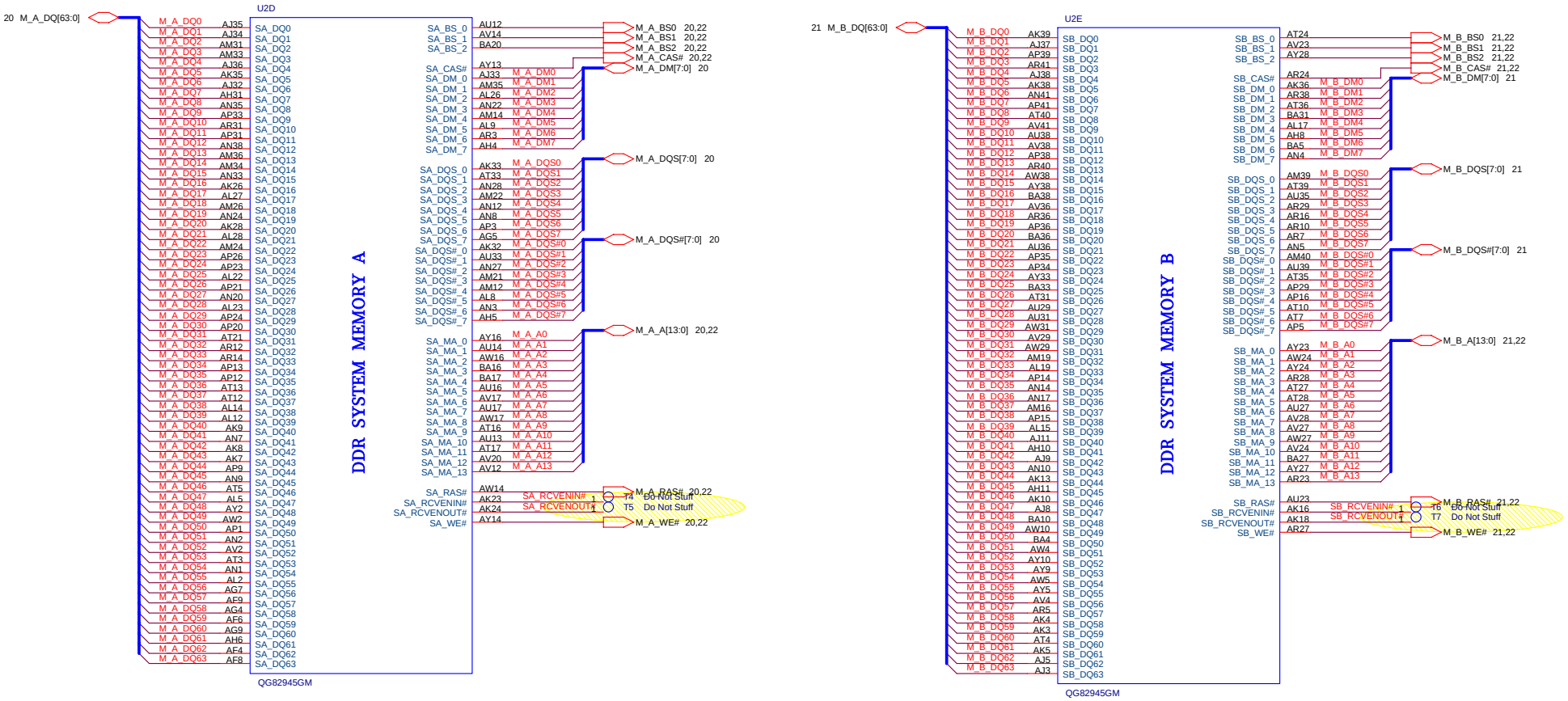
Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 8 of 96



0412Z

ASUSTeK COMPUTER INC.	Title : NB-945GM(GRAPHIC)	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 9 of 96	



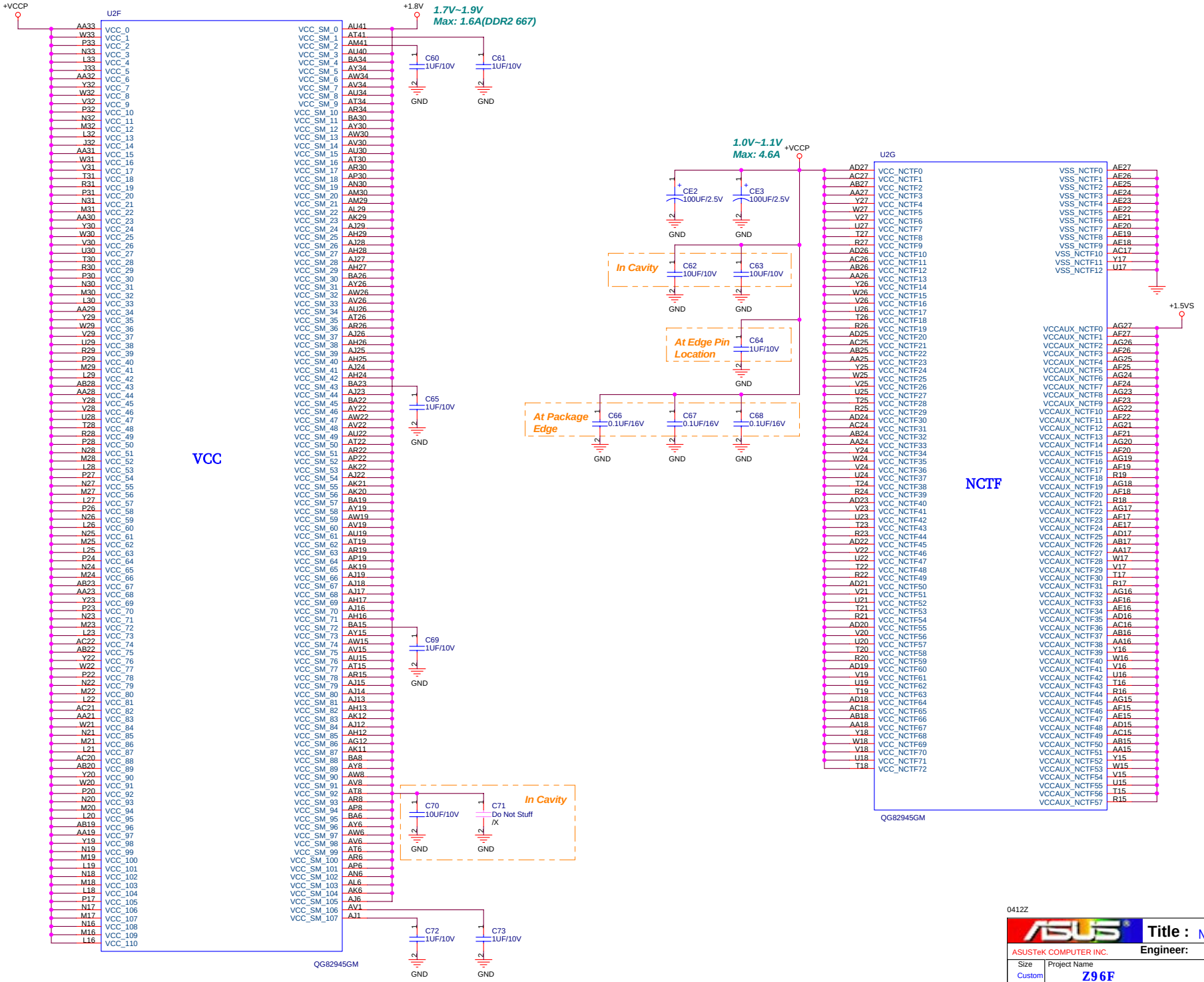
0412Z

Title : NB-945GM(DDR2)

ASUSTeK COMPUTER INC. Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 10 of 96



0412Z

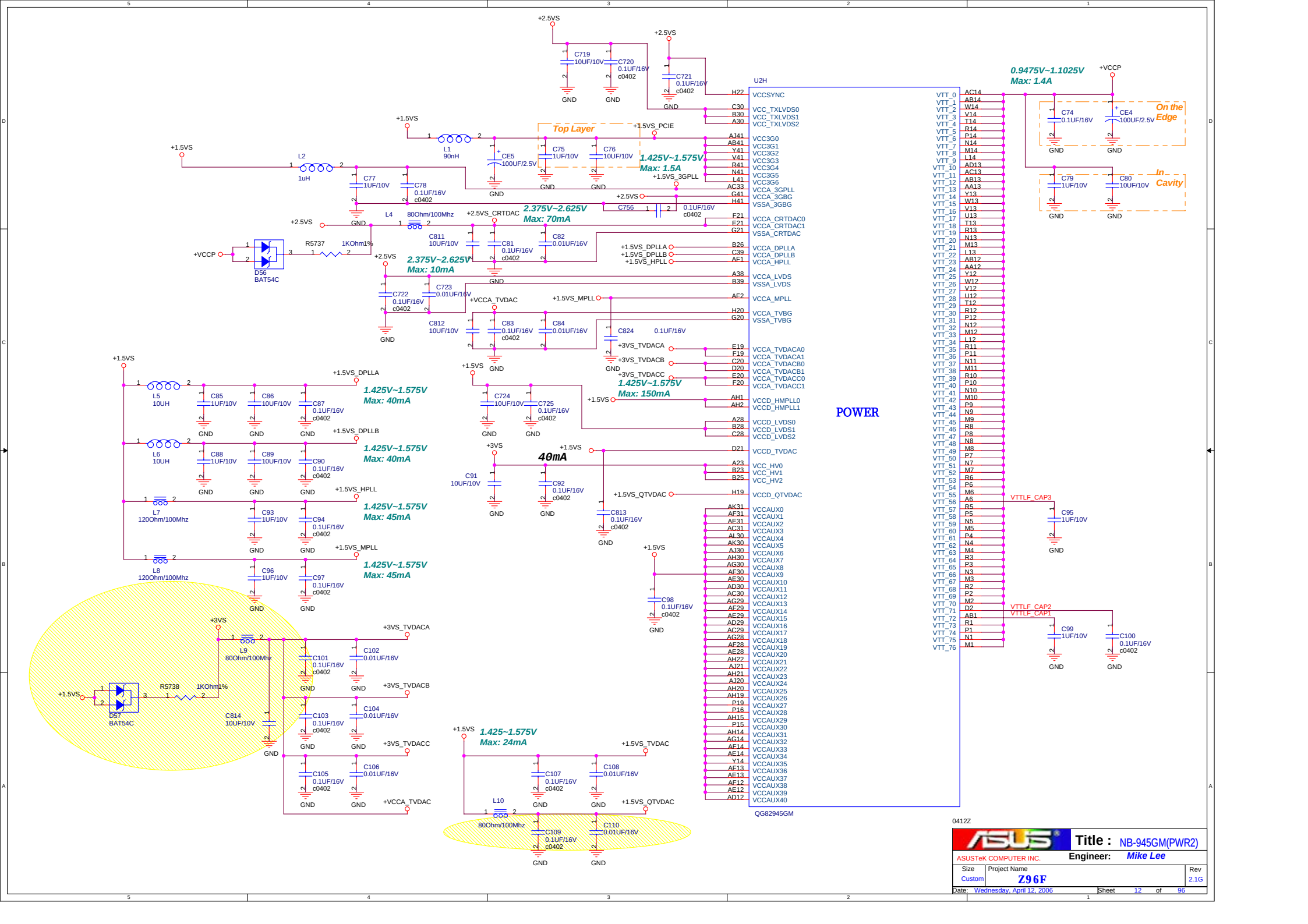
ASUSTeK COMPUTER INC.

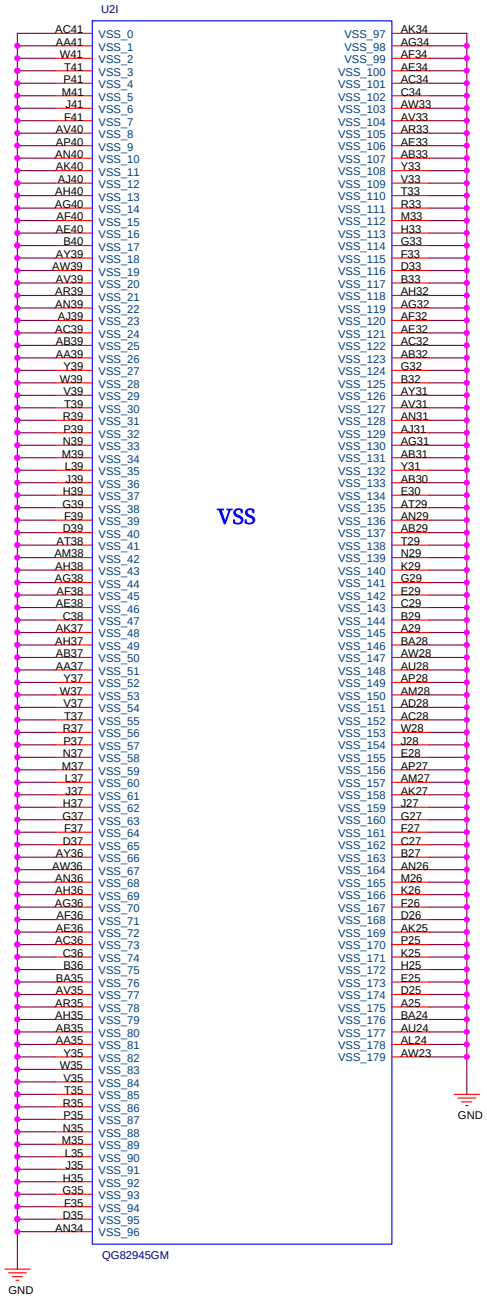
Title : NB-945GM(PWR)

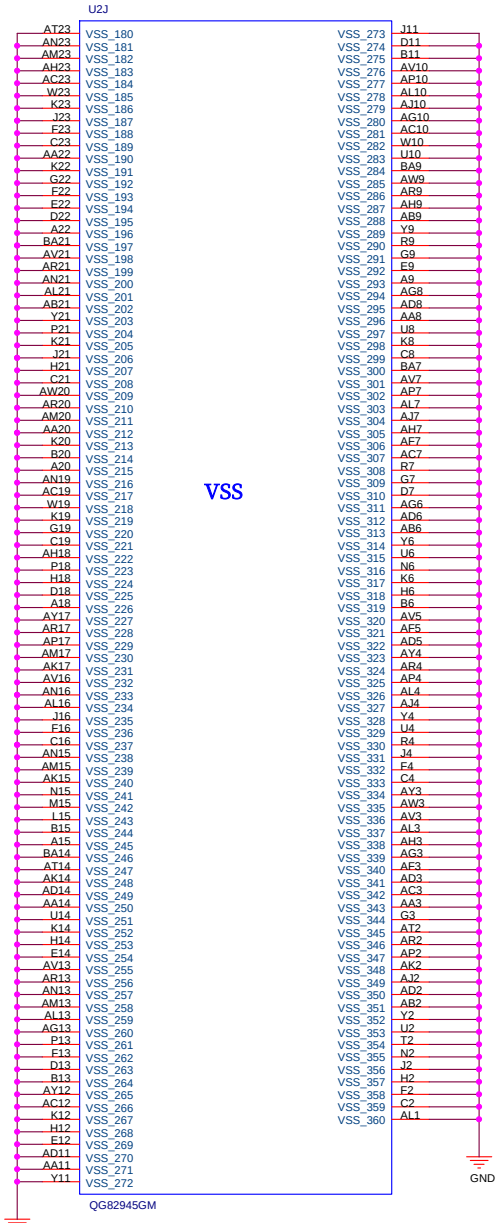
Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 11 of 96

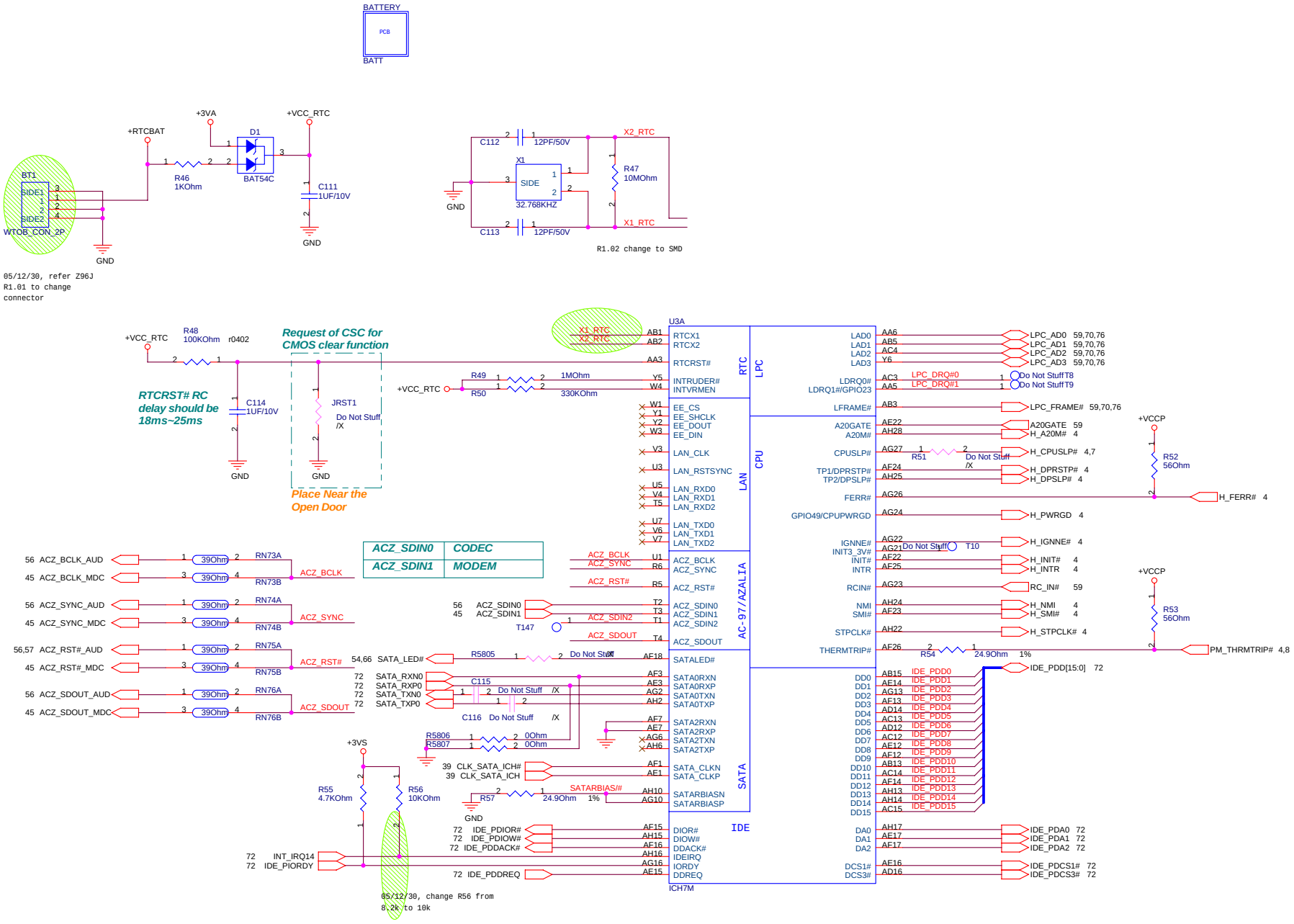

U2H
POWER
QG82945GM
Top Layer
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
2.375V~2.625V
Max: 10mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 150mA
40mA
1.425~1.575V
Max: 24mA
0.9475V~1.1025V
Max: 1.4A
On the Edge
In Cavity
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
D56 BAT54C
D57 BAT54C
0412Z
Title : NB-945GM(PWR2)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96F
Rev 2.1G
Date: Wednesday, April 12, 2006
Sheet 12 of 96





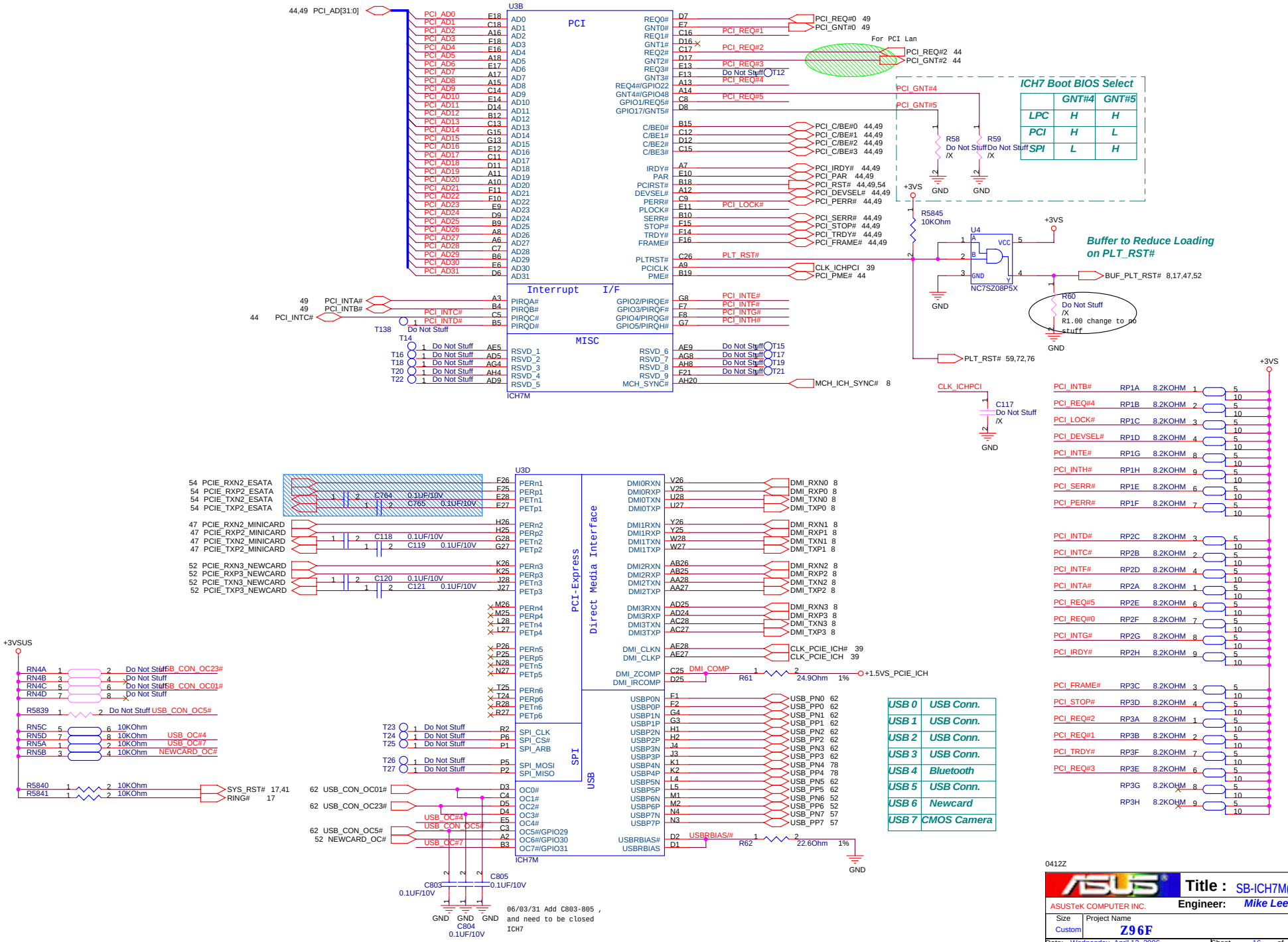
0412Z

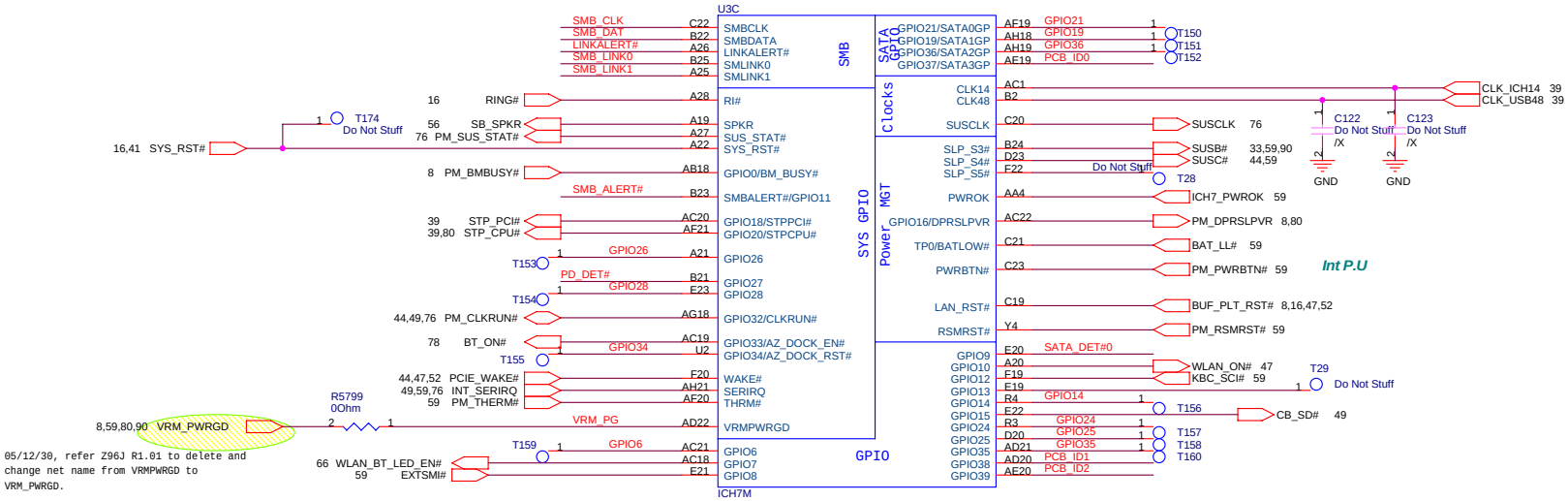
ASUSTeK COMPUTER INC.	Title : NB-945PM(GND)	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 13 of 96	

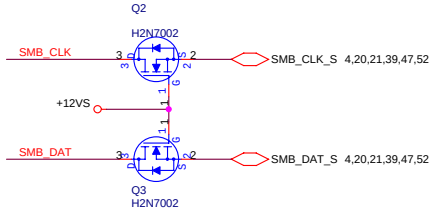


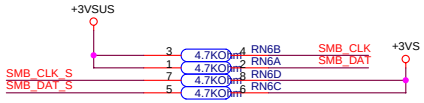
0412Z

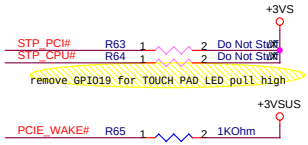
Title : SB-ICH7-M(1)		
ASUSTeK COMPUTER INC.	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 15 of 96	

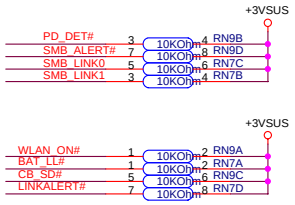

U3B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
For PCI Lan
Buffer to Reduce Loading on PLT_RST#
U3D
PCI-Express
Direct Media Interface
USB
SPI
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 USB Conn.
USB 6 Newcard
USB 7 CMOS Camera
06/03/31 Add C803-805 , and need to be closed ICH7
0412Z
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96F
Rev 2.1G
Date: Wednesday, April 12, 2006
Sheet 16 of 96

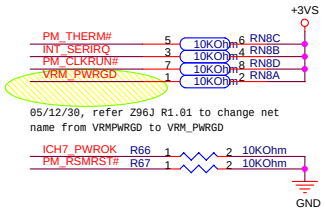


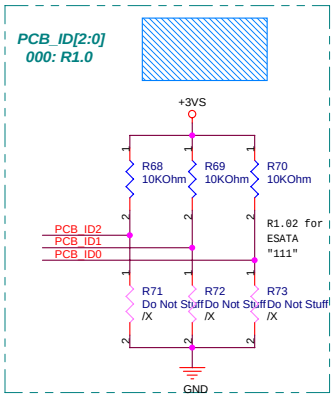












PCB_VID3 : PROJECT CODE

0412Z

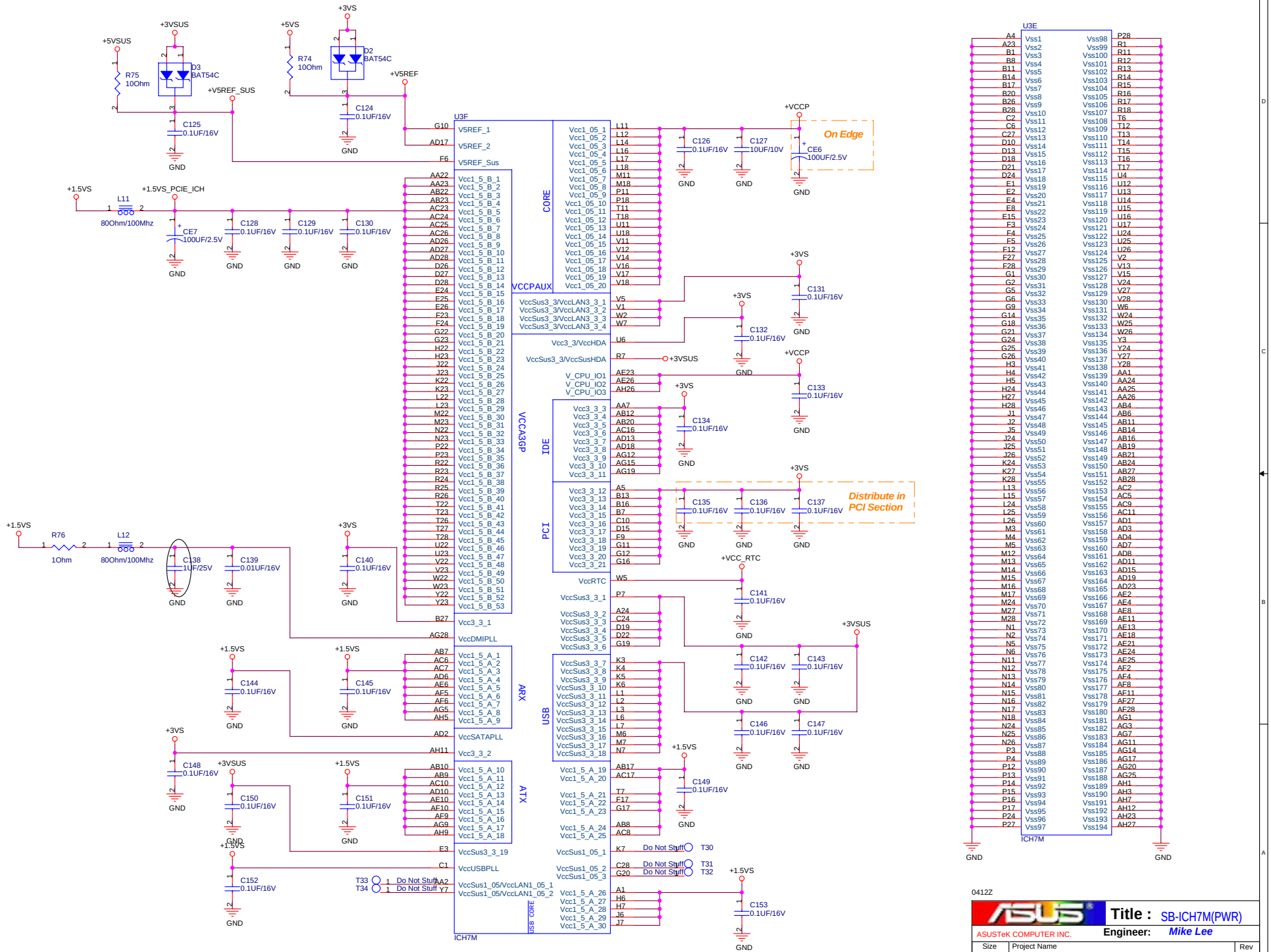
Title : SB-ICH7M(3)

ASUSTeK COMPUTER INC

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 17 of 96

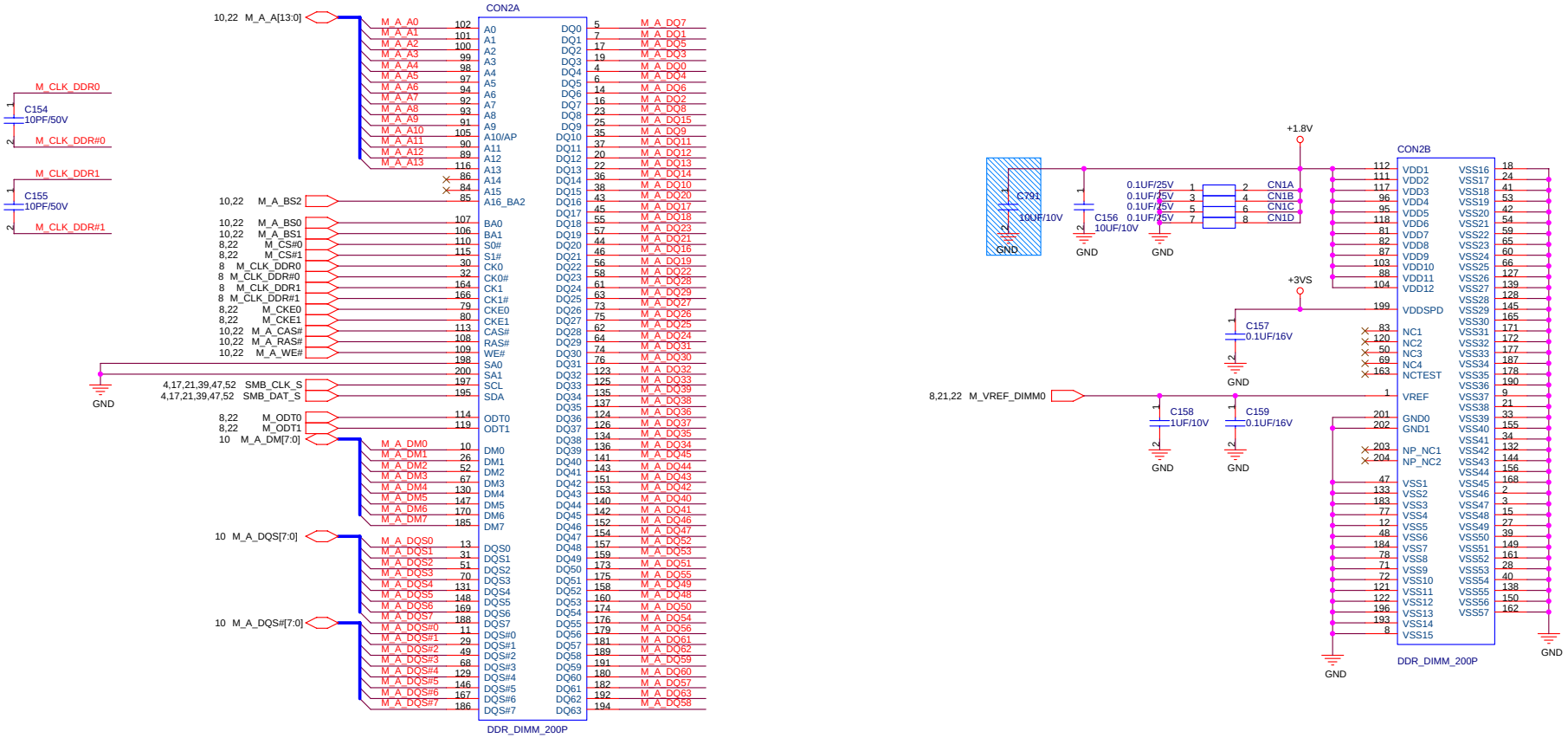


0412Z

Title : SB-ICH7M(PWR)		
ASUSTeK COMPUTER INC.	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 18 of 96	

M_A_DQ[63:0] 10

REV Type

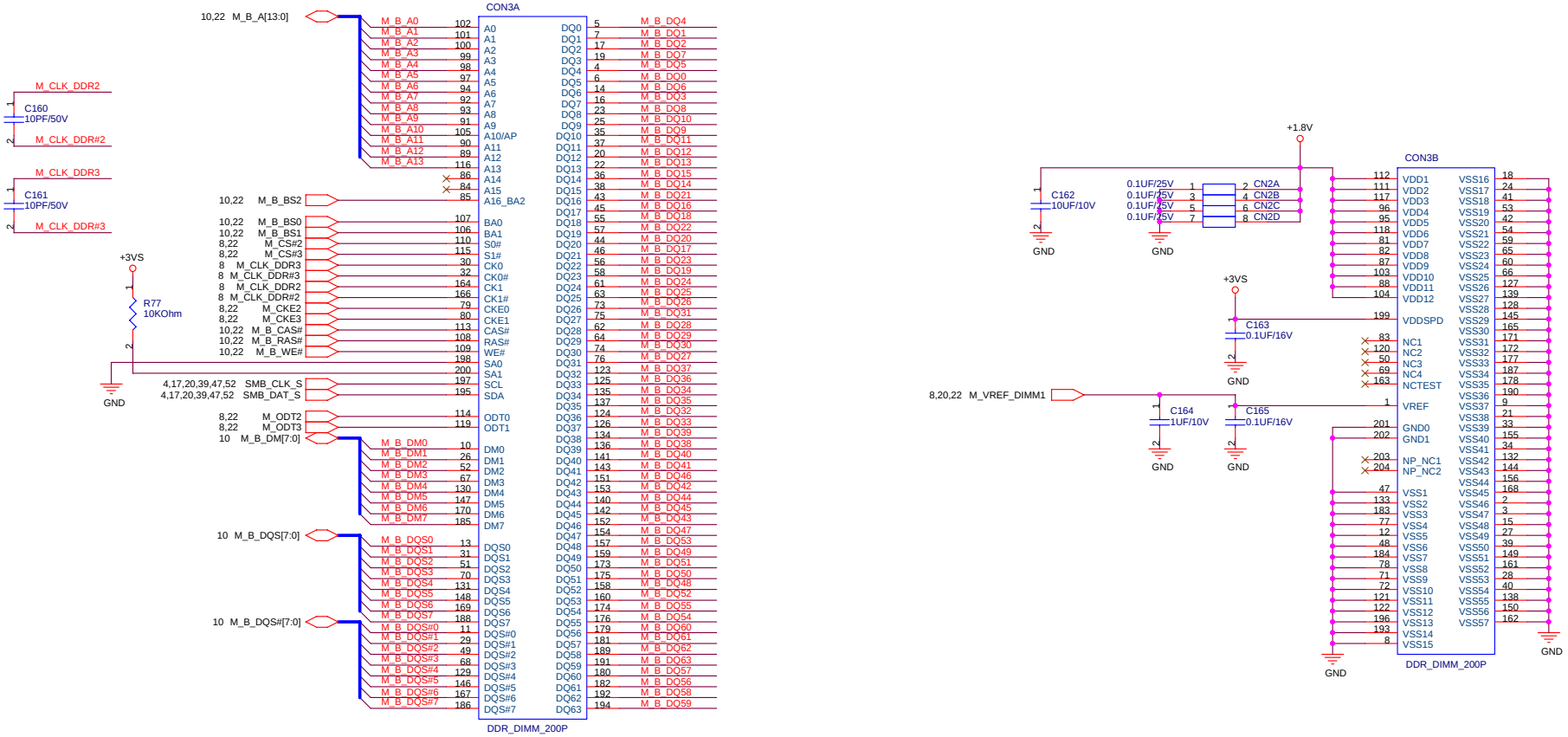


0412Z

ASUSTeK COMPUTER INC.	Title : DDR2 SO-DIMM0	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 20 of 96	

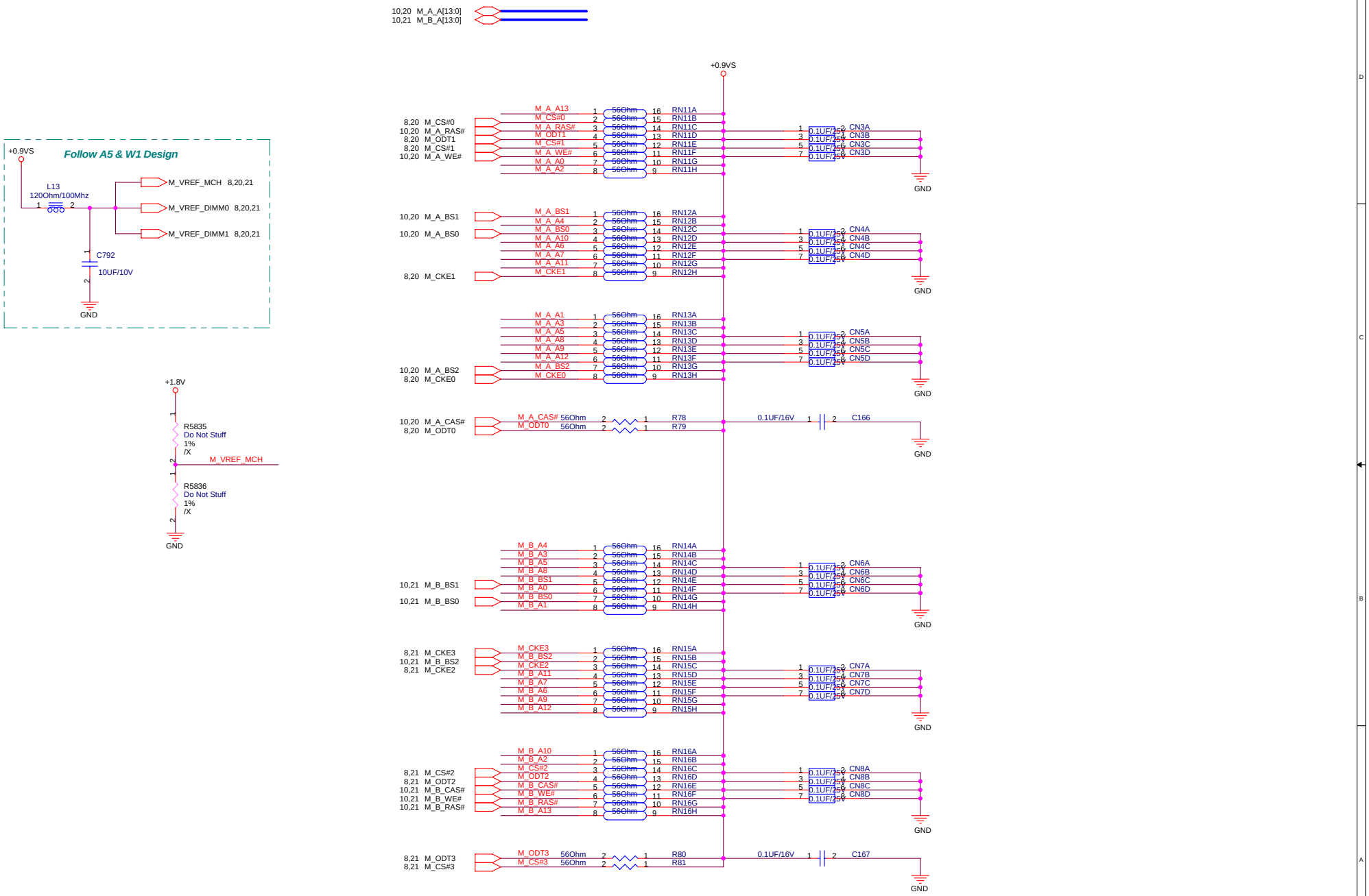
M_B_DQ[63:0] 10

STD Type



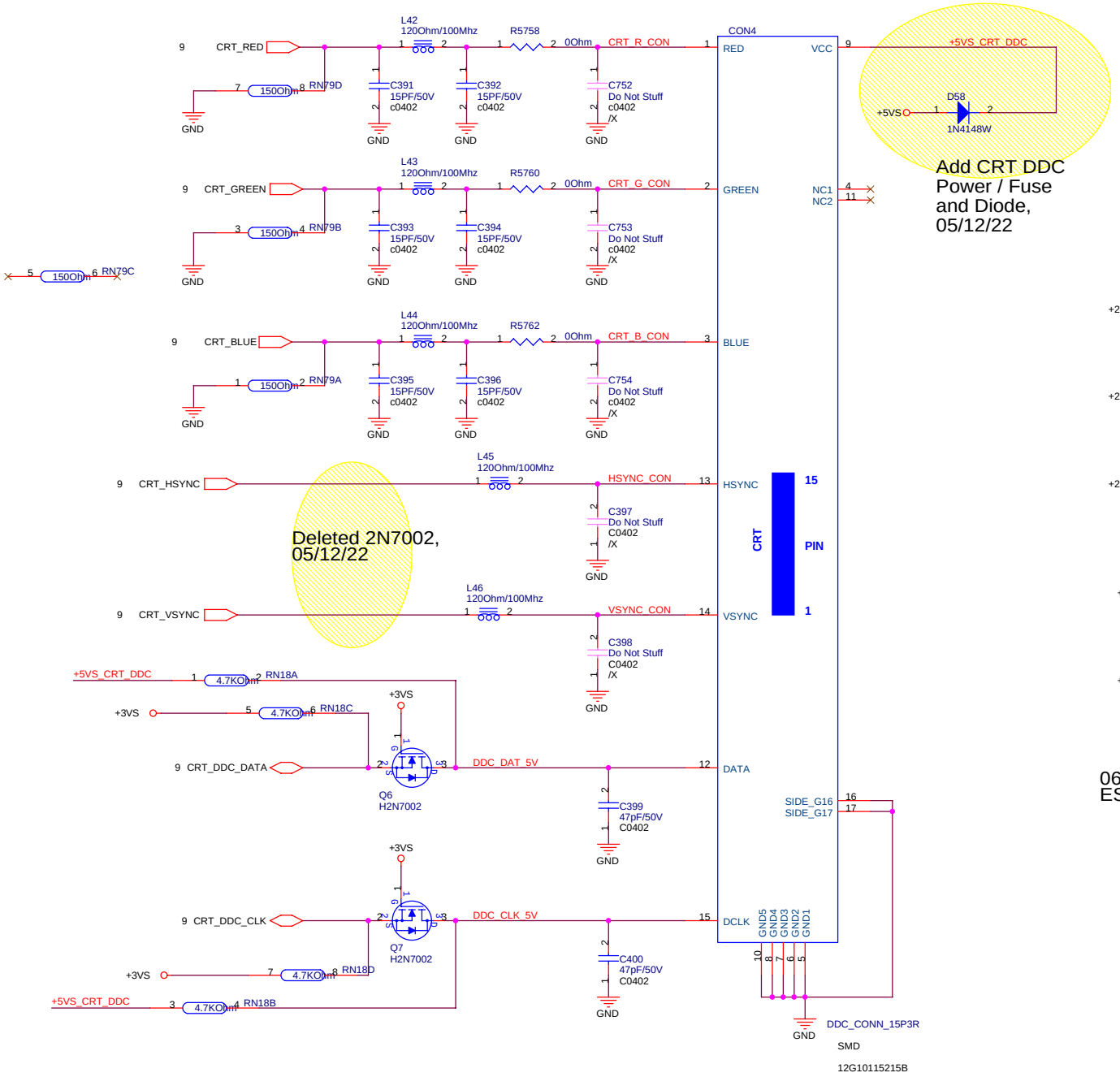
0412Z

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 21 of 96	



0412Z

ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 22 of 96	



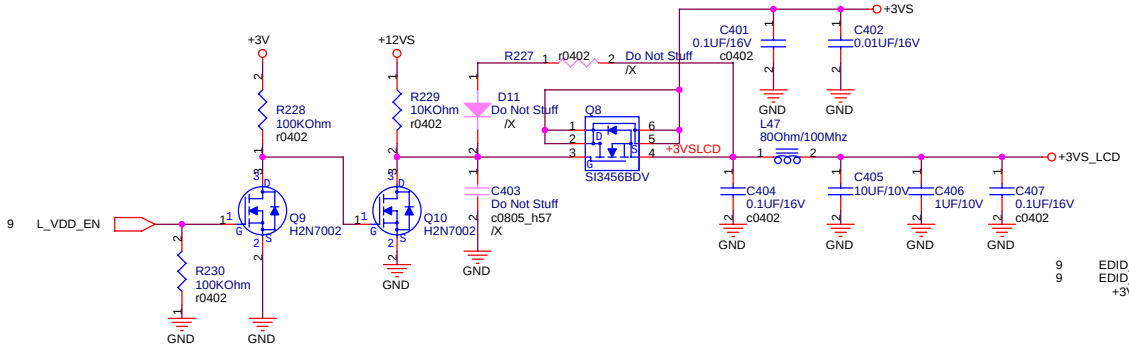
0412Z

ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 32 of 96	

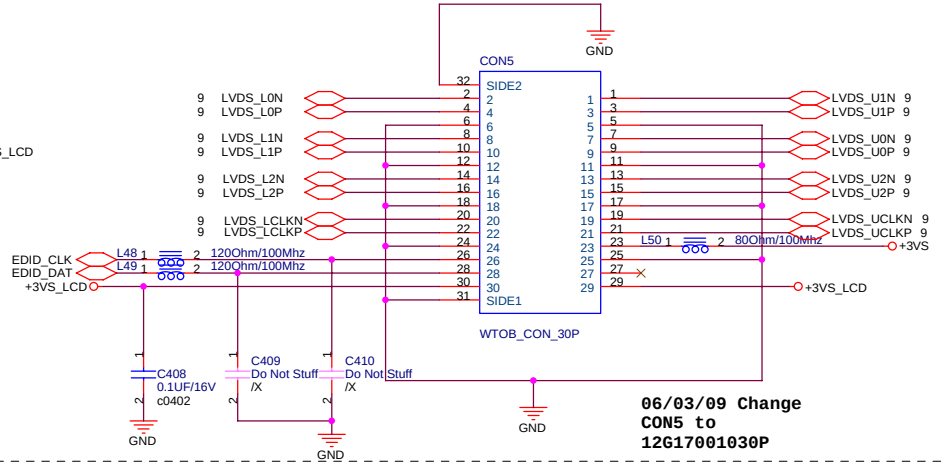
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power



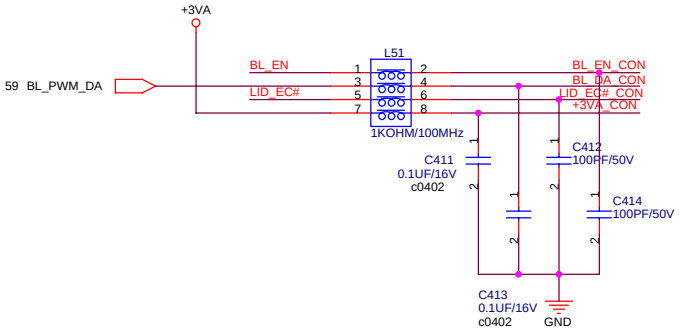
LCD LVDS Interface

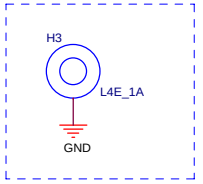


06/03/09 Change CON5 to 12G17001030P

INVERTER Interface/Speaker CONN.

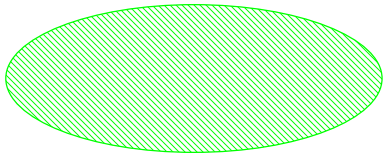
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

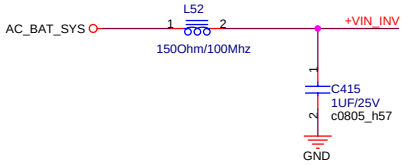


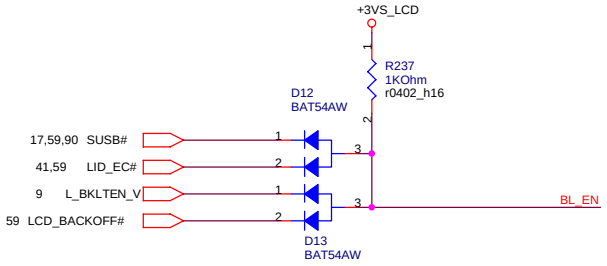


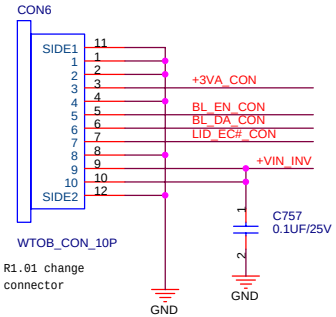
LCD NUT(3.0mm) *1

05/12/30 refer Z96J R1.01 to remove HW pannel ID setting









R1.01 change connector

0412Z

ASUSTeK COMPUTER INC

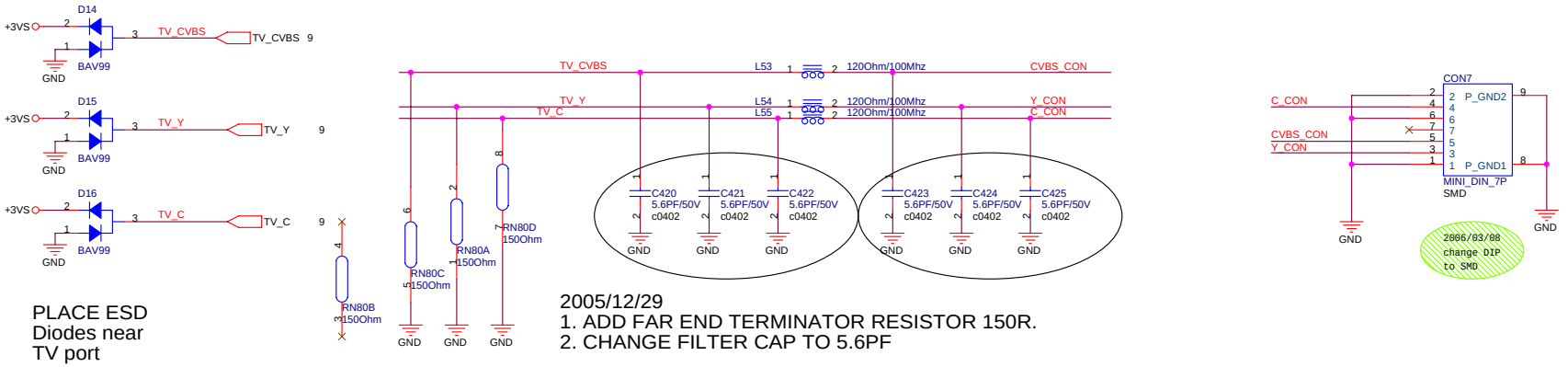
Title : LVDS & INVERTER

Engineer: *Mike Lee*

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 33 of 96

TV OUT



PLACE ESD Diodes near TV port

2005/12/29
1. ADD FAR END TERMINATOR RESISTOR 150R.
2. CHANGE FILTER CAP TO 5.6PF

Max=1200mil Zo=50 Ohm
Chip out 150 Ohm R to 150 Ohm R

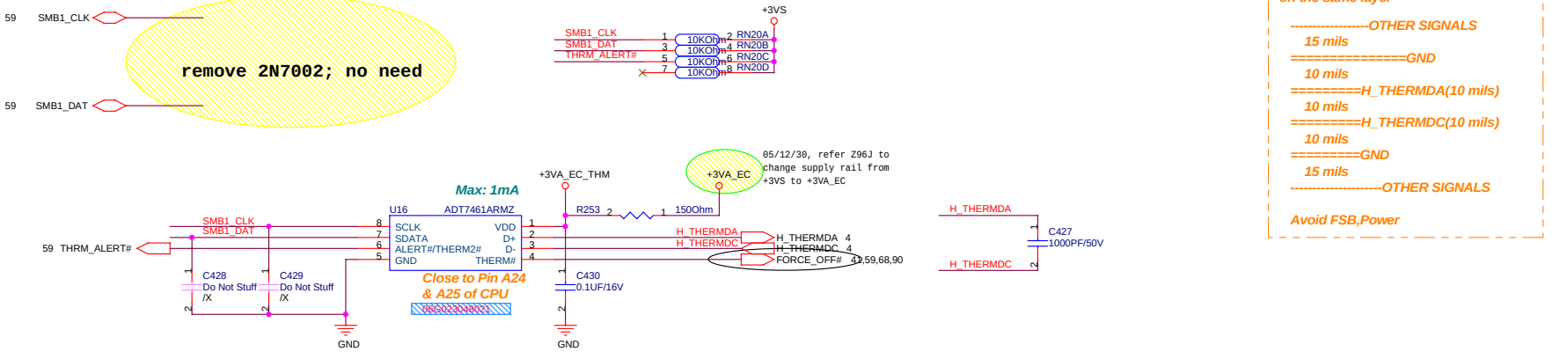
Max=200mil Zo=75 Ohm
150 Ohm R to Filter

Max=500mil Zo=75 Ohm
Filter to TV connector

0412Z

ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 35 of 96	

Thermal Sensor

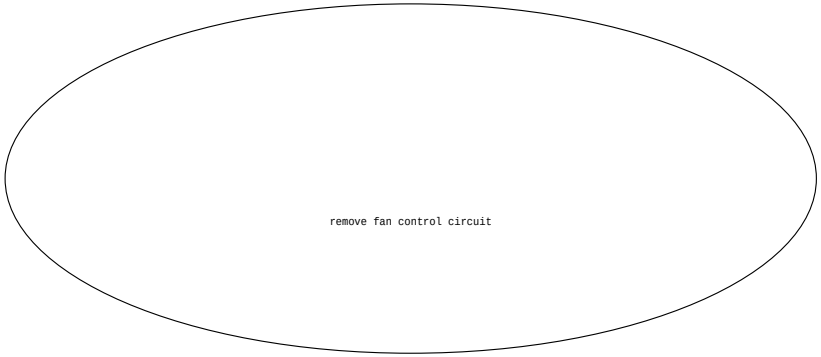


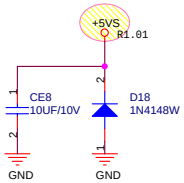
Route H_THERMDA and H_THERMDC on the same layer

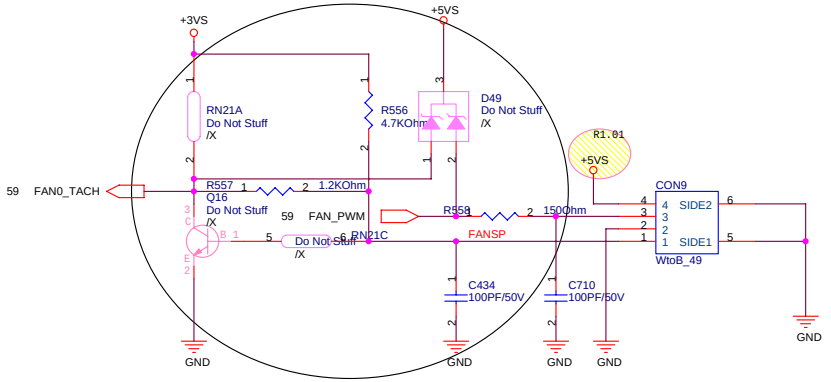
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



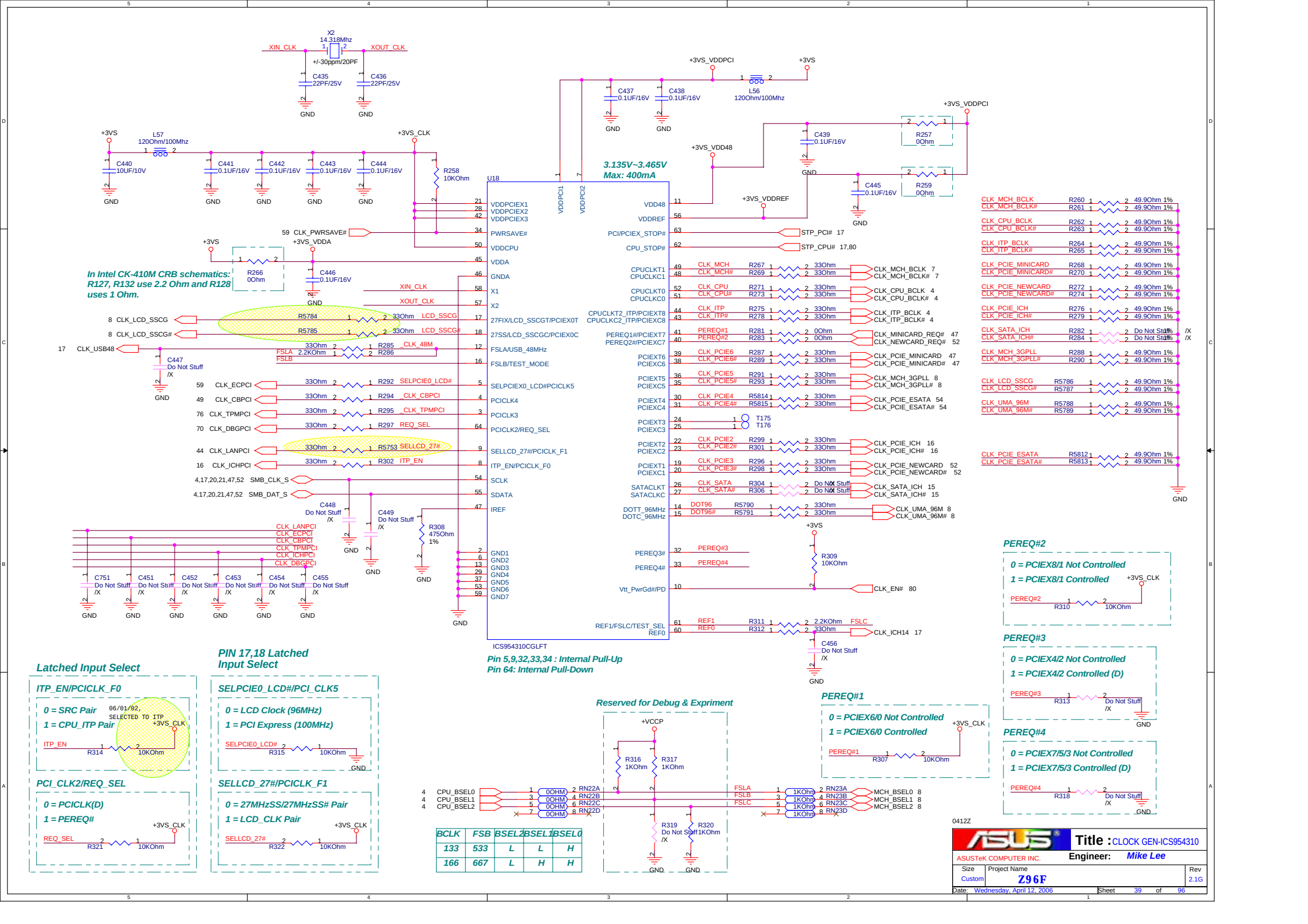


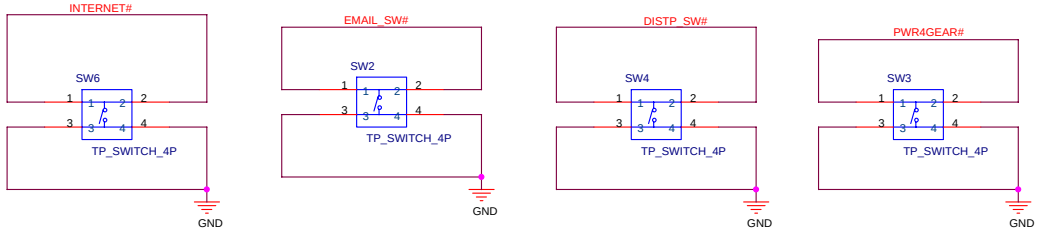


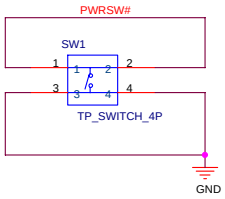
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

0412Z

ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 37 of 96	

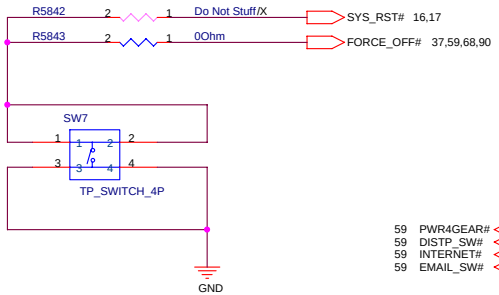

X2
14.318Mhz
XIN_CLK
XOUT_CLK
+/-30ppm/20PF
C435 22PF/25V
C436 22PF/25V
GND
+3VS
L57 120Ohm/100Mhz
+3VS_CLK
C440 10UF/10V
C441 0.1UF/16V
C442 0.1UF/16V
C443 0.1UF/16V
C444 0.1UF/16V
R258 10KOhm
U18
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
ICS954310CGLFT
59 CLK_PWRSAVE#
+3VS_VDDA
R266 0Ohm
C446 0.1UF/16V
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128 uses 1 Ohm.
8 CLK_LCD_SSCG
8 CLK_LCD_SSCG#
R5784 33Ohm LCD_SSCG
R5785 33Ohm LCD_SSCG#
17 CLK_USB48
R285 CLK_48M
FSLA 2.2KOhm
R286
C447 Do Not Stuff /X
59 CLK_ECPCI R292 SELPCIE0_LCD#
49 CLK_CBPCI R294 CLK_CBPCI
76 CLK_TPMPCI R295 CLK_TPMPCI
70 CLK_DBGPCI R297 REQ_SEL
44 CLK_LANPCI R5753 SELLCD_27#
16 CLK_ICHPCI R302 ITP_EN
4,17,20,21,47,52 SMB_CLK_S
4,17,20,21,47,52 SMB_DAT_S
C448 Do Not Stuff /X
C449 Do Not Stuff /X
R308 475Ohm 1%
C751 Do Not Stuff /X
C451 Do Not Stuff /X
C452 Do Not Stuff /X
C453 Do Not Stuff /X
C454 Do Not Stuff /X
C455 Do Not Stuff /X
+3VS_VDDPCI
L56 120Ohm/100Mhz
C437 0.1UF/16V
C438 0.1UF/16V
3.135V~3.465V
Max: 400mA
+3VS_VDD48
C439 0.1UF/16V
R257 0Ohm
+3VS_VDDREF
C445 0.1UF/16V
R259 0Ohm
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
STP_PCI# 17
STP_CPU# 17,80
CPUCLKT1 CPUCLKC1
CPUCLKT0 CPUCLKC0
CPUCLKT2_ITP/PCIEXT8 CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7 PEREQ2#/PCIEXC7
PCIEXT6 PCIEXC6
PCIEXT5 PCIEXC5
PCIEXT4 PCIEXC4
PCIEXT3 PCIEXC3
PCIEXT2 PCIEXC2
PCIEXT1 PCIEXC1
SATACLKT SATACLKC
DOTT_96MHz DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
CLK_EN# 80
CLK_ICH14 17
C456 Do Not Stuff /X
T175
T176
R309 10KOhm
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
CLK_MCH_BCLK R260 49.9Ohm 1%
CLK_MCH_BCLK# R261 49.9Ohm 1%
CLK_CPU_BCLK R262 49.9Ohm 1%
CLK_CPU_BCLK# R263 49.9Ohm 1%
CLK_ITP_BCLK R264 49.9Ohm 1%
CLK_ITP_BCLK# R265 49.9Ohm 1%
CLK_PCIE_MINICARD R268 49.9Ohm 1%
CLK_PCIE_MINICARD# R270 49.9Ohm 1%
CLK_PCIE_NEWCARD R272 49.9Ohm 1%
CLK_PCIE_NEWCARD# R274 49.9Ohm 1%
CLK_PCIE_ICH R276 49.9Ohm 1%
CLK_PCIE_ICH# R279 49.9Ohm 1%
CLK_SATA_ICH R282 Do Not Stuff 1% /X
CLK_SATA_ICH# R284 Do Not Stuff 1% /X
CLK_MCH_3GPLL R288 49.9Ohm 1%
CLK_MCH_3GPLL# R290 49.9Ohm 1%
CLK_LCD_SSCG R5786 49.9Ohm 1%
CLK_LCD_SSCG# R5787 49.9Ohm 1%
CLK_UMA_96M R5788 49.9Ohm 1%
CLK_UMA_96M# R5789 49.9Ohm 1%
CLK_PCIE_ESATA R5812 49.9Ohm 1%
CLK_PCIE_ESATA# R5813 49.9Ohm 1%
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
06/01/02 SELECTED TO ITP
R314 10KOhm
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
REQ_SEL R321 10KOhm
PIN 17,18 Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
SELPCIE0_LCD# R315 10KOhm
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
SELLCD_27# R322 10KOhm
Reserved for Debug & Expriment
+VCCP
R316 1KOhm
R317 1KOhm
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
0OHM RN22A RN22B RN22C RN22D
FSLA FSLB FSLC
1KOhm RN23A RN23B RN23C RN23D
MCH_BSEL0 MCH_BSEL1 MCH_BSEL2
R319 Do Not Stuff /X
R320 1KOhm
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#2 R310 10KOhm
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#3 R313 Do Not Stuff /X
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#1 R307 10KOhm
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
PEREQ#4 R318 Do Not Stuff /X
0412Z
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC.
Engineer: Mike Lee
Size Custom
Project Name Z96F
Rev 2.1G
Date: Wednesday, April 12, 2006
Sheet 39 of 96

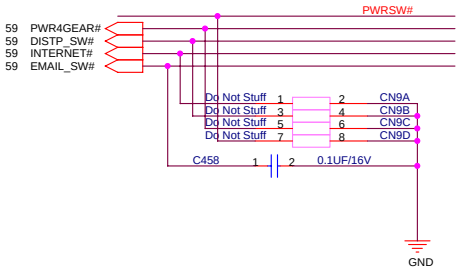


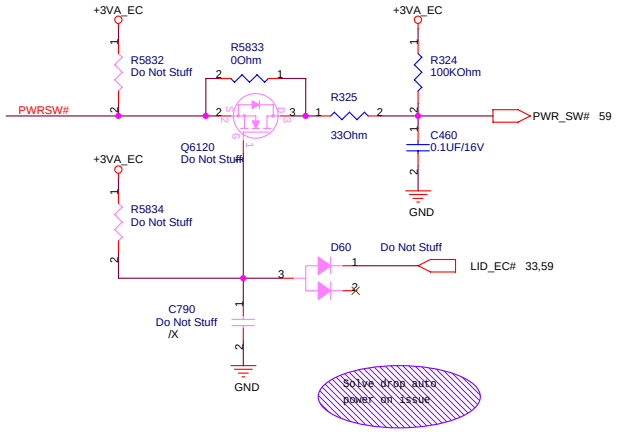


06/03/09 Change SW1-4, SW6-7 to 12G09103004P

SHUT_DOWN# / RESET#

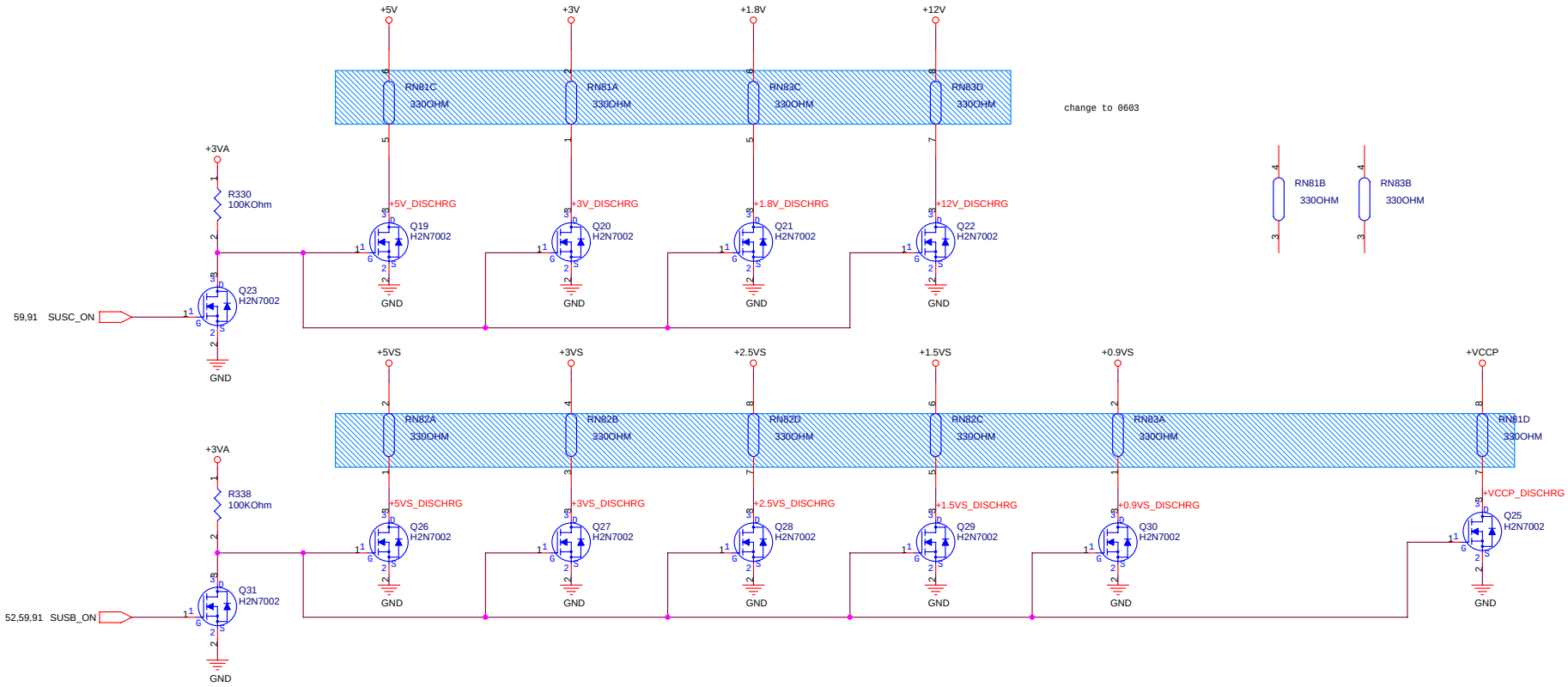






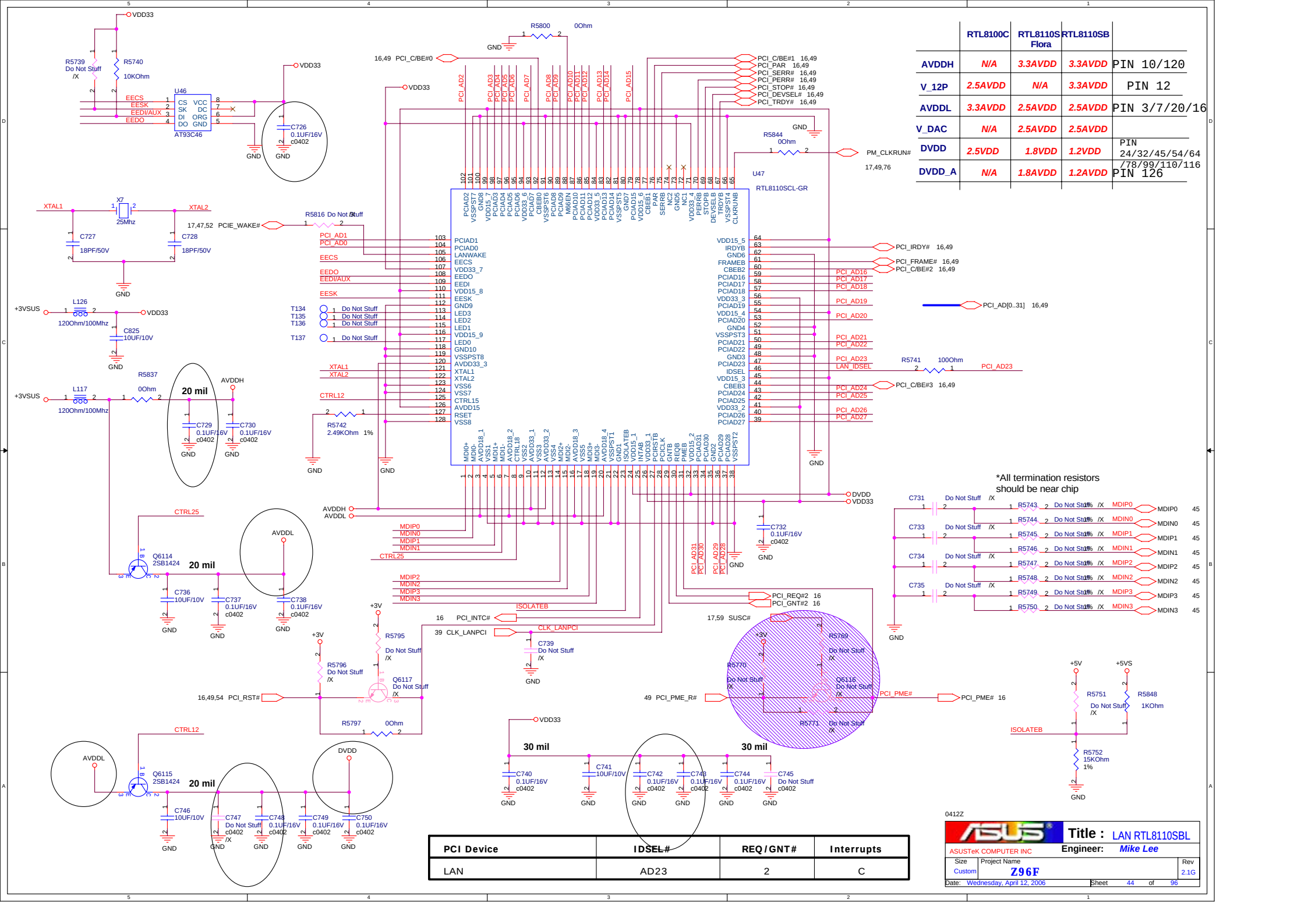
0412Z

ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 41 of 96	



0412Z

ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 42 of 96	



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	2	C

0412Z

ASUSTeK COMPUTER INC

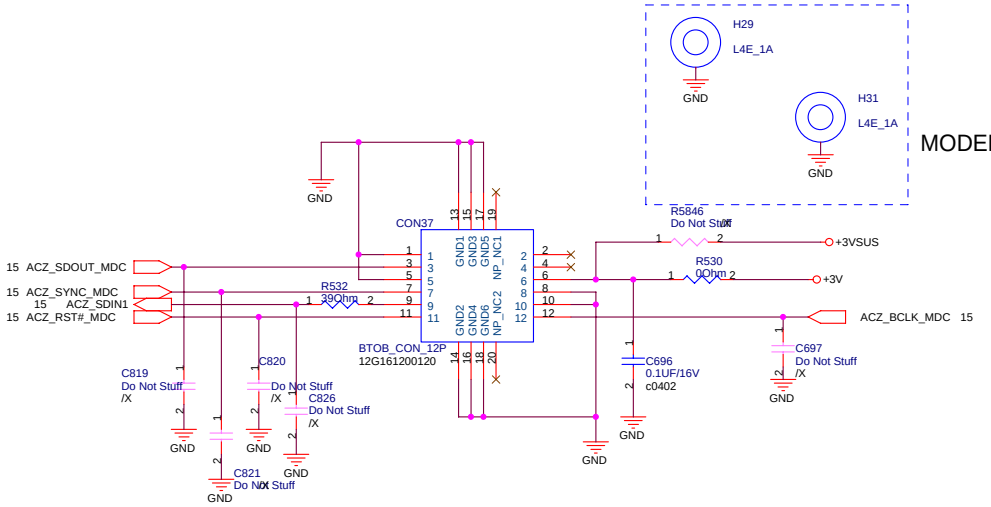
Title : LAN RTL8110SBL

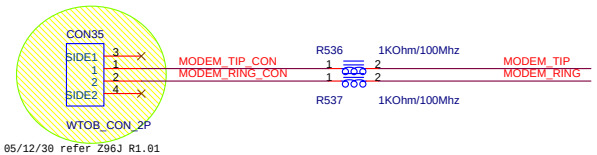
Engineer: Mike Lee

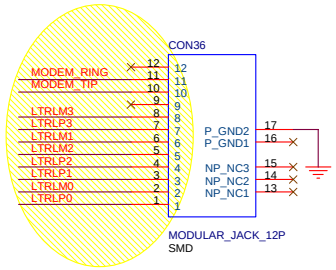
Size	Project Name	Rev
Custom	Z96F	2.1G

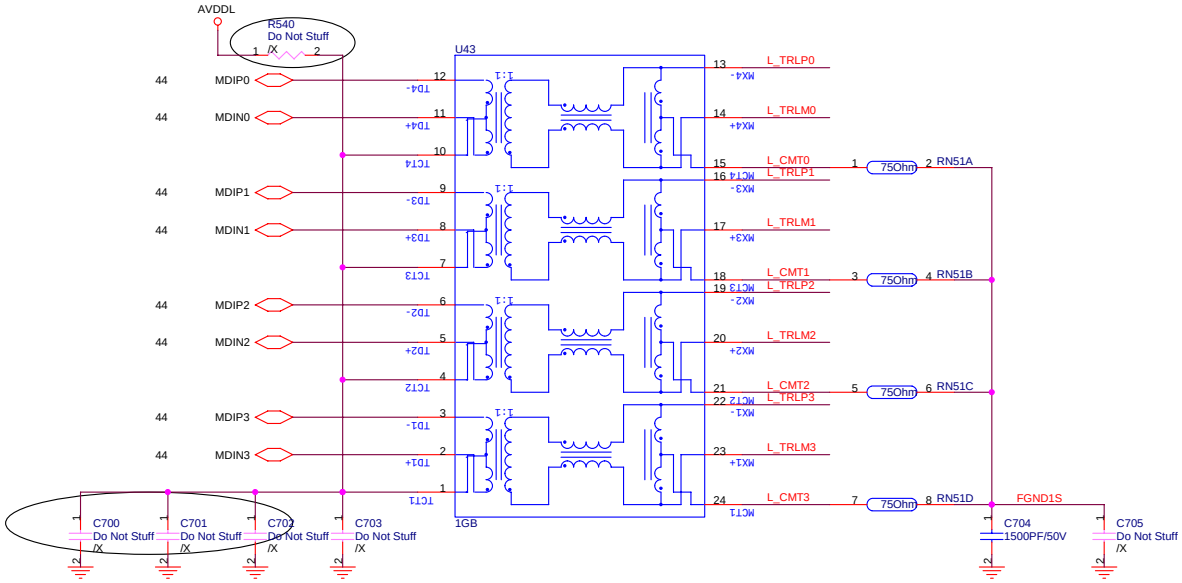
Date: Wednesday, April 12, 2006 Sheet 44 of 96

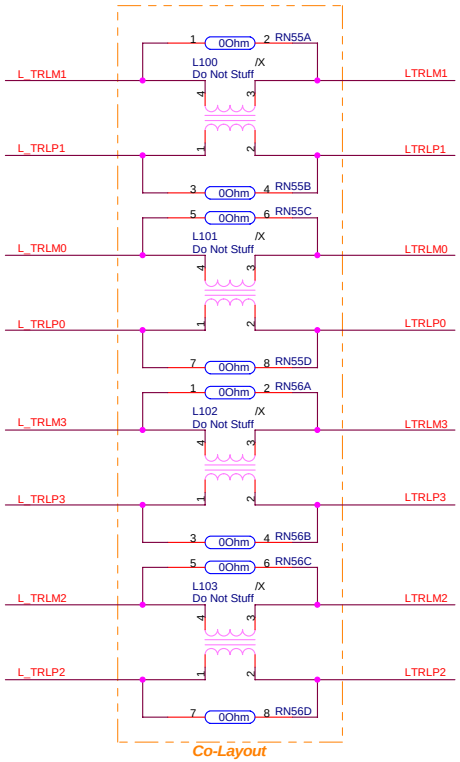
MDC CONN.





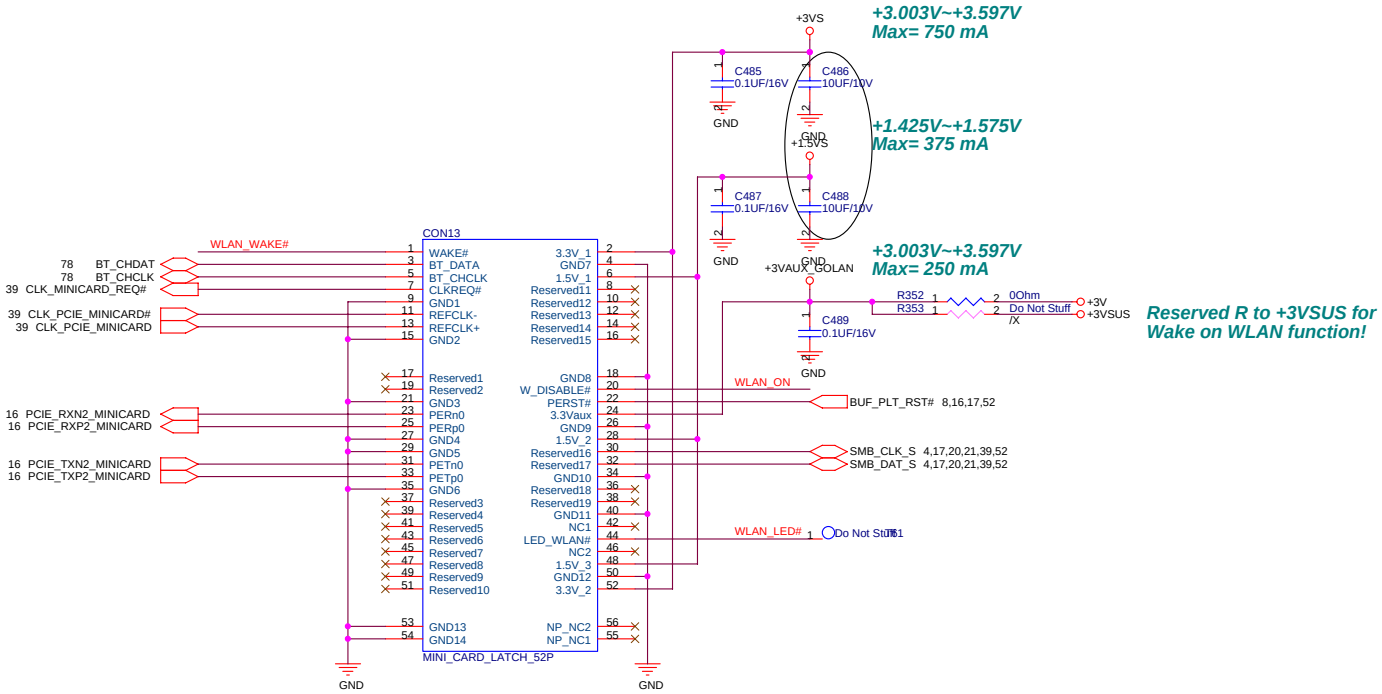




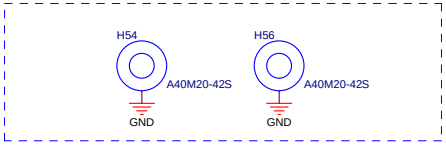


0412Z

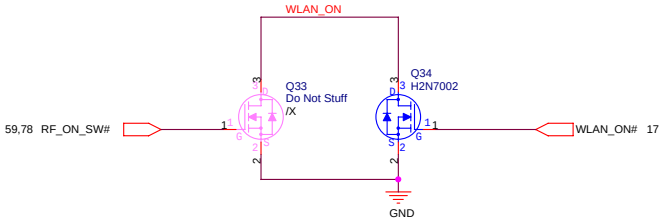
ASUSTeK COMPUTER INC.	Title : RJ45&RJ11	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 45 of 96	

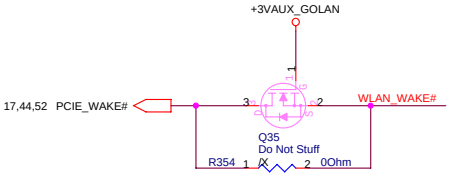


2006/03/31



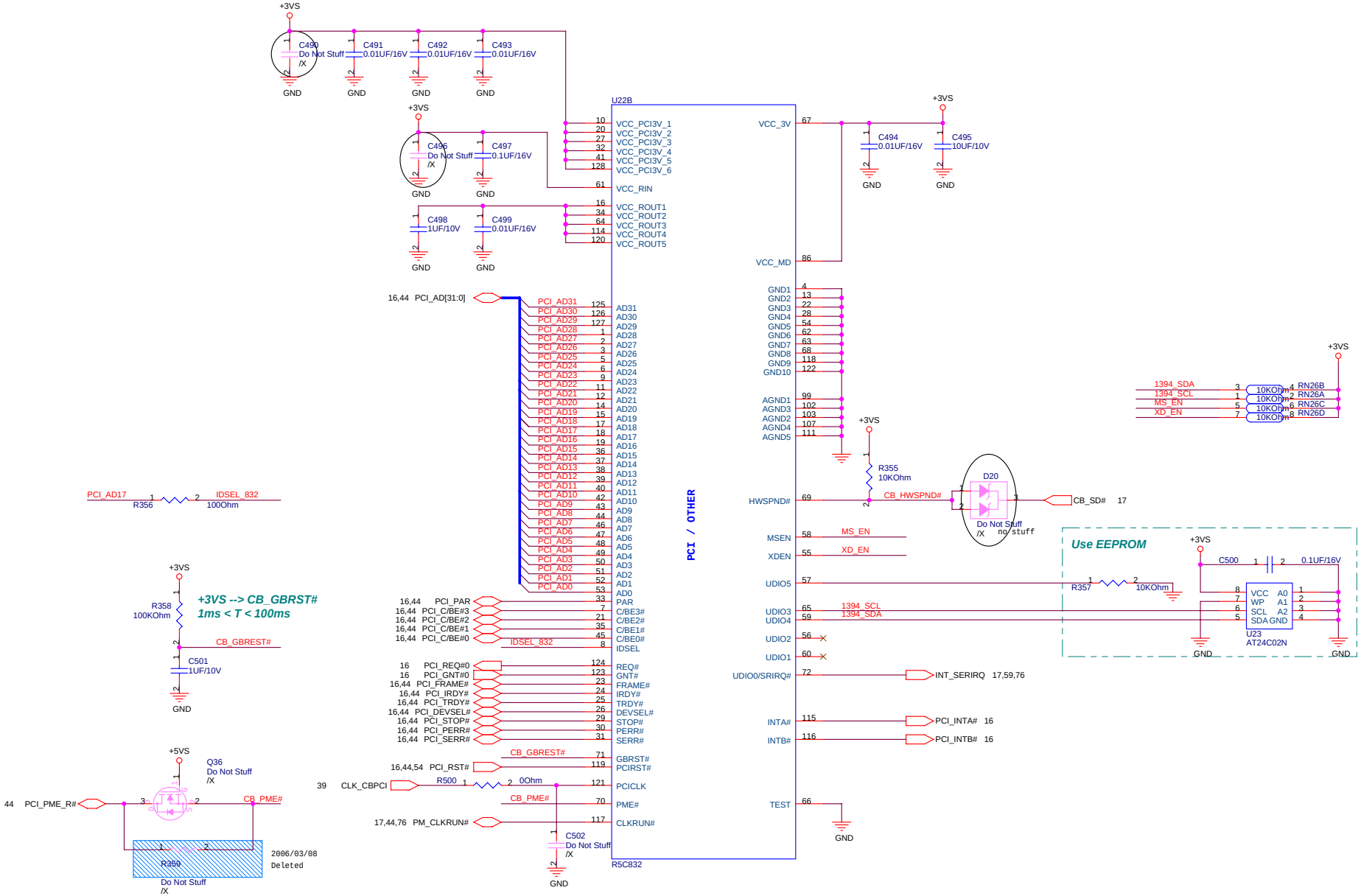
MINI CARD NUT(4.2mm) *2





0412Z

ASUSTeK COMPUTER INC.	Title : MINICARD	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 47 of 96	



PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A

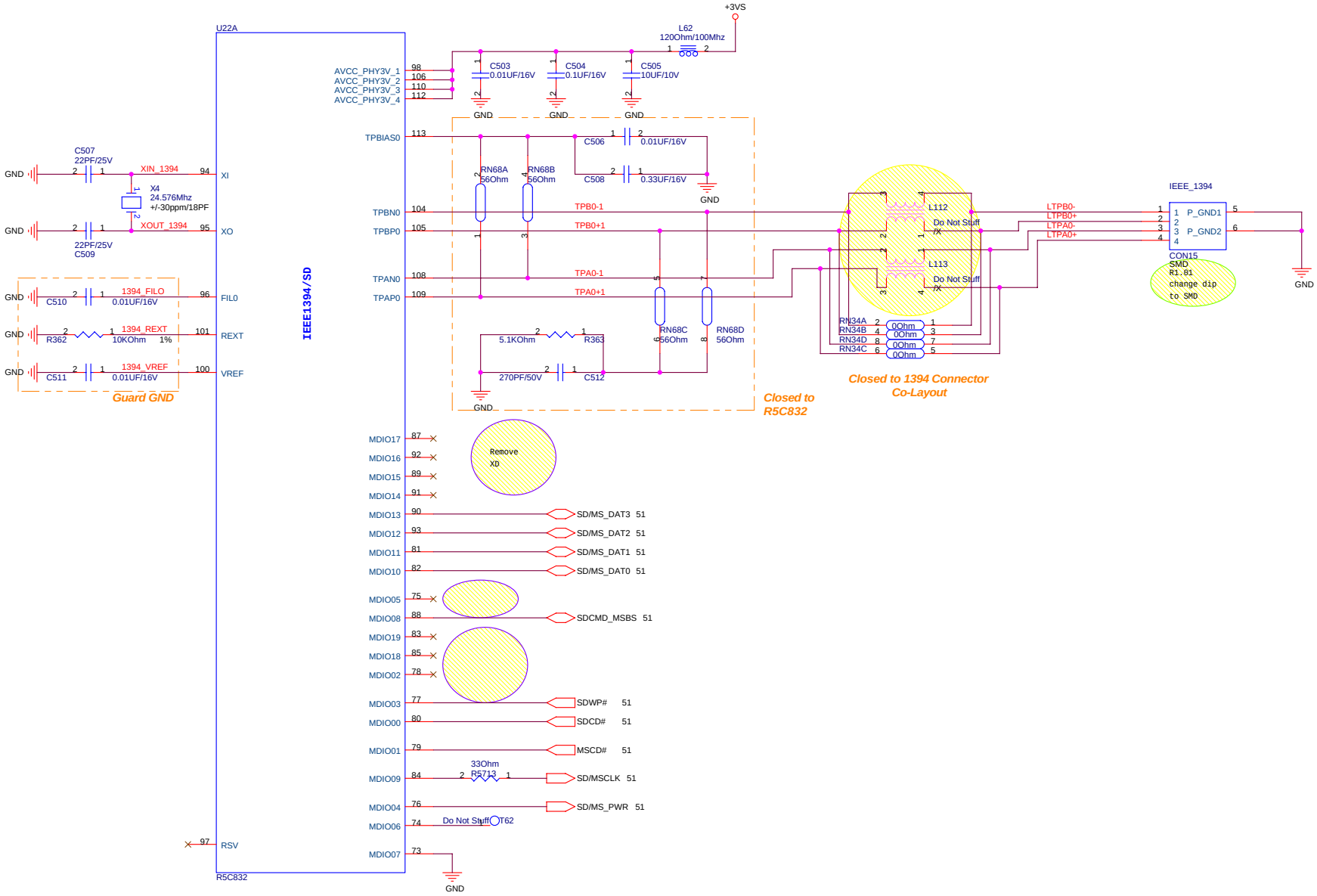
0412Z

Title : CARD1394-R5C832(1)

ASUSTeK COMPUTER INC. MB6 Engineer: Mike Lee

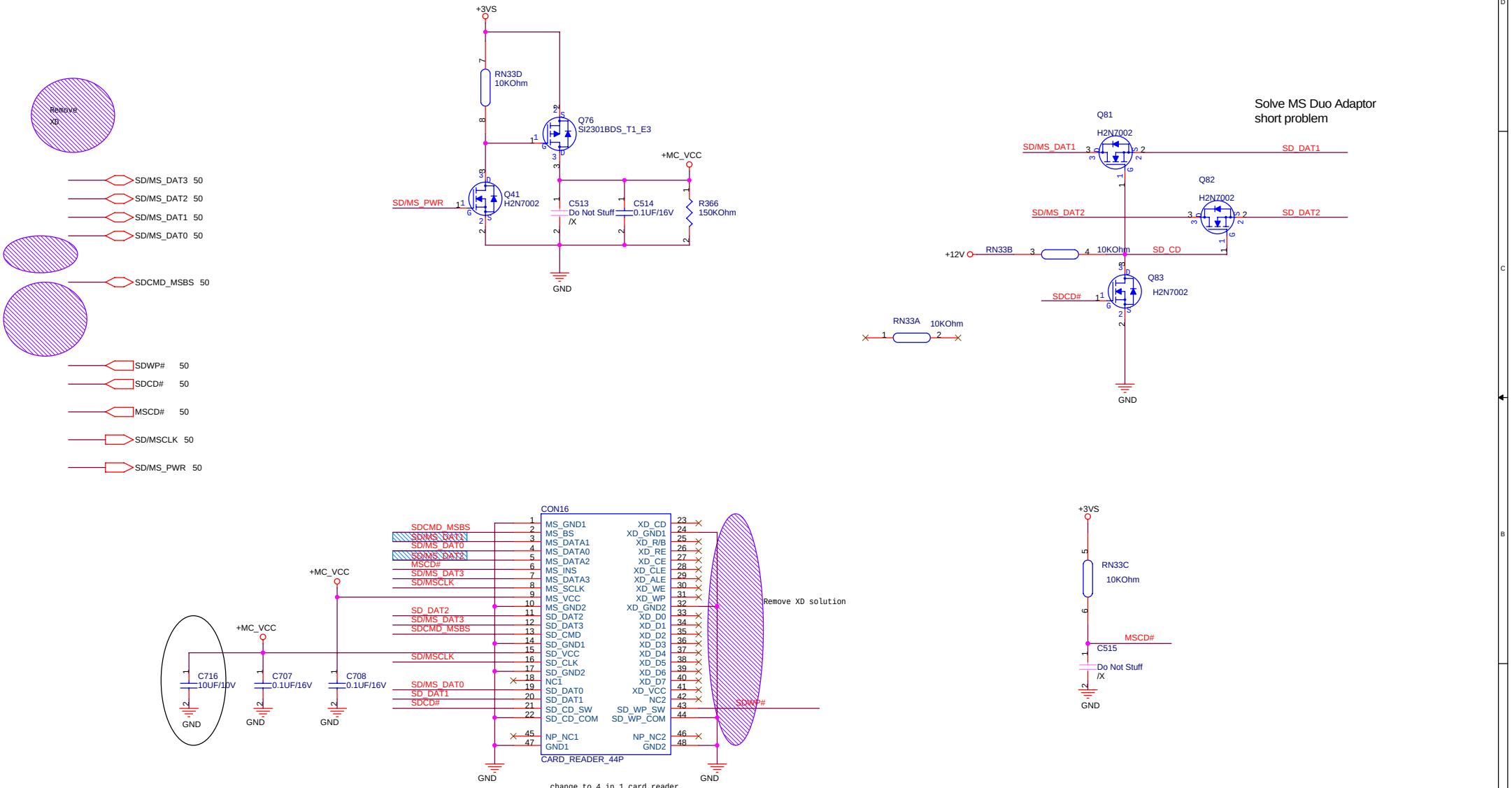
Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 49 of 96



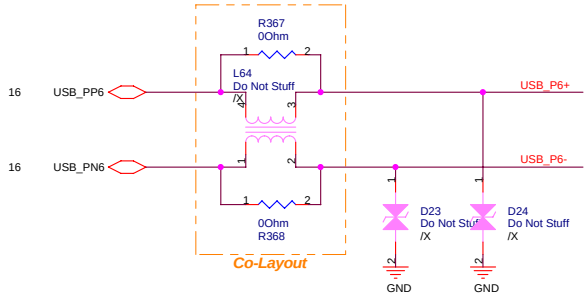
0412Z

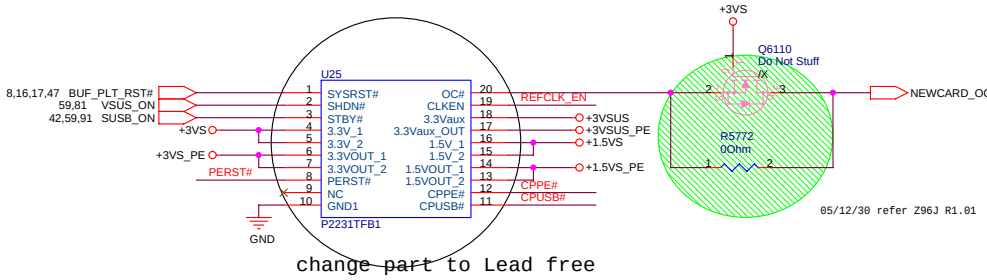
Title : CARD1394-R5C832(2)		
ASUSTeK COMPUTER INC. MB6	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 50 of 96	

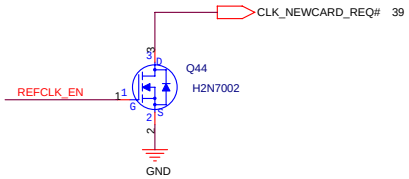


0412Z

ASUSTeK COMPUTER INC	Title : 4 in 1 CARD READER	
	Engineer: Mike Lee	
Size: A3	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 51 of 96	

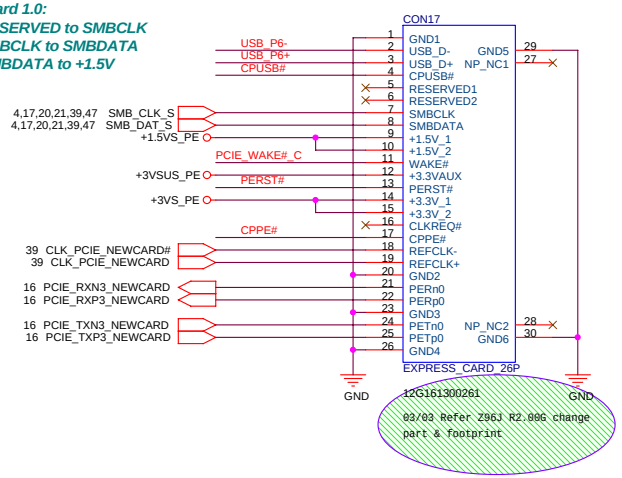


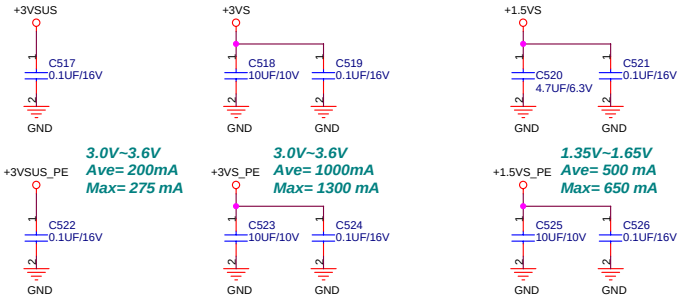


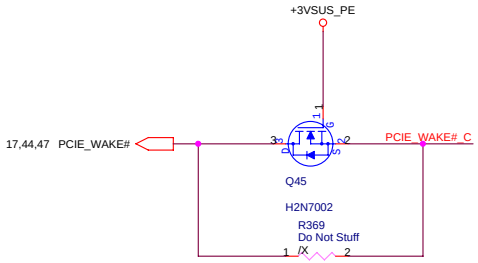


!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

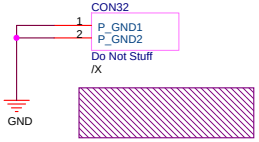
NewCard Header





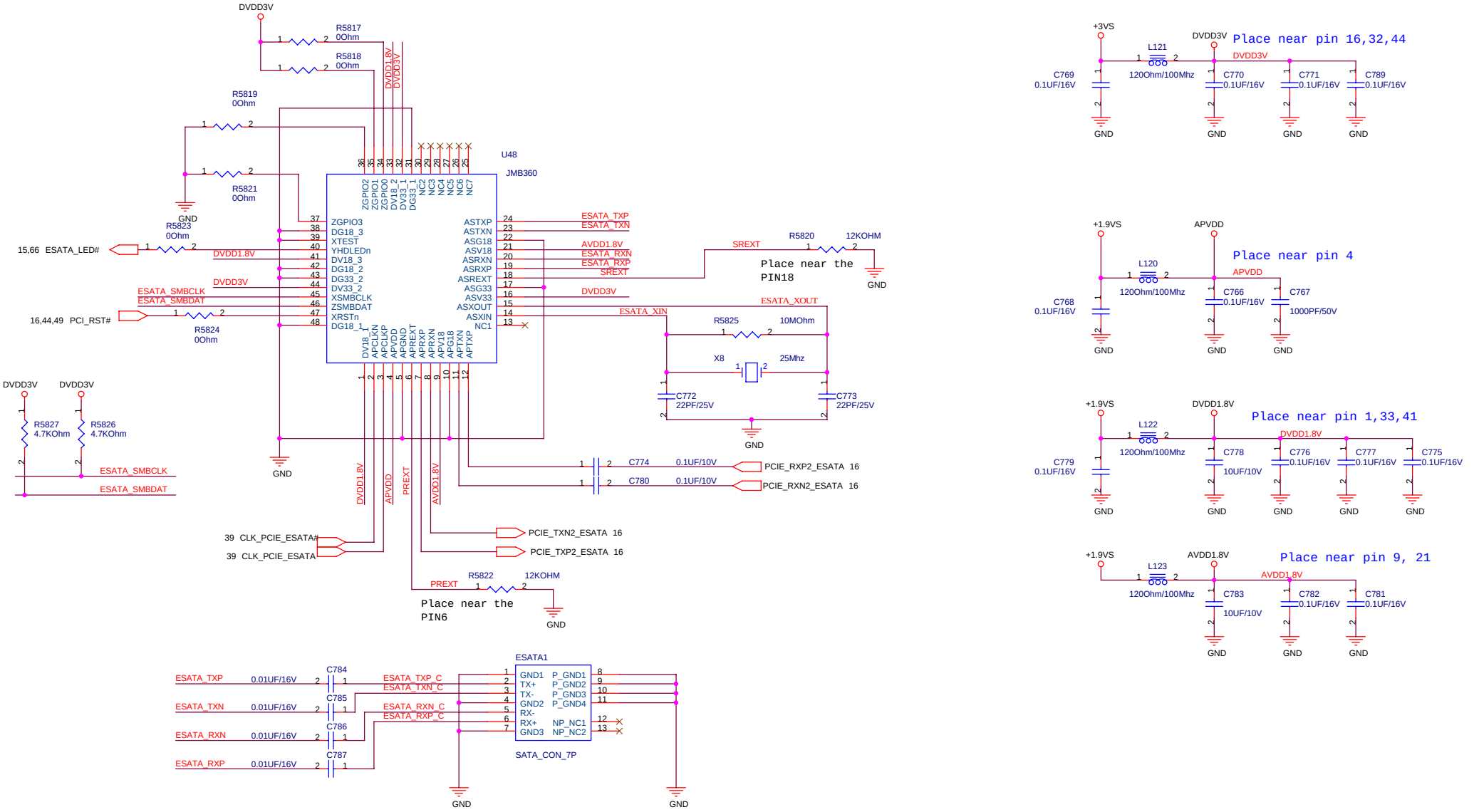


NewCard Ejecter



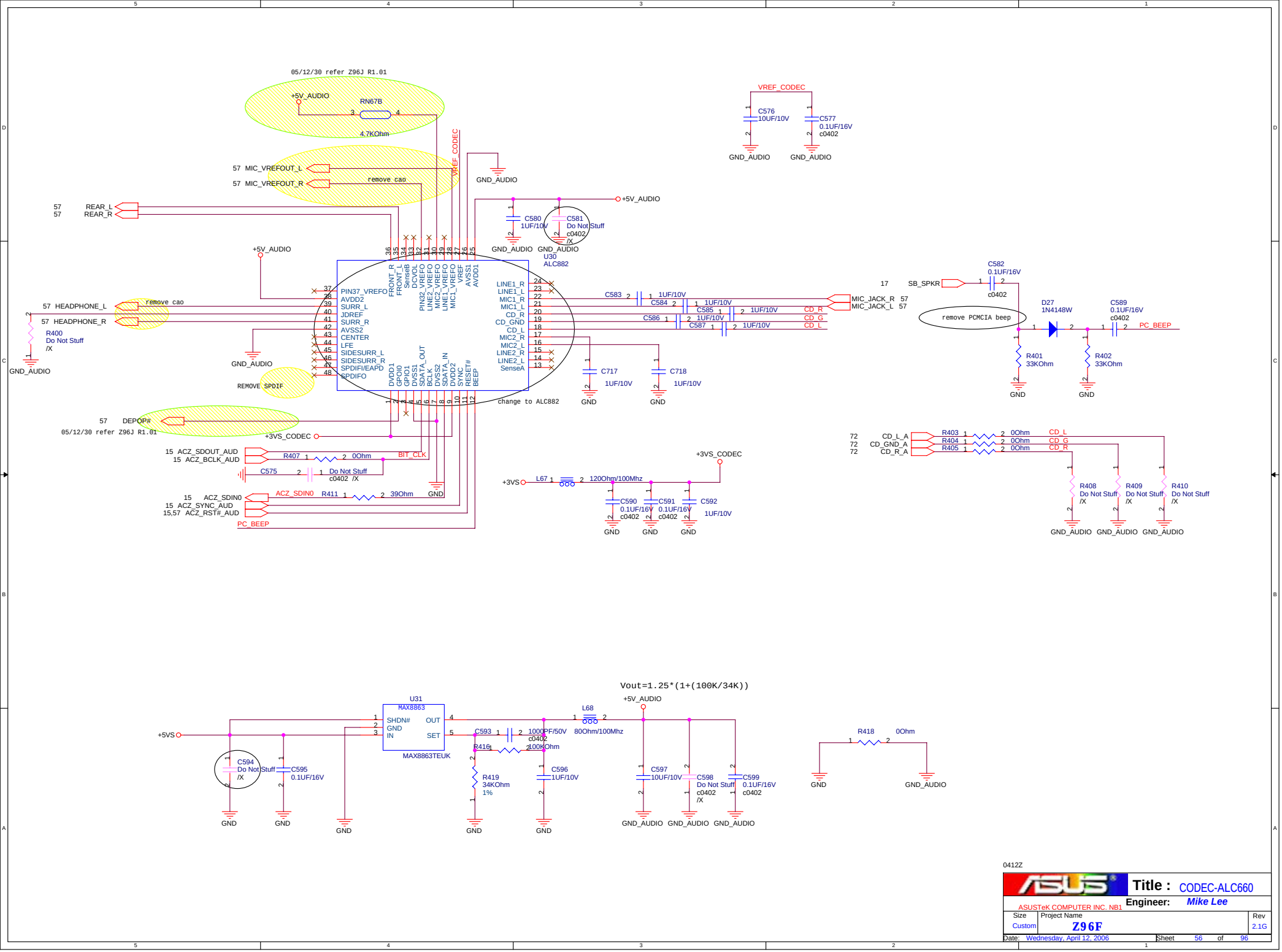
0412Z

ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 52 of 96	



0412Z

ASUSTeK COMPUTER INC	Title : ESATA	
	Engineer: Mike Lee	
Size: A3	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 54 of 96	



0412Z

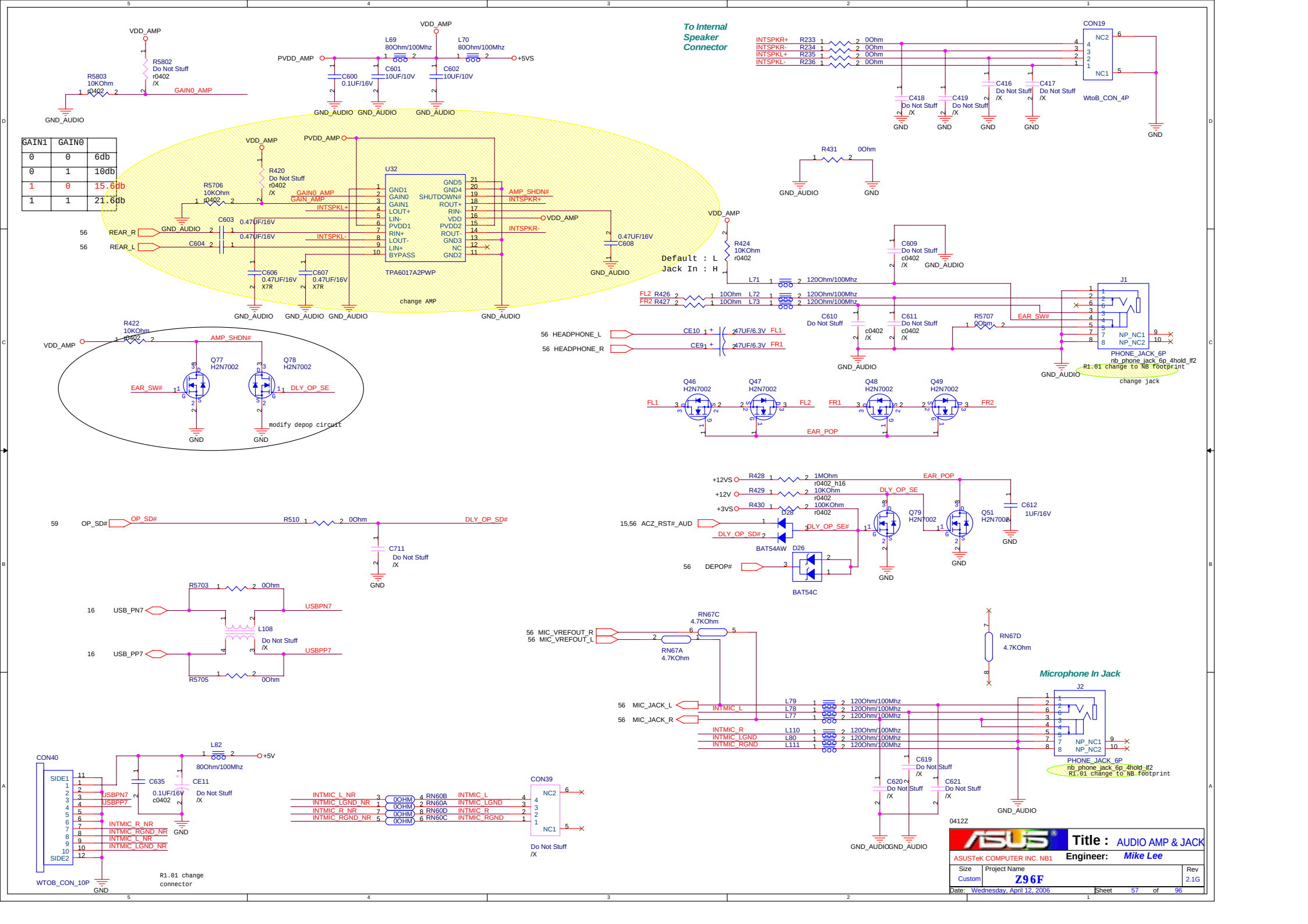
Title : CODEC-ALC660

Engineer: Mike Lee

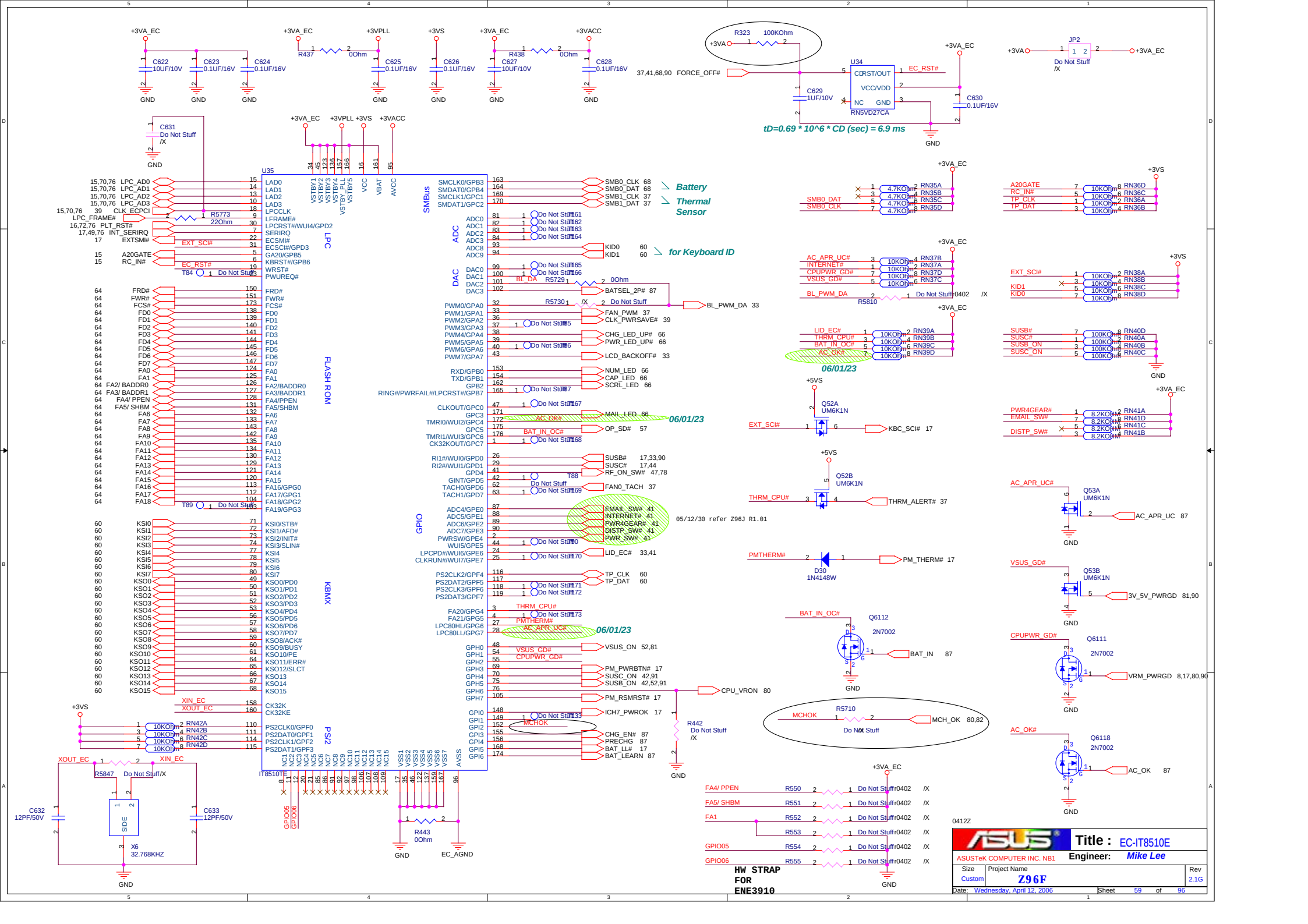
ASUSTeK COMPUTER INC. NB1

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 56 of 96



GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db


U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
ADC
DAC
SMBus
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
06/01/23
05/12/30 refer Z96J R1.01
HW STRAP FOR ENE3910
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Mike Lee
Project Name Z96F
Size Custom
Rev 2.1G
Date: Wednesday, April 12, 2006
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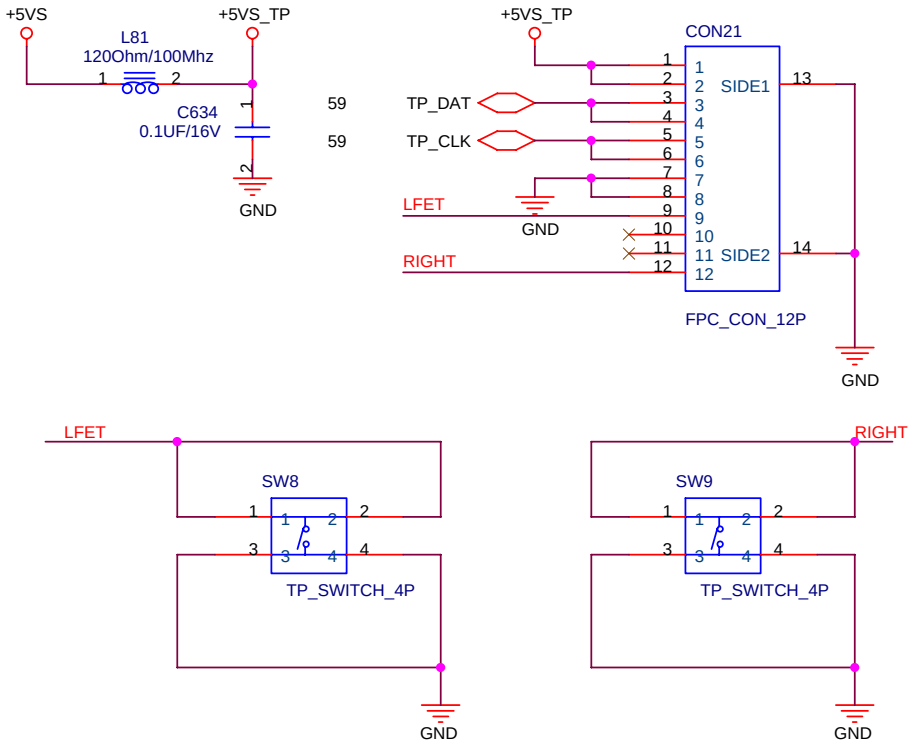
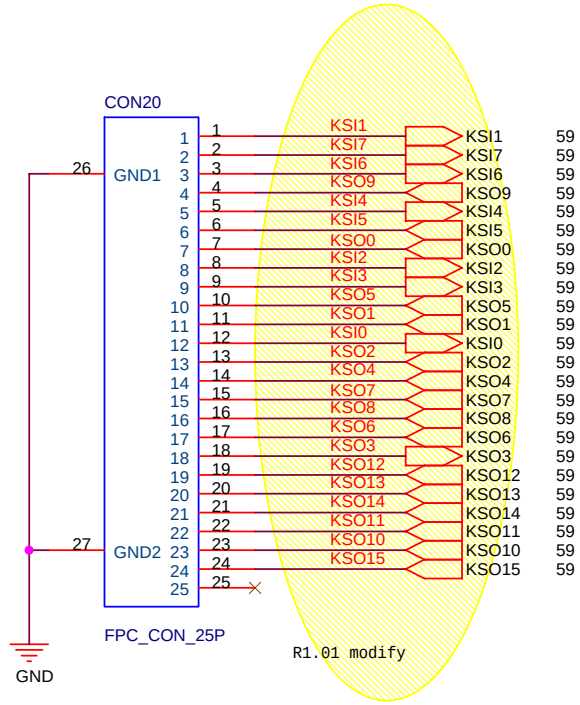
0412Z

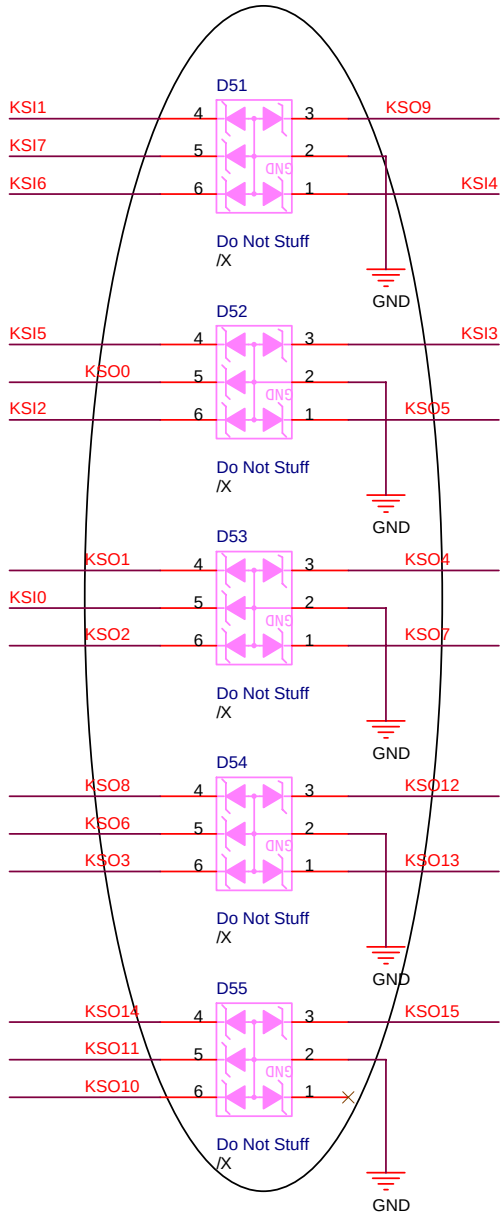
For Touch-Pad

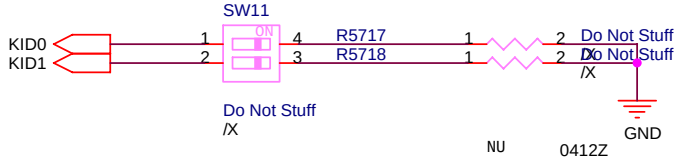


For Keyboard

05/12/29 ESD DIODE PIN SWAPPED



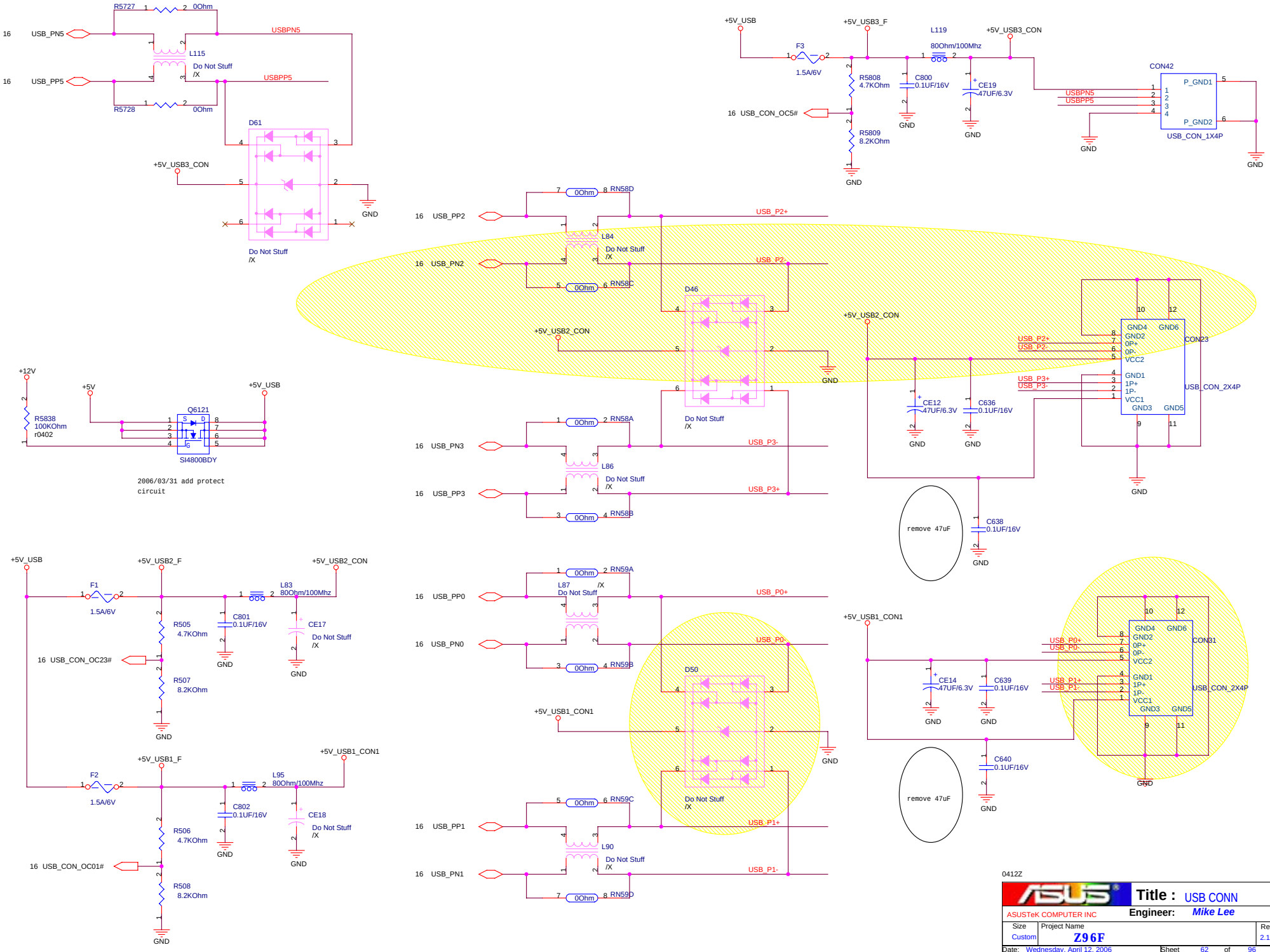




NU

0412Z

ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: Mike Lee	
Size: A4	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 60 of 96	



0412Z

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 62 of 96	

ISA ROM

R1.01 bom add bios rom

EC Hardware Strapping

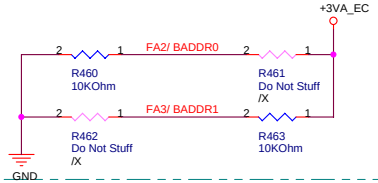
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

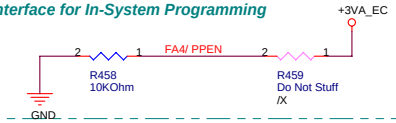


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

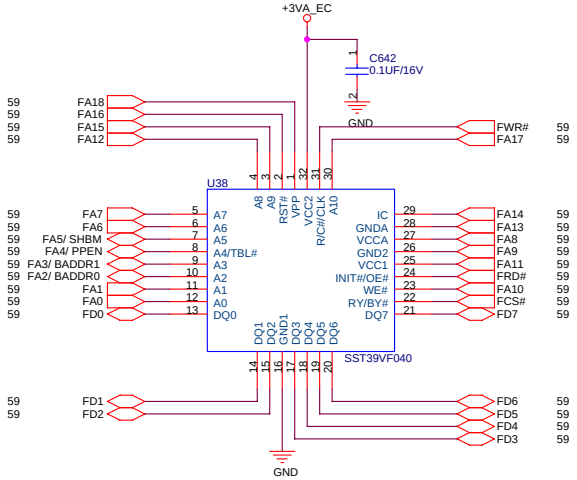
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

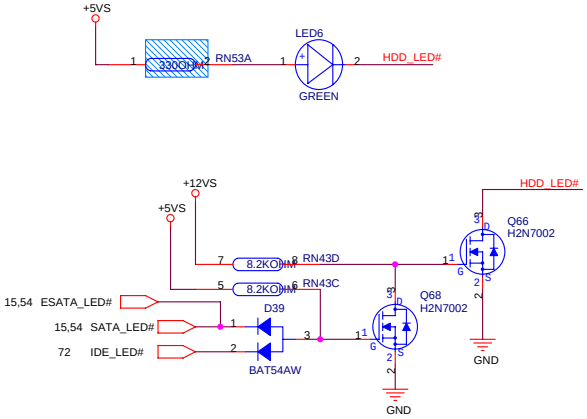


0412Z

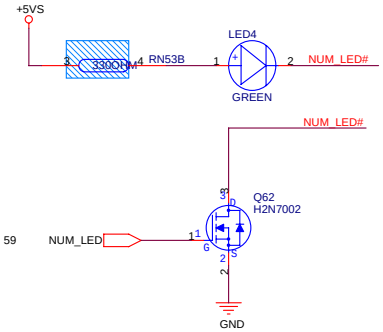
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 64 of 96	

For LED

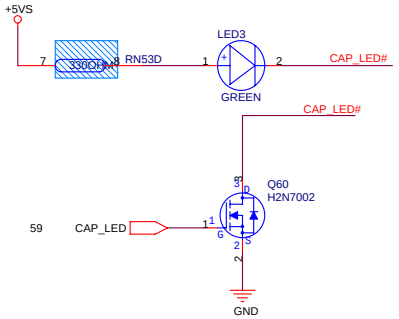
For SATA/IDE LED



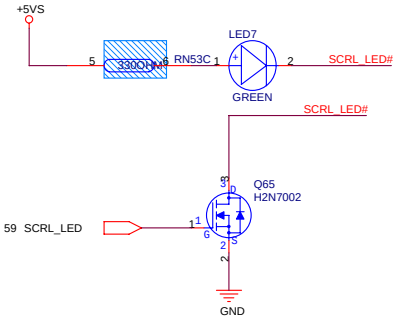
for Num Lock



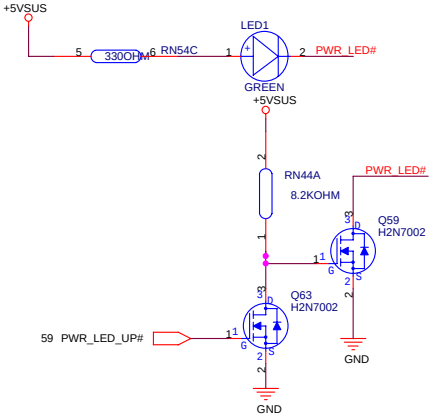
for Cap. Lock



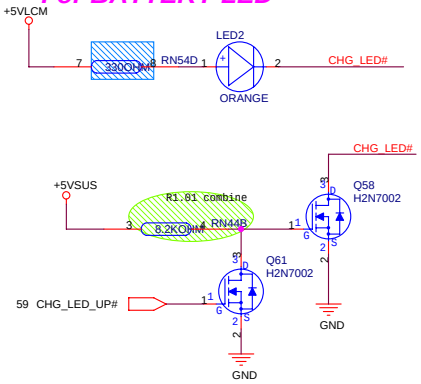
for Scroll Lock



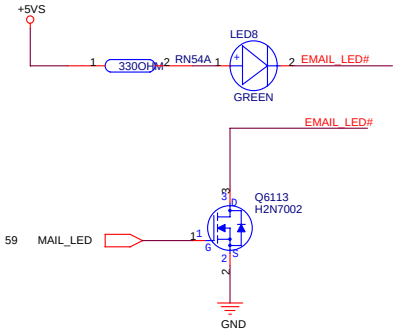
For POWER LED



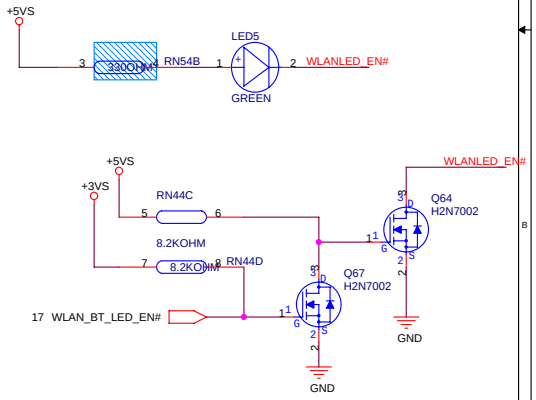
For BATTERY LED



for email



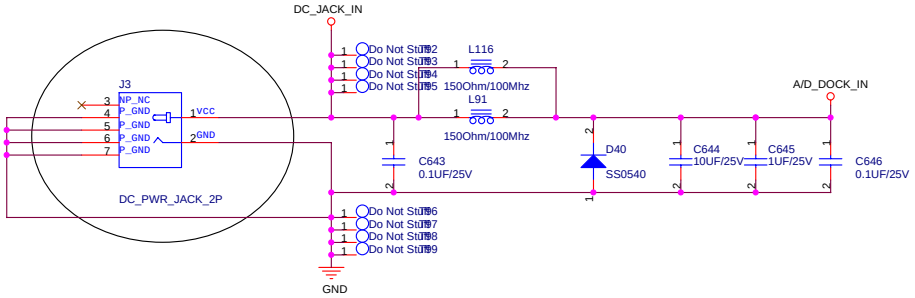
For WireLess LED



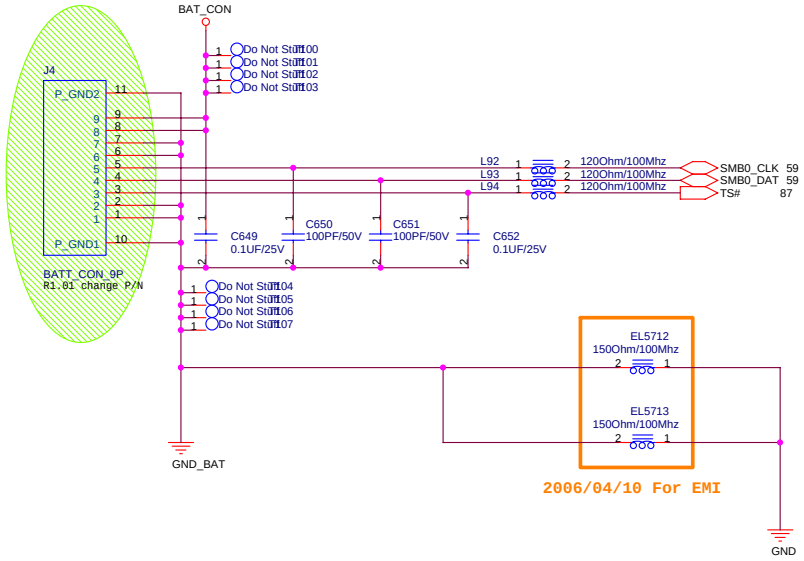
0412Z

ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 66 of 96	

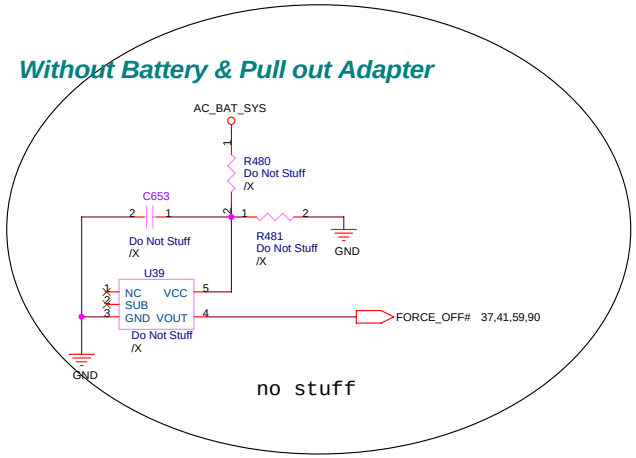
DC IN



BAT IN



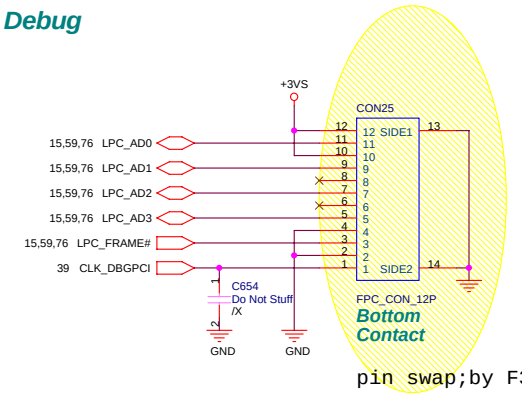
Without Battery & Pull out Adapter



0412Z

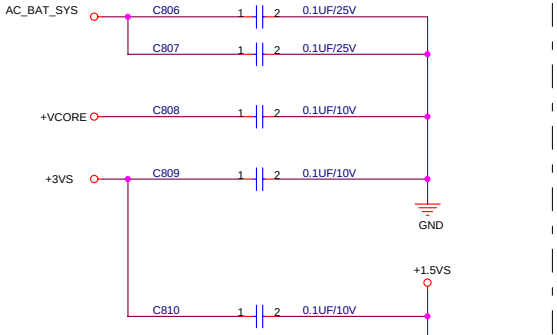
ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 68 of 96	

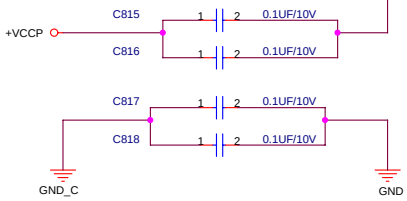
For Debug



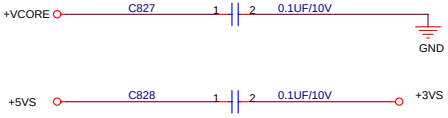
pin swap;by F3J

2006/04/04 Add Stitch caps





2006/04/08 Add Stitch caps

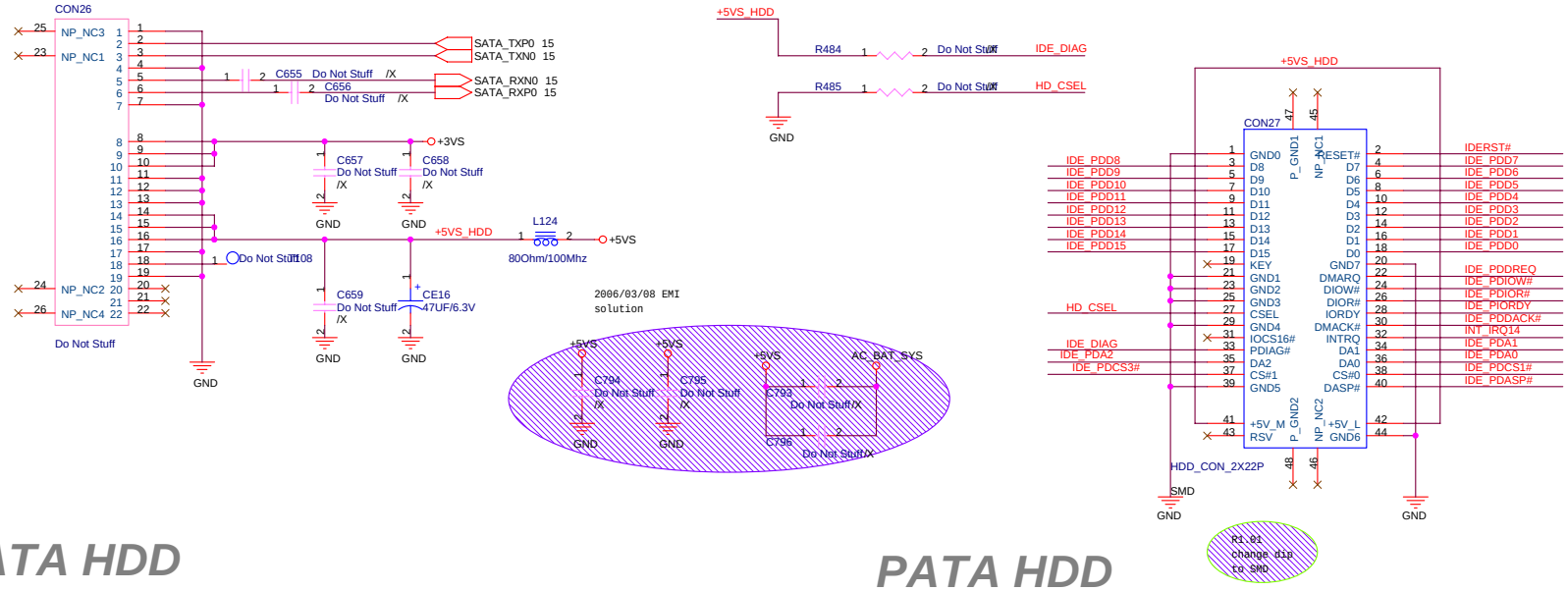


2006/04/10 Add Stitch caps

0412Z

ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 70 of 96	

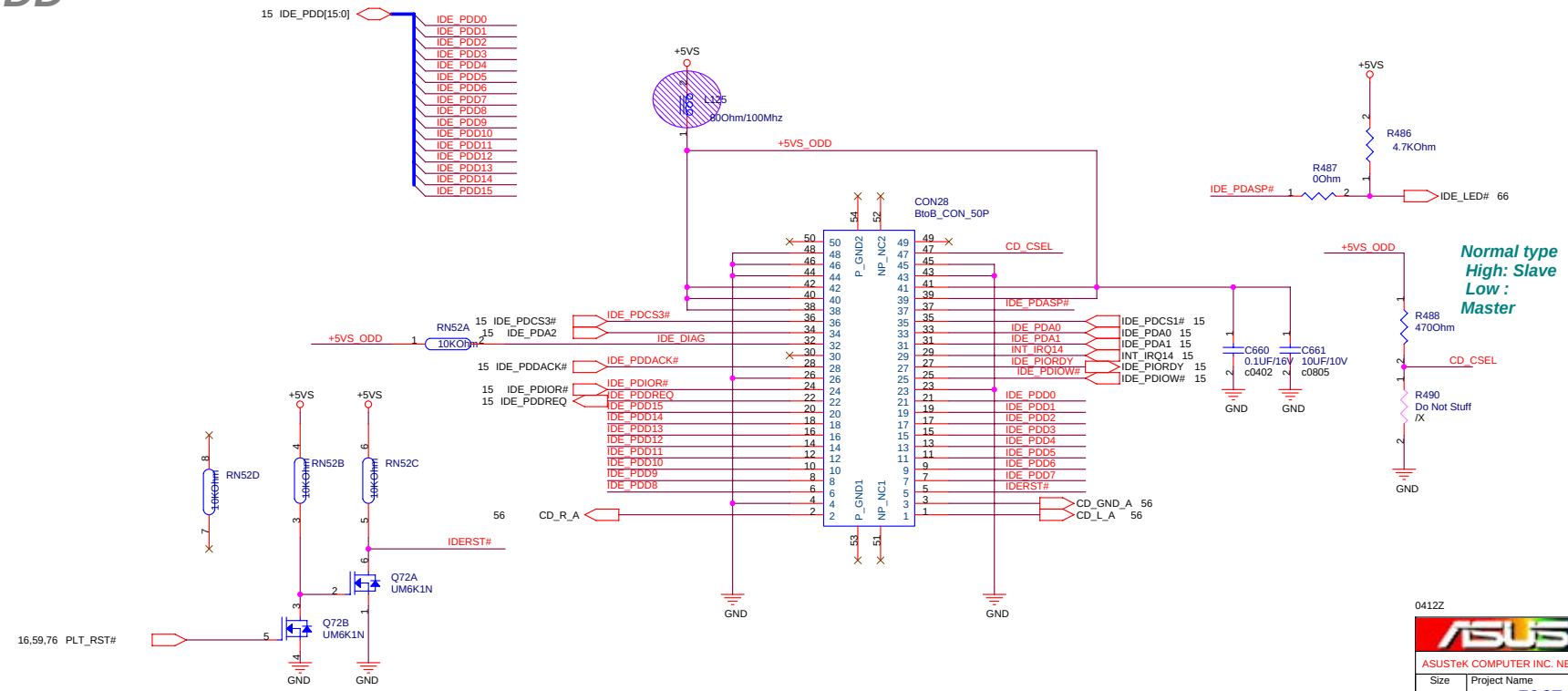
HD_CSEL : Pull-Down, HDD as Master



SATA HDD

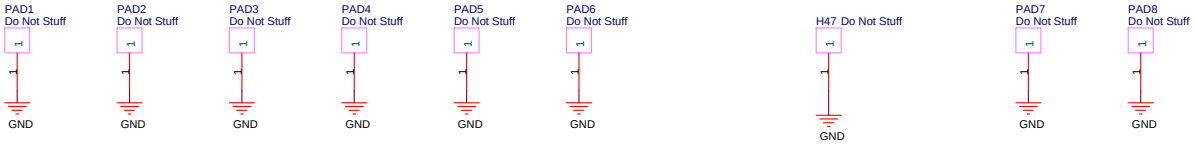
PATA HDD

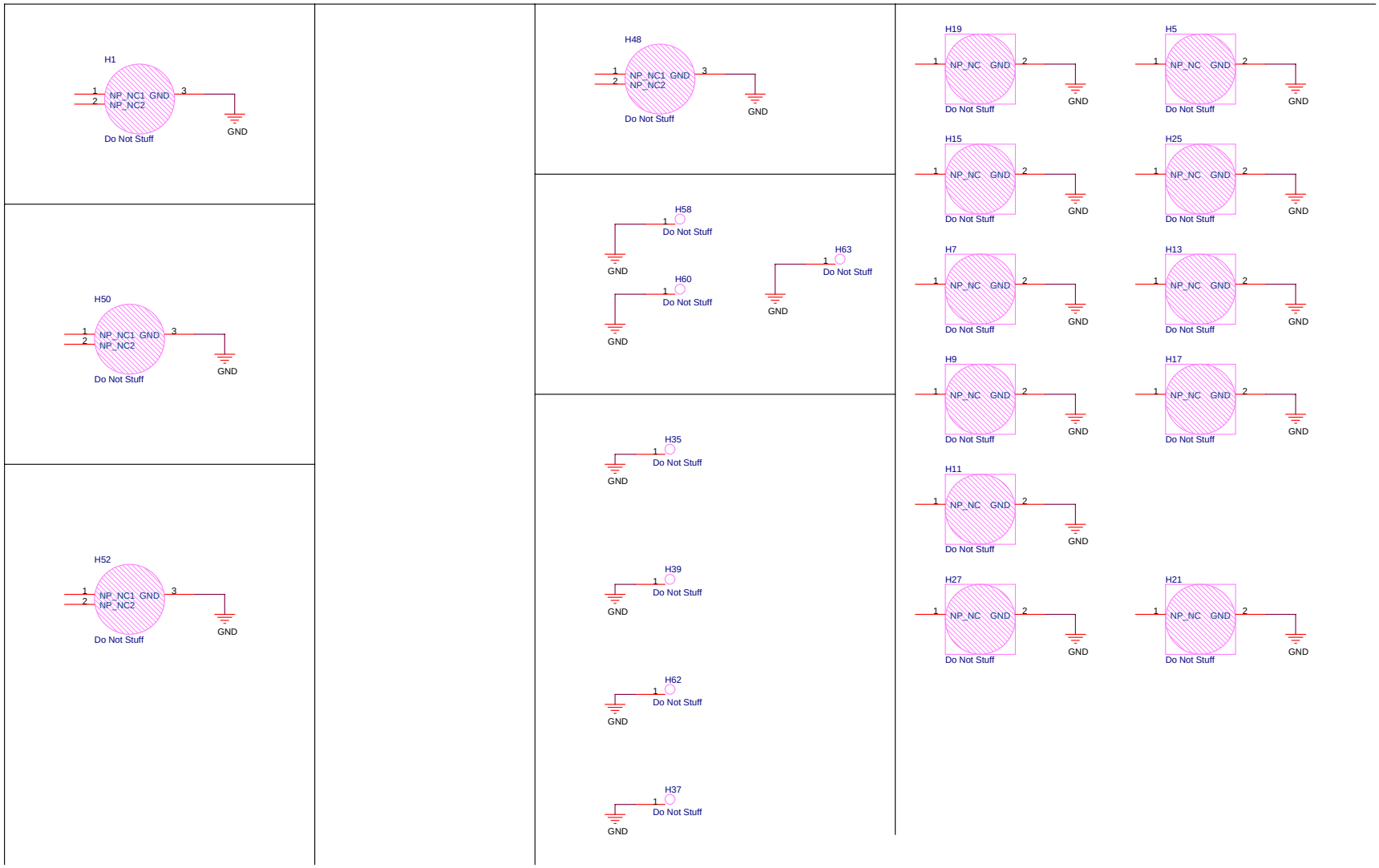
ODD



0412Z

ASUSTeK COMPUTER INC. NB1	Title : SATA-HDD & ODD	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 72 of 96	

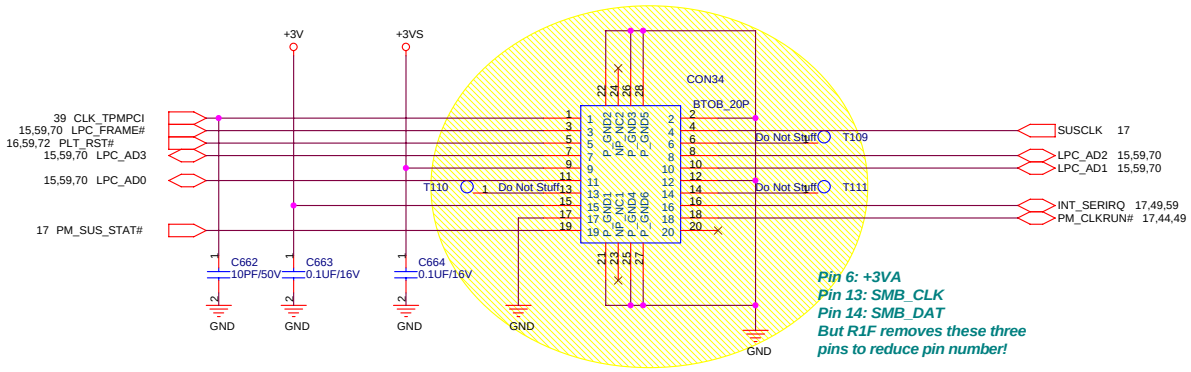


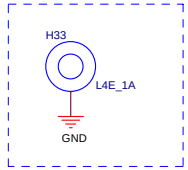


0412Z

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 74 of 96	

For TPM Module

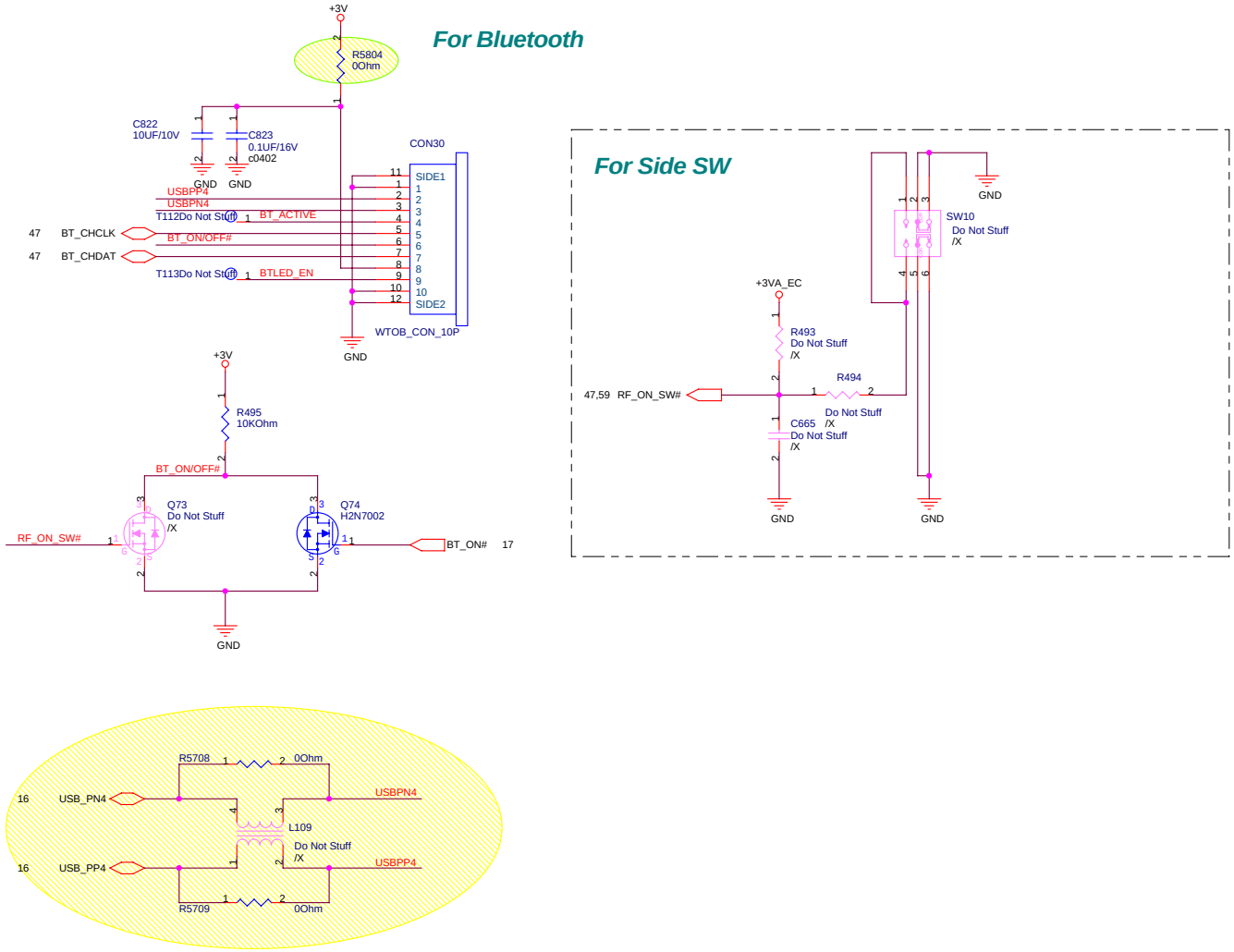




TPM MODULE NUT(3.0mm) *1

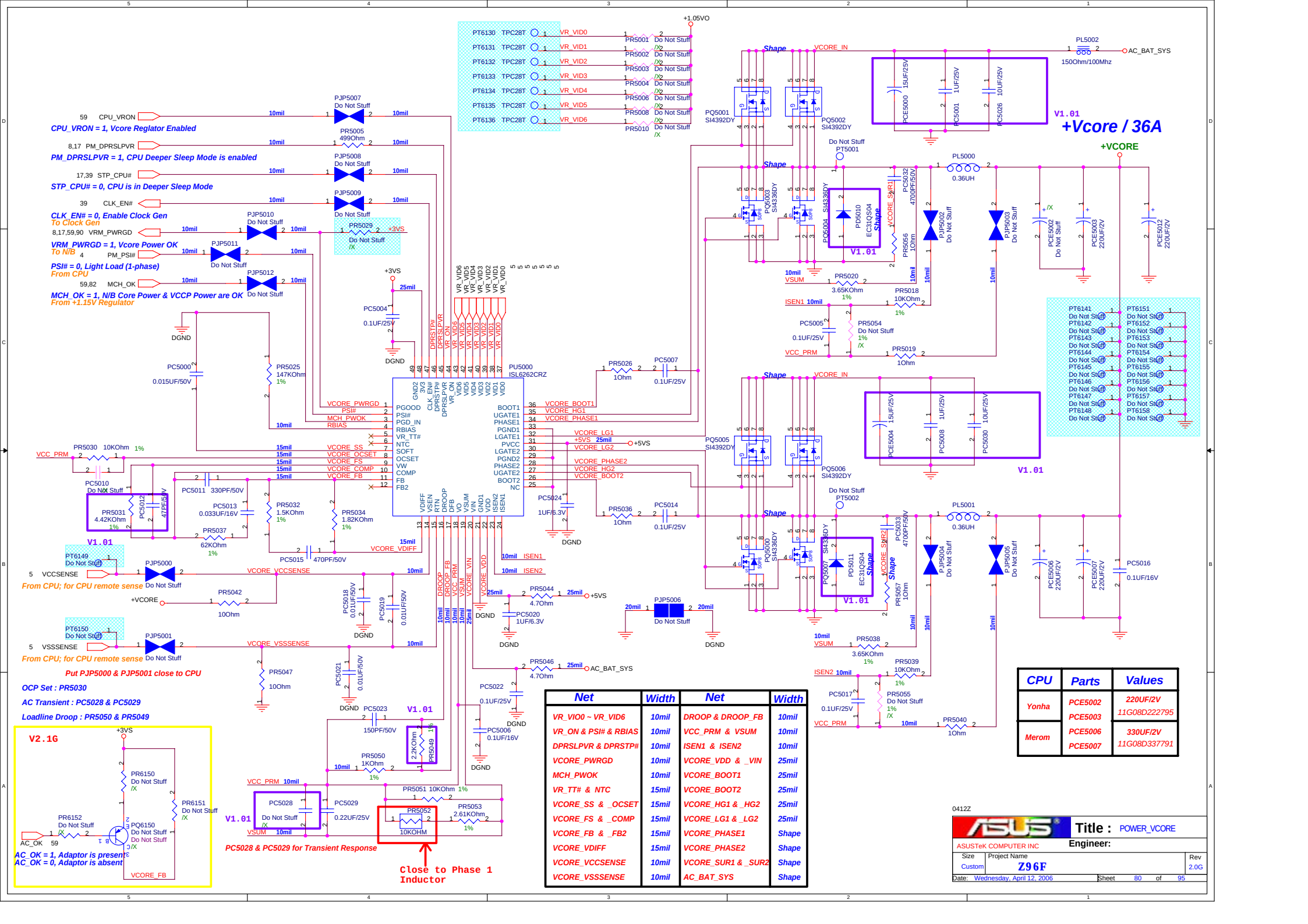
0412Z

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 76 of 96	



0412Z

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Mike Lee	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 78 of 96	



Net	Width	Net	Width
VR_VIO0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

CPU	Parts	Values
Yonha	PCE5002	220UF/2V
	PCE5003	11G08D222795
Merom	PCE5006	330UF/2V
	PCE5007	11G08D337791

0412Z

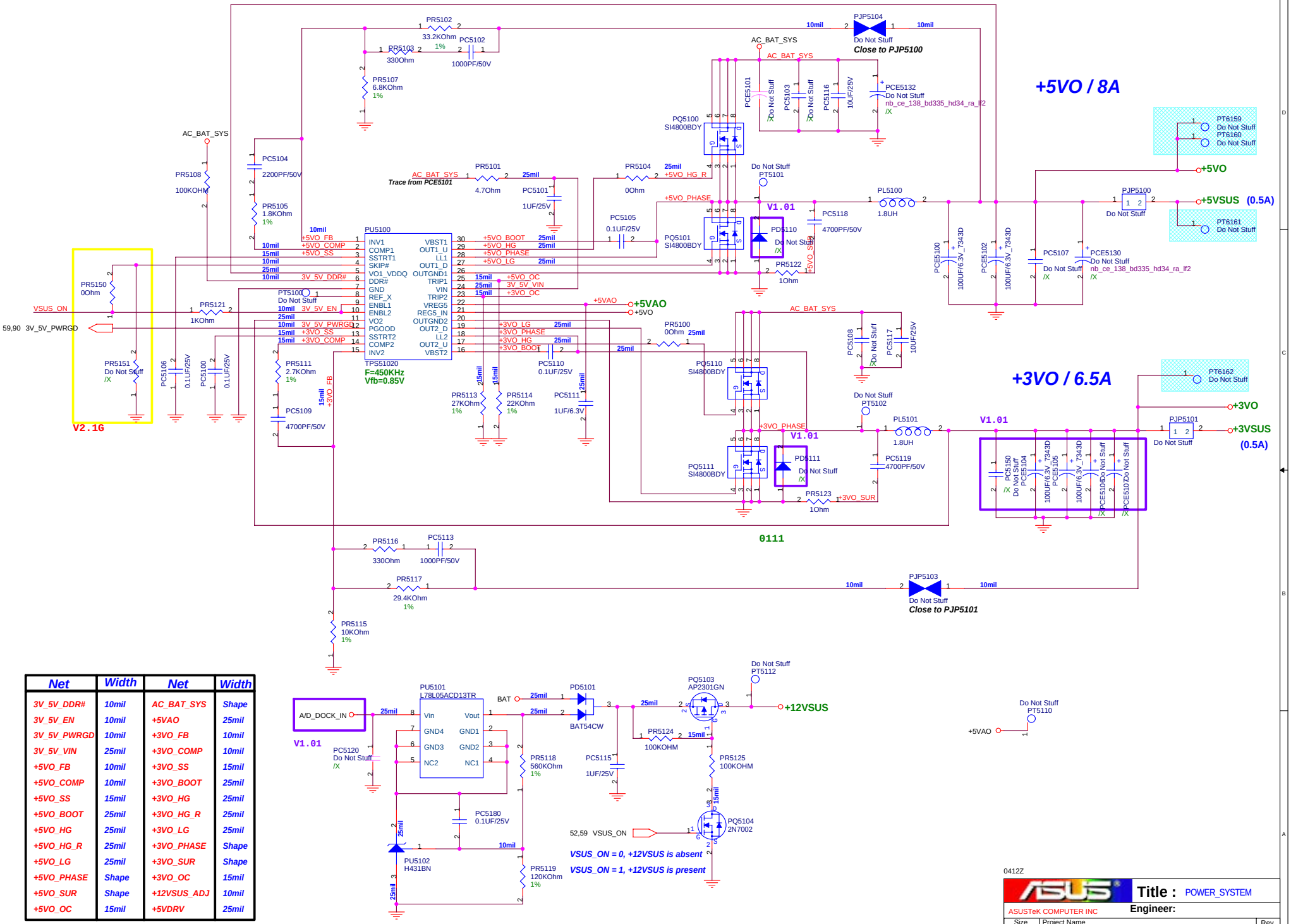
Title : POWER_VCORE

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.0G

Date: Wednesday, April 12, 2006 Sheet 80 of 95



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

0412Z

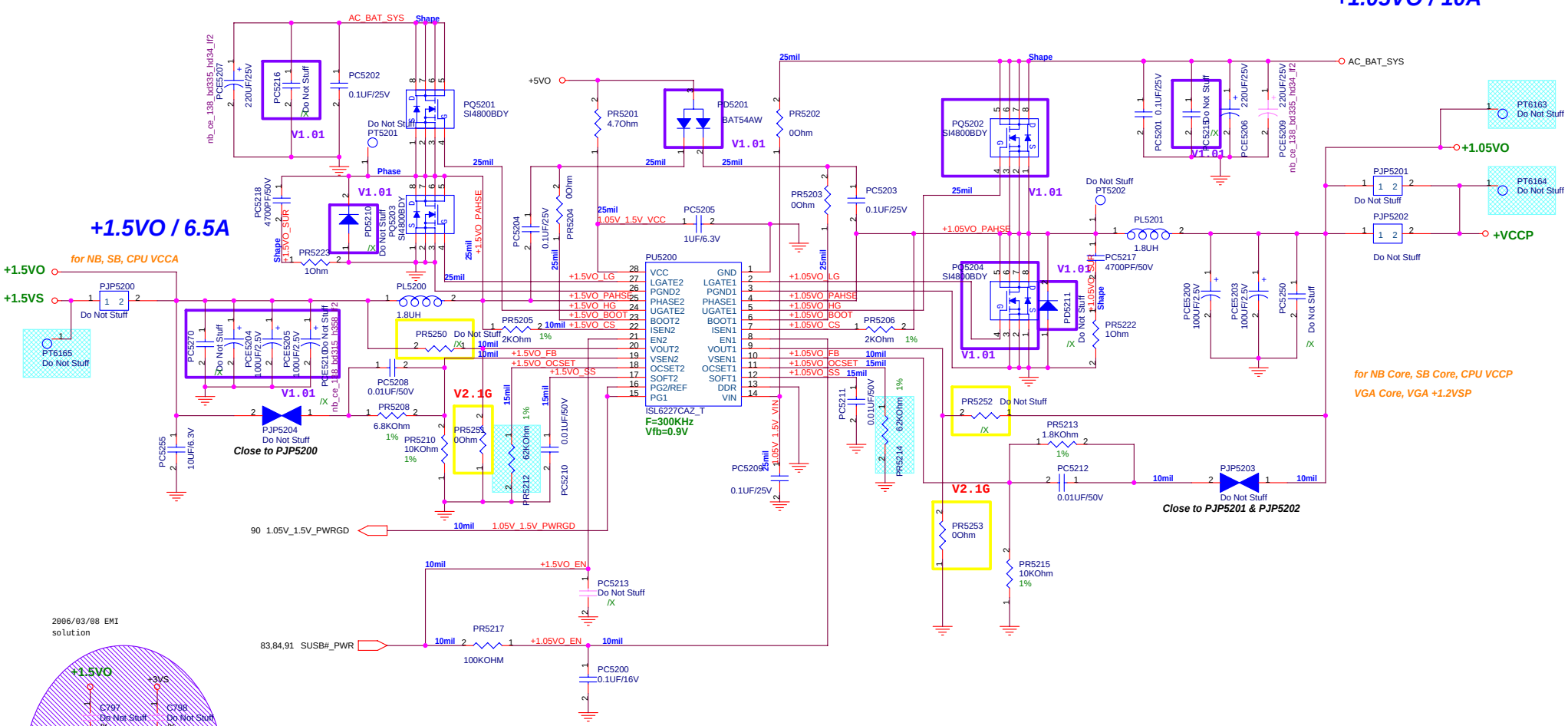
ASUSTeK COMPUTER INC

Title : POWER_SYSTEM

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.0G

Date: Wednesday, April 12, 2006 Sheet 81 of 95



Net	Width	Net	Width
1.05V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.05V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.05V_1.5V_VIN	25mil	+1.05VO_EN	10mil
+1.5VO_EN	10mil	+1.05VO_LG	25mil
+1.5VO_LG	25mil	+1.05VO_HG	25mil
+1.5VO_HG	25mil	+1.05VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.05VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.05VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.05VO_CS	10mil
+1.5VO_CS	10mil	+1.05VO_FB	10mil
+1.5VO_FB	10mil	+1.05VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.05VO_SS	15mil
+1.5VO_SUR	Shape	+1.05VO_SUR	Shape

0412Z

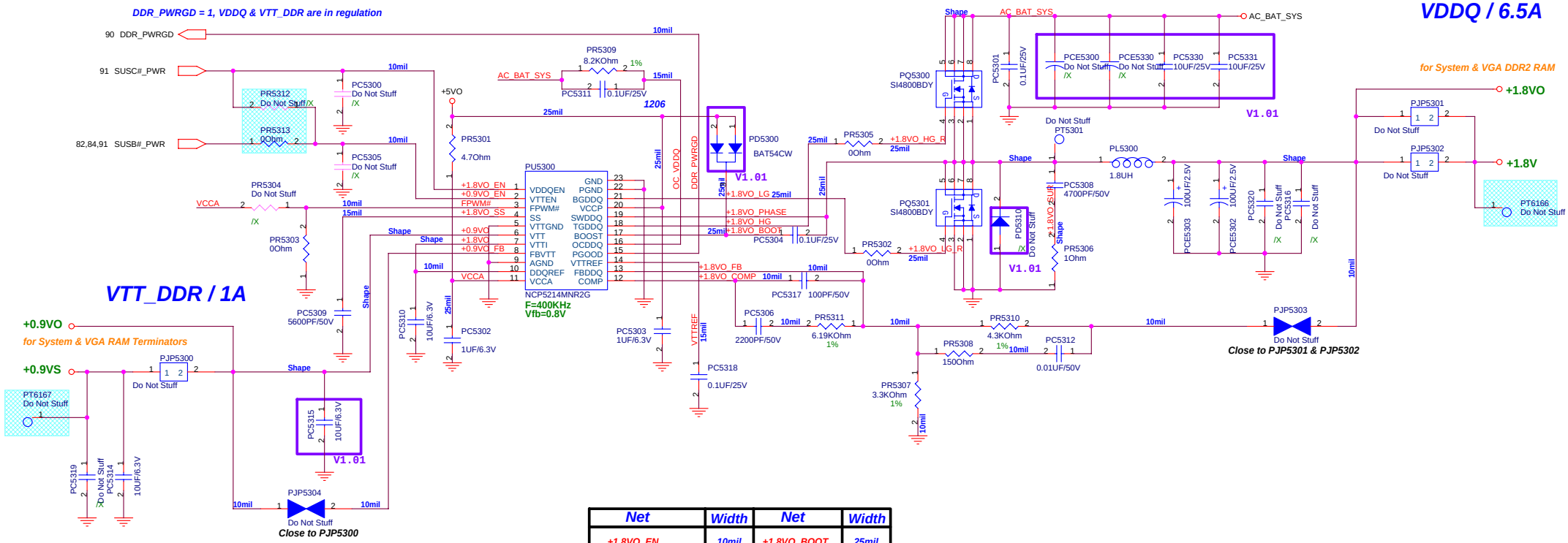
ASUSTeK COMPUTER INC

Title : POWER_I/O_1.5VS & 1.05VS

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.0G

Date: Wednesday, April 12, 2006 Sheet 82 of 95



Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

0412Z

ASUSTeK COMPUTER INC

Title : POWER_I/O_DDR & VTT

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.1G

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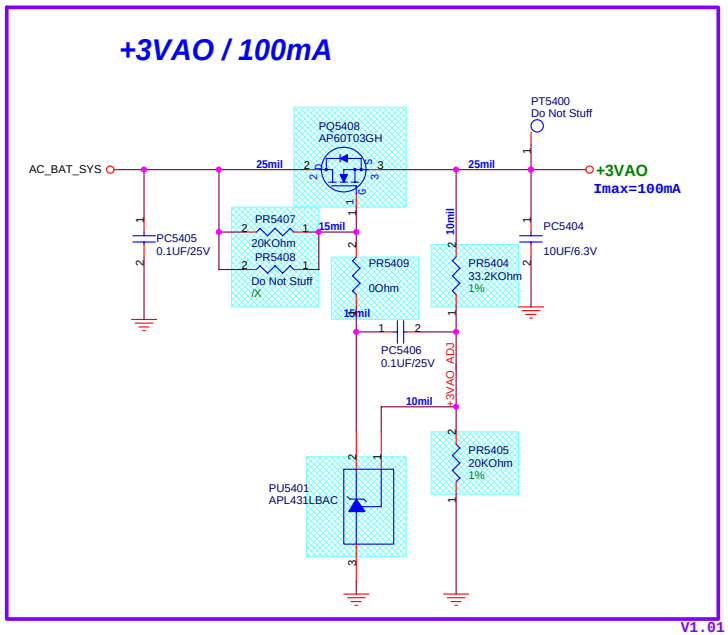
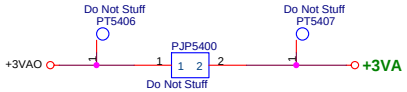
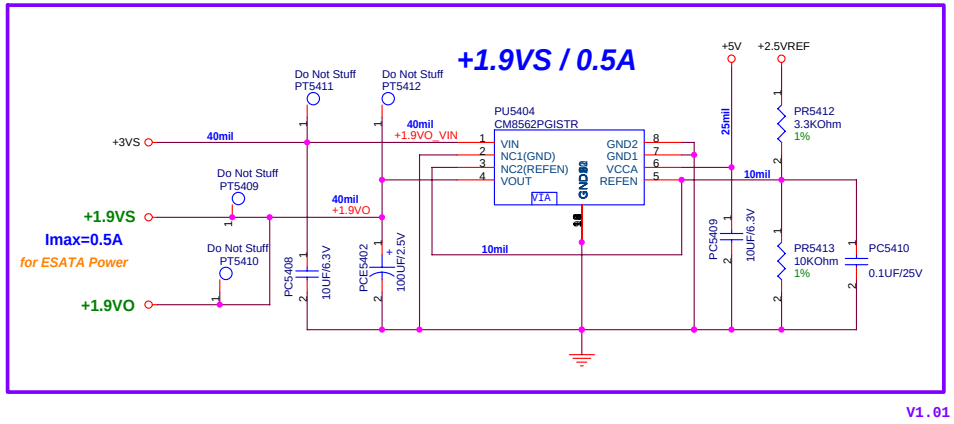
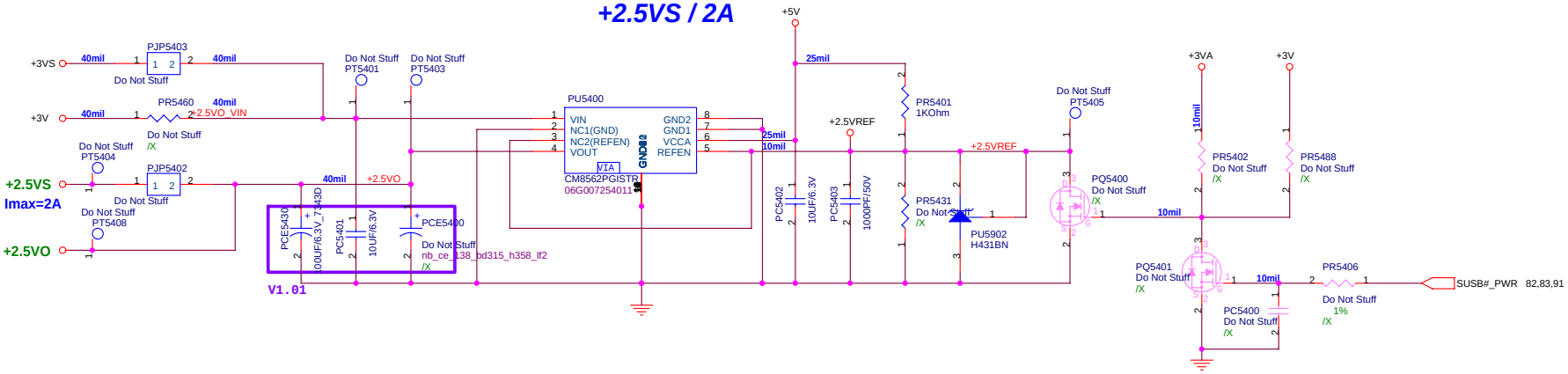








0412Z

ASUSTeK COMPUTER INC

Title : POWER_I/O_+3VA & +2.5V

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.0G

Date: Wednesday, April 12, 2006 Sheet 84 of 95

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Setting the Adapter Input Current Limit

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V

Adaptor Max. Current :

PR5714 = 178K; Ilimit = 4.5A; 90W
PR5714 = 47K; Ilimit = 3.5A; 65W

Setting the Charge Voltage

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V => Vbatt = 4.2V

Setting the Charge Current

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)= 15m Ohm

Pre-Charging Mode :

Precharging current = 148 ~ 152mA
VictI = 0.107V ~ 0.109V

Battery Cell Selection :

BATSEL_2P# = 0, 3 Cells; VictI = 2.084V
=> Icharge = 1.6933A
BATSEL_2P# = 0, 6 or 9 Cells; VictI = 2.111V
=> Icharge = 2.9329A

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

POWER PATH & BAT_LEARN

Battery Voltage

59 BATSEL_2P#
BATSEL_2P# = 1, 6 Cells
BATSEL_2P# = 0, 9 Cells

59 PRECHG
PRECHG = 1, Pre-Charging Mode
Charging Current = 156mA

59 CHG_EN#
CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled

59 AC_OK
AC_OK = 1, Adaptor is present
AC_OK = 0, Adaptor is absent

59 BAT_LEARN
BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

AC_APR_UC = 1, Adaptor is present
AC_APR_UC = 0, Adaptor is absent

BAT_IN = 0; Battery absence
BAT_IN = 1; Battery Plug-in

TS# = 1; Battery absence
TS# = 0; Battery Plug-in

0412Z

ASUSTeK COMPUTER INC

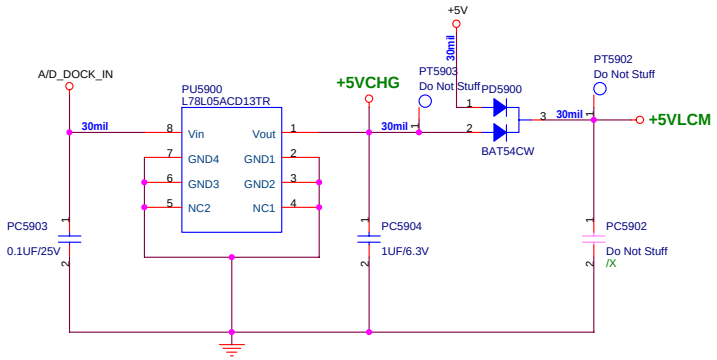
Title : POWER_CHARGER
Engineer:

Size	Project Name	Rev
C	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 87 of 96

REMOVE BATTERY IN DETECT

+5VLCM / +5VCHG



0412Z

Title : POWER_DETECT

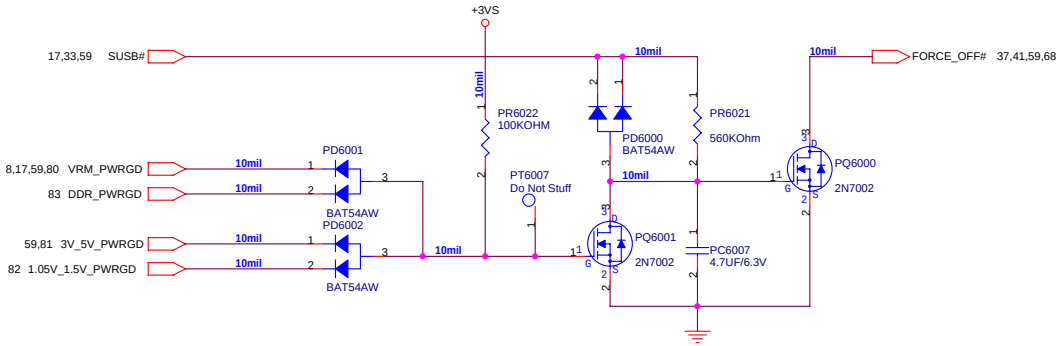
ASUSTeK COMPUTER INC

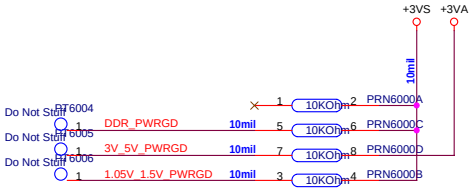
Engineer:

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 89 of 96

Power Good Detecter

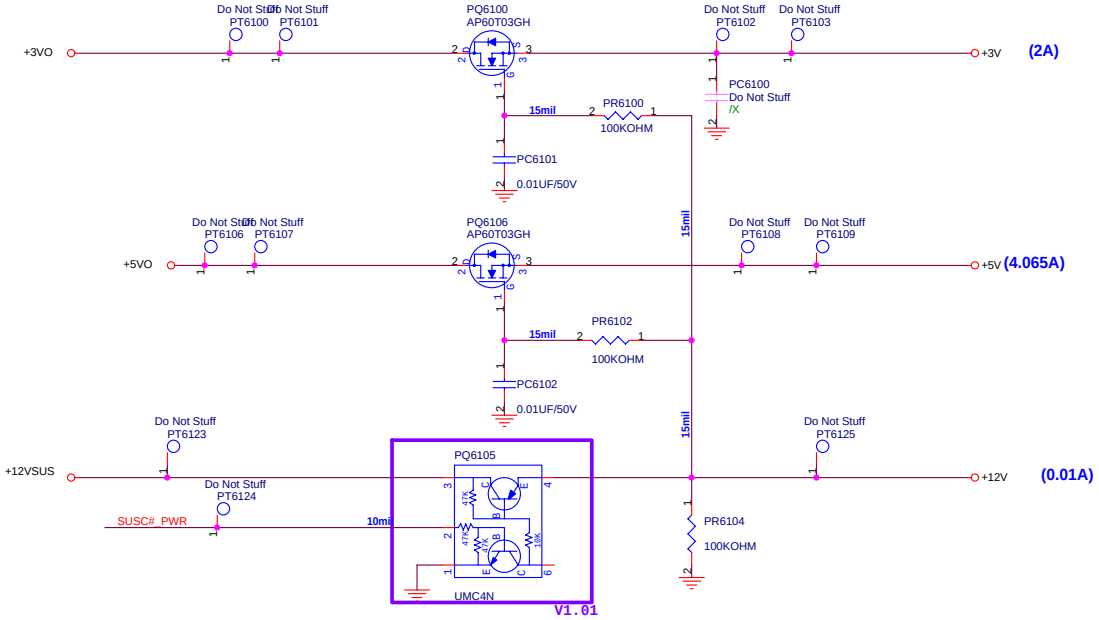


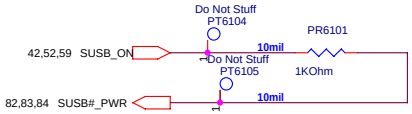


0412Z

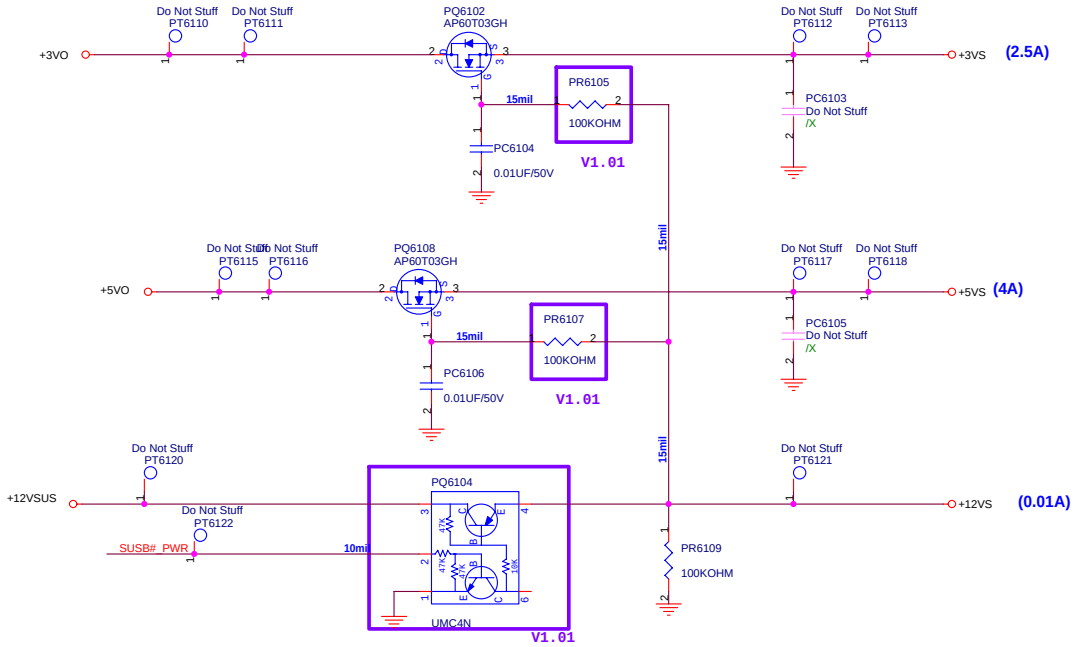
ASUSTeK COMPUTER INC	Title : POWER_PROTECT	
	Engineer:	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 90 of 96	

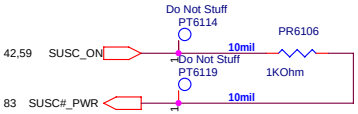
SUSC#_PWR POWER





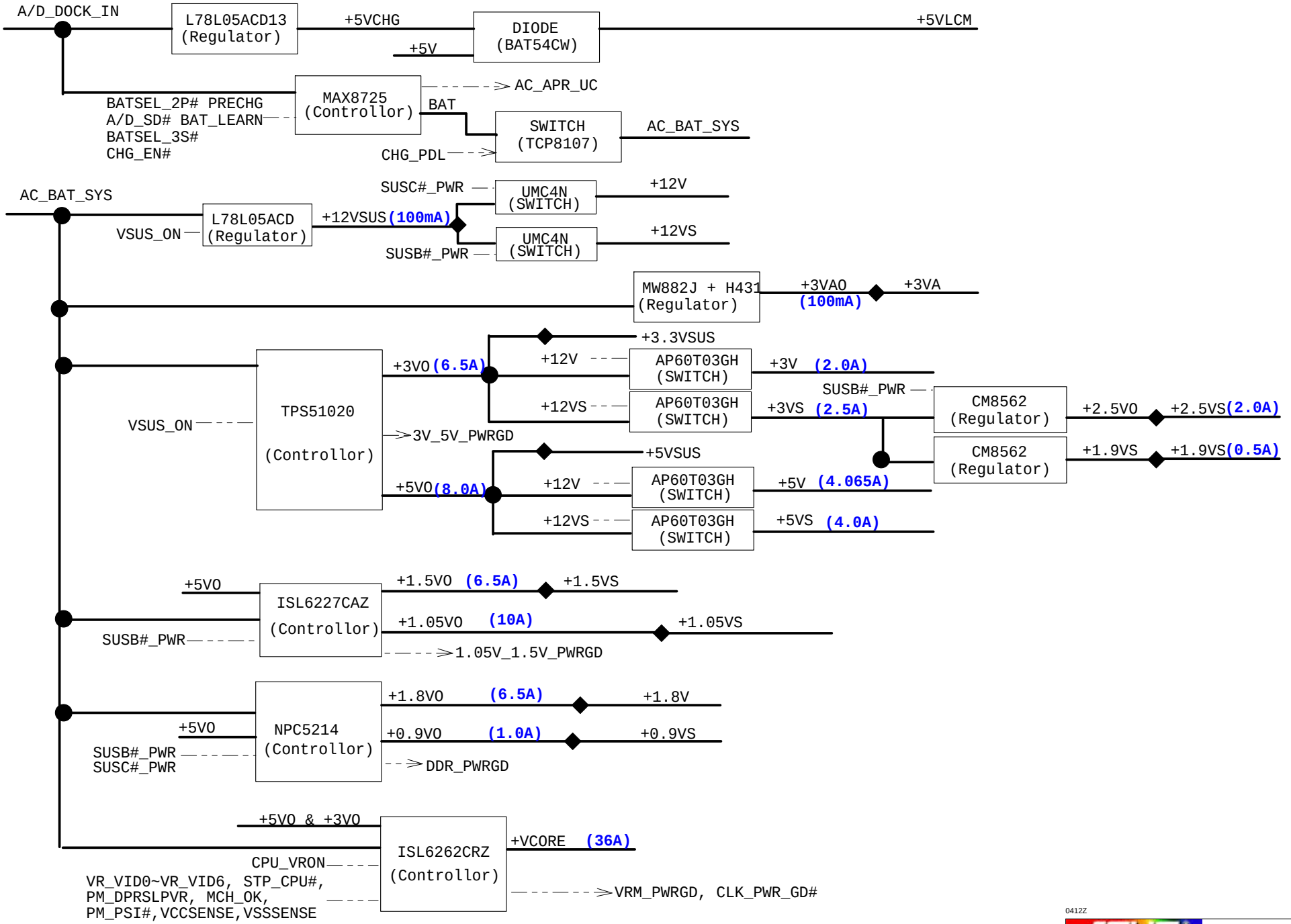
SUSB#_PWR POWER





0412Z

ASUSTeK COMPUTER INC	Title : POWER_LOAD SWITCH	
	Engineer:	
Size: Custom	Project Name: Z96F	Rev: 2.1G
Date: Wednesday, April 12, 2006	Sheet 91 of 96	



0412Z

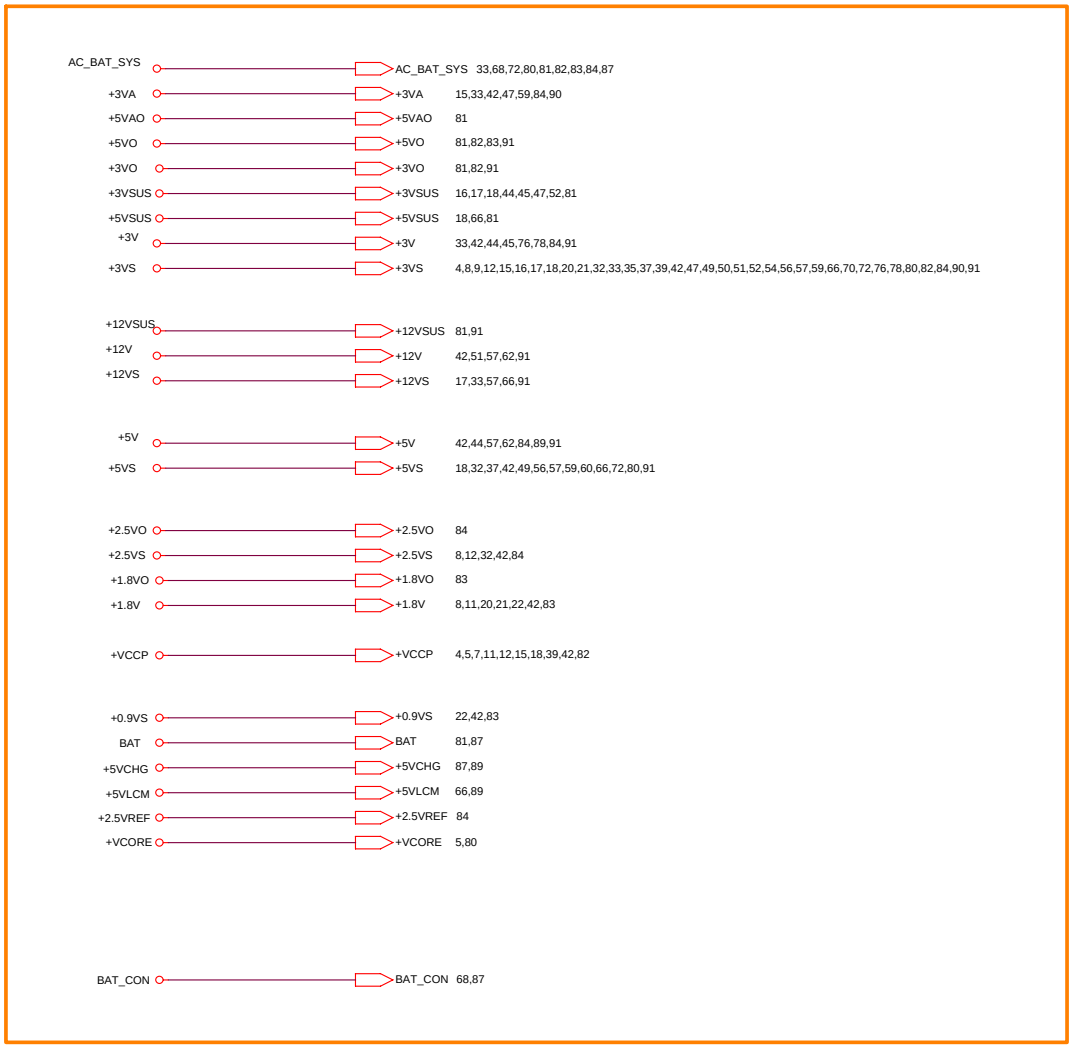
ASUSTeK COMPUTER INC

Title : POWER_FLOWCHART

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.1G

Date: Wednesday, April 12, 2006 Sheet 92 of 96



0106

0412Z

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	Z96F	2.1G

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CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.00G	2006/01/10 1430	Initial release, revision 0.1
	2006/01/11 2100	1. Change NB(U2) part number from 02G010009100 to 02G10009205 2. Change SB(U3) part number from 02G010008800 to 02G10007741 3. Change RN77, RN78 signals. 4. Swap EC(U35) pin33/36/37 signals from CLK_PWRSAVE# / T85 / FAN_PWM to FAN_PWM / CLK_PWRSAVE# / T85. 5. Change power circuit page 81, 82, 83, 87 (refer Z96F_R01_0111_P.DSN) 6. Delete T139-T141, T143-T146 7. Swap Network resistor signals for layout routing.
	2006/01/12 0922	1. Swap L84, L108, L115 signals for layout routing. 2. Change power circuit page 84 (refer Z96F_R01_0111_P1.DSN) 3. Delete T142.
	2006/01/13 1509	1. Add C757 for EMI request. 2. Modify page2 EC GPIO setting notice table. 3. Swap Network resistor signals for layout routing. 4. Change PR4724 PU from MAX8725_LDO to +3VA_EC. 5. Remove AC_APR_UC# from U35.28 to U35.172 6. Delete H41-46
	2006/01/14 1301	1. Delete: R413-R415, R417, F3, C508, R534, R303, R305, RN73-RN76, R5732-R5736. 2. NU(not use): C755, R5765, R5766, R5764, R5768, C71, R47, C513, C514, C707,C708, C517, C524, C526, C568, C642, C741, C744, C745, C726, C706, C404. 3. page32, change RGB far end terminator from Resistor(R5759/R5761/R5763) to Network Resistor(RN79). 4. page35, change TV_OUT signal far end terminator from Resistor(R5755-R5757) to Network Resistor(RN80). 5. page42, change discharge resistor from Resistor(R5774-R5783) to Network Resistor(RN81-RN83). 6. Change RN77 signal. 7. Change 25MHz X'tal (X7) to 07G010Q12500. 8. Change Thermal IC U16 to SOP (06G023026011) 9. Change 0.1UF/25V cap from X7R +/-10% to Y5V+80-20%: C757, C643, C646, C649, C652
	2006/01/16 1530	1. Change power circuit page 80, 81, 82, 83 (refer Z96F_R00_0116_P.DSN) 2. Change X1, X6 package to same as Z84F.
	2006/01/17 1046	1. Swap Network resistor signals for layout routing. 2. Change Codec ALC882(U30) part number from 02G611001300 to 02G611001310.
	2006/01/17 2038	1. Change power circuit page 80, 83 (refer Z96F_R01_0117_P.DSN) 2. Add Network Resistor RN84, RN85(NU, reserved) to block VGA signal between CRT and PortBar connector(EMI request) .
	2006/01/18 1103	1. Swap Network resistor RN81, RN83 signals for layout routing. 2. Stuff C755. 3. NU: C115, C116, R304, R306, R282, R284, R5796, CN10, C655, C656. 4. Add 3 0ohm resistor R5805(NU), R5806, R5807 for SATA function disable.

Rev	Date	Description
	2006/01/18 1645	1. Change power circuit page 81, 82, 83, 84, 87 (refer Z96F_R01_0118_P.DSN) 2. Swap PCIE clock (NEWCARD & MCH_3GPLL) for layout routing. 3. Swap Network resistor RN58, RN77, RN78, RN84, RN85 signals for layout routing.
	2006/01/19 1145	1. Swap Network resistor RN18, RN82, RN85 signals for layout routing. 2. Change U1 (CPU) ,U2 (North Bridge) ,U3 (South Bridge) to Note Book parts.
	2006/01/19 2127	1. Change power circuit page 81 (refer Z96F_R01_0119_P.DSN)
	2006/01/20 1735	1. DEL PORT_BAR. 2. Add an ESATA (page54) and an USB port. 3. Change CON27.47, CON27.48 / CON26.25, CON26.26 / CON28.54, CON28.53 to NC 4. Connect H35-H40, H62, H63 to GND
	2006/01/23 1005	1. Change power circuit page 80- 84, 87, 91 (refer Z96F_R01_0120_P.DSN) 2. DEL RN84, RN85, R5719-R5726.
	2006/01/23 1714	1. Change power circuit page 84, 87, 91 (refer Z96F_R01_0120_P1.DSN) 2. Change ESATA1/ CON42 connector to NB part. 3. Change EC(U35) pin 28 from T174 to AC_APR_UC# signal. 4. Change EC(U35) pin 174 signal from AC_APR_UC# to AC_OK# signal. 5. Add a N-MOS(Q6118) to invert AC_OK signal.
	2006/01/24 1030	1. Change RN53, RN54, RN81-RN83 from 0402 to 0603. 2. Add C764-765, R5812-5815 for ESATA. 3. Add D59, Q6119 to switching XD card power. 4. Change CON21 signal. 5. Change U35.89/RN41.1/SW3.1/SW3.2 signal from EXPLORE_SW# to PWR4GEAR#. 6. Change power circuit page 81 (refer Z96F_R01_0124_P.DSN) 7. Swap Network resistor RN18, RN79, RN78, L115 signals for layout routing. 8. Change page 93 +5VA signal name to +5VAO.
	2006/01/25 1425	1. Change RN70, RN71, RN79, RN80 to LF parts. 2. Change PU5700.6 signal name to AC_OK.
	2006/01/25 2110	1. Swap Network resistor RN33, RN53, RN70, RN79, RN80 signals for layout routing. 2. Change T2R2 to 10M ohms.
	2006/01/26 1822	Change Revision to 1.00G
	2006/02/13 1536	Change C764, C765, C118-C121 from Y5V to X7R Change T2C25, T2C26 from Y5V to X7R
	2006/02/17 1639	Modify Block Diagram

0412Z

ASUSTek COMPUTER INC

Title : History(1)

Engineer: Mike Lee

Size	Project Name	Rev
Custom	Z96F	2.1G

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CIRCUIT UPDATED HISTORY(2)

Rev	Date	Description
1.01G	2006/02/27 1100	1. Change R5710 to NU 2. Add R5816(NU) 3. Change page54 ESATA power from +VRAM to +1.8V 4. Change C717, C718 connection. 5. Swap INTERNAL MIC R/L. 6. Stuff R47 (10M ohms). 7. Change Rev to 1.01G
	2006/03/01 1120	1. Add R5828-5831, C788. 2. Swap LTPB0-/+ common choke (L112) for routing. 3. Swap LTPA0-/+ common choke (L113) for routing. 4. Swap USB_PN5/_PP5 common choke (L115) for layout routing. 5. Swap RN34 signals for layout routing. 6. Change page54 ESATA from SII3132 to JMB360. 7. Change page74 scrow hole type.
	2006/03/02 1819	1. Updated power page80-84, 87, 91 2. Del page55 circuit.
	2006/03/03 1450	1. Add screw hole H63 2. Change ESATA SMBus PU 4.7K to 3V 3. Change ESATA +1.8V to +1.9V 4. Modify page54 ESATA power rail. 5. Updated power circuit page80-82, 84, 87. 6. Change HSYNC/VSYNC level shifter (U44, U45) power rail from 5V to 3.3V.
	2006/03/03 1740	1. Updated power circuit page80-82, 84, 87 (refer Z96F_R101G_0303_P2.DSN). 2. Add PWRSW# mask circuit (page41). 3. Change HSYNC/VSYNC ESD power rail from 5V to 3.3V.
1.1G	2006/03/06 1950	1. Change H54, H56 / H29, H31 / H3 / H33 from screw hole to NUTs. 2. Change X1 / X6 from DIP type to SMD type. 3. Change C112, C113 / C632, C633 value from 20pF to 12pF. 4. For EMI: 1) Add L124. 2) Change R536, R537 from 0R to Bead(1K ohm/100MHz). 3) Stuff R418, R431 with 0R. 4) Change L52 from 80 ohm/100MHz to 150ohm/100MHz). 5) Stuff C411, C412, C413, C414. 5. Change Rev to 1.1G (to meet NB team PN rule)
	2006/03/08 1100	1. Del H23 2. Del C698, C699 3. Add RN73-76, C793-799 (NU, for EMI). 4. NU R359
	2006/03/09 2121	1. Swap RN44, RN54 signals for routing. 2. Stuff R5794, RTC BATT, R68, R69, C517, C524, C526, R550 3. NU R71, R72, R307 4. Change D58 from SS0540 to 1N4148 5. Change CON5 (LVDS CONN) to 12G09103004P 6. Change U16 to ADT7461ARMZ 7. Change SW1-4, SW6-7 to 12G09103004P

Rev	Date	Description
		8. Change X7 part. 9. Change C727-728 from 24p to 18p 10. NU R5770, R5769, Q6116, SW11, R5717, R5718 11. Add C500 for U23 12. Del XD function: Del D59, Q6119, C709.
	2006/03/10 1212	1. Change power circuit page 81-84, 87 (refer Z96F_R11_0310_P.DSN)
	2006/03/10 1538	1. NC CON36.16
	2006/03/13 2013	1. Change R48 from 22K to 100K 2. Del R307. 3. NU R5795, Q6117, R550. 4. Stuff R5797=0R, SW7.
	2006/03/14 1430	1. Change U1 to 12G04600479A 2. Change CON2 to 12G025332003 3. Change CON3 to 12G025122000 4. Change CON36 to 12G142101100 5. Change CON27 to 12G161530444 6. Change CON13 to 12G030100522 7. Change J1, J2 to 12G140031067 8. Change power circuit page 81, 82(refer Z96F_R11_0314_P.DSN)
	2006/03/16 2016	1. Stuff CE2 100UF/2.5V_7343 2. Stuff R307 10K ohm_0402 3. Stuff C627, C741 10UF/10V_0805 4. Stuff C742, C743, C744, C748 0.1UF/16V_0402
2.0G	2006/04/03 0809	1. Change to Rev 2.0 2. Add a MOSFET Q6121 to block USB power 3. Add R5838, C800-C805, D61 4. Change NUT H56, H54 to 4.2mm 5. Change PR5709 P/N 6. Change JRST1 footprint to R0402
	2006/04/03 1527	1. Change JRST1 2. Change power circuit page 80-84, 87, 89-92(refer Z96F_R20_0403_P.DSN)
	2006/04/04 0756	1. Change NEWCARD_CLK from U18.24-25 to U18.19-20 2. Add R5839, R5840, R5841 3. Add R5842, R5843, R5844 4. Stuff R5833 5. NU Q6120, R5832, R5834, R5834, D60
	2006/04/04 2154	1. Add Stitch cap C806-C810 2. Add C811-C814 3. NU R352, Stuff R353 4. Change CON7.6 to GND 5. BIOS1 to SMD and NU U38 (BIOS Socket).
2.1G	2006/04/07 1445	1. Change to Rev 2.1 2. Change power circuit page 84(refer Z96F_R20_0407_P.DSN)

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ASUSTeK COMPUTER INC

Title : History(2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	Z96F	2.1G

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