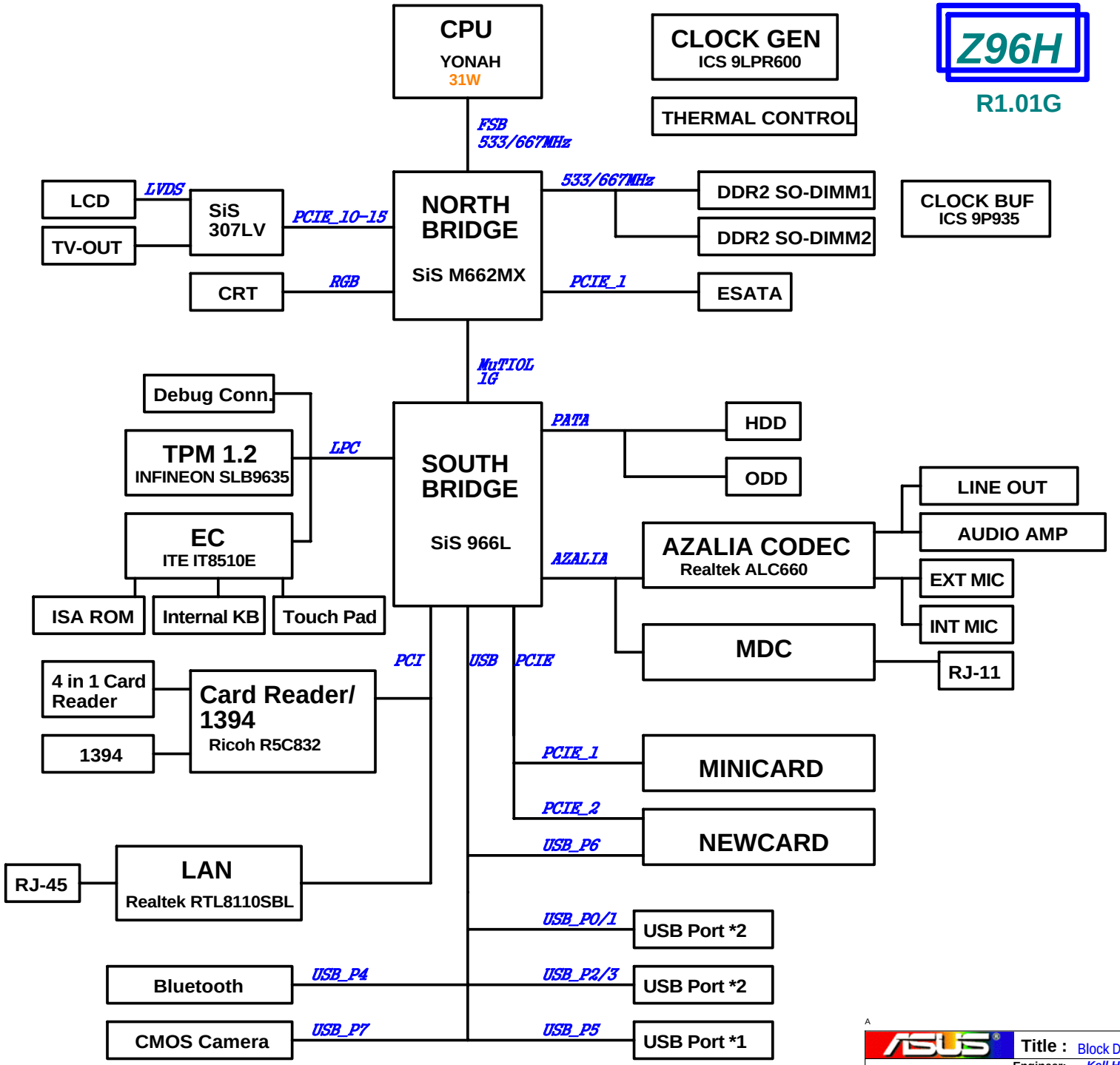


ASUSTek Computer INC.	Title : Block Diagram		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 1 of 60		

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O	H	GPI
37	PWM3/GPA3	/	I		GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	AC_OK#	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

06/01/23

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

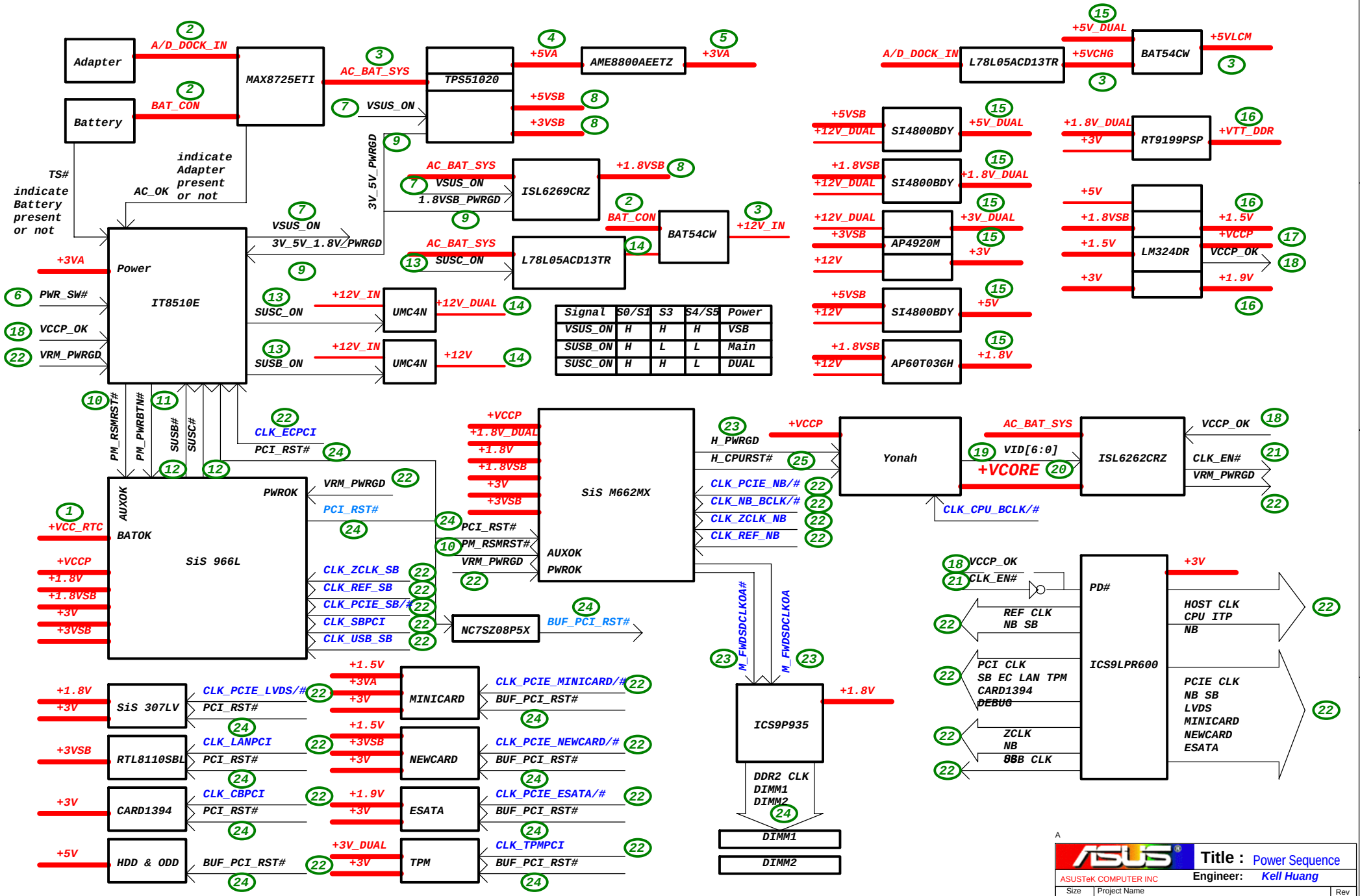
SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	01001100 (4C)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD24	0	C
1394	AD24	0	B
LAN	AD23	1	D

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	I	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

ASUSTek Computer INC.	Title : System Setting	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 2 of 60	


Adapter
A/D_DOCK_IN
MAX8725ETI
AC_BAT_SYS
Battery
BAT_CON
TPS51020
+5VA
AME8800AEETZ
+3VA
+5VSB
+3VSB
VSUS_ON
3V_5V_PWRGD
TS#
indicate Battery present or not
AC_OK
indicate Adapter present or not
Power
IT8510E
PWR_SW#
VCCP_OK
VRM_PWRGD
VSUS_ON
3V_5V_1.8V_PWRGD
SUSC_ON
SUSB_ON
UMC4N
+12V_IN
+12V_DUAL
+12V
ISL6269CRZ
AC_BAT_SYS
VSUS_ON
1.8VSB_PWRGD
+1.8VSB
BAT_CON
BAT54CW
+12V_IN
L78L05ACD13TR
SUSC_ON
Signal | S0/S1 | S3 | S4/S5 | Power
VSUS_ON | H | H | H | VSB
SUSB_ON | H | L | L | Main
SUSC_ON | H | H | L | DUAL
A/D_DOCK_IN
L78L05ACD13TR
+5VCHG
+5V_DUAL
BAT54CW
+5VLCM
+5VSB
+12V_DUAL
SI4800BDY
+5V_DUAL
+1.8VSB
+12V_DUAL
SI4800BDY
+1.8V_DUAL
+12V_DUAL
+3VSB
AP4920M
+3V_DUAL
+3V
+12V
+5VSB
+12V
SI4800BDY
+5V
+1.8VSB
+12V
AP60T03GH
+1.8V
+1.8V_DUAL
+3V
RT9199PSP
+VTT_DDR
+5V
+1.8VSB
+1.5V
LM324DR
+1.5V
+VCCP
VCCP_OK
+3V
+1.9V
PM_RSMRST#
PM_PWRBTN#
SUSB#
SUSC#
SiS 966L
AUXOK
BATOK
PWROK
+VCC_RTC
+VCCP
+1.8V
+1.8VSB
+3V
+3VSB
CLK_ECPCI
PCI_RST#
VRM_PWRGD
CLK_ZCLK_SB
CLK_REF_SB
CLK_PCIE_SB/#
CLK_SBPCI
CLK_USB_SB
SiS M662MX
+VCCP
+1.8V_DUAL
+1.8V
+1.8VSB
+3V
+3VSB
PCI_RST#
PM_RSMRST#
VRM_PWRGD
AUXOK
PWROK
H_PWRGD
H_CPURST#
CLK_PCIE_NB/#
CLK_NB_BCLK/#
CLK_ZCLK_NB
CLK_REF_NB
Yonah
CLK_CPU_BCLK/#
AC_BAT_SYS
VID[6:0]
+VCORE
ISL6262CRZ
VCCP_OK
CLK_EN#
VRM_PWRGD
NC7SZ08P5X
BUF_PCI_RST#
M_FWDSDCLKOA#
M_FWDSDCLKOA
ICS9P935
+1.8V
DDR2 CLK
DIMM1
DIMM2
DIMM1
DIMM2
VCCP_OK
CLK_EN#
PD#
REF CLK
NB SB
PCI CLK
SB EC LAN TPM
CARD1394
DEBUG
ZCLK
NB
BB CLK
ICS9LPR600
+3V
HOST CLK
CPU ITP
NB
PCIE CLK
NB SB
LVDS
MINICARD
NEWCARD
ESATA
SiS 307LV
CLK_PCIE_LVDS/#
PCI_RST#
RTL8110SBL
CLK_LANPCI
PCI_RST#
CARD1394
CLK_CBPCI
PCI_RST#
HDD & ODD
BUF_PCI_RST#
MINICARD
CLK_PCIE_MINICARD/#
BUF_PCI_RST#
NEWCARD
CLK_PCIE_NEWCARD/#
BUF_PCI_RST#
ESATA
CLK_PCIE_ESATA/#
BUF_PCI_RST#
TPM
CLK_TPMPCI
BUF_PCI_RST#
ASUSTeK COMPUTER INC
Title : Power Sequence
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 3 of 60

CIRCUIT UPDATED HISTORY

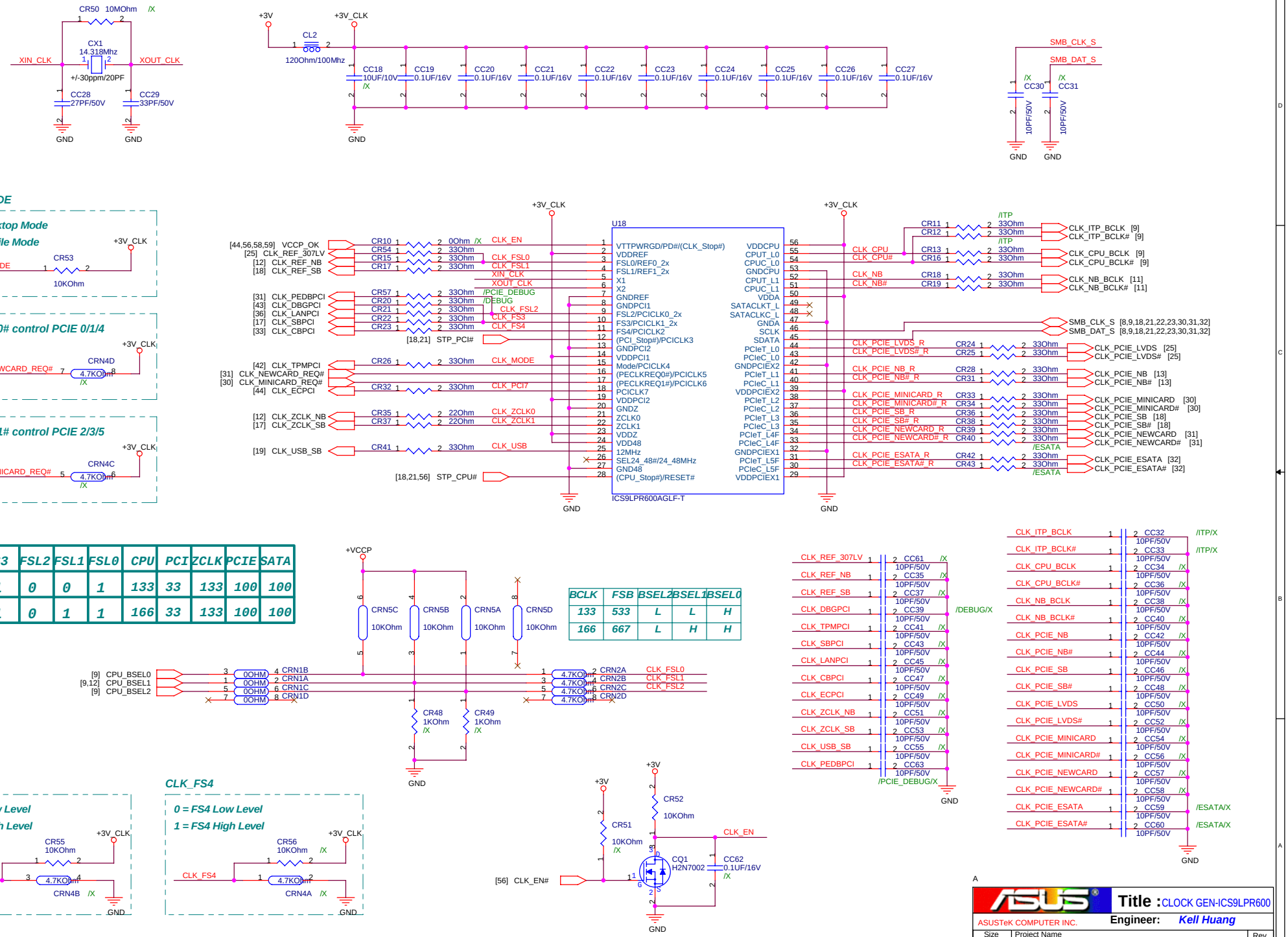
Rev	Date	Description
1.00G	2006/03/06	Z96H Schematic 1.00G (base on Z96F), NB: SiS M662MX SB: SiS 966L

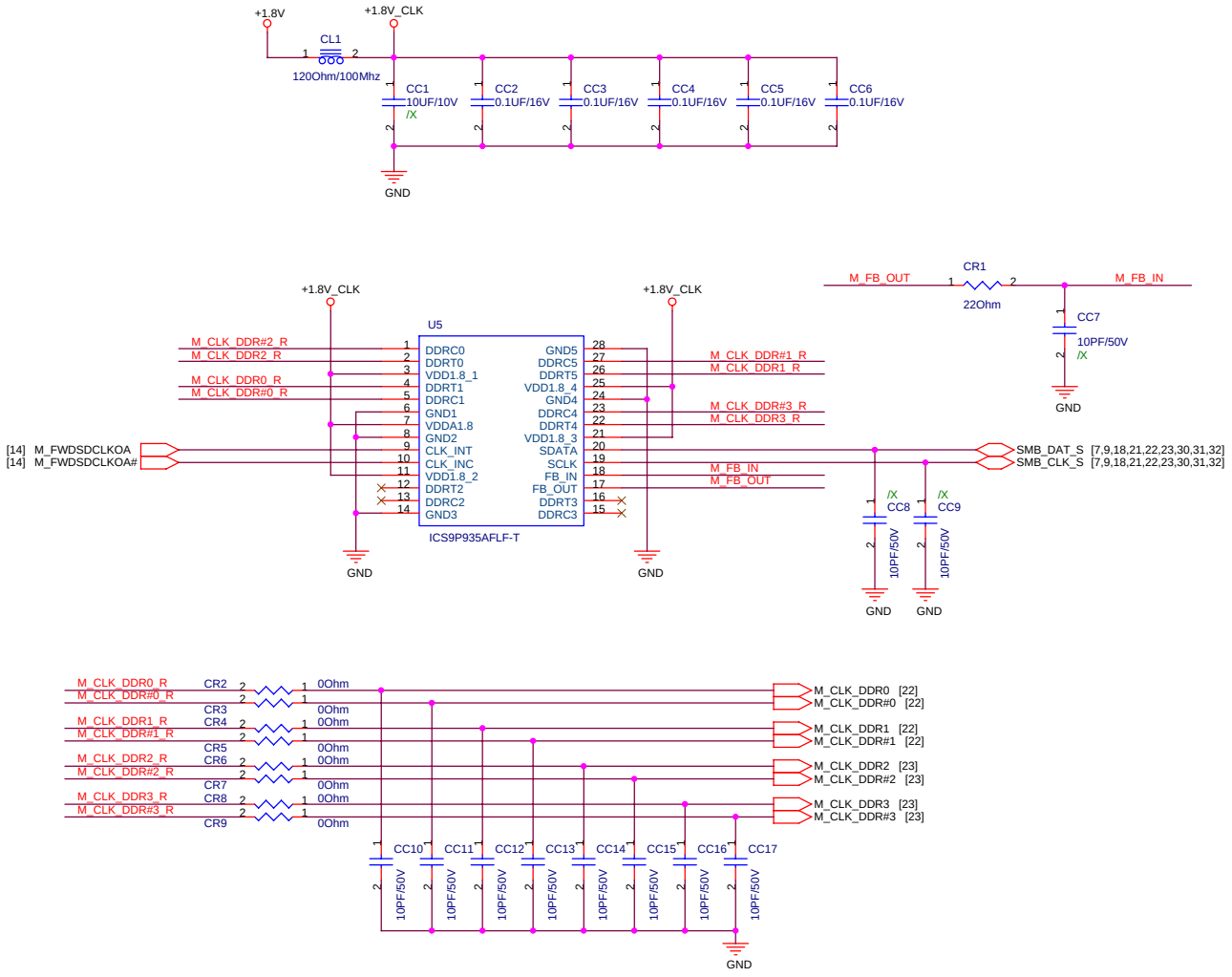
Rev	Date	Description

ASUSTeK COMPUTER INC	Title : History	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 4 of 60	

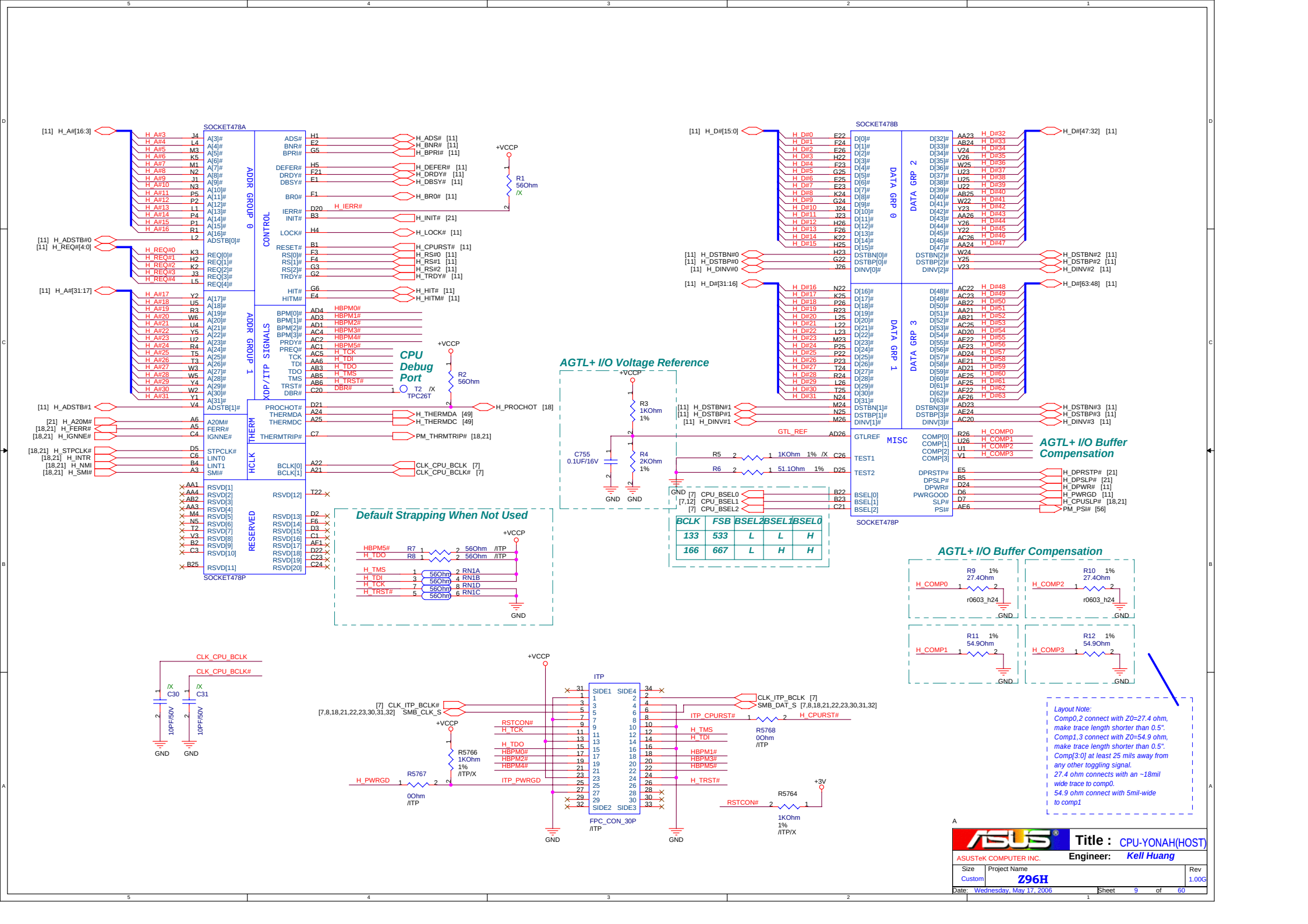
Title :	Blank
ASUSTeK COMPUTER INC	Engineer: Kell Huang
Size: A3	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 5 of 60

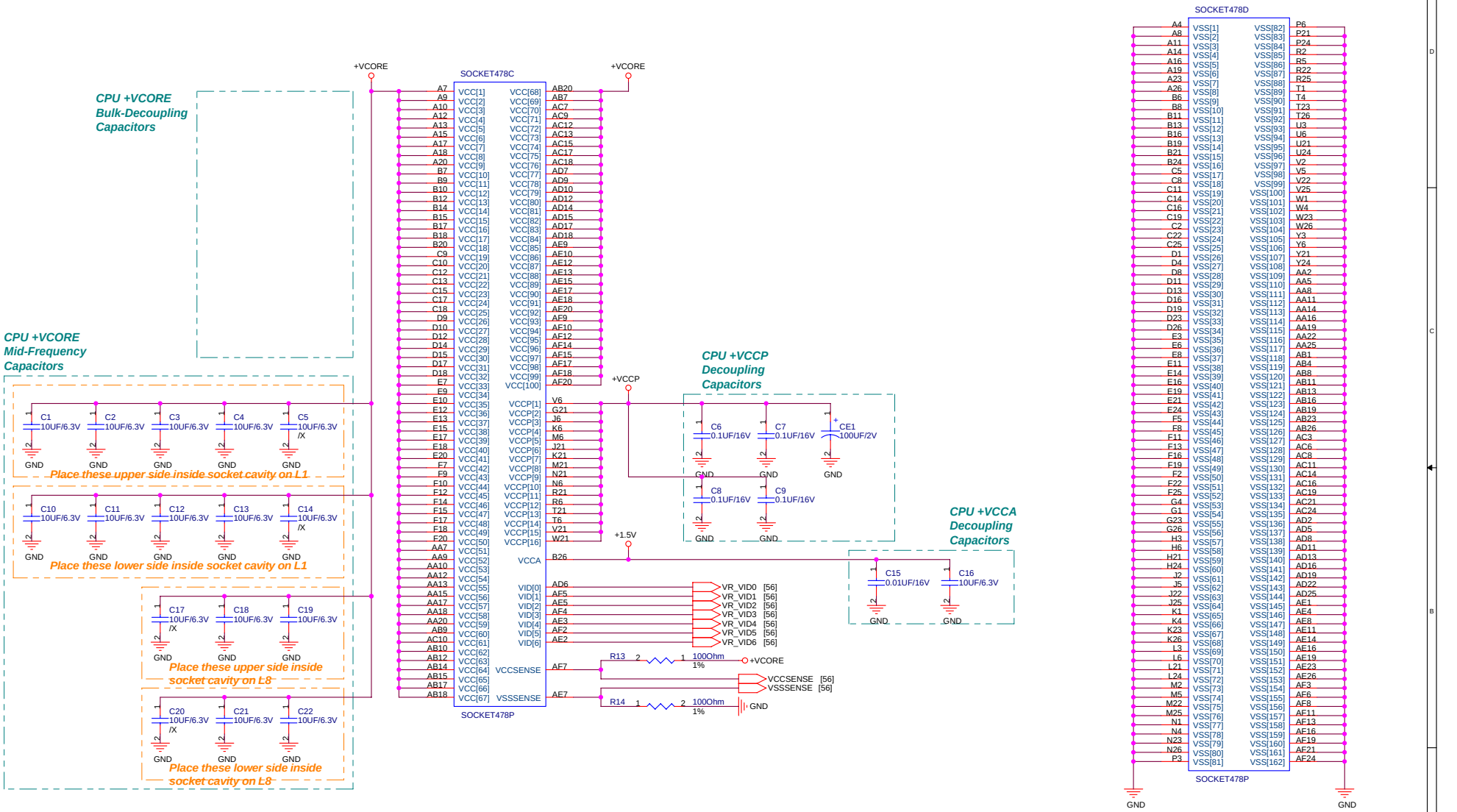
Title :	Blank
ASUSTeK COMPUTER INC	Engineer: Kell Huang
Size: A3	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 6 of 60


CR50 10MOhm /X
CX1 14.318Mhz
XIN_CLK
XOUT_CLK
+/-30ppm/20PF
CC28 27PF/50V
CC29 33PF/50V
GND
+3V
+3V_CLK
CL2
120Ohm/100Mhz
CC18 10UF/10V /X
CC19 0.1UF/16V
CC20 0.1UF/16V
CC21 0.1UF/16V
CC22 0.1UF/16V
CC23 0.1UF/16V
CC24 0.1UF/16V
CC25 0.1UF/16V
CC26 0.1UF/16V
CC27 0.1UF/16V
SMB_CLK_S
SMB_DAT_S
CC30 10PF/50V
CC31 10PF/50V
CLK_MODE
0 = Desktop Mode
1 = Mobile Mode
CR53 10KOhm
PEREQ0# control PCIE 0/1/4
CLK_NEWCARD_REQ#
CRN4D 4.7KOhm /X
PEREQ1# control PCIE 2/3/5
CLK_MINICARD_REQ#
CRN4C 4.7KOhm /X
U18
ICS9LPR600AGLF-T
VTTPWRGD/PD#/(CLK_Stop#)
VDDREF
FSL0/REF0_2x
FSL1/REF1_2x
X1
X2
GNDREF
GNDPCI1
FSL2/PCICLK0_2x
FS3/PCICLK1_2x
FS4/PCICLK2
(PCI_Stop#)/PCICLK3
GNDPCI2
VDDPCI1
Mode/PCICLK4
(PECLKREQ0#)/PCICLK5
(PECLKREQ1#)/PCICLK6
PCICLK7
VDDPCI2
GNDZ
ZCLK0
ZCLK1
VDDZ
VDD48
12MHz
SEL24_48#/24_48MHz
GND48
(CPU_Stop#)/RESET#
VDDCPU
CPUT_L0
CPUC_L0
GNDCPU
CPUT_L1
CPUC_L1
VDDA
SATACLKT_L
SATACLKC_L
GNDA
SCLK
SDATA
PCIeT_L0
PCIeC_L0
GNDPCIEX2
PCIeT_L1
PCIeC_L1
VDDPCIEX2
PCIeT_L2
PCIeC_L2
PCIeT_L3
PCIeC_L3
PCIeT_L4F
PCIeC_L4F
GNDPCIEX1
PCIeT_L5F
PCIeC_L5F
VDDPCIEX1
[44,56,58,59] VCCP_OK
[25] CLK_REF_307LV
[12] CLK_REF_NB
[18] CLK_REF_SB
CR10 0Ohm /X CLK_EN
CR54 33Ohm
CR15 33Ohm CLK_FSL0
CR17 33Ohm CLK_FSL1
XIN_CLK
XOUT_CLK
/PCIE_DEBUG
/DEBUG
CLK_FSL2
CLK_FS3
CLK_FS4
[31] CLK_PEDBPCI
[43] CLK_DBGPCI
[36] CLK_LANPCI
[17] CLK_SBPCI
[33] CLK_CBPCI
CR57 33Ohm
CR20 33Ohm
CR21 33Ohm
CR22 33Ohm
CR23 33Ohm
[18,21] STP_PCI#
[42] CLK_TPMPCI
[31] CLK_NEWCARD_REQ#
[30] CLK_MINICARD_REQ#
[44] CLK_ECPCI
CR26 33Ohm CLK_MODE
CR32 33Ohm CLK_PCI7
[12] CLK_ZCLK_NB
[17] CLK_ZCLK_SB
CR35 22Ohm CLK_ZCLK0
CR37 22Ohm CLK_ZCLK1
[19] CLK_USB_SB
CR41 33Ohm CLK_USB
[18,21,56] STP_CPU#
/ITP
CR11 33Ohm CLK_ITP_BCLK [9]
CR12 33Ohm CLK_ITP_BCLK# [9]
CR13 33Ohm CLK_CPU_BCLK [9]
CR16 33Ohm CLK_CPU_BCLK# [9]
CLK_CPU
CLK_CPU#
CR18 33Ohm CLK_NB_BCLK [11]
CR19 33Ohm CLK_NB_BCLK# [11]
CLK_NB
CLK_NB#
SMB_CLK_S [8,9,18,21,22,23,30,31,32]
SMB_DAT_S [8,9,18,21,22,23,30,31,32]
CLK_PCIE_LVDS_R
CLK_PCIE_LVDS#_R
CR24 33Ohm CLK_PCIE_LVDS [25]
CR25 33Ohm CLK_PCIE_LVDS# [25]
CLK_PCIE_NB_R
CLK_PCIE_NB#_R
CR28 33Ohm CLK_PCIE_NB [13]
CR31 33Ohm CLK_PCIE_NB# [13]
CLK_PCIE_MINICARD_R
CLK_PCIE_MINICARD#_R
CLK_PCIE_SB_R
CLK_PCIE_SB#_R
CLK_PCIE_NEWCARD_R
CLK_PCIE_NEWCARD#_R
CR33 33Ohm CLK_PCIE_MINICARD [30]
CR34 33Ohm CLK_PCIE_MINICARD# [30]
CR36 33Ohm CLK_PCIE_SB [18]
CR38 33Ohm CLK_PCIE_SB# [18]
CR39 33Ohm CLK_PCIE_NEWCARD [31]
CR40 33Ohm CLK_PCIE_NEWCARD# [31]
/ESATA
CLK_PCIE_ESATA_R
CLK_PCIE_ESATA#_R
CR42 33Ohm CLK_PCIE_ESATA [32]
CR43 33Ohm CLK_PCIE_ESATA# [32]
FS4 FS3 FSL2 FSL1 FSL0 CPU PCI ZCLK PCIE SATA
0 1 0 0 1 133 33 133 100 100
0 1 0 1 1 166 33 133 100 100
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
+VCCP
CRN5C 10KOhm
CRN5B 10KOhm
CRN5A 10KOhm
CRN5D 10KOhm
[9] CPU_BSEL0
[9,12] CPU_BSEL1
[9] CPU_BSEL2
0OHM CRN1B
0OHM CRN1A
0OHM CRN1C
0OHM CRN1D
4.7KOhm CRN2A CLK_FSL0
4.7KOhm CRN2B CLK_FSL1
4.7KOhm CRN2C CLK_FSL2
4.7KOhm CRN2D
CR48 1KOhm /X
CR49 1KOhm /X
CLK_REF_307LV CC61 /X
CLK_REF_NB CC35 /X
CLK_REF_SB CC37 /X
CLK_DBGPCI CC39 /X
CLK_TPMPCI CC41 /X
CLK_SBPCI CC43 /X
CLK_LANPCI CC45 /X
CLK_CBPCI CC47 /X
CLK_ECPCI CC49 /X
CLK_ZCLK_NB CC51 /X
CLK_ZCLK_SB CC53 /X
CLK_USB_SB CC55 /X
CLK_PEDBPCI CC63 /X
/DEBUG/X
/PCIE_DEBUG/X
CLK_ITP_BCLK CC32 /ITP/X
CLK_ITP_BCLK# CC33 /ITP/X
CLK_CPU_BCLK CC34 /X
CLK_CPU_BCLK# CC36 /X
CLK_NB_BCLK CC38 /X
CLK_NB_BCLK# CC40 /X
CLK_PCIE_NB CC42 /X
CLK_PCIE_NB# CC44 /X
CLK_PCIE_SB CC46 /X
CLK_PCIE_SB# CC48 /X
CLK_PCIE_LVDS CC50 /X
CLK_PCIE_LVDS# CC52 /X
CLK_PCIE_MINICARD CC54 /X
CLK_PCIE_MINICARD# CC56 /X
CLK_PCIE_NEWCARD CC57 /X
CLK_PCIE_NEWCARD# CC58 /X
CLK_PCIE_ESATA CC59 /ESATA/X
CLK_PCIE_ESATA# CC60 /ESATA/X
CLK_FS3
0 = FS3 Low Level
1 = FS3 High Level
CR55 10KOhm
CRN4B /X
CLK_FS4
0 = FS4 Low Level
1 = FS4 High Level
CR56 10KOhm /X
CRN4A /X
CR52 10KOhm
CR51 10KOhm /X
CQ1 H2N7002
CC62 0.1UF/16V /X
[56] CLK_EN#
Title : CLOCK GEN-ICS9LPR600
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 7 of 60



ASUSTeK COMPUTER INC.	Title : CLOCK BUF-ICS9P935		
	Engineer: Kell Huang		
Size: A3	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 8 of 60		

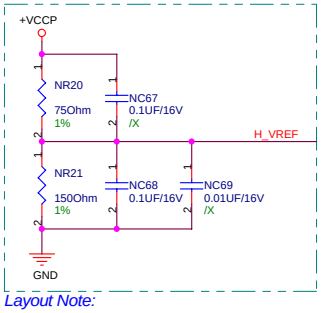

SOCKET478A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
SOCKET478P
CPU Debug Port
TPC26T
AGTL+ I/O Voltage Reference
Default Strapping When Not Used
SOCKET478B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
AGTL+ I/O Buffer Compensation
ITP
FPC_CON_30P
/ITP
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 9 of 60



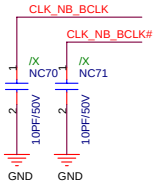
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

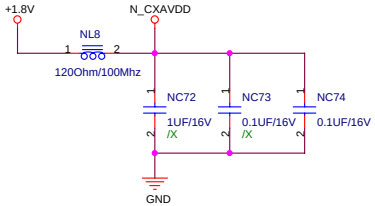
ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 10 of 60	

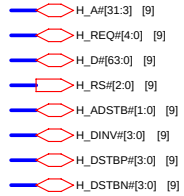
AGTL+ I/O Voltage Reference

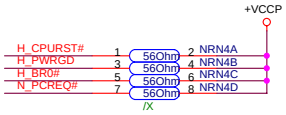


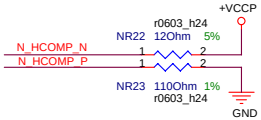
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.







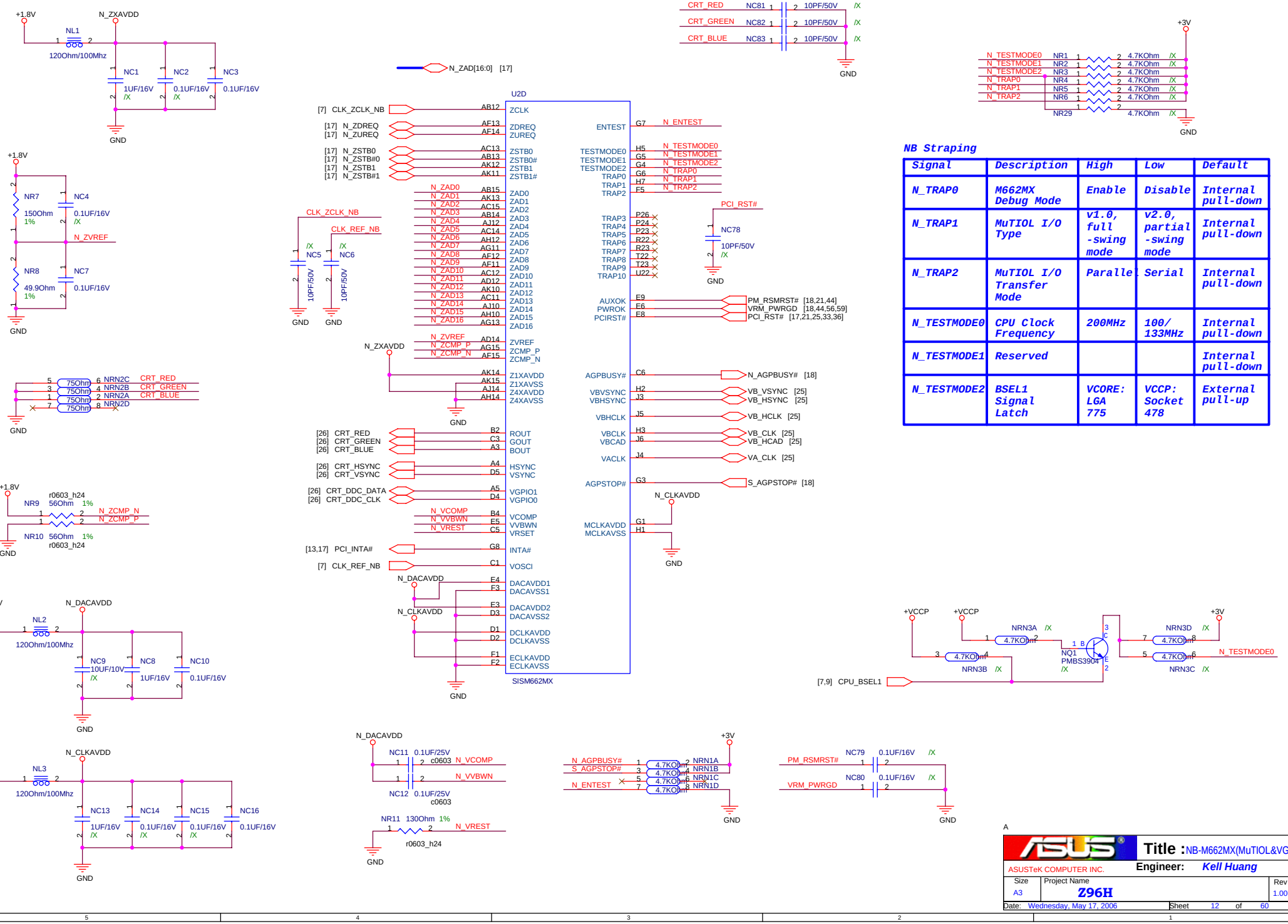


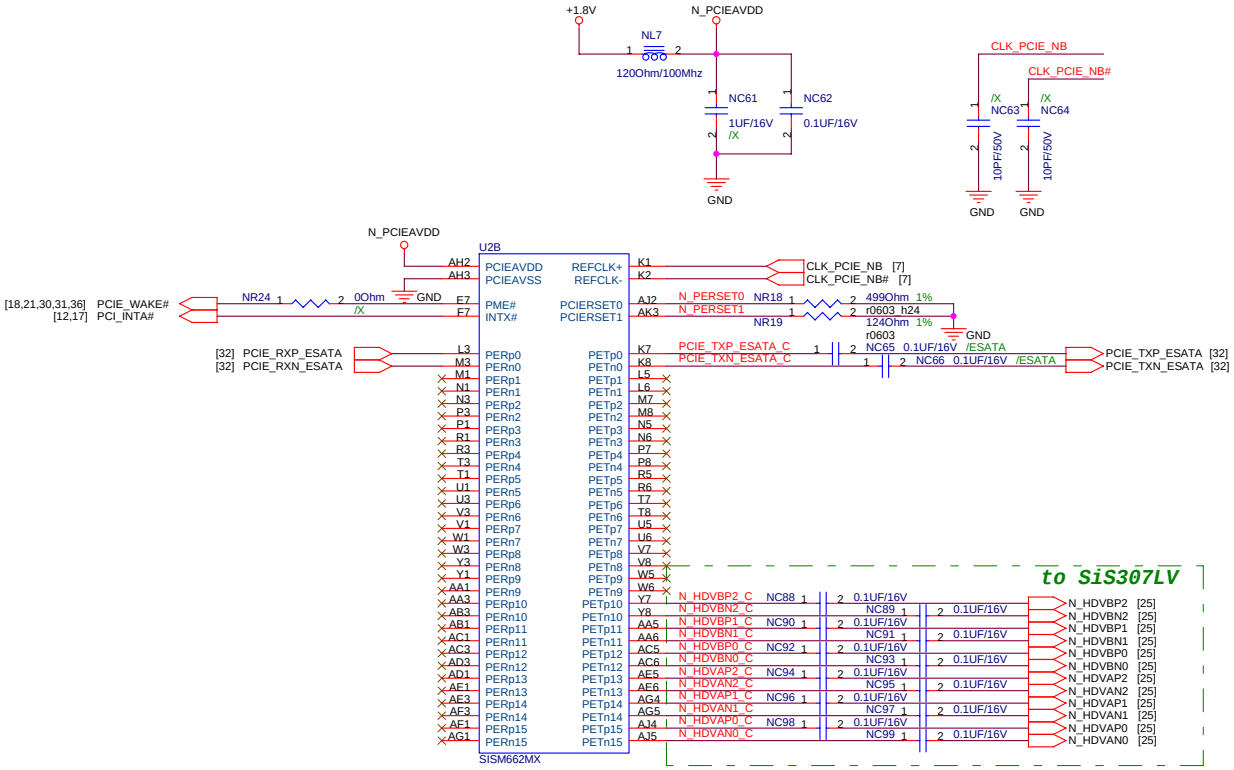


NR22 should be 1%

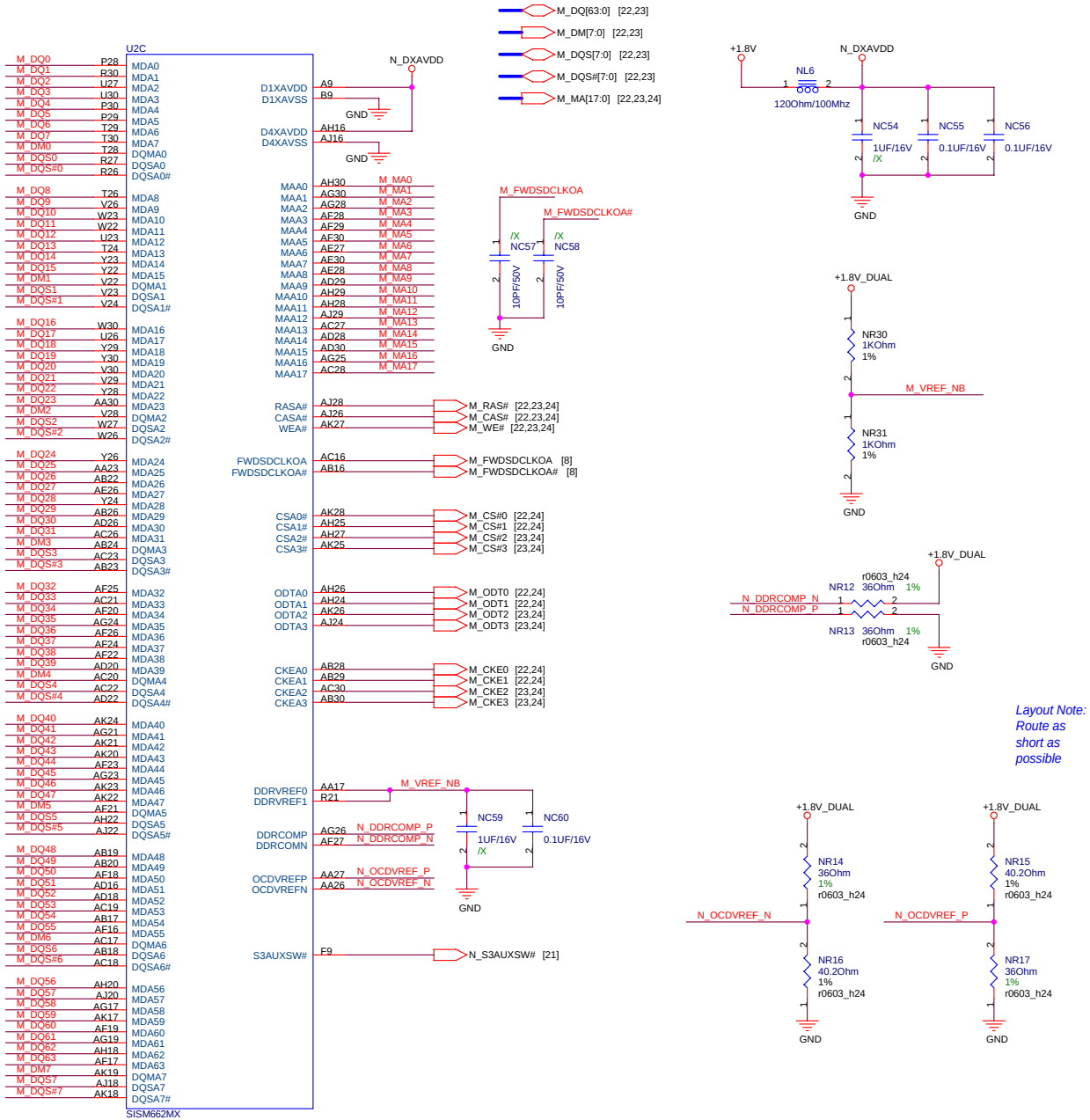
Trace should be 10 mil wide with 20 mil spacing

ASUSTeK COMPUTER INC.	Title : NB-M662MX(HOST)	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 11 of 60	

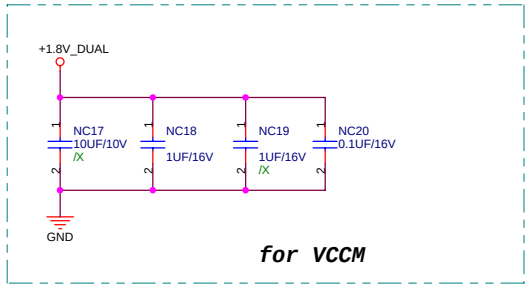

+1.8V
N_ZXAVDD
NL1
120Ohm/100Mhz
NC1 1UF/16V /X
NC2 0.1UF/16V /X
NC3 0.1UF/16V
GND
NR7 150Ohm 1%
NC4 0.1UF/16V /X
N_ZVREF
NR8 49.9Ohm 1%
NC7 0.1UF/16V
CRT_RED NC81 10PF/50V /X
CRT_GREEN NC82 10PF/50V /X
CRT_BLUE NC83 10PF/50V /X
N_ZAD[16:0] [17]
U2D
[7] CLK_ZCLK_NB
[17] N_ZDREQ
[17] N_ZUREQ
[17] N_ZSTB0
[17] N_ZSTB#0
[17] N_ZSTB1
[17] N_ZSTB#1
CLK_ZCLK_NB
CLK_REF_NB
NC5 10PF/50V /X
NC6 10PF/50V /X
PCI_RST#
NC78 10PF/50V /X
ENTEST
TESTMODE0
TESTMODE1
TESTMODE2
TRAP0
TRAP1
TRAP2
TRAP3
TRAP4
TRAP5
TRAP6
TRAP7
TRAP8
TRAP9
TRAP10
AUXOK
PWROK
PCIRST#
PM_RSMRST# [18,21,44]
VRM_PWRGD [18,44,56,59]
PCI_RST# [17,21,25,33,36]
N_ZXAVDD
AGPBUSY#
VBVSYNC
VBHSYNC
VBHCLK
VBCLK
VBCAD
VACLK
AGPSTOP#
N_AGPBUSY# [18]
VB_VSYNC [25]
VB_HSYNC [25]
VB_HCLK [25]
VB_CLK [25]
VB_HCAD [25]
VA_CLK [25]
S_AGPSTOP# [18]
N_CLKAVDD
MCLKAVDD
MCLKAVSS
CRT_RED
CRT_GREEN
CRT_BLUE
NR2N 75Ohm
NR2B 75Ohm
NR2A 75Ohm
NR2D 75Ohm
[26] CRT_RED
[26] CRT_GREEN
[26] CRT_BLUE
[26] CRT_HSYNC
[26] CRT_VSYNC
[26] CRT_DDC_DATA
[26] CRT_DDC_CLK
[13,17] PCI_INTA#
[7] CLK_REF_NB
N_VCOMP
N_VVBWN
N_VREST
N_DACAVDD
N_CLKAVDD
SISM662MX
+3V
N_TESTMODE0 NR1 4.7KOhm /X
N_TESTMODE1 NR2 4.7KOhm /X
N_TESTMODE2 NR3 4.7KOhm
N_TRAP0 NR4 4.7KOhm /X
N_TRAP1 NR5 4.7KOhm /X
N_TRAP2 NR6 4.7KOhm /X
NR29 4.7KOhm /X
NB Straping
Signal | Description | High | Low | Default
N_TRAP0 | M662MX Debug Mode | Enable | Disable | Internal pull-down
N_TRAP1 | MuTIOL I/O Type | v1.0, full-swing mode | v2.0, partial-swing mode | Internal pull-down
N_TRAP2 | MuTIOL I/O Transfer Mode | Parallel | Serial | Internal pull-down
N_TESTMODE0 | CPU Clock Frequency | 200MHz | 100/133MHz | Internal pull-down
N_TESTMODE1 | Reserved | | | Internal pull-down
N_TESTMODE2 | BSEL1 Signal Latch | VCORE: LGA 775 | VCCP: Socket 478 | External pull-up
+VCCP
NRN3A /X
NRN3B /X
NQ1 PMBS3904 /X
NRN3D /X
NRN3C /X
N_TESTMODE0
[7,9] CPU_BSEL1
NL2
NC9 10UF/10V /X
NC8 1UF/16V
NC10 0.1UF/16V
NL3
NC13 1UF/16V /X
NC14 0.1UF/16V /X
NC15 0.1UF/16V /X
NC16 0.1UF/16V
NC11 0.1UF/25V c0603 N_VCOMP
NC12 0.1UF/25V c0603 N_VVBWN
NR11 130Ohm 1% r0603_h24 N_VREST
NR9 56Ohm 1% r0603_h24 N_ZCMP_N
NR10 56Ohm 1% r0603_h24 N_ZCMP_P
N_AGPBUSY#
S_AGPSTOP#
N_ENTEST
NRN1A
NRN1B
NRN1C
NRN1D
PM_RSMRST#
VRM_PWRGD
NC79 0.1UF/16V /X
NC80 0.1UF/16V /X
ASUSTeK COMPUTER INC.
Title : NB-M662MX(MuTIOL&VGA)
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 12 of 60

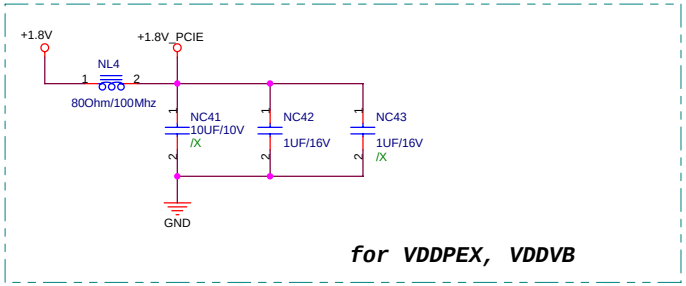


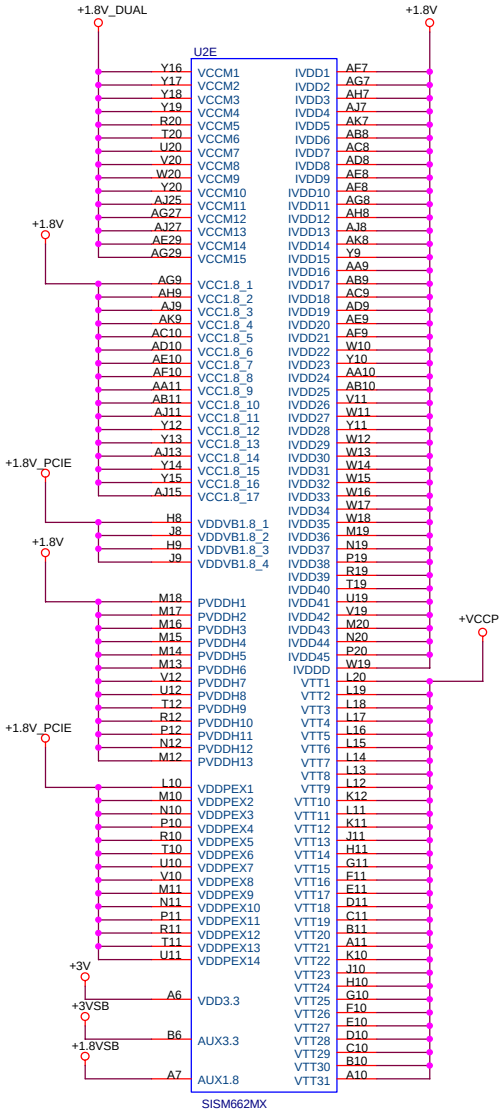
ASUSTeK COMPUTER INC.	Title : NB-M662MX(PCIE)		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 13 of 60		

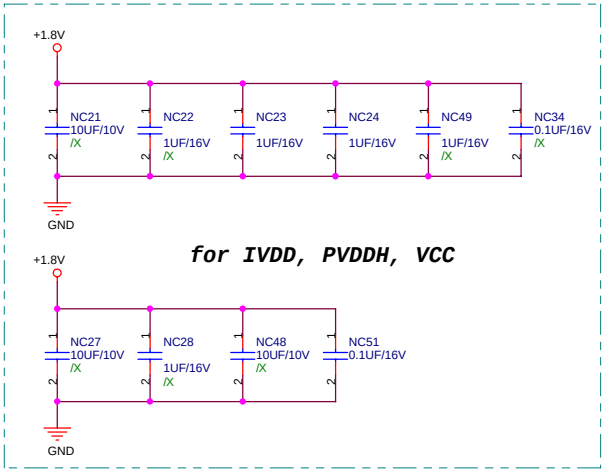


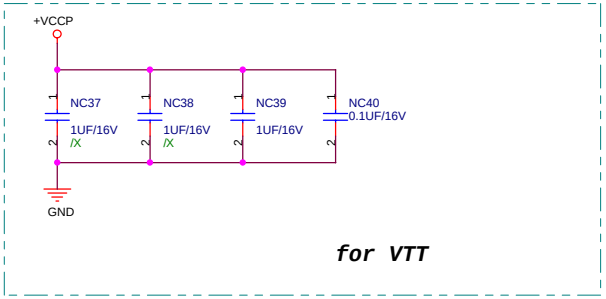
Title :	NB-M662MX(DDR2)	
ASUSTeK COMPUTER INC.	Engineer:	Kell Huang
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 14 of 60	

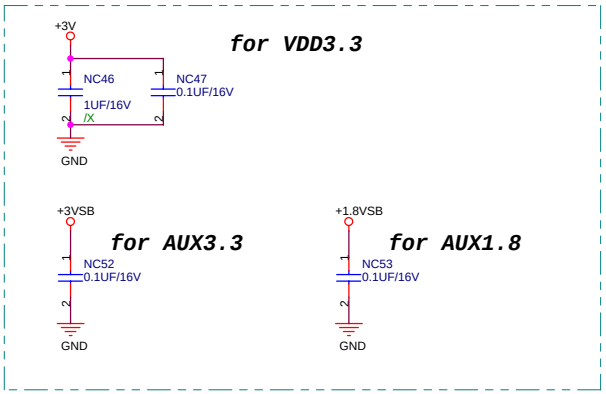






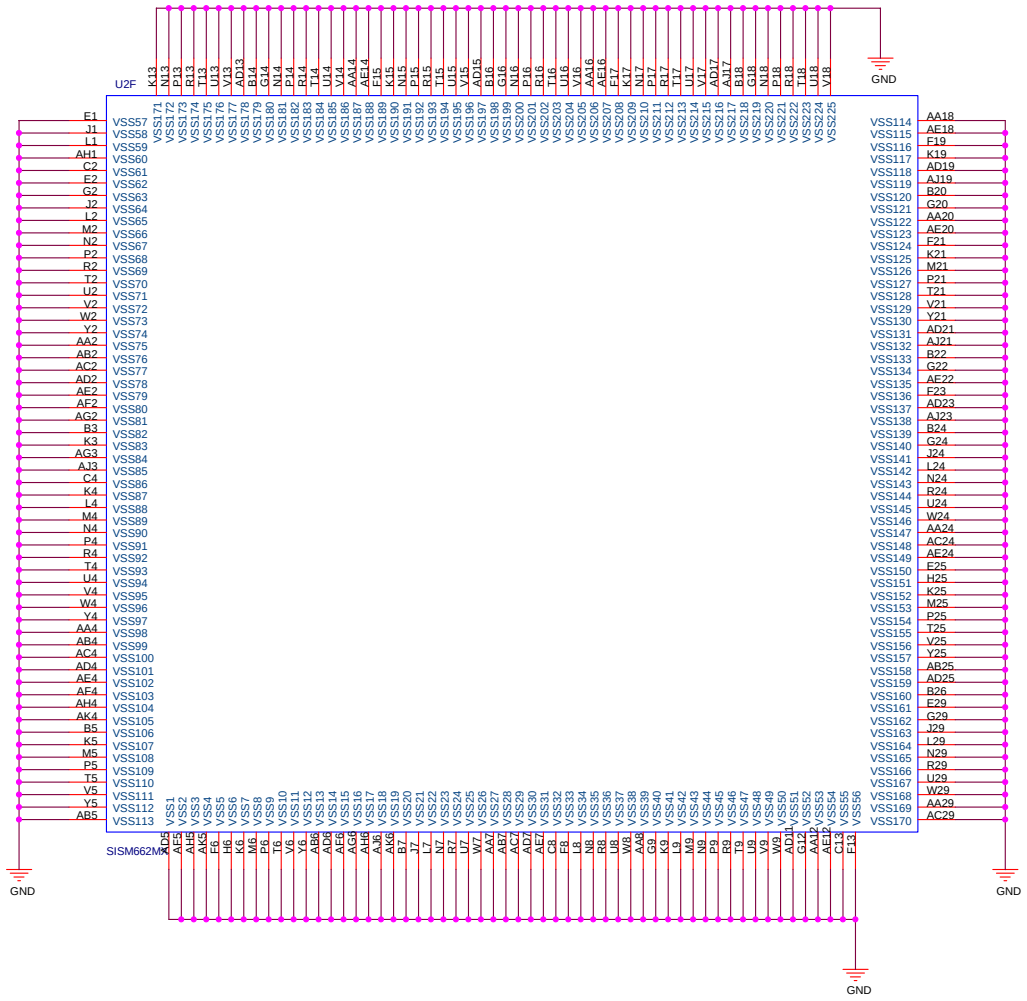




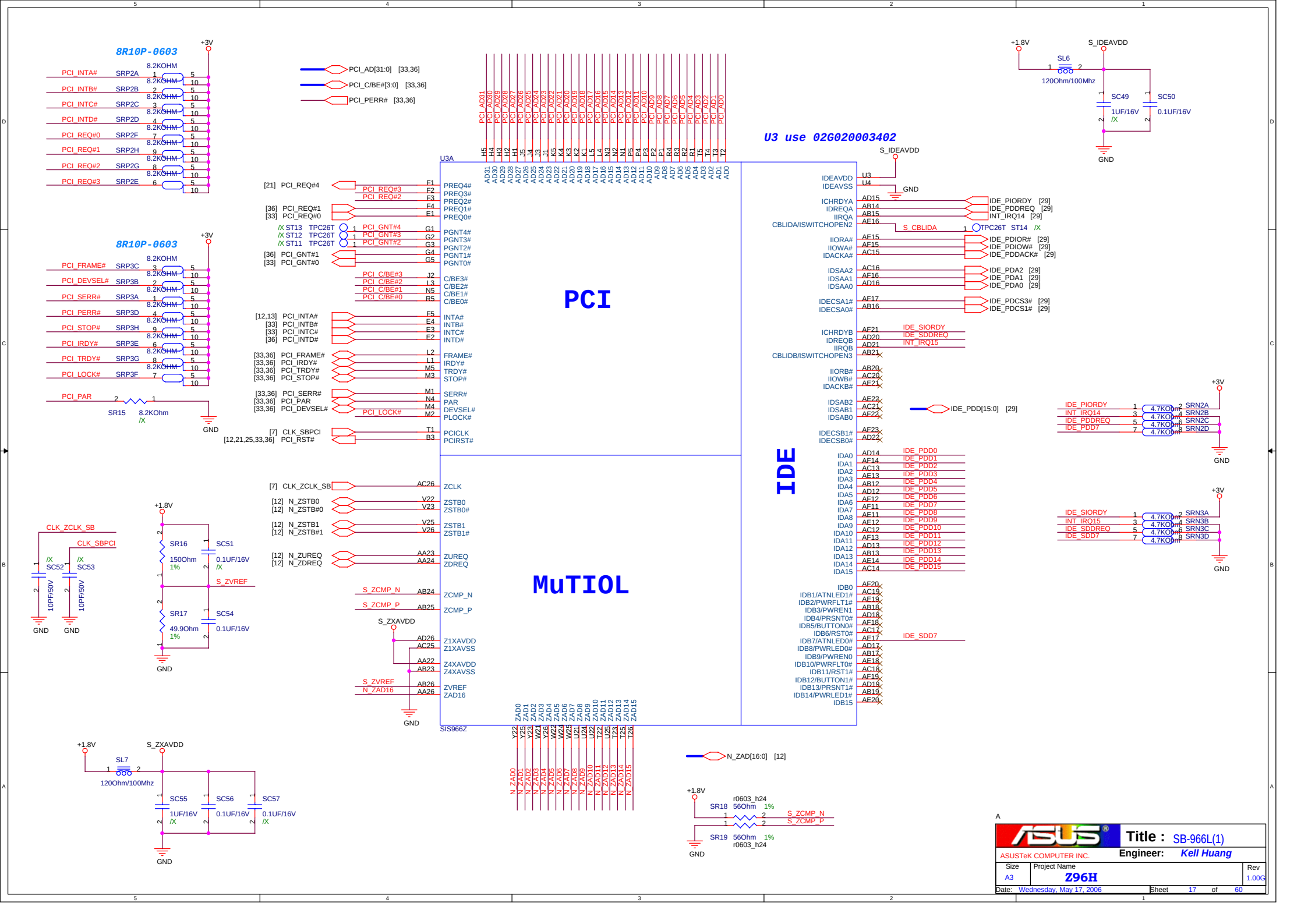


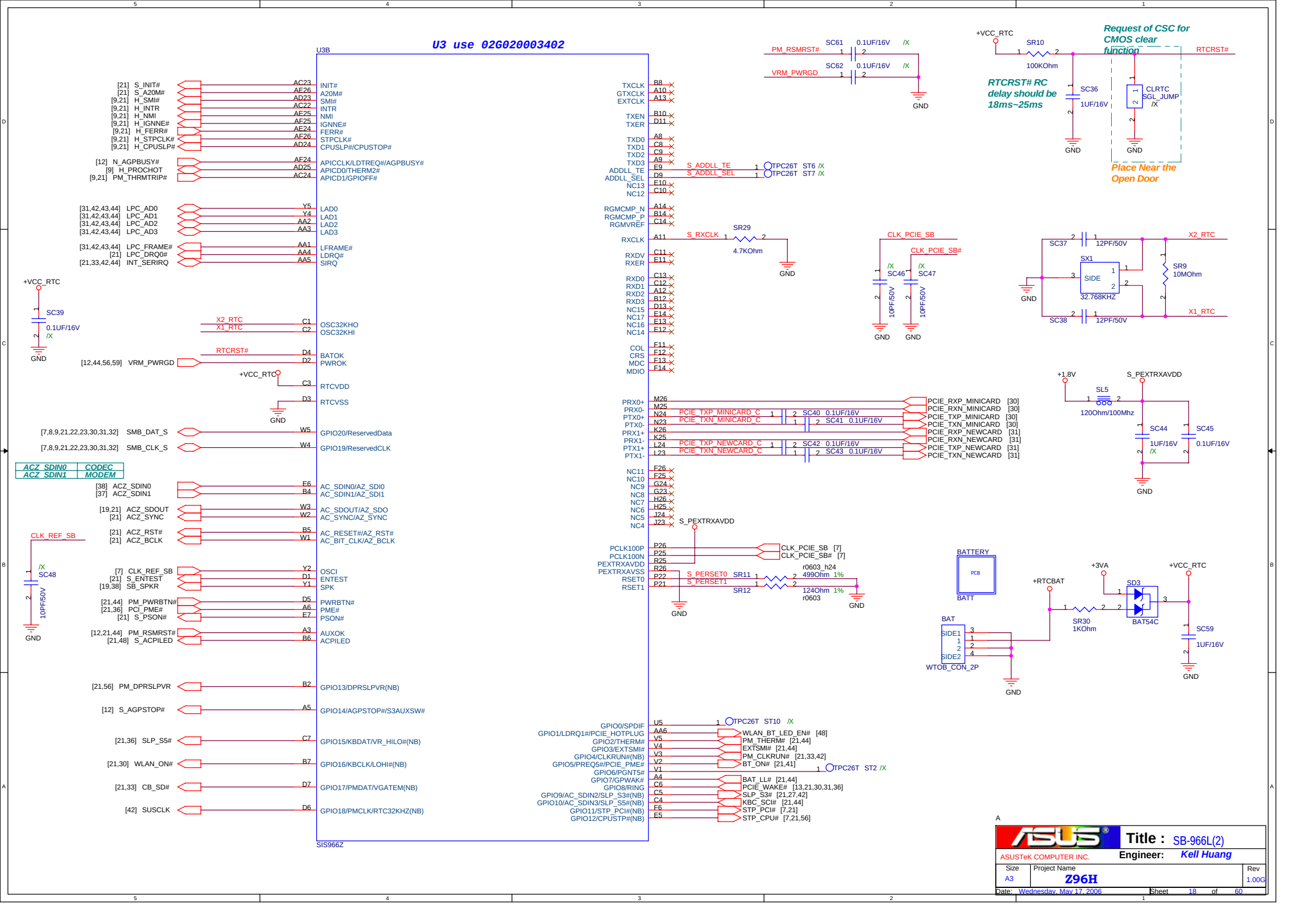
A

ASUSTeK COMPUTER INC.	Title : NB-M662MX(PWR)	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 15 of 60	

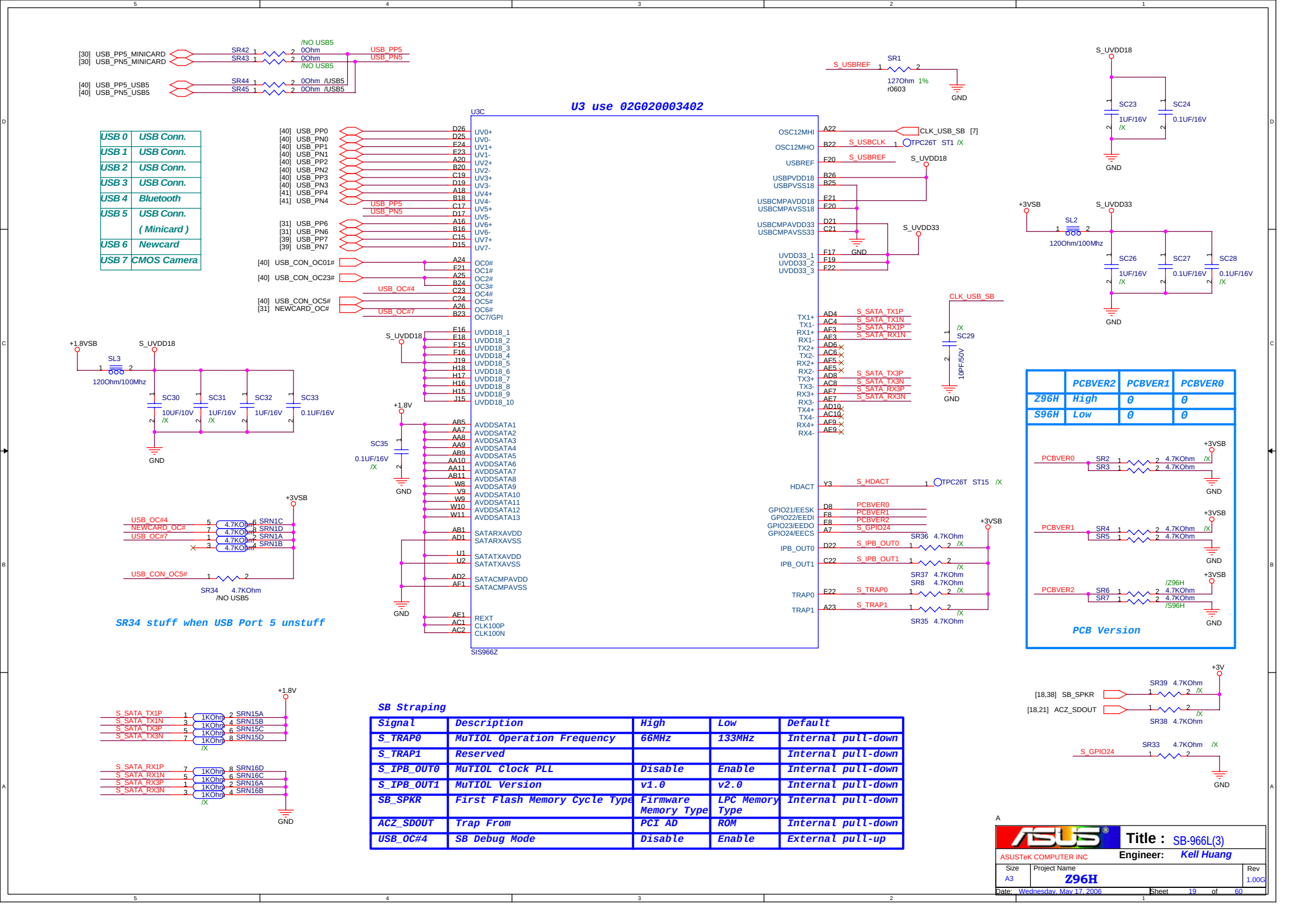


ASUSTeK COMPUTER INC.	Title : NB-M662MX(GND)		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 16 of 60		

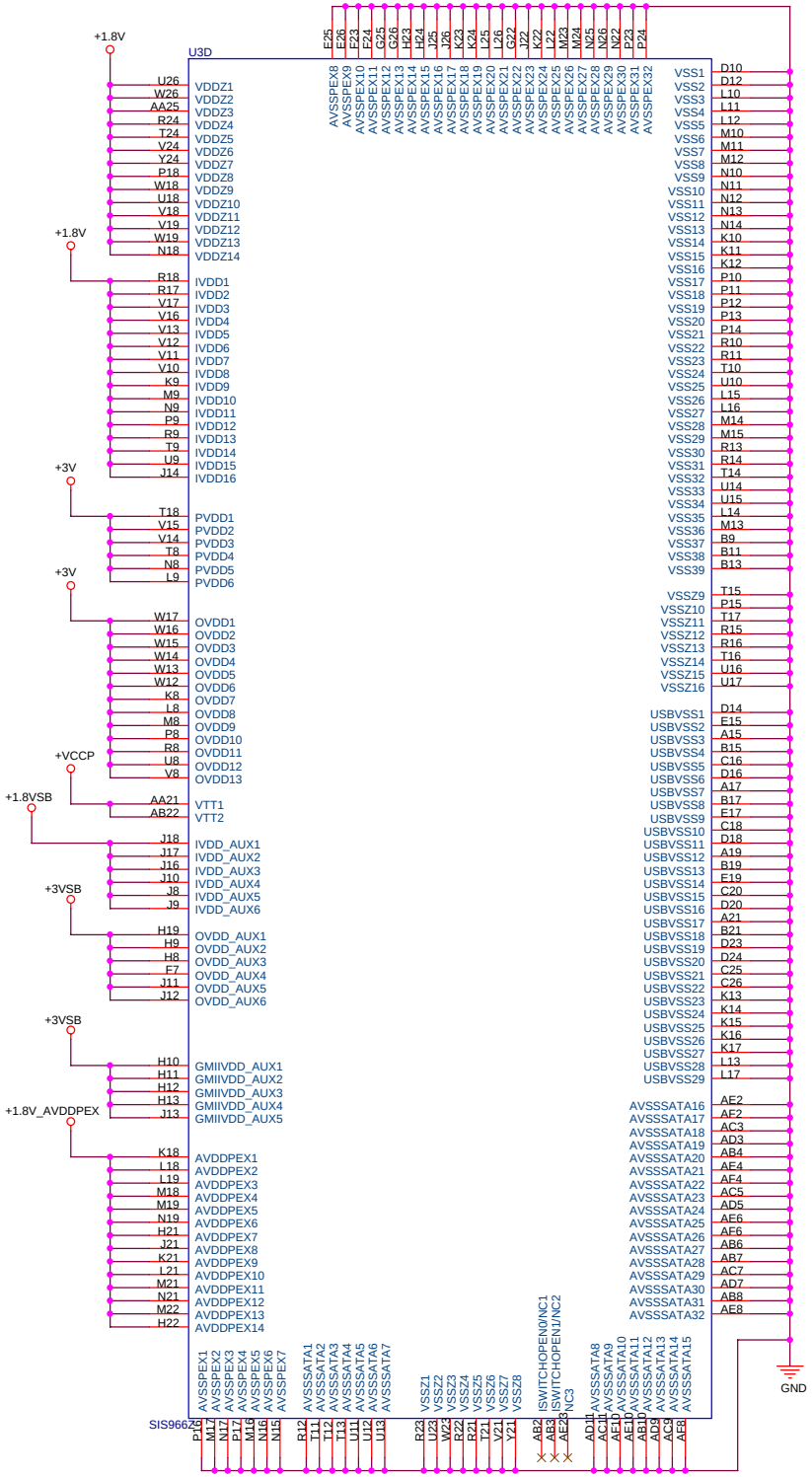

8R10P-0603
+3V
PCI_INTA# SRP2A
PCI_INTB# SRP2B
PCI_INTC# SRP2C
PCI_INTD# SRP2D
PCI_REQ#0 SRP2F
PCI_REQ#1 SRP2H
PCI_REQ#2 SRP2G
PCI_REQ#3 SRP2E
8.2KOHM
8R10P-0603
PCI_FRAME# SRP3C
PCI_DEVSEL# SRP3B
PCI_SERR# SRP3A
PCI_PERR# SRP3D
PCI_STOP# SRP3H
PCI_IRDY# SRP3E
PCI_TRDY# SRP3G
PCI_LOCK# SRP3F
PCI_PAR
SR15 8.2KOhm /X
GND
PCI_AD[31:0] [33,36]
PCI_C/BE#[3:0] [33,36]
PCI_PERR# [33,36]
U3A
PCI
[21] PCI_REQ#4
PCI_REQ#3
PCI_REQ#2
[36] PCI_REQ#1
[33] PCI_REQ#0
/X ST13 TPC26T
/X ST12 TPC26T
/X ST11 TPC26T
PCI_GNT#4
PCI_GNT#3
PCI_GNT#2
[36] PCI_GNT#1
[33] PCI_GNT#0
PCI_C/BE#3
PCI_C/BE#2
PCI_C/BE#1
PCI_C/BE#0
[12,13] PCI_INTA#
[33] PCI_INTB#
[33] PCI_INTC#
[36] PCI_INTD#
[33,36] PCI_FRAME#
[33,36] PCI_IRDY#
[33,36] PCI_TRDY#
[33,36] PCI_STOP#
[33,36] PCI_SERR#
[33,36] PCI_PAR
[33,36] PCI_DEVSEL#
PCI_LOCK#
[7] CLK_SBPCI
[12,21,25,33,36] PCI_RST#
PREQ4#
PREQ3#
PREQ2#
PREQ1#
PREQ0#
PGNT4#
PGNT3#
PGNT2#
PGNT1#
PGNT0#
C/BE3#
C/BE2#
C/BE1#
C/BE0#
INTA#
INTB#
INTC#
INTD#
FRAME#
IRDY#
TRDY#
STOP#
SERR#
PAR
DEVSEL#
PLOCK#
PCICLK
PCIRST#
SIS966Z
MuTIOL
[7] CLK_ZCLK_SB
[12] N_ZSTB0
[12] N_ZSTB0#
[12] N_ZSTB1
[12] N_ZSTB1#
[12] N_ZUREQ
[12] N_ZDREQ
S_ZCMP_N
S_ZCMP_P
S_ZXAVDD
S_ZVREF
N_ZAD16
ZCLK
ZSTB0
ZSTB0#
ZSTB1
ZSTB1#
ZUREQ
ZDREQ
ZCMP_N
ZCMP_P
Z1XAVDD
Z1XAVSS
Z4XAVDD
Z4XAVSS
ZVREF
ZAD16
N_ZAD[16:0] [12]
U3 use 02G020003402
IDE
S_IDEAVDD
IDEAVDD
IDEAVSS
ICHRDYA
IDREQA
IIRQA
CBLIDA/ISWITCHOPEN2
IIORA#
IIOWA#
IDACKA#
IDSAA2
IDSAA1
IDSAA0
IDECSA1#
IDECSA0#
ICHRDYB
IDREQB
IIRQB
CBLIDB/ISWITCHOPEN3
IIORB#
IIOWB#
IDACKB#
IDSAB2
IDSAB1
IDSAB0
IDECSB1#
IDECSB0#
IDA0
IDA1
IDA2
IDA3
IDA4
IDA5
IDA6
IDA7
IDA8
IDA9
IDA10
IDA11
IDA12
IDA13
IDA14
IDA15
IDB0
IDB1/ATNLED1#
IDB2/PWRFLT1#
IDB3/PWREN1
IDB4/PRSNT0#
IDB5/BUTTON0#
IDB6/RST0#
IDB7/ATNLED0#
IDB8/PWRLED0#
IDB9/PWREN0
IDB10/PWRFLT0#
IDB11/RST1#
IDB12/BUTTON1#
IDB13/PRSNT1#
IDB14/PWRLED1#
IDB15
IDE_PIORDY [29]
IDE_PDDREQ [29]
INT_IRQ14 [29]
S_CBLIDA
TPC26T ST14 /X
IDE_PDIOR# [29]
IDE_PDIOW# [29]
IDE_PDDACK# [29]
IDE_PDA2 [29]
IDE_PDA1 [29]
IDE_PDA0 [29]
IDE_PDCS3# [29]
IDE_PDCS1# [29]
IDE_SIORDY
IDE_SDDREQ
INT_IRQ15
IDE_PDD[15:0] [29]
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_SDD7
+1.8V
S_IDEAVDD
SL6
120Ohm/100Mhz
SC49 1UF/16V /X
SC50 0.1UF/16V /X
GND
IDE_PIORDY
INT_IRQ14
IDE_PDDREQ
IDE_PDD7
4.7KOhm
SRN2A
SRN2B
SRN2C
SRN2D
IDE_SIORDY
INT_IRQ15
IDE_SDDREQ
IDE_SDD7
SRN3A
SRN3B
SRN3C
SRN3D
CLK_ZCLK_SB
CLK_SBPCI
SC52 /X 10PF/50V
SC53 /X 10PF/50V
+1.8V
SR16 150Ohm 1%
SC51 0.1UF/16V /X
S_ZVREF
SR17 49.9Ohm 1%
SC54 0.1UF/16V
SL7
120Ohm/100Mhz
SC55 1UF/16V /X
SC56 0.1UF/16V /X
SC57 0.1UF/16V /X
SR18 56Ohm 1%
SR19 56Ohm 1%
r0603_h24
Title : SB-966L(1)
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 17 of 60

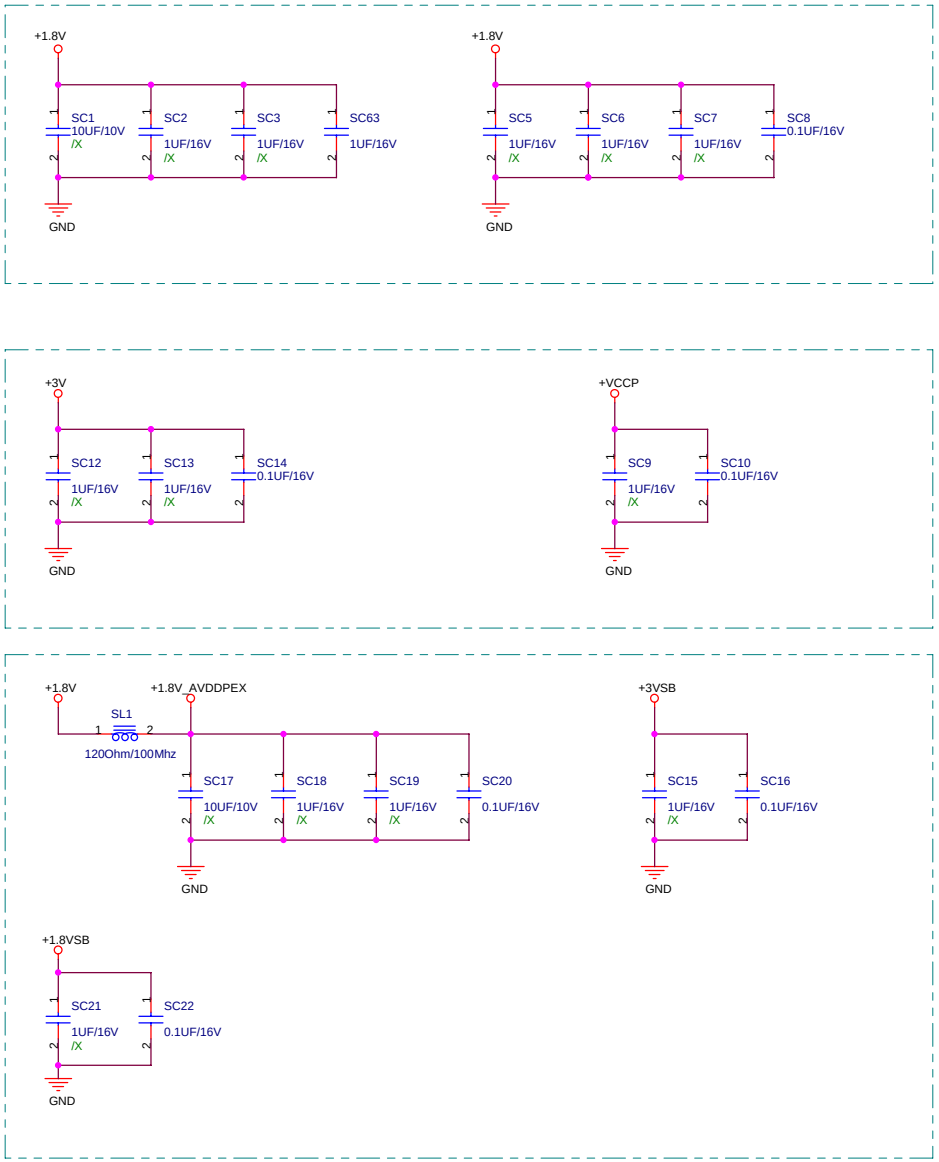


Title :	SB-966L(2)
ASUSTeK COMPUTER INC.	Engineer: Kell Huang
Size: A3	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 18 of 60

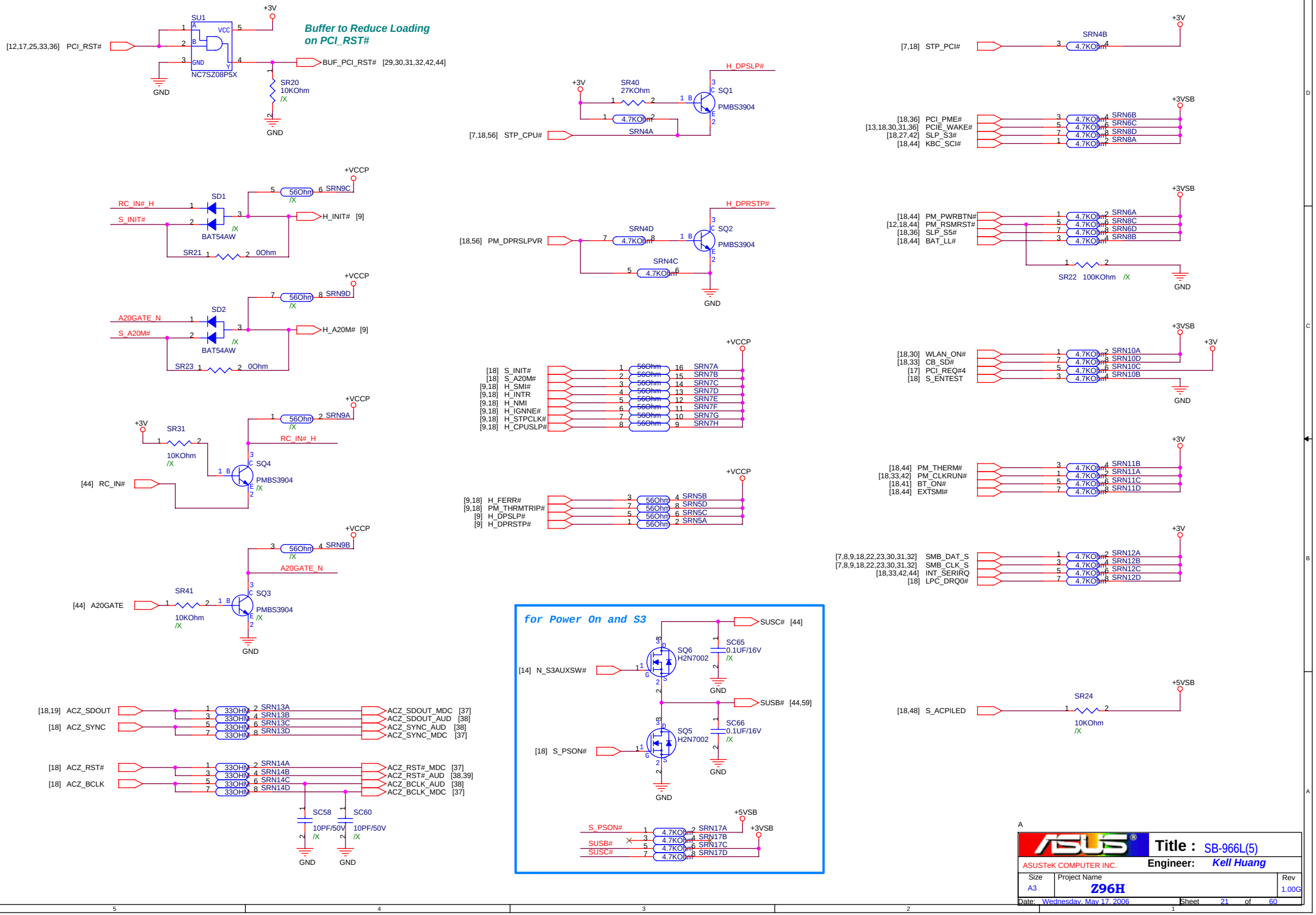

U3 use 02G020003402
U3C
SIS966Z
[30] USB_PP5_MINICARD
[30] USB_PN5_MINICARD
[40] USB_PP5_USB5
[40] USB_PN5_USB5
SR42 SR43 SR44 SR45
/NO USB5
0Ohm
0Ohm /USB5
USB_PP5
USB_PN5
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 USB Conn. (Minicard)
USB 6 Newcard
USB 7 CMOS Camera
[40] USB_PP0
[40] USB_PN0
[40] USB_PP1
[40] USB_PN1
[40] USB_PP2
[40] USB_PN2
[40] USB_PP3
[40] USB_PN3
[41] USB_PP4
[41] USB_PN4
[31] USB_PP6
[31] USB_PN6
[39] USB_PP7
[39] USB_PN7
[40] USB_CON_OC01#
[40] USB_CON_OC23#
[40] USB_CON_OC5#
[31] NEWCARD_OC#
USB_OC#4
USB_OC#7
S_USBREF
SR1
127Ohm 1%
r0603
GND
OSC12MHI
OSC12MHO
USBREF
USBPVDD18
USBPVSS18
USBCMPAVDD18
USBCMPAVSS18
USBCMPAVDD33
USBCMPAVSS33
UVDD33_1
UVDD33_2
UVDD33_3
CLK_USB_SB [7]
S_USBCLK
TPC26T ST1 /X
S_UVDD18
S_UVDD33
SC23 SC24
1UF/16V /X
0.1UF/16V
SL2
120Ohm/100Mhz
SC26 SC27 SC28
+3VSB
+1.8VSB
SL3
SC30 SC31 SC32 SC33
10UF/10V
SC35
0.1UF/16V /X
UVDD18_1
UVDD18_2
UVDD18_3
UVDD18_4
UVDD18_5
UVDD18_6
UVDD18_7
UVDD18_8
UVDD18_9
UVDD18_10
AVDDSATA1
AVDDSATA2
AVDDSATA3
AVDDSATA4
AVDDSATA5
AVDDSATA6
AVDDSATA7
AVDDSATA8
AVDDSATA9
AVDDSATA10
AVDDSATA11
AVDDSATA12
AVDDSATA13
SATARXAVDD
SATARXAVSS
SATATXAVDD
SATATXAVSS
SATACMPAVDD
SATACMPAVSS
REXT
CLK100P
CLK100N
TX1+ TX1- RX1+ RX1- TX2+ TX2- RX2+ RX2- TX3+ TX3- RX3+ RX3- TX4+ TX4- RX4+ RX4-
S_SATA_TX1P
S_SATA_TX1N
S_SATA_RX1P
S_SATA_RX1N
S_SATA_TX3P
S_SATA_TX3N
S_SATA_RX3P
S_SATA_RX3N
CLK_USB_SB
SC29
10PF/50V
HDACT
S_HDACT
TPC26T ST15 /X
GPIO21/EESK
GPIO22/EEDI
GPIO23/EEDO
GPIO24/EECS
PCBVER0
PCBVER1
PCBVER2
S_GPIO24
IPB_OUT0
IPB_OUT1
S_IPB_OUT0
S_IPB_OUT1
SR36 4.7KOhm
SR37 4.7KOhm
SR8 4.7KOhm
SR35 4.7KOhm
TRAP0
TRAP1
S_TRAP0
S_TRAP1
SRN1C SRN1D SRN1A SRN1B
SR34 4.7KOhm /NO USB5
SR34 stuff when USB Port 5 unstuff
PCBVER2 PCBVER1 PCBVER0
Z96H High 0 0
S96H Low 0 0
PCB Version
SR2 SR3 SR4 SR5 SR6 SR7
4.7KOhm /X
/Z96H
/S96H
[18,38] SB_SPKR
[18,21] ACZ_SDOUT
SR39 4.7KOhm /X
SR38 4.7KOhm /X
SR33 4.7KOhm /X
S_SATA_TX1P
S_SATA_TX1N
S_SATA_TX3P
S_SATA_TX3N
S_SATA_RX1P
S_SATA_RX1N
S_SATA_RX3P
S_SATA_RX3N
SRN15A SRN15B SRN15C SRN15D
SRN16D SRN16C SRN16A SRN16B
1KOhm /X
SB Straping
Signal | Description | High | Low | Default
S_TRAP0 | MuTIOL Operation Frequency | 66MHz | 133MHz | Internal pull-down
S_TRAP1 | Reserved | | | Internal pull-down
S_IPB_OUT0 | MuTIOL Clock PLL | Disable | Enable | Internal pull-down
S_IPB_OUT1 | MuTIOL Version | v1.0 | v2.0 | Internal pull-down
SB_SPKR | First Flash Memory Cycle Type | Firmware Memory Type | LPC Memory Type | Internal pull-down
ACZ_SDOUT | Trap From | PCI AD | ROM | Internal pull-down
USB_OC#4 | SB Debug Mode | Disable | Enable | External pull-up
ASUSTeK COMPUTER INC
Title : SB-966L(3)
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 19 of 60

U3 use 02G020003402





ASUSTeK COMPUTER INC.	Title : SB-966L(4)	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 20 of 60	


Buffer to Reduce Loading on PCI_RST#
SU1
NC7SZ08P5X
[12,17,25,33,36] PCI_RST#
BUF_PCI_RST# [29,30,31,32,42,44]
SR20 10KOhm /X
+3V
GND
SD1
BAT54AW
RC_IN#_H
S_INIT#
H_INIT# [9]
SR21 0Ohm
SRN9C
SD2
A20GATE_N
S_A20M#
H_A20M# [9]
SR23 0Ohm
SRN9D
SR31 10KOhm /X
RC_IN#_H
[44] RC_IN#
SRN9A
SQ4 PMBS3904
SR41 10KOhm /X
[44] A20GATE
A20GATE_N
SRN9B
SQ3 PMBS3904
+VCCP
H_DPSLP#
SR40 27KOhm
SQ1 PMBS3904
[7,18,56] STP_CPU#
SRN4A
H_DPRSTP#
[18,56] PM_DPRSLPVR
SRN4D
SQ2 PMBS3904
SRN4C
[18] S_INIT#
[18] S_A20M#
[9,18] H_SMI#
[9,18] H_INTR
[9,18] H_NMI
[9,18] H_IGNNE#
[9,18] H_STPCLK#
[9,18] H_CPUSLP#
SRN7A
SRN7B
SRN7C
SRN7D
SRN7E
SRN7F
SRN7G
SRN7H
[9,18] H_FERR#
[9,18] PM_THRMTRIP#
[9] H_DPSLP#
[9] H_DPRSTP#
SRN5B
SRN5D
SRN5C
SRN5A
[19] ACZ_SDOUT
[18] ACZ_SYNC
[18] ACZ_RST#
[18] ACZ_BCLK
SRN13A
SRN13B
SRN13C
SRN13D
SRN14A
SRN14B
SRN14C
SRN14D
ACZ_SDOUT_MDC [37]
ACZ_SDOUT_AUD [38]
ACZ_SYNC_AUD [38]
ACZ_SYNC_MDC [37]
ACZ_RST#_MDC [37]
ACZ_RST#_AUD [38,39]
ACZ_BCLK_AUD [38]
ACZ_BCLK_MDC [37]
SC58 10PF/50V /X
SC60 10PF/50V /X
for Power On and S3
[14] N_S3AUXSW#
SQ6 H2N7002
SC65 0.1UF/16V /X
SUSC# [44]
SUSB# [44,59]
[18] S_PSON#
SQ5 H2N7002
SC66 0.1UF/16V /X
S_PSON#
SUSB#
SUSC#
SRN17A
SRN17B
SRN17C
SRN17D
+5VSB
[7,18] STP_PCI#
SRN4B
[18,36] PCI_PME#
[13,18,30,31,36] PCIE_WAKE#
[18,27,42] SLP_S3#
[18,44] KBC_SCI#
SRN6B
SRN6C
SRN8D
SRN8A
[18,44] PM_PWRBTN#
[12,18,44] PM_RSMRST#
[18,36] SLP_S5#
[18,44] BAT_LL#
SRN6A
SRN8C
SRN6D
SRN8B
SR22 100KOhm /X
[18,30] WLAN_ON#
[18,33] CB_SD#
[17] PCI_REQ#4
[18] S_ENTEST
SRN10A
SRN10D
SRN10C
SRN10B
[18,44] PM_THERM#
[18,33,42] PM_CLKRUN#
[18,41] BT_ON#
[18,44] EXTSMI#
SRN11B
SRN11A
SRN11C
SRN11D
[7,8,9,18,22,23,30,31,32] SMB_DAT_S
[7,8,9,18,22,23,30,31,32] SMB_CLK_S
[18,33,42,44] INT_SERIRQ
[18] LPC_DRQ0#
SRN12A
SRN12B
SRN12C
SRN12D
[18,48] S_ACPILED
SR24 10KOhm /X
Title : SB-966L(5)
ASUSTeK COMPUTER INC.
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 21 of 60

M_DQ[63:0] [14,23]
M_DQS[7:0] [14,23]
M_DQS#[7:0] [14,23]
M_MA[17:0] [14,23,24]
M_DM[7:0] [14,23]

REV Type

DIMM1A

M_MA0	102	A0	DQ0	5	M_DQ0		
M_MA1	101	A1	DQ1	7	M_DQ1		
M_MA2	100	A2	DQ2	17	M_DQ2		
M_MA3	99	A3	DQ3	19	M_DQ3		
M_MA4	98	A4	DQ4	4	M_DQ5		
M_MA5	97	A5	DQ5	6	M_DQ4		
M_MA6	94	A6	DQ6	14	M_DQ6		
M_MA7	92	A7	DQ7	16	M_DQ7		
M_MA8	93	A8	DQ8	23	M_DQ8		
M_MA9	91	A9	DQ9	25	M_DQ9		
M_MA10	105	A10/AP	DQ10	35	M_DQ11		
M_MA14	90	A11	DQ11	37	M_DQ10		
M_MA15	89	A12	DQ12	20	M_DQ13		
M_MA16	116	A13	DQ13	22	M_DQ12		
M_MA17	86	A14	DQ14	36	M_DQ15		
	84	A15	DQ15	38	M_DQ14		
M_MA13	85	A16_BA2	DQ16	43	M_DQ17		
			DQ17	45	M_DQ16		
M_MA11	107	BA0	DQ18	55	M_DQ22		
M_MA12	106	BA1	DQ19	57	M_DQ23		
[14,24] M_CS#0	110	S0#	DQ20	44	M_DQ20		
[14,24] M_CS#1	115	S1#	DQ21	46	M_DQ21		
[8] M_CLK_DDR0	30	CK0	DQ22	56	M_DQ19		
[8] M_CLK_DDR#0	32	CK0#	DQ23	58	M_DQ18		
[8] M_CLK_DDR1	164	CK1	DQ24	61	M_DQ24		
[8] M_CLK_DDR#1	166	CK1#	DQ25	63	M_DQ25		
[14,24] M_CKE0	79	CKE0	DQ26	73	M_DQ31		
[14,24] M_CKE1	80	CKE1	DQ27	75	M_DQ30		
[14,23,24] M_CAS#	113	CAS#	DQ28	62	M_DQ28		
[14,23,24] M_RAS#	108	RAS#	DQ29	64	M_DQ29		
[14,23,24] M_WE#	109	WE#	DQ30	74	M_DQ27		
	198	SA0	DQ31	76	M_DQ26		
	200	SA1	DQ32	123	M_DQ36		
[7,8,9,18,21,23,30,31,32] SMB_CLK_S	197	SCL	DQ33	125	M_DQ37		
[7,8,9,18,21,23,30,31,32] SMB_DAT_S	195	SDA	DQ34	135	M_DQ34		
			DQ35	137	M_DQ33		
[14,24] M_ODT0	114	ODT0	DQ36	124	M_DQ32		
[14,24] M_ODT1	119	ODT1	DQ37	126	M_DQ35		
			DQ38	134	M_DQ38		
M_DM0	10	DM0	DQ39	136	M_DQ39		
M_DM1	26	DM1	DQ40	141	M_DQ45		
M_DM2	52	DM2	DQ41	143	M_DQ44		
M_DM3	67	DM3	DQ42	151	M_DQ47		
M_DM4	130	DM4	DQ43	153	M_DQ41		
M_DM5	147	DM5	DQ44	140	M_DQ40		
M_DM6	170	DM6	DQ45	142	M_DQ46		
M_DM7	185	DM7	DQ46	152	M_DQ42		
			DQ47	154	M_DQ43		
M_DQS0	13	DQS0	DQ48	157	M_DQ49		
M_DQS1	31	DQS1	DQ49	159	M_DQ48		
M_DQS2	51	DQS2	DQ50	173	M_DQ50		
M_DQS3	70	DQS3	DQ51	175	M_DQ51		
M_DQS4	131	DQS4	DQ52	158	M_DQ53		
M_DQS5	148	DQS5	DQ53	160	M_DQ52		
M_DQS6	169	DQS6	DQ54	174	M_DQ55		
M_DQS7	188	DQS7	DQ55	176	M_DQ54		
M_DQS#0	11	DQS#0	DQ56	179	M_DQ57		
M_DQS#1	29	DQS#1	DQ57	181	M_DQ56		
M_DQS#2	49	DQS#2	DQ58	189	M_DQ59		
M_DQS#3	68	DQS#3	DQ59	191	M_DQ62		
M_DQS#4	129	DQS#4	DQ60	180	M_DQ60		
M_DQS#5	146	DQS#5	DQ61	182	M_DQ61		
M_DQS#6	167	DQS#6	DQ62	192	M_DQ58		
M_DQS#7	186	DQS#7	DQ63	194	M_DQ63		

DDR_DIMM_200P

Group0 Group1 Group2 Group3 Group4 Group5 Group6 Group7

GND

SMB_CLK_S
SMB_DAT_S
/X C26 10PF/50V
/X C27 10PF/50V
GND GND

+1.8V_DUAL

C791 10UF/10V
C156 10UF/10V
0.1UF/25V
0.1UF/25V
0.1UF/25V
0.1UF/25V
CN1A CN1B CN1C CN1D
GND GND GND

+3V

C157 0.1UF/16V /X
GND

[23] M_VREF_DIMM

C158 1UF/16V /X
C159 0.1UF/16V
GND GND

+1.8V_DUAL

R5835 1KOhm 1%
M_VREF_DIMM
R5836 1KOhm 1%
GND

DIMM1B

112	VDD1	VSS16	18		
111	VDD2	VSS17	24		
117	VDD3	VSS18	41		
96	VDD4	VSS19	53		
95	VDD5	VSS20	42		
118	VDD6	VSS21	54		
81	VDD7	VSS22	59		
82	VDD8	VSS23	65		
87	VDD9	VSS24	60		
103	VDD10	VSS25	66		
88	VDD11	VSS26	127		
104	VDD12	VSS27	139		
		VSS28	128		
199	VDDSPD	VSS29	145		
		VSS30	165		
83	NC1	VSS31	171		
120	NC2	VSS32	172		
50	NC3	VSS33	177		
69	NC4	VSS34	187		
163	NCTEST	VSS35	178		
		VSS36	190		
1	VREF	VSS37	9		
		VSS38	21		
201	GND0	VSS39	33		
202	GND1	VSS40	155		
		VSS41	34		
203	NP_NC1	VSS42	132		
204	NP_NC2	VSS43	144		
		VSS44	156		
47	VSS1	VSS45	168		
133	VSS2	VSS46	2		
183	VSS3	VSS47	3		
77	VSS4	VSS48	15		
12	VSS5	VSS49	27		
48	VSS6	VSS50	39		
184	VSS7	VSS51	149		
78	VSS8	VSS52	161		
71	VSS9	VSS53	28		
72	VSS10	VSS54	40		
121	VSS11	VSS55	138		
122	VSS12	VSS56	150		
196	VSS13	VSS57	162		
193	VSS14				
8	VSS15				

DDR_DIMM_200P

GND GND

A

ASUSTeK COMPUTER INC.

Title : DDR2 SO-DIMM1

Engineer: Kell Huang

Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 22 of 60

M_DQ[63:0] [14,22]
M_DQS[7:0] [14,22]
M_DQS#[7:0] [14,22]
M_MA[17:0] [14,22,24]
M_DM[7:0] [14,22]

STD Type

DIMM2A

M_MA0 102 A0
M_MA1 101 A1
M_MA2 100 A2
M_MA3 99 A3
M_MA4 98 A4
M_MA5 97 A5
M_MA6 94 A6
M_MA7 92 A7
M_MA8 93 A8
M_MA9 91 A9
M_MA10 105 A10/AP
M_MA14 90 A11
M_MA15 89 A12
M_MA16 116 A13
M_MA17 86 A14
84 A15
M_MA13 85 A16_BA2
M_MA11 107
M_MA12 106 BA0
110 BA1
[14,24] M_CS#2 115 S0#
[14,24] M_CS#3 30 S1#
[8] M_CLK_DDR2 32 CK0
[8] M_CLK_DDR#2 164 CK0#
[8] M_CLK_DDR3 166 CK1
[8] M_CLK_DDR#3 79 CK1#
[14,24] M_CKE2 80 CKE0
[14,24] M_CKE3 113 CKE1
[14,22,24] M_CAS# 108 CAS#
[14,22,24] M_RAS# 109 RAS#
[14,22,24] M_WE# 198 WE#
200 SA0
[7,8,9,18,21,22,30,31,32] SMB_CLK_S 197 SA1
[7,8,9,18,21,22,30,31,32] SMB_DAT_S 195 SCL
SDA
114 ODT0
[14,24] M_ODT2 119 ODT1
[14,24] M_ODT3
M_DM0 10 DM0
M_DM1 26 DM1
M_DM2 52 DM2
M_DM3 67 DM3
M_DM4 130 DM4
M_DM5 147 DM5
M_DM6 170 DM6
M_DM7 185 DM7
M_DQS0 13 DQS0
M_DQS1 31 DQS1
M_DQS2 51 DQS2
M_DQS3 70 DQS3
M_DQS4 131 DQS4
M_DQS5 148 DQS5
M_DQS6 169 DQS6
M_DQS7 188 DQS7
M_DQS#0 11 DQS#0
M_DQS#1 29 DQS#1
M_DQS#2 49 DQS#2
M_DQS#3 68 DQS#3
M_DQS#4 129 DQS#4
M_DQS#5 146 DQS#5
M_DQS#6 167 DQS#6
M_DQS#7 186 DQS#7

DQ0 5 M_DQ0
DQ1 7 M_DQ1
DQ2 17 M_DQ2
DQ3 19 M_DQ3
DQ4 4 M_DQ5
DQ5 6 M_DQ4
DQ6 14 M_DQ6
DQ7 16 M_DQ7
DQ8 23 M_DQ8
DQ9 25 M_DQ9
DQ10 35 M_DQ11
DQ11 37 M_DQ10
DQ12 20 M_DQ13
DQ13 22 M_DQ12
DQ14 36 M_DQ15
DQ15 38 M_DQ14
DQ16 43 M_DQ17
DQ17 45 M_DQ16
DQ18 55 M_DQ22
DQ19 57 M_DQ23
DQ20 44 M_DQ20
DQ21 46 M_DQ21
DQ22 56 M_DQ19
DQ23 58 M_DQ18
DQ24 61 M_DQ24
DQ25 63 M_DQ25
DQ26 73 M_DQ31
DQ27 75 M_DQ30
DQ28 62 M_DQ28
DQ29 64 M_DQ29
DQ30 74 M_DQ27
DQ31 76 M_DQ26
DQ32 123 M_DQ36
DQ33 125 M_DQ37
DQ34 135 M_DQ34
DQ35 137 M_DQ33
DQ36 124 M_DQ32
DQ37 126 M_DQ35
DQ38 134 M_DQ38
DQ39 136 M_DQ39
DQ40 141 M_DQ45
DQ41 143 M_DQ44
DQ42 151 M_DQ47
DQ43 153 M_DQ41
DQ44 140 M_DQ40
DQ45 142 M_DQ46
DQ46 152 M_DQ42
DQ47 154 M_DQ43
DQ48 157 M_DQ49
DQ49 159 M_DQ48
DQ50 173 M_DQ50
DQ51 175 M_DQ51
DQ52 158 M_DQ53
DQ53 160 M_DQ52
DQ54 174 M_DQ55
DQ55 176 M_DQ54
DQ56 179 M_DQ57
DQ57 181 M_DQ56
DQ58 189 M_DQ59
DQ59 191 M_DQ62
DQ60 180 M_DQ60
DQ61 182 M_DQ61
DQ62 192 M_DQ58
DQ63 194 M_DQ63

DDR_DIMM_200P

Group0
Group1
Group2
Group3
Group4
Group5
Group6
Group7

+3V
R77 10KOhm
GND

+1.8V_DUAL
C162 10UF/10V
0.1UF/25V 1 2 CN2A
0.1UF/25V 3 4 CN2B
0.1UF/25V 5 6 CN2C
0.1UF/25V 7 8 CN2D
GND GND
+3V
C163 0.1UF/16V /X
GND
[22] M_VREF_DIMM
C164 1UF/16V /X
C165 0.1UF/16V
GND GND

DIMM2B

112 VDD1 VSS16 18
111 VDD2 VSS17 24
117 VDD3 VSS18 41
96 VDD4 VSS19 53
95 VDD5 VSS20 42
118 VDD6 VSS21 54
81 VDD7 VSS22 59
82 VDD8 VSS23 65
87 VDD9 VSS24 60
103 VDD10 VSS25 66
88 VDD11 VSS26 127
104 VDD12 VSS27 139
VSS28 128
199 VDDSPD VSS29 145
VSS30 165
83 NC1 VSS31 171
120 NC2 VSS32 172
50 NC3 VSS33 177
69 NC4 VSS34 187
163 NCTEST VSS35 178
VSS36 190
1 VREF VSS37 9
VSS38 21
201 GND0 VSS39 33
202 GND1 VSS40 155
VSS41 34
203 NP_NC1 VSS42 132
204 NP_NC2 VSS43 144
VSS44 156
47 VSS1 VSS45 168
133 VSS2 VSS46 2
183 VSS3 VSS47 3
77 VSS4 VSS48 15
12 VSS5 VSS49 27
48 VSS6 VSS50 39
184 VSS7 VSS51 149
78 VSS8 VSS52 161
71 VSS9 VSS53 28
72 VSS10 VSS54 40
121 VSS11 VSS55 138
122 VSS12 VSS56 150
196 VSS13 VSS57 162
193 VSS14
8 VSS15

DDR_DIMM_200P

GND GND

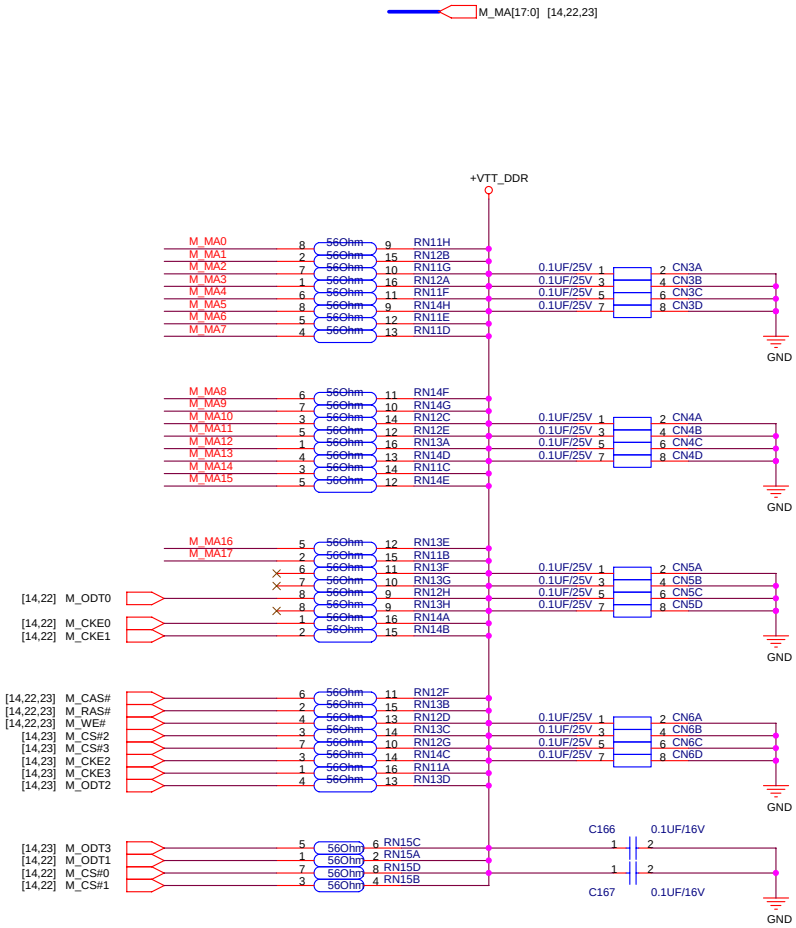
A

Title : DDR2 SO-DIMM2

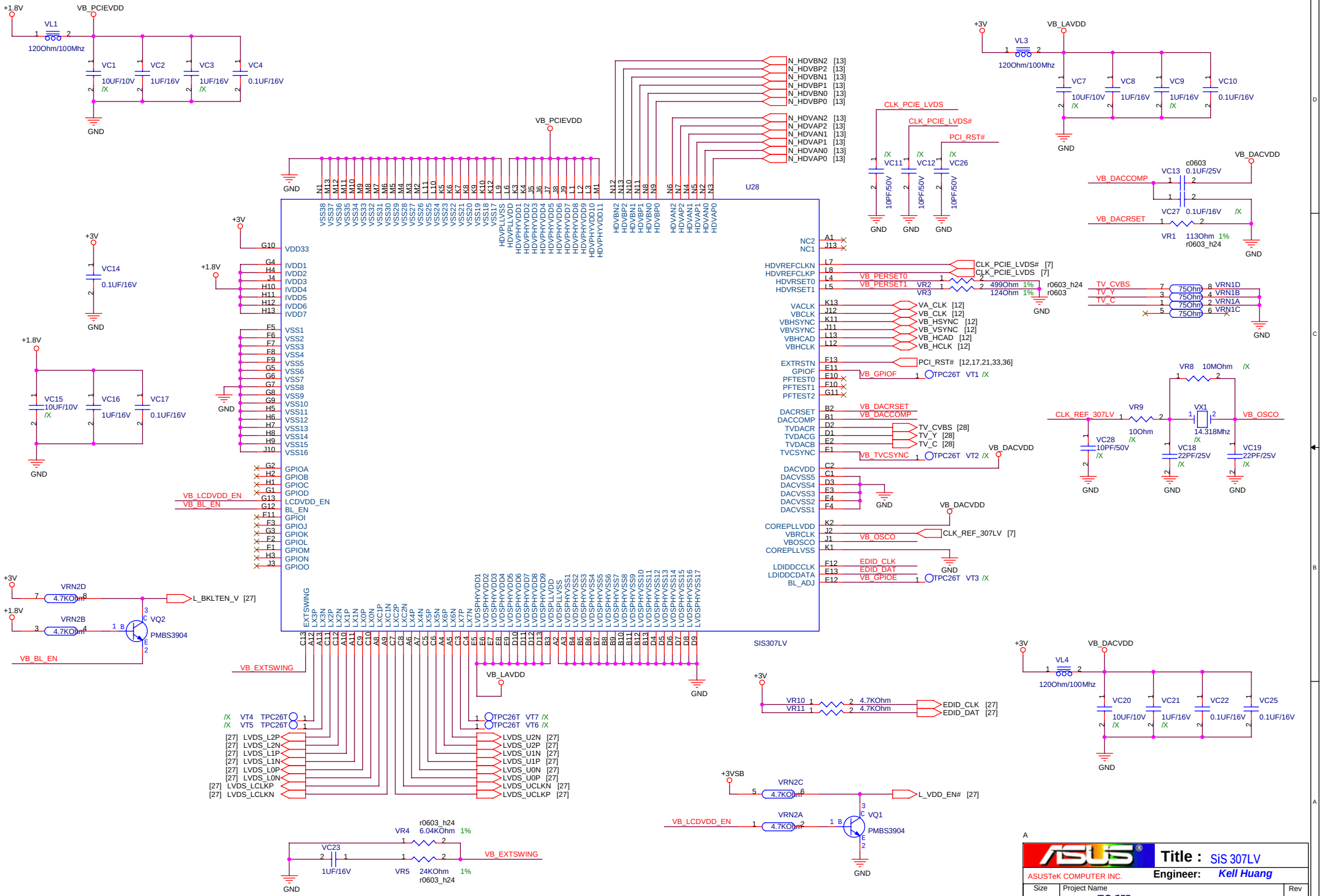
ASUSTeK COMPUTER INC. NB1 Engineer: Kell Huang

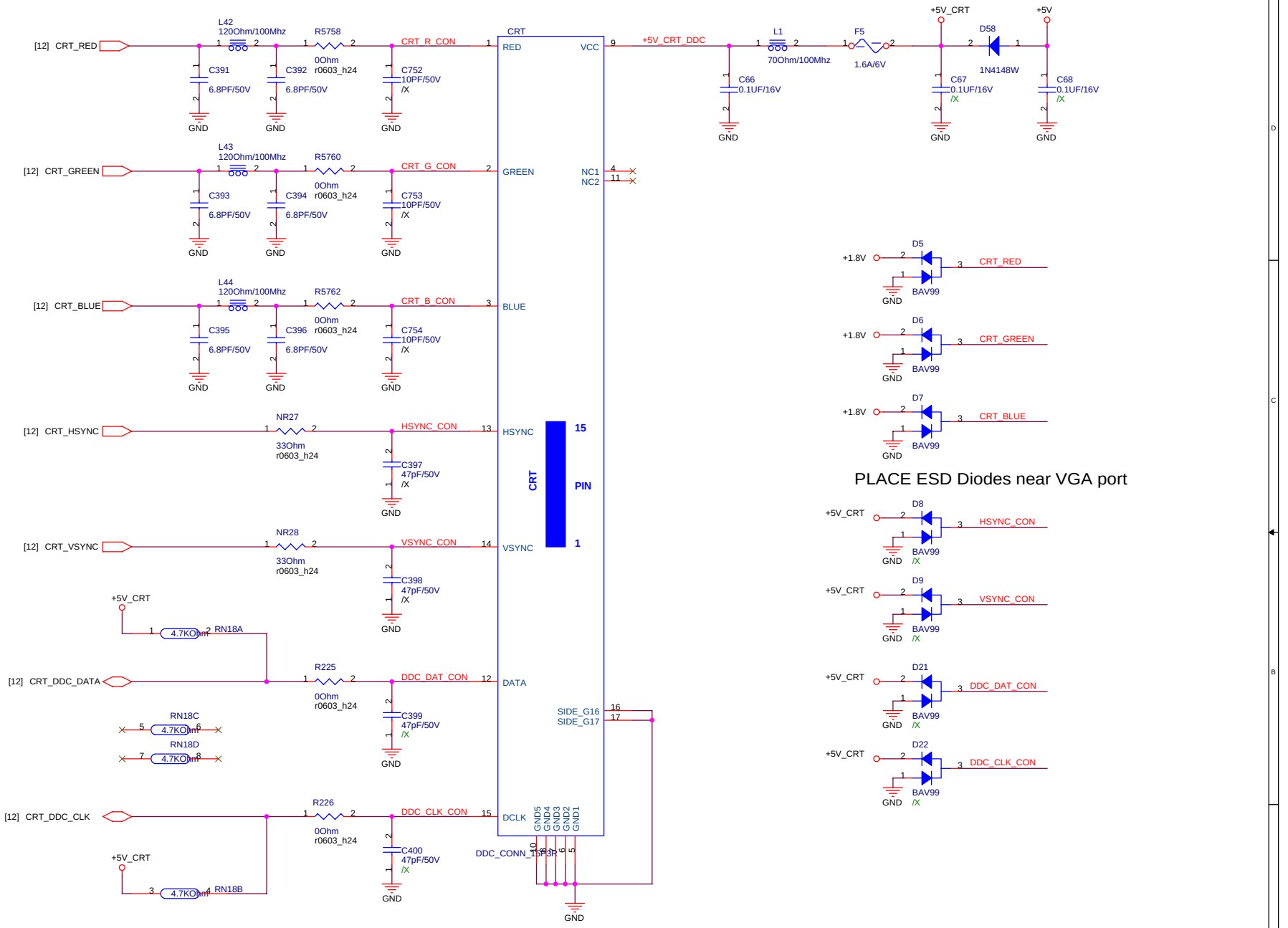
Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 23 of 60



ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 24 of 60		

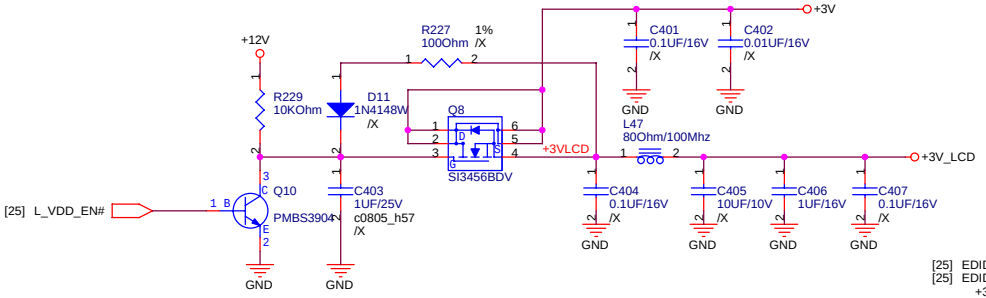

U28
SIS307LV
VB_PCIEVDD
VB_LAVDD
VB_DACVDD
VL1
120Ohm/100Mhz
VL3
VL4
VC1
VC2
VC3
VC4
VC7
VC8
VC9
VC10
VC11
VC12
VC13
VC14
VC15
VC16
VC17
VC18
VC19
VC20
VC21
VC22
VC23
VC25
VC26
VC27
VC28
10UF/10V
1UF/16V
0.1UF/16V
10PF/50V
22PF/25V
c0603
r0603_h24
VR1
VR2
VR3
VR4
VR5
VR8
VR9
VR10
VR11
VX1
14.318Mhz
10Ohm
113Ohm 1%
499Ohm 1%
124Ohm 1%
6.04KOhm 1%
24KOhm 1%
4.7KOhm
10MOhm
VRN1D
VRN1B
VRN1A
VRN1C
75Ohm
VRN2D
VRN2B
VRN2C
VRN2A
PMBS3904
VQ1
VQ2
TPC26T
VT1
VT2
VT3
VT4
VT5
VT6
VT7
GND
+1.8V
+3V
+3VSB
N_HDVBN2 [13]
N_HDVBP2 [13]
N_HDVBN1 [13]
N_HDVBP1 [13]
N_HDVBN0 [13]
N_HDVBP0 [13]
N_HDVAN2 [13]
N_HDVAP2 [13]
N_HDVAN1 [13]
N_HDVAP1 [13]
N_HDVAN0 [13]
N_HDVAP0 [13]
CLK_PCIE_LVDS
CLK_PCIE_LVDS#
PCI_RST#
CLK_PCIE_LVDS# [7]
CLK_PCIE_LVDS [7]
VB_PERSET0
VB_PERSET1
VA_CLK [12]
VB_CLK [12]
VB_HSYNC [12]
VB_VSYNC [12]
VB_HCAD [12]
VB_HCLK [12]
PCI_RST# [12,17,21,33,36]
VB_GPIOF
VB_DACRSET
VB_DACCOMP
TV_CVBS [28]
TV_Y [28]
TV_C [28]
VB_TVCSYNC
CLK_REF_307LV [7]
VB_OSCO
EDID_CLK
EDID_DAT
VB_GPIOE
L_BKLTEN_V [27]
L_VDD_EN# [27]
VB_LCDVDD_EN
VB_BL_EN
VB_EXTSWING
LVDS_L2P [27]
LVDS_L2N [27]
LVDS_L1P [27]
LVDS_L1N [27]
LVDS_L0P [27]
LVDS_L0N [27]
LVDS_LCLKP [27]
LVDS_LCLKN [27]
LVDS_U2N [27]
LVDS_U2P [27]
LVDS_U1N [27]
LVDS_U1P [27]
LVDS_U0N [27]
LVDS_U0P [27]
LVDS_UCLKN [27]
LVDS_UCLKP [27]
EDID_CLK [27]
EDID_DAT [27]
TV_CVBS
TV_Y
TV_C
VRN1D
VRN1B
VRN1A
VRN1C
ASUSTeK COMPUTER INC.
Title : SiS 307LV
Engineer: Kell Huang
Size A3
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 25 of 60



ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 26 of 60	

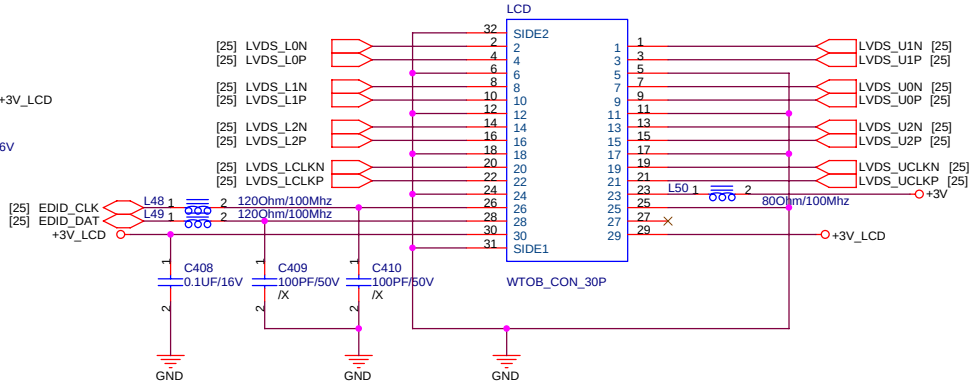
LCD Backlight Control

LCD Power



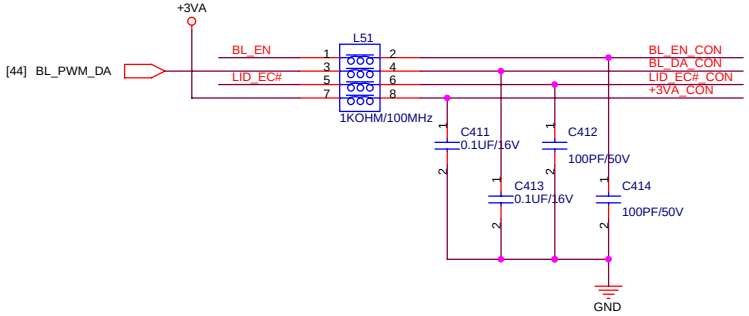
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

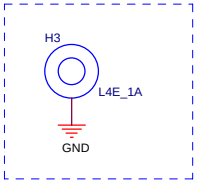
LCD LVDS Interface



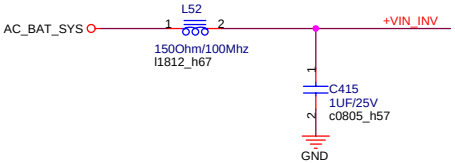
INVERTER Interface/Speaker CONN.

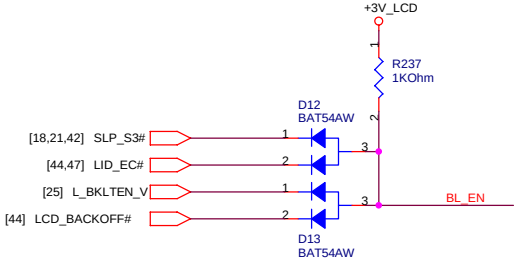
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

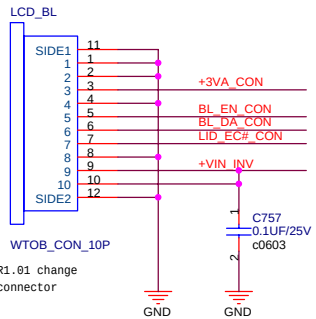




LCD NUT(3.0mm) *1



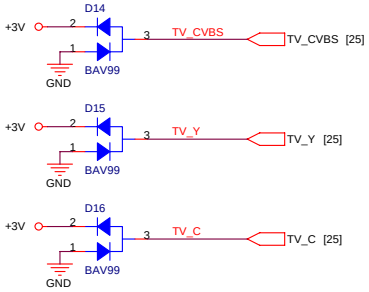




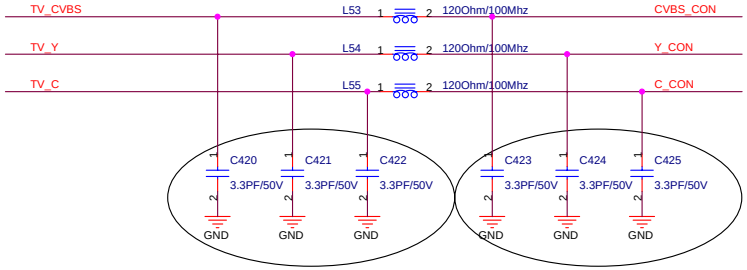
R1.01 change connector

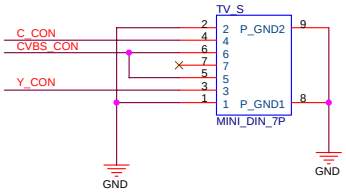
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 27 of 60	

TV OUT



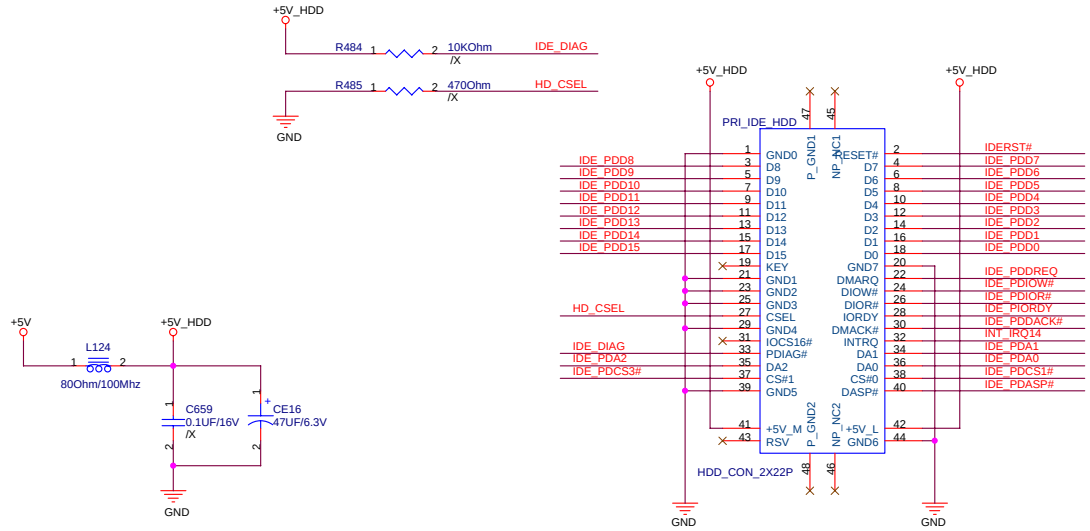
PLACE ESD Diodes near TV port





ASUSTeK COMPUTER INC	Title : TV OUT CONN		
	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 28 of 60		

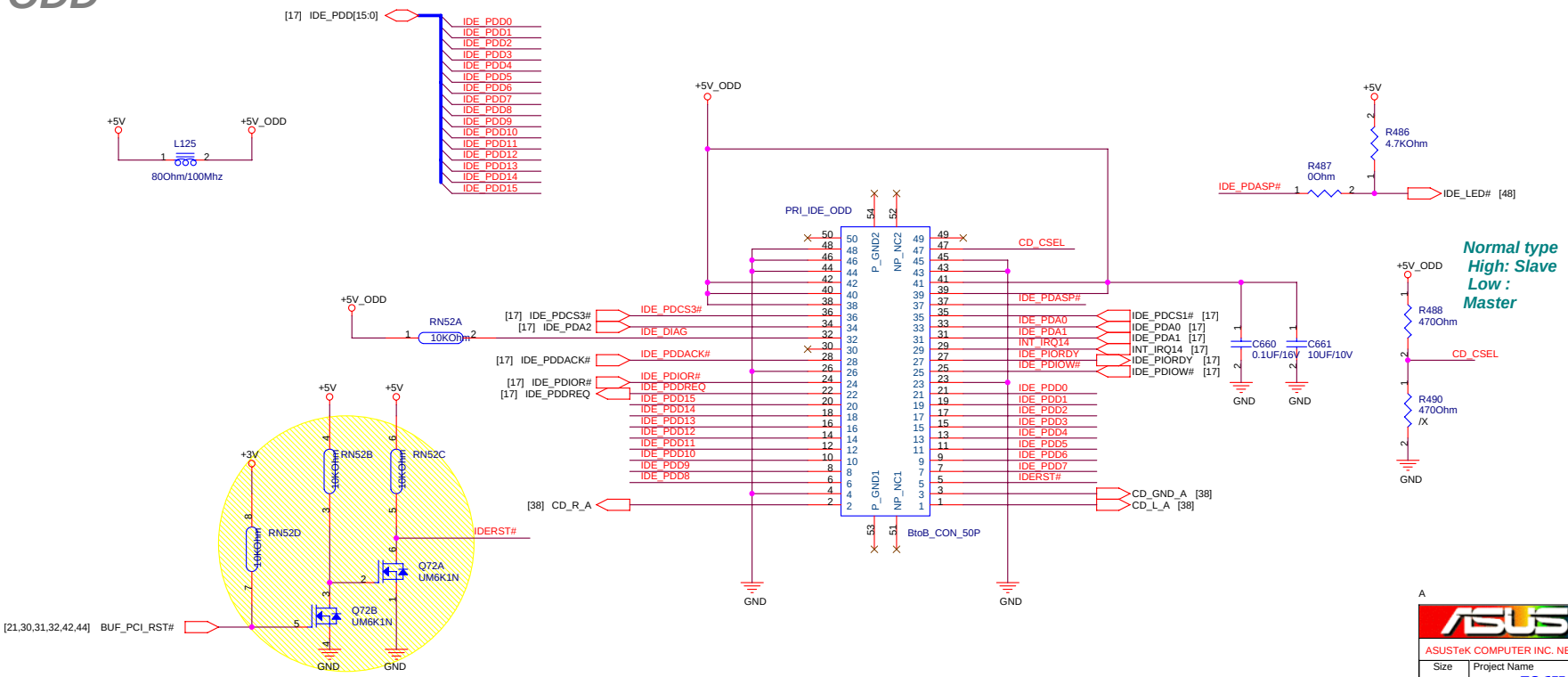
HD_CSEL : Pull-Down, HDD as Master



Remove SATA HDD

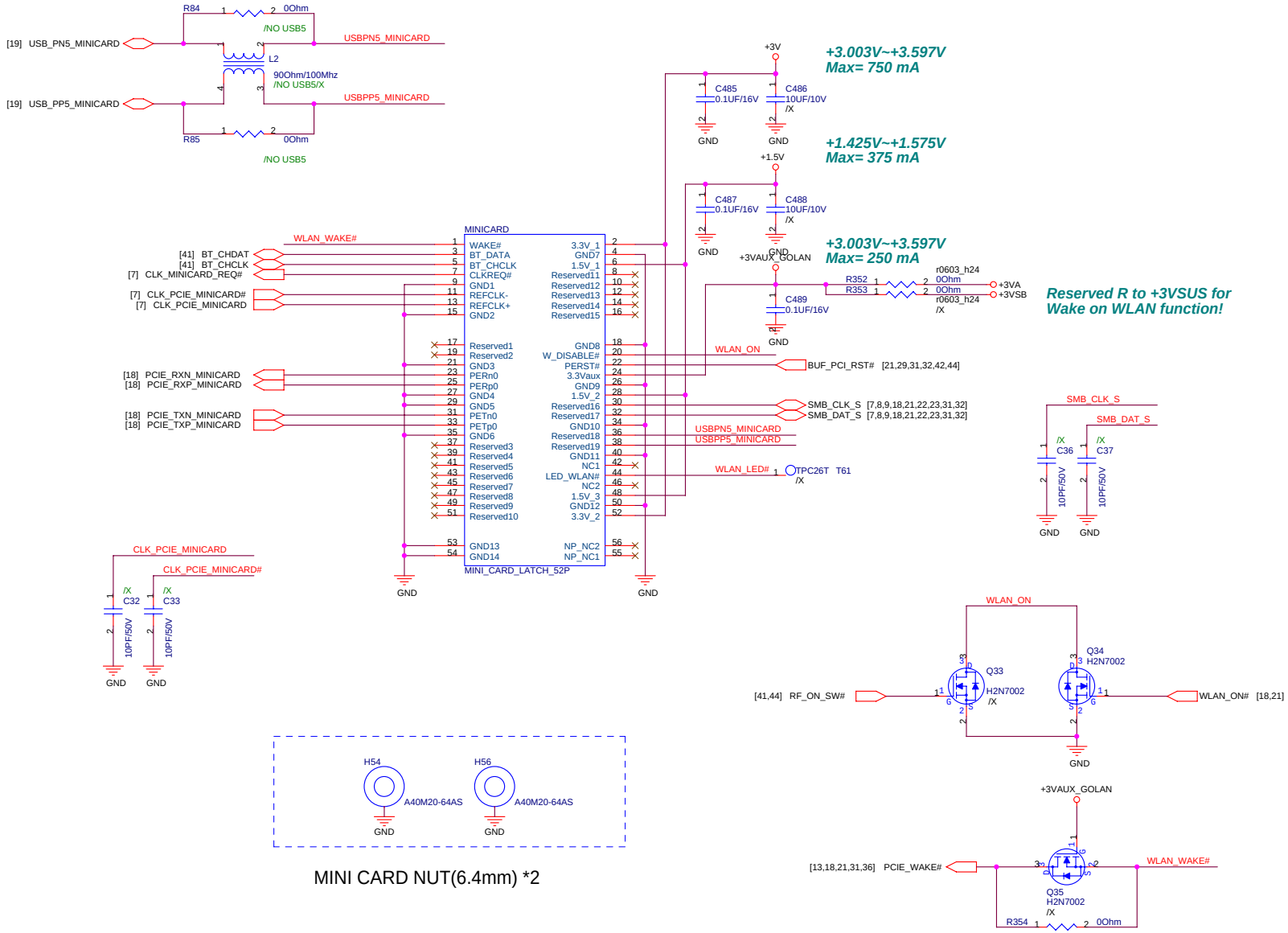
PATA HDD

ODD

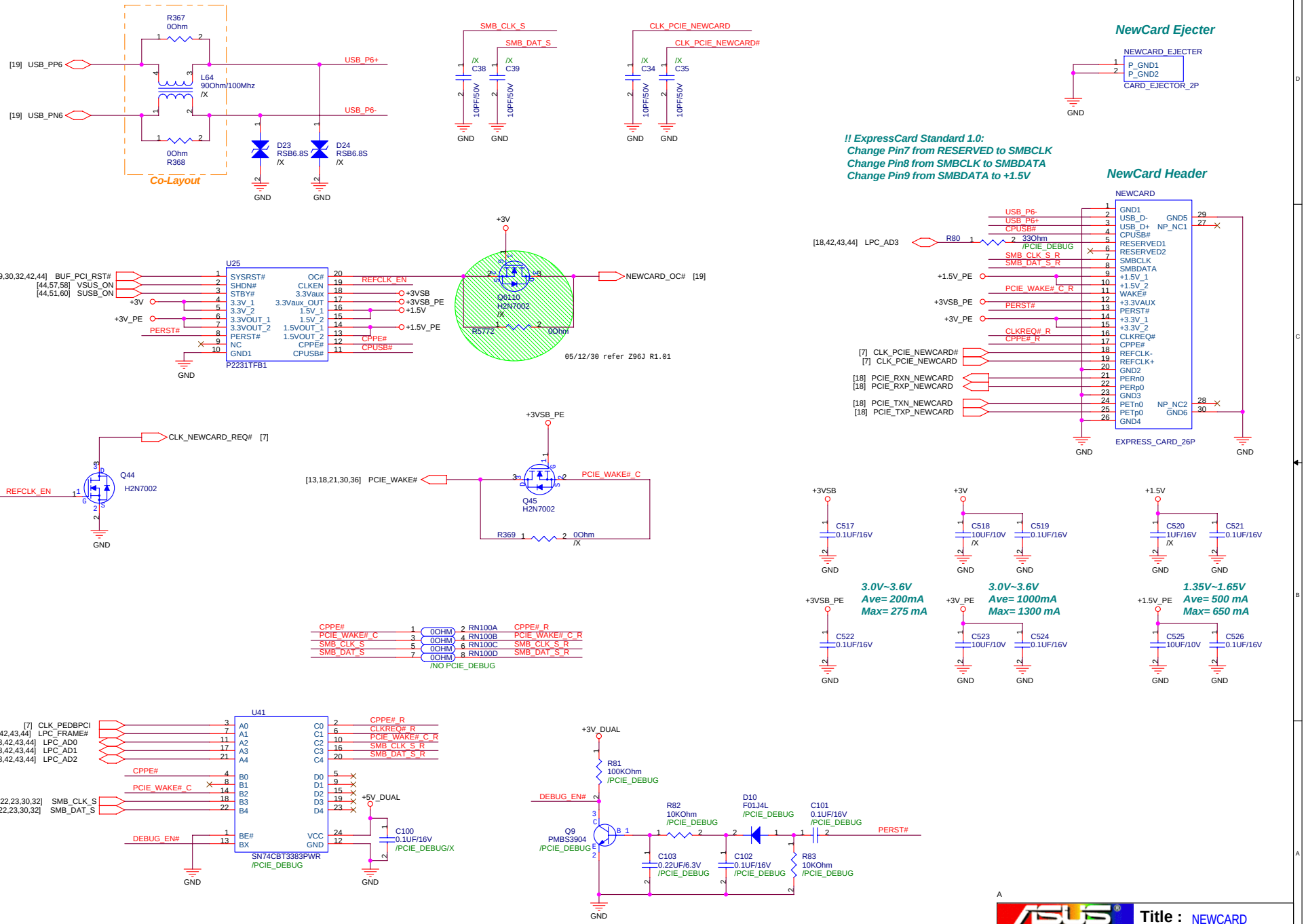


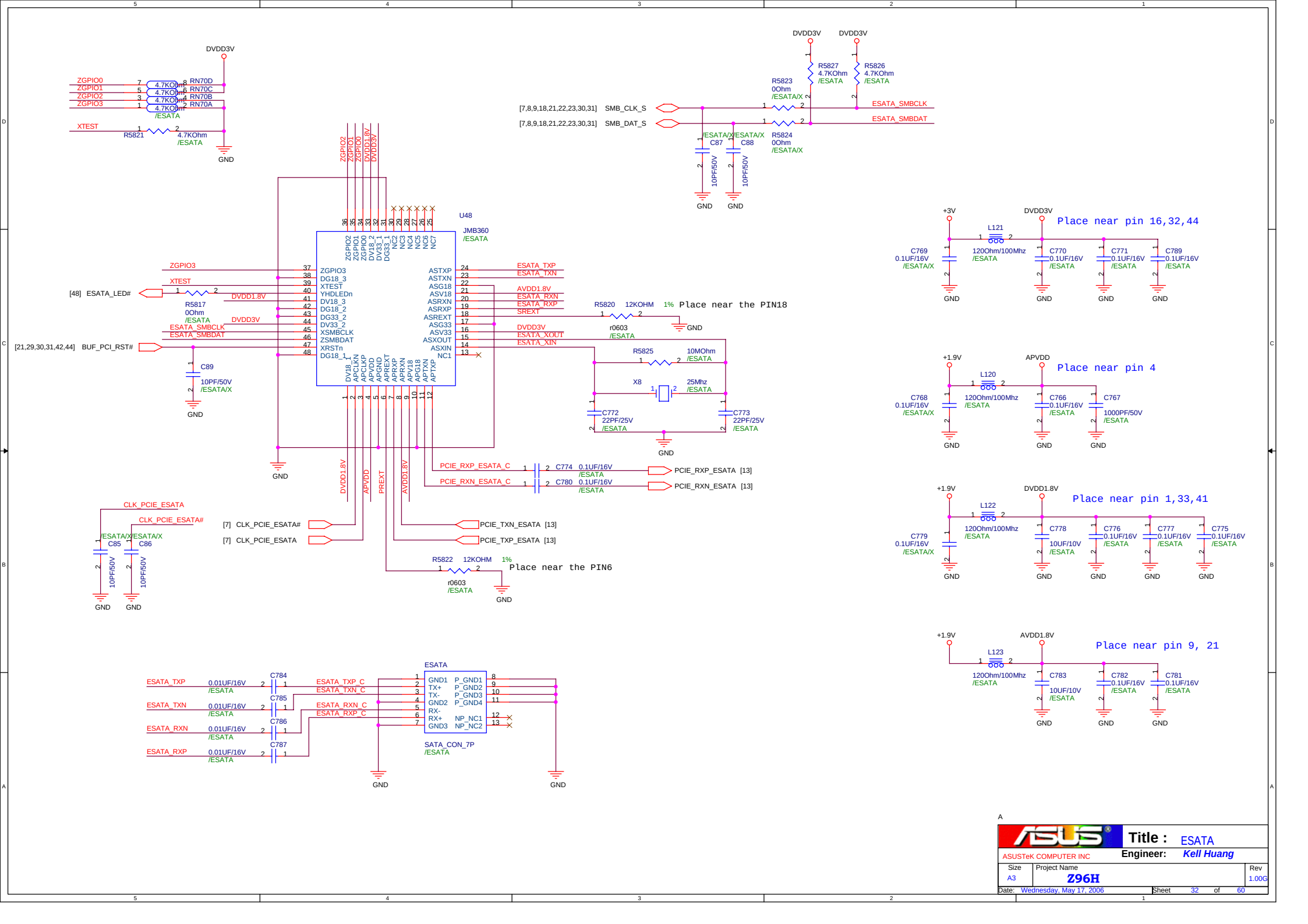
Normal type
High: Slave
Low : Master

ASUSTeK COMPUTER INC. NB1	Title : HDD & ODD	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 29 of 60	

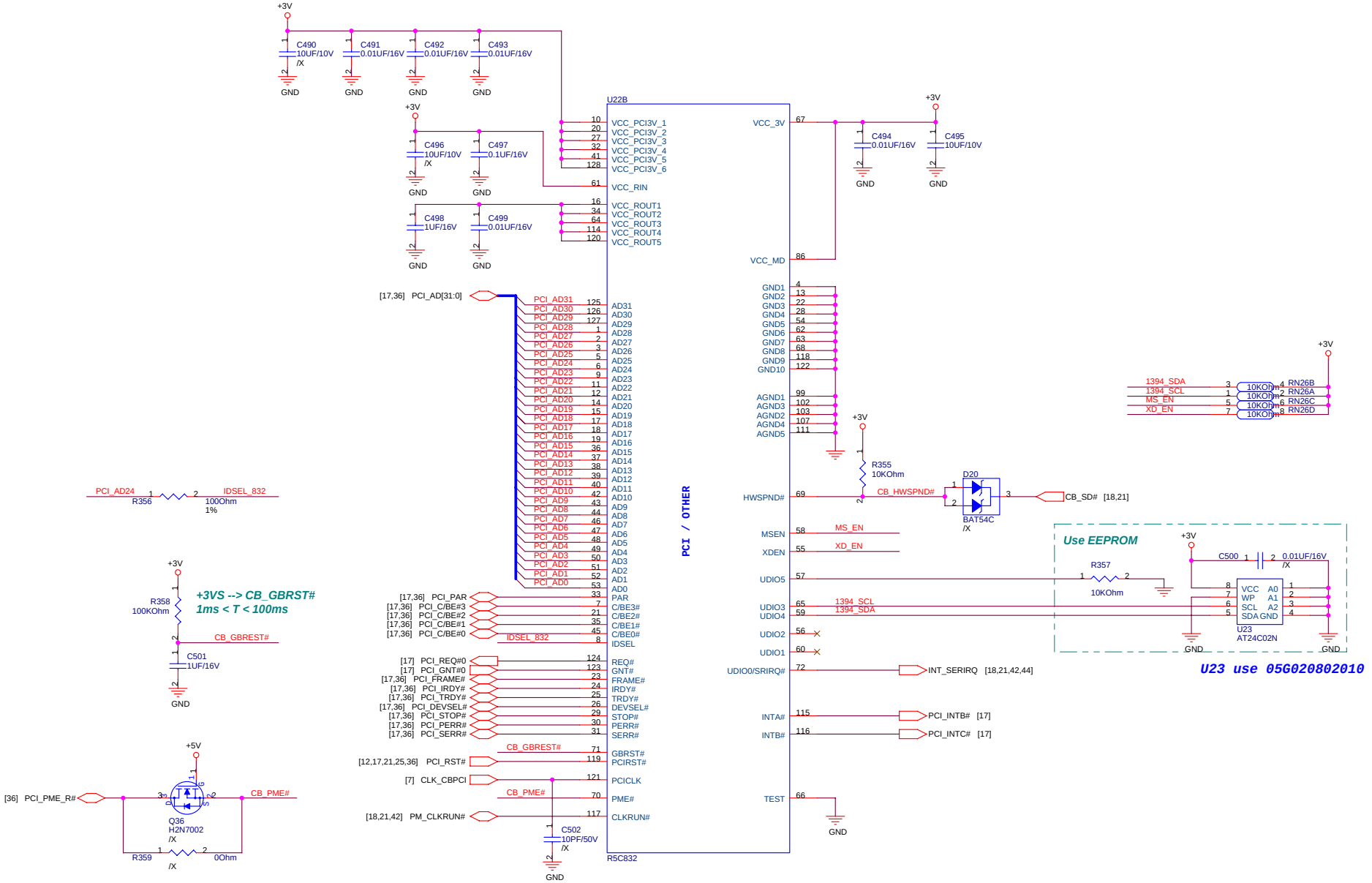


ASUSTeK COMPUTER INC.	Title : MINICARD	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 30 of 60	


R367
0Ohm
[19] USB_PP6
[19] USB_PN6
L64
90Ohm/100Mhz
/X
USB_P6+
USB_P6-
0Ohm
R368
Co-Layout
D23
RSB6.8S
/X
D24
RSB6.8S
/X
GND
SMB_CLK_S
SMB_DAT_S
/X
C38
C39
10PF/50V
CLK_PCIE_NEWCARD
CLK_PCIE_NEWCARD#
C34
C35
NewCard Ejecter
NEWCARD_EJECTER
P_GND1
P_GND2
CARD_EJECTOR_2P
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V
NewCard Header
NEWCARD
U25
[21,29,30,32,42,44] BUF_PCI_RST#
[44,57,58] VSUS_ON
[44,51,60] SUSB_ON
SYSRST#
SHDN#
STBY#
3.3V_1
3.3V_2
3.3VOUT_1
3.3VOUT_2
PERST#
NC
GND1
OC#
CLKEN
3.3Vaux
3.3Vaux_OUT
1.5V_1
1.5V_2
1.5VOUT_1
1.5VOUT_2
CPPE#
CPUSB#
P2231TFB1
REFCLK_EN
+3VSB
+3VSB_PE
+1.5V
+1.5V_PE
+3V
+3V_PE
Q6110
H2N7002
R5772
0Ohm
NEWCARD_OC# [19]
05/12/30 refer Z96J R1.01
[18,42,43,44] LPC_AD3
R80
33Ohm
/PCIE_DEBUG
SMB_CLK_S_R
SMB_DAT_S_R
PCIE_WAKE#_C_R
CLKREQ#_R
CPPE#_R
[7] CLK_PCIE_NEWCARD#
[7] CLK_PCIE_NEWCARD
[18] PCIE_RXN_NEWCARD
[18] PCIE_RXP_NEWCARD
[18] PCIE_TXN_NEWCARD
[18] PCIE_TXP_NEWCARD
GND1
USB_D-
USB_D+
CPUSB#
RESERVED1
RESERVED2
SMBCLK
SMBDATA
+1.5V_1
+1.5V_2
WAKE#
+3.3VAUX
PERST#
+3.3V_1
+3.3V_2
CLKREQ#
CPPE#
REFCLK-
REFCLK+
GND2
PERn0
PERp0
GND3
PETn0
PETp0
GND4
GND5
GND6
NP_NC1
NP_NC2
EXPRESS_CARD_26P
CLK_NEWCARD_REQ# [7]
Q44
H2N7002
[13,18,21,30,36] PCIE_WAKE#
Q45
H2N7002
R369
0Ohm
/X
+3VSB_PE
C517
0.1UF/16V
C518
10UF/10V
C519
C520
1UF/16V
C521
3.0V~3.6V
Ave= 200mA
Max= 275 mA
C522
3.0V~3.6V
Ave= 1000mA
Max= 1300 mA
C523
C524
1.35V~1.65V
Ave= 500 mA
Max= 650 mA
C525
C526
CPPE#
PCIE_WAKE#_C
SMB_CLK_S
SMB_DAT_S
0OHM
RN100A
RN100B
RN100C
RN100D
CPPE#_R
PCIE_WAKE#_C_R
SMB_CLK_S_R
SMB_DAT_S_R
/NO PCIE_DEBUG
U41
[7] CLK_PEDBPCI
[18,42,43,44] LPC_FRAME#
[18,42,43,44] LPC_AD0
[18,42,43,44] LPC_AD1
[18,42,43,44] LPC_AD2
[7,8,9,18,21,22,23,30,32] SMB_CLK_S
[7,8,9,18,21,22,23,30,32] SMB_DAT_S
DEBUG_EN#
A0
A1
A2
A3
A4
B0
B1
B2
B3
B4
BE#
BX
C0
C1
C2
C3
C4
D0
D1
D2
D3
D4
VCC
GND
SN74CBT3383PWR
/PCIE_DEBUG
+5V_DUAL
C100
0.1UF/16V
/PCIE_DEBUG/X
+3V_DUAL
R81
100KOhm
/PCIE_DEBUG
DEBUG_EN#
Q9
PMBS3904
/PCIE_DEBUG
R82
10KOhm
/PCIE_DEBUG
D10
F01J4L
/PCIE_DEBUG
C101
0.1UF/16V
/PCIE_DEBUG
PERST#
C103
0.22UF/6.3V
/PCIE_DEBUG
C102
0.1UF/16V
/PCIE_DEBUG
R83
10KOhm
/PCIE_DEBUG
Title : NEWCARD
ASUSTeK COMPUTER INC. NB1
Engineer: Kell Huang
Size
Custom
Project Name
Z96H
Rev
1.00G
Date: Wednesday, May 17, 2006
Sheet 31 of 60

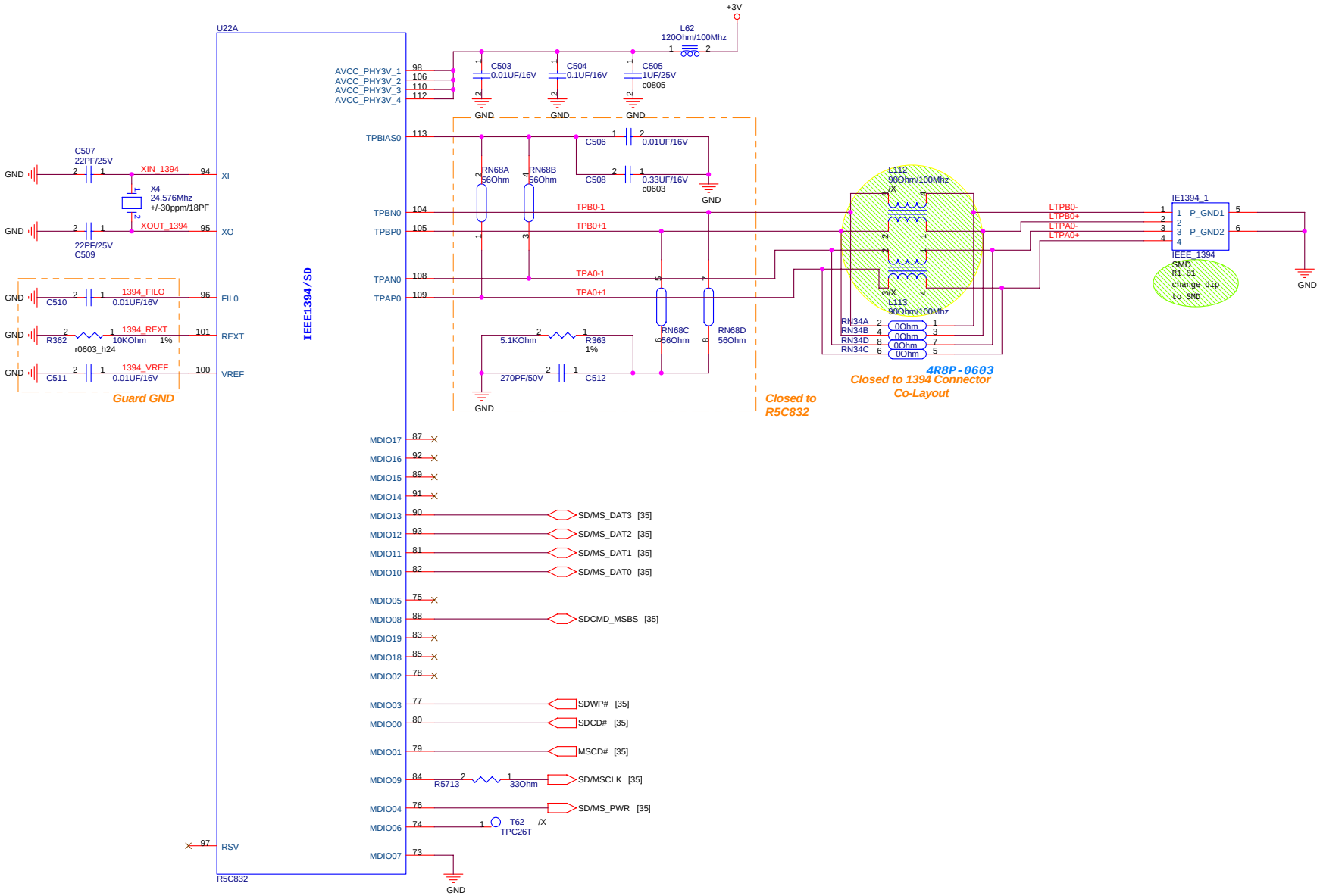


ASUSTeK COMPUTER INC	Title : ESATA		
	Engineer: Kell Huang		
Size: A3	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 32 of 60		

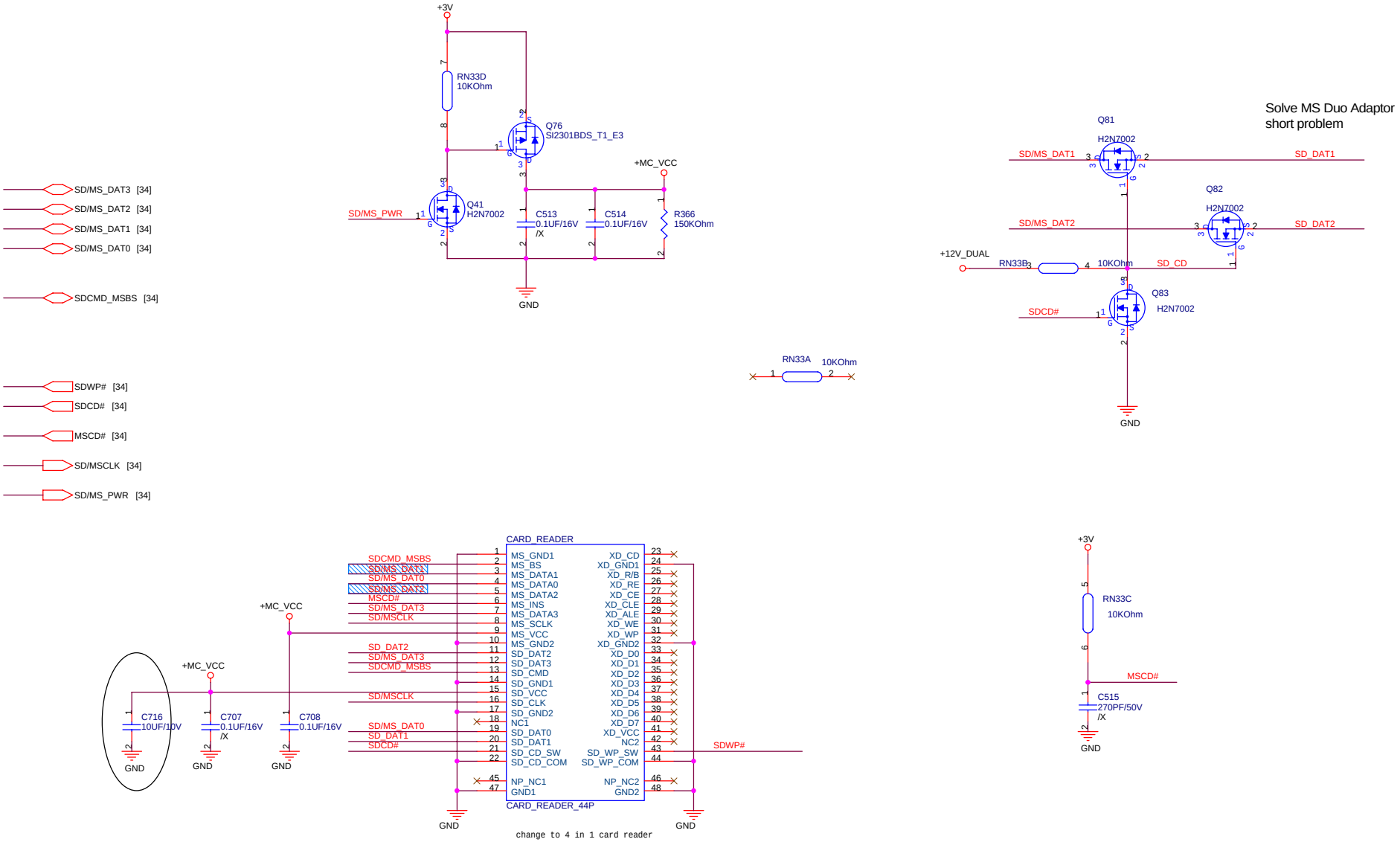


PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD24	0	C
1394	AD24	0	B

Title : CARD1394-R5C832(1)			
ASUSTeK COMPUTER INC. MB6	Engineer: Kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 33 of 60		



Title : CARD1394-R5C832(2)			
ASUSTeK COMPUTER INC. MB6	Engineer: kell Huang		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 34 of 60		



ASUSTeK COMPUTER INC		Title : 4 in 1 CARD READER	
		Engineer: Kell Huang	
Size: A3	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006		Sheet 35 of 60	

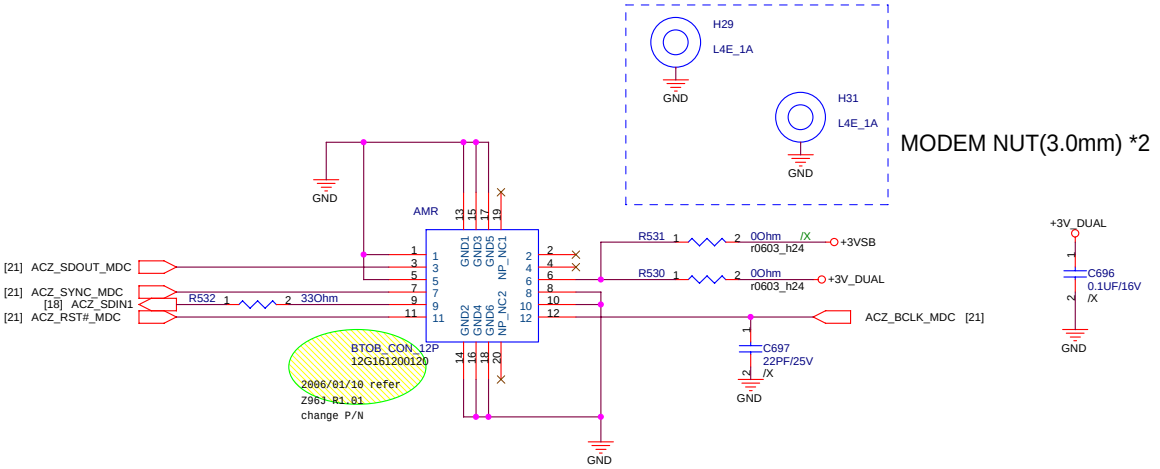
PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	1	D

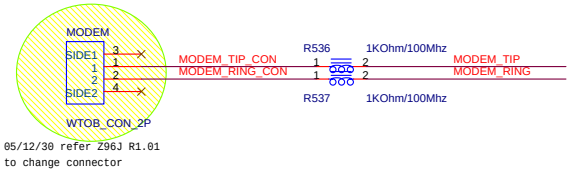
	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64/78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

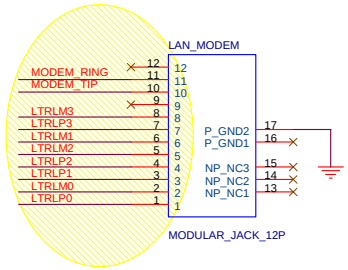
*All termination resistors should be near chip

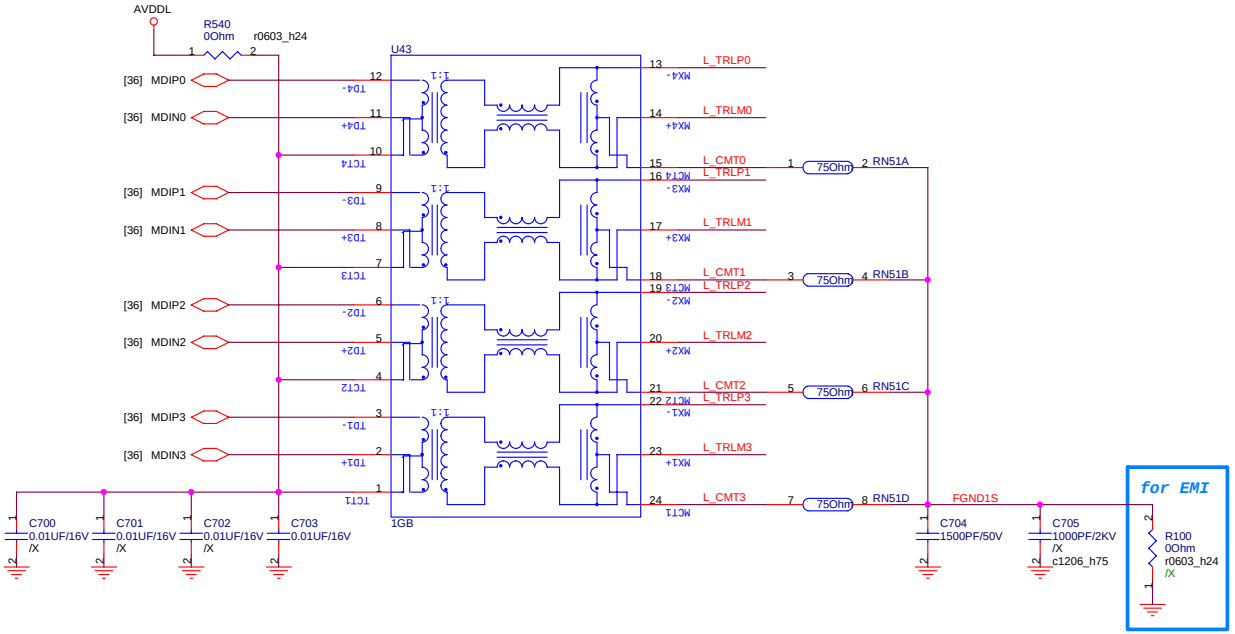
Title :	LAN RTL8110SBL
ASUSTeK COMPUTER INC	Engineer: Kell Huang
Size: Custom	Project Name: Z96H
Rev: 1.00G	
Date: Wednesday, May 17, 2006	Sheet 36 of 60

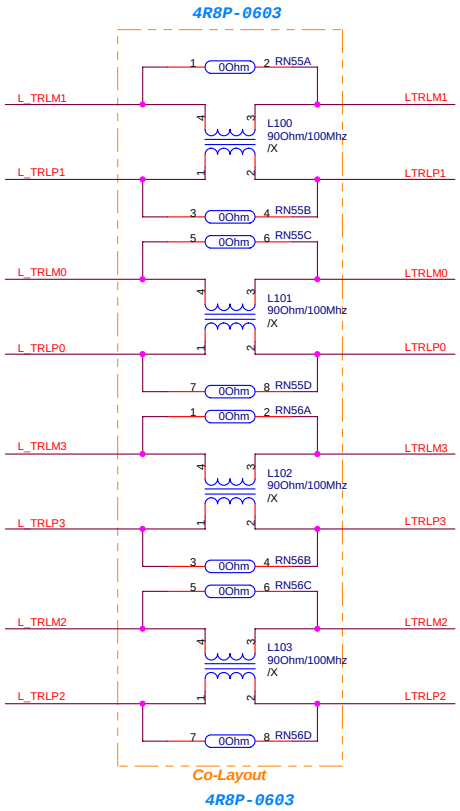
MDC CONN.











A

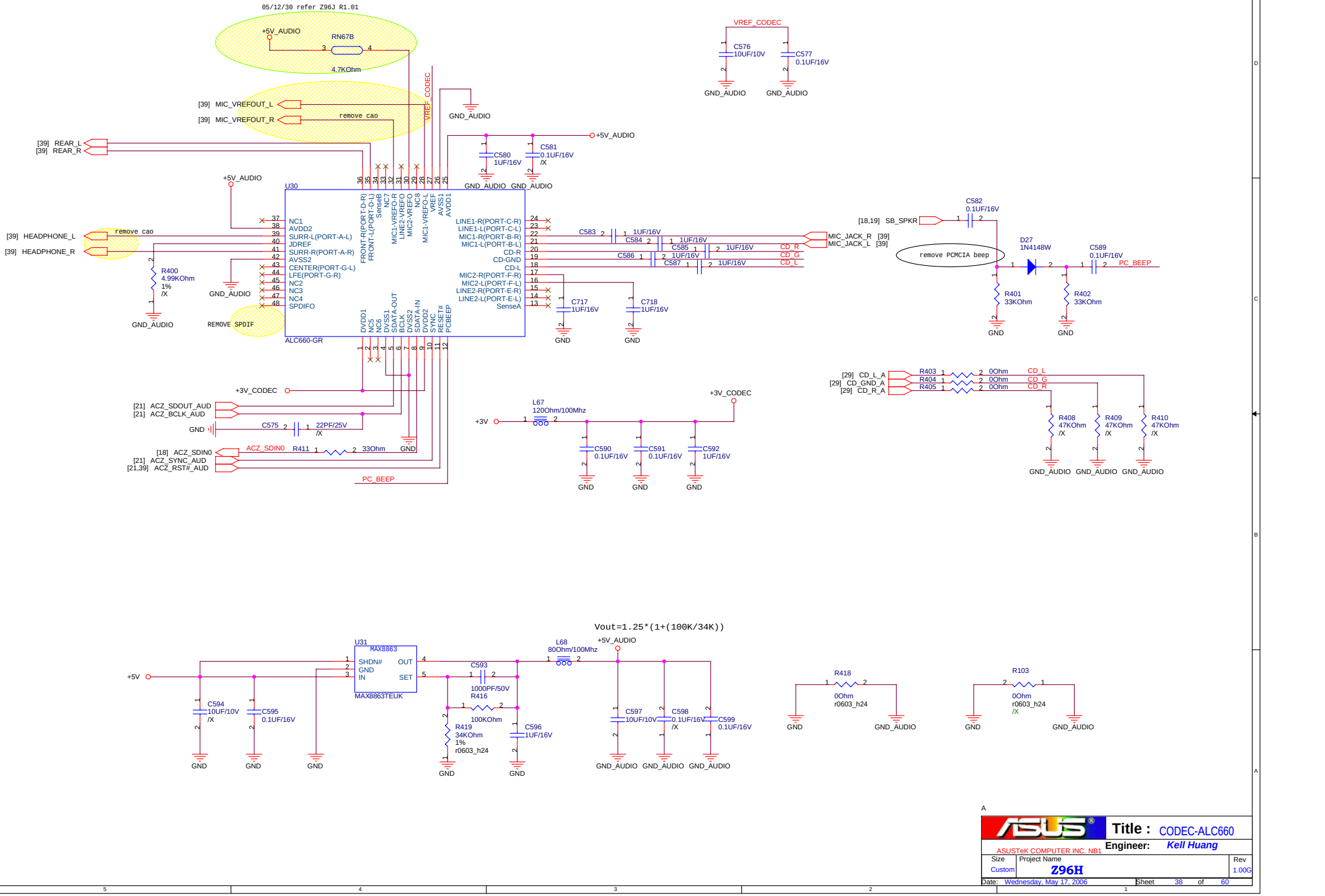
ASUSTeK COMPUTER INC.

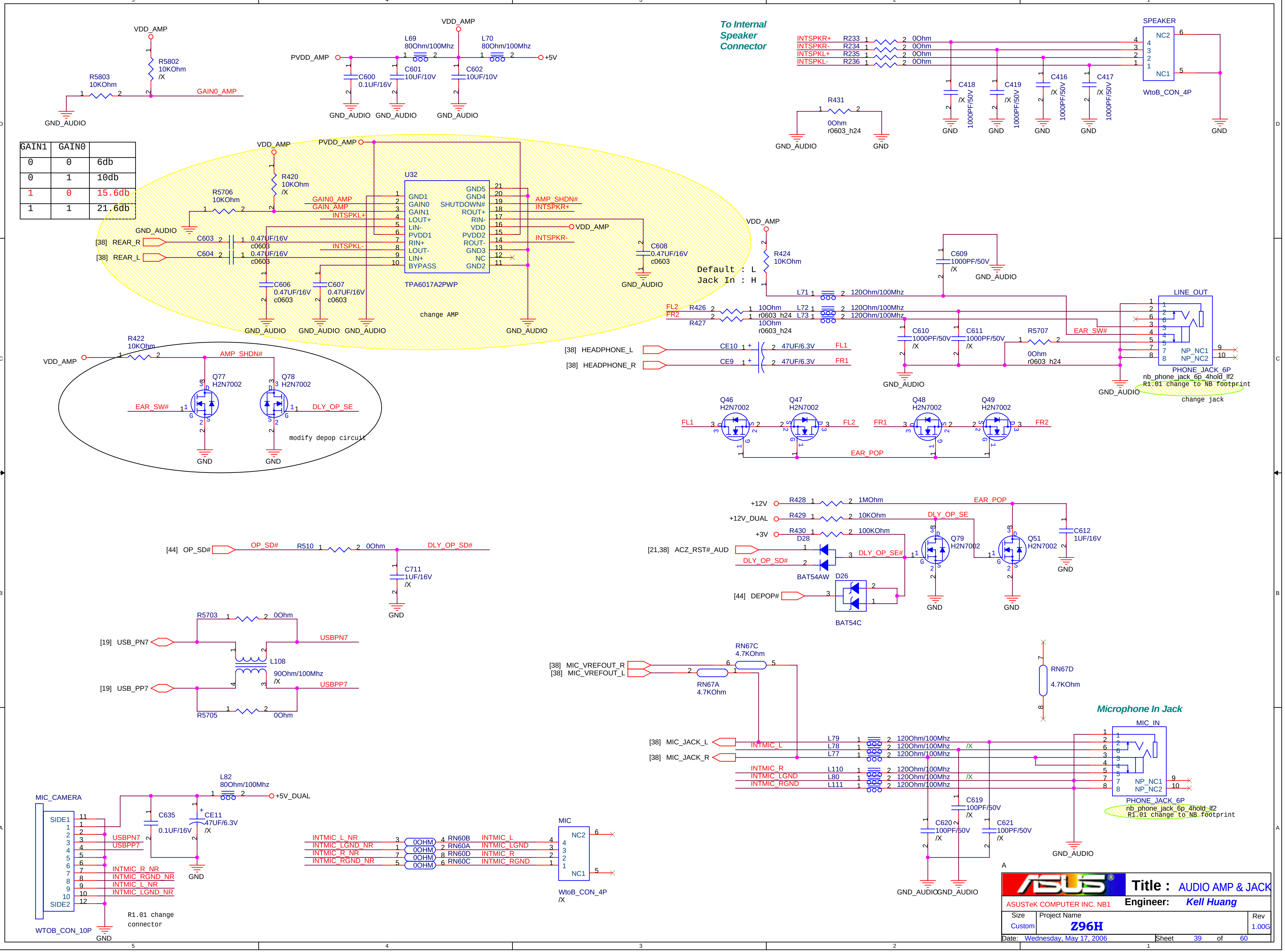
Title : RJ45&RJ11

Engineer: Kell Huang

Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 37 of 60


05/12/30 refer Z96J R1.01
+5V_AUDIO
RN67B
4.7KOhm
[39] MIC_VREFOUT_L
[39] MIC_VREFOUT_R
remove cao
VREF_CODEC
GND_AUDIO
[39] REAR_L
[39] REAR_R
C580 1UF/16V
C581 0.1UF/16V /X
U30
ALC660-GR
NC1
AVDD2
SURR-L(PORT-A-L)
JDREF
SURR-R(PORT-A-R)
AVSS2
CENTER(PORT-G-L)
LFE(PORT-G-R)
NC2
NC3
NC4
SPDIFO
FRONT-R(PORT-D-R)
FRONT-L(PORT-D-L)
SenseB
NC7
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
NC8
MIC1-VREFO-L
VREF
AVSS1
AVDD1
LINE1-R(PORT-C-R)
LINE1-L(PORT-C-L)
MIC1-R(PORT-B-R)
MIC1-L(PORT-B-L)
CD-R
CD-GND
CD-L
MIC2-R(PORT-F-R)
MIC2-L(PORT-F-L)
LINE2-R(PORT-E-R)
LINE2-L(PORT-E-L)
SenseA
DVDD1
NC5
NC6
DVSS1
SDATA-OUT
BCLK
SDATA-IN
DVDD2
SYNC
RESET#
PCBEEP
[39] HEADPHONE_L
[39] HEADPHONE_R
R400 4.99KOhm 1% /X
REMOVE SPDIF
C583 1UF/16V
C584 1UF/16V
C585 1UF/16V
C586 1UF/16V
C587 1UF/16V
CD_R
CD_G
CD_L
MIC_JACK_R [39]
MIC_JACK_L [39]
C717 1UF/16V
C718 1UF/16V
GND
[18,19] SB_SPKR
C582 0.1UF/16V
remove PCMIA beep
D27 1N4148W
C589 0.1UF/16V
PC_BEEP
R401 33KOhm
R402 33KOhm
+3V_CODEC
[21] ACZ_SDOUT_AUD
[21] ACZ_BCLK_AUD
C575 22PF/25V /X
[18] ACZ_SDIN0
[21] ACZ_SYNC_AUD
[21,39] ACZ_RST#_AUD
ACZ_SDIN0
R411 33Ohm
PC_BEEP
L67 120Ohm/100Mhz
+3V
C590 0.1UF/16V
C591 0.1UF/16V
C592 1UF/16V
[29] CD_L_A
[29] CD_GND_A
[29] CD_R_A
R403 0Ohm
R404 0Ohm
R405 0Ohm
R408 47KOhm /X
R409 47KOhm /X
R410 47KOhm /X
GND_AUDIO
Vout=1.25*(1+(100K/34K))
U31
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
+5V
L68 80Ohm/100Mhz
C593 1000PF/50V
R416 100KOhm
R419 34KOhm 1% r0603_h24
C596 1UF/16V
C594 10UF/10V /X
C595 0.1UF/16V
C597 10UF/10V
C598 0.1UF/16V /X
C599 0.1UF/16V
R418 0Ohm r0603_h24
R103 0Ohm r0603_h24 /X
Title : CODEC-ALC660
Engineer: Kell Huang
ASUSTeK COMPUTER INC. NB1
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 38 of 60



GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db

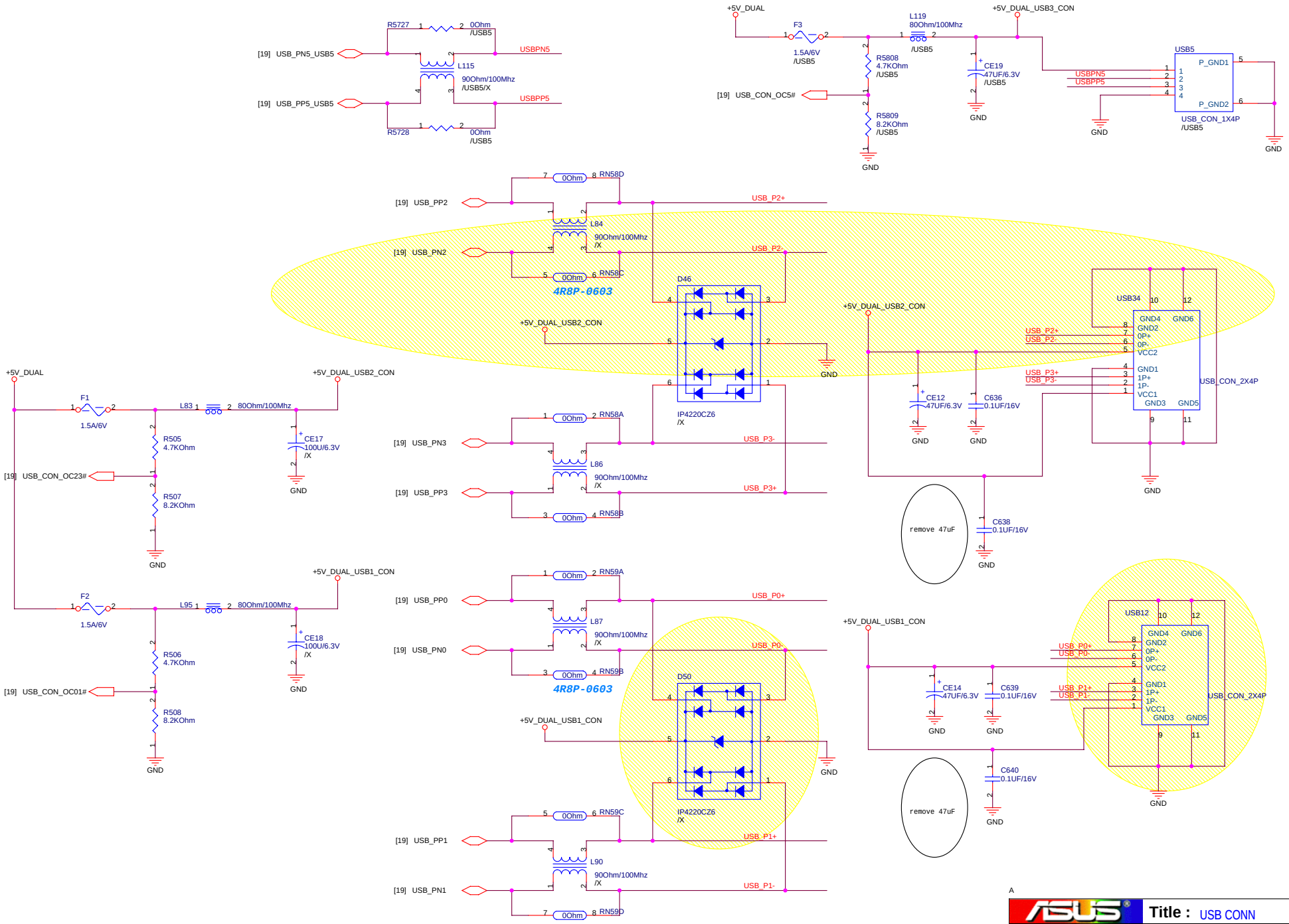
ASUSTeK COMPUTER INC. NB1

Title : AUDIO AMP & JACK

Engineer: Kell Huang

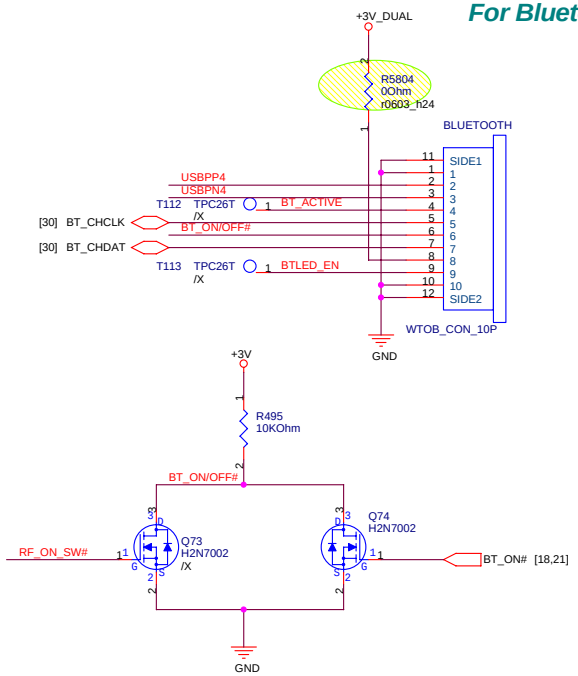
Size	Project Name	Rev
Custom	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 39 of 60

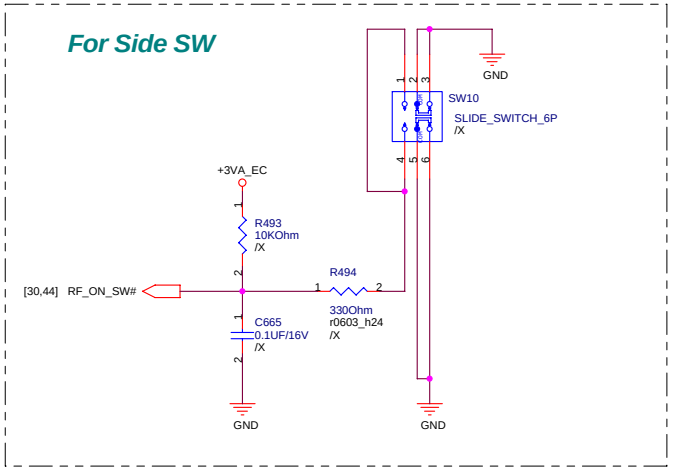


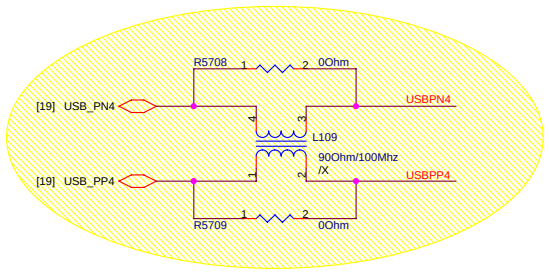
ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 40 of 60	

For Bluetooth



For Side SW

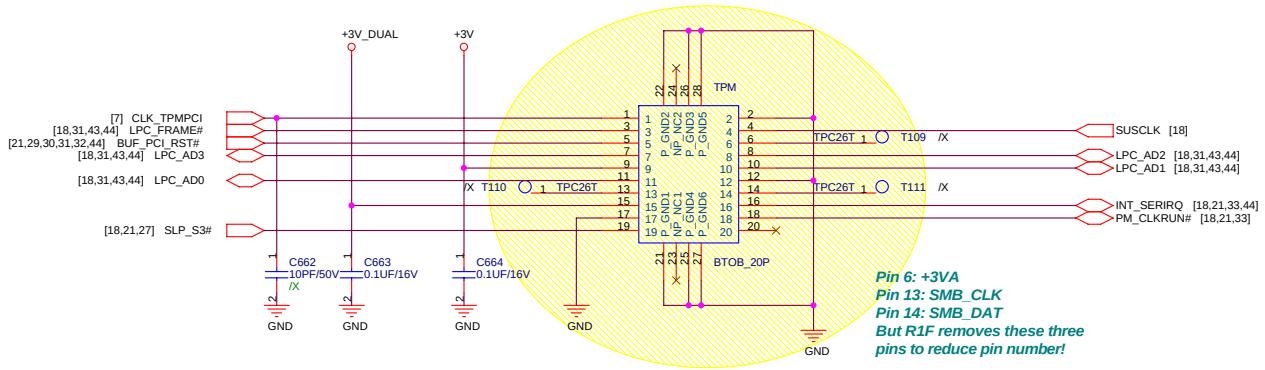




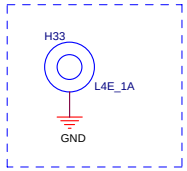
A

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 41 of 60	

For TPM Module



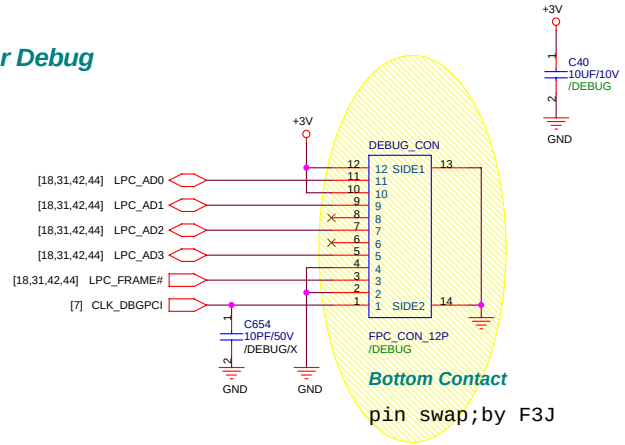
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!



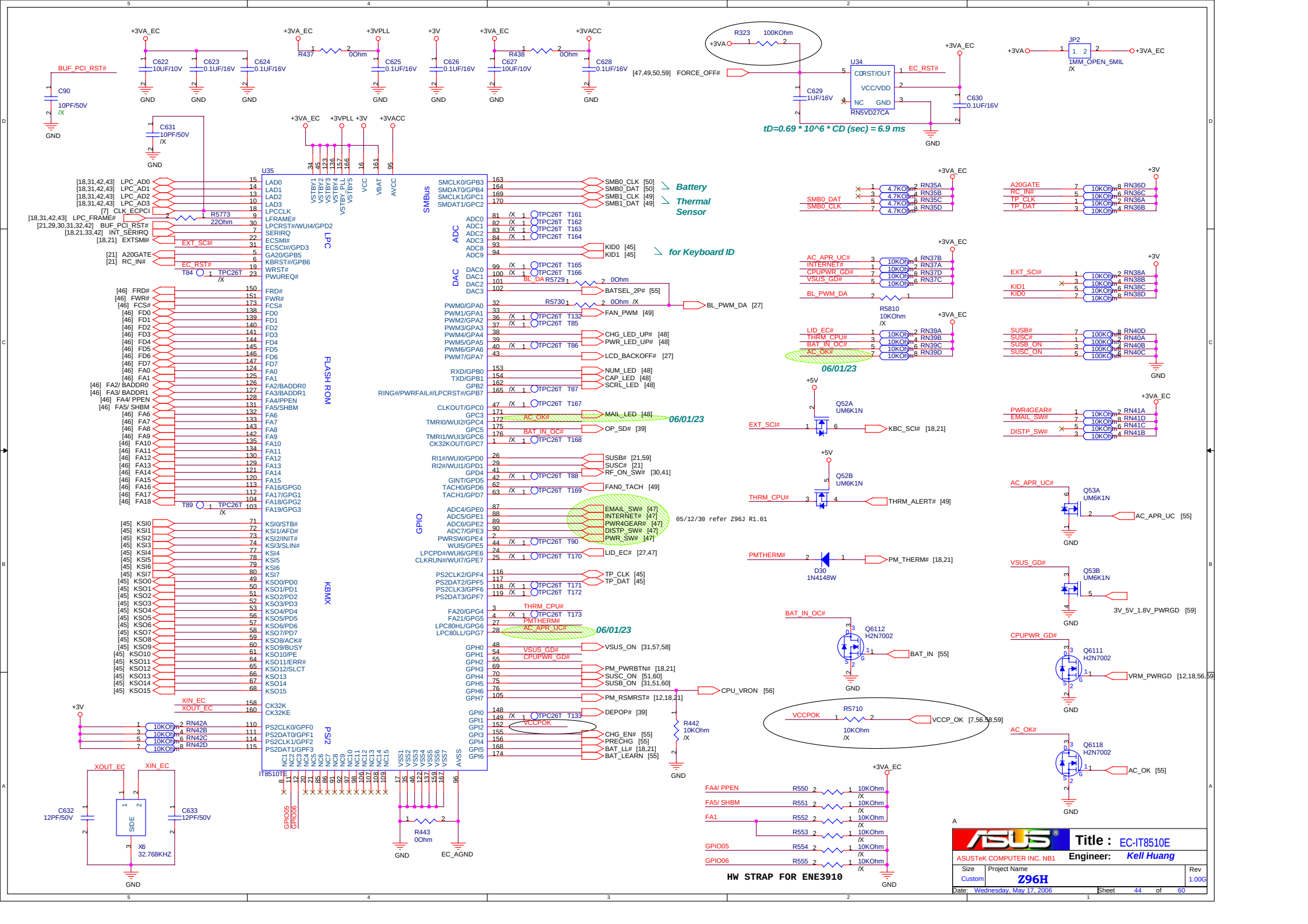
TPM MODULE NUT(3.0mm) *1

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 42 of 60	

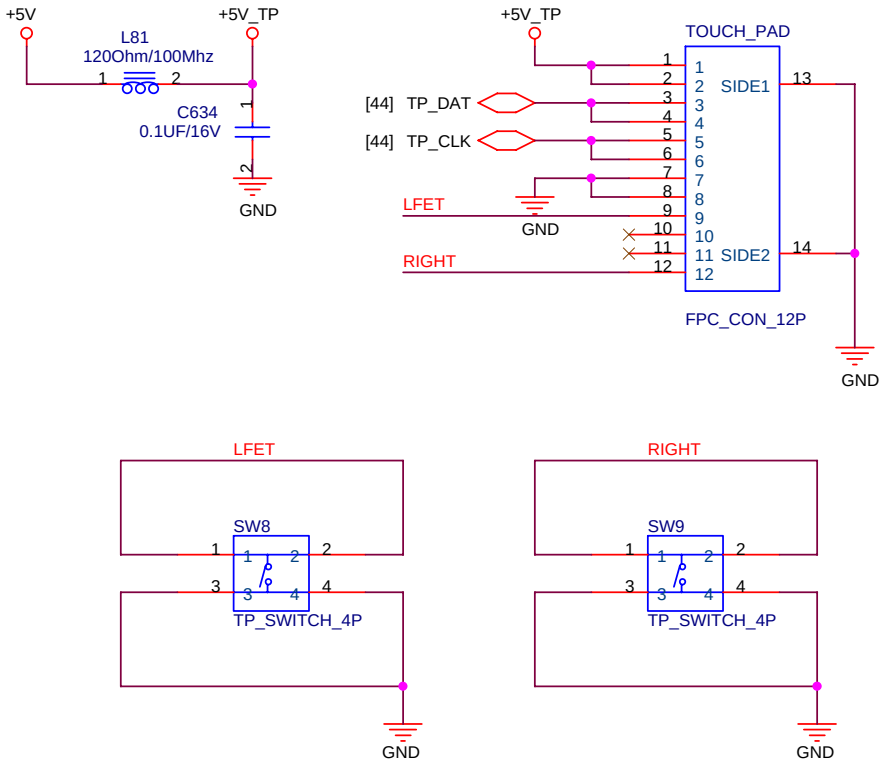
For Debug



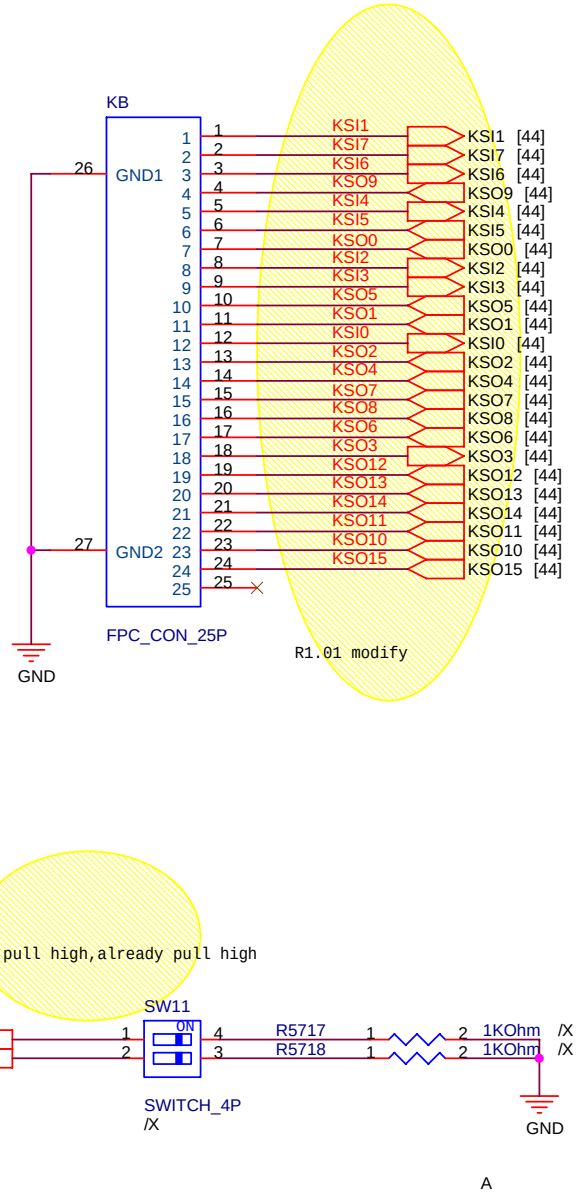
ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 43 of 60	


U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
for Keyboard ID
06/01/23
05/12/30 refer Z96J R1.01
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
HW STRAP FOR ENE3910
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Kell Huang
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 44 of 60

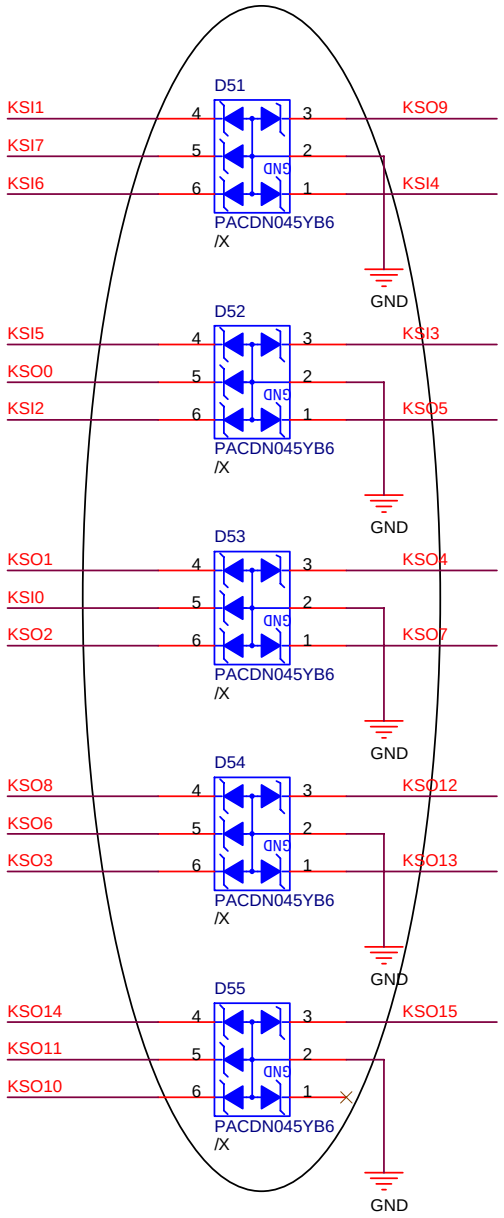
For Touch-Pad



For Keyboard

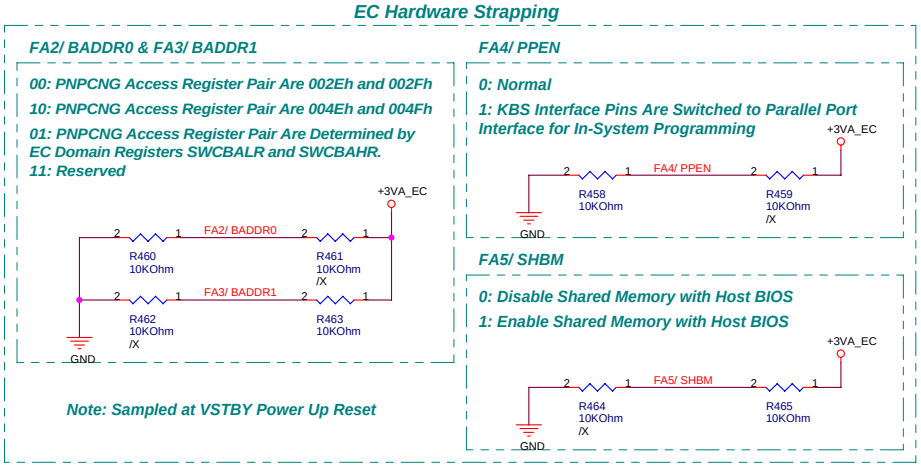


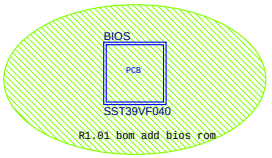
05/12/29 ESD DIODE PIN SWAPPED

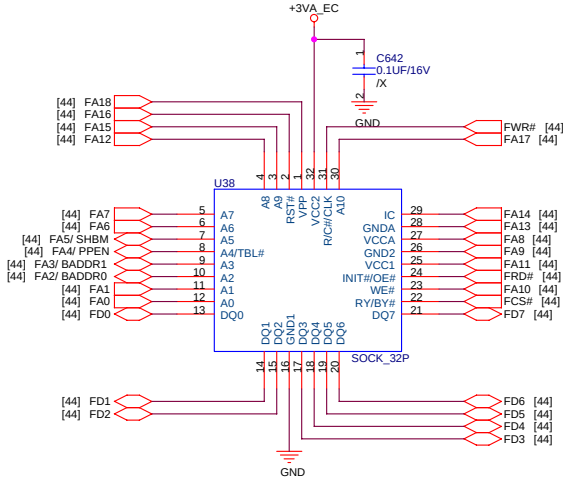


ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: Kell Huang	
Size: A4	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 45 of 60	

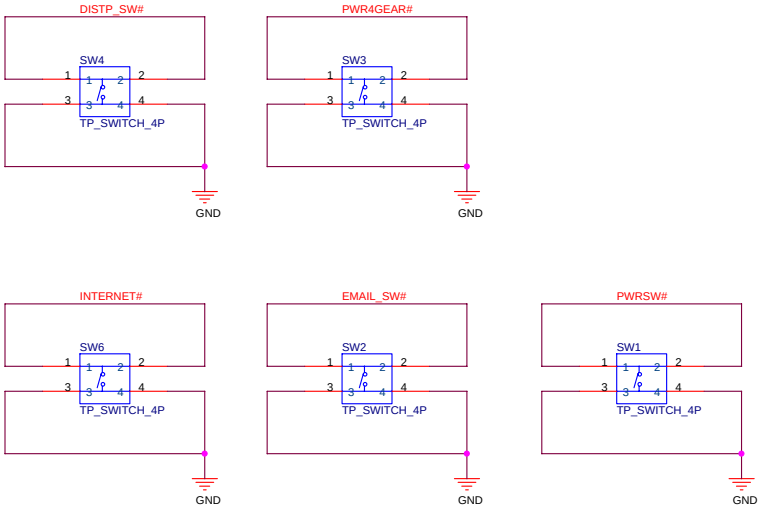
ISA ROM

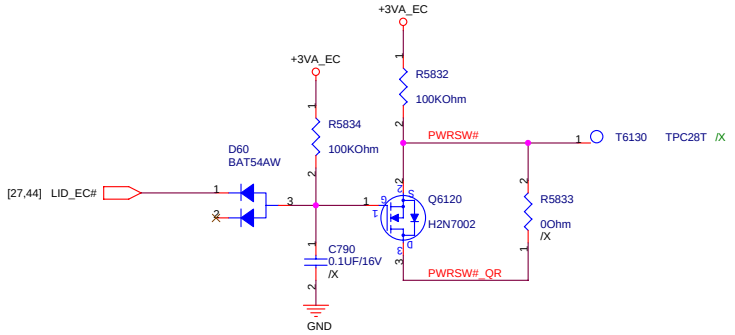




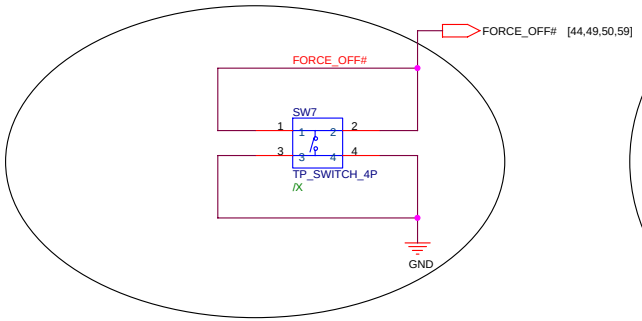


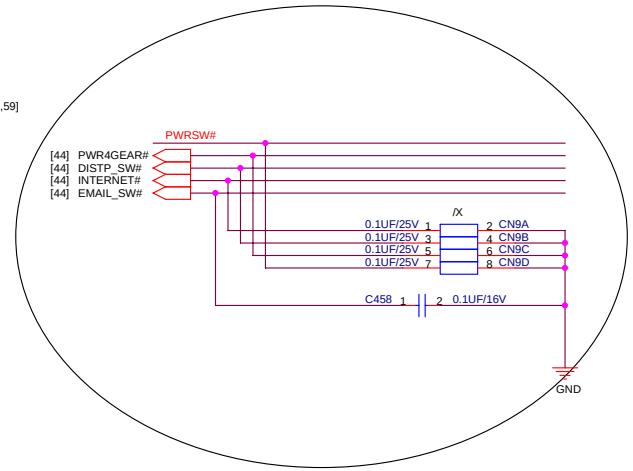
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 46 of 60	

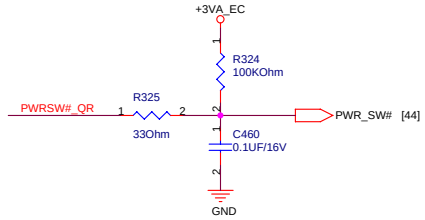




SHUT_DOWN#





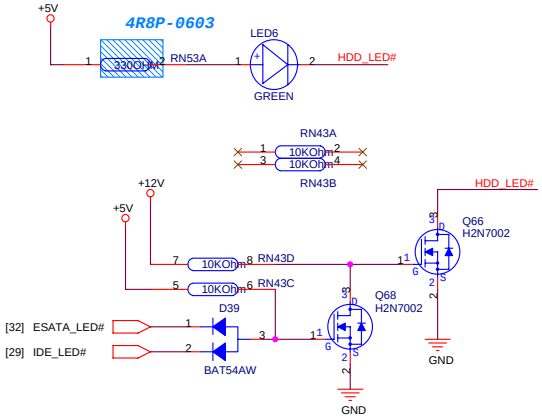


A

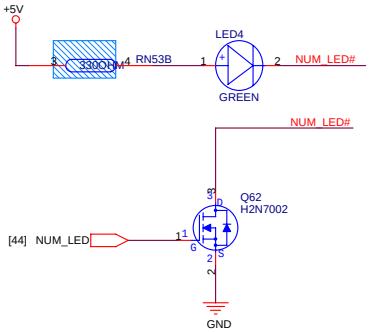
ASUSTeK COMPUTER INC	Title : SWITCH	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 47 of 60	

For LED

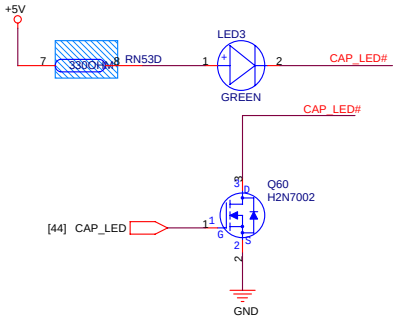
For SATA/IDE LED



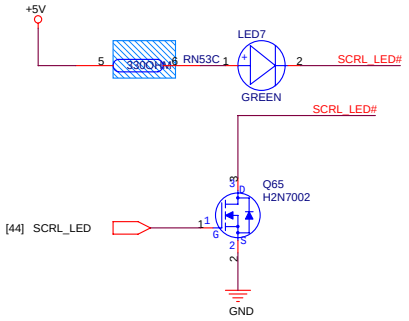
for Num Lock



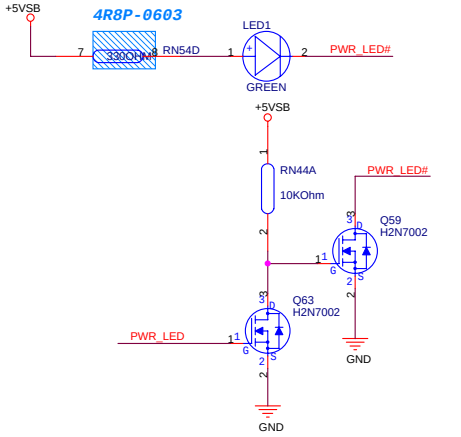
for Cap. Lock



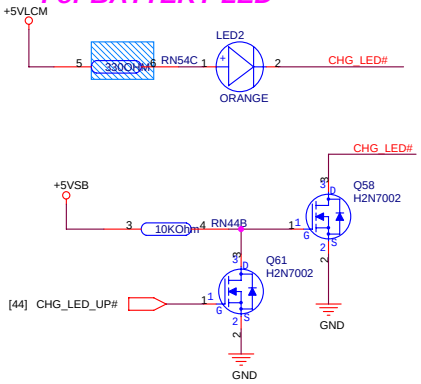
for Scroll Lock



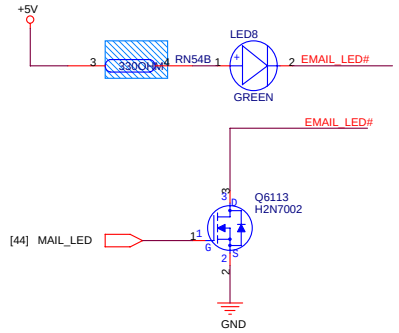
For POWER LED



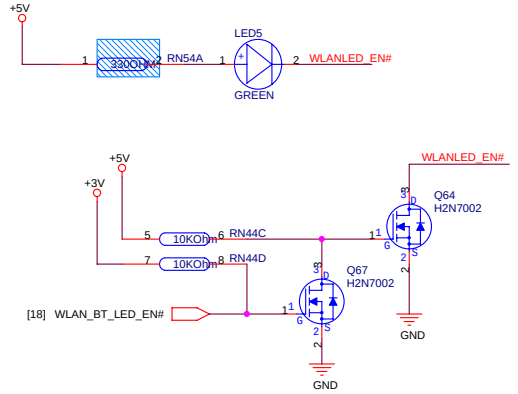
For BATTERY LED

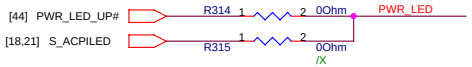


for email



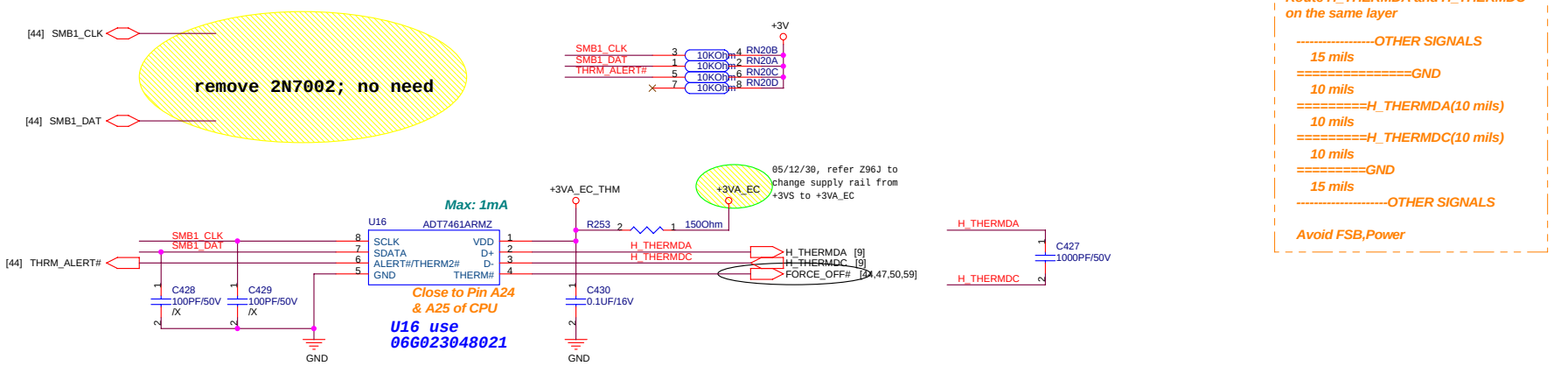
For WireLess LED



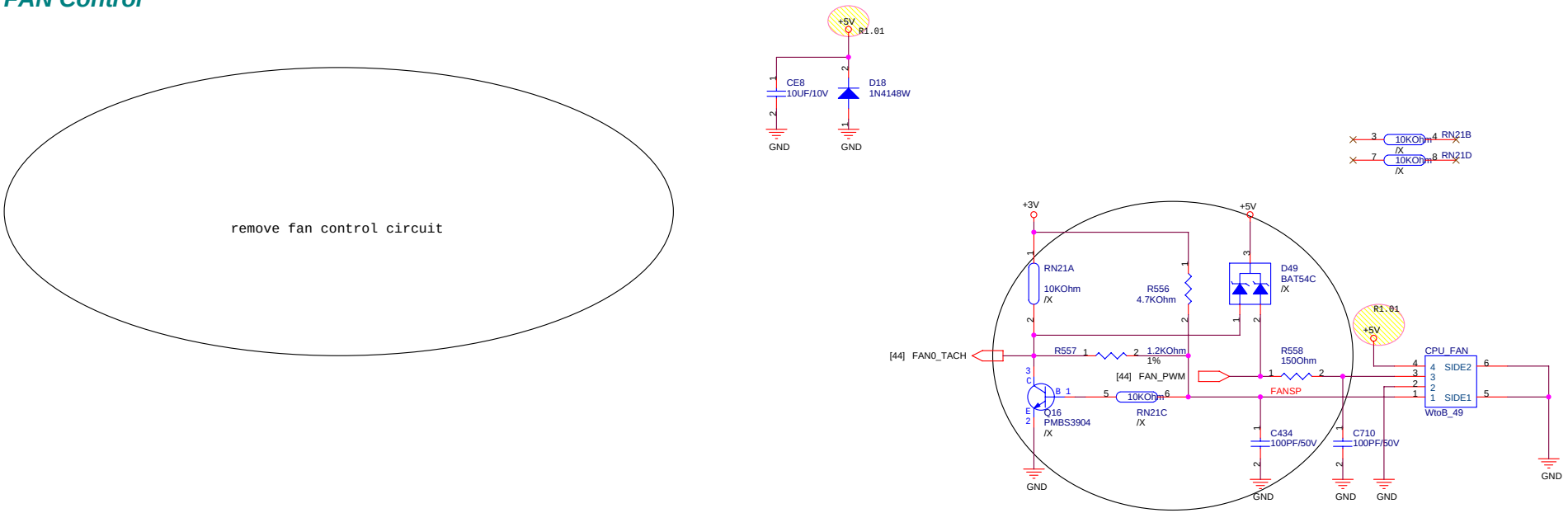


Title : LED		
ASUSTeK COMPUTER INC	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 48 of 60	

Thermal Sensor



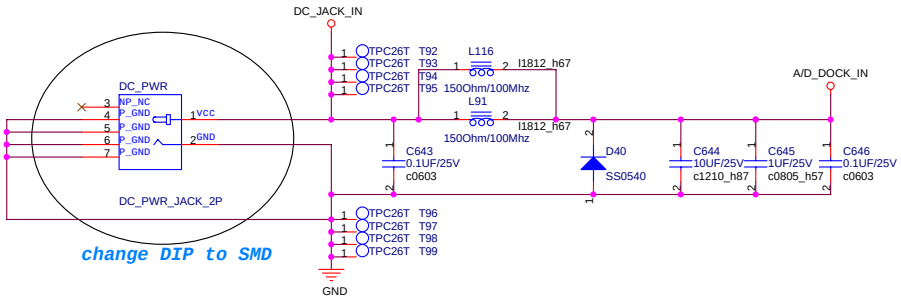
DC FAN Control



CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 49 of 60	

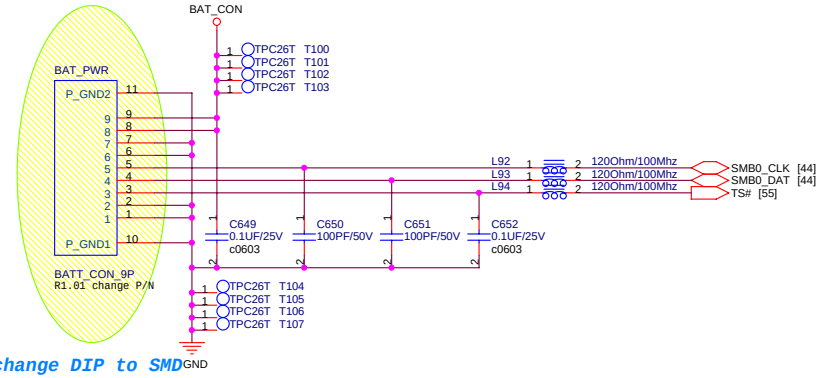
DC IN



change DIP to SMD

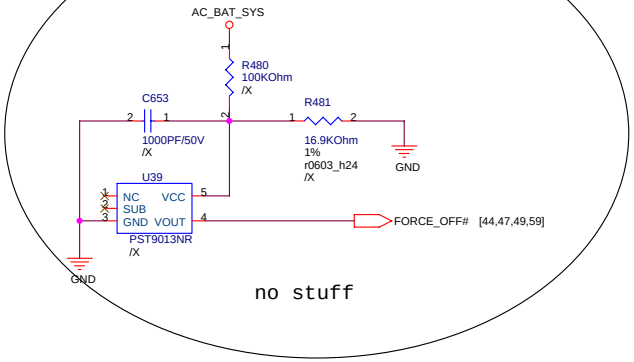
remove AC DC detect; no need

BAT IN



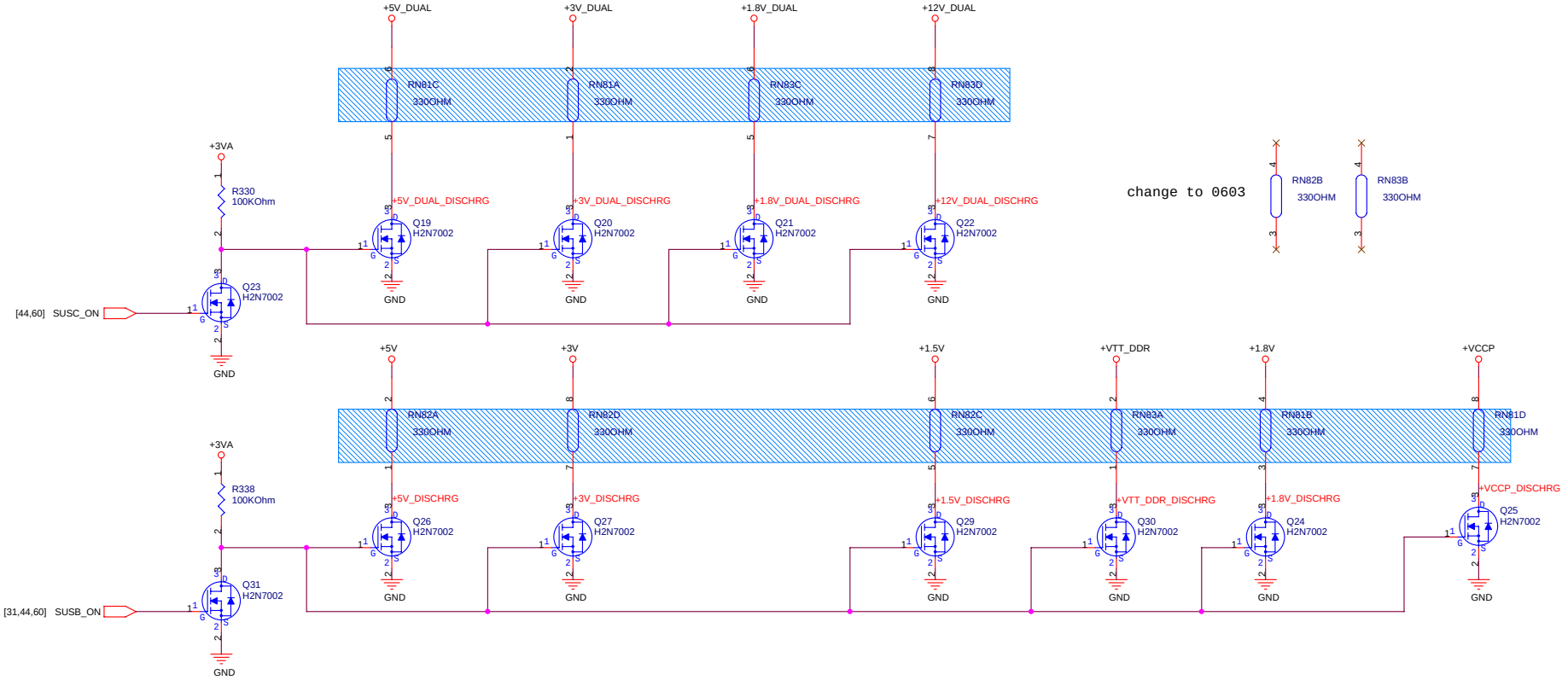
change DIP to SMD

Without Battery & Pull out Adapter



no stuff

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 50 of 60	



ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 51 of 60	

PAD1 SMD394X197

PAD2 SMD394X197

PAD3 SMD394X197

PAD4 SMD394X197

PAD5 SMD394X197

PAD6 SMD1248X197_PT

H47 C236

PAD7 SMD1890X197_PT

PAD8 SMD197X1803

H1

2DRILL_D71N_D110N

H48

2DRILL_D110N_D71N

H19

H5

H15

H25

H7

H13

H9

H17

H11

H27

H21

S354D110N

H50

2DRILL_D87N_D110N

H58

C256D126

H60

C256D126

H52

2DRILL_D110N_D87N

H35

C315D163

H39

C315D163

H62

C315D163

H37

C315D163

H70

C315D163

H71

C315D163

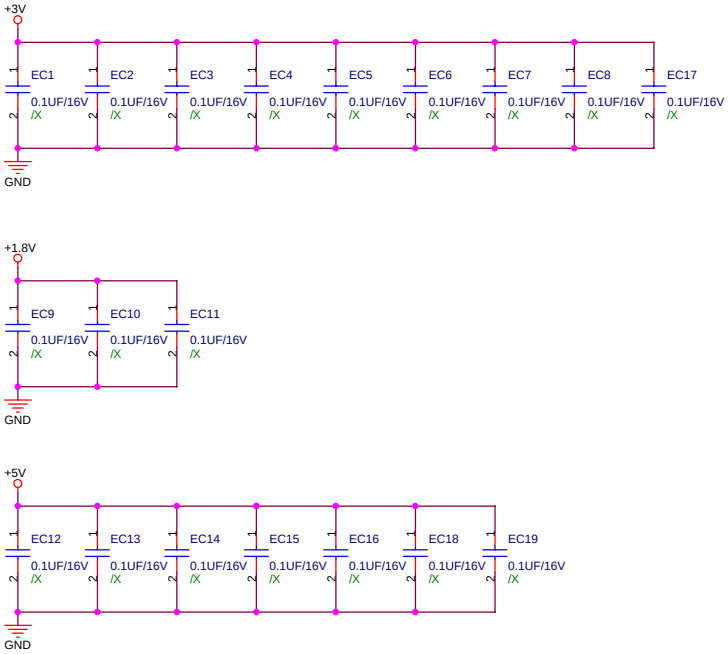
H72

C315D163

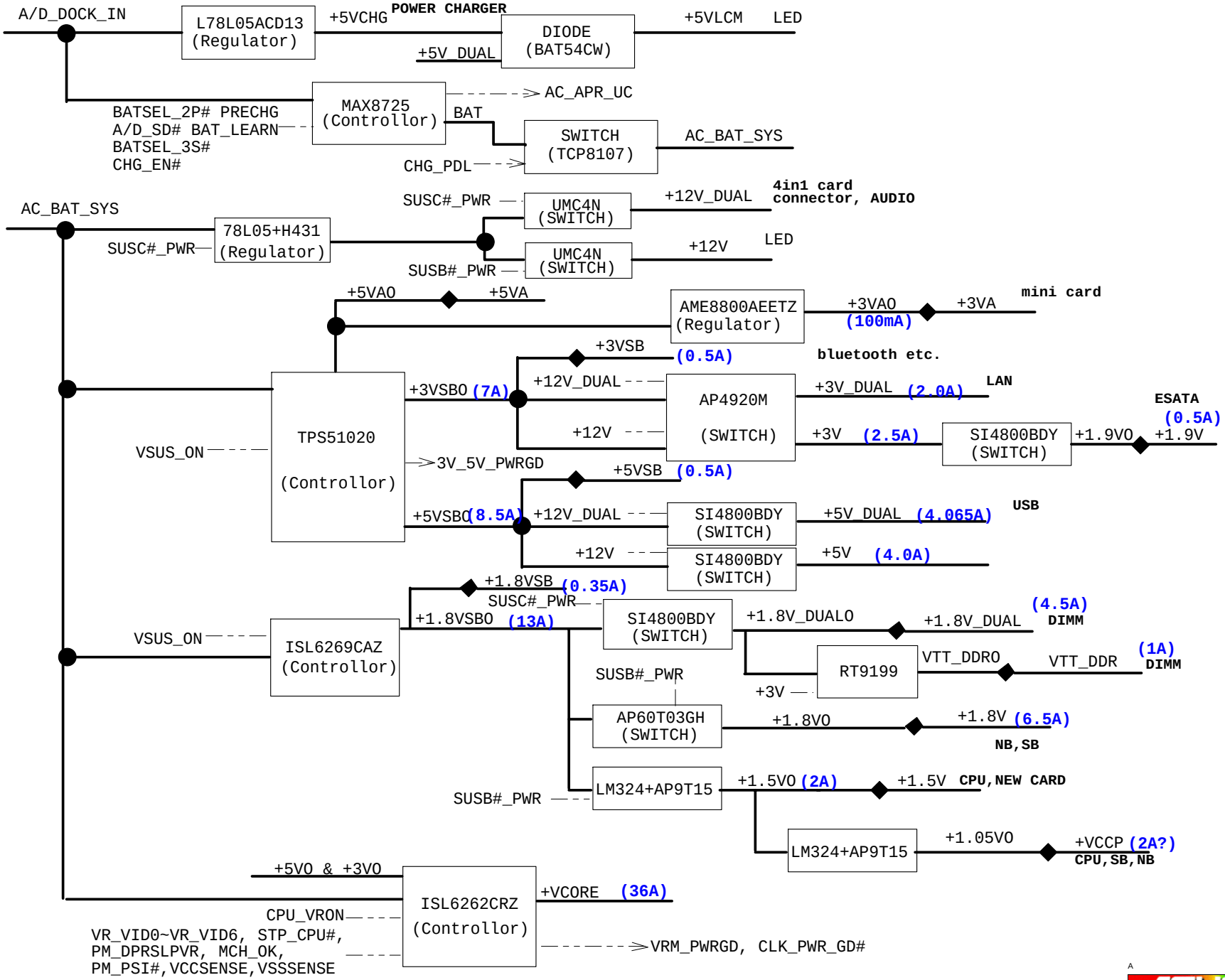
for NB

GND

ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: Kell Huang	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 52 of 60	

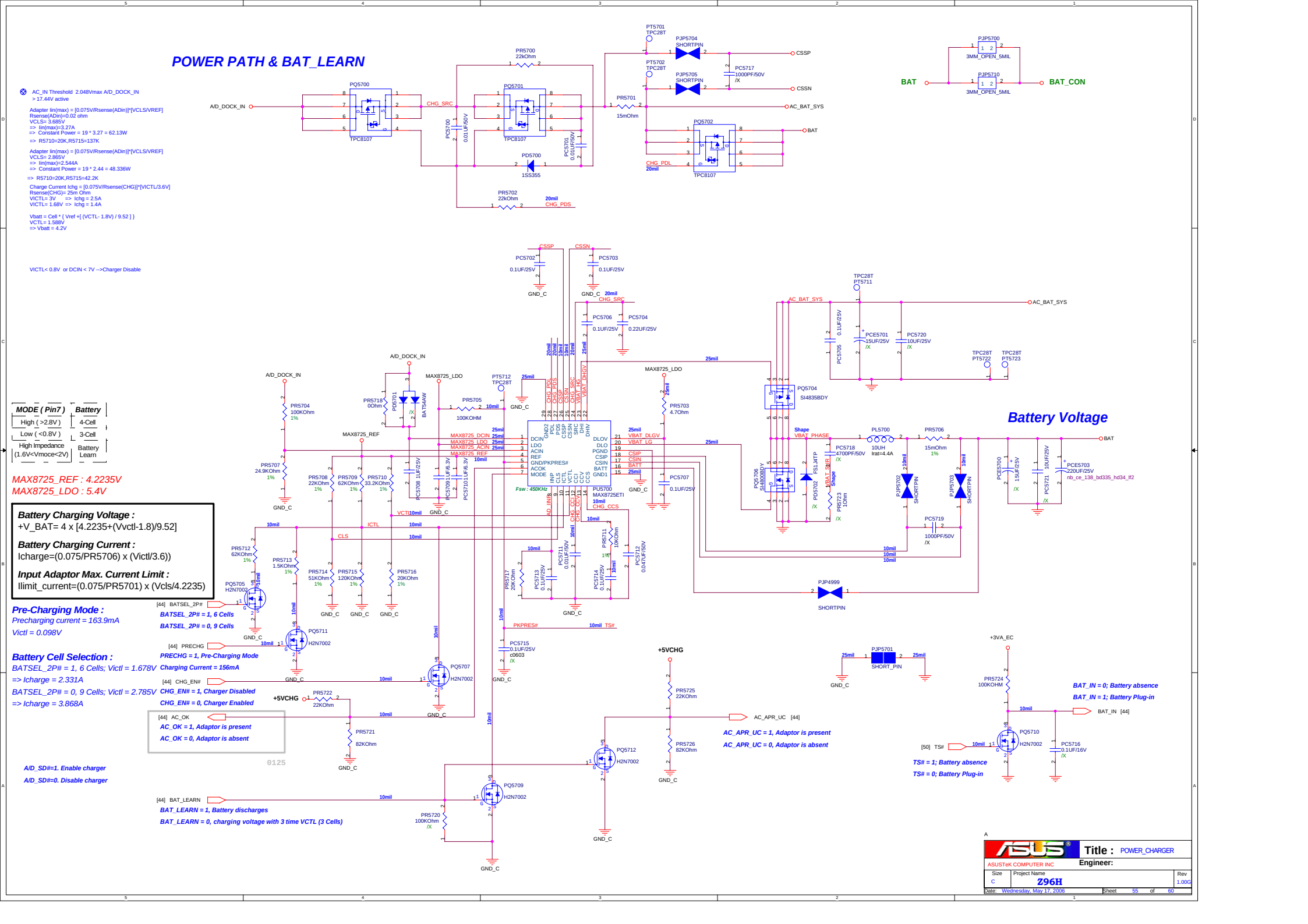


ASUSTeK COMPUTER INC.	Title : EMI	
	Engineer: Kell Huang	
Size: A3	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 53 of 60	



ASUSTeK COMPUTER INC	Title : POWER_FLOWCHART	
	Engineer:	
Size: Custom	Project Name: Z96H	Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 54 of 60	

POWER PATH & BAT_LEARN



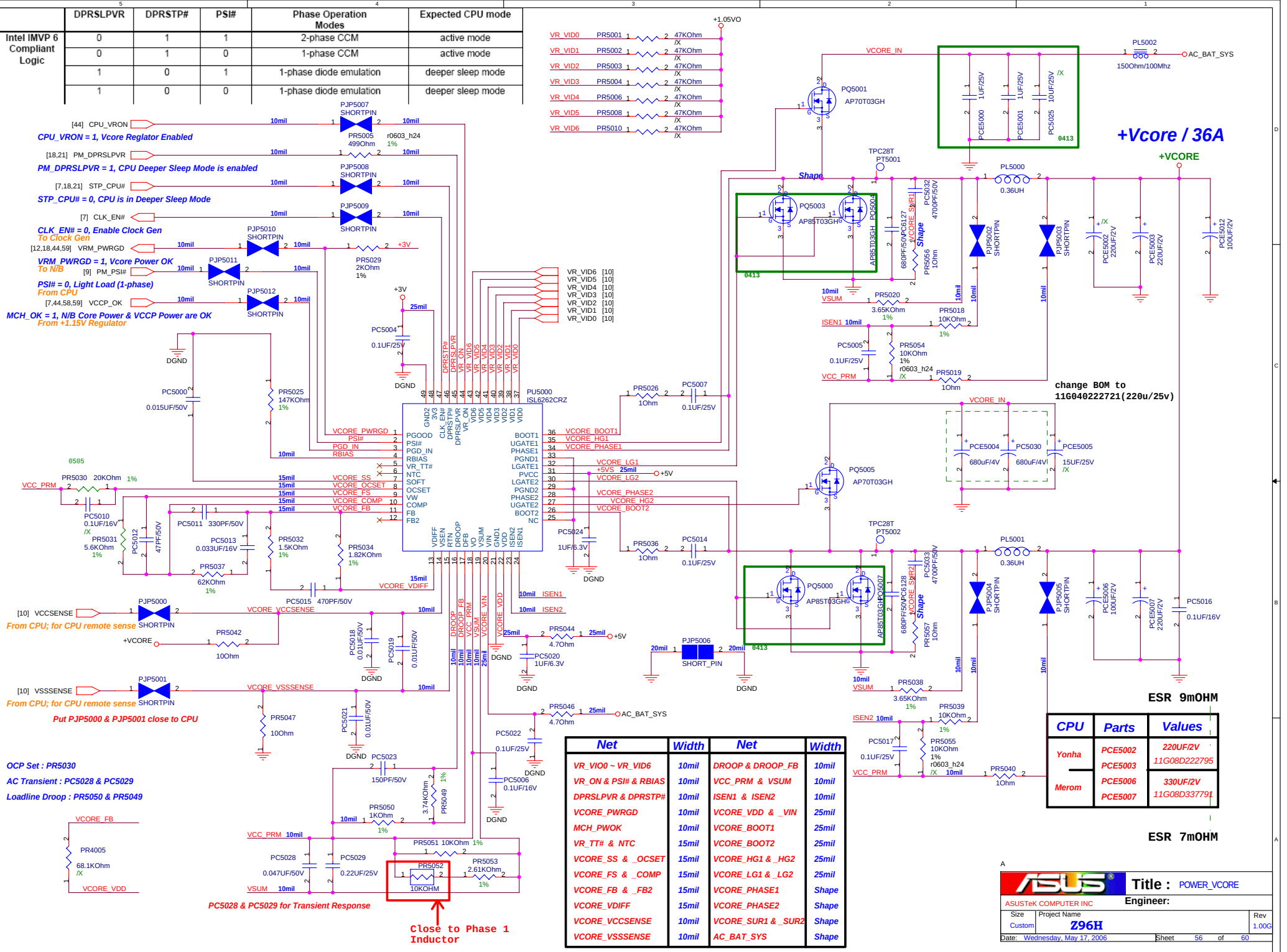
ASUSTeK COMPUTER INC
Engineer:

Size	Project Name	Rev
C	Z96H	1.00G

Title : POWER_CHARGER

Date: Wednesday, May 17, 2006 Sheet 55 of 60

	DPRSLPVR	DPRSTP#	PSI#	Phase Operation Modes	Expected CPU mode
Intel IMVP 6 Compliant Logic	0	1	1	2-phase CCM	active mode
	0	1	0	1-phase CCM	active mode
	1	0	1	1-phase diode emulation	deeper sleep mode
	1	0	0	1-phase diode emulation	deeper sleep mode



Net	Width	Net	Width
VR_VIO0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

CPU	Parts	Values
Yonha	PCE5002	220UF/2V 11G08D222795
	PCE5003	
Merom	PCE5006	330UF/2V 11G08D337791
	PCE5007	

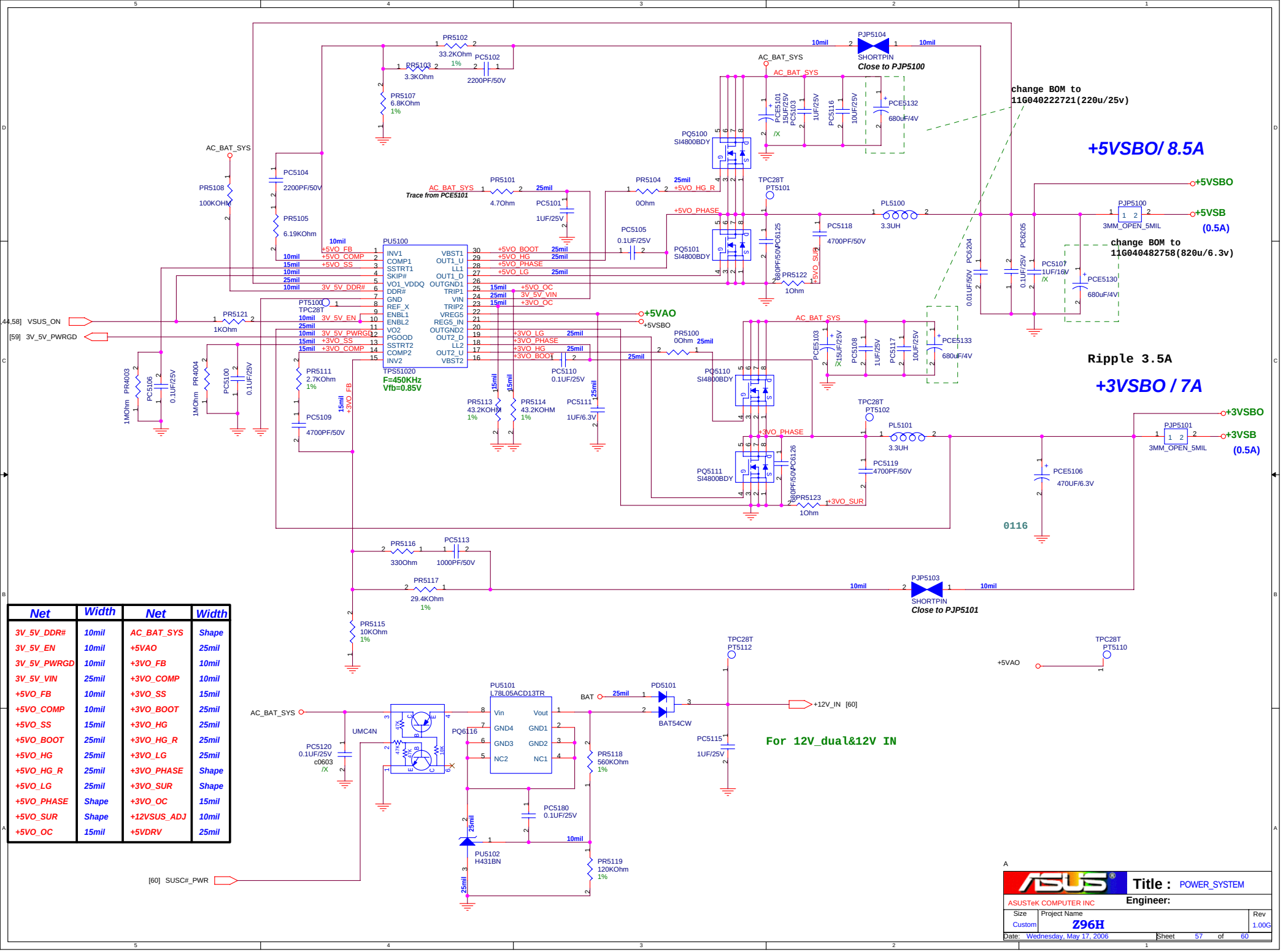
ASUSTeK COMPUTER INC

Title : POWER_VCORE

Engineer:

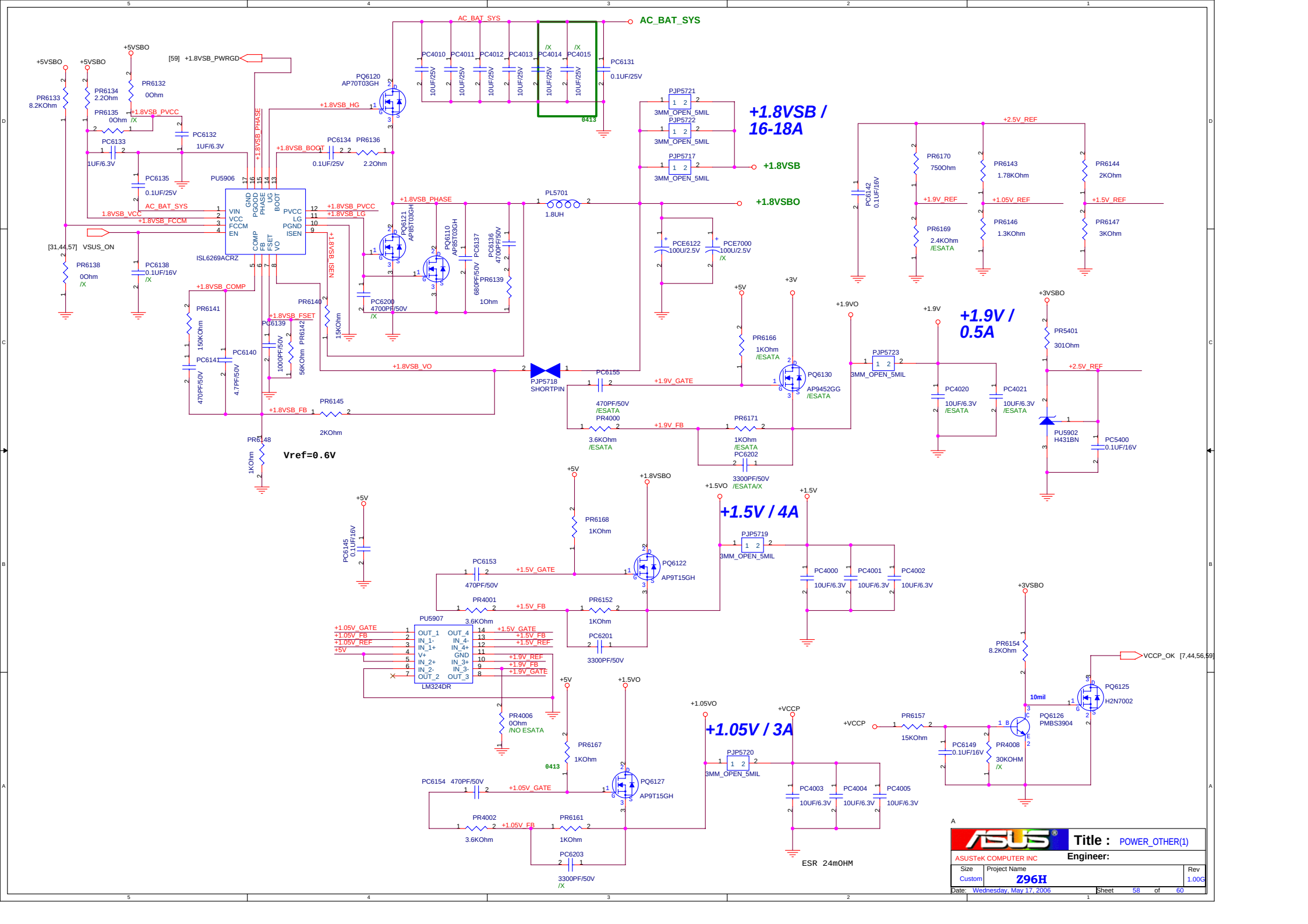
Size	Project Name	Rev
Custom	Z96H	1.00G

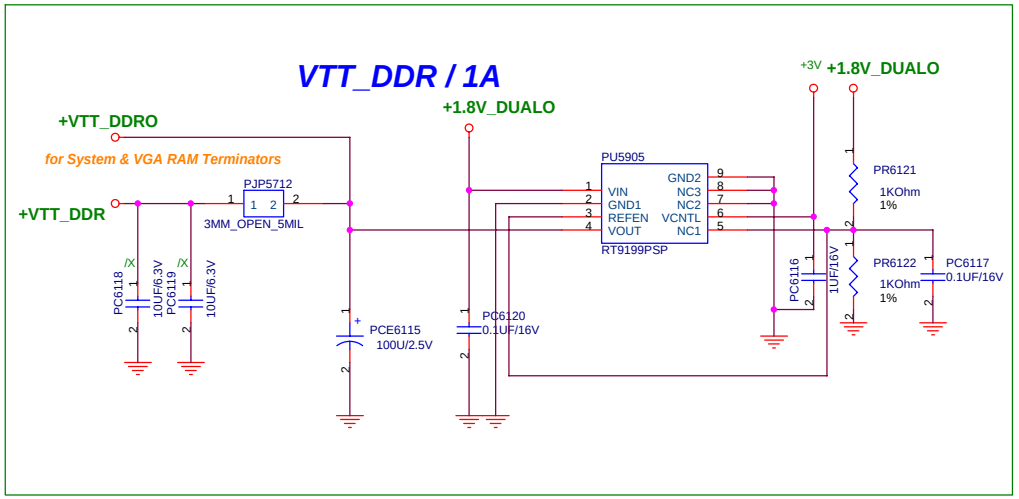
Date: Wednesday, May 17, 2006 Sheet 56 of 60

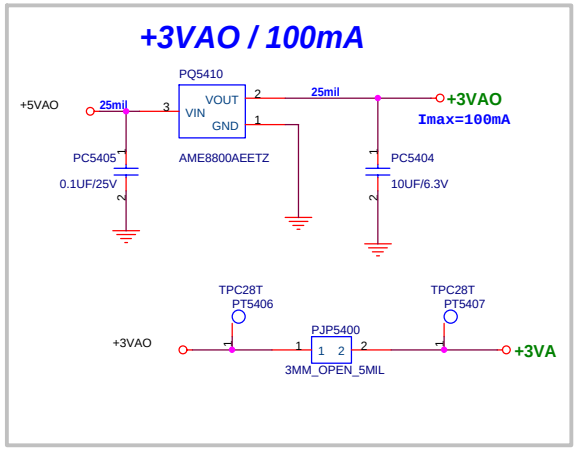


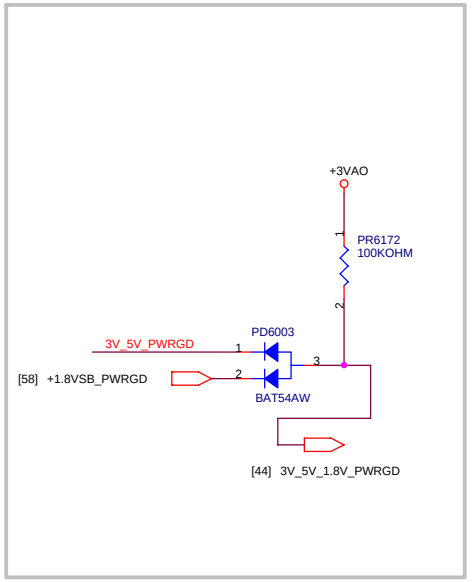
Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

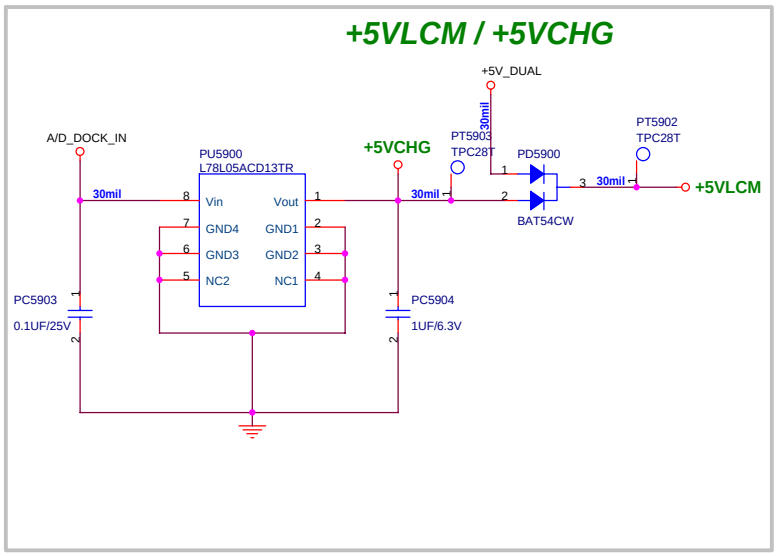
Title : POWER_SYSTEM			
ASUSTeK COMPUTER INC	Engineer:		
Size: Custom	Project Name: Z96H		Rev: 1.00G
Date: Wednesday, May 17, 2006	Sheet 57 of 60		

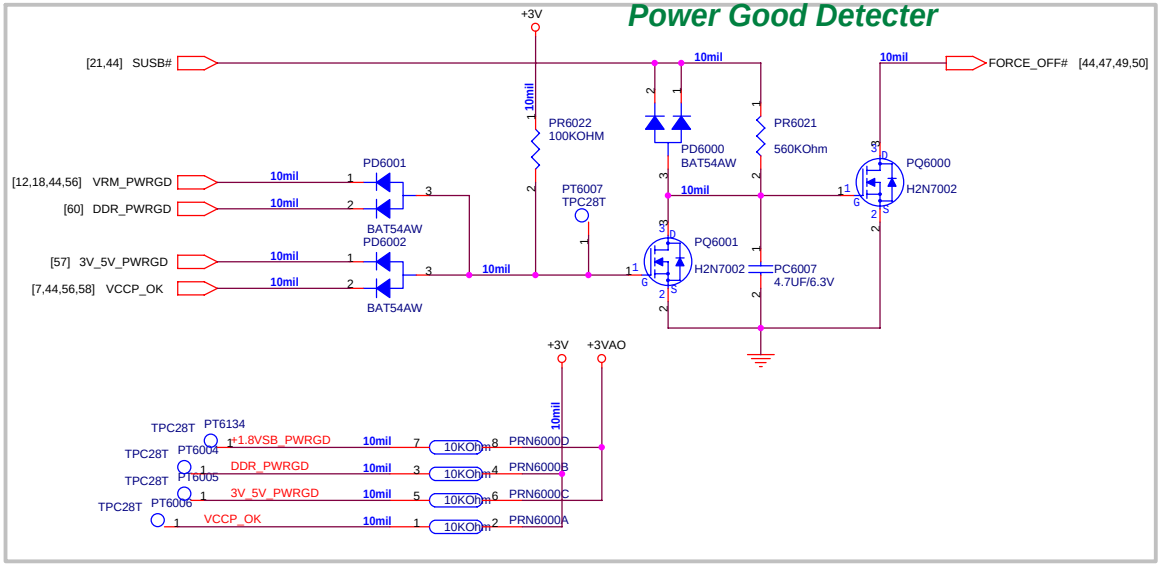

AC_BAT_SYS
+1.8VSB / 16-18A
+1.8VSB
+1.8VSBO
+1.9V / 0.5A
+1.5V / 4A
+1.05V / 3A
ESR 24mOHM
Vref=0.6V
ISL6269ACRZ
PU5906
LM324DR
PU5907
PU5902 H431BN
PQ6120 AP70T03GH
PQ6121 AP85T03GH
PQ6110 AP85T03GH
PQ6130 AP9452GG /ESATA
PQ6122 AP9T15GH
PQ6127 AP9T15GH
PQ6125 H2N7002
PQ6126 PMBS3904
PJP5718 SHORTPIN
PL5701 1.8UH
[59] +1.8VSB_PWRGD
[31,44,57] VSUS_ON
VCCP_OK [7,44,56,59]
Title : POWER_OTHER(1)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name Z96H
Rev 1.00G
Date: Wednesday, May 17, 2006
Sheet 58 of 60











A

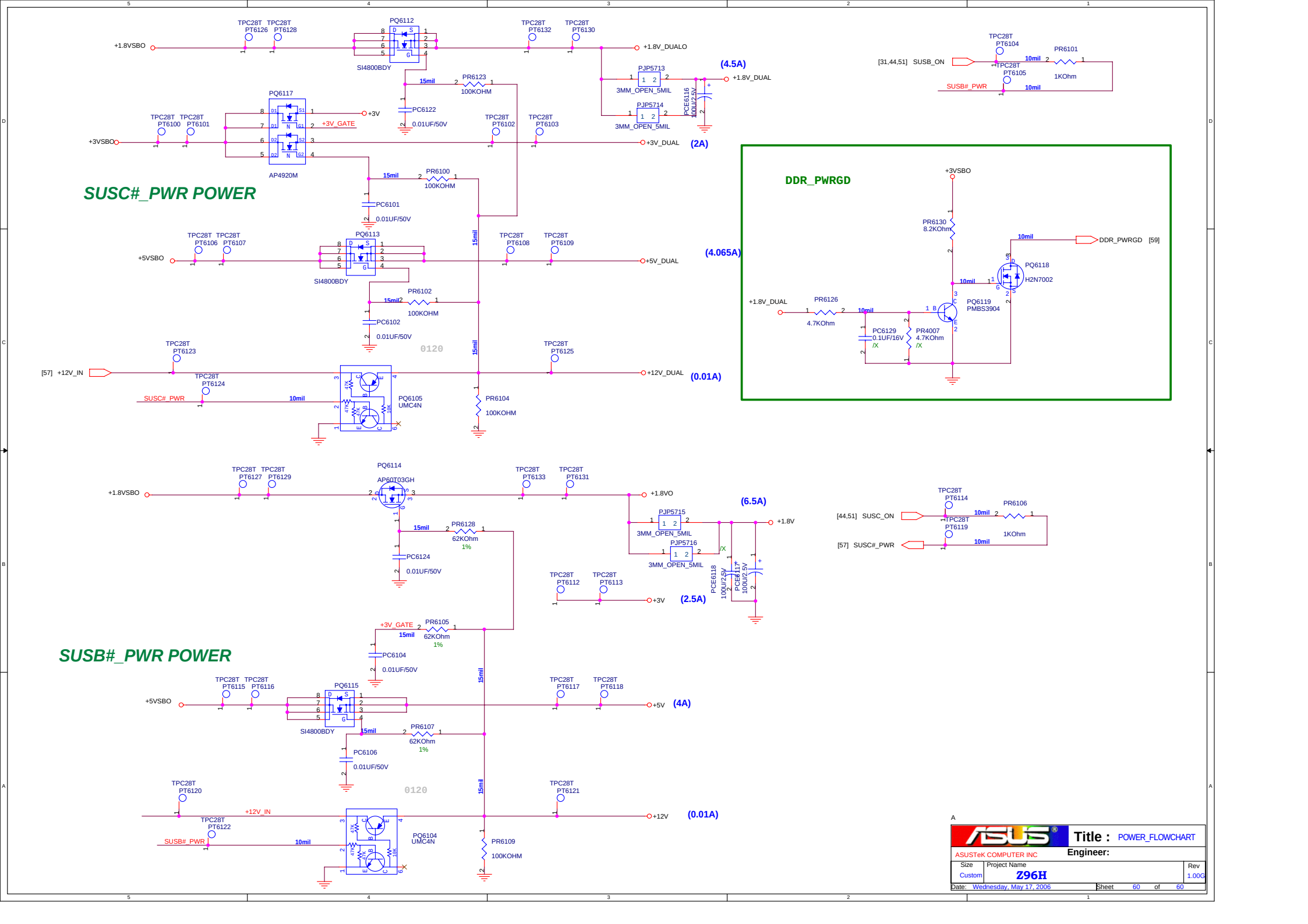
ASUSTeK COMPUTER INC

Title : POWER_OTHER(2)

Engineer:

Size	Project Name	Rev
A3	Z96H	1.00G

Date: Wednesday, May 17, 2006 Sheet 59 of 60


SUSC#_PWR POWER
+1.8VSBO
PQ6112
SI4800BDY
+1.8V_DUALO
(4.5A)
+1.8V_DUAL
PJP5713
3MM_OPEN_5MIL
PJP5714
3MM_OPEN_5MIL
PCE6116
100U/2.5V
PR6123
100KOHM
PC6122
0.01UF/50V
PQ6117
AP4920M
+3V
+3V_GATE
+3VSBO
+3V_DUAL
(2A)
PR6100
100KOHM
PC6101
0.01UF/50V
PQ6113
SI4800BDY
+5VSBO
+5V_DUAL
(4.065A)
PR6102
100KOHM
PC6102
0.01UF/50V
0120
[57] +12V_IN
SUSC#_PWR
PQ6105
UMC4N
PR6104
100KOHM
+12V_DUAL
(0.01A)
DDR_PWRGD
+3VSBO
PR6130
8.2KOhm
PQ6118
H2N7002
DDR_PWRGD [59]
+1.8V_DUAL
PR6126
4.7KOhm
PQ6119
PMBS3904
PC6129
0.1UF/16V
/X
PR4007
4.7KOhm
/X
[31,44,51] SUSB_ON
PR6101
1KOhm
SUSB#_PWR
SUSB#_PWR POWER
+1.8VSBO
PQ6114
AP60T03GH
+1.8VO
(6.5A)
+1.8V
PJP5715
3MM_OPEN_5MIL
PJP5716
3MM_OPEN_5MIL
PCE6118
100U/2.5V
PCE6117
100U/2.5V
PR6128
62KOhm
1%
PC6124
0.01UF/50V
+3V
(2.5A)
PR6105
62KOhm
1%
PC6104
0.01UF/50V
+5VSBO
PQ6115
SI4800BDY
+5V
(4A)
PR6107
62KOhm
1%
PC6106
0.01UF/50V
0120
+12V_IN
SUSB#_PWR
PQ6104
UMC4N
PR6109
100KOHM
+12V
(0.01A)
[44,51] SUSC_ON
PR6106
1KOhm
[57] SUSC#_PWR
Title : POWER_FLOWCHART
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
Z96H
Rev
1.00G
Date: Wednesday, May 17, 2006
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