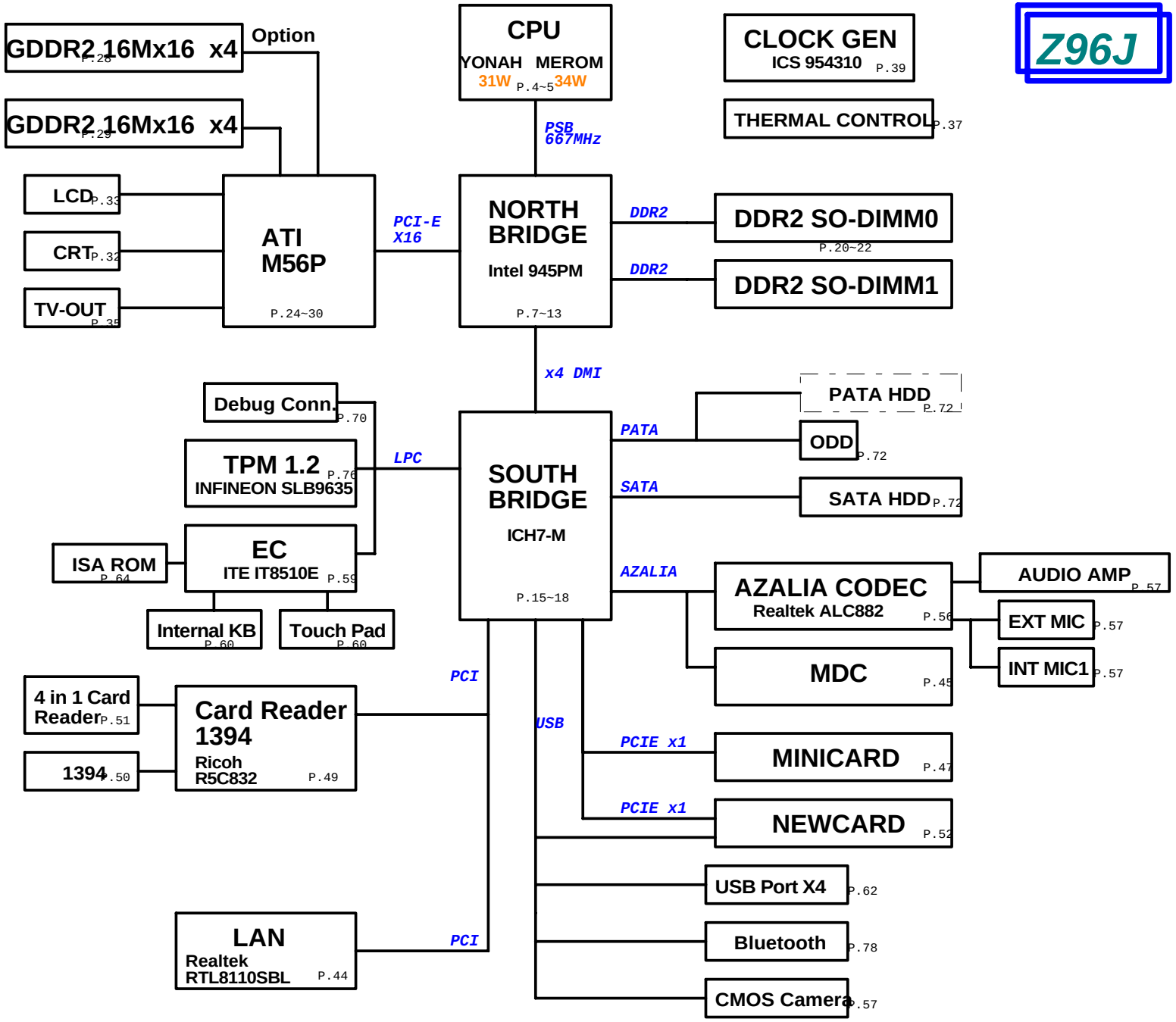

Z96J
GDDR2 16Mx16 x4
P.28
Option
GDDR2 16Mx16 x4
P.29
CPU
YONAH MEROM
31W 34W
P.4~5
CLOCK GEN
ICS 954310 P.39
THERMAL CONTROL P.37
PSB
667MHz
LCD P.33
CRT P.32
TV-OUT P.35
ATI
M56P
P.24~30
PCI-E
X16
NORTH
BRIDGE
Intel 945PM
P.7~13
DDR2
DDR2 SO-DIMM0
P.20~22
DDR2
DDR2 SO-DIMM1
x4 DMI
Debug Conn. P.70
TPM 1.2
INFINEON SLB9635 P.76
LPC
SOUTH
BRIDGE
ICH7-M
P.15~18
PATA
PATA HDD P.72
ODD P.72
SATA
SATA HDD P.72
ISA ROM P.64
EC
ITE IT8510E P.59
Internal KB P.60
Touch Pad P.60
AZALIA
AZALIA CODEC
Realtek ALC882 P.56
AUDIO AMP P.57
EXT MIC P.57
INT MIC1 P.57
MDC P.45
PCI
4 in 1 Card
Reader P.51
1394 P.50
Card Reader
1394
Ricoh
R5C832 P.49
USB
PCIE x1
MINICARD P.47
PCIE x1
NEWCARD P.52
USB Port X4 P.62
Bluetooth P.78
CMOS Camera P.57
PCI
LAN
Realtek
RTL8110SBL P.44
Title : Block Diagram
ASUSTek Computer INC.
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 1 of 92

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0100110X (98)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

ASUSTek Computer INC.

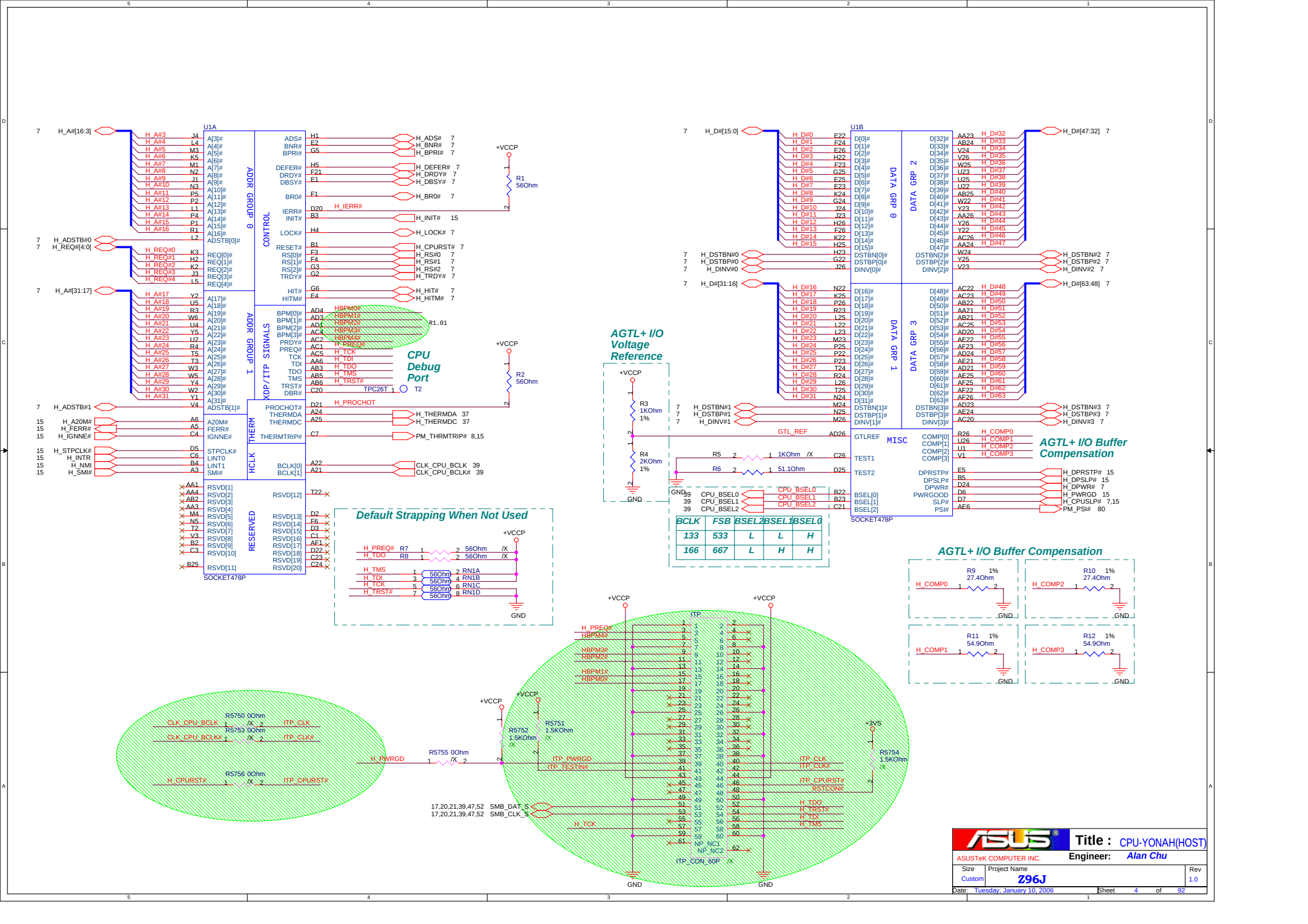
Title : <Title>

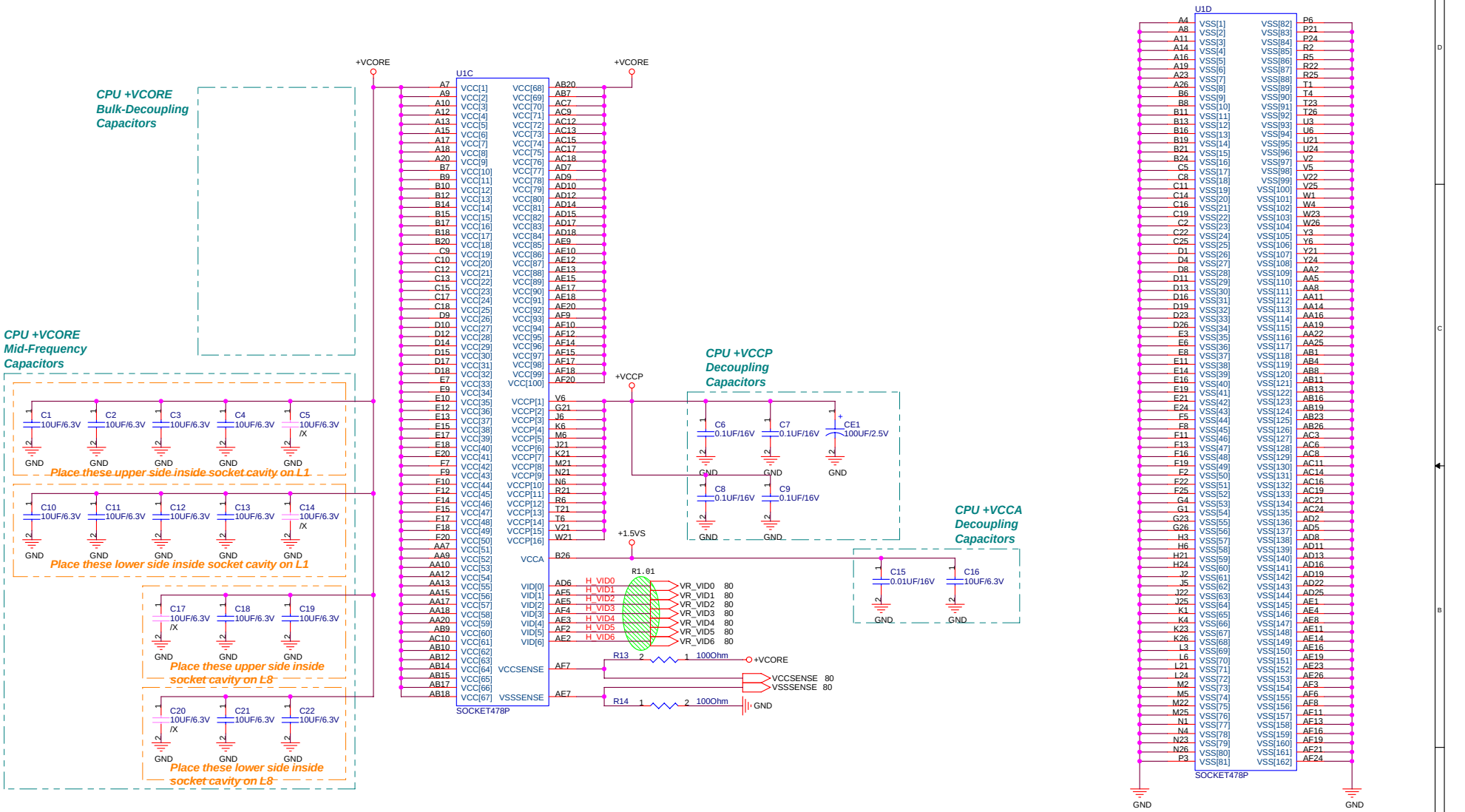
Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

Date: Tuesday, January 10, 2006 Sheet 2 of 92

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 3 of 92

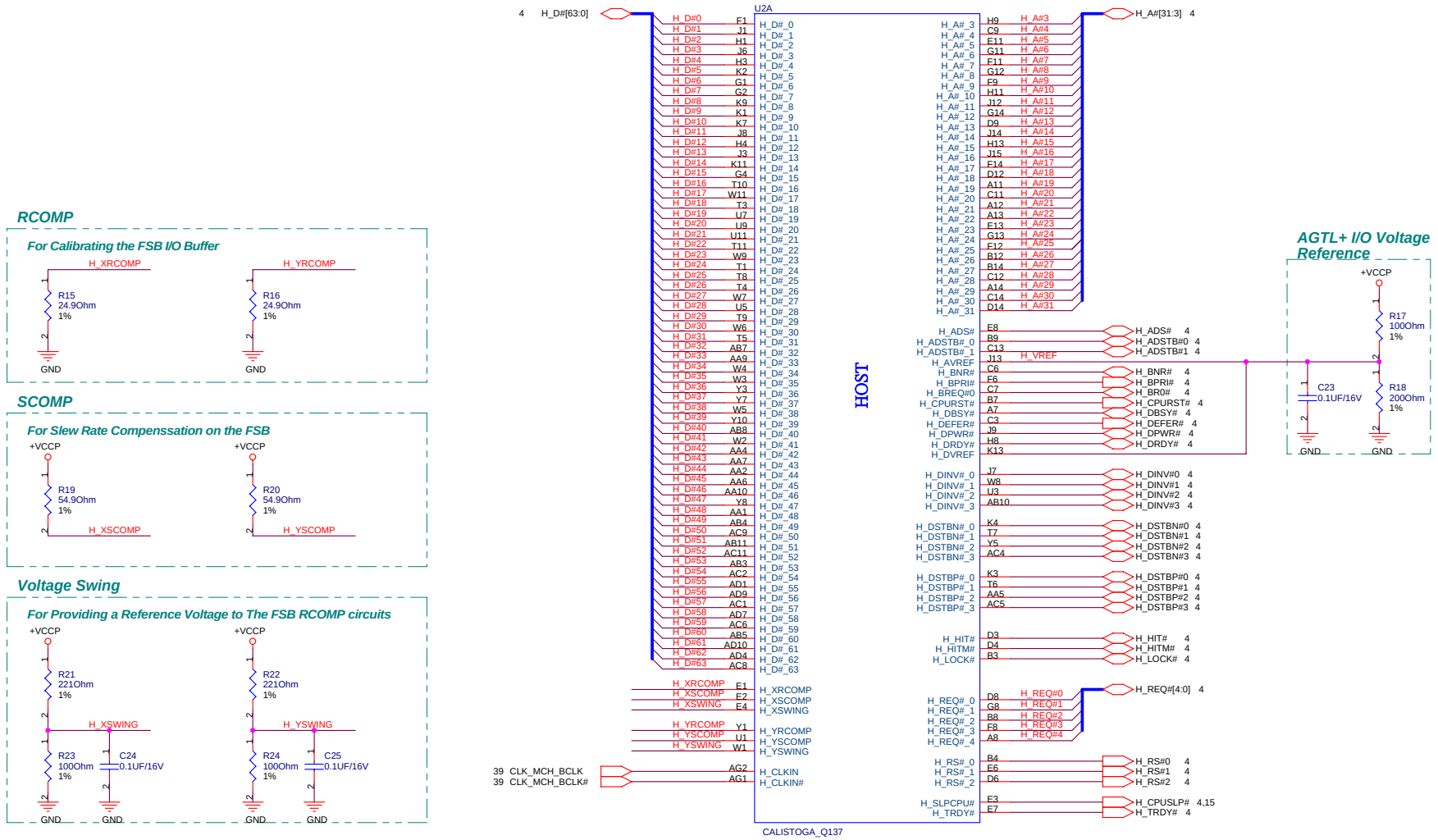

U1A
U1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478P
CPU Debug Port
AGTL+ I/O Voltage Reference
AGTL+ I/O Buffer Compensation
Default Strapping When Not Used
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 4 of 92



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 5 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Frank Wang
Size: Custom	Project Name: F3J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 6 of 92



ASUSTeK COMPUTER INC.	Title : NB-945PM(HOST)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 7 of 92	

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — R25 1KOhm /X — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — R26 1KOhm /X — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — R27 1KOhm /X — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — R30 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 1KOhm /X — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — R34 1KOhm /X — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+2.5VS — MCH_CFG_18 — R35 1KOhm /X

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — R37 1KOhm /X — GND

CFG19 : DMI Lane Reversal

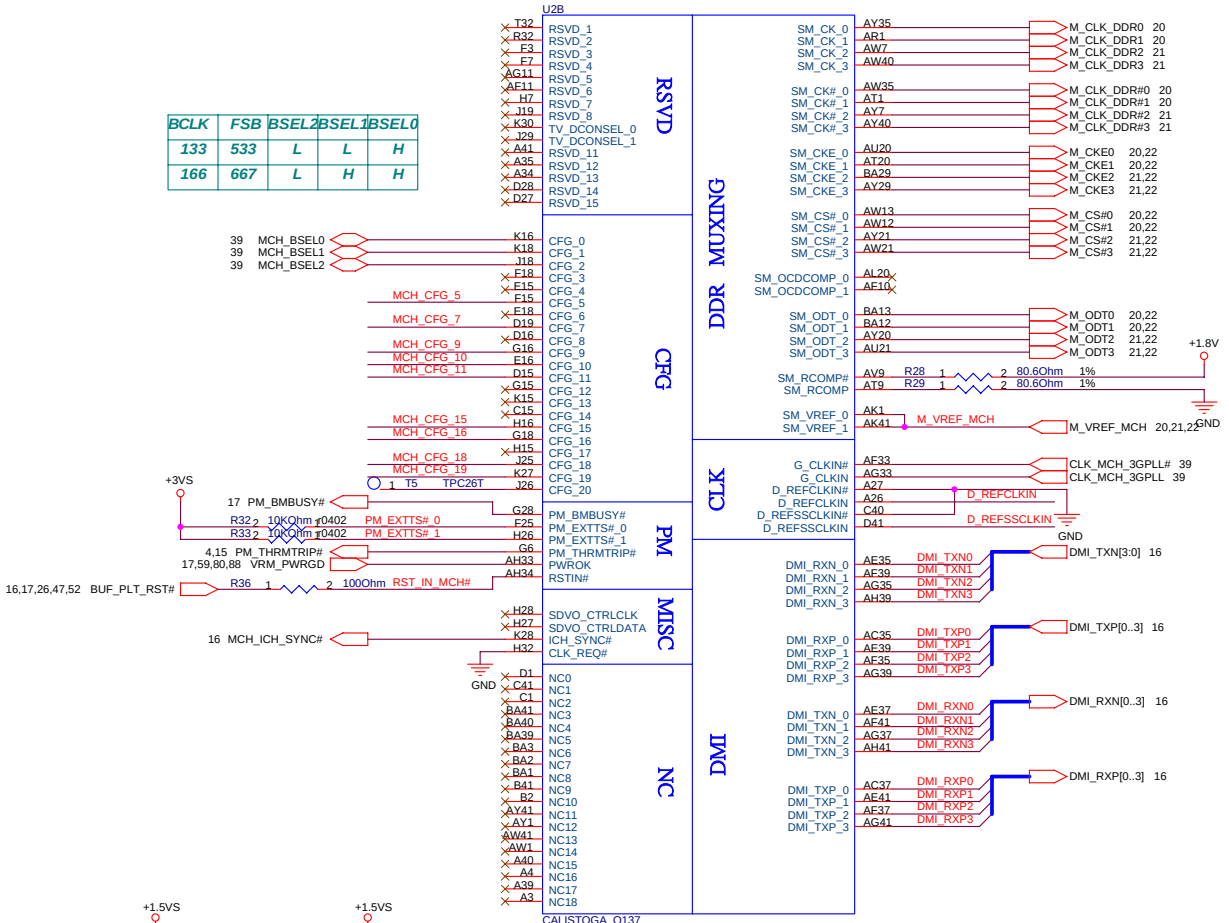
0 = Normal Operation (D)

1 = Lanes Reversed

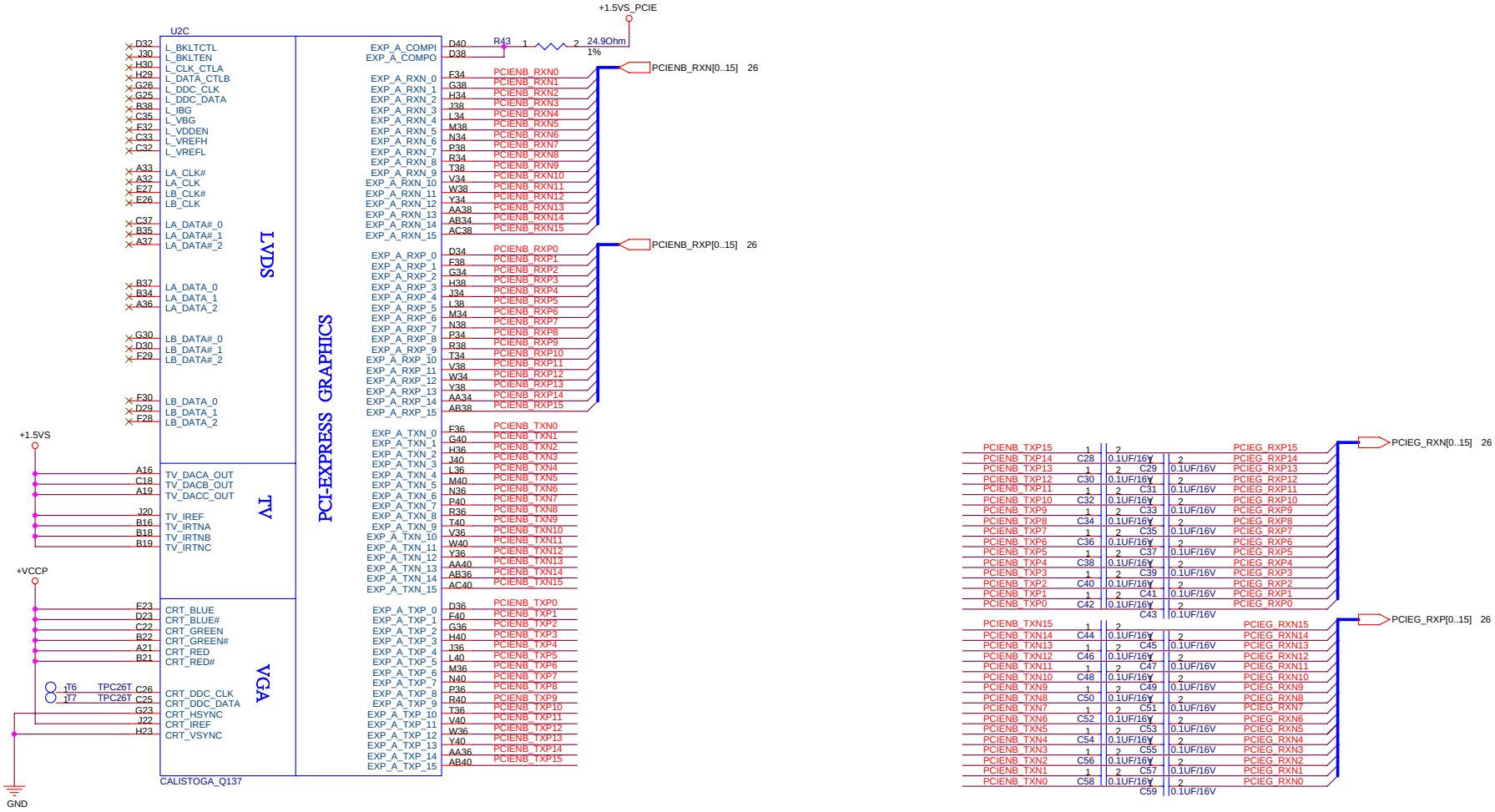
+2.5VS — MCH_CFG_19 — R38 1KOhm /X — GND

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

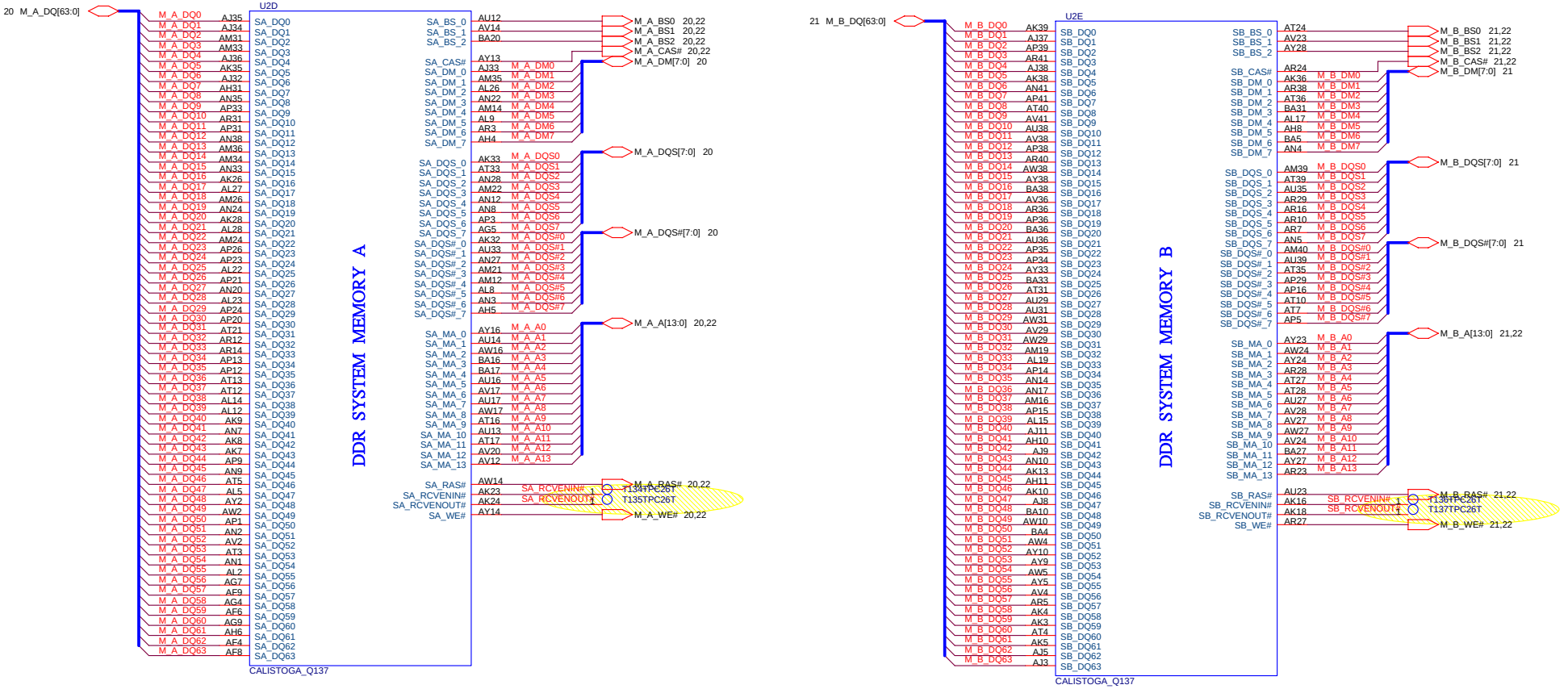
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



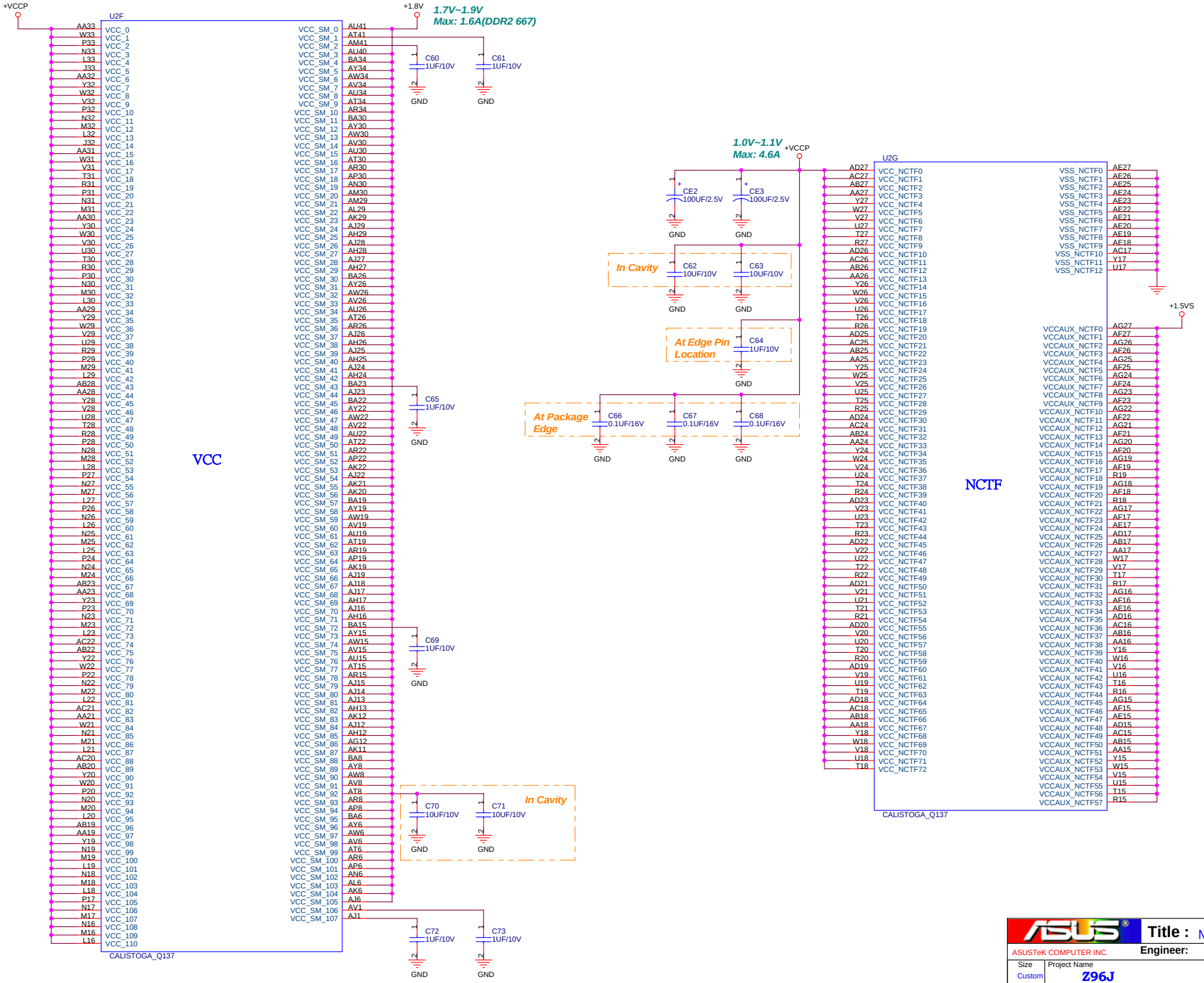
ASUSTeK COMPUTER INC.	Title : NB-945PM(DMI & CFG)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 8 of 92	



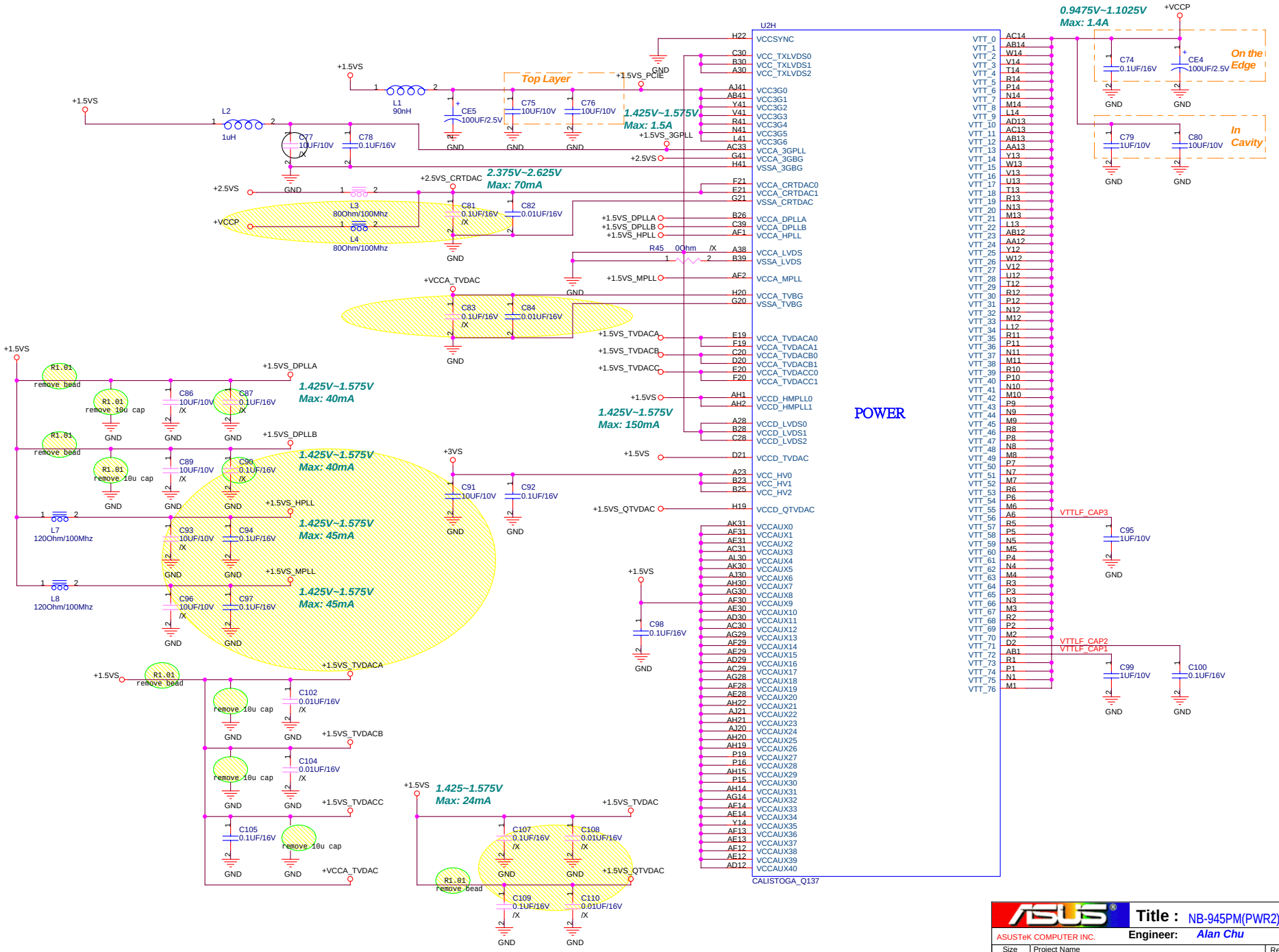
Title :	NB_945PM(GRAPHIC)
ASUSTeK COMPUTER INC.	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 9 of 92

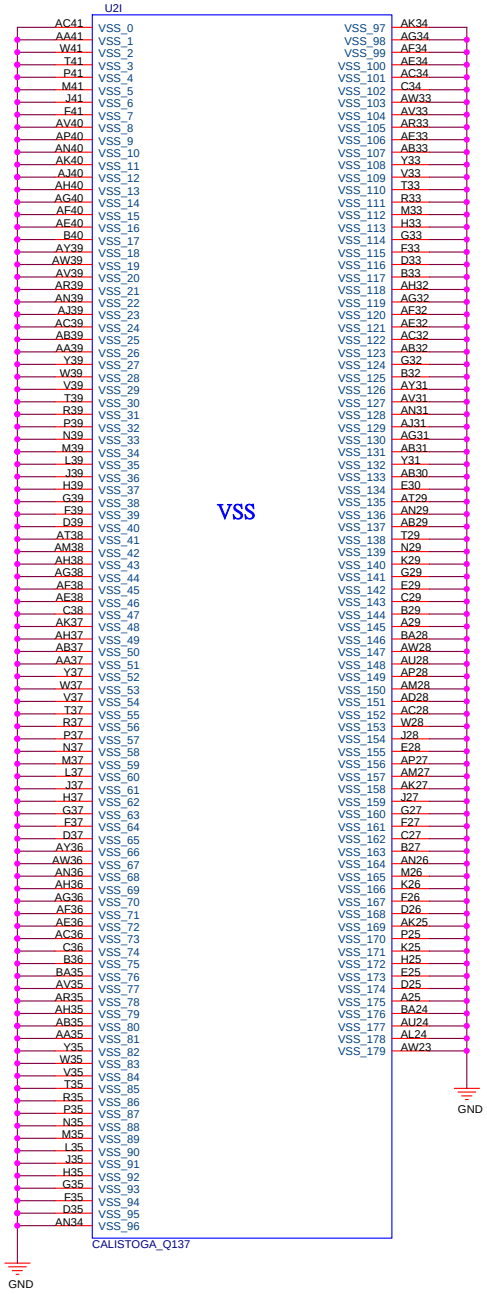


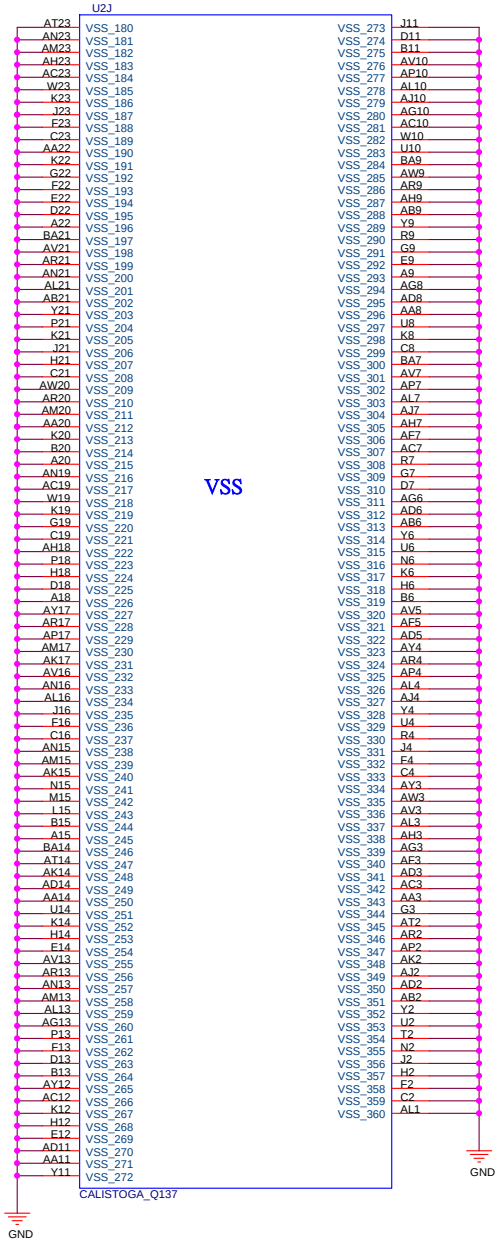
ASUSTeK COMPUTER INC.	Title : NB-945PM(DDR2)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 10 of 92	



Title :	NB-945PM(PWR)	
ASUSTeK COMPUTER INC.	Engineer:	Alan Chu
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 11 of 92	

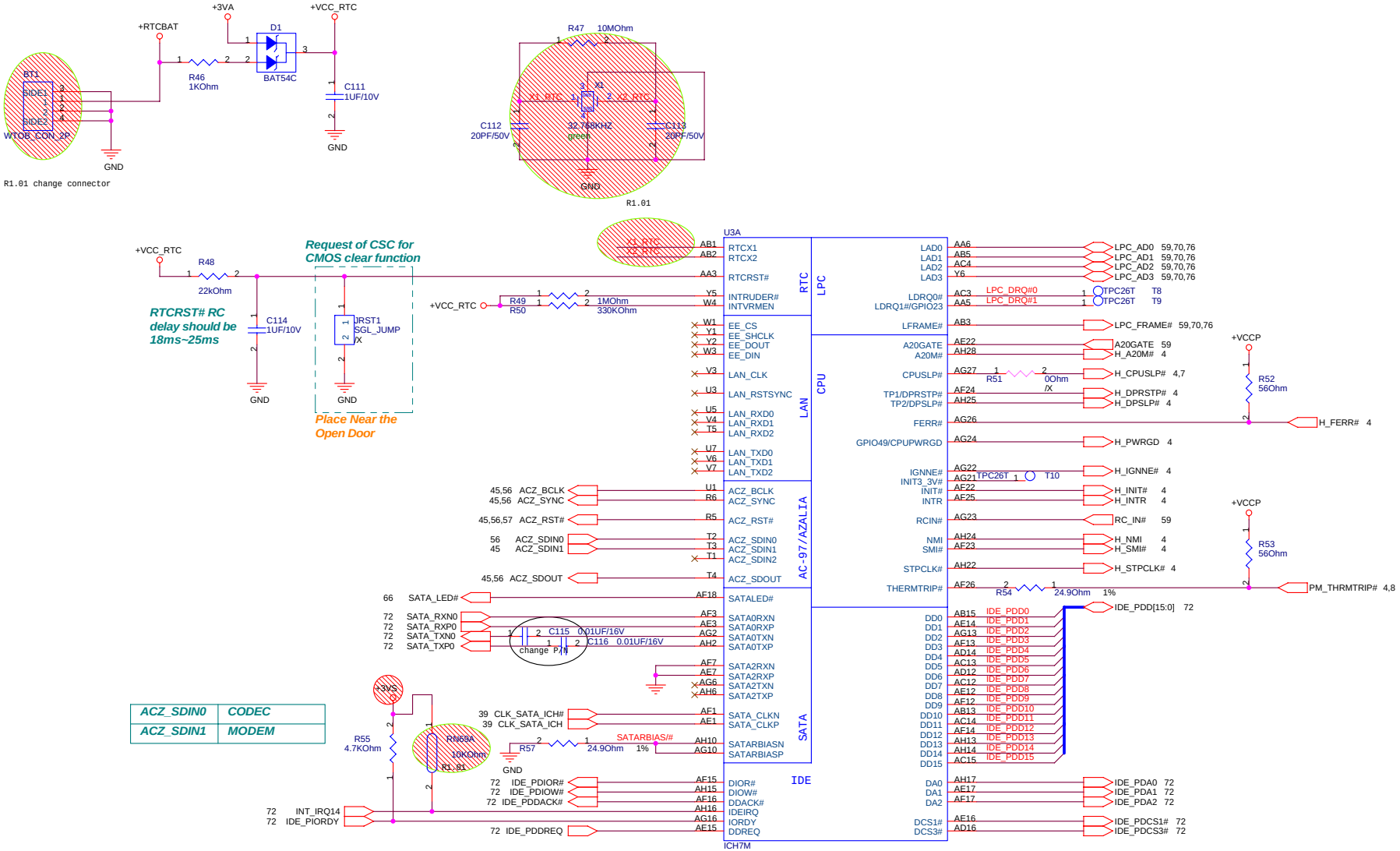

U2H
POWER
CALISTOGA_Q137
Top Layer
On the Edge
In Cavity
0.9475V~1.1025V
Max: 1.4A
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 150mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
1.425~1.575V
Max: 24mA
+1.5VS
+2.5VS
+VCCP
+3VS
+1.5VS_PCIE
+1.5VS_3GPLL
+2.5VS_CRTDAC
+VCCA_TVDAC
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS_TVDACA
+1.5VS_TVDACB
+1.5VS_TVDACC
+1.5VS_QTVDAC
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
L1 90nH
L2 1uH
L3 80Ohm/100Mhz
L4 80Ohm/100Mhz
L7 120Ohm/100Mhz
L8 120Ohm/100Mhz
R45 0Ohm /X
R1.01 remove bead
R1.01 remove 10u cap
remove 10u cap
remove bead
GND
ASUSTeK COMPUTER INC.
Title : NB-945PM(PWR2)
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 12 of 92



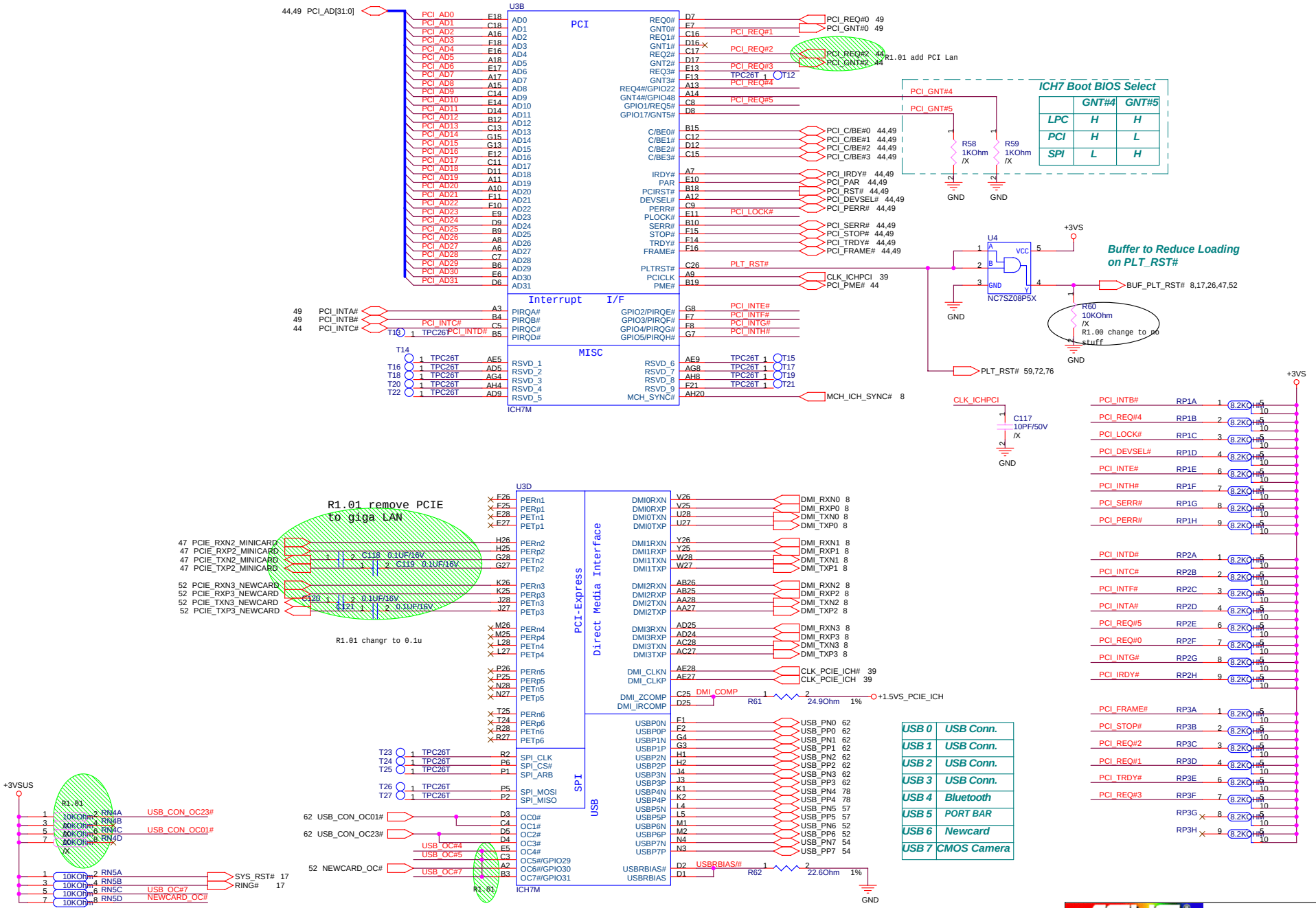


ASUSTeK COMPUTER INC.	Title : NB-945PM(GND)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 13 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 14 of 92



Title :	SB-ICH7-M(1)
ASUSTeK COMPUTER INC.	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 15 of 92


U3B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4
GNT#5
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
NC7SZ08P5X
R1.01 add PCI Lan
R1.01 remove PCIE to giga LAN
R1.01 changr to 0.1u
U3D
PCI-Express
Direct Media Interface
SPI
USB
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 PORT BAR
USB 6 Newcard
USB 7 CMOS Camera
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
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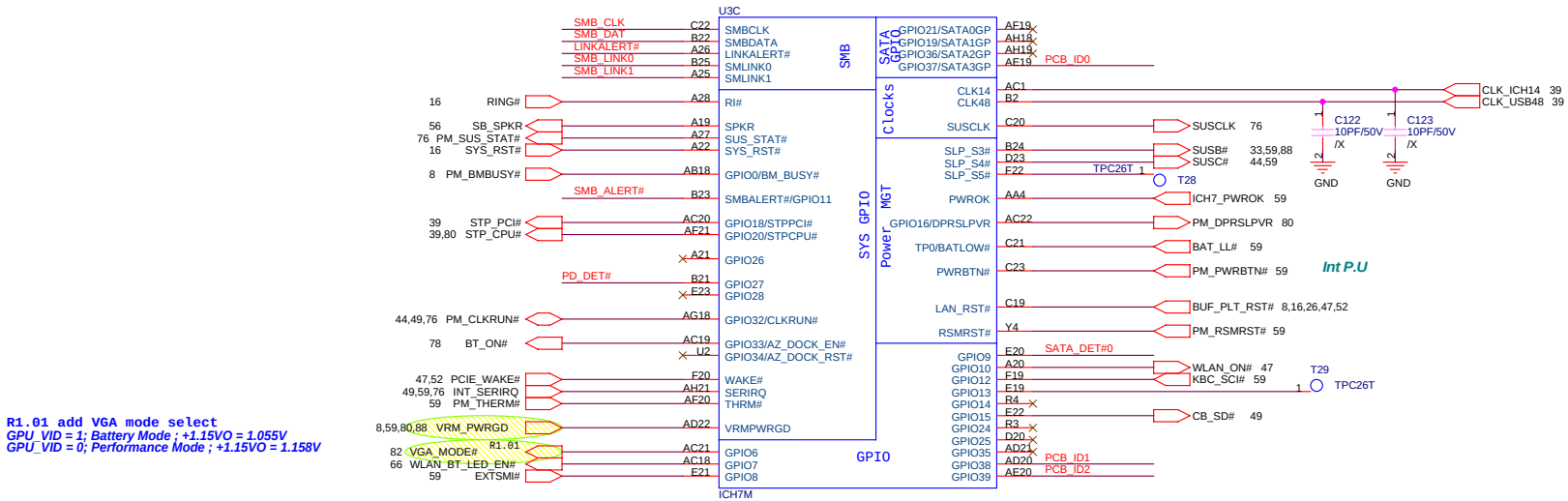
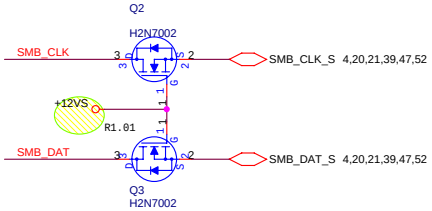
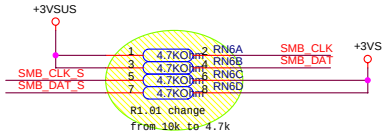
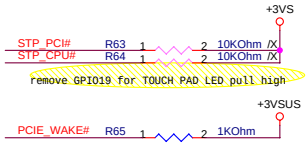
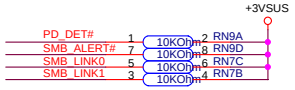


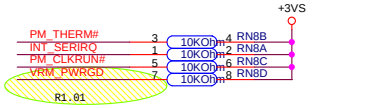
R1.01 add VGA mode select
GPU_VID = 1; Battery Mode ; +1.15VO = 1.055V
GPU_VID = 0; Performance Mode ; +1.15VO = 1.158V

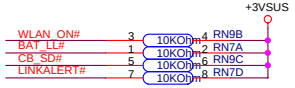


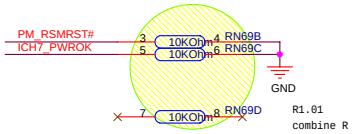


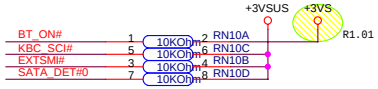


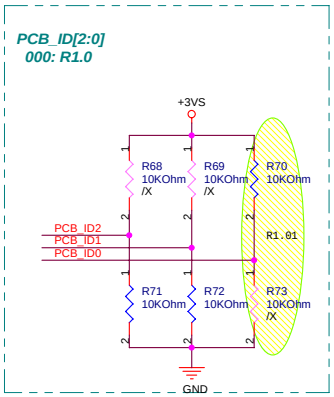




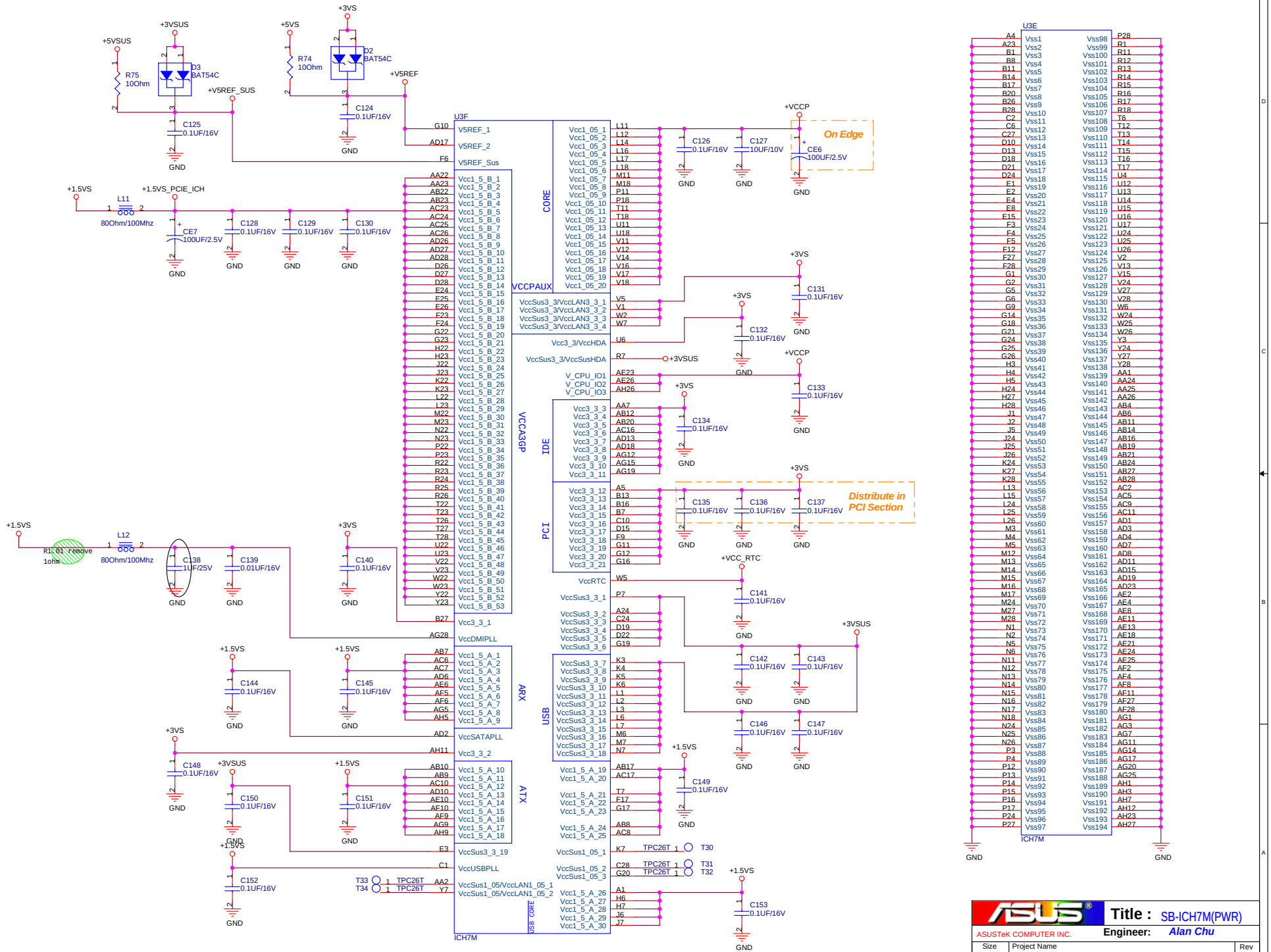








ASUSTeK COMPUTER INC	Title : SB-ICH7M(3)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96J		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 17 of 92		


+3VSUS
+5VSUS
R75
10Ohm
D3
BAT54C
+5VS
R74
10Ohm
D2
BAT54C
+3VS
+5VREF
+V5REF_SUS
C124
0.1UF/16V
C125
0.1UF/16V
GND
U3F
G10
V5REF_1
AD17
V5REF_2
F6
V5REF_Sus
+1.5VS
+1.5VS_PCIE_ICH
L11
80Ohm/100Mhz
CE7
100UF/2.5V
C128
0.1UF/16V
C129
0.1UF/16V
C130
0.1UF/16V
AA22
AA23
AB22
AB23
AC23
AC24
AC25
AC26
AD26
AD27
AD28
D26
D27
D28
E24
E25
E26
F23
F24
G22
G23
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J22
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P23
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R26
T22
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T26
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T28
U22
U23
V22
V23
W22
W23
Y22
Y23
Vcc1_5_B_1
Vcc1_5_B_2
Vcc1_5_B_3
Vcc1_5_B_4
Vcc1_5_B_5
Vcc1_5_B_6
Vcc1_5_B_7
Vcc1_5_B_8
Vcc1_5_B_9
Vcc1_5_B_10
Vcc1_5_B_11
Vcc1_5_B_12
Vcc1_5_B_13
Vcc1_5_B_14
Vcc1_5_B_15
Vcc1_5_B_16
Vcc1_5_B_17
Vcc1_5_B_18
Vcc1_5_B_19
Vcc1_5_B_20
Vcc1_5_B_21
Vcc1_5_B_22
Vcc1_5_B_23
Vcc1_5_B_24
Vcc1_5_B_25
Vcc1_5_B_26
Vcc1_5_B_27
Vcc1_5_B_28
Vcc1_5_B_29
Vcc1_5_B_30
Vcc1_5_B_31
Vcc1_5_B_32
Vcc1_5_B_33
Vcc1_5_B_34
Vcc1_5_B_35
Vcc1_5_B_36
Vcc1_5_B_37
Vcc1_5_B_38
Vcc1_5_B_39
Vcc1_5_B_40
Vcc1_5_B_41
Vcc1_5_B_42
Vcc1_5_B_43
Vcc1_5_B_44
Vcc1_5_B_45
Vcc1_5_B_46
Vcc1_5_B_47
Vcc1_5_B_48
Vcc1_5_B_49
Vcc1_5_B_50
Vcc1_5_B_51
Vcc1_5_B_52
Vcc1_5_B_53
CORE
B27
Vcc3_3_1
AG28
VccDMIPLL
+1.5VS
L12
R1_01 remove
1ohm
80Ohm/100Mhz
C138
1UF/25V
C139
0.01UF/16V
C140
0.1UF/16V
AB7
AC6
AC7
AD6
AE6
AE5
AF6
AG5
AH5
Vcc1_5_A_1
Vcc1_5_A_2
Vcc1_5_A_3
Vcc1_5_A_4
Vcc1_5_A_5
Vcc1_5_A_6
Vcc1_5_A_7
Vcc1_5_A_8
Vcc1_5_A_9
ARX
C144
0.1UF/16V
C145
0.1UF/16V
AD2
VccSATAPLL
AH11
Vcc3_3_2
C148
0.1UF/16V
C150
0.1UF/16V
C151
0.1UF/16V
AB10
AB9
AC10
AD10
AE10
AE10
AF9
AG9
AH9
Vcc1_5_A_10
Vcc1_5_A_11
Vcc1_5_A_12
Vcc1_5_A_13
Vcc1_5_A_14
Vcc1_5_A_15
Vcc1_5_A_16
Vcc1_5_A_17
Vcc1_5_A_18
ATX
E3
VccSus3_3_19
C1
VccUSBPLL
C152
0.1UF/16V
T33
T34
TPC26T
AA2
Y7
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
USB CORE
ICH7M
VCCPAUX
L11
L12
L14
L16
L17
L18
M11
M18
P11
P18
T11
T18
U11
U18
V11
V12
V14
V16
V17
V18
Vcc1_05_1
Vcc1_05_2
Vcc1_05_3
Vcc1_05_4
Vcc1_05_5
Vcc1_05_6
Vcc1_05_7
Vcc1_05_8
Vcc1_05_9
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Vcc1_05_13
Vcc1_05_14
Vcc1_05_15
Vcc1_05_16
Vcc1_05_17
Vcc1_05_18
Vcc1_05_19
Vcc1_05_20
C126
0.1UF/16V
C127
10UF/10V
+VCCP
On Edge
CE6
100UF/2.5V
V5
V1
W2
W7
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
U6
Vcc3_3/VccHDA
R7
VccSus3_3/VccSusHDA
+3VSUS
C131
0.1UF/16V
C132
0.1UF/16V
AE23
AE26
AH26
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
C133
0.1UF/16V
VCC3GP
IDE
AA7
AB12
AB20
AC16
AD13
AD18
AG12
AG15
AG19
Vcc3_3_3
Vcc3_3_4
Vcc3_3_5
Vcc3_3_6
Vcc3_3_7
Vcc3_3_8
Vcc3_3_9
Vcc3_3_10
Vcc3_3_11
C134
0.1UF/16V
PCI
A5
B13
B16
B7
C10
D15
F9
G11
G12
G16
Vcc3_3_12
Vcc3_3_13
Vcc3_3_14
Vcc3_3_15
Vcc3_3_16
Vcc3_3_17
Vcc3_3_18
Vcc3_3_19
Vcc3_3_20
Vcc3_3_21
C135
0.1UF/16V
C136
0.1UF/16V
C137
0.1UF/16V
Distribute in
PCI Section
W5
VccRTC
+VCC_RTC
C141
0.1UF/16V
P7
VccSus3_3_1
A24
C24
D19
D22
G19
VccSus3_3_2
VccSus3_3_3
VccSus3_3_4
VccSus3_3_5
VccSus3_3_6
C142
0.1UF/16V
C143
0.1UF/16V
K3
K4
K5
K6
L1
L2
L3
L6
L7
M6
M7
N7
VccSus3_3_7
VccSus3_3_8
VccSus3_3_9
VccSus3_3_10
VccSus3_3_11
VccSus3_3_12
VccSus3_3_13
VccSus3_3_14
VccSus3_3_15
VccSus3_3_16
VccSus3_3_17
VccSus3_3_18
USB
C146
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C147
0.1UF/16V
AB17
AC17
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F17
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AC8
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Vcc1_5_A_23
Vcc1_5_A_24
Vcc1_5_A_25
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VccSus1_05_2
VccSus1_05_3
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T31
T32
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H7
J6
J7
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Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
C153
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U3E
A4
A23
B1
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W26
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AA25
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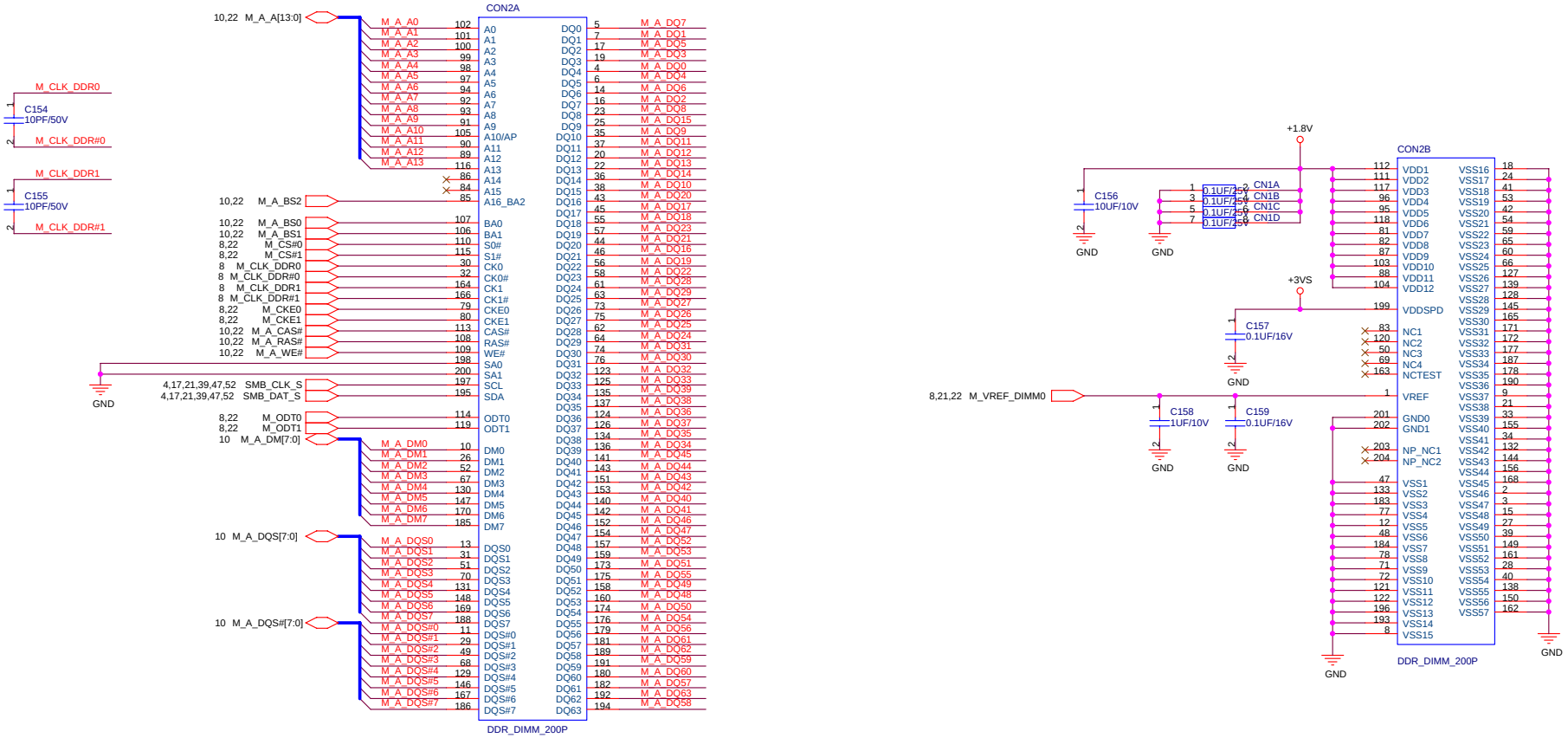
AF27
AF28
AG1
AG3
AG7
AG11
AG14
AG17
AG20
AG25
AH1
AH3
AH7
AH12
AH23
AH27
ICH7M
Title : SB-ICH7M(PWR)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size
Custom
Project Name
Z96J
Rev
1.0
Date: Tuesday, January 10, 2006
Sheet 18 of 92

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 19 of 92

M_A_DQ[63:0] 10

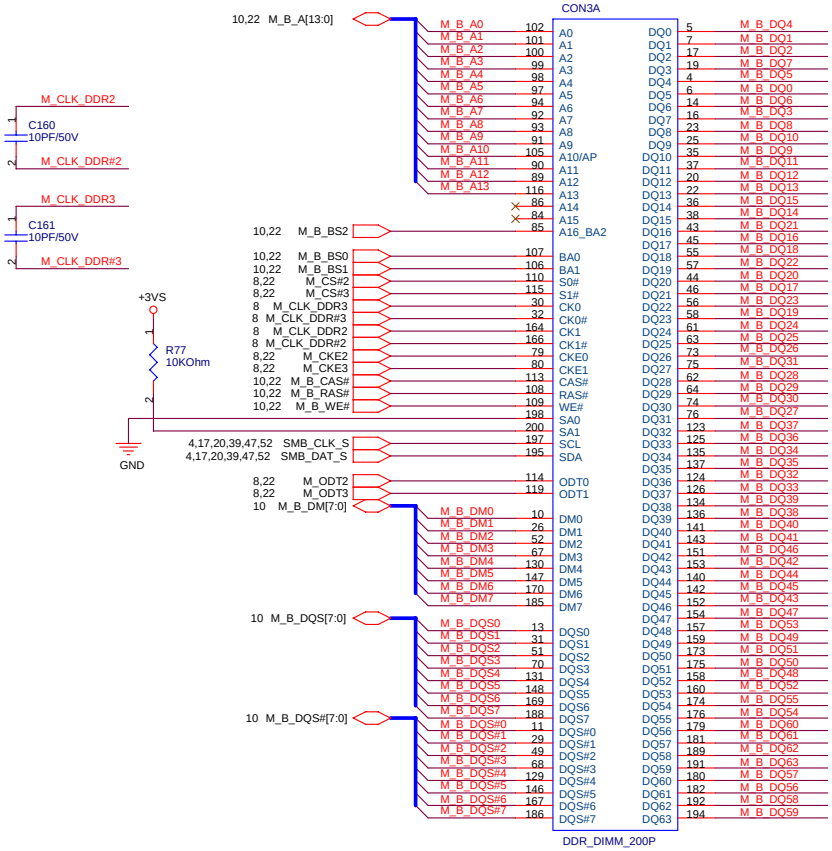
REV Type

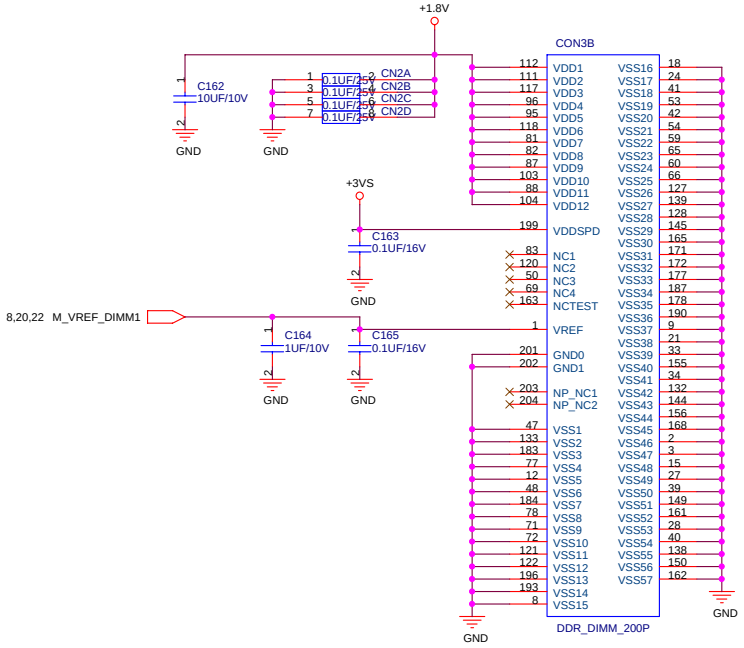


ASUSTeK COMPUTER INC.	Title : DDR2 SO-DIMM0	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 20 of 92	

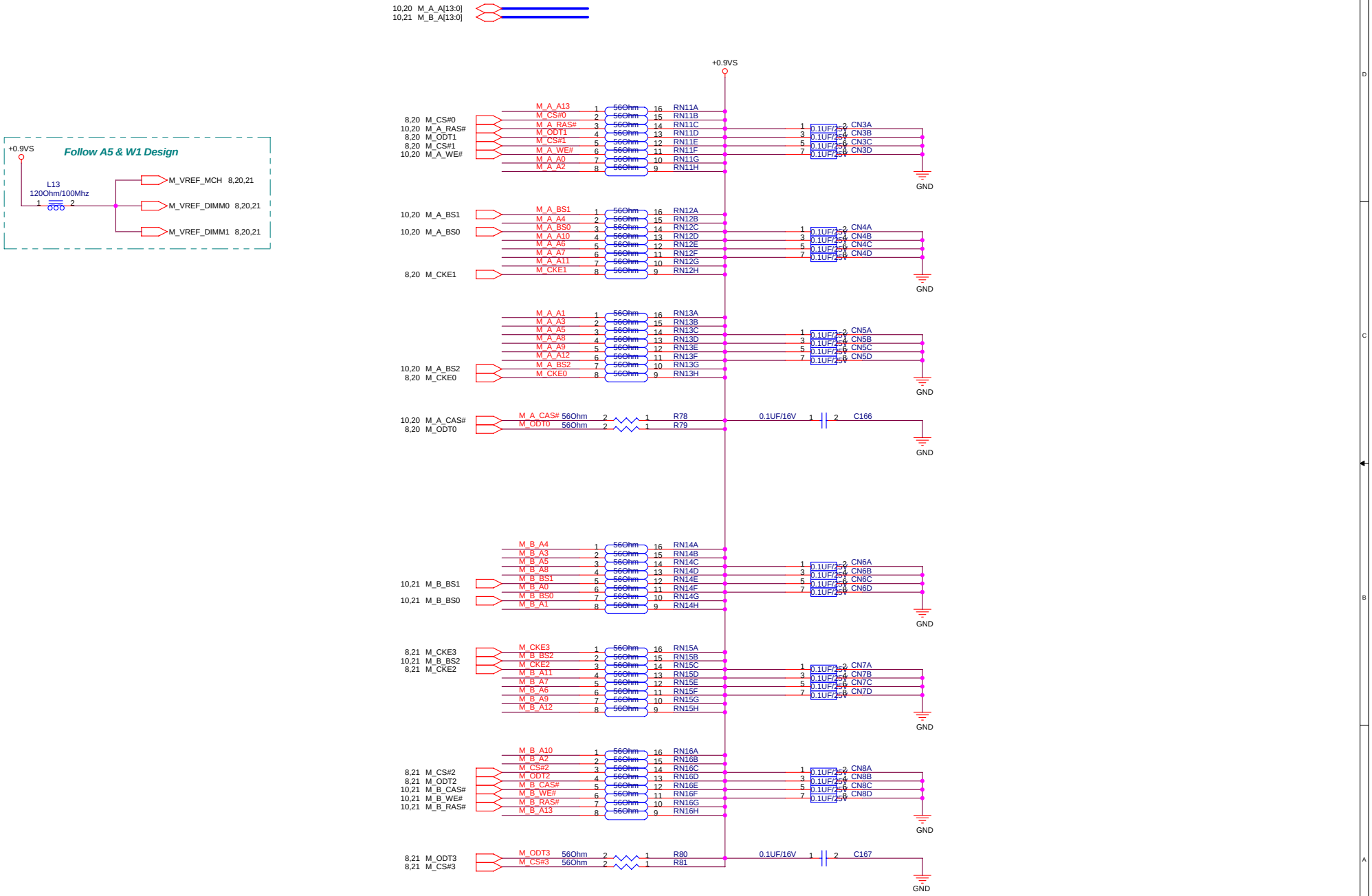
M_B_DQ[63:0] 10

STD Type





ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96J		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 21 of 92		



ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 22 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 23 of 92

GPIO[0]: Tx Power Savings Enable
0: 50% Tx output swing
1: full Tx output swing (recommended)
(default 0, internal pull-down)

GPIO[1]: Tx De-emphasis Enable
0: Tx de-emphasis disbale
1: Tx de-emphasis enable
(default 0, internal pull-down)

MID / Vendor /SIZE	3	2	1	0
Samsung 128M	0	0	0	0
Samsung 256M	0	0	0	1
Hynix 128M	0	0	1	0
Hynix 256M	0	0	1	1
Infineon 128M	0	1	0	0
Infineon 256M	0	1	0	1
	0	1	1	0
	0	1	1	1

R1.01 add thermal detect from EC

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800
PANEL ID0 RESERVE FOR VENDOR

GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01

Spread Spectrum

Down Spread Spectrum for EMI Attenuation

	0	/ 1	/ NC.
P1819B :	-1.25	-1.75	x.
MK1726 :	-1.8	-2.5	-0.6.

PWR_CTRL: HIGH(1.0V) / LOW(1.08V)
PULL DOWN IF USED FOR POWER PLAY

1.65V VREF Divider close to M56

U5B — PART 2 OF 7 — VIDEO & MULTIMEDIA — M56_P

Can be left unconnect if not used.
Can be unconnect if not used.

remove DVI

ADM1032ARMZ-2

YAGEO/RC0603FR-07121RL <G>

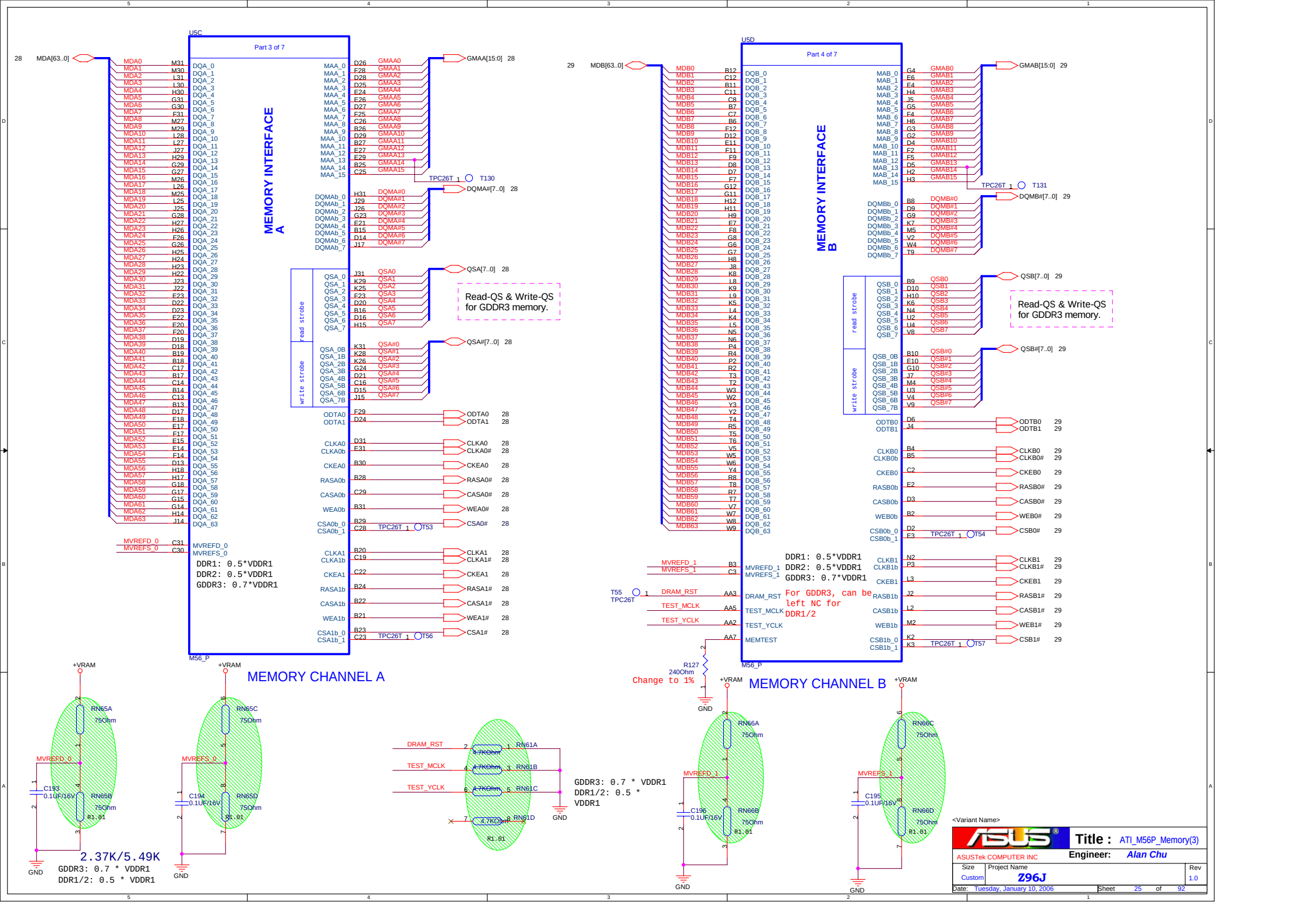
YAGEO/RC0402FR-07499RL <G>

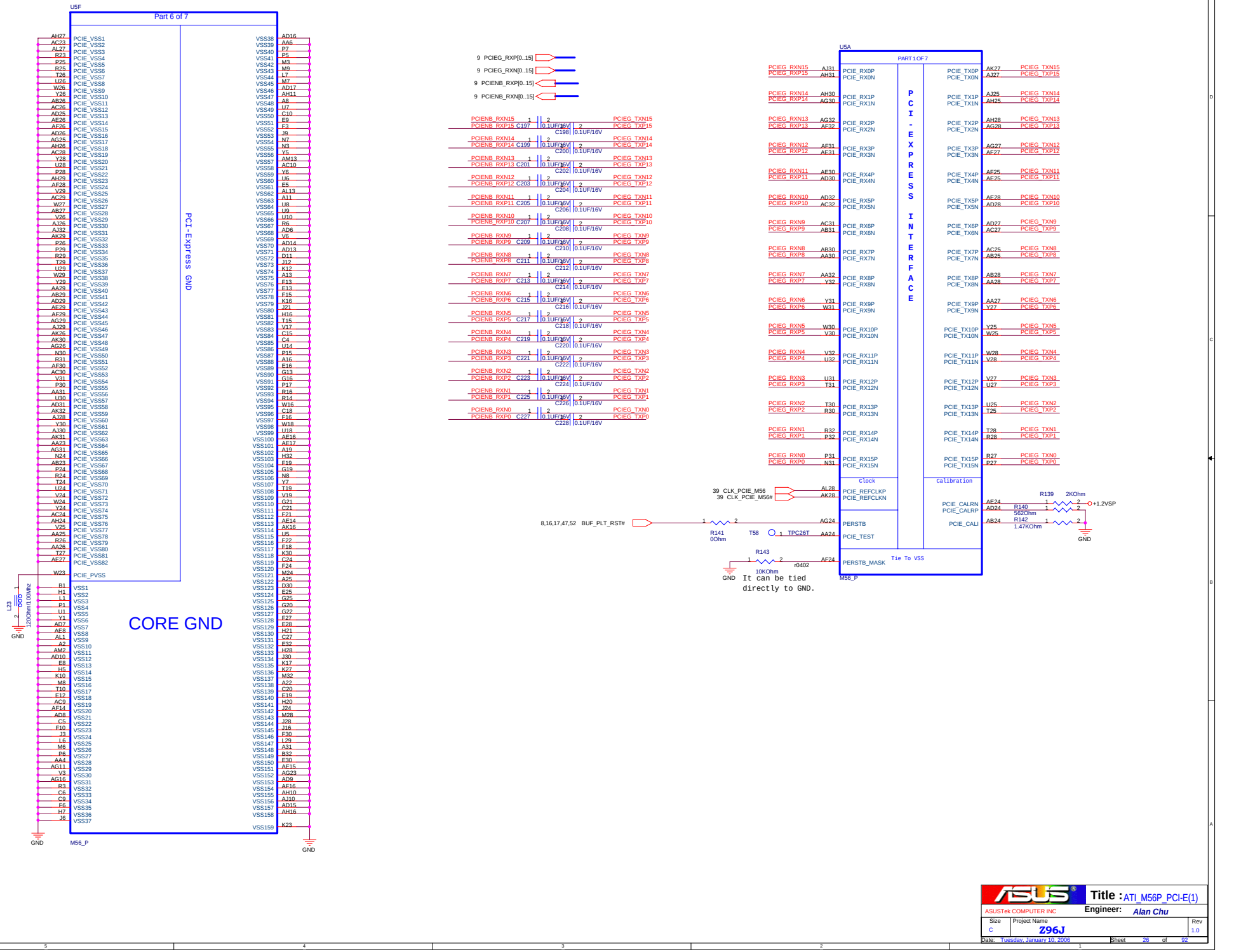
ASUSTek COMPUTER INC
Engineer: Alan Chu

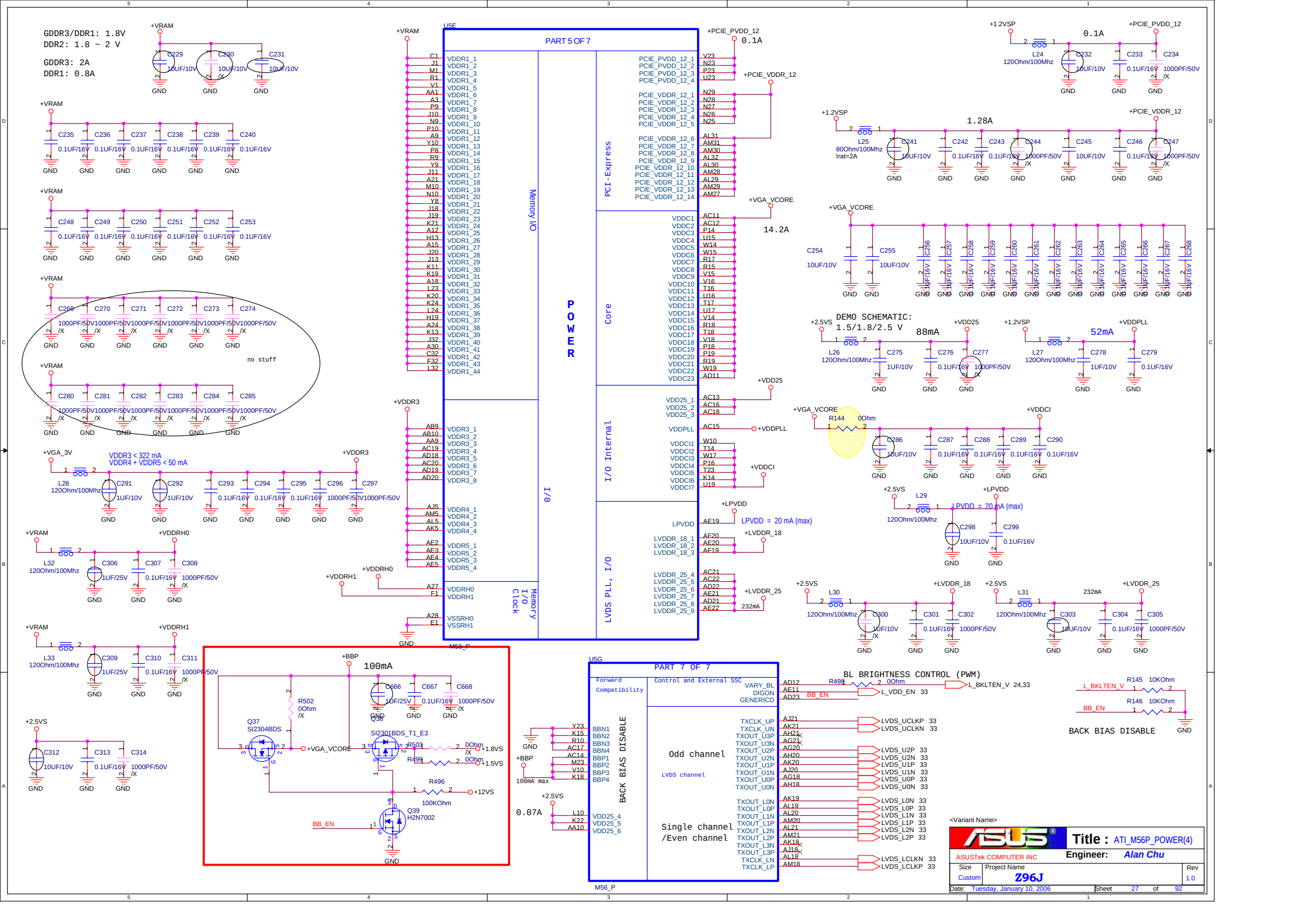
Title : ATI_M56P_MAIN(2)

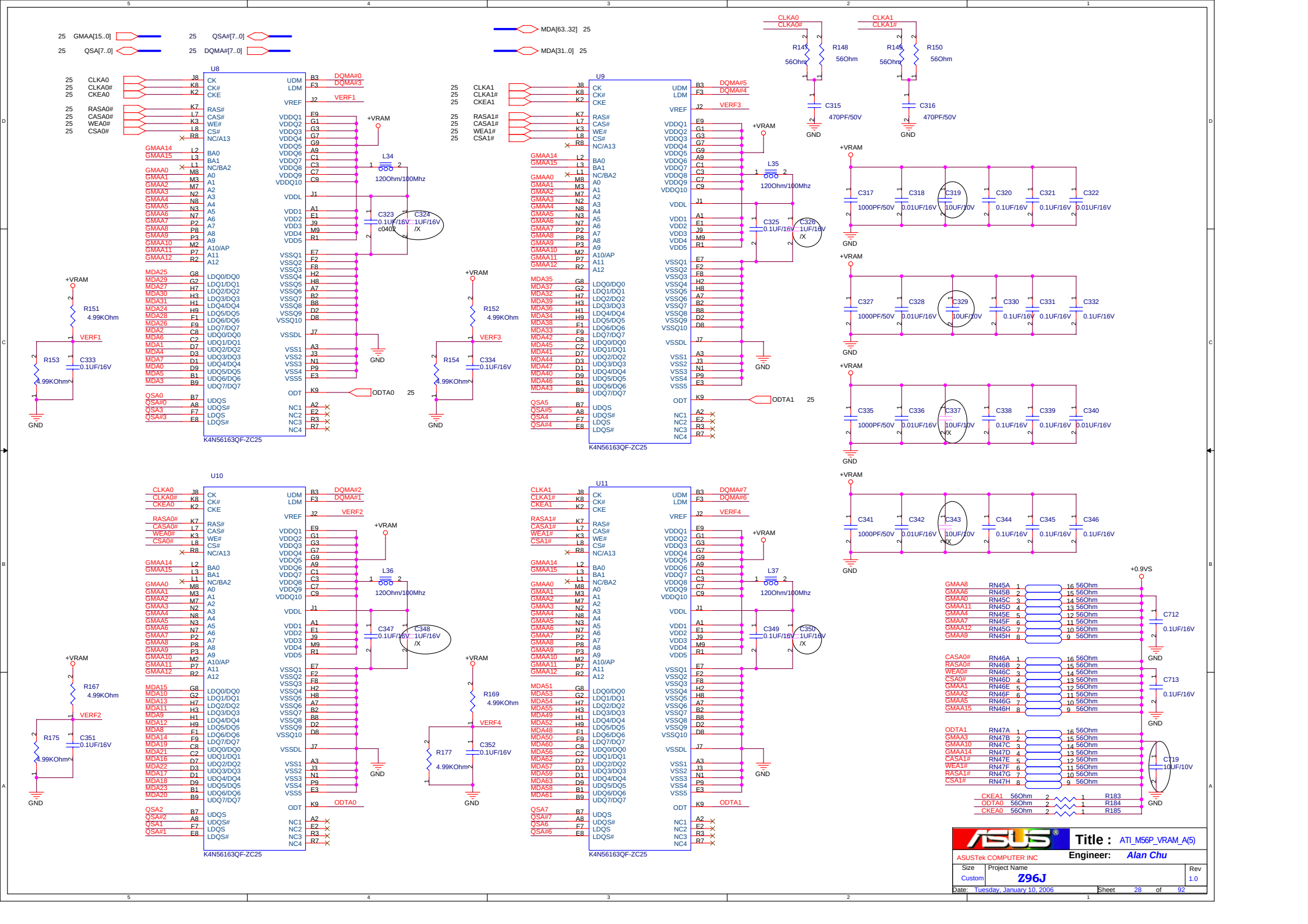
Size	Project Name	Rev
Custom	Z96J	1.0

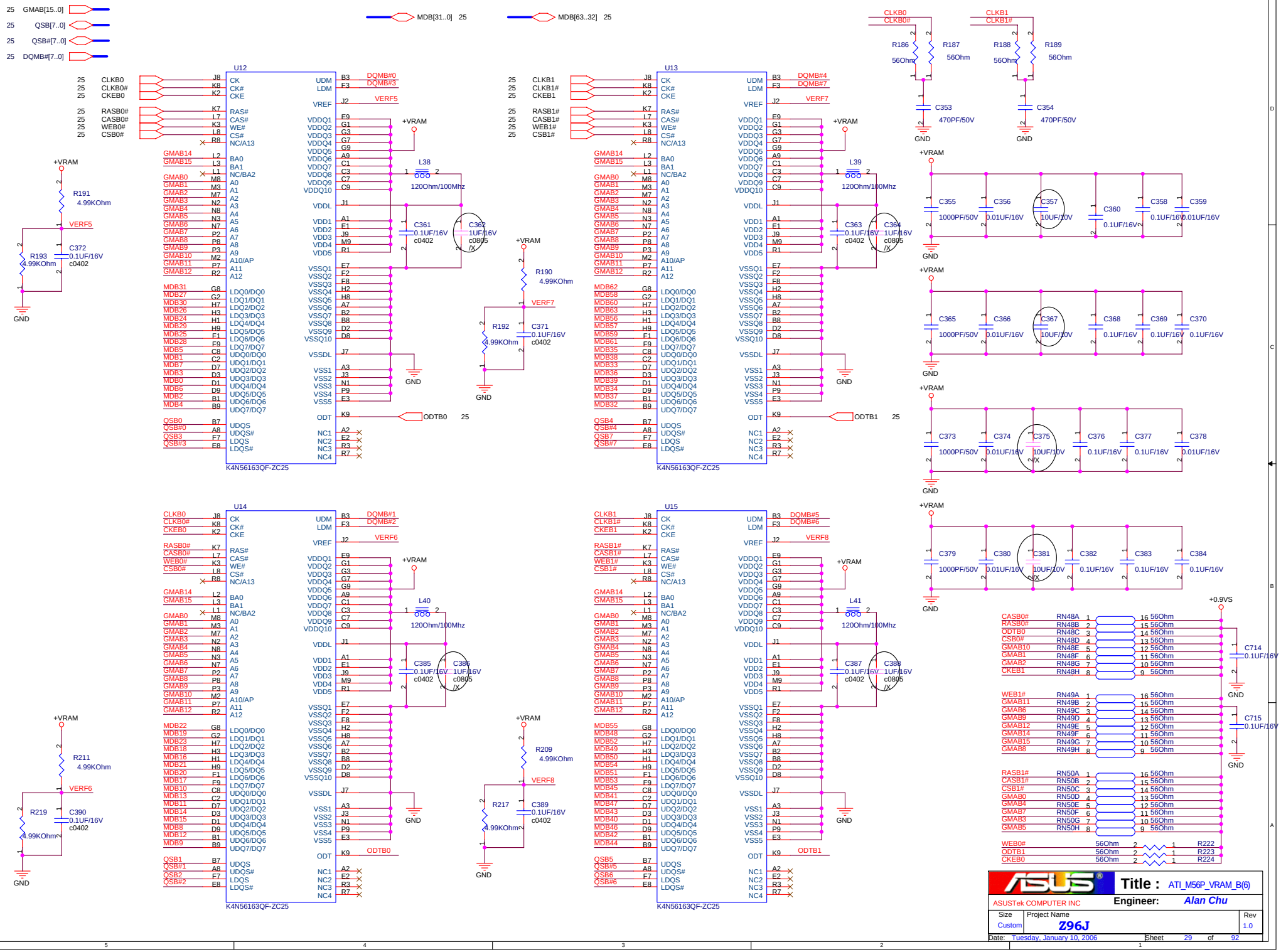
Date: Tuesday, January 10, 2006 Sheet 24 of 92

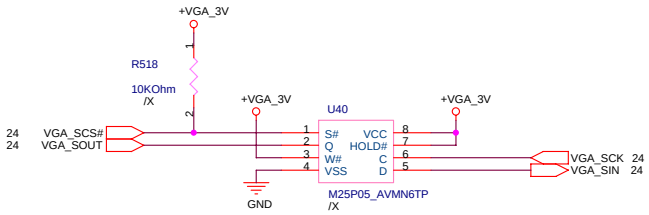

U5C
Part 3 of 7
MEMORY INTERFACE A
28 MDA[63..0]
MDA0 M31
MDA1 M30
MDA2 L31
MDA3 L30
MDA4 H30
MDA5 G31
MDA6 G30
MDA7 F31
MDA8 M27
MDA9 M29
MDA10 L28
MDA11 L27
MDA12 J27
MDA13 H29
MDA14 G29
MDA15 G27
MDA16 M26
MDA17 L26
MDA18 M25
MDA19 L25
MDA20 J25
MDA21 G28
MDA22 H27
MDA23 H26
MDA24 F26
MDA25 G26
MDA26 H25
MDA27 H24
MDA28 H23
MDA29 H22
MDA30 J23
MDA31 J22
MDA32 F23
MDA33 D22
MDA34 D23
MDA35 F22
MDA36 E20
MDA37 F20
MDA38 D19
MDA39 D18
MDA40 B19
MDA41 B18
MDA42 C17
MDA43 B17
MDA44 C14
MDA45 B14
MDA46 C13
MDA47 B13
MDA48 D17
MDA49 E18
MDA50 E17
MDA51 F17
MDA52 E15
MDA53 E14
MDA54 F14
MDA55 D13
MDA56 H18
MDA57 H17
MDA58 G18
MDA59 G17
MDA60 G15
MDA61 G14
MDA62 H14
MDA63 J14
DQA_0 DQA_1 DQA_2 DQA_3 DQA_4 DQA_5 DQA_6 DQA_7 DQA_8 DQA_9 DQA_10 DQA_11 DQA_12 DQA_13 DQA_14 DQA_15 DQA_16 DQA_17 DQA_18 DQA_19 DQA_20 DQA_21 DQA_22 DQA_23 DQA_24 DQA_25 DQA_26 DQA_27 DQA_28 DQA_29 DQA_30 DQA_31 DQA_32 DQA_33 DQA_34 DQA_35 DQA_36 DQA_37 DQA_38 DQA_39 DQA_40 DQA_41 DQA_42 DQA_43 DQA_44 DQA_45 DQA_46 DQA_47 DQA_48 DQA_49 DQA_50 DQA_51 DQA_52 DQA_53 DQA_54 DQA_55 DQA_56 DQA_57 DQA_58 DQA_59 DQA_60 DQA_61 DQA_62 DQA_63
MVREFD_0 C31
MVREFS_0 C30
MVREFD_0
MVREFS_0
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
MAA_0 MAA_1 MAA_2 MAA_3 MAA_4 MAA_5 MAA_6 MAA_7 MAA_8 MAA_9 MAA_10 MAA_11 MAA_12 MAA_13 MAA_14 MAA_15
D26 GMAA0
F28 GMAA1
D28 GMAA2
D25 GMAA3
E24 GMAA4
E26 GMAA5
D27 GMAA6
F25 GMAA7
C26 GMAA8
B26 GMAA9
D29 GMAA10
B27 GMAA11
E27 GMAA12
E29 GMAA13
B25 GMAA14
C25 GMAA15
GMAA[15:0] 28
TPC26T 1 T130
DQMAb_0 DQMAb_1 DQMAb_2 DQMAb_3 DQMAb_4 DQMAb_5 DQMAb_6 DQMAb_7
H31 DQMA#0
J29 DQMA#1
J26 DQMA#2
G23 DQMA#3
F21 DQMA#4
B15 DQMA#5
D14 DQMA#6
J17 DQMA#7
DQMA#[7..0] 28
read strobe
write strobe
QSA_0 QSA_1 QSA_2 QSA_3 QSA_4 QSA_5 QSA_6 QSA_7
J31 QSA0
K29 QSA1
K25 QSA2
F23 QSA3
D20 QSA4
B16 QSA5
D16 QSA6
H15 QSA7
QSA[7..0] 28
Read-QS & Write-QS for GDDR3 memory.
QSA_0B QSA_1B QSA_2B QSA_3B QSA_4B QSA_5B QSA_6B QSA_7B
K31 QSA#0
K28 QSA#1
K26 QSA#2
G24 QSA#3
D21 QSA#4
C16 QSA#5
D15 QSA#6
J15 QSA#7
QSA#[7..0] 28
ODTA0 ODTA1
F29 ODTA0
D24 ODTA1
ODTA0 28
ODTA1 28
CLKA0 CLKA0b
D31 CLKA0
E31 CLKA0#
CLKA0 28
CLKA0# 28
CKEA0 B30 CKEA0 28
RASA0b B28 RASA0# 28
CASA0b C29 CASA0# 28
WEA0b B31 WEA0# 28
CSA0b_0 CSA0b_1
B29 C28 TPC26T 1 T53
CSA0# 28
CLKA1 CLKA1b
B20 CLKA1
C19 CLKA1#
CLKA1 28
CLKA1# 28
CKEA1 C22 CKEA1 28
RASA1b B24 RASA1# 28
CASA1b B22 CASA1# 28
WEA1b B21 WEA1# 28
CSA1b_0 CSA1b_1
B23 C23 TPC26T 1 T56
CSA1# 28
M56_P
MEMORY CHANNEL A
U5D
Part 4 of 7
MEMORY INTERFACE B
29 MDB[63..0]
MDB0 B12
MDB1 C12
MDB2 B11
MDB3 C11
MDB4 C8
MDB5 B7
MDB6 C7
MDB7 B6
MDB8 E12
MDB9 D12
MDB10 E11
MDB11 F11
MDB12 F9
MDB13 D8
MDB14 D7
MDB15 E7
MDB16 G12
MDB17 G11
MDB18 H12
MDB19 H11
MDB20 H9
MDB21 E7
MDB22 F8
MDB23 G8
MDB24 G6
MDB25 G7
MDB26 H8
MDB27 J8
MDB28 K8
MDB29 L8
MDB30 K9
MDB31 L9
MDB32 K5
MDB33 L4
MDB34 K4
MDB35 L5
MDB36 N5
MDB37 N6
MDB38 P4
MDB39 R4
MDB40 P2
MDB41 R2
MDB42 T3
MDB43 T2
MDB44 W3
MDB45 W2
MDB46 Y3
MDB47 Y2
MDB48 T4
MDB49 R5
MDB50 T5
MDB51 T6
MDB52 V5
MDB53 W5
MDB54 W6
MDB55 Y4
MDB56 R8
MDB57 T8
MDB58 R7
MDB59 T7
MDB60 V7
MDB61 W7
MDB62 W8
MDB63 W9
DQB_0 DQB_1 DQB_2 DQB_3 DQB_4 DQB_5 DQB_6 DQB_7 DQB_8 DQB_9 DQB_10 DQB_11 DQB_12 DQB_13 DQB_14 DQB_15 DQB_16 DQB_17 DQB_18 DQB_19 DQB_20 DQB_21 DQB_22 DQB_23 DQB_24 DQB_25 DQB_26 DQB_27 DQB_28 DQB_29 DQB_30 DQB_31 DQB_32 DQB_33 DQB_34 DQB_35 DQB_36 DQB_37 DQB_38 DQB_39 DQB_40 DQB_41 DQB_42 DQB_43 DQB_44 DQB_45 DQB_46 DQB_47 DQB_48 DQB_49 DQB_50 DQB_51 DQB_52 DQB_53 DQB_54 DQB_55 DQB_56 DQB_57 DQB_58 DQB_59 DQB_60 DQB_61 DQB_62 DQB_63
MVREFD_1 B3
MVREFS_1 C3
T55 TPC26T 1
DRAM_RST AA3
TEST_MCLK AA5
TEST_YCLK AA2
MEMTEST AA7
MVREFD_1
MVREFS_1
DRAM_RST
TEST_MCLK
TEST_YCLK
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
For GDDR3, can be left NC for DDR1/2
MAB_0 MAB_1 MAB_2 MAB_3 MAB_4 MAB_5 MAB_6 MAB_7 MAB_8 MAB_9 MAB_10 MAB_11 MAB_12 MAB_13 MAB_14 MAB_15
G4 GMAB0
E6 GMAB1
E4 GMAB2
H4 GMAB3
J5 GMAB4
G5 GMAB5
F4 GMAB6
H6 GMAB7
G3 GMAB8
G2 GMAB9
D4 GMAB10
F2 GMAB11
F5 GMAB12
D5 GMAB13
H2 GMAB14
H3 GMAB15
GMAB[15:0] 29
TPC26T 1 T131
DQMBb_0 DQMBb_1 DQMBb_2 DQMBb_3 DQMBb_4 DQMBb_5 DQMBb_6 DQMBb_7
B8 DQMB#0
D9 DQMB#1
G9 DQMB#2
K7 DQMB#3
M5 DQMB#4
V2 DQMB#5
W4 DQMB#6
T9 DQMB#7
DQMB#[7..0] 29
read strobe
write strobe
QSB_0 QSB_1 QSB_2 QSB_3 QSB_4 QSB_5 QSB_6 QSB_7
B9 QSB0
D10 QSB1
H10 QSB2
K6 QSB3
N4 QSB4
U2 QSB5
U4 QSB6
V8 QSB7
QSB[7..0] 29
Read-QS & Write-QS for GDDR3 memory.
QSB_0B QSB_1B QSB_2B QSB_3B QSB_4B QSB_5B QSB_6B QSB_7B
B10 QSB#0
E10 QSB#1
G10 QSB#2
J7 QSB#3
M4 QSB#4
U3 QSB#5
V4 QSB#6
V9 QSB#7
QSB#[7..0] 29
ODTB0 ODTB1
D6 ODTB0
J4 ODTB1
ODTB0 29
ODTB1 29
CLKB0 CLKB0b
B4 CLKB0
B5 CLKB0#
CLKB0 29
CLKB0# 29
CKEB0 C2 CKEB0 29
RASB0b E2 RASB0# 29
CASB0b D3 CASB0# 29
WEB0b B2 WEB0# 29
CSB0b_0 CSB0b_1
D2 E3 TPC26T 1 T54
CSB0# 29
CLKB1 CLKB1b
N2 CLKB1
P3 CLKB1#
CLKB1 29
CLKB1# 29
CKEB1 L3 CKEB1 29
RASB1b J2 RASB1# 29
CASB1b L2 CASB1# 29
WEB1b M2 WEB1# 29
CSB1b_0 CSB1b_1
K2 K3 TPC26T 1 T57
CSB1# 29
M56_P
MEMORY CHANNEL B
+VRAM
RN65A 75Ohm
MVREFD_0
C193 0.1UF/16V
RN65B 75Ohm
R1.01
2.37K/5.49K
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
GND
RN65C 75Ohm
MVREFS_0
C194 0.1UF/16V
RN65D 75Ohm
R1.01
GND
DRAM_RST
TEST_MCLK
TEST_YCLK
RN61A 4.7KOhm
RN61B 4.7KOhm
RN61C 4.7KOhm
RN61D 4.7KOhm
R1.01
GND
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
R127 240Ohm
Change to 1%
GND
RN66A 75Ohm
MVREFD_1
C196 0.1UF/16V
RN66B 75Ohm
R1.01
GND
RN66C 75Ohm
MVREFS_1
C195 0.1UF/16V
RN66D 75Ohm
R1.01
GND
<Variant Name>
ASUSTek COMPUTER INC
Title : ATI_M56P_Memory(3)
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 25 of 92


U5F
Part 6 of 7
PCI-Express GND
CORE GND
M56_P
U5A
PART 1 OF 7
PCI-EXPRESS INTERFACE
Clock
Calibration
Tie To VSS
M56_P
It can be tied directly to GND.
Title : ATI_M56P_PCI-E(1)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size C
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 26 of 92


GDDR3/DDR1: 1.8V
DDR2: 1.8 ~ 2 V
GDDR3: 2A
DDR1: 0.8A
PART 5 OF 7
POWER
Memory I/O
PCI-Express
Core
I/O Internal
LVDS PLL, I/O
Memory I/O Clock
0/I
no stuff
VDDR3 < 322 mA
VDDR4 + VDDR5 < 50 mA
LPVDD = 20 mA (max)
DEMO SCHEMATIC:
1.5/1.8/2.5 V
PART 7 OF 7
BACK BIAS DISABLE
Odd channel
Single channel
/Even channel
BL BRIGHTNESS CONTROL (PWM)
BACK BIAS DISABLE
Title : ATI_M56P_POWER(4)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Project Name Z96J
Size Custom
Rev 1.0
Sheet 27 of 92
Date: Tuesday, January 10, 2006

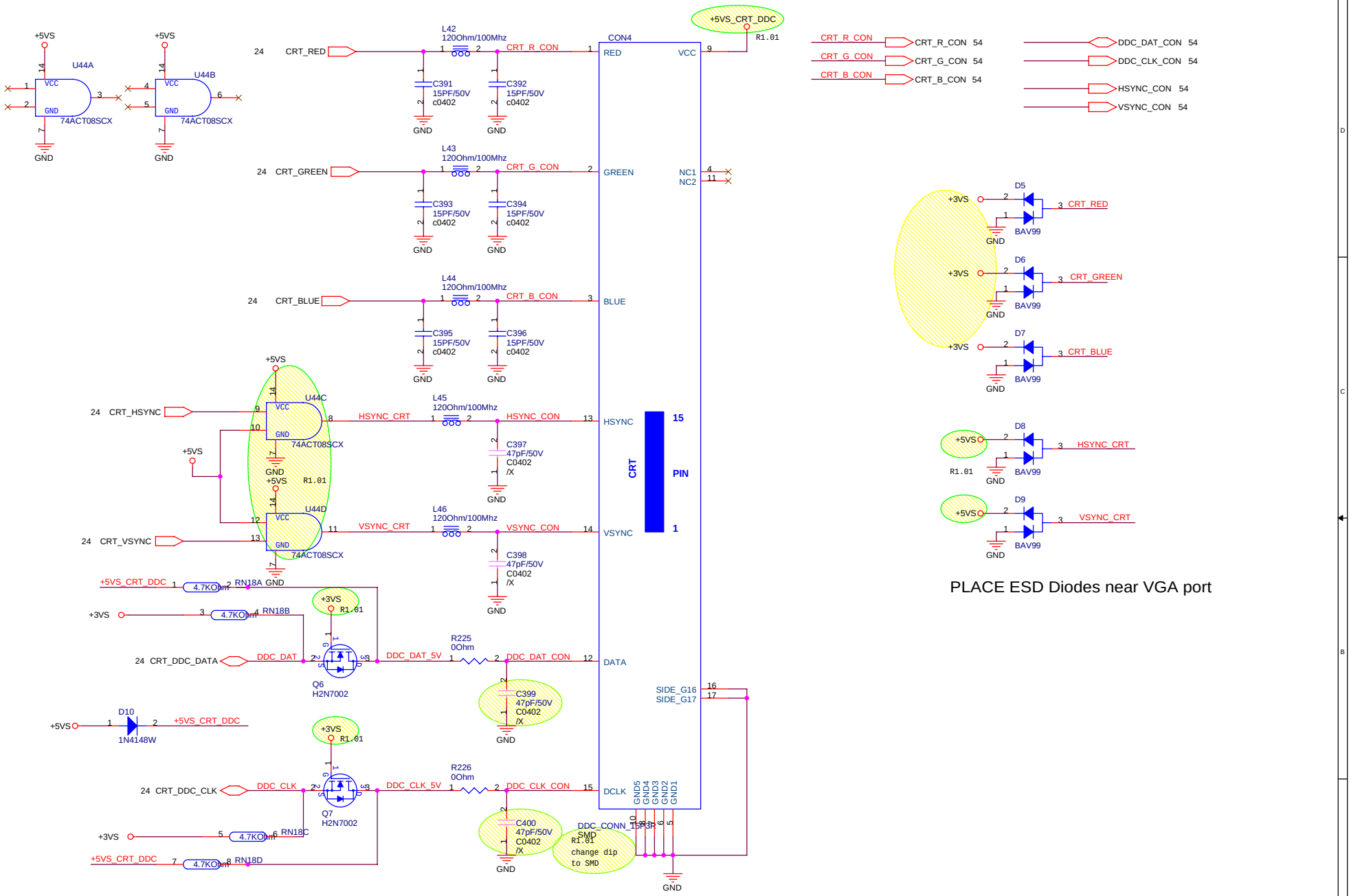

25 GMAA[15..0]
25 QSA[7..0]
25 QSA#[7..0]
25 DQMA#[7..0]
MDA[63..32] 25
MDA[31..0] 25
U8
U9
U10
U11
K4N56163QF-ZC25
+VRAM
GND
+0.9VS
L34
L35
L36
L37
120Ohm/100Mhz
VERF1
VERF2
VERF3
VERF4
VERF5
VERF6
VERF7
VERF8
ODTA0
ODTA1
R151 4.99KOhm
R152 4.99KOhm
R153 4.99KOhm
R154 4.99KOhm
R167 4.99KOhm
R169 4.99KOhm
R175 4.99KOhm
R177 4.99KOhm
C323 0.1UF/16V c0402
C324 1UF/16V /X
C325 0.1UF/16V
C326 1UF/16V /X
C333 0.1UF/16V
C334 0.1UF/16V
C347 0.1UF/16V
C348 1UF/16V /X
C349 0.1UF/16V
C350 1UF/16V /X
C351 0.1UF/16V
C352 0.1UF/16V
R141 56Ohm
R148 56Ohm
R149 56Ohm
R150 56Ohm
C315 470PF/50V
C316 470PF/50V
C317 1000PF/50V
C318 0.01UF/16V
C319 10UF/10V
C320 0.1UF/16V
C321 0.1UF/16V
C322 0.01UF/16V
C327 1000PF/50V
C328 0.01UF/16V
C329 10UF/10V
C330 0.1UF/16V
C331 0.1UF/16V
C332 0.1UF/16V
C335 1000PF/50V
C336 0.01UF/16V
C337 10UF/10V /X
C338 0.1UF/16V
C339 0.1UF/16V
C340 0.01UF/16V
C341 1000PF/50V
C342 0.01UF/16V
C343 10UF/10V /X
C344 0.1UF/16V
C345 0.1UF/16V
C346 0.1UF/16V
C712 0.1UF/16V
C713 0.1UF/16V
C719 10UF/10V
RN45A RN45B RN45C RN45D RN45E RN45F RN45G RN45H
RN46A RN46B RN46C RN46D RN46E RN46F RN46G RN46H
RN47A RN47B RN47C RN47D RN47E RN47F RN47G RN47H
56Ohm
R183 R184 R185
CKEA1 ODTA0 CKEA0
Title : ATI_M56P_VRAM_A(5)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 28 of 92


25 GMAB[15..0]
25 QSB[7..0]
25 QSB#[7..0]
25 DQMB#[7..0]
MDB[31..0] 25
MDB[63..32] 25
U12
U13
U14
U15
K4N56163QF-ZC25
+VRAM
GND
ODTB0 25
ODTB1 25
L38
L39
L40
L41
120Ohm/100Mhz
R191 4.99KOhm
R193 4.99KOhm
C372 0.1UF/16V c0402
R190 4.99KOhm
R192 4.99KOhm
C371 0.1UF/16V c0402
R211 4.99KOhm
R219 4.99KOhm
C390 0.1UF/16V c0402
R209 4.99KOhm
R217 4.99KOhm
C389 0.1UF/16V c0402
C361 0.1UF/16V c0402
C362 1UF/16V c0805 /X
C363 0.1UF/16V c0402
C364 1UF/16V c0805 /X
C385 0.1UF/16V c0402
C386 1UF/16V c0805 /X
C387 0.1UF/16V c0402
C388 1UF/16V c0805 /X
CLKB0 CLKB0#
CLKB1 CLKB1#
R186 56Ohm
R187 56Ohm
R188 56Ohm
R189 56Ohm
C353 470PF/50V
C354 470PF/50V
C355 1000PF/50V
C356 0.01UF/16V
C357 10UF/10V
C360 0.1UF/16V
C358 0.1UF/16V
C359 0.01UF/16V
C365 1000PF/50V
C366 0.01UF/16V
C367 10UF/10V
C368 0.1UF/16V
C369 0.1UF/16V
C370 0.1UF/16V
C373 1000PF/50V
C374 0.01UF/16V
C375 10UF/10V /X
C376 0.1UF/16V
C377 0.1UF/16V
C378 0.01UF/16V
C379 1000PF/50V
C380 0.01UF/16V
C381 10UF/10V /X
C382 0.1UF/16V
C383 0.1UF/16V
C384 0.1UF/16V
+0.9VS
C714 0.1UF/16V
C715 0.1UF/16V
RN48A RN48B RN48C RN48D RN48E RN48F RN48G RN48H 56Ohm
RN49A RN49B RN49C RN49D RN49E RN49F RN49G RN49H 56Ohm
RN50A RN50B RN50C RN50D RN50E RN50F RN50G RN50H 56Ohm
R222 R223 R224 56Ohm
Title : ATI_M56P_VRAM_B(6)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 29 of 92



ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 30 of 92	

Title :	
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 31 of 92



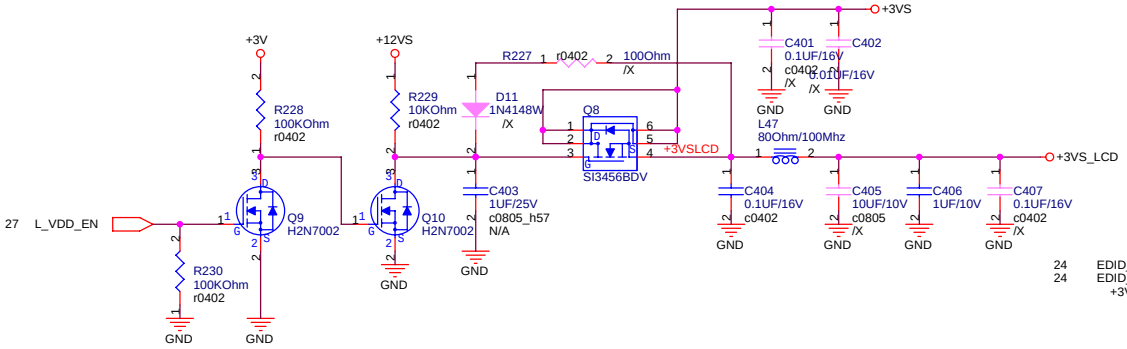
PLACE ESD Diodes near VGA port

ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 32 of 92	

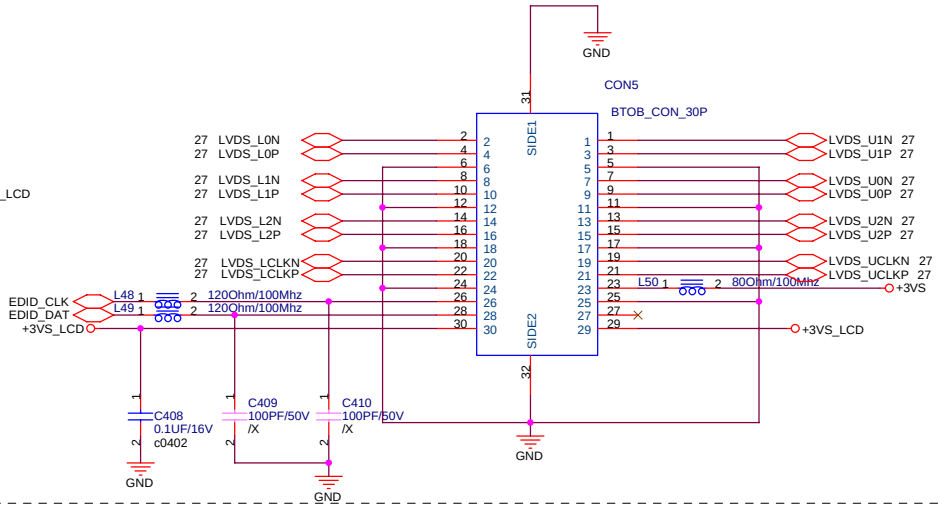
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power

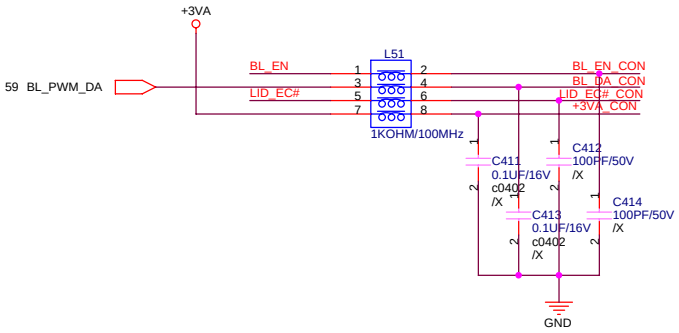


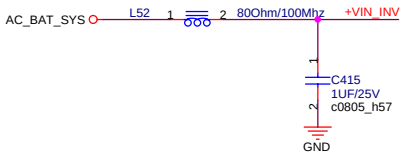
LCD LVDS Interface

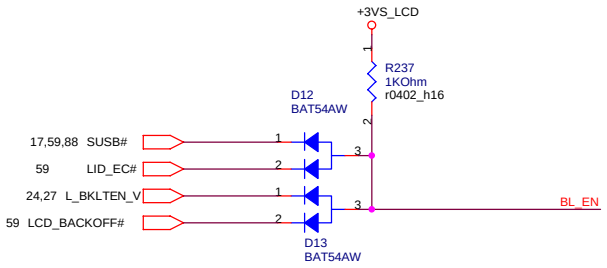


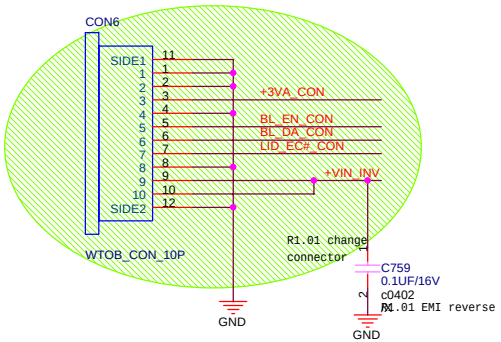
INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.







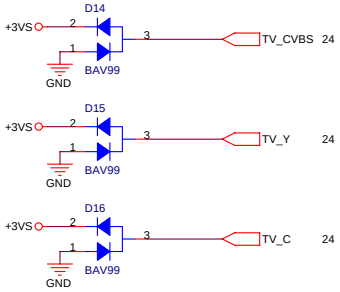


R1.01 remove HW reserve pannel ID

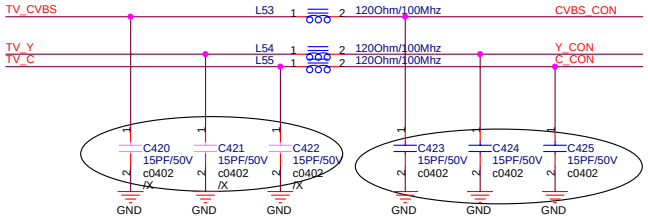
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 33 of 92	

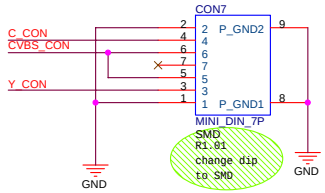
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 34 of 92

TV OUT



PLACE ESD
Diodes near
TV port

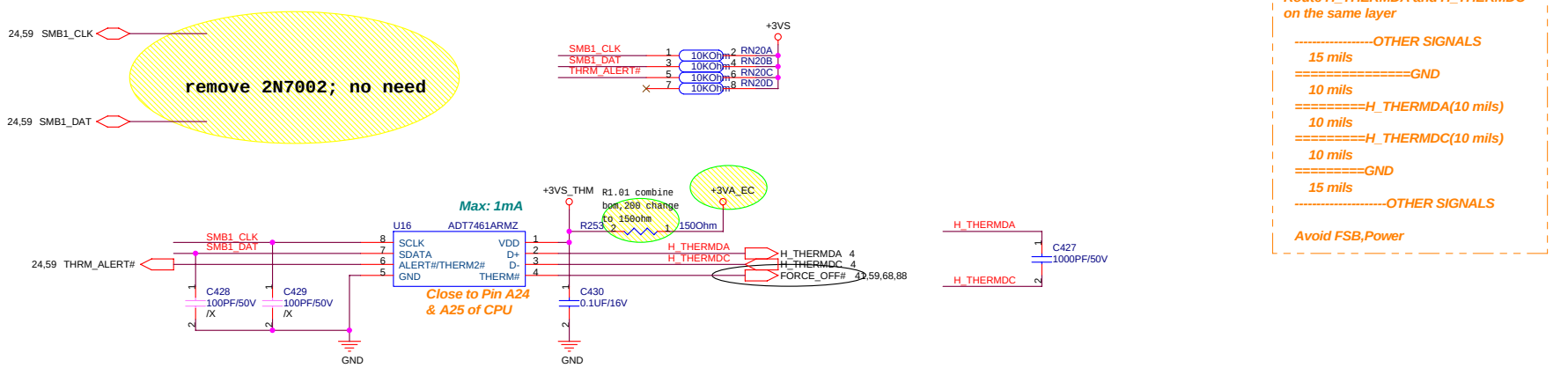




ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 35 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 36 of 92

Thermal Sensor

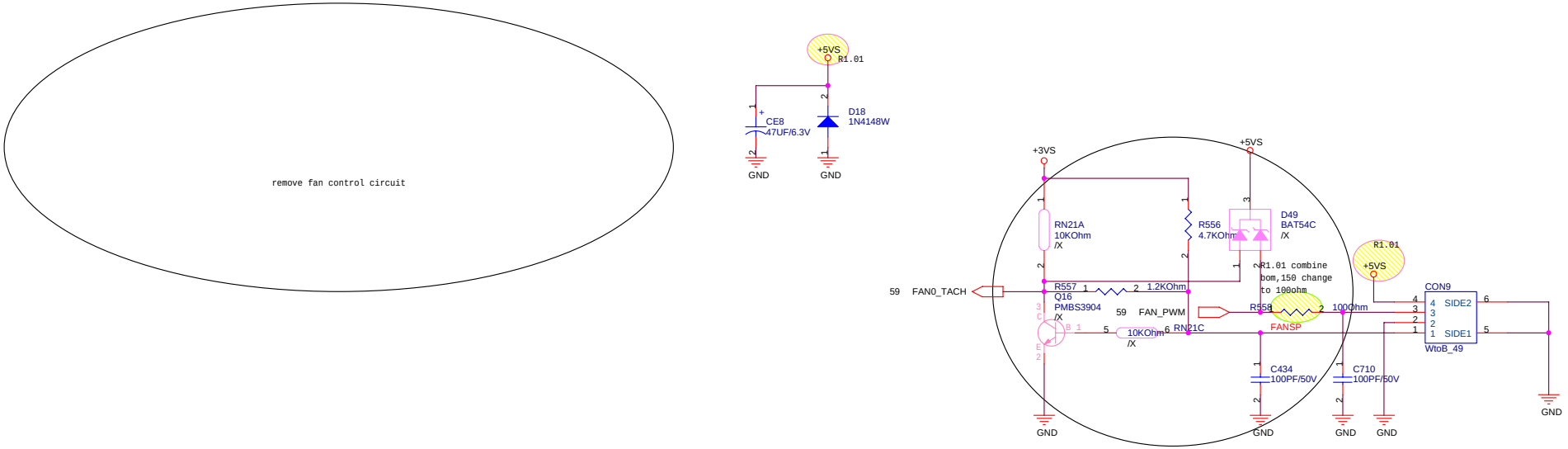


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

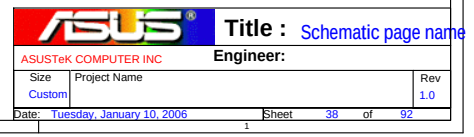
Avoid FSB,Power

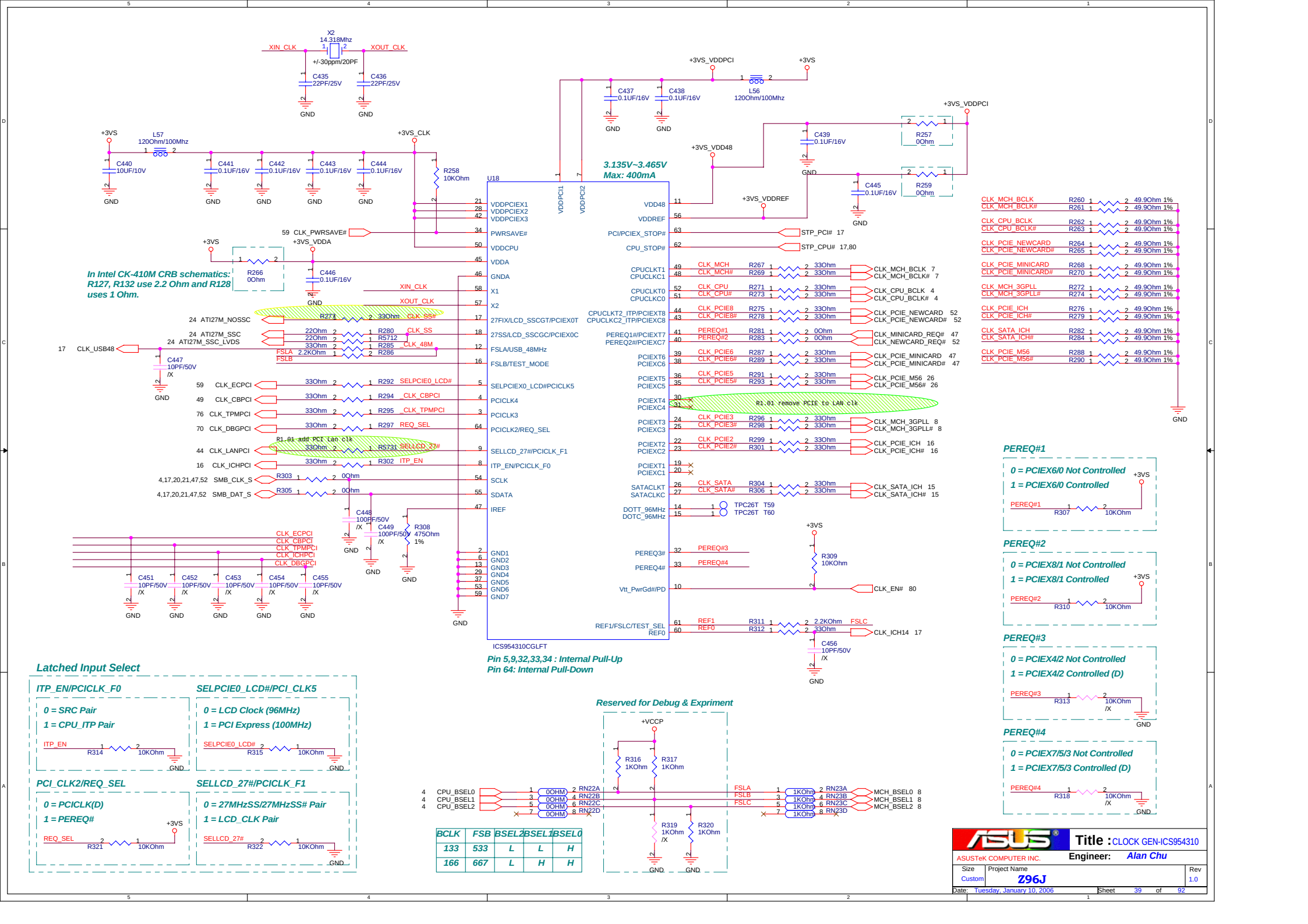
DC FAN Control



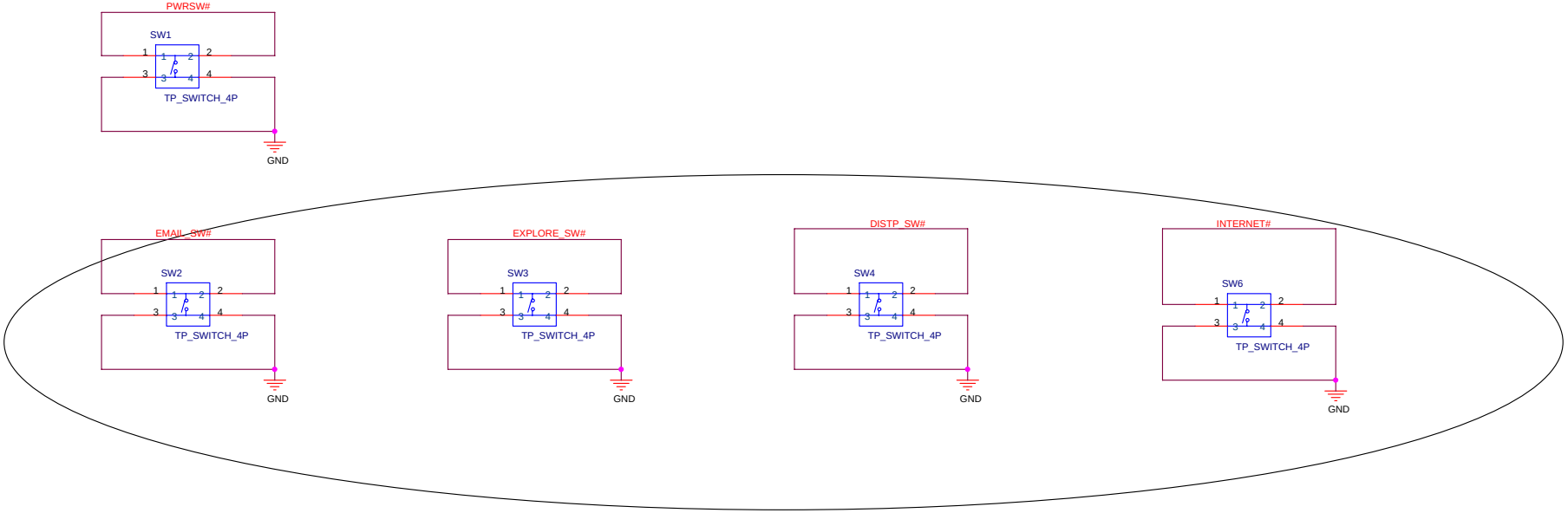
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 37 of 92	

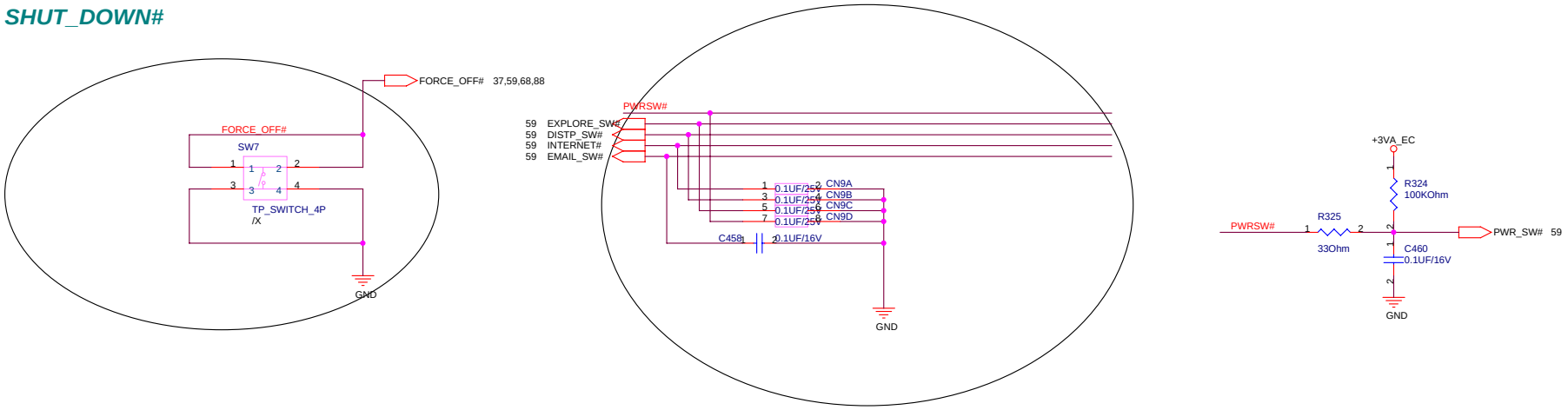

Title : Schematic page name
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
Rev
1.0
Date: Tuesday, January 10, 2006
Sheet 38 of 92


X2
14.318Mhz
XIN_CLK
XOUT_CLK
+/-30ppm/20PF
C435 22PF/25V
C436 22PF/25V
GND
+3VS
L57 120Ohm/100Mhz
+3VS_CLK
C440 10UF/10V
C441 0.1UF/16V
C442 0.1UF/16V
C443 0.1UF/16V
C444 0.1UF/16V
R258 10KOhm
U18
VDDPCIEX1
VDDPCIEX2
VDDPCIEX3
PWRSAVE#
VDDCPU
VDDA
GNDA
X1
X2
27FIX/LCD_SSCGT/PCIEX0T
27SS/LCD_SSCGC/PCIEX0C
FSLA/USB_48MHz
FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5
PCICLK4
PCICLK3
PCICLK2/REQ_SEL
SELLCD_27#/PCICLK_F1
ITP_EN/PCICLK_F0
SCLK
SDATA
IREF
GND1
GND2
GND3
GND4
GND5
GND6
GND7
ICS954310CGLFT
59 CLK_PWRSAVE#
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128 uses 1 Ohm.
R266 0Ohm
C446 0.1UF/16V
24 ATI27M_NOSSC
24 ATI27M_SSC
24 ATI27M_SSC_LVDS
17 CLK_USB48
C447 10PF/50V /X
59 CLK_ECPCI
49 CLK_CBPCI
76 CLK_TPMPCI
70 CLK_DBGPCI
44 CLK_LANPCI
16 CLK_ICHPCI
R1.01 add PCI Lan clk
4,17,20,21,47,52 SMB_CLK_S
4,17,20,21,47,52 SMB_DAT_S
C448 100PF/50V /X
C449 100PF/50V /X
R308 475Ohm 1%
C451 10PF/50V /X
C452 10PF/50V /X
C453 10PF/50V /X
C454 10PF/50V /X
C455 10PF/50V /X
+3VS_VDDPCI
C437 0.1UF/16V
C438 0.1UF/16V
L56 120Ohm/100Mhz
3.135V~3.465V
Max: 400mA
VDDPCI1
VDDPCI2
VDD48
VDDREF
PCI/PCIEX_STOP#
CPU_STOP#
CPUCLKT1
CPUCLKC1
CPUCLKT0
CPUCLKC0
CPUCLKT2_ITP/PCIEXT8
CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7
PEREQ2#/PCIEXC7
PCIEXT6
PCIEXC6
PCIEXT5
PCIEXC5
PCIEXT4
PCIEXC4
PCIEXT3
PCIEXC3
PCIEXT2
PCIEXC2
PCIEXT1
PCIEXC1
SATACLKT
SATACLKC
DOTT_96MHz
DOTC_96MHz
PEREQ3#
PEREQ4#
Vtt_PwrGd#/PD
REF1/FSLC/TEST_SEL
REF0
+3VS_VDD48
+3VS_VDDREF
C439 0.1UF/16V
C445 0.1UF/16V
R257 0Ohm
R259 0Ohm
STP_PCI# 17
STP_CPU# 17,80
CLK_EN# 80
CLK_ICH14 17
C456 10PF/50V /X
R309 10KOhm
R311 2.2KOhm FSLC
R312 33Ohm
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
CLK_MCH_BCLK R260 49.9Ohm 1%
CLK_MCH_BCLK# R261 49.9Ohm 1%
CLK_CPU_BCLK R262 49.9Ohm 1%
CLK_CPU_BCLK# R263 49.9Ohm 1%
CLK_PCIE_NEWCARD R264 49.9Ohm 1%
CLK_PCIE_NEWCARD# R265 49.9Ohm 1%
CLK_PCIE_MINICARD R268 49.9Ohm 1%
CLK_PCIE_MINICARD# R270 49.9Ohm 1%
CLK_MCH_3GPLL R272 49.9Ohm 1%
CLK_MCH_3GPLL# R274 49.9Ohm 1%
CLK_PCIE_ICH R276 49.9Ohm 1%
CLK_PCIE_ICH# R279 49.9Ohm 1%
CLK_SATA_ICH R282 49.9Ohm 1%
CLK_SATA_ICH# R284 49.9Ohm 1%
CLK_PCIE_M56 R288 49.9Ohm 1%
CLK_PCIE_M56# R290 49.9Ohm 1%
R1.01 remove PCIE to LAN clk
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
R307 10KOhm
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
R310 10KOhm
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
R313 10KOhm /X
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
R318 10KOhm /X
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
R314 10KOhm
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
R315 10KOhm
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
R321 10KOhm
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
R322 10KOhm
Reserved for Debug & Expriment
+VCCP
R316 1KOhm
R317 1KOhm
R319 1KOhm /X
R320 1KOhm
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
RN22A
RN22B
RN22C
RN22D
RN23A
RN23B
RN23C
RN23D
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 39 of 92

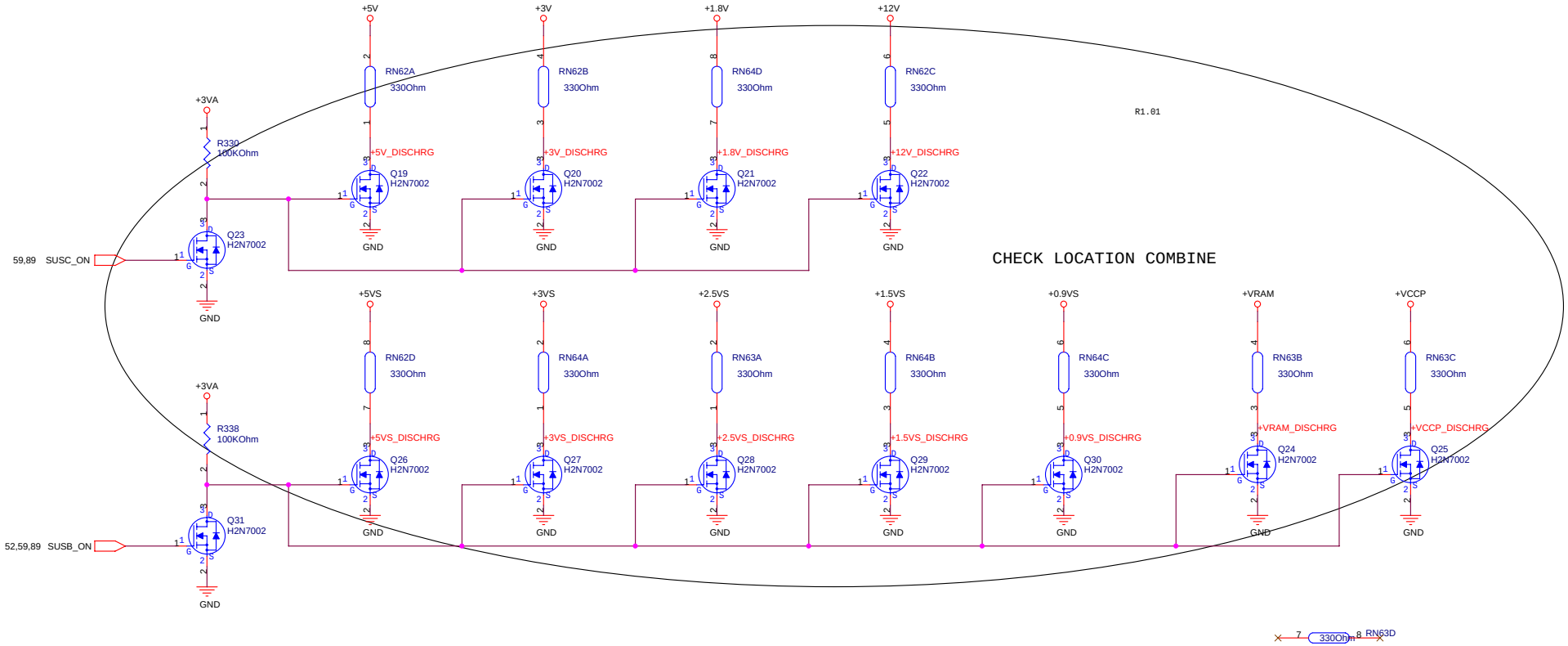
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 40 of 92



SHUT_DOWN#

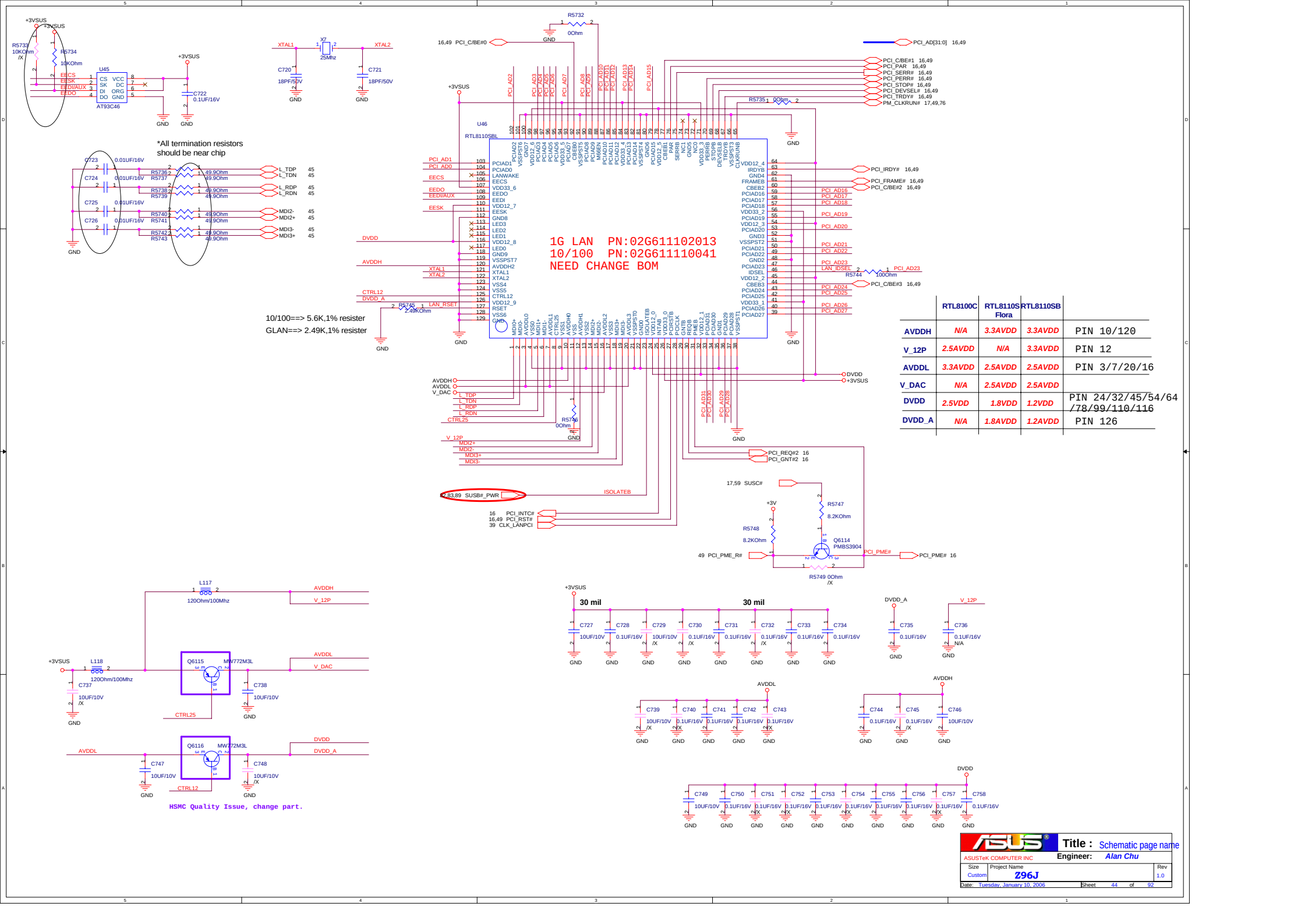


ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 41 of 92	



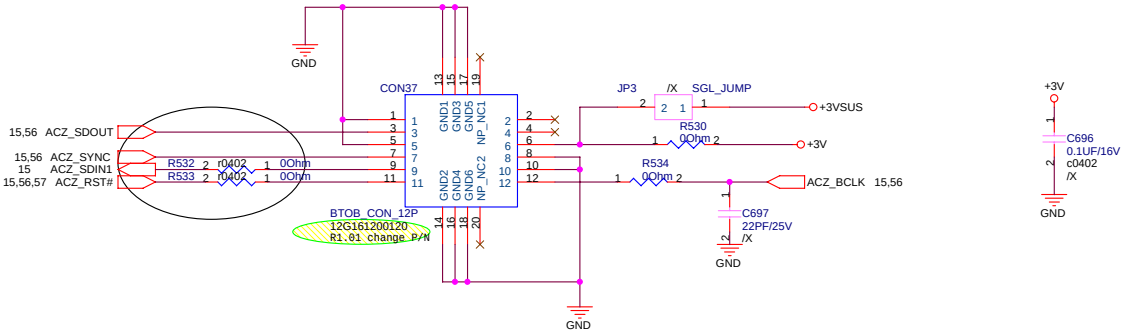
ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 42 of 92	

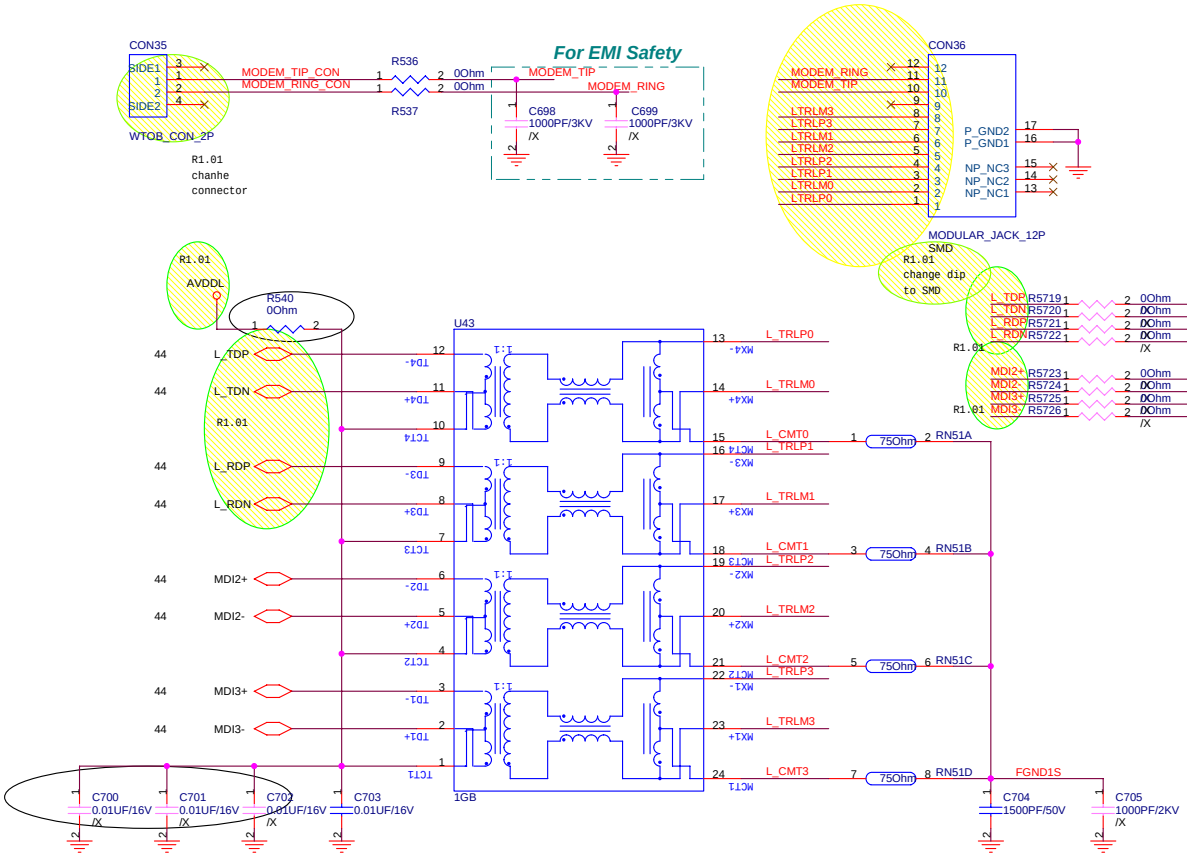
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 43 of 92

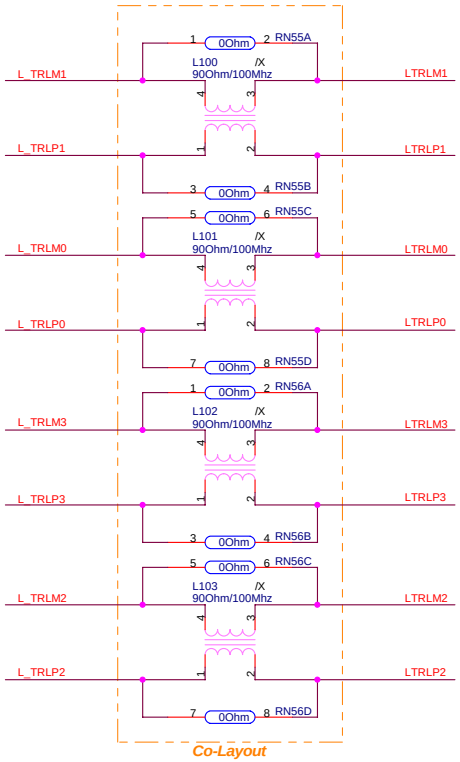


	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

MDC CONN.







ASUSTeK COMPUTER INC.

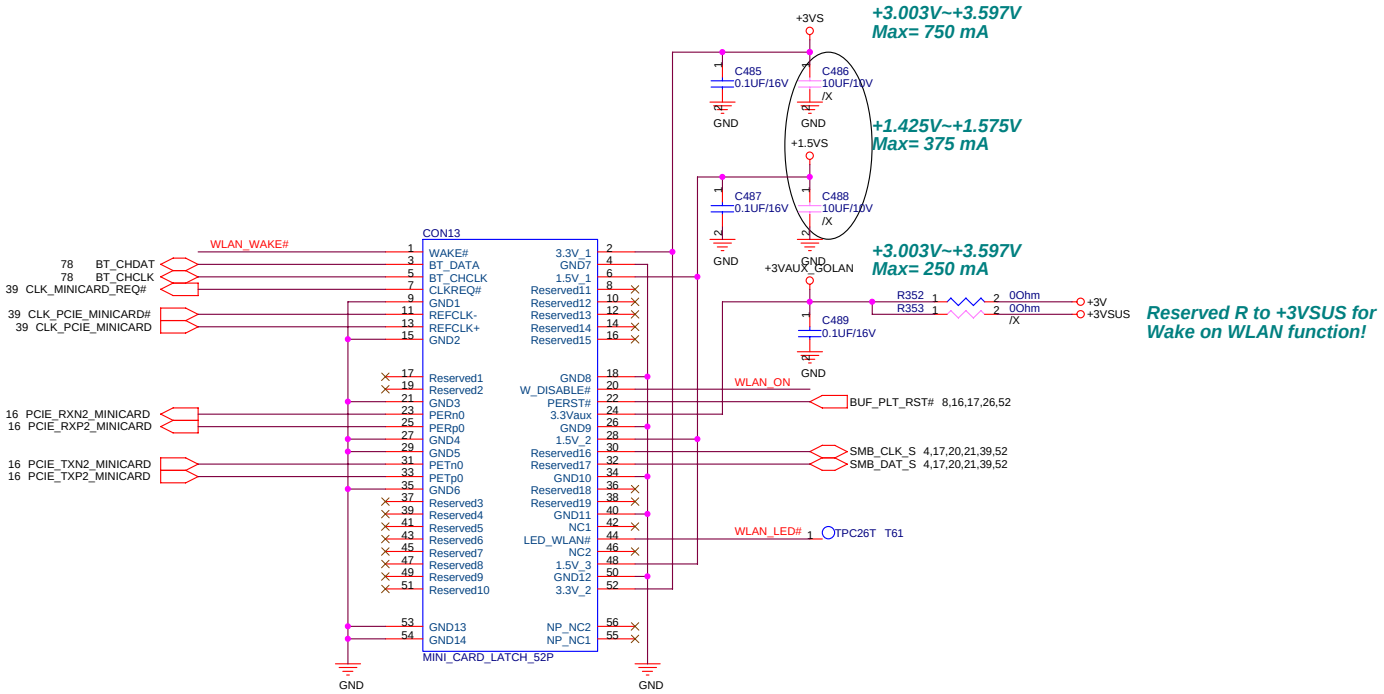
Title : RJ45&RJ11

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

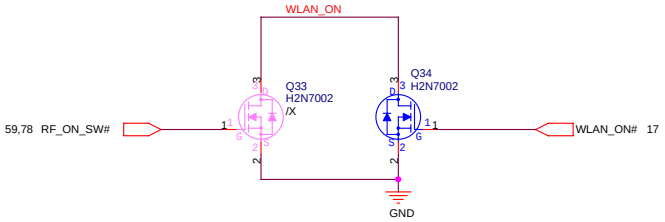
Date: Tuesday, January 10, 2006 Sheet 45 of 92

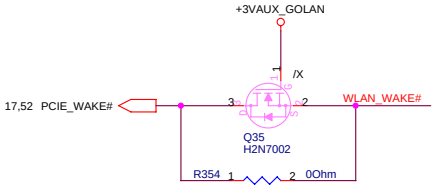
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 46 of 92



H54 & H56

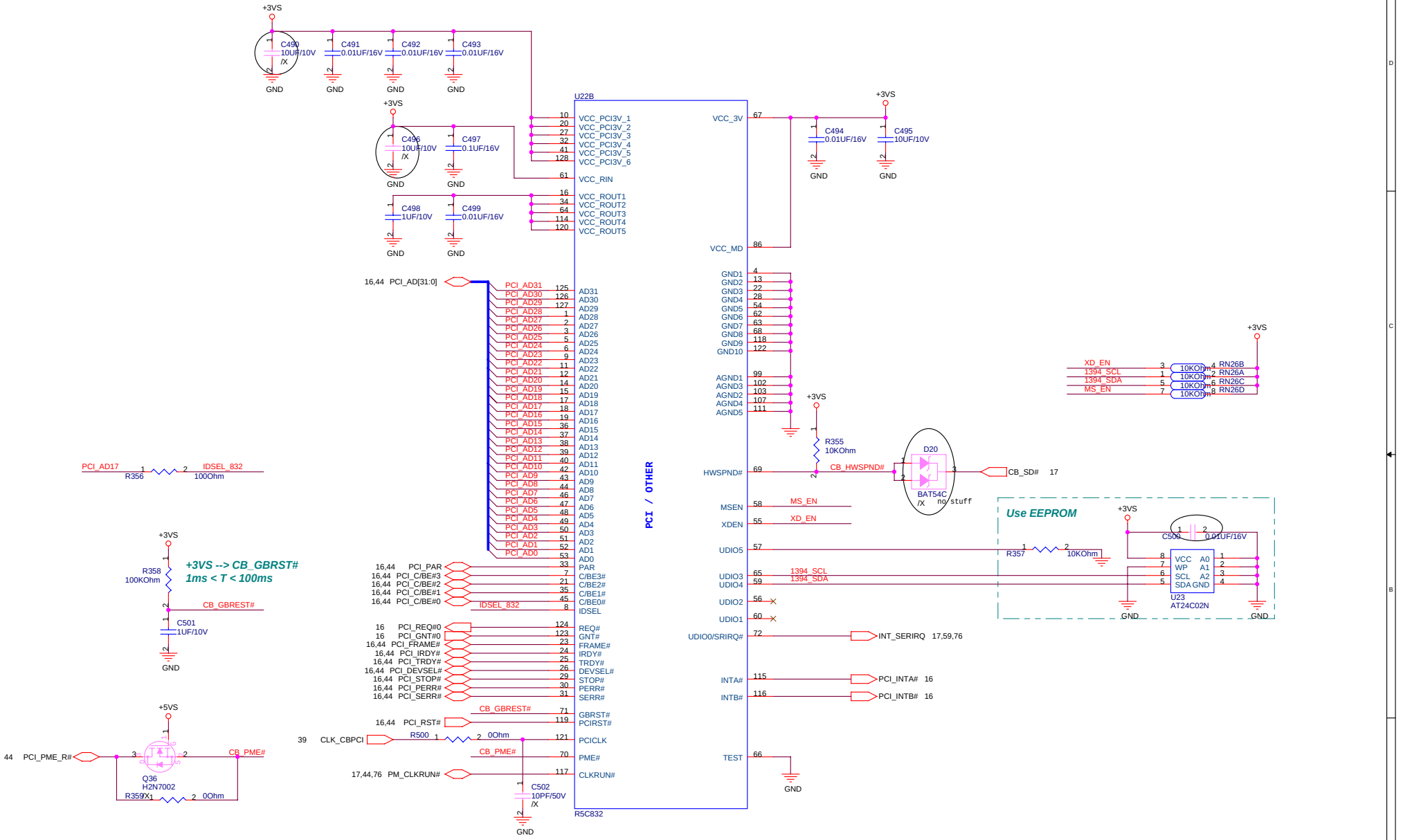
R1.01 remove connector,change to screw





ASUSTeK COMPUTER INC.	Title : MINICARD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 47 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 48 of 92



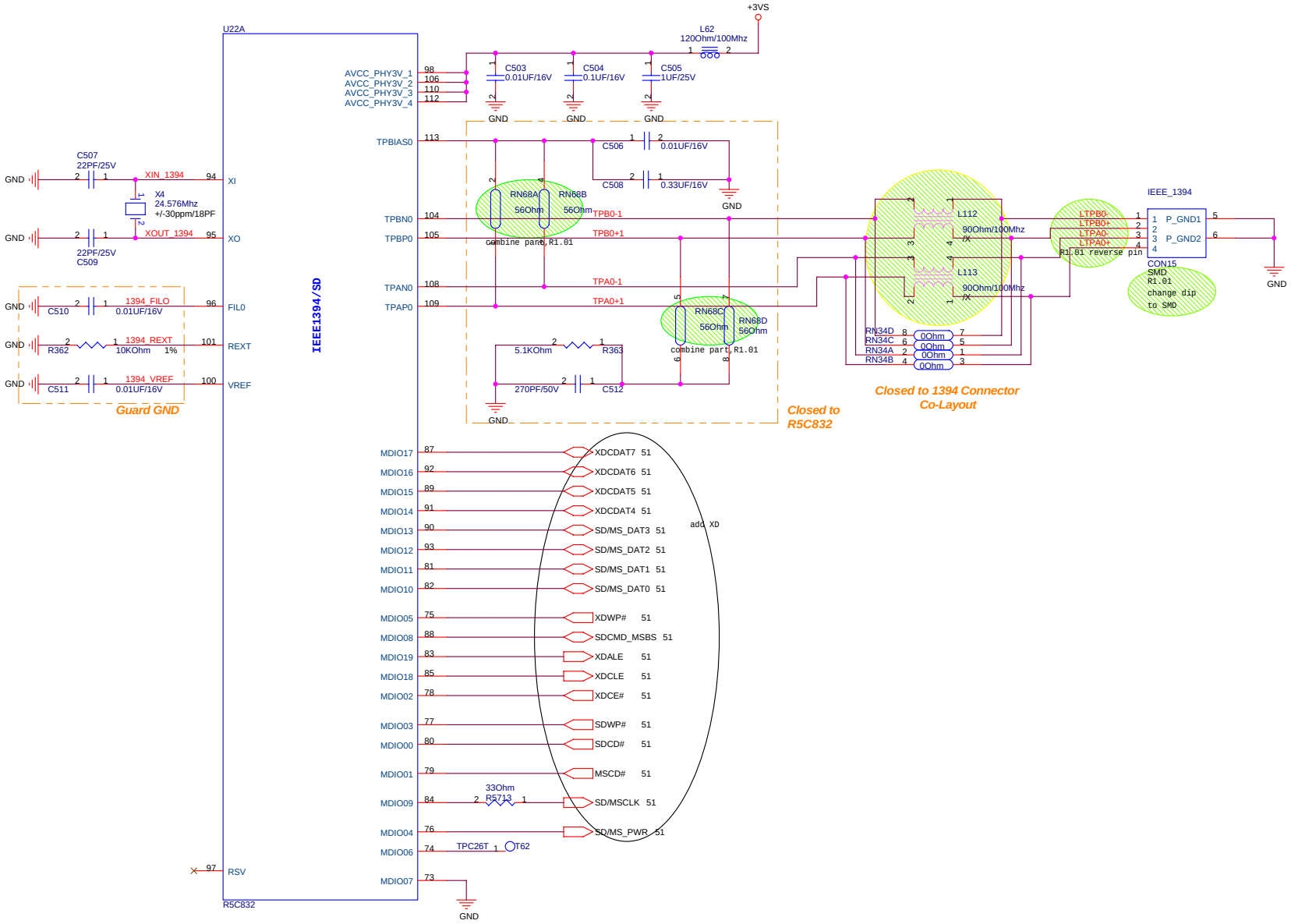
ASUSTeK COMPUTER INC. MB6

Title : CARD1394-R5C832(1)

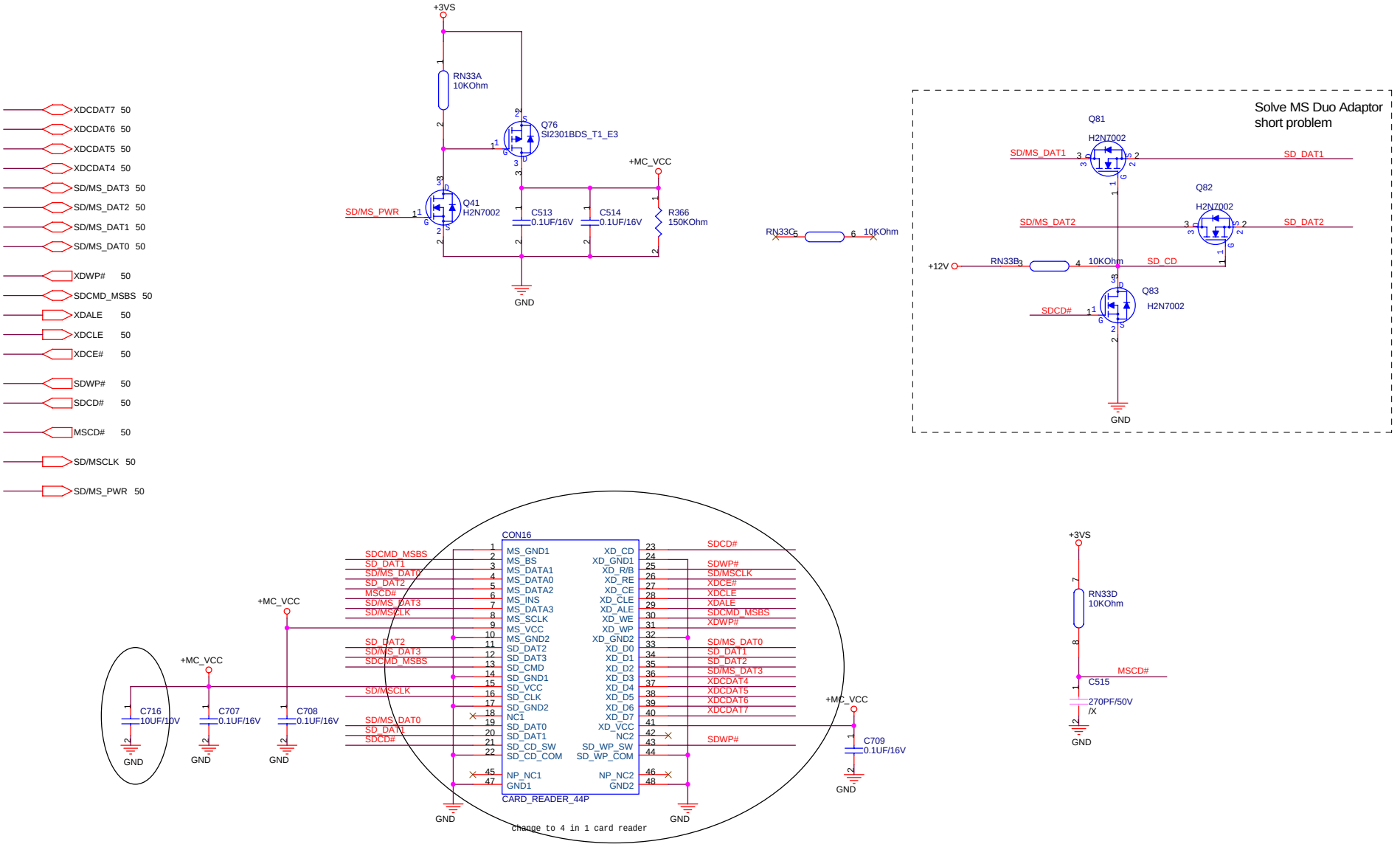
Engineer: ALAN CHU

Size	Project Name	Rev
Custom	Z96J	1.0

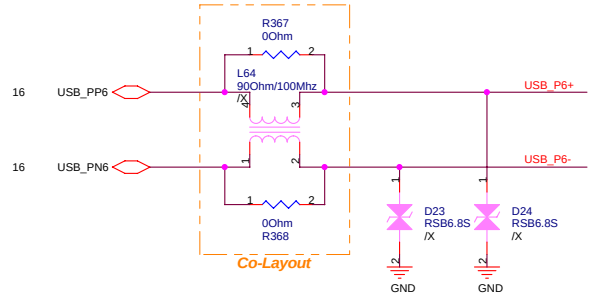
Date: Tuesday, January 10, 2006 Sheet 49 of 92

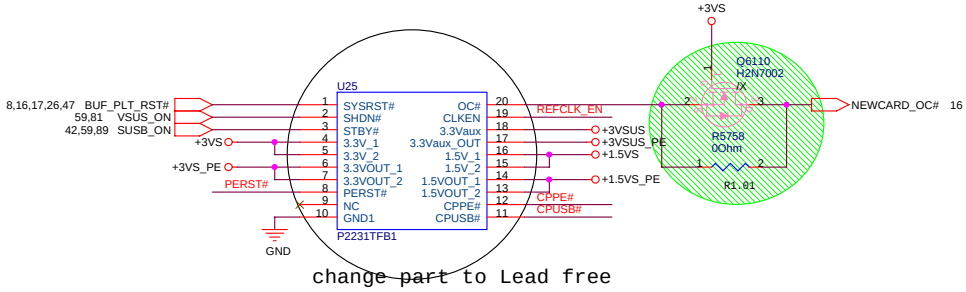


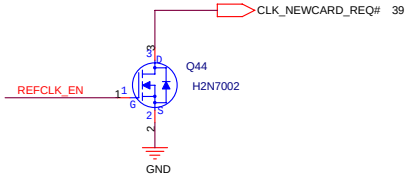
ASUSTeK COMPUTER INC. MB6	Title : CARD1394-R5C832(2)	
	Engineer: ALAN CHU	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 50 of 92	



ASUSTeK COMPUTER INC	Title : 4 in 1 CARD READER	
	Engineer: ALAN CHU	
Size: A3	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 51 of 92	

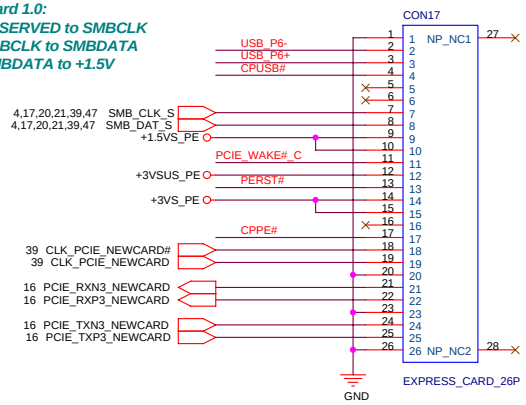


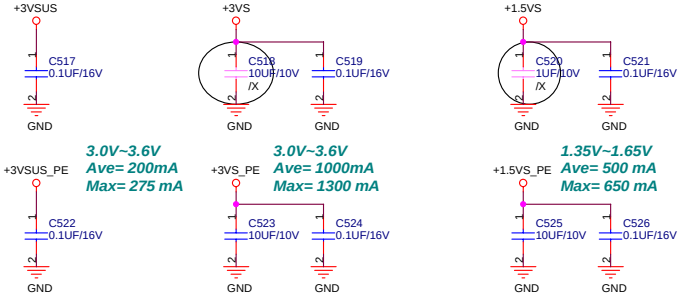


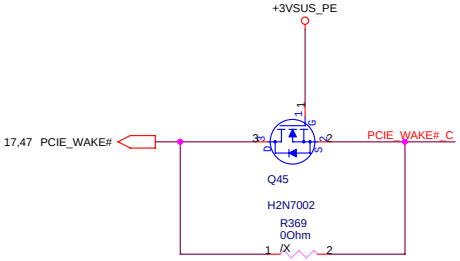


NewCard Header

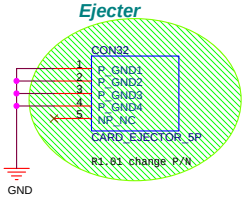
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V







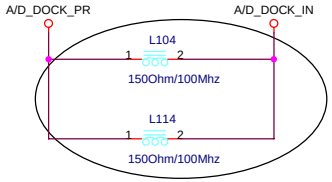
NewCard Ejecter

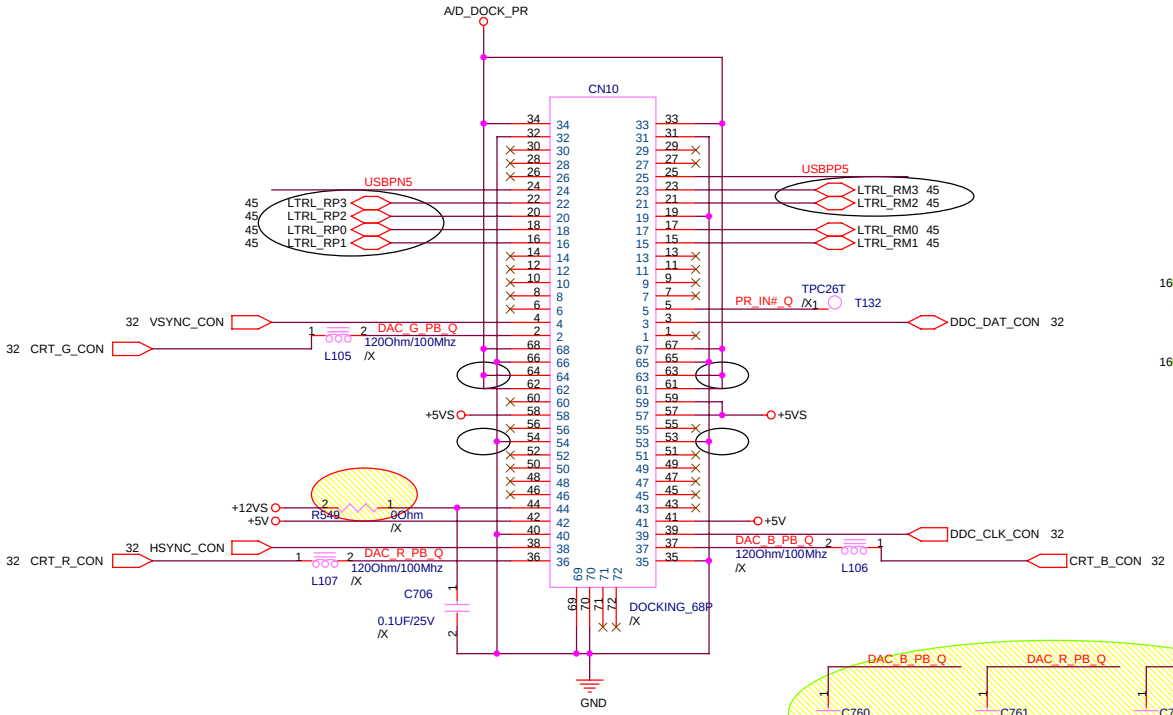


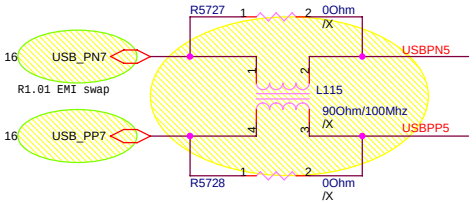
ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 52 of 92	

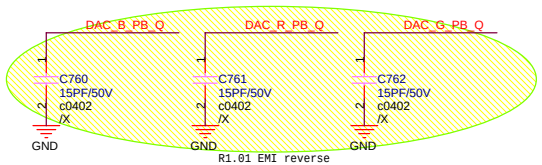
Title :	<Title>
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: A	Project Name: PROJECT NAME
Rev: 1.00	
Date: Tuesday, January 10, 2006	Sheet 53 of 92

PORT BAR III



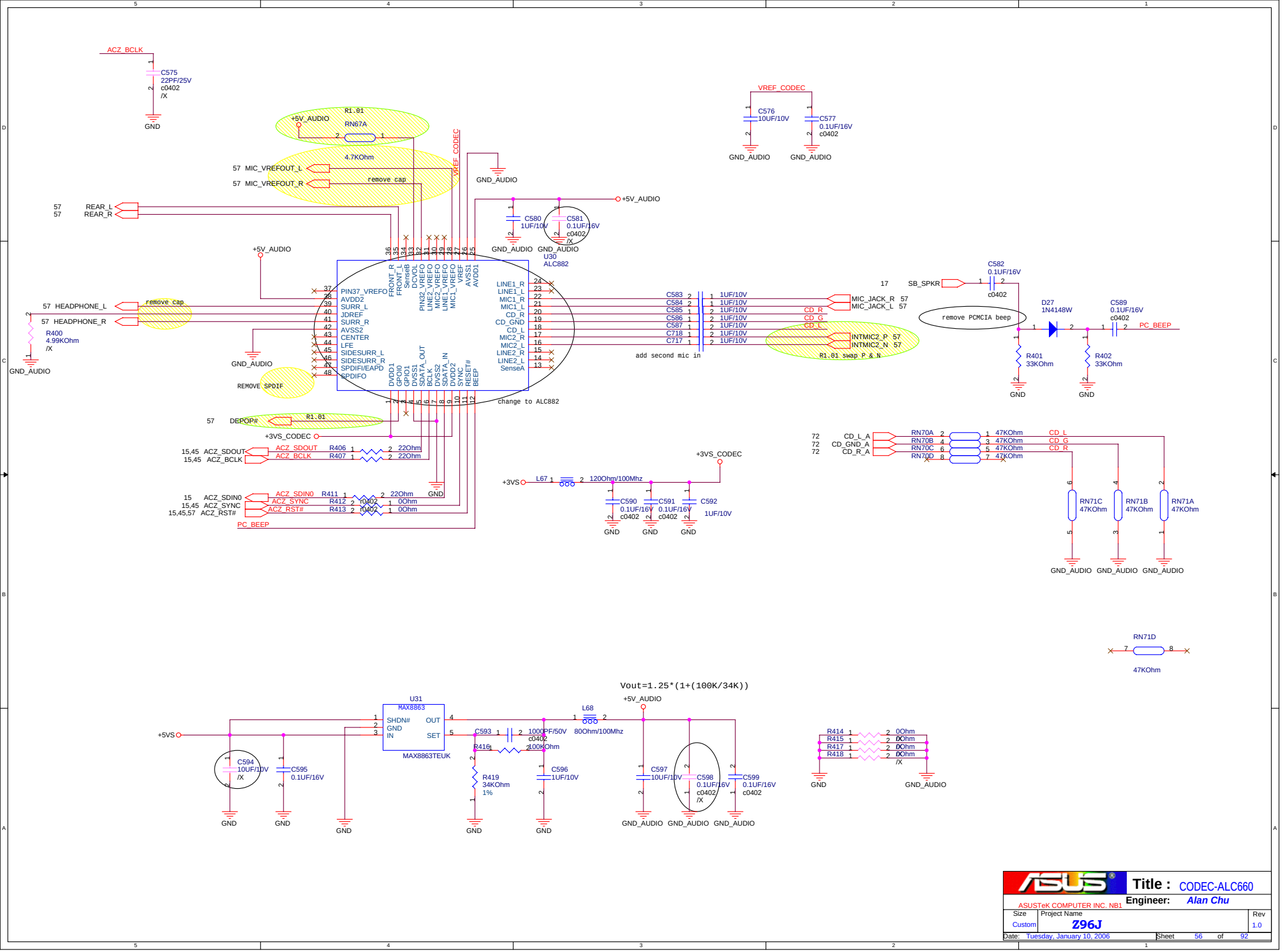


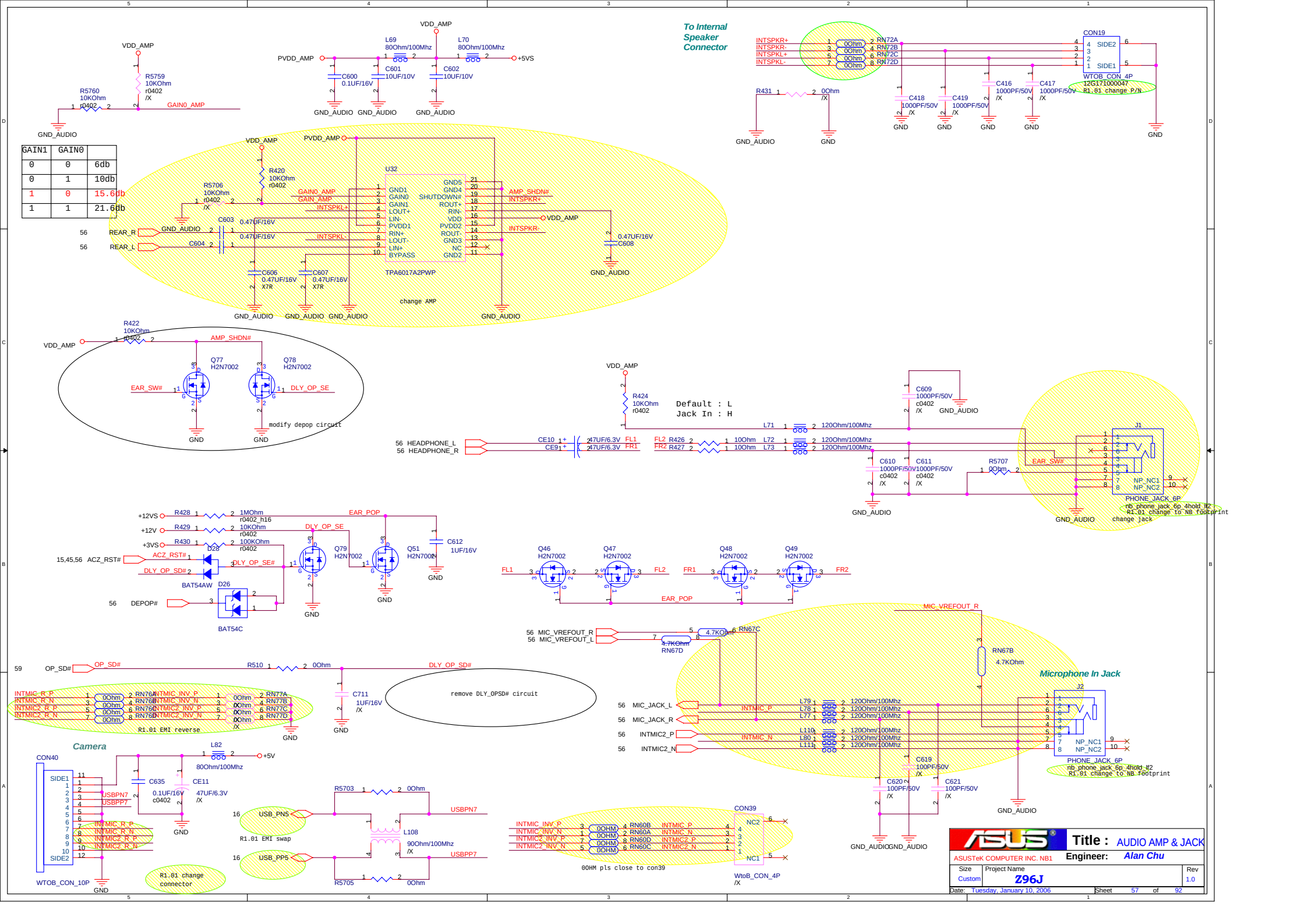




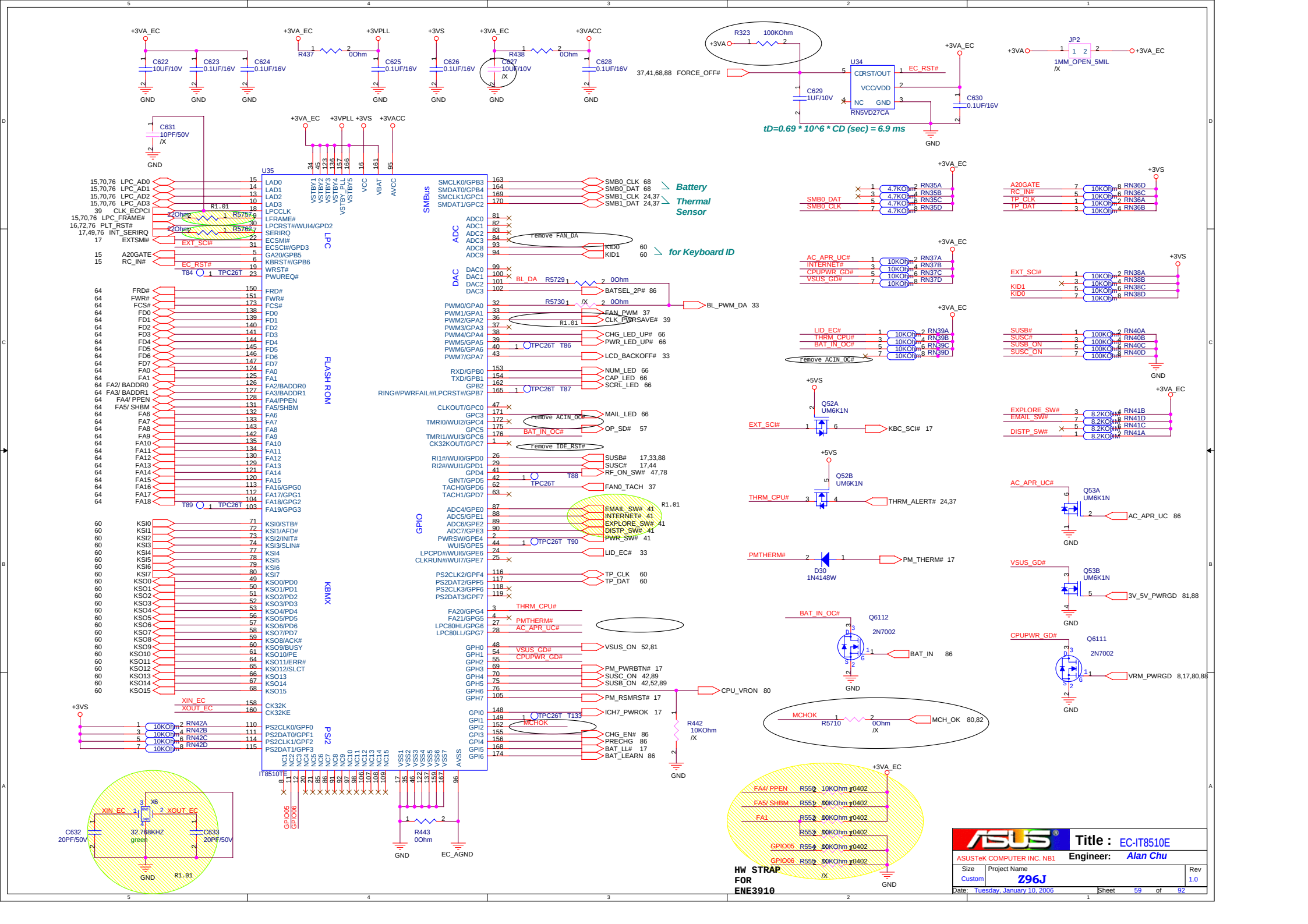
ASUSTeK COMPUTER INC	Title : <Title>	
	Engineer: Alan Chu	
Size: A3	Project Name: PROJECT NAME	Rev: 1.00
Date: Tuesday, January 10, 2006	Sheet 54 of 92	

Title :	Z96J
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 55 of 92

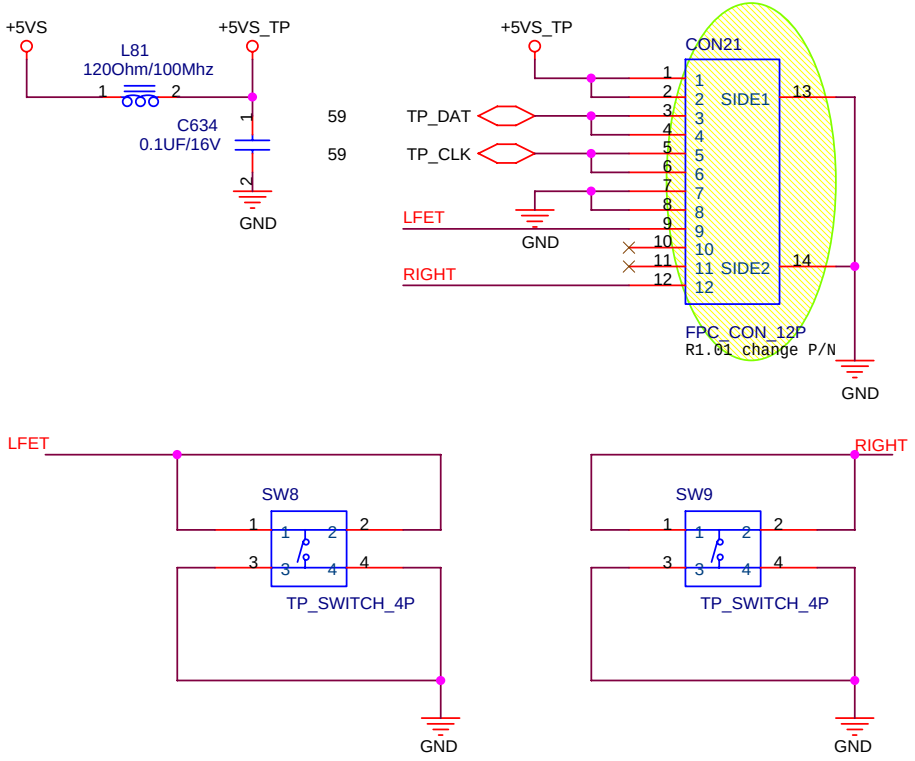

ACZ_BCLK
C575
22PF/25V
c0402
/X
GND
+5V_AUDIO
R1.01
RN67A
4.7KOhm
57 MIC_VREFOUT_L
57 MIC_VREFOUT_R
remove cap
VREF_CODEC
GND_AUDIO
57 REAR_L
57 REAR_R
C580
1UF/10V
C581
0.1UF/16V
c0402
/X
U30
ALC882
PIN37_VREFO
AVDD2
SURR_L
JDREF
SURR_R
AVSS2
CENTER
LFE
SIDESURR_L
SIDESURR_R
SPDIFI/EAPD
SPDIFO
LINE1_R
LINE1_L
MIC1_R
MIC1_L
CD_R
CD_GND
CD_L
MIC2_R
MIC2_L
LINE2_R
LINE2_L
SenseA
57 HEADPHONE_L
57 HEADPHONE_R
R400
4.99KOhm
/X
REMOVE SPDIF
change to ALC882
C583
C584
C585
C586
C587
C718
C717
1UF/10V
MIC_JACK_R 57
MIC_JACK_L 57
CD_R
CD_G
CD_L
INTMIC2_P 57
INTMIC2_N 57
R1.01 swap P & N
add second mic in
17 SB_SPKR
C582
0.1UF/16V
c0402
remove PCMCIA beep
D27
1N4148W
C589
0.1UF/16V
c0402
PC_BEEP
R401
33KOhm
R402
33KOhm
GND
57 DEPOP#
R1.01
+3VS_CODEC
15,45 ACZ_SDOUT
15,45 ACZ_BCLK
ACZ_SDOUT
ACZ_BCLK
R406
R407
22Ohm
15 ACZ_SDIN0
15,45 ACZ_SYNC
15,45,57 ACZ_RST#
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#
R411
R412
R413
0Ohm
PC_BEEP
+3VS
L67
120Ohm/100Mhz
C590
C591
C592
0.1UF/16V
1UF/10V
c0402
72 CD_L_A
72 CD_GND_A
72 CD_R_A
RN70A
RN70B
RN70C
RN70D
47KOhm
RN71C
RN71B
RN71A
RN71D
U31
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
Vout=1.25*(1+(100K/34K))
L68
80Ohm/100Mhz
C593
1000PF/50V
R416
100KOhm
R419
34KOhm
1%
C596
1UF/10V
C594
10UF/10V
C595
0.1UF/16V
C597
10UF/10V
C598
0.1UF/16V
C599
0.1UF/16V
R414
R415
R417
R418
Title : CODEC-ALC660
Engineer: Alan Chu
ASUSTeK COMPUTER INC. NB1
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 56 of 92


To Internal Speaker Connector
CON19
WTOB_CON_4P
12G171000047
R1.01 change P/N
GAIN1 GAIN0
0 0 6db
0 1 10db
1 0 15.6db
1 1 21.6db
U32
TPA6017A2PWP
change AMP
modify depop circuit
Default : L
Jack In : H
PHONE_JACK_6P
nb_phone_jack_6p_4hold_H2
R1.01 change to NB footprint
change jack
Microphone In Jack
J2
remove DLY_OPSD# circuit
R1.01 EMI reverse
Camera
CON40
WTOB_CON_10P
R1.01 change connector
R1.01 EMI swap
00HM pls close to con39
CON39
WtoB_CON_4P
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chu
Size Custom
Project Name Z96J
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 57 of 92

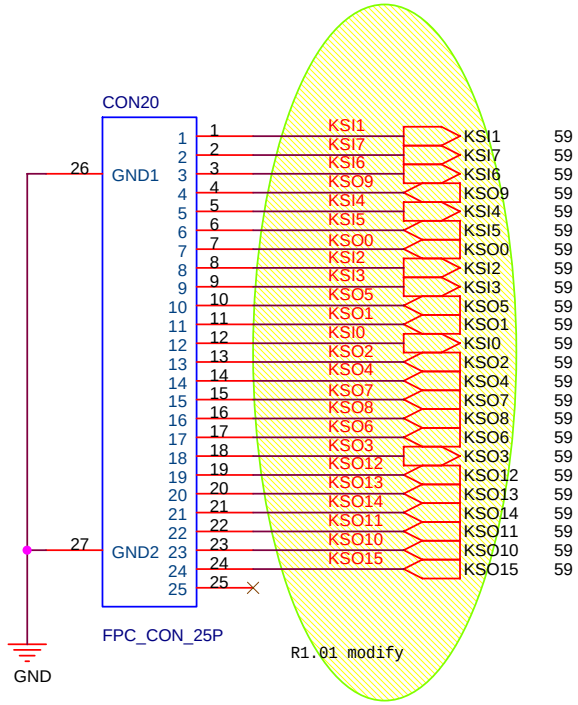
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 58 of 92

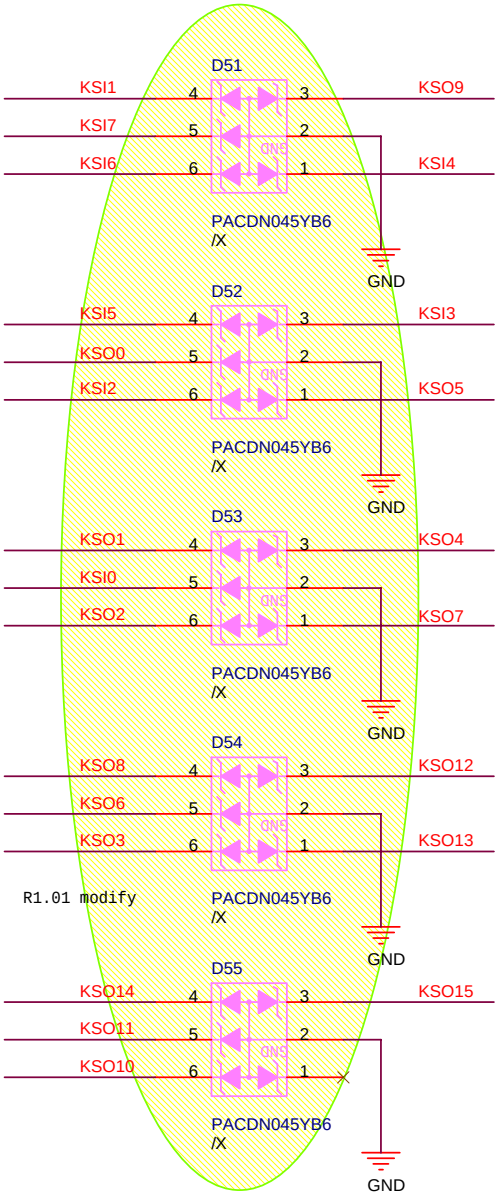

U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
ADC
DAC
SMBus
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
HW STRAP FOR ENE3910
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chu
Project Name Z96J
Size Custom
Rev 1.0
Date: Tuesday, January 10, 2006
Sheet 59 of 92

For Touch-Pad

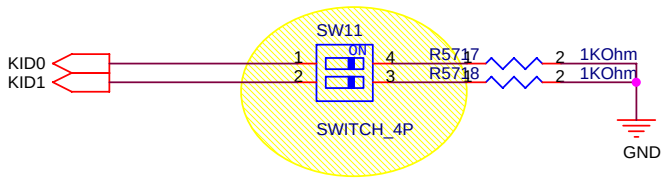


For Keyboard



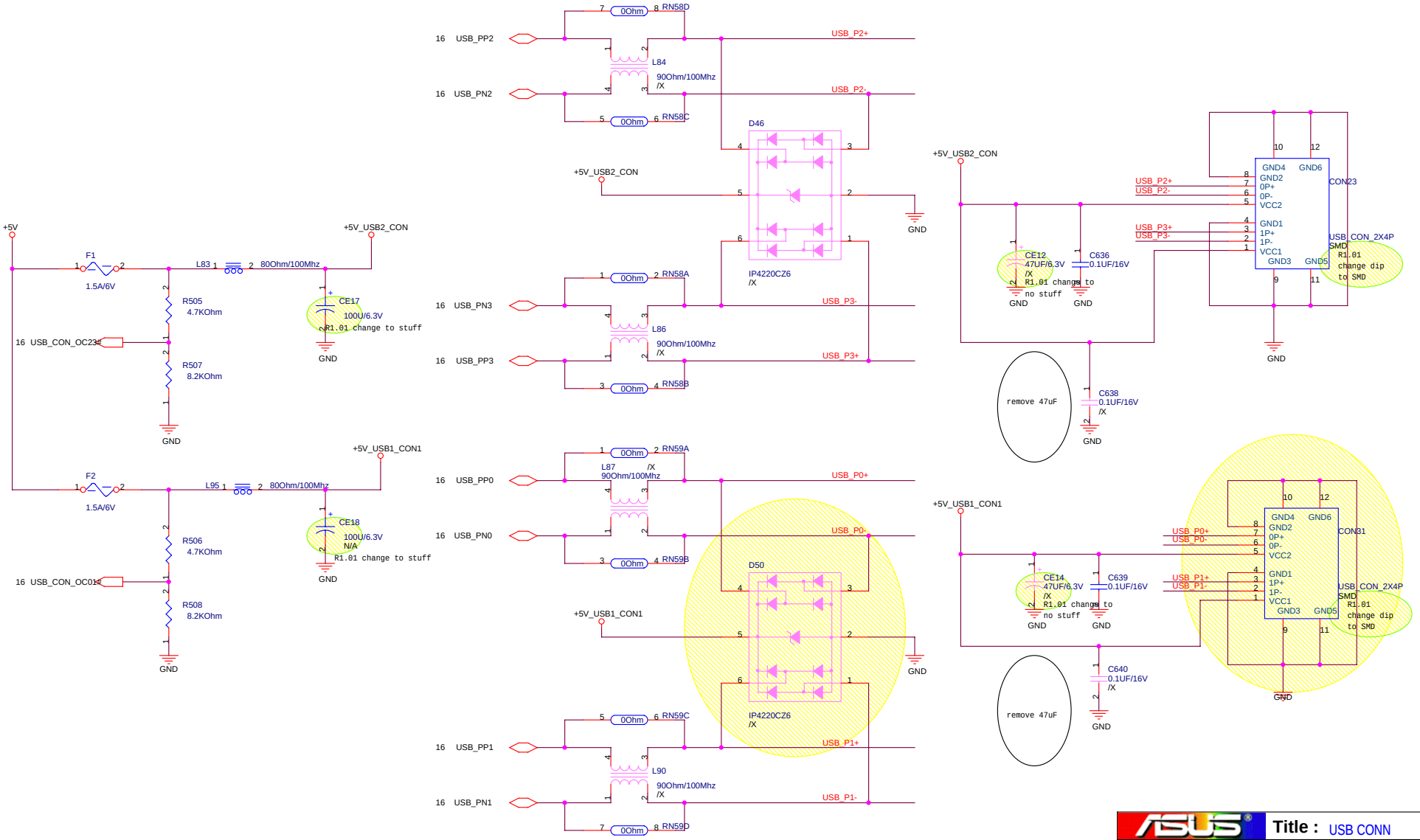


remove pull high,already pull high



ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: ALAN CHU	
Size: A4	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 60 of 92	

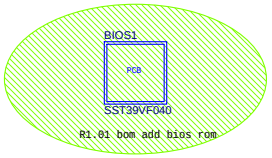
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 61 of 92



ASUSTeK COMPUTER INC	Title : USB CONN		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96J		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 62 of 92		

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 63 of 92

ISA ROM



EC Hardware Strapping

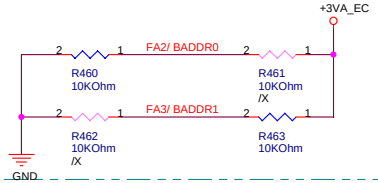
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

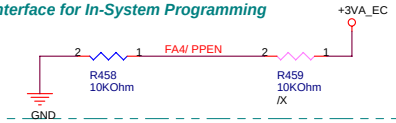


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

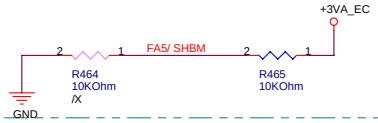
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

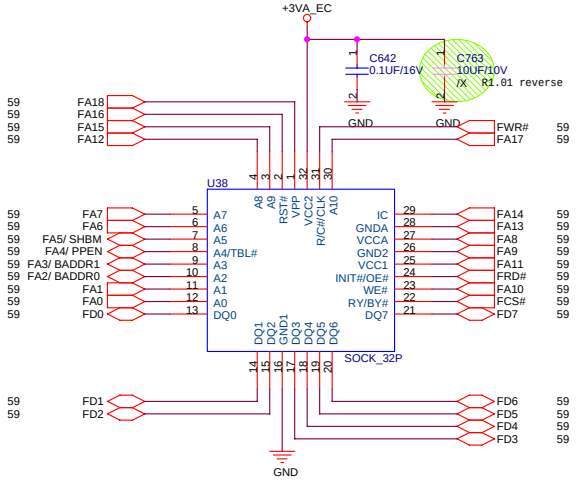


FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



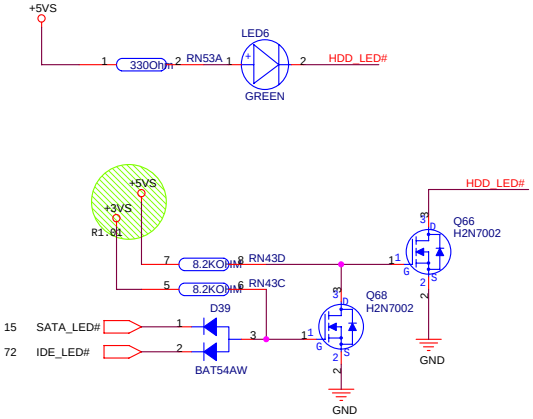


ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 64 of 92	

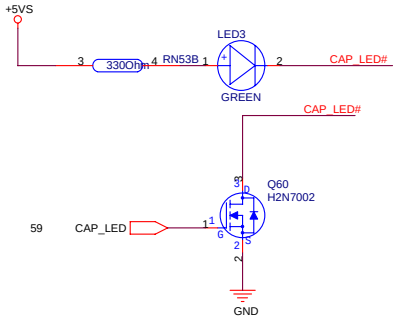
ASUSTeK COMPUTER INC	Title : Schematic page name
	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 65 of 92

For LED

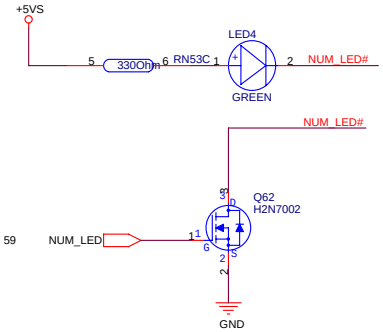
For SATA/IDE LED



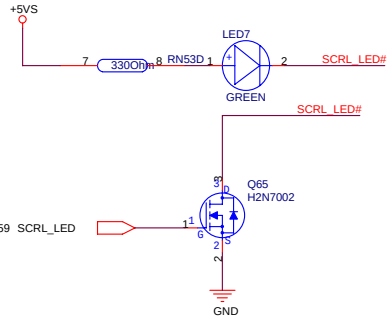
for Cap. Lock



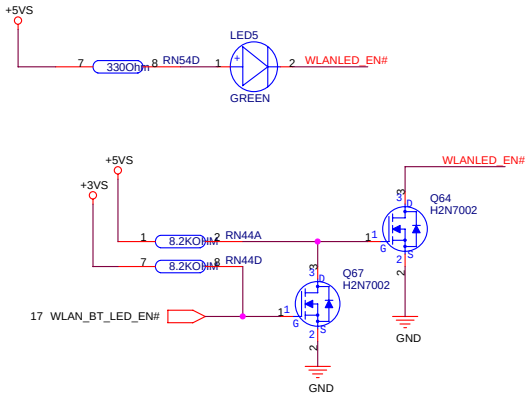
for Num Lock



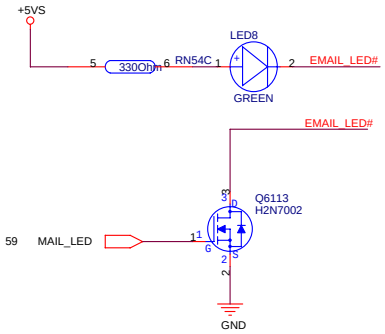
for Scroll Lock



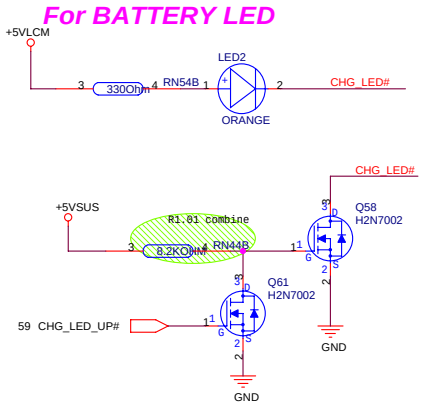
For WireLess LED



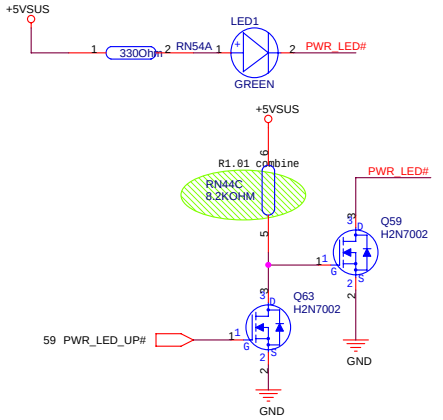
for email



For BATTERY LED



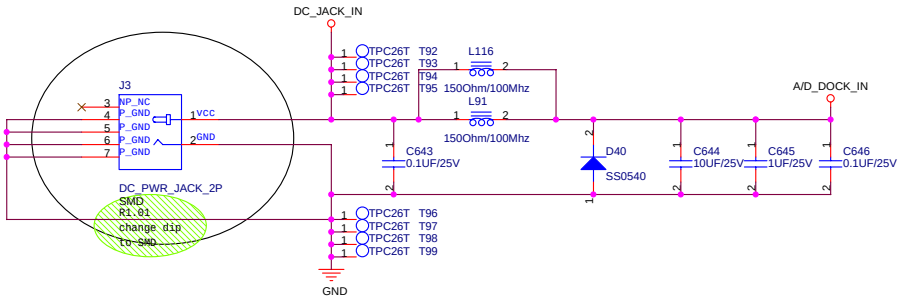
For POWER LED



ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 66 of 92	

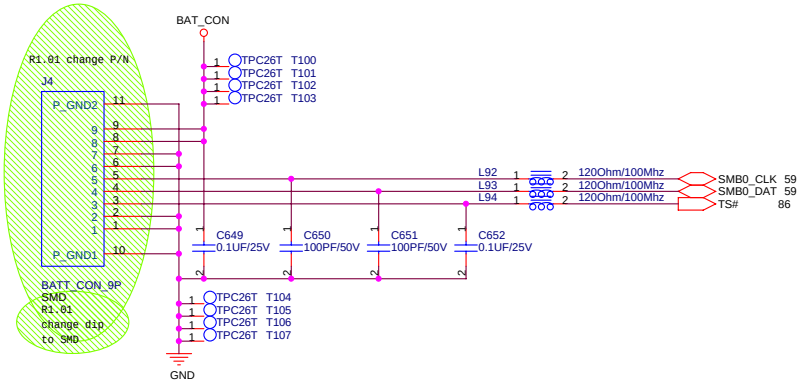
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 67 of 92

DC IN

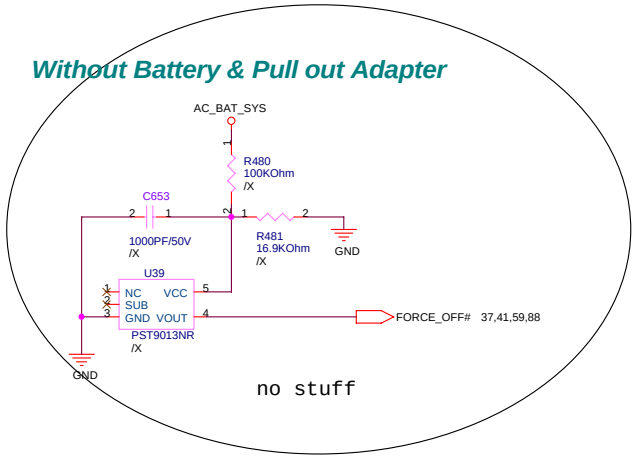


remove AC DC detect; no need

BAT IN



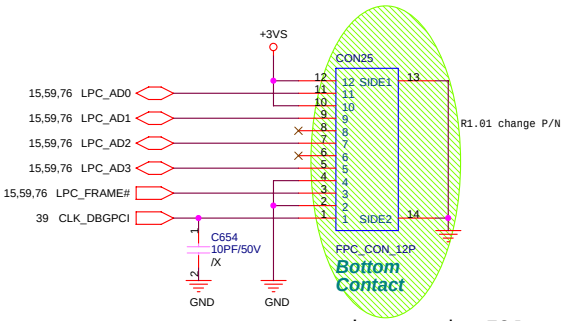
Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 68 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 69 of 92

For Debug

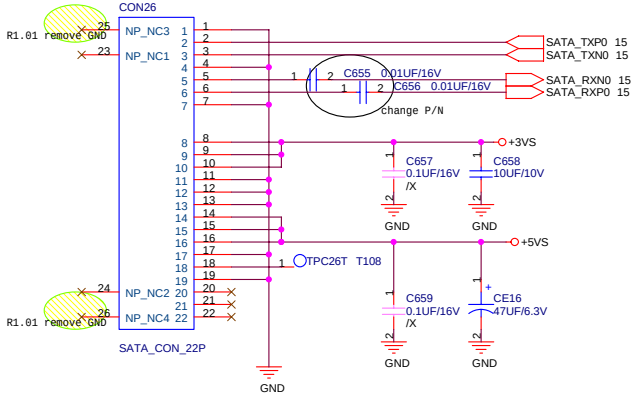


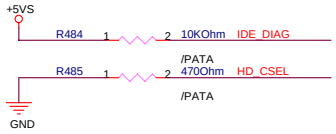
pin swap;by F3J

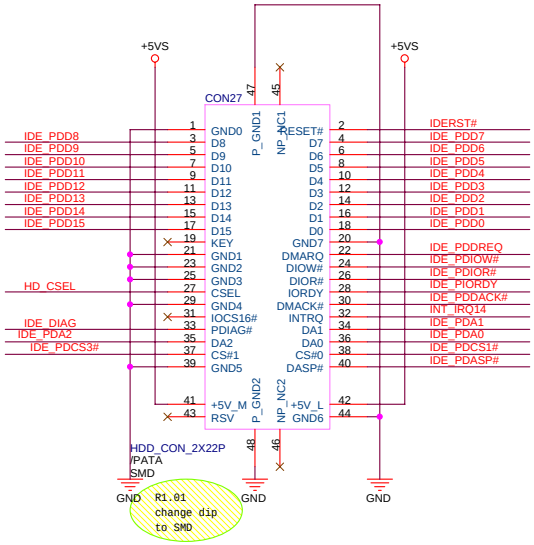
ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 70 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 71 of 92

HD_CSEL : Pull-Down, HDD as Master

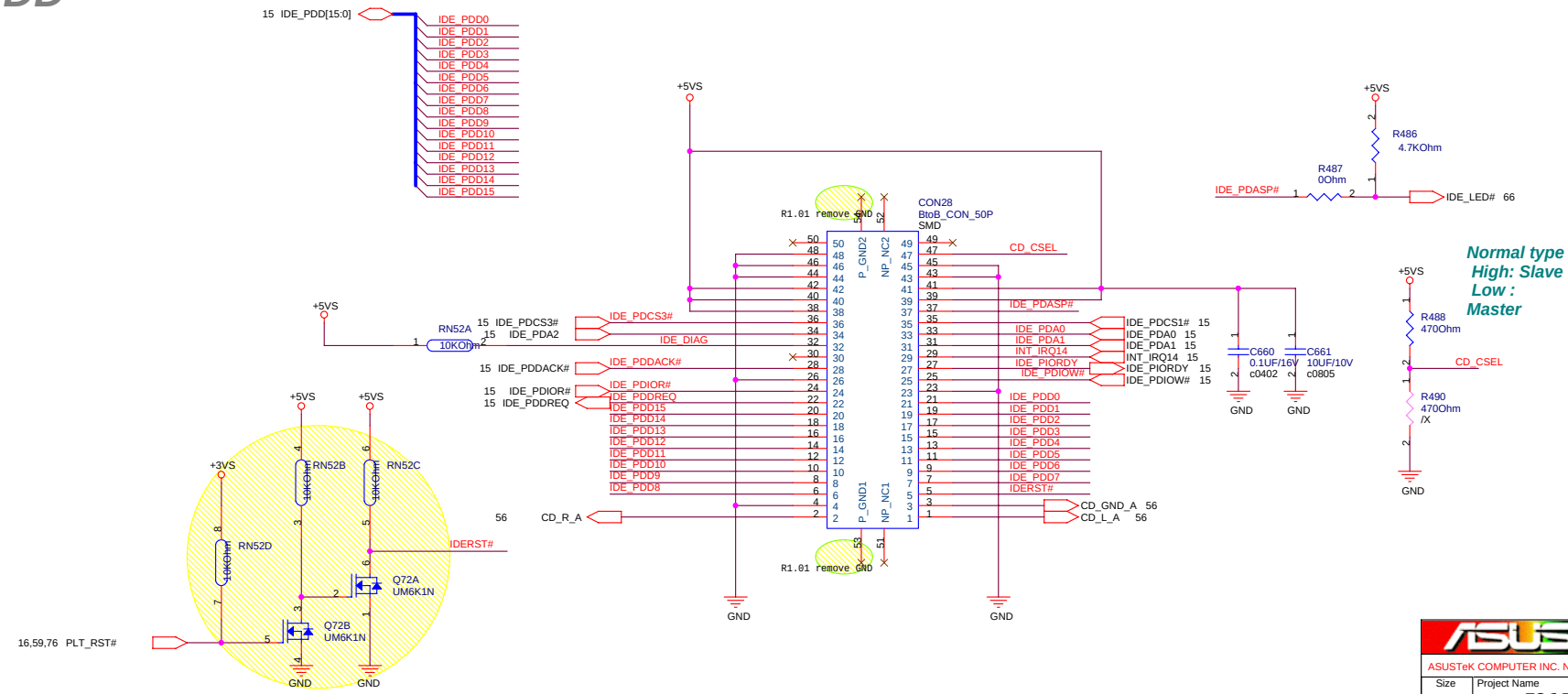






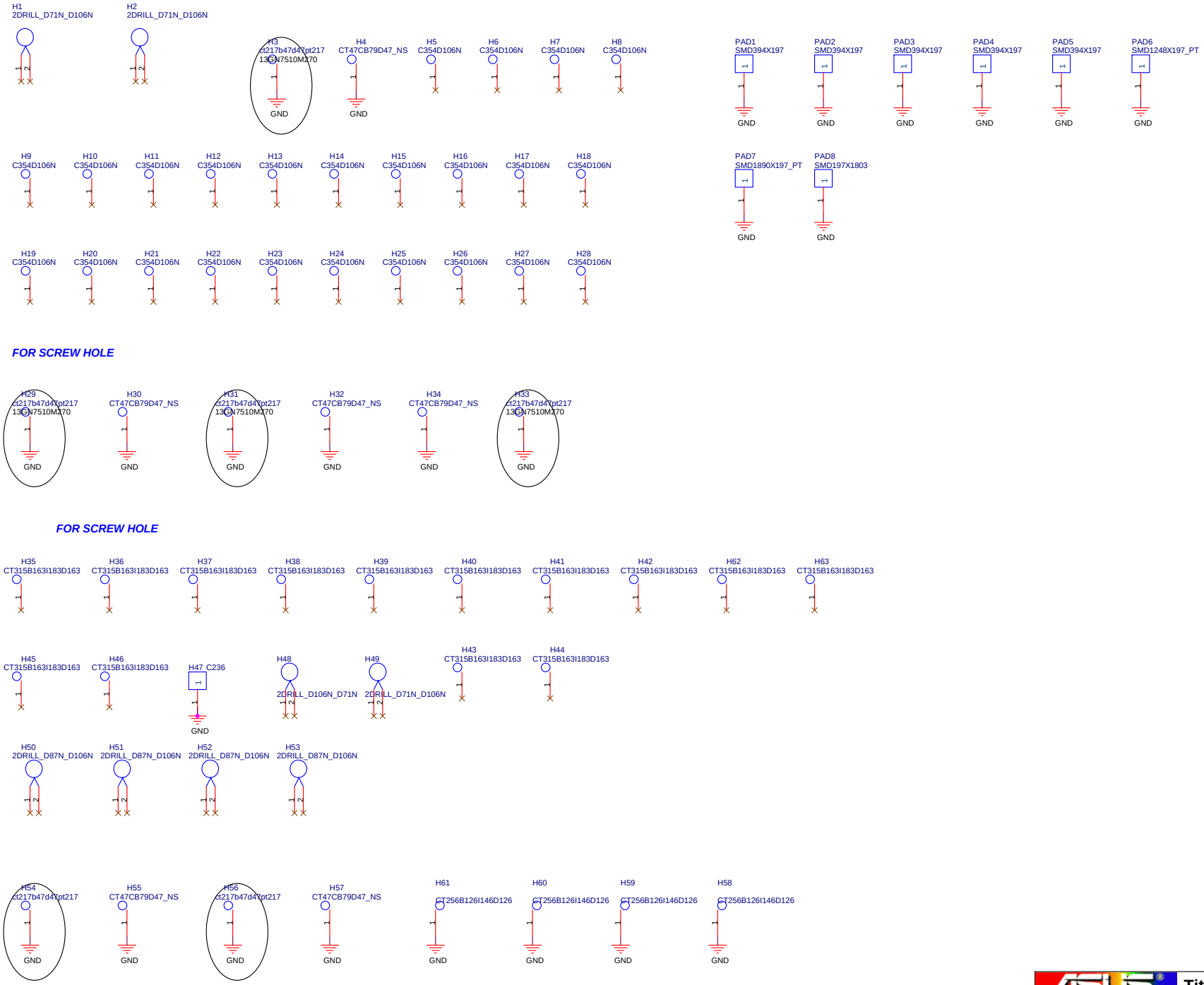
SATA HDD

ODD



ASUSTeK COMPUTER INC. NB1	Title : SATA-HDD & ODD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 72 of 92	

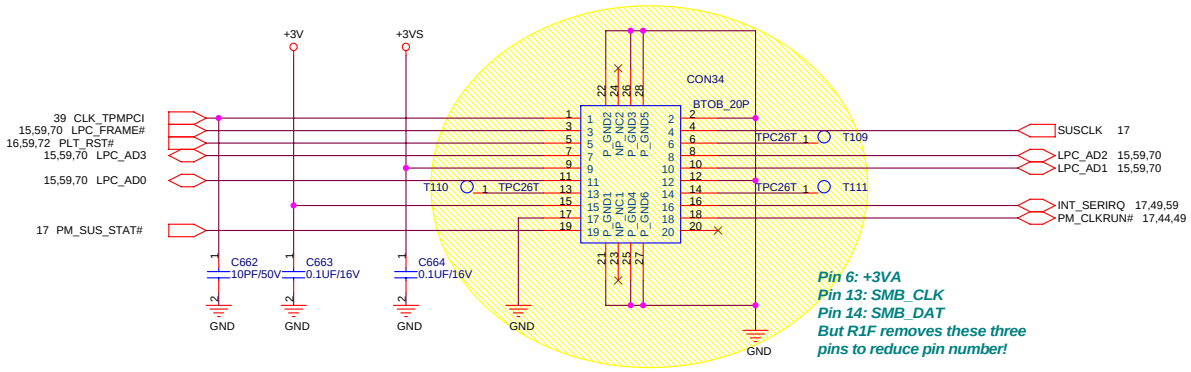
Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 73 of 92



ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: ALan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 74 of 92	

Title :	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 75 of 92

For TPM Module

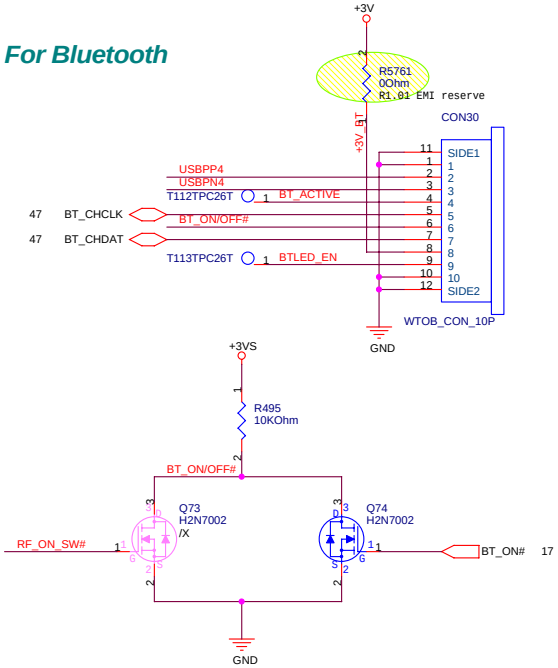


Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

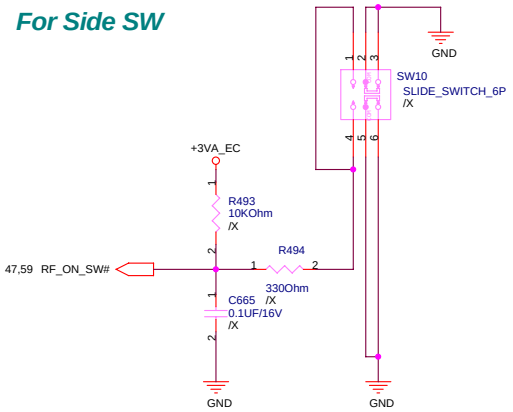
ASUSTeK COMPUTER INC	Title : TPM		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96J		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 76 of 92		

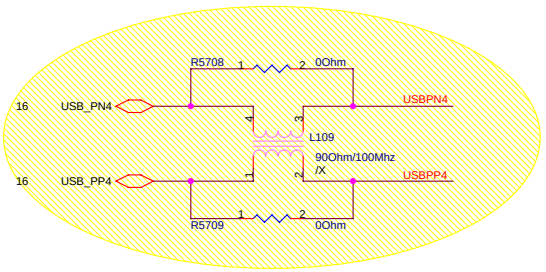
Title:	Schematic page name
ASUSTeK COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96J
Rev: 1.0	
Date: Tuesday, January 10, 2006	Sheet 77 of 92

For Bluetooth



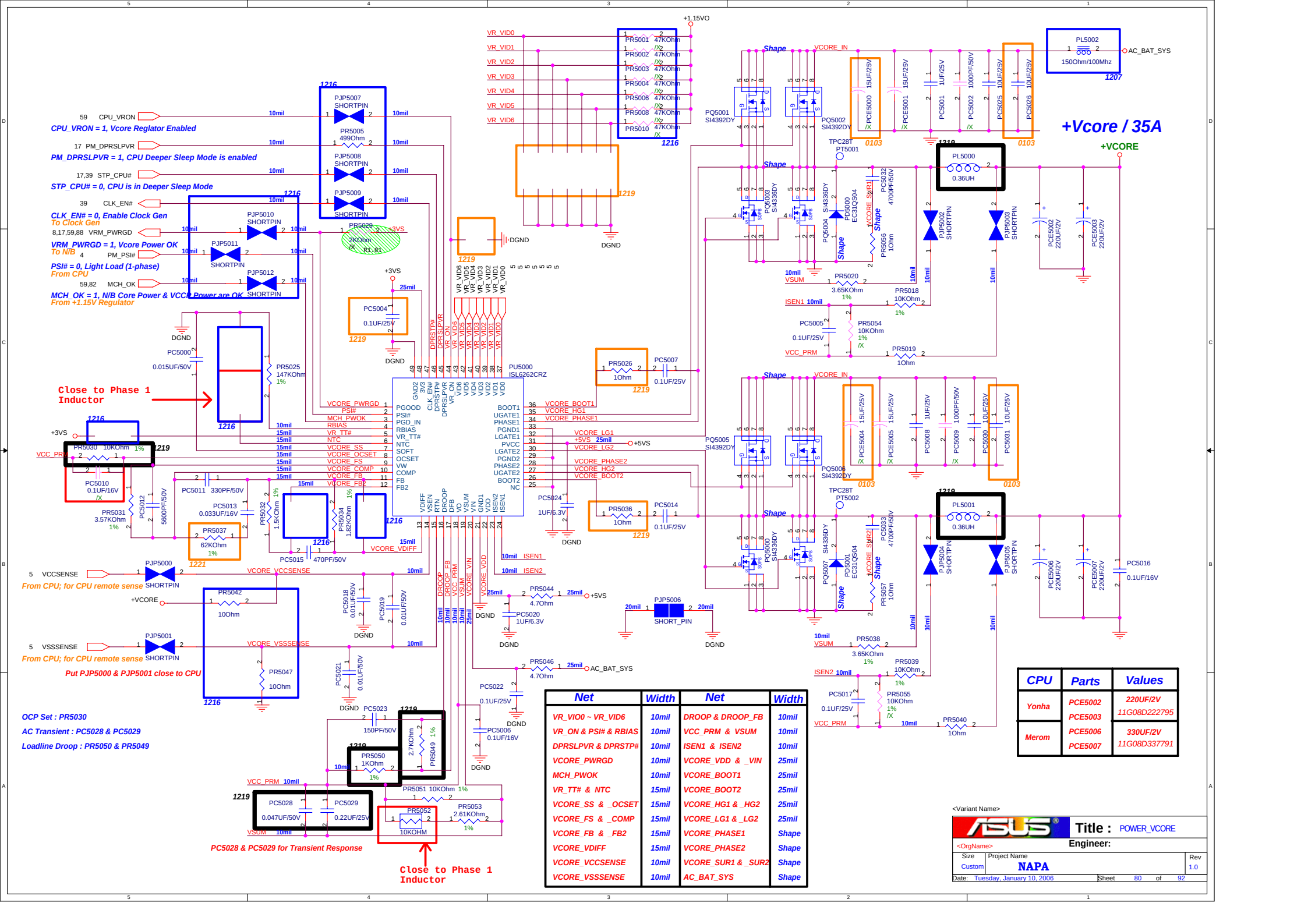
For Side SW





ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 78 of 92	

ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Alan Chu*	
Size: Custom	Project Name: Z96J	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 79 of 92	



Net	Width	Net	Width
VR_VIO0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape

CPU	Parts	Values
Yonha	PCE5002	220UF/2V
	PCE5003	11G08D222795
Merom	PCE5006	330UF/2V
	PCE5007	11G08D337791

<Variant Name>

Title : POWER_VCORE

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	1.0

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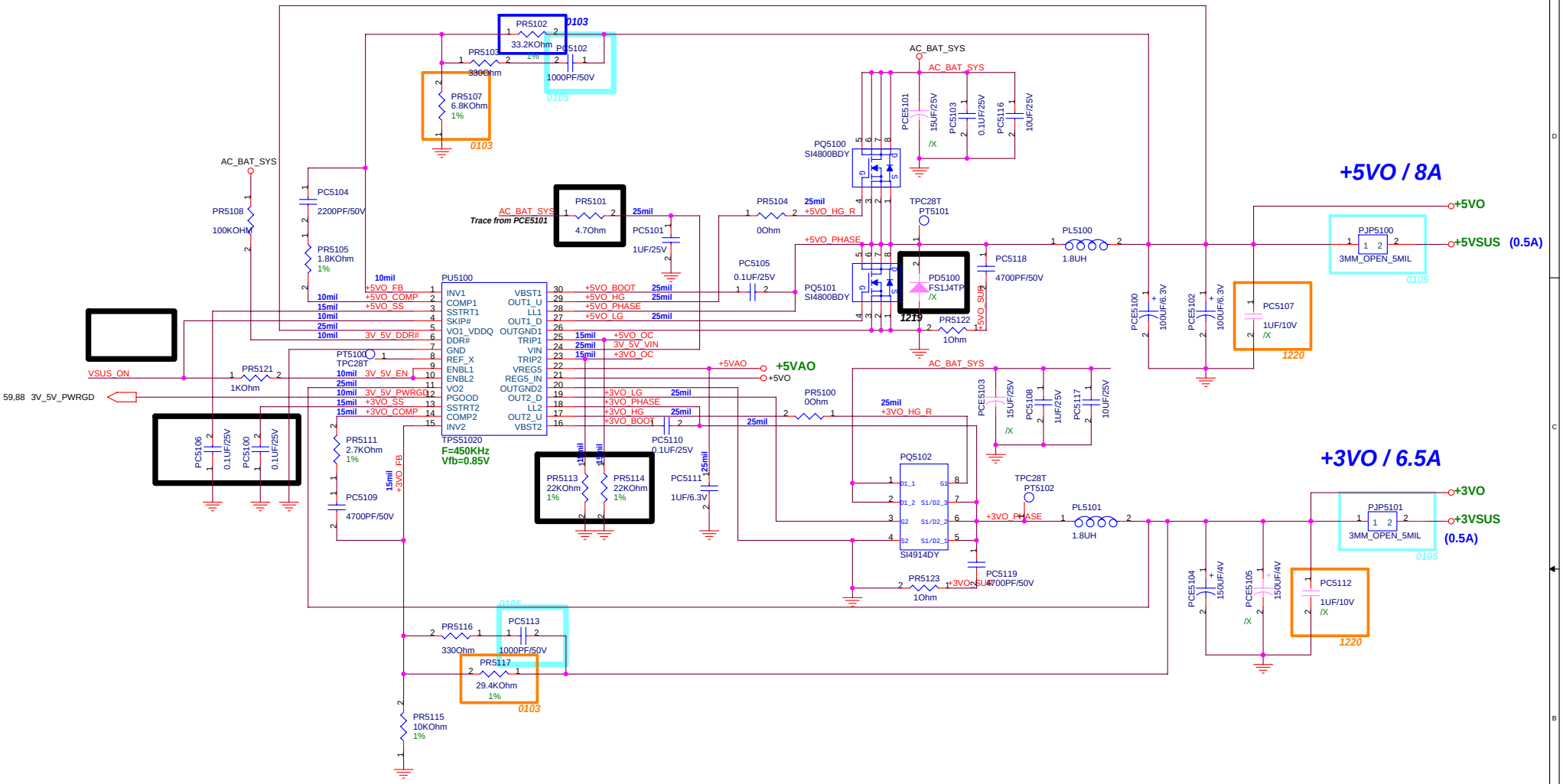
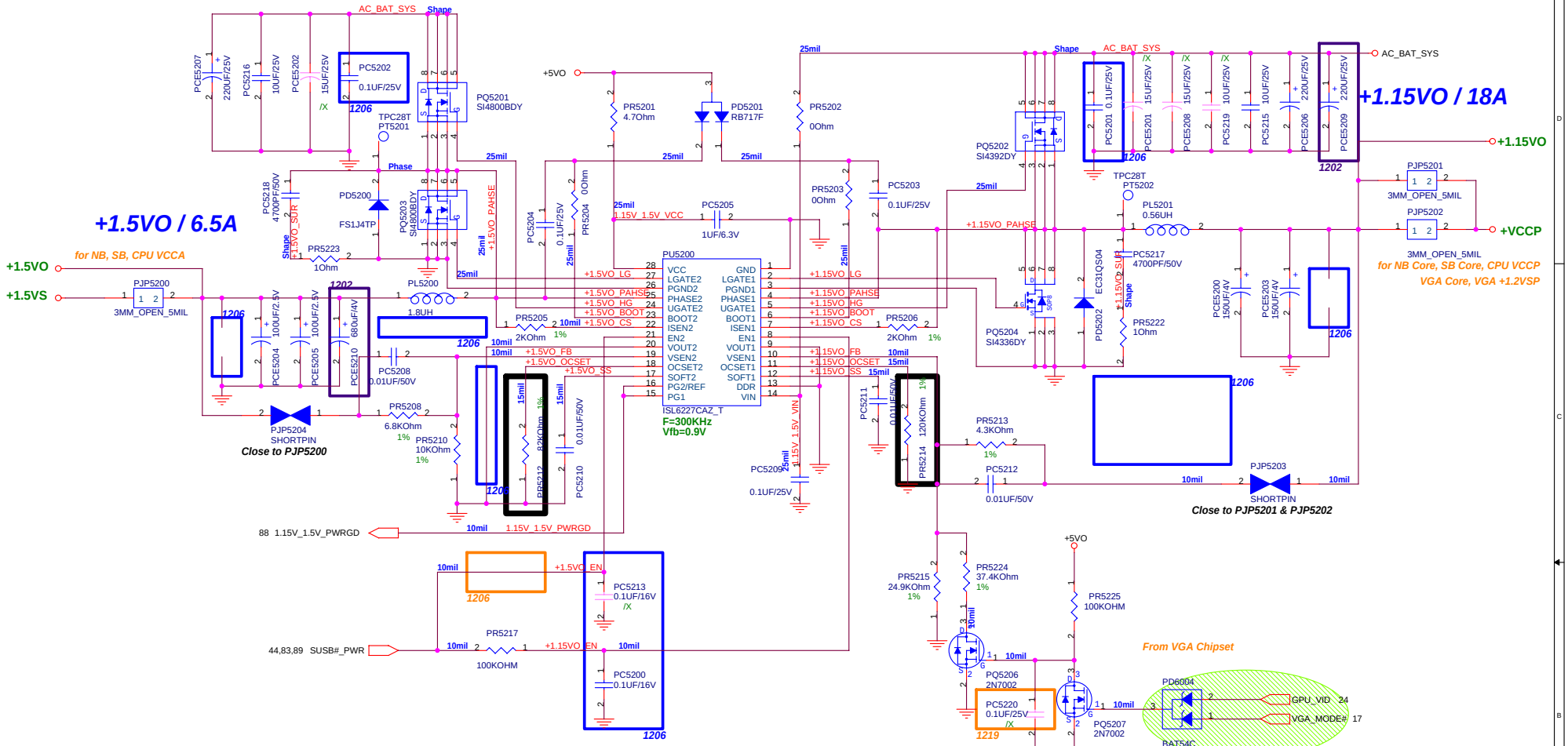


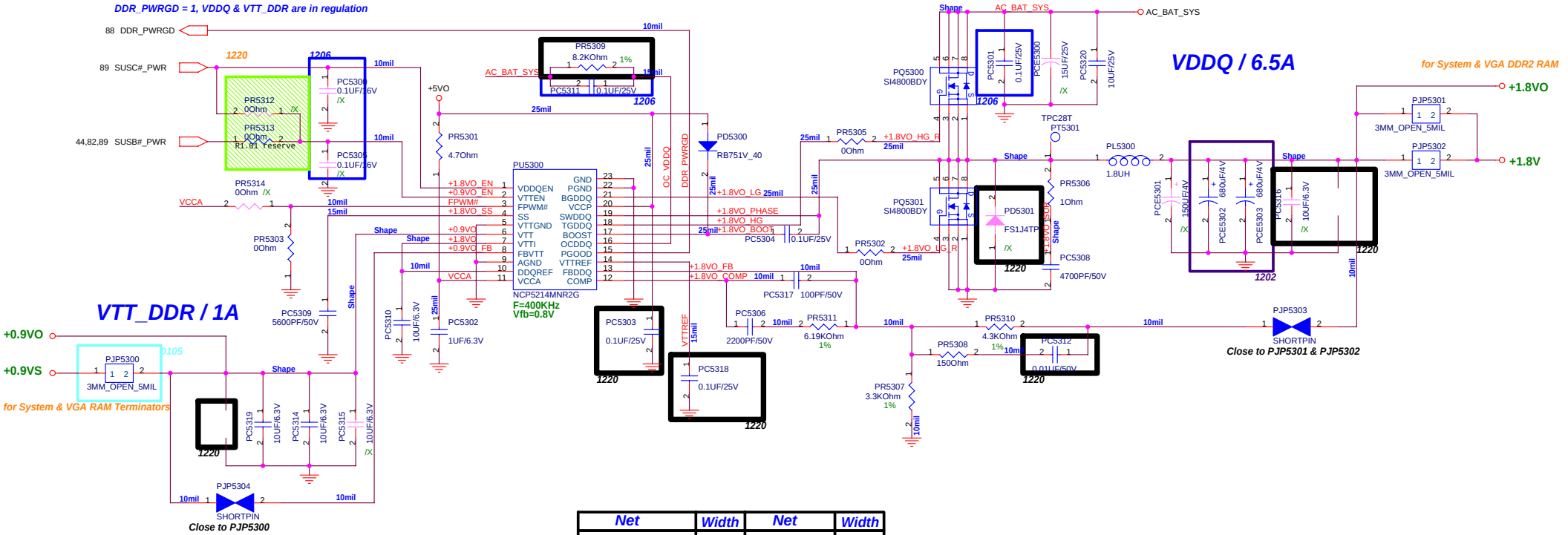
Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 81 of 92	



Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

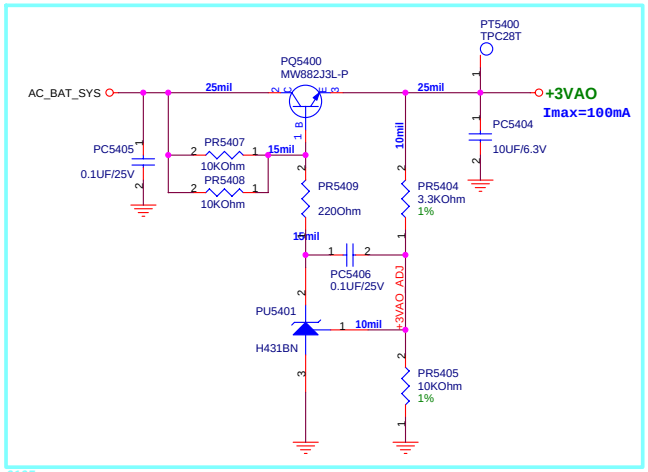
ASUS	Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 82 of 92		

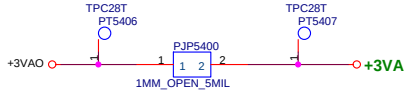


Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

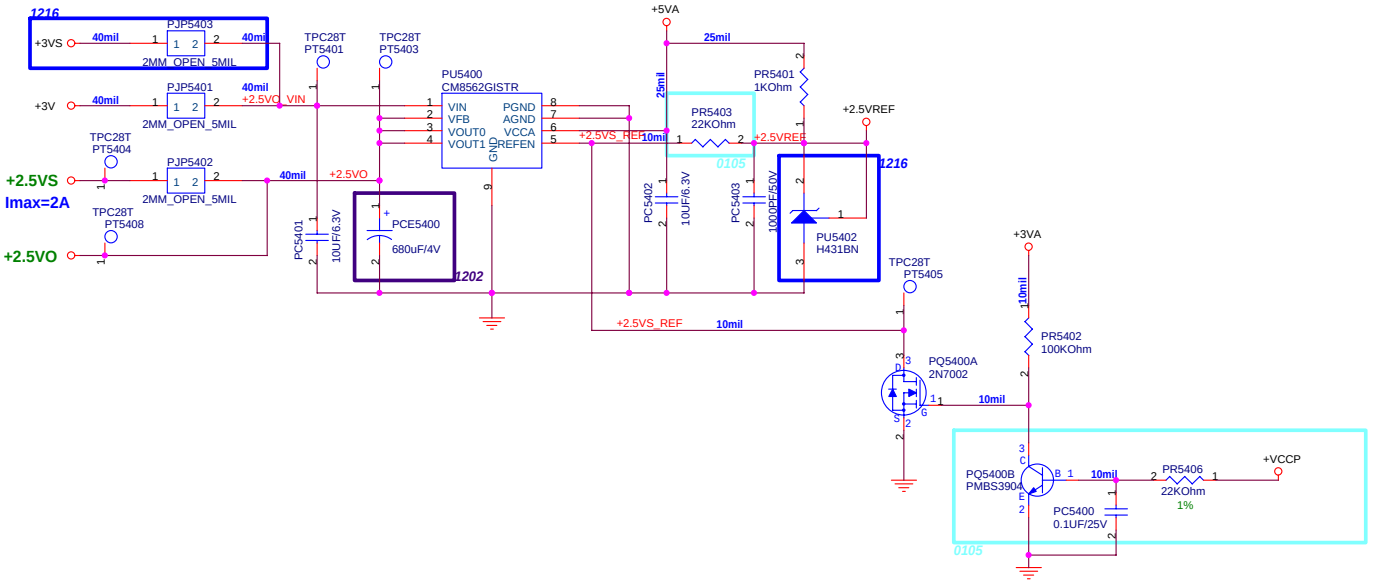
Title :	POWER_I/O_DDR & VTT		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 83 of 92		

+3VAO / 100mA





+2.5VS / 2A



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
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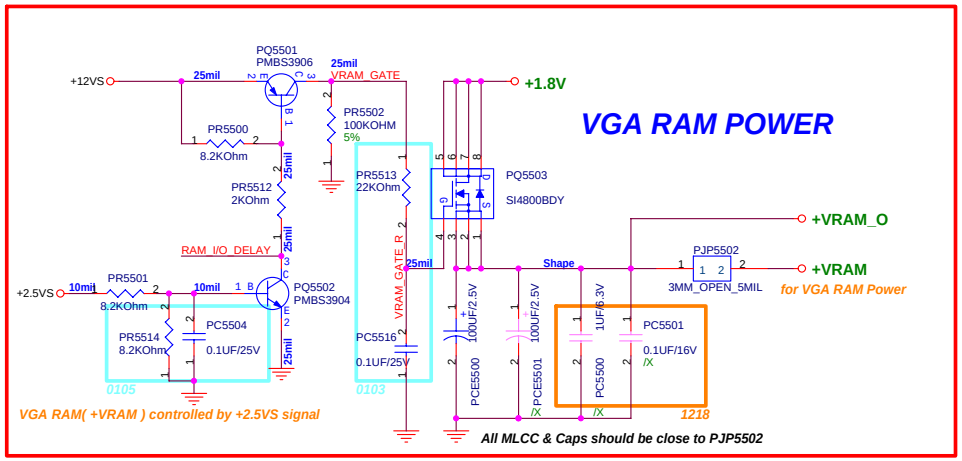
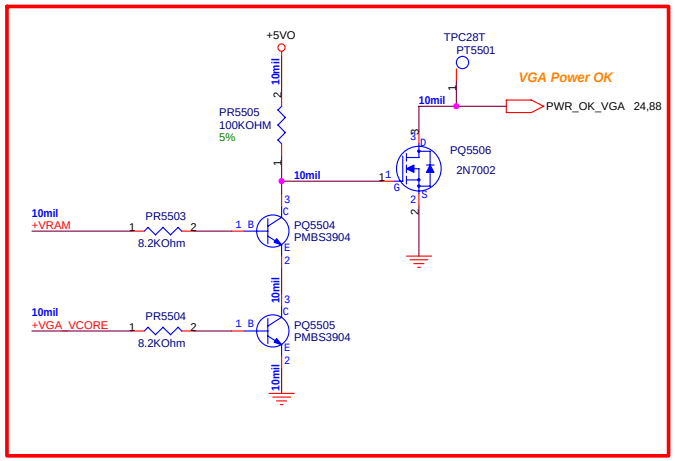
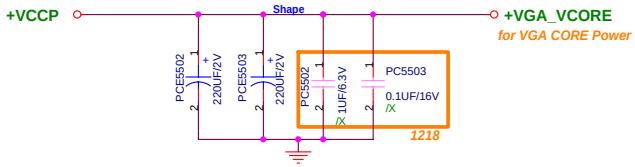
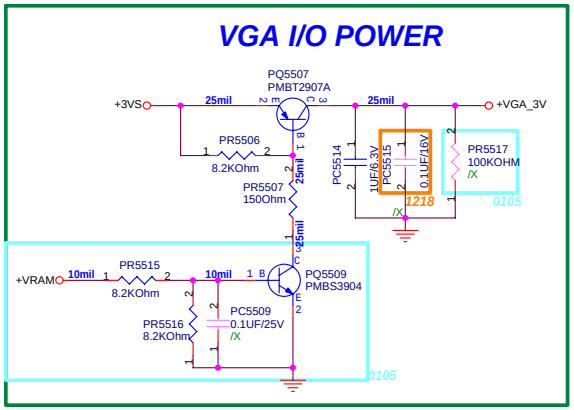




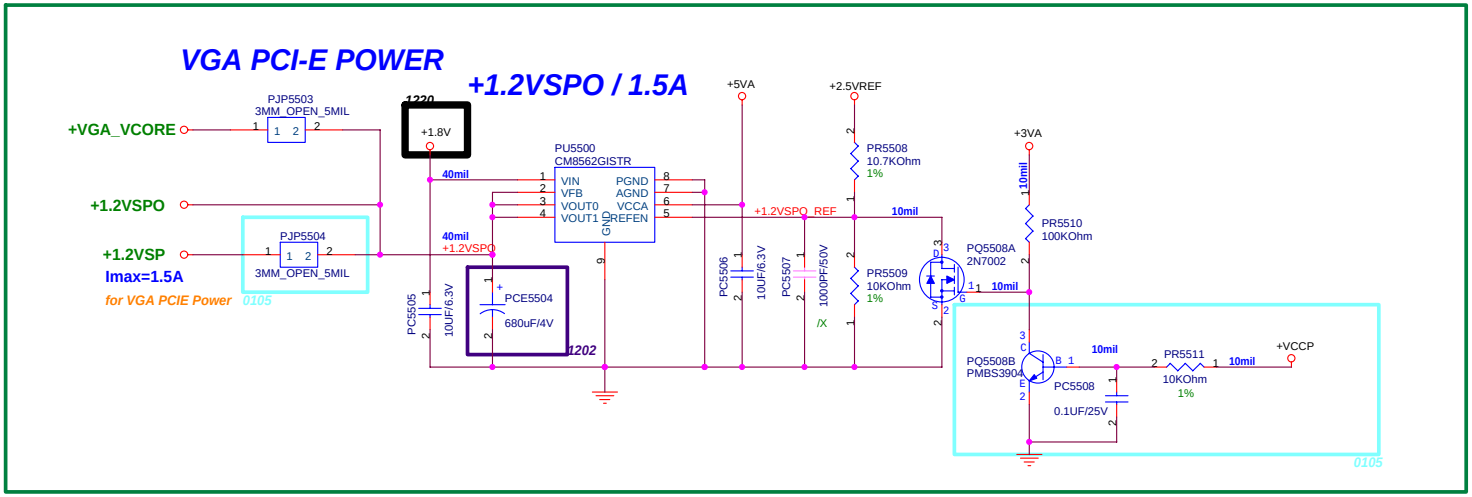
VGA CORE POWER



VGA I/O POWER



VGA PCI-E POWER



ASUS	Title : POWER_VGA_CORE & RAM	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
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POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R5710=20K,R5715=137K

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R5710=20K,R5715=42.2K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)= 25m Ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.588V
=> Vbatt = 4.2V

VICTL< 0.8V or DCIN < 7V -->Charger Disable

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725_REF : 4.2235V
MAX8725_LDO : 5.4V

Battery Charging Voltage :
+V_BAT= 4 x [4.2235+(Vvctl-1.8)/9.52]

Battery Charging Current :
Icharge=(0.075/PR5706) x (Victl/3.6))

Input Adaptor Max. Current Limit :
Ilimit_current=(0.075/PR5701) x (Vcls/4.2235)

Pre-Charging Mode :
Precharging current = 163.9mA
Victl = 0.098V

Battery Cell Selection :
BATSEL_2P# = 1, 6 Cells; Victl = 1.678V
=> Icharge = 2.331A
BATSEL_2P# = 0, 9 Cells; Victl = 2.785V
=> Icharge = 3.868A

Adaptor Max. Current :
PR5714 = 178K; Ilimit = 4.5A; 90W
PR5714 = 47K; Ilimit = 3.5A; 65W

Battery Voltage

BAT_IN_OC# = 1; Battery absence
BAT_IN_OC# = 0; Battery Plug-in

TS# = 1; Battery absence
TS# = 0; Battery Plug-in

BATSEL_2P# = 1, 6 Cells
BATSEL_2P# = 0, 9 Cells

PRECHG = 1, Pre-Charging Mode
Charging Current = 156mA

CHG_EN# = 1, Charger Disabled
CHG_EN# = 0, Charger Enabled

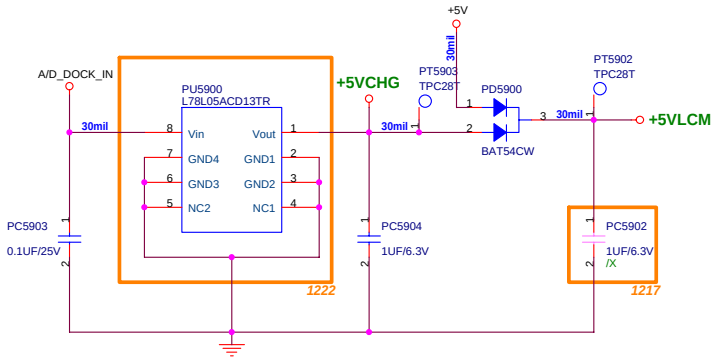
AC_APR_UC = 1, Adaptor is present
AC_APR_UC = 0, Adaptor is absent

BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

ASUS	Title :	POWER_CHARGER	
<OrgName>	Engineer:		
Size: C	Project Name: NAPA		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 86 of 92		

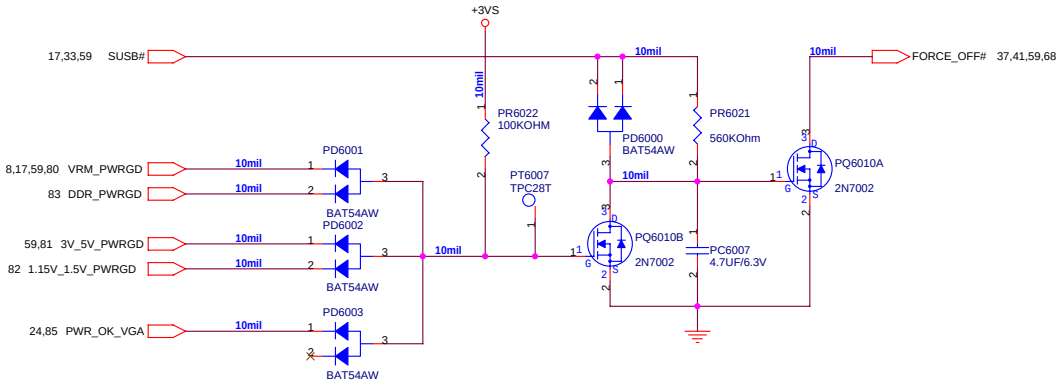
REMOVE BATTERY IN DETECT

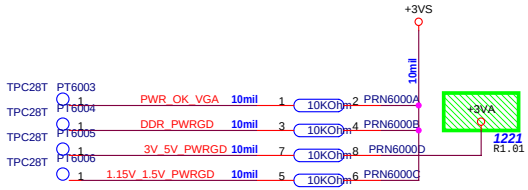
+5VLCM / +5VCHG



Title : POWER_DETECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 87 of 92	

Power Good Detecter





Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
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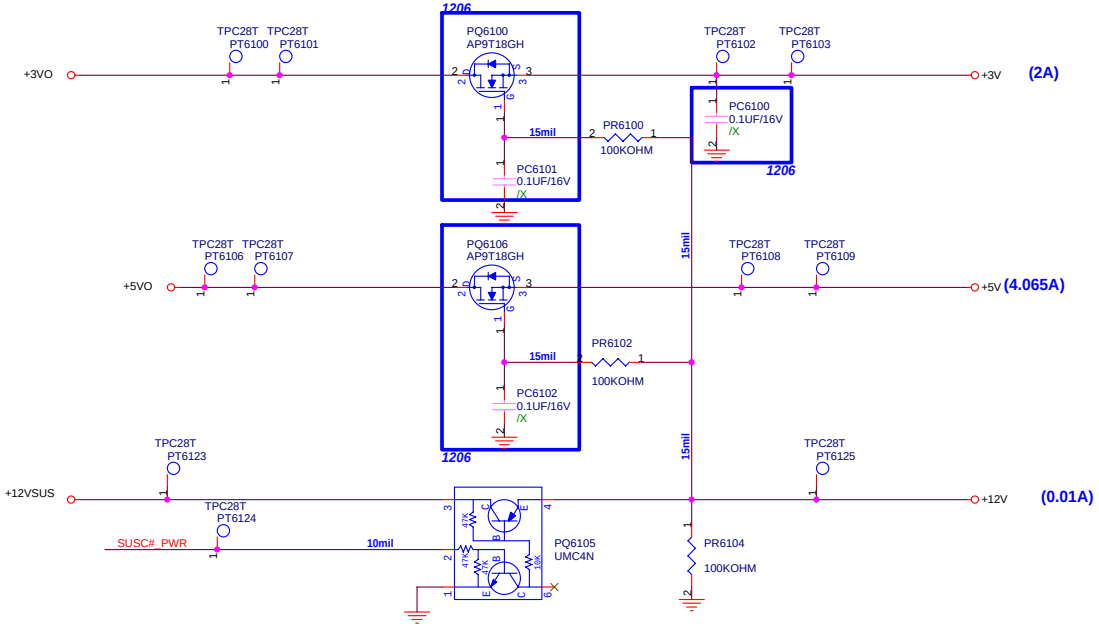
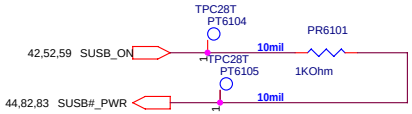
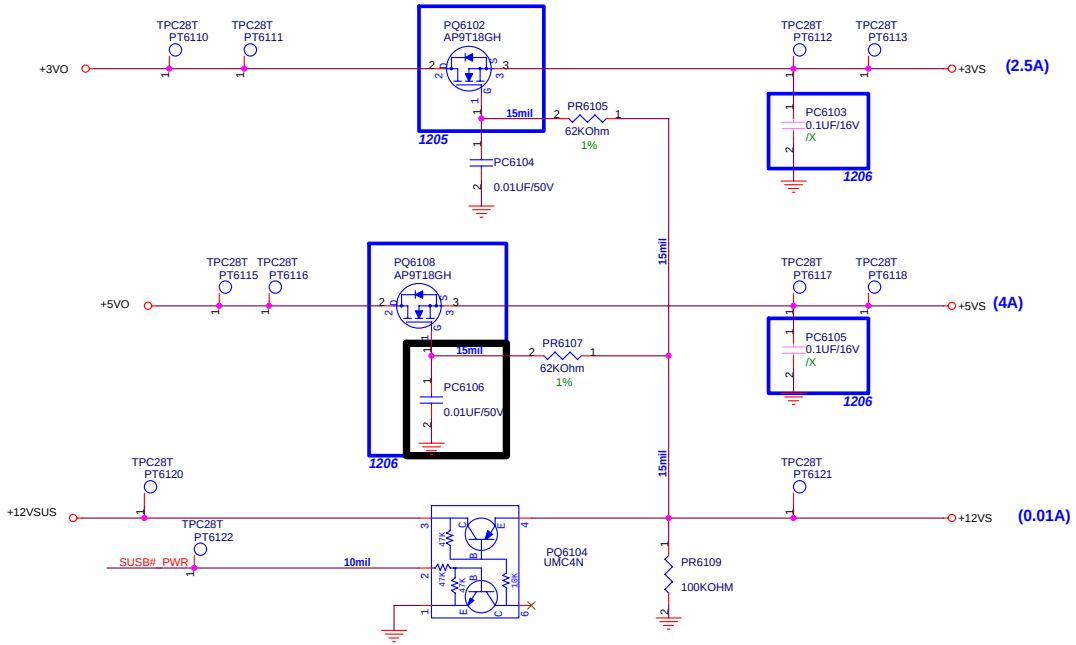
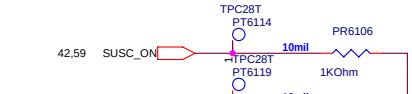
SUSC#_PWR POWER

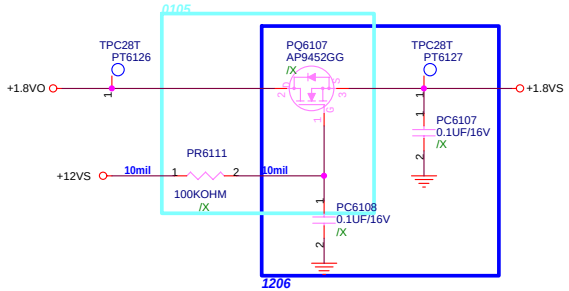




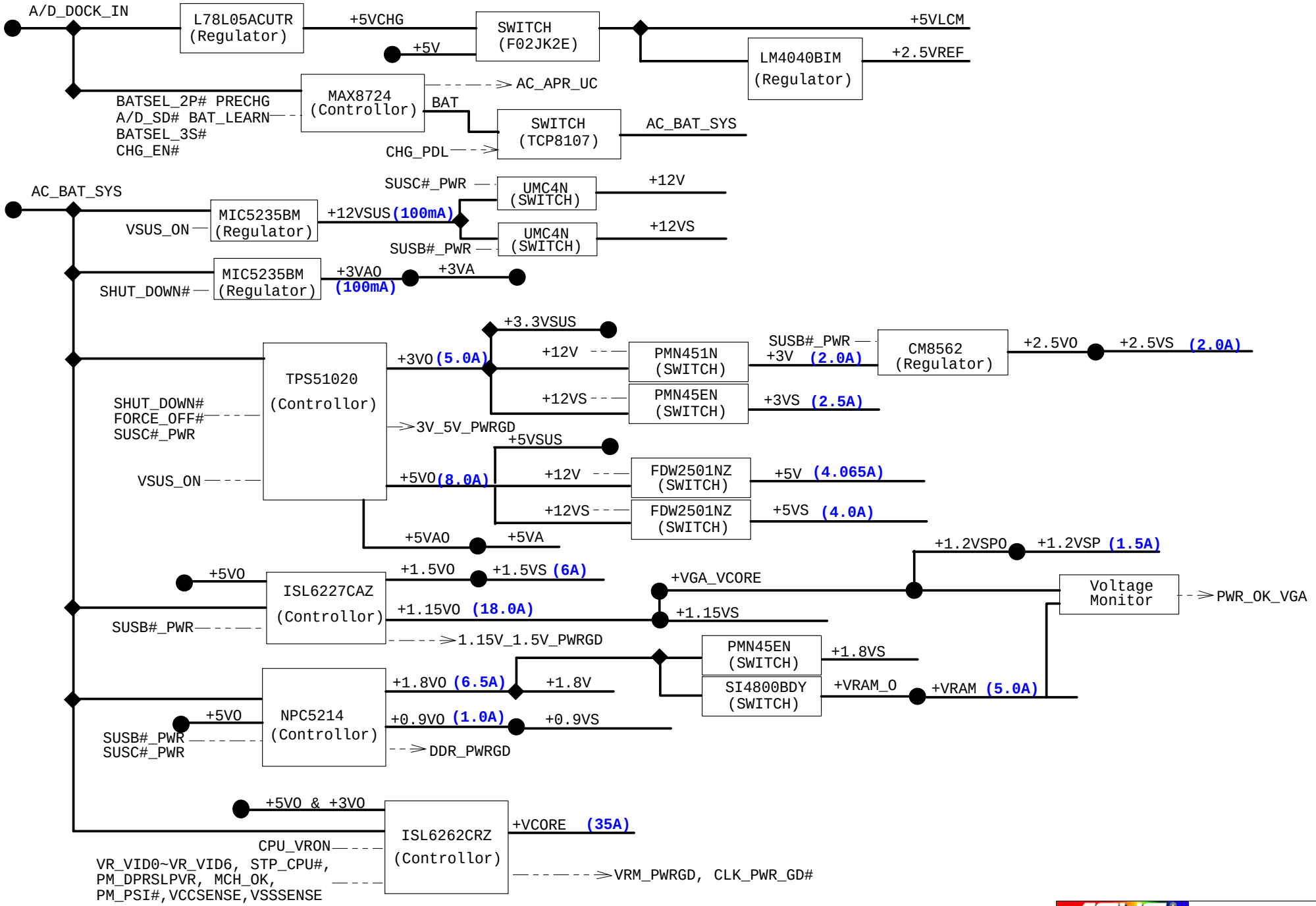
SUSB#_PWR POWER







ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 89 of 92	



Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
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Title : POWER_SIGNAL			
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 1.0
Date: Tuesday, January 10, 2006	Sheet 91 of 92		

Rev	Date	Description
1.0	10/04/05	1. Initial release.

Rev	Date	Description

ASUSTek COMPUTER INC

Title : History

Engineer: *Alan Chu*

Size	Project Name	Rev
Custom	Z96J	1.0

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