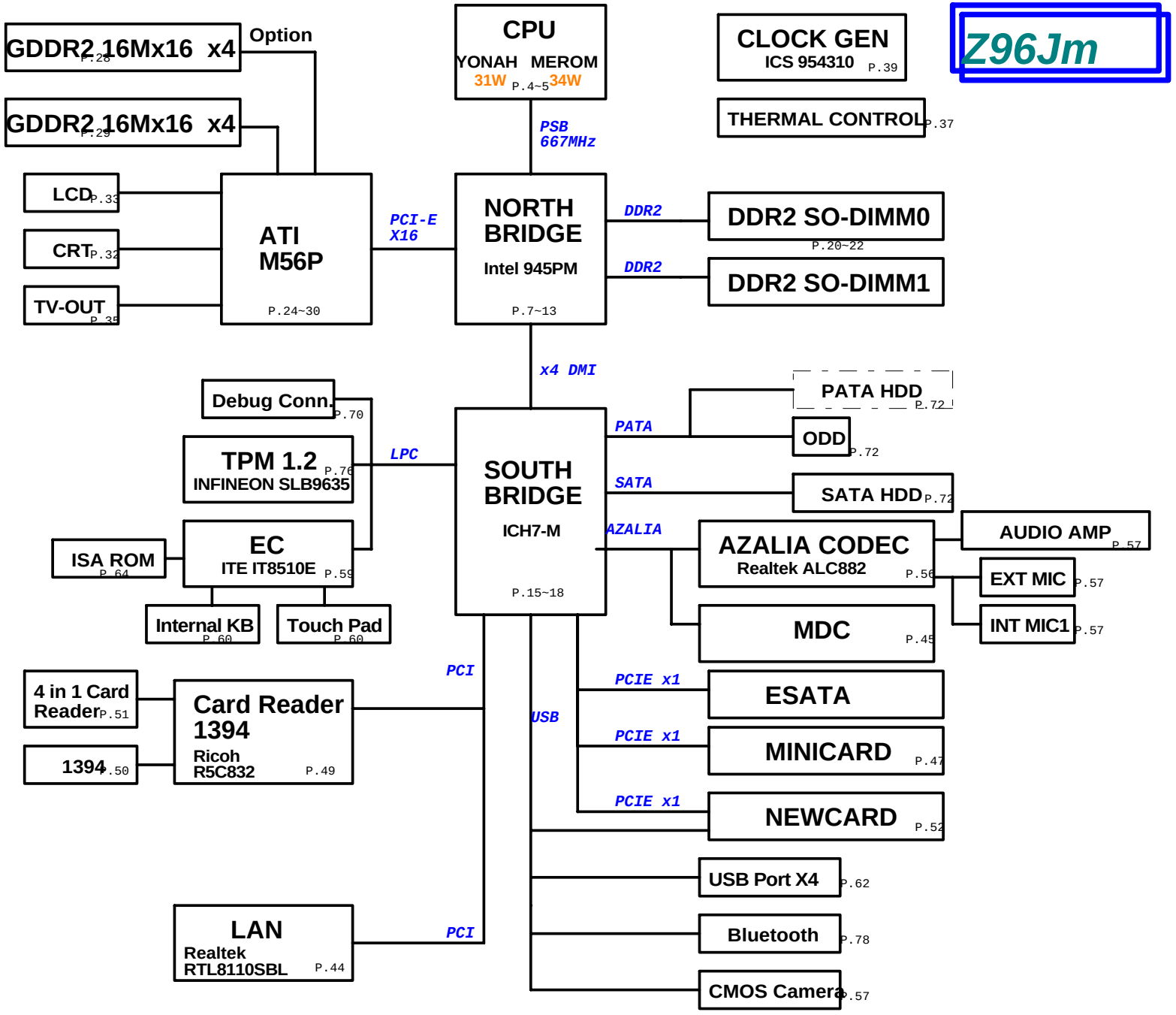

GDDR2 16Mx16 x4
P.28
Option
GDDR2 16Mx16 x4
P.29
LCD P.33
CRT P.32
TV-OUT P.35
ATI M56P
P.24~30
PCI-E X16
CPU
YONAH MEROM
31W 34W
P.4~5
PSB 667MHz
NORTH BRIDGE
Intel 945PM
P.7~13
DDR2
DDR2 SO-DIMM0
P.20~22
DDR2
DDR2 SO-DIMM1
CLOCK GEN
ICS 954310 P.39
THERMAL CONTROL P.37
Z96Jm
x4 DMI
Debug Conn. P.70
TPM 1.2
INFINEON SLB9635 P.76
LPC
EC
ITE IT8510E P.59
ISA ROM P.64
Internal KB P.60
Touch Pad P.60
SOUTH BRIDGE
ICH7-M
P.15~18
PATA
PATA HDD P.72
ODD P.72
SATA
SATA HDD P.72
AZALIA
AZALIA CODEC
Realtek ALC882 P.56
AUDIO AMP P.57
EXT MIC P.57
INT MIC1 P.57
MDC P.45
PCI
4 in 1 Card Reader P.51
1394 P.50
Card Reader 1394
Ricoh R5C832 P.49
USB
PCIE x1
ESATA
PCIE x1
MINICARD P.47
PCIE x1
NEWCARD P.52
USB Port X4 P.62
Bluetooth P.78
CMOS Camera P.57
PCI
LAN
Realtek RTL8110SBL P.44
Title : Block Diagram
ASUSTek Computer INC.
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 1 of 91

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4//GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

Pin	Pin Name	Signal Name	Type	Default	
48	GPH0	VSUS_ON	O	L	GPI
54	GPH1	VSUS_GD#	I	H	GPI
55	GPH2	CPUPWR_GD#	I	H	GPI
69	GPH3	PM_PWRBTN#	O	H	GPI
70	GPH4	SUSC_ON	O	L	GPI
75	GPH5	SUSB_ON	O	L	GPI
76	GPH6	CPU_VRON	O	L	GPI
105	GPH7	PM_RSMRST#	O	L	GPI
148	GPI0	ICH7_PWROK	O	L	GPI
149	GPI1	/	O		GPI
152	GPI2	MCHOK	I	L	GPI
155	GPI3	CHG_EN#	O	H	GPI
156	GPI4	PRECHG	O	L	GPI
168	GPI5	BAT_LL#	O	H	GPI
174	GPI6	BAT_LEARN	O	L	GPI
93	ADC8	KID0	I		
94	ADC9	KID1	I		
101	DAC2	BL_PWM_DA	O		
102	DAC3	BATSEL_2P#	O		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0100110X (98)

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

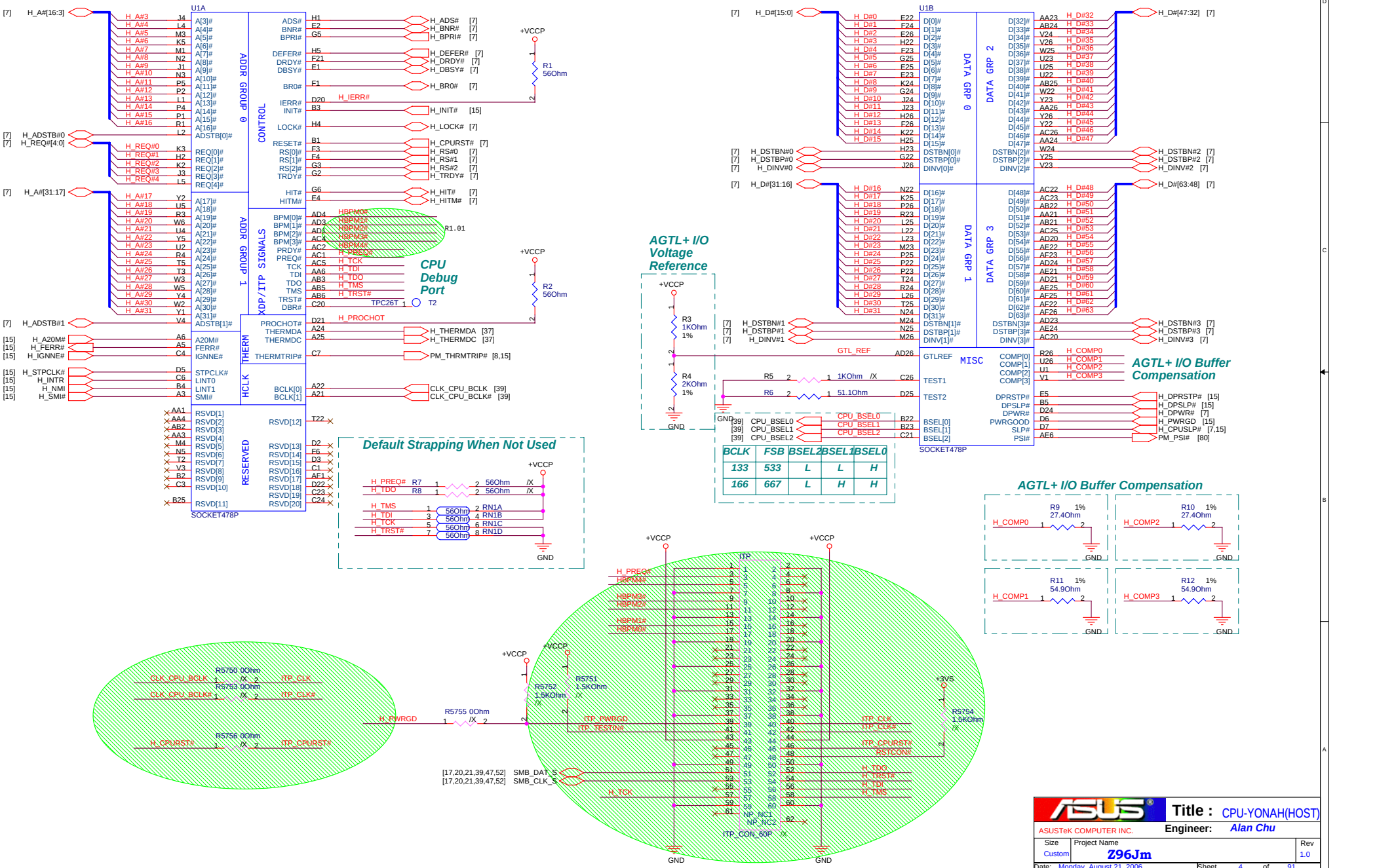
ASUSTek Computer INC.

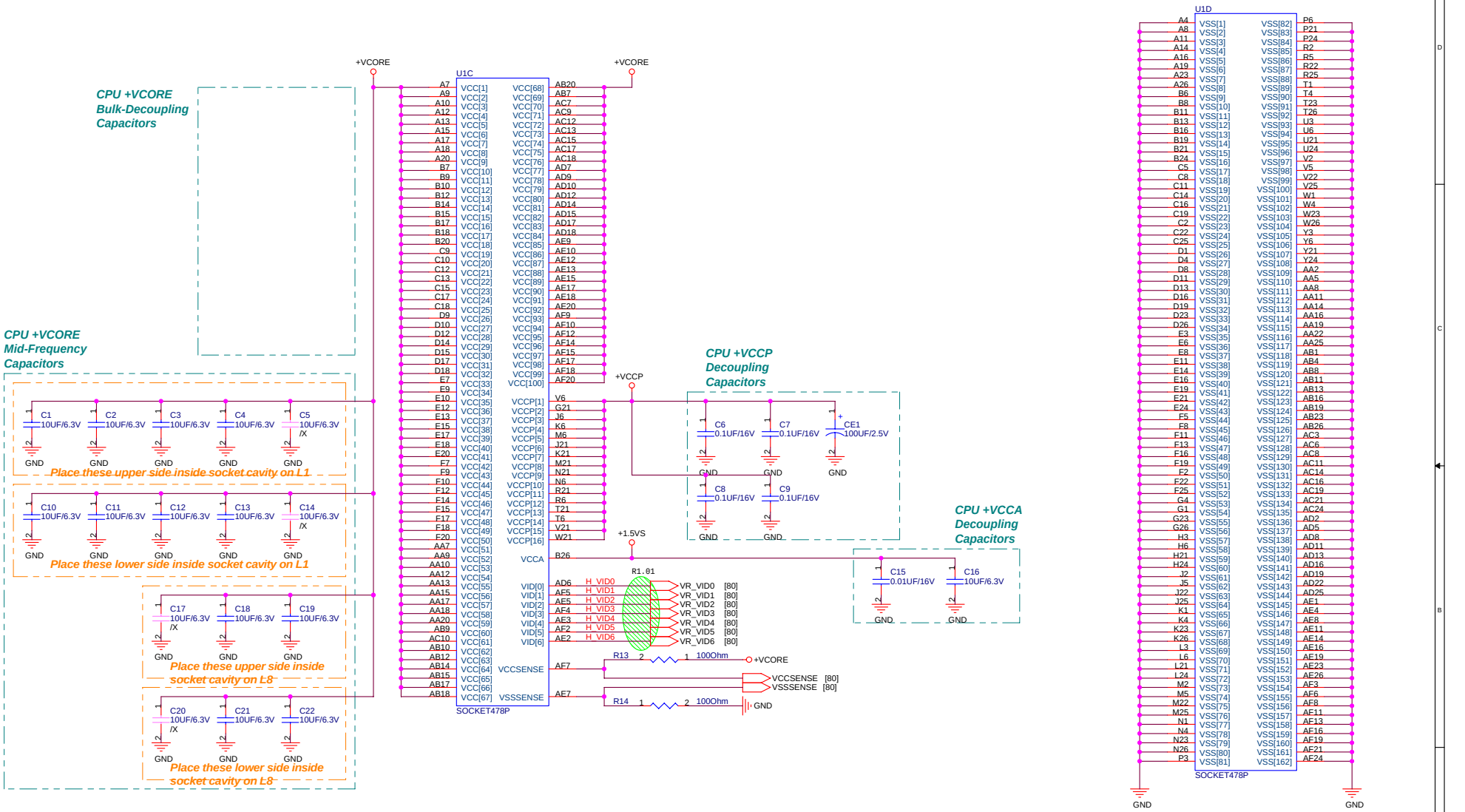
Title : <Title>

Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

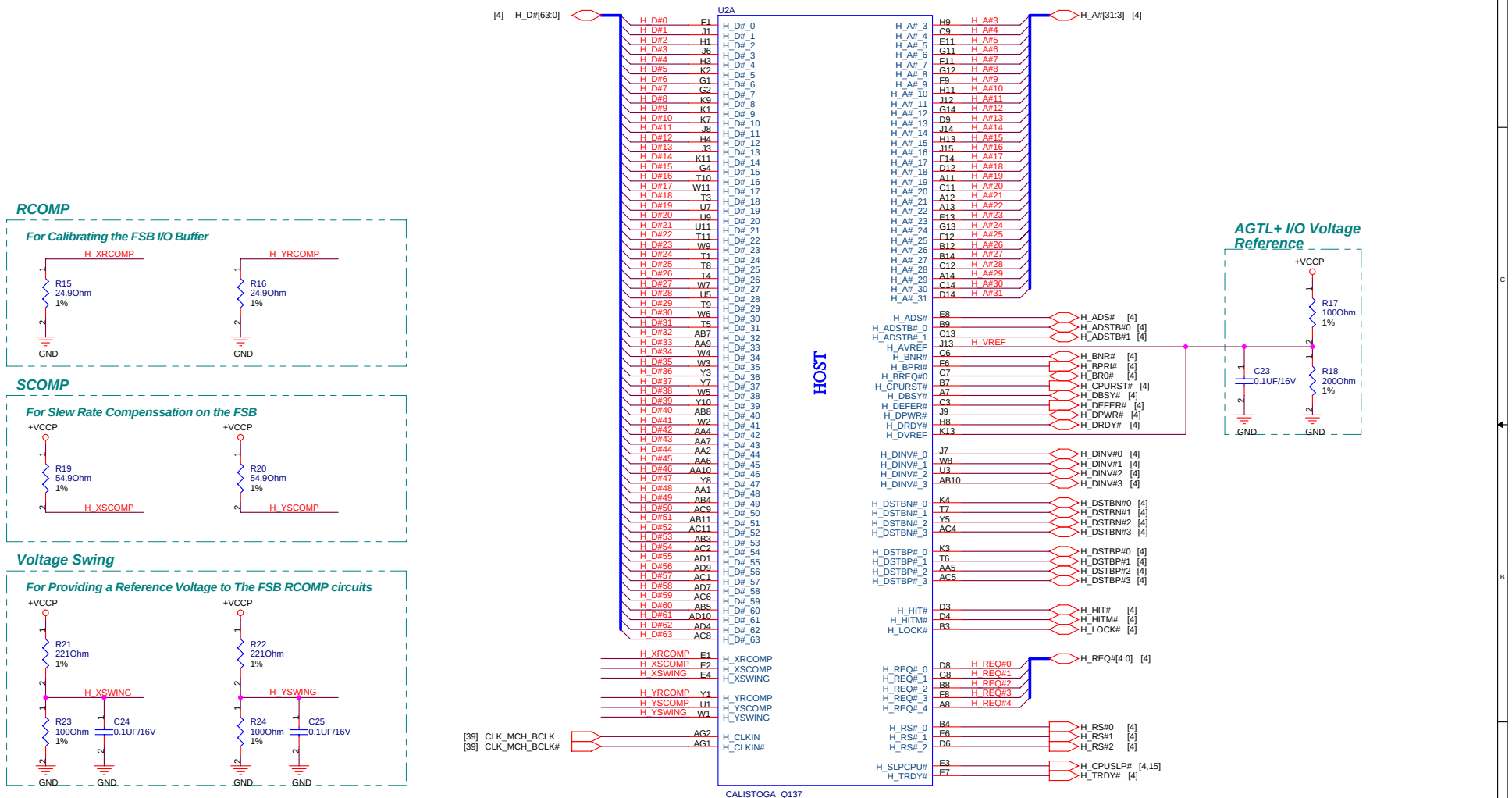
Date: Monday, August 21, 2006 Sheet 2 of 91


U1A
U1B
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
HCLK
RESERVED
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478P
CPU Debug Port
AGTL+ I/O Voltage Reference
AGTL+ I/O Buffer Compensation
Default Strapping When Not Used
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
ITP
Title : CPU-YONAH(HOST)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 4 of 91



+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*R1F: 10UF *16*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*

ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 5 of 91	



ASUSTeK COMPUTER INC.	Title : NB-945PM(HOST)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 7 of 91	

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — 1 — R25 /X — 2 — 1KOhm — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — 1 — R26 /X — 2 — 1KOhm — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable

1 = Normal Operation (D)

MCH_CFG_15 — 1 — R27 /X — 2 — 1KOhm — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — 1 — R30 — 2 — 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — 1 — R31 /X — 2 — 1KOhm — GND

CFG10 : HOST PLL VCO Select

0 = Reserved

1 = Mobility (D)

MCH_CFG_10 — 1 — R34 /X — 2 — 1KOhm — GND

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+2.5VS

MCH_CFG_18 — 1 — R35 /X — 2 — 1KOhm

CFG11 : PSB 4x CLK Enable

0 = 4x Enable

1 = 8x Enable (D)

MCH_CFG_11 — 1 — R37 /X — 2 — 1KOhm — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

+2.5VS

MCH_CFG_19 — 1 — R38 /X — 2 — 1KOhm — GND

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

U2B

RSVD: T32 RSVD_1, R32 RSVD_2, F3 RSVD_3, E7 RSVD_4, AG11 RSVD_5, AF11 RSVD_6, H7 RSVD_7, J19 RSVD_8, K30 TV_DCONSEL_0, J29 TV_DCONSEL_1, A41 RSVD_11, A35 RSVD_12, A34 RSVD_13, D28 RSVD_14, D27 RSVD_15

CFG: [39] MCH_BSEL0 → K16 CFG_0; [39] MCH_BSEL1 → K18 CFG_1; [39] MCH_BSEL2 → J18 CFG_2; F18 CFG_3; E15 CFG_4; MCH_CFG_5 → F15 CFG_5; MCH_CFG_7 → E18 CFG_6; D19 CFG_7; MCH_CFG_9 → D16 CFG_8; MCH_CFG_10 → G16 CFG_9; MCH_CFG_11 → E16 CFG_10; D15 CFG_11; G15 CFG_12; K15 CFG_13; C15 CFG_14; MCH_CFG_15 → H16 CFG_15; MCH_CFG_16 → G18 CFG_16; H15 CFG_17; MCH_CFG_18 → J25 CFG_18; MCH_CFG_19 → K27 CFG_19; J26 CFG_20

PM: +3VS; [17] PM_BMBUSY# → G28 PM_BMBUSY#; R32 2 10KOhm r0402 1 → PM_EXTTS# 0 → F25 PM_EXTTS#_0; R33 2 10KOhm r0402 1 → PM_EXTTS# 1 → H26 PM_EXTTS#_1; [4,15] PM_THRMTRIP# → G6 PM_THRMTRIP#; [17,59,80,88] VRM_PWRGD → AH33 PWROK; [16,17,26,47,52] BUF_PLT_RST# → R36 1 — 2 100Ohm RST_IN_MCH# → AH34 RSTIN#

MISC: [16] MCH_ICH_SYNC# → H28 SDVO_CTRLCLK, H27 SDVO_CTRLDATA, K28 ICH_SYNC#, H32 CLK_REQ#

NC: D1, C41, C1, BA41, BA40, BA39, BA3, BA2, BA1, B41, B2, AY41, AY1, AW41, AW1, A40, A4, A39, A3 → NC0 … NC18

CALISTOGA_Q137

DDR MUXING:

SM_CK_0 AY35 — M_CLK_DDR0 [20]
SM_CK_1 AR1 — M_CLK_DDR1 [20]
SM_CK_2 AW7 — M_CLK_DDR2 [21]
SM_CK_3 AW40 — M_CLK_DDR3 [21]

SM_CK#_0 AW35 — M_CLK_DDR#0 [20]
SM_CK#_1 AT1 — M_CLK_DDR#1 [20]
SM_CK#_2 AY7 — M_CLK_DDR#2 [21]
SM_CK#_3 AY40 — M_CLK_DDR#3 [21]

SM_CKE_0 AU20 — M_CKE0 [20,22]
SM_CKE_1 AT20 — M_CKE1 [20,22]
SM_CKE_2 BA29 — M_CKE2 [21,22]
SM_CKE_3 AY29 — M_CKE3 [21,22]

SM_CS#_0 AW13 — M_CS#0 [20,22]
SM_CS#_1 AW12 — M_CS#1 [20,22]
SM_CS#_2 AY21 — M_CS#2 [21,22]
SM_CS#_3 AW21 — M_CS#3 [21,22]

SM_OCDCOMP_0 AL20
SM_OCDCOMP_1 AF10

SM_ODT_0 BA13 — M_ODT0 [20,22]
SM_ODT_1 BA12 — M_ODT1 [20,22]
SM_ODT_2 AY20 — M_ODT2 [21,22]
SM_ODT_3 AU21 — M_ODT3 [21,22]

+1.8V
SM_RCOMP# AV9 — R28 1 — 2 80.6Ohm 1%
SM_RCOMP AT9 — R29 1 — 2 80.6Ohm 1%
GND

SM_VREF_0 AK1
SM_VREF_1 AK41 — M_VREF_MCH → M_VREF_MCH [20,21,22]

CLK:

G_CLKIN# AF33 — CLK_MCH_3GPLL# [39]
G_CLKIN AG33 — CLK_MCH_3GPLL [39]
D_REFCLKIN# A27
D_REFCLKIN A26 — D_REFCLKIN
D_REFSSCLKIN# C40
D_REFSSCLKIN D41 — D_REFSSCLKIN
GND

DMI:

DMI_RXN_0 AE35 — DMI_TXN0
DMI_RXN_1 AE39 — DMI_TXN1
DMI_RXN_2 AG35 — DMI_TXN2
DMI_RXN_3 AH39 — DMI_TXN3 → DMI_TXN[3:0] [16]

DMI_RXP_0 AC35 — DMI_TXP0
DMI_RXP_1 AE39 — DMI_TXP1
DMI_RXP_2 AE35 — DMI_TXP2
DMI_RXP_3 AG39 — DMI_TXP3 → DMI_TXP[0..3] [16]

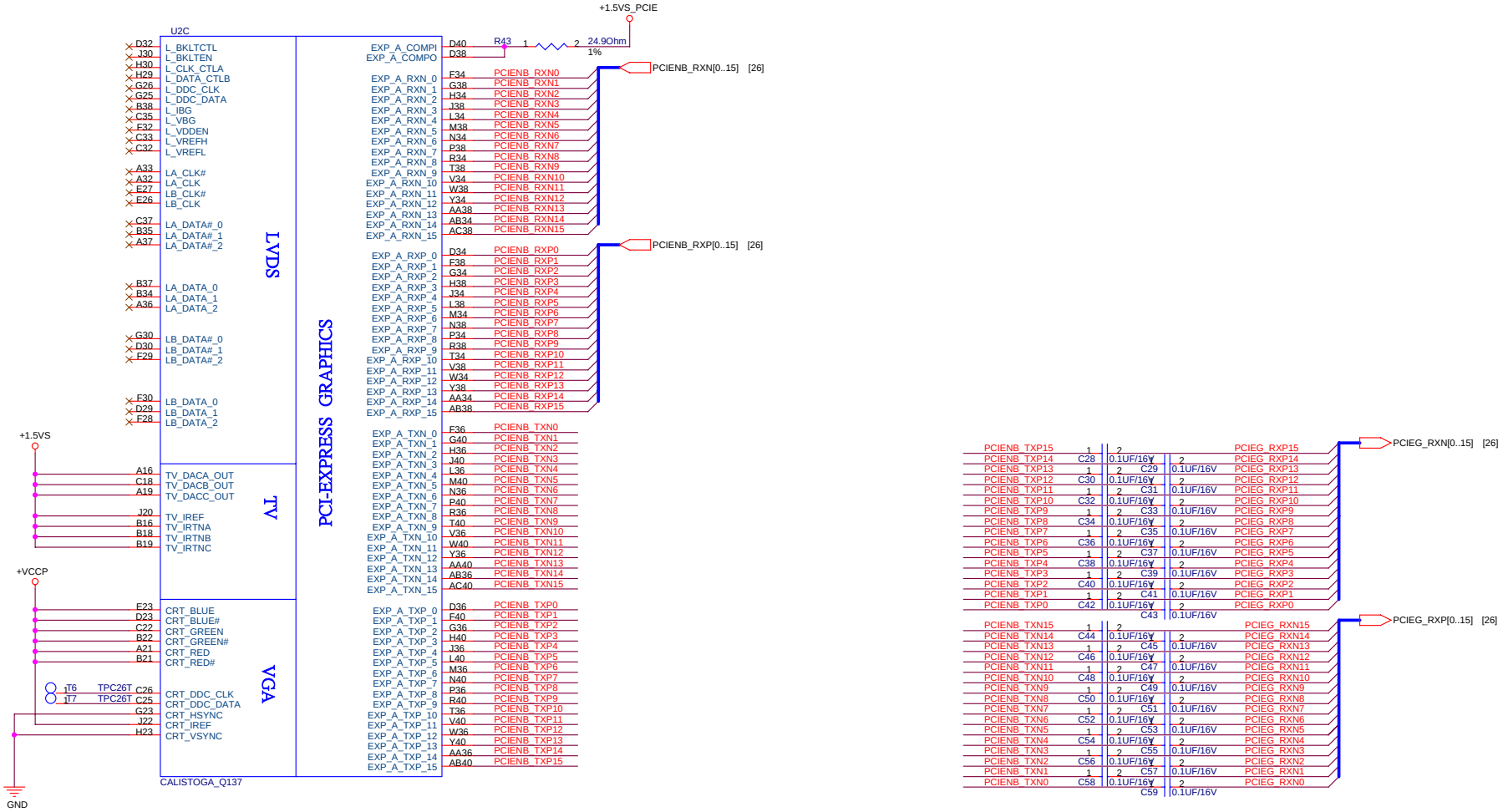
DMI_TXN_0 AE37 — DMI_RXN0
DMI_TXN_1 AE41 — DMI_RXN1
DMI_TXN_2 AG37 — DMI_RXN2
DMI_TXN_3 AH41 — DMI_RXN3 → DMI_RXN[0..3] [16]

DMI_TXP_0 AC37 — DMI_RXP0
DMI_TXP_1 AE41 — DMI_RXP1
DMI_TXP_2 AE37 — DMI_RXP2
DMI_TXP_3 AG41 — DMI_RXP3 → DMI_RXP[0..3] [16]

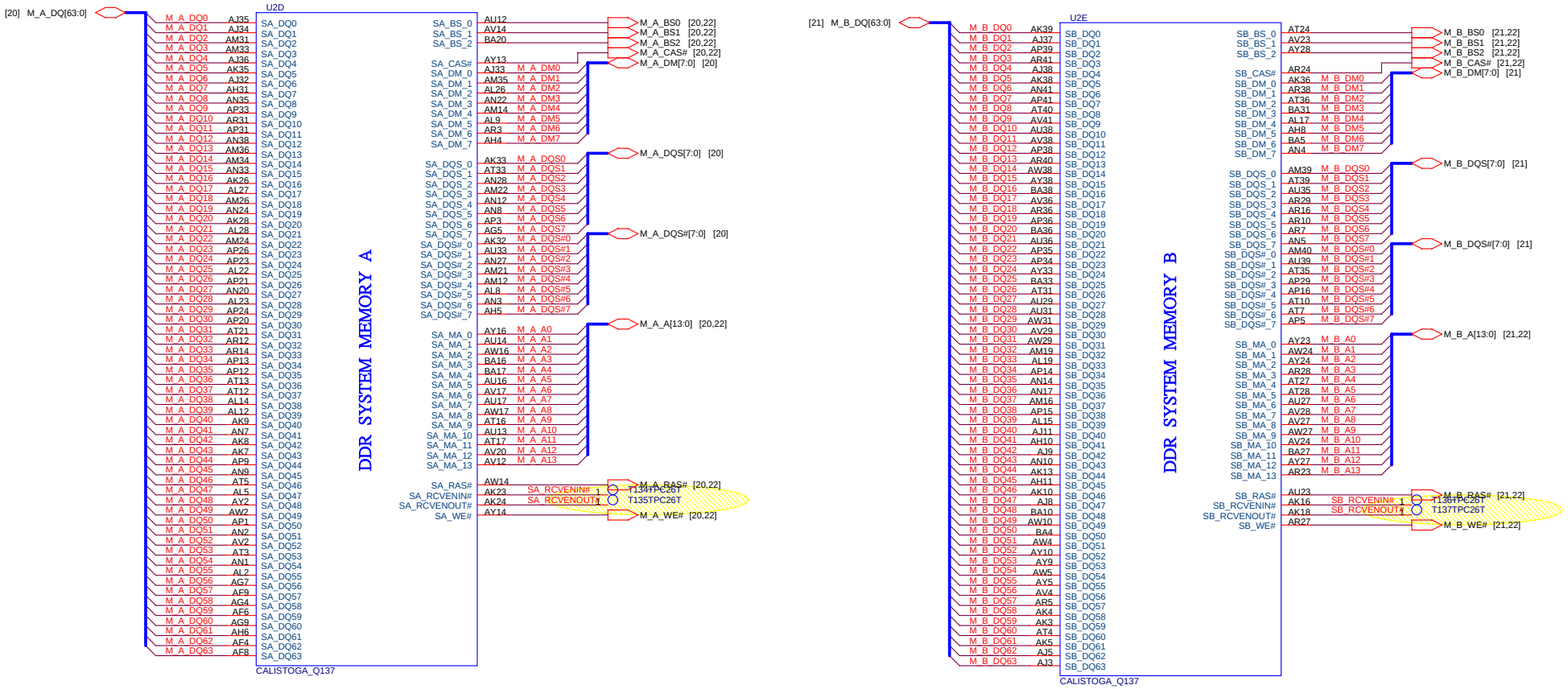
+1.5VS — R39 10KOhm r0402 — D_REFSSCLKIN
+1.5VS — R40 10KOhm r0402 — D_REFCLKIN
R41 10KOhm r0402 /X — GND
R42 10KOhm r0402 /X — GND
CHANGE TO PULL DOWN

M_VREF_MCH — C26 0.1UF/16V — GND
M_VREF_MCH — C27 1UF/10V — GND

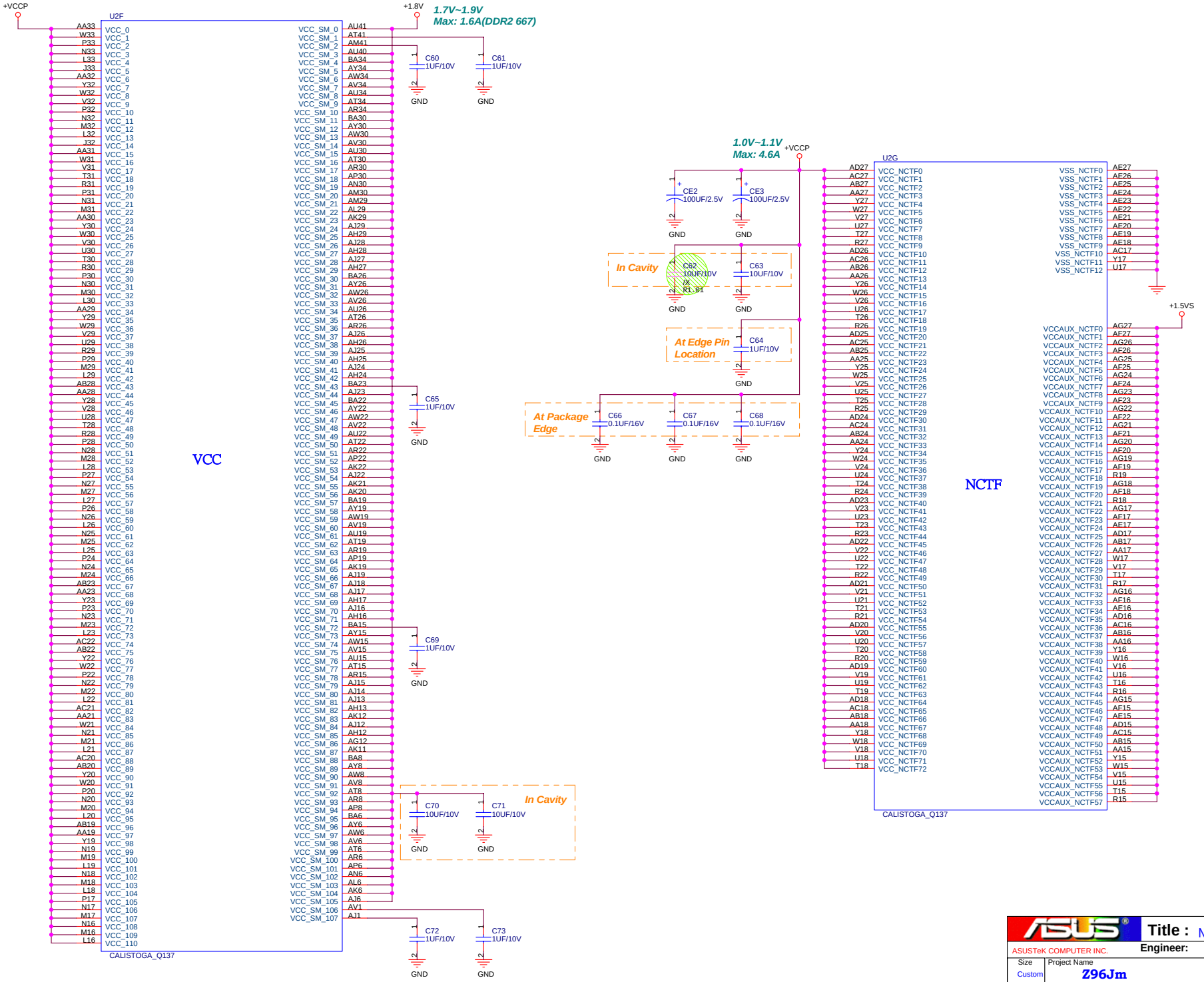
ASUSTeK COMPUTER INC.	Title : NB-945PM(DMI & CFG)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 8 of 91	



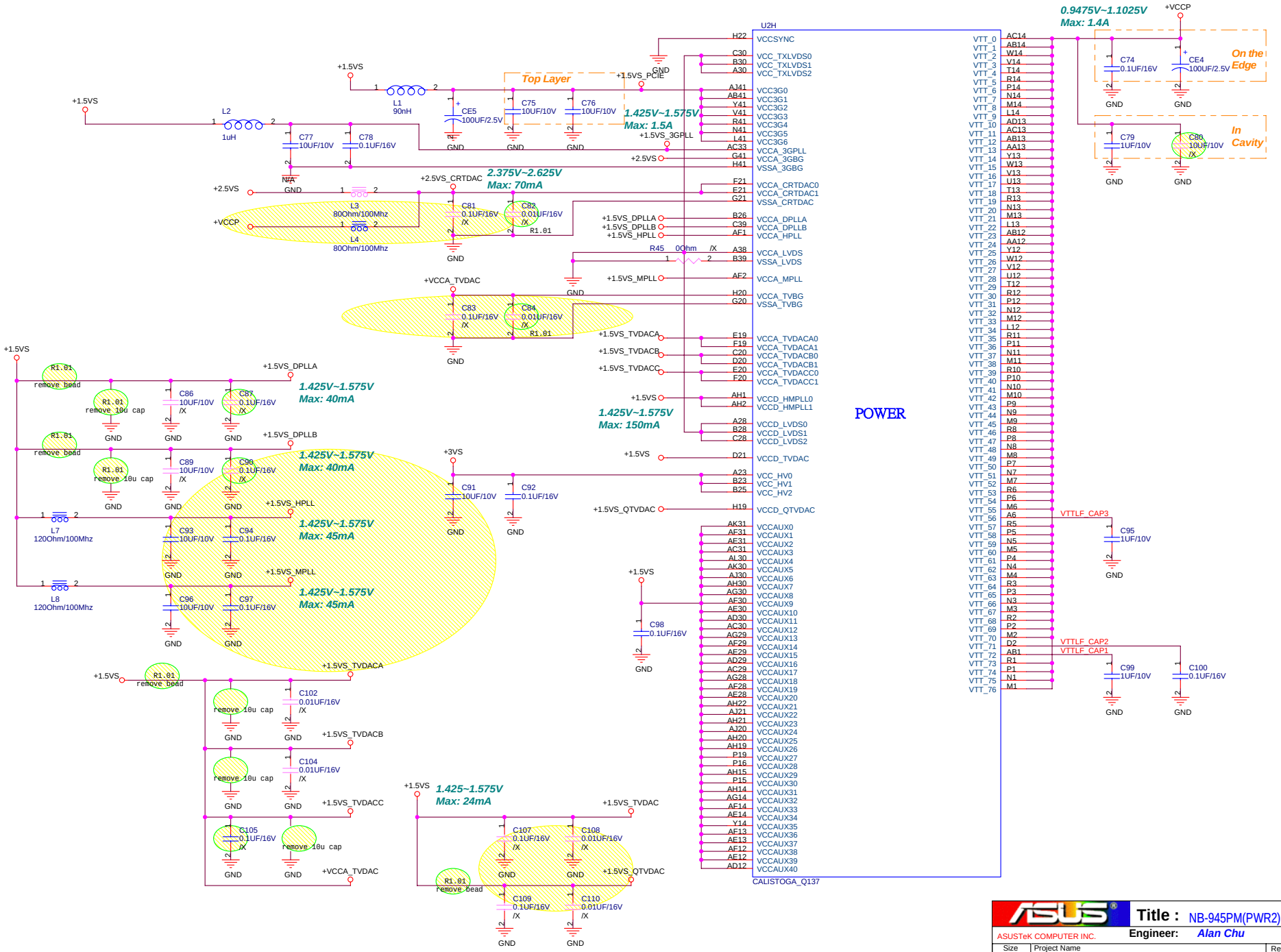
Title :	NB_945PM(GRAPHIC)
ASUSTeK COMPUTER INC.	Engineer: Alan Chu
Size: Custom	Project Name: Z96Jm
Rev: 1.0	
Date: Monday, August 21, 2006	Sheet 9 of 91

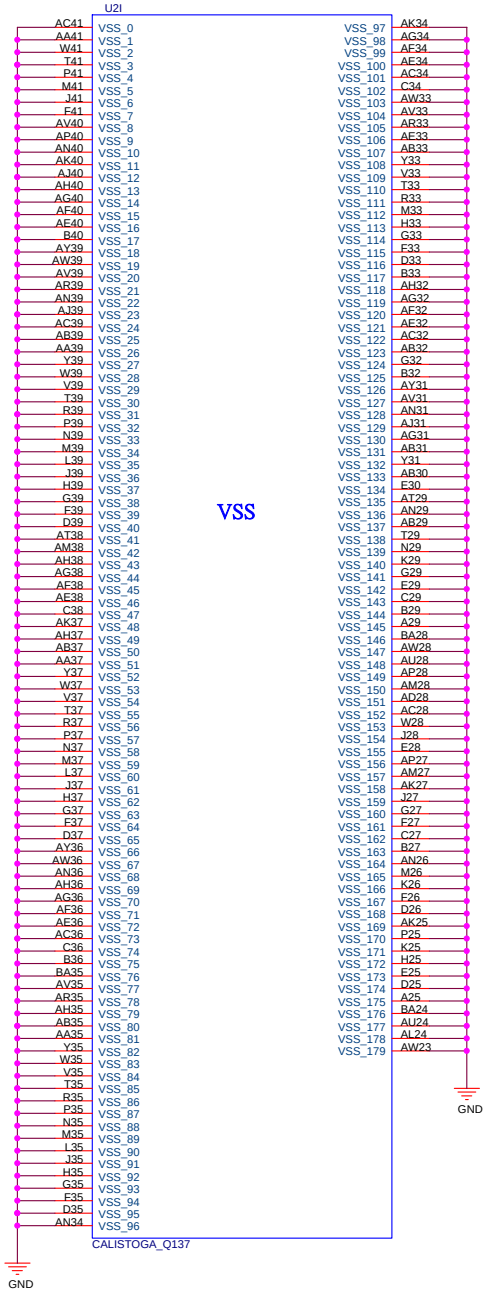


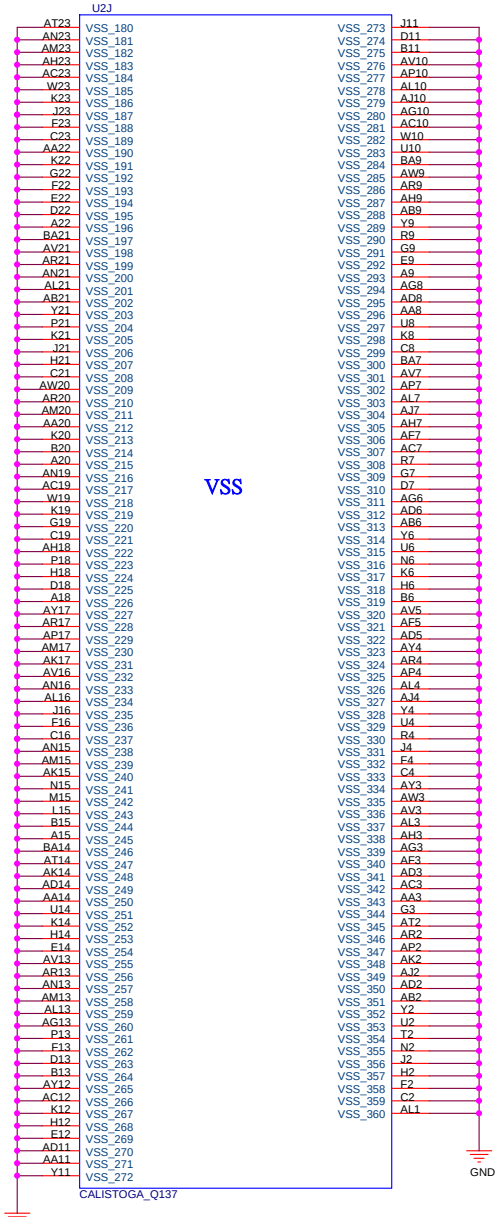
ASUSTeK COMPUTER INC.	Title : NB-945PM(DDR2)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 10 of 91	



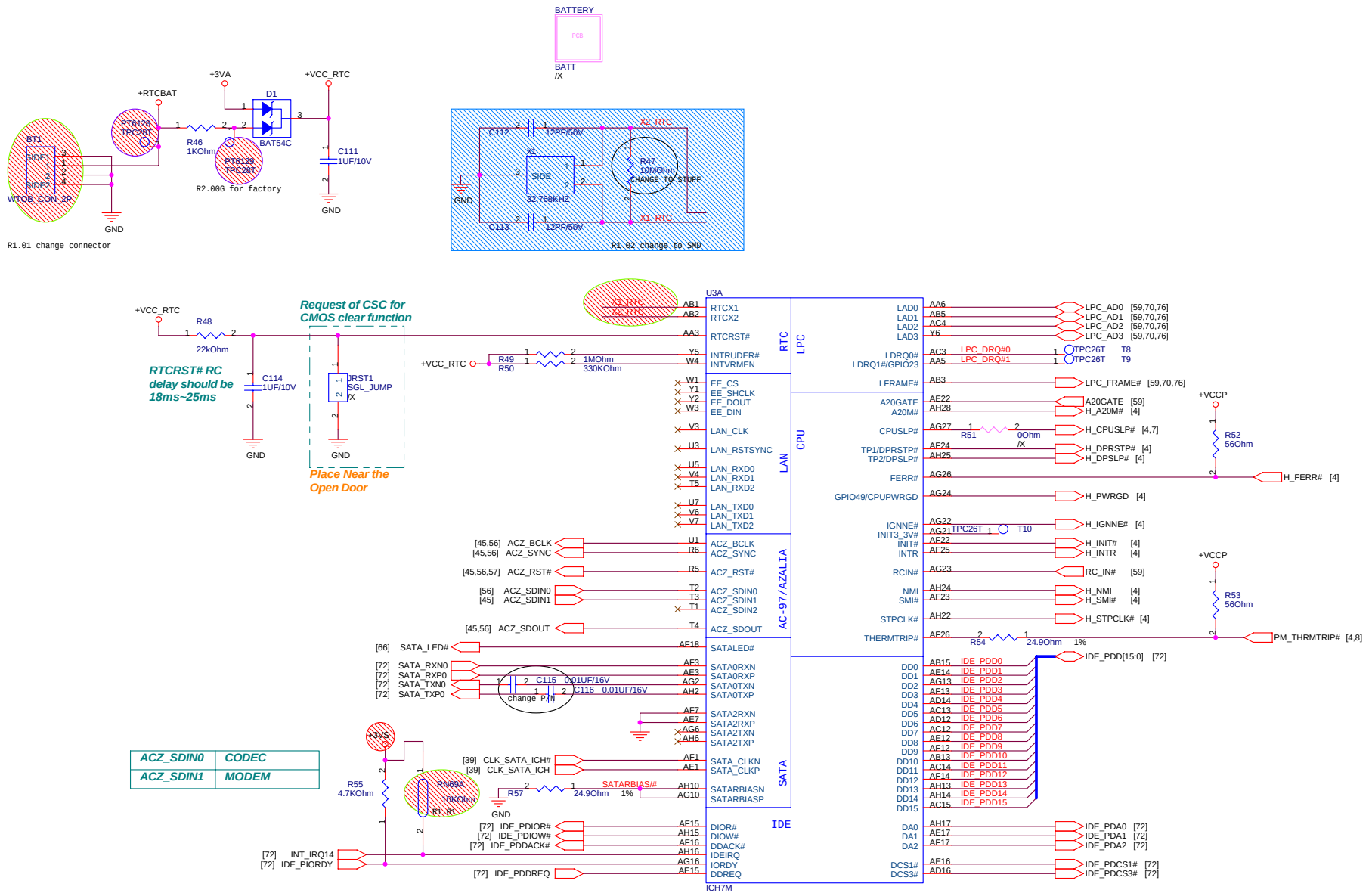
ASUSTeK COMPUTER INC.	Title : NB-945PM(PWR)	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 11 of 91	


POWER
U2H
CALISTOGA_Q137
Top Layer
On the Edge
In Cavity
+1.5VS
+1.5VS_PCIE
+1.5VS_3GPLL
+2.5VS
+2.5VS_CRTDAC
+VCCP
+VCCA_TVDAC
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS_TVDACA
+1.5VS_TVDACB
+1.5VS_TVDACC
+1.5VS_QTVDAC
+3VS
0.9475V~1.1025V
Max: 1.4A
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 150mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
1.425~1.575V
Max: 24mA
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
Title : NB-945PM(PWR2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 12 of 91

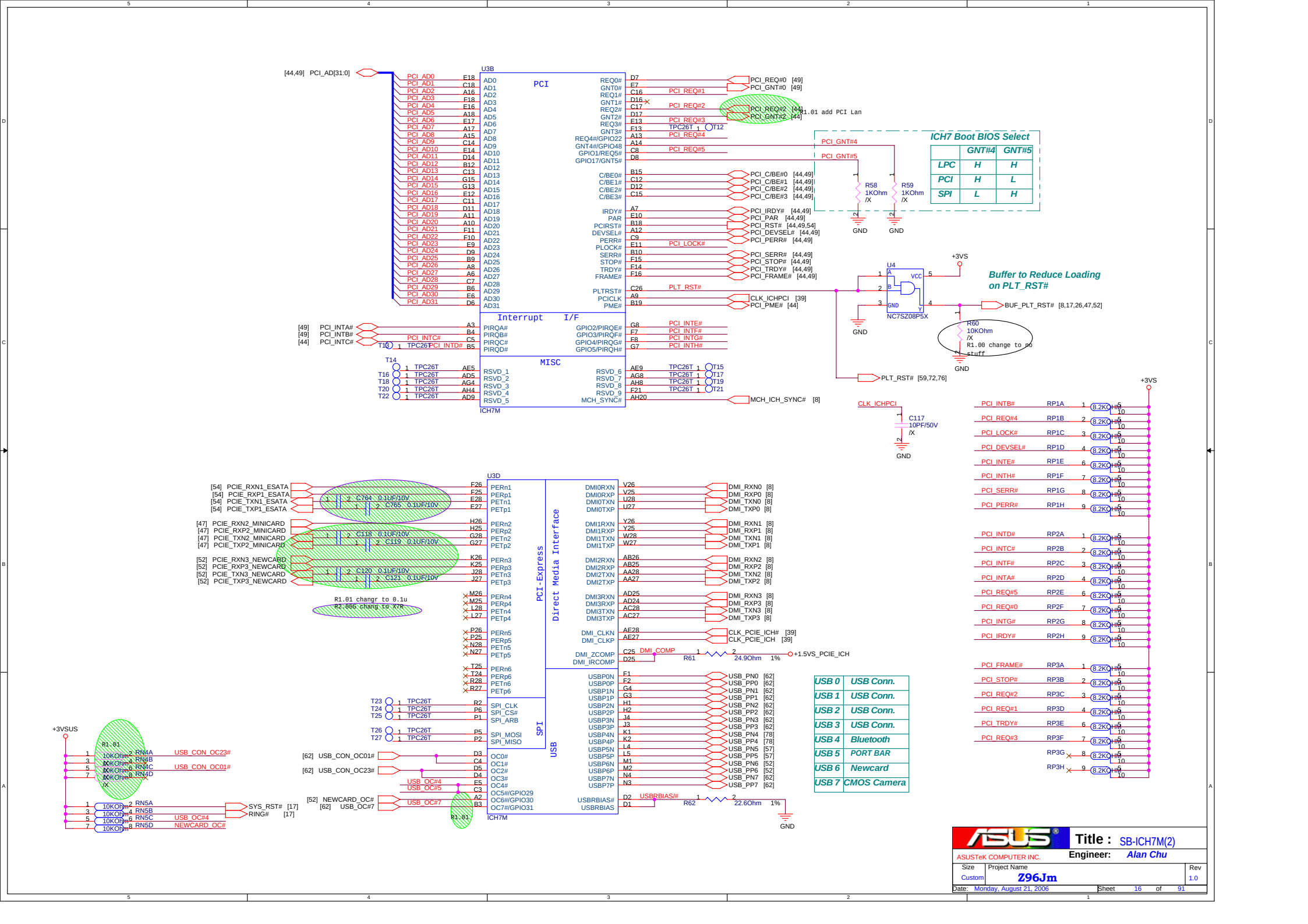


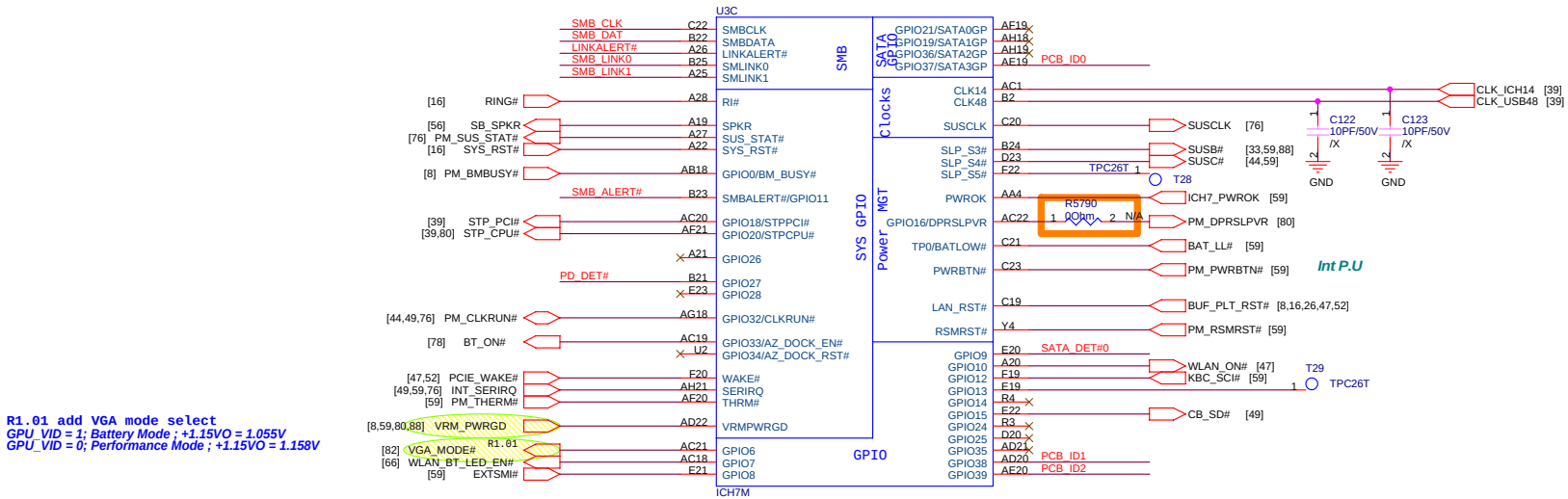


ASUSTeK COMPUTER INC.	Title : NB-945PM(GND)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 13 of 91		



Title :	SB-ICH7-M(1)
ASUSTeK COMPUTER INC.	Engineer: Alan Chu
Size: Custom	Project Name: Z96Jm
Rev: 1.0	
Date: Monday, August 21, 2006	Sheet 15 of 91

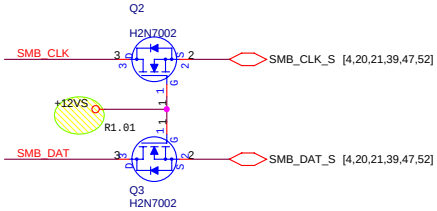

U3B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
U4
NC7SZ08P5X
U3D
PCI-Express
Direct Media Interface
SPI
USB
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 PORT BAR
USB 6 Newcard
USB 7 CMOS Camera
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 16 of 91

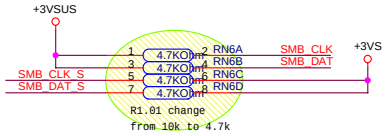


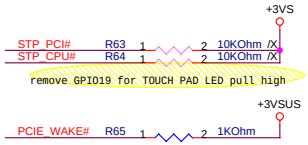
R1.01 add VGA mode select

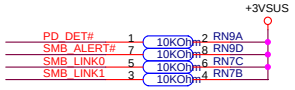
GPU_VID = 1; Battery Mode ; +1.15VO = 1.055V

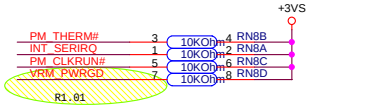
GPU_VID = 0; Performance Mode ; +1.15VO = 1.158V

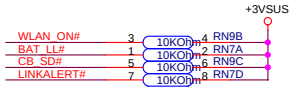


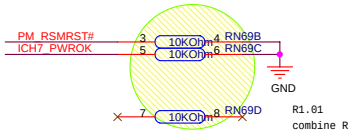


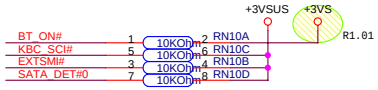


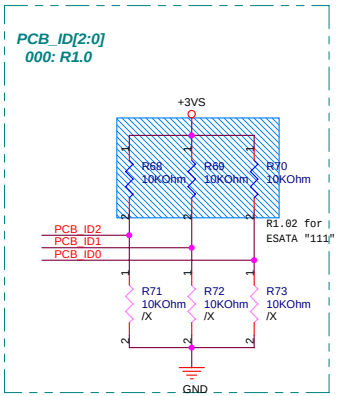












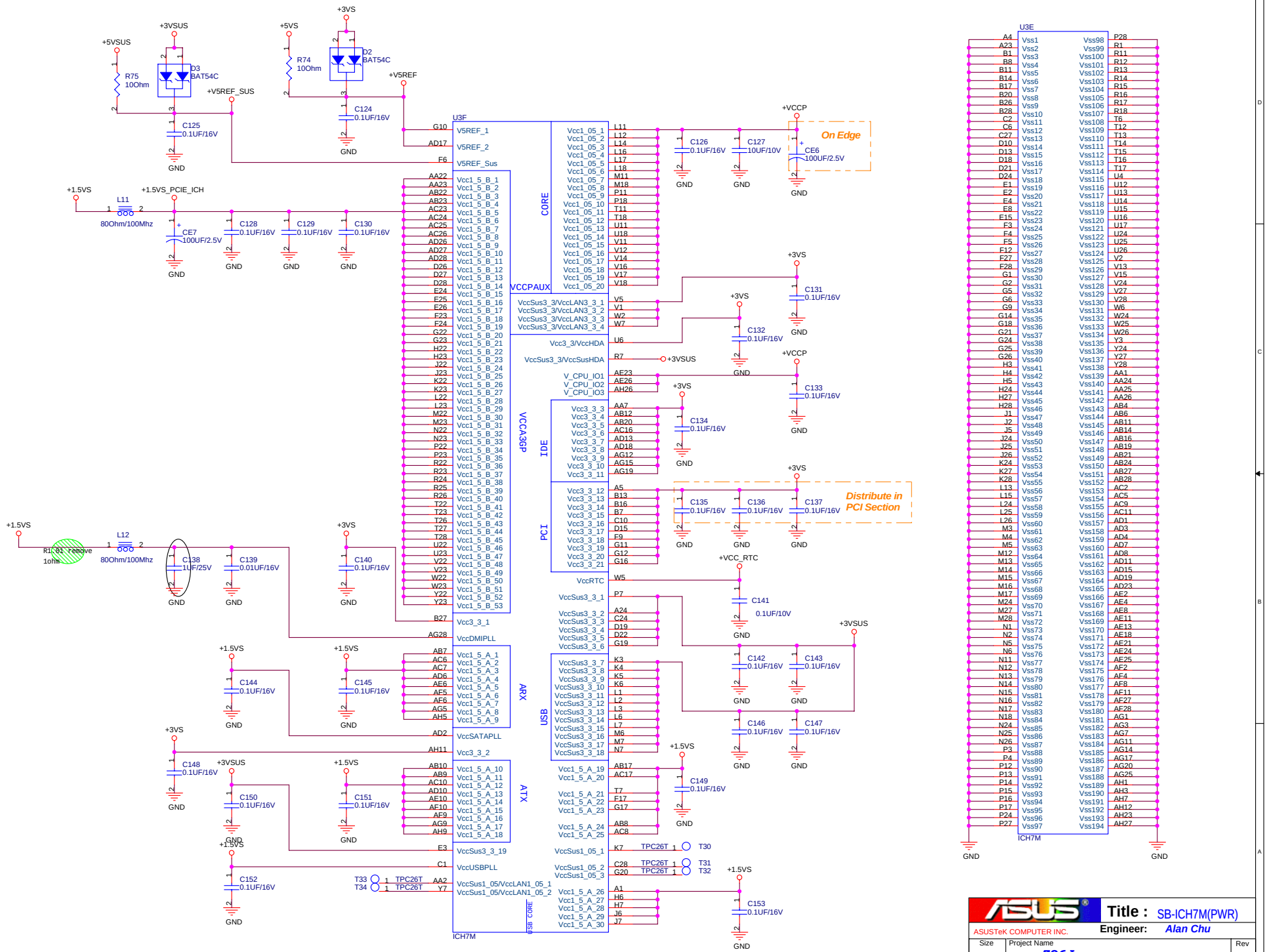
ASUSTeK COMPUTER INC

Title : SB-ICH7M(3)

Engineer: *Alan Chu*

Size	Project Name	Rev
Custom	Z96Jm	1.0

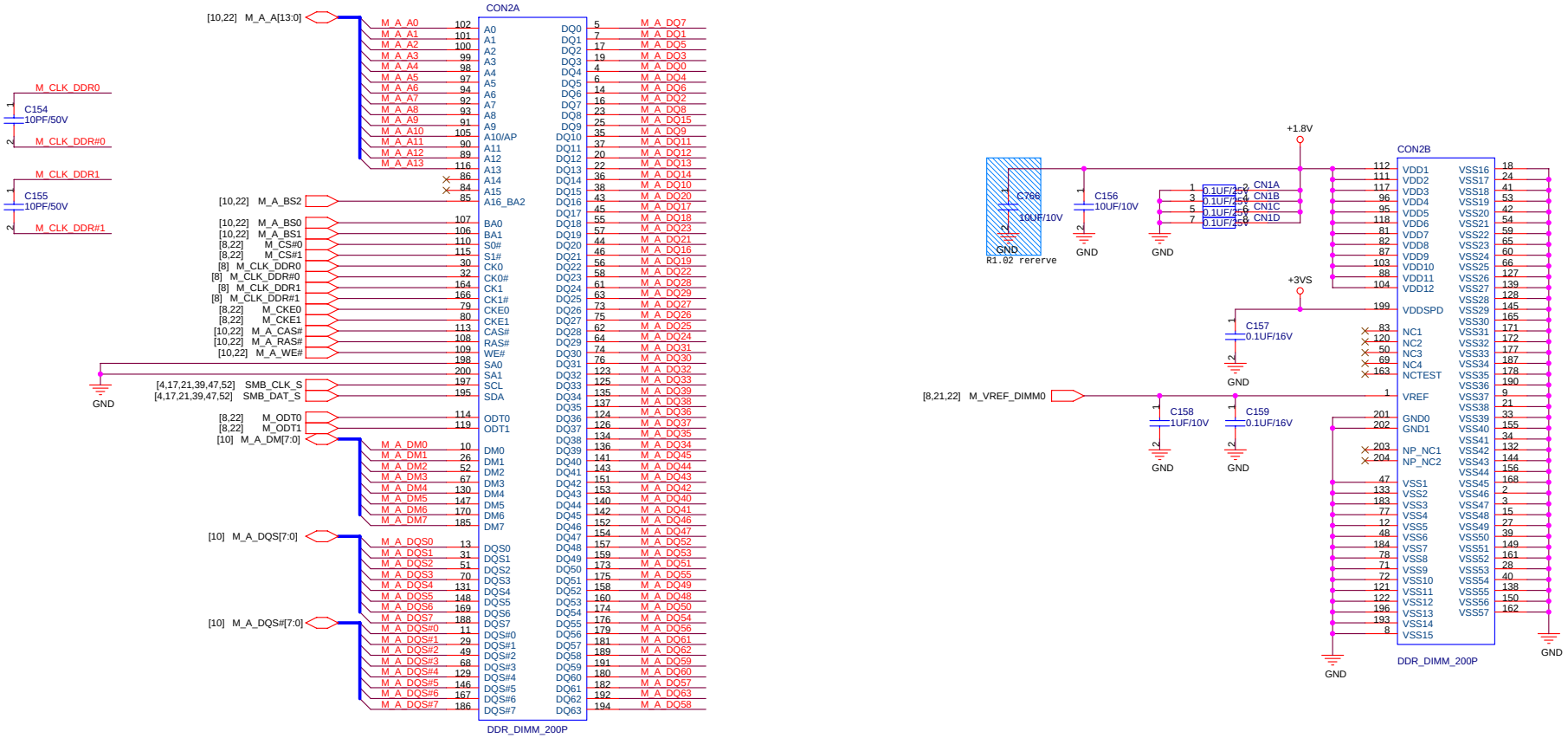
Date: Monday, August 21, 2006 Sheet 17 of 91



ASUSTeK COMPUTER INC.	Title : SB-ICH7M(PWR)		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 18 of 91		

M_A_DQ[63:0] [10]

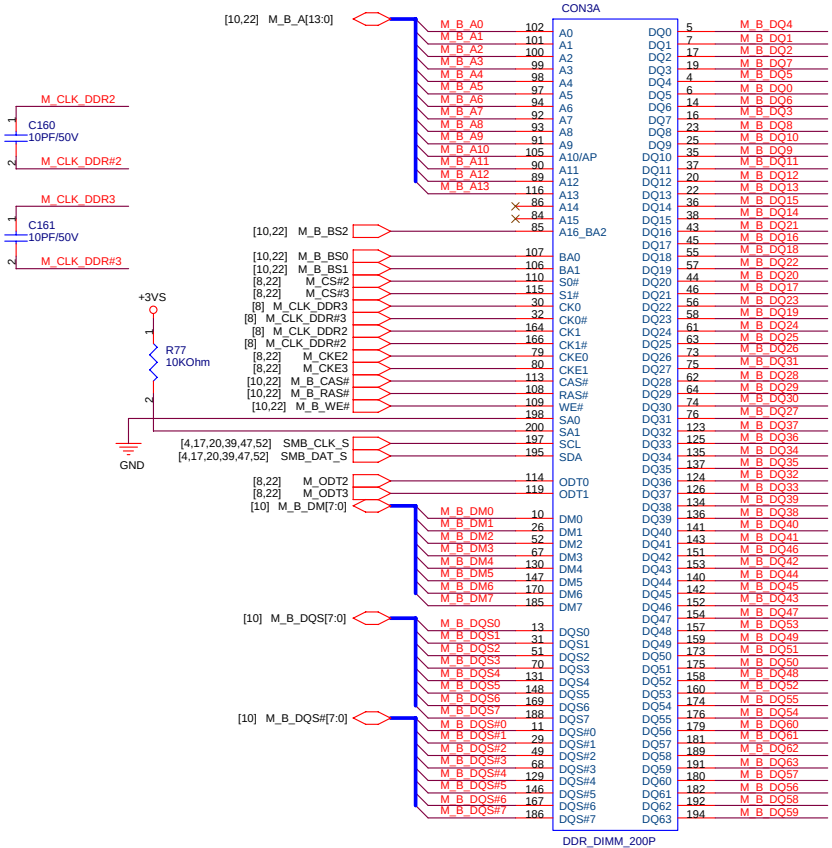
REV Type

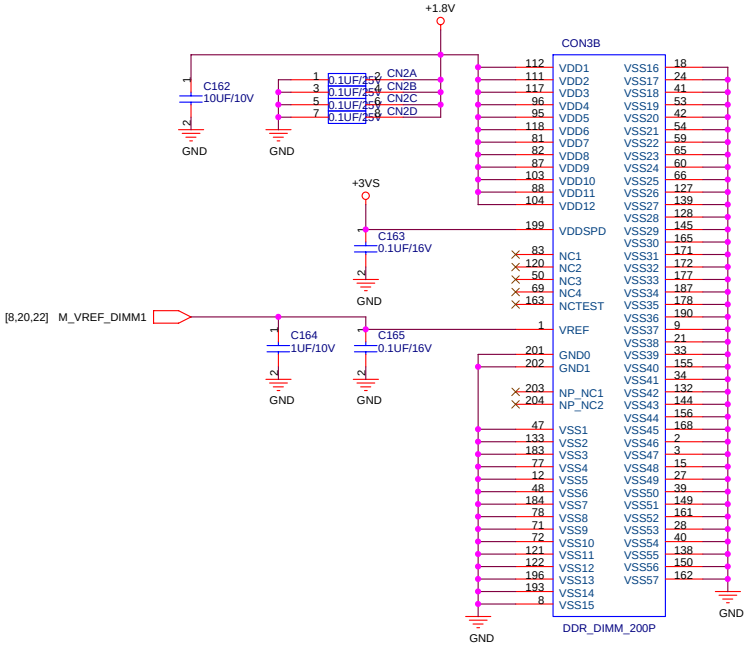


ASUSTeK COMPUTER INC.	Title : DDR2 SO-DIMM0		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 20 of 91		

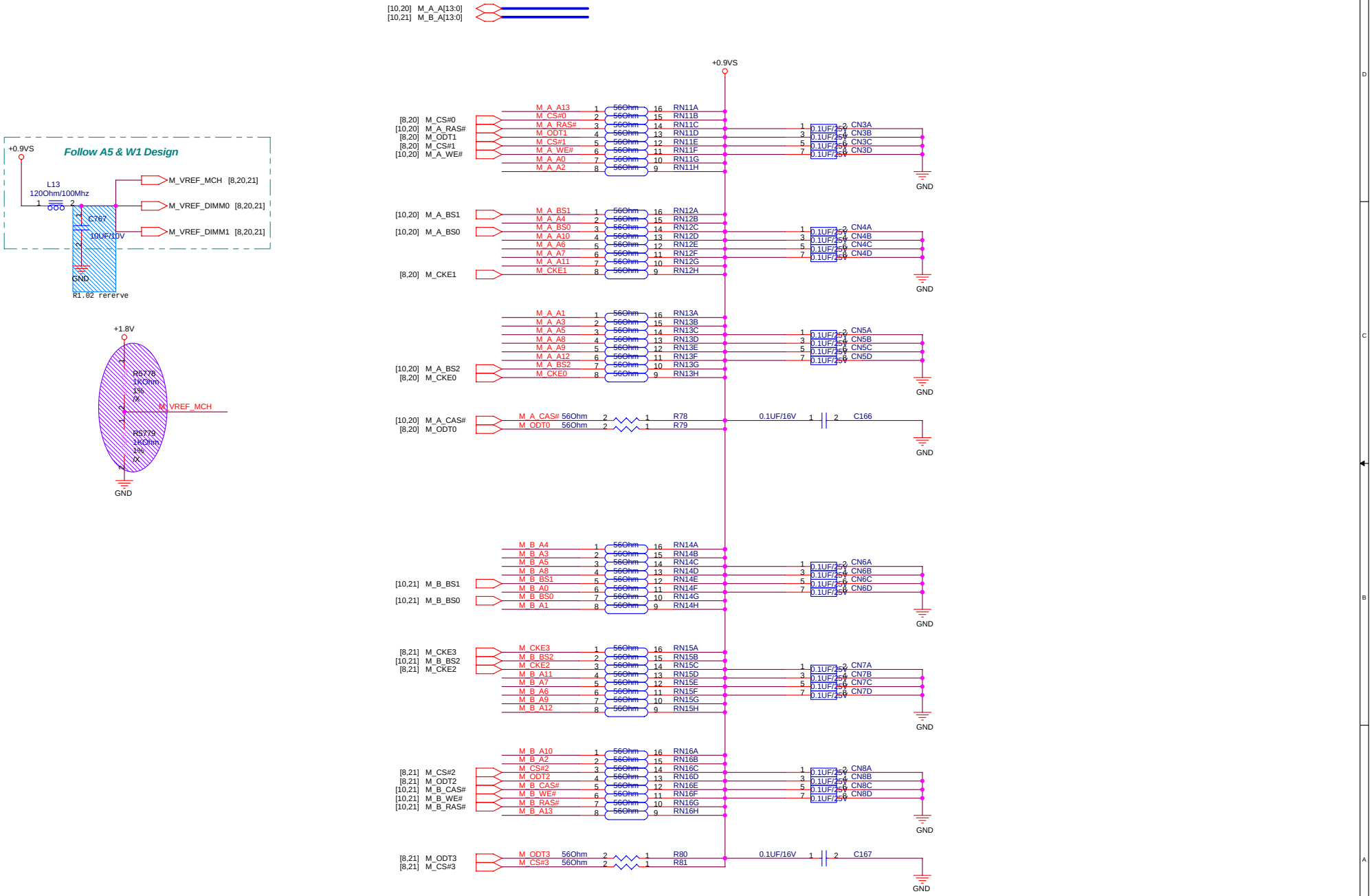
M_B_DQ[63:0] [10]

STD Type





ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 21 of 91		



ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 22 of 91	

GPIO[0]: Tx Power Savings Enable
0: 50% Tx output swing
1: full Tx output swing (recommended)
(default 0, internal pull-down)

GPIO[1]: Tx De-emphasis Enable
0: Tx de-emphasis disbale
1: Tx de-emphasis enable
(default 0, internal pull-down)

R1.01 add thermal detect from EC

MID / Vendor /SIZE	3	2	1	0
Samsung 128M	0	0	0	0
Samsung 256M	0	0	0	1
Hynix 128M	0	0	1	0
Hynix 256M	0	0	1	1
Infineon 128M	0	1	0	0
Infineon 256M	0	1	0	1
	0	1	1	0
	0	1	1	1

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800
PANEL ID0 RESERVE FOR VENDOR

GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01

Spread Spectrum

Down Spread Spectrum for EMI Attenuation

	SRS : 0	/ 1 / NC.
P1819B :	-1.25	-1.75 x.
MK1726 :	-1.8	-2.5 -0.6.

PWR_CTRL: HIGH(1.0V) / LOW(1.08V)
PULL DOWN IF USED FOR POWER PLAY

1.65V VREF Divider close to M56

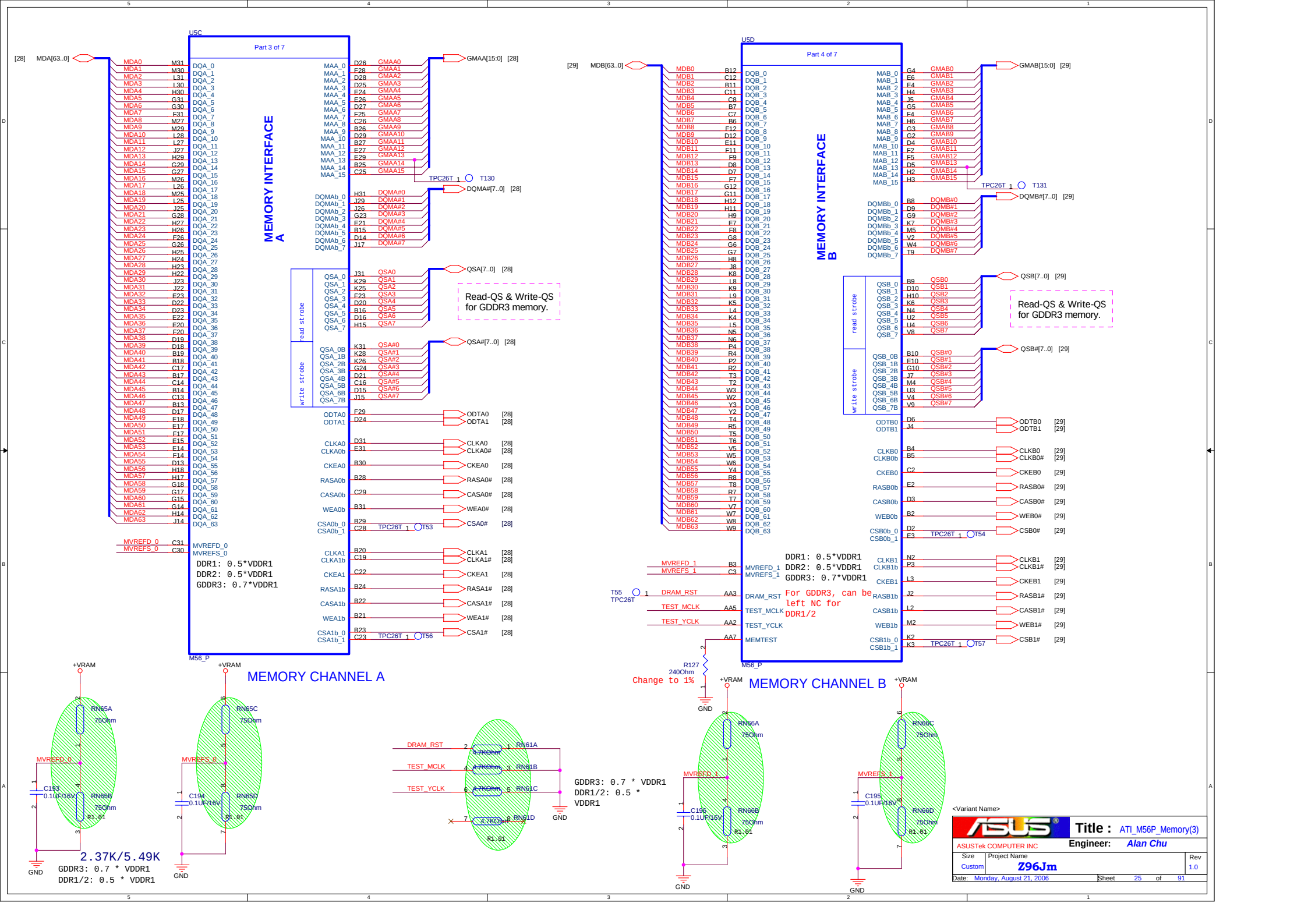
remove DVI

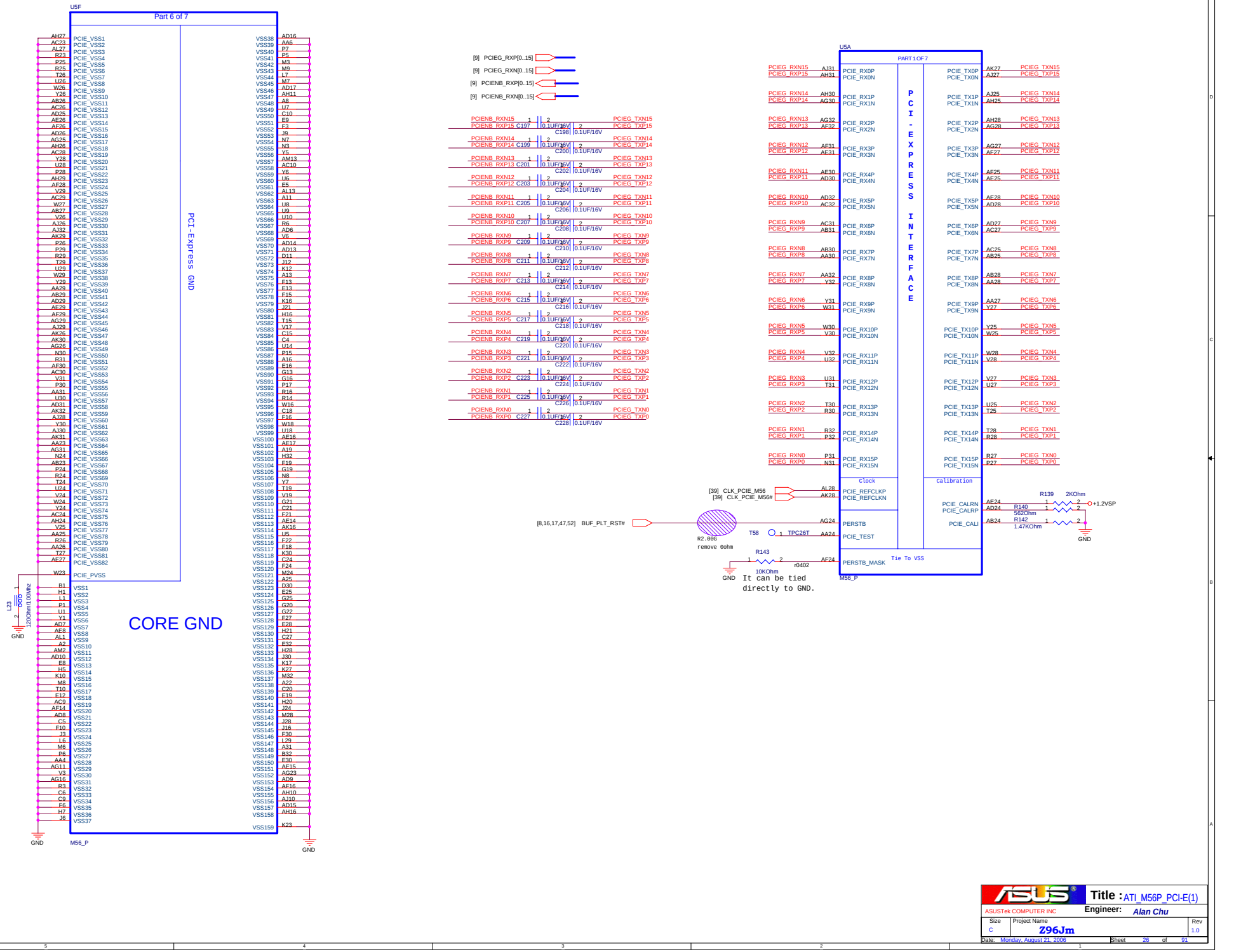
left unconnect if not used.

unconnect if not used.

R1.01 combine R

Title :	ATI_M56P_MAIN(2)
ASUSTek COMPUTER INC	Engineer: Alan Chu
Size: Custom	Project Name: Z96Jm
Rev: 1.0	
Date: Monday, August 21, 2006	Sheet 24 of 91


U5C
Part 3 of 7
MEMORY INTERFACE A
[28] MDA[63..0]
MDA0 M31
MDA1 M30
MDA2 L31
MDA3 L30
MDA4 H30
MDA5 G31
MDA6 G30
MDA7 F31
MDA8 M27
MDA9 M29
MDA10 L28
MDA11 L27
MDA12 J27
MDA13 H29
MDA14 G29
MDA15 G27
MDA16 M26
MDA17 L26
MDA18 M25
MDA19 L25
MDA20 J25
MDA21 G28
MDA22 H27
MDA23 H26
MDA24 F26
MDA25 G26
MDA26 H25
MDA27 H24
MDA28 H23
MDA29 H22
MDA30 J23
MDA31 J22
MDA32 F23
MDA33 D22
MDA34 D23
MDA35 F22
MDA36 E20
MDA37 F20
MDA38 D19
MDA39 D18
MDA40 B19
MDA41 B18
MDA42 C17
MDA43 B17
MDA44 C14
MDA45 B14
MDA46 C13
MDA47 B13
MDA48 D17
MDA49 E18
MDA50 E17
MDA51 F17
MDA52 E15
MDA53 E14
MDA54 F14
MDA55 D13
MDA56 H18
MDA57 H17
MDA58 G18
MDA59 G17
MDA60 G15
MDA61 G14
MDA62 H14
MDA63 J14
MVREFD_0 C31
MVREFS_0 C30
MVREFD_0
MVREFS_0
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
M56_P
GMAA[15:0] [28]
TPC26T_1 T130
DQMA#[7..0] [28]
QSA[7..0] [28]
QSA#[7..0] [28]
read strobe
write strobe
Read-QS & Write-QS for GDDR3 memory.
ODTA0 [28]
ODTA1 [28]
CLKA0 [28]
CLKA0# [28]
CKEA0 [28]
RASA0# [28]
CASA0# [28]
WEA0# [28]
CSA0# [28]
CLKA1 [28]
CLKA1# [28]
CKEA1 [28]
RASA1# [28]
CASA1# [28]
WEA1# [28]
CSA1# [28]
TPC26T_1 T53
TPC26T_1 T56
MEMORY CHANNEL A
+VRAM
RN65A 75Ohm
RN65B 75Ohm
RN65C 75Ohm
RN65D 75Ohm
C193 0.1UF/16V
C194 0.1UF/16V
R1.01
GND
2.37K/5.49K
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
U5D
Part 4 of 7
MEMORY INTERFACE B
[29] MDB[63..0]
MDB0 B12
MDB1 C12
MDB2 B11
MDB3 C11
MDB4 C8
MDB5 B7
MDB6 C7
MDB7 B6
MDB8 E12
MDB9 D12
MDB10 E11
MDB11 F11
MDB12 F9
MDB13 D8
MDB14 D7
MDB15 E7
MDB16 G12
MDB17 G11
MDB18 H12
MDB19 H11
MDB20 H9
MDB21 E7
MDB22 F8
MDB23 G8
MDB24 G6
MDB25 G7
MDB26 H8
MDB27 J8
MDB28 K8
MDB29 L8
MDB30 K9
MDB31 L9
MDB32 K5
MDB33 L4
MDB34 K4
MDB35 L5
MDB36 N5
MDB37 N6
MDB38 P4
MDB39 R4
MDB40 P2
MDB41 R2
MDB42 T3
MDB43 T2
MDB44 W3
MDB45 W2
MDB46 Y3
MDB47 Y2
MDB48 T4
MDB49 R5
MDB50 T5
MDB51 T6
MDB52 V5
MDB53 W5
MDB54 W6
MDB55 Y4
MDB56 R8
MDB57 T8
MDB58 R7
MDB59 T7
MDB60 V7
MDB61 W7
MDB62 W8
MDB63 W9
MVREFD_1 B3
MVREFS_1 C3
MVREFD_1
MVREFS_1
DDR1: 0.5*VDDR1
DDR2: 0.5*VDDR1
GDDR3: 0.7*VDDR1
DRAM_RST AA3
TEST_MCLK AA5
TEST_YCLK AA2
MEMTEST AA7
For GDDR3, can be left NC for DDR1/2
T55 TPC26T 1
R127 240Ohm 1%
Change to 1%
M56_P
GMAB[15:0] [29]
TPC26T_1 T131
DQMB#[7..0] [29]
QSB[7..0] [29]
QSB#[7..0] [29]
Read-QS & Write-QS for GDDR3 memory.
ODTB0 [29]
ODTB1 [29]
CLKB0 [29]
CLKB0# [29]
CKEB0 [29]
RASB0# [29]
CASB0# [29]
WEB0# [29]
CSB0# [29]
CLKB1 [29]
CLKB1# [29]
CKEB1 [29]
RASB1# [29]
CASB1# [29]
WEB1# [29]
CSB1# [29]
TPC26T_1 T54
TPC26T_1 T57
MEMORY CHANNEL B
+VRAM
RN66A 75Ohm
RN66B 75Ohm
RN66C 75Ohm
RN66D 75Ohm
C195 0.1UF/16V
C196 0.1UF/16V
R1.01
GND
DRAM_RST
TEST_MCLK
TEST_YCLK
RN61A 4.7KOhm
RN61B 4.7KOhm
RN61C 4.7KOhm
RN61D 4.7KOhm
R1.01
GDDR3: 0.7 * VDDR1
DDR1/2: 0.5 * VDDR1
<Variant Name>
Title : ATI_M56P_Memory(3)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 25 of 91


U5F
Part 6 of 7
PCI-Express GND
CORE GND
M56_P
GND
L23
600
120Ohm/100Mhz
PCIE_VSS1
PCIE_VSS2
PCIE_VSS3
PCIE_VSS4
PCIE_VSS5
PCIE_VSS6
PCIE_VSS7
PCIE_VSS8
PCIE_VSS9
PCIE_VSS10
PCIE_VSS11
PCIE_VSS12
PCIE_VSS13
PCIE_VSS14
PCIE_VSS15
PCIE_VSS16
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VSS158
VSS159
[9] PCIEG_RXP[0..15]
[9] PCIEG_RXN[0..15]
[9] PCIENB_RXP[0..15]
[9] PCIENB_RXN[0..15]
PCIENB_RXN15 PCIENB_RXP15 C197 C198 PCIEG_TXN15 PCIEG_TXP15
PCIENB_RXN14 PCIENB_RXP14 C199 C200 PCIEG_TXN14 PCIEG_TXP14
PCIENB_RXN13 PCIENB_RXP13 C201 C202 PCIEG_TXN13 PCIEG_TXP13
PCIENB_RXN12 PCIENB_RXP12 C203 C204 PCIEG_TXN12 PCIEG_TXP12
PCIENB_RXN11 PCIENB_RXP11 C205 C206 PCIEG_TXN11 PCIEG_TXP11
PCIENB_RXN10 PCIENB_RXP10 C207 C208 PCIEG_TXN10 PCIEG_TXP10
PCIENB_RXN9 PCIENB_RXP9 C209 C210 PCIEG_TXN9 PCIEG_TXP9
PCIENB_RXN8 PCIENB_RXP8 C211 C212 PCIEG_TXN8 PCIEG_TXP8
PCIENB_RXN7 PCIENB_RXP7 C213 C214 PCIEG_TXN7 PCIEG_TXP7
PCIENB_RXN6 PCIENB_RXP6 C215 C216 PCIEG_TXN6 PCIEG_TXP6
PCIENB_RXN5 PCIENB_RXP5 C217 C218 PCIEG_TXN5 PCIEG_TXP5
PCIENB_RXN4 PCIENB_RXP4 C4 C219 C220 PCIEG_TXN4 PCIEG_TXP4
PCIENB_RXN3 PCIENB_RXP3 C221 C222 PCIEG_TXN3 PCIEG_TXP3
PCIENB_RXN2 PCIENB_RXP2 C223 C224 PCIEG_TXN2 PCIEG_TXP2
PCIENB_RXN1 PCIENB_RXP1 C225 C226 PCIEG_TXN1 PCIEG_TXP1
PCIENB_RXN0 PCIENB_RXP0 C227 C228 PCIEG_TXN0 PCIEG_TXP0
0.1UF/16V
U5A
PART 1 OF 7
PCI-EXPRESS INTERFACE
PCIE_RX0P PCIE_RX0N AJ31 AH31
PCIE_RX1P PCIE_RX1N AH30 AG30
PCIE_RX2P PCIE_RX2N AG32 AF32
PCIE_RX3P PCIE_RX3N AF31 AE31
PCIE_RX4P PCIE_RX4N AE30 AD30
PCIE_RX5P PCIE_RX5N AD32 AC32
PCIE_RX6P PCIE_RX6N AC31 AB31
PCIE_RX7P PCIE_RX7N AB30 AA30
PCIE_RX8P PCIE_RX8N AA32 Y32
PCIE_RX9P PCIE_RX9N Y31 W31
PCIE_RX10P PCIE_RX10N W30 V30
PCIE_RX11P PCIE_RX11N V32 U32
PCIE_RX12P PCIE_RX12N U31 T31
PCIE_RX13P PCIE_RX13N T30 R30
PCIE_RX14P PCIE_RX14N R32 P32
PCIE_RX15P PCIE_RX15N P31 N31
PCIEG_RXN15 PCIEG_RXP15
PCIEG_RXN14 PCIEG_RXP14
PCIEG_RXN13 PCIEG_RXP13
PCIEG_RXN12 PCIEG_RXP12
PCIEG_RXN11 PCIEG_RXP11
PCIEG_RXN10 PCIEG_RXP10
PCIEG_RXN9 PCIEG_RXP9
PCIEG_RXN8 PCIEG_RXP8
PCIEG_RXN7 PCIEG_RXP7
PCIEG_RXN6 PCIEG_RXP6
PCIEG_RXN5 PCIEG_RXP5
PCIEG_RXN4 PCIEG_RXP4
PCIEG_RXN3 PCIEG_RXP3
PCIEG_RXN2 PCIEG_RXP2
PCIEG_RXN1 PCIEG_RXP1
PCIEG_RXN0 PCIEG_RXP0
Clock
PCIE_REFCLKP AL28
PCIE_REFCLKN AK28
[39] CLK_PCIE_M56
[39] CLK_PCIE_M56#
PERSTB AG24
PCIE_TEST AA24
PERSTB_MASK AF24
Tie To VSS
Calibration
PCIE_CALRN AE24
PCIE_CALRP AD24
PCIE_CALI AB24
R139 2KOhm
R140 562Ohm
R142 1.47KOhm
+1.2VSP
GND
[8,16,17,47,52] BUF_PLT_RST#
R2.00G
remove 0ohm
T58 TPC26T
R143 10KOhm r0402
It can be tied directly to GND.
PCIE_TX0P PCIE_TX0N AK27 AJ27 PCIEG_TXN15 PCIEG_TXP15
PCIE_TX1P PCIE_TX1N AJ25 AH25 PCIEG_TXN14 PCIEG_TXP14
PCIE_TX2P PCIE_TX2N AH28 AG28 PCIEG_TXN13 PCIEG_TXP13
PCIE_TX3P PCIE_TX3N AG27 AF27 PCIEG_TXN12 PCIEG_TXP12
PCIE_TX4P PCIE_TX4N AF25 AE25 PCIEG_TXN11 PCIEG_TXP11
PCIE_TX5P PCIE_TX5N AE28 AD28 PCIEG_TXN10 PCIEG_TXP10
PCIE_TX6P PCIE_TX6N AD27 AC27 PCIEG_TXN9 PCIEG_TXP9
PCIE_TX7P PCIE_TX7N AC25 AB25 PCIEG_TXN8 PCIEG_TXP8
PCIE_TX8P PCIE_TX8N AB28 AA28 PCIEG_TXN7 PCIEG_TXP7
PCIE_TX9P PCIE_TX9N AA27 Y27 PCIEG_TXN6 PCIEG_TXP6
PCIE_TX10P PCIE_TX10N Y25 W25 PCIEG_TXN5 PCIEG_TXP5
PCIE_TX11P PCIE_TX11N W28 V28 PCIEG_TXN4 PCIEG_TXP4
PCIE_TX12P PCIE_TX12N V27 U27 PCIEG_TXN3 PCIEG_TXP3
PCIE_TX13P PCIE_TX13N U25 T25 PCIEG_TXN2 PCIEG_TXP2
PCIE_TX14P PCIE_TX14N T28 R28 PCIEG_TXN1 PCIEG_TXP1
PCIE_TX15P PCIE_TX15N R27 P27 PCIEG_TXN0 PCIEG_TXP0
M56_P
Title : ATI_M56P_PCI-E(1)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size C
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 26 of 91

GDDR3/DDR1: 1.8V
DDR2: 1.8 ~ 2 V

GDDR3: 2A
DDR1: 0.8A

PART 5 OF 7

POWER

Memory I/O

0/I

PCI-Express

Core

I/O Internal

LVDS PLL, I/O

Memory I/O Clock

no stuff

VDDR3 < 322 mA
VDDR4 + VDDR5 < 50 mA

PART 7 OF 7

BACK BIAS DISABLE

Odd channel

Single channel /Even channel

LVDS channel

DEMO SCHEMATIC: 1.5/1.8/2.5 V

BL BRIGHTNESS CONTROL (PWM)

BACK BIAS DISABLE

<Variant Name>

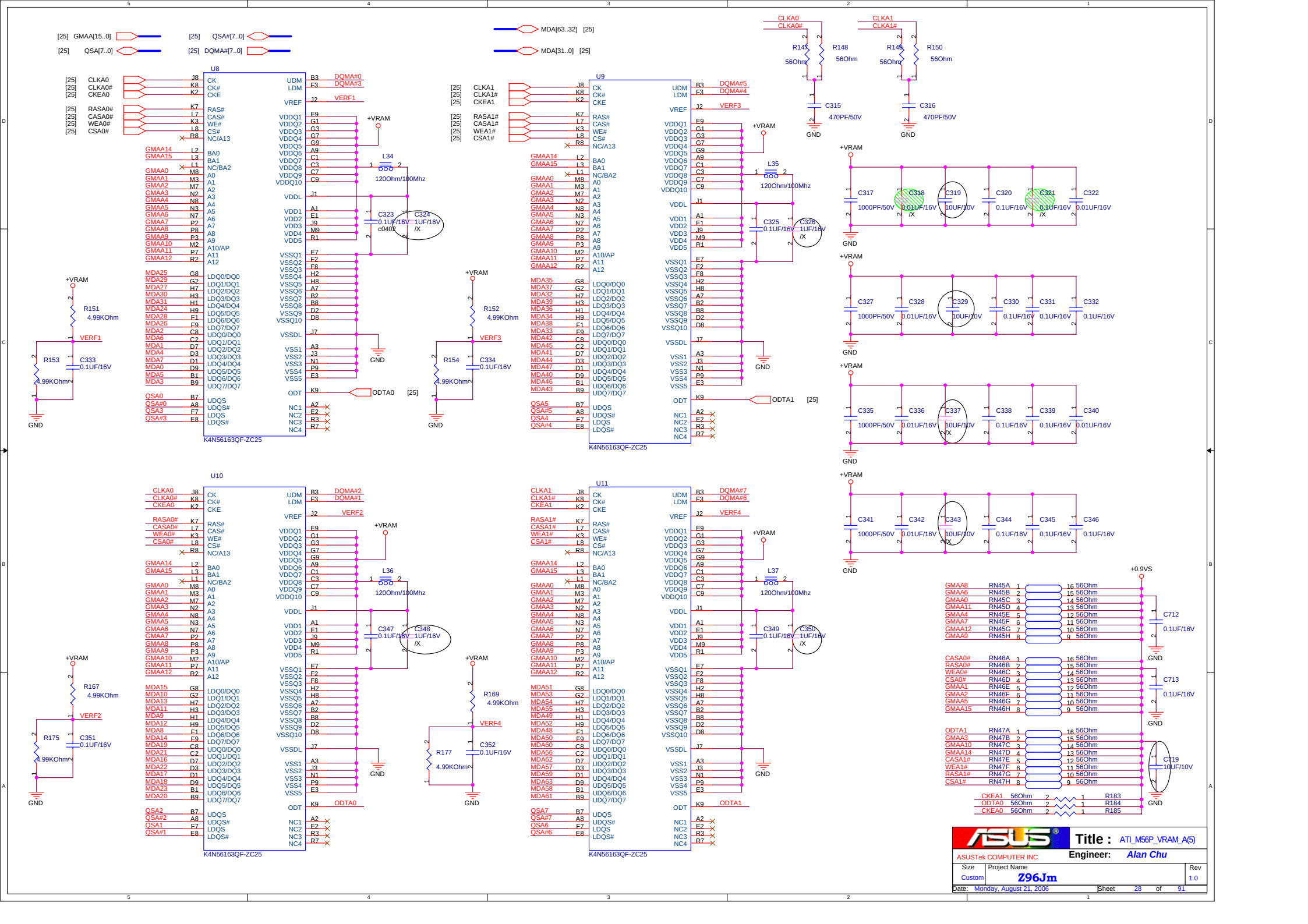
ASUSTek COMPUTER INC

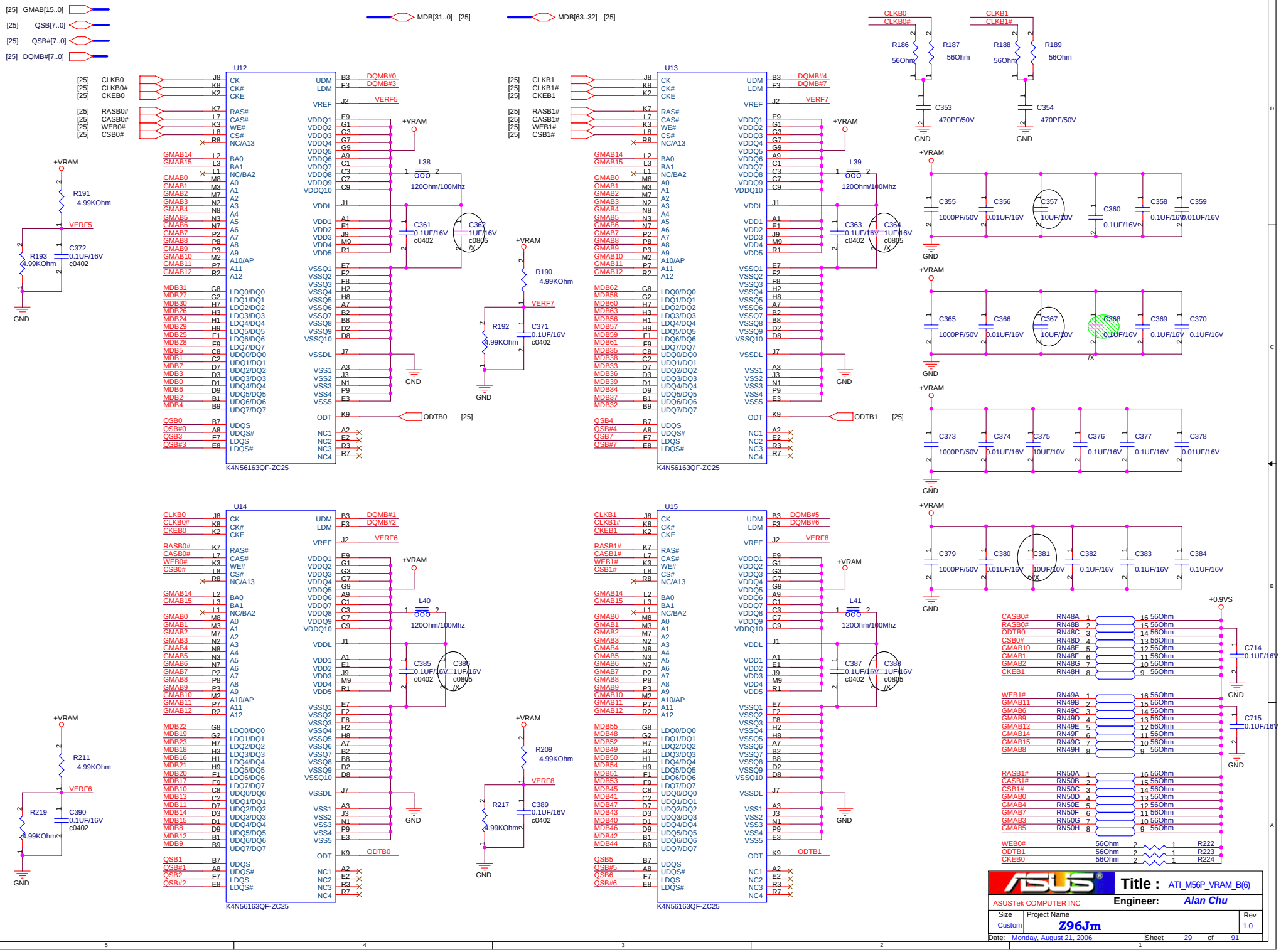
Title : ATI_M56P_POWER(4)

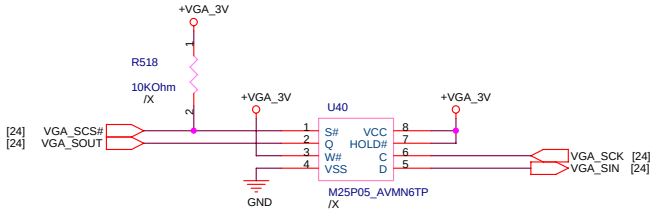
Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

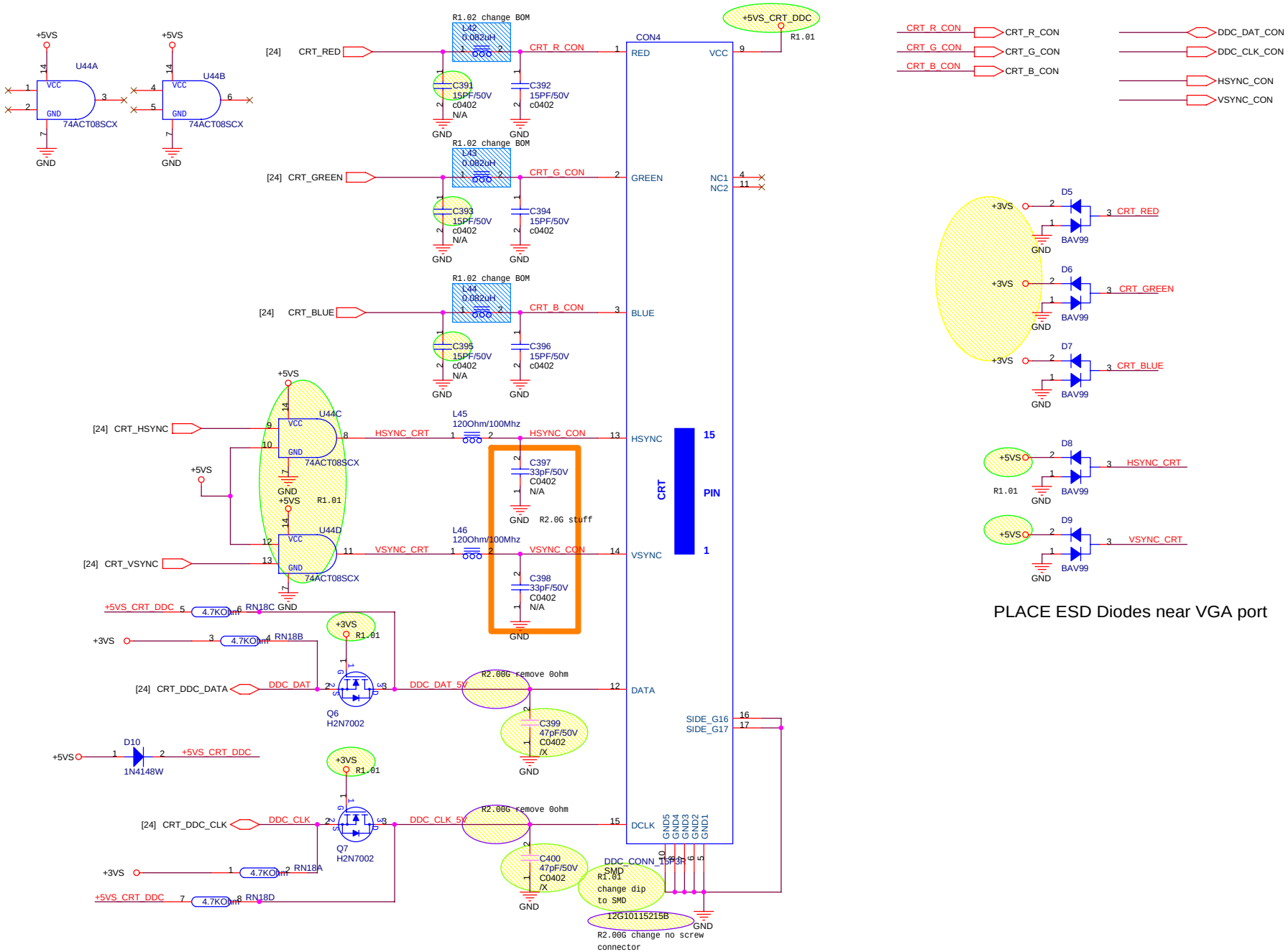
Date: Monday, August 21, 2006 Sheet 27 of 91


[25] GMAA[15..0]
[25] QSA[7..0]
[25] QSA#[7..0]
[25] DQMA#[7..0]
MDA[63..32] [25]
MDA[31..0] [25]
U8
U9
U10
U11
K4N56163QF-ZC25
+VRAM
GND
R151 4.99KOhm
R152 4.99KOhm
R153 4.99KOhm
R154 4.99KOhm
R167 4.99KOhm
R169 4.99KOhm
R175 4.99KOhm
R177 4.99KOhm
C333 0.1UF/16V
C334 0.1UF/16V
C351 0.1UF/16V
C352 0.1UF/16V
L34 120Ohm/100Mhz
L35 120Ohm/100Mhz
L36 120Ohm/100Mhz
L37 120Ohm/100Mhz
C323 0.1UF/16V c0402
C324 1UF/16V /X
C325 0.1UF/16V
C326 1UF/16V /X
C347 0.1UF/16V
C348 1UF/16V /X
C349 0.1UF/16V
C350 1UF/16V /X
CLKA0
CLKA0#
CLKA1
CLKA1#
R145 56Ohm
R148 56Ohm
R149 56Ohm
R150 56Ohm
C315 470PF/50V
C316 470PF/50V
C317 1000PF/50V
C318 0.01UF/16V /X
C319 10UF/10V
C320 0.1UF/16V
C321 0.1UF/16V /X
C322 0.01UF/16V
C327 1000PF/50V
C328 0.01UF/16V
C329 10UF/10V
C330 0.1UF/16V
C331 0.1UF/16V
C332 0.1UF/16V
C335 1000PF/50V
C336 0.01UF/16V
C337 10UF/10V /X
C338 0.1UF/16V
C339 0.1UF/16V
C340 0.01UF/16V
C341 1000PF/50V
C342 0.01UF/16V
C343 10UF/10V /X
C344 0.1UF/16V
C345 0.1UF/16V
C346 0.1UF/16V
+0.9VS
RN45A RN45B RN45C RN45D RN45E RN45F RN45G RN45H
RN46A RN46B RN46C RN46D RN46E RN46F RN46G RN46H
RN47A RN47B RN47C RN47D RN47E RN47F RN47G RN47H
56Ohm
C712 0.1UF/16V
C713 0.1UF/16V
C719 10UF/10V
R183 R184 R185
CKEA1 ODTA0 CKEA0
Title : ATI_M56P_VRAM_A(5)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 28 of 91


[25] GMAB[15..0]
[25] QSB[7..0]
[25] QSB#[7..0]
[25] DQMB#[7..0]
MDB[31..0] [25]
MDB[63..32] [25]
U12
U13
U14
U15
K4N56163QF-ZC25
+VRAM
GND
R191 4.99KOhm
R193 4.99KOhm
R190 4.99KOhm
R192 4.99KOhm
R211 4.99KOhm
R219 4.99KOhm
R209 4.99KOhm
R217 4.99KOhm
C372 0.1UF/16V c0402
C361 0.1UF/16V c0402
C362 1UF/16V c0805 /X
C371 0.1UF/16V c0402
C385 0.1UF/16V c0402
C386 1UF/16V c0805 /X
C390 0.1UF/16V c0402
C389 0.1UF/16V c0402
L38 120Ohm/100Mhz
L39 120Ohm/100Mhz
L40 120Ohm/100Mhz
L41 120Ohm/100Mhz
CLKB0
CLKB0#
CLKB1
CLKB1#
R186 56Ohm
R187 56Ohm
R188 56Ohm
R189 56Ohm
C353 470PF/50V
C354 470PF/50V
C355 1000PF/50V
C356 0.01UF/16V
C357 10UF/10V
C360 0.1UF/16V
C358 0.1UF/16V
C359 0.01UF/16V
C365 1000PF/50V
C366 0.01UF/16V
C367 10UF/10V
C368 0.1UF/16V
C369 0.1UF/16V
C370 0.1UF/16V
C373 1000PF/50V
C374 0.01UF/16V
C375 10UF/10V
C376 0.1UF/16V
C377 0.1UF/16V
C378 0.01UF/16V
C379 1000PF/50V
C380 0.01UF/16V
C381 10UF/10V
C382 0.1UF/16V
C383 0.1UF/16V
C384 0.1UF/16V
+0.9VS
C714 0.1UF/16V
C715 0.1UF/16V
RN48A RN48B RN48C RN48D RN48E RN48F RN48G RN48H 56Ohm
RN49A RN49B RN49C RN49D RN49E RN49F RN49G RN49H 56Ohm
RN50A RN50B RN50C RN50D RN50E RN50F RN50G RN50H 56Ohm
WEB0# ODTB1 CKEB0 R222 R223 R224 56Ohm
Title : ATI_M56P_VRAM_B(6)
ASUSTek COMPUTER INC
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 29 of 91



ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: *Alan Chu*	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 30 of 91	

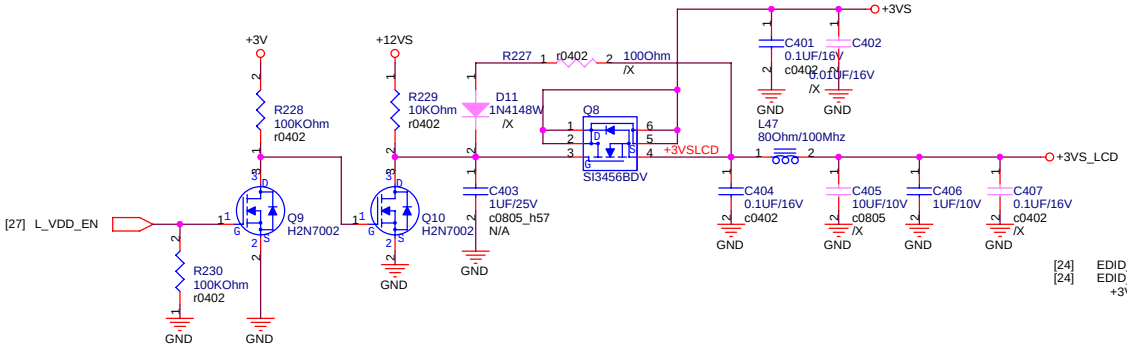


ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 32 of 91	

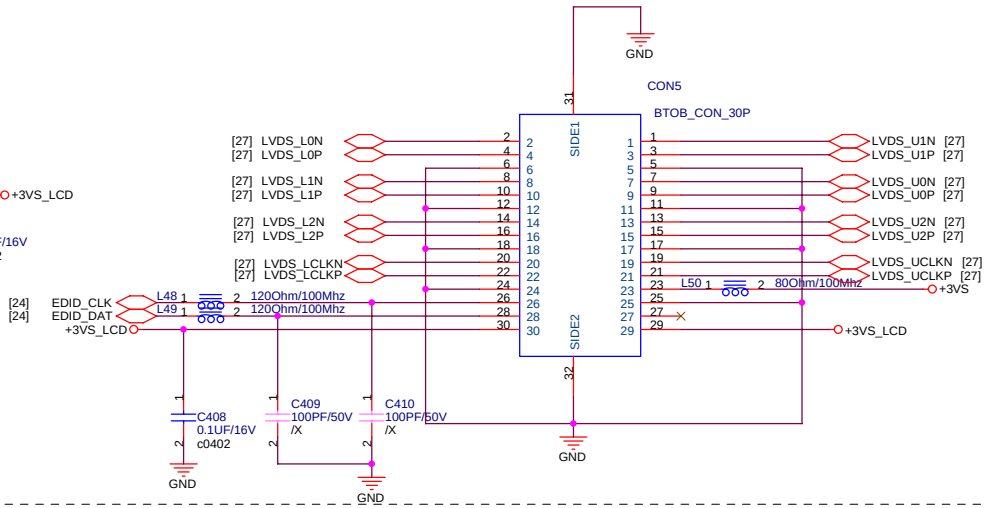
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD Power

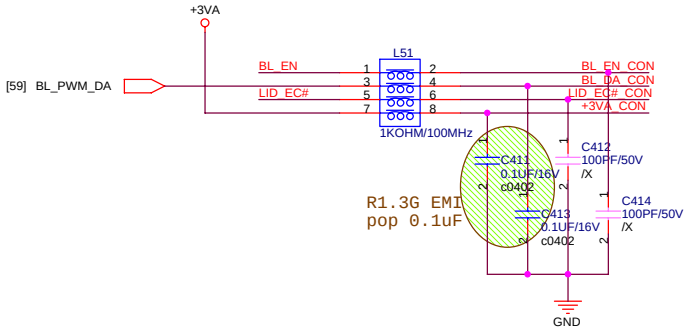


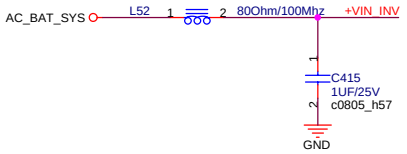
LCD LVDS Interface

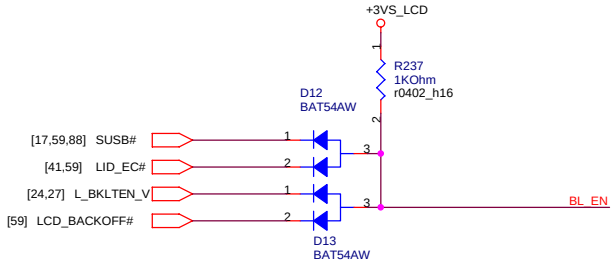


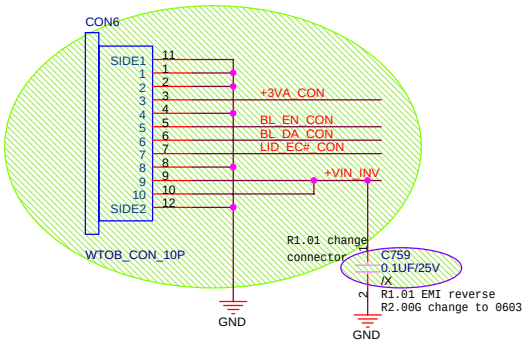
INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.





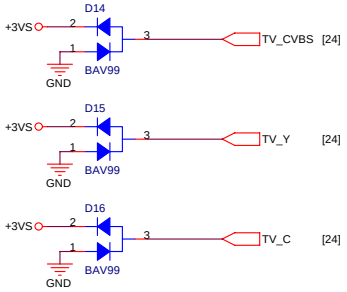




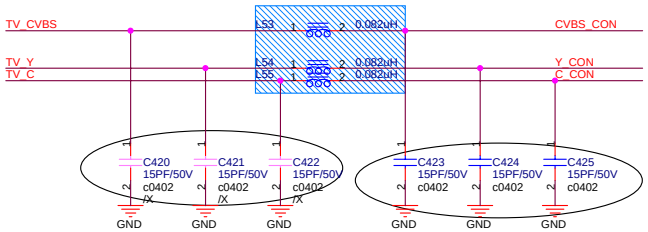
R1.01 remove HW reserve pannel ID

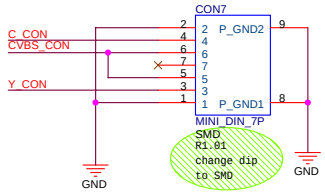
ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 33 of 91	

TV OUT



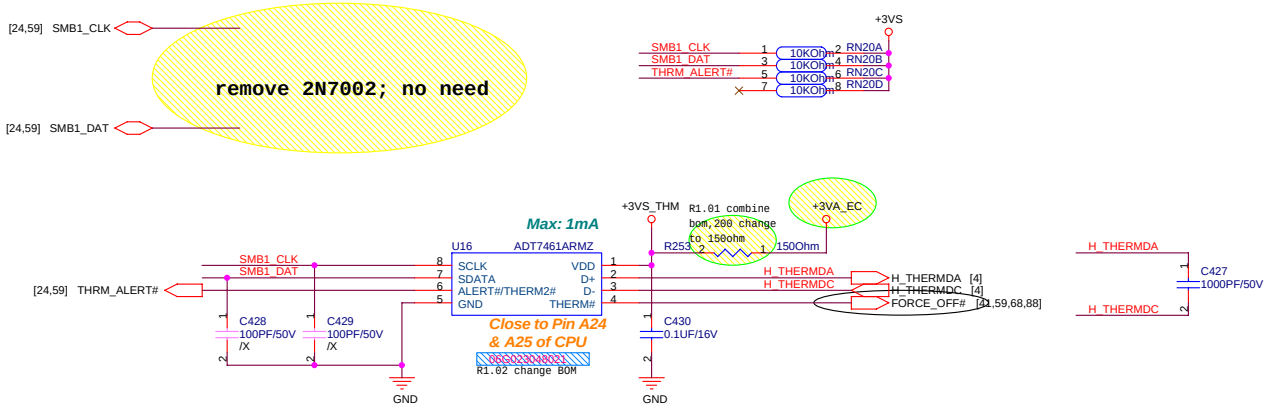
PLACE ESD
Diodes near
TV port





ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 35 of 91		

Thermal Sensor

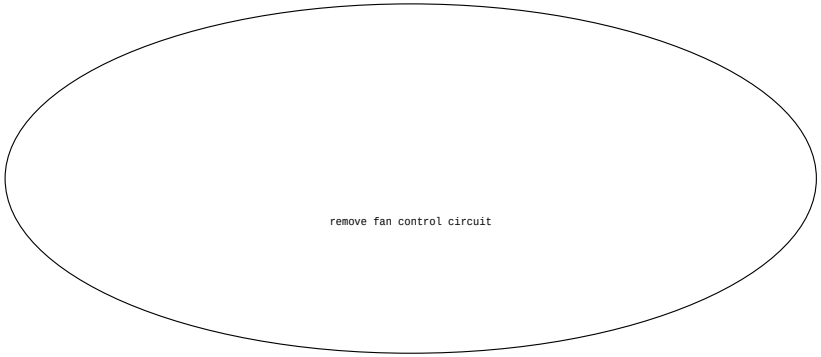


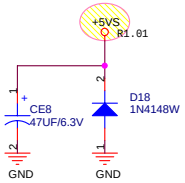
Route H_THERMDA and H_THERMDC on the same layer

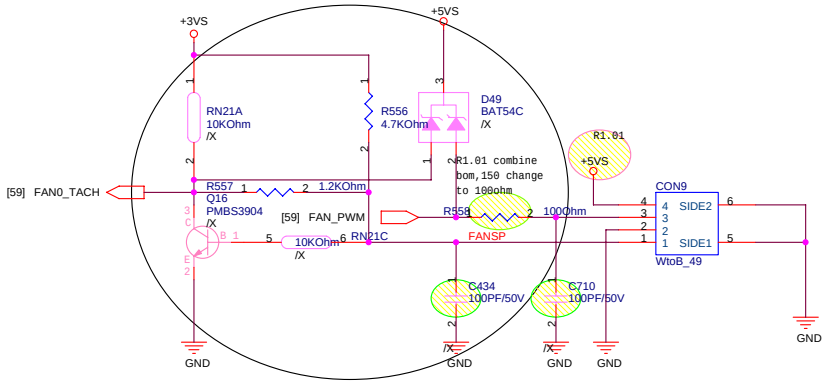
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control

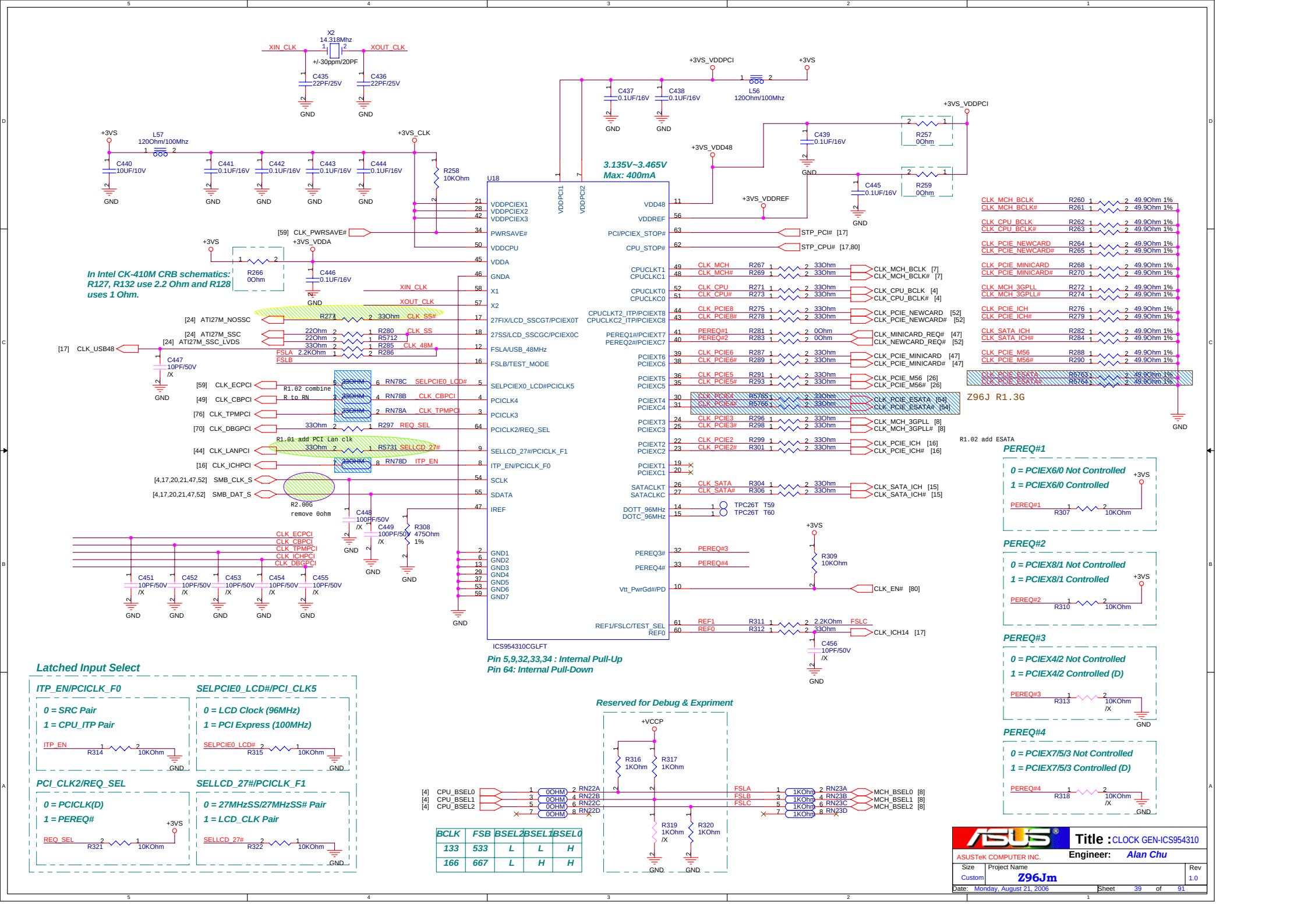






CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 37 of 91	



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

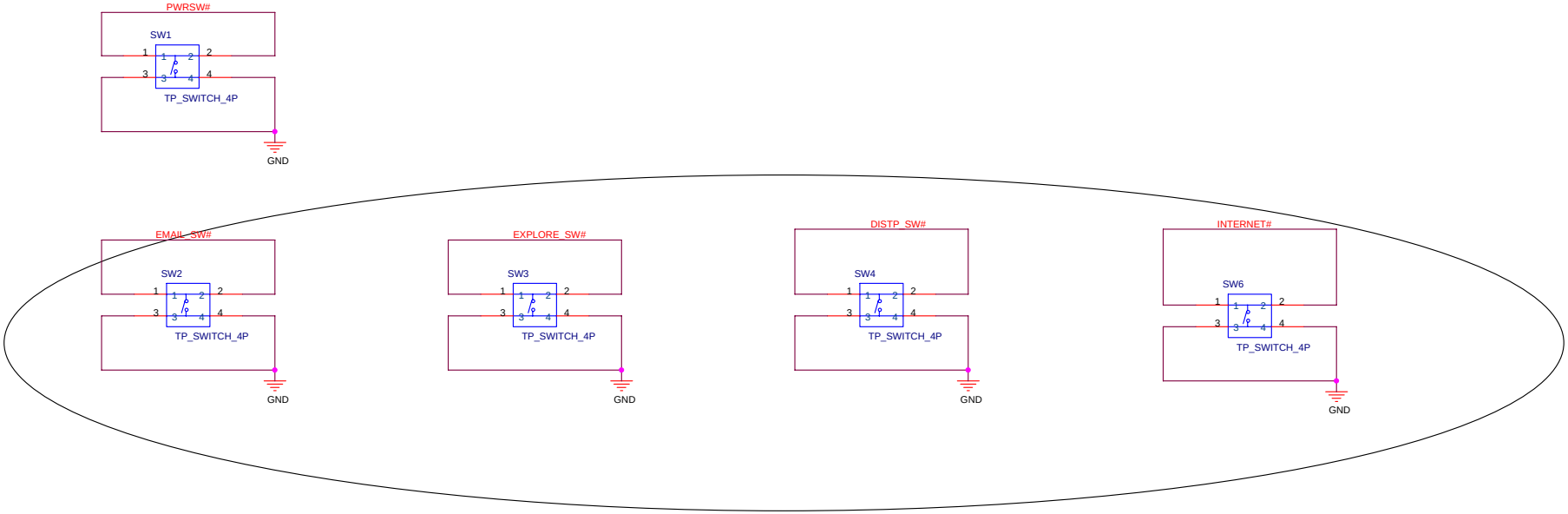
ASUSTeK COMPUTER INC.

Title : CLOCK GEN-ICS954310

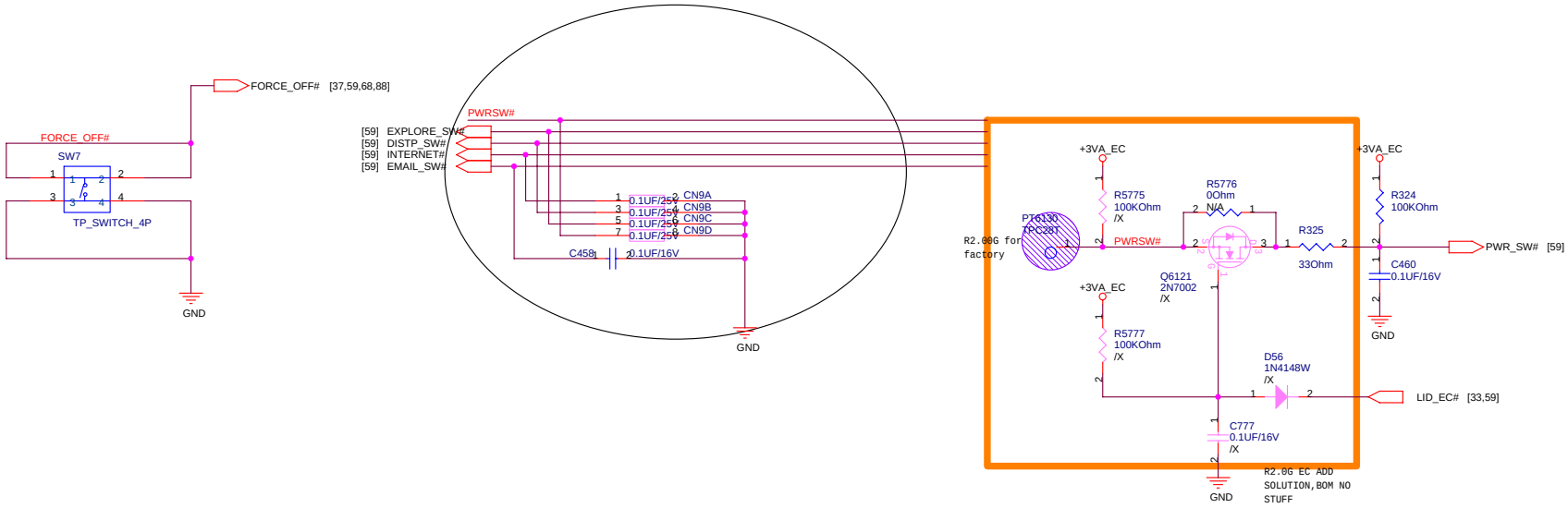
Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

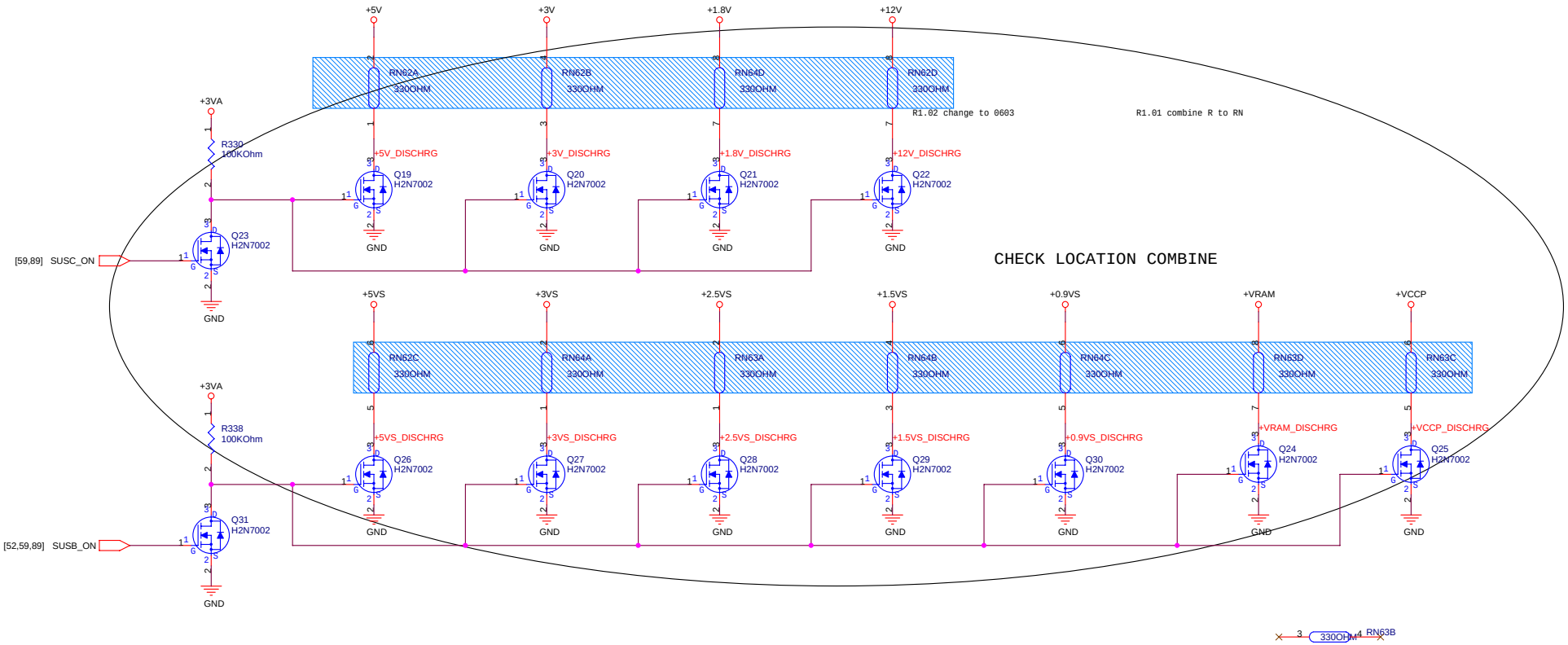
Date: Monday, August 21, 2006 Sheet 39 of 91



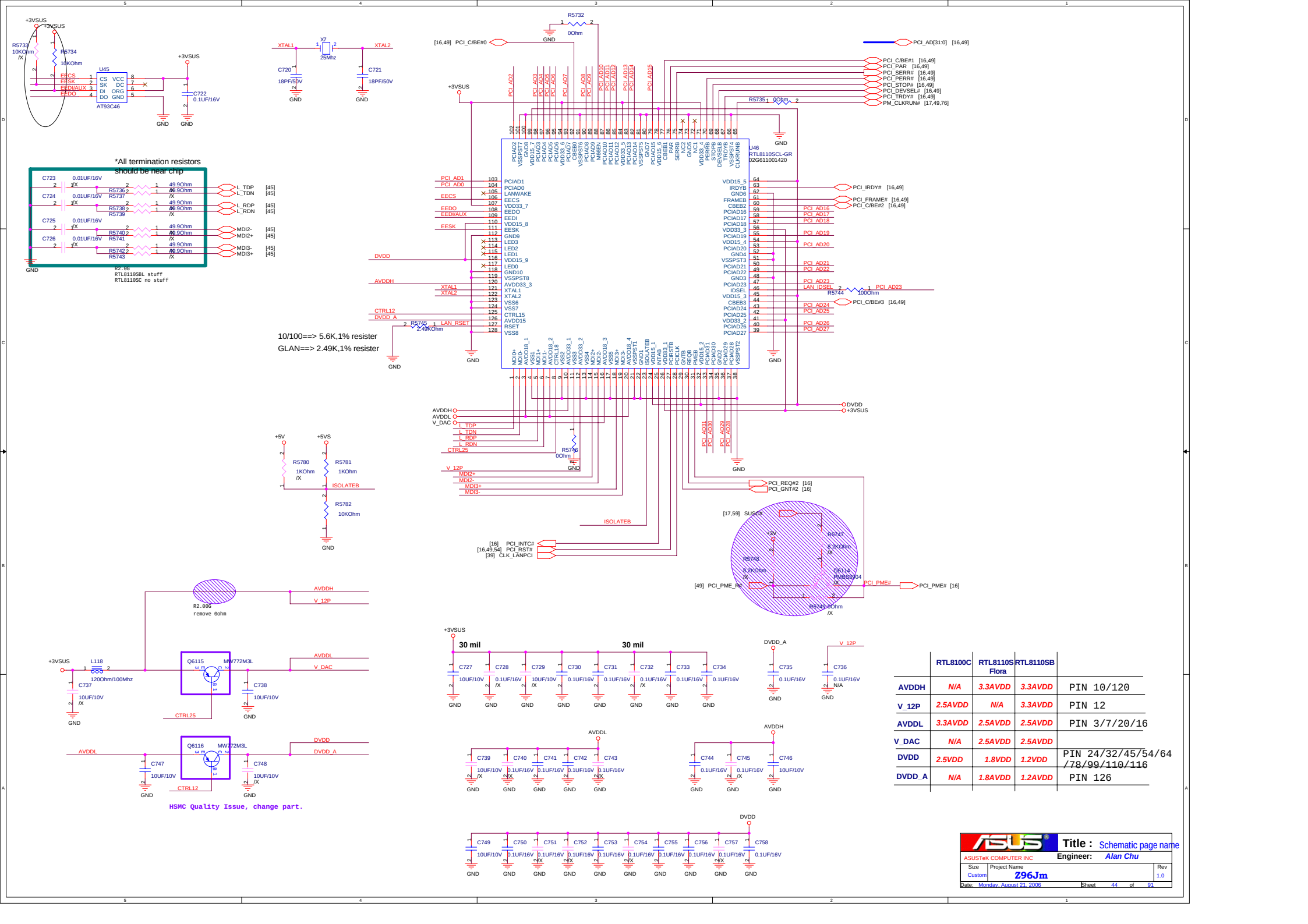
SHUT_DOWN#



ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 41 of 91	



ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 42 of 91	



	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

ASUSTeK COMPUTER INC

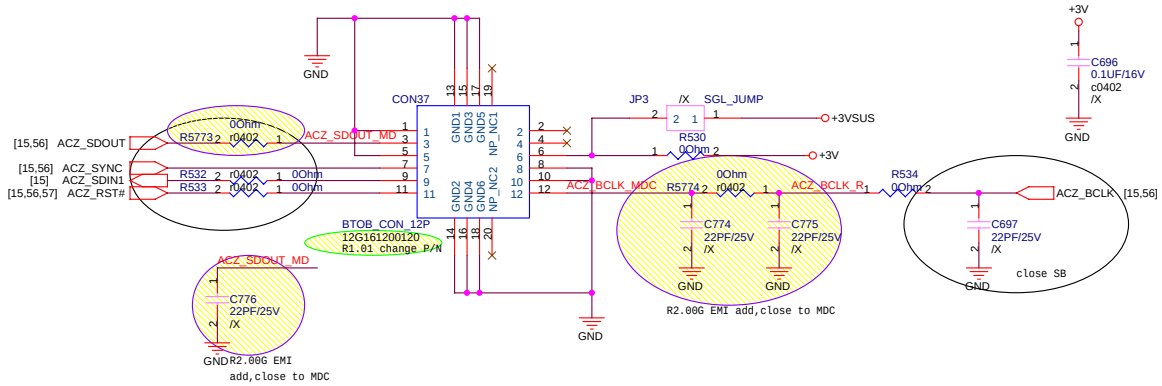
Title : Schematic page name

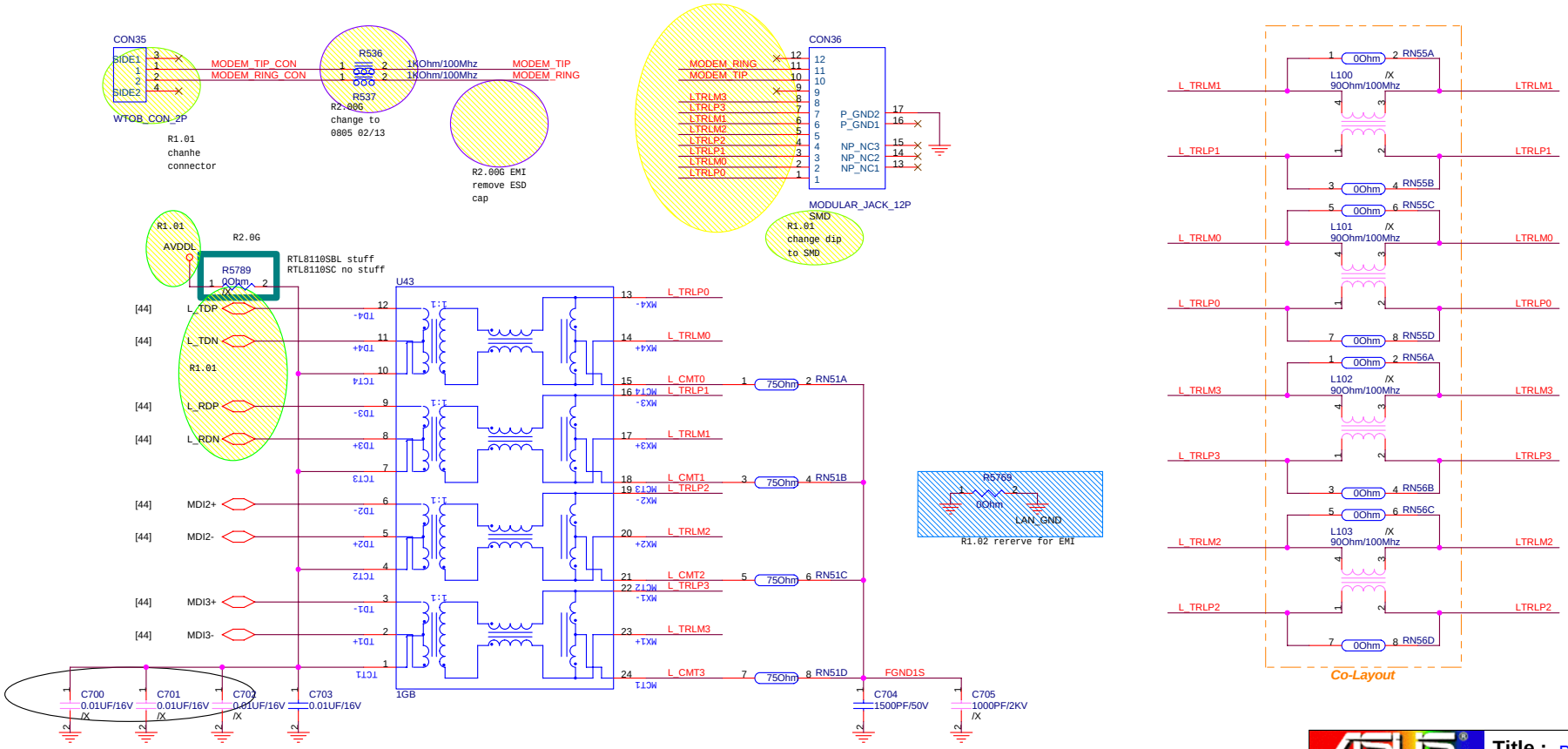
Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96Jm	1.0

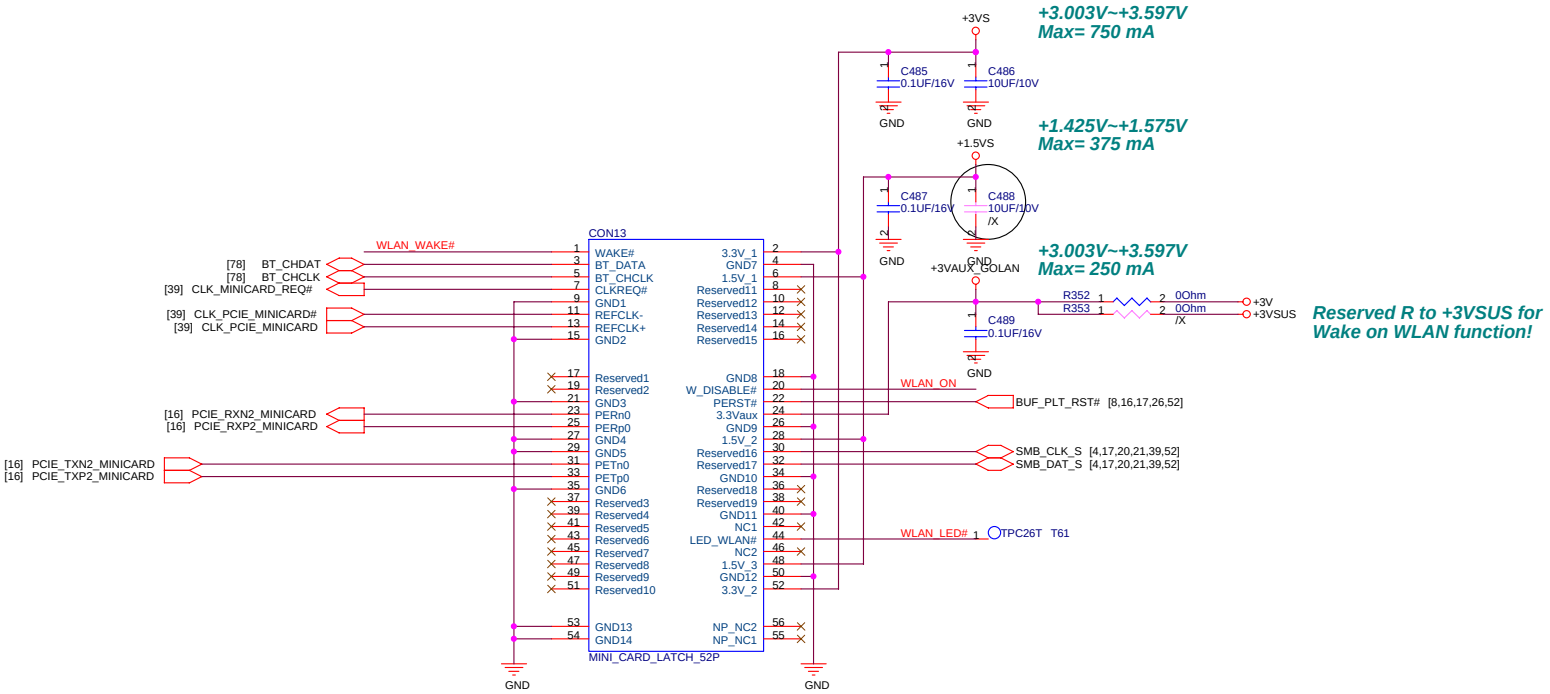
Date: Monday, August 21, 2006 Sheet 44 of 91

MDC CONN.



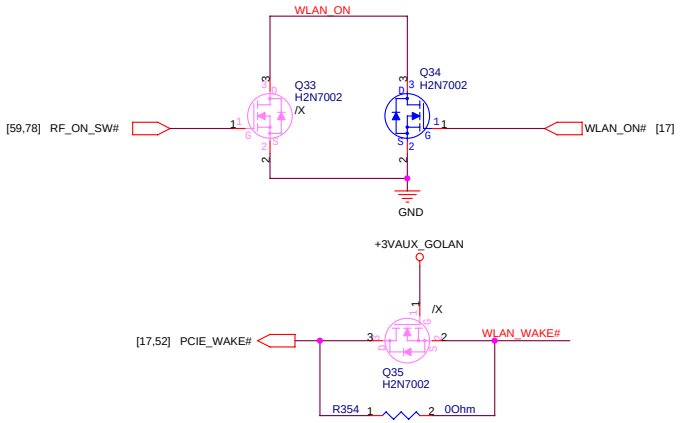


ASUSTeK COMPUTER INC.	Title : RJ45&RJ11	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 45 of 91	

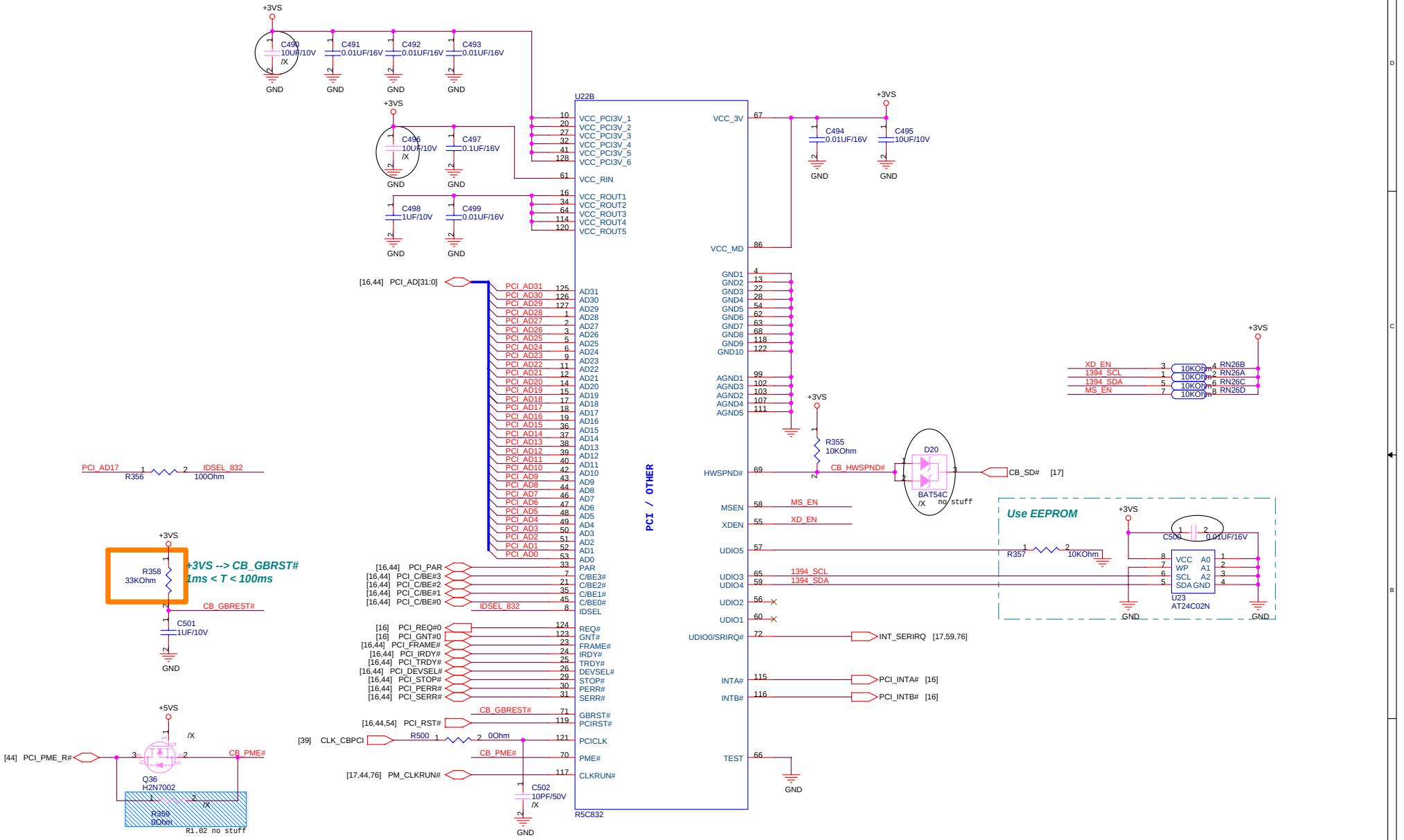


H54 & H56

R1.01 remove
connector,change to
screw



ASUSTeK COMPUTER INC.	Title : MINICARD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 47 of 91	



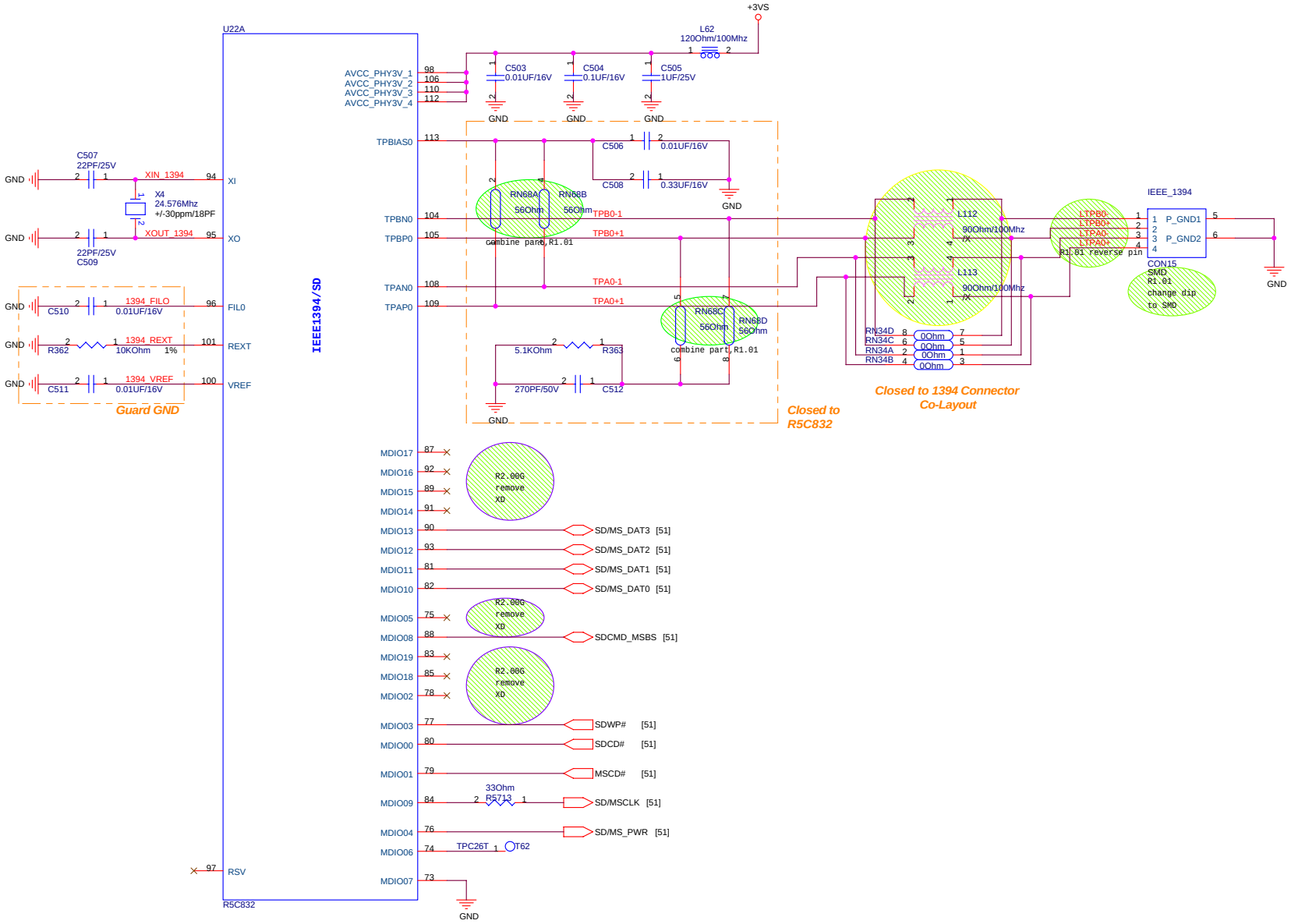
ASUSTeK COMPUTER INC. MB6

Title : CARD1394-R5C832(1)

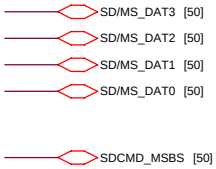
Engineer: *ALAN CHU*

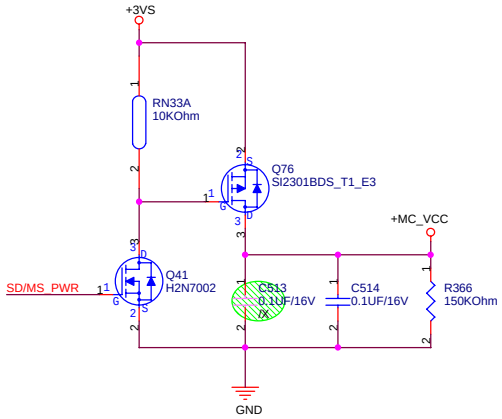
Size	Project Name	Rev
Custom	Z96Jm	1.0

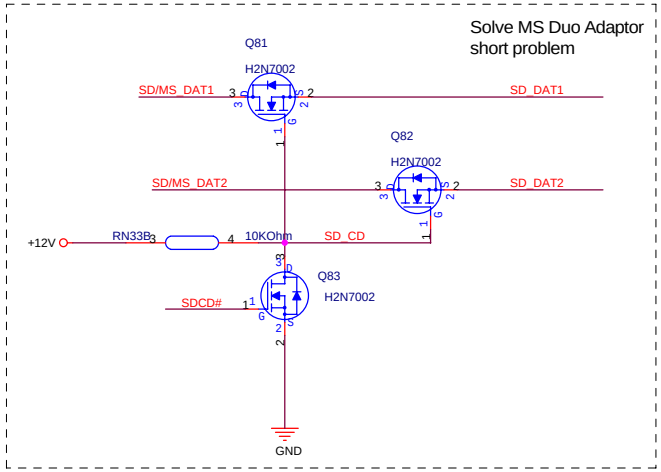
Date: Monday, August 21, 2006 Sheet 49 of 91

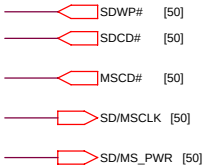


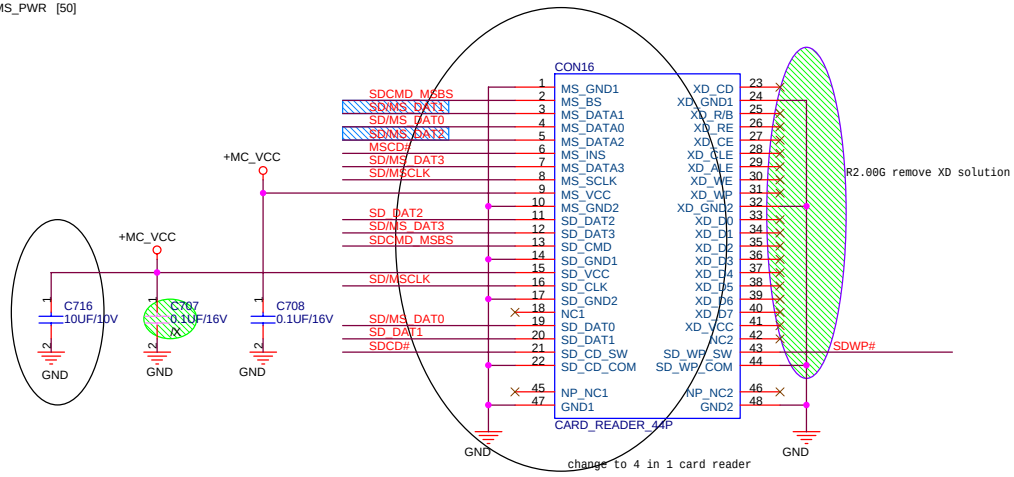
ASUSTeK COMPUTER INC. MB6	Title : CARD1394-R5C832(2)	
	Engineer: ALAN CHU	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 50 of 91	

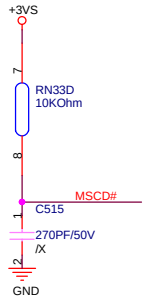




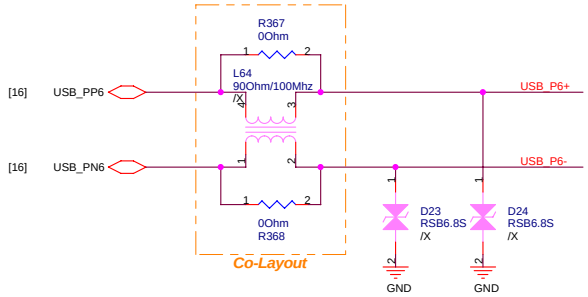


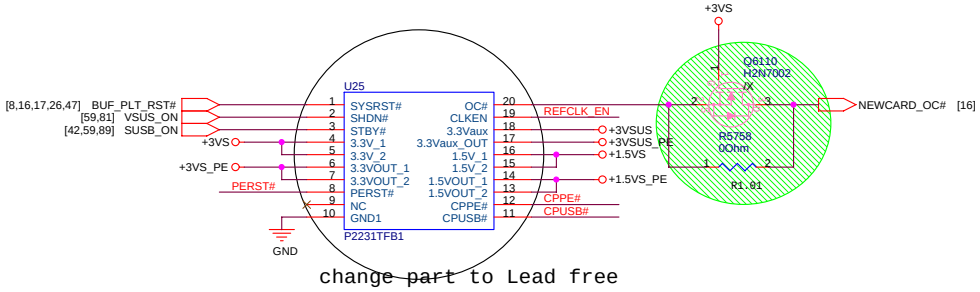


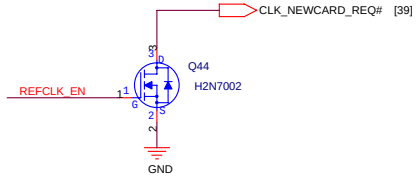




ASUSTeK COMPUTER INC	Title : 4 in 1 CARD READER	
	Engineer: ALAN CHU	
Size: A3	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 51 of 91	

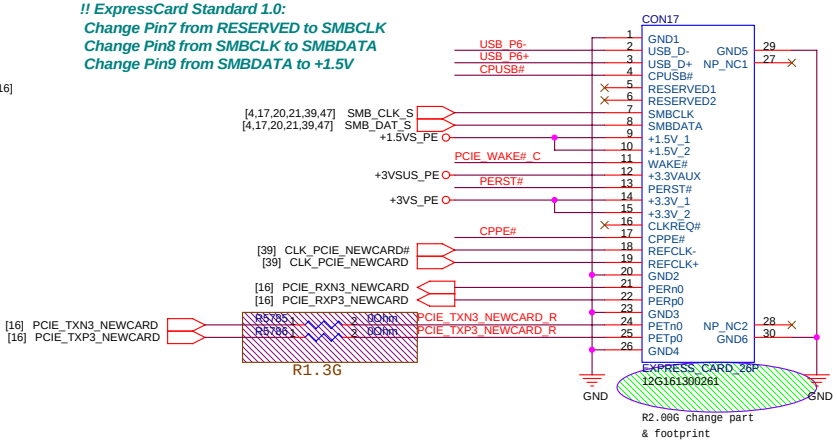




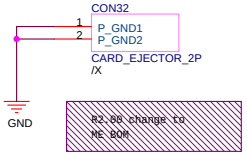


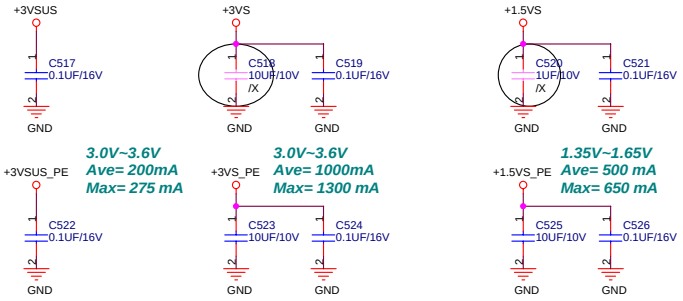
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

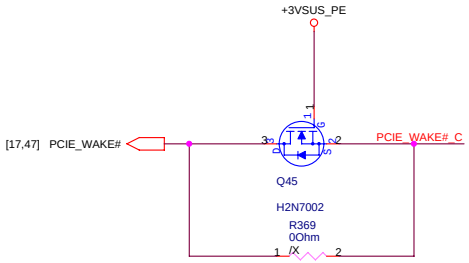
NewCard Header



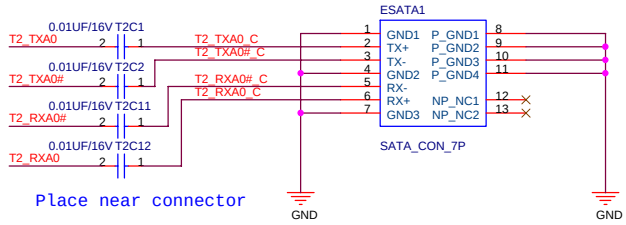
NewCard Ejecter

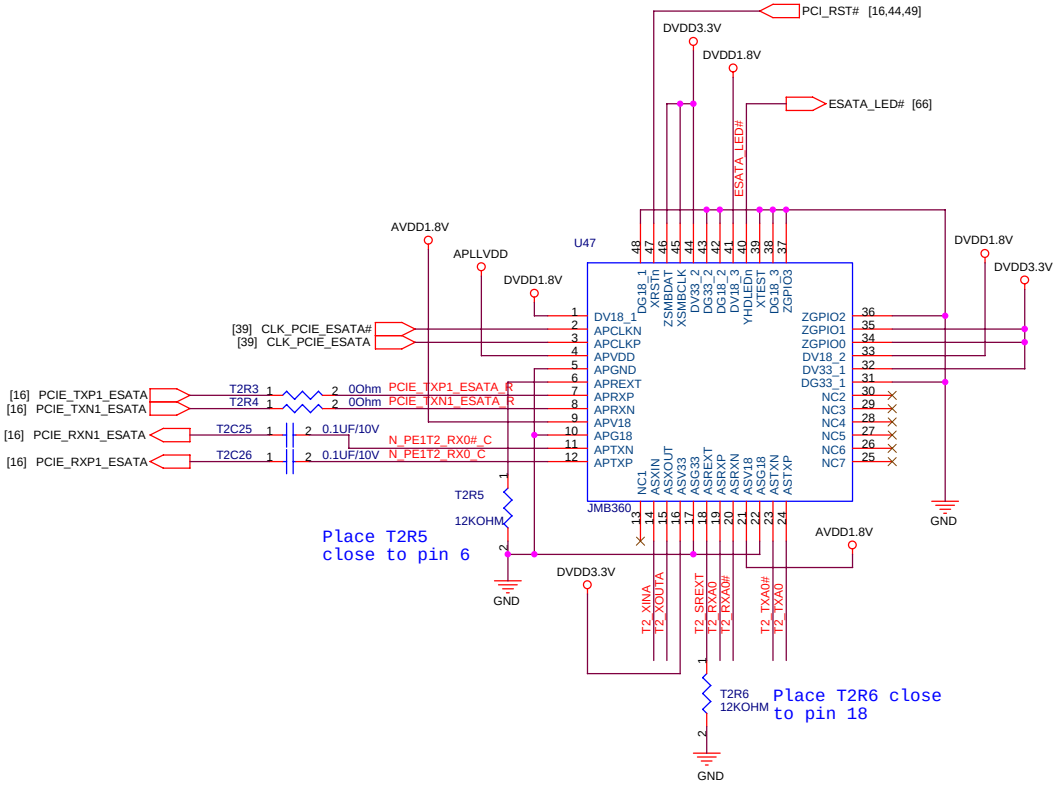


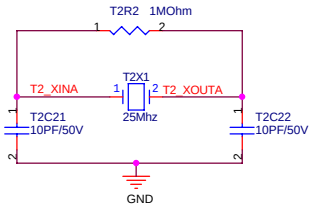


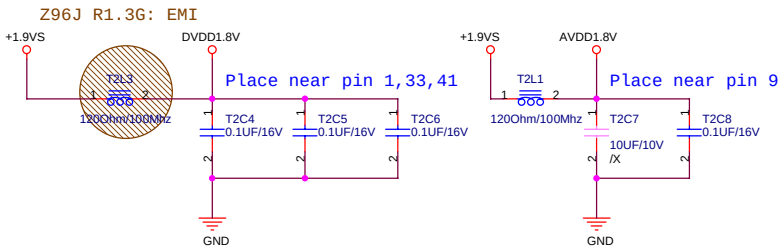


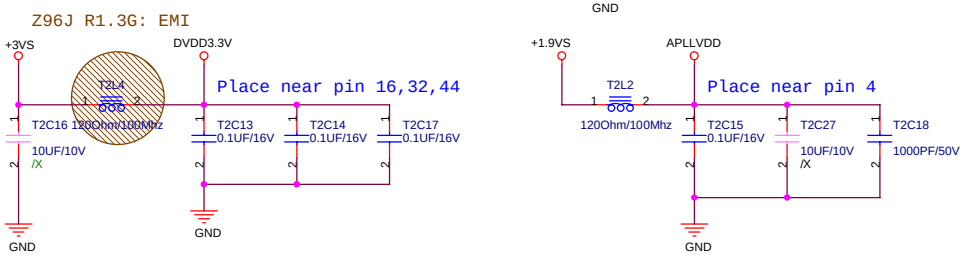
ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 52 of 91	



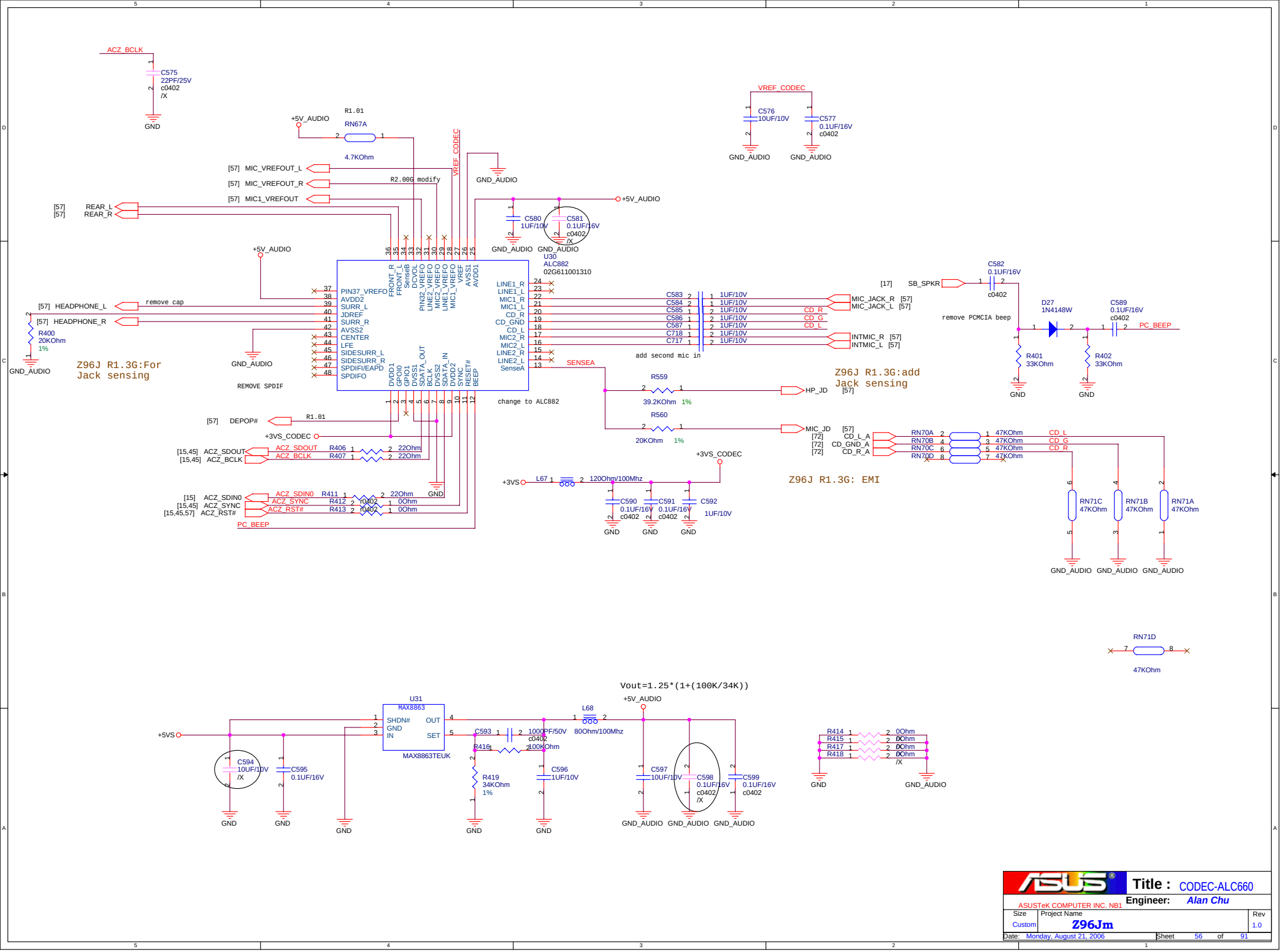


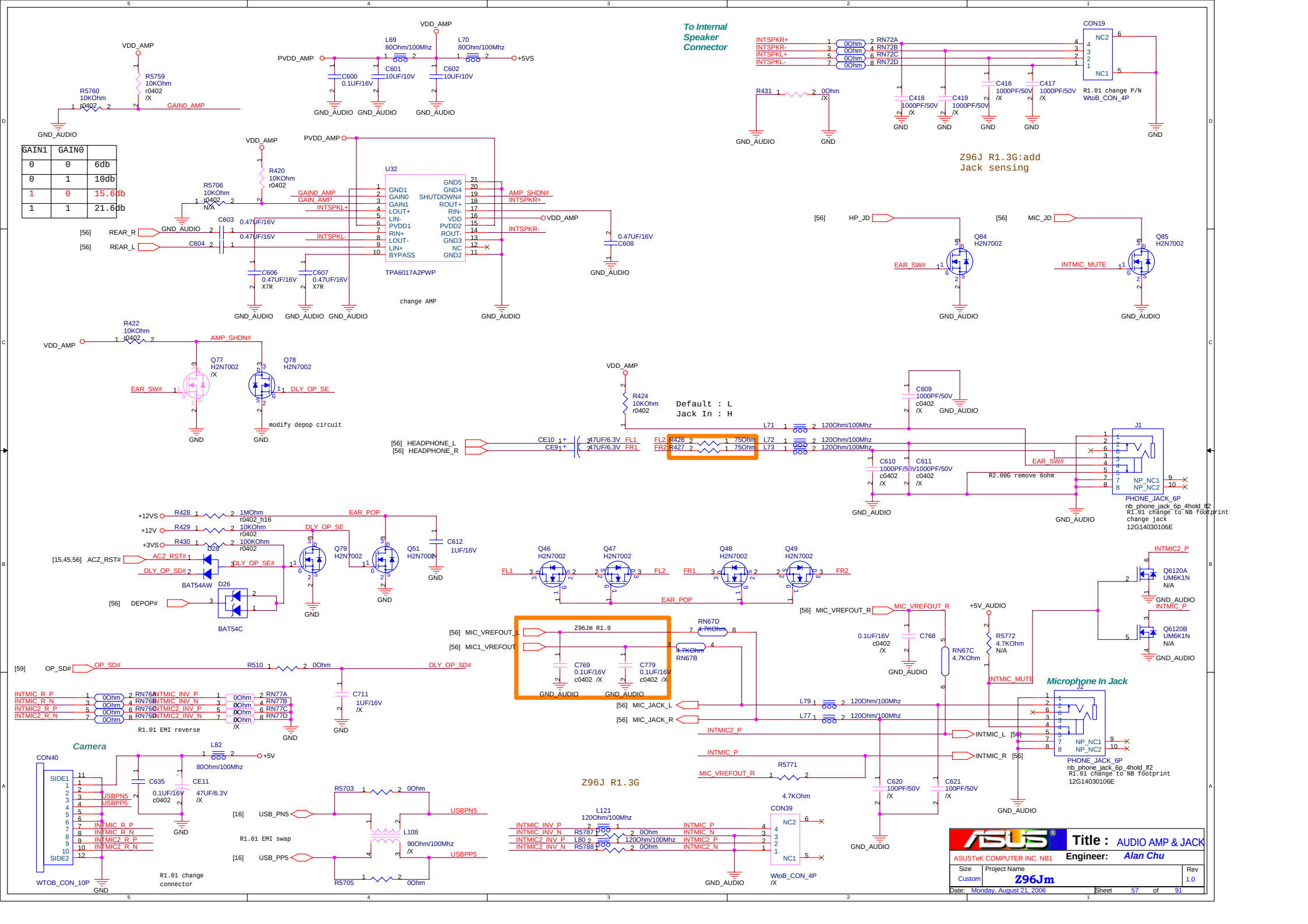


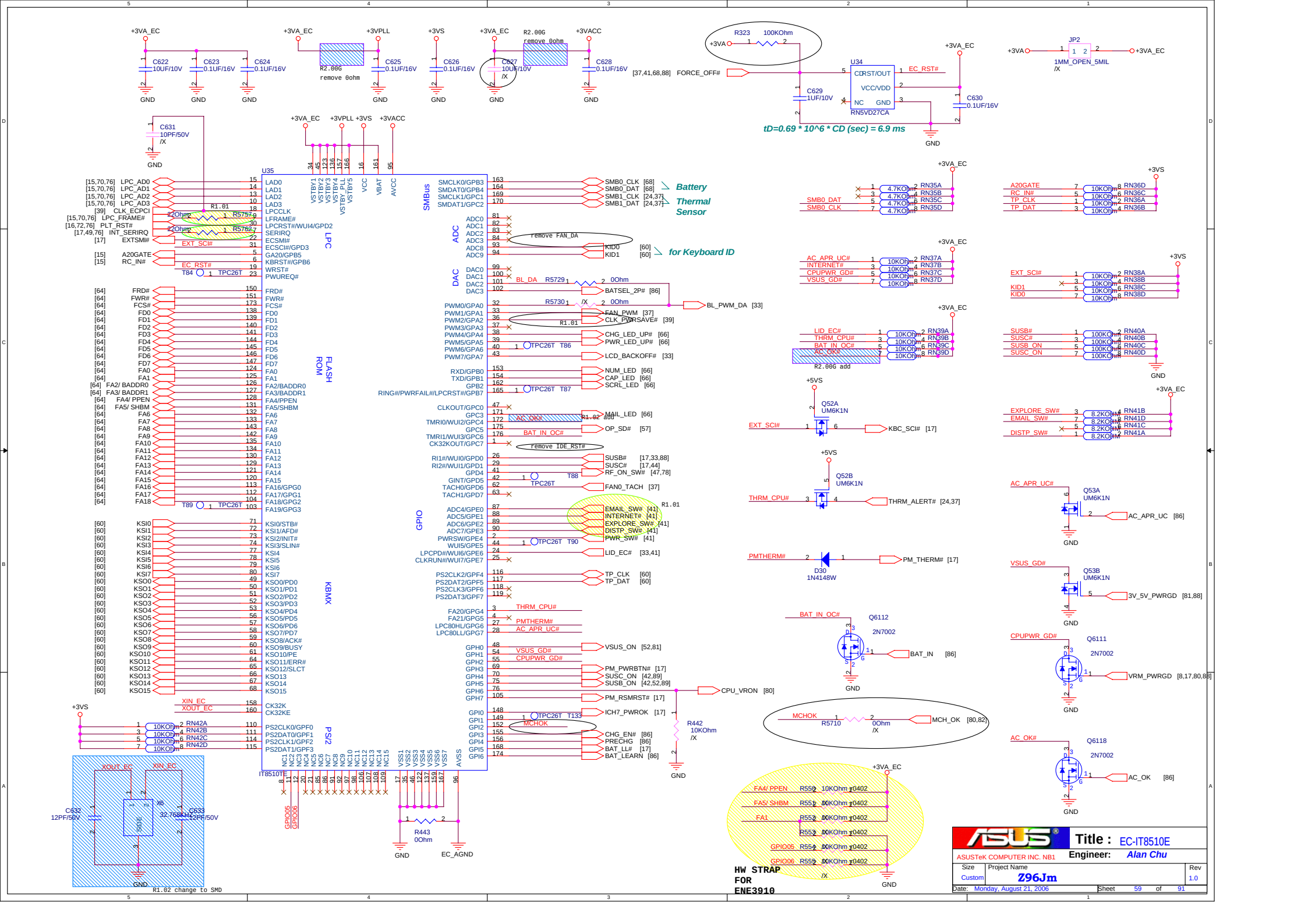




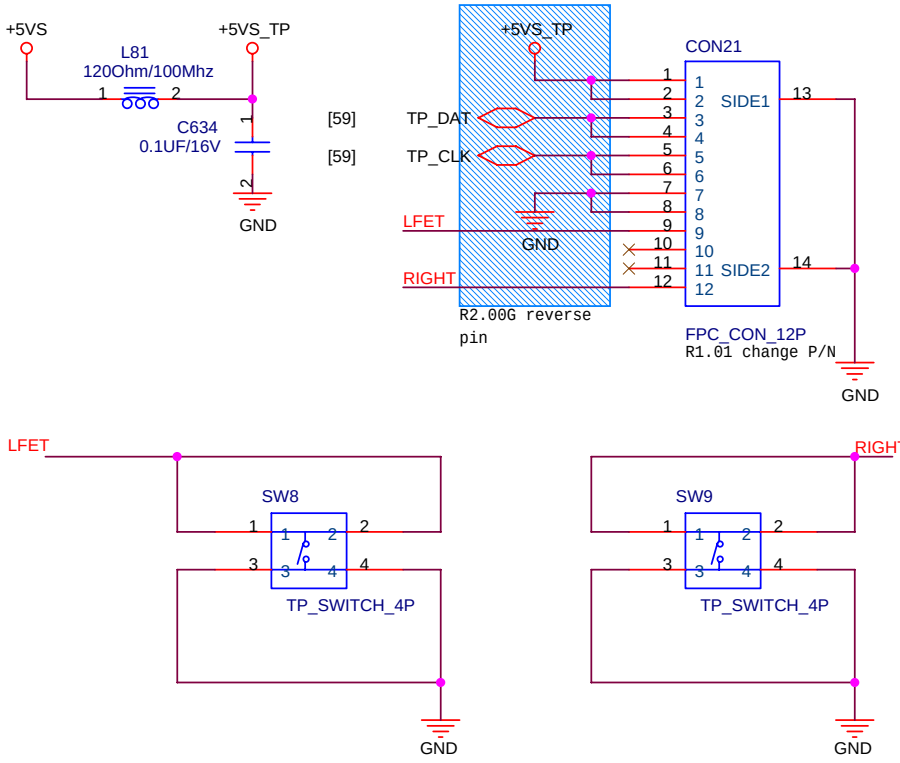
ASUSTeK COMPUTER INC	Title : ESATA JMB360	
	Engineer: Alan Chu	
Size: A3	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 54 of 91	


ACZ_BCLK
C575
22PF/25V
c0402
/X
GND
+5V_AUDIO
R1.01
RN67A
4.7KOhm
[57] MIC_VREFOUT_L
[57] MIC_VREFOUT_R
[57] MIC1_VREFOUT
R2.00G modify
VREF_CODEC
GND_AUDIO
[57] REAR_L
[57] REAR_R
C580
1UF/10V
C581
0.1UF/16V
c0402
/X
U30
ALC882
02G611001310
PIN37_VREFO
AVDD2
SURR_L
JDREF
SURR_R
AVSS2
CENTER
LFE
SIDESURR_L
SIDESURR_R
SPDIFI/EAPD
SPDIFO
FRONT_R
FRONT_L
SenseB
DCVOL
PIN2_VREFO
LINE2_VREFO
MIC2_VREFO
LINE1_VREFO
MIC1_VREFO
VREF
AVSS1
AVDD1
LINE1_R
LINE1_L
MIC1_R
MIC1_L
CD_R
CD_GND
CD_L
MIC2_R
MIC2_L
LINE2_R
LINE2_L
SenseA
DVDD1
GPIO0
GPIO1
DVSS1
SDATA_OUT
BCLK
SDATA_IN2
SDATA_IN
DVDD2
SYNC
RESET#
BEEP
[57] HEADPHONE_L
[57] HEADPHONE_R
remove cap
R400
20KOhm
1%
GND_AUDIO
Z96J R1.3G:For
Jack sensing
REMOVE SPDIF
C583
C584
C585
C586
C587
C718
C717
1UF/10V
CD_R
CD_G
CD_L
add second mic in
MIC_JACK_R [57]
MIC_JACK_L [57]
INTMIC_R [57]
INTMIC_L [57]
SENSEA
R559
39.2KOhm 1%
HP_JD
[57]
change to ALC882
Z96J R1.3G:add
Jack sensing
[17] SB_SPKR
C582
0.1UF/16V
c0402
remove PCMCIA beep
D27
1N4148W
C589
0.1UF/16V
c0402
PC_BEEP
R401
33KOhm
R402
33KOhm
GND
[57] DEPOP#
R1.01
+3VS_CODEC
[15,45] ACZ_SDOUT
[15,45] ACZ_BCLK
ACZ_SDOUT
ACZ_BCLK
R406
R407
22Ohm
R560
20KOhm 1%
MIC_JD [57]
[72] CD_L_A
[72] CD_GND_A
[72] CD_R_A
RN70A
RN70B
RN70C
RN70D
47KOhm
CD_L
CD_G
CD_R
Z96J R1.3G: EMI
RN71C
47KOhm
RN71B
47KOhm
RN71A
47KOhm
GND_AUDIO
[15] ACZ_SDIN0
[15,45] ACZ_SYNC
[15,45,57] ACZ_RST#
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#
R411
R412
R413
0Ohm
PC_BEEP
+3VS
L67
120Ohm/100Mhz
C590
C591
C592
0.1UF/16V
1UF/10V
c0402
RN71D
47KOhm
Vout=1.25*(1+(100K/34K))
U31
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
+5VS
L68
80Ohm/100Mhz
C593
1000PF/50V
100KOhm
R416
R419
34KOhm
1%
C594
10UF/10V
C595
0.1UF/16V
C596
1UF/10V
C597
10UF/10V
C598
0.1UF/16V
C599
0.1UF/16V
R414
R415
R417
R418
0Ohm
Title : CODEC-ALC660
Engineer: Alan Chu
ASUSTeK COMPUTER INC. NB1
Size
Custom
Project Name
Z96Jm
Rev
1.0
Date: Monday, August 21, 2006
Sheet 56 of 91

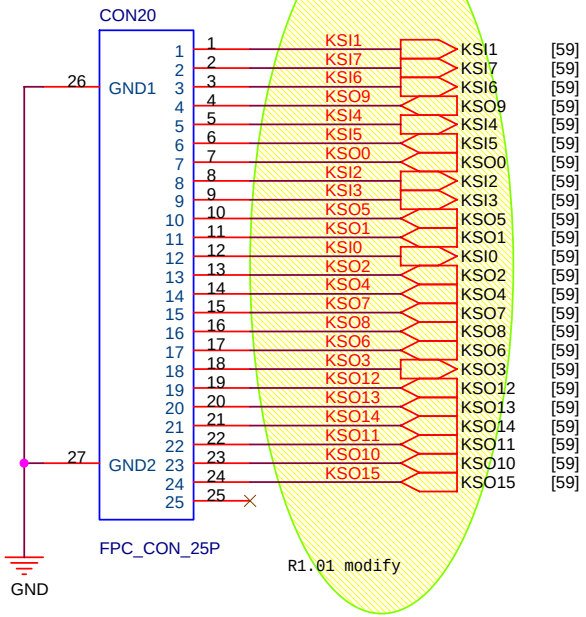

VDD_AMP
R5759 10KOhm r0402 /X
R5760 10KOhm r0402
GAIN0_AMP
GND_AUDIO
L69 80Ohm/100Mhz
L70 80Ohm/100Mhz
PVDD_AMP
+5VS
C600 0.1UF/16V
C601 10UF/10V
C602 10UF/10V
GAIN1 GAIN0 Gain
0 0 6db
0 1 10db
1 0 15.6db
1 1 21.6db
R420 10KOhm r0402
R5706 10KOhm r0402 N/A
GAIN_AMP
INTSPKL+
INTSPKL-
INTSPKR+
AMP_SHDN#
U32
GND1 GAIN0 GAIN1 LOUT+ LIN- PVDD1 RIN+ LOUT- LIN+ BYPASS
GND5 GND4 SHUTDOWN# ROUT+ RIN- VDD PVDD2 ROUT- GND3 NC GND2
TPA6017A2PWP
change AMP
C603 0.47UF/16V
C604 0.47UF/16V
C606 0.47UF/16V X7R
C607 0.47UF/16V X7R
C608 0.47UF/16V
[56] REAR_R
[56] REAR_L
To Internal Speaker Connector
INTSPKR+
INTSPKR-
INTSPKL+
INTSPKL-
RN72A 0Ohm
RN72B 0Ohm
RN72C 0Ohm
RN72D 0Ohm
R431 0Ohm /X
CON19
NC2 NC1
C416 1000PF/50V /X
C417 1000PF/50V /X
C418 1000PF/50V /X
C419 1000PF/50V /X
R1.01 change P/N WtoB_CON_4P
Z96J R1.3G:add Jack sensing
[56] HP_JD
[56] MIC_JD
Q84 H2N7002
Q85 H2N7002
EAR_SW#
INTMIC_MUTE
R422 10KOhm r0402
Q77 H2N7002 /X
Q78 H2N7002
DLY_OP_SE
modify depop circuit
R424 10KOhm r0402
Default : L
Jack In : H
C609 1000PF/50V c0402 /X
L71 120Ohm/100Mhz
L72 120Ohm/100Mhz
L73 120Ohm/100Mhz
CE10 47UF/6.3V FL1
CE9 47UF/6.3V FR1
FL2 R426 75Ohm
FR2 R427 75Ohm
[56] HEADPHONE_L
[56] HEADPHONE_R
C610 1000PF/50V c0402 /X
C611 1000PF/50V c0402 /X
R2.00G remove 0ohm
J1
NP_NC1 NP_NC2
PHONE_JACK_6P
nb_phone_jack_6p_4hold_lf2
R1.01 change to NB footprint
change jack
12G14030106E
+12VS
+12V
+3VS
R428 1MOhm r0402_h16
R429 10KOhm r0402
R430 100KOhm r0402
D28
BAT54AW
D26
BAT54C
ACZ_RST#
DLY_OP_SD#
DLY_OP_SE#
DEPOP#
EAR_POP
Q79 H2N7002
Q51 H2N7002
C612 1UF/16V
Q46 H2N7002
Q47 H2N7002
Q48 H2N7002
Q49 H2N7002
[56] MIC_VREFOUT_R
[56] MIC_VREFOUT_L
[56] MIC1_VREFOUT
Z96Jm R1.0
RN67D 4.7KOhm
RN67B 4.7KOhm
C769 0.1UF/16V c0402 /X
C779 0.1UF/16V c0402 /X
C768 0.1UF/16V c0402 /X
RN67C 4.7KOhm
R5772 4.7KOhm N/A
+5V_AUDIO
INTMIC2_P
INTMIC_P
Q6120A UM6K1N N/A
Q6120B UM6K1N N/A
[59] OP_SD#
R510 0Ohm
C711 1UF/16V /X
INTMIC_R_P
INTMIC_R_N
INTMIC2_R_P
INTMIC2_R_N
RN76A RN76B RN76C RN76D
RN77A RN77B RN77C RN77D
R1.01 EMI reverse
[56] MIC_JACK_L
[56] MIC_JACK_R
L79 120Ohm/100Mhz
L77 120Ohm/100Mhz
INTMIC_L [56]
INTMIC_R [56]
Microphone In Jack
J2
PHONE_JACK_6P
nb_phone_jack_6p_4hold_lf2
R1.01 change to NB footprint
12G14030106E
Camera
CON40
SIDE1 SIDE2
USBPN5
USBPP5
L82 80Ohm/100Mhz
+5V
C635 0.1UF/16V c0402
CE11 47UF/6.3V /X
WTOB_CON_10P
R1.01 change connector
R5703 0Ohm
R5705 0Ohm
L108 90Ohm/100Mhz /X
[16] USB_PN5
[16] USB_PP5
R1.01 EMI swap
Z96J R1.3G
L121 120Ohm/100Mhz
R5787 0Ohm
R5788 0Ohm
L80 120Ohm/100Mhz
INTMIC_INV_P
INTMIC_INV_N
INTMIC2_INV_P
INTMIC2_INV_N
INTMIC_P
INTMIC_N
INTMIC2_P
INTMIC2_N
R5771 4.7KOhm
C620 100PF/50V /X
C621 100PF/50V /X
CON39
WtoB_CON_4P /X
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chu
Size Custom
Project Name Z96Jm
Rev 1.0
Date: Monday, August 21, 2006
Sheet 57 of 91

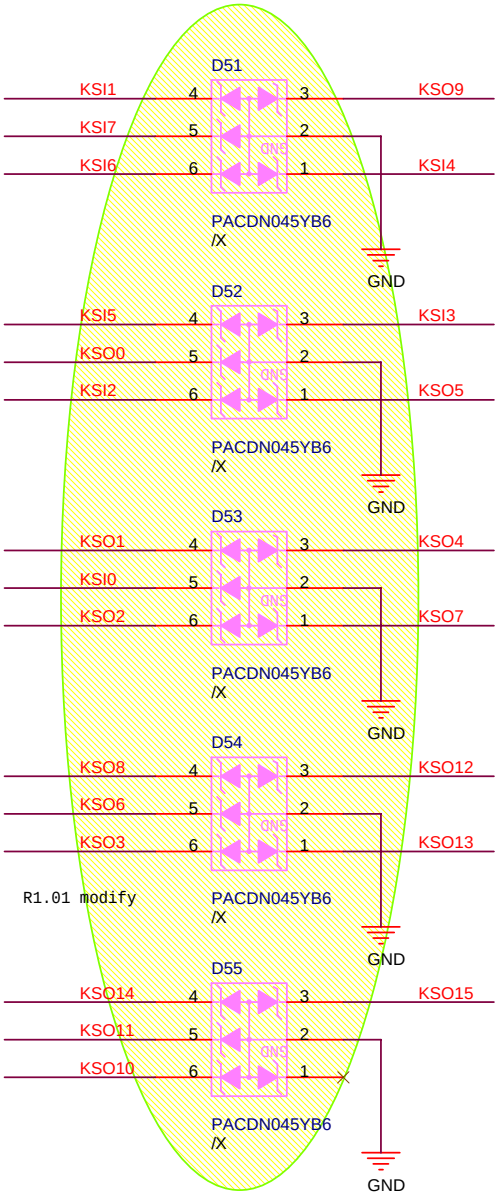

U35
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
SMBus
ADC
DAC
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
HW STRAP FOR ENE3910
R1.02 change to SMD
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chu
Project Name Z96Jm
Size Custom
Rev 1.0
Date: Monday, August 21, 2006
Sheet 59 of 91

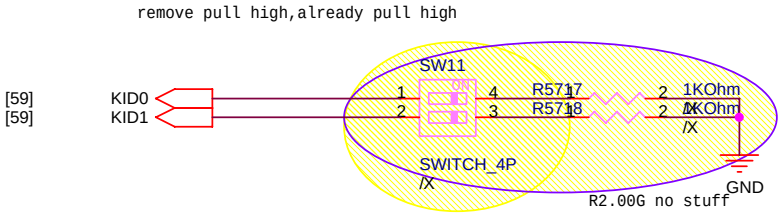
For Touch-Pad



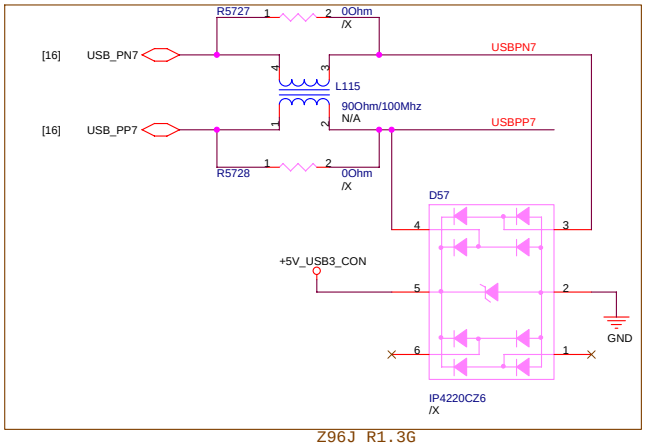
For Keyboard



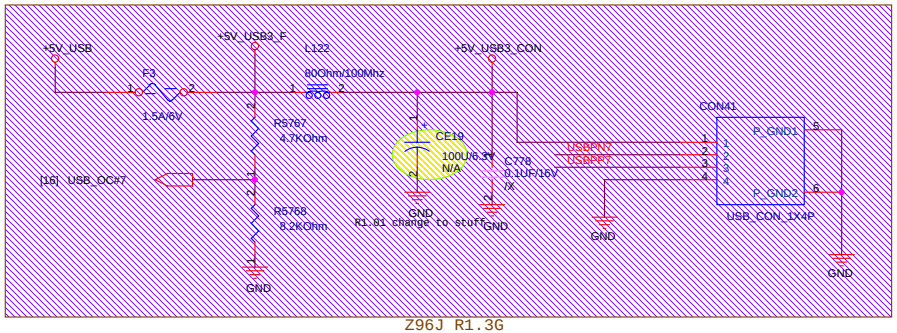




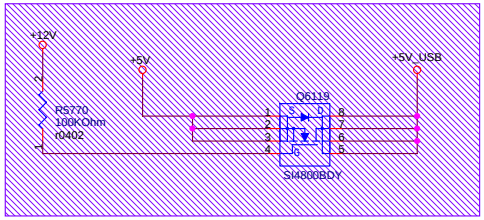
ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB	
	Engineer: ALAN CHU	
Size: A4	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 60 of 91	



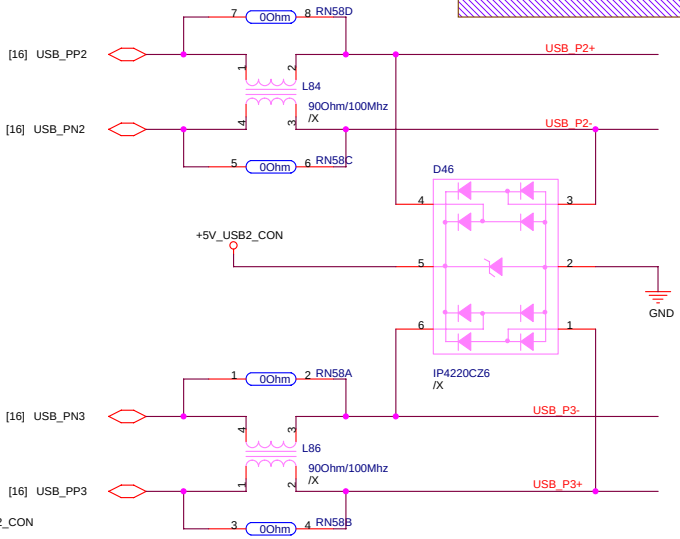
Z96J R1.3G

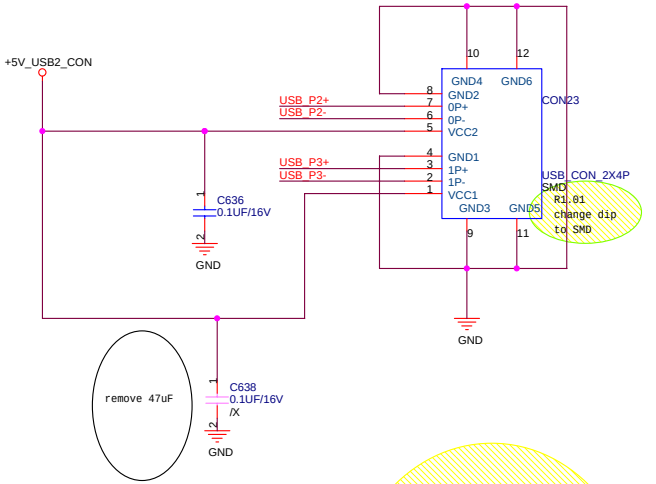


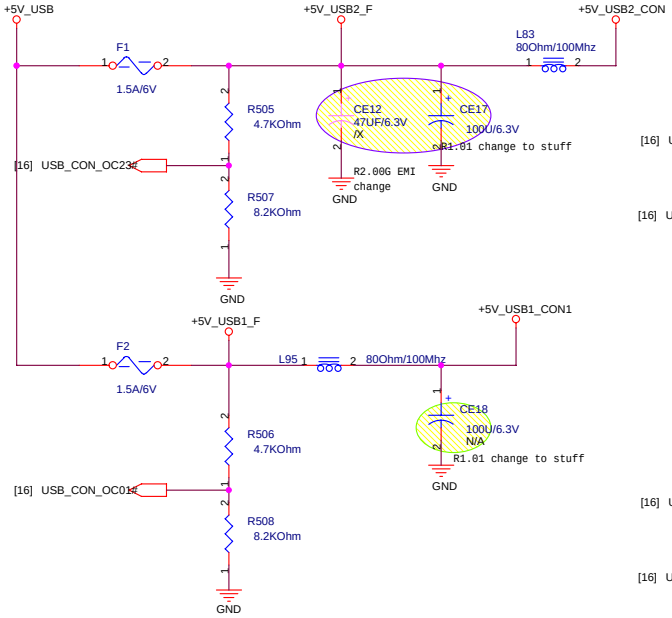
Z96J R1.3G

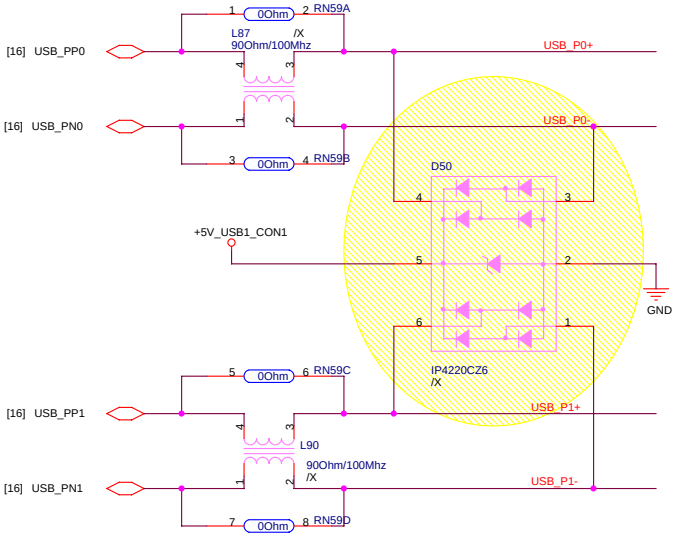


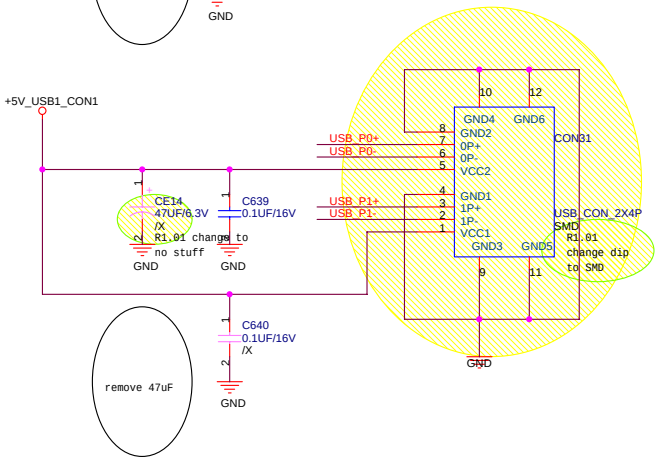
R2.00 add protect circuit





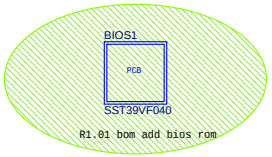






ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 62 of 91	

ISA ROM



EC Hardware Strapping

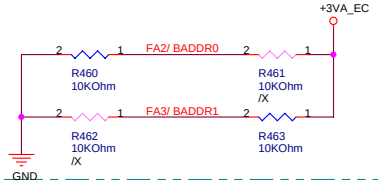
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

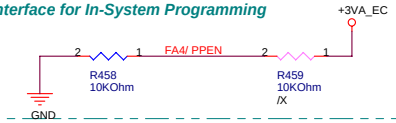


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

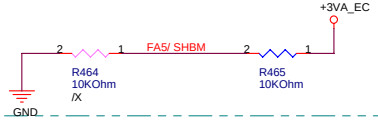
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

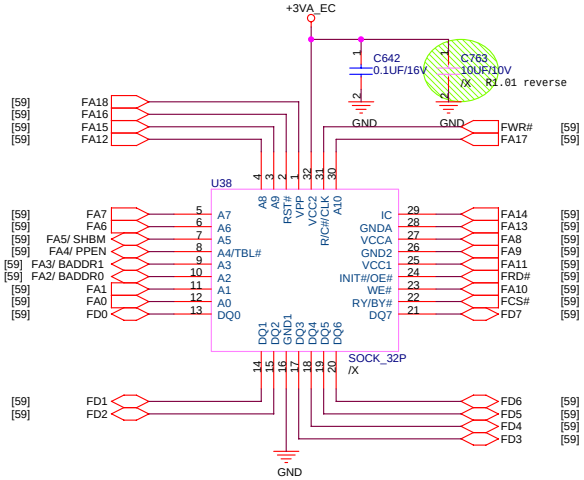


FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

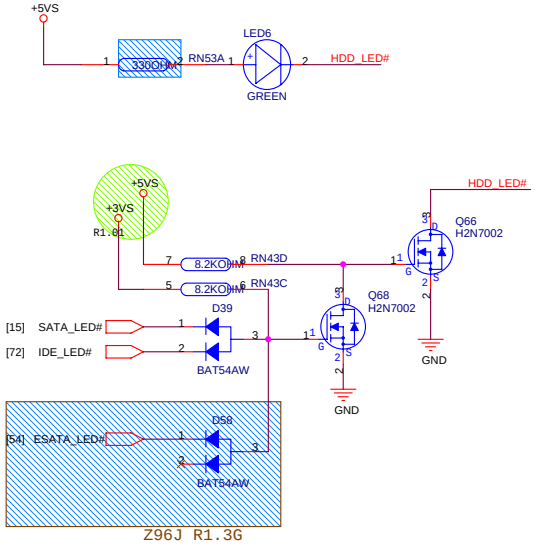




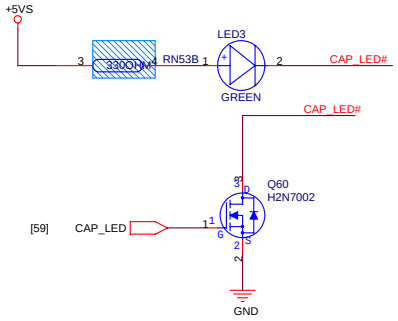
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 64 of 91	

For LED

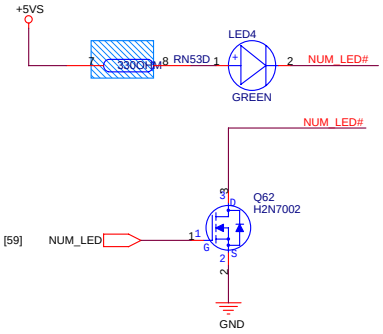
For SATA/IDE LED



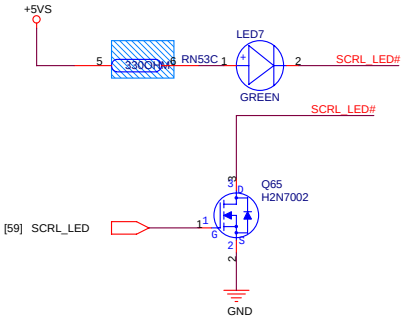
for Cap. Lock



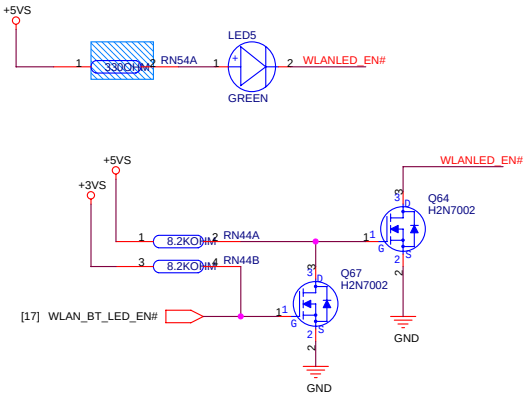
for Num Lock



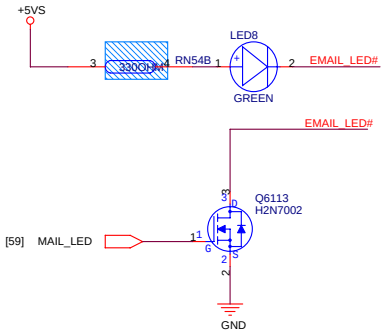
for Scroll Lock



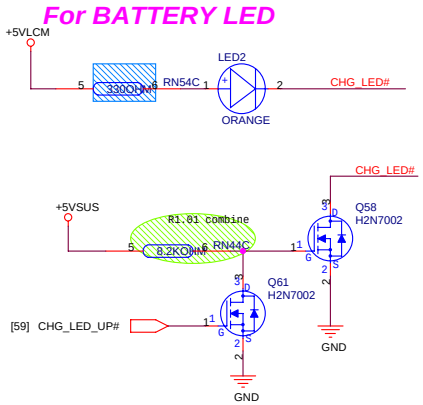
For WireLess LED



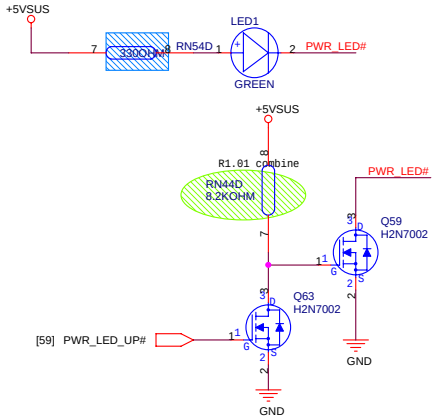
for email



For BATTERY LED

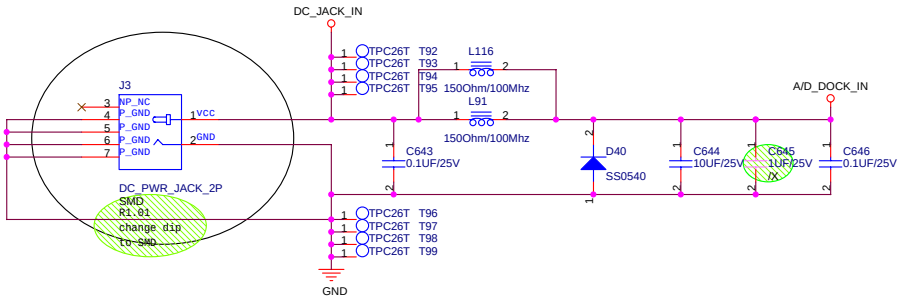


For POWER LED



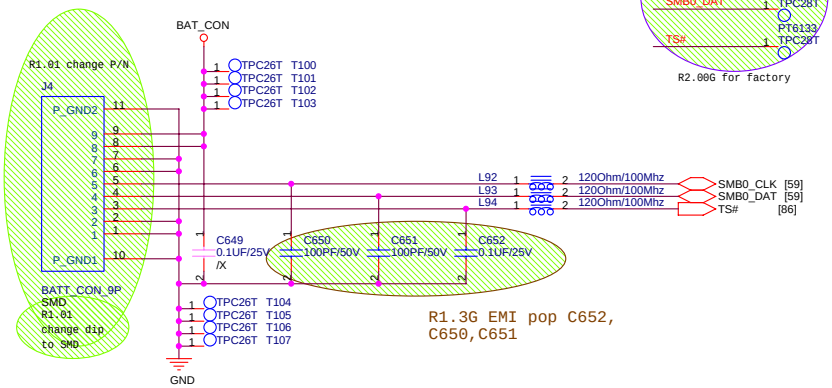
ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 66 of 91	

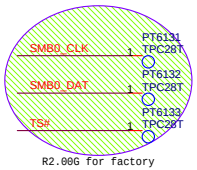
DC IN



remove AC DC detect; no need

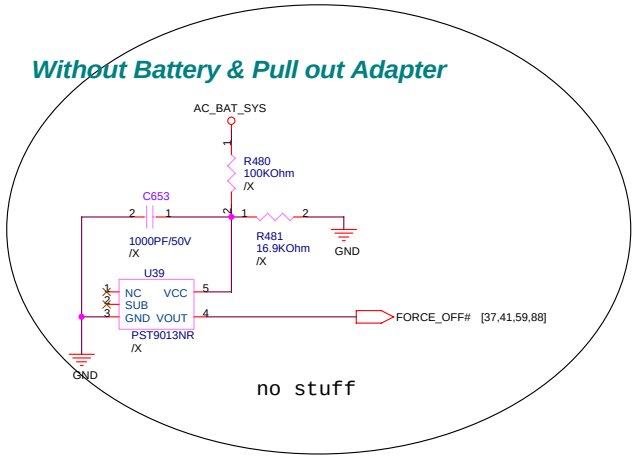
BAT IN





R1.3G EMI pop C652, C650,C651

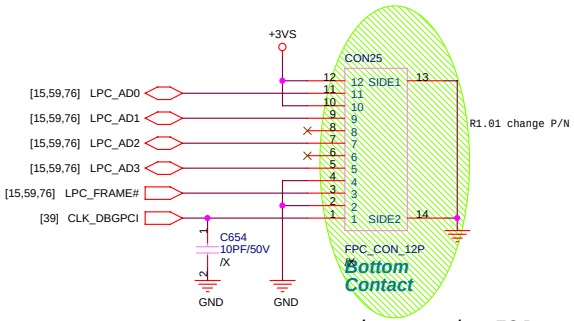
Without Battery & Pull out Adapter



no stuff

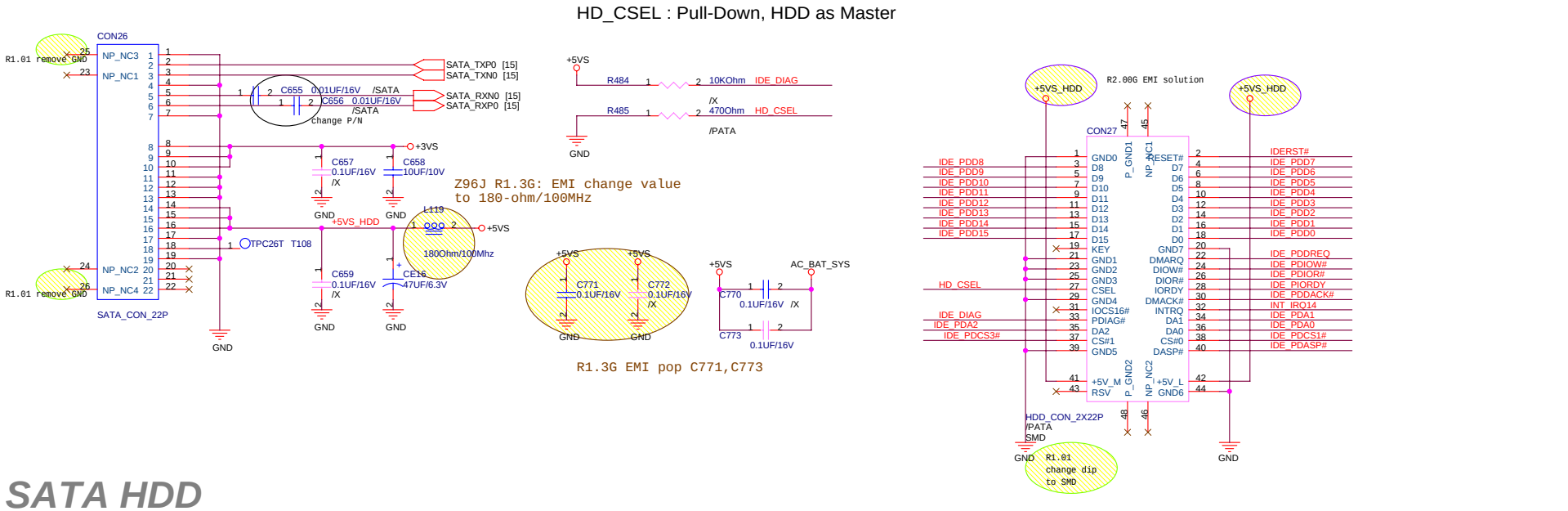
ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 68 of 91	

For Debug



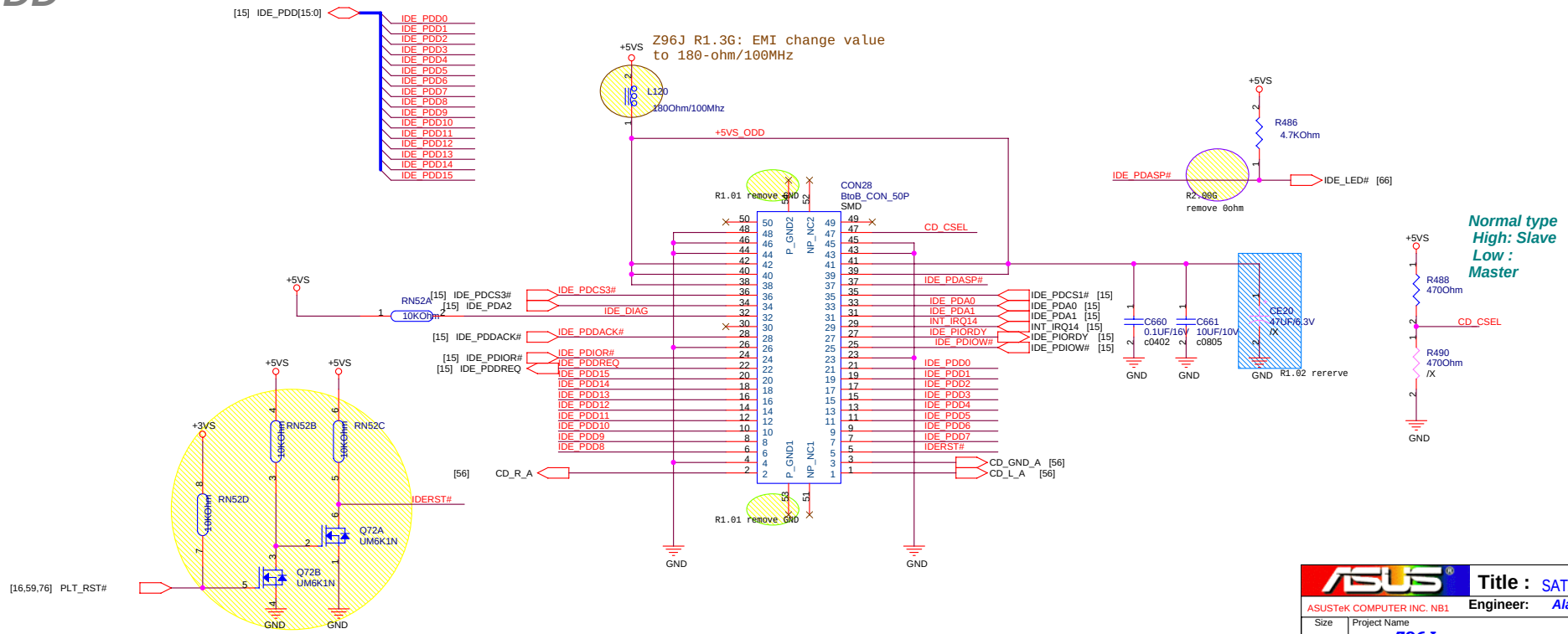
pin swap;by F3J

ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 70 of 91	



SATA HDD

ODD



ASUSTeK COMPUTER INC. NB1	Title : SATA-HDD & ODD	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 72 of 91	

H1
2DRILL_D71N_D106N

H2
2DRILL_D71N_D106N

H3
ct217b47d4Tpt217
13GN7510M270
GND

H4
CT47CB79D47_NS
GND

H5
C354D106N

H6
C354D106N

H7
C354D106N

H8
C354D106N

PAD1
SMD394X197
GND

PAD2
SMD394X197
GND

PAD3
SMD394X197
GND

PAD4
SMD394X197
GND

PAD5
SMD394X197
GND

PAD6
SMD1248X197_PT
GND

H9 C354D106N
H10 C354D106N
H11 C354D106N
H12 C354D106N
H13 C354D106N
H14 C354D106N
H15 C354D106N
H16 C354D106N
H17 C354D106N
H18 C354D106N

PAD7
SMD1890X197_PT
GND

PAD8
SMD197X1803
GND

H19 C354D106N
H20 C354D106N
H21 C354D106N
H22 C354D106N
H25 C354D106N
H26 C354D106N
H27 C354D106N
H28 C354D106N

FOR SCREW HOLE

H29
ct217b47d4Tpt217
13GN7510M270
GND

H30
CT47CB79D47_NS
GND

H31
ct217b47d4Tpt217
13GN7510M270
GND

H32
CT47CB79D47_NS
GND

H34
CT47CB79D47_NS
GND

H33
ct217b47d4Tpt217
13GN7510M270
GND

FOR SCREW HOLE

H35 CT315B163I183D163 GND
H36 CT315B163I183D163 GND
H37 CT315B163I183D163 GND
H38 CT315B163I183D163 GND
H39 CT315B163I183D163 GND
H40 CT315B163I183D163 GND
H41 CT315B163I183D163 GND
H42 CT315B163I183D163 GND
H62 CT315B163I183D163 GND
H63 CT315B163I183D163 GND

H45 CT315B163I183D163 GND
H46 CT315B163I183D163 GND

H47_C236
GND

H48
2DRILL_D106N_D71N

H49
2DRILL_D71N_D106N

H43 CT315B163I183D163 GND
H44 CT315B163I183D163 GND

H50
C354D106N

H51
C354D106N

R2.006 modify

H52
2DRILL_D87N_D106N

H53
2DRILL_D87N_D106N

H54
ct217b47d4Tpt217
GND

H55
CT47CB79D47_NS
GND

H56
ct217b47d4Tpt217
GND

H57
CT47CB79D47_NS
GND

H61
CT256B126I146D126
GND

H60
CT256B126I146D126
GND

H59
CT256B126I146D126
GND

H58
CT256B126I146D126
GND

ASUSTeK COMPUTER INC

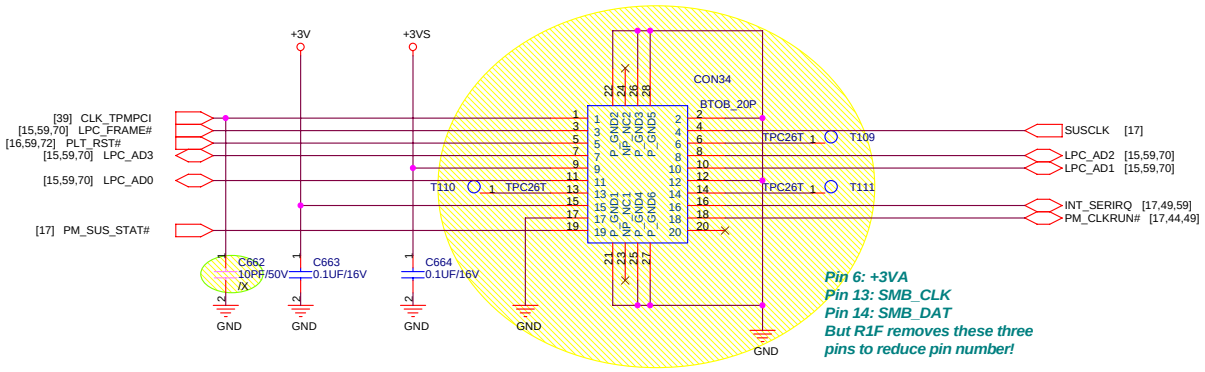
Title : SREW HOLE

Engineer: *ALan Chu*

Size	Project Name	Rev
Custom	Z96Jm	1.0

Date: Monday, August 21, 2006 Sheet 74 of 91

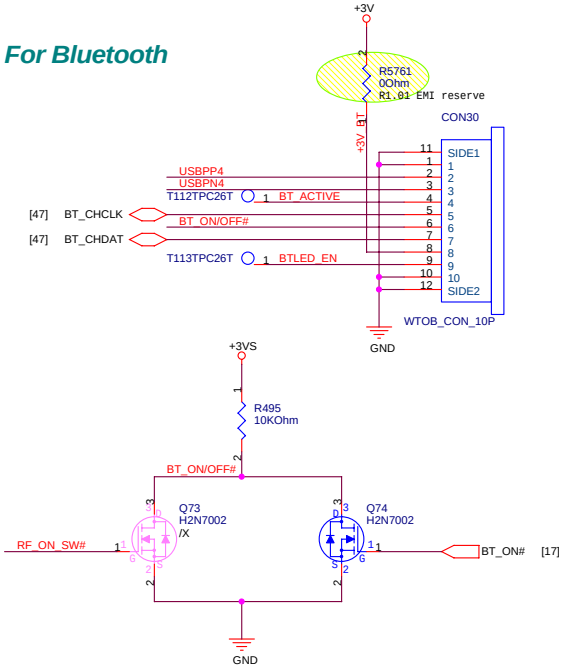
For TPM Module



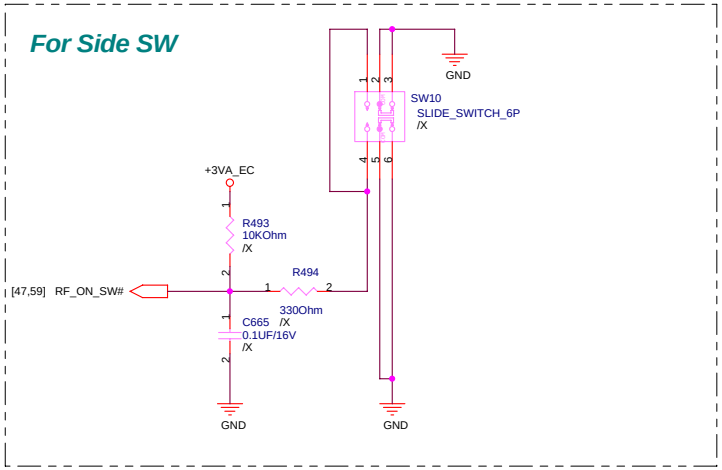
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

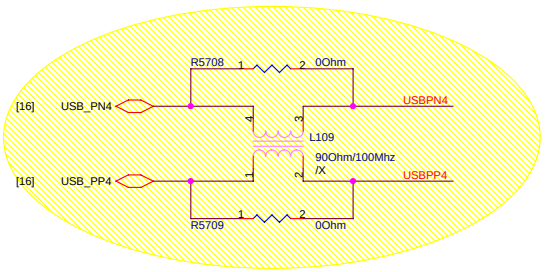
ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Alan Chu	
Size: Custom	Project Name: Z96Jm	Rev: 1.0
Date: Monday, August 21, 2006	Sheet 76 of 91	

For Bluetooth

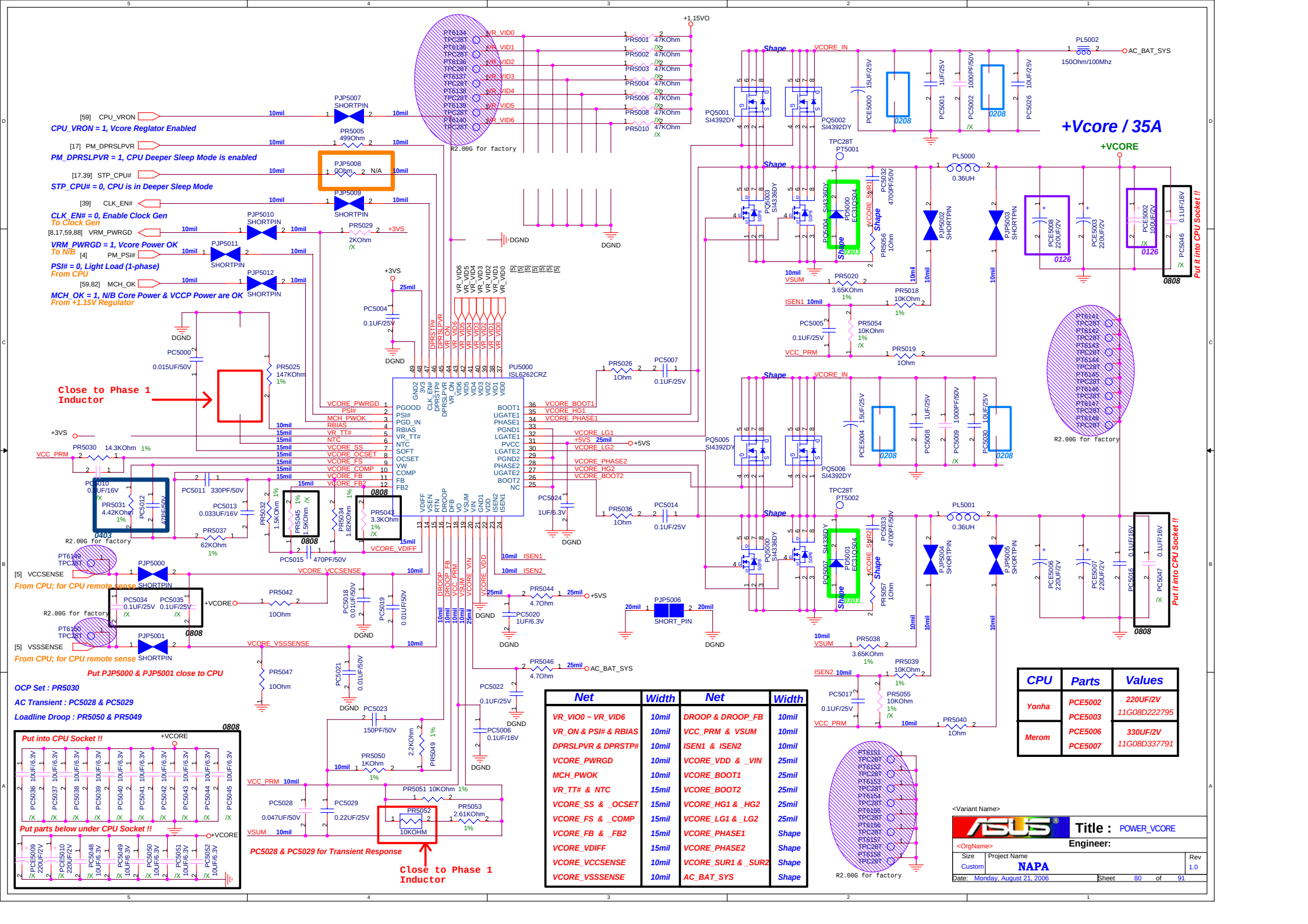


For Side SW



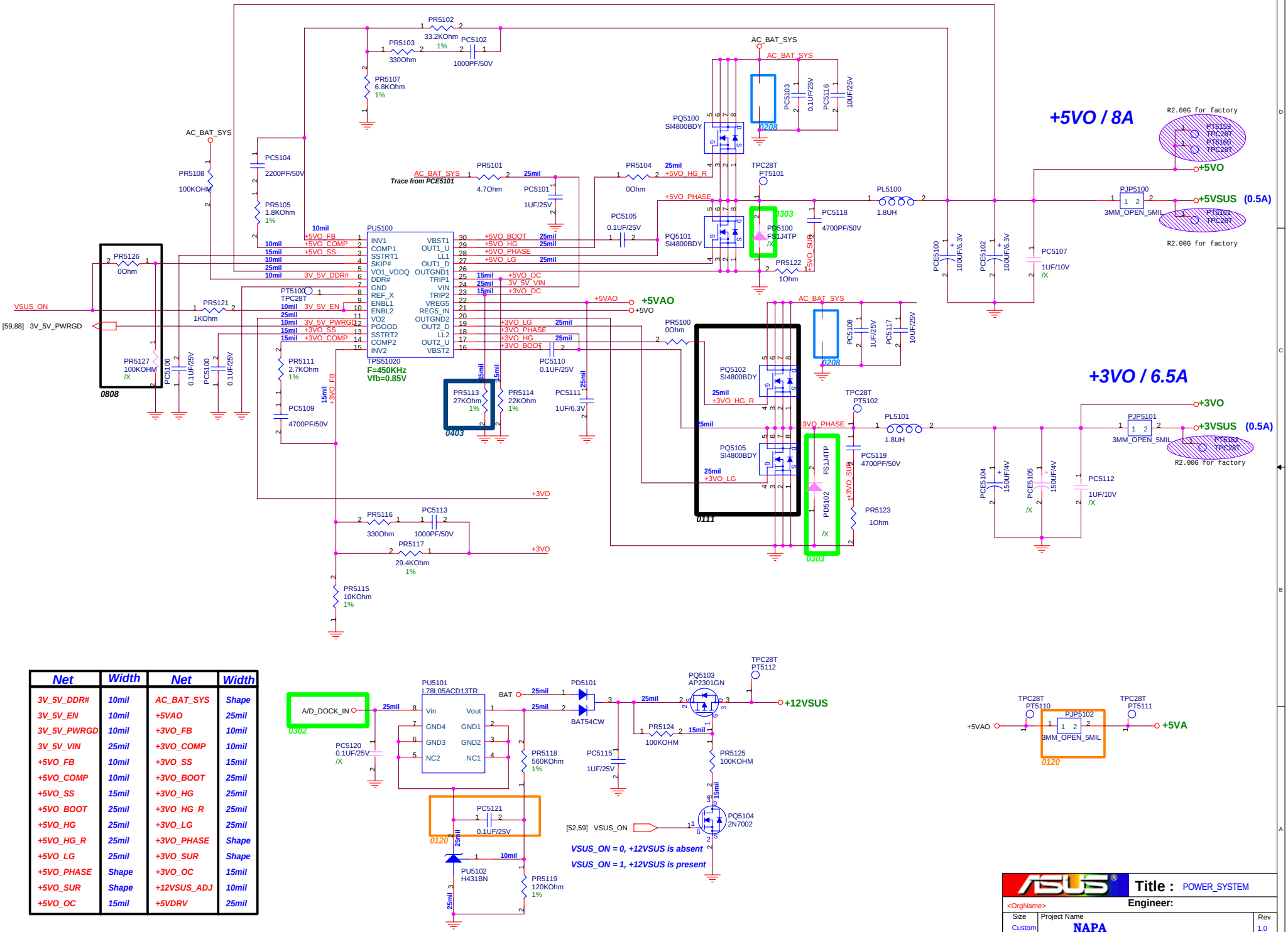


ASUSTeK COMPUTER INC	Title : Blue Tooth		
	Engineer: Alan Chu		
Size: Custom	Project Name: Z96Jm		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 78 of 91		



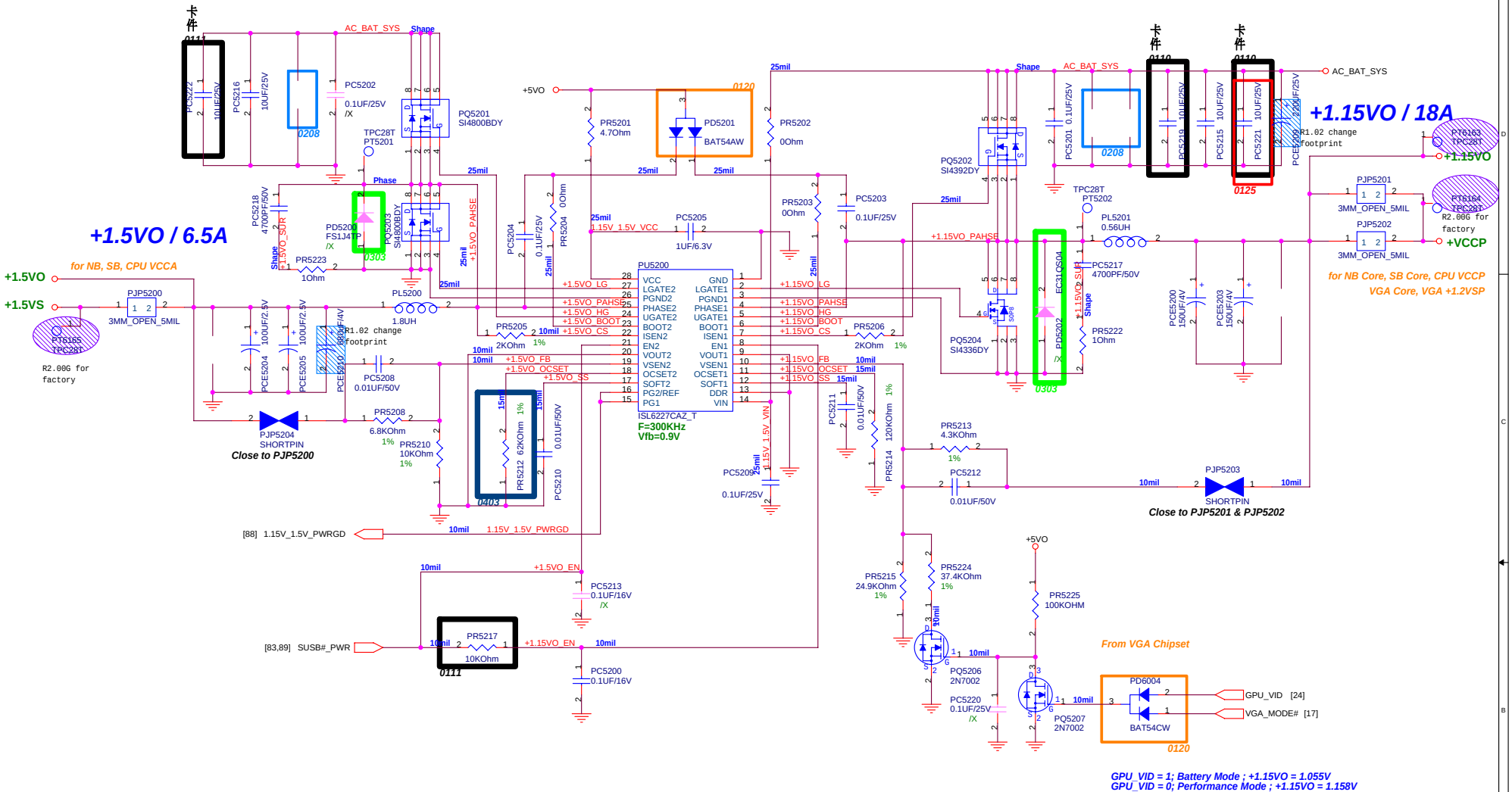
CPU	Parts	Values
Yonha	PCE5002	220UF/2V
	PCE5003	11G08D222795
Merom	PCE5006	330UF/2V
	PCE5007	11G08D337791

Net	Width	Net	Width
VR_VID0 ~ VR_VID6	10mil	DROOP & DROOP_FB	10mil
VR_ON & PSI# & RBIAS	10mil	VCC_PRM & VSUM	10mil
DPRSLPVR & DPRSTP#	10mil	ISEN1 & ISEN2	10mil
VCORE_PWRGD	10mil	VCORE_VDD & _VIN	25mil
MCH_PWOK	10mil	VCORE_BOOT1	25mil
VR_TT# & NTC	15mil	VCORE_BOOT2	25mil
VCORE_SS & _OCSET	15mil	VCORE_HG1 & _HG2	25mil
VCORE_FS & _COMP	15mil	VCORE_LG1 & _LG2	25mil
VCORE_FB & _FB2	15mil	VCORE_PHASE1	Shape
VCORE_VDIFF	15mil	VCORE_PHASE2	Shape
VCORE_VCCSENSE	10mil	VCORE_SUR1 & _SUR2	Shape
VCORE_VSSSENSE	10mil	AC_BAT_SYS	Shape



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

ASUS	Title : POWER_SYSTEM		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 1.0
Date: Monday, August 21, 2006	Sheet 81 of 91		



Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

ASUS

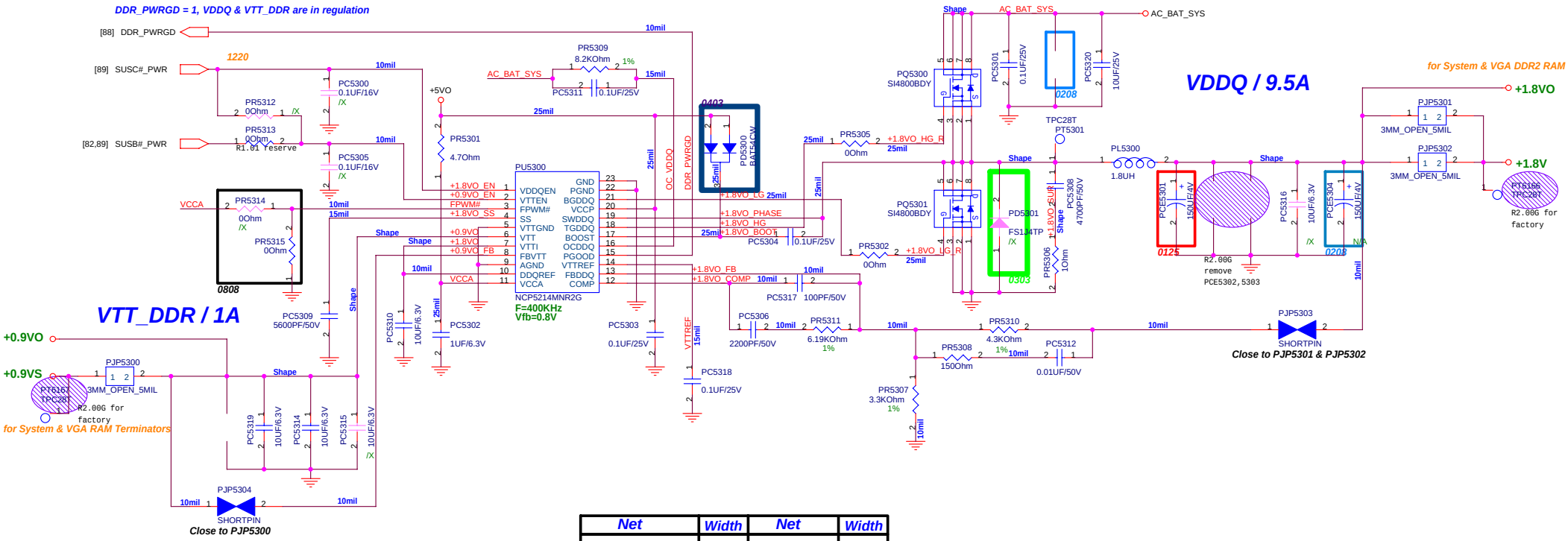
Title : POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

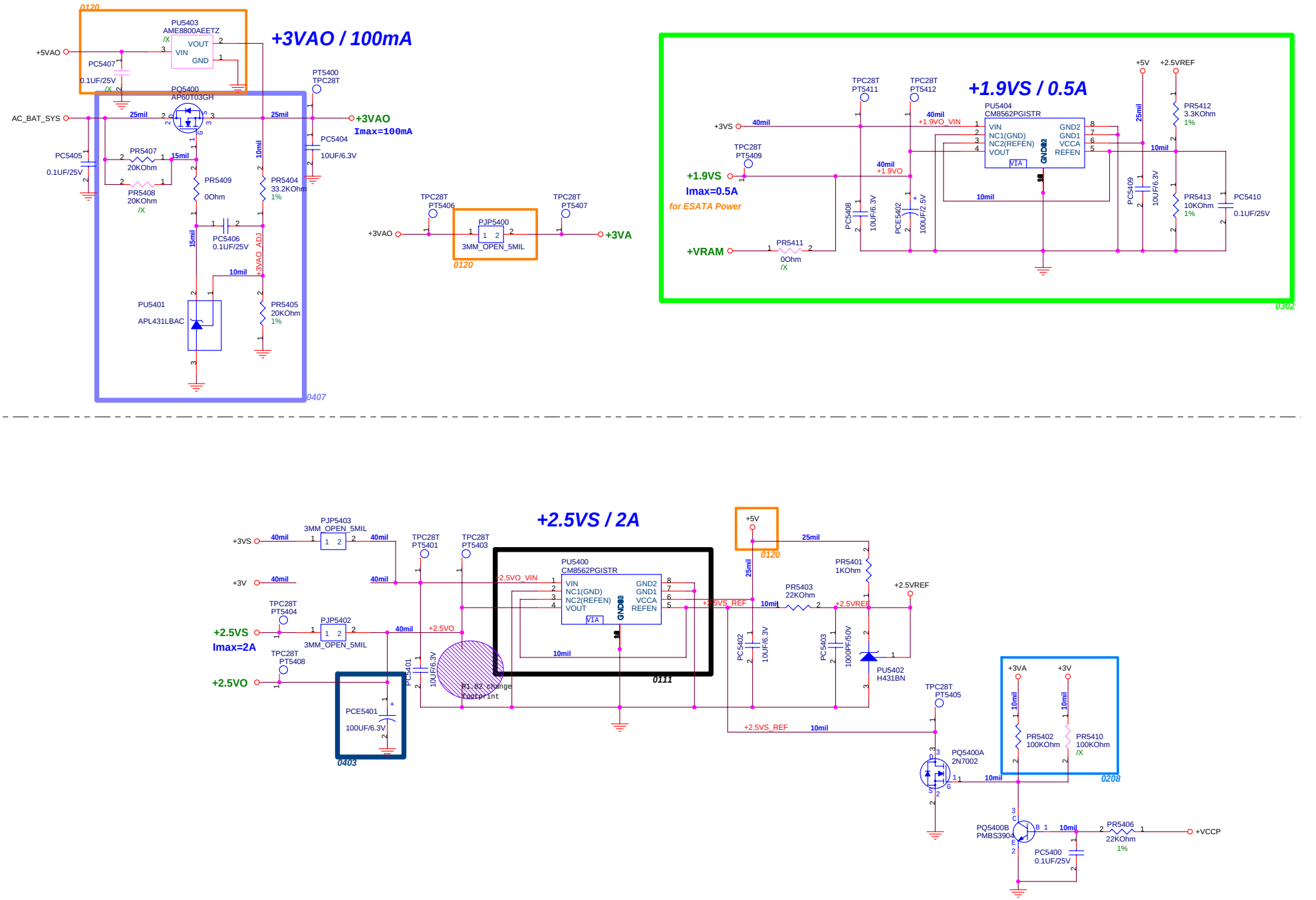
Size	Project Name	Rev
Custom	NAPA	1.0

Date: Monday, August 21, 2006 Sheet 82 of 91

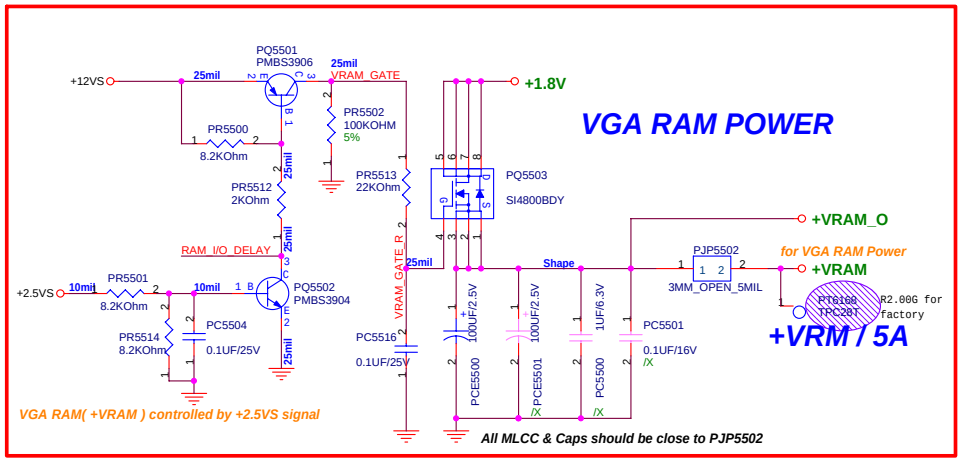


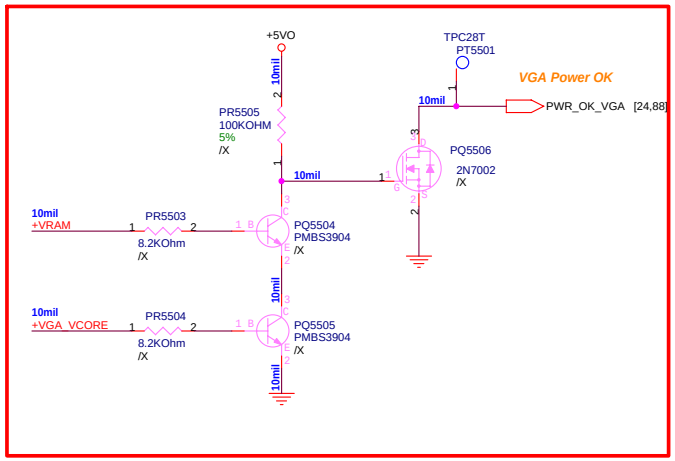
Net	Width	Net	Width
+1.8VO_EN	10mil	+1.8VO_BOOT	25mil
+1.8VO	Shape	+1.8VO_COMP	10mil
+0.9VO_EN	10mil	+1.8VO_HG_R	25mil
+0.9VO	Shape	+1.8VO_LG_R	25mil
+0.9VO_FB	10mil	+1.8VO_HG	25mil
+1.8VO --> DDQREF	10mil	+1.8VO_LG	25mil
VTTREF	15mil	+1.8VO_PHASE	Shape
FPWM#	10mil	+1.8VO_SUR	Shape
VCCA	10mil	+1.8VO_FB	10mil
DDR_PWRGD	10mil	+1.8VO_SS	15mil
OC_VDDQ	15mil	AC_BAT_SYS	Shape

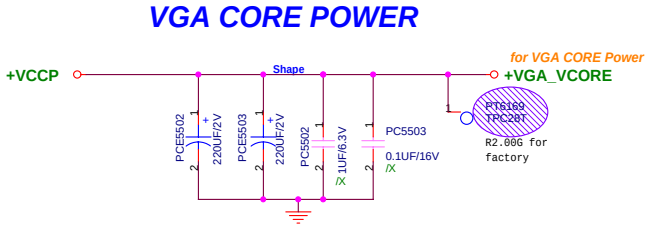
Title :	POWER_I/O_DDR & VTT		
<OrgName>	Engineer:		
Size: Custom	Project Name: NAPA		Rev: 2.1
Date: Monday, August 21, 2006	Sheet 83 of 91		

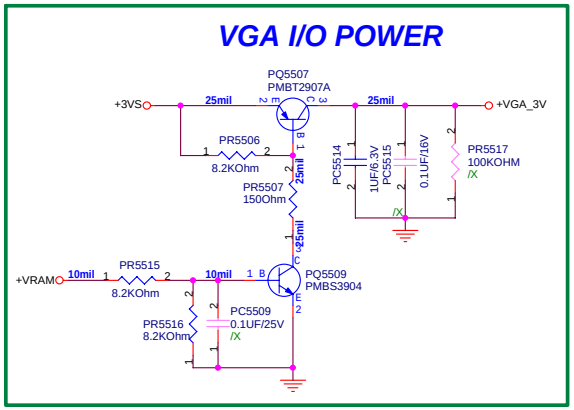


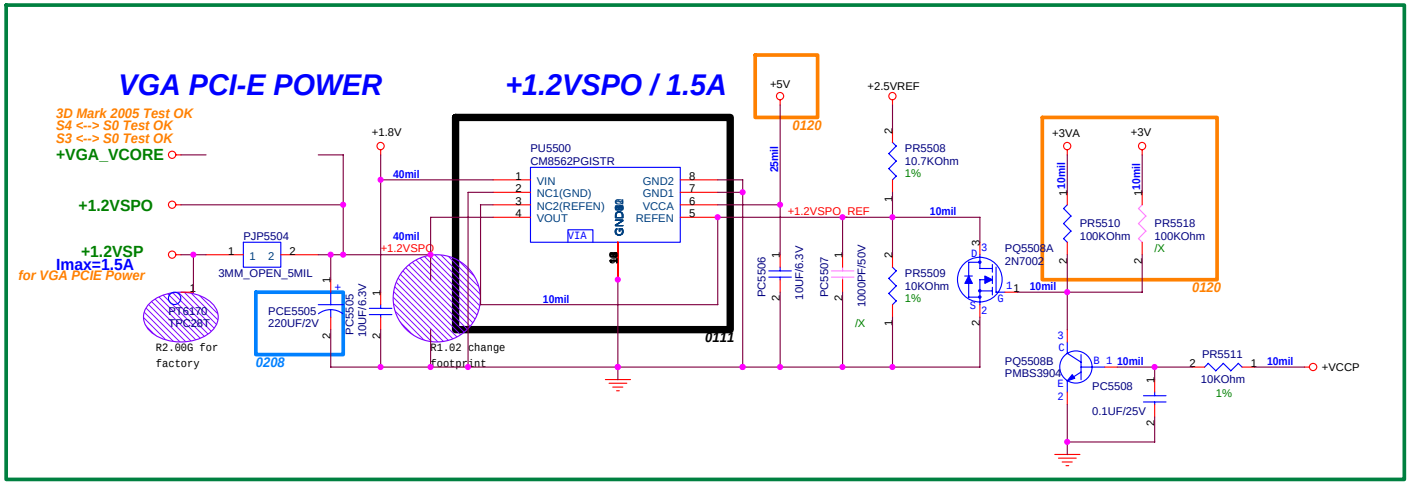
Title :	POWER_I/O_+3VA & +2.5V
<OrgName>	Engineer:
Size: Custom	Project Name: NAPA
Rev: 2.1	
Date: Monday, August 21, 2006	Sheet 84 of 91





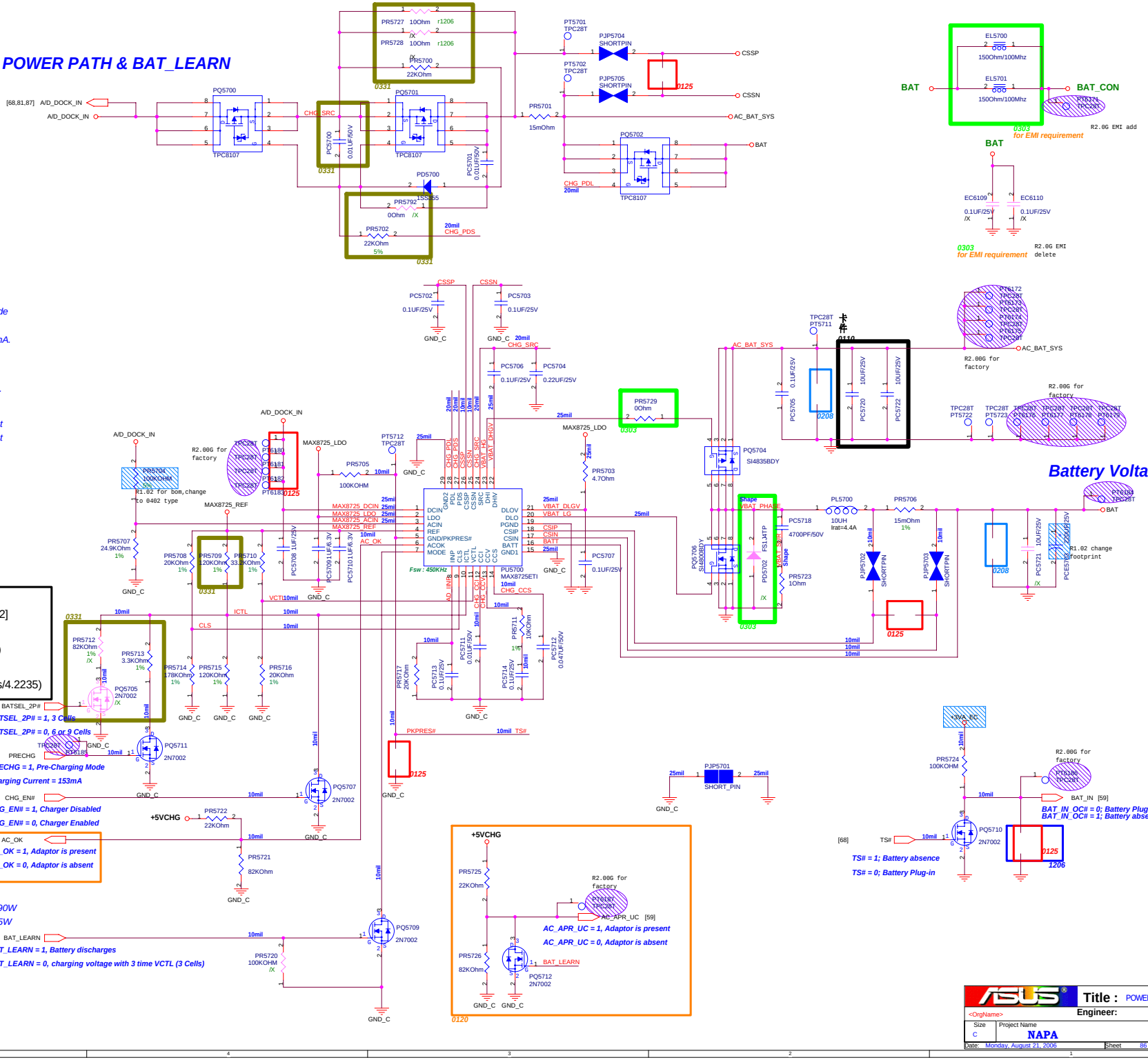






ASUS	Title : POWER_VGA_CORE & RAM	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 85 of 91	

POWER PATH & BAT_LEARN



Charger shut down condition :

1. Victl < 0.06V
2. PKPRES# > 55% of MAX8725_LDO
3. AC Adaptor Removed

The timing of PDL & PDS switch :

BAT - A/D_DOCK_IN > 100mV--> Battery mode

The current capacity of MAX8725_LDO is 10mA.

VBAT_DLGV is a voltage for driving MOSFET.

MAX8725_ACIN < 10.27V, AC Adaptor absent

MAX8725_ACIN > 10.27V, AC Adaptor absent

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

Battery Charging Voltage :
+V_BAT= 3 x [4.2235+(Vvctl-1.8)/9.52]

Battery Charging Current :
Icharge=(0.075/PR5706) x (Victl/3.6))

Input Adaptor Max. Current Limit :
Ilimit_current=(0.075/PR5701) x (Vcls/4.2235)

Pre-Charging Mode :

Precharging current = 150 ~ 160mA

Victl = 0.100V ~ 0.120V

Battery Cell Selection :

BATSEL_2P# = 1, 6 Cells; Victl = 2.084V => Icharge = 2.894A

BATSEL_2P# = 0, 9 Cells; Victl = 3.219V => Icharge = 4.472A

Adaptor Max. Current :

PR5714 = 178K; Vcls = 3.79V, Ilimit = 4.5A; 90W

PR5714 = 47K; Vcls = 2.96V, Ilimit = 3.5A; 65W

BATSEL_SP# = 1, 3-Cell

Victl = 1.22V / Icharge = 1.69A

BATSEL_SP# = 0, 6-Cell or 9-Cell

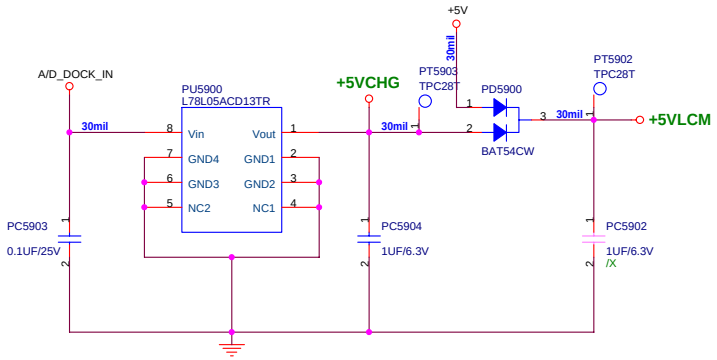
Victl = 2.11V / Icharge = 2.93A

Battery Voltage

ASUS	Title :	POWER_CHARGER	
<OrgName>	Engineer:		
Size: C	Project Name: NAPA		Rev: 2.1
Date: Monday, August 21, 2006	Sheet 86 of 91		

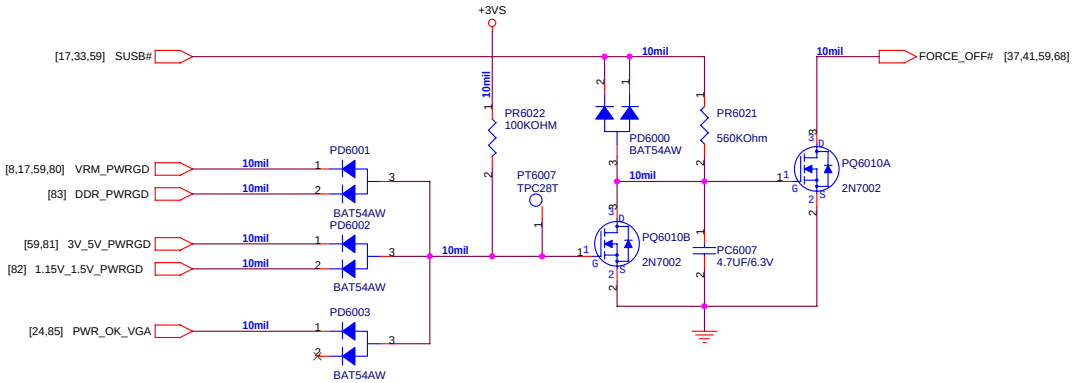
REMOVE BATTERY IN DETECT

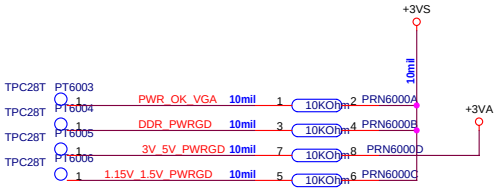
+5VLCM / +5VCHG



Title : POWER_DETECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 87 of 91	

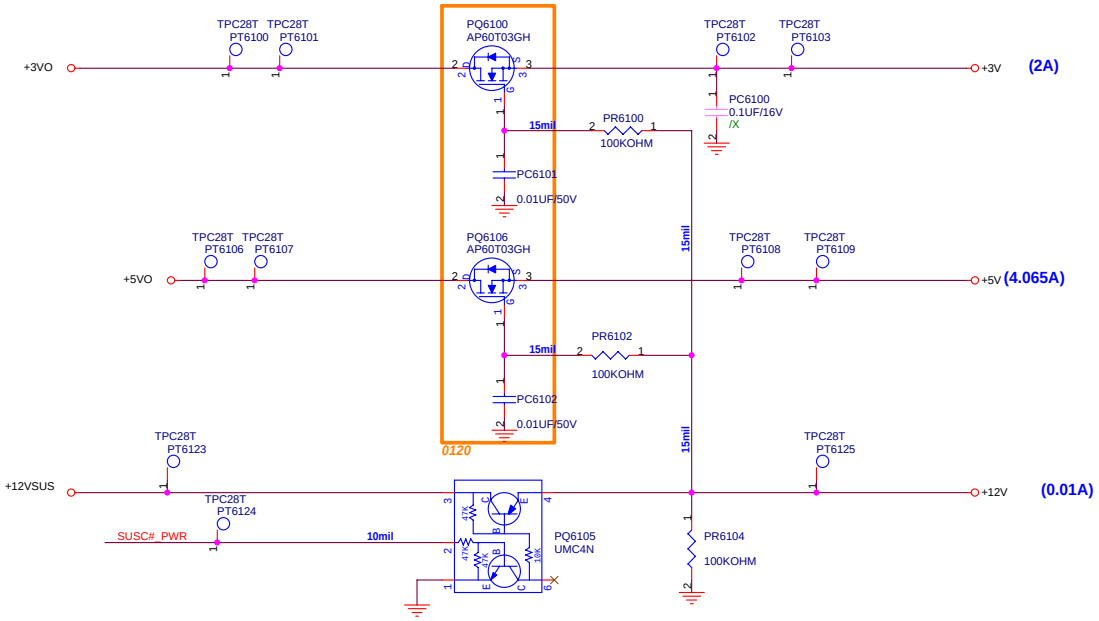
Power Good Detecter

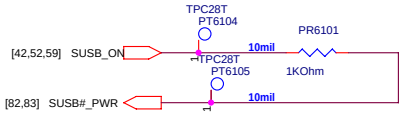




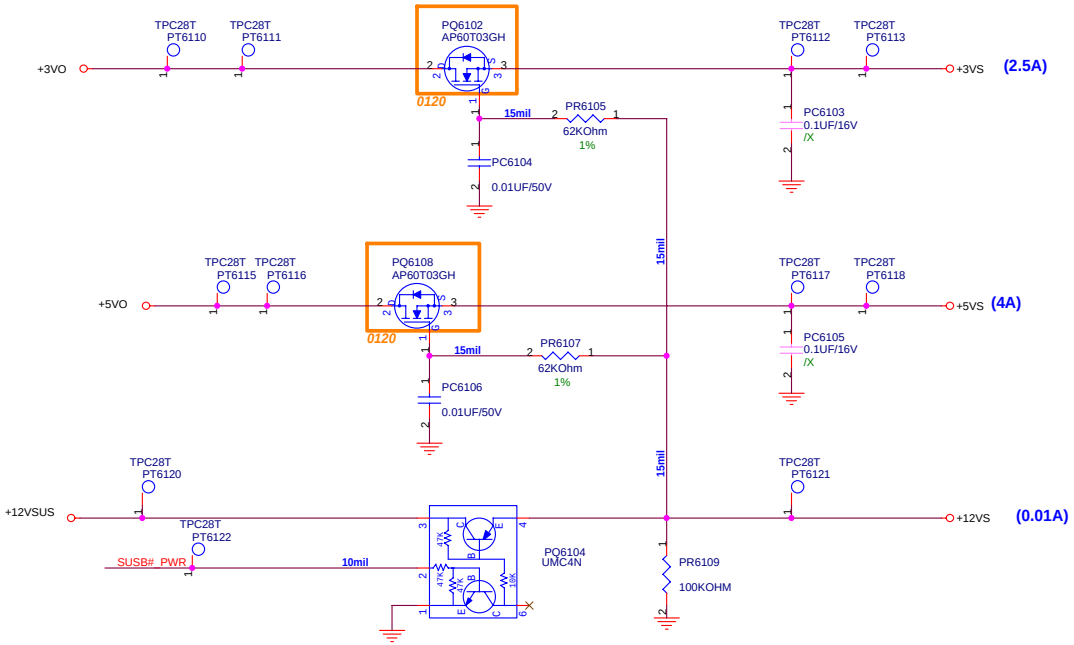
ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 88 of 91	

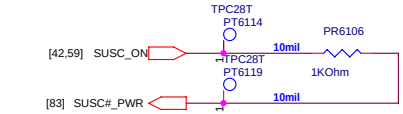
SUSC#_PWR POWER

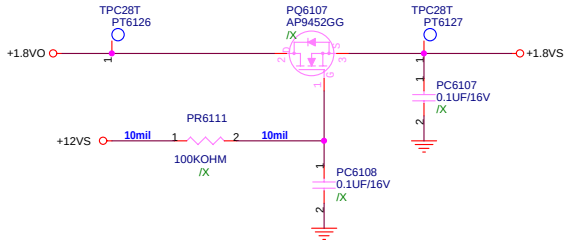




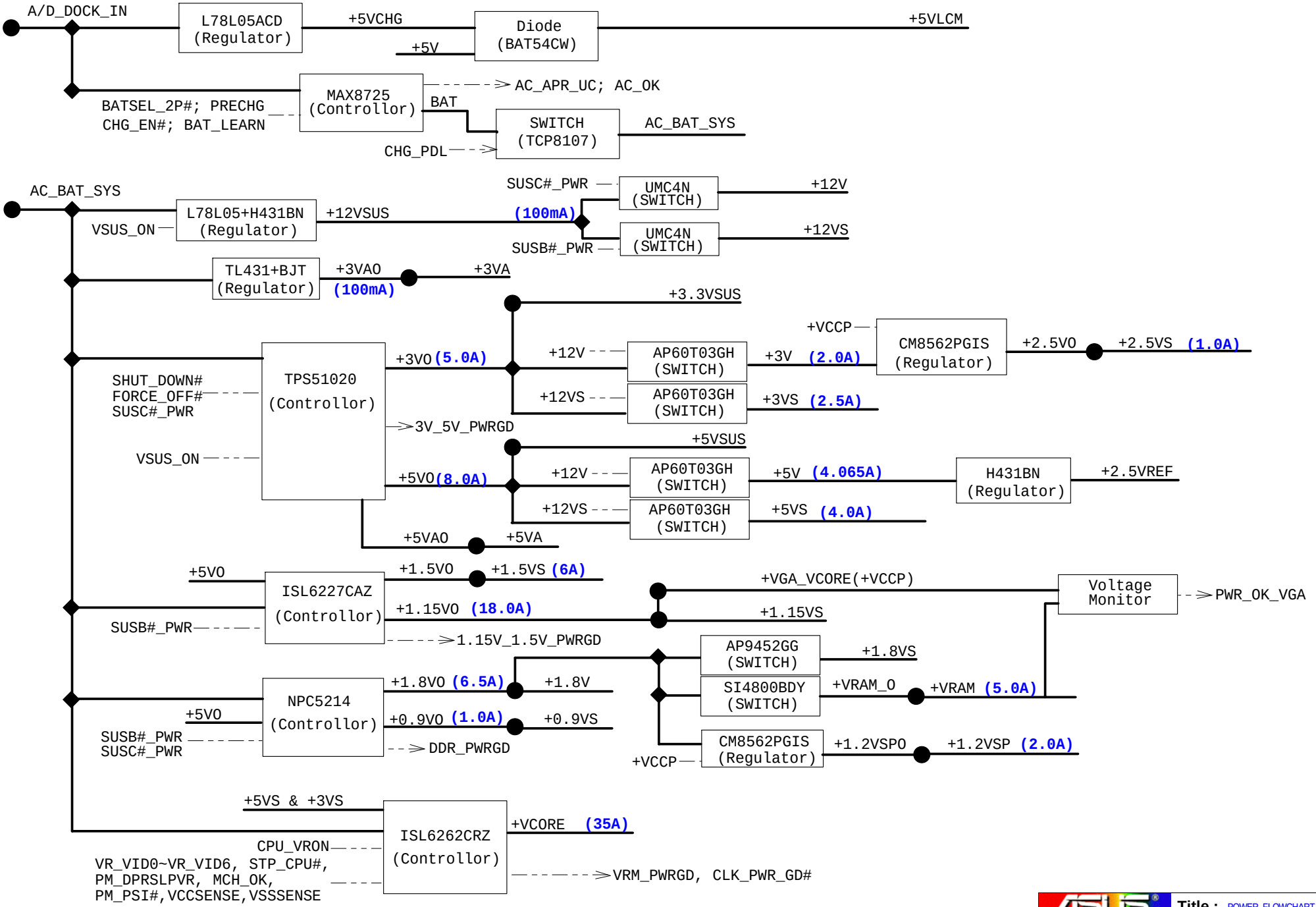
SUSB#_PWR POWER



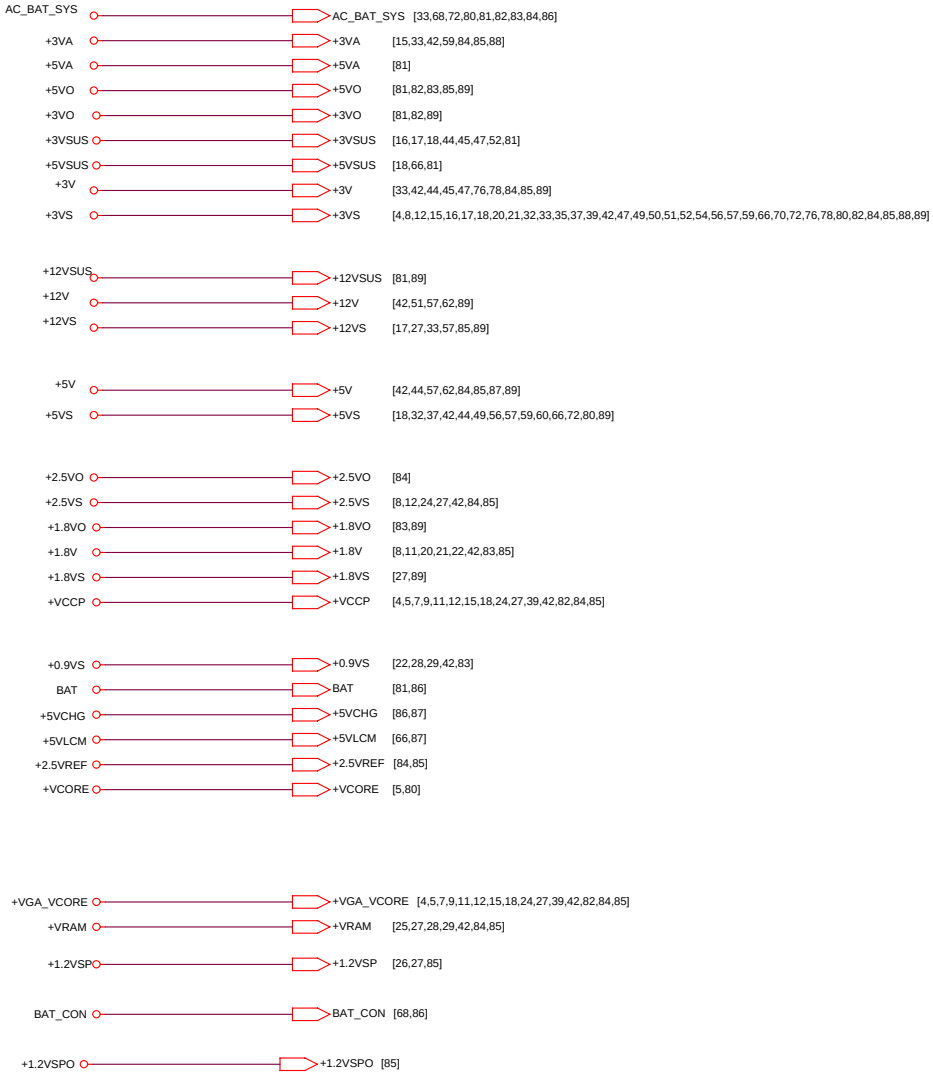




ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 89 of 91	



ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 90 of 91	



ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.1
Date: Monday, August 21, 2006	Sheet 91 of 91	