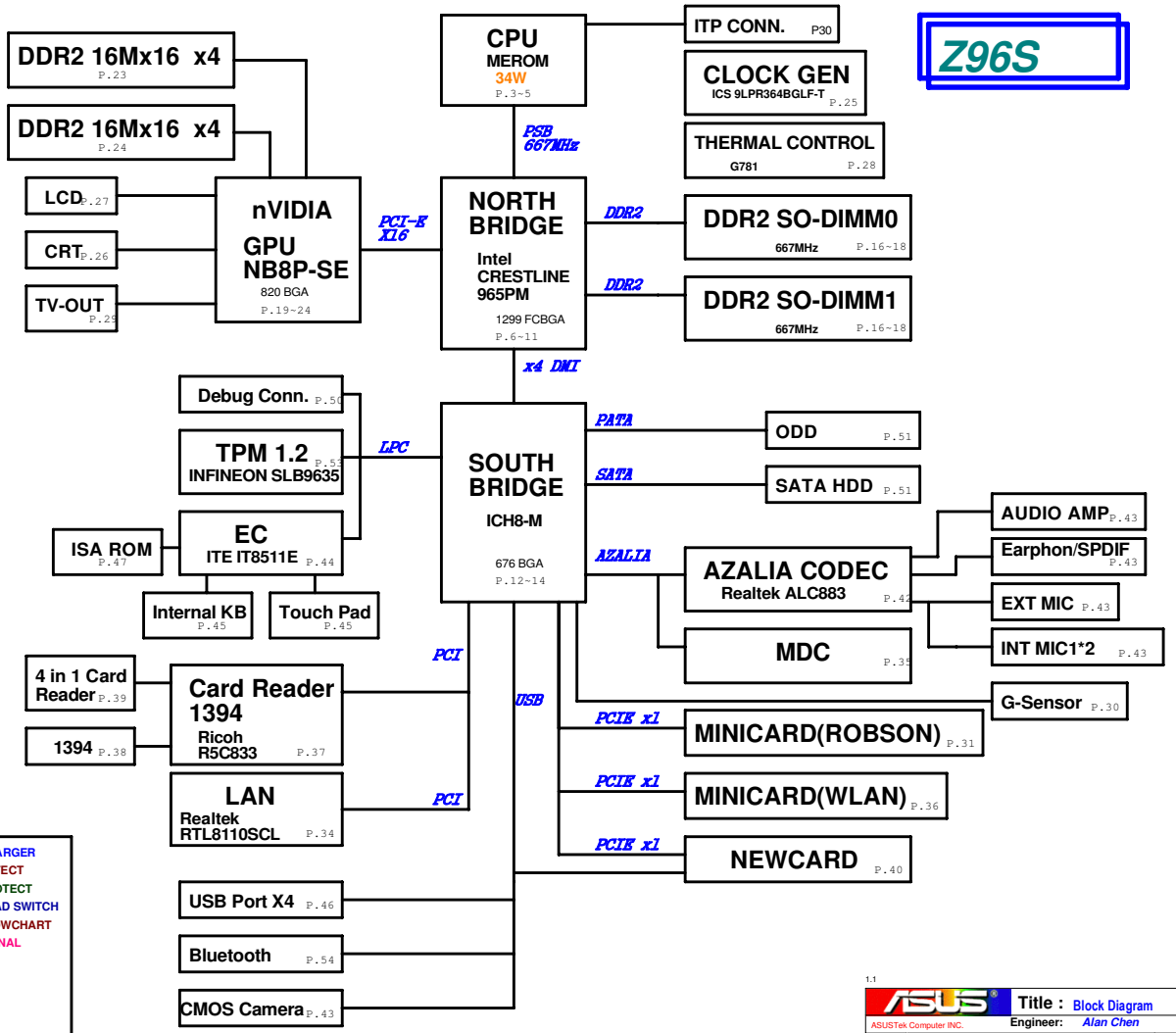


1.1

ASUSTek Computer INC.

Title : Block Diagram

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期三, 十月 30, 2007 Sheet 1 of 67

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM_DA	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	CLK_PWRSAVE#	O
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	N/A	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0GPB4	SMB0_DAT	I/O
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	Mail_LED	O
172	TMRI0/WUI2/GPC4	AC_OK#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	N/A	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	EMAIL_SW#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	EXPLORE_SW#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	N/A	
25	CLKRUN#/WUI7/GPE7	N/A	
101	GPJ2/DAC2	BL_DA	O
102	GPJ3/DAC3	BATSEL_2P#	O
81	GPK0/ADC0	P_PMON	I
22	ECSMI#/GPM0	EXT_SMI#	O
116	PS2CLK2/GPF4	TP_CLK	I/O
117	PS2DAT2/GPF5	TP_DAT	I/O
118	PS2CLK3/GPF6	N/A	
119	PS2DAT3/GPF7	N/A	
113	FA16/GPG0	FA16	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	N/A	
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	PMTHERM#	O
27	LPC80HL/GPG6	THRM_CPU#	I
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	SB_PWRGD	O
149	GPI1	N/A	
152	GPI2	MCHOK	I
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AG12	GPIO0/BMBUSY#	PM_BMBUSY#	I/O	Core(To:3.3V)	GPI
AJ8	GPIO1/TACH1	VDDR_SEL0	I/O	Core(To:3.3V)	GPI
F8	GPIO2/PIRQE#	INT_SHIFT_LOW#	I(OD)	Core(To:5V)	GPI
G11	GPIO3/PIRQF#	INT_SHIFT_HIGH#	I(OD)	Core(To:5V)	GPI
F12	GPIO4/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
B3	GPIO5/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AJ9	GPIO6/TACH2	VDDR_SEL1	I/O	Core(To:3.3V)	GPI
AH9	GPIO7/TACH3	VDDR_SEL2	I/O	Core(To:3.3V)	GPI
AE16	GPIO08	EXT_SMI#	I/O	SUS(To:3.3V)	GPI
AG19	GPIO09/WOL_EN	TP	I/O	SUS(To:3.3V)	GPI
AJ24	GPIO10/CLGPIO1	TP	I/O	SUS(To:3.3V)	GPI
AG22	SMBALERT#/GPIO11	NC	I/O	SUS(To:3.3V)	Native
AC19	GPIO12	EXT_SCI#	I/O	SUS(To:3.3V)	GPI
AH21	GPIO13/GLAN_DOCL#	NC	I/O	SUS(To:3.3V)	Native
AF22	GPIO14/CLGPIO2	TP	I/O	SUS(To:3.3V)	GPI
AE20	GPIO15/STP_PCI#	STP_PCI#	I/O	SUS(To:3.3V)	Native
AJ14	GPIO16/DPRSLPVR	PM_DPRSLPVR	I/O	Core(To:3.3V)	Native
AG8	GPIO17/TACH0	PM_EXTTS#0	I/O	Core(To:3.3V)	GPI
AH12	GPIO18	VCORE_SEL0	I/O	Core(To:3.3V)	GPO
AJ10	GPIO19/SATA1GP	CB_SD#	I/O	Core(To:3.3V)	GPI
AE11	GPIO20	VCORE_SEL1	I/O	Core(To:3.3V)	GPO
AJ12	GPIO21/SATA0GP	WLAN_BT_LED_EN#	I/O	Core(To:3.3V)	GPI
AG10	GPIO22/SCLOCK	TP	I/O	Core(To:3.3V)	GPI
E6	GPIO23/LDRQ1#	TP	I/O	Core(To:3.3V)	Native
AJ27	GPIO24/CLGPIO0	TP	I/O	SUS(To:3.3V)	GPO
AG18	GPIO25/STP_CPU#	STP_CPU#	I/O	SUS(To:3.3V)	Native
AH27	GPIO26/S4_STATE#	TP	I/O	SUS(To:3.3V)	Native
AH25	GPIO27/QRT_STATE0	VGMCH_SEL0	I/O	SUS(To:3.3V)	GPO
AD16	GPIO28/QRT_STATE1	VGMCH_SEL1	I/O	SUS(To:3.3V)	GPO
AG17	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
AD12	GPIO30/OC#6	NEWCARD_OC#	I/O	SUS(To:3.3V)	Native
AJ18	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	I/O	Core(To:3.3V)	GPO
AE10	GPIO33/HDA_DOCK_EN#	TP	I/O	Core(To:3.3V)	GPO
AG14	GPIO34/HDA_DOCK_RST#	TP	I/O	Core(To:3.3V)	GPO
AG13	GPIO35/SATACLKREQ#	VGPU_SEL1	I/O	Core(To:3.3V)	GPO
AF11	GPIO36/SATA2GP	WLAN_ON#	I/O	Core(To:3.3V)	GPI
AG11	GPIO37/SATA3GP	BT_ON#	I/O	Core(To:3.3V)	GPI
AF9	GPIO38/SLOAD	PM_EXTTS#1	I/O	Core(To:3.3V)	GPI
AJ11	GPIO39/SDATAOUT0	CLK_PWRSAVE#	I/O	Core(To:3.3V)	GPI
AG16	GPIO40/OC1#	USB_CON_OC01#	I/O	SUS(To:3.3V)	Native
AG15	GPIO41/OC2#	USB_CON_OC23#	I/O	SUS(To:3.3V)	Native

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AD16	GPIO42/OC3#	USB_CON_OC23#	I/O	SUS(To:3.3V)	Native
AG17	GPIO43/OC4#	USB_CON_OC4#	I/O	SUS(To:3.3V)	Native
N/A	GPIO44	N/A	I/O	N/A	N/A
N/A	GPIO45	N/A	I/O	N/A	N/A
N/A	GPIO46	N/A	I/O	N/A	N/A
N/A	GPIO47	N/A	I/O	N/A	N/A
AD10	GPIO48/SDATAOUT1	TP	I/O	Core(To:3.3V)	GPI
AG29	GPIO49/CPUPWRGD	H_PWRGD	I/O	V_CPU_IO	Native
E18	GPIO50/REQ1#	PCI_REQ#1	I/O	Core(To:5.5V)	Native
C18	GPIO51/GNT1#	TP	I/O	Core(To:3.3V)	Native
B19	GPIO52/REQ2#	PCI_REQ#2	I/O	Core(To:5.5V)	Native
F18	GPIO53/GNT2#	PCI_GNT#2	I/O	Core(To:3.3V)	Native
A11	GPIO54/REQ3#	PCI_REQ#3	I/O	Core(To:5.5V)	Native
C10	GPIO55/GNT3#	NC	I/O	Core(To:3.3V)	Native

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	REQ#0/GNT#0	INTB-->INTB
1394	AD17	REQ#0/GNT#0	INTA-->INTA
LAN	AD23	REQ#2/GNT#2	INTA-->INTC

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

1.1

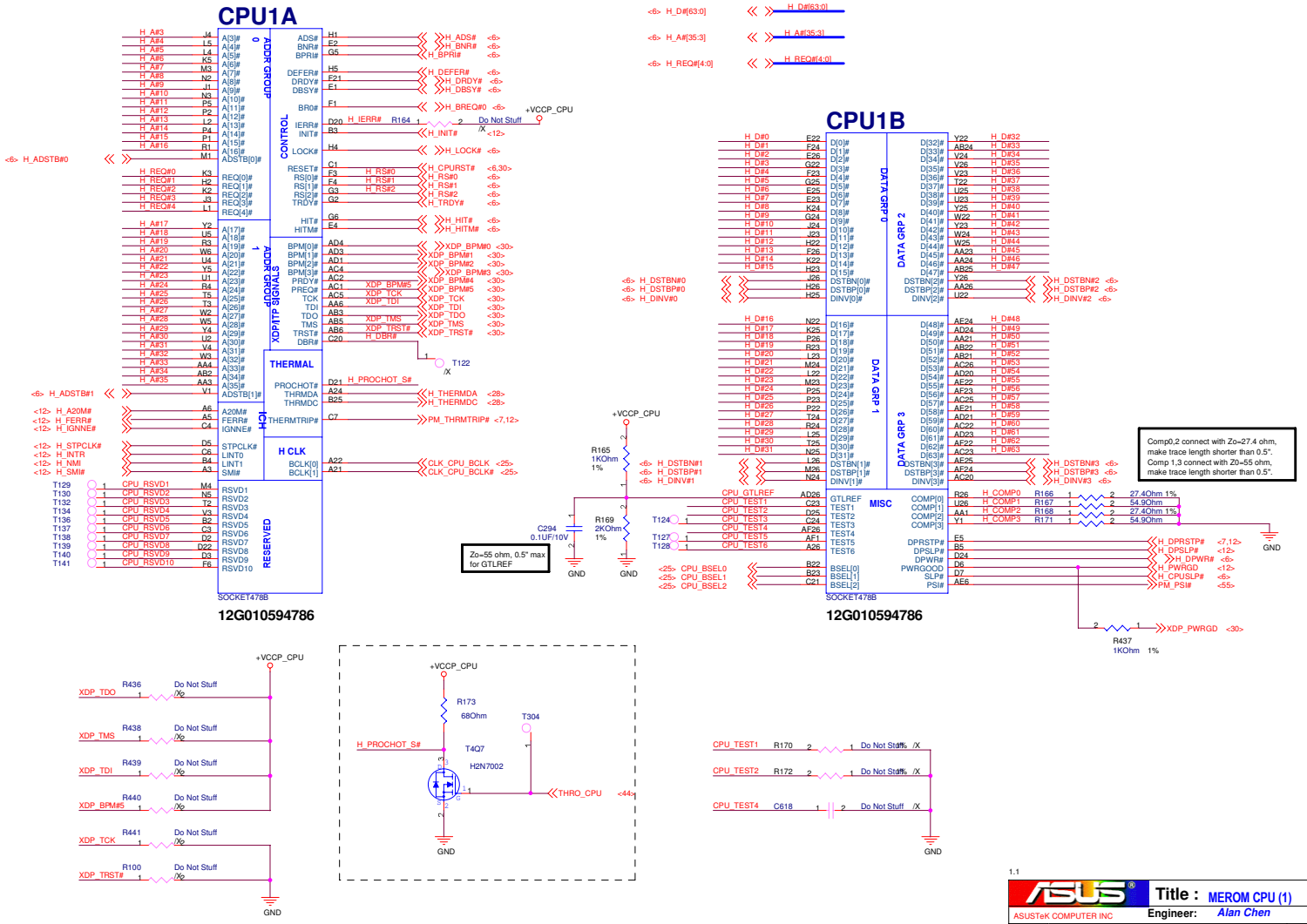
ASUSTek Computer INC.

Title : System Setting

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期二, 六月 30, 2007 Sheet 2 of 67



1.1

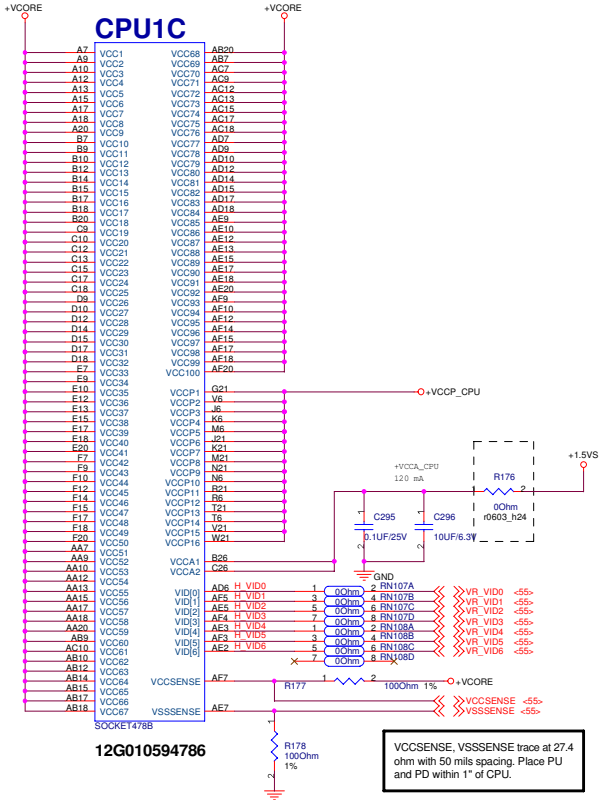
ASUSTeK COMPUTER INC

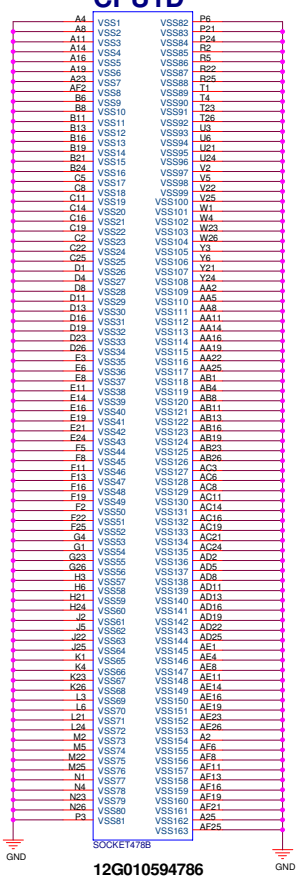
Title : MEROM CPU (1)

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

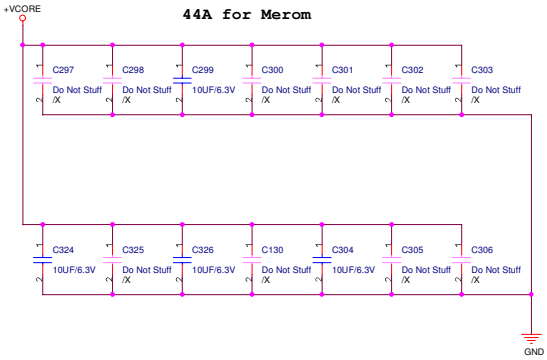
Date: 星期二, 五月 30, 2007 Sheet 3 of 67

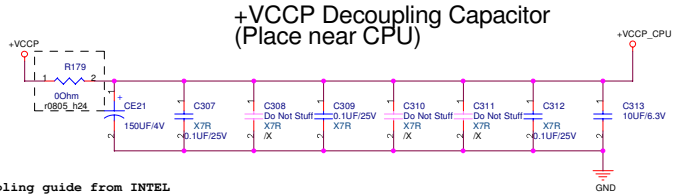




1.1

ASUSTeK COMPUTER INC	Title : MEROM CPU (2)		
	Engineer: Alan Chen		
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期二, 五月 30, 2007	Sheet 4 of 67		





Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

1.1

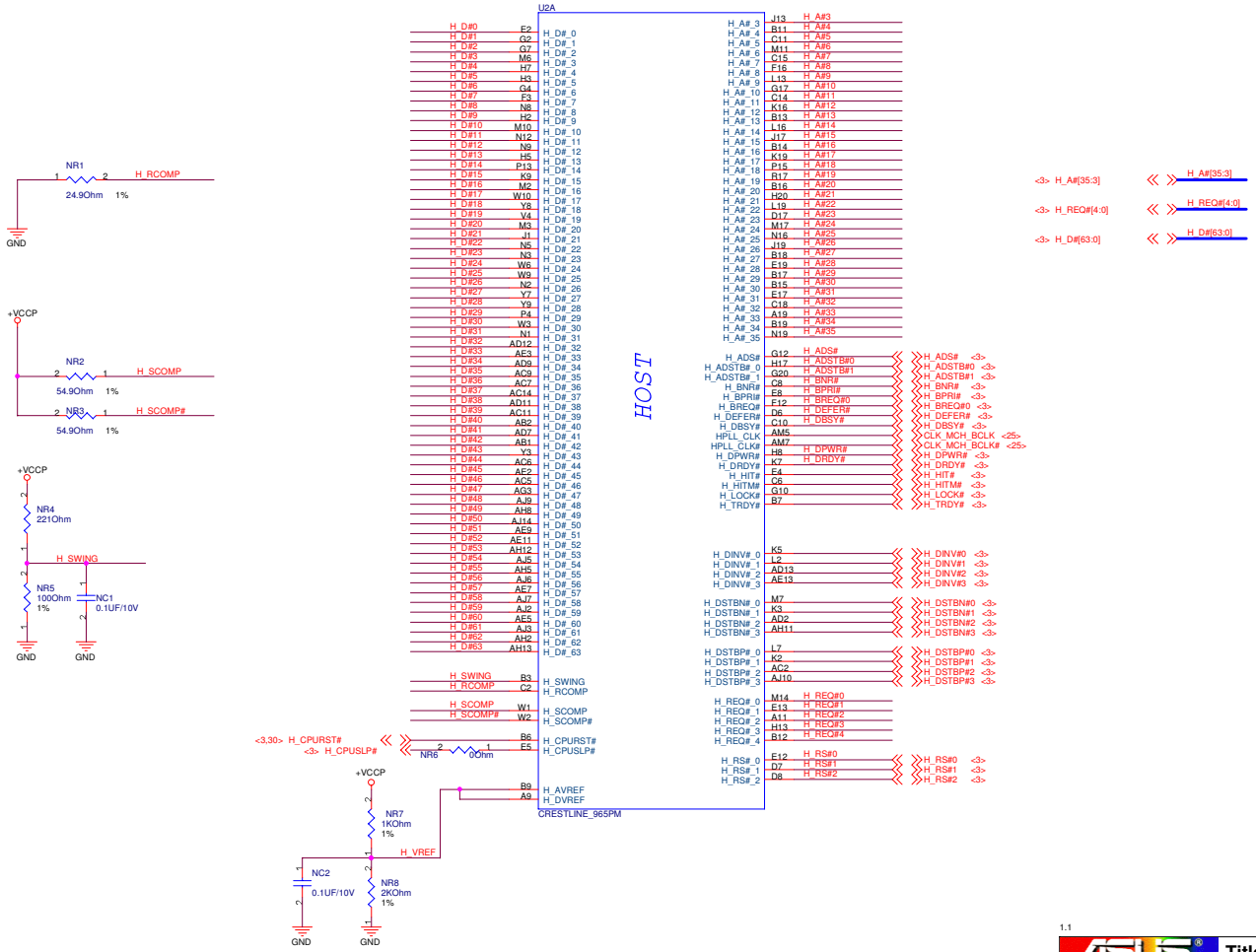
ASUSTek COMPUTER INC. NB1

Title : CPU CAP and HOLES

Engineer: Alan Chen

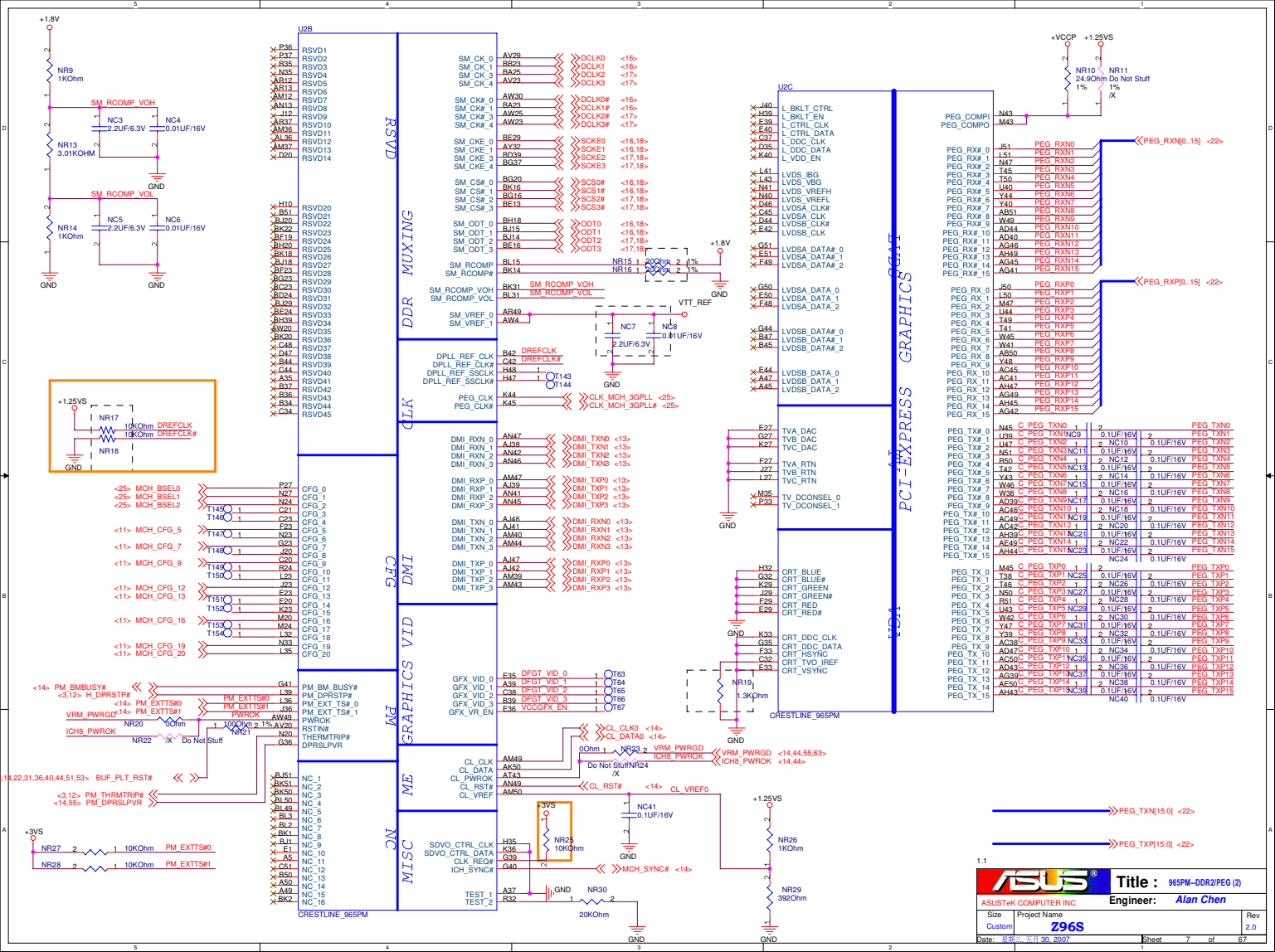
Size	Project Name	Rev
Custom	Z96S	2.0

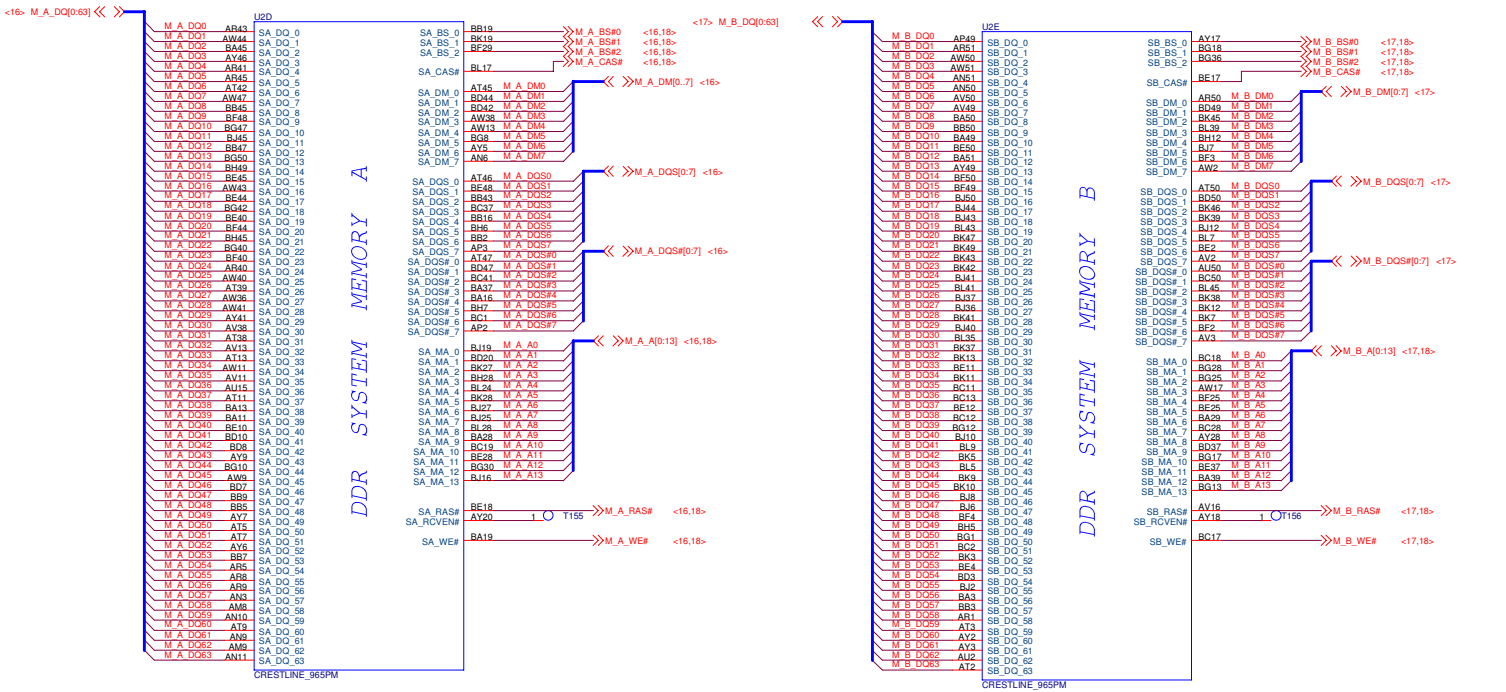
Date: 星期二, 五月 30, 2007 Sheet 5 of 67



1.1

ASUSTeK COMPUTER INC	Title : 965PM -- CPU (1)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期二, 五月 30, 2007	Sheet 6 of 67	


U2B
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
MISC
GRAPHICS
PCI-EXPRESS
DDI
CRESTLINE_965PM
U2C
+1.8V
+1.25VS
+3VS
+VCCP
GND
VTT_REF
NR9 1KOhm
NR13 3.01KOHM
NR14 1KOhm
NC3 2.2UF/6.3V
NC4 0.01UF/16V
NC5 2.2UF/6.3V
NC6 0.01UF/16V
SM_RCOMP_VOH
SM_RCOMP_VOL
NR17 10KOhm DREFCLK
NR18 10KOhm DREFCLK#
NR10 24.9Ohm 1%
NR11 Do Not Stuff 1% /X
NC7 2.2UF/6.3V
NC8 0.01UF/16V
NR15 1 200Ohm 2 1%
NR16 1 200Ohm 2 1%
NR19 1.3KOhm
NR23 0Ohm
NR24 Do Not Stuff /X
NC41 0.1UF/16V
NR25 10KOhm
NR26 1KOhm
NR29 392Ohm
NR30 20KOhm
NR27 10KOhm PM_EXTTS#0
NR28 10KOhm PM_EXTTS#1
NR20 0Ohm
NR21 100Ohm 1% 1/16W
NR22 /X Do Not Stuff
PEG_RXN[0..15] <22>
PEG_RXP[0..15] <22>
PEG_TXN[15:0] <22>
PEG_TXP[15:0] <22>
Title : 965PM-DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer: Alan Chen
Size Custom
Project Name Z96S
Rev 2.0
Date: 星期一 五月 30, 2007
Sheet 7 of 67



1.1

ASUSTeK COMPUTER INC	Title : 965PM--DDR2 bus (3)		
	Engineer: Alan Chen		
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期二, 五月 30, 2007	Sheet 8 of 67		

1310 mA for External GFX

3138 mA

7700 mA

POWER

U2G

CRESTLINE_965PM

VCC CORE

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

U2F

VCC NCTF

VSS NCTF

VSS SCB

VCC AXM

VCC AXM NCTF

POWER

540 mA

1.1

ASUSTeK COMPUTER INC

Title : 965PM--POWER (4)

Engineer: Alan Chen

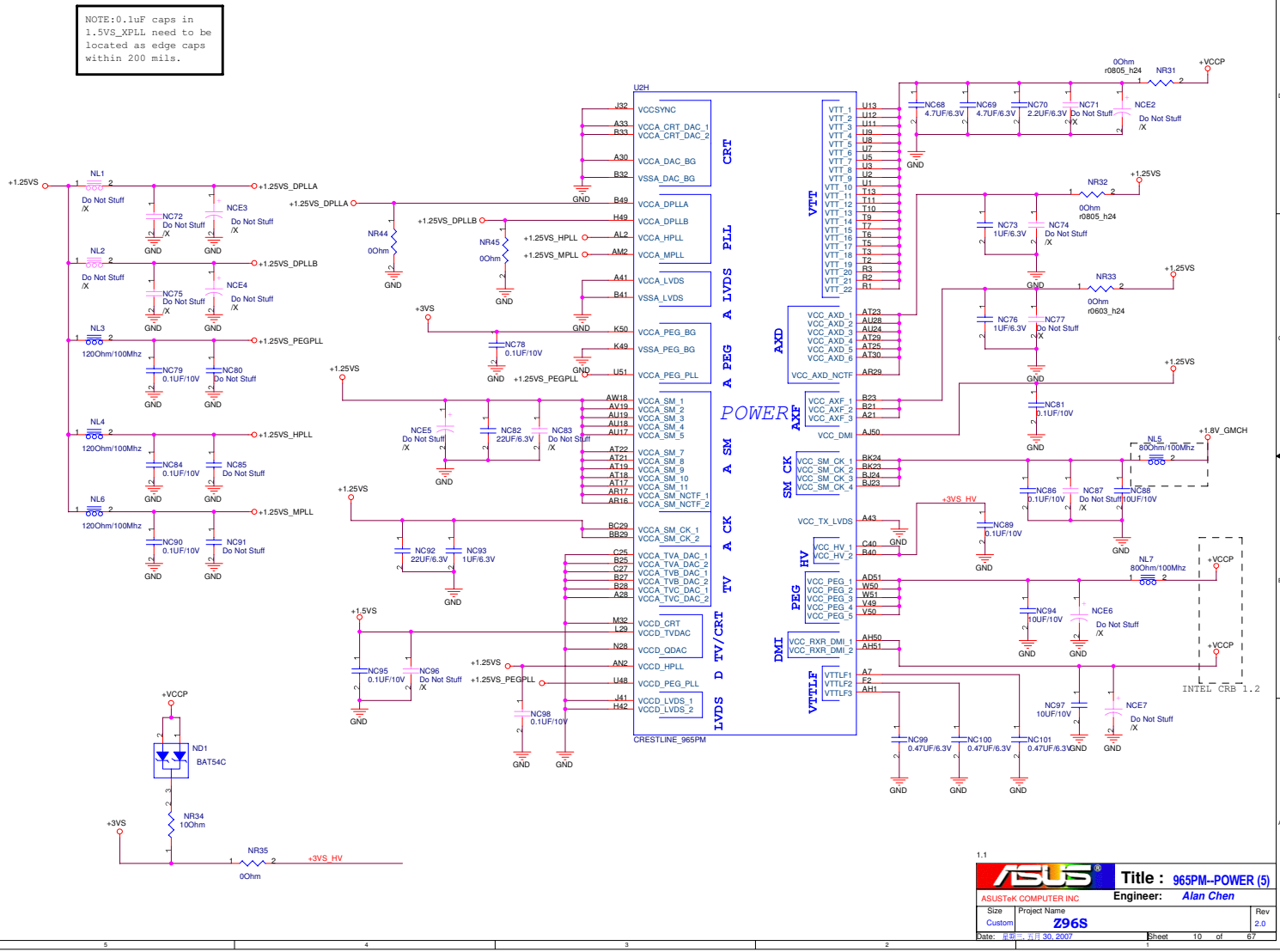
Size: Custom

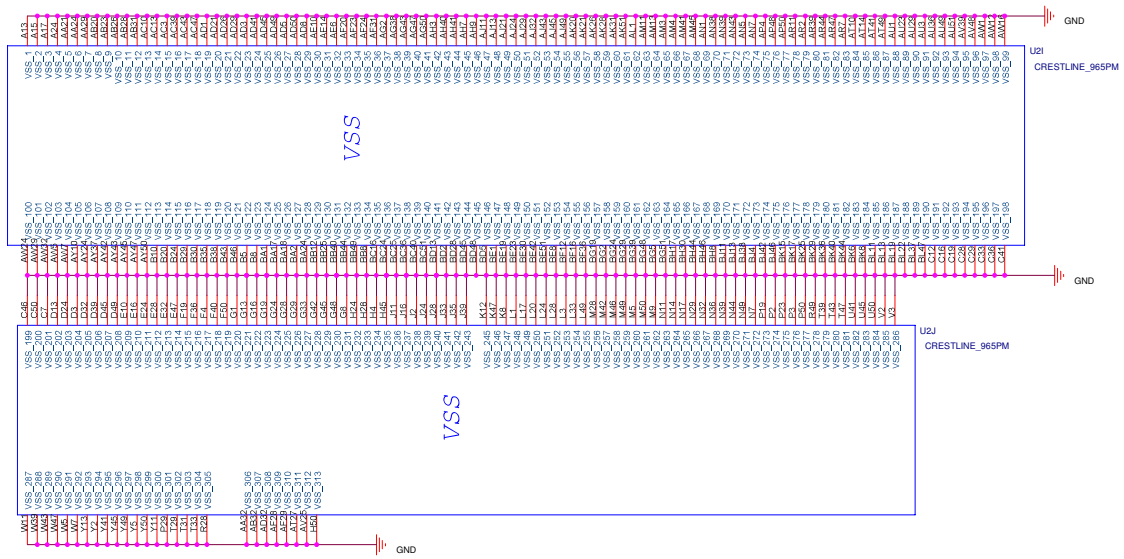
Project Name: Z96S

Rev: 2.0

Date: 星期三, 六月 30, 2007

Sheet 9 of 67


NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
U2H
CRESTLINE_965PM
POWER
CRT
A LVDS PLL
A PEG
A SM
A CK
TV
TV/CRT
LVDS
VTT
AXD
AXE
SM CK
HV
PEG
DMI
VTTLF
+1.25VS
+1.25VS_DPLLA
+1.25VS_DPLLB
+1.25VS_PEGPLL
+1.25VS_HPLL
+1.25VS_MPLL
+3VS
+3VS_HV
+1.5VS
+VCCP
+1.8V_GMCH
GND
Do Not Stuff
/X
INTEL CRB 1.2
ASUSTeK COMPUTER INC
Title : 965PM--POWER (5)
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: 星期二, 五月 30, 2007
Sheet 10 of 67
HIGH = LANES REVERSED



<7> MCH_CFG_5

NR37
Do Not Stuff
/X

GND

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

<7> MCH_CFG_7

NR39
Do Not Stuff
/X

GND

CFG7 : CPU STRAP

HIGH = Mobile CPU (Default)

LOW = Reserved

<7> MCH_CFG_9

NR42
Do Not Stuff
/X

GND

CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

HIGH = Normal Operation (Default)

<7> MCH_CFG_16

NR43
Do Not Stuff
/X

GND

CFG16 : Dynamic ODT STRAP

Low = Dynamic ODT Disabled

HIGH = Dyanamic ODT Enabled (default)

+3VS

NR38
Do Not Stuff
/X

<7> MCH_CFG_19

CFG19 : DMI LANE REVERSAL

LOW = NORMAL (default)

HIGH = LANES REVERSED

+3VS

NR41
Do Not Stuff
/X

<7> MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE

LOW = ONLY SDVO or PCIE is Operational

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

<7> MCH_CFG_13

NR36
Do Not Stuff
/X

GND

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

<7> MCH_CFG_12

NR40
Do Not Stuff

GND

1.1

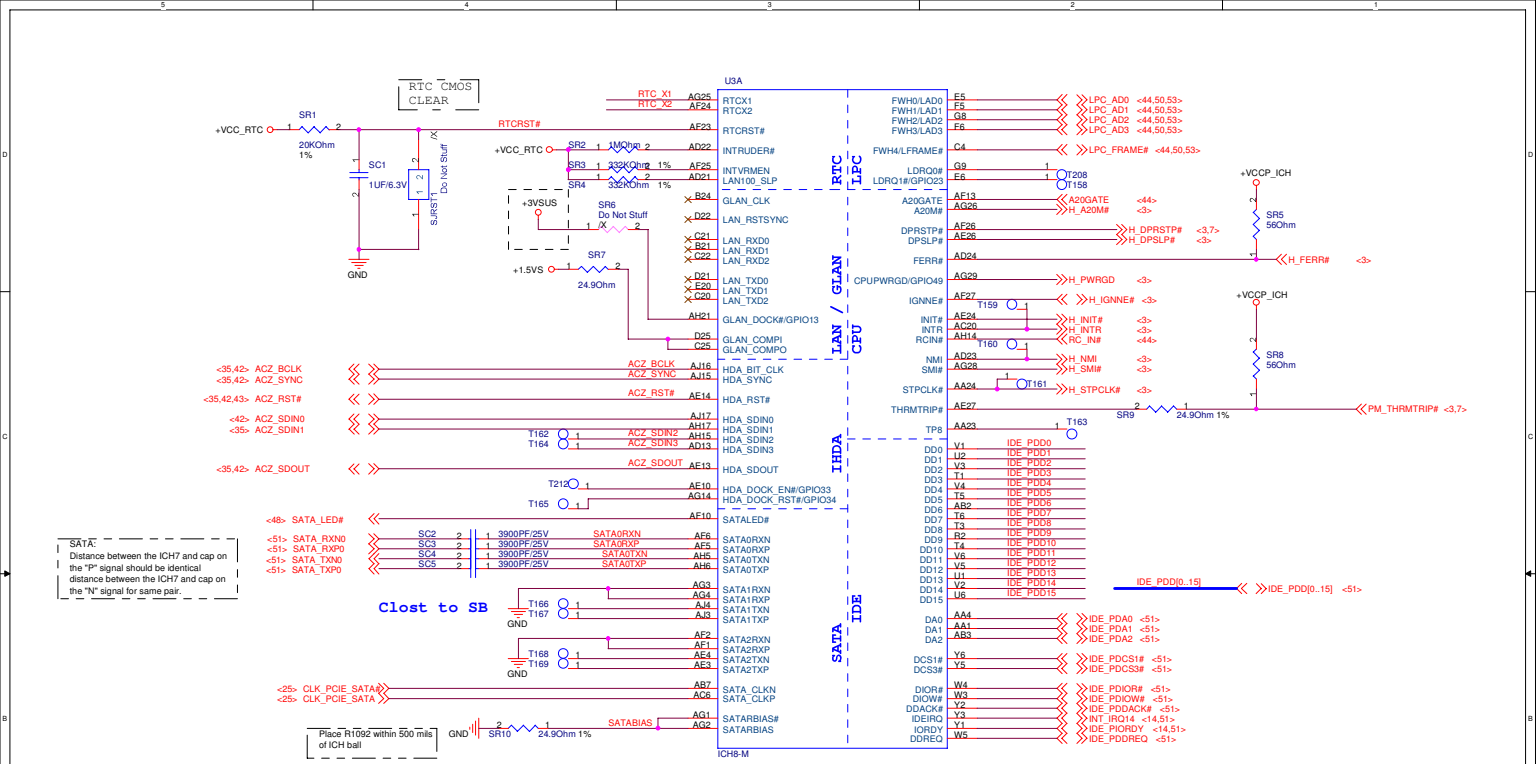
ASUSTeK COMPUTER INC

Title : GND/Strapping (6)

Engineer: Alan Chen

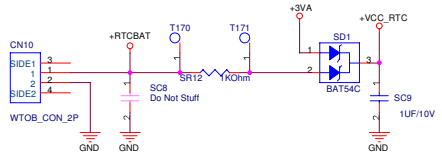
Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期二, 五月 30, 2007 Sheet 11 of 67

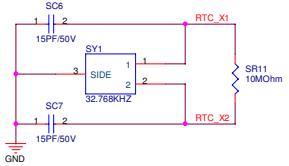


SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

RTC BAT

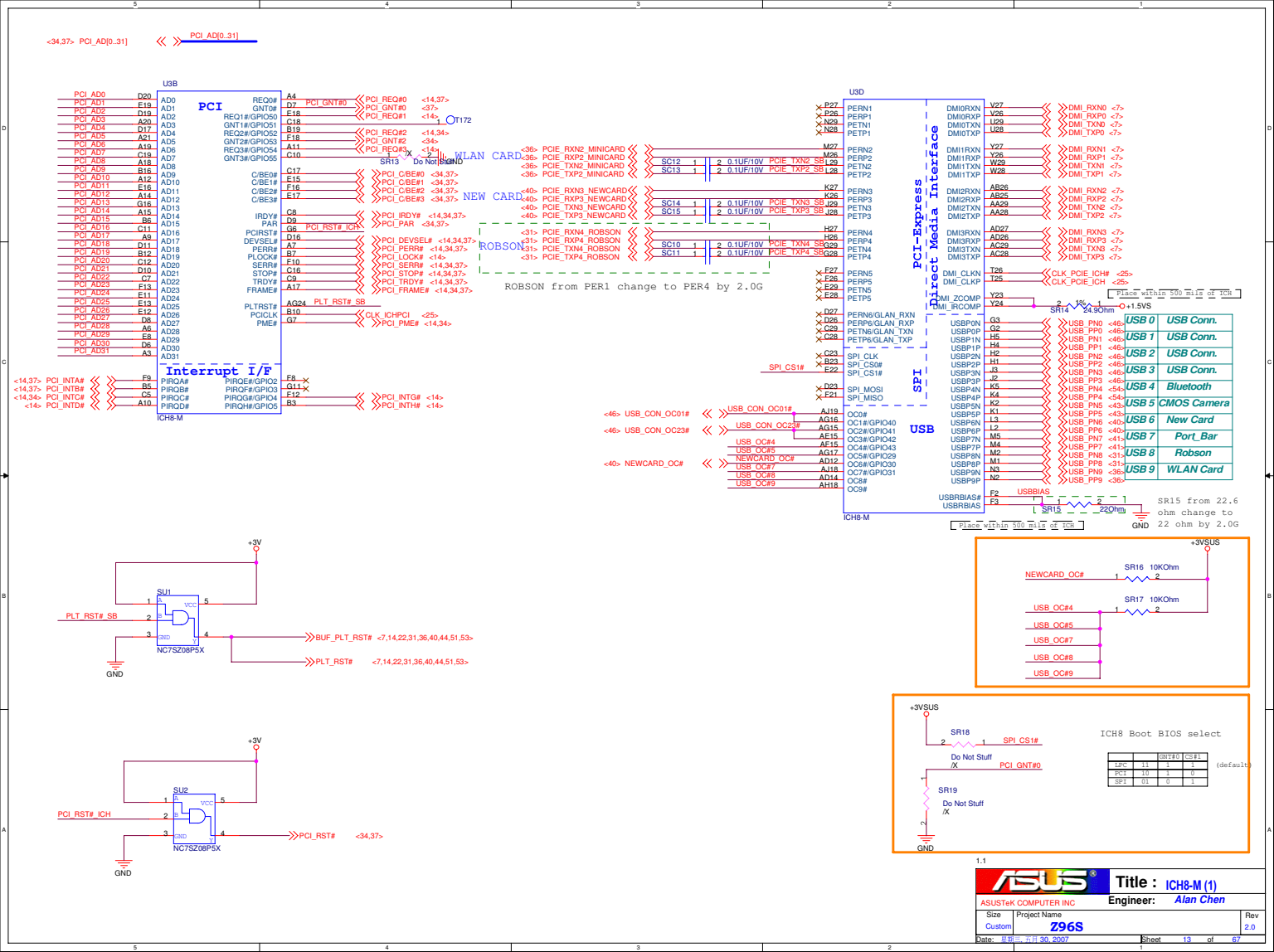


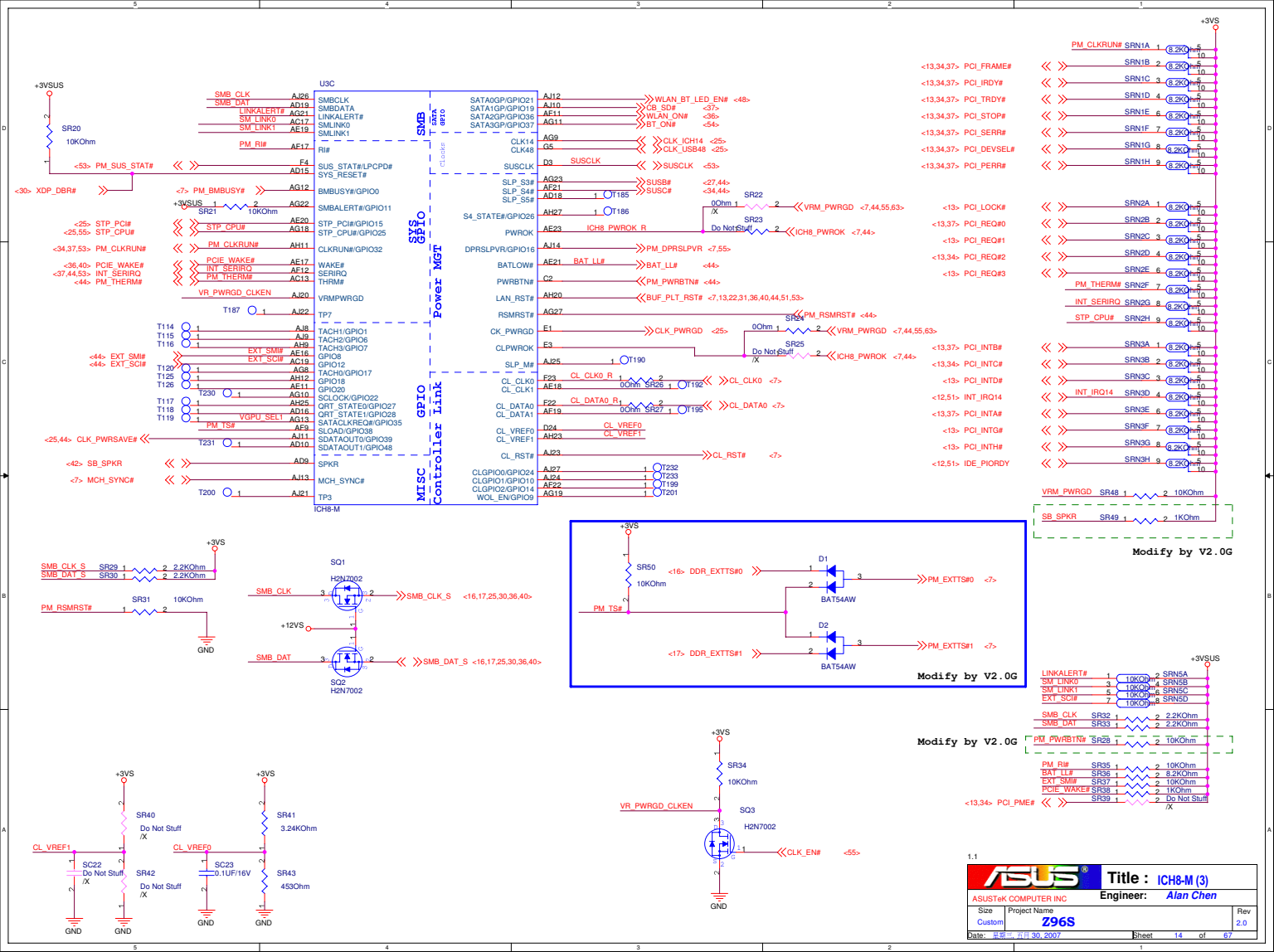
RTC Battery
P/N=07-016322032

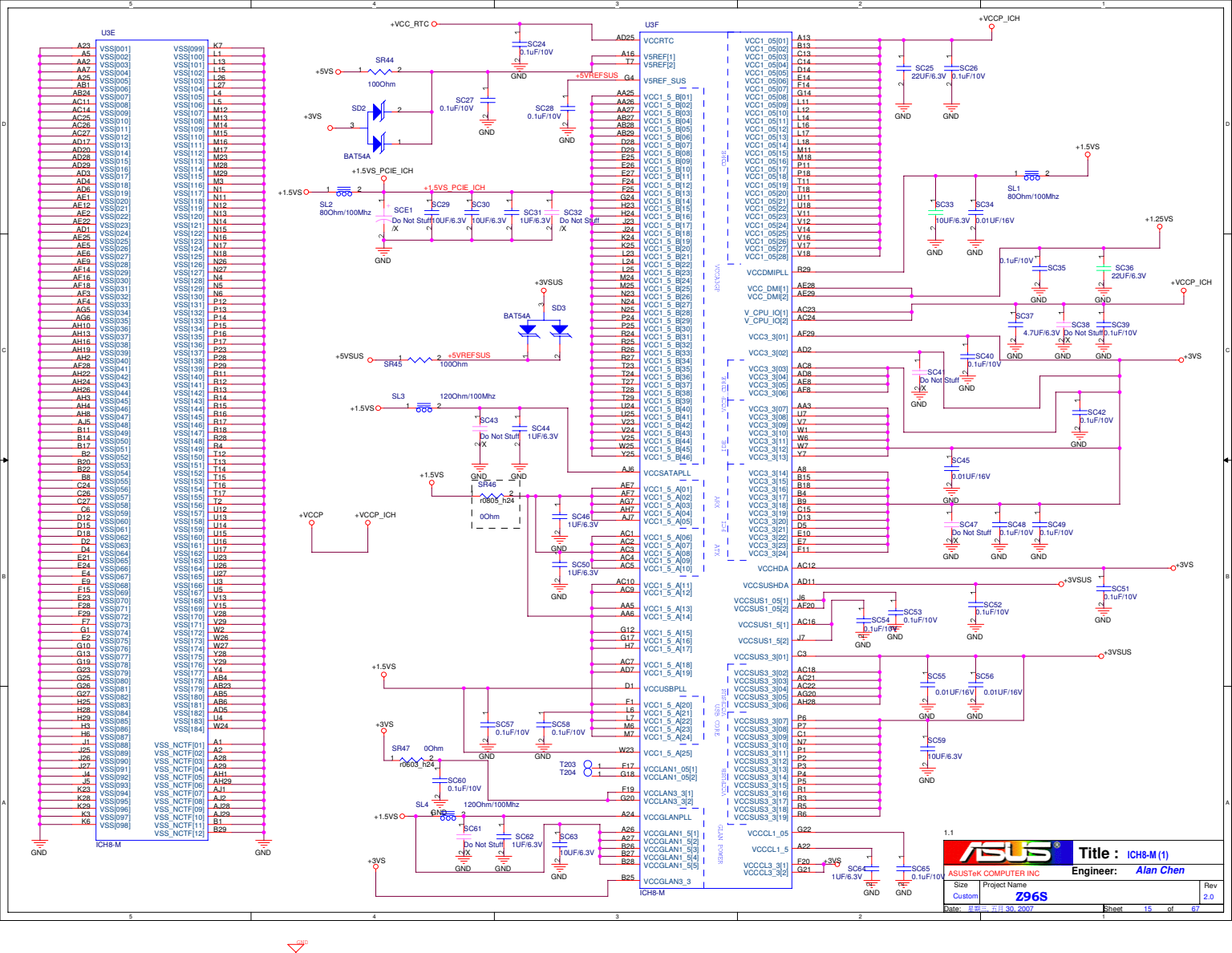


1.1

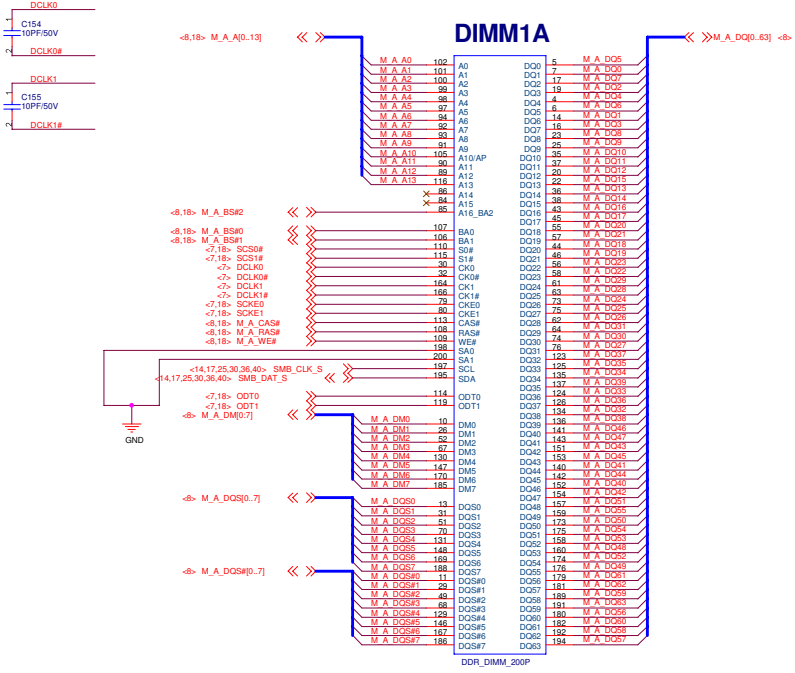
ASUSTeK COMPUTER INC	Title : ICH8-M (1)	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 六月 30, 2007	Sheet 12 of 67	


PCI_AD[0..31]
U3B
PCI
Interrupt I/F
ICH8-M
WLAN CARD
NEW CARD
ROBSON
ROBSON from PER1 change to PER4 by 2.0G
U3D
PCI-Express
Direct Media Interface
SPI
USB
Place within 500 mils of ICH
SR14 24.9Ohm 1%
+1.5VS
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 CMOS Camera
USB 6 New Card
USB 7 Port_Bar
USB 8 Robson
USB 9 WLAN Card
SR15 22Ohm
SR15 from 22.6 ohm change to 22 ohm by 2.0G
SU1
NC7SZ08P5X
BUF_PLT_RST#
PLT_RST#
SU2
SR16 10KOhm
SR17 10KOhm
SR18
SR19
Do Not Stuff
ICH8 Boot BIOS select
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: Alan Chen
Project Name Z96S
Rev 2.0
Sheet 13 of 67

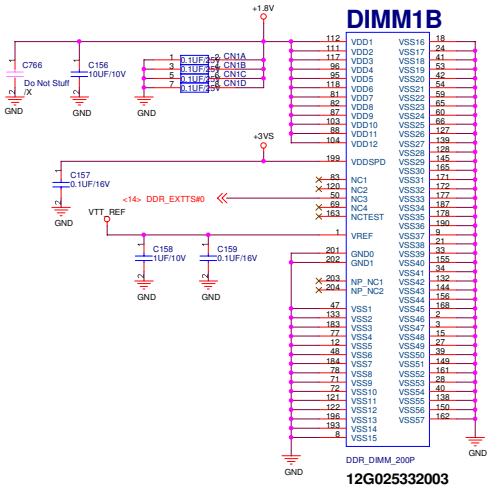

U3C
ICH8-M
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SMB
SYS GPIO
Power MGT
GPIO Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
WLAN_BT_LED_EN# <48>
CB_SD# <37>
WLAN_ON# <36>
BT_ON# <54>
CLK_ICH14 <25>
CLK_USB48 <25>
SUSB# <27,44>
SUSC# <34,44>
ICH8_PWROK_R
BAT_LL#
PM_DPRSLPVR <7,55>
PM_PWRBTN# <44>
BUF_PLT_RST# <7,13,22,31,36,40,44,51,53>
PM_RSMRST# <44>
CLK_PWRGD <25>
VRM_PWRGD <7,44,55,63>
ICH8_PWROK <7,44>
CL_CLK0 <7>
CL_DATA0 <7>
CL_VREF0
CL_VREF1
CL_RST# <7>
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
PM_RI#
PM_PWRBTN#
PM_SUS_STAT# <53>
XDP_DBR# <30>
PM_BMBUSY# <7>
STP_PCI# <25>
STP_CPU# <25,55>
PM_CLKRUN# <34,37,53>
PCIE_WAKE# <36,40>
INT_SERIRQ <37,44,53>
PM_THERM# <44>
VR_PWRGD_CLKEN
EXT_SMI# <44>
EXT_SCI# <44>
VGPU_SEL1
PM_TS# <25,44>
SB_SPKR <42>
MCH_SYNC# <7>
SR20 10KOhm
SR21 10KOhm
SR22 0Ohm /X
SR23 Do Not Stuff
SR24 0Ohm
SR25 Do Not Stuff /X
T187
T230
T231
T200
+3VSUS
+3VS
GND
PM_CLKRUN# SRN1A 8.2KOhm
PCI_FRAME# SRN1B 8.2KOhm
PCI_IRDY# SRN1C 8.2KOhm
PCI_TRDY# SRN1D 8.2KOhm
PCI_STOP# SRN1E 8.2KOhm
PCI_SERR# SRN1F 8.2KOhm
PCI_DEVSEL# SRN1G 8.2KOhm
PCI_PERR# SRN1H 8.2KOhm
PCI_LOCK# SRN2A 8.2KOhm
PCI_REQ#0 SRN2B 8.2KOhm
PCI_REQ#1 SRN2C 8.2KOhm
PCI_REQ#2 SRN2D 8.2KOhm
PCI_REQ#3 SRN2E 8.2KOhm
PM_THERM# SRN2F 8.2KOhm
INT_SERIRQ SRN2G 8.2KOhm
STP_CPU# SRN2H 8.2KOhm
PCI_INTB# SRN3A 8.2KOhm
PCI_INTC# SRN3B 8.2KOhm
PCI_INTD# SRN3C 8.2KOhm
INT_IRQ14 SRN3D 8.2KOhm
PCI_INTA# SRN3E 8.2KOhm
PCI_INTG# SRN3F 8.2KOhm
PCI_INTH# SRN3G 8.2KOhm
IDE_PIORDY SRN3H 8.2KOhm
VRM_PWRGD SR48 10KOhm
SB_SPKR SR49 1KOhm
Modify by V2.0G
SMB_CLK_S SR29 2.2KOhm
SMB_DAT_S SR30 2.2KOhm
PM_RSMRST# SR31 10KOhm
SQ1 H2N7002
SQ2 H2N7002
SMB_CLK_S <16,17,25,30,36,40>
SMB_DAT_S <16,17,25,30,36,40>
+12VS
SR50 10KOhm
D1 BAT54AW
D2 BAT54AW
PM_TS#
PM_EXTTS#0 <7>
PM_EXTTS#1 <7>
<16> DDR_EXTTS#0
<17> DDR_EXTTS#1
Modify by V2.0G
LINKALERT# SRN5A 10KOhm
SM_LINK0 SRN5B 10KOhm
SM_LINK1 SRN5C 10KOhm
EXT_SCI# SRN5D 10KOhm
SMB_CLK SR32 2.2KOhm
SMB_DAT SR33 2.2KOhm
PM_PWRBTN# SR28 10KOhm
PM_RI# SR35 10KOhm
BAT_LL# SR36 8.2KOhm
EXT_SMI# SR37 10KOhm
PCIE_WAKE# SR38 1KOhm
SR39 Do Not Stuff /X
PCI_PME# <13,34>
Modify by V2.0G
SR34 10KOhm
SQ3 H2N7002
VR_PWRGD_CLKEN
CLK_EN# <55>
SR40 Do Not Stuff /X
SR41 3.24KOhm
SR42 Do Not Stuff /X
SR43 453Ohm
SC22 Do Not Stuff /X
SC23 0.1UF/16V
CL_VREF1
CL_VREF0
1.1
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: Alan Chen
Size Custom
Project Name Z96S
Rev 2.0
Date: 星期三, 九月 30, 2007
Sheet 14 of 67


U3E
ICH8-M
U3F
ICH8-M
SR44
100Ohm
SD2
BAT54A
SC24
0.1uF/10V
SC27
0.1uF/10V
SC28
0.1uF/10V
+5VREFSUS
SL2
80Ohm/100Mhz
SCE1
Do Not Stuff
/X
SC29
10UF/6.3V
SC30
10UF/6.3V
SC31
1UF/6.3V
SC32
Do Not Stuff
/X
SD3
BAT54A
SR45
100Ohm
SL3
120Ohm/100Mhz
SC43
Do Not Stuff
/X
SC44
1UF/6.3V
SR46
0ohm
SC46
1UF/6.3V
SC50
1UF/6.3V
SR47
0Ohm
SC57
0.1uF/10V
SC58
0.1uF/10V
SC60
0.1uF/10V
SL4
120Ohm/100Mhz
SC61
Do Not Stuff
/X
SC62
1UF/6.3V
SC63
10UF/6.3V
SL1
80Ohm/100Mhz
SC25
22UF/6.3V
SC26
0.1uF/10V
SC33
10UF/6.3V
SC34
0.1uF/16V
SC35
0.1uF/10V
SC36
22UF/6.3V
SC37
4.7UF/6.3V
SC38
Do Not Stuff
/X
SC39
0.1uF/10V
SC40
0.1uF/10V
SC4
Do Not Stuff
/X
SC42
0.1uF/10V
SC45
0.01UF/16V
SC47
Do Not Stuff
/X
SC48
0.1uF/10V
SC49
0.1uF/10V
SC51
0.1uF/10V
SC52
0.1uF/10V
SC53
0.1uF/10V
SC54
0.1uF/10V
SC55
0.01UF/16V
SC56
0.01UF/16V
SC59
10UF/6.3V
SC64
1UF/6.3V
SC65
0.1uF/10V
+VCC_RTC
+5VS
+3VS
+1.5VS
+1.5VS_PCIE_ICH
+3VSUS
+5VSUS
+1.5VS
+VCCP
+VCCP_ICH
+1.5VS
+3VS
+1.5VS
+3VS
+VCCP_ICH
+1.25VS
+3VS
+3VSUS
+3VSUS
+3VS
GND
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: 星期二, 五月 30, 2007
Sheet 15 of 67

REV Type



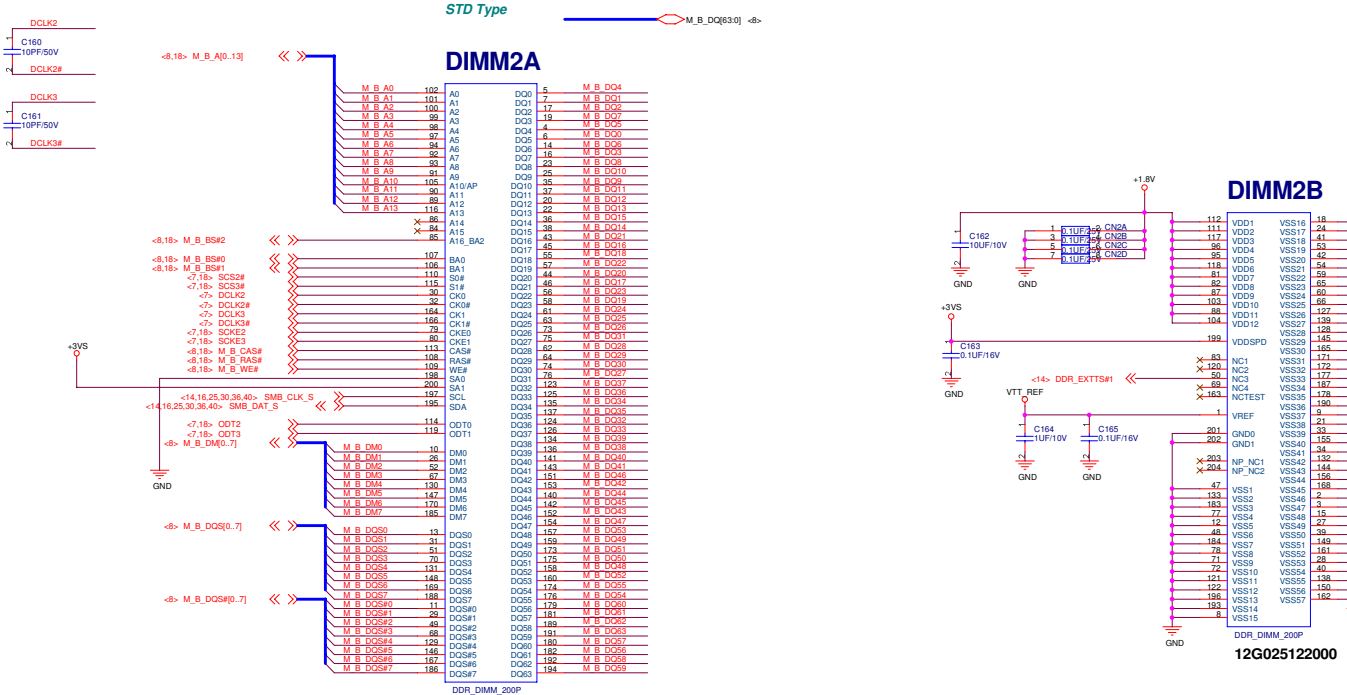
12G025332003



12G025332003

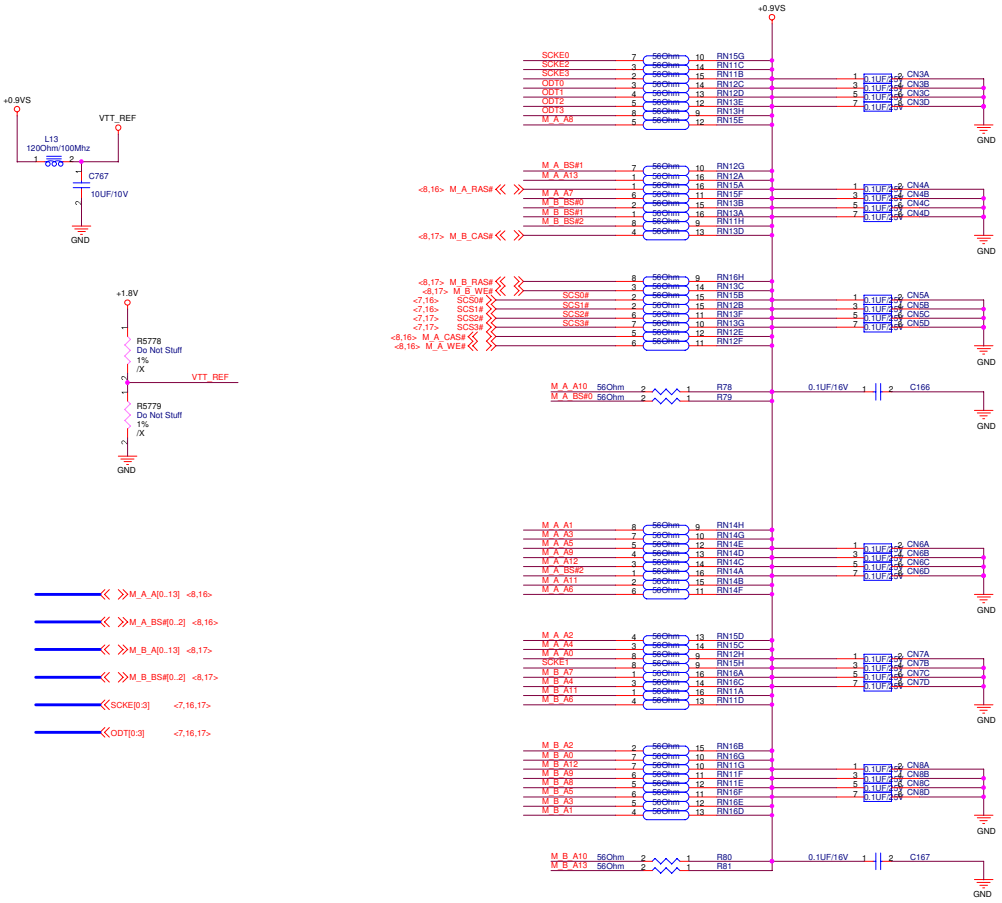
1.1

ASUSTeK COMPUTER INC.	Title :	DDR2 SO-DIMM0	
	Engineer:	Alan Chen	
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 16 of 67		



1.1

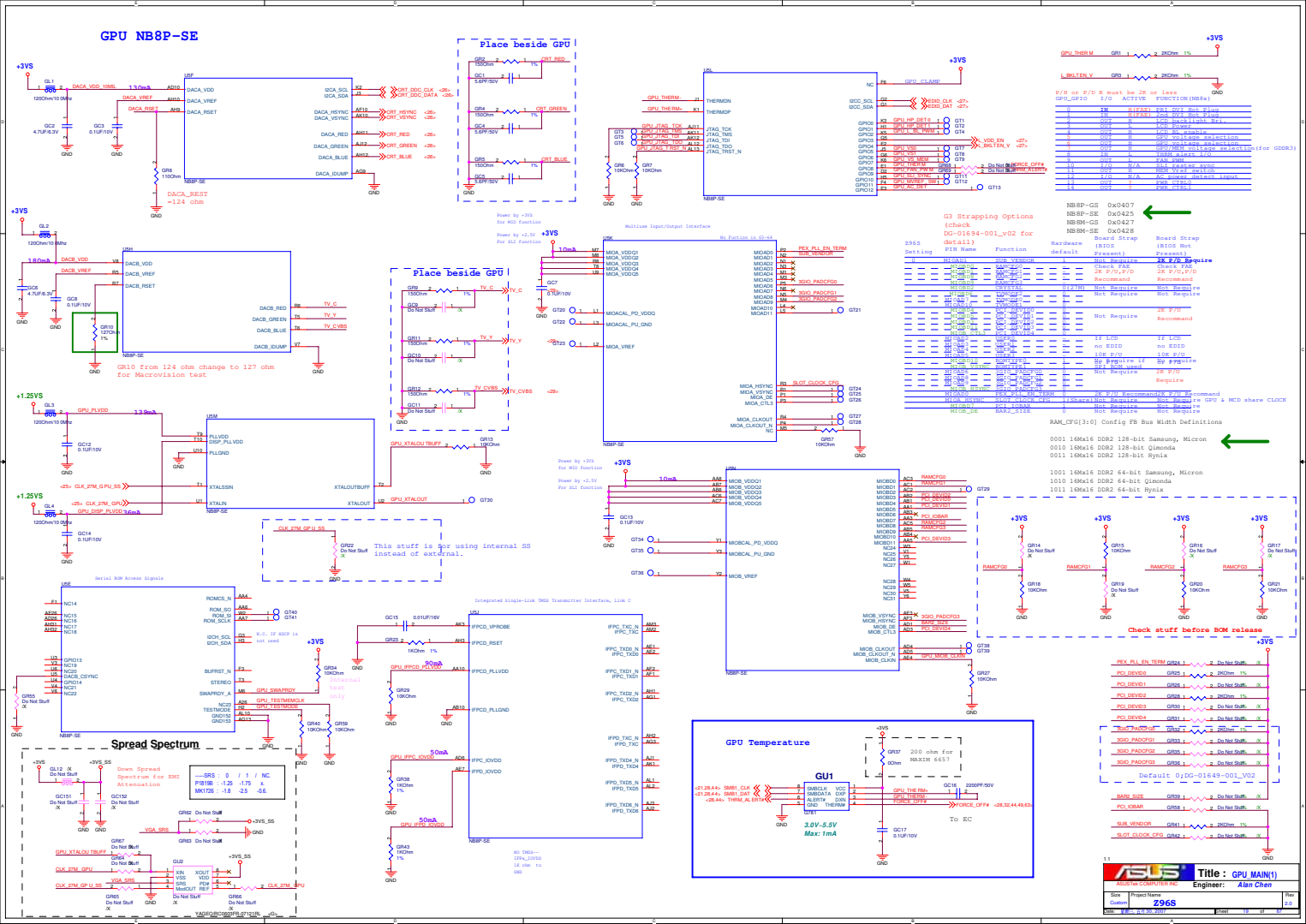
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期二, 六月 30, 2007	Sheet 17 of 67	

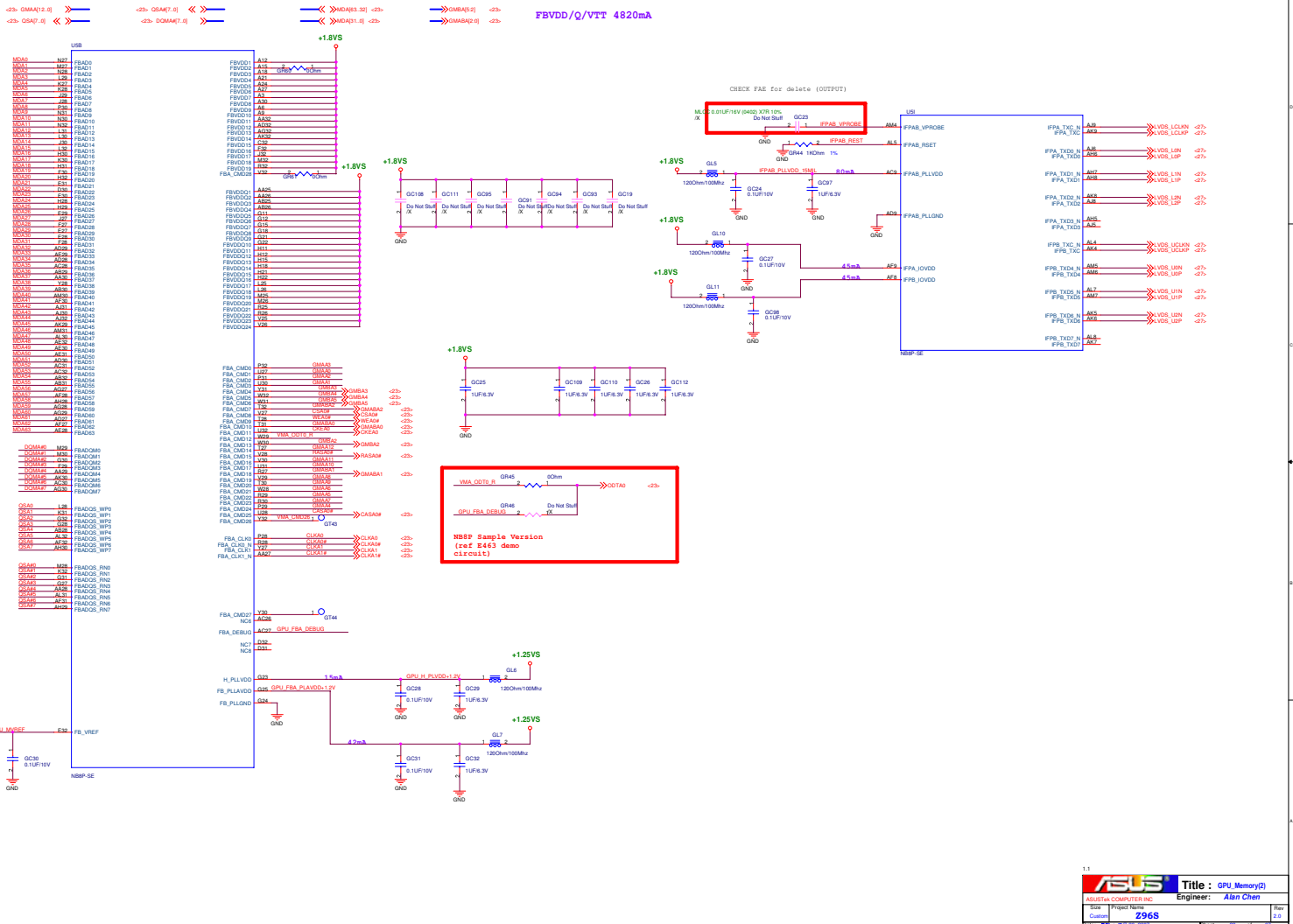


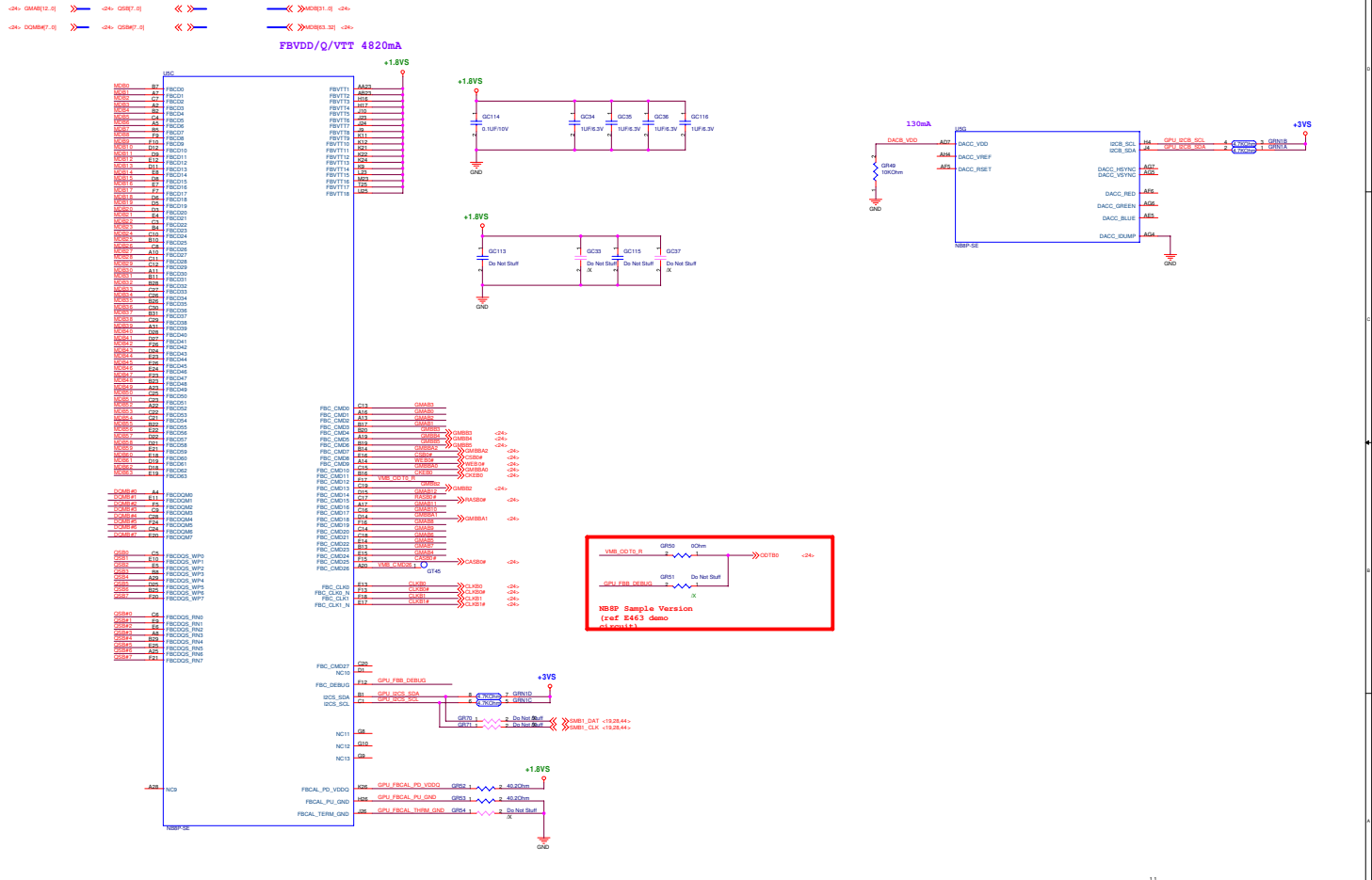
1.1

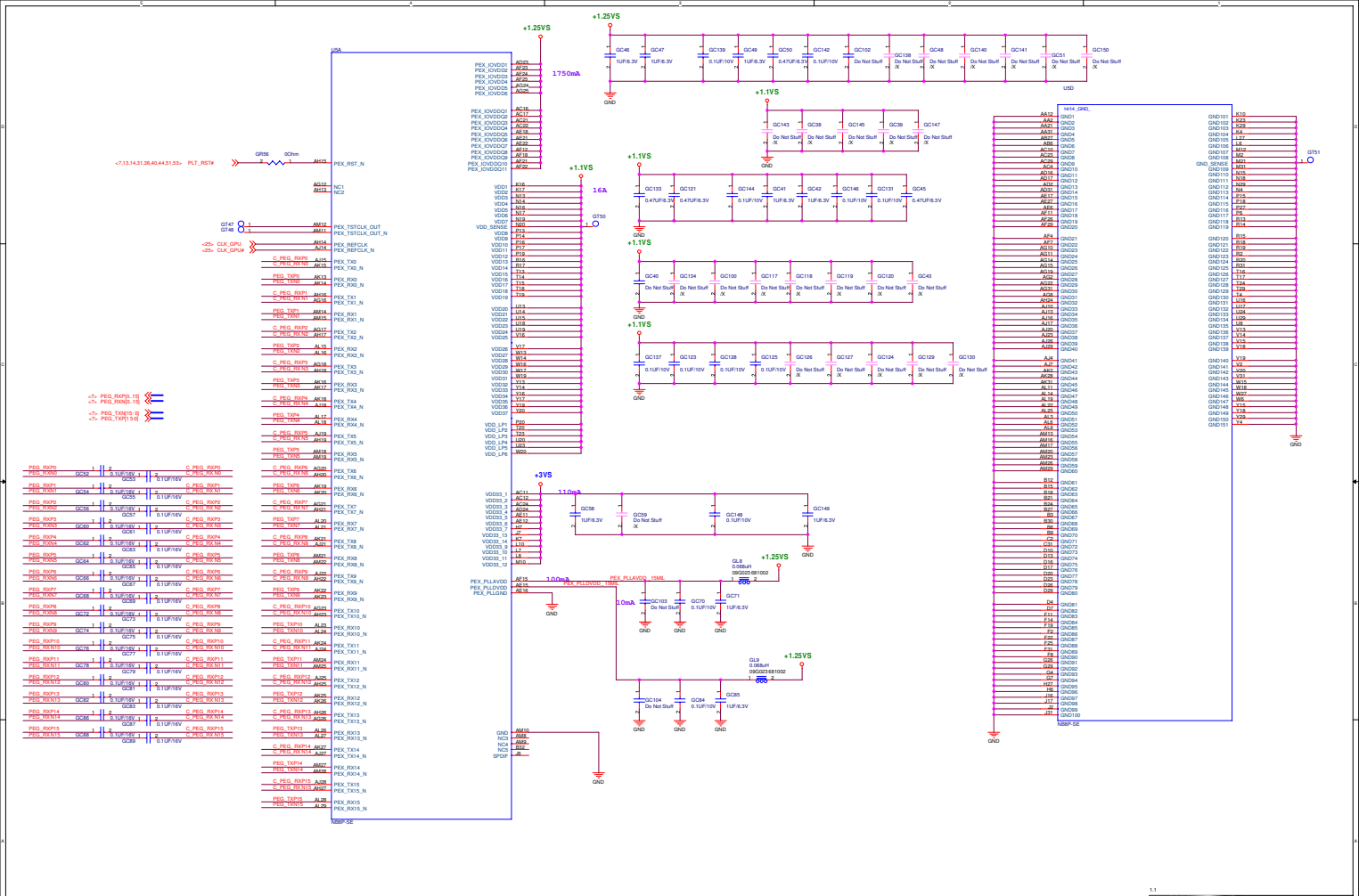
ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 18 of 67	

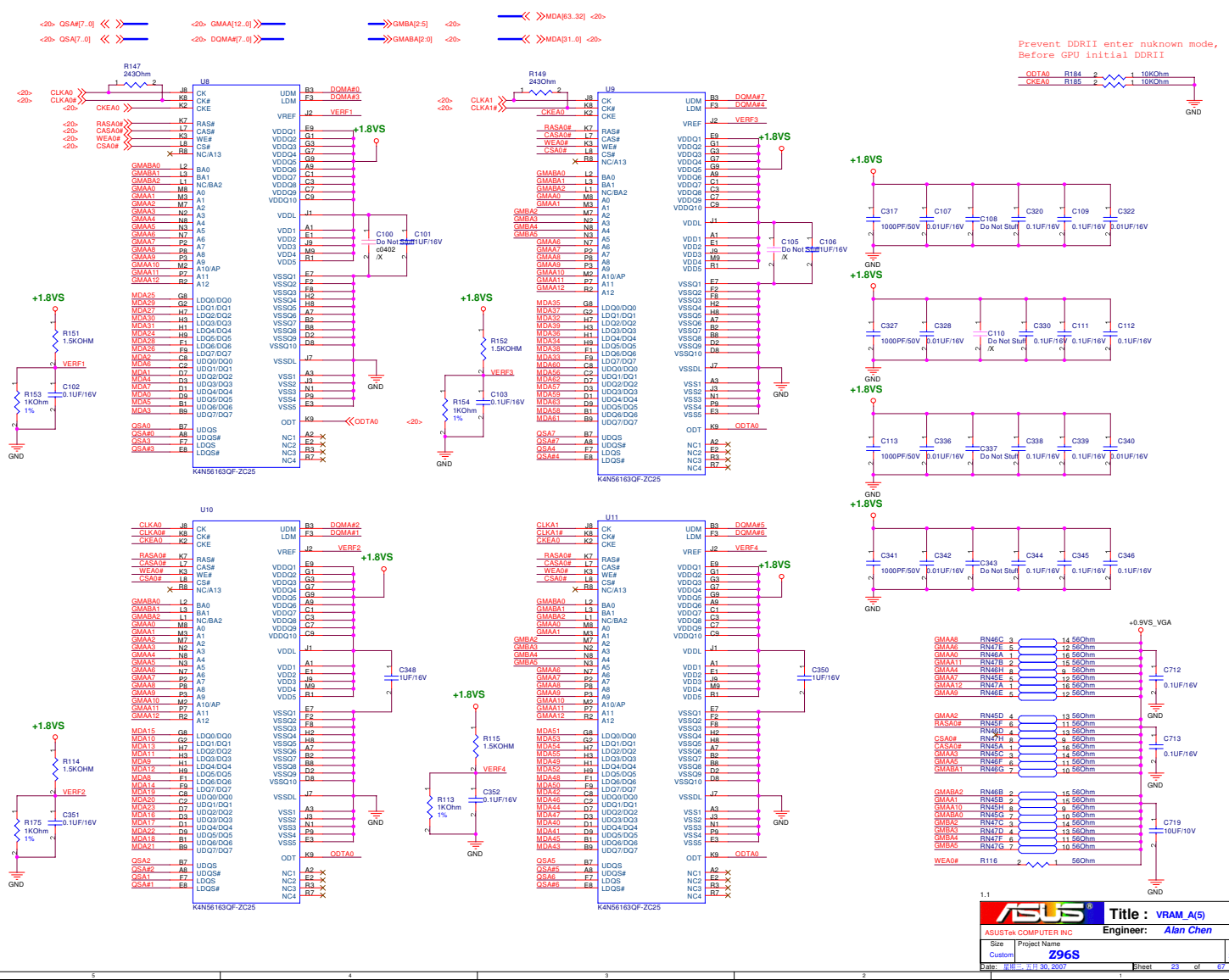
GPU NB8P-SE

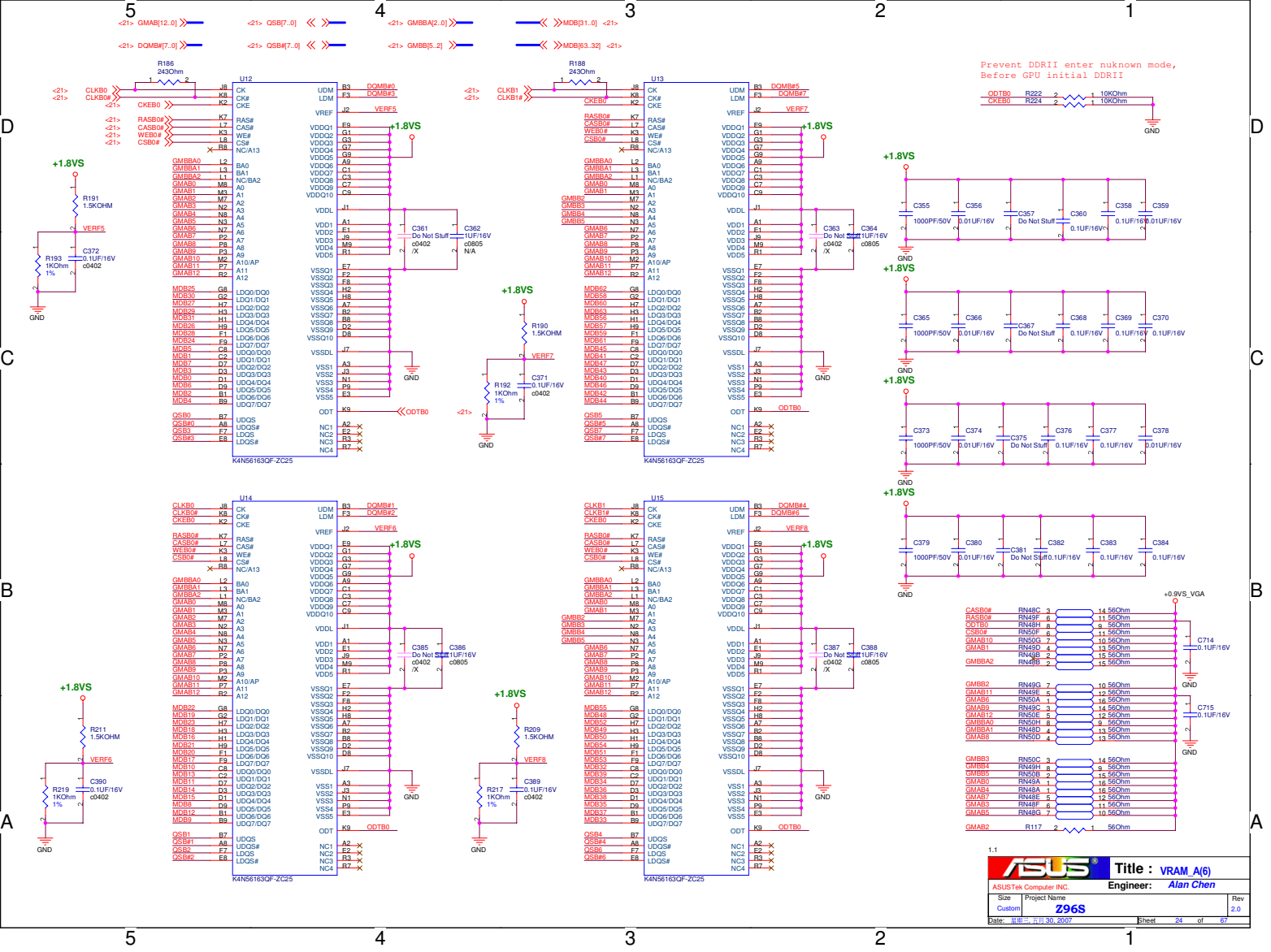

Place beside GPU
Place beside GPU
Spread Spectrum
GPU Temperature
GU1
DACA_REST
>124 ohm
GR10 from 124 ohm change to 127 ohm
for Macrovision test
Down Spread
Spectrum for EMI
Attenuation
G3 Strapping Options
(check
DG-01694-001_v02 for
detail)
Z96S
Setting
PIN Name
Function
Hardware
default
Board Strap
(BIOS Not
Present)
Board Strap
(BIOS Not
Present)
Not Require
2K P/D Require
Check FAE
2K P/U,P/D
Recommand
Not Require
Not Require
2K P/U
Recommand
If LCD
no EDID
10K P/U
No Require if
SLI Card used
Not Require
2K P/U
Require
2K P/U Recommand
Not Require
Not Require GPU & MCD share CLOCK
Not Require
Not Require
NB8P-GS 0x0407
NB8P-SE 0x0425
NB8M-GS 0x0427
NB8M-SE 0x0428
RAM_CFG[3:0] Config FB Bus Width Definitions
0001 16Mx16 DDR2 128-bit Samsung, Micron
0010 16Mx16 DDR2 128-bit Qimonda
0011 16Mx16 DDR2 128-bit Hynix
1001 16Mx16 DDR2 64-bit Samsung, Micron
1010 16Mx16 DDR2 64-bit Qimonda
1011 16Mx16 DDR2 64-bit Hynix
Check stuff before BOM release
Default 0;DG-01649-001_V02
Title : GPU_MAIN(1)
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: Tuesday, July 10, 2007
Sheet 19 of 67

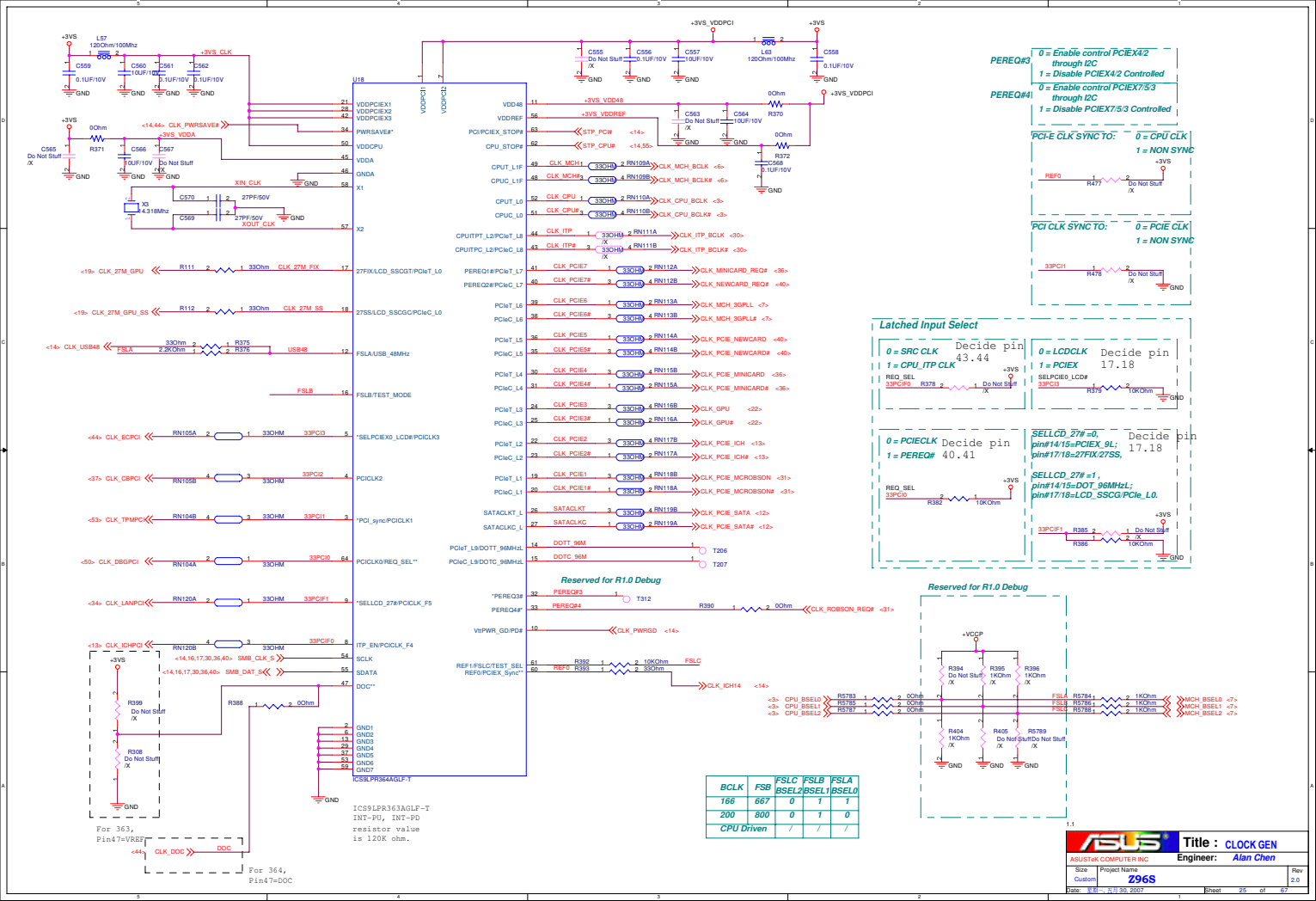

FBVDD/Q/VTT 4820mA
CHECK FAE for delete (OUTPUT)
USB
NB8P-SE
USI
NB8P Sample Version
(ref E463 demo
circuit)
Title : GPU_Memory(2)
ASUSTeK COMPUTER INC.
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: 星期一, 五月 30, 2007
Sheet 20 of 67

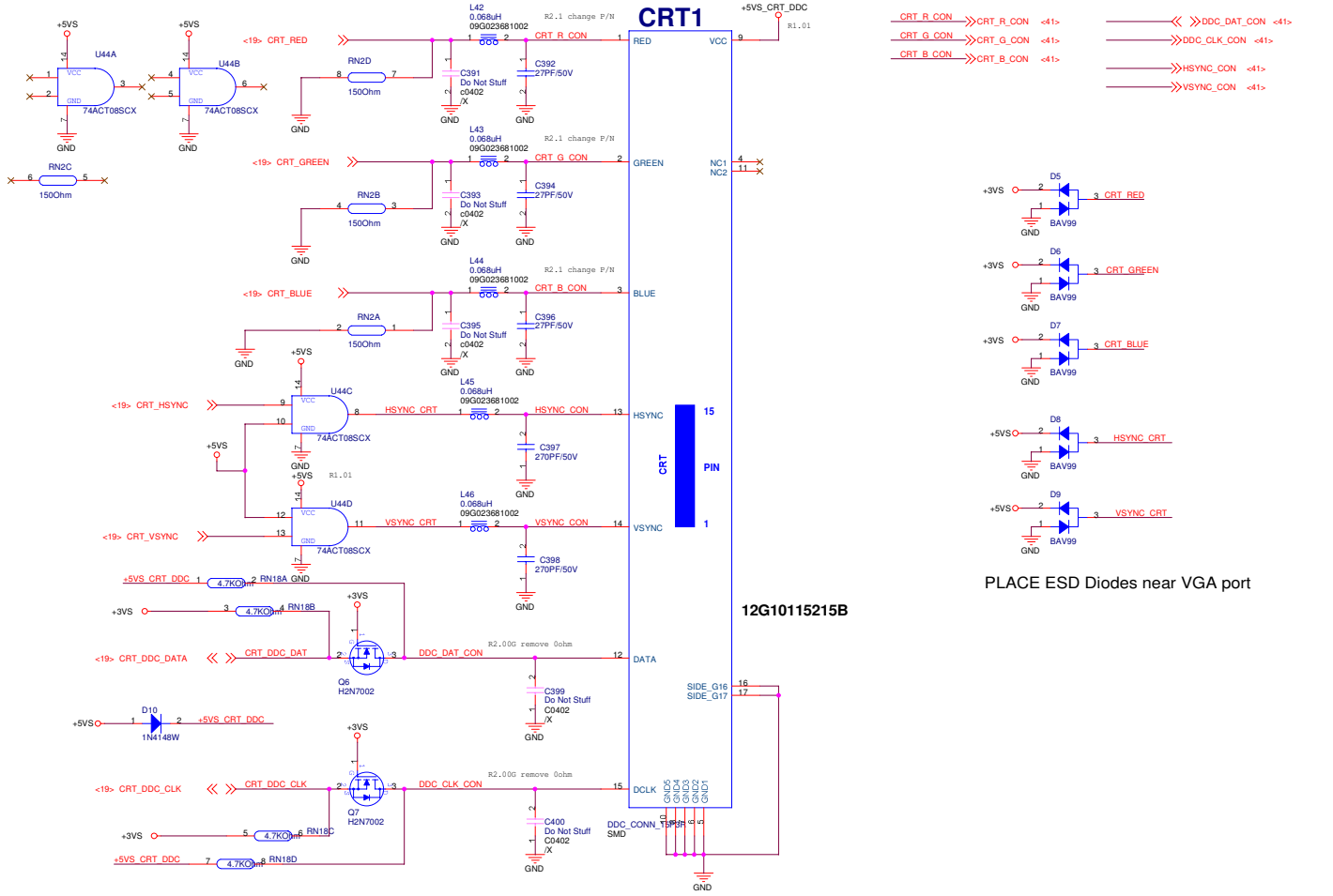

FBVDD/Q/VTT 4820mA
+1.8VS
+3VS
130mA
NB8P-SE
Do Not Stuff
NB8P Sample Version
(ref E463 demo
GPU_PCI-E(3)
Alan Chen
Z96S


+1.25VS
+1.1VS
+3VS
GND
USD
U8A
NB8P-SE
Title : GPU_POWER_GND(4)
ASUSTek COMPUTER INC
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: 日期二, 8 月 30, 2007
Sheet 22 of 67


Prevent DDRII enter nuknown mode,
Before GPU initial DDRII
ODTA0 R184 10KOhm
CKEA0 R185 10KOhm
GND
U8
U9
U10
U11
K4N56163QF-ZC25
+1.8VS
+0.9VS_VGA
R147 243Ohm
R149 243Ohm
R151 1.5KOHM
R152 1.5KOHM
R114 1.5KOHM
R115 1.5KOHM
R153 1KOhm 1%
R154 1KOhm 1%
R175 1KOhm 1%
R113 1KOhm 1%
C100 Do Not Stuff c0402 /X
C101 1UF/16V
C102 0.1UF/16V
C103 0.1UF/16V
C105 Do Not Stuff /X
C106 1UF/16V
C317 1000PF/50V
C107 0.01UF/16V
C108 Do Not Stuff
C320 0.1UF/16V
C109 0.1UF/16V
C322 0.01UF/16V
C327 1000PF/50V
C328 0.01UF/16V
C110 Do Not Stuff /X
C330 0.1UF/16V
C111 0.1UF/16V
C112 0.1UF/16V
C113 1000PF/50V
C336 0.01UF/16V
C337 Do Not Stuff
C338 0.1UF/16V
C339 0.1UF/16V
C340 0.01UF/16V
C341 1000PF/50V
C342 0.01UF/16V
C343 Do Not Stuff
C344 0.1UF/16V
C345 0.1UF/16V
C346 0.1UF/16V
C348 1UF/16V
C350 1UF/16V
C351 0.1UF/16V
C352 0.1UF/16V
C712 0.1UF/16V
C713 0.1UF/16V
C719 10UF/10V
RN46C 56Ohm
RN47E 56Ohm
RN46A 56Ohm
RN47B 56Ohm
RN46H 56Ohm
RN45E 56Ohm
RN47A 56Ohm
RN46E 56Ohm
RN45D 56Ohm
RN47H 56Ohm
RN45A 56Ohm
RN45C 56Ohm
RN46F 56Ohm
RN46G 56Ohm
RN46B 56Ohm
RN45B 56Ohm
RN45H 56Ohm
RN45G 56Ohm
RN47C 56Ohm
RN47D 56Ohm
RN47G 56Ohm
R116 56Ohm
Title : VRAM_A(5)
ASUSTek COMPUTER INC
Engineer: Alan Chen
Size Custom
Project Name Z96S
Rev 2.0
Date: 五月 30, 2007
Sheet 23 of 67


Prevent DDRII enter nuknown mode,
Before GPU initial DDRII
Title : VRAM_A(6)
ASUSTek Computer INC.
Engineer: Alan Chen
Project Name
Z96S
Rev
2.0
Sheet 24 of 67
Date: 星期三, 五月 30, 2007


U18
ICS9LPR364AGLF-T
ICS9LPR363AGLF-T
INT-PU, INT-PD
resistor value
is 120K ohm.
For 363,
Pin47=VREF
For 364,
Pin47=DOC
Reserved for R1.0 Debug
Reserved for R1.0 Debug
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
PCI-E CLK SYNC TO:
0 = CPU CLK
1 = NON SYNC
PCI CLK SYNC TO:
0 = PCIE CLK
1 = NON SYNC
Latched Input Select
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27# =0,
pin#14/15=PCIEX_9L;
pin#17/18=27FIX/27SS,
SELLCD_27# =1 ,
pin#14/15=DOT_96MHzL;
pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
BCLK | FSB | FSLC BSEL2 | FSLB BSEL1 | FSLA BSEL0
166 | 667 | 0 | 1 | 1
200 | 800 | 0 | 1 | 0
CPU Driven | | / | / | /
ASUSTeK COMPUTER INC
Title : CLOCK GEN
Engineer: Alan Chen
Project Name 2968
Rev 2.0
Sheet 25 of 67



12G10115215B

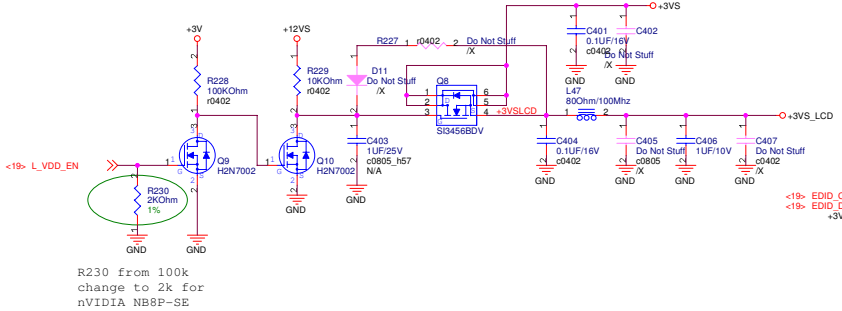
PLACE ESD Diodes near VGA port

1.1

ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 六月 30, 2007	Sheet 26 of 67	

LCD Backlight Control

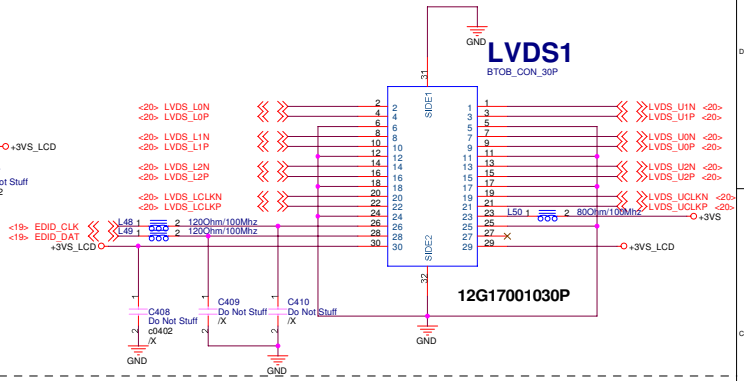
LCD Power



R230 from 100k
change to 2k for
nVIDIA NB8P-SE

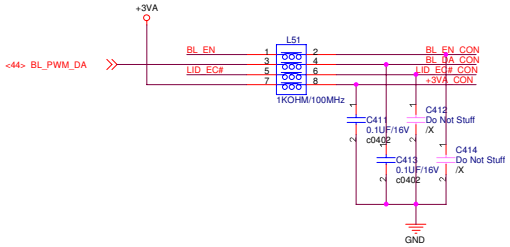
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

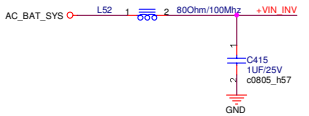
LCD LVDS Interface

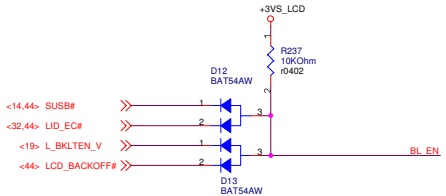


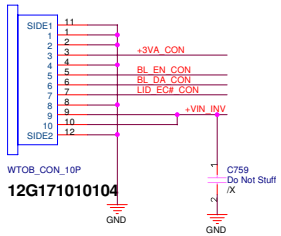
INVERTER
Interface/Speaker
CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.





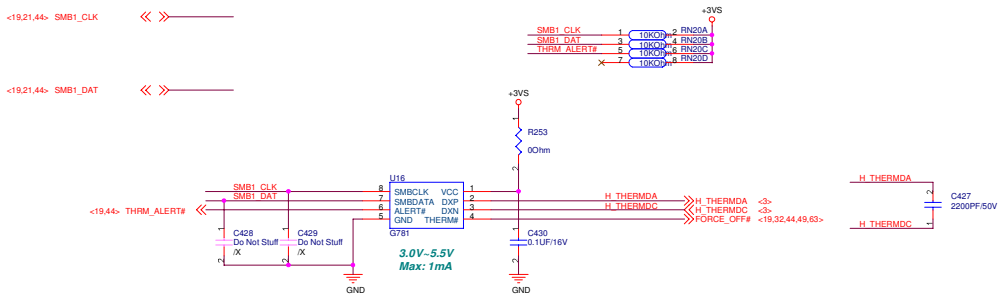




1.1

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期二, 五月 30, 2007	Sheet 27 of 67	

Thermal Sensor

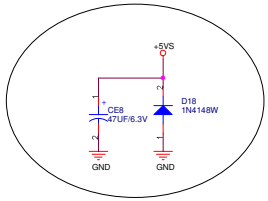


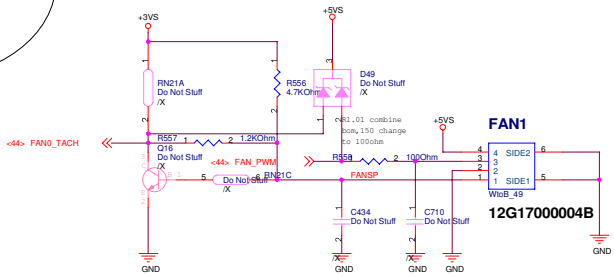
Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



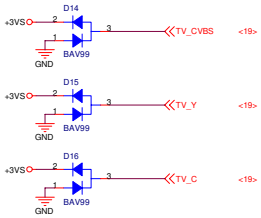


CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted by EC

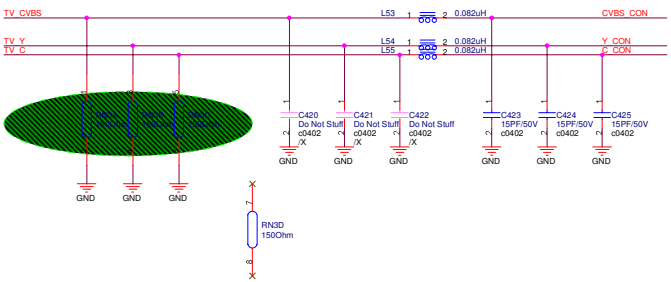
1.1

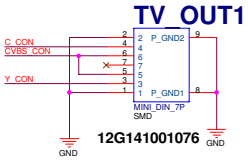
ASUSTeK COMPUTER INC.	Title : THER SENSOR & FAN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 28 of 67	

TV OUT



PLACE ESD
Diodes near
TV port

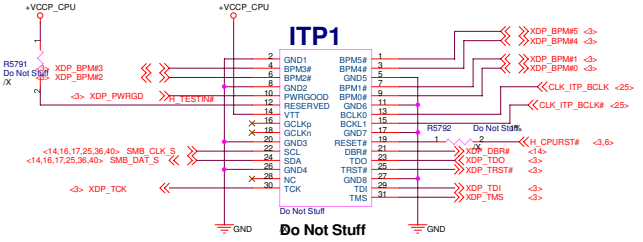




1.1

ASUSTeK COMPUTER INC	Title : TV OUT & DVI CON.	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 29 of 67	

ITP



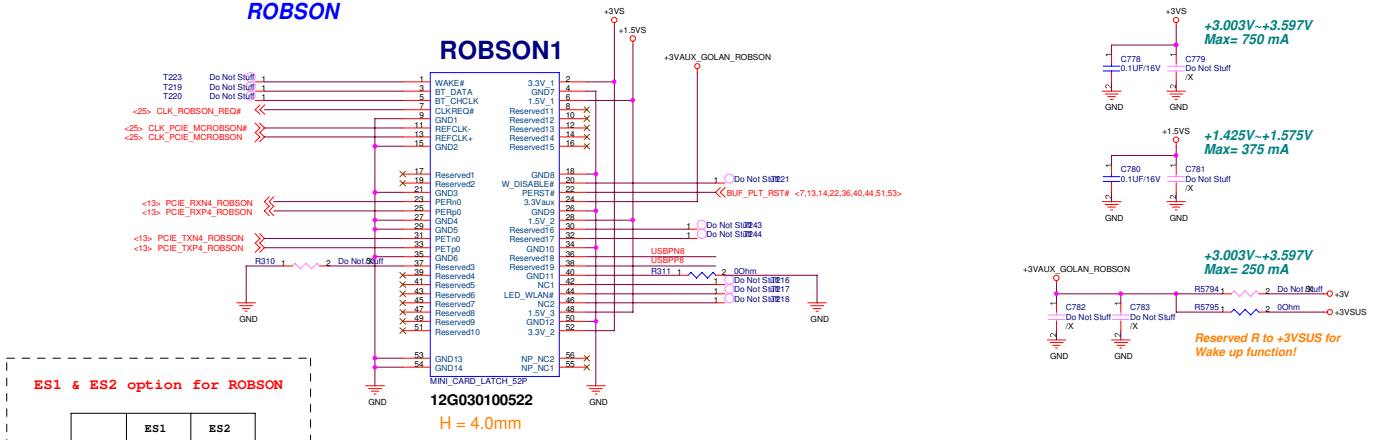
1.1

Title : ITP

ASUSTek Computer INC. Engineer: Alan Chen

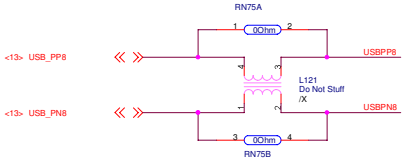
Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期三, 五月 30, 2007 Sheet 30 of 67



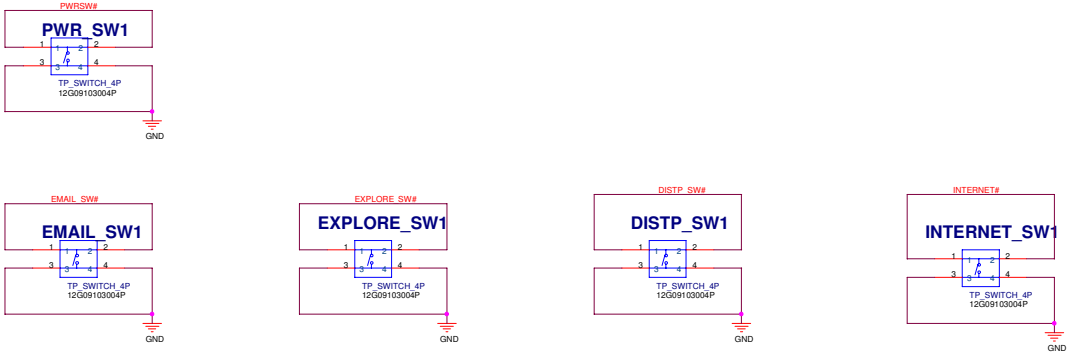
ES1 & ES2 option for ROBSON

	ES1	ES2
R310	N/A	Mount
R311	Mount	N/A

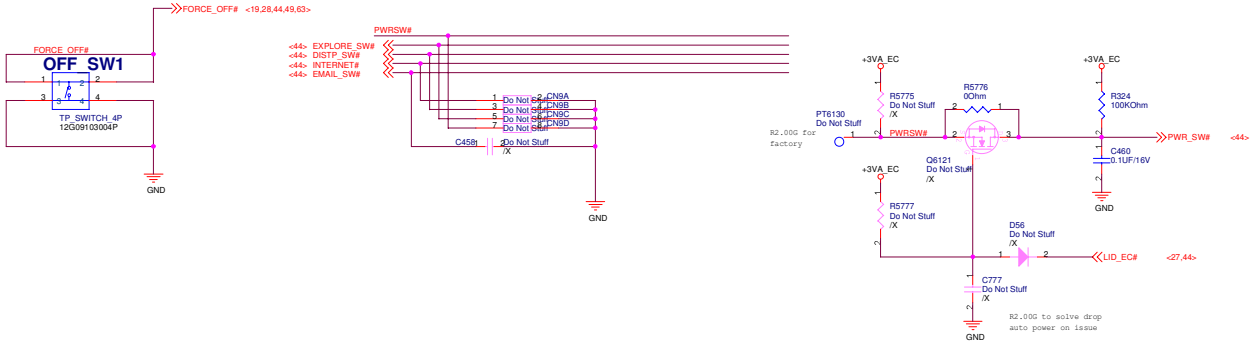


1.1

ASUSTek Computer INC.	Title : Mini Card	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 31 of 67	

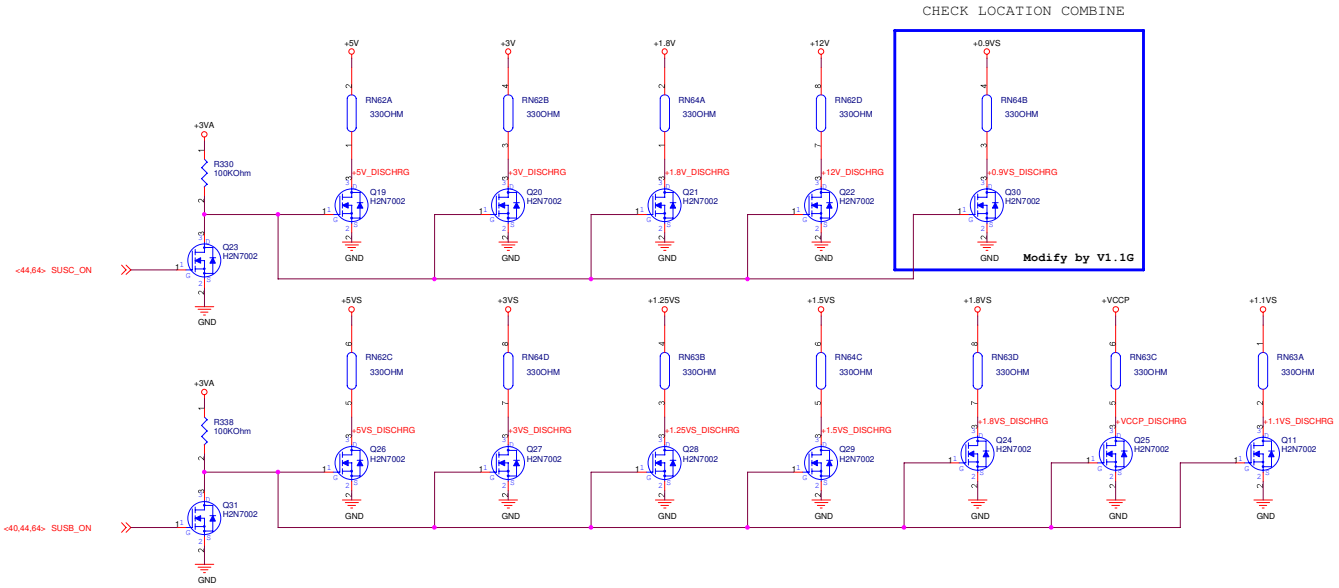


SHUT_DOWN#



1.1

ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 32 of 67	



1.1

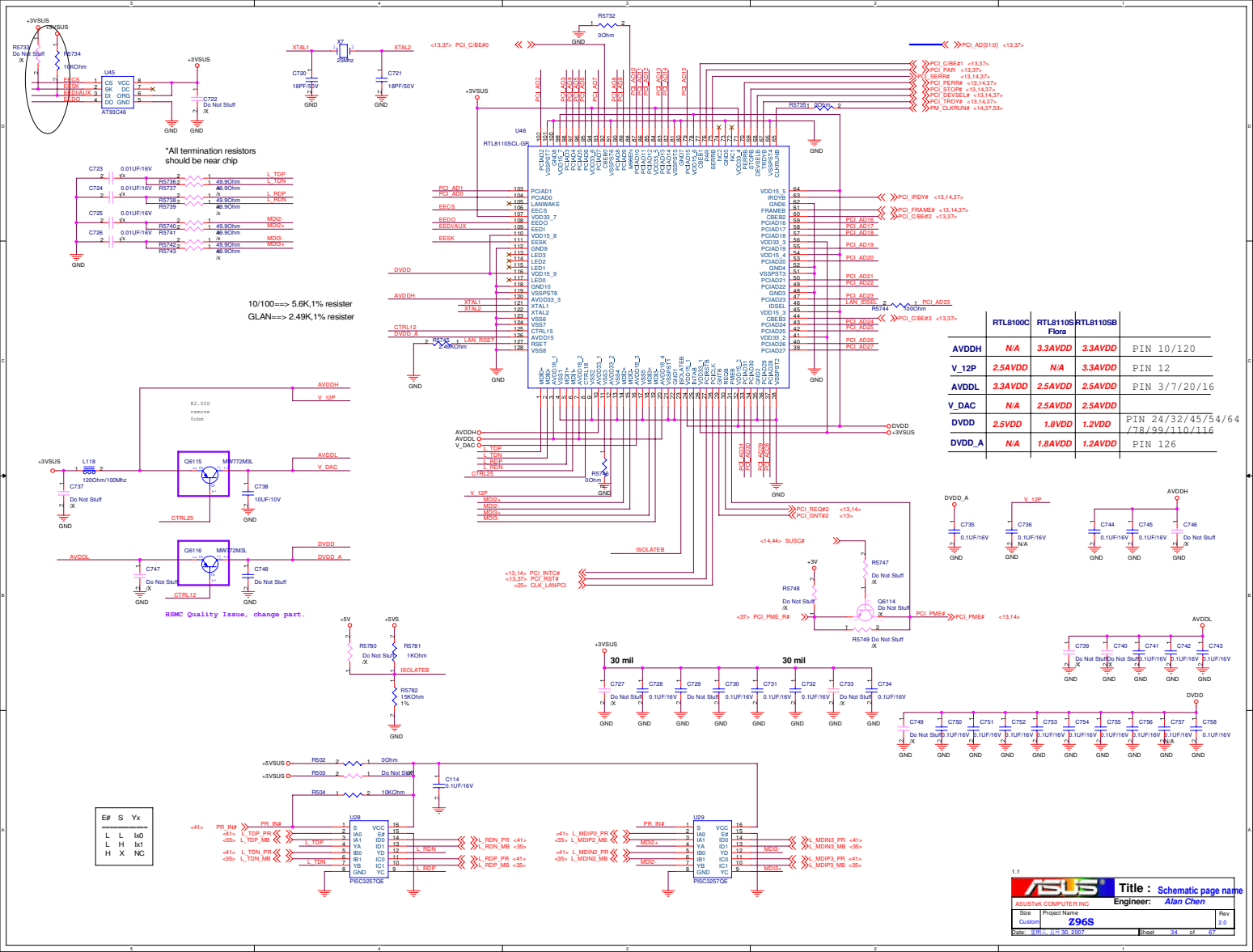
Title : DISCHARGE & EMI CAP

ASUSTeK COMPUTER INC. NB1

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期二, 十月 30, 2007 Sheet 33 of 67

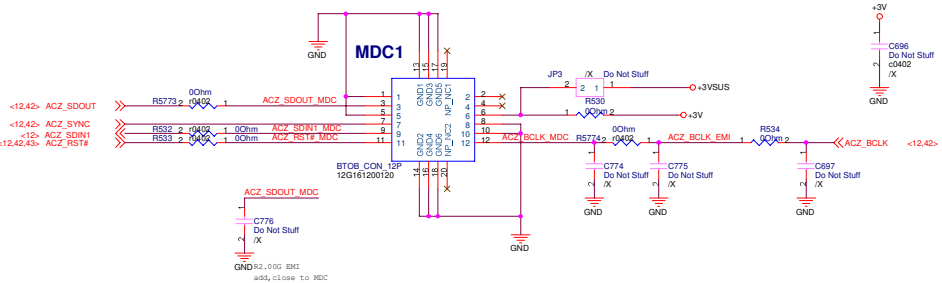


	RTL8100C	RTL8110S Flora	RTL8110SB	
AVDDH	N/A	3.3AVDD	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	N/A	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD	PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	2.5AVDD	
DVDD	2.5VDD	1.8VDD	1.2VDD	PIN 24/32/45/54/64 /78/99/110/116
DVDD_A	N/A	1.8AVDD	1.2AVDD	PIN 126

E#	S	Yx
L	L	Ix0
L	H	Ix1
H	X	NC

Title :	Schematic page name	
ASUSTeK COMPUTER INC	Engineer:	Alan Chen
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期二, 五月 30, 2007	Sheet 34 of 67	

MDC CONN.

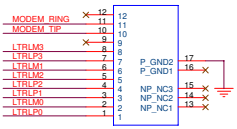


RING1

WTOB_CON_2P

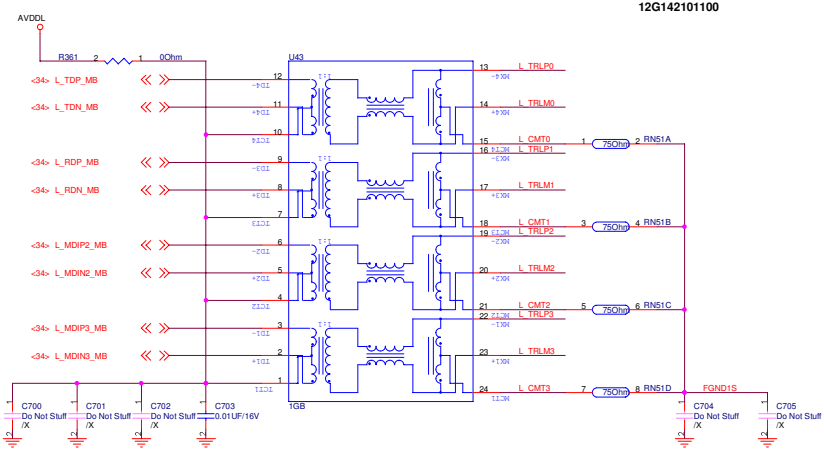
12G17100002C

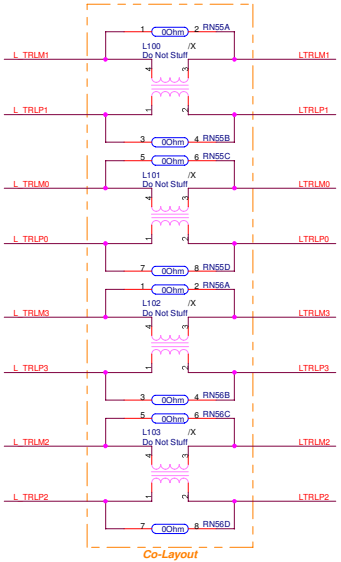
RJ45_RJ11



MODULAR_JACK_12P

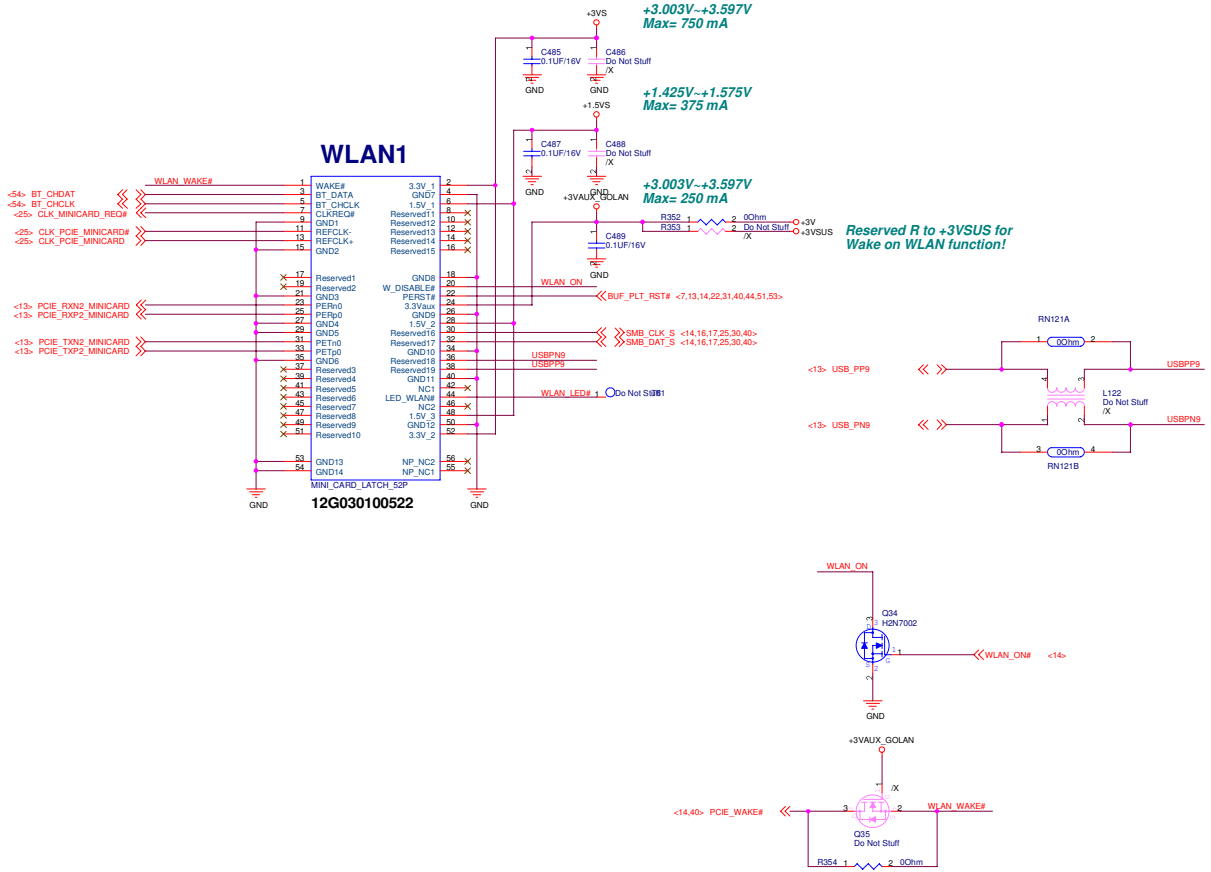
12G142101100





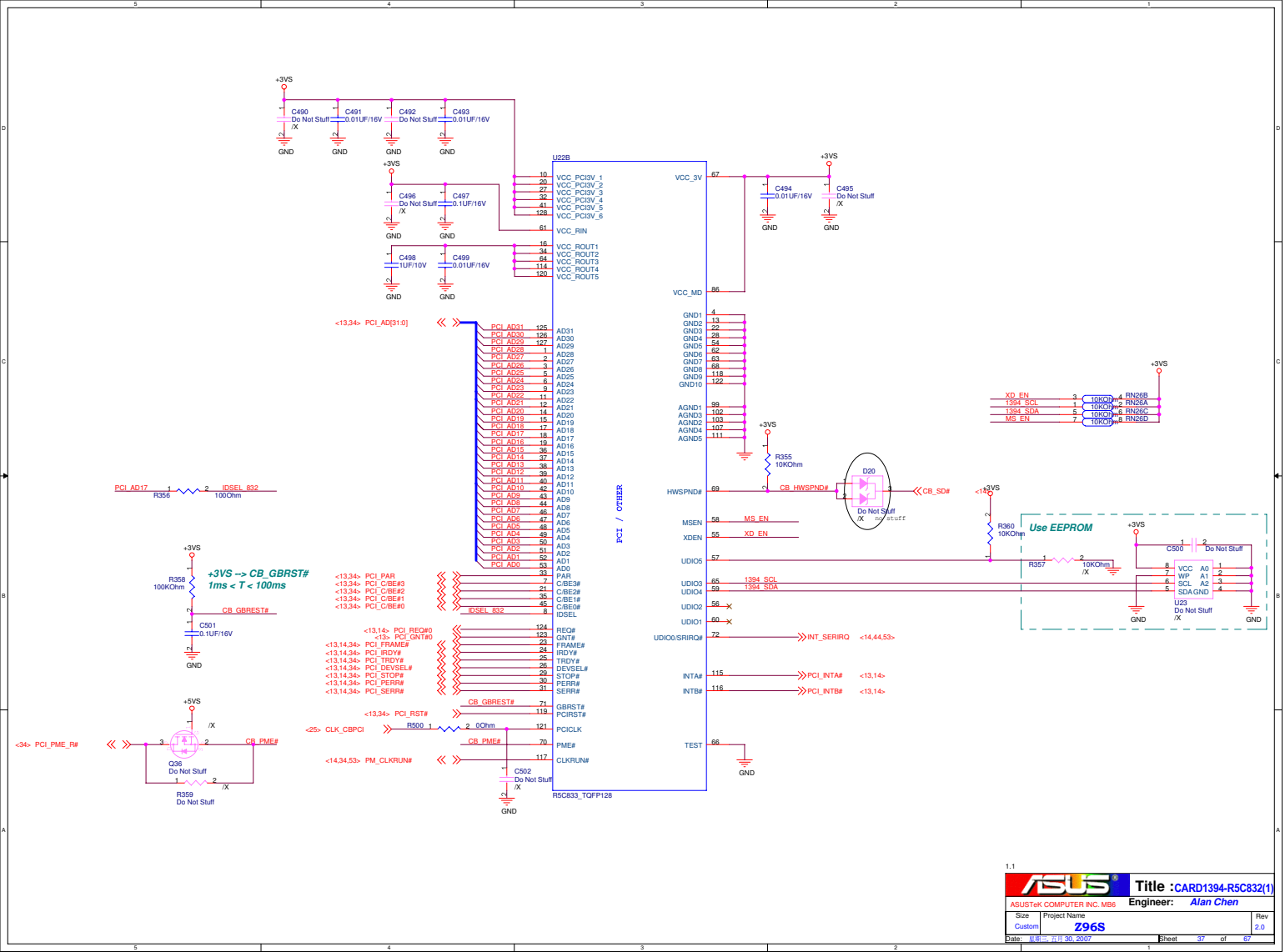
1.1

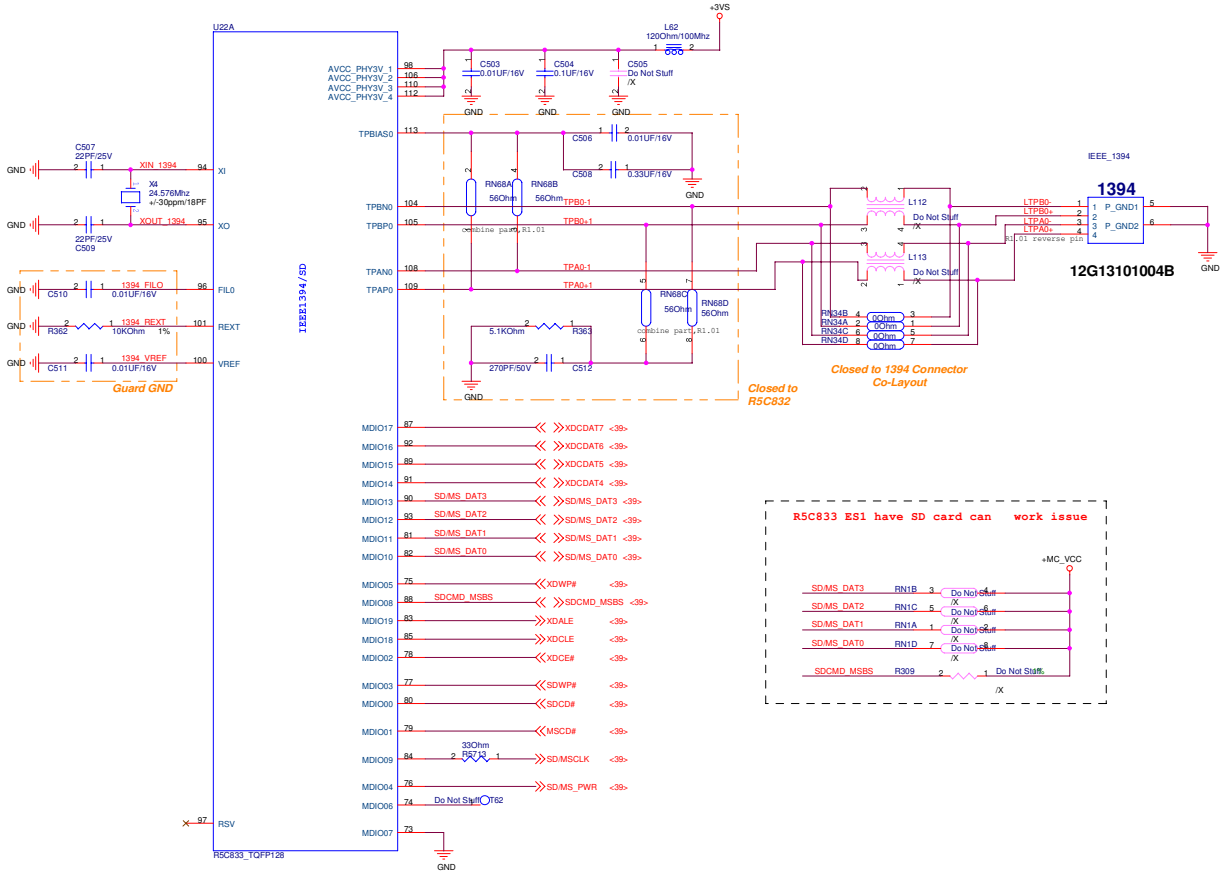
ASUSTeK COMPUTER INC.	Title : RJ45&RJ11	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 35 of 67	



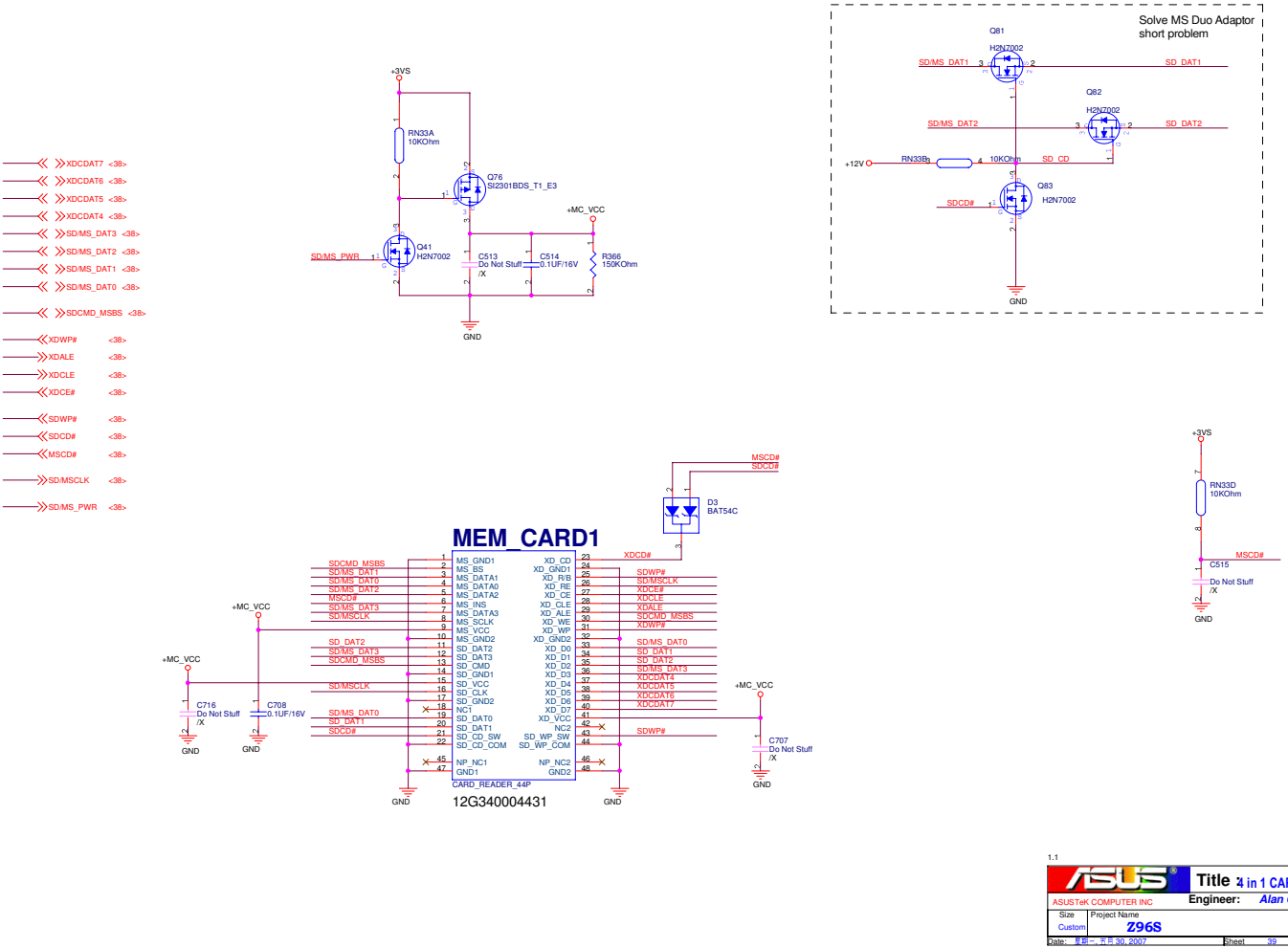
1.1

ASUSTeK COMPUTER INC.	Title : MINICARD	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 36 of 67	


U22B
R5C833_TQFP128
PCI / OTHER
+3VS
GND
+5VS
C490 Do Not Stuff /X
C491 0.01UF/16V
C492 Do Not Stuff
C493 0.01UF/16V
C494 0.01UF/16V
C495 Do Not Stuff /X
C496 Do Not Stuff /X
C497 0.1UF/16V
C498 1UF/10V
C499 0.01UF/16V
C500 Do Not Stuff
C501 0.1UF/16V
C502 Do Not Stuff /X
R355 10KOhm
R356 100Ohm
R357 10KOhm /X
R358 100KOhm
R359 Do Not Stuff
R360 10KOhm
R500 0Ohm
RN26A 10KOhm
RN26B 10KOhm
RN26C 10KOhm
RN26D 10KOhm
D20 Do Not Stuff /X
Q36 Do Not Stuff
U23 Do Not Stuff /X
Use EEPROM
+3VS --> CB_GBRST#
1ms < T < 100ms
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND3
AGND2
AGND4
AGND5
HWSPND#
CB_HWSPND#
CB_SD#
MSEN
MS_EN
XDEN
XD_EN
UDIO5
UDIO3
UDIO4
1394_SCL
1394_SDA
UDIO2
UDIO1
UDIO0/SRIRQ#
INT_SERIRQ
INTA#
PCI_INTA#
INTB#
PCI_INTB#
TEST
<13,34> PCI_AD[31:0]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
<13,34> PCI_PAR
<13,34> PCI_C/BE#3
<13,34> PCI_C/BE#2
<13,34> PCI_C/BE#1
<13,34> PCI_C/BE#0
IDSEL_832
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
<13,14> PCI_REQ#0
<13> PCI_GNT#0
REQ#
GNT#
<13,14,34> PCI_FRAME#
<13,14,34> PCI_IRDY#
<13,14,34> PCI_TRDY#
<13,14,34> PCI_DEVSEL#
<13,14,34> PCI_STOP#
<13,14,34> PCI_PERR#
<13,14,34> PCI_SERR#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
CB_GBRST#
GBRST#
<13,34> PCI_RST#
PCIRST#
<25> CLK_CBPCI
PCICLK
CB_PME#
PME#
<14,34,53> PM_CLKRUN#
CLKRUN#
<34> PCI_PME_R#
PCI_AD17
IDSEL_832
<13>
CB_GBRST#
XD_EN
1394_SCL
1394_SDA
MS_EN
<14,44,53>
<13,14>
<13,14>
1.1
Title : CARD1394-R5C832(1)
ASUSTeK COMPUTER INC. MB6
Engineer: Alan Chen
Size: Custom
Project Name: Z96S
Rev: 2.0
Date: 星期三, 六月 30, 2007
Sheet 37 of 67



1.1	Title : CARD1394-R5C832(2)		
ASUSTeK COMPUTER INC. MB6	Engineer: Alan Chen		
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 38 of 67		



1.1

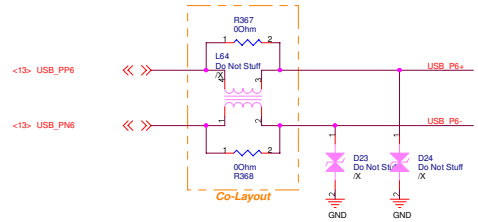
ASUSTeK COMPUTER INC

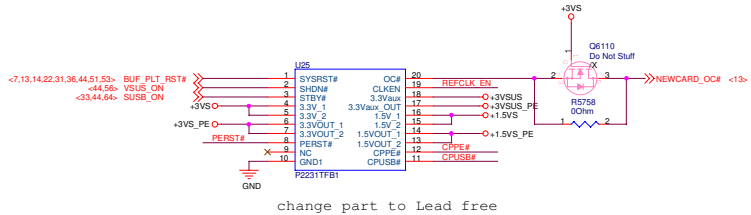
Title: 4 in 1 CARD READER

Engineer: Alan Chen

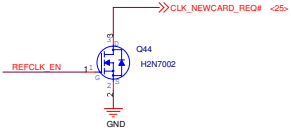
Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期一, 十月 30, 2007 Sheet 39 of 67





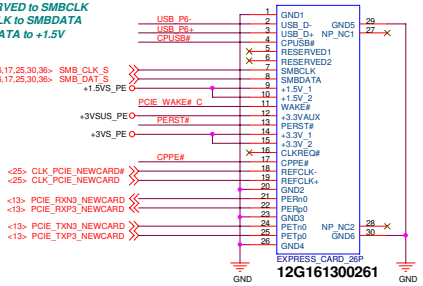
change part to Lead free

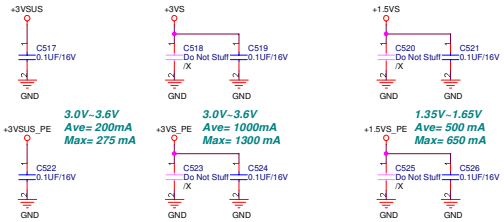


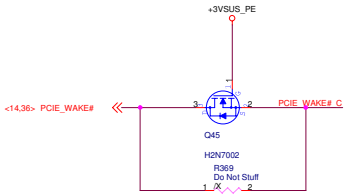
NewCard
Header

EXPRESS1

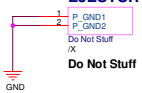
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V







NewCard
Ejecter



Do Not Stuff

1.1

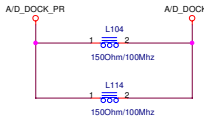
Title : NEWCARD

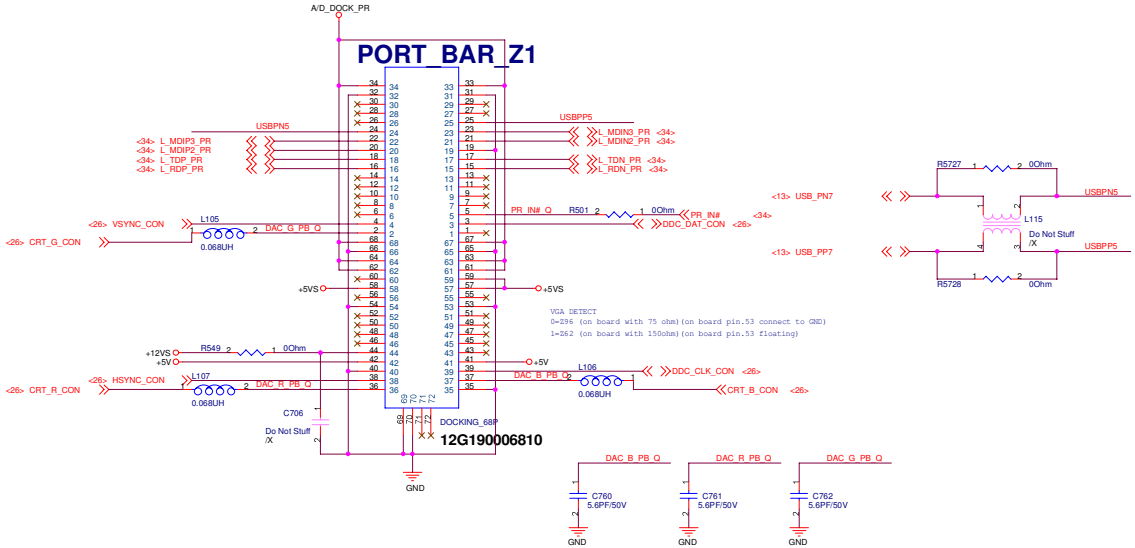
ASUSTeK COMPUTER INC. NB1 Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期三, 五月 30, 2007 Sheet 40 of 67

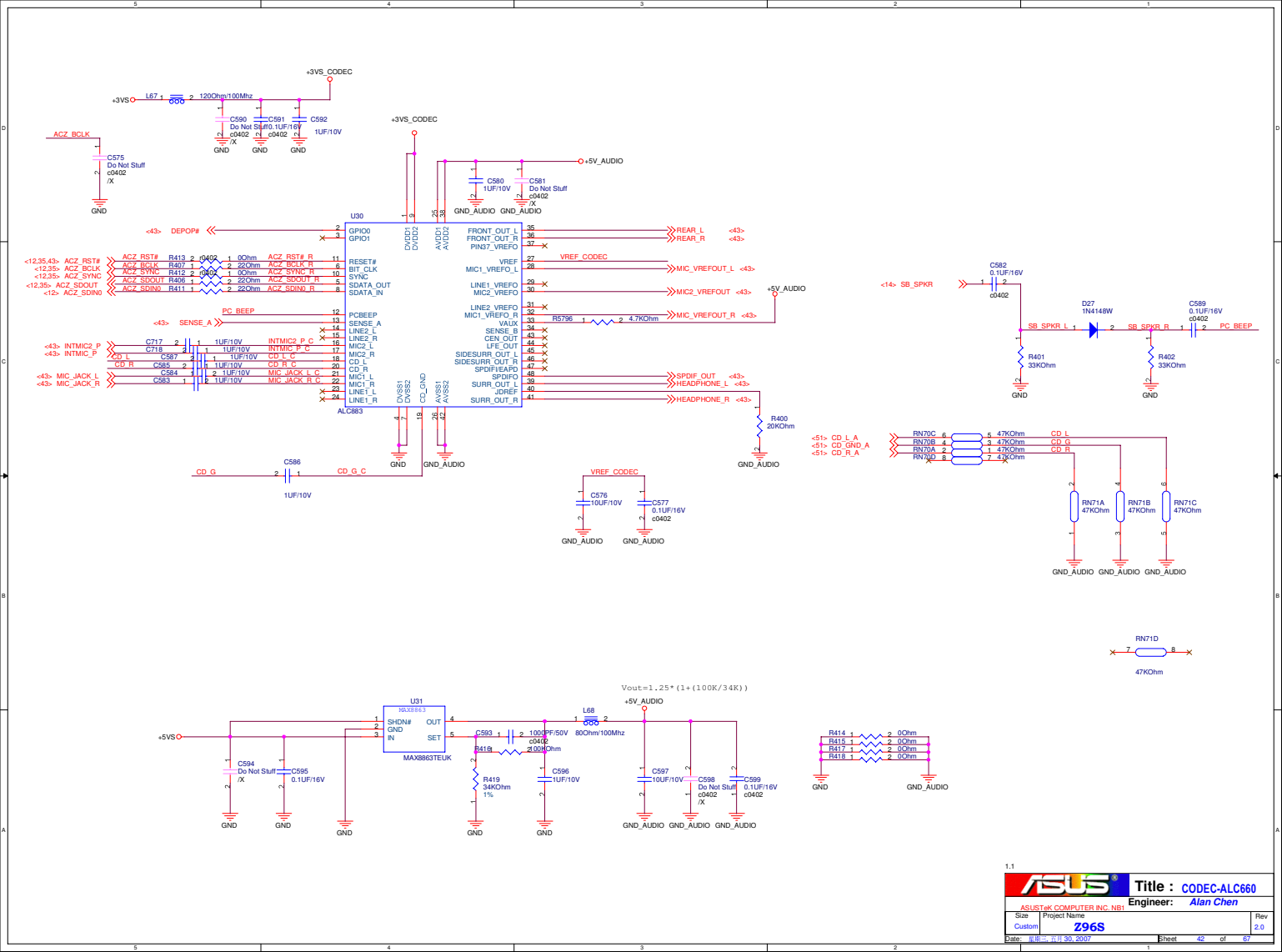
PORT BAR III



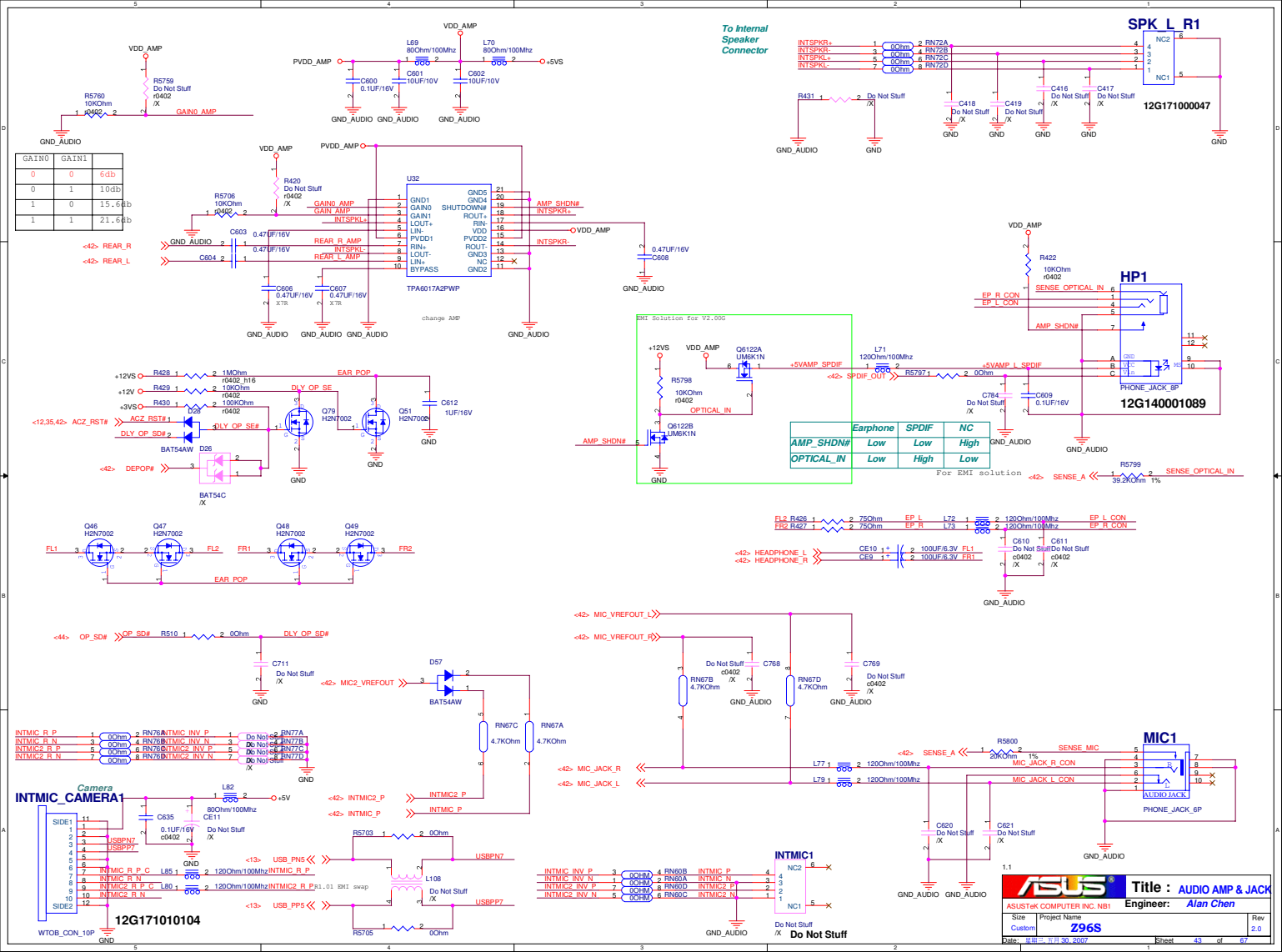


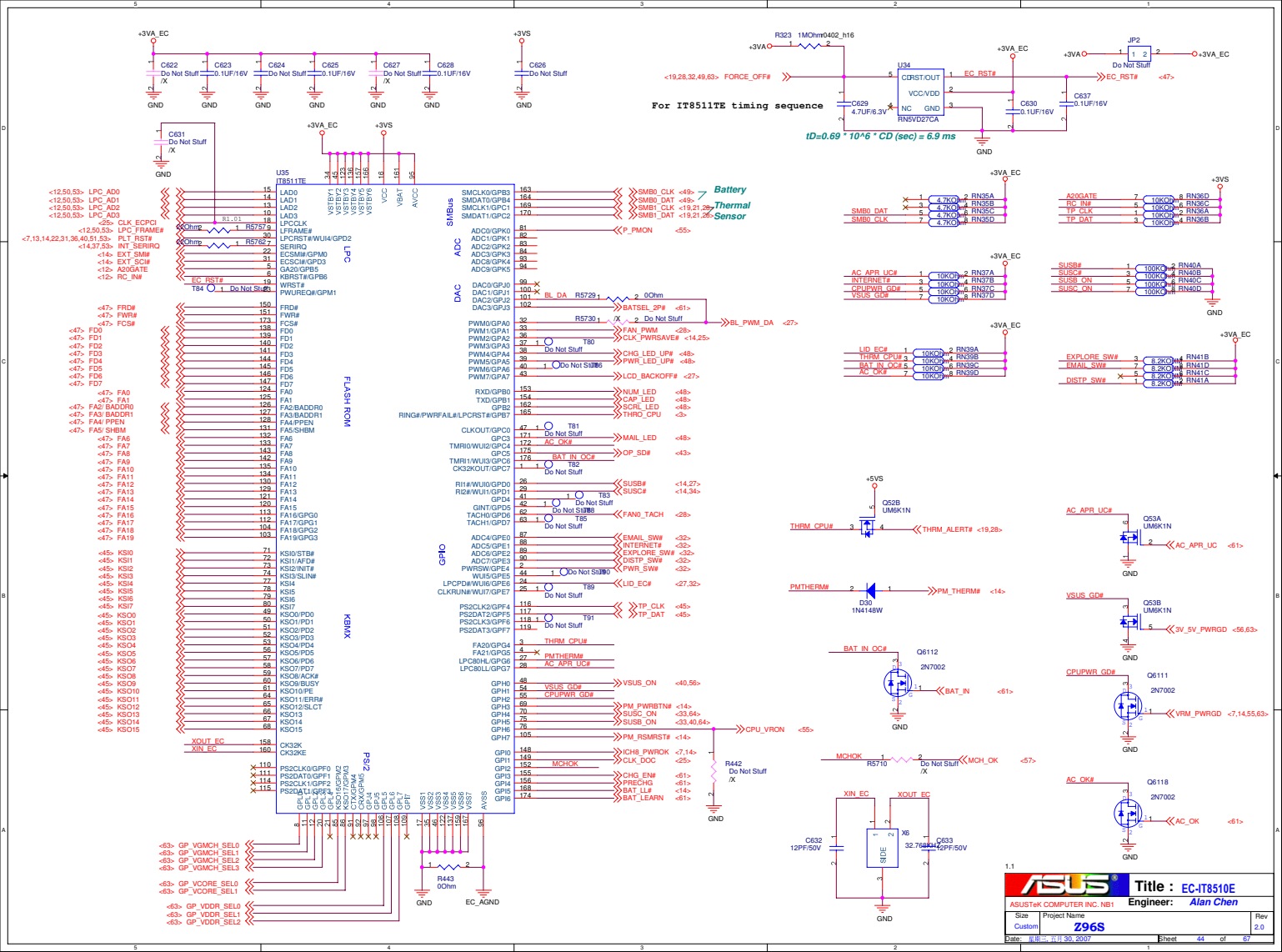
1.1

ASUSTeK COMPUTER INC	Title : <Title>	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期一, 五月 30, 2007	Sheet 41 of 67	

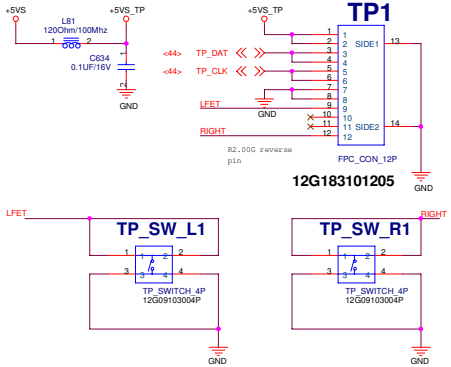


1.1	Title : CODEC-ALC660		
	ASUSTeK COMPUTER INC. NB1	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期三, 五月 30, 2007		Sheet 42 of 67	

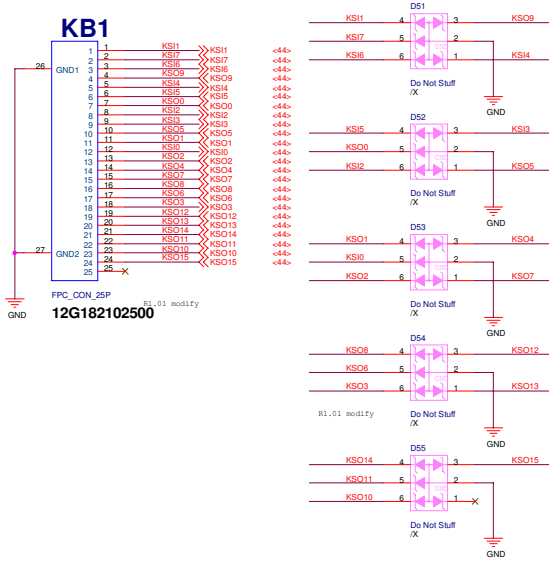

To Internal Speaker Connector
SPK_L_R1
12G171000047
HP1
12G140001089
PHONE_JACK_8P
MIC1
PHONE_JACK_6P
AUDIO JACK
INTMIC_CAMERA1
WTOB_CON_10P
12G171010104
INTMIC1
Do Not Stuff
Do Not Stuff
GAIN0 GAIN1
0 0 6db
0 1 10db
1 0 15.6db
1 1 21.6db
TPA6017A2PWP
change AMP
EMI Solution for V2.00G
Earphone SPDIF NC
AMP_SHDN# Low Low High
OPTICAL_IN Low High Low
For EMI solution
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chen
Title : AUDIO AMP & JACK
Size Custom
Project Name Z96S
Rev 2.0
Date: 星期二, 五月 30, 2007
Sheet 43 of 67


For IT8511TE timing sequence
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Battery
Thermal
Sensor
U35
IT8511TE
U34
RN5VD27CA
JP2
Do Not Stuff
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
LPC
GPIO
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer: Alan Chen
Project Name
Z96S
Size
Custom
Rev
2.0
Date: 星期三, 五月 30, 2007
Sheet 44 of 67

For Touch-Pad

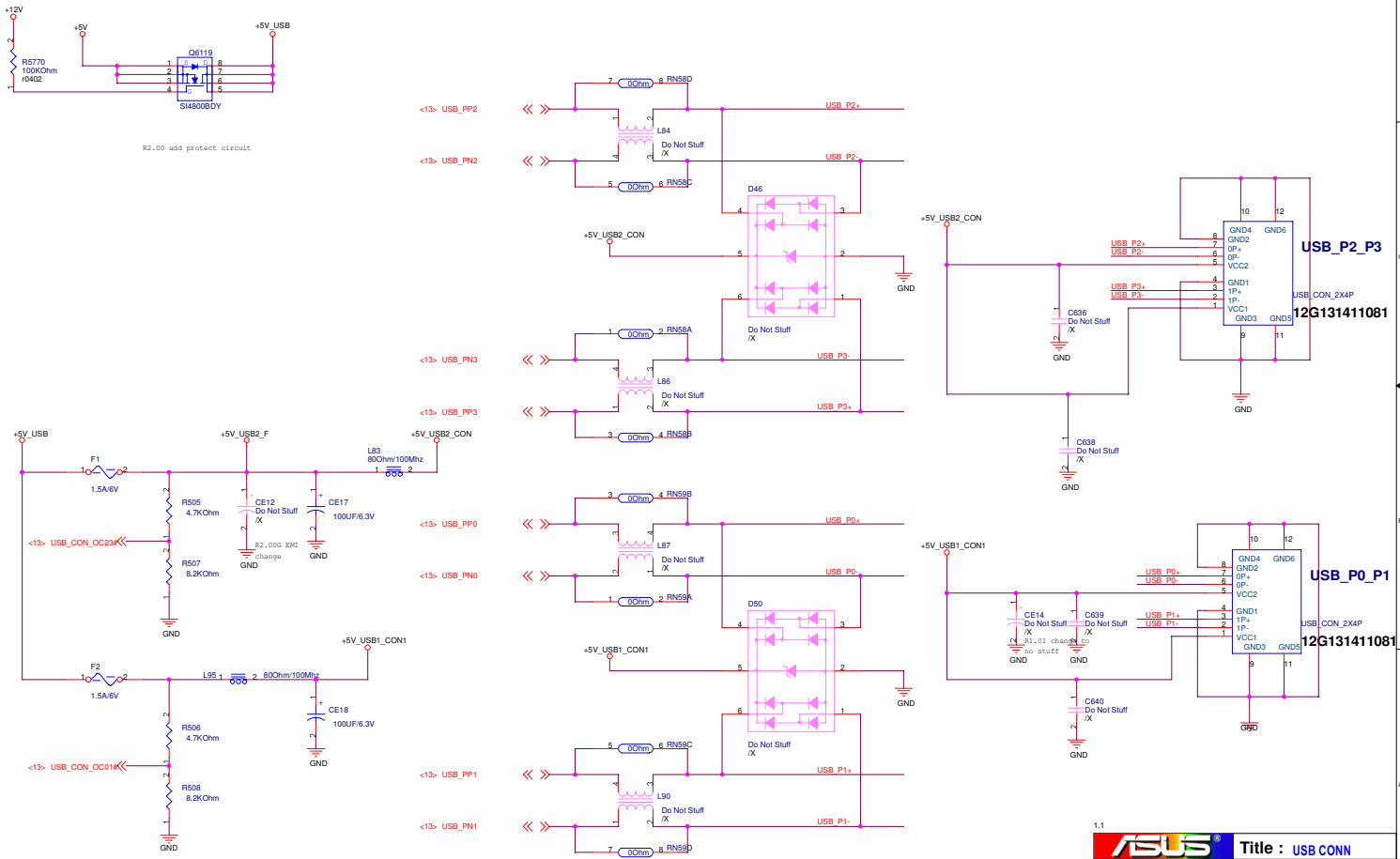


For Keyboard



1.1

ASUSTeK COMPUTER INC. MB6	Title : Touch Pad & KB		
	Engineer: Alan Chen		
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 45 of 67		



1.1

ASUSTeK COMPUTER INC

Title : USB CONN

Engineer: Alan Chen

Size	Project Name	Rev
Custom	Z96S	2.0

Date: 星期三, 五月 30, 2007 Sheet 46 of 67

ISA ROM

EC Hardware Strapping

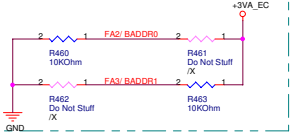
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved



FA4/ PPEN

0: Normal

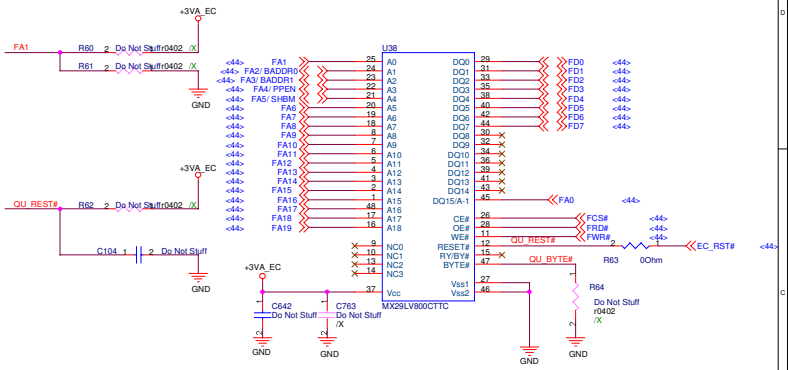
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS

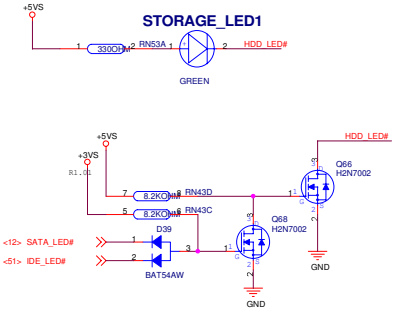
Note: Sampled at VSTBY Power Up Reset



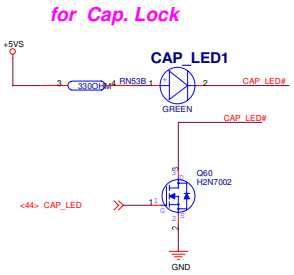
BIOS:05G001204043

For LED

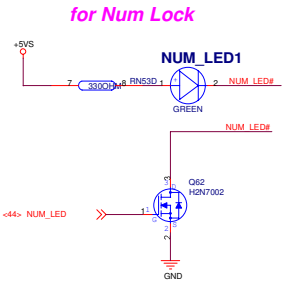
For SATA/IDE LED



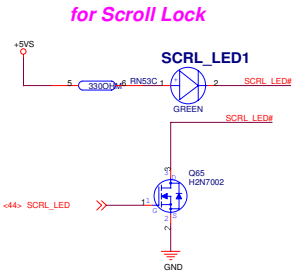
for Cap. Lock



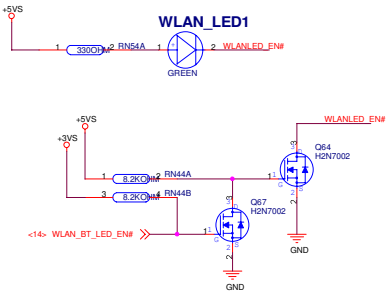
for Num Lock



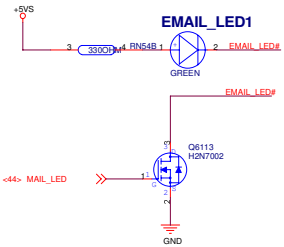
for Scroll Lock



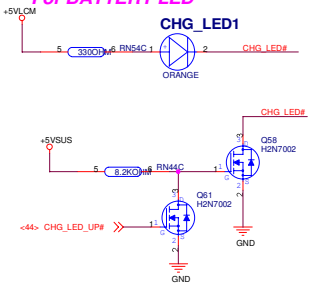
For WireLess LED



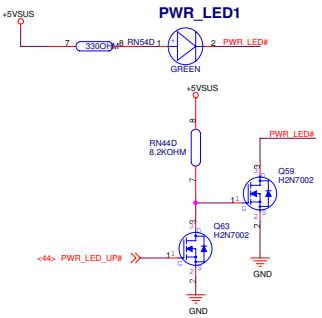
for email



For BATTERY LED



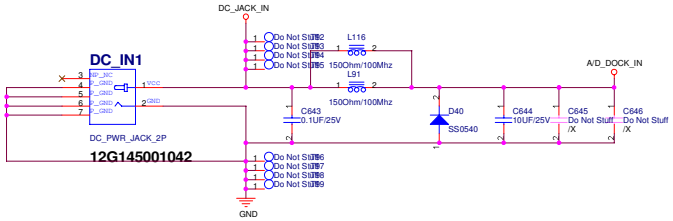
For POWER LED



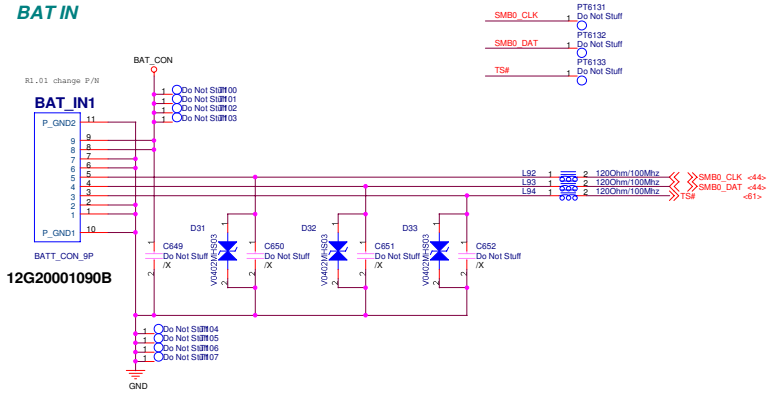
1.1

ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 48 of 67	

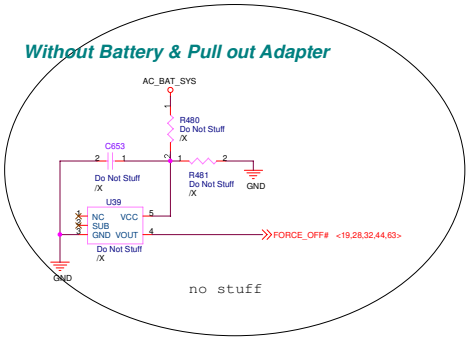
DC IN



BAT IN



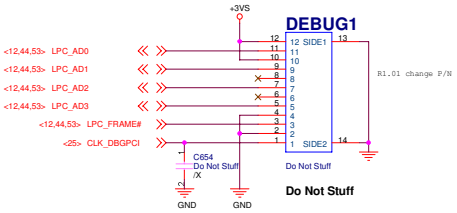
Without Battery & Pull out Adapter



1.1

ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 49 of 67	

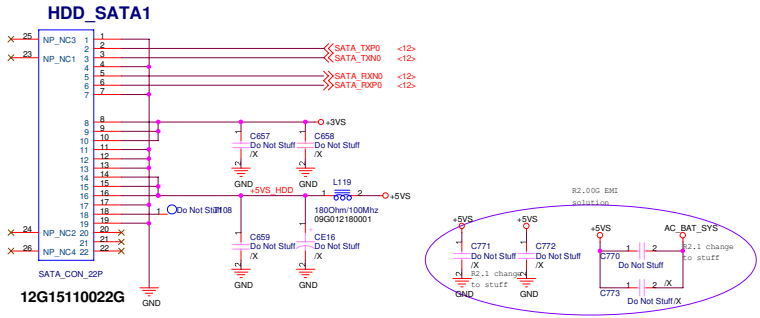
For Debug



pin swap;by F3J

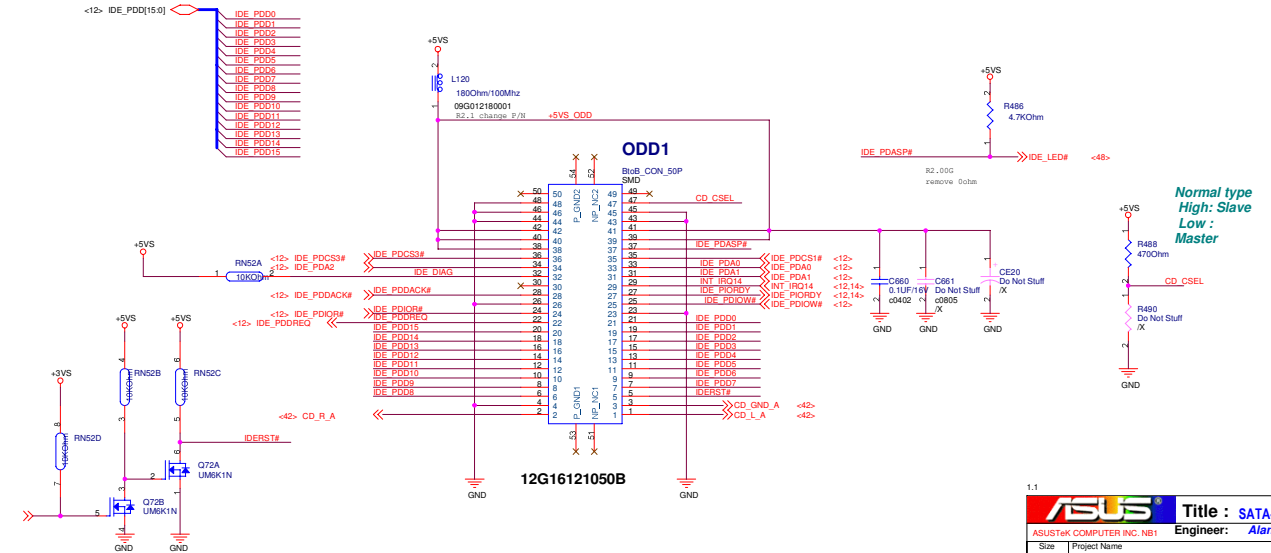
1.1

ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期二, 六月 30, 2007	Sheet 50 of 67	

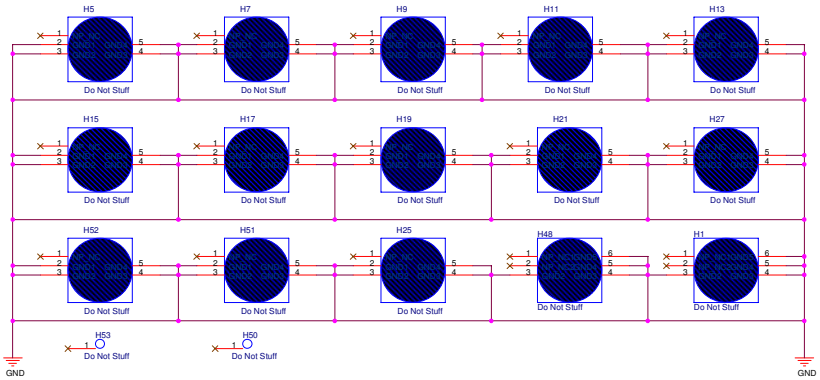


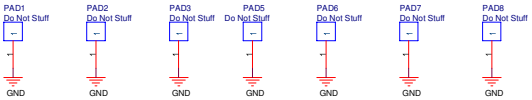
SATA HDD

ODD

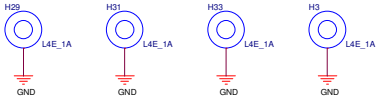


1.1	Title : SATA-HDD & ODD		
ASUSTeK COMPUTER INC. NB1	Engineer: Alan Chen		
Size: Custom	Project Name: Z96S		Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 51 of 67		

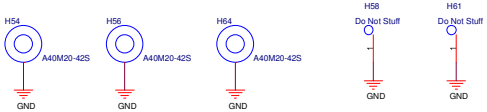




FOR SCREW HOLE



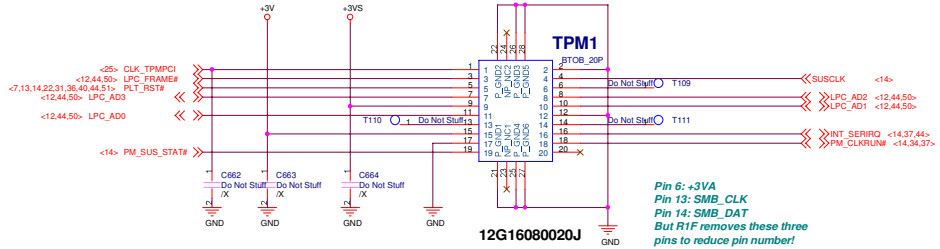
FOR SCREW HOLE



1.1

ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 52 of 67	

For TPM Module

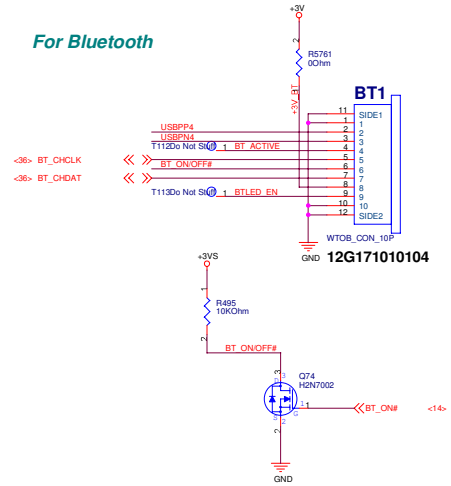


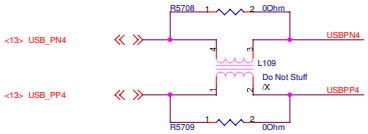
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

1.1

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 53 of 67	

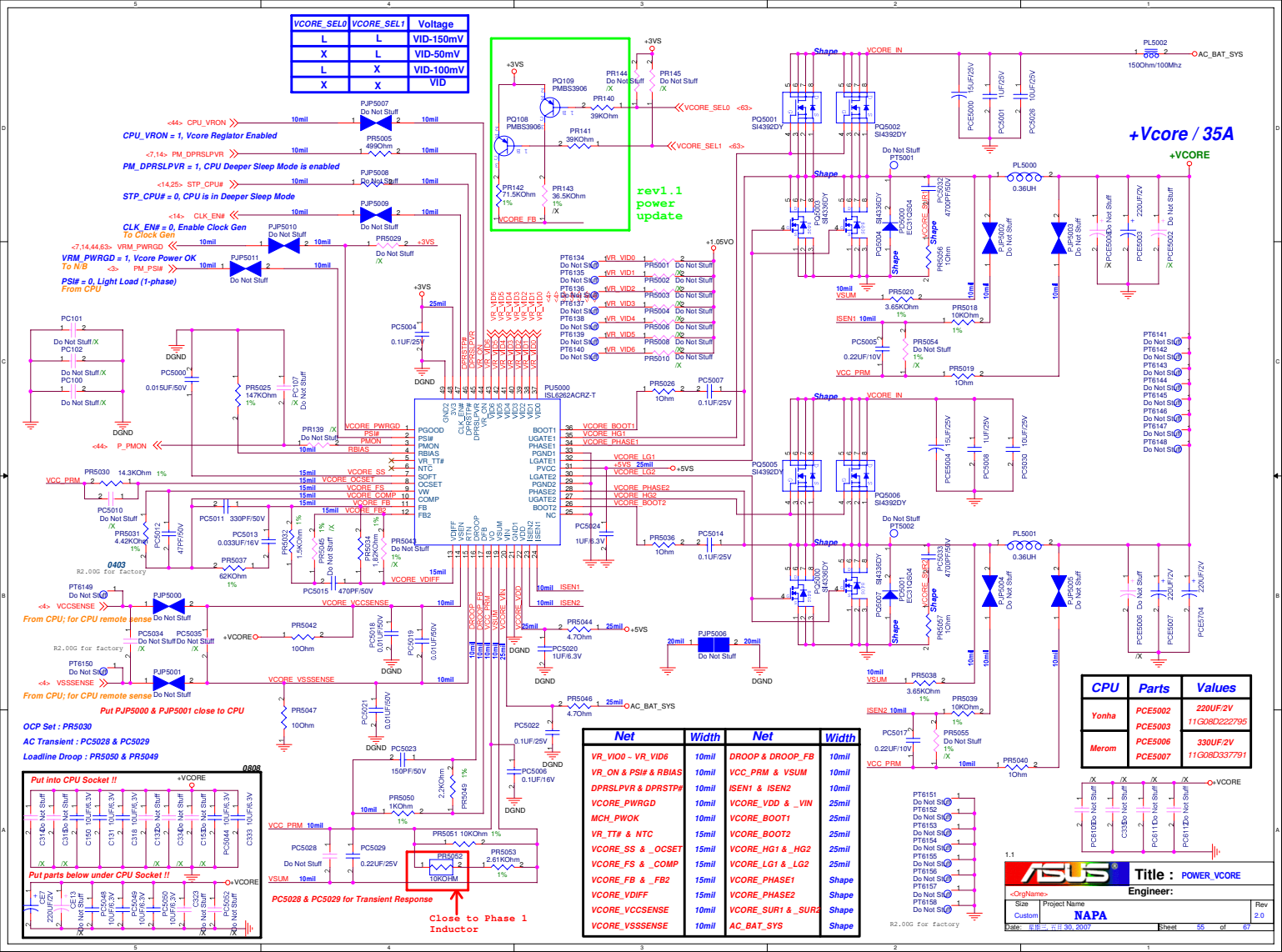
For Bluetooth

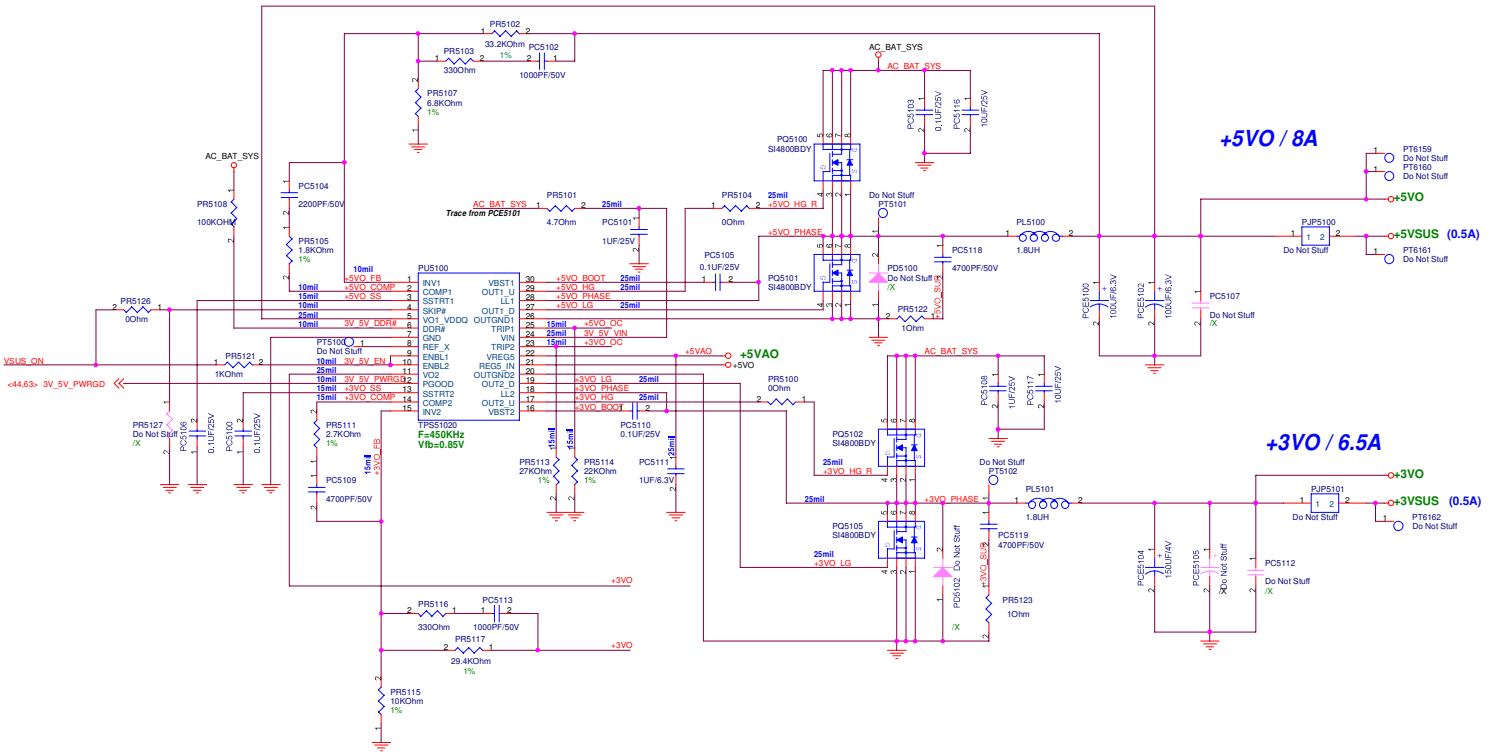




1.1

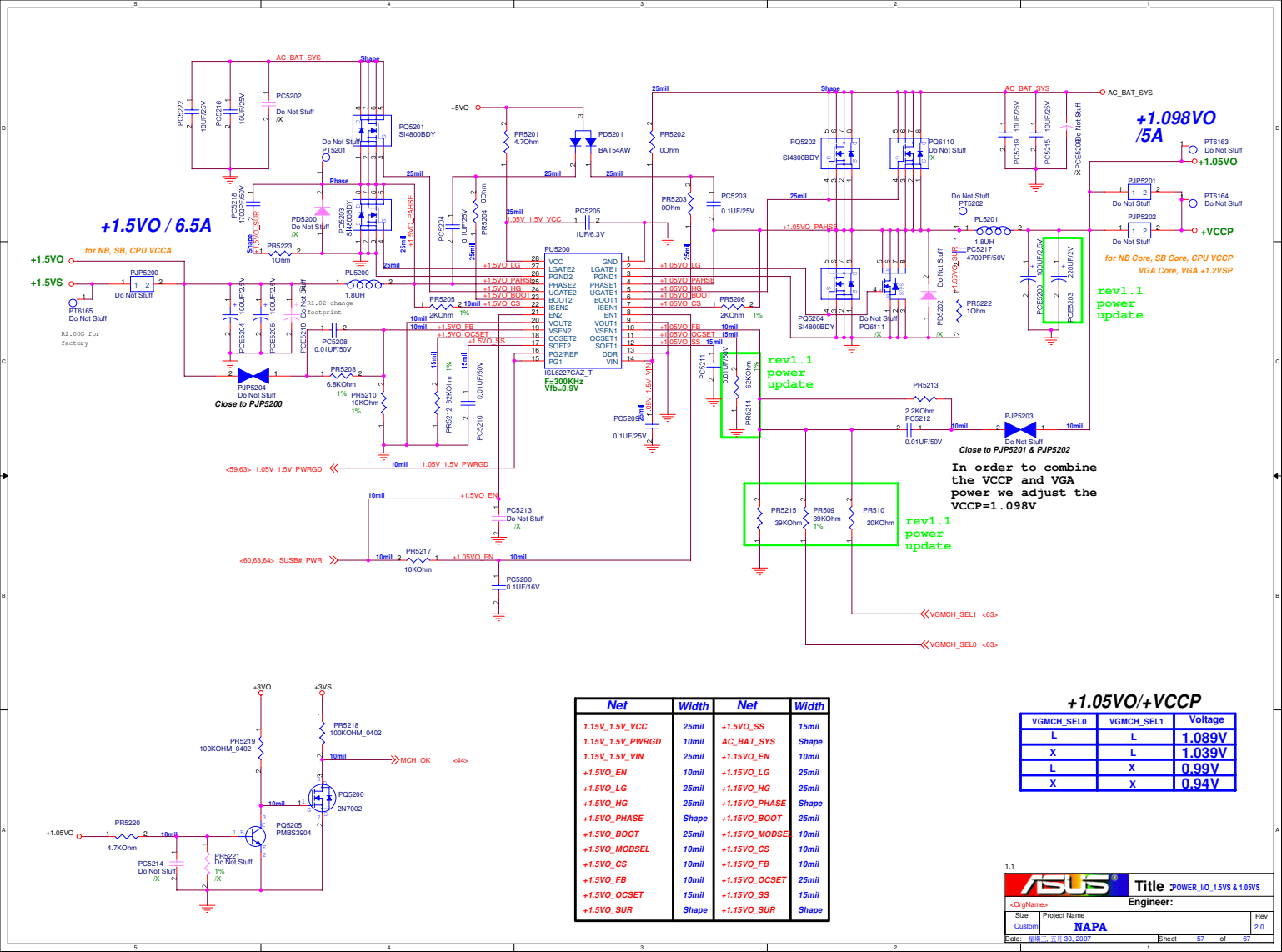
ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Alan Chen	
Size: Custom	Project Name: Z96S	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 54 of 67	


VCORE_SEL0 VCORE_SEL1 Voltage
L L VID-150mV
X L VID-50mV
L X VID-100mV
X X VID
rev1.1 power update
+Vcore / 35A
+VCORE
CPU_VRON = 1, Vcore Reglator Enabled
PM_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled
STP_CPU# = 0, CPU is in Deeper Sleep Mode
CLK_EN# = 0, Enable Clock Gen
To Clock Gen
VRM_PWRGD = 1, Vcore Power OK
To NB
PSI# = 0, Light Load (1-phase)
From CPU
From CPU; for CPU remote sense
Put PJP5000 & PJP5001 close to CPU
OCP Set : PR5030
AC Transient : PC5028 & PC5029
Loadline Droop : PR5050 & PR5049
Put into CPU Socket !!
Put parts below under CPU Socket !!
PC5028 & PC5029 for Transient Response
Close to Phase 1 Inductor
CPU Parts Values
Yonha PCE5002 220UF/2V
PCE5003 11G08D222795
Merom PCE5006 330UF/2V
PCE5007 11G08D337791
Net Width Net Width
VR_VID0 ~ VR_VID6 10mil DROOP & DROOP_FB 10mil
VR_ON & PSI# & RBIAS 10mil VCC_PRM & VSUM 10mil
DPRSLPVR & DPRSTP# 10mil ISEN1 & ISEN2 10mil
VCORE_PWRGD 10mil VCORE_VDD & _VIN 25mil
MCH_PWOK 10mil VCORE_BOOT1 25mil
VR_TT# & NTC 15mil VCORE_BOOT2 25mil
VCORE_SS & _OCSET 15mil VCORE_HG1 & _HG2 25mil
VCORE_FS & _COMP 15mil VCORE_LG1 & _LG2 25mil
VCORE_FB & _FB2 15mil VCORE_PHASE1 Shape
VCORE_VDIFF 15mil VCORE_PHASE2 Shape
VCORE_VCCSENSE 10mil VCORE_SUR1 & _SUR2 Shape
VCORE_VSSSENSE 10mil AC_BAT_SYS Shape
Title : POWER_VCORE
Engineer:
NAPA
Date: 星期二, 五月 30, 2007
Sheet 55 of 67



Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil

1.1			
<OrgName>		Title : POWER_SYSTEM	
		Engineer:	
Size: Custom	Project Name: NAPA		Rev: 2.0
Date: 星期三, 五月 30, 2007		Sheet 56 of 67	



Net	Width	Net	Width
1.15V_1.5V_VCC	25mil	+1.5VO_SS	15mil
1.15V_1.5V_PWRGD	10mil	AC_BAT_SYS	Shape
1.15V_1.5V_VIN	25mil	+1.15VO_EN	10mil
+1.5VO_EN	10mil	+1.15VO_LG	25mil
+1.5VO_LG	25mil	+1.15VO_HG	25mil
+1.5VO_HG	25mil	+1.15VO_PHASE	Shape
+1.5VO_PHASE	Shape	+1.15VO_BOOT	25mil
+1.5VO_BOOT	25mil	+1.15VO_MODSEL	10mil
+1.5VO_MODSEL	10mil	+1.15VO_CS	10mil
+1.5VO_CS	10mil	+1.15VO_FB	10mil
+1.5VO_FB	10mil	+1.15VO_OCSET	25mil
+1.5VO_OCSET	15mil	+1.15VO_SS	15mil
+1.5VO_SUR	Shape	+1.15VO_SUR	Shape

+1.05VO/+VCCP

VGMCH_SEL0	VGMCH_SEL1	Voltage
L	L	1.089V
X	L	1.039V
L	X	0.99V
X	X	0.94V

1.1

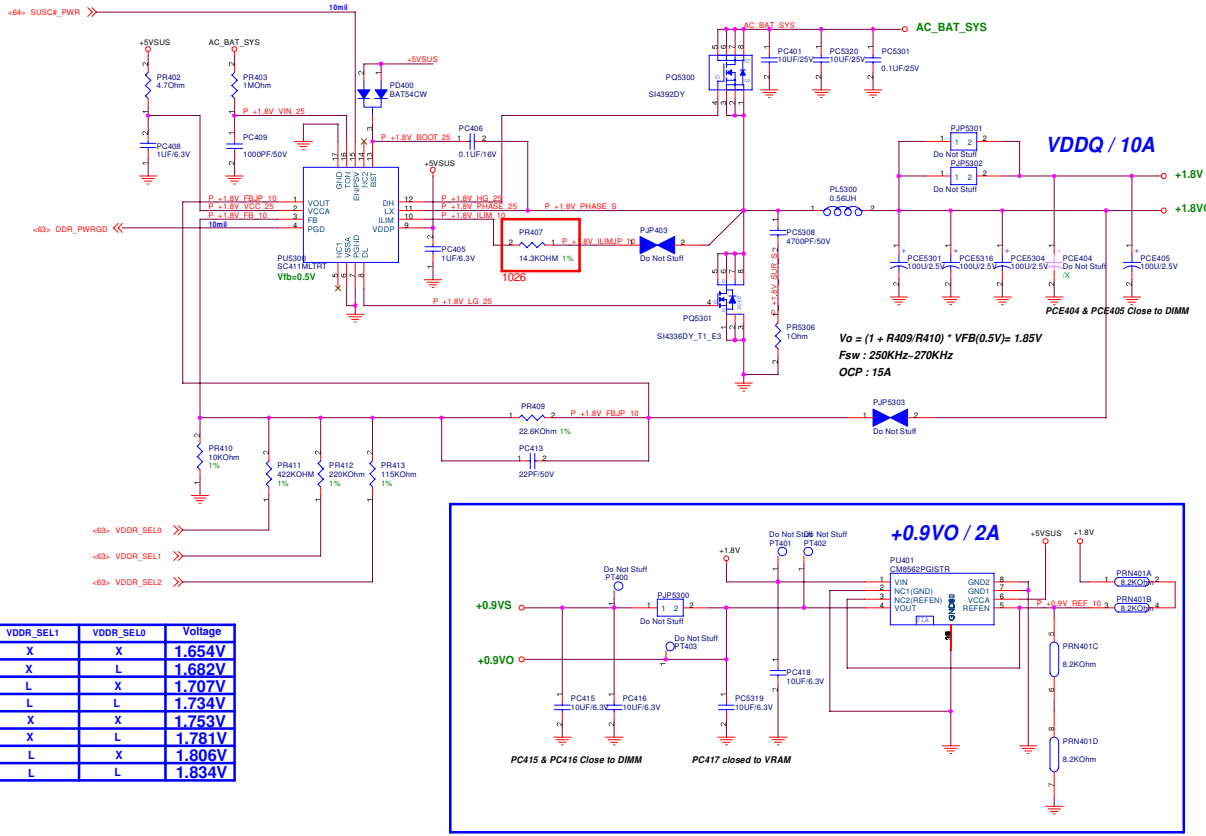
Title: POWER_I/O_1.5VS & 1.05VS

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: 星期三, 五月 30, 2007 Sheet 57 of 67



+VDDQ

VDDR_SEL2	VDDR_SEL1	VDDR_SEL0	Voltage
X	X	X	1.654V
X	X	L	1.682V
X	L	X	1.707V
X	L	L	1.734V
L	X	X	1.753V
L	X	L	1.781V
L	L	X	1.806V
L	L	L	1.834V

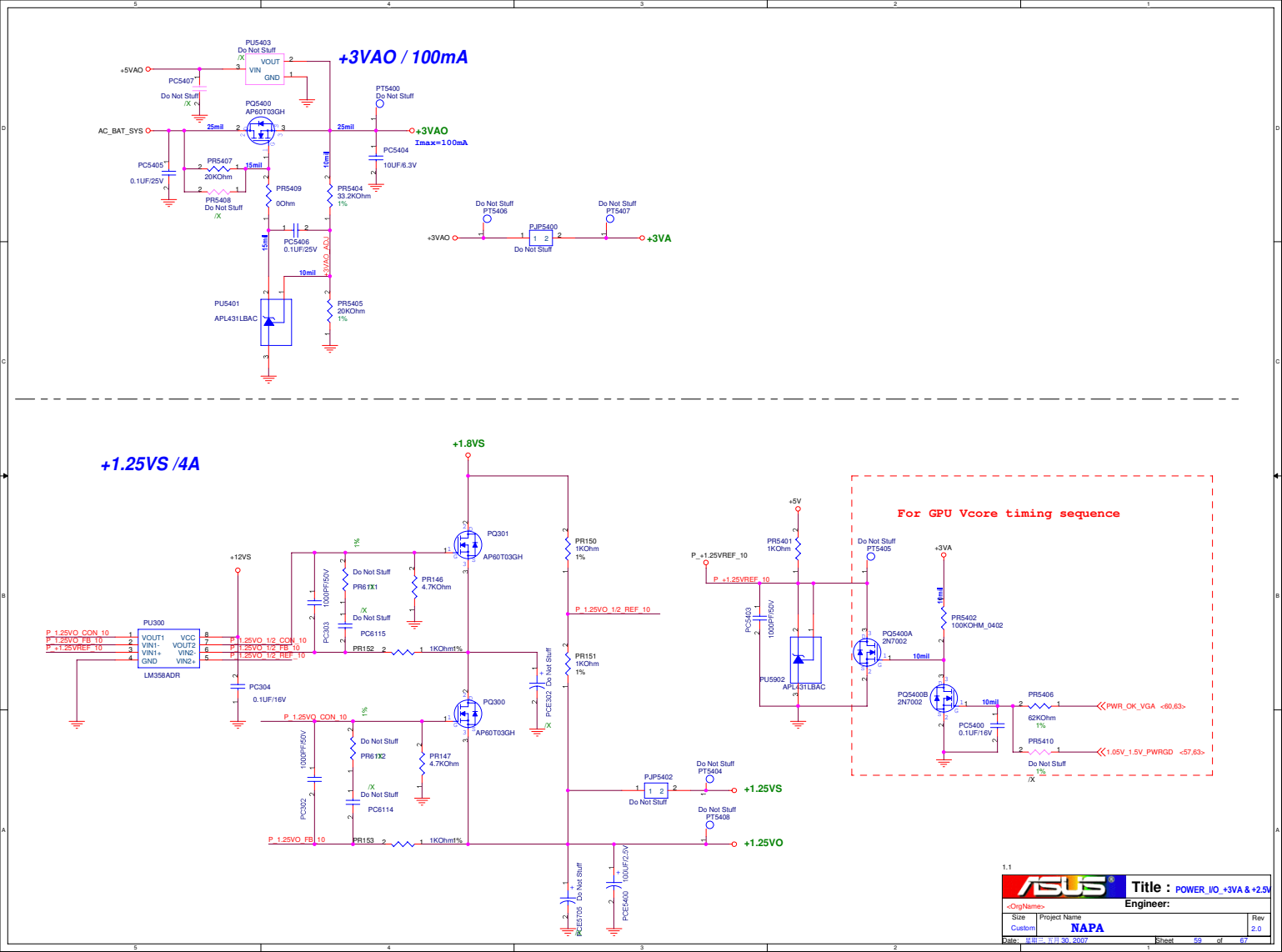
1.1

Title : POWER_I/O_DDR & VTT

<OrgName> Engineer:

Size: Custom | Project Name: NAPA | Rev: 2.0

Date: 星期三, 六月 30, 2007 | Sheet 58 of 67



1.1

ASUS

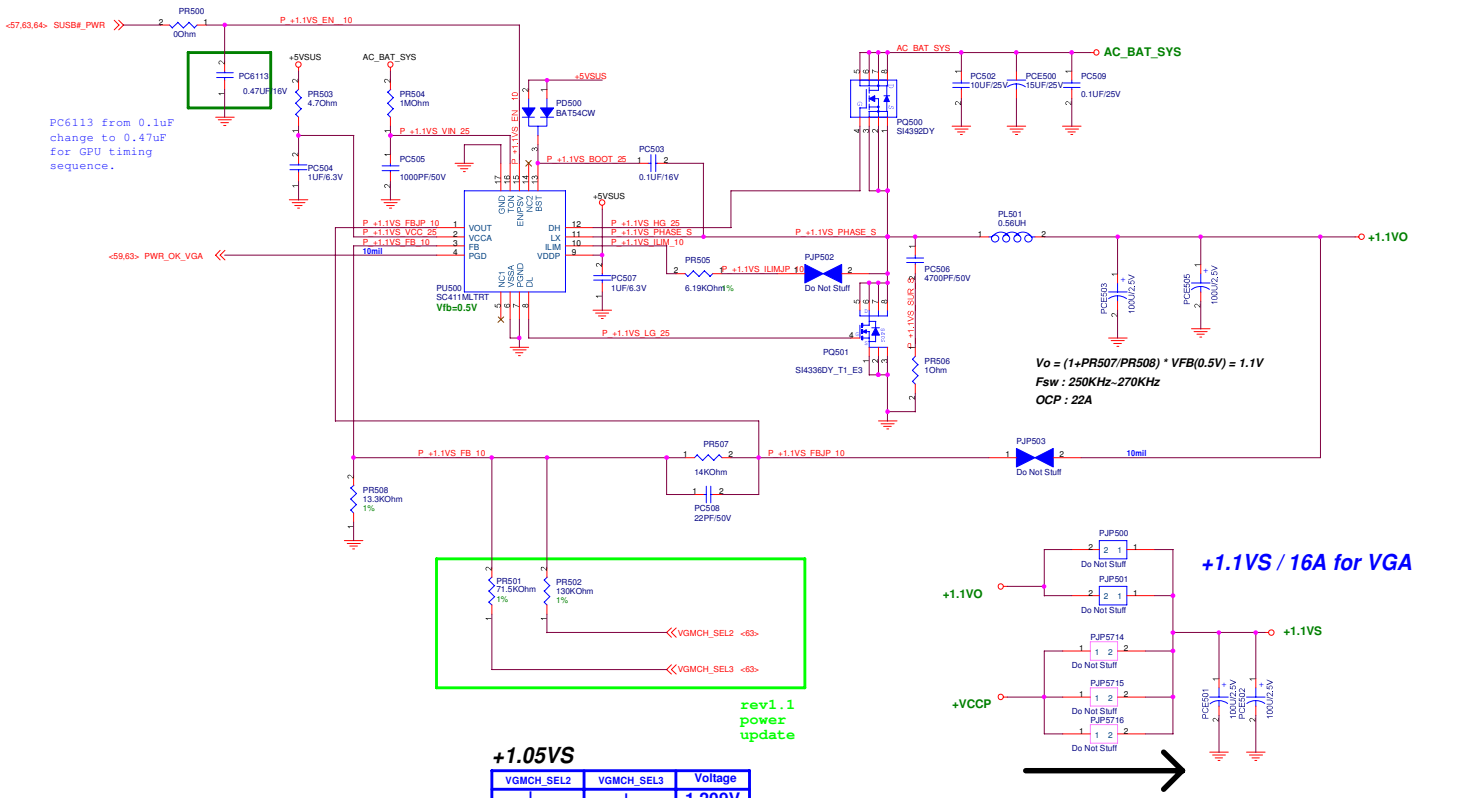
Title : POWER_I/O +3VA & +2.5V

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: 星期二, 八月 30, 2007 Sheet 59 of 67



+1.05VS

VGMCH_SEL2	VGMCH_SEL3	Voltage
L	L	1.209V
X	L	1.154V
L	X	1.109V
X	X	1.054V

1.1

Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 60 of 67	

POWER PATH & BAT_LEARN

Charger shut down condition :

1. Victl < 0.06V
2. PKPRES# > 55% of MAX8725_LDO
3. AC Adaptor Removed

The timing of PDL & PDS switch :

BAT - A/D_DOCK_IN > 100mV--> Battery mode

The current capacity of MAX8725_LDO is 10mA.

VBAT_DLGV is a voltage for driving MOSFET.

MAX8725_ACIN < 10.27V, AC Adaptor absent

MAX8725_ACIN > 10.27V, AC Adaptor absent

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V<Vmoce<2V)	Battery Learn

MAX8725_REF : 4.2235V

MAX8725_LDO : 5.4V

Battery Charging Voltage :
+V_BAT= 3 x [4.2235+(Vvctl-1.8)/9.52]

Battery Charging Current :
Icharge=(0.075/PR5706) x (Victl/3.6))

Input Adaptor Max. Current Limit :
Ilimit_current=(0.075/PR5701) x (Vcls/4.2235)

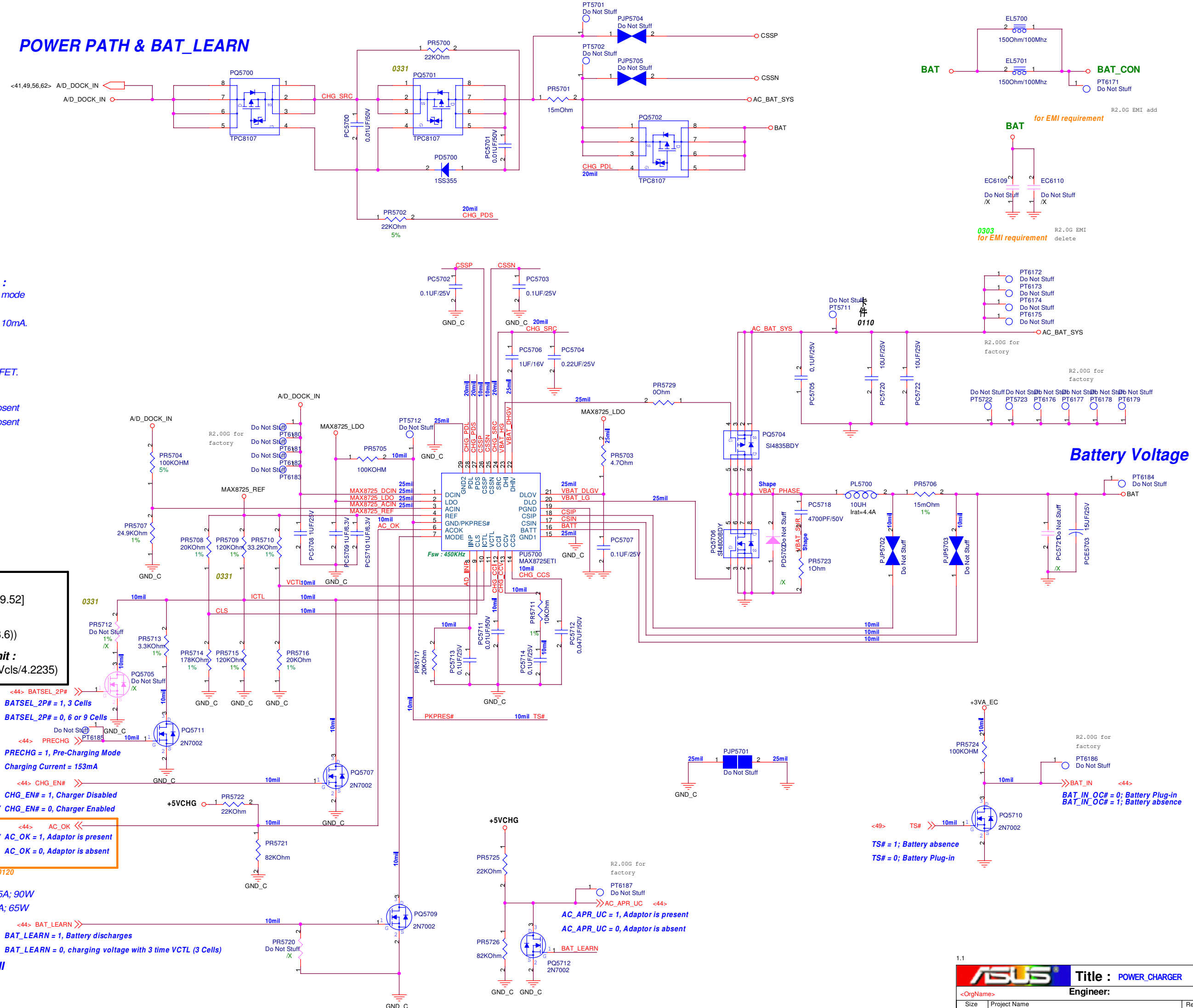
Pre-Charging Mode :
Precharging current = 150 ~ 160mA
Victl = 0.100V ~ 0.120V

Battery Cell Selection :
BATSEL_2P# = 1, 6 Cells; Victl = 2.084V
=> Icharge = 2.894A
BATSEL_2P# = 0, 9 Cells; Victl = 3.219V
=> Icharge = 4.472A

Adaptor Max. Current :
PR5714 = 178K; Vcls = 3.79V, Ilimit = 4.5A; 90W
PR5714 = 47K; Vcls = 2.96V, Ilimit = 3.5A; 65W

BATSEL_SP# = 1, 3-Cell
Victl = 1.22V / Icharge = 1.69A

BATSEL_SP# = 0, 6-Cell or 9-Cell
Victl = 2.11V / Icharge = 2.93A

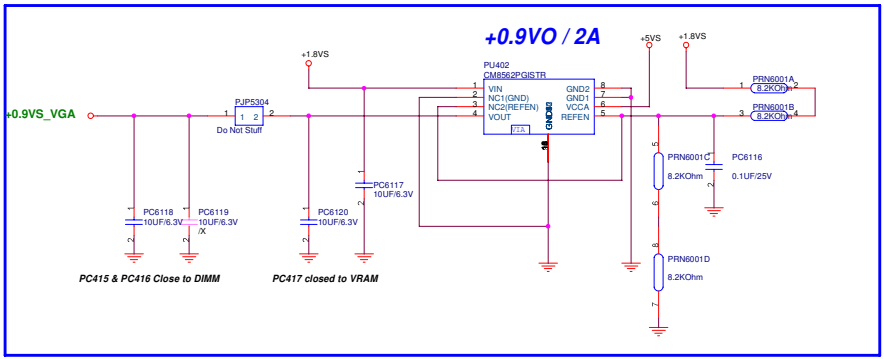


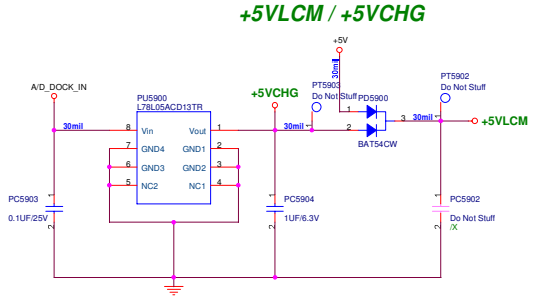
Title : POWER_CHARGER

Engineer:

Size: C | Project Name: NAPA | Rev: 2.0

Date: 星期三, 五月 30, 2007 | Sheet 61 of 67

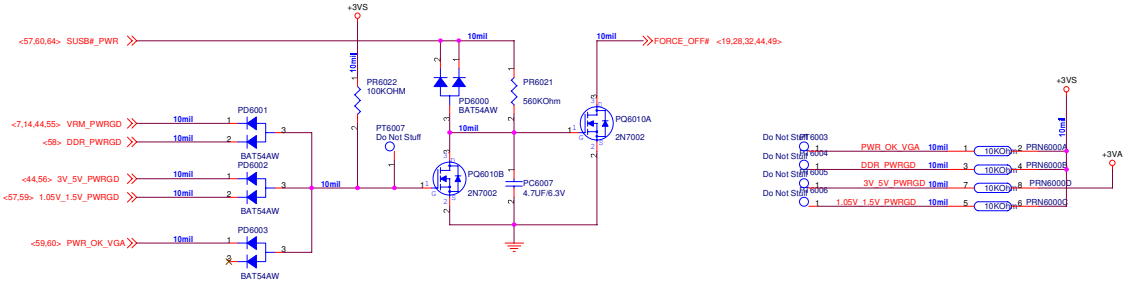




1.1

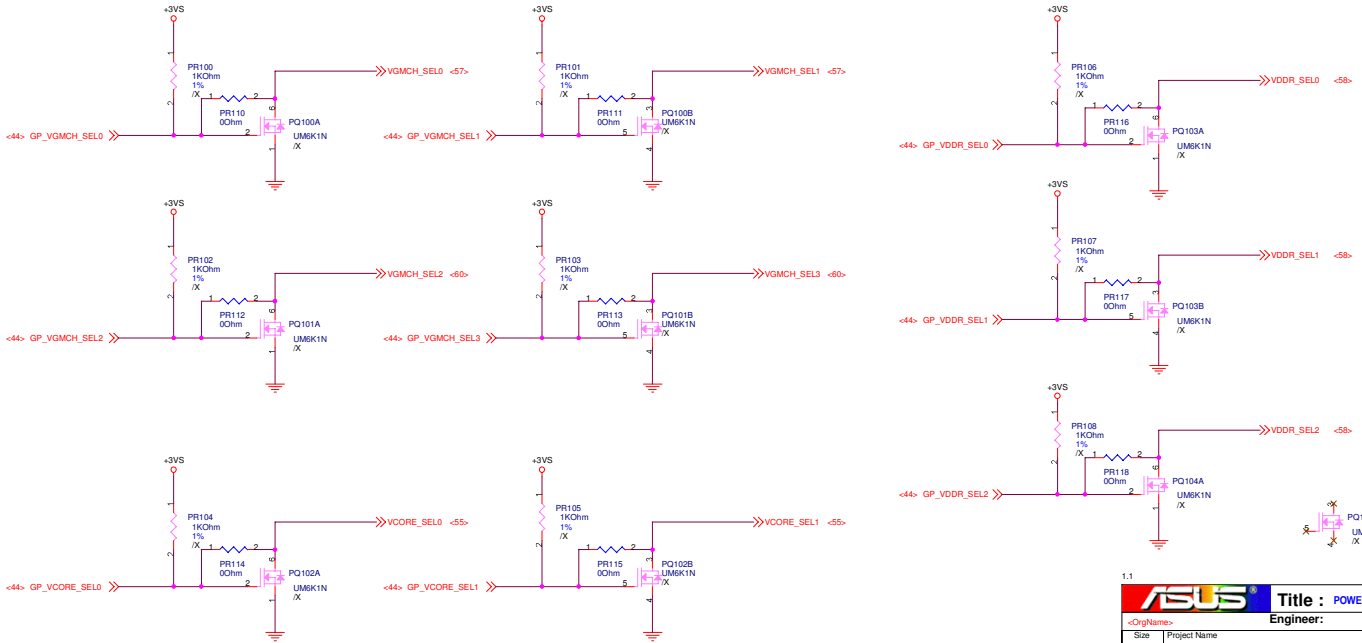
<OrgName>	Title : POWER_DETECT	
	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 62 of 67	

Power Good Detecter



Power Voltage control

Modify V2.0G



1.1

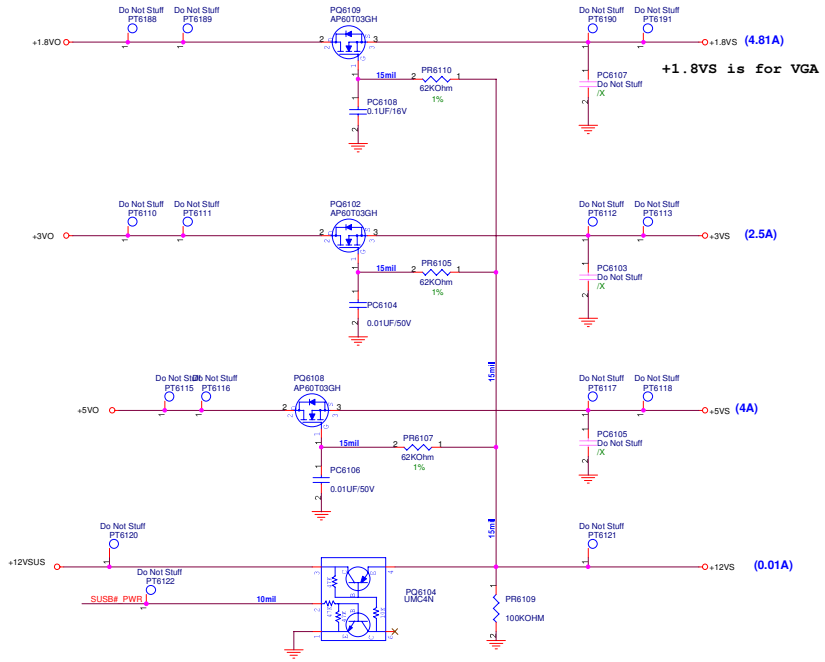
Title : POWER_PROTECT

<OrgName> Engineer:

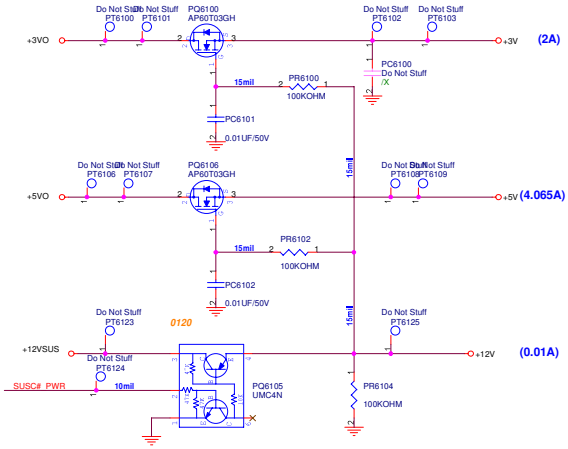
Size: Custom | Project Name: NAPA | Rev: 2.0

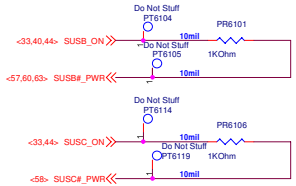
Date: 星期三, 五月 30, 2007 | Sheet 63 of 67

SUSB#_PWR POWER



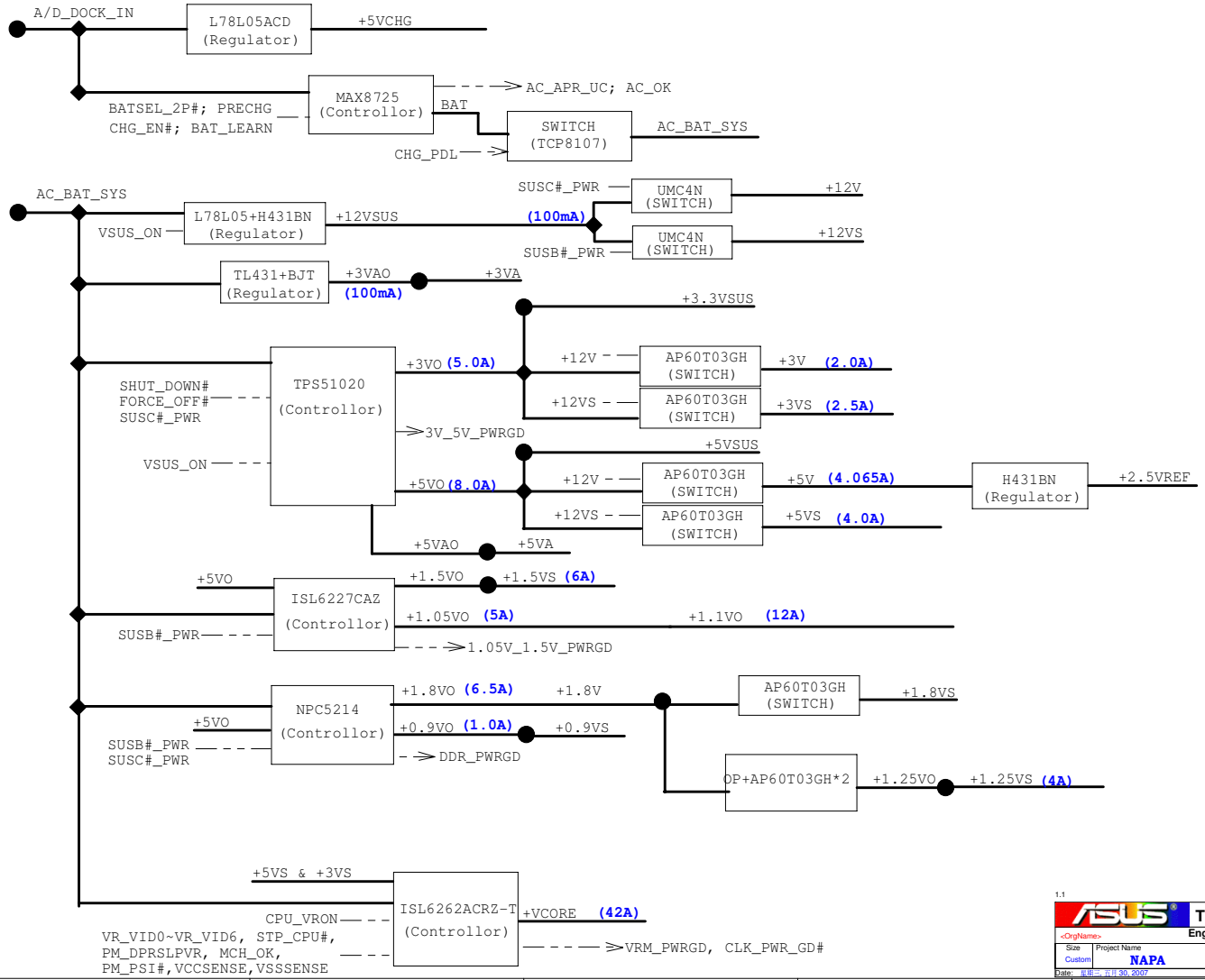
SUSC#_PWR POWER





1.1

Title : POWER_LOAD SWITCH		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 2.0
Date: 星期三, 五月 30, 2007	Sheet 64 of 67	



1.1

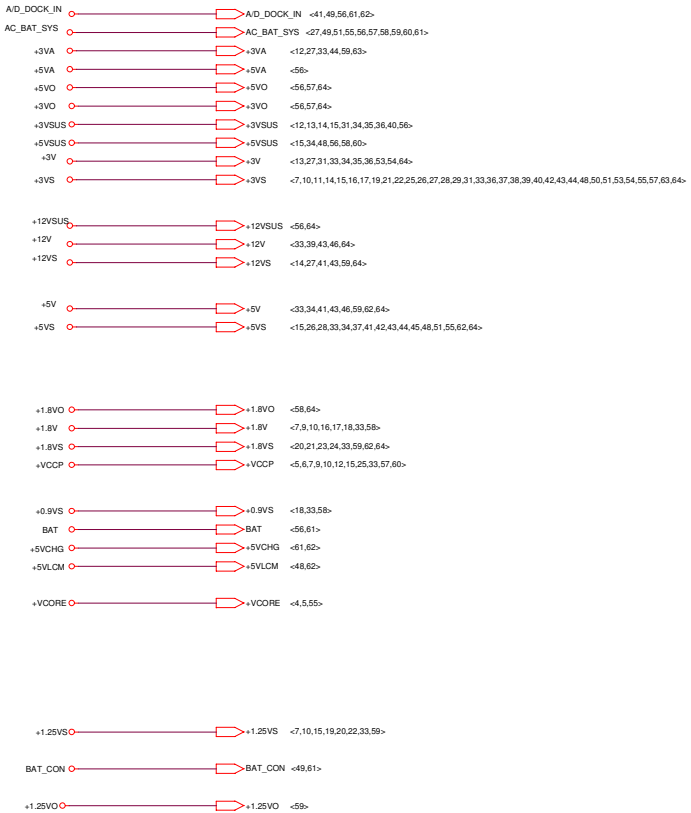
Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: 星期三, 五月 30, 2007 Sheet 65 of 67



1.1

Title : POWER_SIGNAL

<OrgName>

Engineer: Alan Chen

Size	Project Name	Rev
Custom	NAPA	2.0

Date: 星期三, 五月 30, 2007 Sheet 66 of 67

Rev	Date	Description
1.0	10/27/06	Placement: I/O is the same as Z96JP V2.1,and modify I/O location name.
1.0	10/27/06	Schematic:Refer the Z98S.
1.0	10/27/06	1.Add Mini-card Robson1 connector for function request<P31>
1.1	01/02/07	1.PC6113 from 0.1uF change to 0.47uF for GPU timing sequence<P60>
1.1	01/02/07	2.GR25,GR28 load 2k ohm for GPU PCI-DEVID setting<P19>
1.1	01/02/07	3.GR14 /N,GR18 load 10k ohm,GR19 /N,GR15 load 10k ohm for VRAM setting <P19>
1.1	01/02/07	4.U5H Pin_R5 from DACA_VREF change to DACB_VREF for TV Vref net name issue<P19>
1.1	01/02/07	5.R147,R149,R186,R188 from 499 ohm change to 120 ohm for VRAM clock termination<P23,24>
1.1	01/02/07	6.R379 load 10k ohm for GPU 27M clock enable setting<P25>
1.1	01/02/07	7.GPU LVDS_Lx & LVDS_Ux exchange for LVDS pindefine issue<P20>
1.1	01/02/07	8.SR48 pull +3VSUS change to pull +3VS for timing issue<P14>
1.1	01/02/07	9.R382 from pull GND change to pull +3VS for PEREQ# setting<P25>
1.1	01/02/07	10.R253 pin1 pull +3VA_EC change to pull +3VS <P28>
1.1	01/02/07	11.MIC1 Connector from 12G14001106M change to 12G14030106E for ME request<P43>
1.1	01/02/07	12.Del R424,Q32 for Earphon & SPDIF issue<P43>
1.1	01/02/07	13.Modify EC pindefine:Pin3(THRM_CPU#),Pin4(N/C),Pin27(PMTHERM#),Pin24(LID_EC#)<P44>
1.1	01/02/07	14.U45(EEPROM),R5734 load for LAN MAC issue<P34>
1.1	01/02/07	15.R378 /N for ITP clock setting==>Disable<P25>
1.1	01/02/07	16.Del G-Sensor component <P30>

Rev	Date	Description