BRIGHTON

CPU : VIA ISAIAH
Chip Set : VIA VX800
Remarks :

Model Name	: BRIGHTON MAIN
PCB Part No	:
Dev. Step	: PV
Revision	: 1.0
T.R. Date	: 2008.11.07

DRAW	CHECK	APPROVAL

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DESIGN: YH.KIM	DATE: 9/4/2008	TITLE: BRIGHTON(VIA) MAIN COVER	SAMSUNG ELECTRONICS
CHECK: GS.CHO	DEV. STEP: ADV1		
APPROVAL: JG.GOO	REV: 0.5		PART NO.: BA41-undefi
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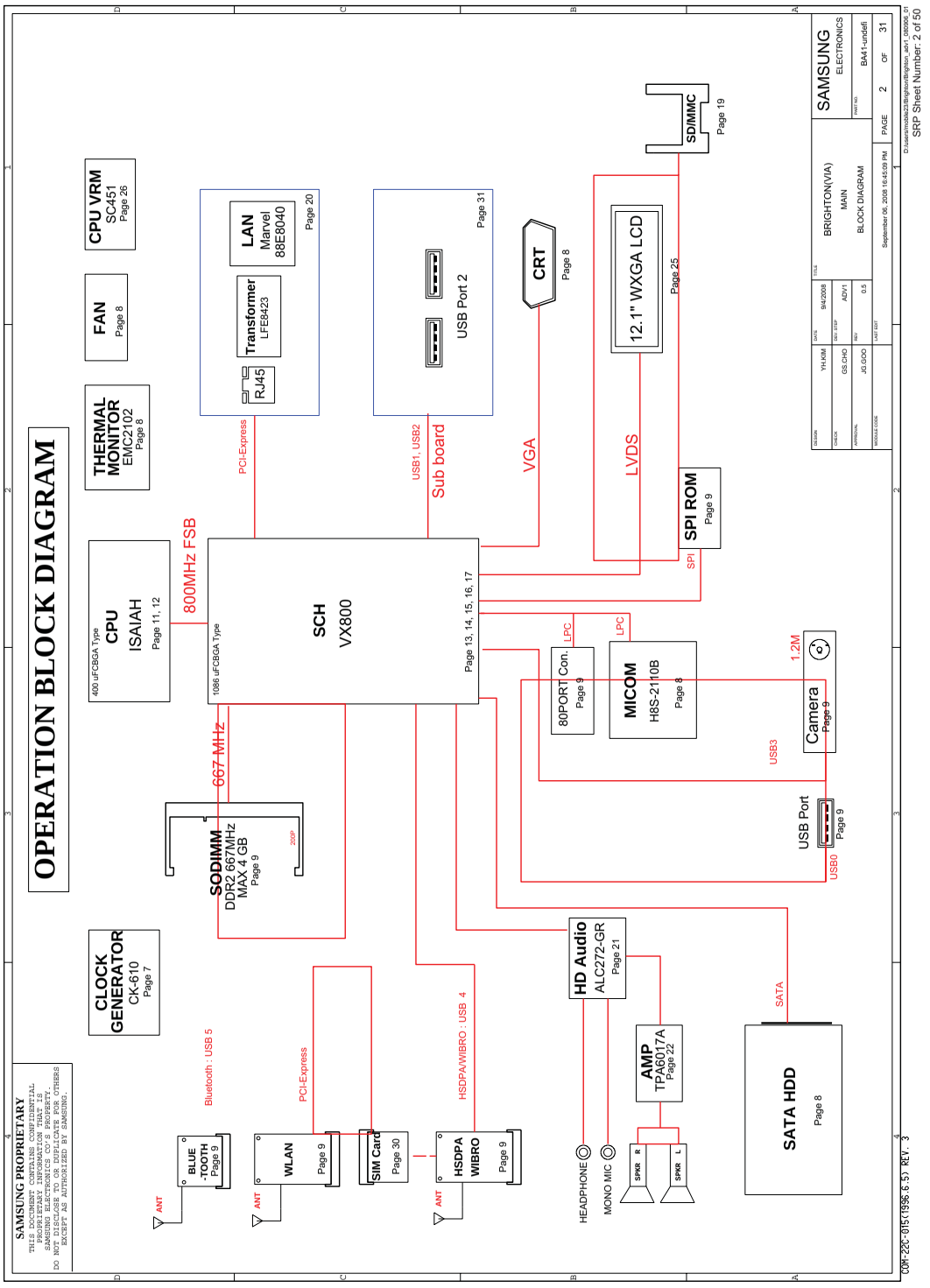
8. Block Diagram and Schematic

8. Block Diagram and Schematic



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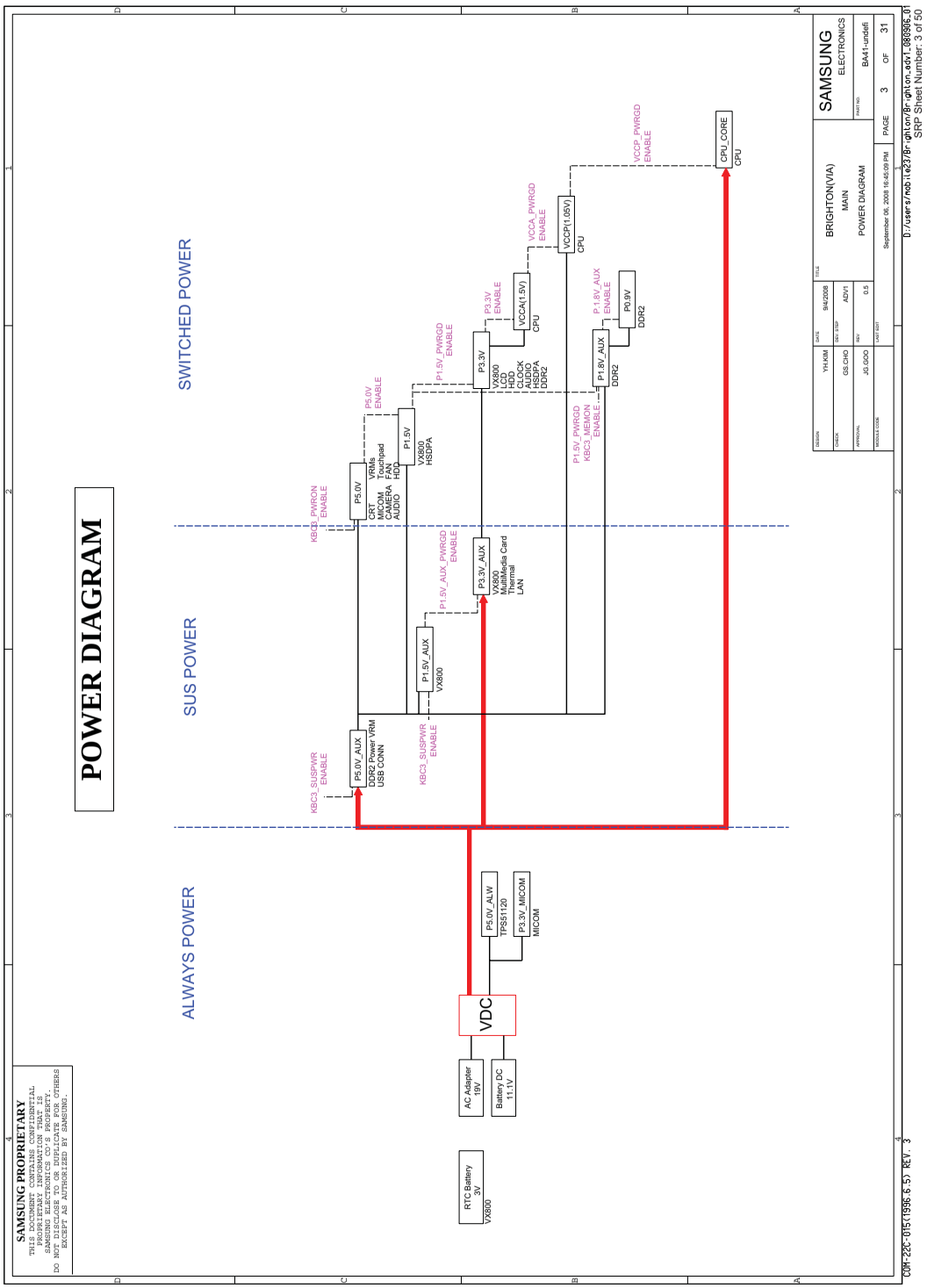

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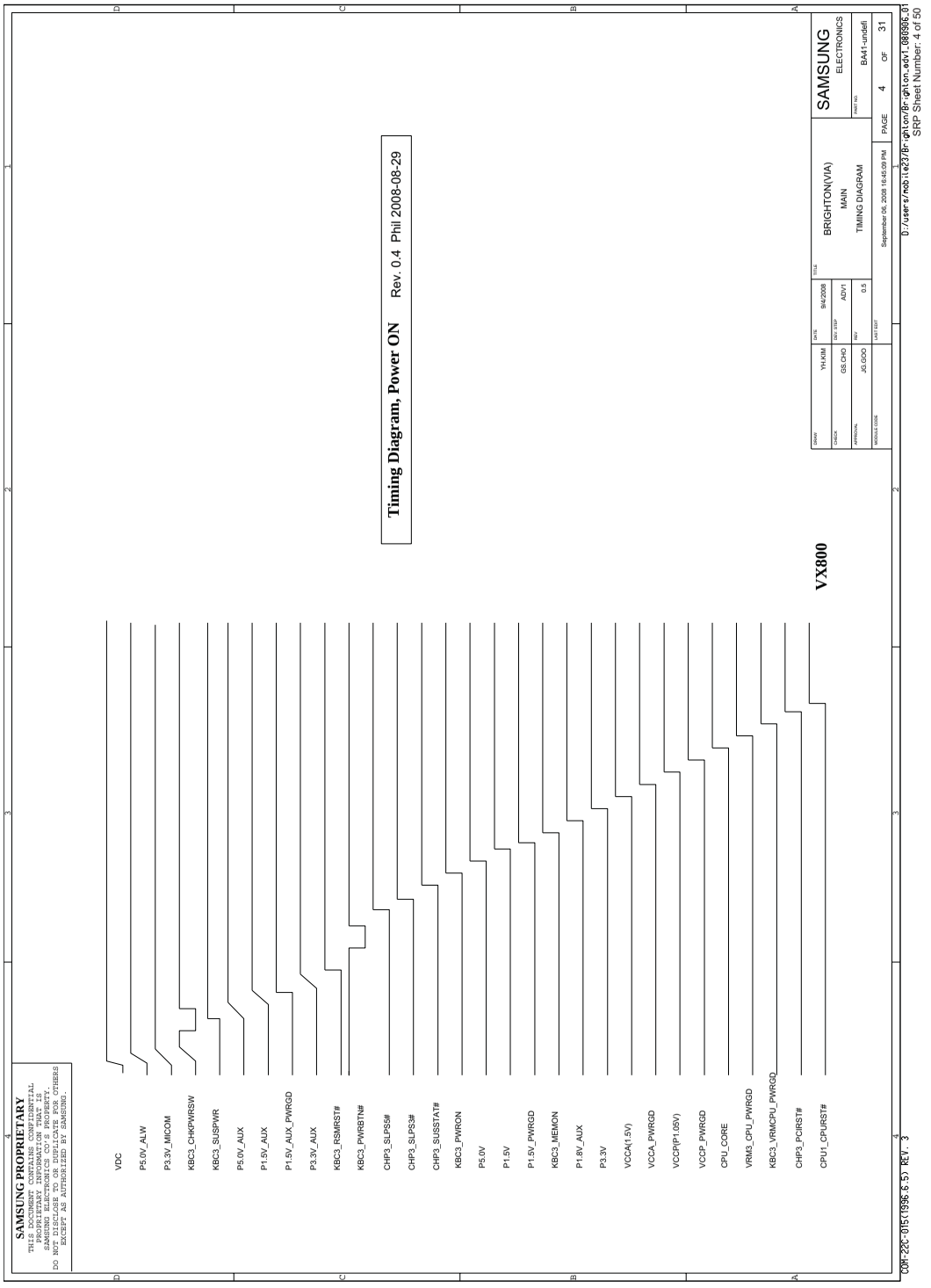

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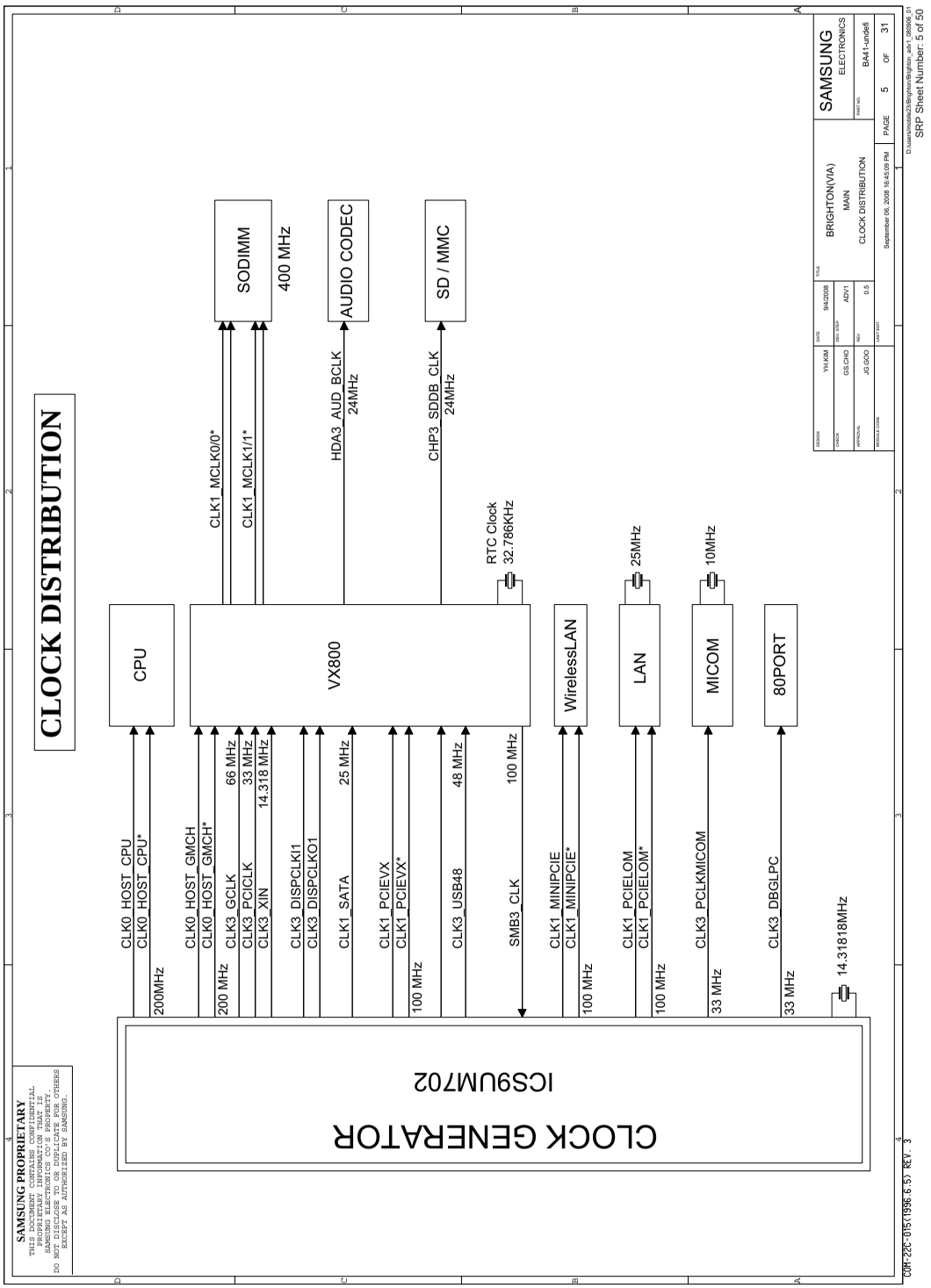

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Wired LAN	AD21	3	G
USB Hub to PCI LPC Bridge/IDE/AC97/SMBUS	AD29(internal) AD30(internal) AD31(internal)	Programable	

I²C / SMB Address

Devices	Address	Hex	Bus
VX800	**Master**	-	**SMBUS Master**
ICS9UM702(Clock Generator) SODIMM0	1101 001x 1010 000X	D2h A0h	Clock, Unused Clock Output Disable -
MICOM	**Master**		
BATTERY THERMAL MORNITOR	0001 011h x111 1010	16h 7Ah	

USB PORT Assign

Port0	Main BD USB Port
Port1	SUB BD USB Port1
Port2	SUB BD USB Port2
Port3	Camera
Port4	HSDPA
Port5	Bluetooth

System Power States

Power Rail	Devices (Page Number)
P5V	FAN(8) MICOM(8) CRT(8) CAMERA(9) AUDIO(20) VRMs(25) TOUCHPAD(9) HDD(8)
P3.3V	VX800(13) LCD(24) HDD(8) CLOCK(7) AUDIO(20) HSDPA(9) DDR2(9)
P1.5V	VX800(13) HSDPA(9)
VCCA(P1.5V)	CPU(11)
VCCP(1.05V)	CPU(11)
P5V_AUX	DDR2 PWR VRM(10) USB(9,30)
P3.3V_AUX	VX800(13) MULTIMEDIA CARD(18) THERMAL(8) LAN(19)
P1.8V_AUX	DDR2(9)
P1.5V_AUX	VX800(13)
CPU_CORE	CPU(11)

Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (6 to 19V)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P1.8V_AUX	GMCH/DDR II Power Source(off in S4-S5)
P1.5V_AUX	GMCH Power Source(off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
VCCA(1.5V)	1.5V CPU power rail.(off in S3-S5)
VCCP(1.05V)	1.05V CPU power rail.(off in S3-S5)
CPU_CORE	Core voltage for VIA NANO CPU.
P3.3V_MICOM	3.3V always on power rail for MICOM
LCD_VDD3.3V	3.3V (LCD)
VCC_CRT	5V (CRT)
2.5V_LAN	2.5V(88E8040)
P4.75_AUD	4.75V (ALC272)
P5.0V_AUD	5V(ALC272)
P5.0V_AMP	5V (Audio AMP)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	DOTHAN-ULV Base Stealey HIGH FREQUENCY MODE
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V	DOTHAN-ULV Base Stealey LOW FREQUENCY MODE
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V	
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V	
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V	
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V	
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V	
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V	DOTHAN-ULV Base Stealey DEEPER SLEEP MODE Refer to page??
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

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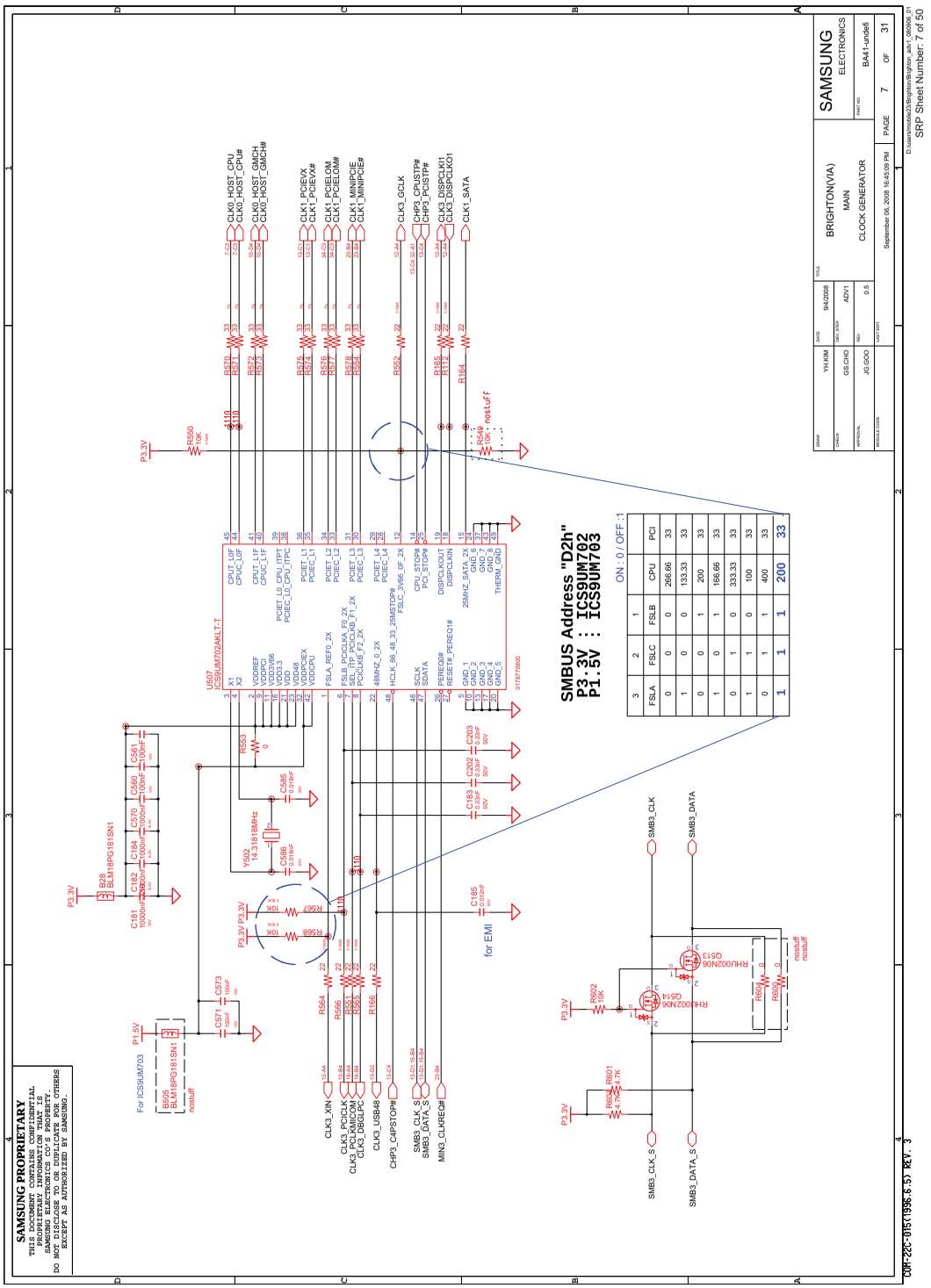

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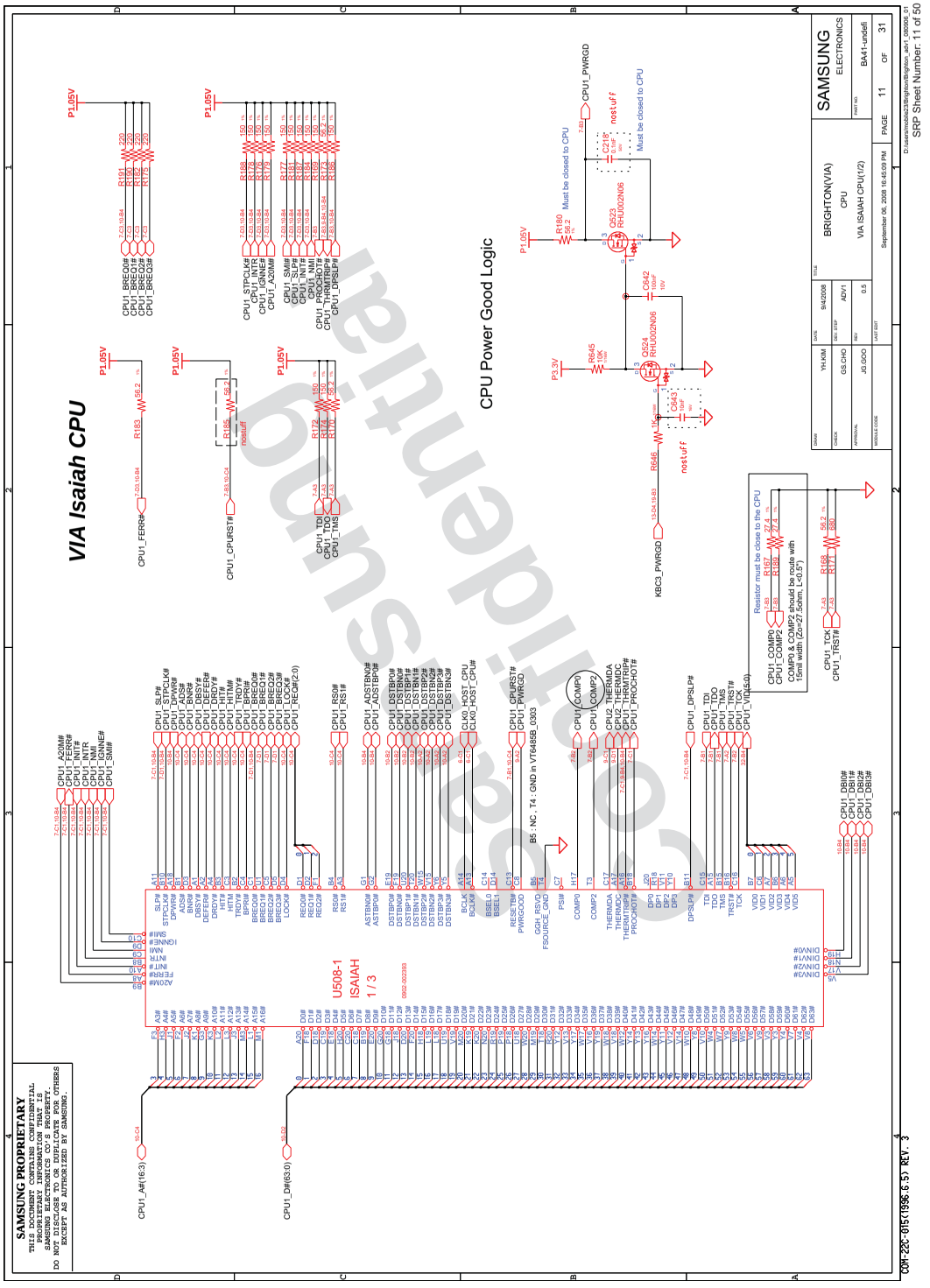

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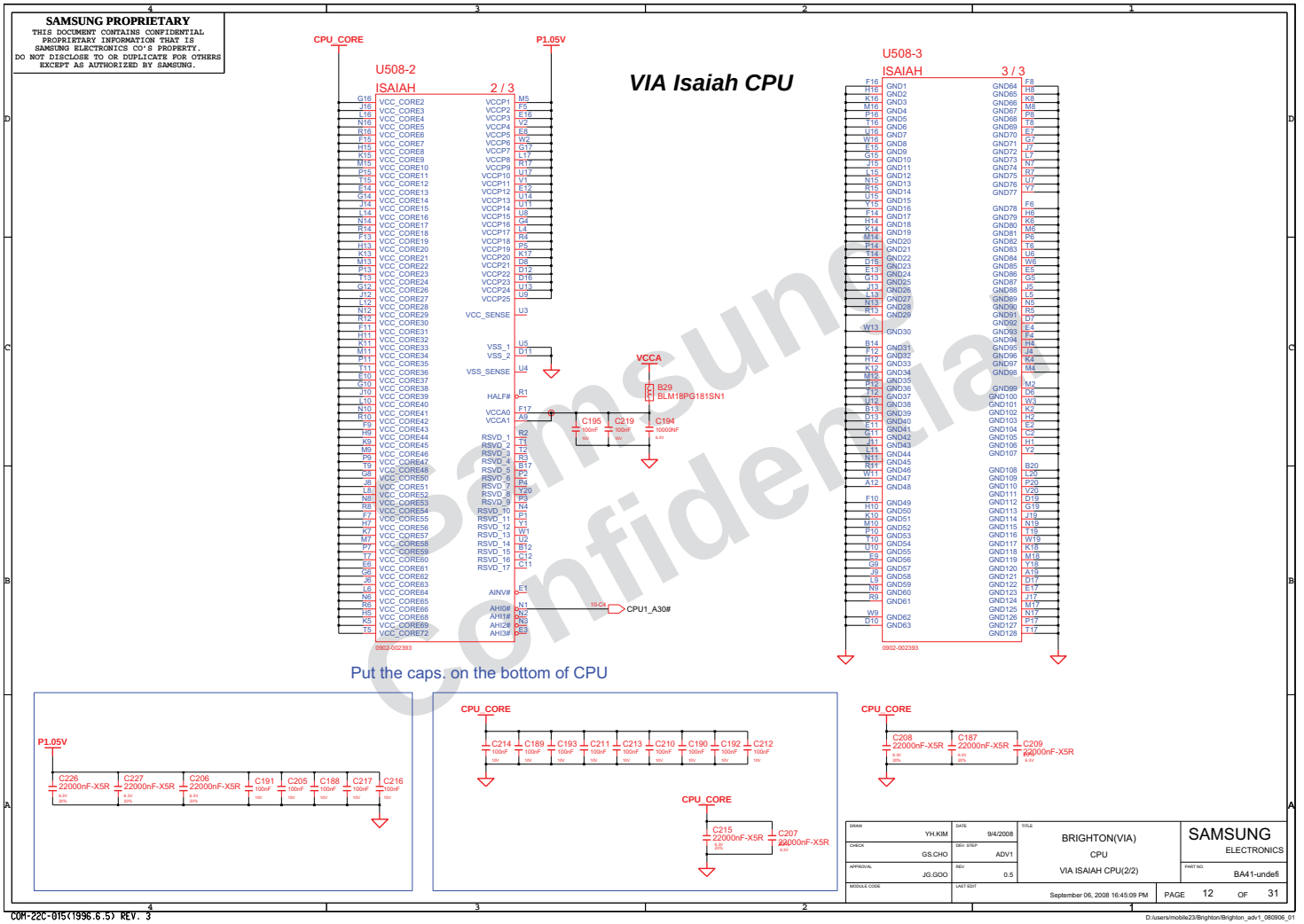

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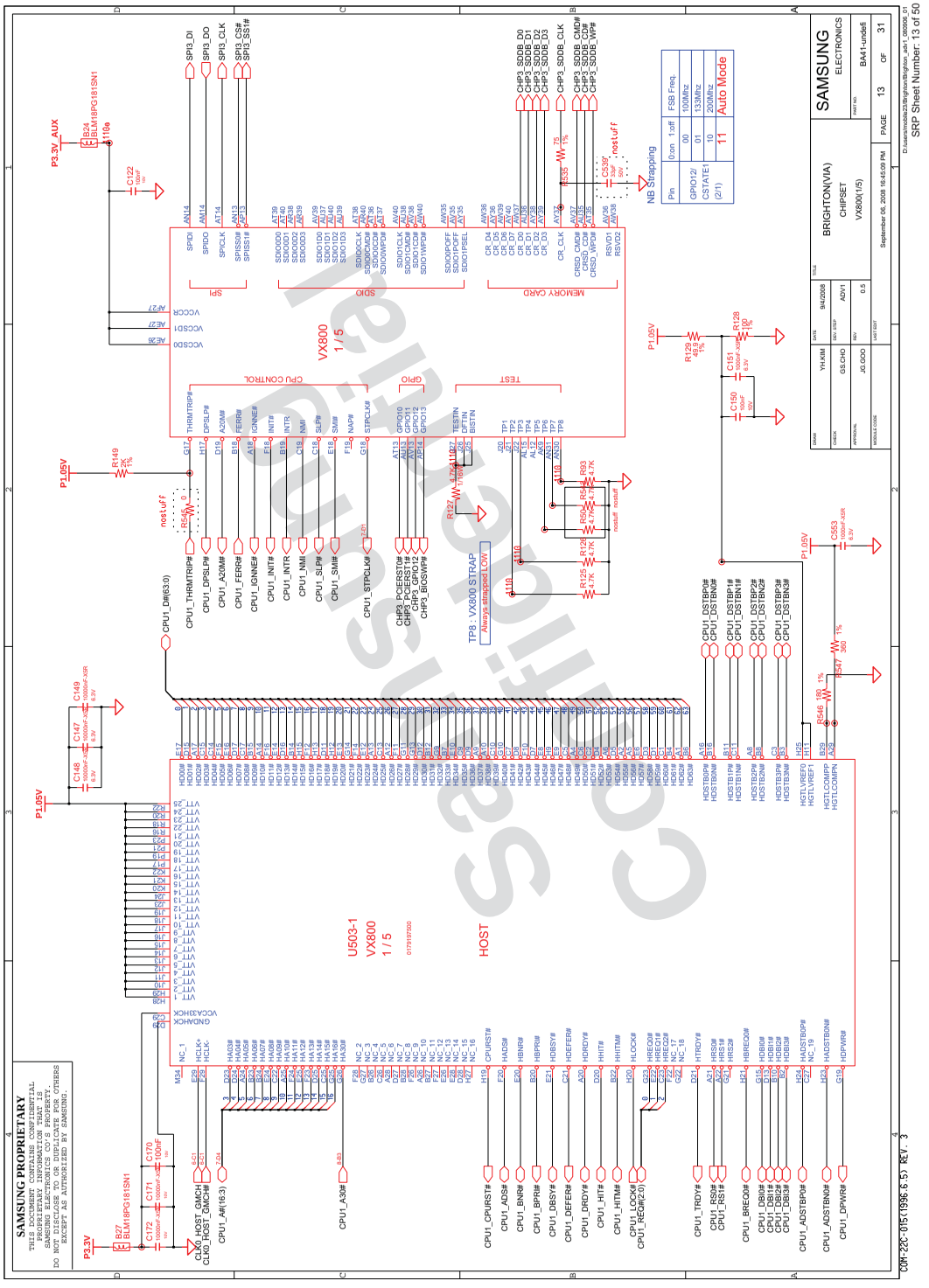

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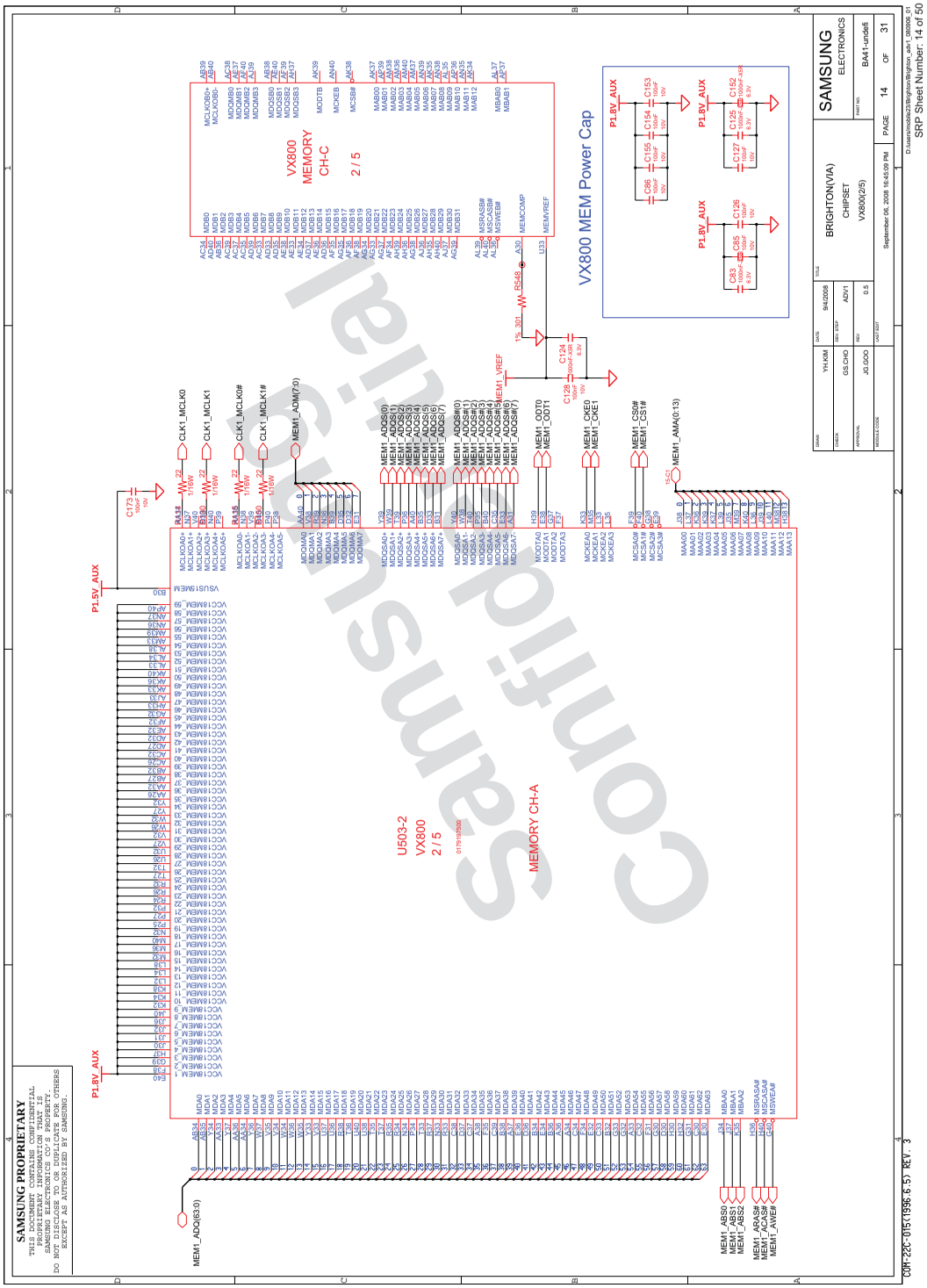

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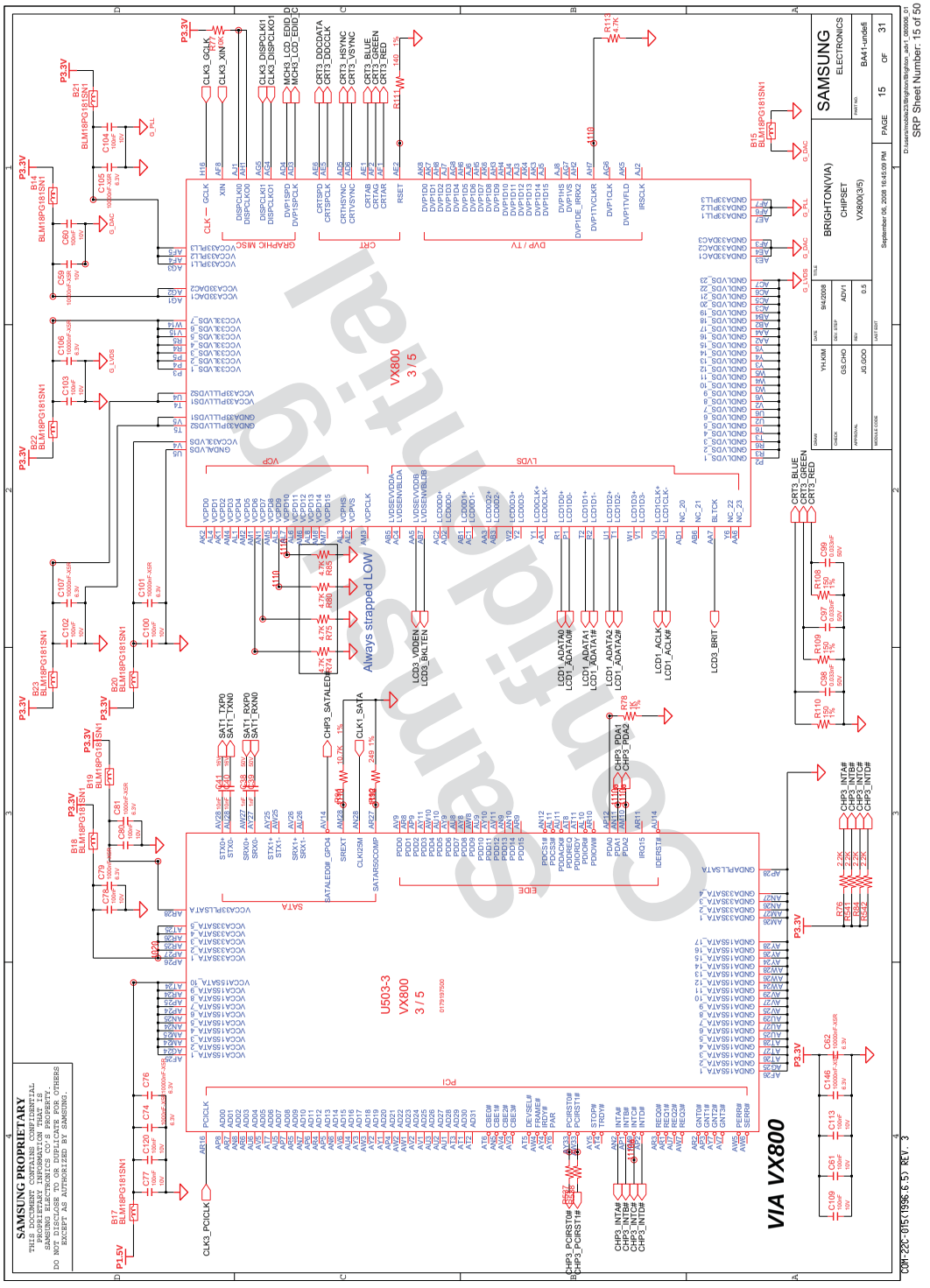

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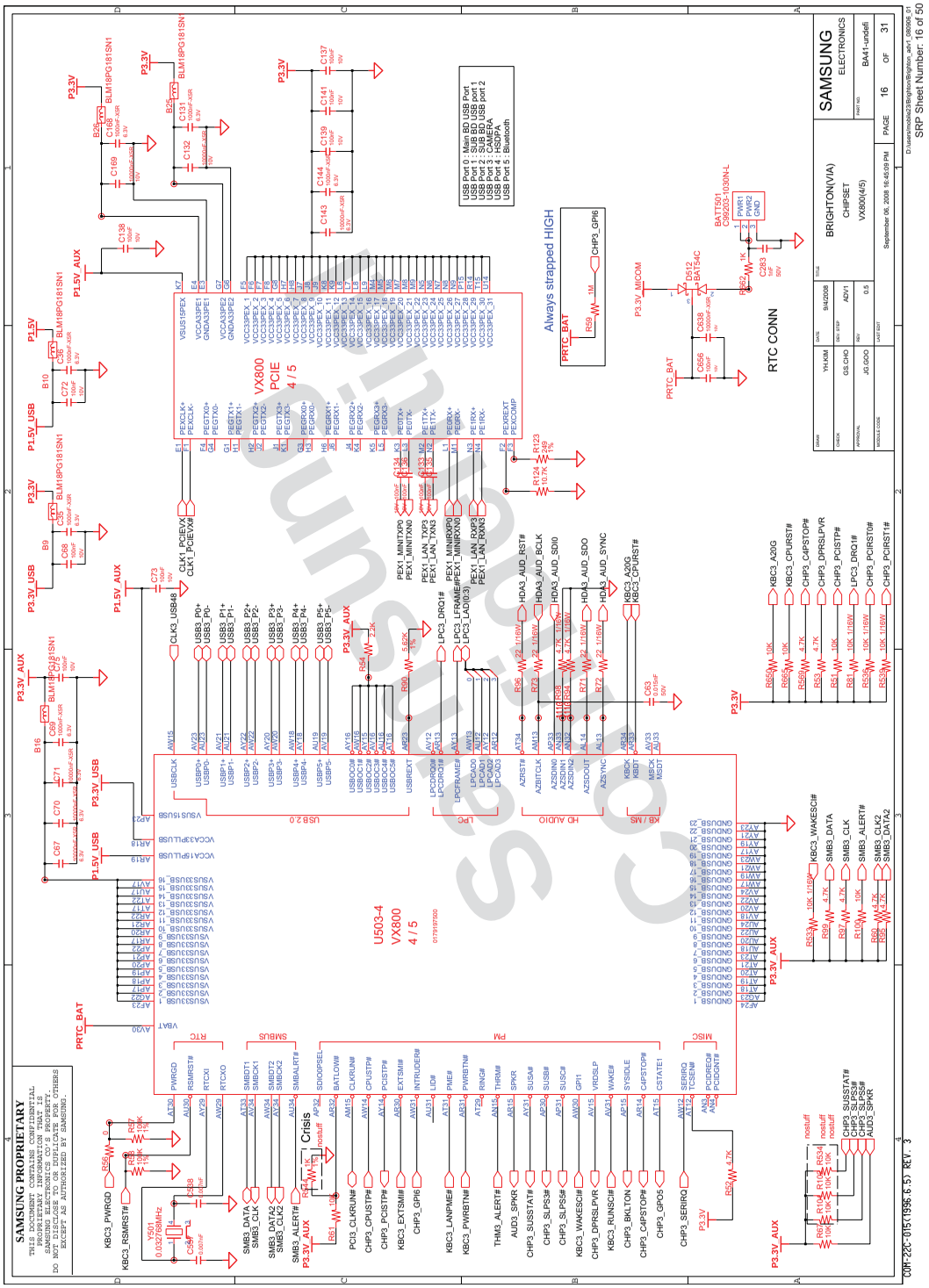

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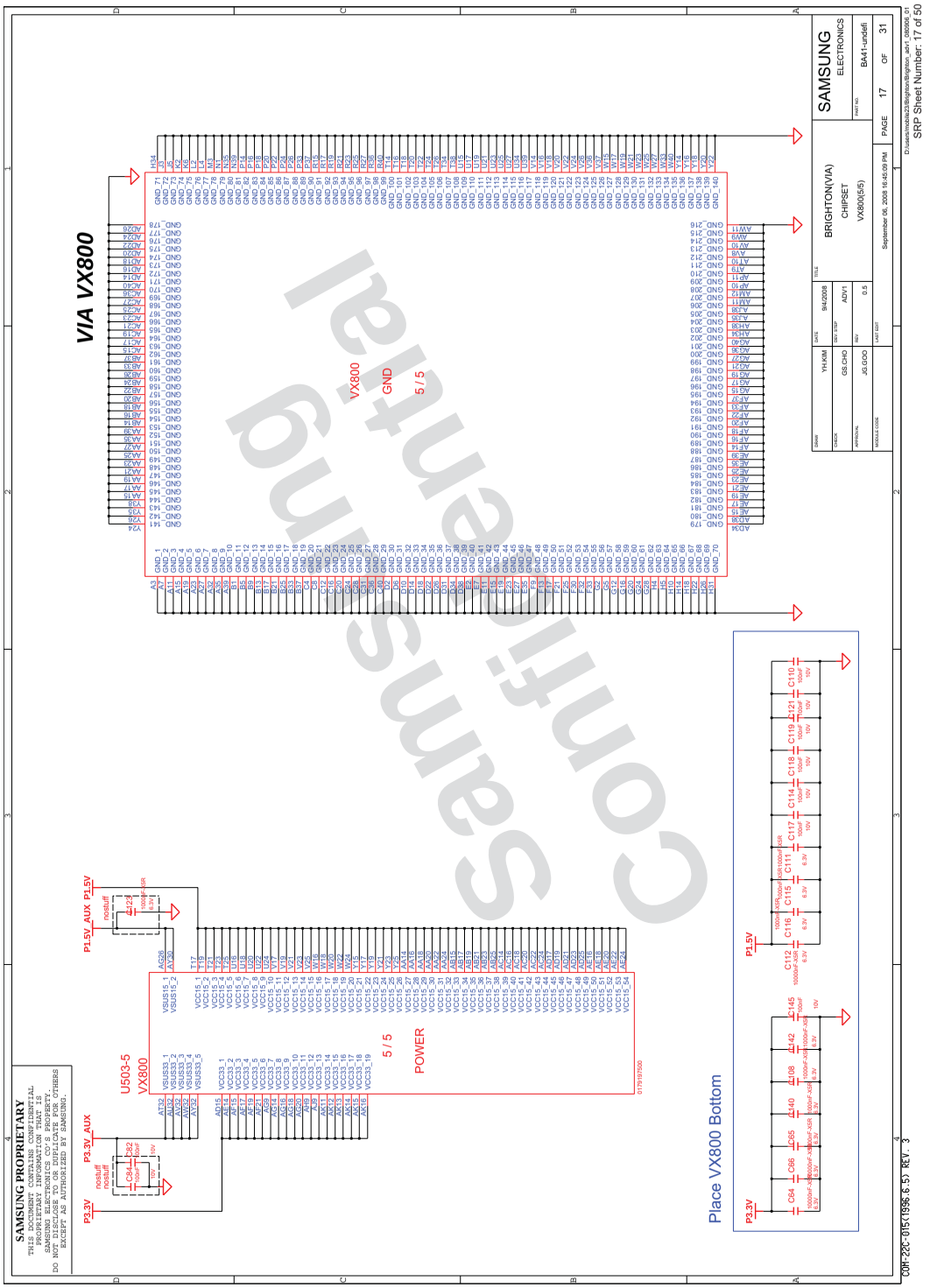

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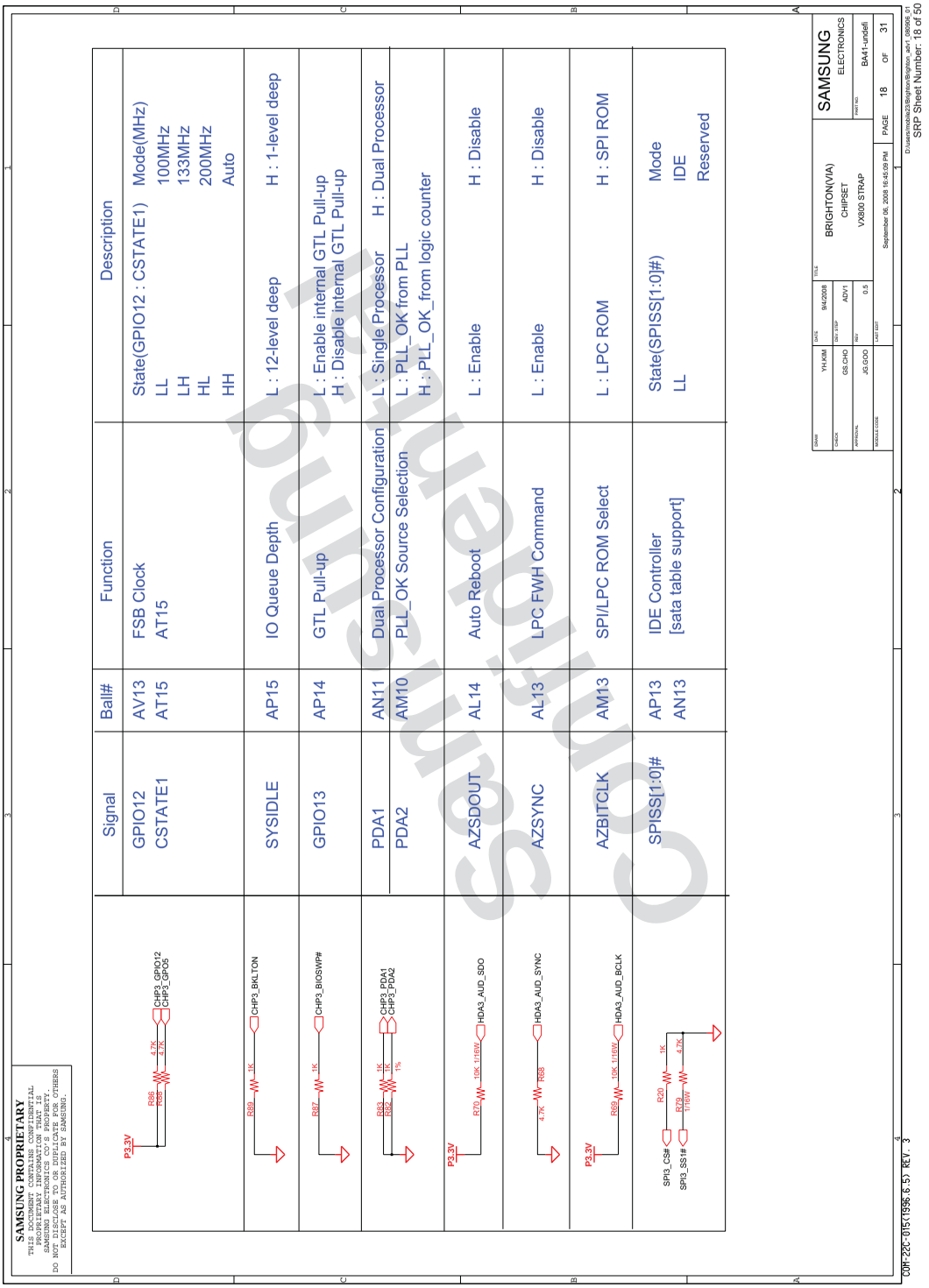

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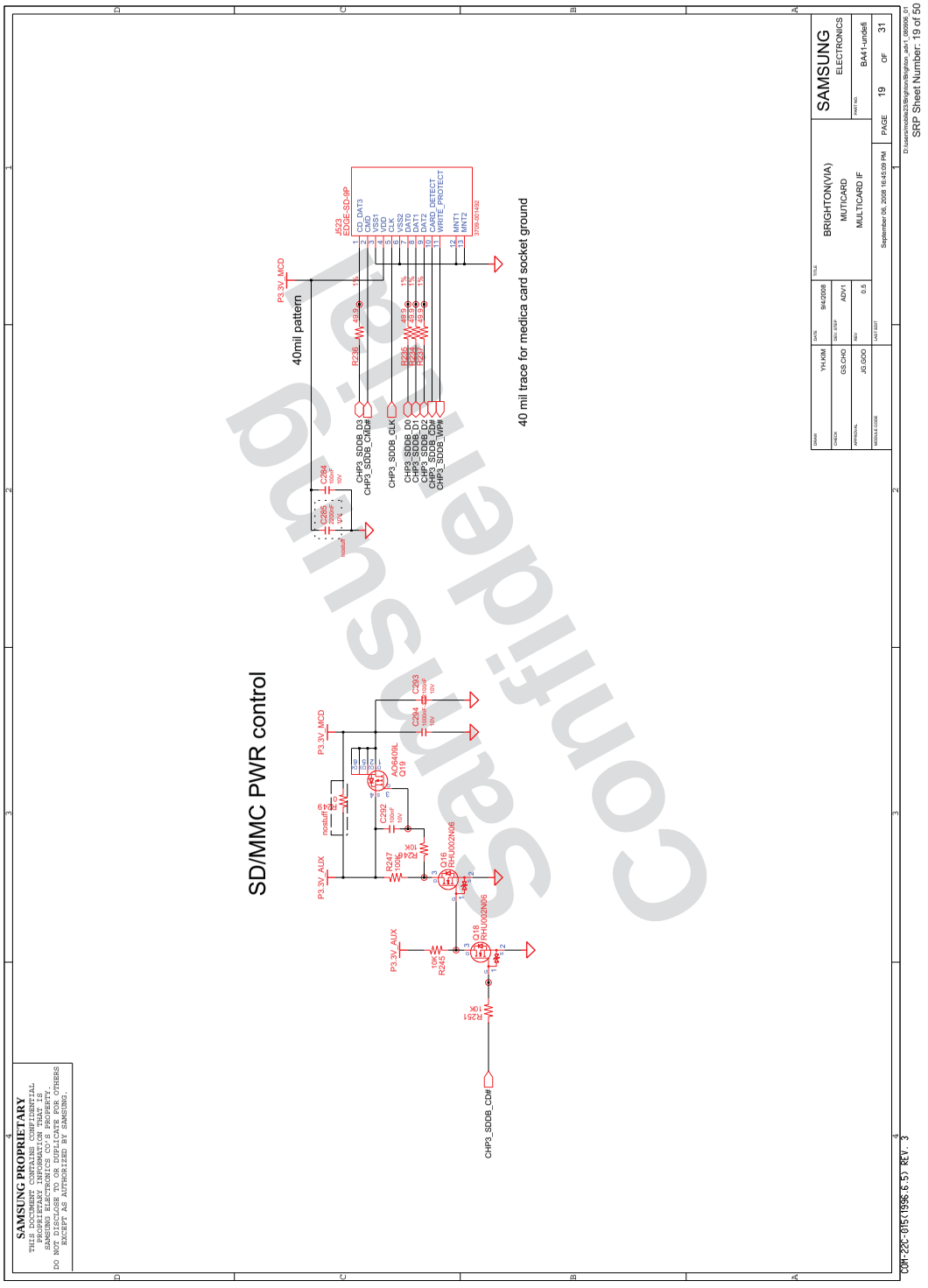

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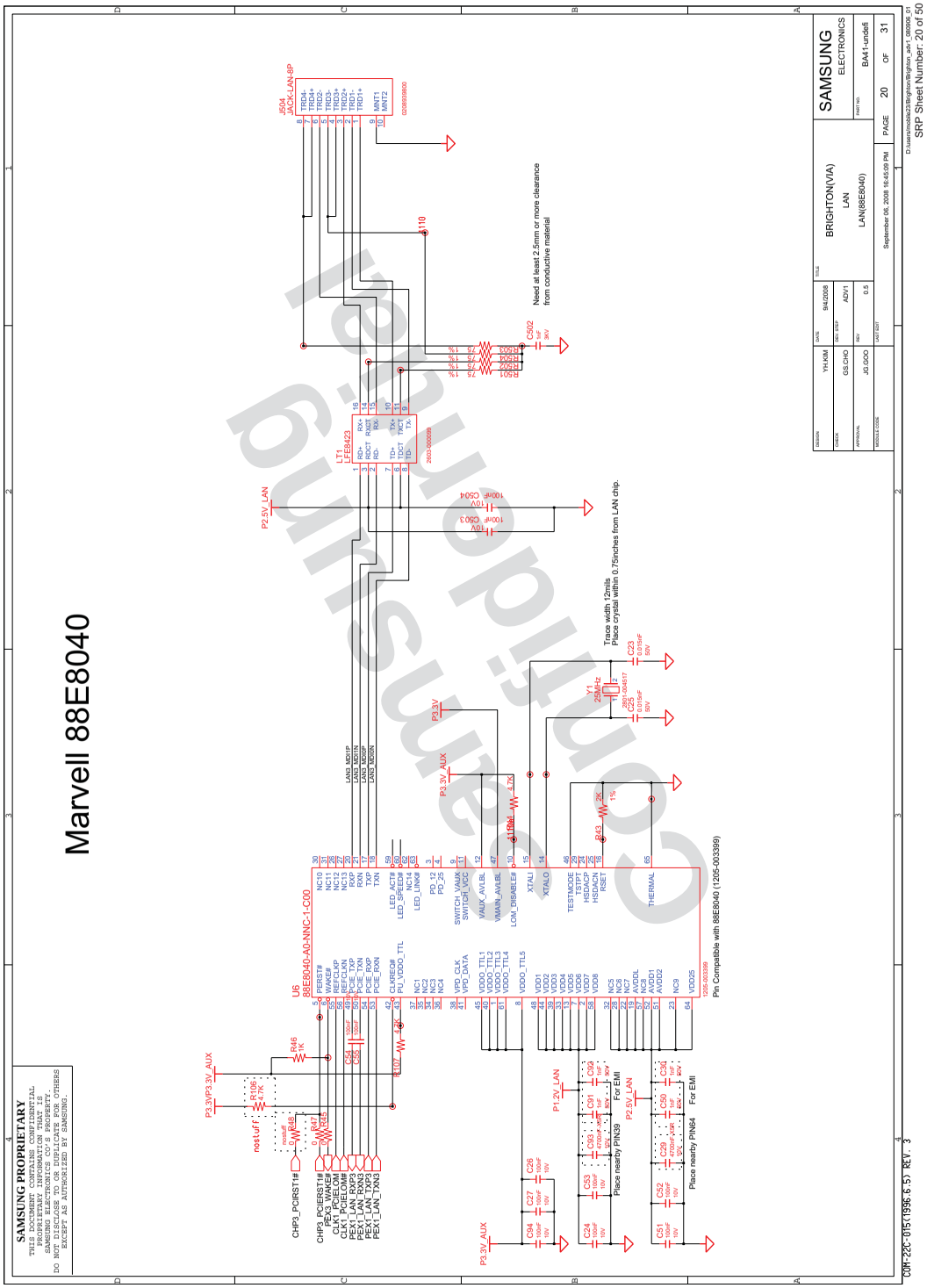

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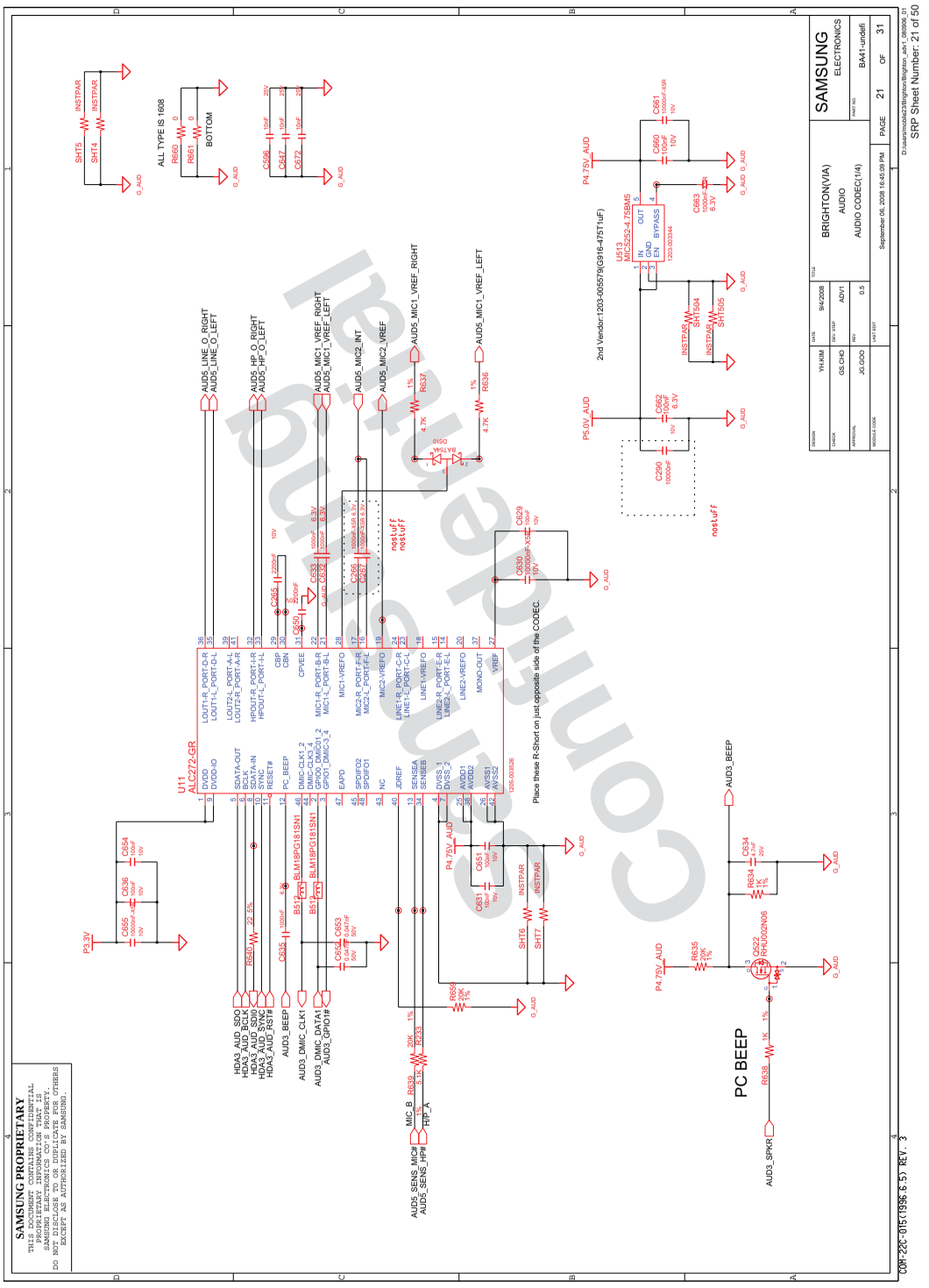

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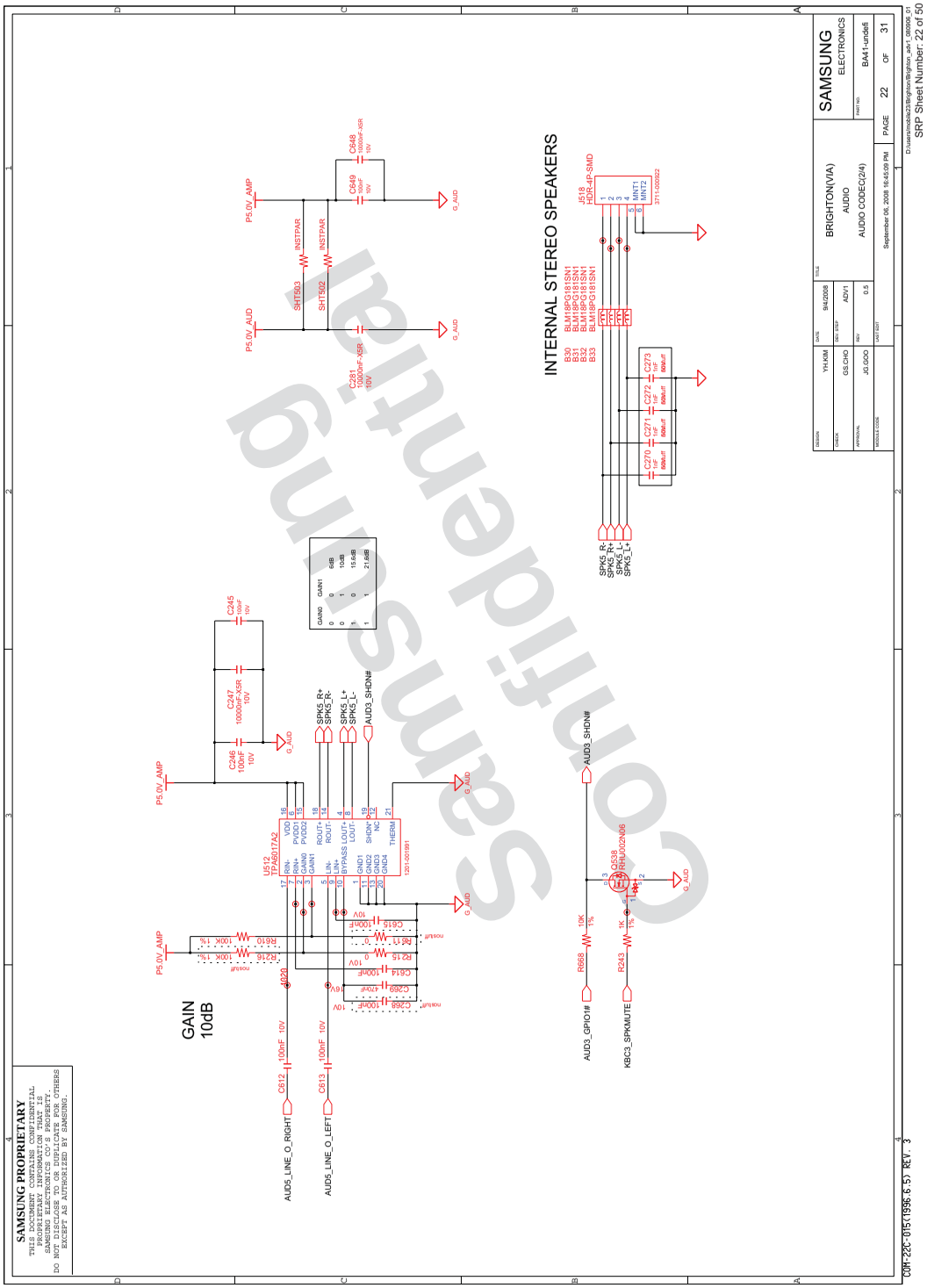

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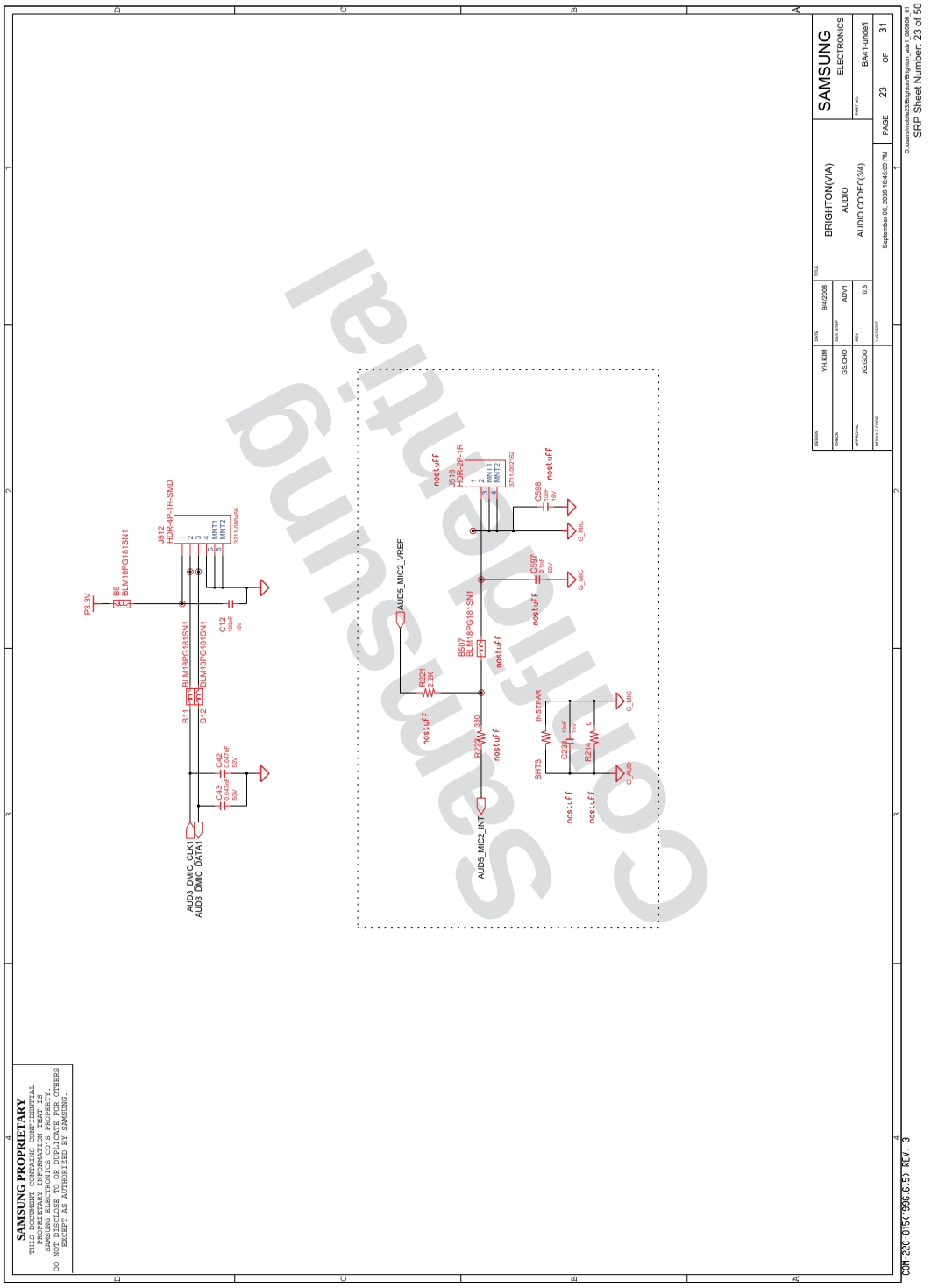

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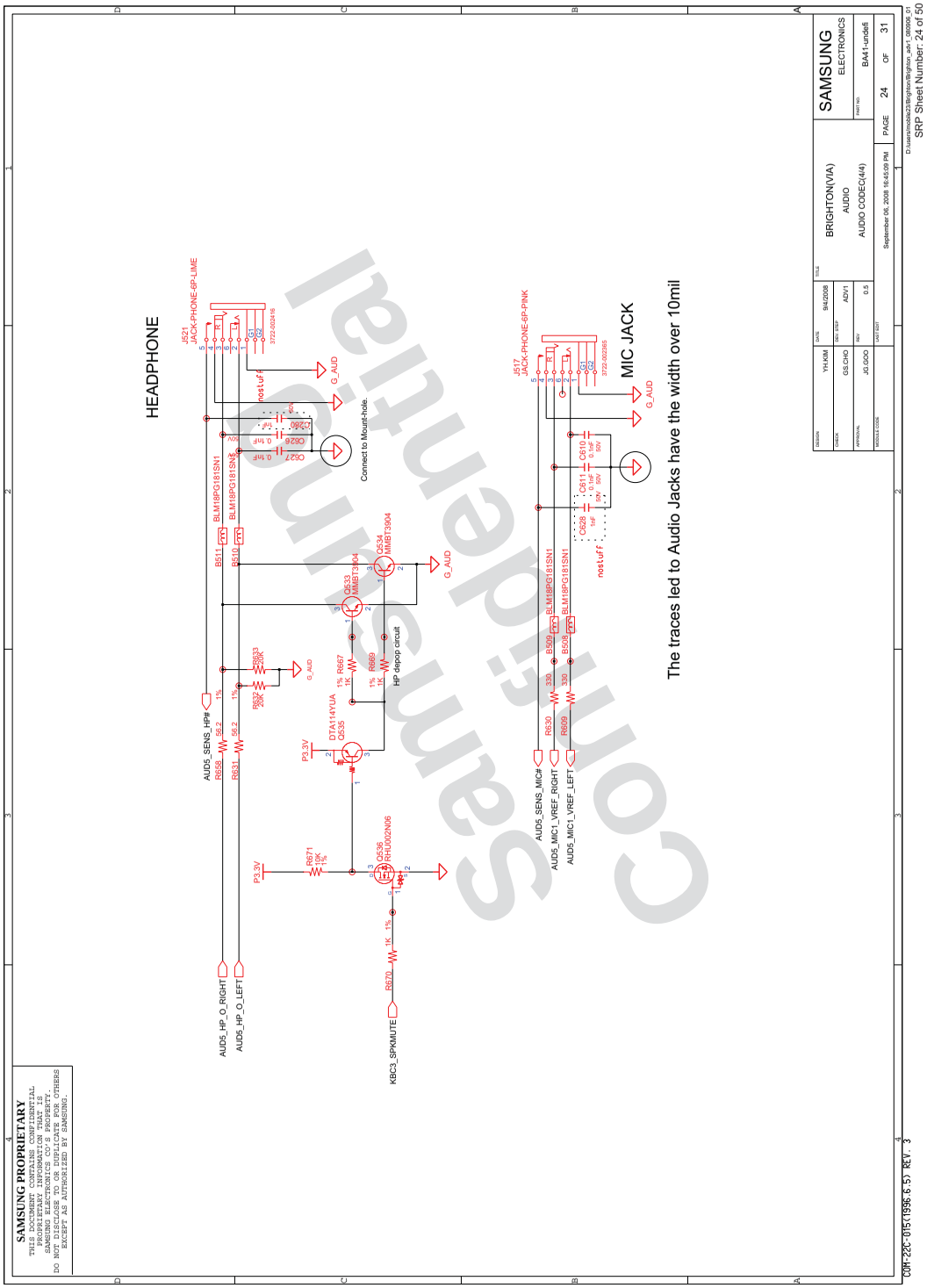

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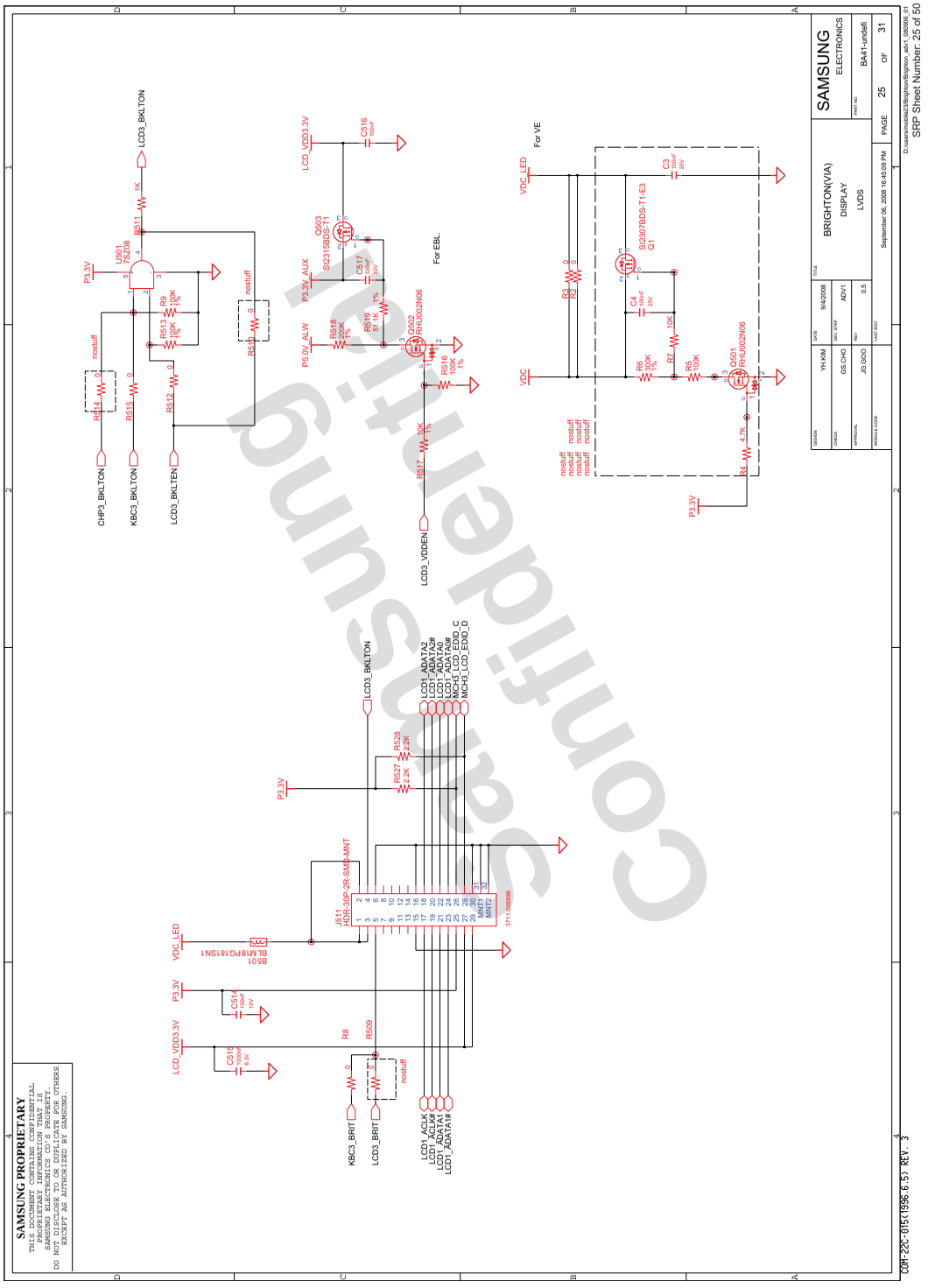

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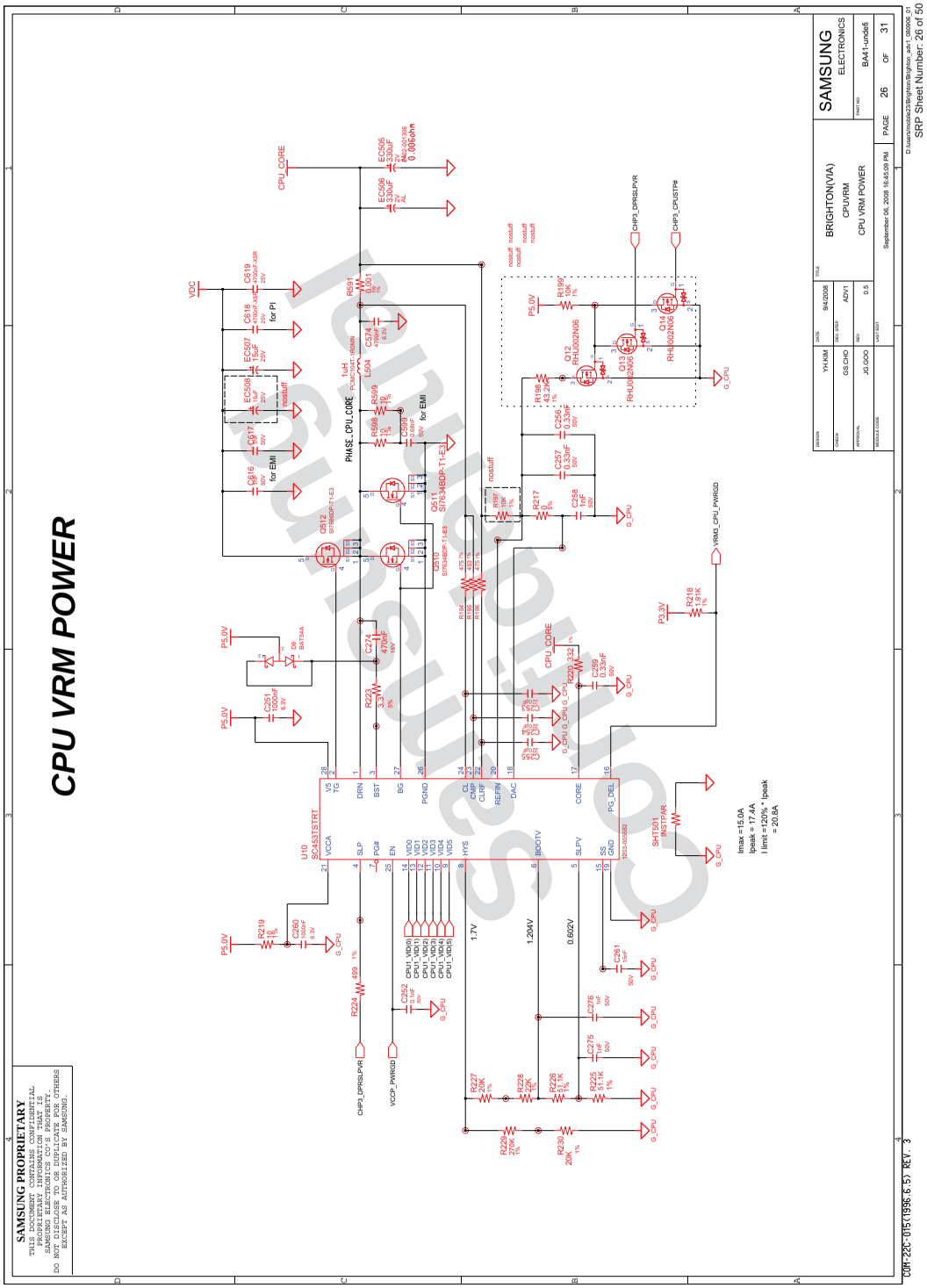

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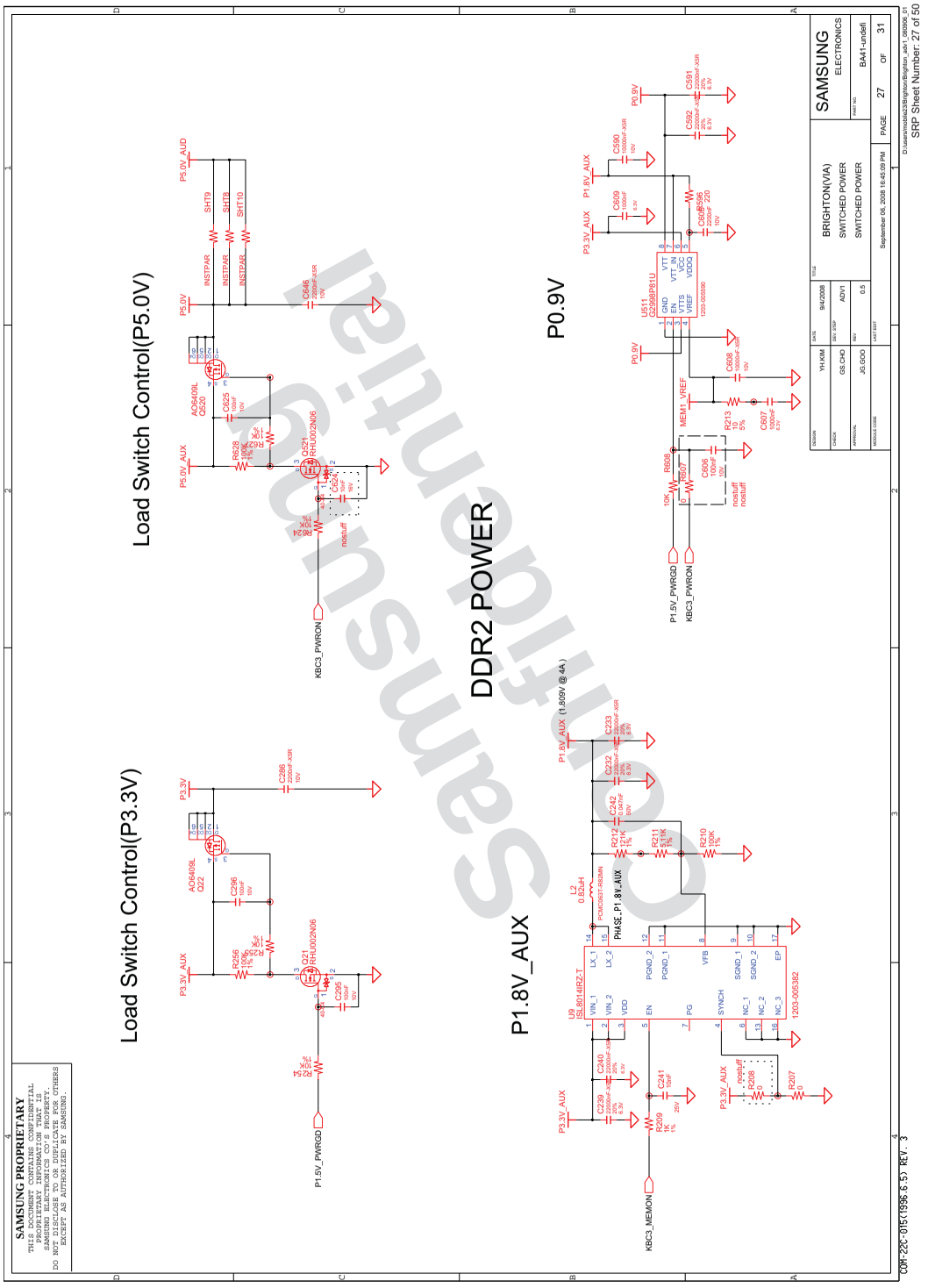

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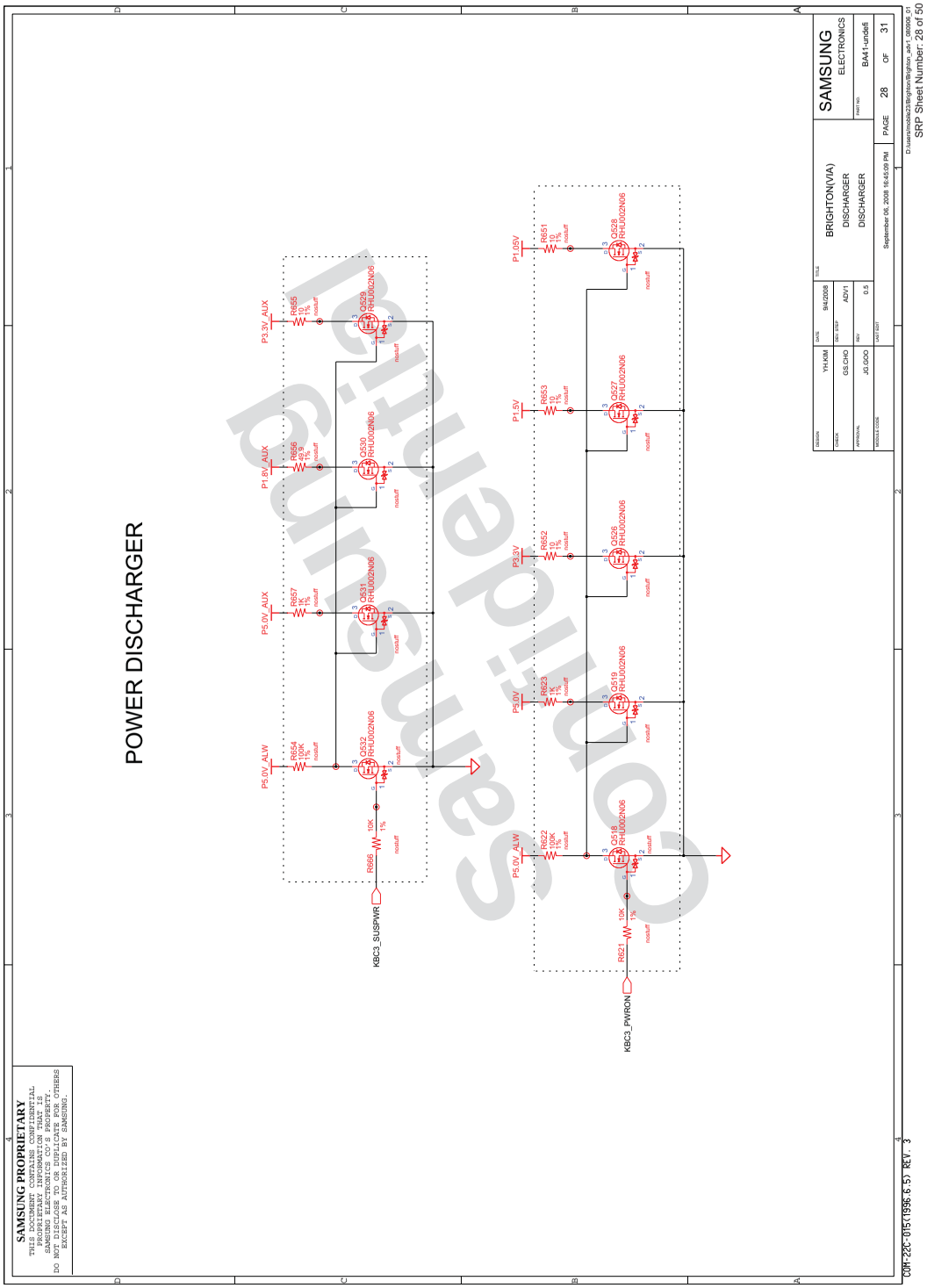

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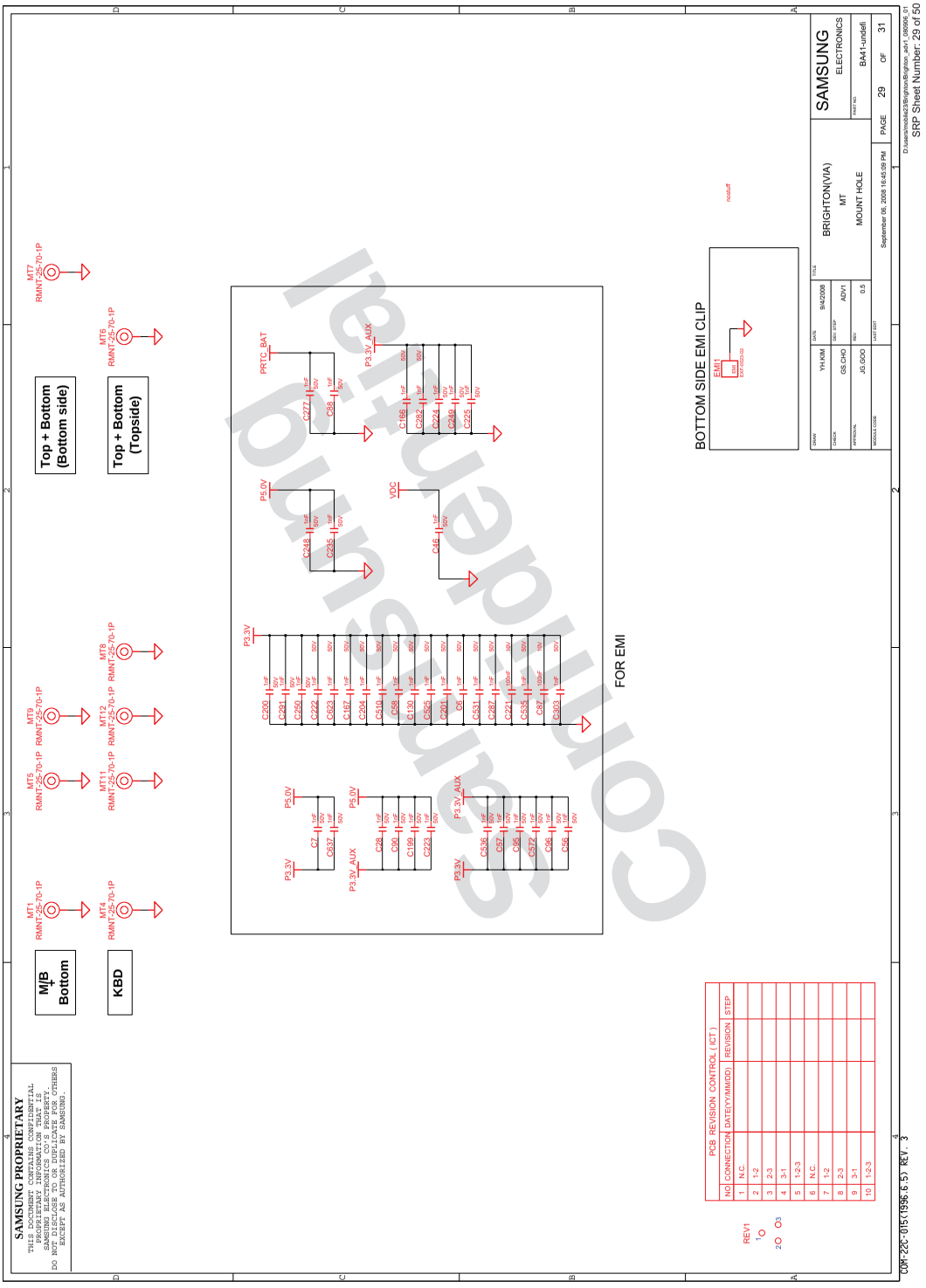

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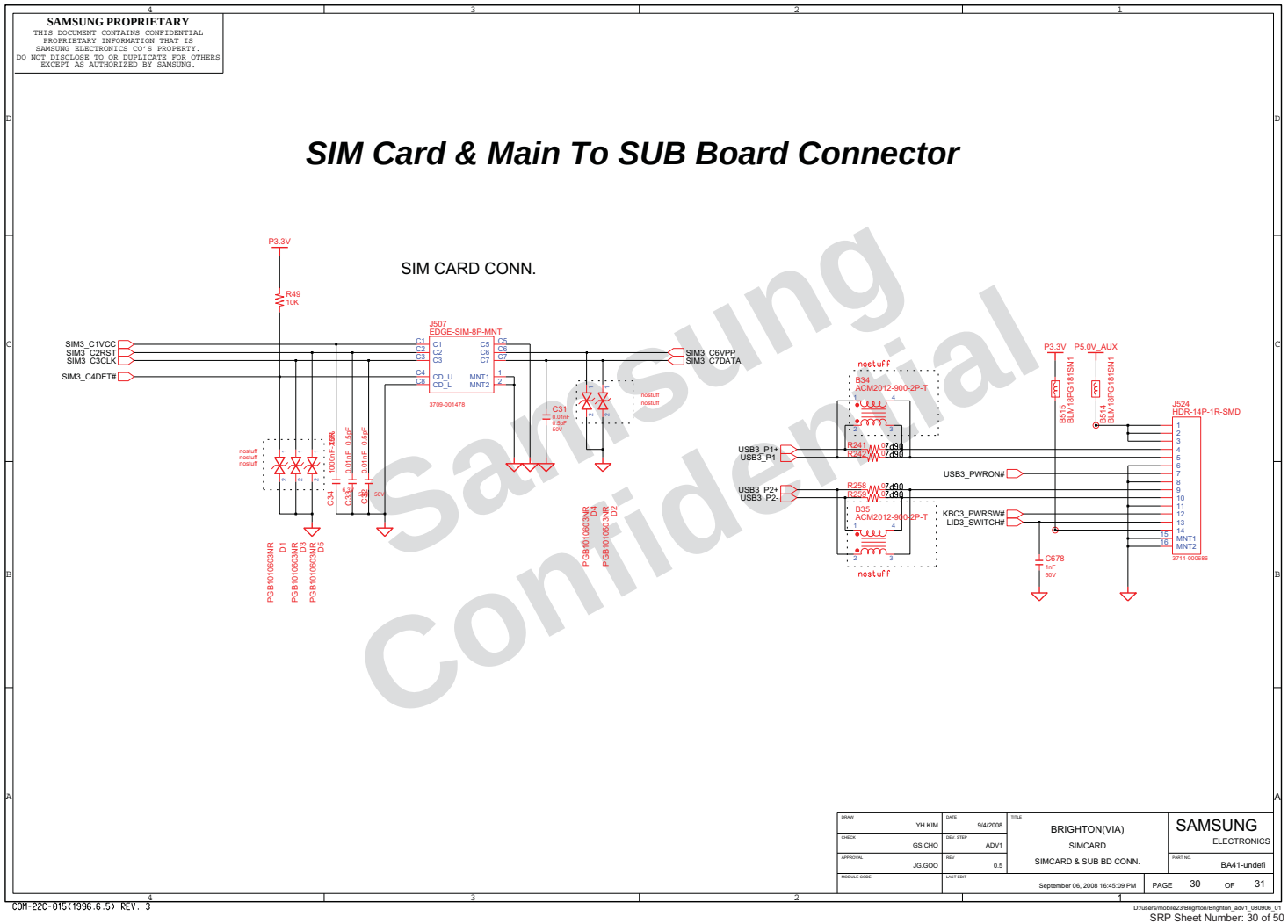

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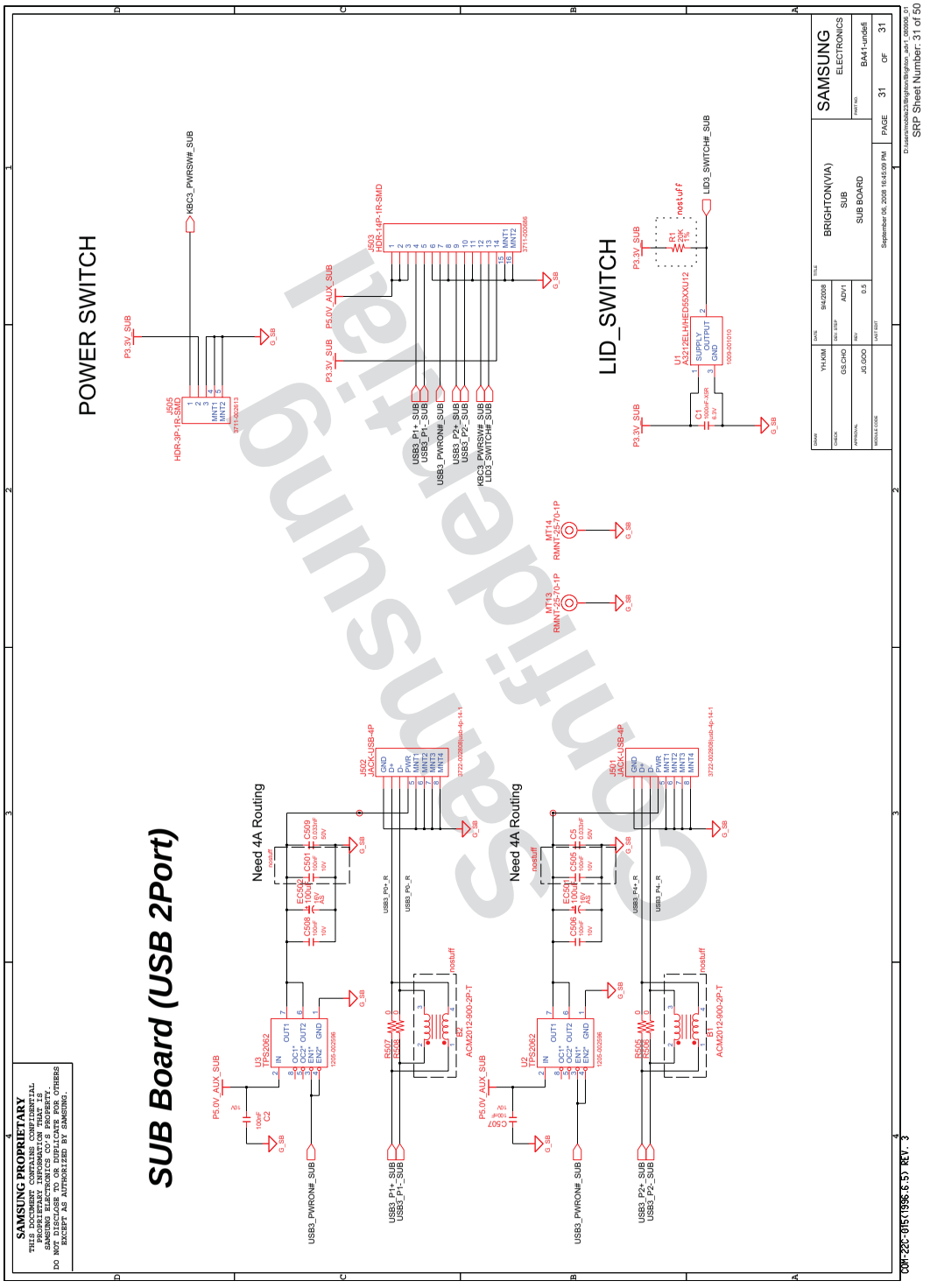

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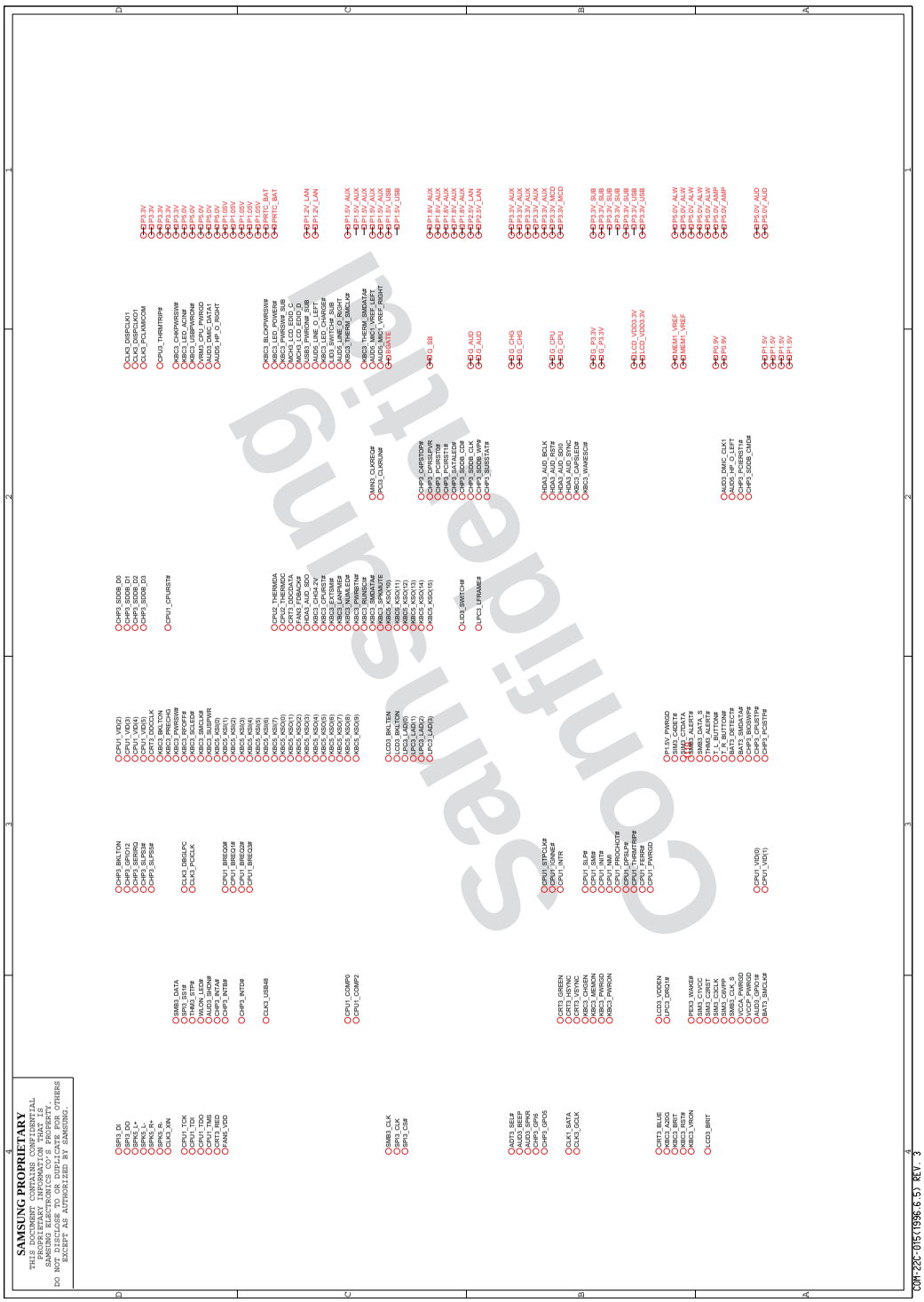

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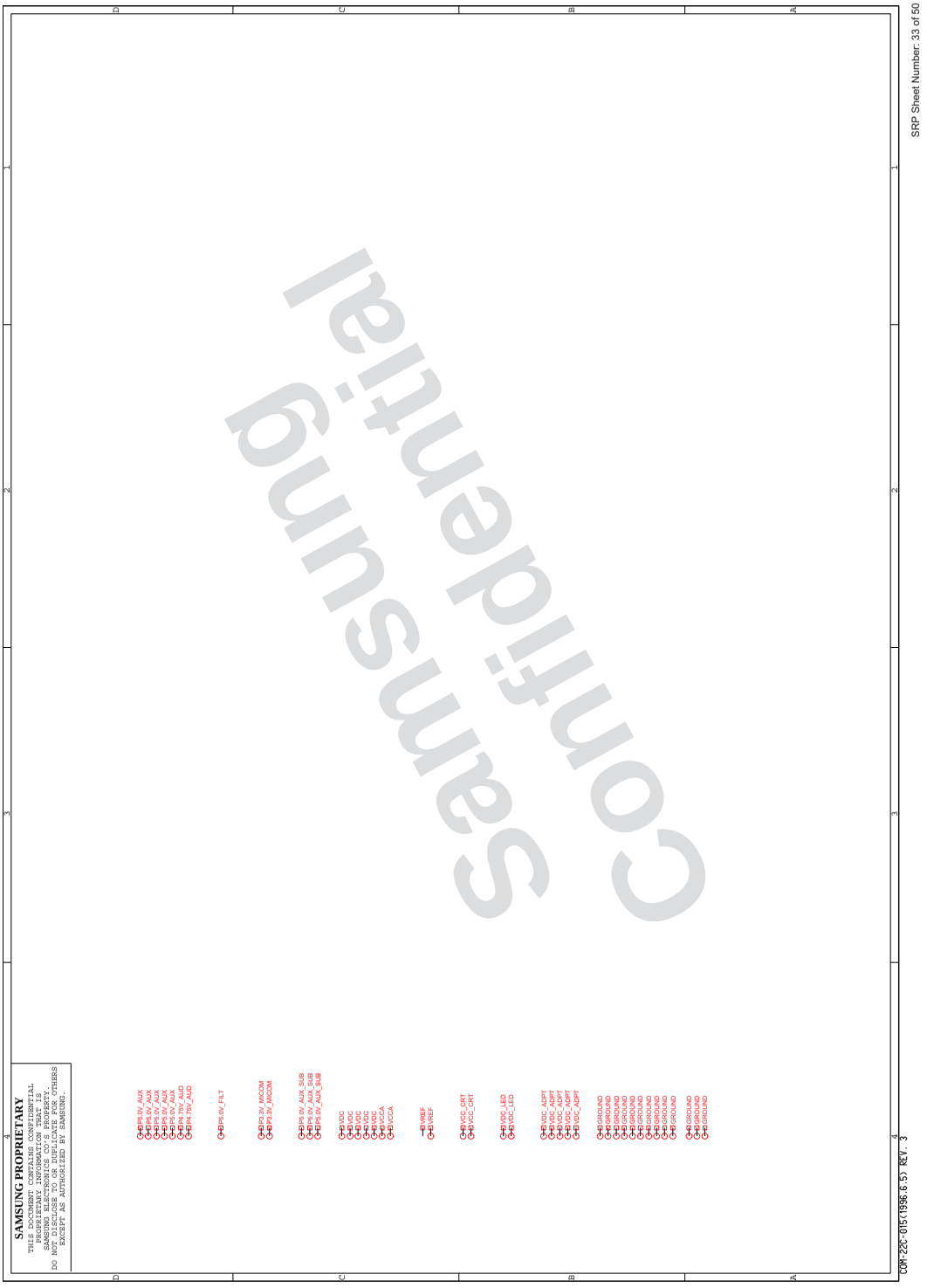

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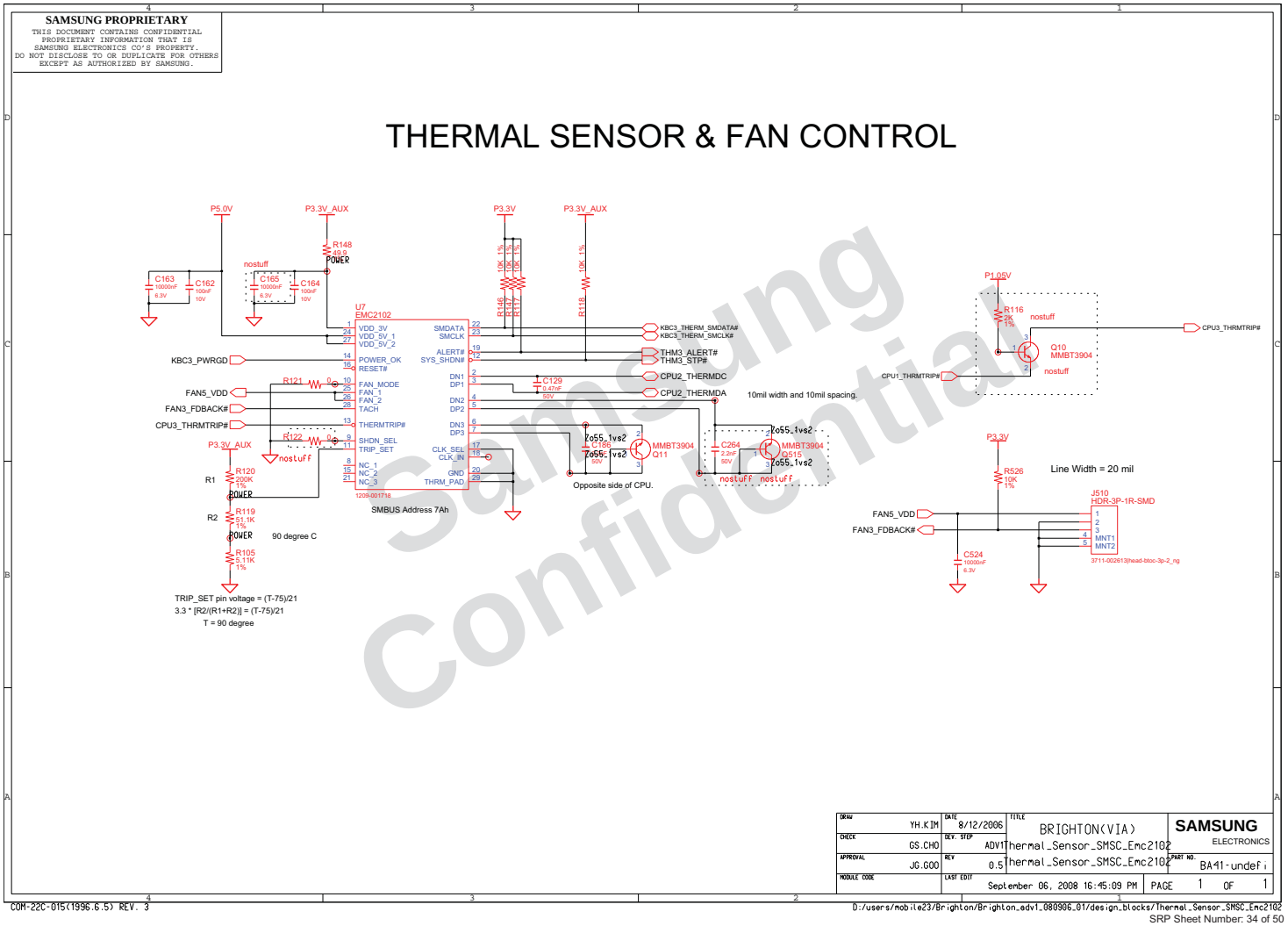

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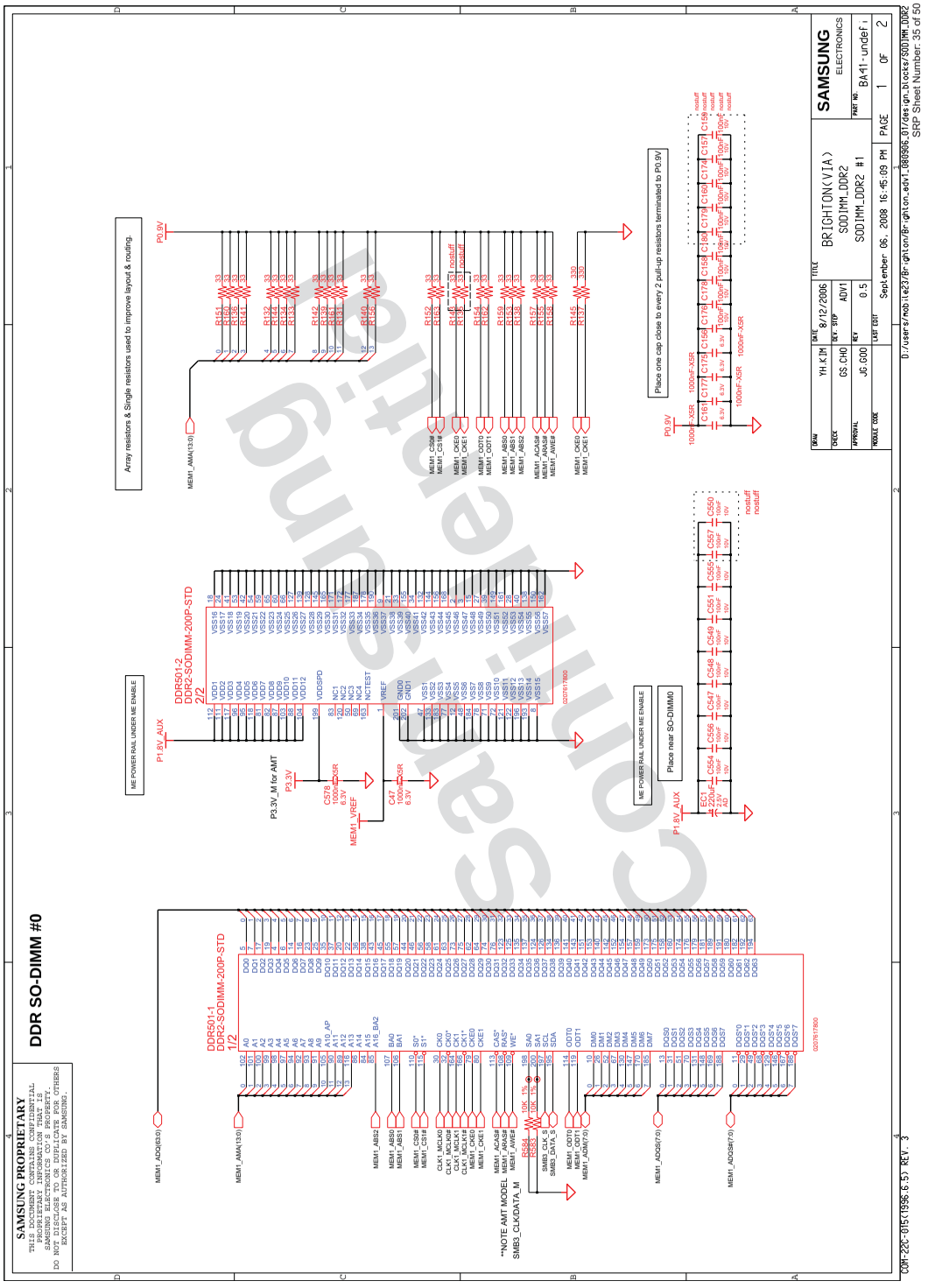

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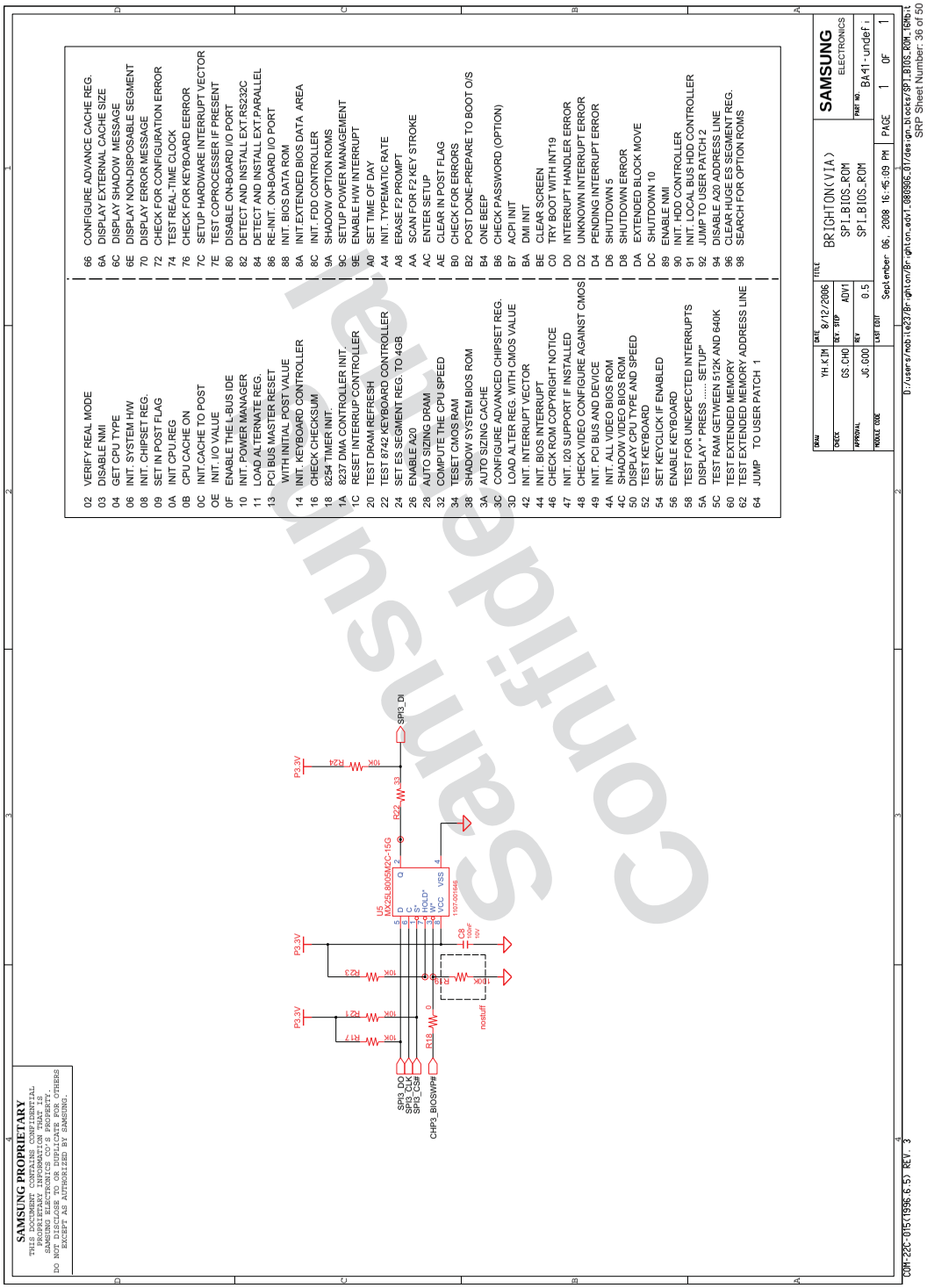

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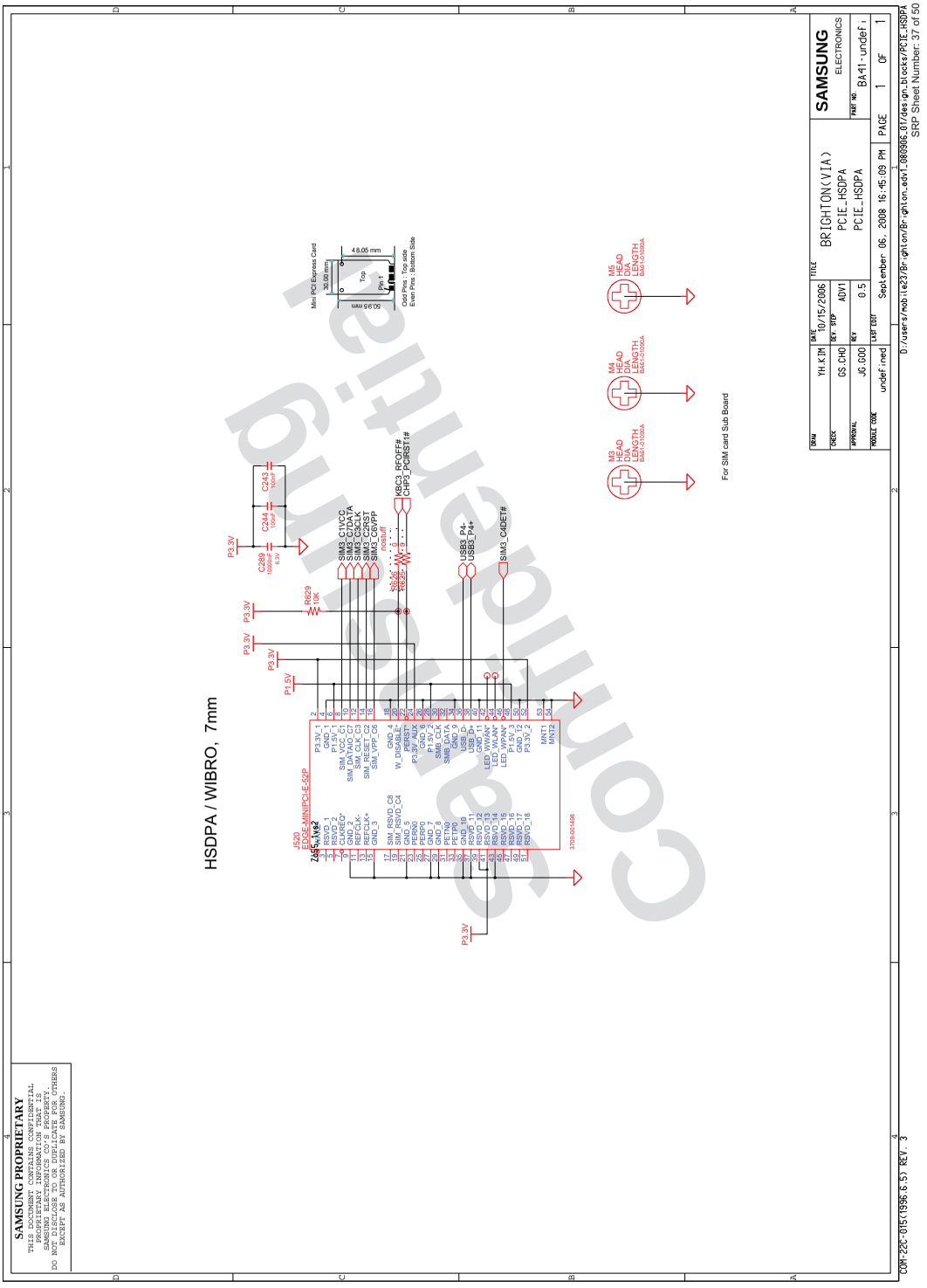

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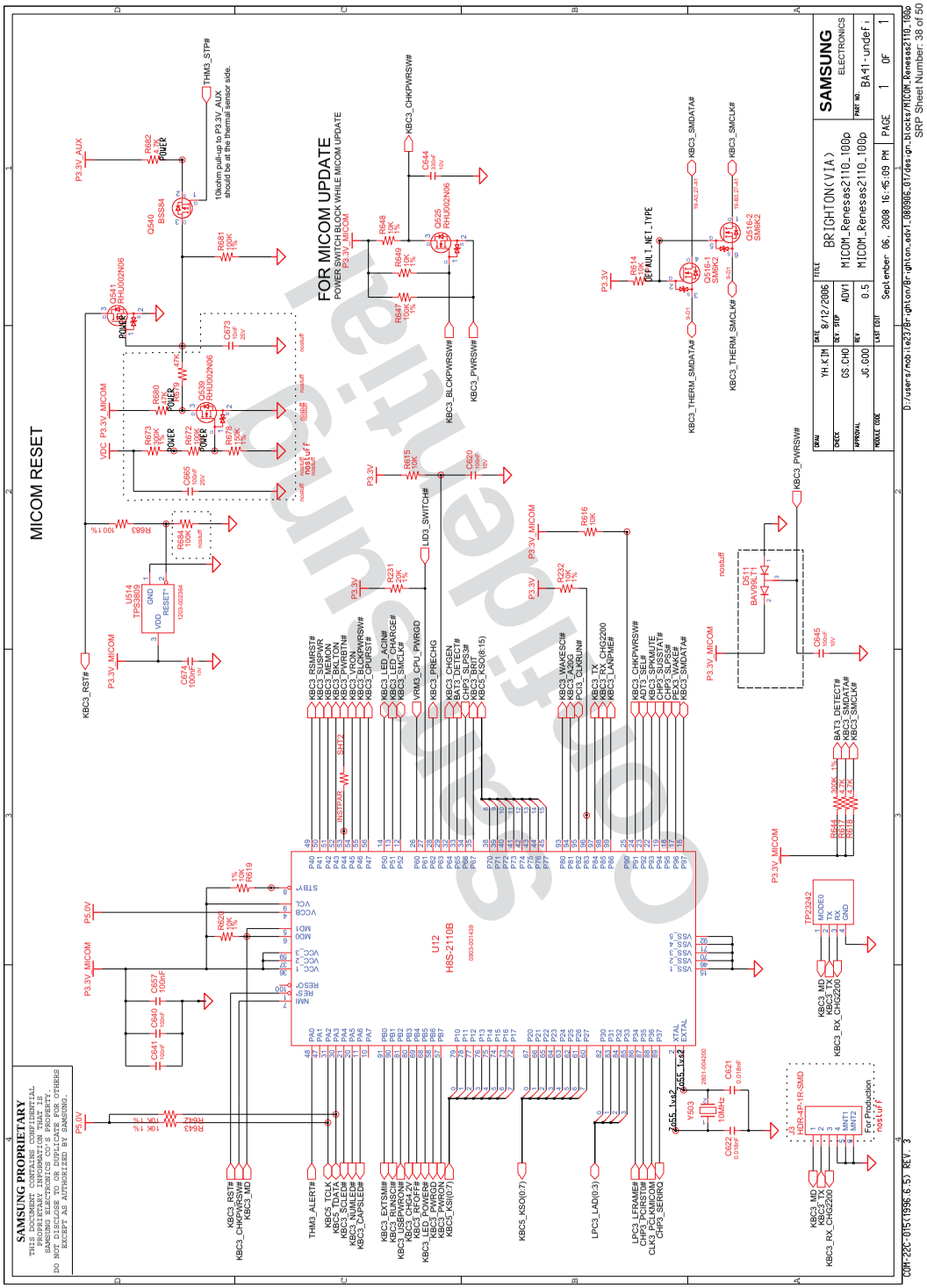

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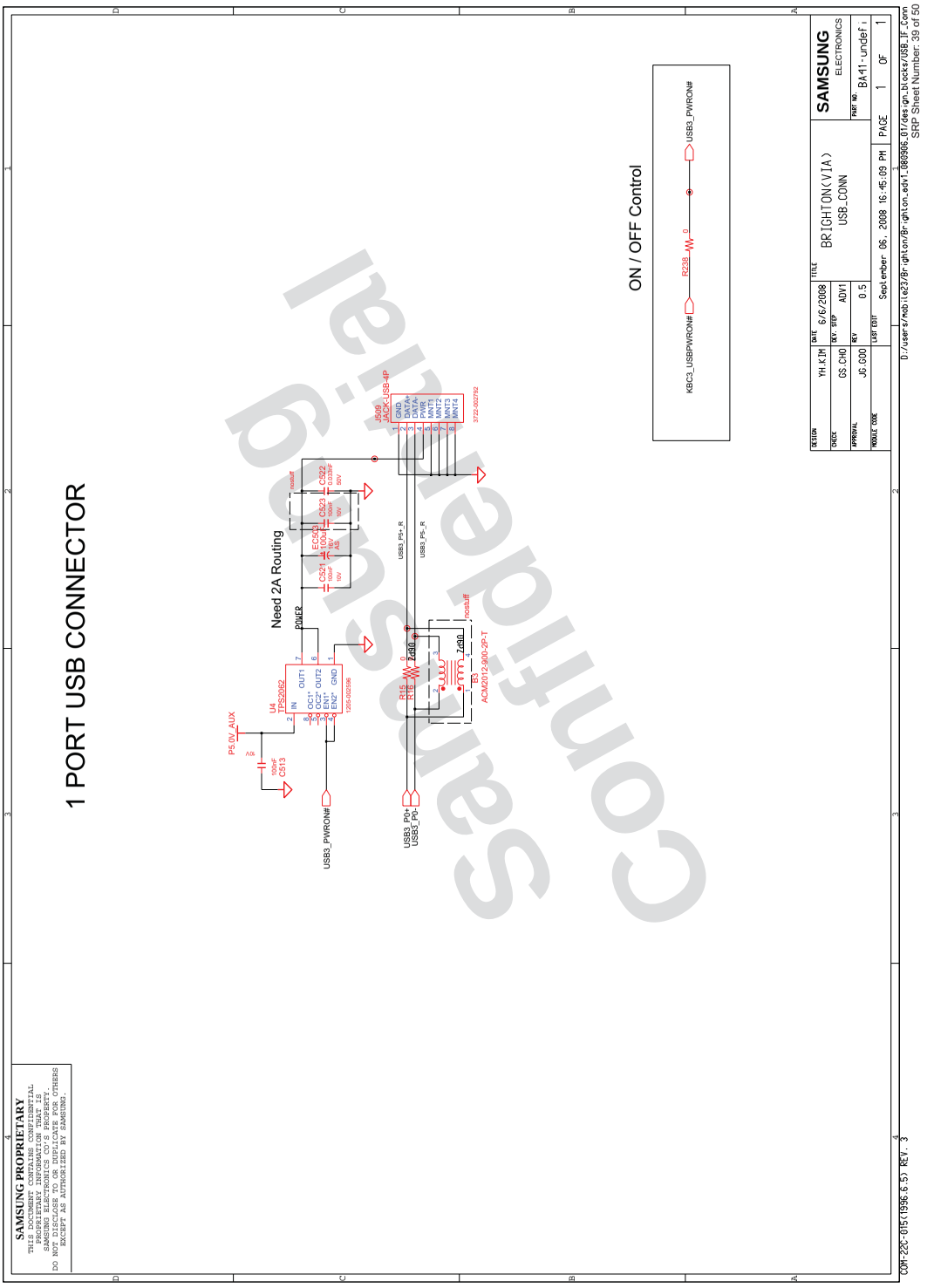

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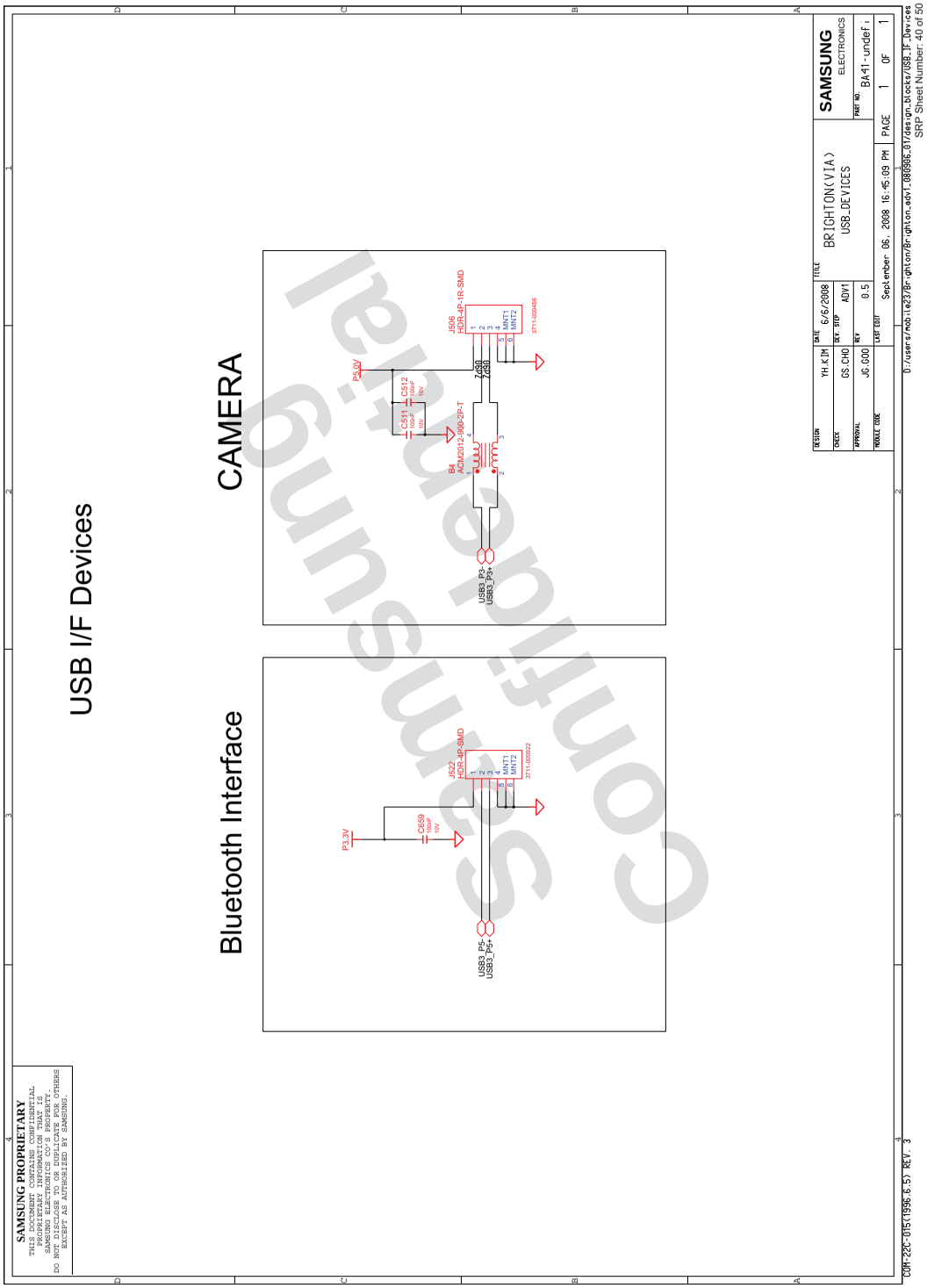

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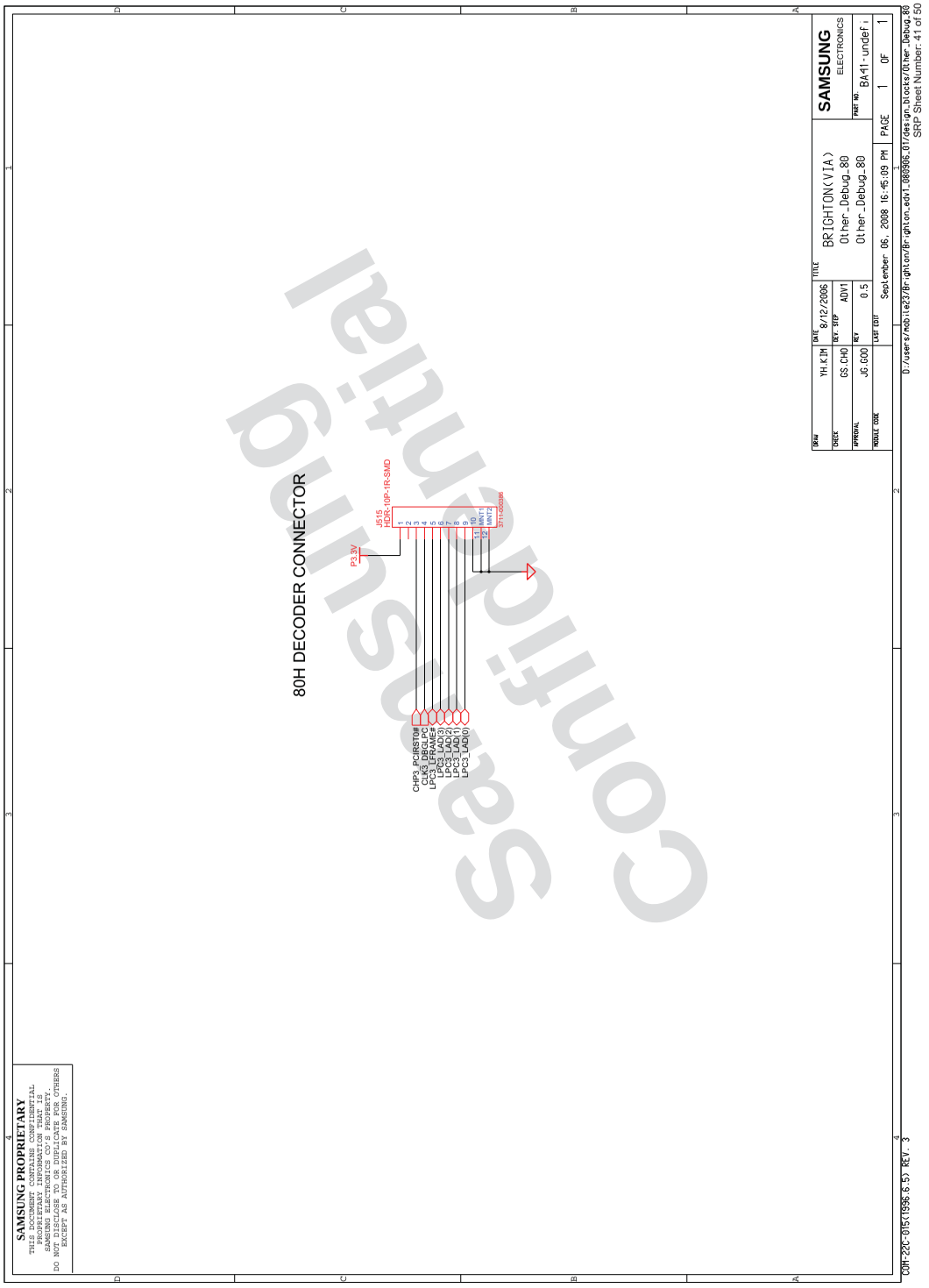

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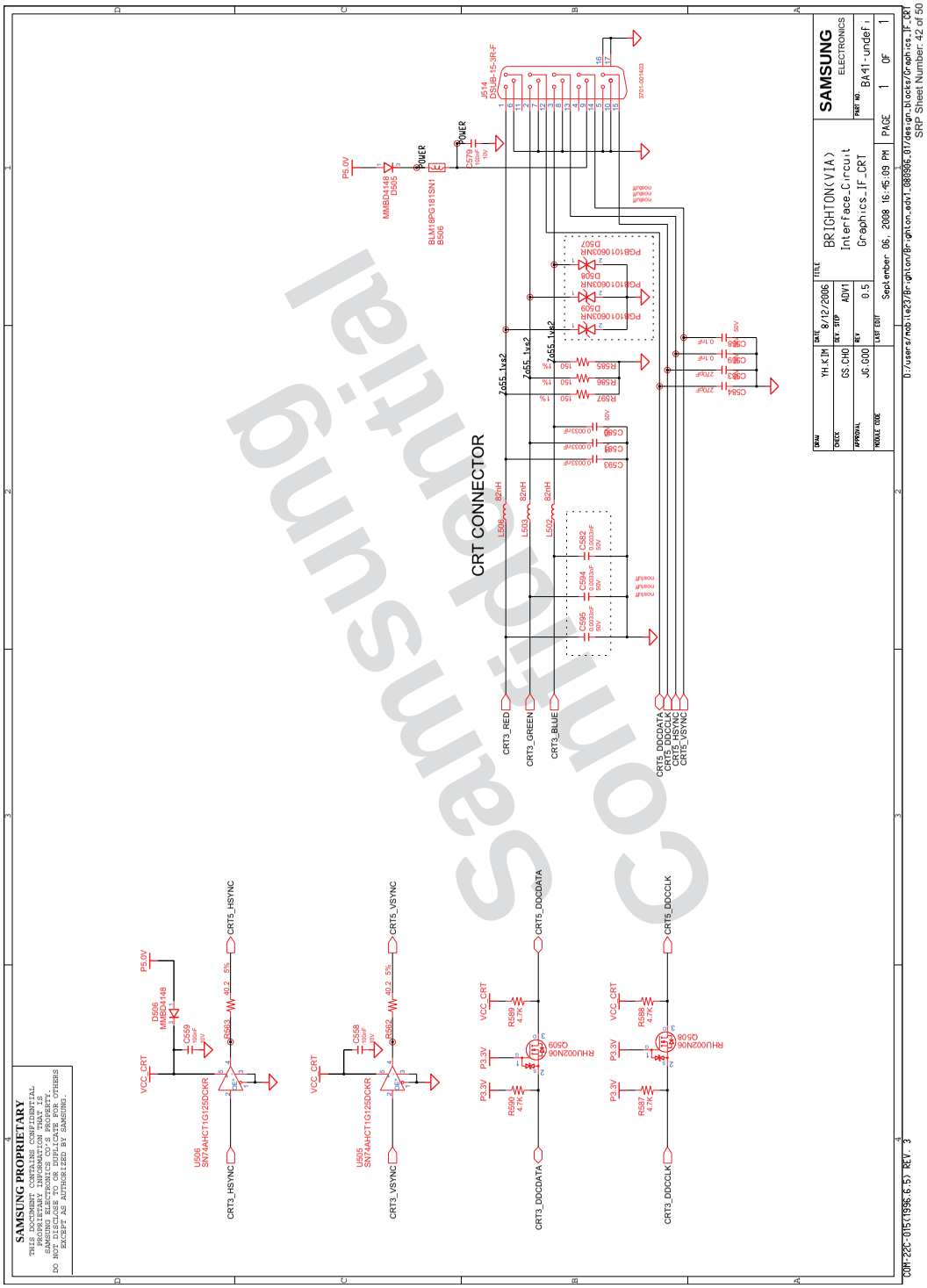

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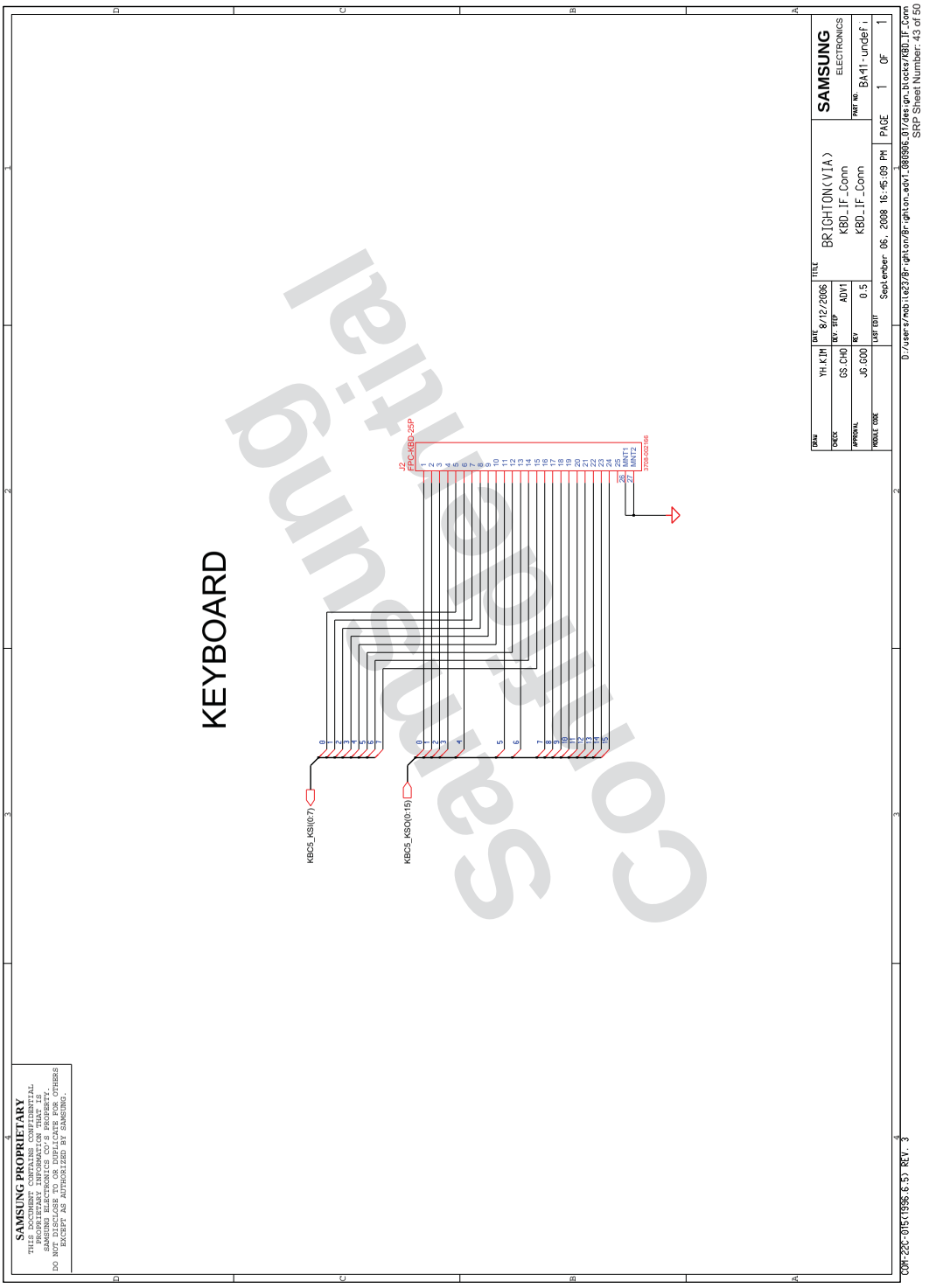

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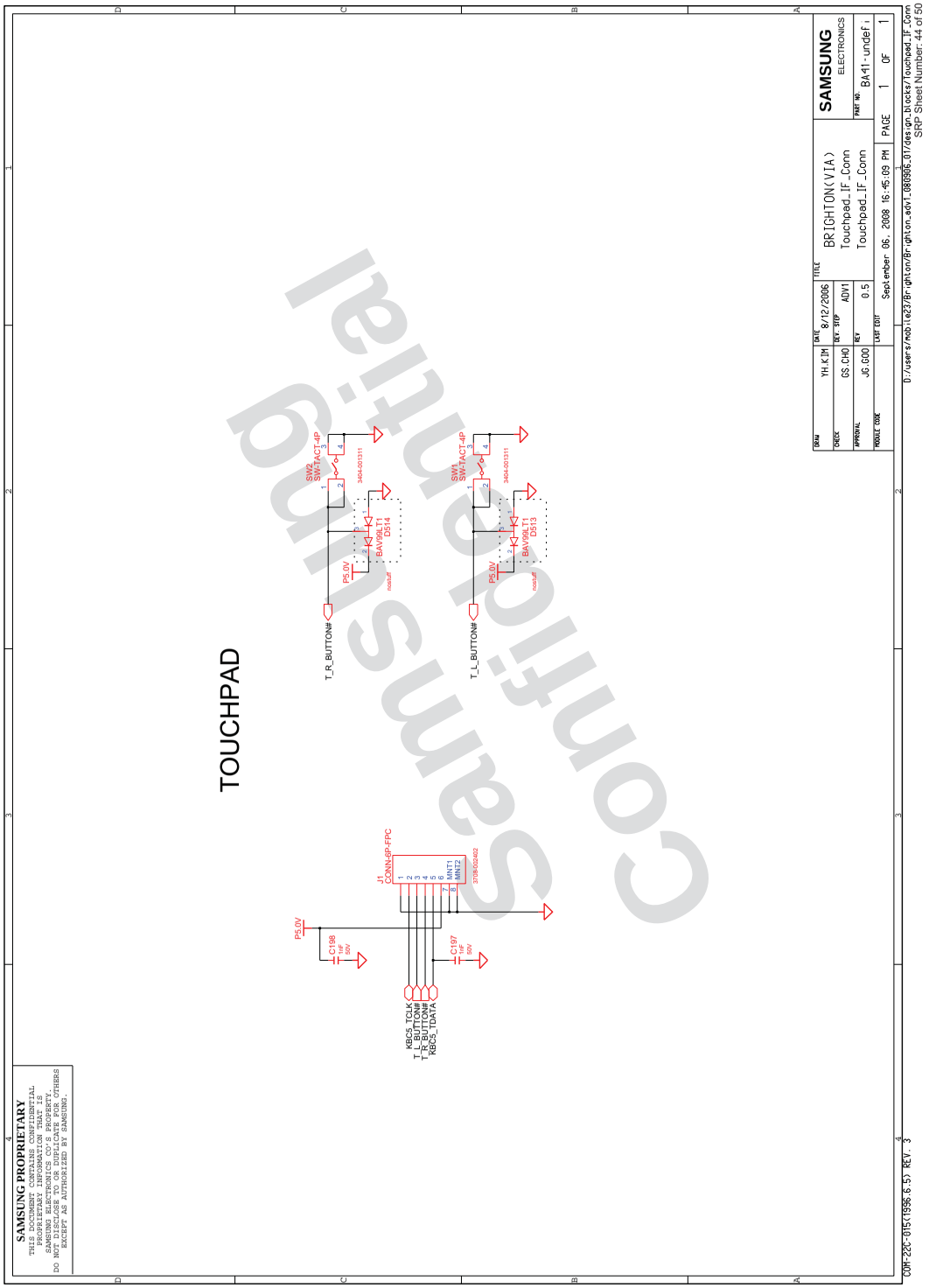
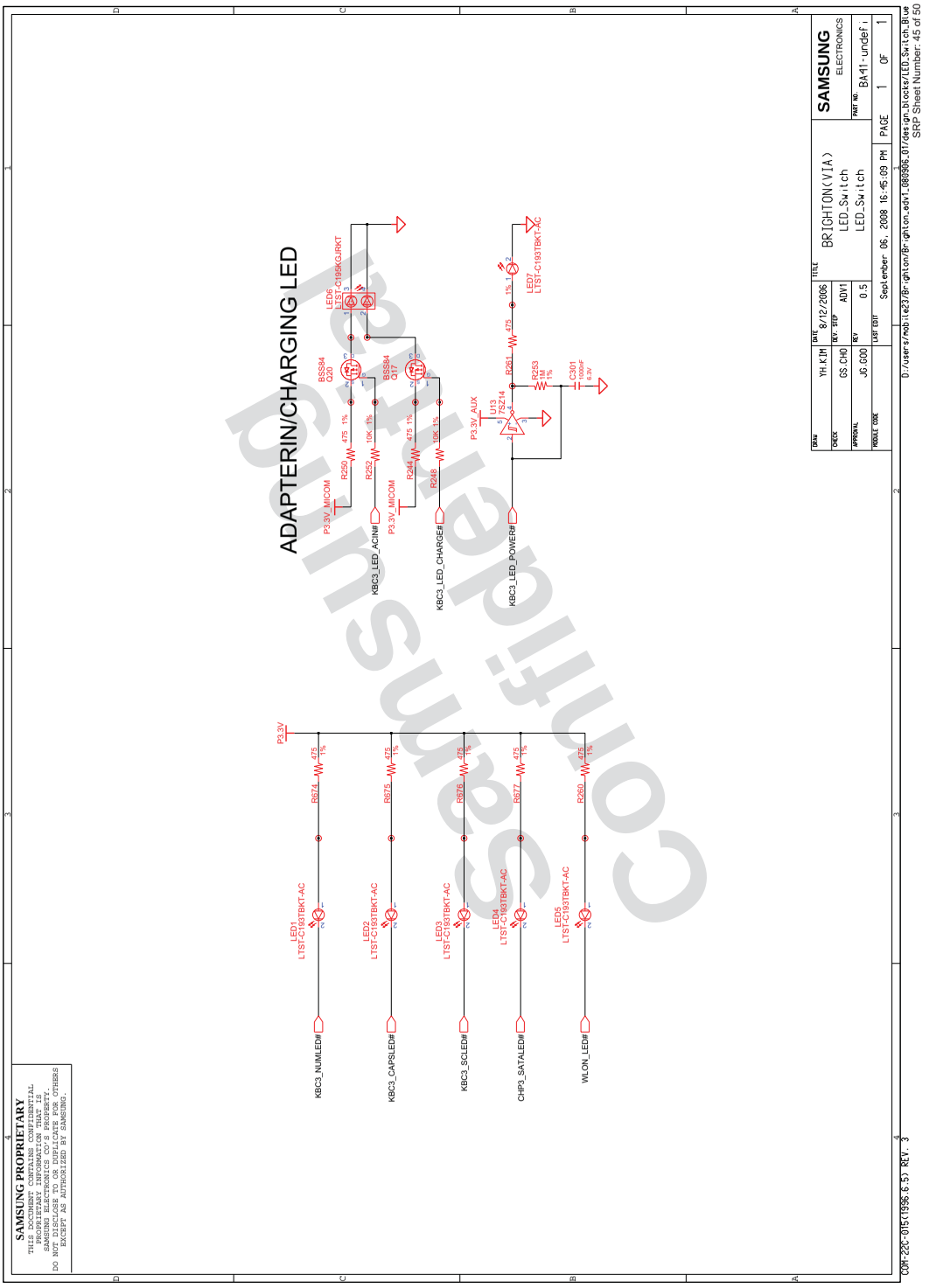
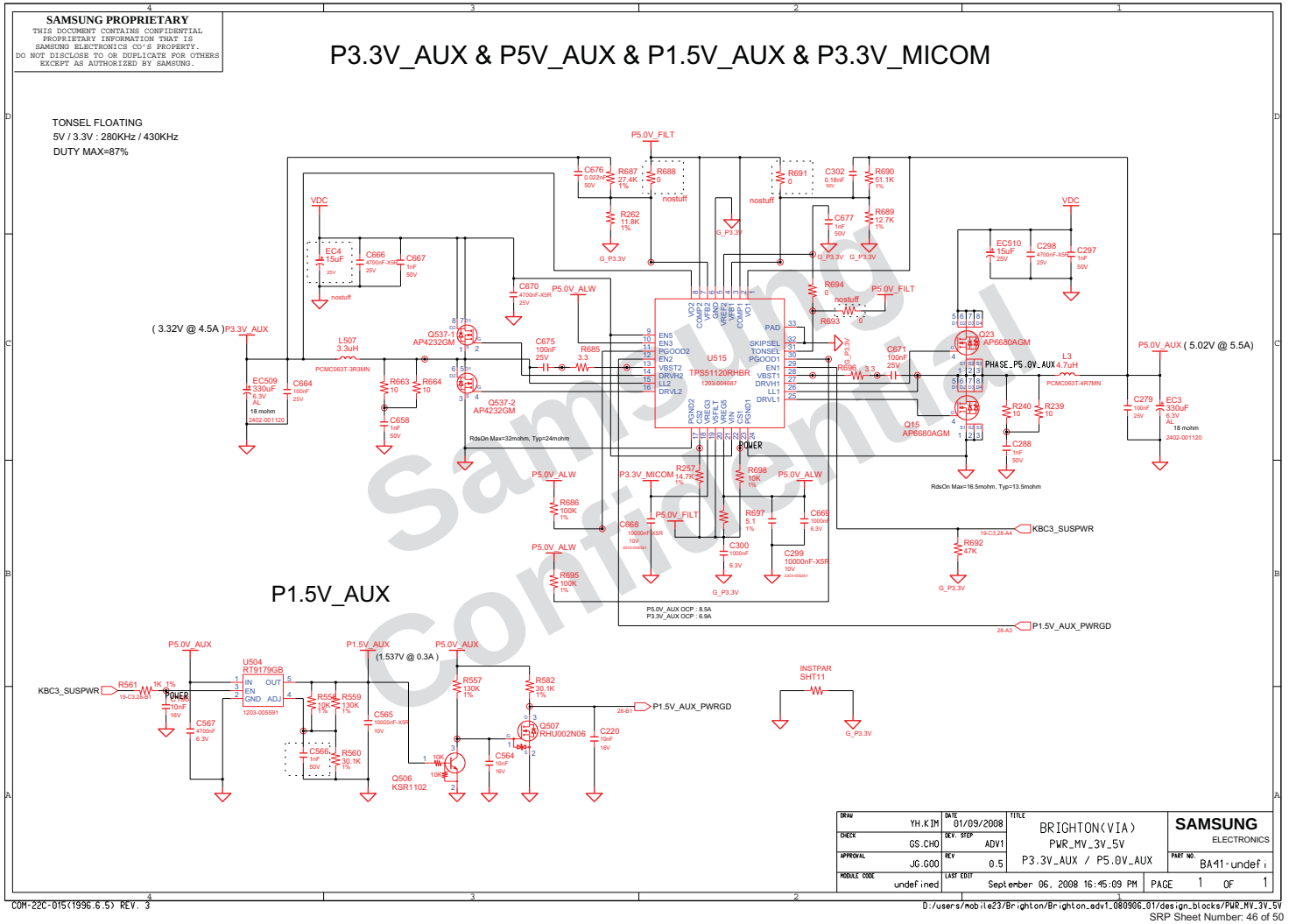


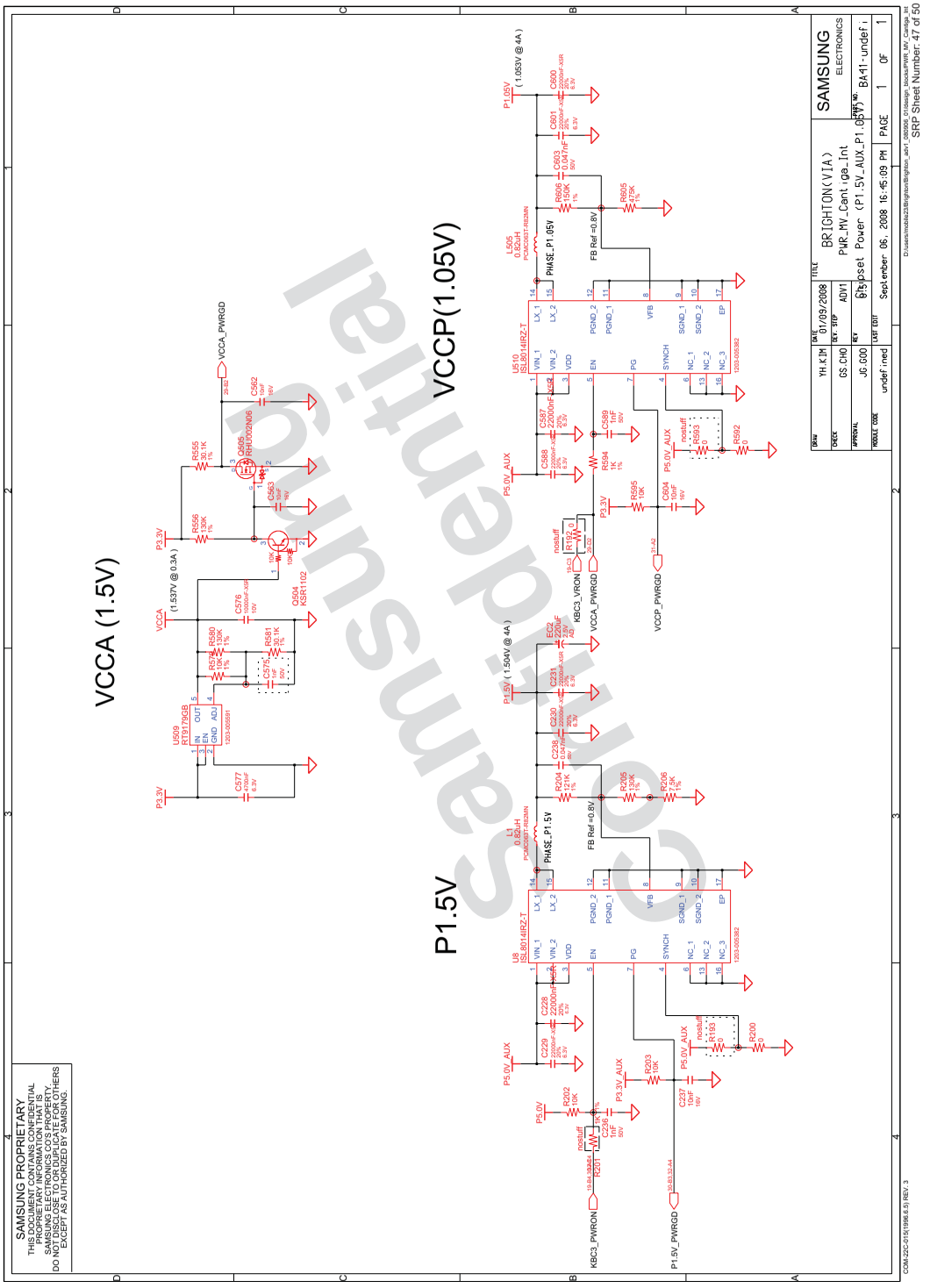
8. Block Diagram and Schematic



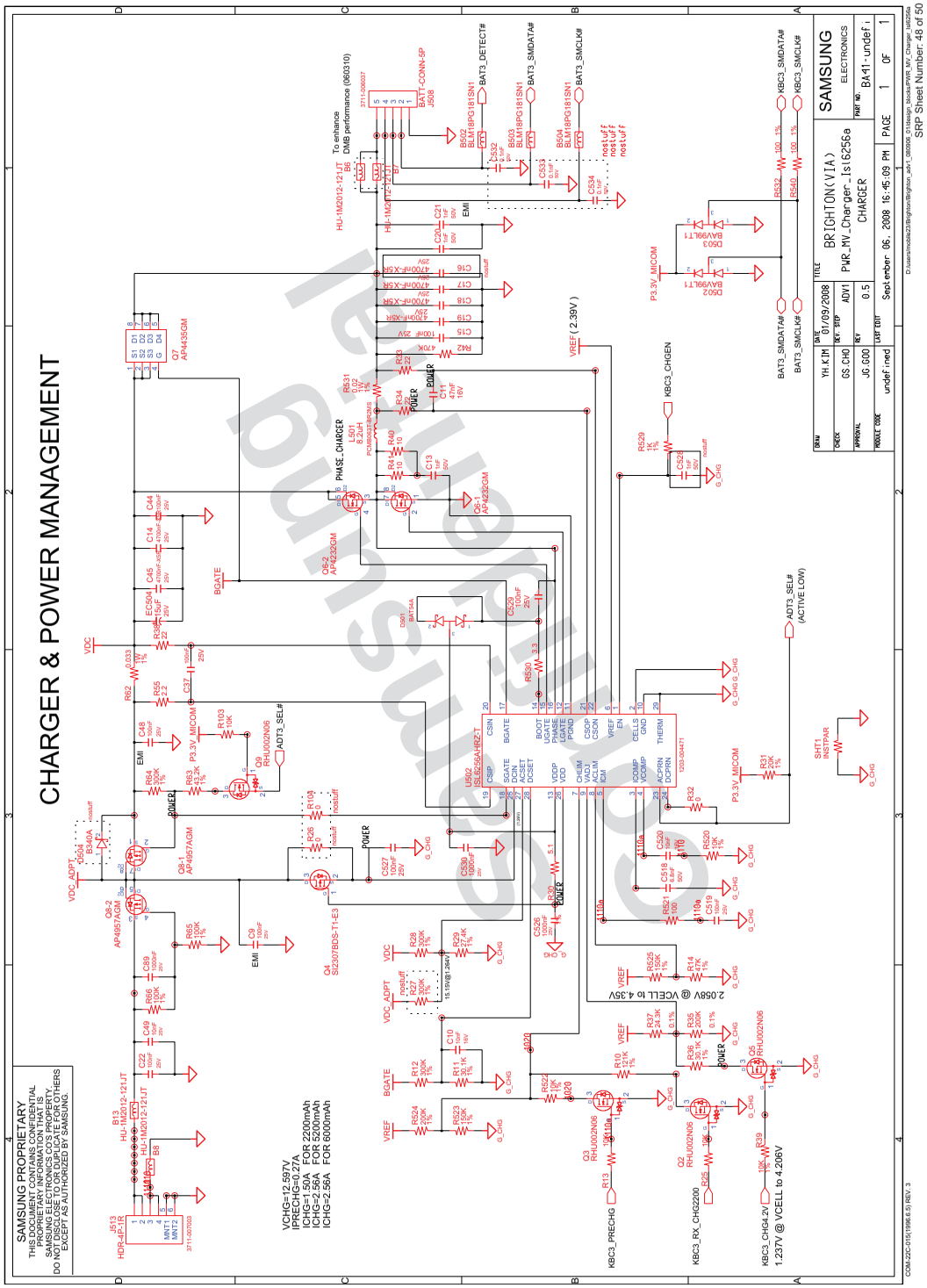
8. Block Diagram and Schematic



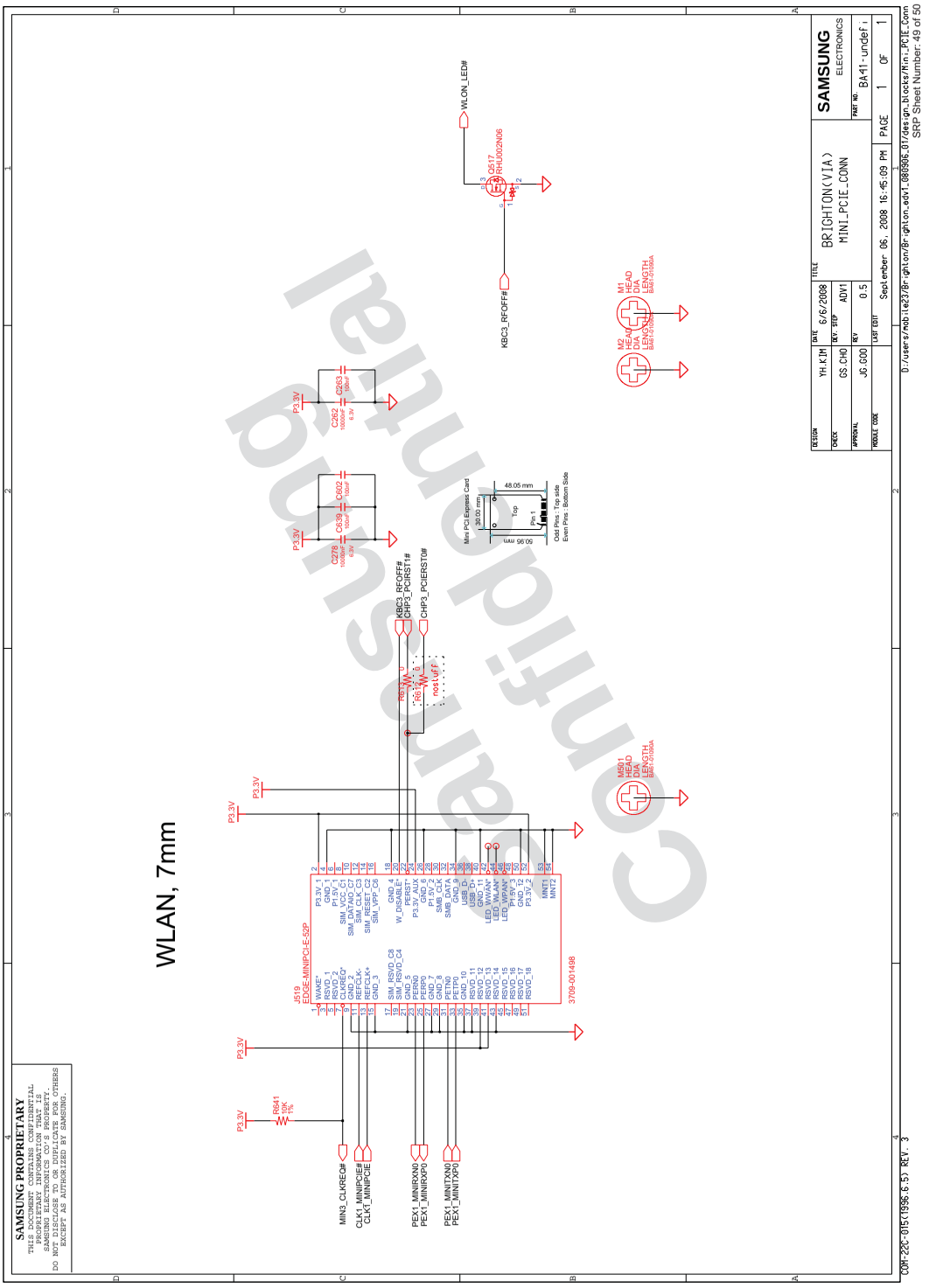
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic