

TORINO

PCB thickness: 1mm

CPU : INTEL YONAH-2M
Chip Set : INTEL 945GM & ICH7-M
Remarks : 2 Spindle

Model Name : TORINO
PBA Name : MAIN
PCB Code : BA41-00602A/3A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2006.1.23

DRAW	CHECK	APPROVAL
-	-	-

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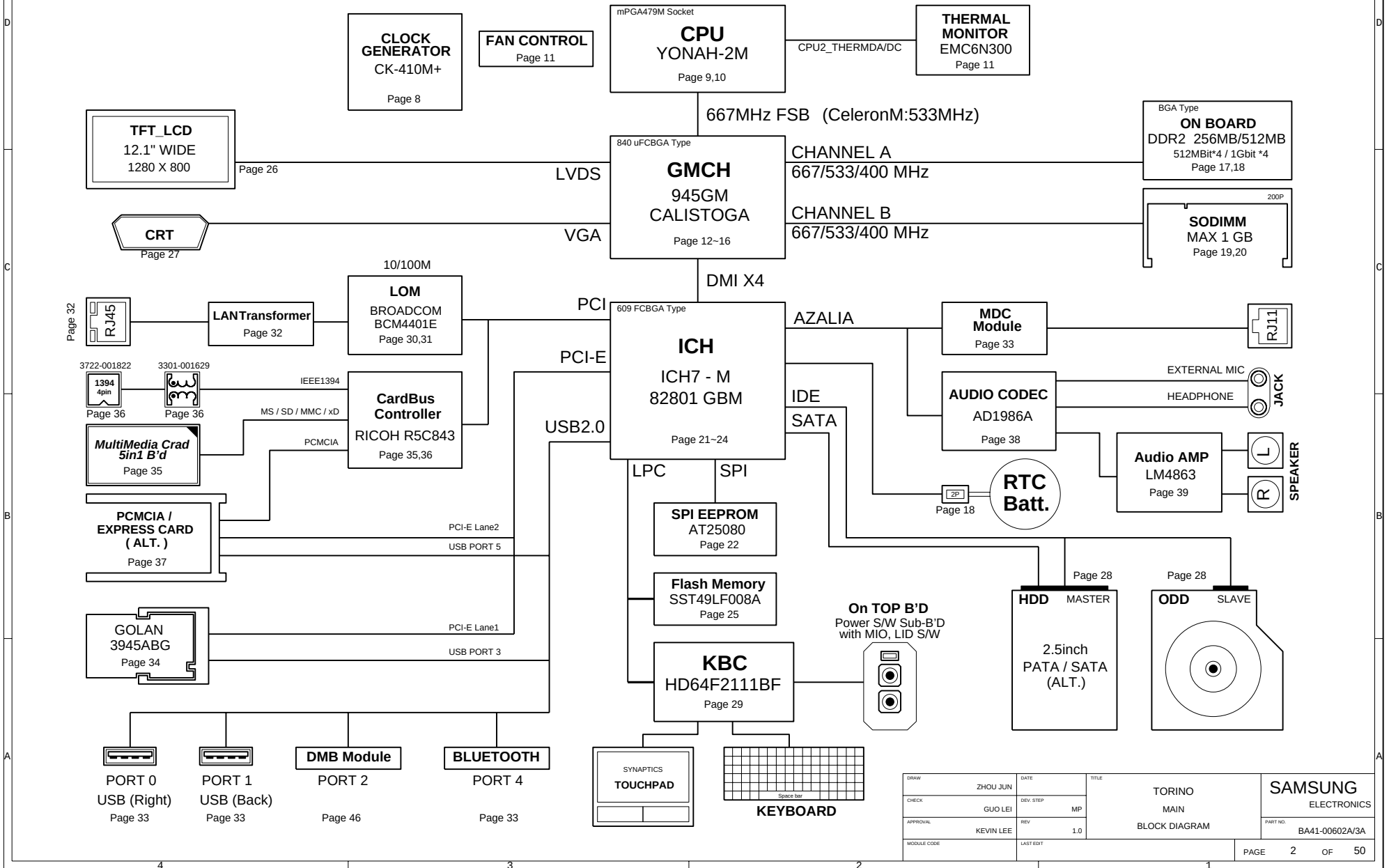
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DIAGRAM

DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP		COVER	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		CONTENTS	PART NO.
MODULE CODE		LAST EDIT				BA41-00602A/3A
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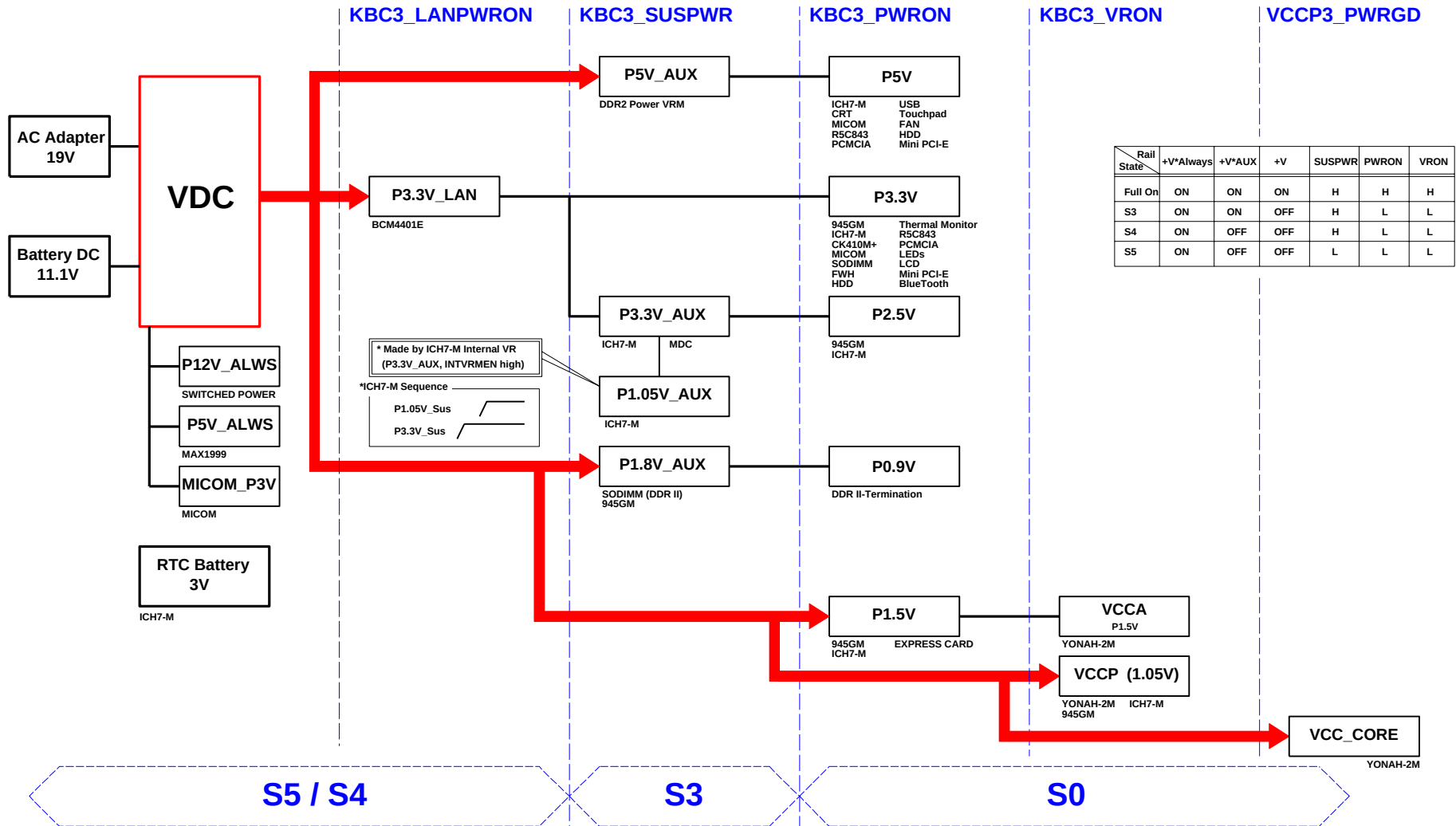
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OPERATION BLOCK DIAGRAM

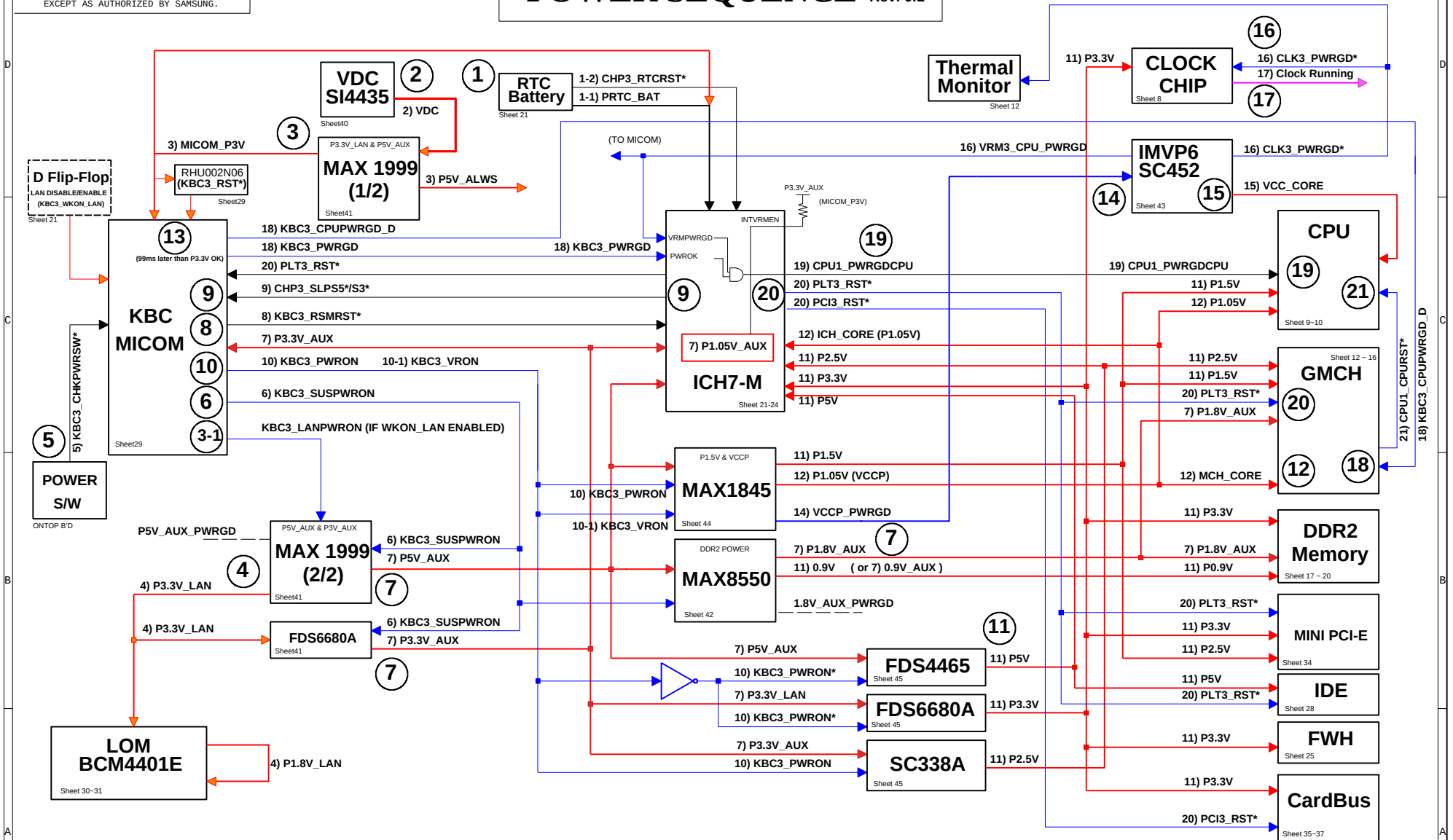


DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	MAIN	MAIN	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	BLOCK DIAGRAM		PART NO.
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POWER DIAGRAM



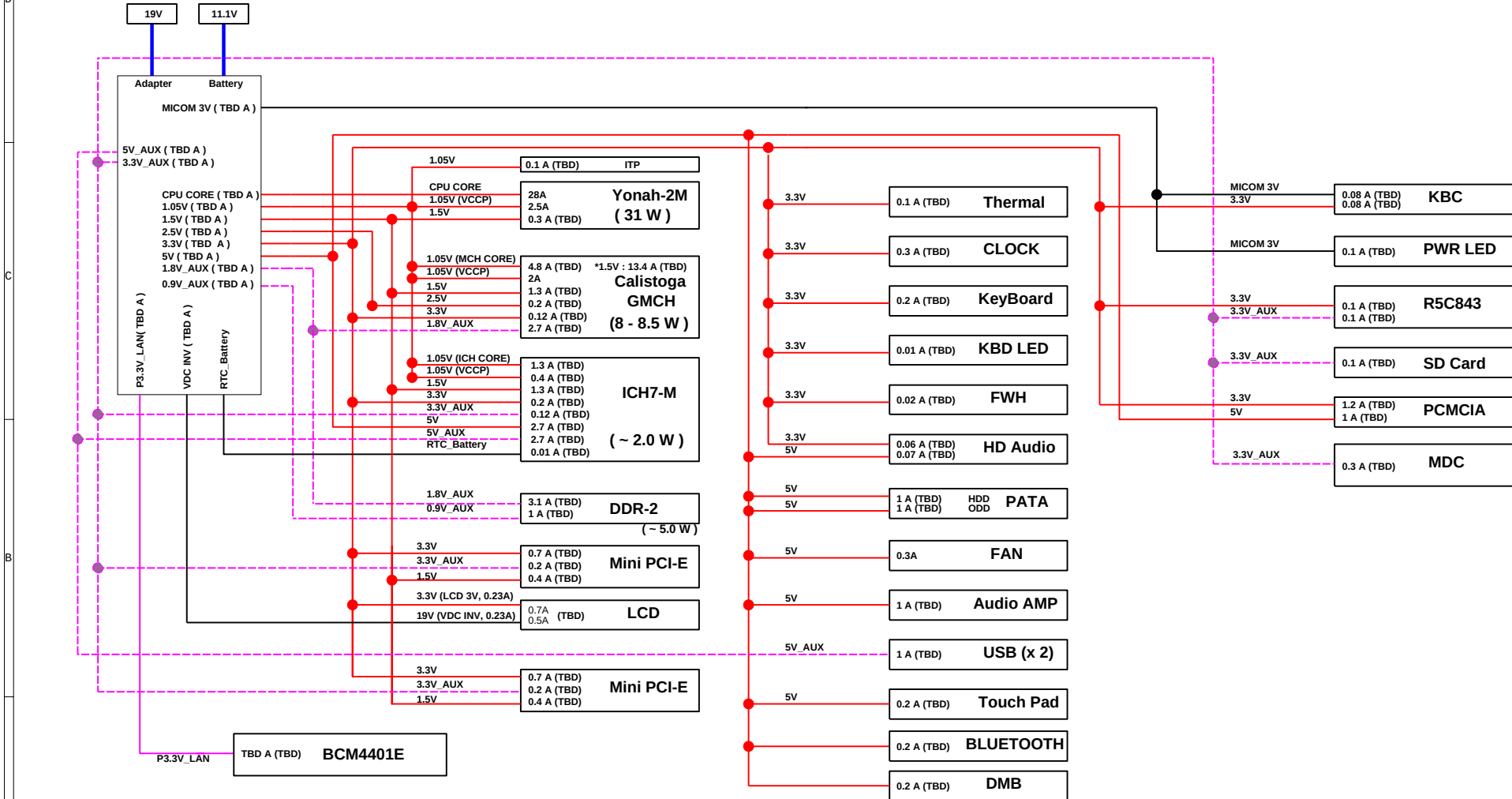
POWER SEQUENCE Rev. 0.1

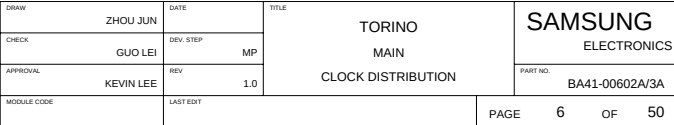


POWER RAILS ANALYSIS

Rev. 0.1

— S0 - S5
- - - S0 - S3
— OFF IN S3 - S5





BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for Processor (1.308-1.068V)
VTT	DOTAN/ALVISO Processor System Bus(PSB) Termination (1.05V) GMCH & ICH7 Core Voltage
P1.8V_AUX	1.8V power rail for DDR2 (off in S4-S5)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_LAN	3.3V power rail (Always On)
PRTC_BAT	3.0V power rail (ALWAYS ON)
MICOM_P3V	3.3V always on power rail for MICOM
P5V_ALWS	5V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
SODIMM1	1010 001X	A2h	-
CK-410M+ (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
BATTERY	0001 011X	16h	-
EMC6N300(CPU Thermal Sensor)	0101 111X	5Eh	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	DMB CARD
3	MINIPCI-E
4	BLUETOOTH
5	EXPRESS CARD
6	RESERVED
7	RESERVED

System Power States

- CHP3_SLP1S1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLP3S3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLP4S4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLP5S5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

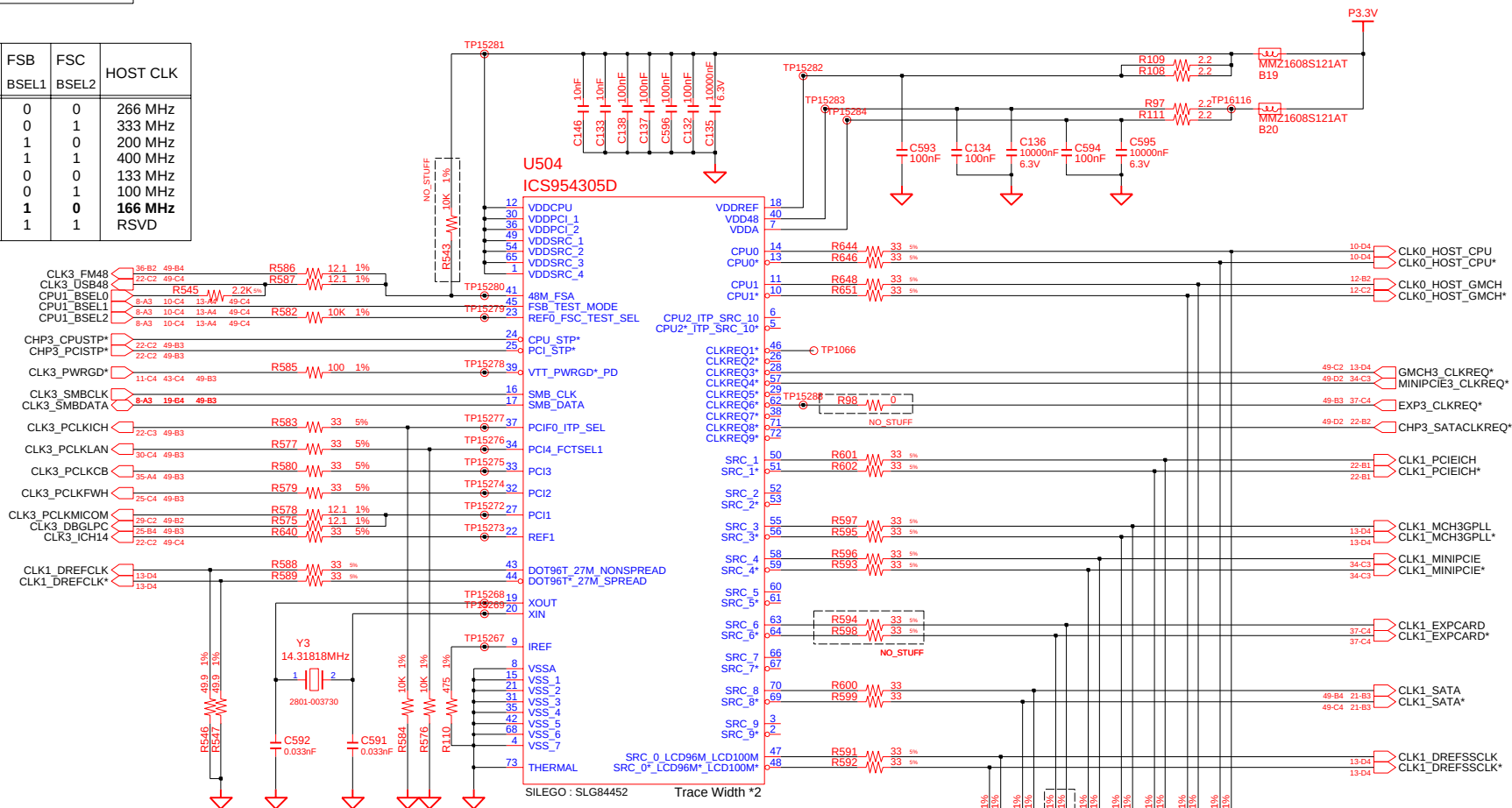
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0 0	1.0000 V	1 0 1 0 0 0 0 1	0.4875 V
0 0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0 1	0.9875 V	1 0 1 0 0 0 1 0	0.4750 V
0 0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 0 1 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 1 0 0	1.4625 V	0 1 0 1 0 0 1 1	0.9625 V	1 0 1 0 0 1 0 0	0.4500 V
0 0 0 0 1 0 0 0	1.4500 V	0 1 0 1 1 0 0 0	0.9500 V	1 0 1 0 1 0 0 1	0.4375 V
0 0 0 0 1 0 0 1	1.4375 V	0 1 0 1 1 0 0 1	0.9375 V	1 0 1 0 1 0 1 0	0.4250 V
0 0 0 0 1 0 1 0	1.4250 V	0 1 0 1 1 0 1 0	0.9250 V	1 0 1 0 1 0 1 1	0.4125 V
0 0 0 0 1 0 1 1	1.4125 V	0 1 0 1 1 0 1 1	0.9125 V	1 0 1 0 1 0 0 0	0.4000 V
0 0 0 1 0 0 0 0	1.4000 V	0 1 1 0 0 0 0 0	0.9000 V	1 0 1 0 1 0 0 1	0.3875 V
0 0 0 1 0 0 0 1	1.3875 V	0 1 1 0 0 0 0 1	0.8875 V	1 0 1 0 1 0 1 0	0.3750 V
0 0 0 1 0 0 1 0	1.3750 V	0 1 1 0 0 0 1 0	0.8750 V	1 0 1 0 1 0 1 1	0.3625 V
0 0 0 1 0 0 1 1	1.3625 V	0 1 1 0 0 0 1 1	0.8625 V	1 0 1 0 1 1 0 0	0.3500 V
0 0 0 1 0 1 0 0	1.3500 V	0 1 1 0 1 0 0 0	0.8500 V	1 0 1 0 1 1 0 1	0.3375 V
0 0 0 1 0 1 0 1	1.3375 V	0 1 1 0 1 0 0 1	0.8375 V	1 0 1 0 1 1 1 0	0.3250 V
0 0 0 1 0 1 1 0	1.3250 V	0 1 1 0 1 0 1 0	0.8250 V	1 0 1 0 1 1 1 1	0.3125 V
0 0 0 1 0 1 1 1	1.3125 V	0 1 1 0 1 0 1 1	0.8125 V	1 1 0 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0 0	0.8000 V	1 1 0 0 0 0 0 1	0.2875 V
0 0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 0 1	0.7875 V	1 1 0 0 0 0 1 0	0.2750 V
0 0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 0 1 0	0.7750 V	1 1 0 0 0 0 1 1	0.2625 V
0 0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 0 1 1	0.7625 V	1 1 0 0 0 1 0 0	0.2500 V
0 0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0 0	0.7500 V	1 1 0 0 0 1 0 1	0.2375 V
0 0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 0 1	0.7375 V	1 1 0 0 0 1 1 0	0.2250 V
0 0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 0 1 0	0.7250 V	1 1 0 0 0 1 1 1	0.2125 V
0 0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 0 1 1	0.7125 V	1 1 0 0 1 0 0 0	0.2000 V
0 0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0 0	0.7000 V	1 1 0 0 1 0 0 1	0.1875 V
0 0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 0 1	0.6875 V	1 1 0 0 1 0 1 0	0.1750 V
0 0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 0 1 0	0.6750 V	1 1 0 0 1 0 1 1	0.1625 V
0 0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 0 1 1	0.6625 V	1 1 0 0 1 1 0 0	0.1500 V
0 0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 0 0	0.6500 V	1 1 0 0 1 1 0 1	0.1375 V
0 0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 0 1	0.6375 V	1 1 0 0 1 1 1 0	0.1250 V
0 0 0 1 1 1 1 0	1.1250 V	1 0 0 0 0 1 1 0	0.6250 V	1 1 0 0 1 1 1 1	0.1125 V
0 0 0 1 1 1 1 1	1.1125 V	1 0 0 0 0 1 1 1	0.6125 V	1 1 0 0 0 0 0 0	0.1000 V
0 0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 0 0 0	0.6000 V	1 1 0 0 0 0 0 1	0.0875 V
0 0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 0 1	0.5875 V	1 1 0 0 0 0 1 0	0.0750 V
0 0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 1 0	0.5750 V	1 1 0 0 0 0 1 1	0.0625 V
0 0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 0 1 1	0.5625 V	1 1 0 0 0 1 0 0	0.0500 V
0 0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0 0	0.5500 V	1 1 0 0 0 1 0 1	0.0375 V
0 0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0 1	0.5375 V	1 1 0 0 0 1 1 0	0.0250 V
0 0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1 0	0.5250 V	1 1 0 0 0 1 1 1	0.0125 V
0 0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1 1	0.5125 V	1 1 0 0 1 1 0 0	0.0000 V
		1 0 0 0 1 0 0 0	0.5000 V	1 1 0 0 1 1 0 1	0.0000 V
				1 1 0 0 1 1 1 0	0.0000 V
				1 1 0 0 1 1 1 1	0.0000 V
				1 1 0 0 1 1 0 0	0.0000 V
				1 1 0 0 1 1 0 1	0.0000 V
				1 1 0 0 1 1 1 0	0.0000 V
				1 1 0 0 1 1 1 1	0.0000 V
				1 1 0 0 1 1 0 0	0.0000 V
				1 1 0 0 1 1 0 1	0.0000 V
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				1 1 0 0 1 1 1 1	0.0000 V
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				1 1 0 0 1 1 1 1	0

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CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
➡	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

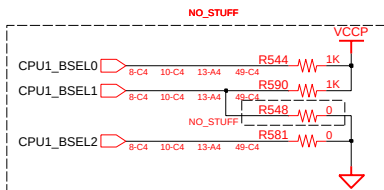
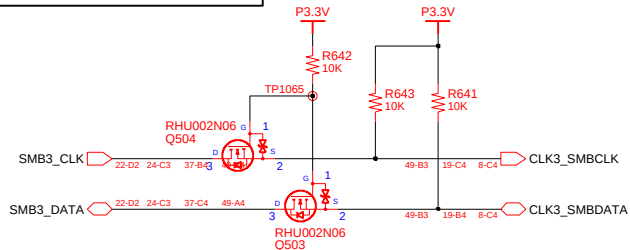


FCTSEL1	Pin43	Pin44	Pin47	Pin48
0	DOT96T	DOT96C	LCD100/96T	LCD100/96C
1	27MHz	27MHz	SRC0_T	SRC0_C

Place 14.318MHz within
500mils of Clock chip

CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SLG8LP455
	CY28447

Place Termination
close to CK-410M+



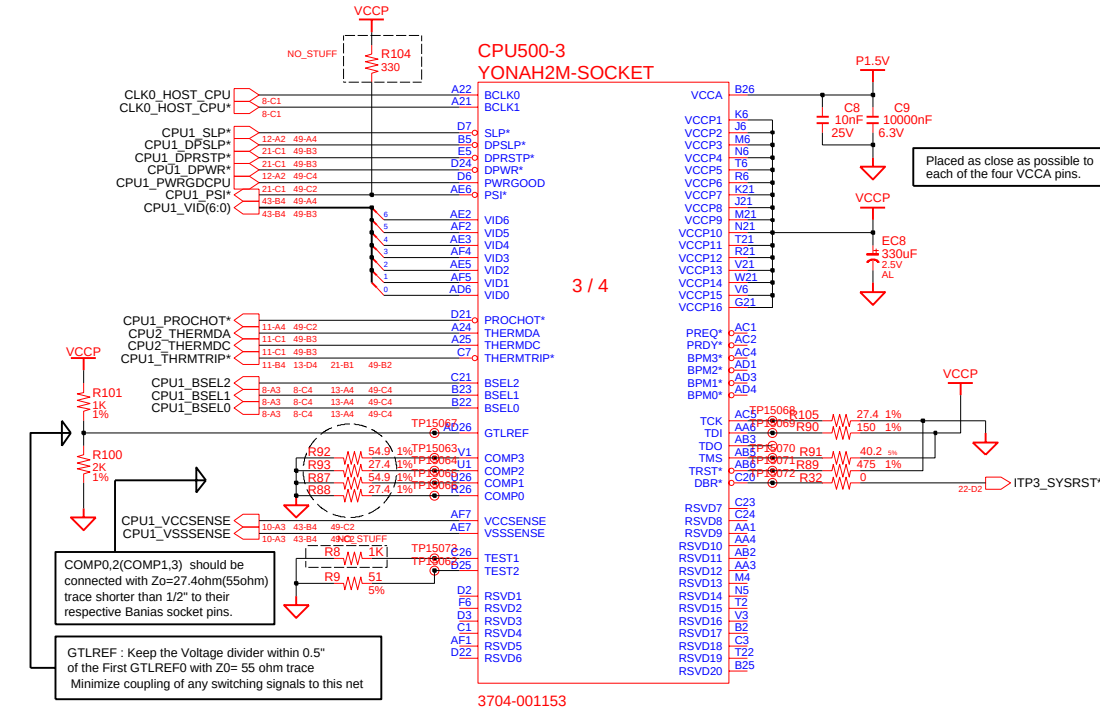
DRAW	ZHOU JUN	DATE		TORINO MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP		
APPROVAL	KEVIN LEE	REV	1.0		
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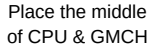
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CPU SOCKET : YONAH-2M



A

Place near to
DDR2 SODIMM



Line Width = 20 mil

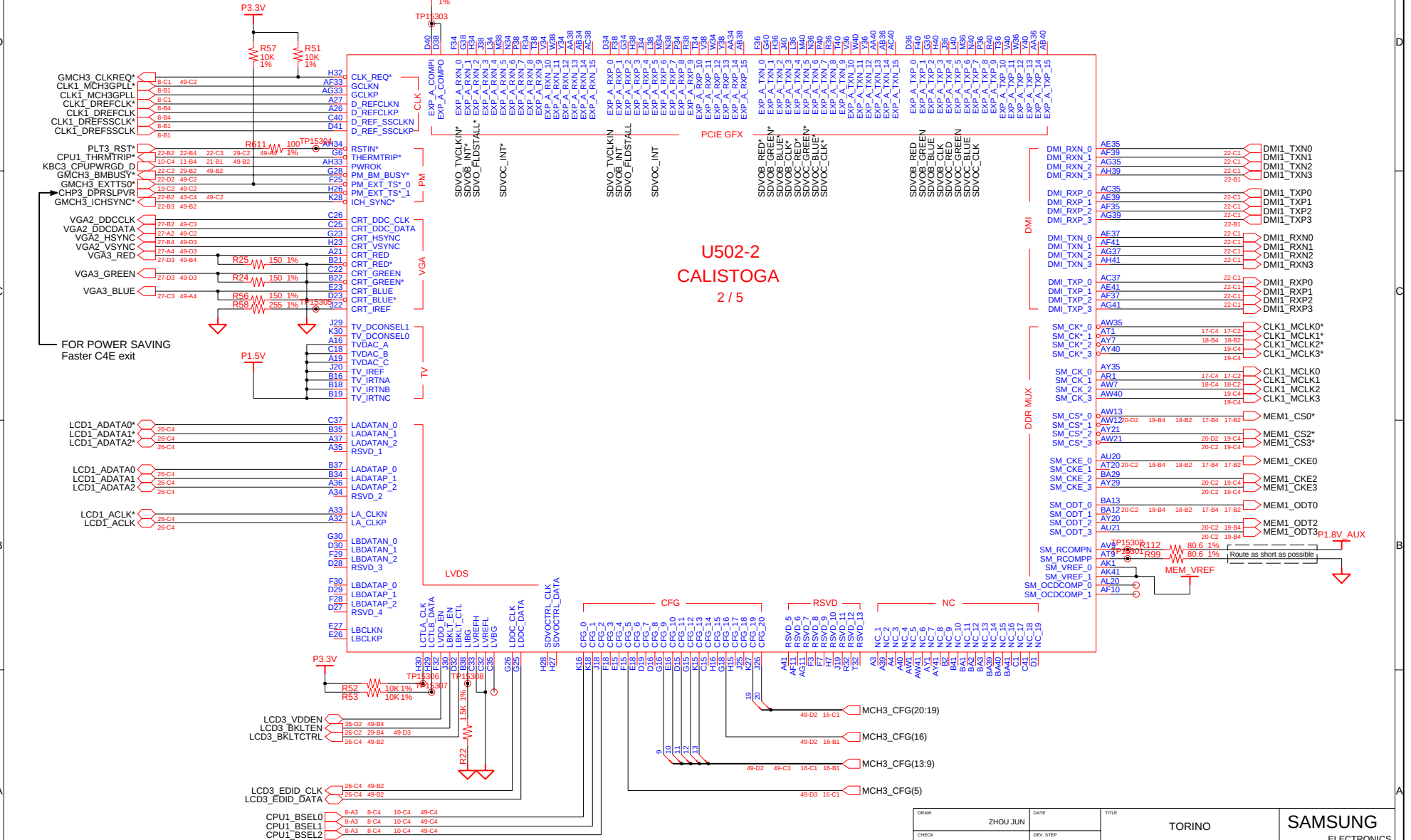


DRAW		DATE		TITLE TORINO MAIN THERMAL MONITOR		SAMSUNG ELECTRONICS	
CHECK		DEV. STEP					
APPROVAL		REV				PART NO.	
ZHOU JUN		MP		1.0		BA41-00602A/3A	
KEVIN LEE		1.0					
MODULE CODE		LAST EDIT				PAGE 11 OF 50	

[illegible]

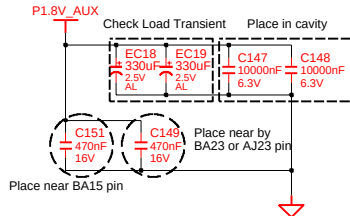
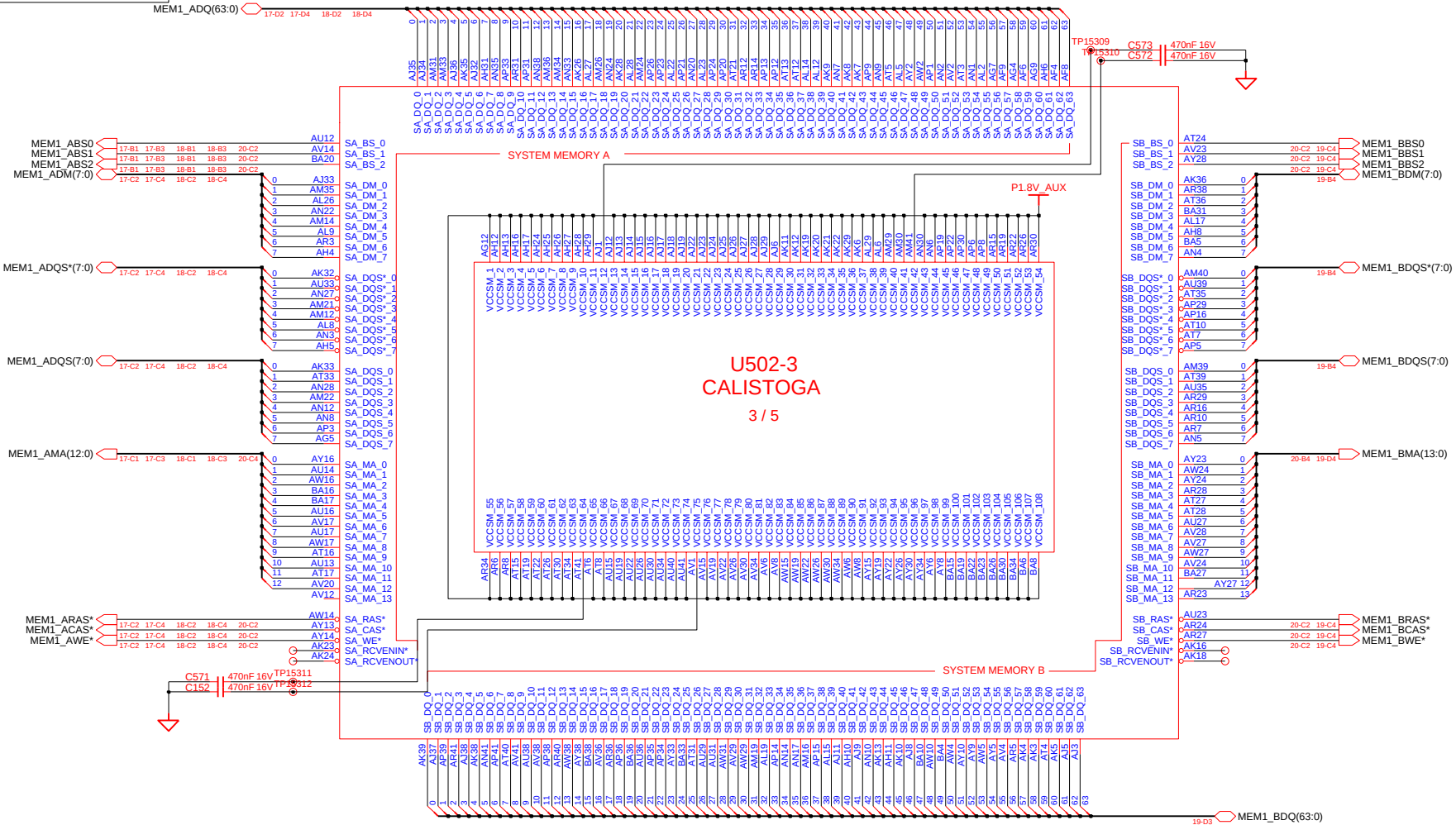
DRAW	ZHOU JUN	DATE	TITLE TORINO MAIN 945GM(1)	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP			MP
APPROVAL	KEVIN LEE	REV			1.0
MODULE CODE		LAST EDIT			
			PAGE	12 OF 50	

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DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	MAIN	945GM(2)	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT				BA41-00602A/3A
PAGE 13 OF 50						

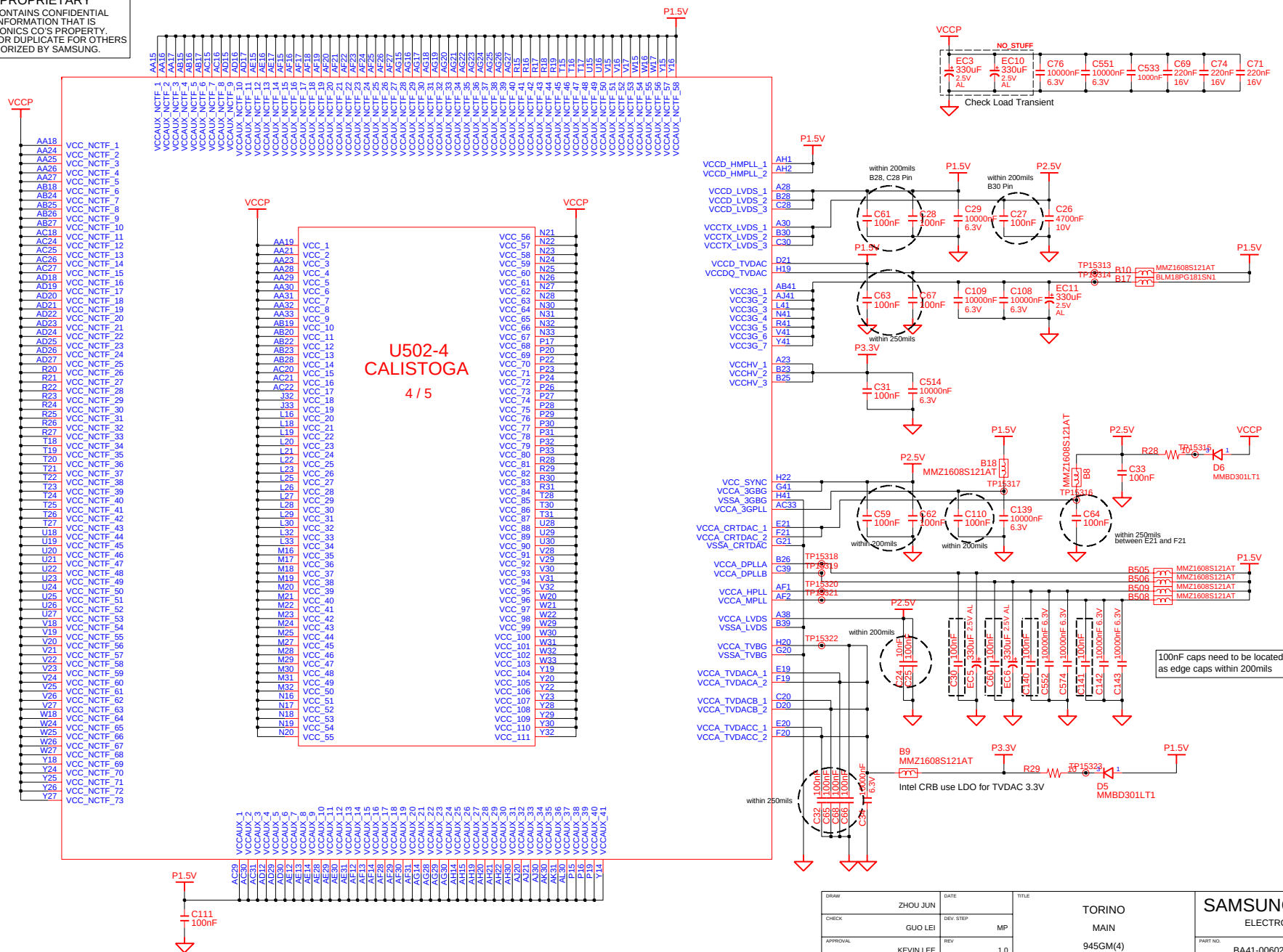
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Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

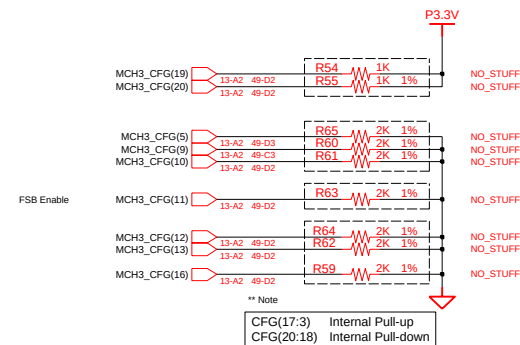
DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	MAIN	945GM(3)	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT				BA41-00602A/3A
						PAGE 14 OF 50

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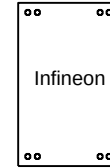
DRAW		DATE		TITLE		TORINO MAIN 945GM(4)		SAMSUNG ELECTRONICS	
CHECK		DEV. STEP							
MP		REV							
APPROVAL		KEVIN LEE		1.0		PART NO.		BA41-00602A/3A	
MODULE CODE		LAST EDIT				PAGE		15 OF 50	

** Note *POCAFEB-10 Only (Remove in MP Model)		
Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-11 (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only (def.)	SDVO and PCIE X1 Simultaneously

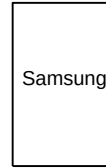


CFG(17:3)	Internal Pull-up
CFG(20:18)	Internal Pull-down

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with 8 dummy-ball
92-BALL Package

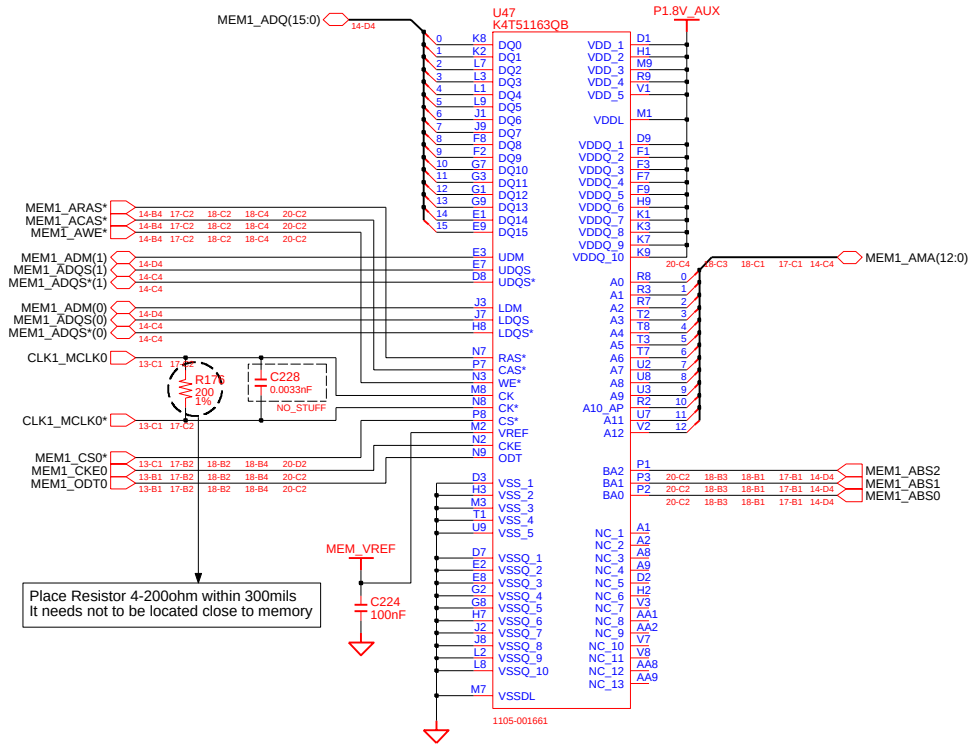


without dummy-ball
84-BALL Package

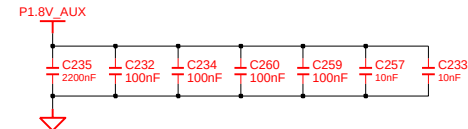
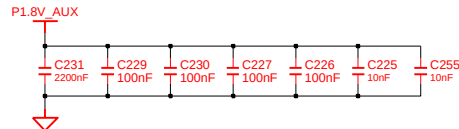
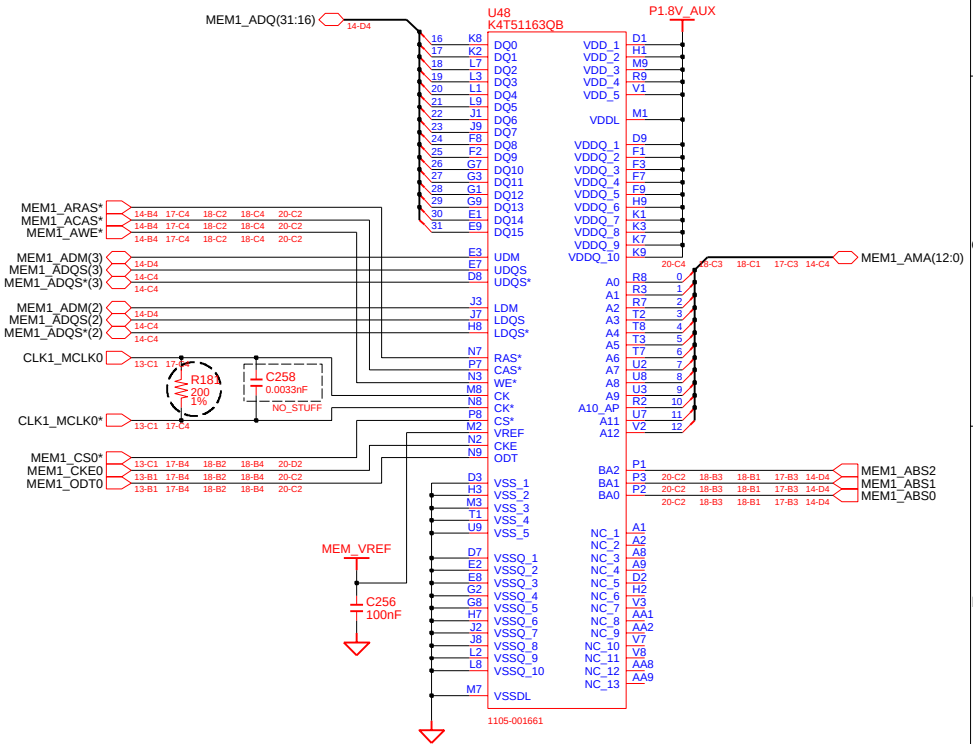
DDR2 ON BOARD MEMORY

- 1Gbit DDR2-667MHz x16 I/O
- SAMSUNG: K4T1G044QA-ZCE6
- 1Gbit DDR2-533MHz x16 I/O
- SAMSUNG: K4T1G044QA-ZCD5
- INFINEON: HYB18T1G160AF-3.7

D0

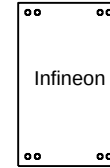


D1

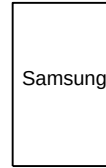


DRAW	ZHOU JUN	DATE		TITLE	TORINO MAIN ON B'D MEMORY(1)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP			PART NO. BA41-00602A/3A
APPROVAL	KEVIN LEE	REV	1.0			PAGE 17 OF 50
MODULE CODE		LAST EDIT				

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with 8 dummy-ball
92-BALL Package

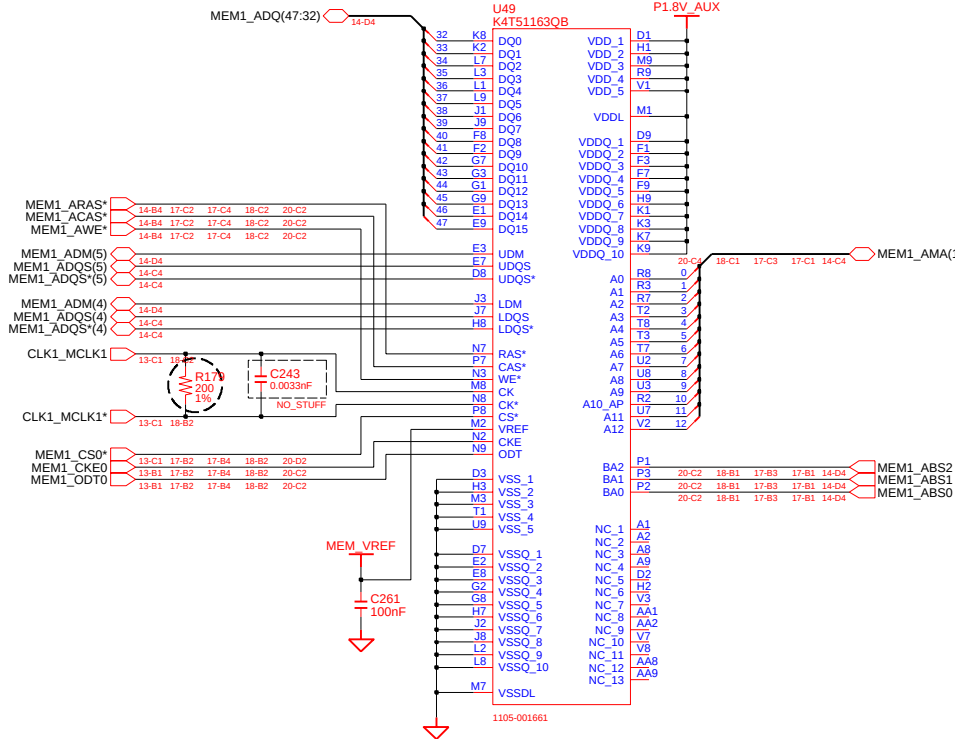


without dummy-ball
84-BALL Package

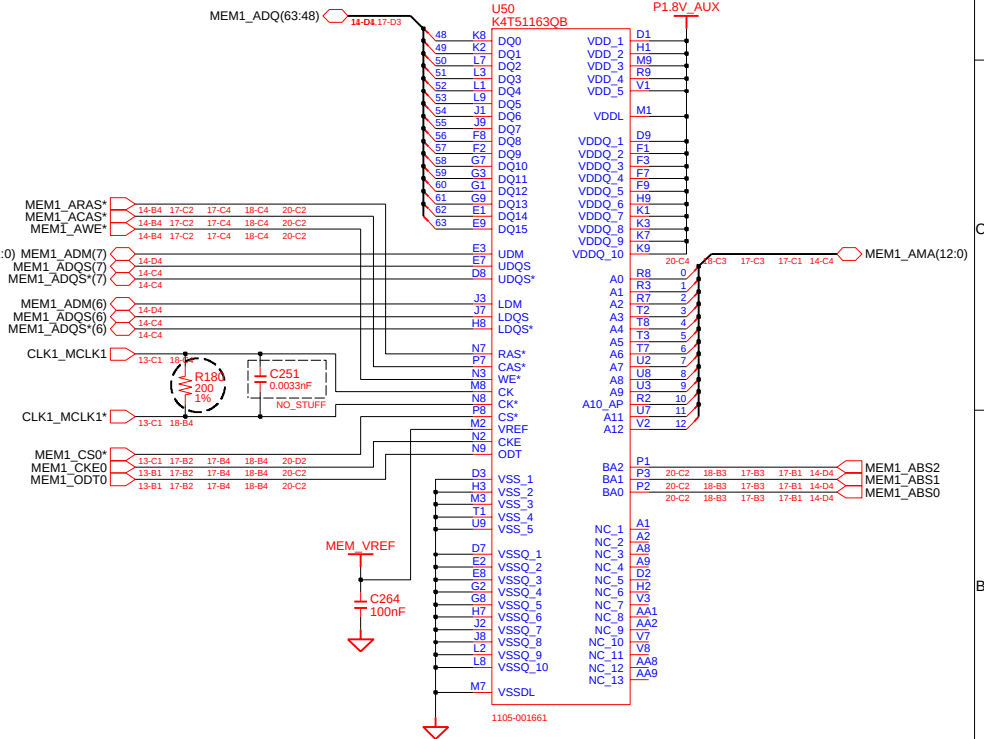
DDR2 ON BOARD MEMORY

- 1Gbit DDR2-667MHz x16 I/O
- SAMSUNG: K4T1G044QA-ZCE6
- 1Gbit DDR2-533MHz x16 I/O
- SAMSUNG: K4T1G044QA-ZCD5
- INFINEON: HYB18T1G160AF-3.7

D2

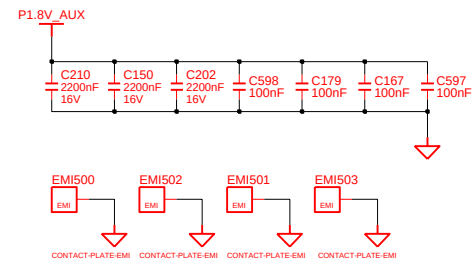
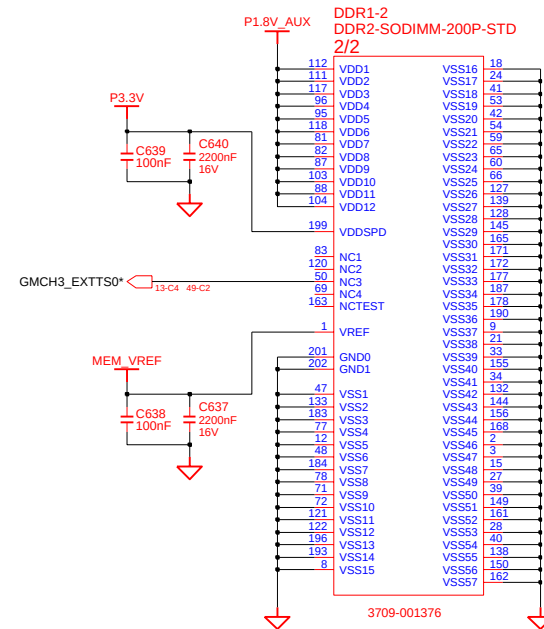
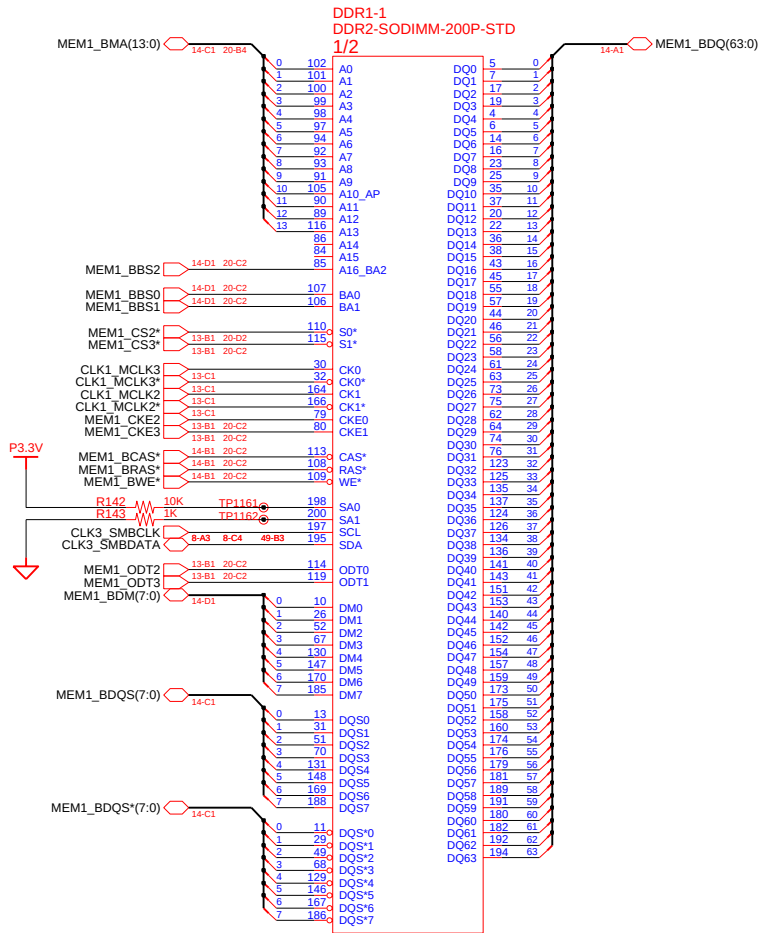


D3



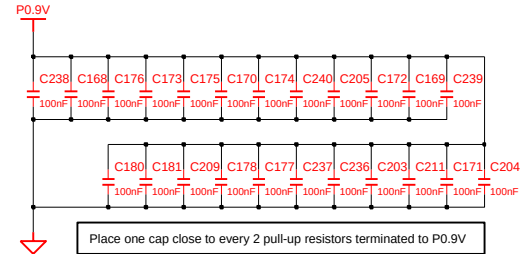
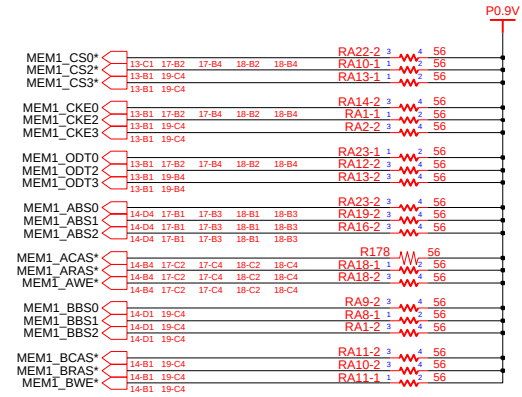
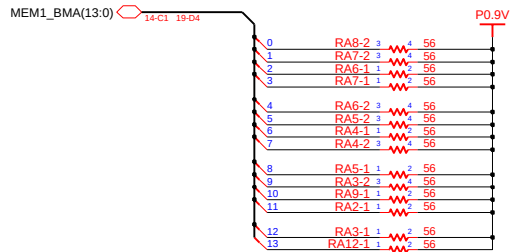
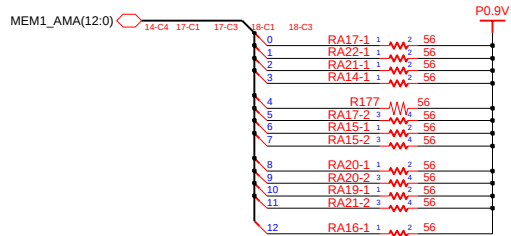
DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	MAIN	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0	ON B'D MEMORY(2)	PART NO.	BA41-00602A/3A
MODULE CODE		LAST EDIT			PAGE	18 OF 50

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DRAW	ZHOU JUN	DATE		TITLE	TORINO MAIN	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP			
APPROVAL	KEVIN LEE	REV	1.0	DDR2 SODIMM SOCKET		PART NO. BA41-00602A/3A
MODULE CODE		LAST EDIT				PAGE 19 OF 50

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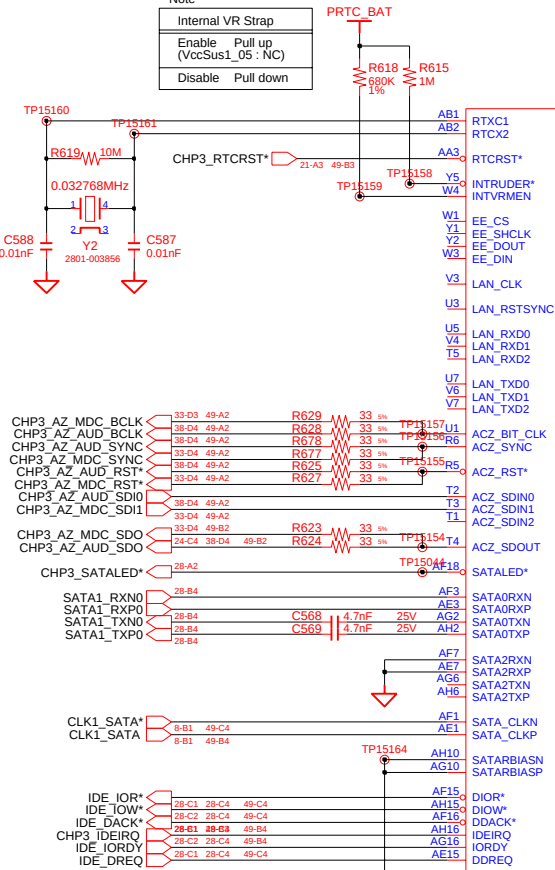
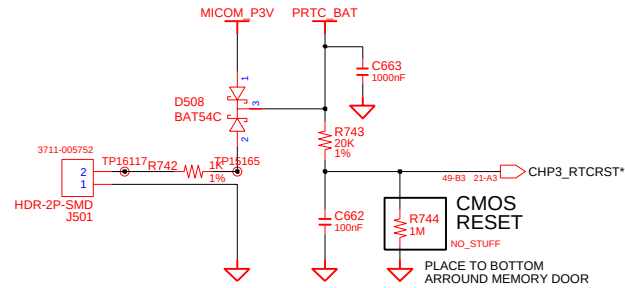


DRAW	ZHOU JUN	DATE		TITLE		SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	TORINO		ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	MAIN		PART NO.
MODULE CODE		LAST EDIT		DDR2 TERMINATION		BA41-00602A/3A
PAGE 20 OF 50						

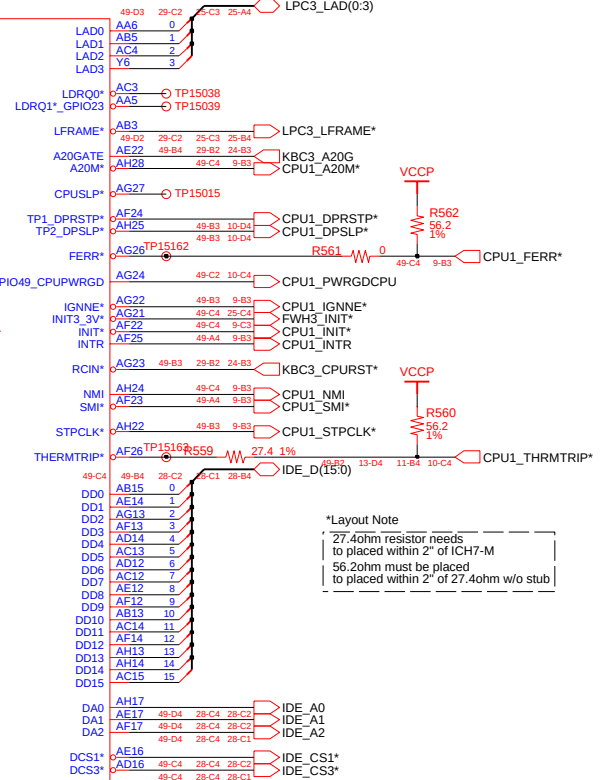
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**Note

Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down

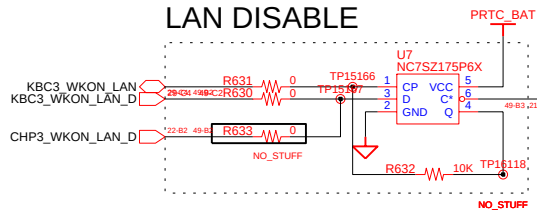


U40-1
ICH7-M
1 / 5

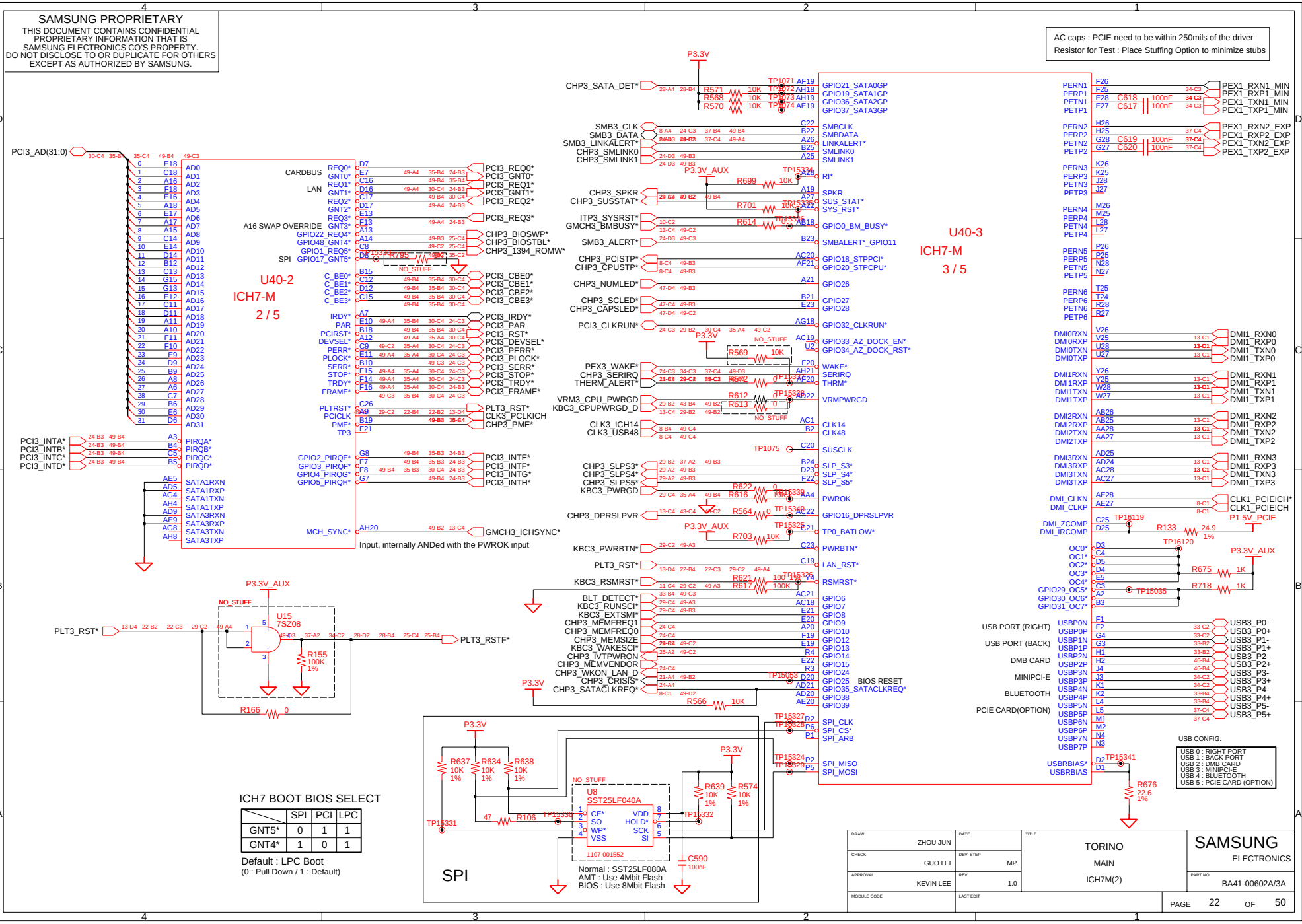


*Layout Note
27.4ohm resistor needs
to be placed within 2" of ICH7-M
56.2ohm must be placed
to be placed within 2" of 27.4ohm w/o stub

LAN DISABLE



DRAW	ZHOU JUN	DATE		TITLE	TORINO	SAMSUNG
CHECK	GUO LEI	DEV. STEP	MP	MAIN	ICH7M(1)	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT				BA41-00602A/3A
PAGE 21 OF 50						



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AC caps : PCIE need to be within 250mils of the driver
Resistor for Test : Place Stuffed Option to minimize stubs

PCB AD(31:0)

U40-2
ICH7-M
2 / 5

U40-3
ICH7-M
3 / 5

U5
75S208

U8
SST25LF040A

U9
SST25LF080A

U10
SST25LF080A

U11
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U12
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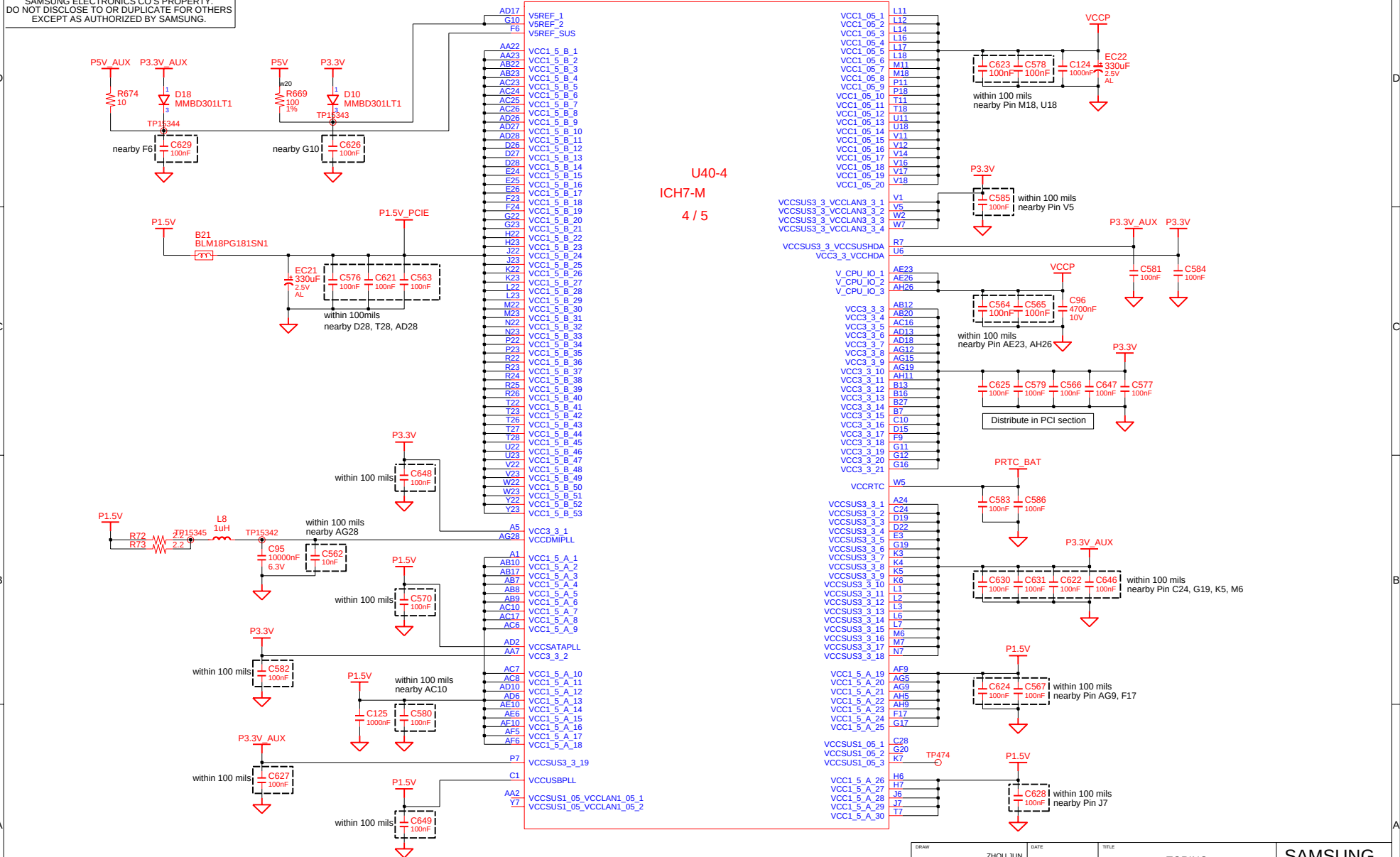
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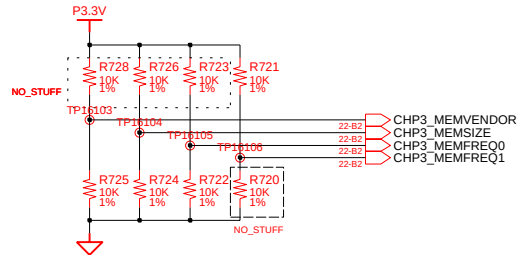
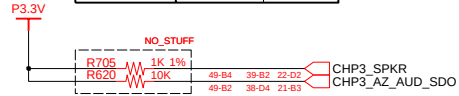
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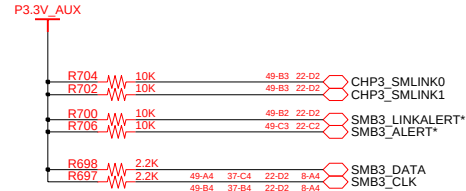
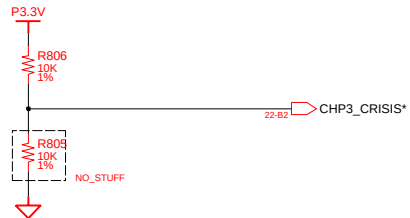
ICH7-M Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
AC97_SDOUT	Safe Mode	TBD

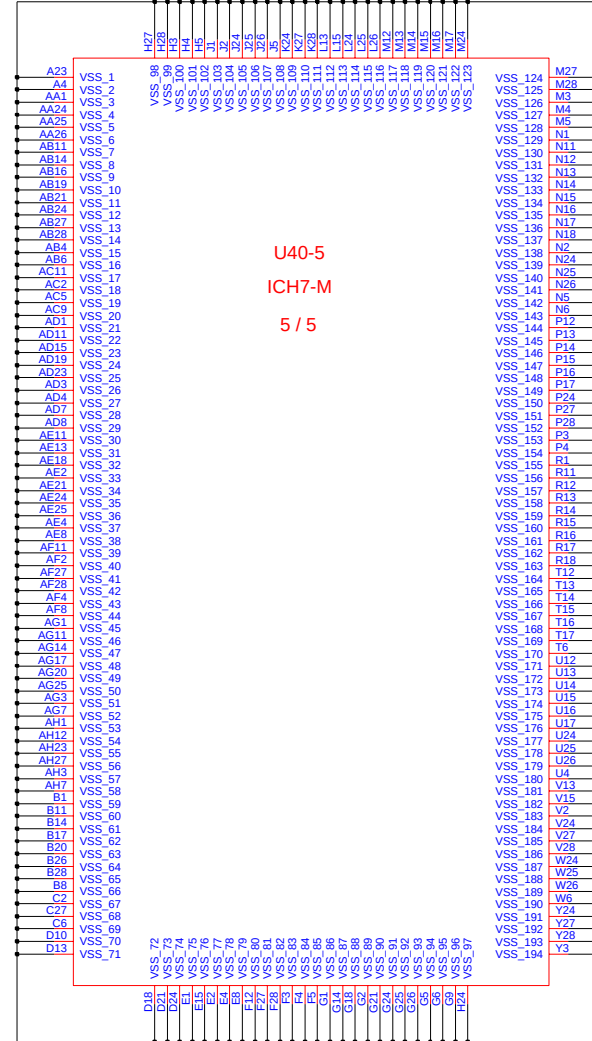
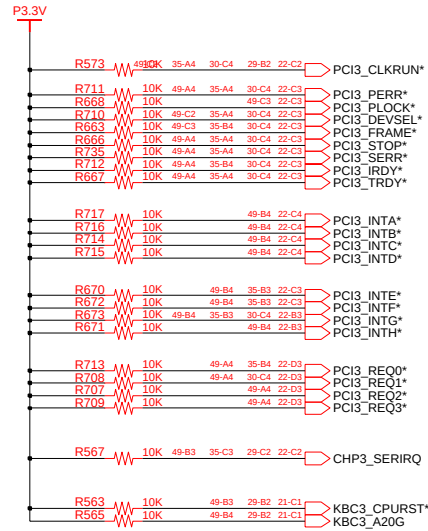


On-Board Memory Type Straps

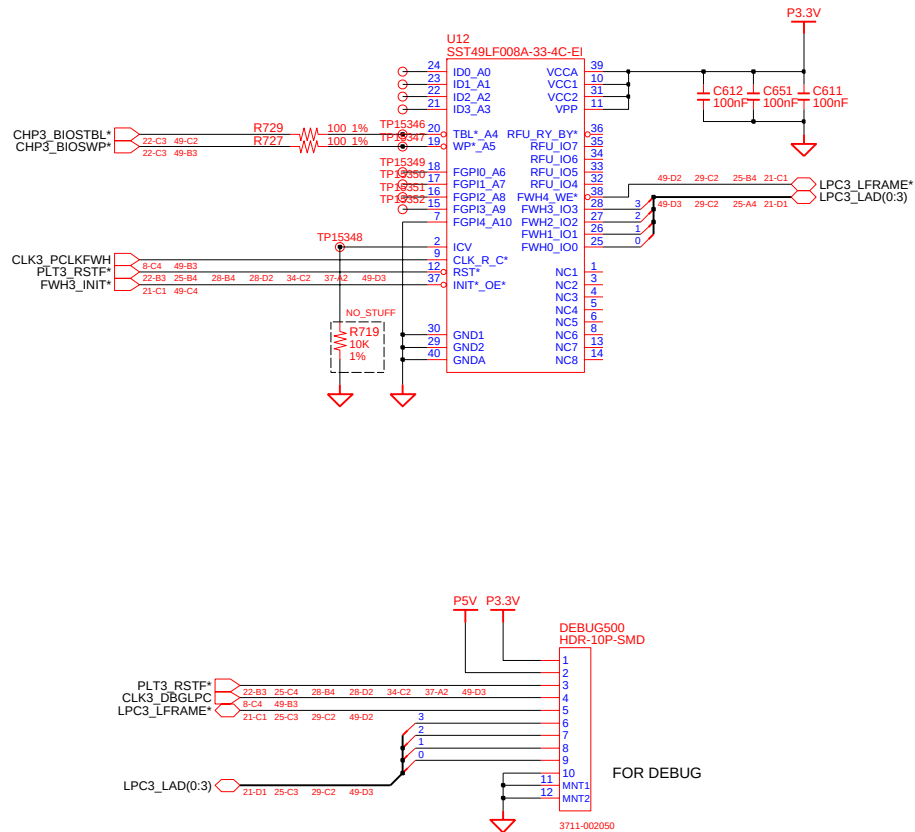
CHP3_MEMVENDOR	
0	SAMSUNG
1	INFINEON
CHP3_MEMSIZE	
0	256MB
1	512MB
CHP3_MEMFREQ[0:1]	
00	400MHz
01	533MHz
10	667MHz
11	Disable On-Board Memory



Wake on PCI-E, OD, Pull-up to ALWAYS power



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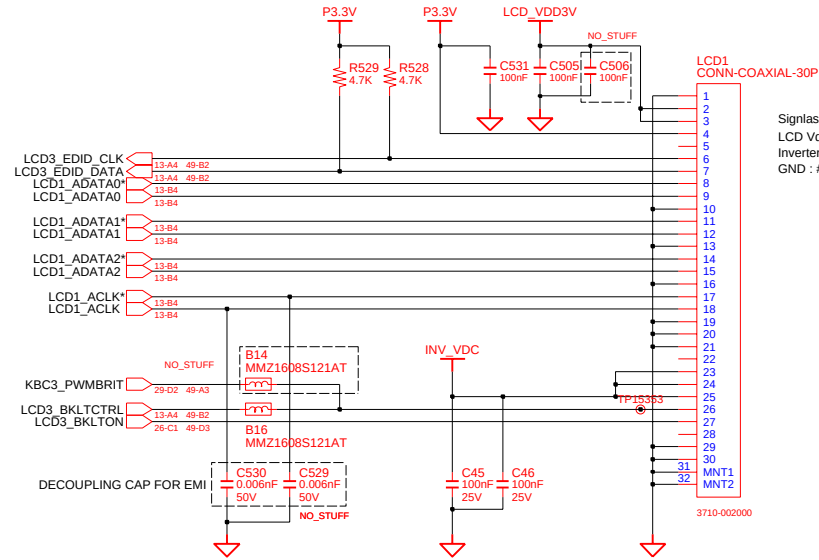


- | | | | |
|----|---|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD EERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET
WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 14 | INIT. KEYBOARD CONTROLLER | 88 | INIT. BIOS DATA ROM |
| 16 | CHECK CHECKSUM | 8A | INIT.EXTENDED BIOS DATA AREA |
| 18 | 8254 TIMER INIT. | 8C | INIT. FDD CONTROLLER |
| 1A | 8237 DMA CONTROLLER INIT. | 9A | SHADOW OPTION ROMS |
| 1C | RESET INTERRUPT CONTROLLER | 9C | SETUP POWER MANAGEMENT |
| 20 | TEST DRAM REFRESH | 9E | ENABLE H/W INTERRUPT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A0 | SET TIME OF DAY |
| 24 | SET ES SEGMENT REG. TO 4GB | A4 | INIT. TYPEMATIC RATE |
| 26 | ENABLE A20 | A8 | ERASE F2 PROMPT |
| 28 | AUTO SIZING DRAM | AA | SCAN FOR F2 KEY STROKE |
| 32 | COMPUTE THE CPU SPEED | AC | ENTER SETUP |
| 34 | TESET CMOS RAM | AE | CLEAR IN POST FLAG |
| 38 | SHADOW SYSTEM BIOS ROM | B0 | CHECK FOR ERRORS |
| 3A | AUTO SIZING CACHE | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B4 | ONE BEEP |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B6 | CHECK PASSWORD (OPTION) |
| 42 | INIT. INTERRUPT VECTOR | B7 | ACPI INIT |
| 44 | INIT. BIOS INTERRUPT | BA | DMI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BE | CLEAR SCREEN |
| 47 | INIT. I20 SUPPORT IF INSTALLED | C0 | TRY BOOT WITH INT19 |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D0 | INTERRUPT HANDLER ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D2 | UNKNOWN INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 50 | DISPLAY CPU TYPE AND SPEED | D8 | SHUTDOWN ERROR |
| 52 | TEST KEYBOARD | DA | EXTENDED BLOCK MOVE |
| 54 | SET KEYCLICK IF ENABLED | DC | SHUTDOWN 10 |
| 56 | ENABLE KEYBOARD | 89 | ENABLE NMI |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 90 | INIT. HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 92 | JUMP TO USER PATCH 2 |
| 60 | TEST EXTENDED MEMORY | 94 | DISABLE A20 ADDRESS LINE |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 96 | CLEAR HUGE ES SEGMENT REG. |
| 64 | JUMP TO USER PATCH 1 | 98 | SEARCH FOR OPTION ROMS |

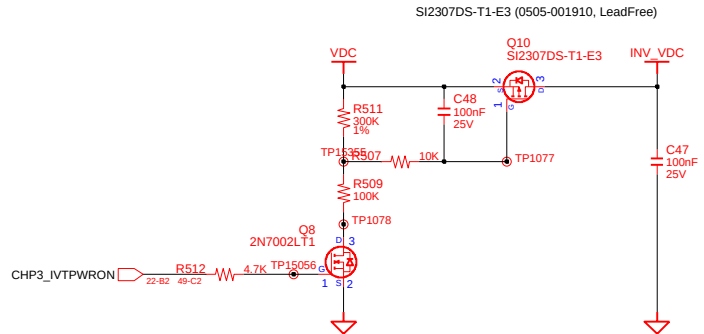
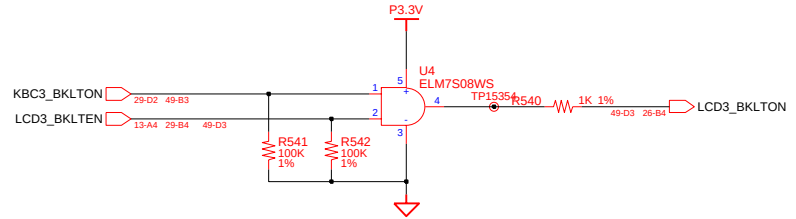
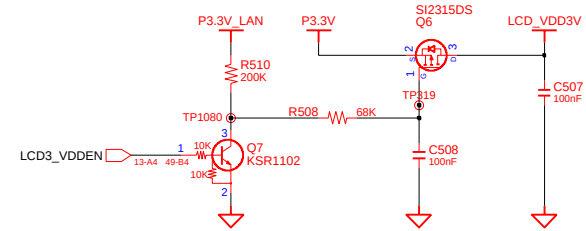
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CHECK	GUO LEI	DEV. STEP	MP	MAIN	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0	FWH	PART NO.	BA41-00602A/3A
MODULE CODE		LAST EDIT			PAGE	25 OF 50

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WXGA LCD CONNECTOR



Signal : #40AWG
LCD Vdd : #36AWG
Inverter Vdd : #36AWG
GND : #36AWG

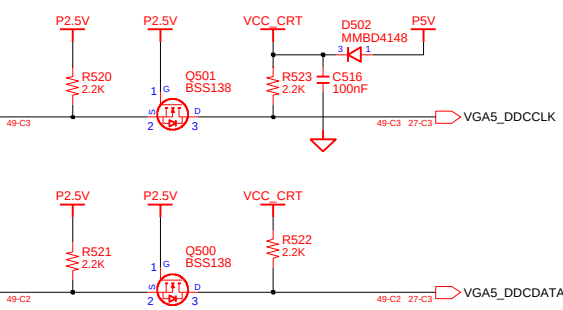


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MODULE CODE		LAST EDIT				
						PART NO. BA41-00602A/3A
						PAGE 26 OF 50

A
B
C
D

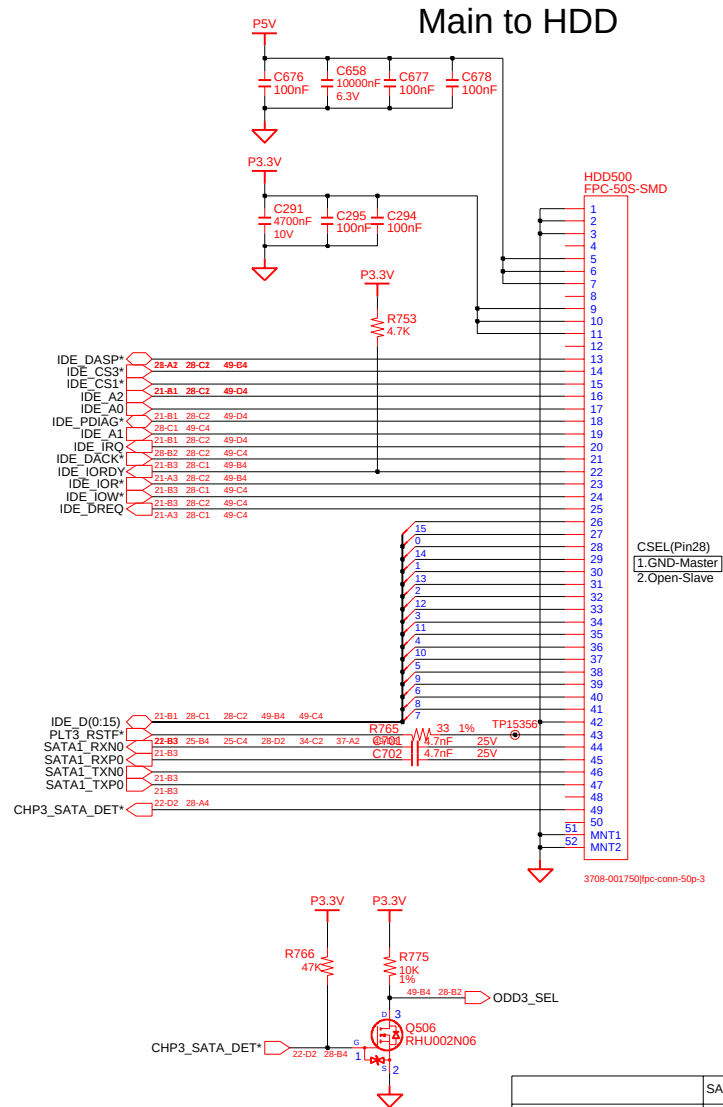
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B504
MMZ1608S121A7

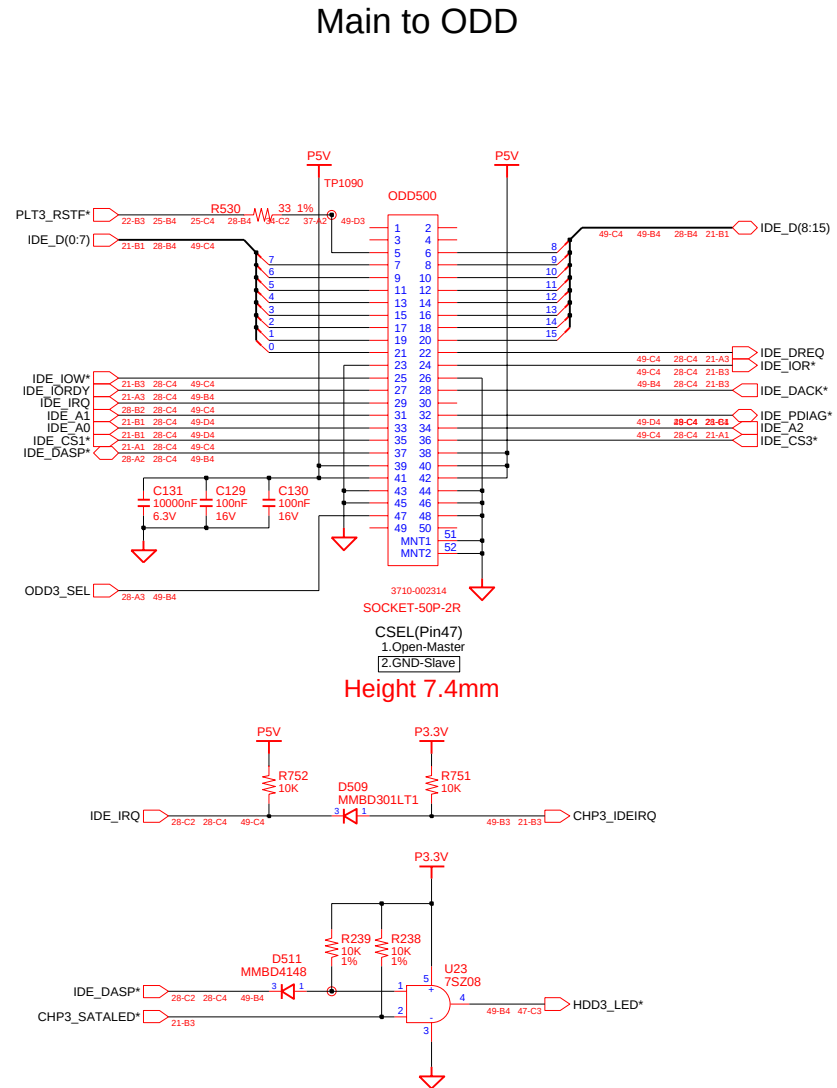


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APPROVAL	KEVIN LEE	REV							1.0
MODULE CODE		LAST EDIT				PART NO.		BA41-00602A/3A	
						PAGE	27	OF	50

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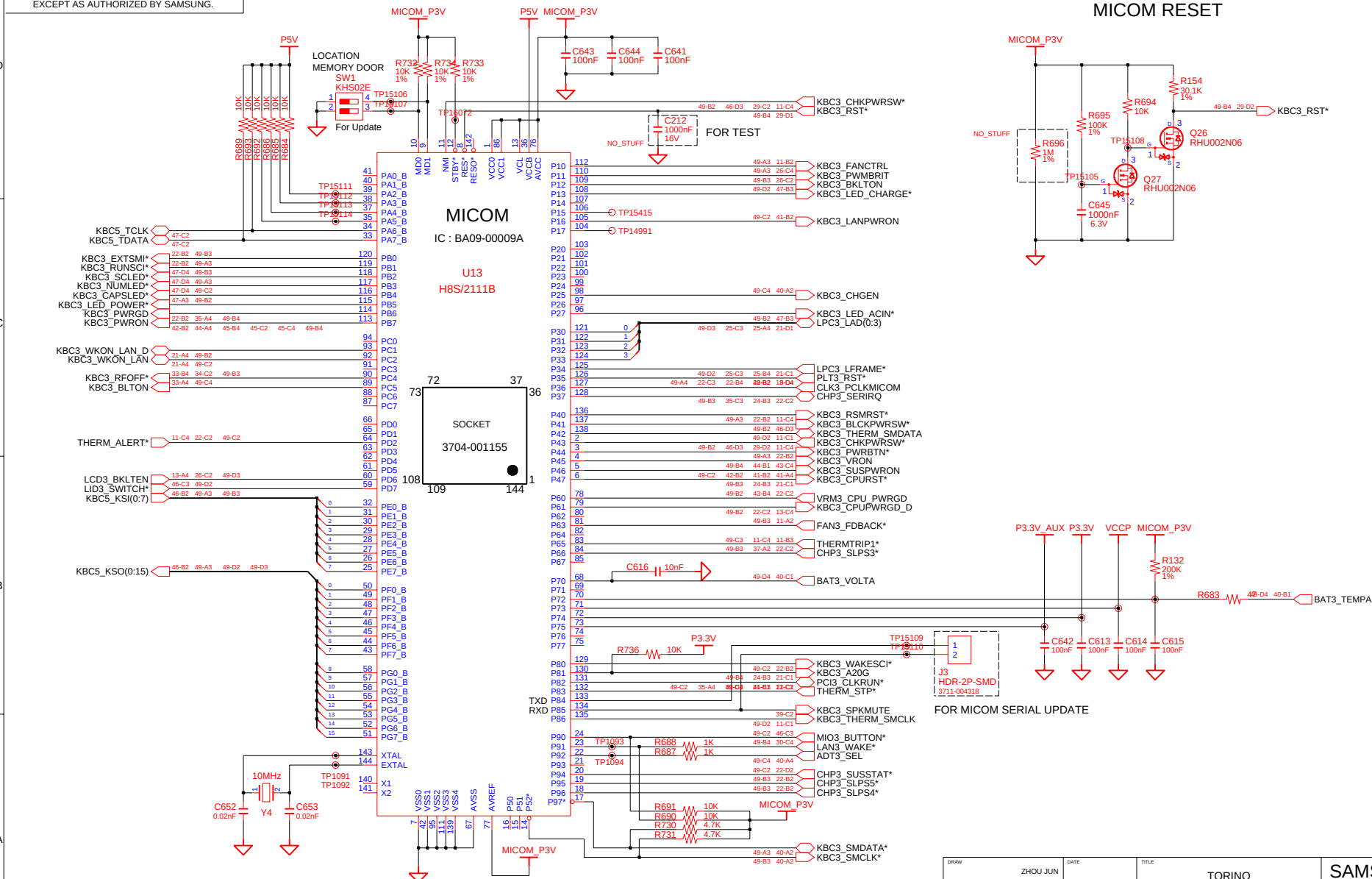


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)



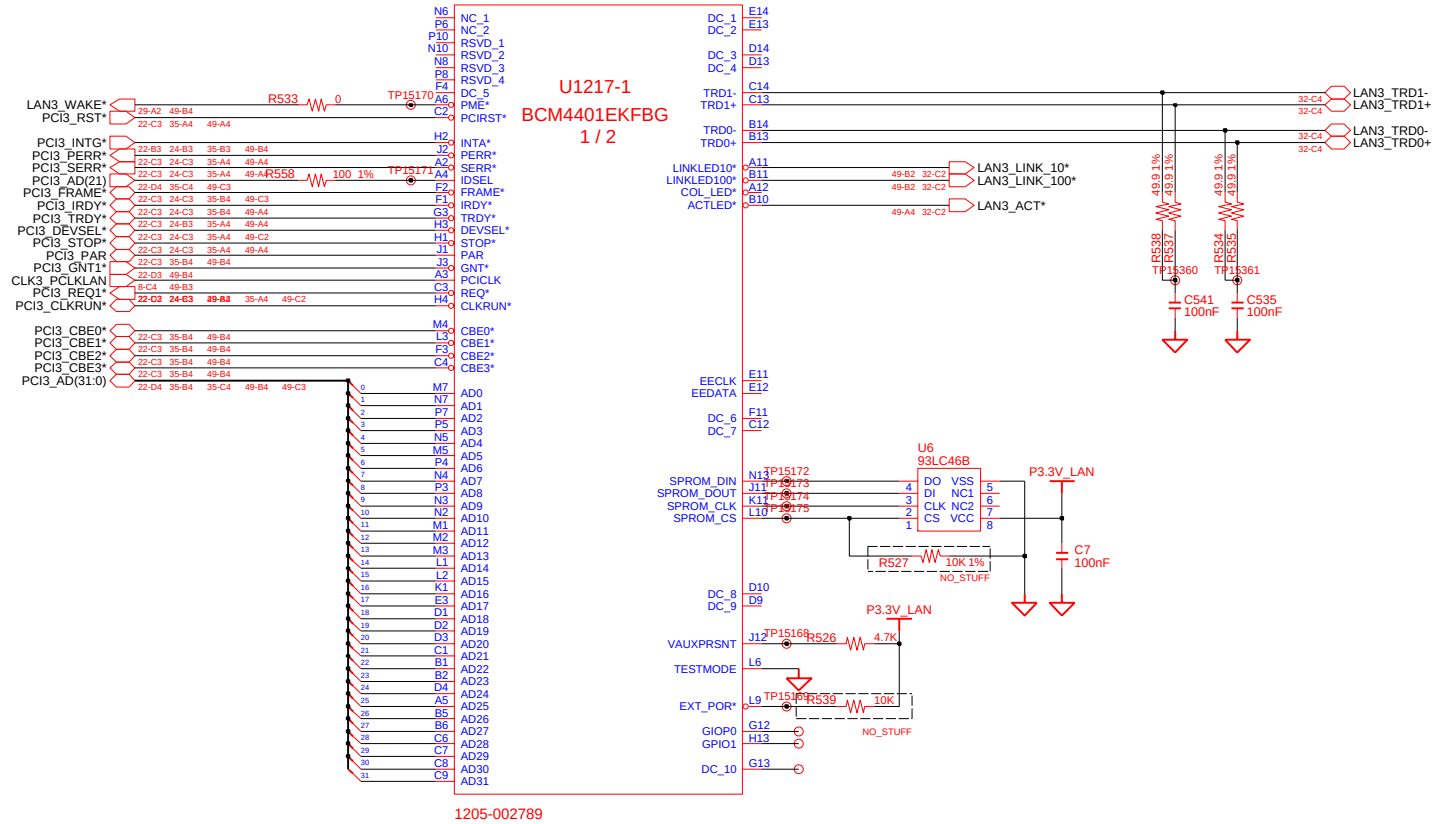
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APPROVAL	KEVIN LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT				BA41-00602A/3A
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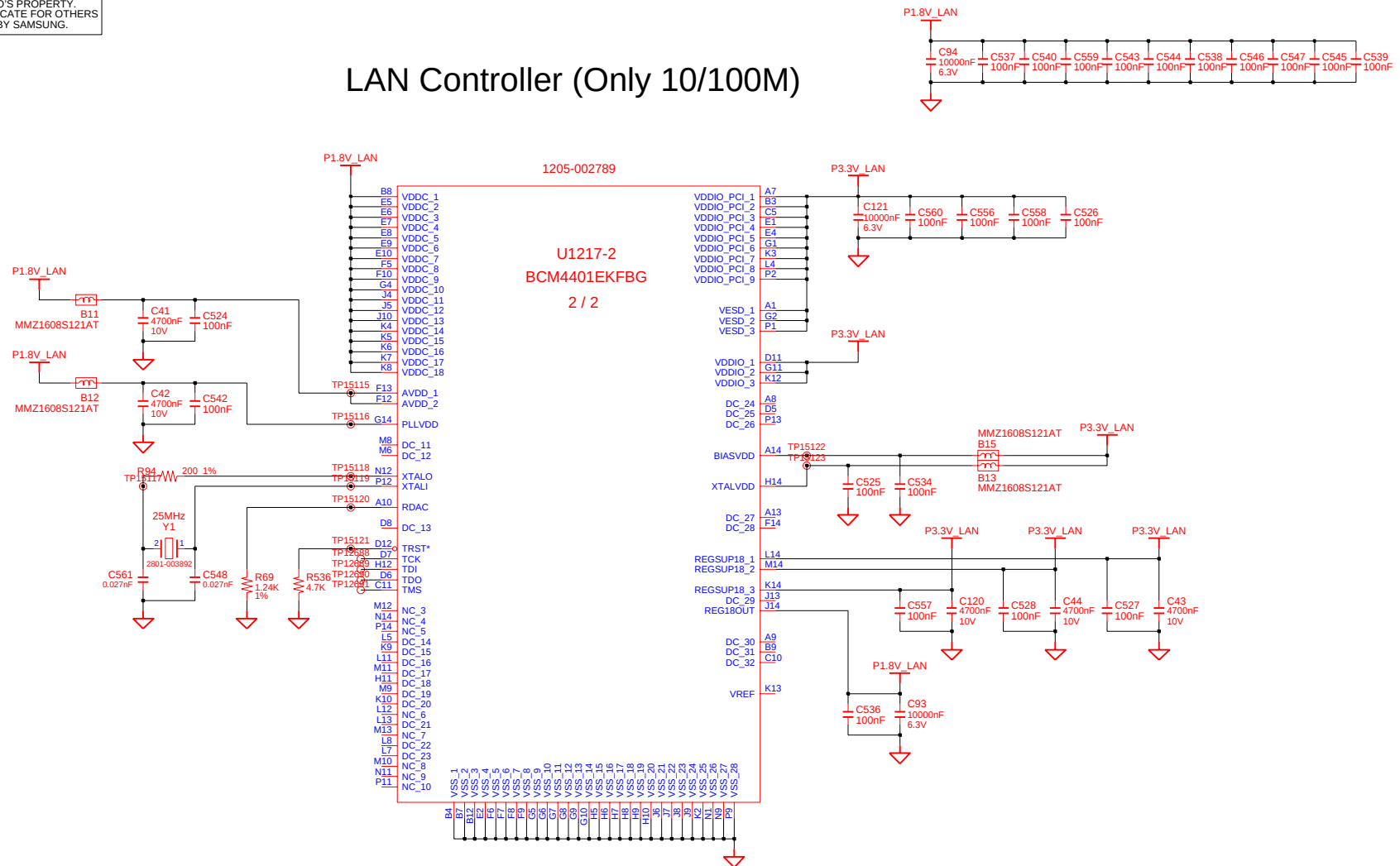
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APPROVAL	KEVIN LEE	REV	1.0	MICOM	PART NO.	BA41-00602A/3A
MODULE CODE		LAST EDIT			PAGE	29 OF 50

LAN Controller (Only 10/100M)



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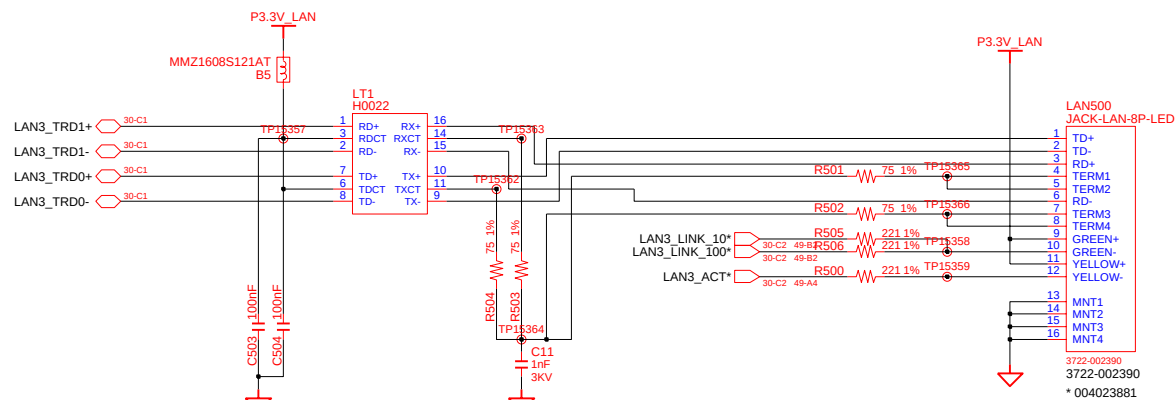
LAN Controller (Only 10/100M)



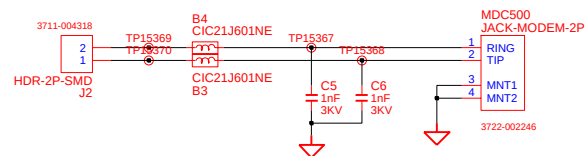
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APPROVAL		KEVIN LEE		REV					1.0
MODULE CODE		LAST EDIT							PAGE
							PART NO.		BA41-00602A/3A

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LAN Connector



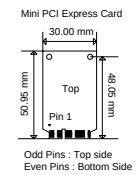
MODEM Connector



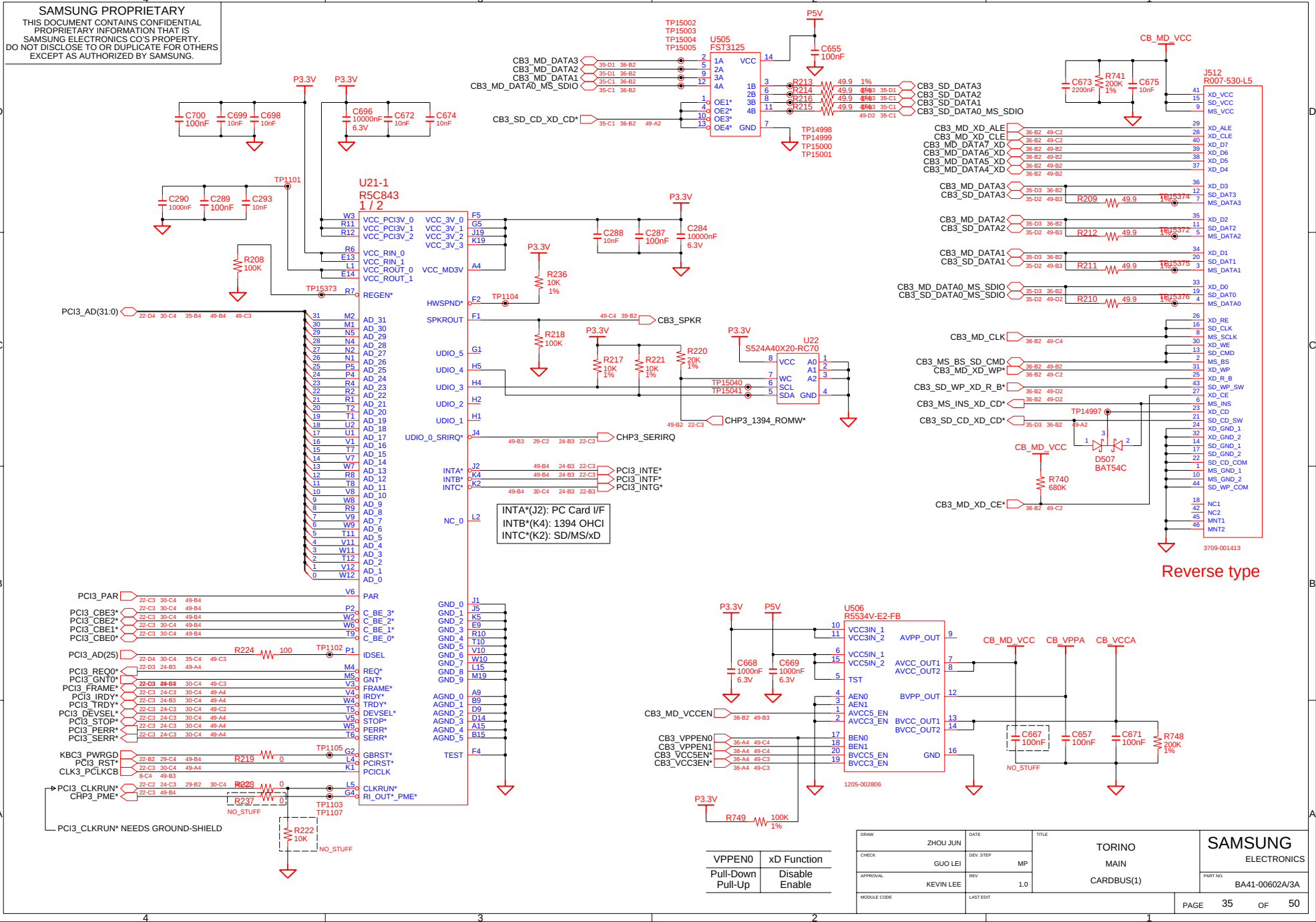
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CHECK	GUO LEI	DEV. STEP		MP	PART NO.	
APPROVAL	KEVIN LEE	REV		1.0	BA41-00602A/3A	
MODULE CODE		LAST EDIT		PAGE	32 OF 50	

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ZHOU JUN		DEV. STEP					
CHECK		MP					
APPROVAL		REV		TORINO MAIN CARDBUS(1)		PART NO.	
KEVIN LEE		1.0				BA41-00602A/3A	
MODULE CODE		LAST EDIT				PAGE	35 OF 50

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U21-2
R5C843
2/2

CB3_CAD(31:0) 37-D2 49-C3 49-C4 49-D4

31 B19 CAD_31_CDATA_10
30 C18 CAD_30_CDATA_9
29 D19 CAD_29_CDATA_1
28 D18 CAD_28_CDATA_8
27 E19 CAD_27_CDATA_0
26 E16 CAD_26_CADR_1
25 F18 CAD_25_CADR_1
24 F15 CAD_24_CADR_2
23 G18 CAD_23_CADR_3
22 G15 CAD_22_CADR_4
21 H18 CAD_21_CADR_5
20 H15 CAD_20_CADR_6
19 J18 CAD_19_CADR_25
18 J16 CAD_18_CADR_7
17 J15 CAD_17_CADR_24
16 P16 CAD_16_CADR_17
15 P19 CAD_15_IOWR* USB_D-
14 R19 CAD_14_CADR_9
13 P18 CAD_13_IORD* USB_D+
12 R18 CAD_12_CADR_11
11 T19 CAD_11_OE*
10 T18 CAD_10_CE_2*
9 U19 CAD_9_CADR_10
8 U18 CAD_8_CDATA_15
7 W17 CAD_7_CDATA_7
6 W17 CAD_6_CDATA_13
5 W16 CAD_5_CDATA_6
4 V16 CAD_4_CDATA_12
3 W15 CAD_3_CDATA_5
2 V15 CAD_2_CDATA_11
1 T15 CAD_1_CDATA_4
0 R14 CAD_0_CDATA_3

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37-C3 49-C4 V19 CC_BE_0*_CE_1*

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37-B3 49-C4 F19 AUDIO_BVD_2
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37-D3 49-B4 w15 CCD_2*_CD_2*_CCD_2*
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37-B3 49-C3 K16 CFRAME*_CADR_23
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37-A3 49-B4 1% A_CLKRUN*_WP_IOIS16*
37-B3 49-B4 H19 A_CRST*_RESET

37-C3 49-D4 N19 CADR_19
37-C3 49-D4 N16 CADR_18
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37-B3 49-D4 C19 CDATA_2_PERST*

35-A2 49-C3 R13 VCCSEN*_VCC3EN*
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37-B3 49-C4 H16 CVS_2_VS_2*_CVS_2

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V14 USBDP
W14 USBDM

CB3_CAD(31:0) 37-D2 49-C3 49-C4 49-D4

31 B19 CAD_31_CDATA_10
30 C18 CAD_30_CDATA_9
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28 D18 CAD_28_CDATA_8
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25 F18 CAD_25_CADR_1
24 F15 CAD_24_CADR_2
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22 G15 CAD_22_CADR_4
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18 J16 CAD_18_CADR_7
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15 P19 CAD_15_IOWR* USB_D-
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12 R18 CAD_12_CADR_11
11 T19 CAD_11_OE*
10 T18 CAD_10_CE_2*
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8 U18 CAD_8_CDATA_15
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4 V16 CAD_4_CDATA_12
3 W15 CAD_3_CDATA_5
2 V15 CAD_2_CDATA_11
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37-B3 49-C4 H16 CVS_2_VS_2*_CVS_2

37-B3 49-B4 R17 A_CLK_CADR_16
37-A3 49-B4 1% A_CLKRUN*_WP_IOIS16*
37-B3 49-B4 H19 A_CRST*_RESET

37-C3 49-D4 N19 CADR_19
37-C3 49-D4 N16 CADR_18
37-C3 49-C4 W18 CDATA_14
37-B3 49-D4 C19 CDATA_2_PERST*

35-A2 49-C3 R13 VCCSEN*_VCC3EN*
35-A2 49-C3 T13 VCC3EN*
35-A2 49-C4 V13 VPPEN_0
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W14 USBDM

CB3_CAD(31:0) 37-D2 49-C3 49-C4 49-D4

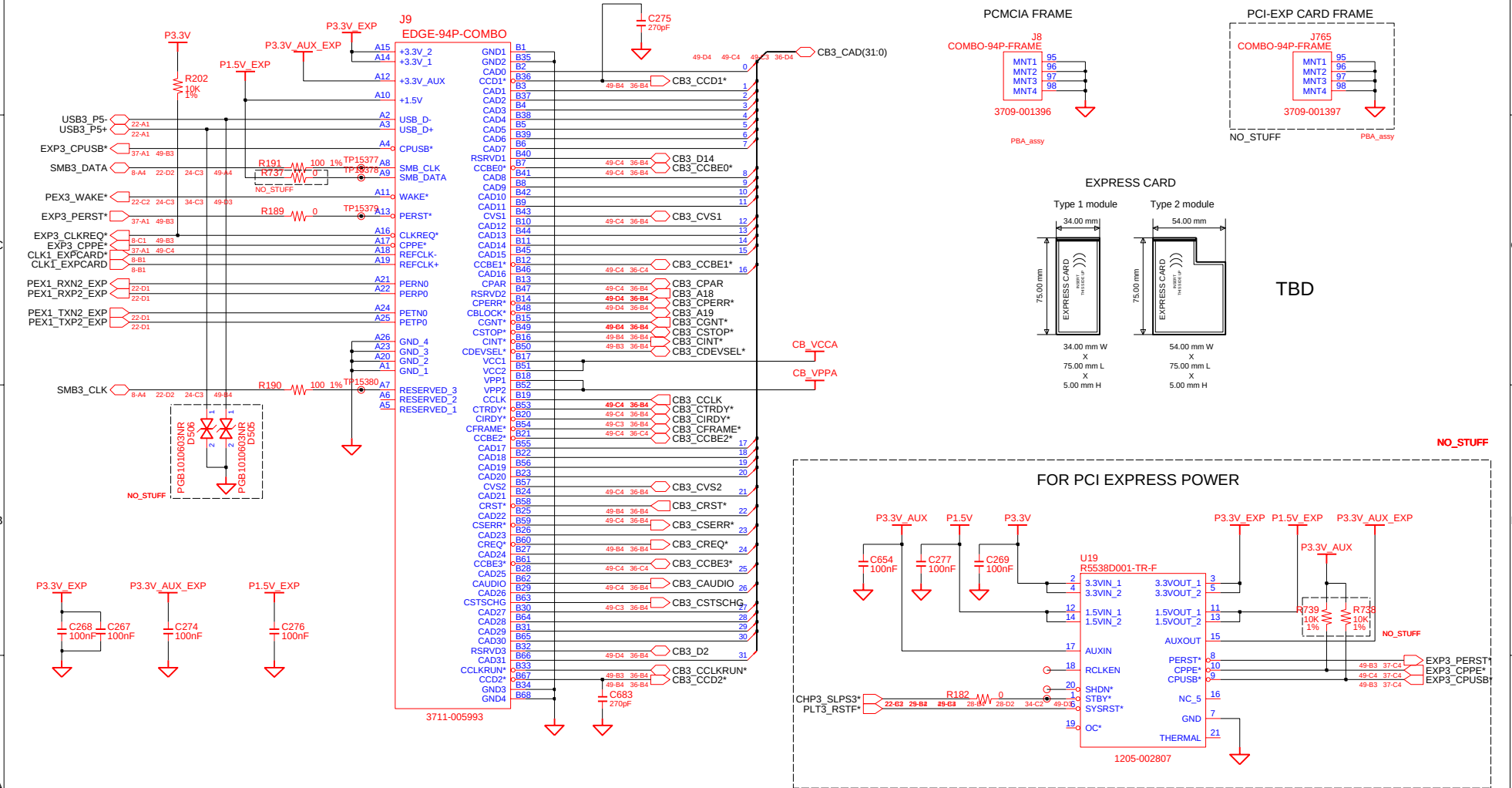
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25 F18 CAD_25_CADR_1
24 F15 CAD_24_CADR_2
23 G18 CAD_23_CADR_3
22 G15 CAD_22_CADR_4
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19 J18 CAD_19_CADR_25
18 J16 CAD_18_CADR_7
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16 P16 CAD_16_CADR_17
15 P19 CAD_15_IOWR* USB_D-
14 R19 CAD_14_CADR_9
13 P18 CAD_13_IORD* USB_D+
12 R18 CAD_12_CADR_11
11 T19 CAD_11_OE*
10 T18 CAD_10_CE_2*
9 U19 CAD_9_CADR_10
8 U18 CAD_8_CDATA_15
7 W17 CAD_7_CDATA_7
6 W17 CAD_6_CDATA_13
5 W16 CAD_5_CDATA_6
4 V16 CAD_4_CDATA_12
3 W15 CAD_3_CDATA_5
2 V15 CAD_2_CDATA_11
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0 R14 CAD_0_CDATA_3

37-B3 49-C4 F16 CC_BE_3*_REG*
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37-C3 49-C4 V19 CC_BE_0*_CE_1*

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37-B3 49-C

DRAW	ZHOU JUN	DATE	TORINO MAIN CARDBUS(2)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP		
APPROVAL	KEVIN LEE	REV		BA41-00602A/3A
MODULE CODE	LAST EDIT			PAGE 36 OF 50

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CHECK	GUO LEI	DEV. STEP	MP	MAIN	PCMCIA	ELECTRONICS
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MODULE CODE		LAST EDIT				BA41-00602A/3A
						PAGE 37 OF 50

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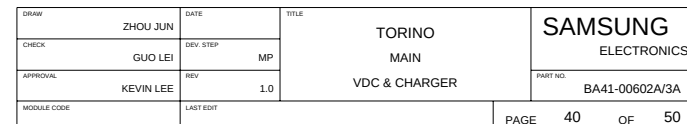




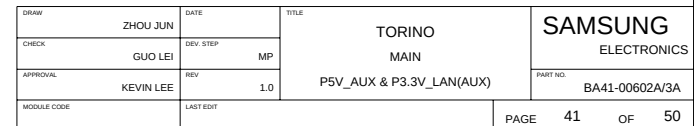
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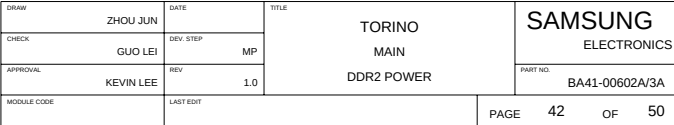
CHARGER & POWER MANAGEMENT



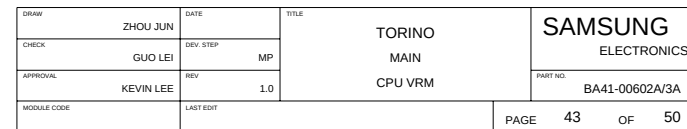
P5V_AUX & P3.3V_LAN(AUX)



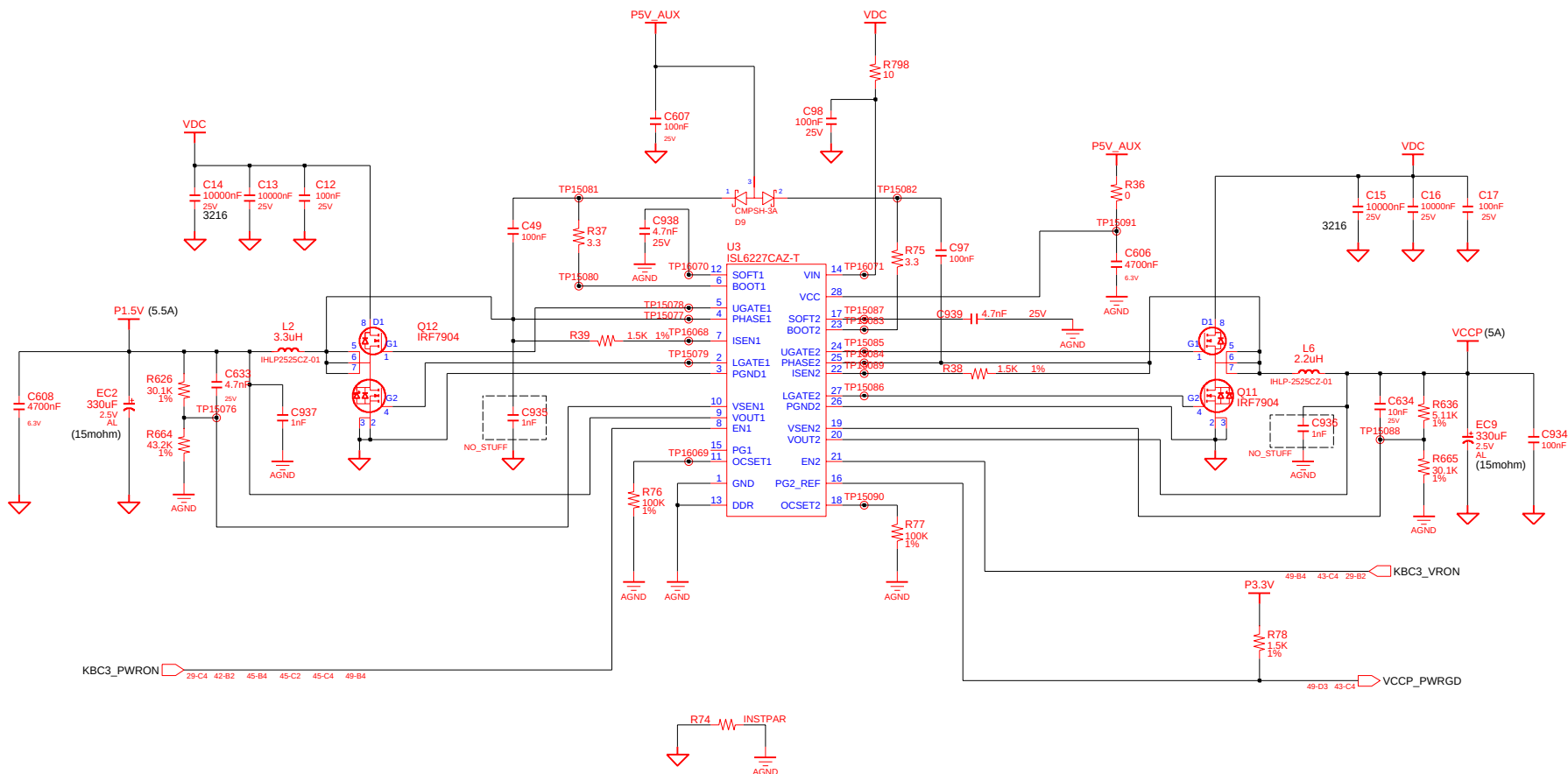
DDR2 POWER



CPU VRM [SEMTECH]

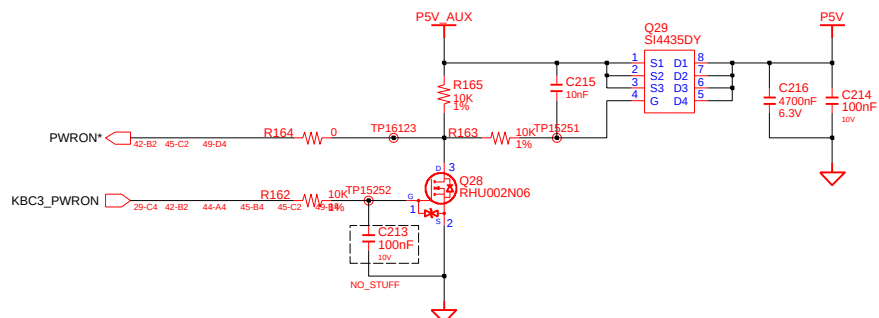


P1.5V & VCCP

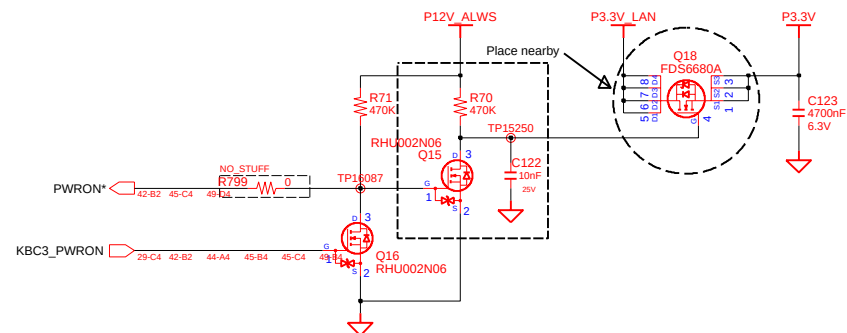


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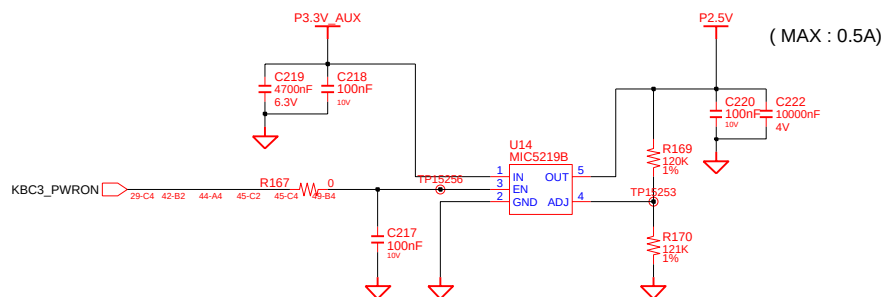
Switched Power On (P5V)



Switched Power On (P3.3V)



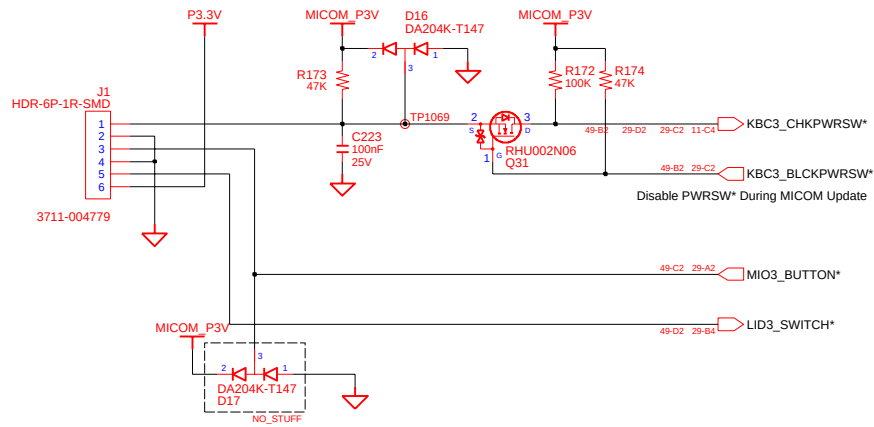
Switched Power On (P2.5V)



DRAW	ZHOU JUN	DATE	TORINO MAIN SWITCHED POWER				SAMSUNG			
CHECK	GUO LEI	DEV. STEP					MP	ELECTRONICS		
APPROVAL	KEVIN LEE	REV					1.0	PART NO. BA41-00602A/3A		
MODULE CODE		LAST EDIT					PAGE	45	OF	50

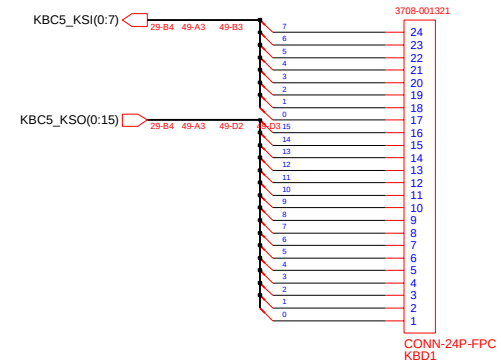
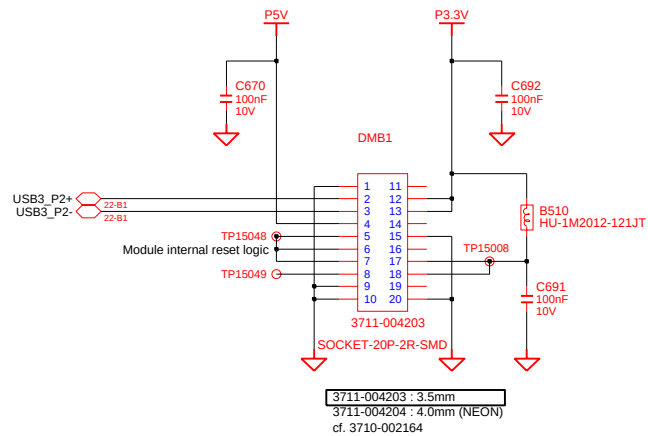
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Power Switch Connector



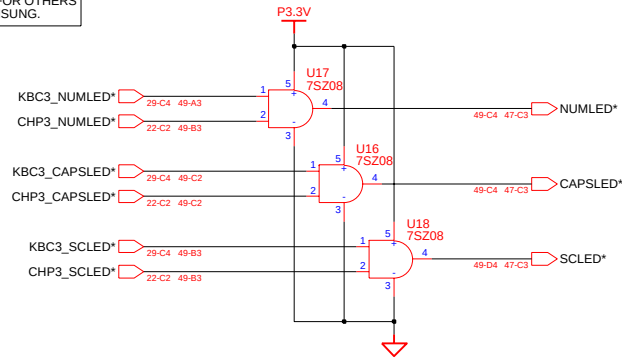
KEYBOARD

OPTION: DMB INTERFACE

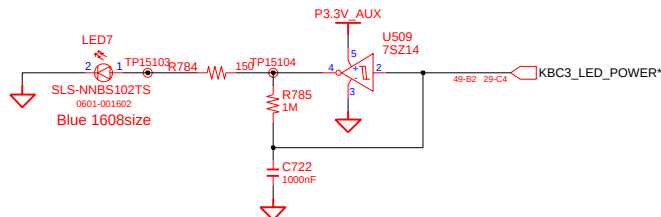
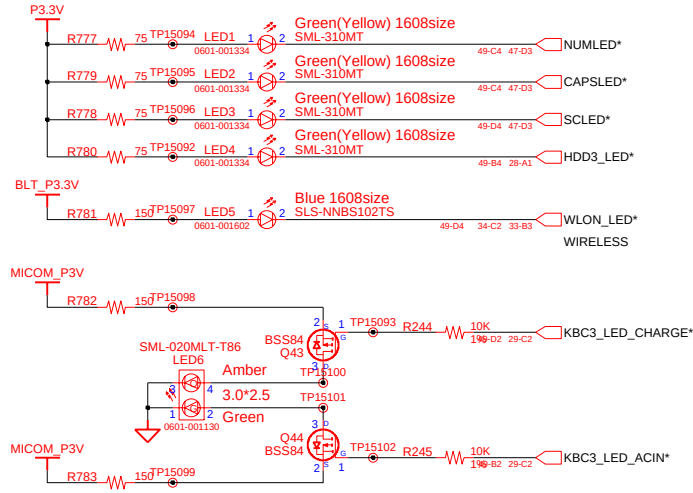


DRAW	ZHOU JUN	DATE		TITLE	TORINO MAIN	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP			
APPROVAL	KEVIN LEE	REV	1.0	MICOM RESET & POWER S/W		PART NO. BA41-00602A/3A
MODULE CODE		LAST EDIT				PAGE 46 OF 50

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LEDS



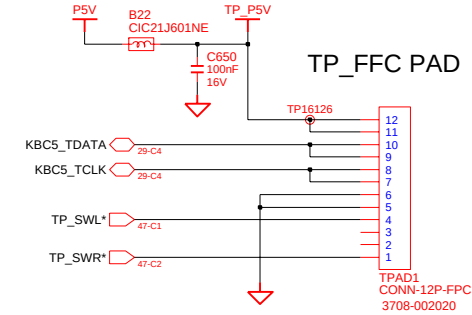
* 1608 Size LEDs

0601-001334 Green C Grade
0601-001602 Blue C Grade
0601-001784 Yellow B Grade

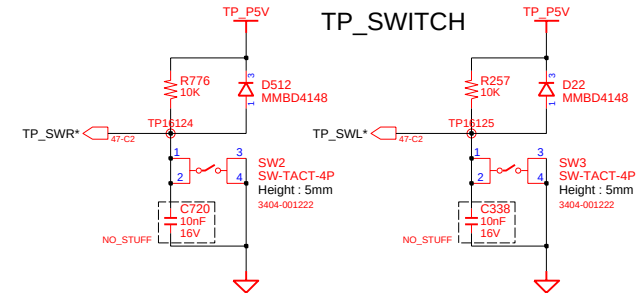
* 3216 Size LEDs

0601-000189 Green 3.2*1.6*1.1
0601-001737 Blue 3.0*1.5*1.4
0601-001130 Amber,Green 3.0*2.5

TOUCH PAD

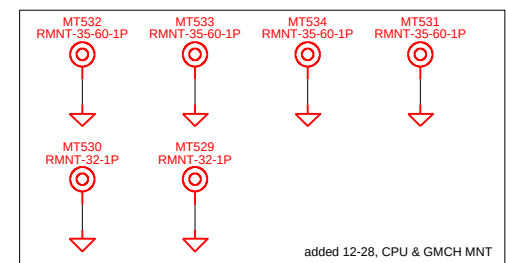
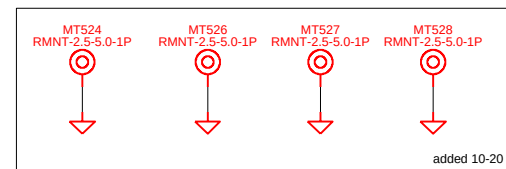
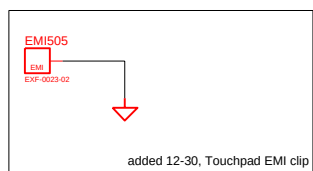
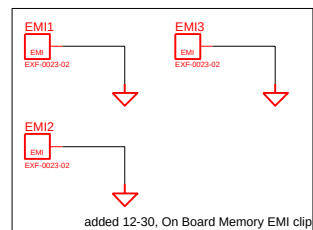
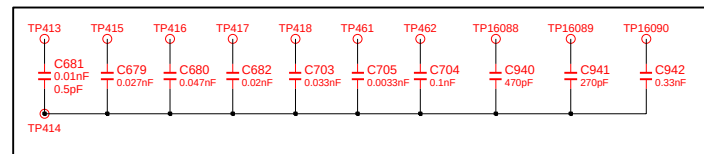
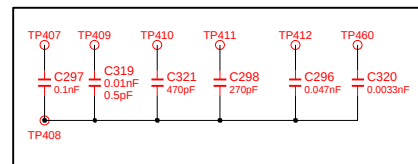
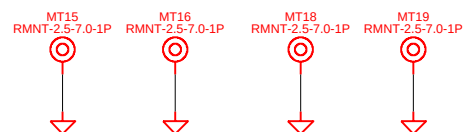
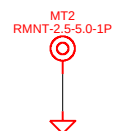
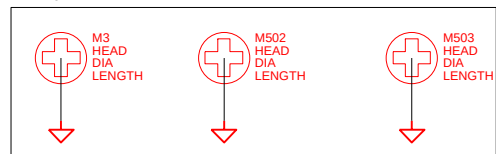


TP_SWITCH



DRAW	ZHOU JUN	DATE		TORINO MAIN SUB B'D & LED	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP		
APPROVAL	KEVIN LEE	REV	1.0		PART NO.
MODULE CODE		LAST EDIT		PAGE	47 OF 50

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REV1
1 O
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TP15882(CM1C1)	TP15769(WLON_LED)	TP15722(PEK3_WAKE)	TP15594(KBC5_KSO(3))	TP15417(KBC5_KSO(1))	TP16060(CHP3_SATCLCRKREQ)	TP15590(P33V_1AN
TP15883(MIC2)	TP15770(AUD03_EAPD)	TP15773(PLT3_RSTF)	TP15595(KBC5_KSO(4))	TP15418(KBC5_KSO(2))	TP16061(CHP3_LED_CHARGE)	TP15591(P33V_2AN
TP15884(COEX1)	TP15771(AUD05_SPOIF	TP15664(THERM_STP)	TP15596(KBC5_KSO(5))	TP15419(KBC5_KSO(3))	TP16062(KBC3_THERM_SMCLKE	TP15582(P33V_1AN
TP15885(COEX2)	TP15772(BAT3_TEMP)	TP15665(VCCP_PWRGD	TP15597(KBC5_KSO(6))	TP15386(KBC5_KSO(14))	TP16063(KBC3_MS_INS_XD_CD	
TP15886(COEX3)	TP15773(BAT3_VREF)	TP15666(KBC5_HS10V)	TP15598(KBC5_KSO(7))	TP15387(KBC5_KSO(15))	TP16064(KBC3_WP_XD_18"	TP15526(P15V_P0IE
TP15887(ULMS)	TP15774(CB3_CAD(0))	TP15667(VGA2_VSYNC	TP15599(KBC5_KSO(8))	TP15391(LD03_SWITCH"	TP16065(KBC3_THERM_SMDATA	TP15527(P15V_P0IE
TP15888(CB3_D2)	TP15775(CB3_CAD(1))	TP15668(KBC5_GREEN	TP15600(KBC5_KSO(9))	TP15392(LPC3_LFRAME"	TP16066(MINIPC13_CLKREQ"	TP15531(P33V_AUO_EXP
TP15889(DIE_A0)	TP15776(CB3_CAD(2))	TP15669(VGA5_HSYNC	TP15604(LCD3_BKLTEN	TP15393(MCH3_CFG(0))	TP16067(KBC3_SD_DATA1_MS_SDIO	TP15536(VDC
TP15890(DIE_A1)	TP15777(CB3_CAD(3))	TP15670(VGA5_VSYNC	TP15605(LCD3_BKLTEN	TP15394(MCH3_CFG(1))	TP16069(AGND	TP15537(VDC
TP15891(CB3_CPD)	TP15778(CB3_CPD)	TP15671(AUD03_EAPD)	TP15606(LPC3_LAD(1)	TP15395(MCH3_CFG(2))	TP16070(AGND_VCC	TP15538(VDC
TP15904(PWRON"	TP15779(CB3_CAD(5))	TP15672(AUD03_PCBEEP	TP15607(LPC3_LAD(2)	TP15396(MCH3_CFG(3))	TP16010(AVDD	TP15539(VDC
TP15905(SCLED"	TP15780(CB3_CAD(6))	TP15673(AUD05_SPK_+L	TP15608(LPC3_LAD(1)	TP15397(MCH3_CFG(6))	TP16011(AVDD_VDD	TP15540(VDC
TP15906(CB3_A18	TP15781(CB3_CAD(7))	TP15674(AUD05_SPK_-L	TP15609(LPC3_LAD(3))	TP15398(MCH3_CFG(9))	TP16024(AGND_AVD	TP15542(VCC_CRT
TP15907(CB3_A19	TP15782(CB3_CAD(8))	TP15675(AUD05_SPK_-R	TP15610(MCH3_CFG(6))	TP15399(MCH3_CFG(10))	TP16025(AGND_CHG	TP15546(VCC_CORE
TP15908(CB3_D14	TP15783(CB3_CAD(9))	TP15676(AUD05_SPK_+R	TP15611(MCH3_CFG(7))	TP15400(MCH3_CFG(11))	TP15547(VCC_CORE	TP15547(VCC_CORE
TP15909(DIE_IRQ)	TP15784(CB3_CAU(0)	TP15677(BAT3_SMCLK"	TP15449(PCB3_AD(10))	TP15519(PCB3_CLKRUN"	TP16032(BATT_DC	TP15548(VCC_CORE
TP15864(NUMLED"	TP15785(CB3_CBE0"	TP15678(BLT_DETECT"	TP15450(PCB3_AD(11))	TP15518(PCB3_DEVELR"	TP16033(BATT_DC	TP15549(VCC_CORE
TP15865(CB3_D23_SEL	TP15786(CB3_CBE1"	TP15679(CB3_CAD(10))	TP15451(PCB3_AD(12))	TP15517(THERM_ALERT"		TP15550(VCC_CORE
TP15866(CAPSLED"	TP15787(CB3_CBE2"	TP15680(CB3_CAD(11))	TP15452(PCB3_AD(13))	TP15516(VDD_D0C0DATA	TP15877(OEMD	TP16073(P33V_3V
TP15867(CB3_CCU)	TP15788(CB3_CBE3"	TP15681(CB3_CAD(12))	TP15453(PCB3_AD(14))	TP15515(VGA5_AGN	TP15878(OE_AGN	TP16074(P33V_3V
TP15868(CB3_CPAR	TP15789(CB3_CIRDY"	TP15682(CB3_CAD(13))	TP15454(PCB3_AD(15))	TP15514(CB3_MD_XD_ALE	TP15981(OE_AGN	TP16075(P33V_3V
TP15869(CB3_CVS1	TP15790(CB3_CPERP"	TP15683(CB3_CAD(14))	TP15455(PCB3_AD(16))	TP15513(CB3_MD_XD_CE"	TP15982(KBC_VCCA	TP16076(P33V_3V
TP15870(CB3_CVS2	TP15791(CB3_CSERR"	TP15684(CB3_CAD(15))	TP15456(PCB3_AD(17))	TP15512(CB3_MD_XD_CLE	TP15991(OE_VPP	TP16077(VCCP
TP15871(CB3_CSTOP	TP15792(CB3_CSTOP"	TP15685(CB3_CAD(16))	TP15457(PCB3_AD(18))	TP15511(CB3_MD_XD_WP"	TP16000(CHG_REF	TP16078(VCCP
TP15872(CPU1_A1M	TP15793(CB3_CTMV"	TP15686(CB3_CAD(17))	TP15458(PCB3_AD(19))	TP15510(CHP3_BATT	TP15910(CB3_MD_VCC	TP16079(VCCP
TP15873(HF_OUT_L	TP15794(CB3_MD_CLK	TP15687(CB3_CAD(18))	TP15459(PCB3_AD(20))	TP15509(CHP3_CAPSLED"	TP15942(INV_VDD	TP16080(VCCP
TP15874(HF_OUT_R	TP15795(CB3_VPPEN)	TP15688(CB3_CAD(19))	TP15460(PCB3_AD(21))	TP15508(CHP3_OPRSLVR	TP15947(LCD_VDD3V	TP16081(GROUND
TP15875(DIE_CS1"	TP15796(CB3_VPPEN1	TP15689(CB3_CAD(20))	TP15461(PCB3_AD(22))	TP15507(CHP3_LUTPWRRN	TP15952(LDO_P5_4V	TP16082(GROUND
TP15876(DIE_CS3"	TP15798(CB3_SATA"	TP15690(CB3_CAD(21))	TP15462(PCB3_AD(23))	TP15506(CHP3_SVTTPAT	TP15957(MEM_VREF	TP16093(GROUND
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TP15878(DIE_D1)	TP15760(CB3_CLK3_USB48	TP15692(CB3_CAD(23))	TP15464(PCB3_AD(25))	TP15490(CPU1_PWRGDENSE	TP15961(MEM_VREF	TP16096(GROUND
TP15879(DIE_D(2)	TP15761(CPU1_A20M"	TP15693(CB3_CAD(24))	TP15588(CB3_CAD(26))	TP15491(CPU1_VCCSENSE	TP15582(MICOM_P3V	TP16095(GROUND
TP15880(DIE_D(3)	TP15764(CPU1_BSEL0	TP15694(CB3_CAD(25))	TP15589(OCP3_AD(27))	TP15492(CPU1_VCCSENSE	TP15963(MICOM_P3V	TP16097(GROUND
TP15881(DIE_D(4)	TP15765(CPU1_BSEL					

DRAW	ZHOU JUN	DATE		TORINO MAIN TEST POINT(1)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	MP		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE			LAST EDIT		
				PAGE	49 OF 50

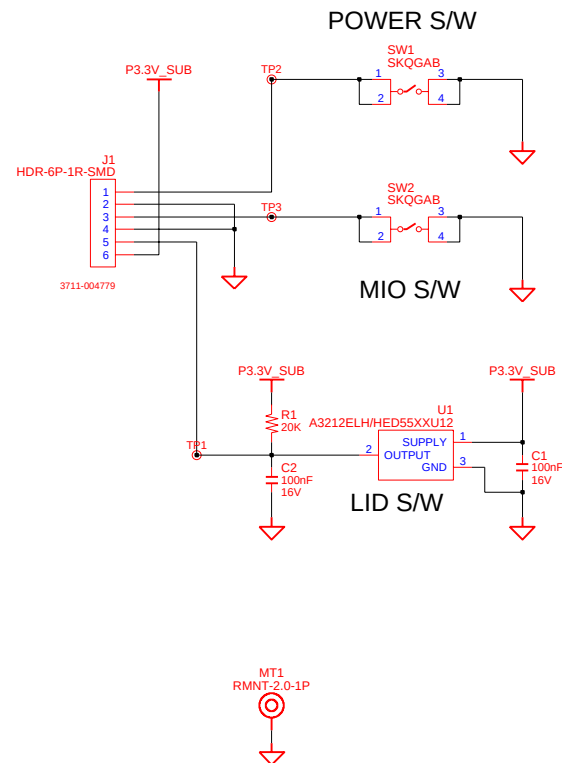
ON-TOP BOARD

CPU : Intel YONAH
Chip Set : Intel 945GM & ICH7-M
Remarks : ON TOP BOARD

Model Name : TORINO
PBA Name : On-Top
PCB Code : BA59-01851A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2006.1.5

DRAW	CHECK	APPROVAL

ON TOP BOARD



DRAW		ZHOU, JUN		DATE	TITLE	TORINO ON TOP ON TOP	SAMSUNG		
CHECK		GUO, LEI		DEV. STEP			MP	ELECTRONICS	
APPROVAL		LEE, KEVIN		REV				1.0	PART NO.
MODULE CODE		LAST EDIT					PAGE	1	OF