

HABANA-C

CPU : Intel Dothan -2M
Chip Set : RC410MD & SB450
Remarks : Mobility Platform

Model Name : HABANA-C
PBA Name : MAIN
PCB Code : BA41-00615A
Dev. Step : PRR
Revision : 1.0
T.R. Date : 2005.12.26

DRAW	CHECK	APPROVAL
DS.JIANG	DJ.XU	KEVINLEE

Owner : SESC R & D

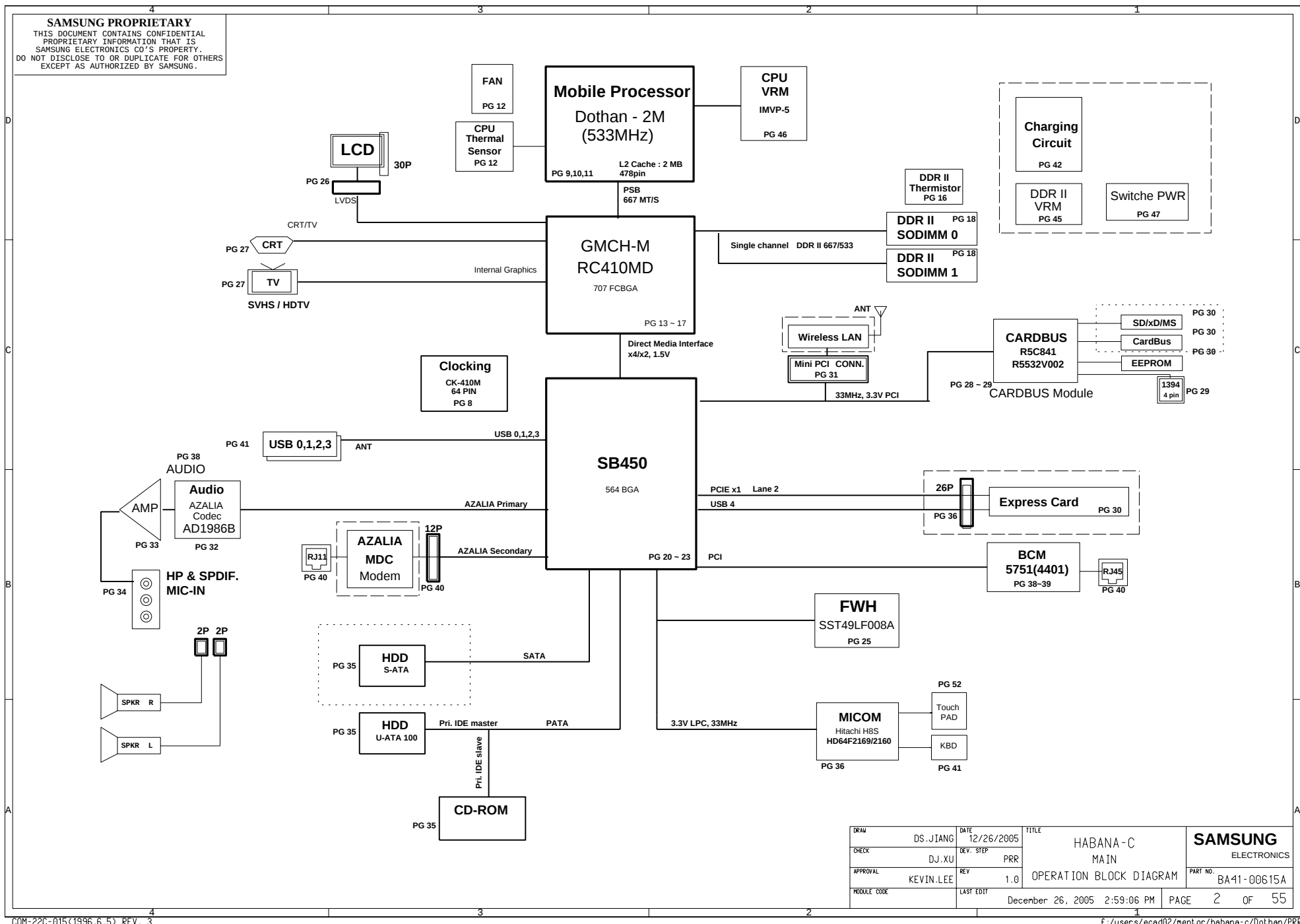
Signature :

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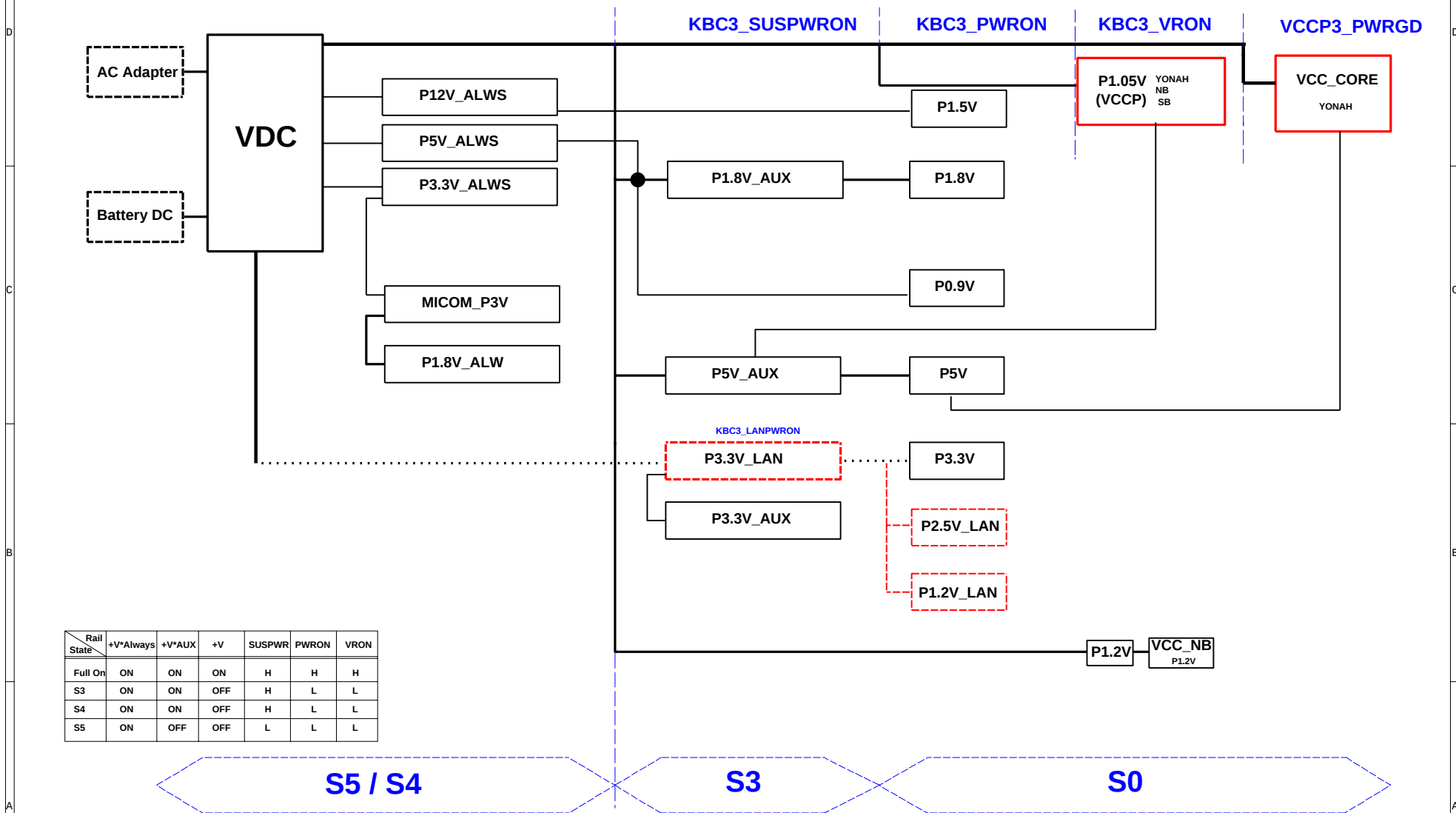
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CHECK	DJ.XU	DEV. STEP	PRR		COVER	
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	1 OF 55	

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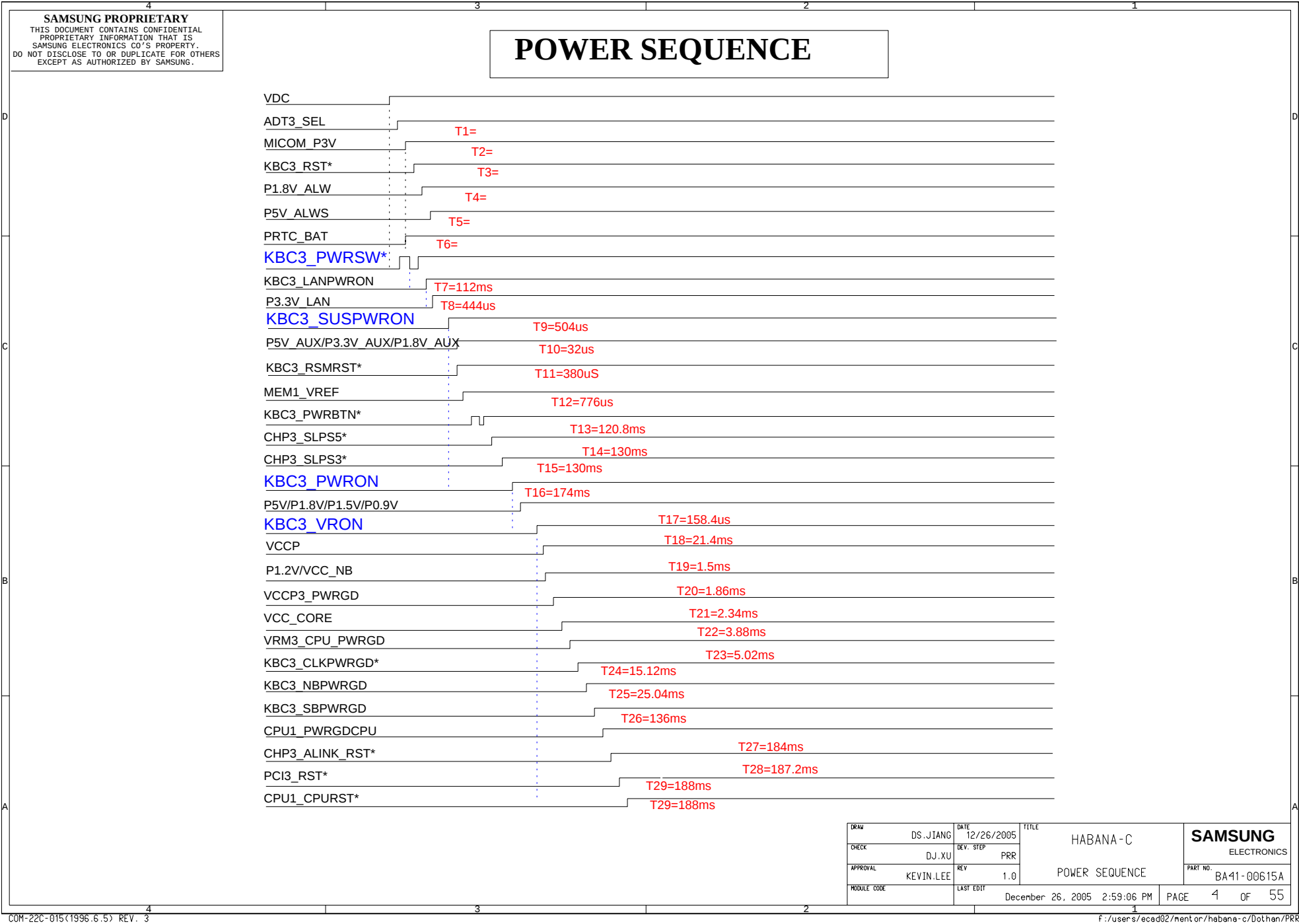


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Power Diagram



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
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APPROVAL	KEVIN.LEE	REV	1.0			
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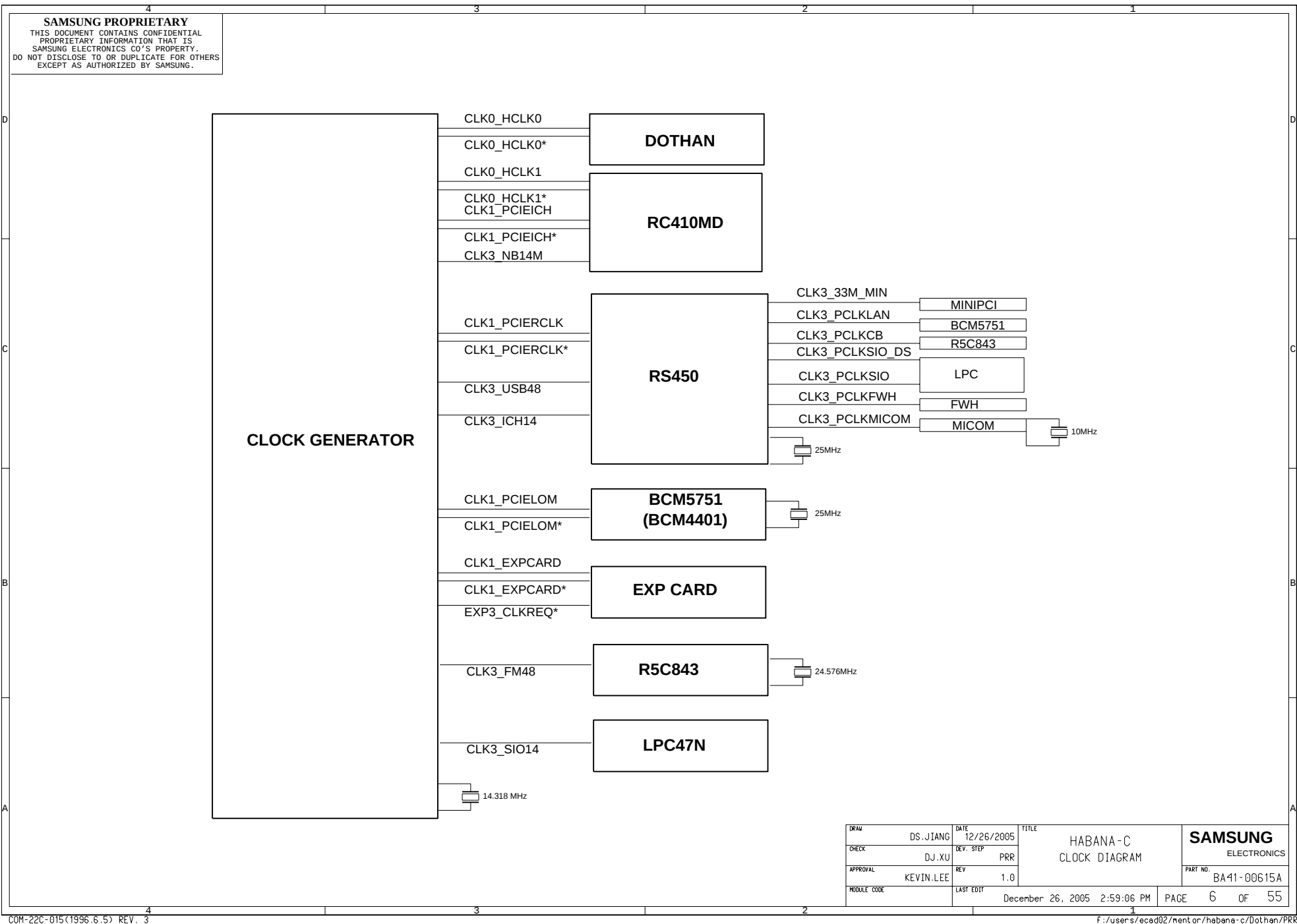


A B C D

POWER RAILS ANALYSIS



COM-22C-015(1996.6.5) REV. 3



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD24	0	E,F,G
LAN	AD21	1	C
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/I2E/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VCC_CORE	CPU
VCCP	CPU RC410MD SB450
VCC_NB	RC410MD
P1.2V	RC410MD VCC_NB
P1.5V	CPU EXPCARD
P1.8V	RC410MD SB450 R5C843
P0.9V	DDR2
P5V	FAN THERMAL CRT SB450 R5C483 MINIPCI AD1986B HDD ODD MICOM USB TOUCH-PAD VCC_CORE
P3.3V	SYSTEM POWER
P2.5V_LAN	BCM5751
P1.2V_LAN	BCM5751
P1.8V_AUX	DDR2 P1.8V RC410MD
P5V_AUX	THERMAL LCD P1.2V P5V
P3.3V_LAN	LCD BCM5751 P3.3V
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB450 THERMAL
P12V_ALWS	VCC_NB P1.5V P3.3V P1.8V
P5V_ALWS	P3.3V DDR2-PWR
P3.3V_ALWS	MICOM_P3V
MICOM_P3V	THERMAL SB450 MICOM LED P1.8V_ALWS
P1.8V_ALW	SB450
VDC	Primary DC system power supply (7 to 21V)

I C / SMB Address

Devices	Address	Hex	Bus
SB450	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	SYSTEM PORT C
4	EXPRESS CARD

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB450	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

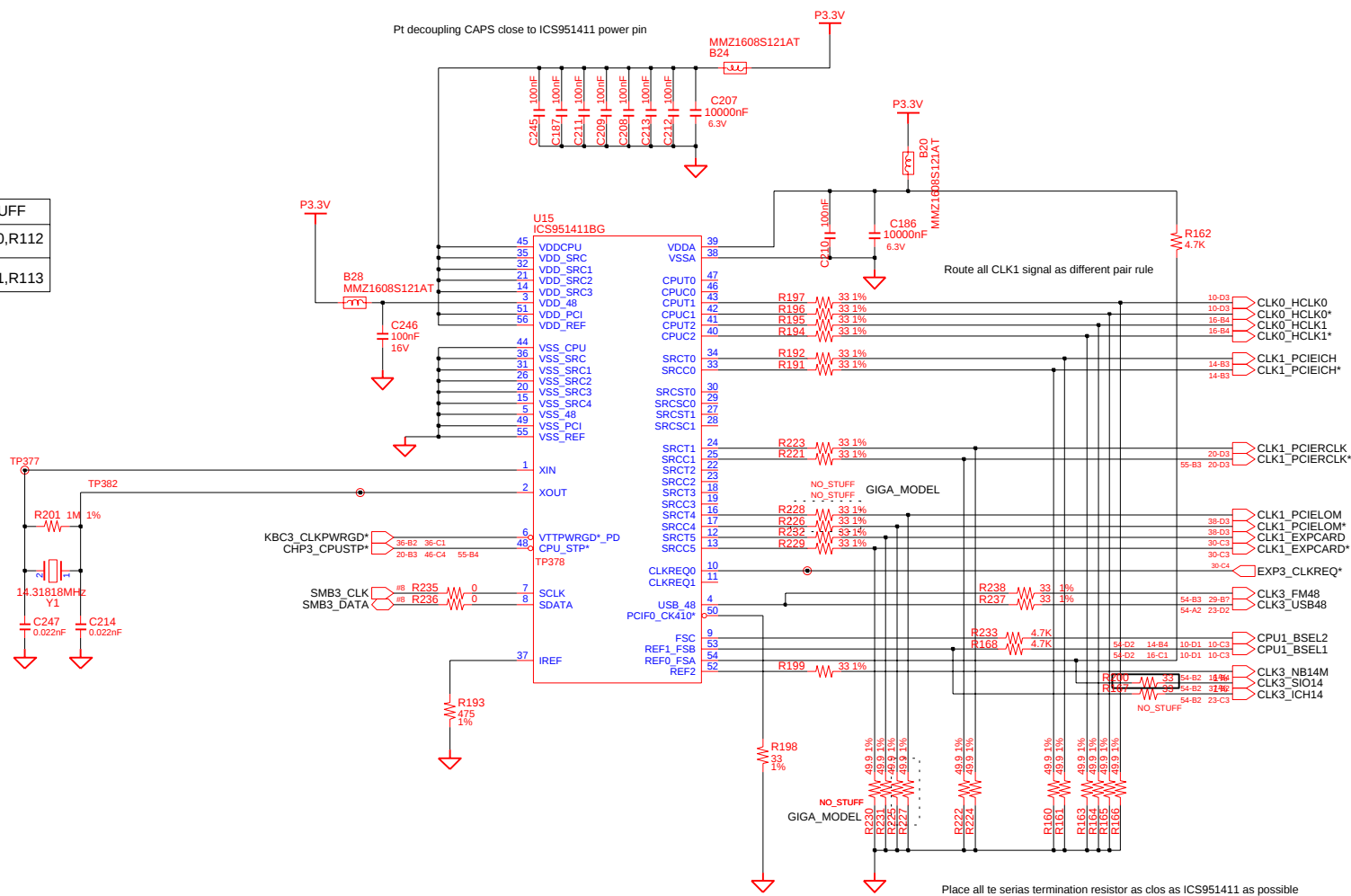
HFM Voltage
770:1.26V->1.372V
730,740,750,760:1.26->1.356V

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG
CHECK	DJ.XU	DEV. STEP	PRR		MAIN	ELECTRONICS
APPROVAL	KEVIN.LEE	REV	1.0	BOARD INFORMATION	PART NO.	BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	7	OF 55

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	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

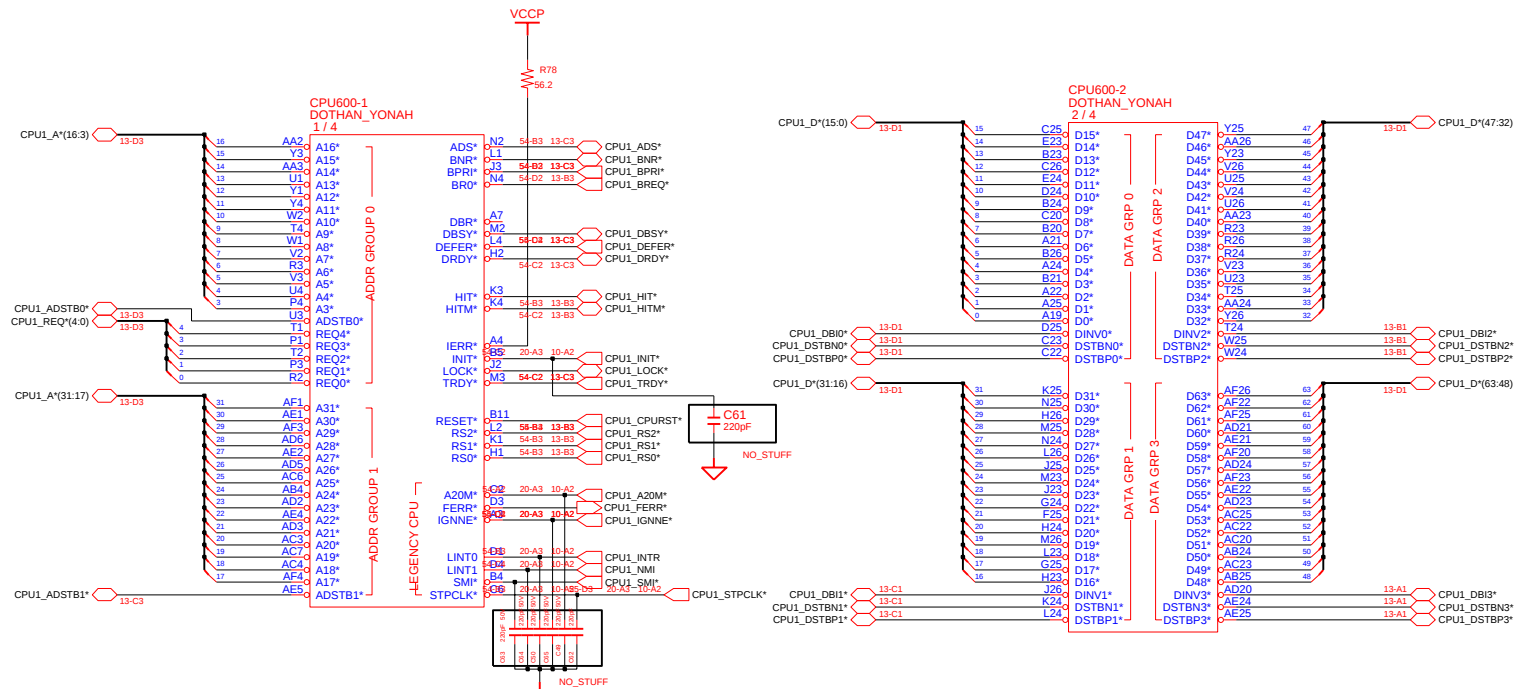
FSB	STUFF	NO STUFF
400MHz	R119,R141,R113	R121,R140,R112
533MHz	R119,R140,R112	R121,R141,R113



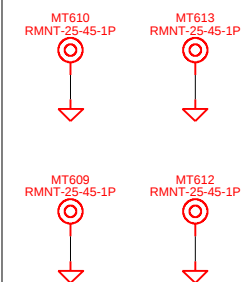
Place all te serial termination resistor as clos as ICS951411 as possible

DRAM	DS.JIANG	DATE	12/26/2005	TITLE HABANA-C MAIN CLOCK GENERATOR	
CHECK	DJ.XU	DEV. STEP	PRR		
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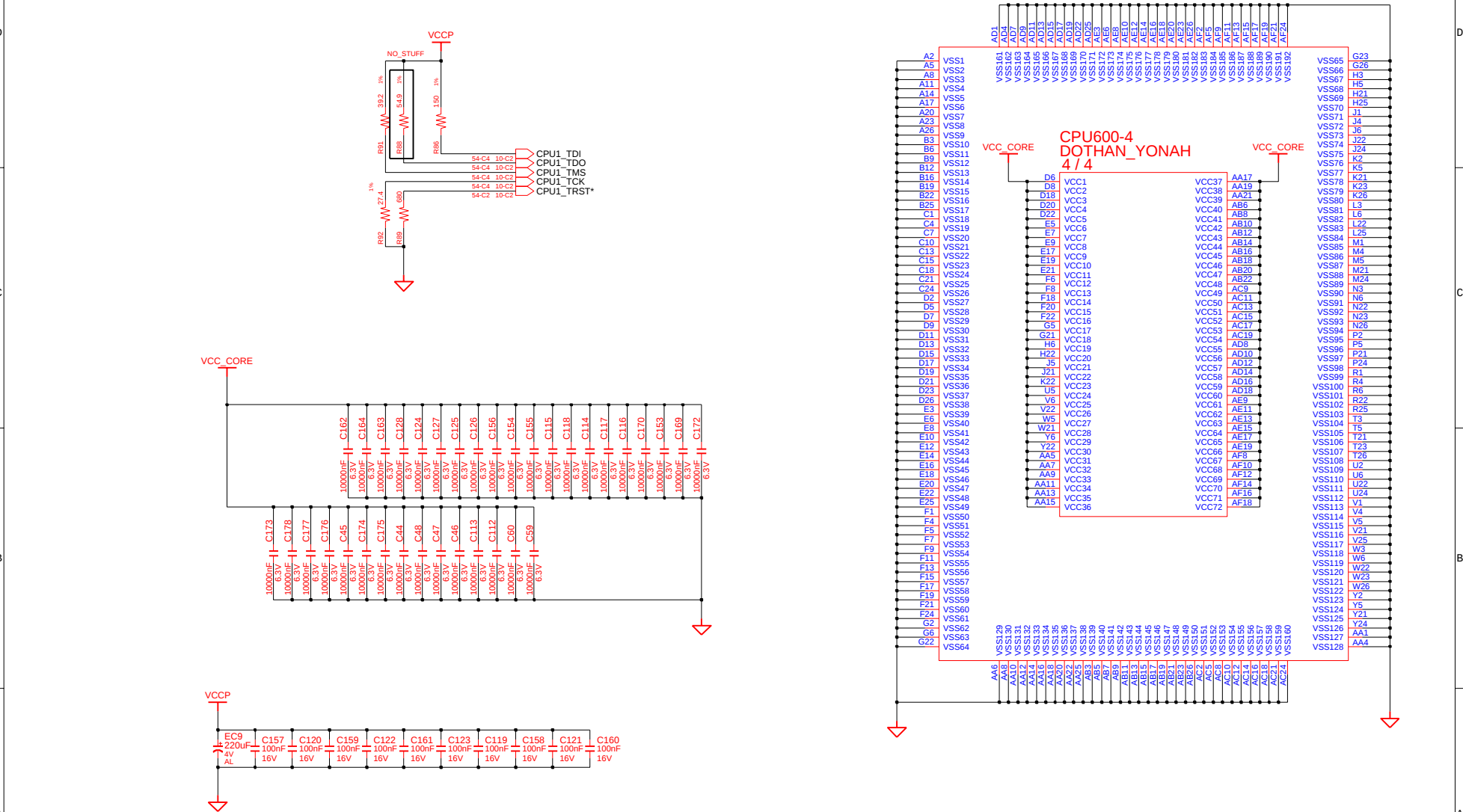
**NOTE



RHE SUPPORTER

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	9 OF 55	

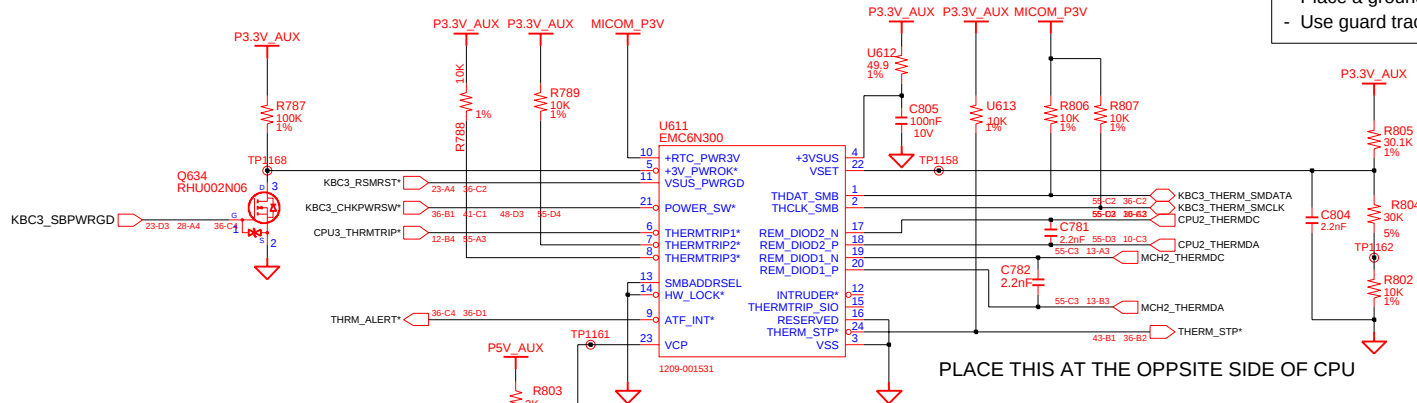
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CPU / DDR2 Thermal Sensor

Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



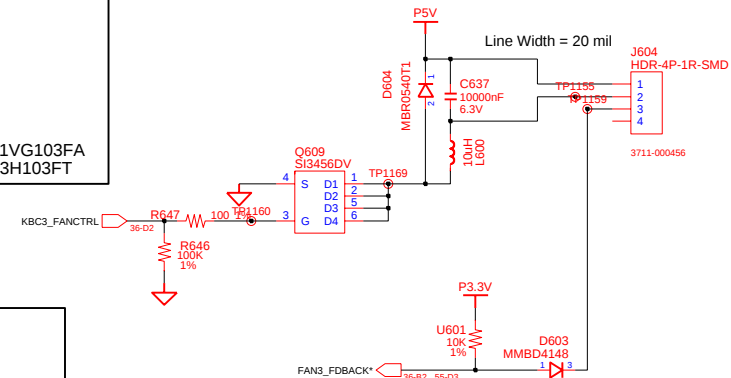
PLACE NEAR TO DDR2 SODIMM

$V_{set} = (T_p - 75) / 16$ Where $T_p = 75$ to 106 degree C
Set Trip point = 105 degree C
 $V_{set} = (105 - 75) / 16 = 1.875V$
Guardian Temp-tolerance = ± 3 degree C

TH1:
Panasonic 1% 0603 10K ohm @ 25 degree C.P/N: ERTJ1VG103FA
Mitsubishi 1% 0603 10K ohm @ 25 degree C.P/N: TH11-3H103FT

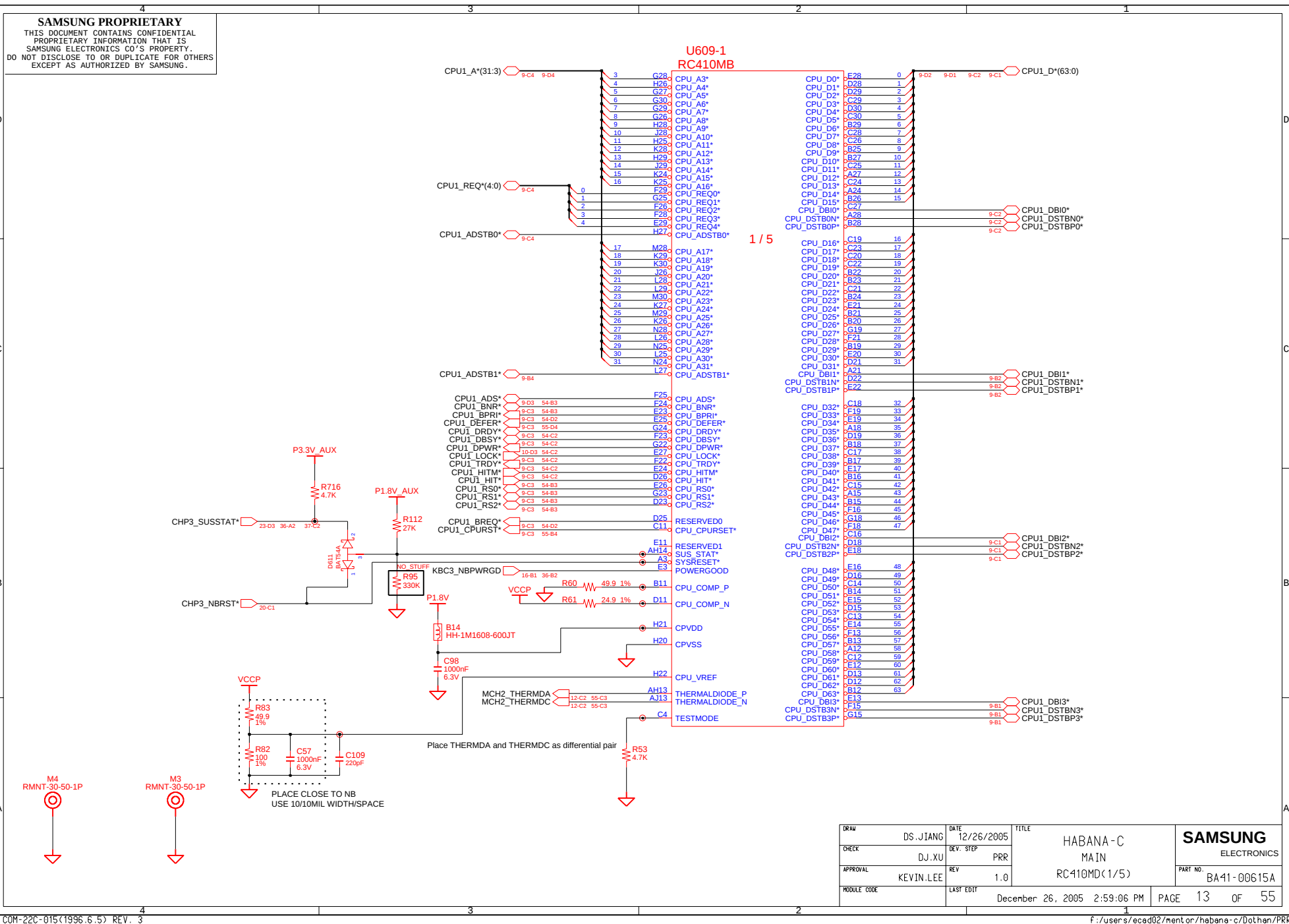
VCP voltage = $5V * TH1 / (TH1 + 2.21K)$
When TH1 is 10kohm, VCP is 4.1V.
If TH1 is 1kohm, VCP is 1.56V.

FAN Control Logic

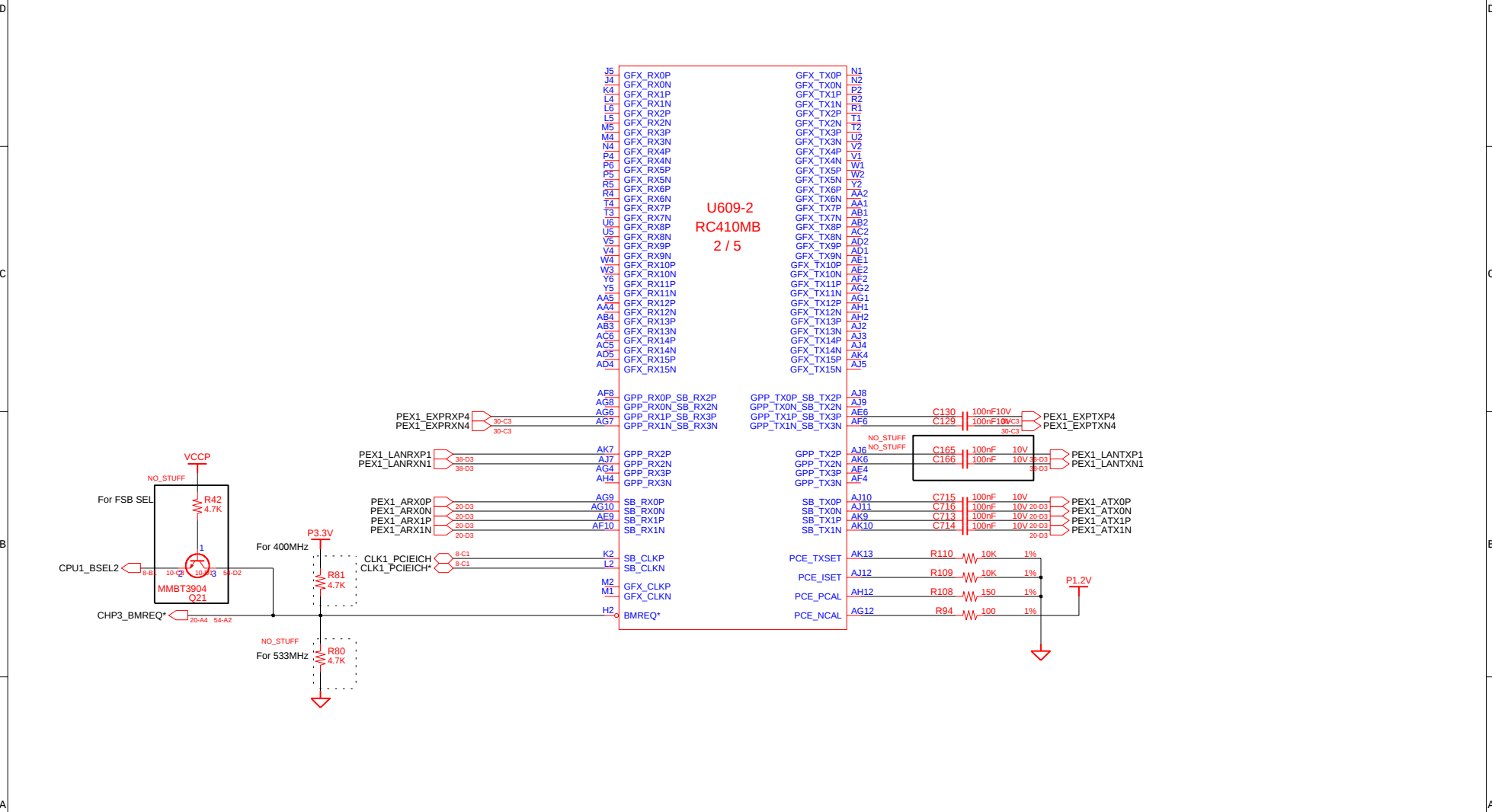


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	THERMAL SENSOR/FAN CONTRL	PART NO.	BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	12	OF 55

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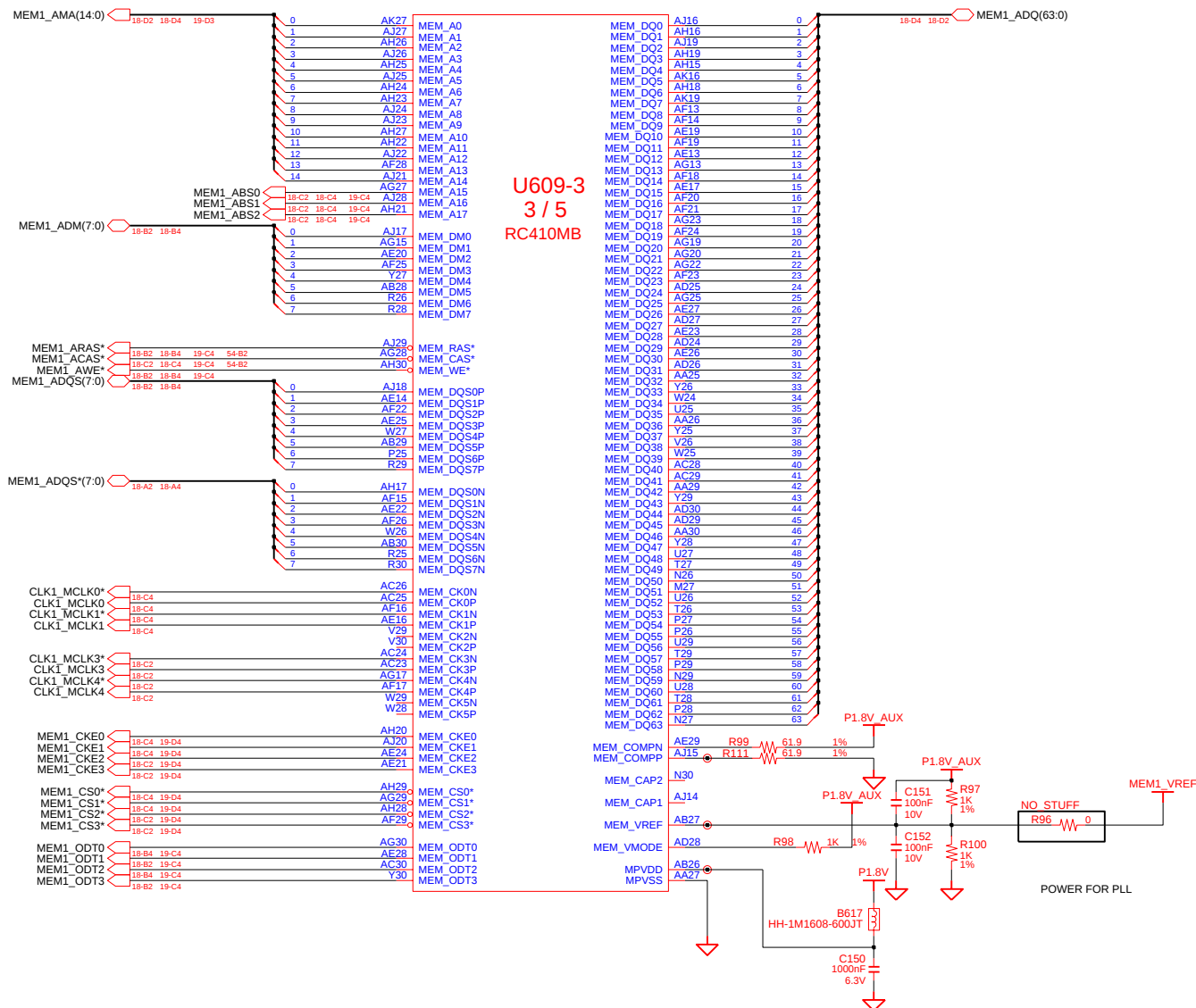


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CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM	
MODULE CODE						
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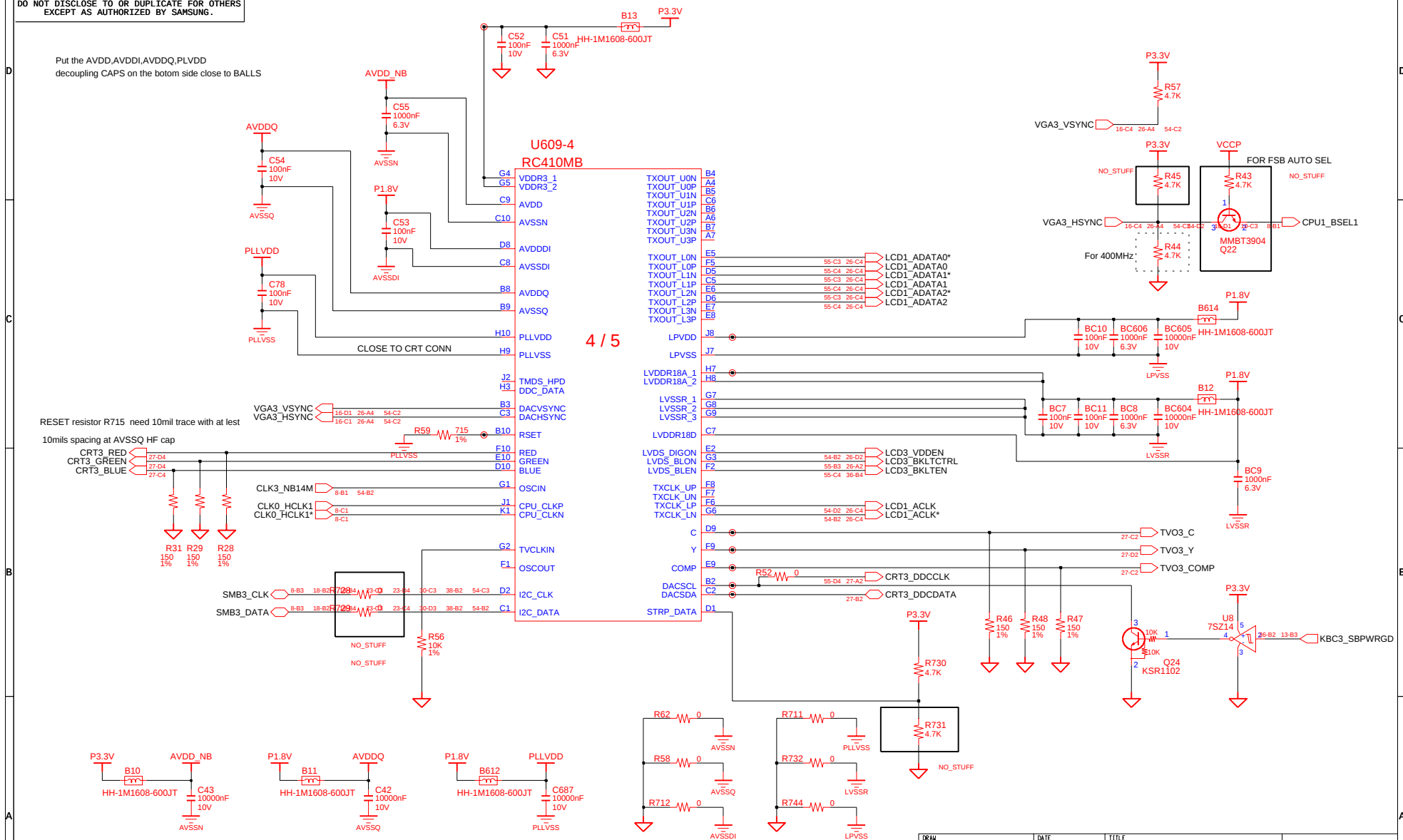
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CHECK	DJ. XU	DEV. STEP	PRR			
APPROVAL	KEVIN. LEE	REV	1.0			
MODULE CODE	LAST EDIT		December 26, 2005 2:59:06 PM			
				PART NO.	BA41-00615A	

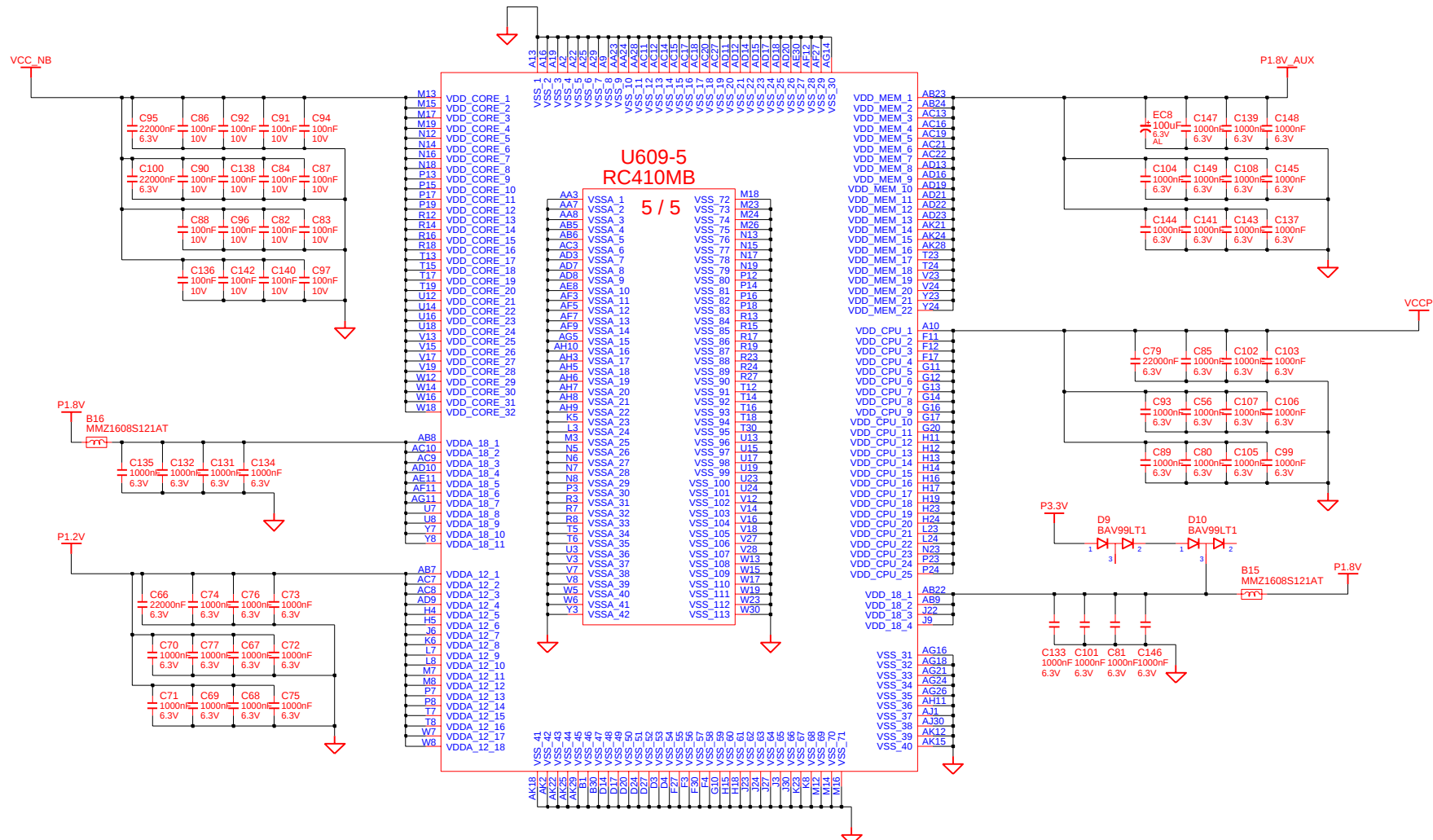
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Put the AVDD,AVDDI,AVDDQ,PLVDD
decoupling CAPS on the botom side close to BALLS



DRAM	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN RC410MD(4/5)	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
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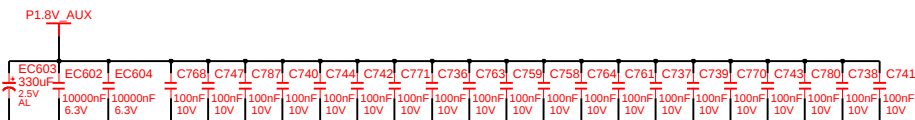
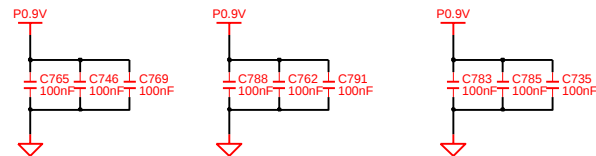
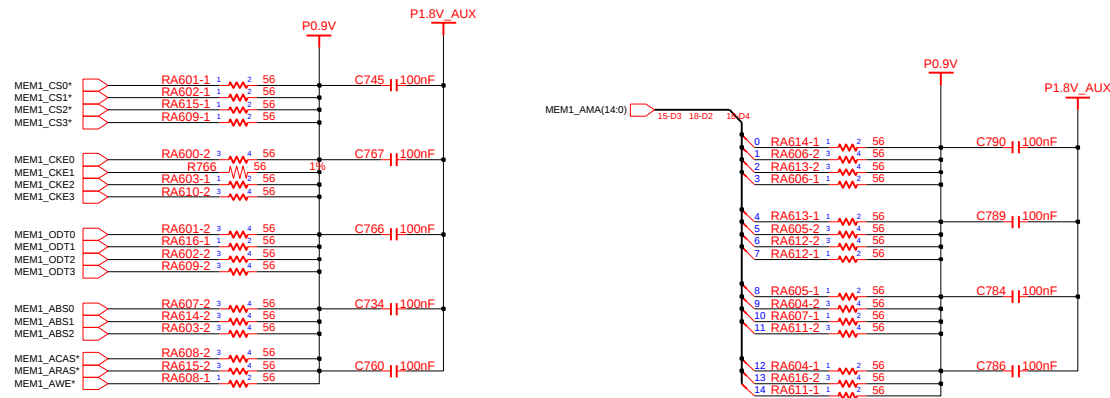
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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	LAST EDIT		December 26, 2005 2:59:06 PM			
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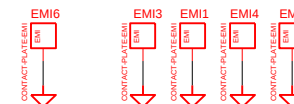
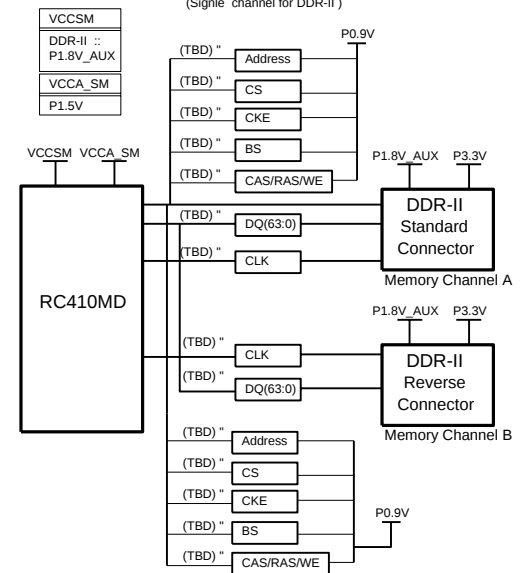
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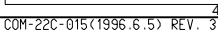


DE-COUPLING FOR SODIMM 1 AND 2

Memory Topology

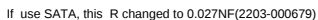


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR		MAIN	
APPROVAL	KEVIN.LEE	REV	1.0		DDR2 - TERMINATION	
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f:/users/ecad02/mentor/habana-c/Dothan/PRK

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D

C

B

A

D

C

B

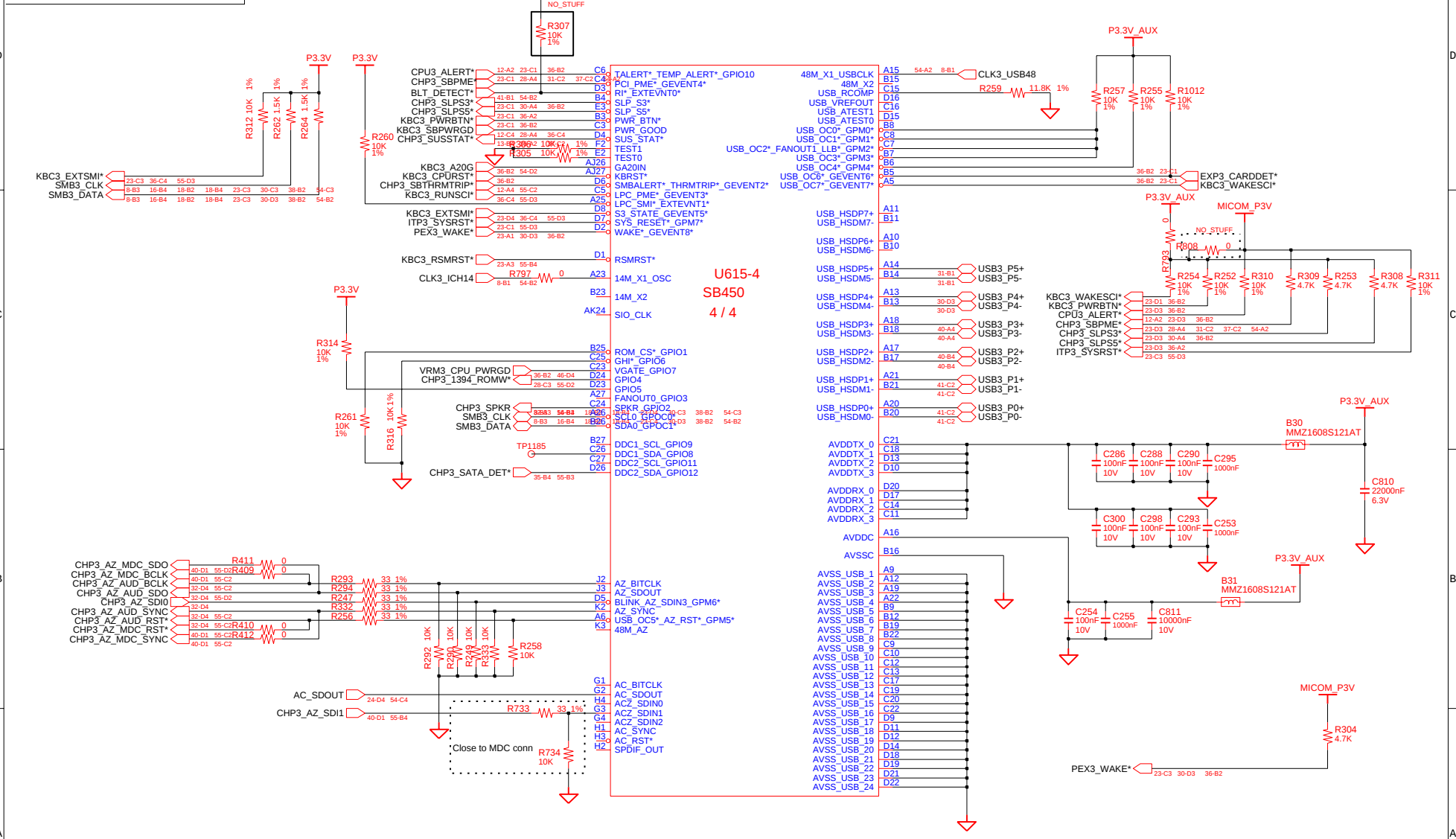
A

A30	VDDQ_1	E19
D30	VDDQ_2	E22
E24	VDDQ_3	E23
E25	VDDQ_4	E26
J5	VDDQ_5	VSS_15
K1	VDDQ_6	VSS_16
K5	VDDQ_7	VSS_17
N5	VDDQ_8	VSS_18
P5	VDDQ_9	VSS_19
R1	VDDQ_10	VSS_20
U5	VDDQ_11	VSS_21
U26	VDDQ_12	VSS_22
U30	VDDQ_13	VSS_23
V5	VDDQ_14	VSS_24
V26	VDDQ_15	VSS_25
Y1	VDDQ_16	VSS_26
Y26	VDDQ_17	VSS_27
AA5	VDDQ_18	VSS_28
AA26	VDDQ_19	VSS_29
AB5	VDDQ_20	VSS_30
AC30	VDDQ_21	VSS_31
AD5	VDDQ_22	VSS_32
AD26	VDDQ_23	VSS_33
AE1	VDDQ_24	VSS_34
AE5	VDDQ_25	VSS_35
AE26	VDDQ_26	VSS_36
AF6	VDDQ_27	VSS_37
AF7	VDDQ_28	VSS_38
AF24	VDDQ_29	VSS_39
AF25	VDDQ_30	VSS_40
AK1	VDDQ_31	VSS_41
AK4	VDDQ_32	VSS_42
AK26	VDDQ_33	VSS_43
AK30	VDDQ_34	VSS_44
M12	VDD_1	VSS_45
M13	VDD_2	VSS_46
M18	VDD_3	VSS_47
M19	VDD_4	VSS_48
N12	VDD_5	VSS_49
N13	VDD_6	VSS_50
N18	VDD_7	VSS_51
N19	VDD_8	VSS_52
V12	VDD_9	VSS_53
V13	VDD_10	VSS_54
V18	VDD_11	VSS_55
V19	VDD_12	VSS_56
W12	VDD_13	VSS_57
W13	VDD_14	VSS_58
W18	VDD_15	VSS_59
W19	VDD_16	VSS_60
A3	S5_3.3V_1	VSS_61
A7	S5_3.3V_2	VSS_62
E6	S5_3.3V_3	VSS_63
E7	S5_3.3V_4	VSS_64
E1	S5_3.3V_5	VSS_65
F5	S5_3.3V_6	VSS_66
E9	S5_1.8V_1	VSS_67
E10	S5_1.8V_2	VSS_68
E20	S5_1.8V_3	VSS_69
E21	S5_1.8V_4	VSS_70
E13	USB_PHY_1.8V_1	VSS_71
E14	USB_PHY_1.8V_2	VSS_72
E16	USB_PHY_1.8V_3	VSS_73
E17	USB_PHY_1.8V_4	VSS_74
C30	CPU_PWR	VSS_75
AG6	V5_VREF	VSS_76
A24	AVDDCK	VSS_77
B24	AVSSCK	VSS_78
A4	VSS_1	VSS_79
A8	VSS_2	VSS_80
A29	VSS_3	VSS_81
B28	VSS_4	VSS_82
C1	VSS_5	VSS_83
E5	VSS_6	VSS_84
E8	VSS_7	VSS_85
E11	VSS_8	VSS_86
E12	VSS_9	VSS_87
E15	VSS_10	VSS_88
E18	VSS_11	VSS_89
		VSS_90
		VSS_91
		VSS_92
		VSS_93
		VSS_94
		VSS_95
		VSS_96
		VSS_97
		VSS_98

U615-3
SB450
3 / 4

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	SB450(3/4)		
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	22 OF 55	

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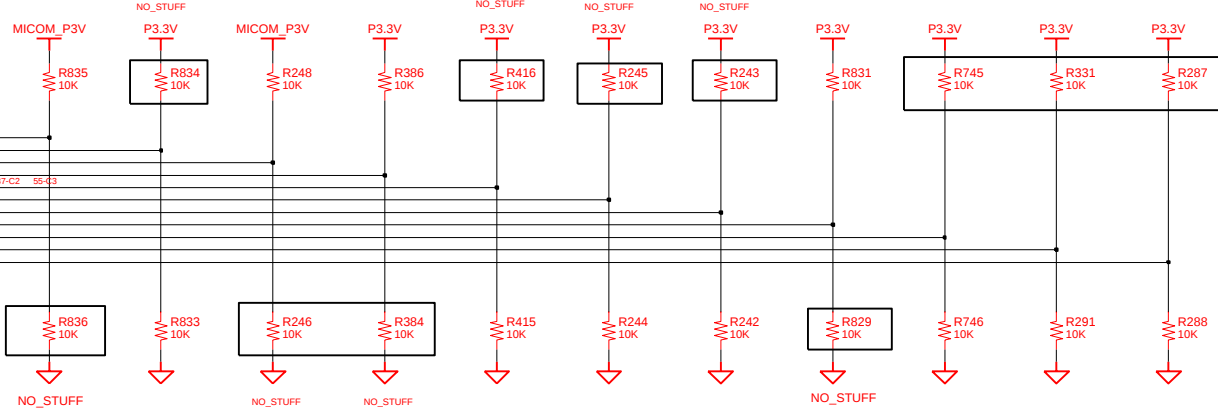


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN SB450(4/4)	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	23	OF 55

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REQUIRED SYSTE STRAPS

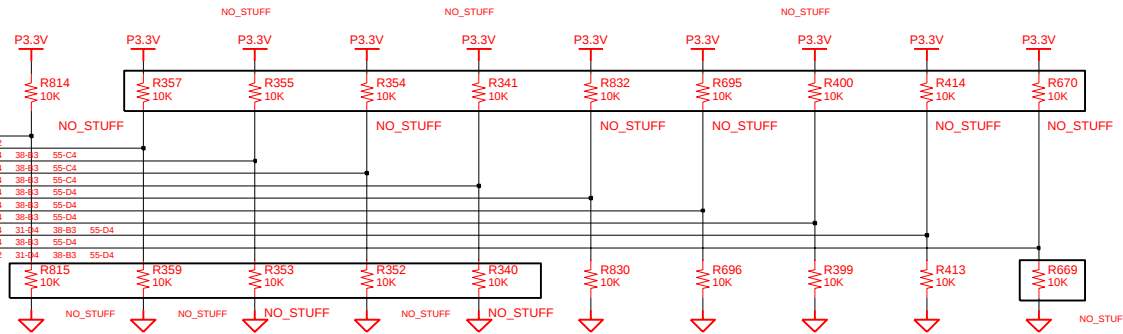
AUTO_ON* 20-A2 54-C4
AC_SDOUT 23-B4 54-C4
RTC_CLK 20-A2 54-C4
LPC3_LFRAME 20-A2 25-A3 25-B4 25-C3 36-C2 37-C2 55-A3
CLK3_PCLKCB 20-D2 29-A4 54-D1
CLK3_PCLKSIO_DS 20-D2 37-C2 55-D2
CLK3_PCLKSIO 20-D2 37-C2 55-B4
CLK3_PCLKFWH 20-D2 25-B4 25-C4 55-B4
CLK3_PCLKMICOM 20-D2 36-C2 55-B3
CLK3_DBG LPC 20-D2 25-B3 54-D1
PCI3_CLK8 20-D2 54-B2



	AUTO_ON	AC_SDOUT	RTC_CLK	LPC3_FRAME	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	PCI3_CLK6	PCI3_CLK7,PCI3_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	Enable thermtrip* on power up	48MHZ OSC MODE	USB PHY PWRDOWN DISABLE	USE USB PLL	PCI-E lane auto detect	CPU I/F = KB	ROM TYPE H.H = PCI ROM H.L = LPCROM I LPC ADDRESS MAPPED BELOW 1 M
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXRERNAL RTC	Disable thermtrip* on power up	48MHZ XTAL MODE	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	Force PCI-E to lane2	CPU I/F = P4	LPC ADDRESS MAPPED TO TOP 4G L.H = LPC ROM II L.L = FWH ROM

DEBUS STRAPS

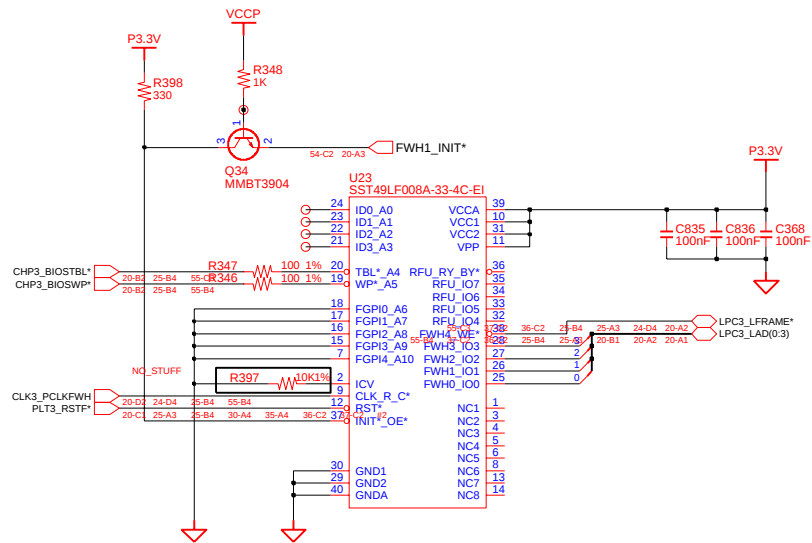
IDE5_DACK* 21-D2 35-C3 54-C2
PCI3_AD(31) 20-D2 28-C4 31-D4 38-A3 55-C4
PCI3_AD(30) 20-D2 28-C4 31-D4 38-A3 55-C4
PCI3_AD(29) 20-D2 28-C4 31-D4 38-A3 55-C4
PCI3_AD(28) 20-D2 28-C4 31-D4 38-A3 55-C4
PCI3_AD(27) 20-D2 28-C4 31-D4 38-A3 55-D4
PCI3_AD(26) 20-D2 28-C4 31-D4 38-A3 55-D4
PCI3_AD(25) 20-D2 28-C4 31-D4 38-A3 55-D4
PCI3_AD(24) 20-D2 28-B4 28-C4 31-D4 38-B3 55-D4
PCI3_AD(23) 20-D2 28-C4 31-D4 38-A3 55-D4
20-D2 28-C4 31-C2 31-A3 38-B3 55-D4



	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0		STRAPS	
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	24 OF 55	

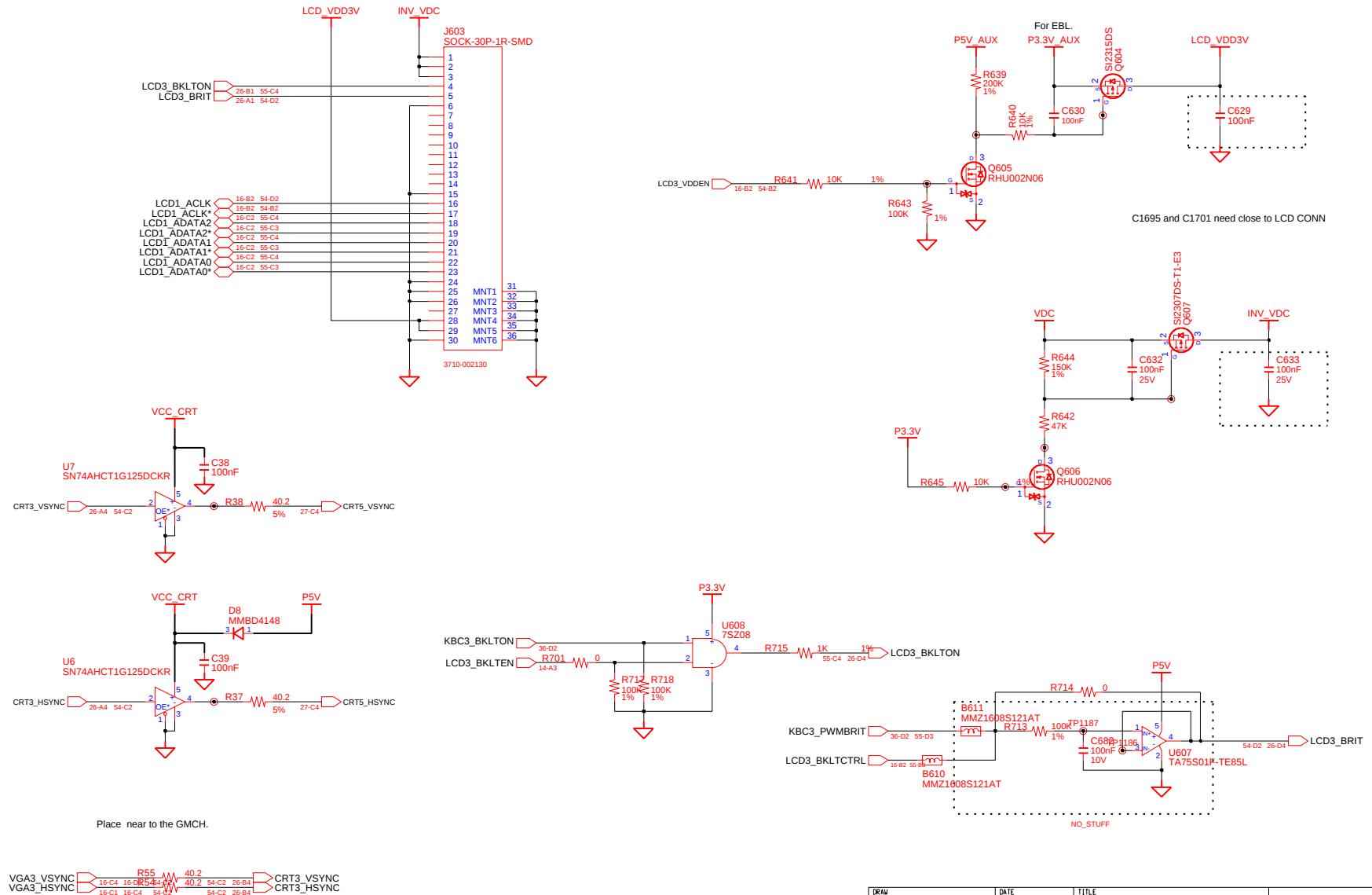
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02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG
CHECK	DJ.XU	DEV. STEP	PRR		MAIN	ELECTRONICS
APPROVAL	KEVIN.LEE	REV	1.0		FIRMWARE HUB	PART NO.
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM			BA41-00615A
				PAGE	25	OF 55

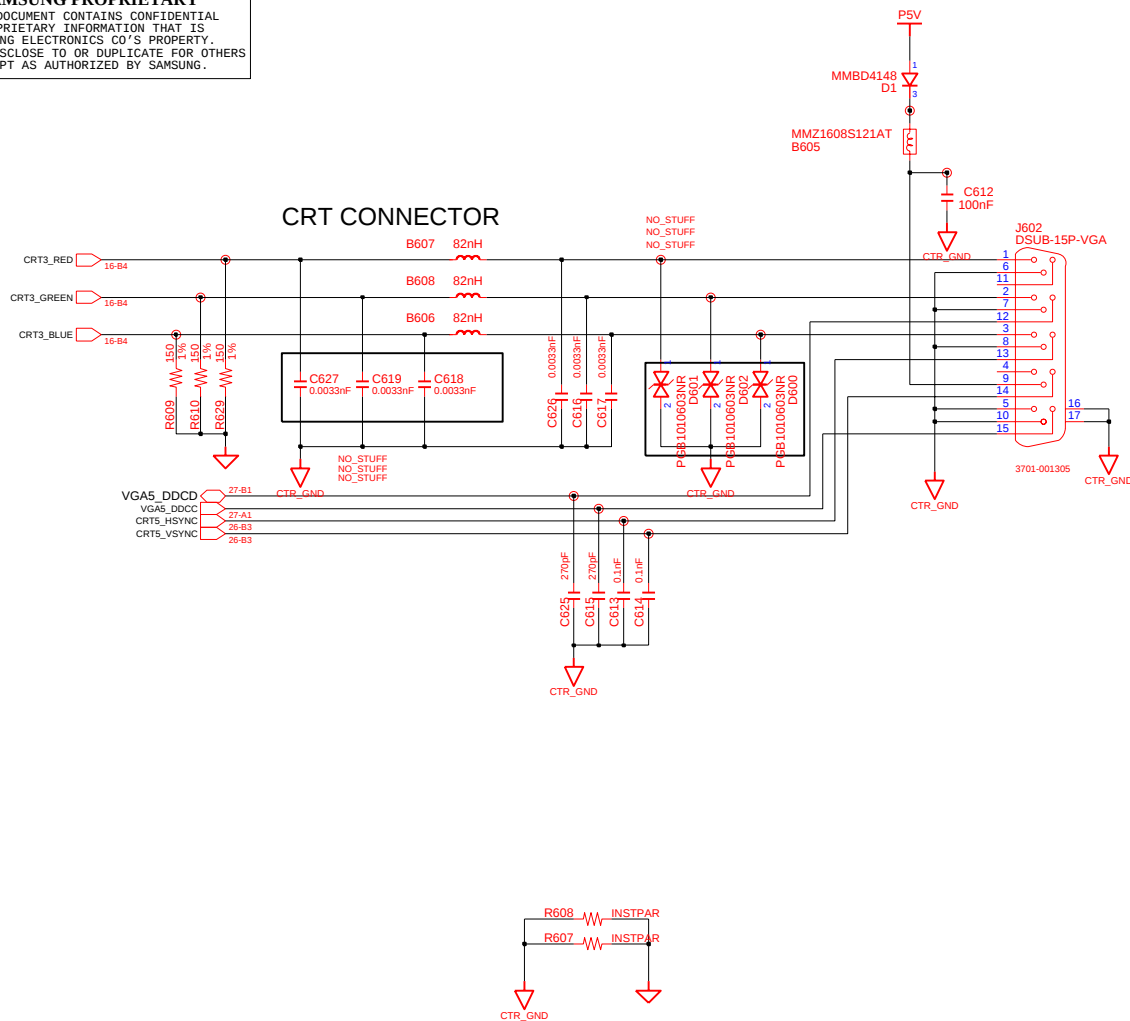
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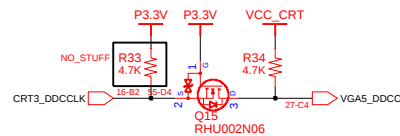
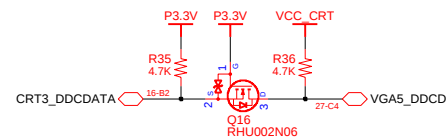
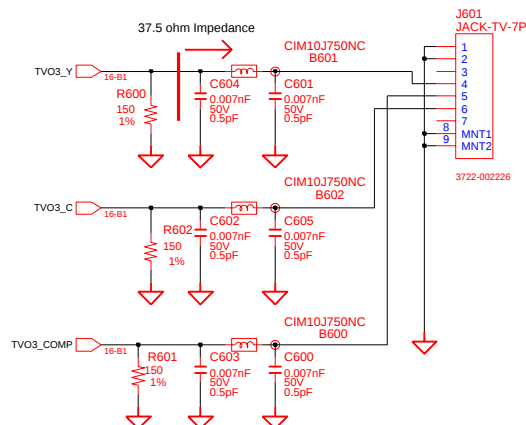
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CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	26	OF 55

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CRT CONNECTOR



TV-OUT(S-VHS,COMPONENT)



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG
CHECK	DJ.XU	DEV. STEP	PRR			ELECTRONICS
APPROVAL	KEVIN.LEE	REV	1.0		CRT AND TV-OUT	PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	27	OF 55



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J617 COMBO-94P-FRAME

EXPRESS CARD

Type 1 module
Type 2 module

U27 R5538D001-TR-F

CHP3 SLPS3*
PLT3_RSTP*

DRW DS.JIANG 12/26/2005
CHECK DJ.XU DEV. STEP PRR
APPROVAL KEVIN.LEE REV 1.0
MODULE CODE LAST EDIT

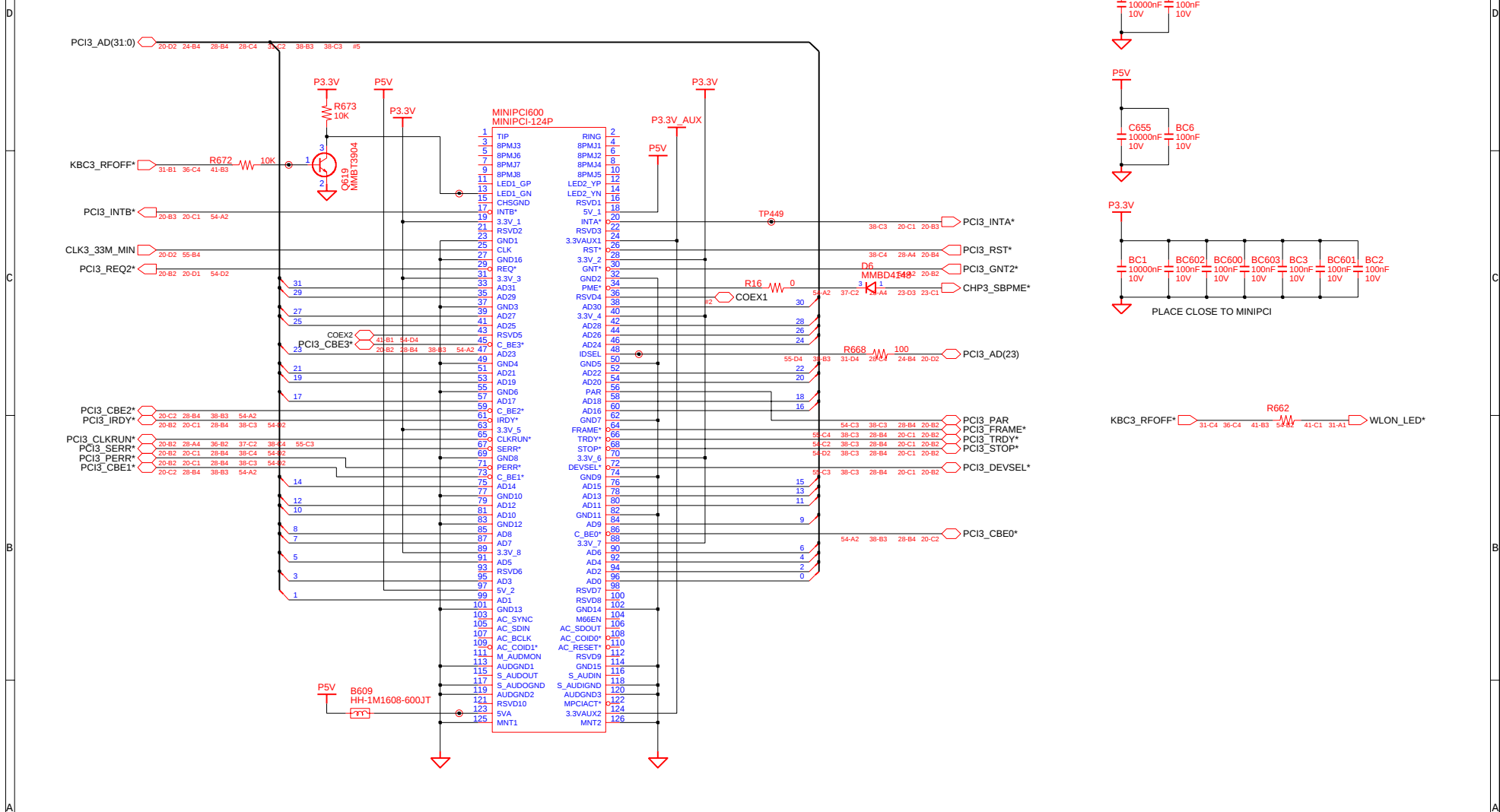
HABANA-C
EXPRESS CARD

SAMSUNG ELECTRONICS
PART NO. BA41-00615A

December 26, 2005 2:59:06 PM PAGE 30 OF 55

COM-22C-015(1996.6.5) REV. 3

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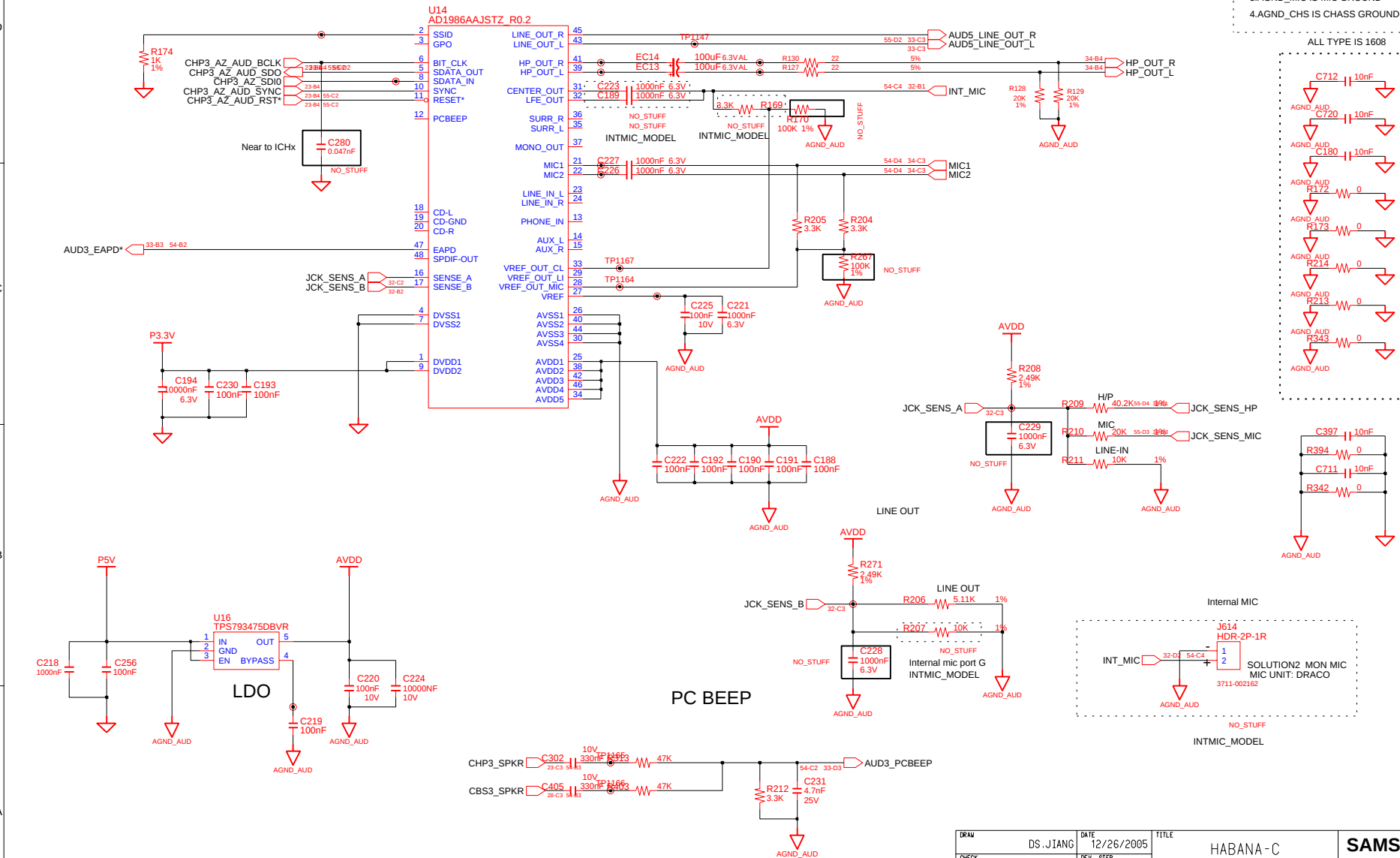


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	31	OF 55
MODULE CODE	undefined					

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- 1.AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASS GROUND

ALL TYPE IS 1608



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	32	OF 55

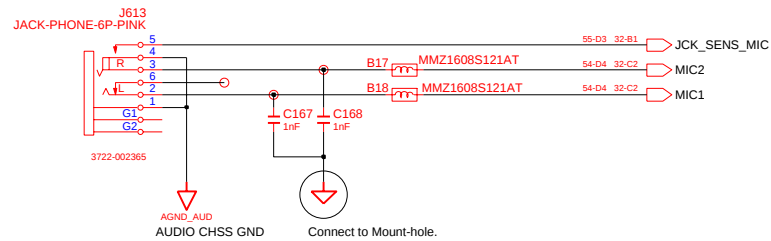
A



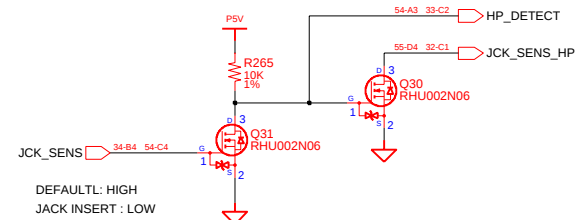
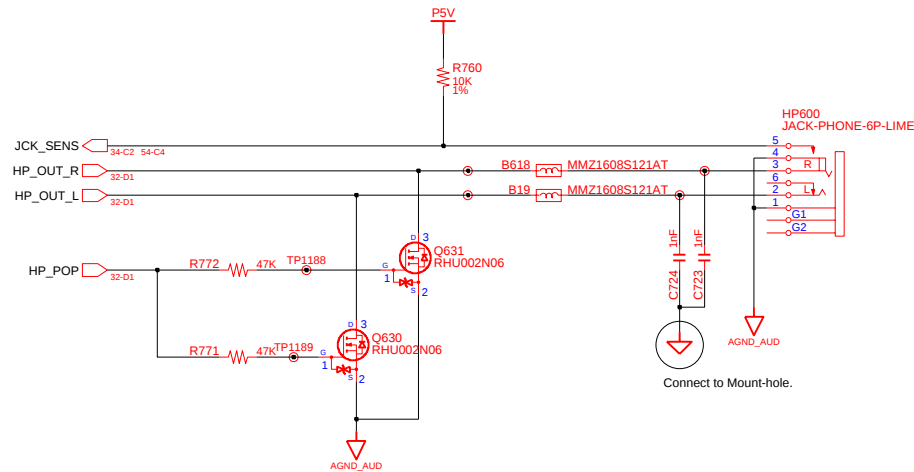
COM-22C-015(1996.6.5) REV. 3

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MIC JACK



HEADPHONE

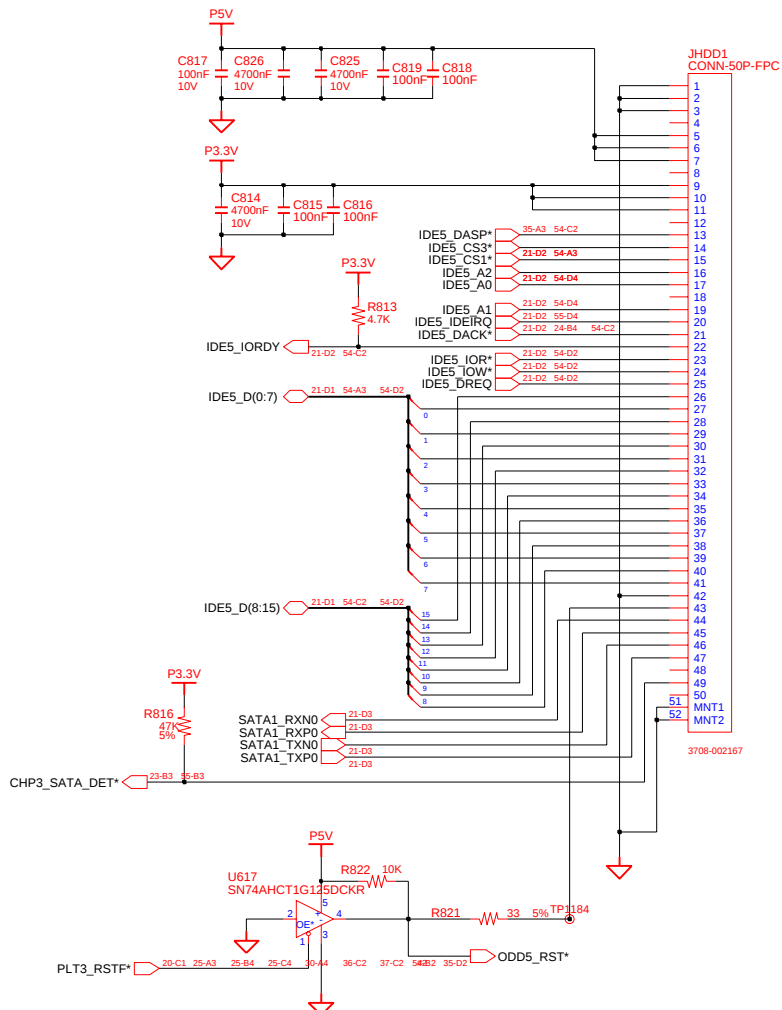


The traces led to Audio Jacks have the width over 10mil

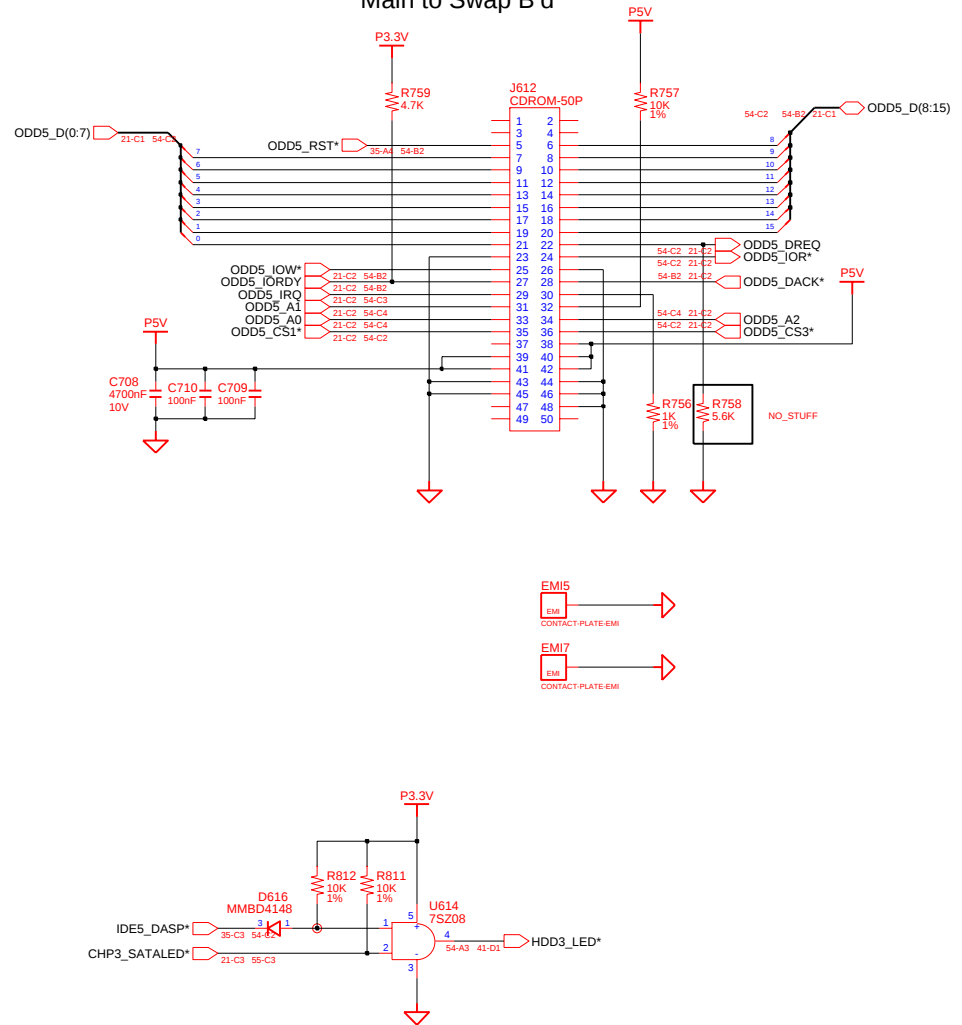
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	34	OF 55

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Main to HDD

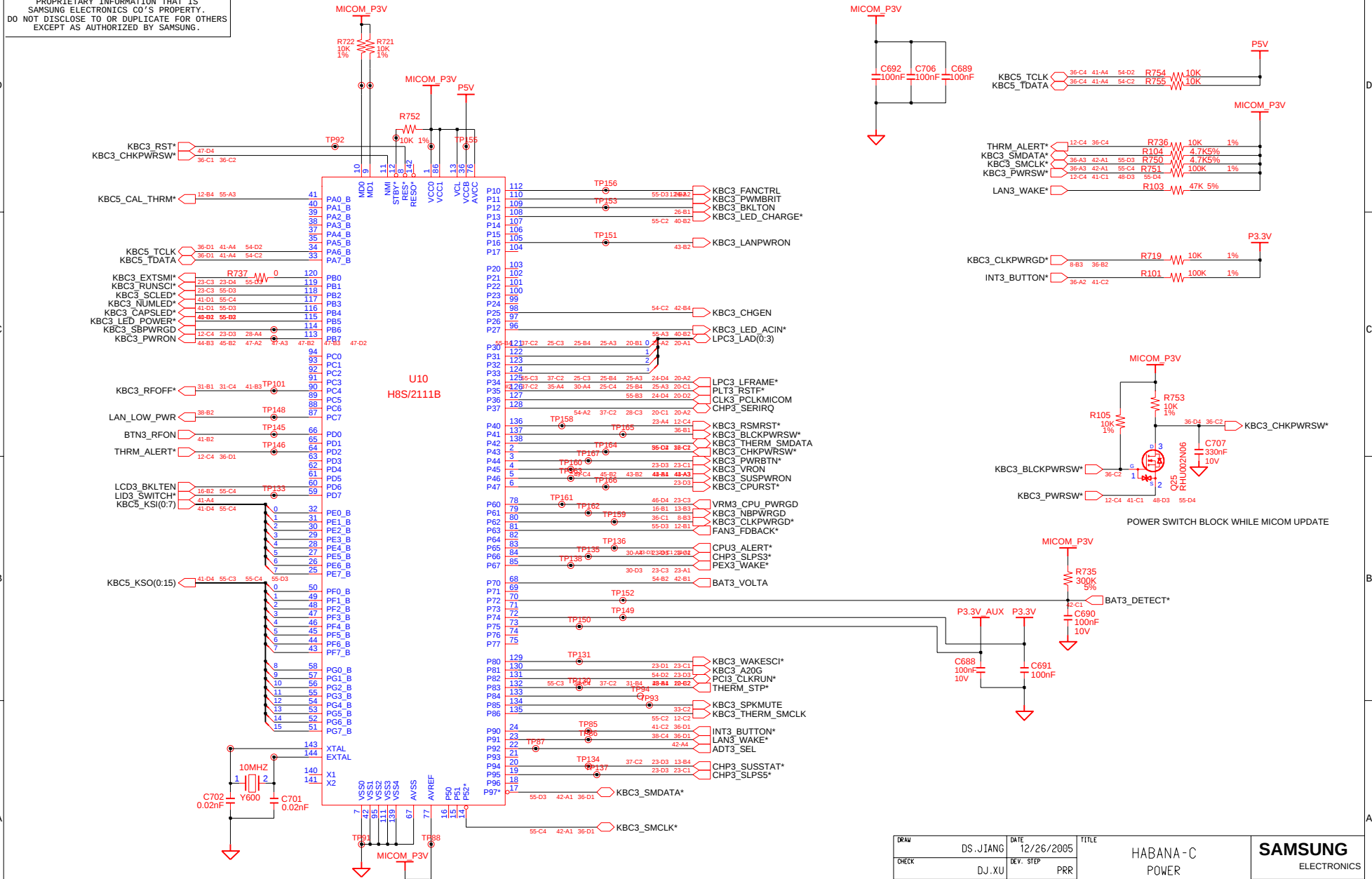


Main to Swap B'd



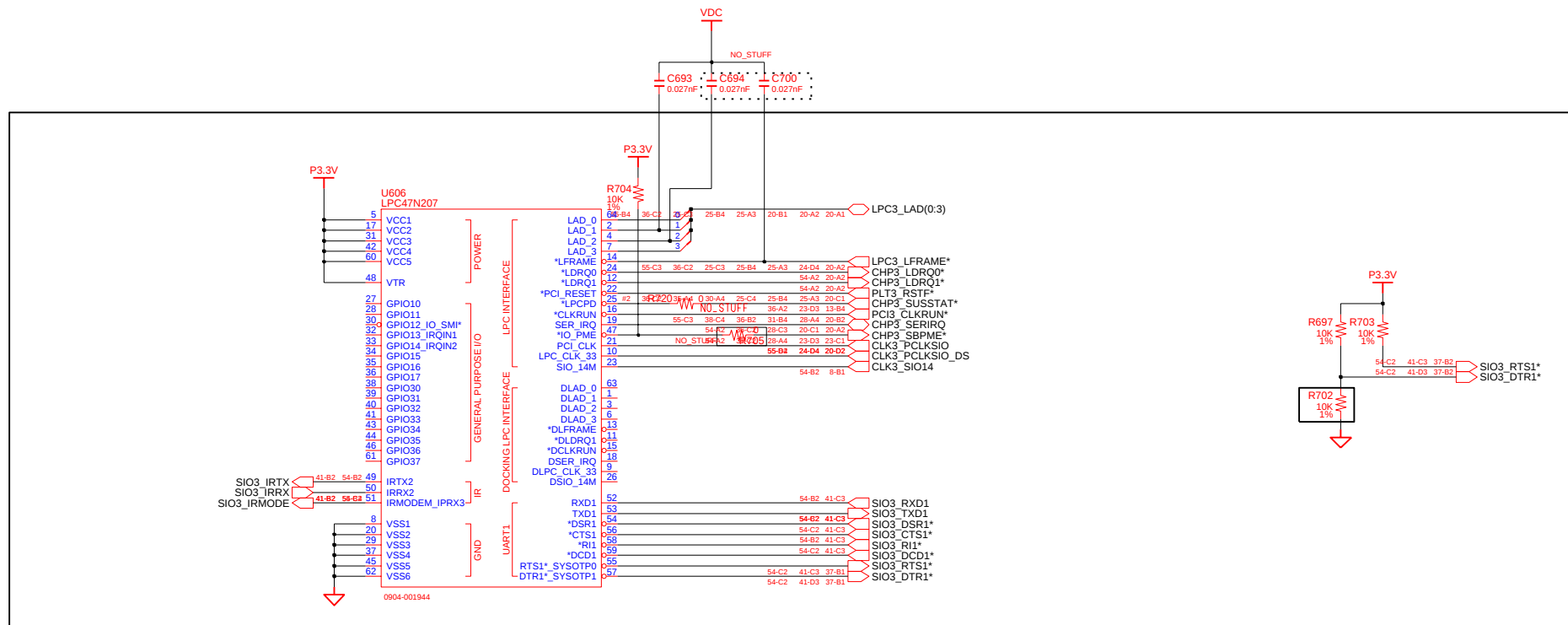
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	35	OF 55

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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER MICOM	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	36	OF 55

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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN LPC	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	37 OF 55	

BCM4401E pin to pin

DRAM	DS. JIANG	DATE	12/26/2005	HABANA-C MAIN LAN	SAMSUNG ELECTRONICS
CHECK	DJ. XU	DEV. STEP	PRR		
APPROVAL	KEVIN. LEE	REV	1.0		
PART NO.			BA41-00615A		
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	38 OF 55

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U17-2 BCM5751MKFBG 2/2

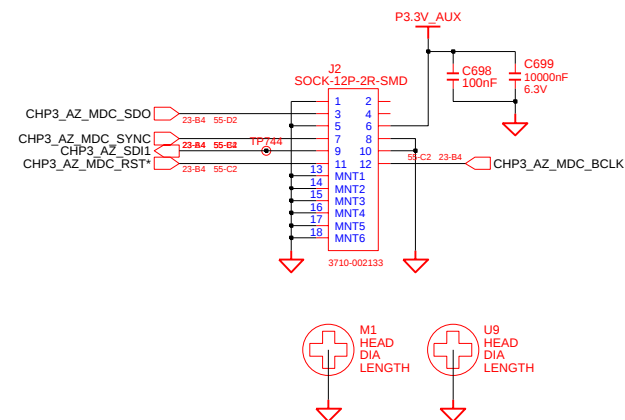
Pin List:

Pin	Function
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E5	VDDC_2
E6	VDDC_3
E7	VDDC_4
E8	VDDC_5
E9	VDDC_6
F5	VDDC_7
F10	VDDC_8
G4	VDDC_9
J4	VDDC_10
J5	VDDC_11
J10	VDDC_12
K4	VDDC_13
K5	VDDC_14
K6	VDDC_15
K7	VDDC_16
K8	VDDC_17
K8	VDDC_18
F13	AVDDL_AVDD_1
F13	AVDDL_AVDD_2
G14	GPHY_PLLVDD_PLLVDD
M8	PCIE_PLLVDD_DC
M6	PCIE_SDSVDD_DC
N12	XTALO
P12	XTALI
A10	RDAC
D8	PCIE_TST_DC
D12	TRST*
D7	TCK
H12	TDI
O6	TDO
C11	TMS
M12	DC_NC_1
N14	DC_NC_2
P14	DC_NC_3
L5	DC_NC_3
K9	DC_2
L11	DC_3
M11	DC_4
H11	DC_4
M9	DC_6
K10	DC_7
L12	DC_NC_4
M13	DC_8
L8	DC_NC_5
L7	NC_DC_1
M10	NC_DC_2
N11	NC_1
N11	NC_2
P11	NC_3
B4	V_S_1
B7	V_S_2
B2	V_S_3
B1	V_S_4
B6	V_S_5
B5	V_S_6
B3	V_S_7
B8	V_S_8
G5	V_S_9
G6	V_S_10
G7	V_S_11
G8	V_S_12
G9	V_S_13
H5	V_S_14
H6	V_S_15
H7	V_S_16
H8	V_S_17
H9	V_S_18
H10	V_S_19
H11	V_S_20
H12	V_S_21
H13	V_S_22
H14	V_S_23
H15	V_S_24
H16	V_S_25
H17	V_S_26
H18	V_S_27
H19	V_S_28
H20	V_S_29
H21	V_S_30
H22	V_S_31
H23	V_S_32
H24	V_S_33
H25	V_S_34
H26	V_S_35
H27	V_S_36
H28	V_S_37
H29	V_S_38
H30	V_S_39
H31	V_S_40
H32	V_S_41
H33	V_S_42
H34	V_S_43
H35	V_S_44
H36	V_S_45
H37	V_S_46
H38	V_S_47
H39	V_S_48
H40	V_S_49
H41	V_S_50
H42	V_S_51
H43	V_S_52
H44	V_S_53
H45	V_S_54
H46	V_S_55
H47	V_S_56
H48	V_S_57
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H52	V_S_61
H53	V_S_62
H54	V_S_63
H55	V_S_64
H56	V_S_65
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H59	V_S_68
H60	V_S_69
H61	V_S_70
H62	V_S_71
H63	V_S_72
H64	V_S_73
H65	V_S_74
H66	V_S_75
H67	V_S_76
H68	V_S_77
H69	V_S_78
H70	V_S_79
H71	V_S_80
H72	V_S_81
H73	V_S_82
H74	V_S_83
H75	V_S_84
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H122	V_S_131
H123	V_S_132
H124	V_S_133
H	

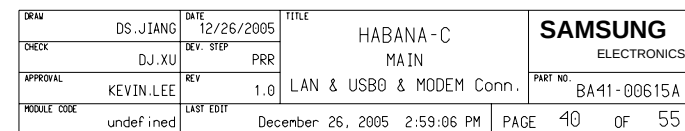
COM-22C-015(1996.6.5) REV. 3

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H1286	H5015

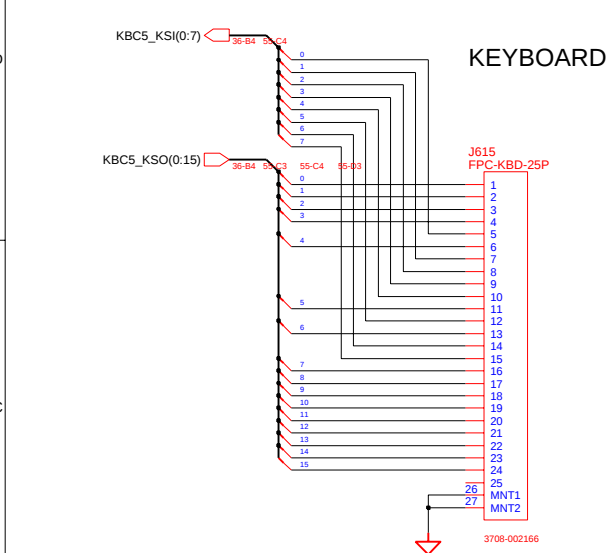
MDC Connector



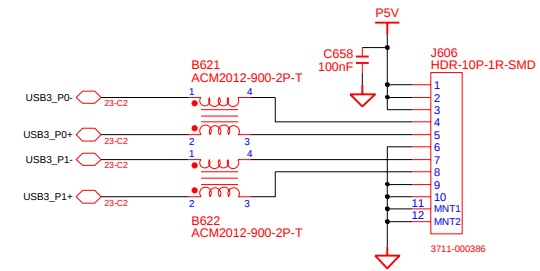
Schematic diagram of the LED driver circuit for the LED600 and LED601. The circuit includes two LED drivers. The first driver, for LED600 (SML-020MLT-T86), uses a BSS84 Q635 MOSFET and a TP232 transistor. It is powered by MICOM P3V and has a feedback network with R824 (150 ohms) and R823 (10K). The second driver, for LED601 (CL-150PG-CD-T), uses a BSS84 Q636 MOSFET and a TP237 transistor. It is powered by MICOM P3V and has a feedback network with R826 (150 ohms) and R825 (10K). The output of the second driver is connected to the LED601. The circuit also includes a P3.3V AUX supply, a TS7S14F comparator, and a TP184 transistor. The output of the comparator is connected to the LED601. The circuit is powered by KBC3_LED_ACIN* and KBC3_LED_CHARGE*.



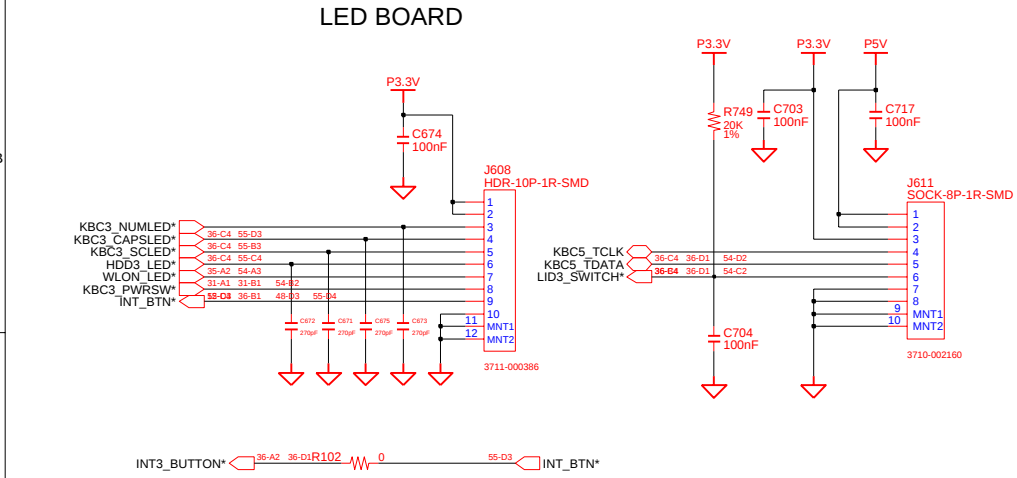
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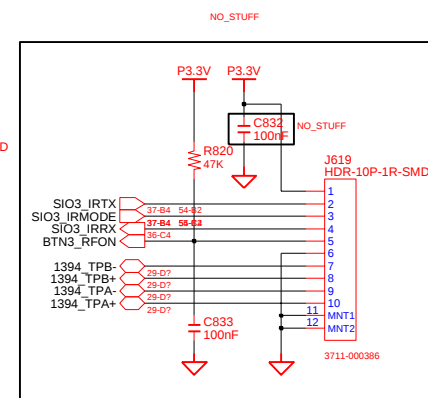
USB_SIO BOARD



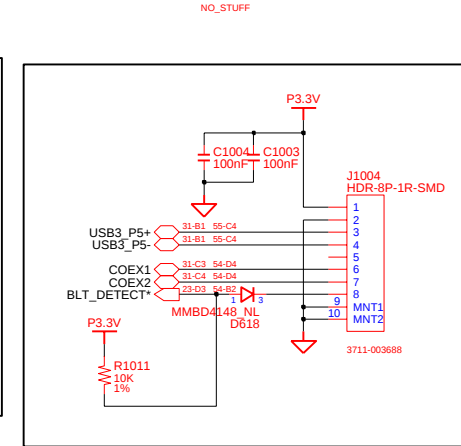
TOUCHPAD



1394_IR BOARD

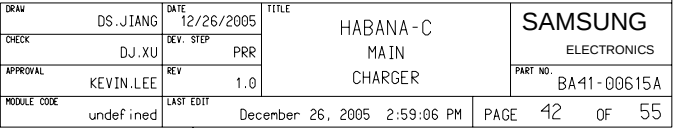


Bluetooth Interface



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN	BA41-00615A	
APPROVAL	KEVIN.LEE	REV	1.0	B'D TO B'D CONNECTOR	PART NO.	
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	41	OF 55

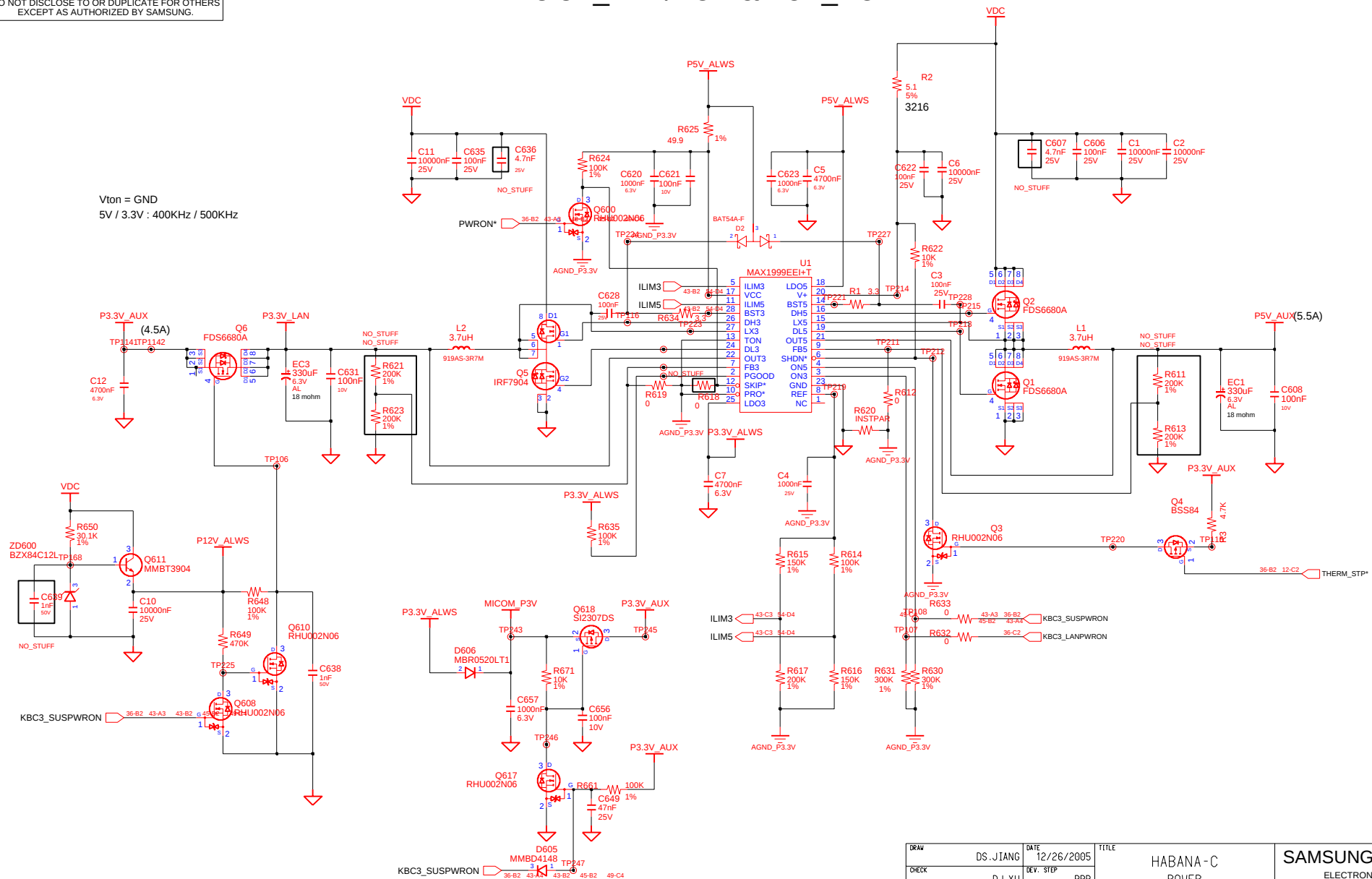
CHARGER & POWER MANAGEMENT



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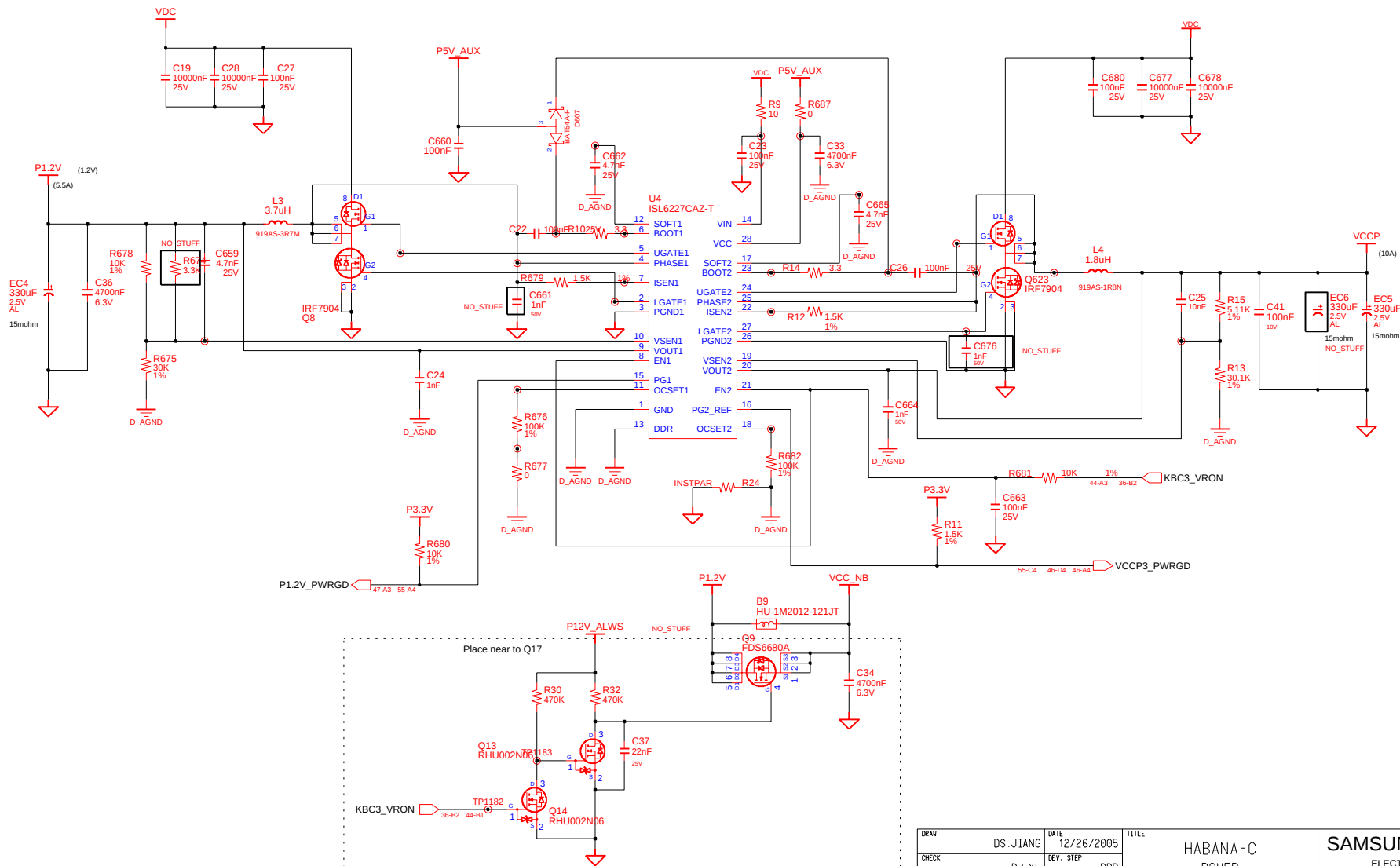
P3.3V_LAN/AUX & P5V_AUX

Vton = GND
5V / 3.3V : 400KHz / 500KHz



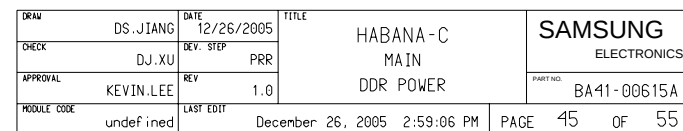
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0		P3.3V ALWAYS & P5V_AUX	
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	43	OF 55

P1.2V(VCC_NB) & VCCP (1.05V)

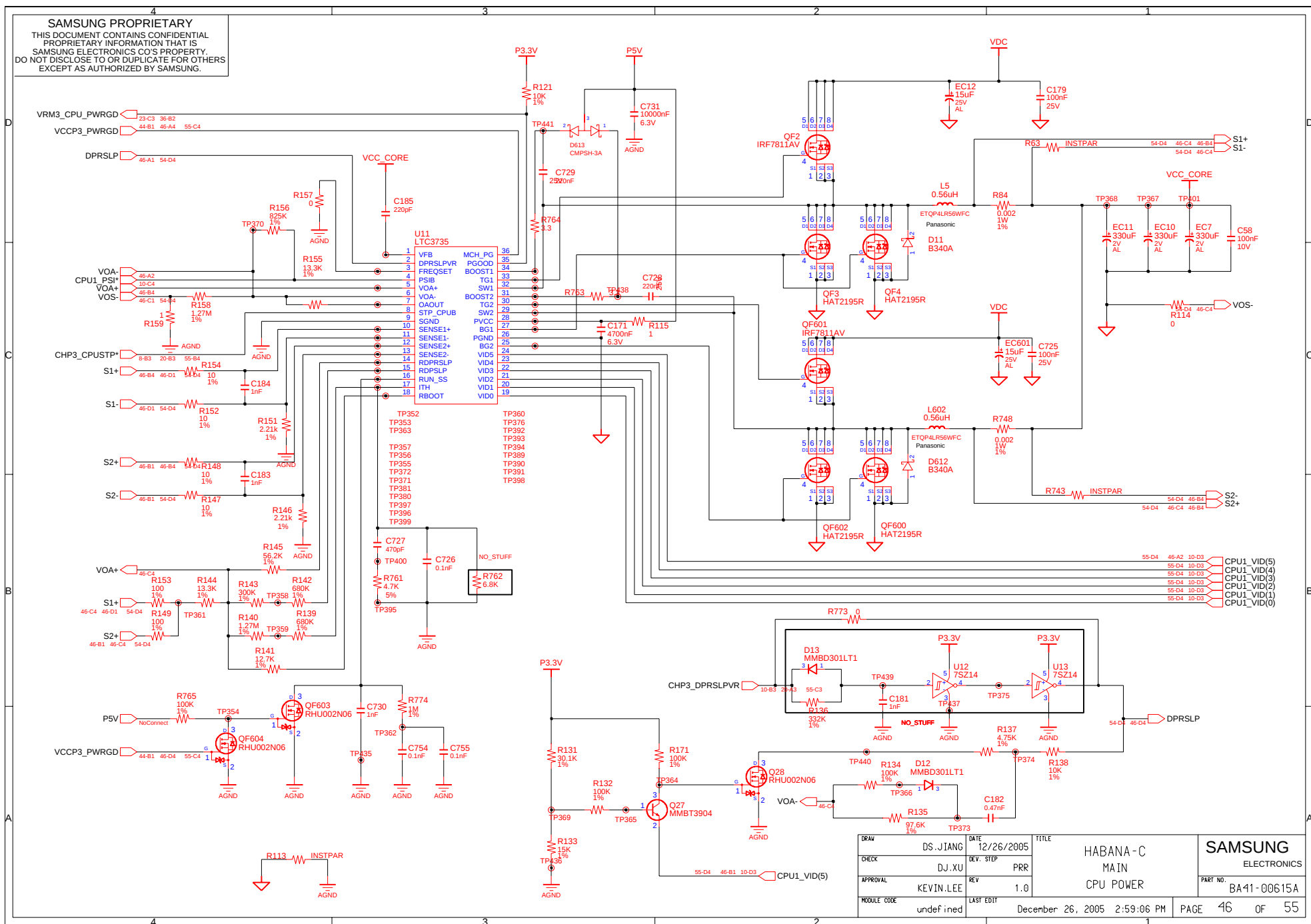


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER P1.2V & VCCP	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	44	OF 55

DDR2 Power

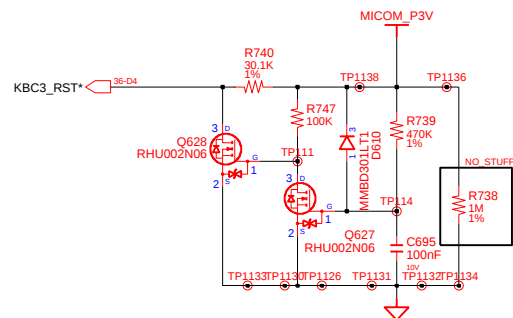


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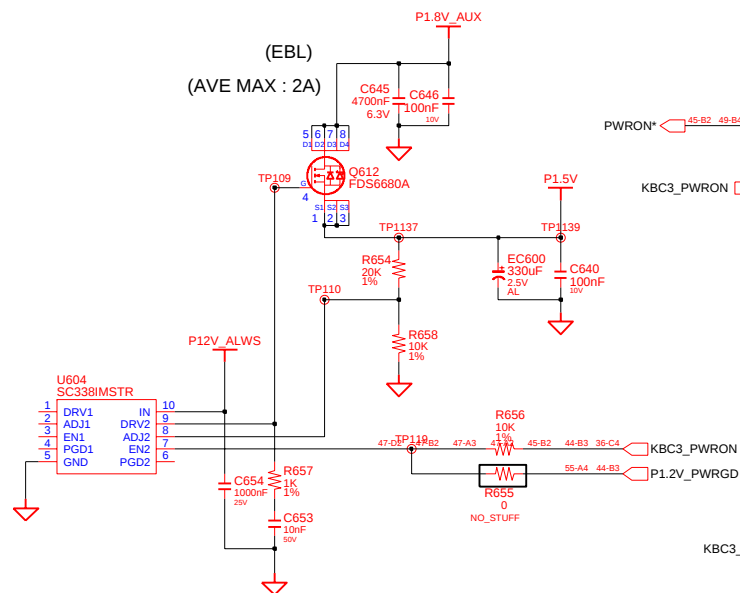


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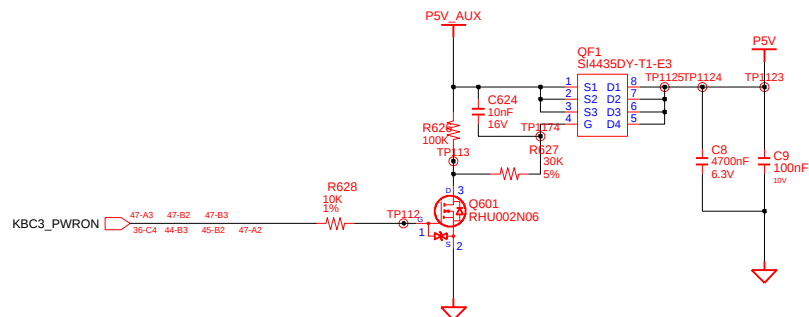
MICOM RESET



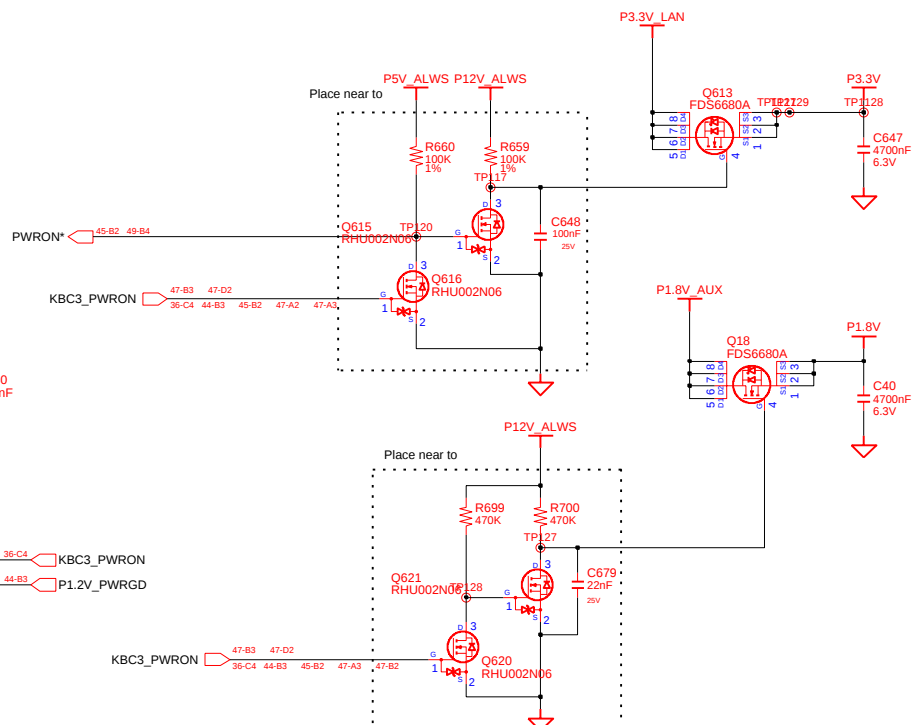
P1.5V POWER



Switched Power On (P5V)

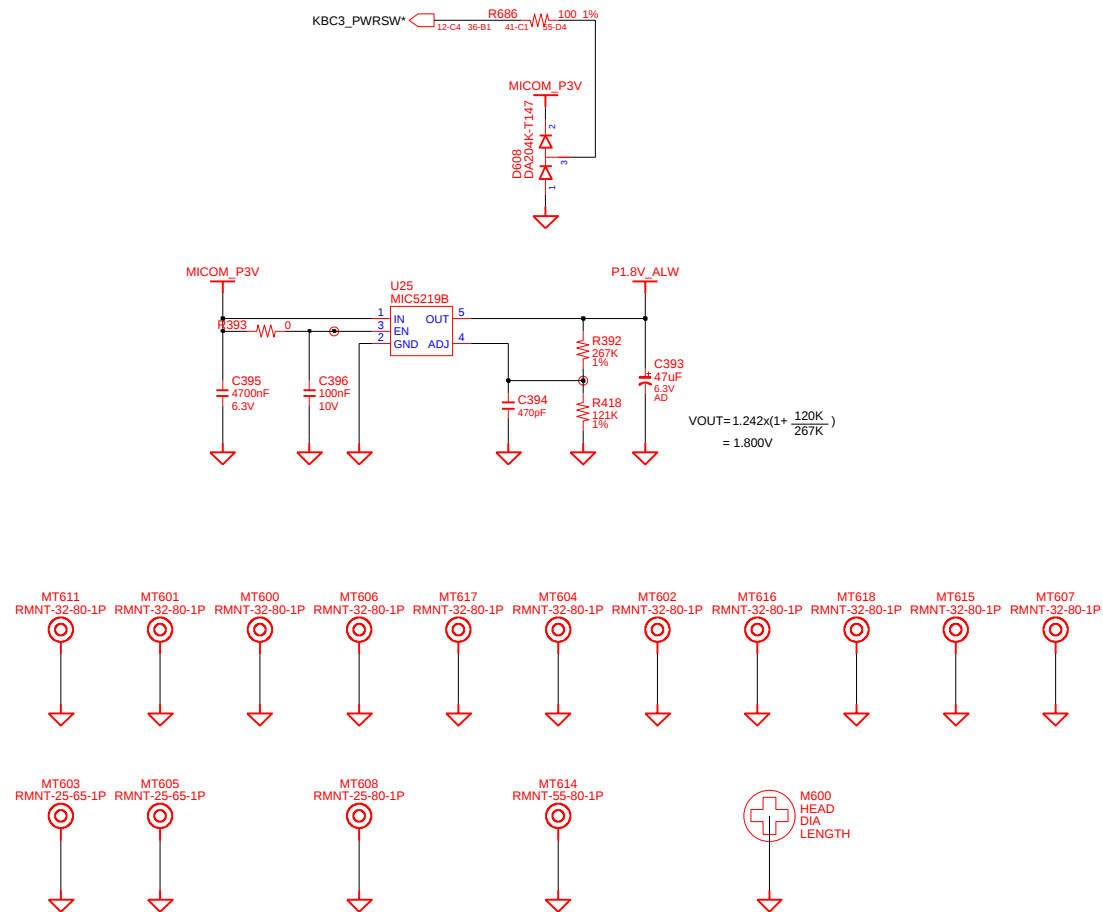


Switched Power On (P3.3V & 1.8V)

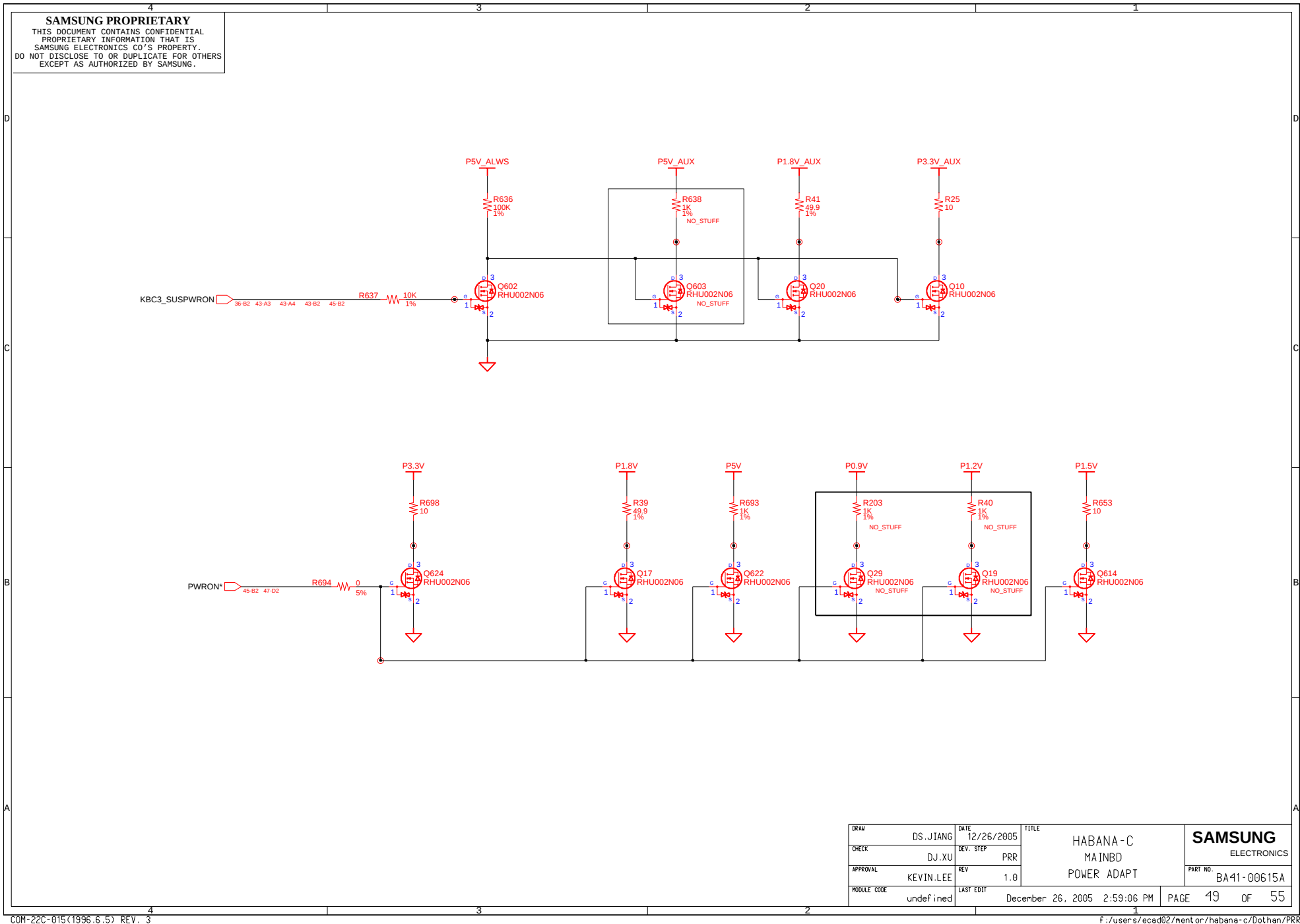


DRAWN	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN	SAMSUNG ELECTRONICS
CHECK	DJ.XU	REV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
				MICOM & SWITCHED POWER	PART NO.	BA41-00615A
MODULE CODE	undefined	LAST EDIT		December 26, 2005 2:59:06 PM	PAGE	47 OF 55

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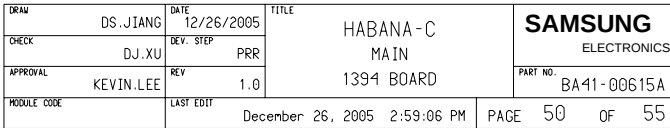


DRAW	DS..JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG
CHECK	DJ.XU	DEV. STEP	PRR			ELECTRONICS
APPROVAL	KEVIN.LEE	REV	1.0	P1.2V & P2.5V AUX POWER	PART NO.	BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	48	OF 55



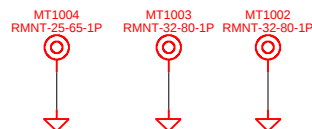
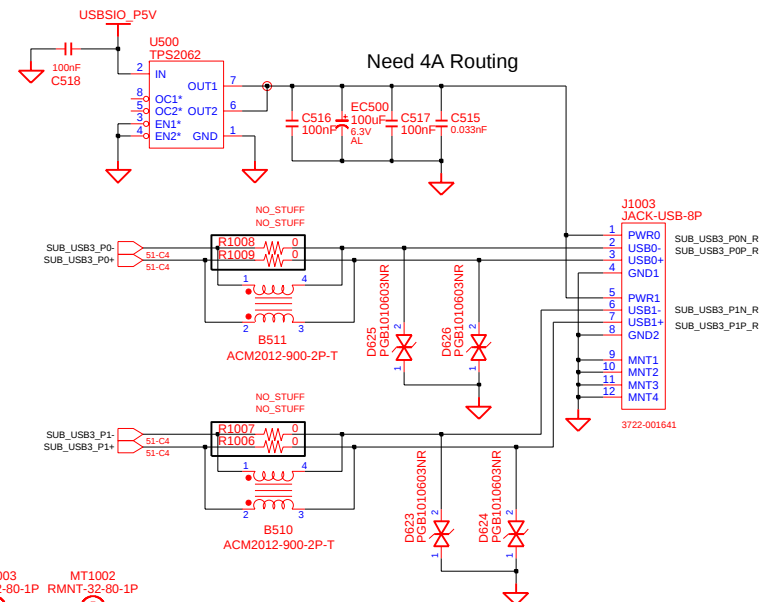
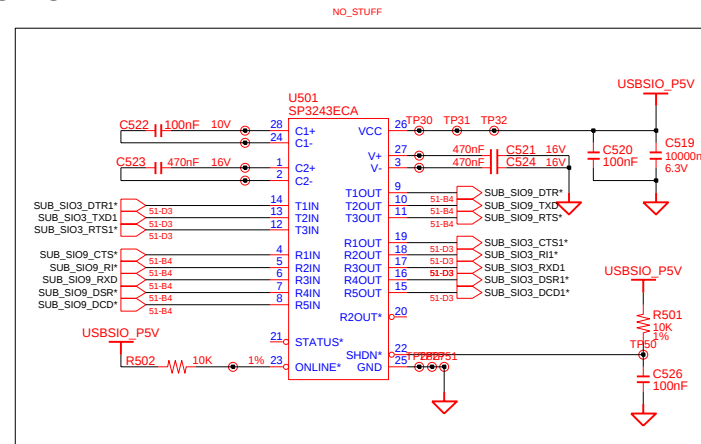
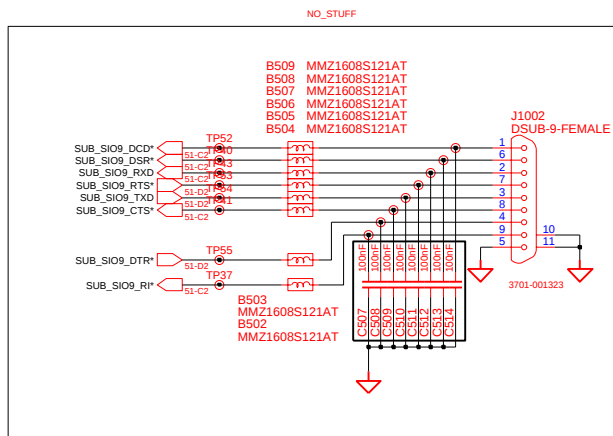
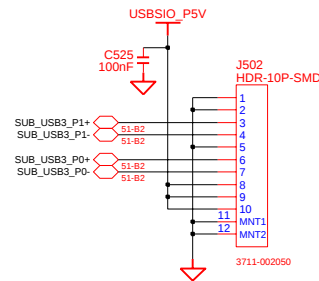
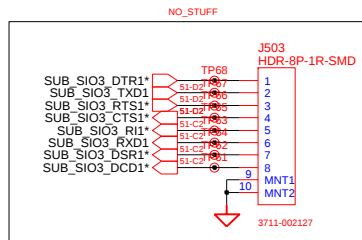
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAINBD POWER ADAPT	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	49 OF 55	

1394 IR BOARD



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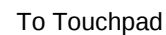
USB_SIO BOARD



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER USB BOARD	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	51	OF 55

A

NO_STUFF



f:/users/ecad02/mentor/habana-c/Dothan/PRR

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TP8690 ILIM3
TP8700 ILIM5
TP8710 OPRSLP
TP8720 IDE5_A0
TP8730 IDE5_A1
TP8740 IDE5_A2
TP8750 INT_MIC
TP8760 ODD5_A0
TP8770 ODD5_A1
TP8780 ODD5_A2
TP8790 RTC_CLK
TP8800 AC_SDOOUT
TP8810 AUTO_ON*
TP8820 CPU1_NMI
TP8830 CPU1_TCK
TP8840 CPU1_TDI
TP8850 CPU1_TDO
TP8860 CPU1_TMS
TP8870 JCK_SENS

TP856 ○ ODD5_IRQ
TP857 ○ PCI3_PAR
TP858 ○ SATA1_X1
TP859 ○ SMB3_CLK

TP831 CBS3_CCLK
TP832 CBS3_CPAR
TP833 CBS3_CVS1
TP834 CBS3_CVS2
TP835 CBS3_SPKR
TP836 CHP3_SPKR

TP841 CPU1_INTR

TP845 CPU1_SLP.
TP846 CPU1_SMI.
TP847 HDD3_LED.

TP849 ○ IDE5_CS1*
TP850 ○ IDE5_CS3*
TP851 ○ IDE5_D(0)
TP852 ○ IDE5_D(1)
TP853 ○ IDE5_D(2)
TP854 ○ IDE5_D(3)
TP855 ○ IDE5_D(4)

TP815 ☐ IDE5-D(5)
TP816 ☐ IDE5-D(6)
TP817 ☐ IDE5-D(7)
TP818 ☐ IDE5-D(8)
TP819 ☐ IDE5-D(9)
TP820 ☐ IDE5-DREQ
TP821 ☐ IDE5-IOR*
TP822 ☐ IDE5-IOW*
TP823 ☐ KBC3-A20G
TP824 ☐ KBC5-TCLK
TP825 ☐ LAN3-ACT*

TP827O LCD3_BRIT

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TP828 00DD5 C51.*
TP829 00DD5 C53.*
TP830 00DD5 D(0)
TP785 00DD5 D(1)
TP786 00DD5 D(2)
TP787 00DD5 D(3)
TP788 00DD5 D(4)
TP789 00DD5 D(5)
TP790 00DD5 D(6)
TP791 00DD5 D(7)
TP792 00DD5 D(8)
TP793 00DD5 D(9)
TP794 00DD5 DREQ
TP795 00DD5 IOR.*
TP796 00DD5 IOW.*
TP797 00DD5 RST.*
TP798 PC13 CLK8
TP799 00D13 IRRX
TP800 00D13 IRTX
TP801 00D13 R11.*
TP802 00D13 RxD1
TP803 00D13 IxD1
TP804 CMBL3 LED
TP805 CMBL3 LED
TP806 CAUD3 EAPD
TP807 CAUD3 EAPD
TP808 CAUD3 A.D1
TP809 CBPS3 CCD1
TP810 CBPS3 CCD2
TP811 CBPS3 CNT1
TP812 CBPS3 CNT2
TP813 CBPS3 CREQ
TP814 CBPS3 CRST.*
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TP776○CLK3_ICH14
TP777○CLK3_NB14M
TP778○CLK3_SIO14

TP780 CPU1_A20M*

TP783 CPU1_BSEL1
TP784 CPU1_BSEL2

TP755 CPU1_FERR.
TP757 CPU1_INIT.

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TP760 CPU1_TRST#
TP761 CRT3_HSYNC
TP762 CRT3_VSYNC
TP763 EXP3_SPPE#
TP764 FWH1_INIT#
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TP768 IDE5_D(13)
TP769 IDE5_D(14)
TP770 IDE5_D(15)
TP771 IDE5_DACK#
TP772 IDE5_DASP#
TP773 IDE5_IORDY
TP774 KBC3_CHGEN
TP775 KBC5_TDATA

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TP513 LCD3_VDDEN

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TP523C ODD5.LORDY
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TP746C PC13.CBE2
TP747C PC13.CBE3
TP748C PC13.GNT0
TP749C PC13.GNT1
TP750C PC13.GNT2
TP751C PC13.INTB

TP492○PCI3_INTC•
TP493○PCI3_INTD•
TP494○PCI3_INTE•
TP495○PCI3_INTF•
TP496○PCI3_INTG•
TP497○PCI3_INTH•
TP498○PCI3_IRDY•
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TP500○PCI3_REQ0•
TP501○PCI3_REQ1•
TP502○PCI3_REQ2•
TP503○PCI3_REQ3•
TP504○PCI3_RSTF•
TP505○PCI3_SERR•
TP506○PCI3_STOP•
TP507○PCI3_TRDY•

TP508 OPLT3_RSTF•

TP509 ○ SI03_CTS1
TP510 ○ SI03_DCD1
TP511 ○ SI03_DSR1
TP464 ○ SI03_DTR1
TP465 ○ SI03_RTS1

TP467 ○ VGA3_HSYNC
TP468 ○ VGA3_VSYNC
TP469 ○ AUD3_EAPD_A
TP470 ○ AUD3_PCBEFP

TP4710BAT3_SMCLK•

TP473 CBRS3_A_A_18
TP474 CBRS3_A_A_19
TP475 CBRS3_A_D_14
TP476 CBRS3_CAD(0)
TP477 CBRS3_CAD(1)
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TP487 CBRS3_CBE09
TP488 CBRS3_CBE1
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TP462CLK3_DBG_LPC

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CHECK	XU, DJ	DEV. STEP	PRR			
APPROVAL	LEE, KEVIN	REV	1.0			
				PART NO.	BA41-00615A	
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3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

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CHECK	XU, DJ	DEV. STEP	PRR				
APPROVAL	LEE, KEVIN	REV	1.0				
				TP		PART NO.	BA41-00615A
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