

FIRENZE-R

CPU : Yonah 667
Chip Set : CALISTOGA & ICH7-M
Remarks : Mobility Platform

Model Name : FIRENZE-R
PBA Name : MAIN
PCB Code : BA41-00655A/B
Dev. Step : SR
Revision : 1.0
T.R. Date : 2006.03.09

DRAW	CHECK	APPROVAL
SON,C.W	YUN,C.Y	LIM,J.G

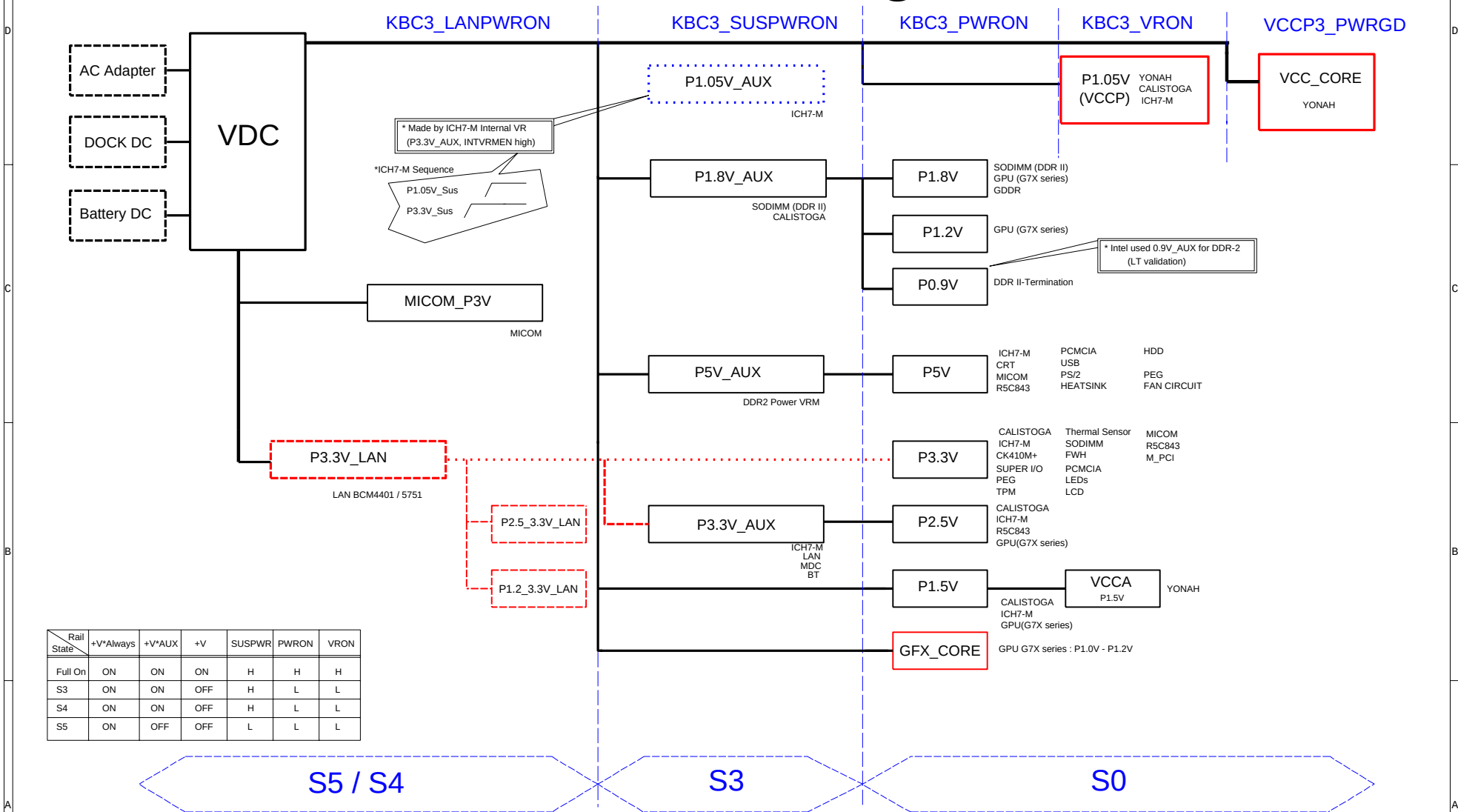
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-00655A
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	1 OF 55	

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Power Diagram



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	x	-
Internal MAC	AD24(internal)	-	B
AC Link	-	-	E

VDC	Primary DC system power supply (7 to 21V)
CORE	Core voltage for DOTHAN (1.306-1.068V)
VCCP	YONAH/CALISTOGA Processor System Bus(PSB) Termination (1.05V)
	MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
MEM1_VREF	0.9V power rail (off in S4-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P5V_ALWS	5V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001x	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

System Power States

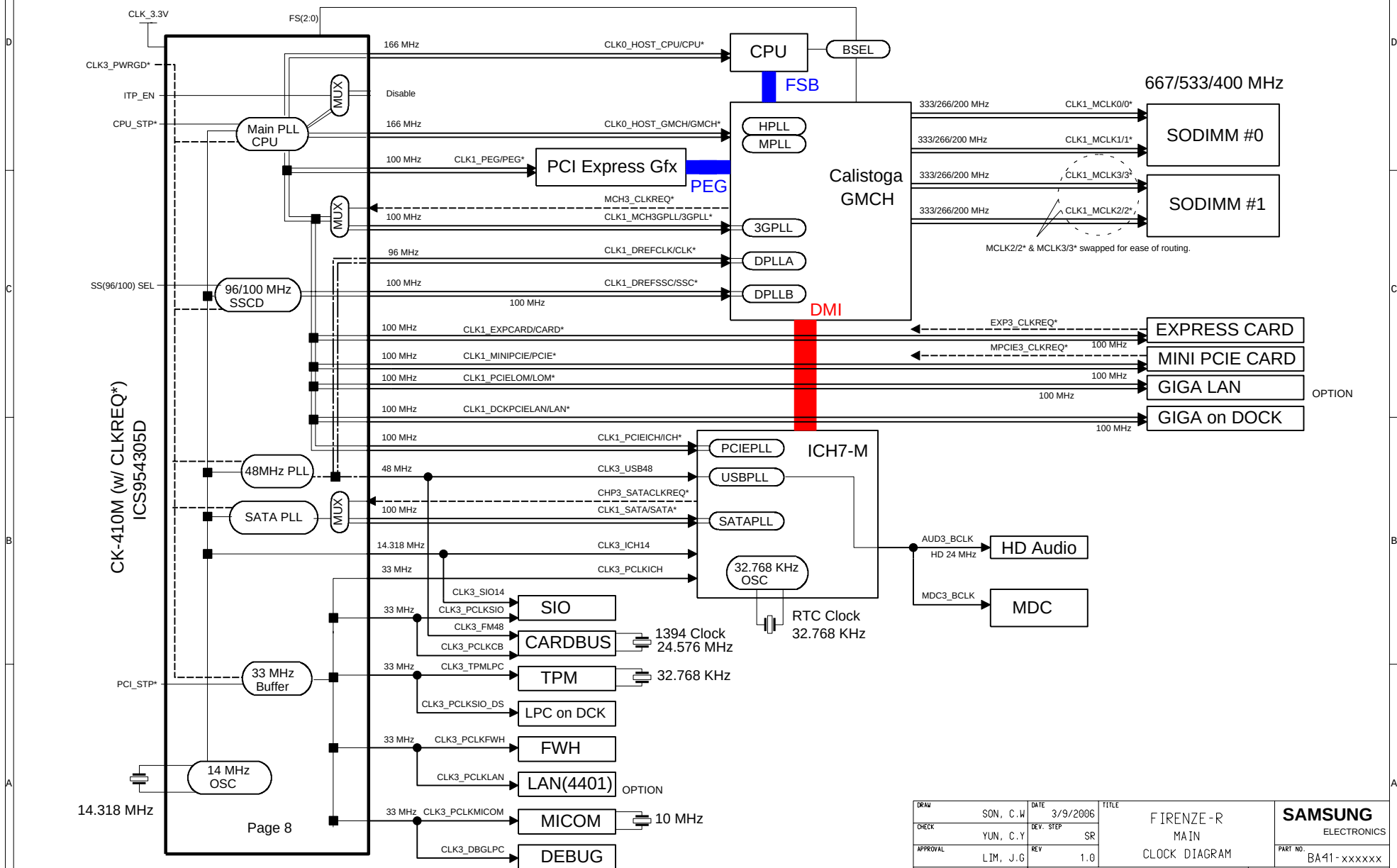
CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	H8S/2111B
Crystal	14.318MHz	CLOCK-Generator	CK-410M+
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	BROADCOM LAN
Crystal	24MHz	Finger Printer	AES2501A

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	1.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 0 1	0.7750 V	1 1 0 0 1 0 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 1 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 1 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 1	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 1	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.

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CHECK	YUN, C.Y	DEV. STEP	SR		
APPROVAL	LIM, J.G	REV	1.0		
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM		

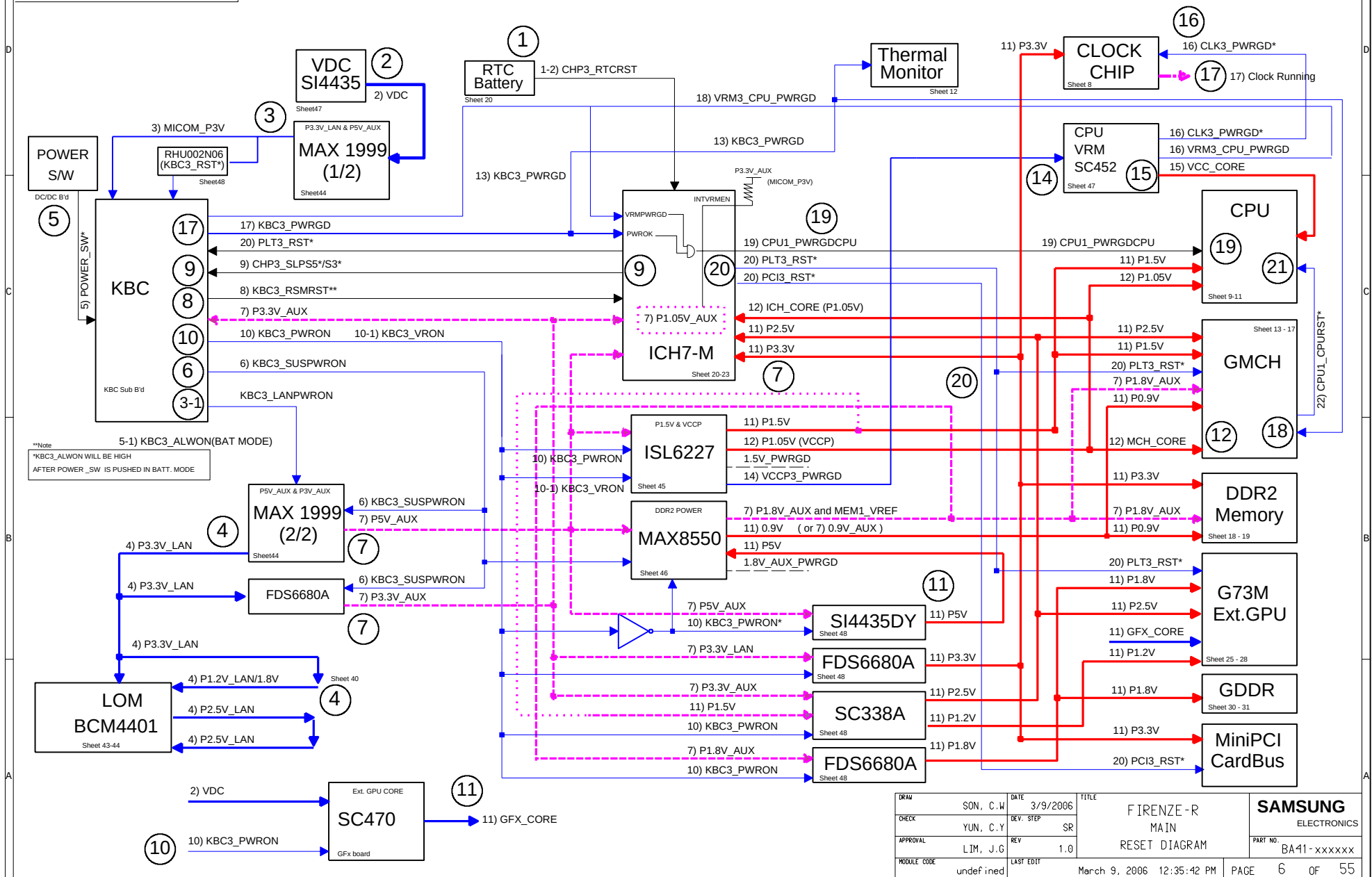
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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	5	OF 55

RESET DIAGRAM

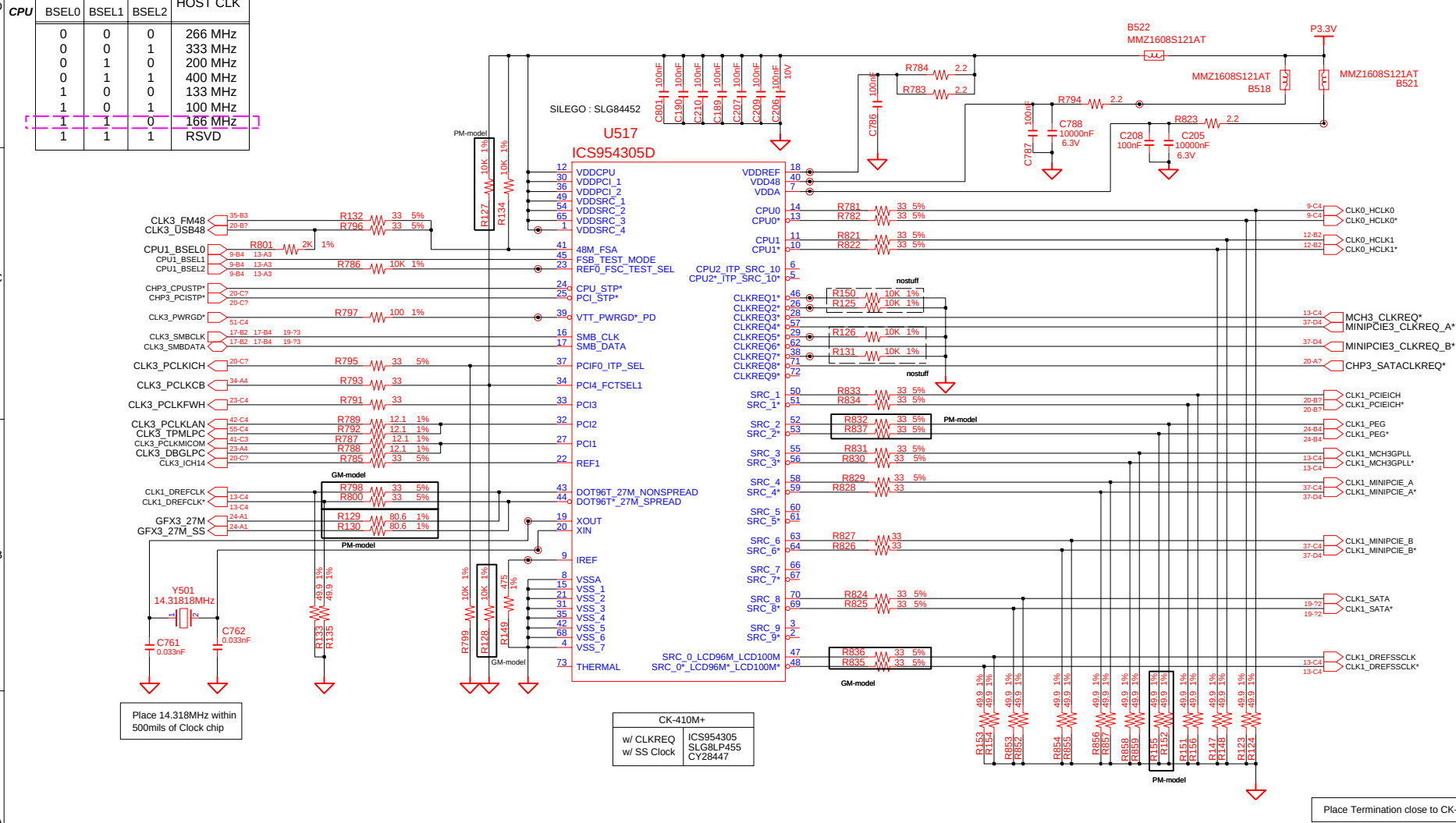


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APPROVAL	LIM, J.G	REV	1.0			
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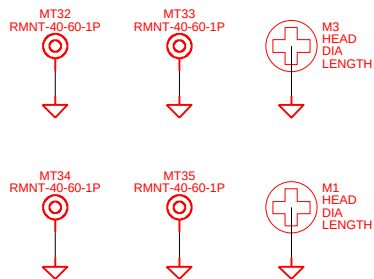
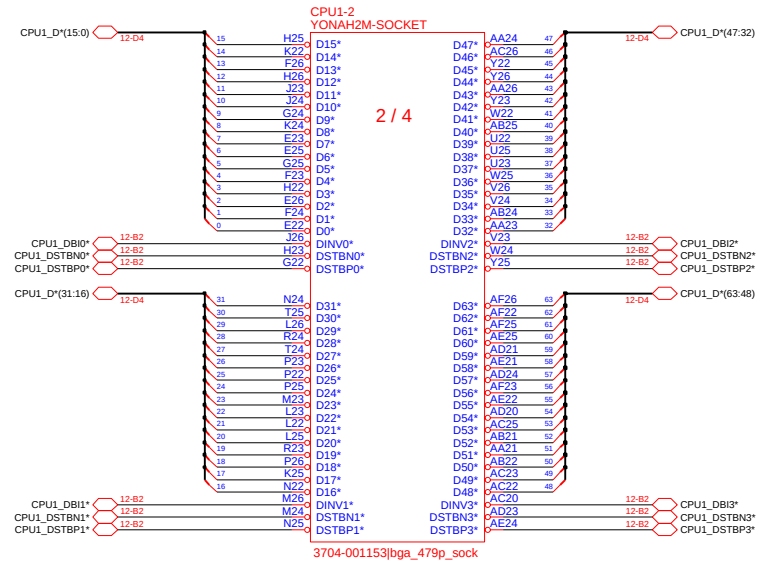
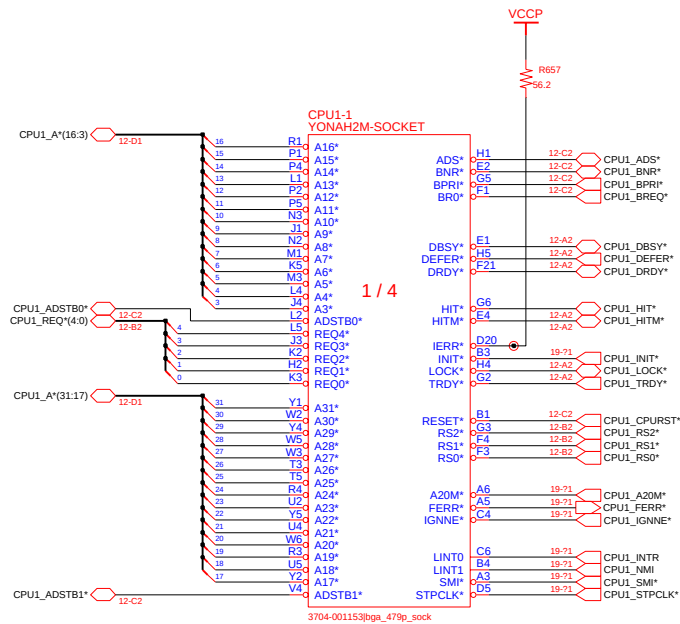
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FCTSEL1(43,44,47,48)	1: 27M & SRC0	0: DOT96 & LCD100
ITP_EN (5,6)	1: CPU_ITP pair	0: SRC pair

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



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APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	8	OF 55

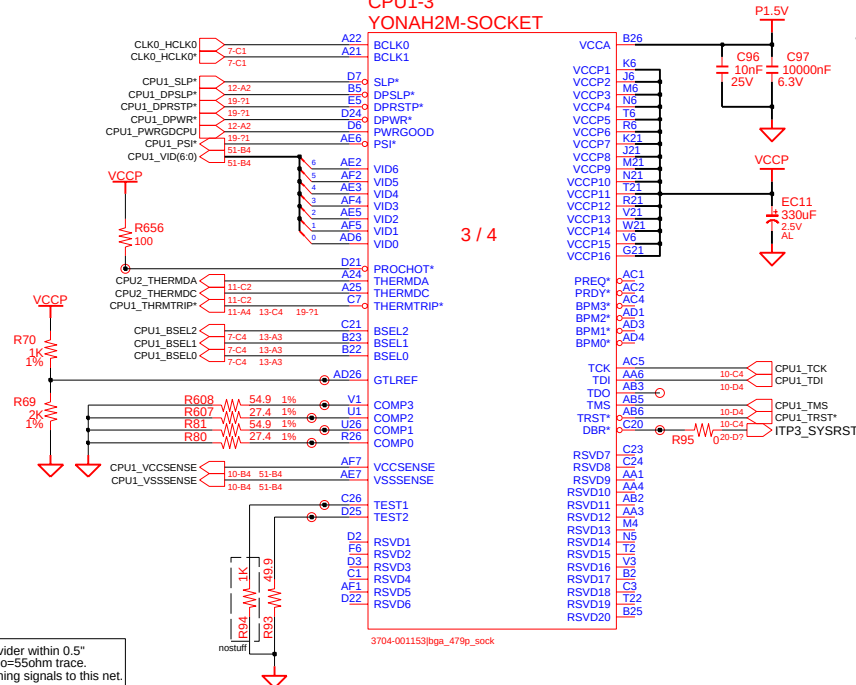
4

3

2

1

CPU1-3
YONAH2M-SOCKET



GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.

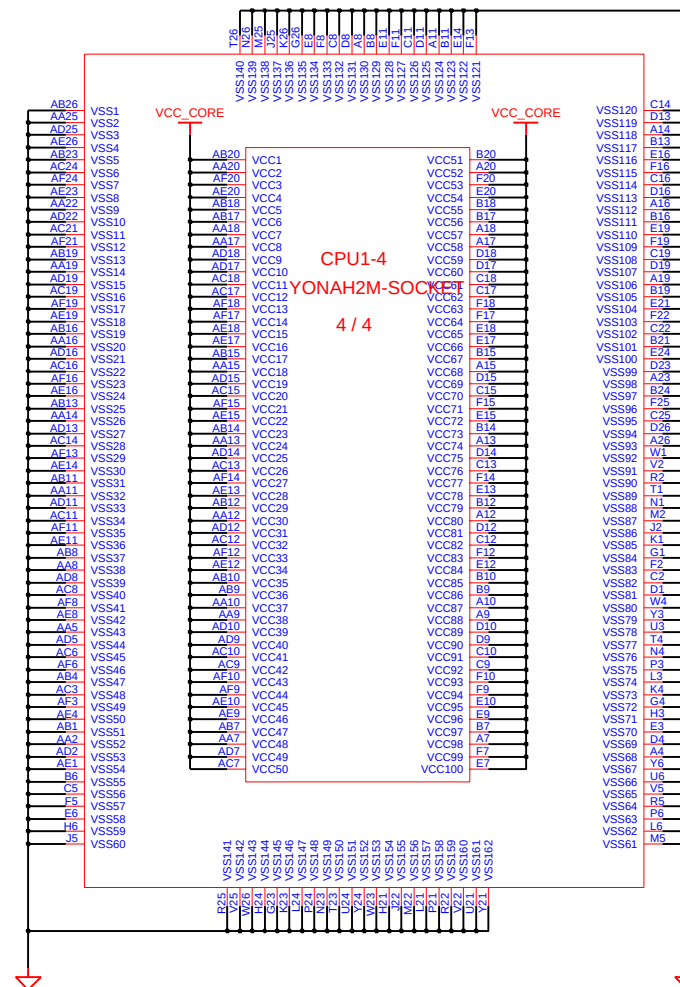
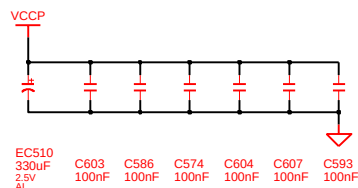
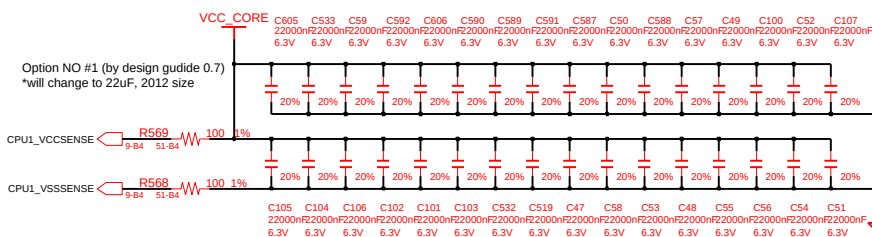
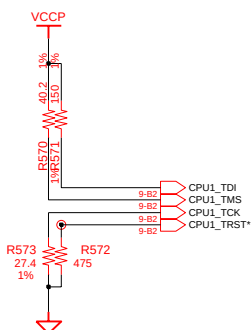
COMP0,2(3) should be connected with Zo=27.4ohm(55ohm)
trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 0 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				***11111111**: 0V power good asserted.	
Active		Deeper Sip			
DPRSLPVR 0		DPRSLPVR 1			
DPRSTP* 1		DPRSTP* 0			
PSI2* 0 or 1		PSI2* 0 or 1			

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

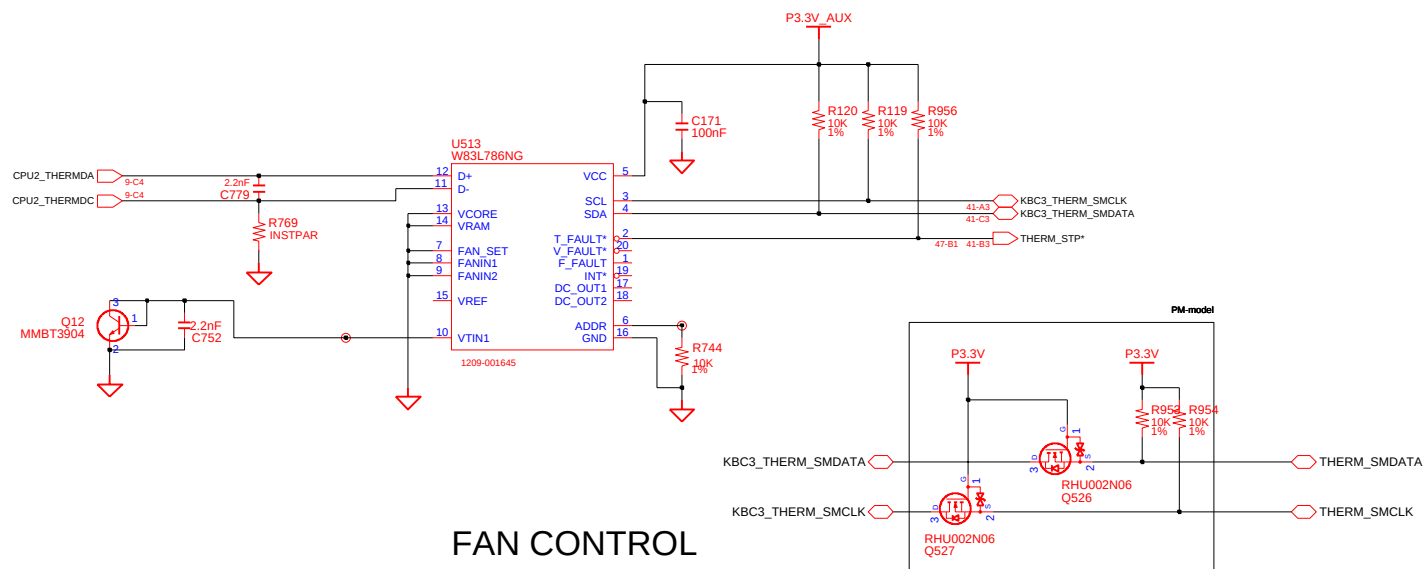
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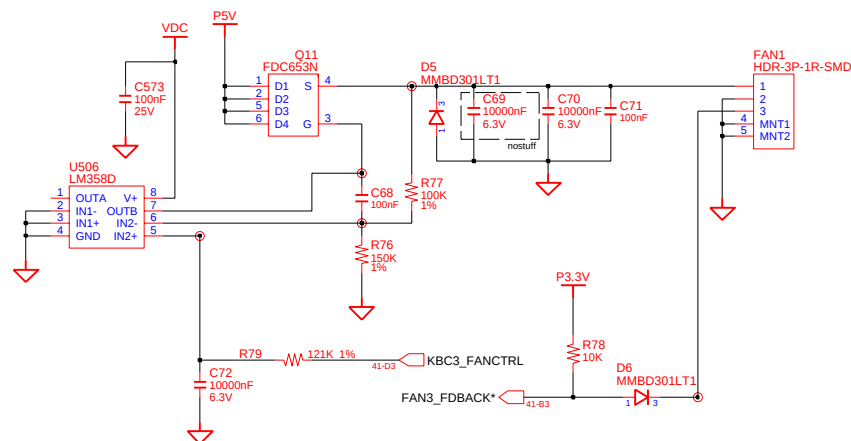
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CPU/GFX Thermal Sensor



FAN CONTROL



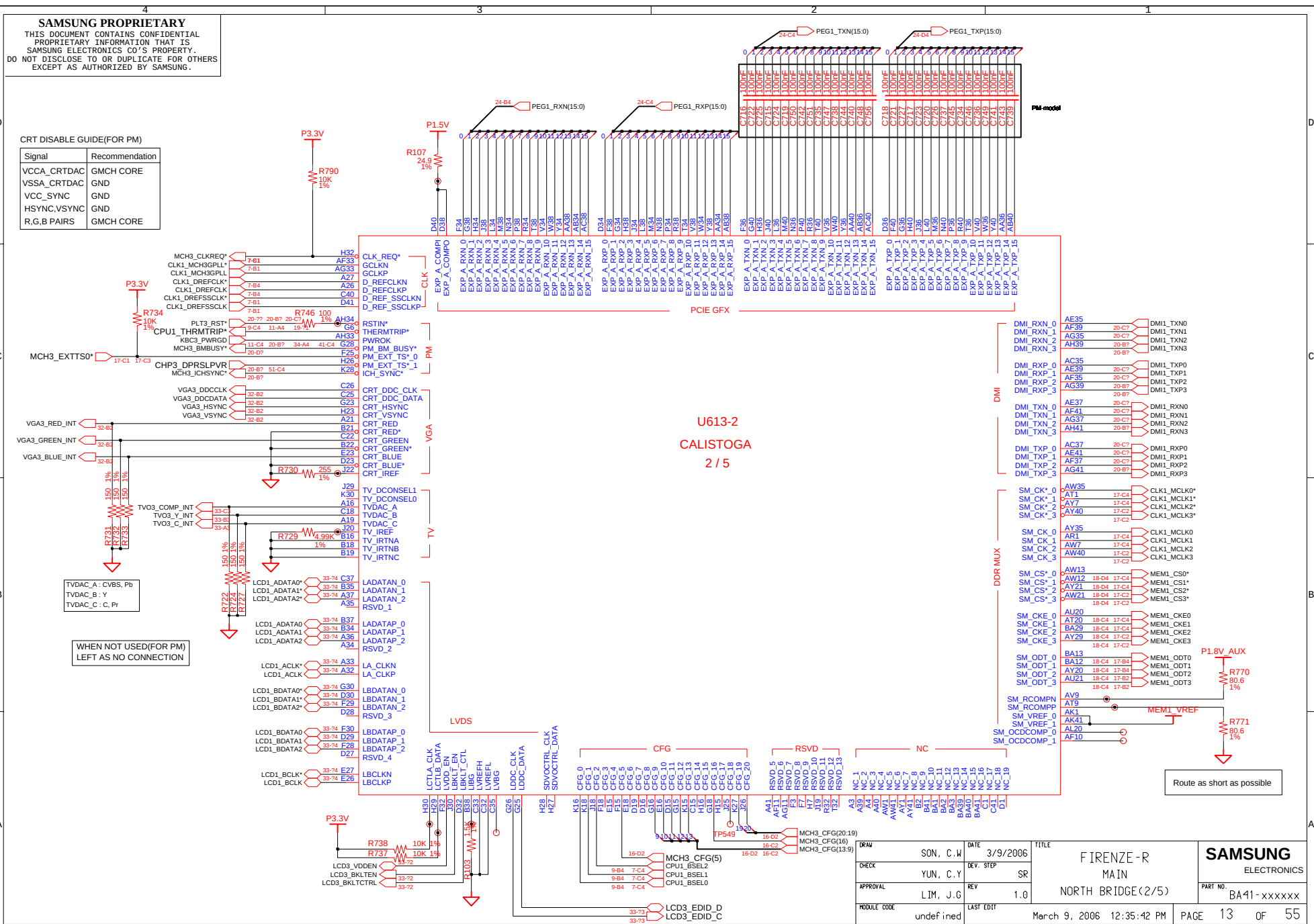
DRW	SON, C.W	DATE	3/9/2006	TITLE			FIRENZE-R MAIN			SAMSUNG ELECTRONICS		
CHECK	YUN, C.Y	DEV. STEP	SR									
APPROVAL	LIM, J.G	REV	1.0	THERMAL SENSOR/FAN CTRL			PART NO.			BA41-xxxxxx		
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM									

[illegible]

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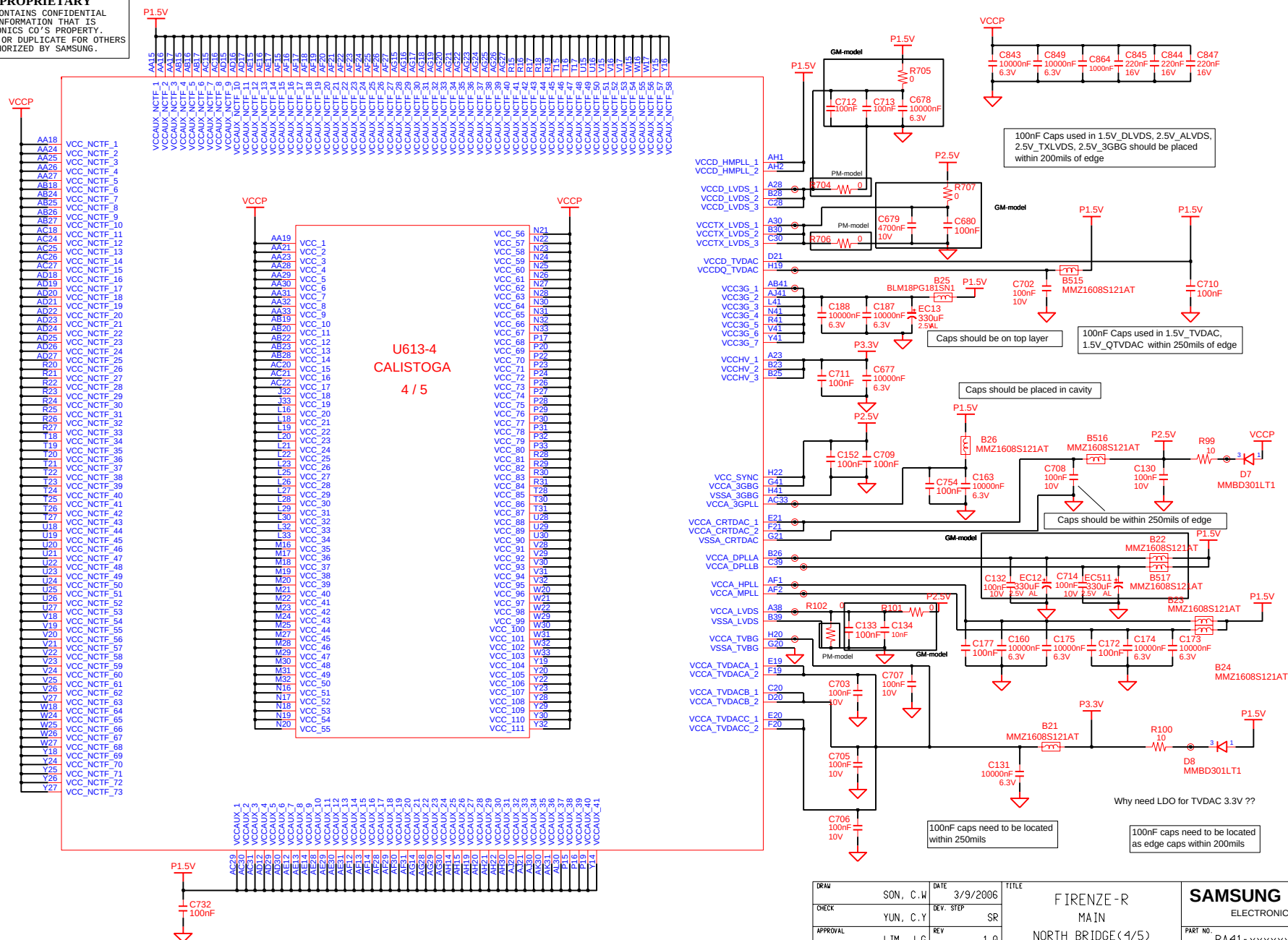
CRT DISABLE GUIDE(FOR PM)

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC_VSYNC	GND
R,G,B PAIRS	GMCH CORE



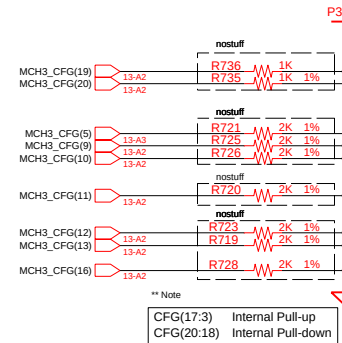
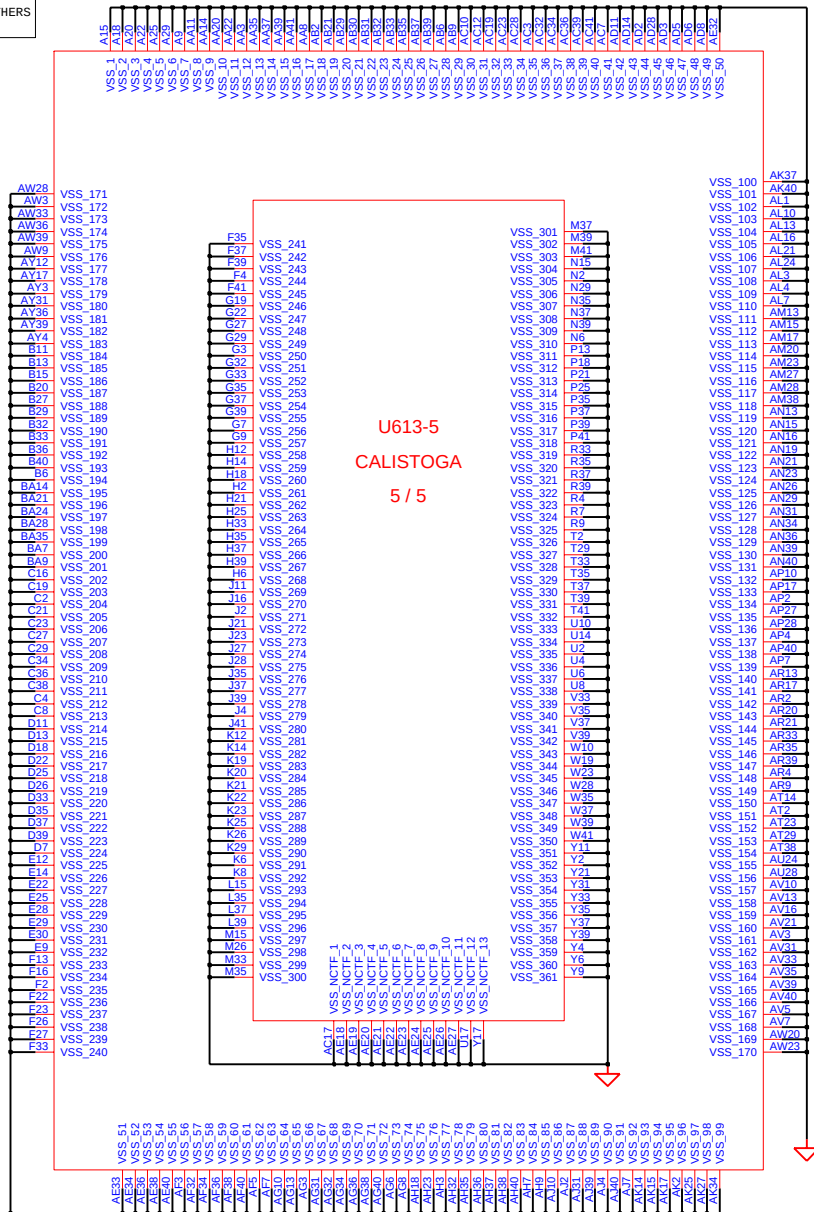
SDVO Mode	PEG (SAGP) Mode
SDVOSB_RED*	EXP_TXN_0
SDVOSB_RED	EXP_TXP_0
SDVOSB_GREEN*	EXP_TXN_1
SDVOSB_GREEN	EXP_TXP_1
SDVOSB_BLUE*	EXP_TXN_2
SDVOSB_BLUE	EXP_TXP_2
SDVOSB_CLK*	EXP_TXN_3
SDVOSB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOSB_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOSB_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOSB_INT*	EXP_RXN_1
SDVOSB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

COM-22C-015(1996.6.5) REV. 3



DATE	SON, C.W.	3/9/2006	TITLE FIRENZE-R MAIN NORTH BRIDGE(4/5)		SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y.	DEV. STEP SR				
APPROVAL	LIM, J.G.	REV 1.0				
MODULE CODE		LAST EDIT		PART NO.		
undefined		March 9, 2006 12:35:42 PM		BA41-xxxxxx		
				PAGE	15 OF 55	

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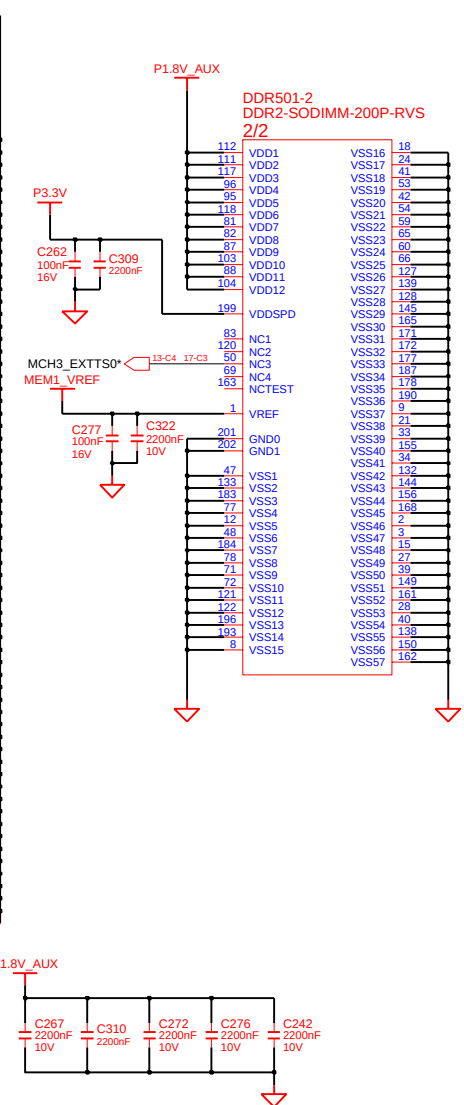
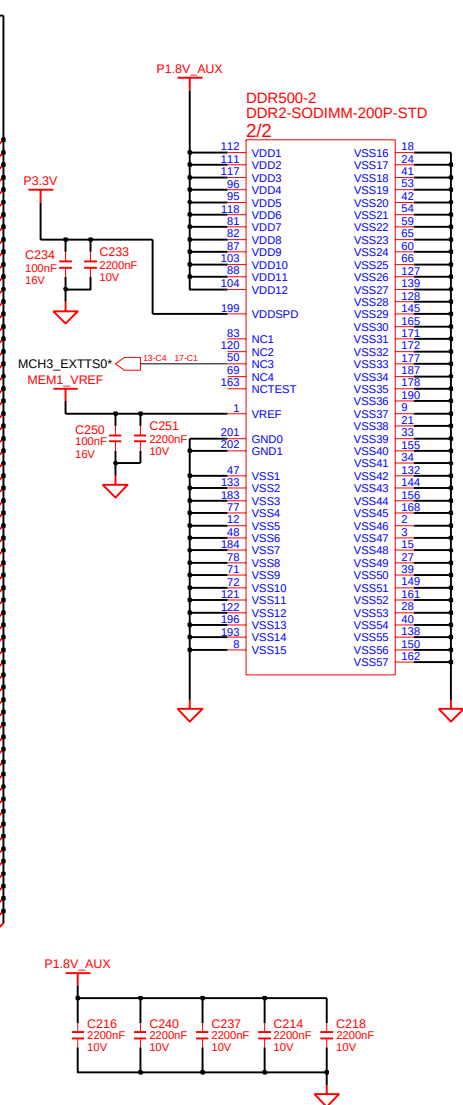
** Note *POCAFE10 Only (Remove in MP Model)

Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

When CFG 13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clock power-up/power-down. Intel strongly recommends leaving CFG 13:12 = NC (Internal PU to '11') to ensure low avg.power.

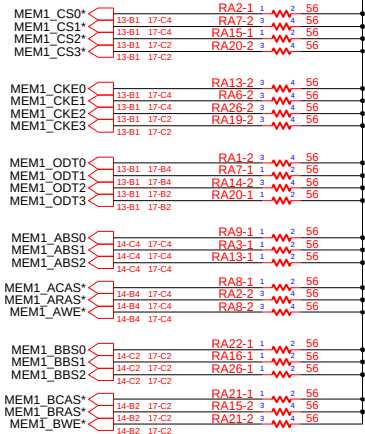
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CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	16	OF 55

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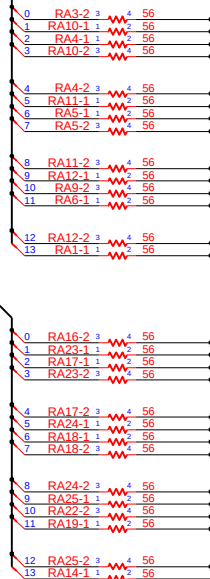
DATE	SON, C.W.	3/9/2006	TITLE FIRENZE-R MAIN DDR2-SODIMM			SAMSUNG ELECTRONICS			
CHECK	YUN, C.Y.	DEV. STEP							SR
APPROVAL	LIM, J.G.	REV							1.0
MODULE CODE	undefined		LAST EDIT	March 9, 2006	12:35:42 PM	PAGE	17	OF	55

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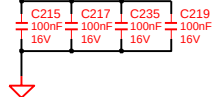


MEM1_AMA(13:0) 14-B4 17-D4

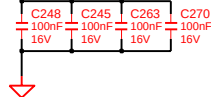
MEM1_BMA(13:0) 14-B2 17-D2



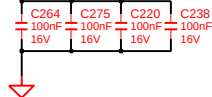
P1.8V_AUX



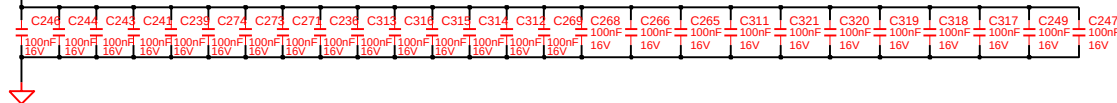
P1.8V_AUX



P1.8V_AUX

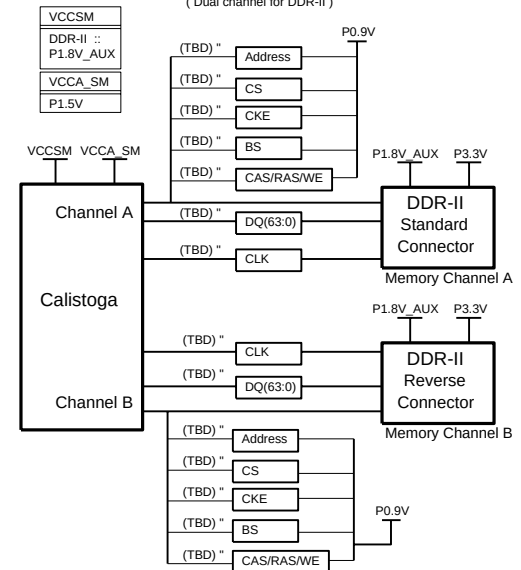


P0.9V



Memory Topology

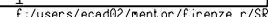
(Dual channel for DDR-II)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN DDR2 - TERMINATION	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	18	OF 55

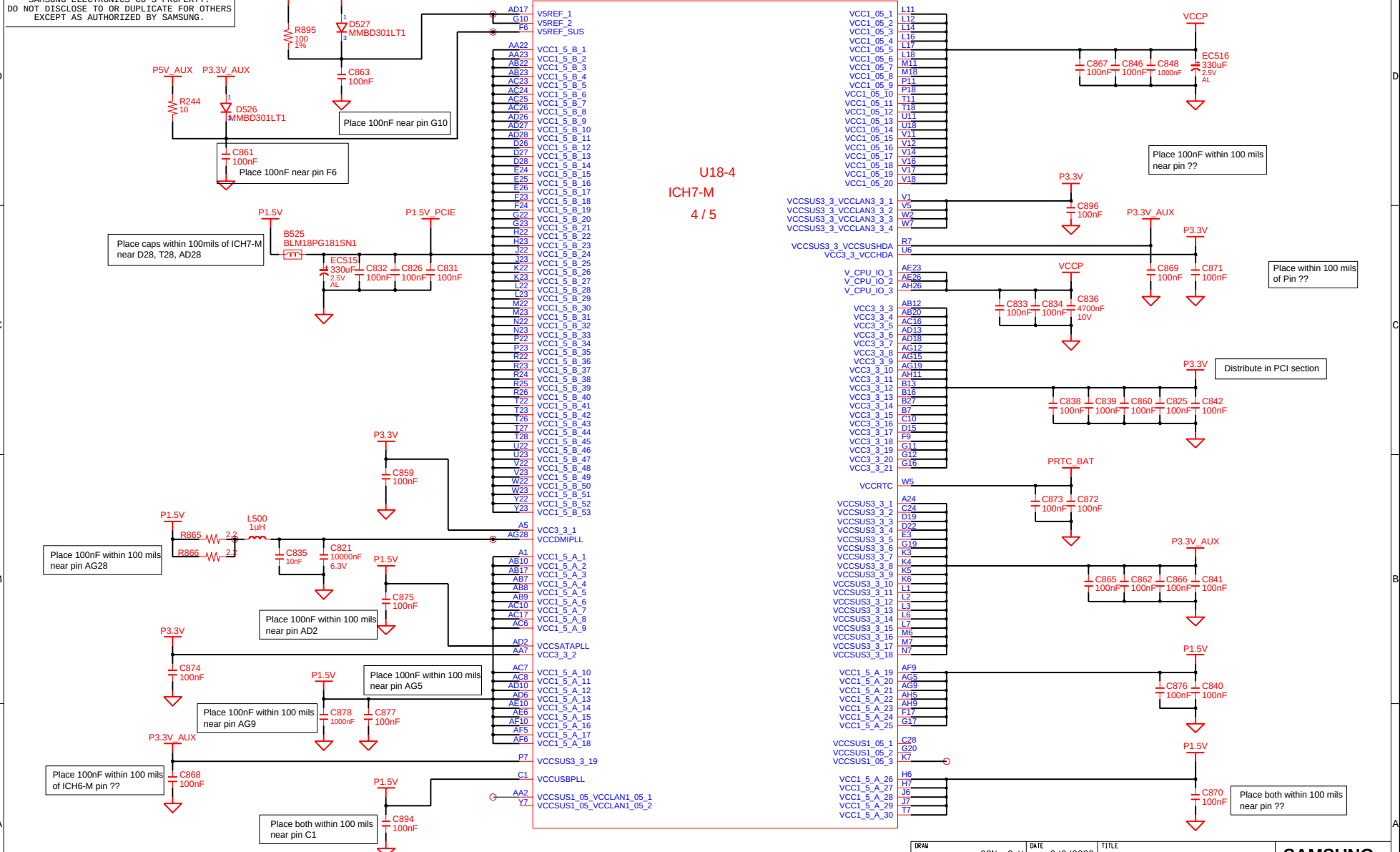
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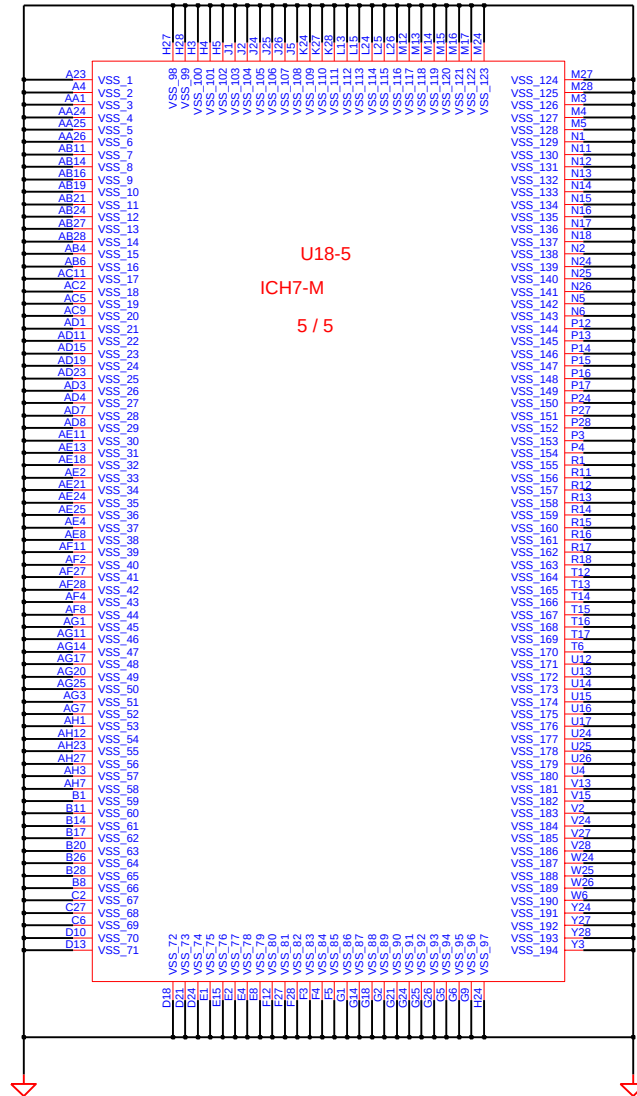
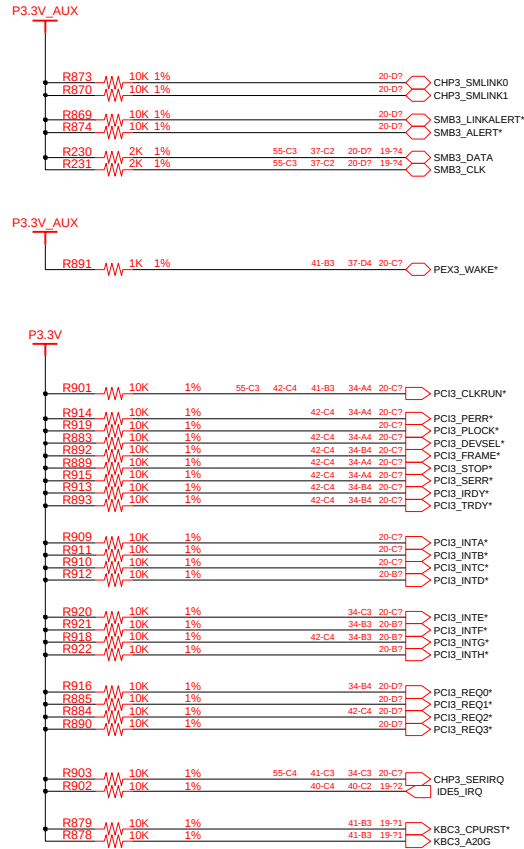
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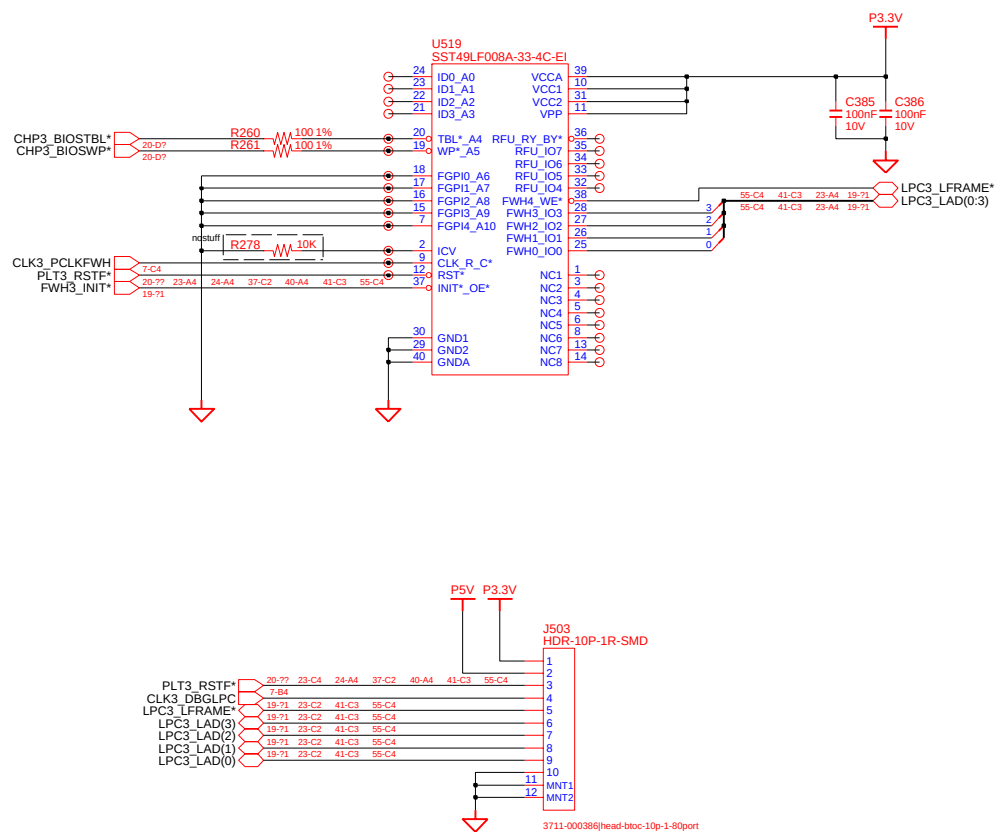


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(3/4)		
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	21 OF 55	

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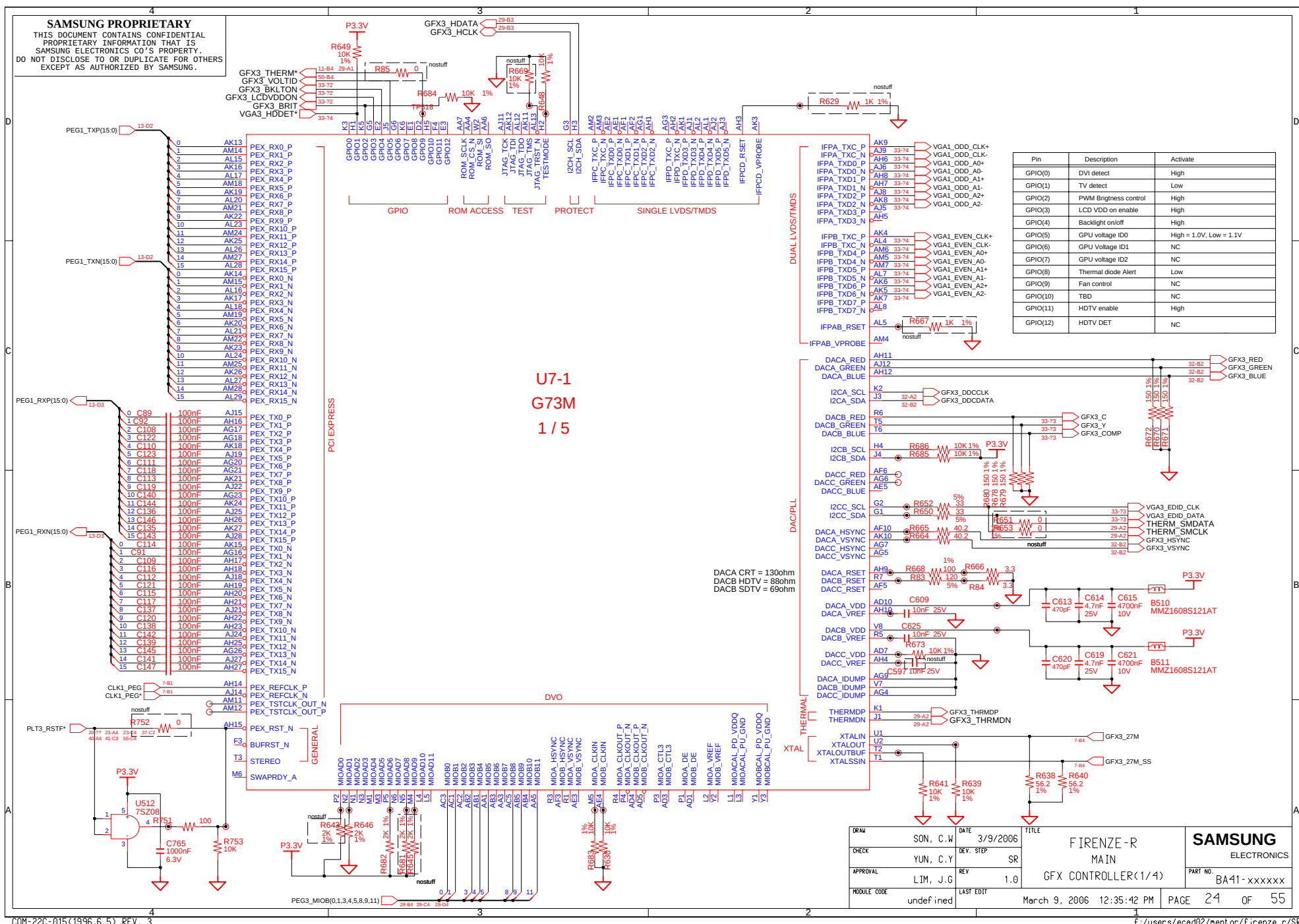
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- | | | | |
|----|------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| 0E | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET | 86 | RE-INIT. ON-BOARD I/O PORT |
| | WITH INITIAL POST VALUE | 88 | INIT. BIOS DATA ROM |
| 14 | INIT. KEYBOARD CONTROLLER | 8A | INIT.EXTENDED BIOS DATA AREA |
| 16 | CHECK CHECKSUM | 8C | INIT. FDD CONTROLLER |
| 18 | 8254 TIMER INIT. | 9A | SHADOW OPTION ROMS |
| 1A | 8237 DMA CONTROLLER INIT. | 9C | SETUP POWER MANAGEMENT |
| 1C | RESET INTERRUPT CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 20 | TEST DRAM REFRESH | A0 | SET TIME OF DAY |
| 22 | TEST 8742 KEYBOARD CONTROLLER | A4 | INIT. TYPEMATIC RATE |
| 24 | SET ES SEGMENT REG. TO 4GB | A8 | ERASE F2 PROMPT |
| 26 | ENABLE A20 | AA | SCAN FOR F2 KEY STROKE |
| 28 | AUTO SIZING DRAM | AC | ENTER SETUP |
| 32 | COMPUTE THE CPU SPEED | AE | CLEAR IN POST FLAG |
| 34 | TESET CMOS RAM | B0 | CHECK FOR ERRORS |
| 38 | SHADOW SYSTEM BIOS ROM | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3A | AUTO SIZING CACHE | B4 | ONE BEEP |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B6 | CHECK PASSWORD (OPTION) |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B7 | ACPI INIT |
| 42 | INIT. INTERRUPT VECTOR | BA | DMI INIT |
| 44 | INIT. BIOS INTERRUPT | BE | CLEAR SCREEN |
| 46 | CHECK ROM COPYRIGHT NOTICE | C0 | TRY BOOT WITH INT19 |
| 47 | INIT. I20 SUPPORT IF INSTALLED | D0 | INTERRUPT HANDLER ERROR |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | D2 | UNKNOWN INTERRUPT ERROR |
| 49 | INIT. PCI BUS AND DEVICE | D4 | PENDING INTERRUPT ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D6 | SHUTDOWN 5 |
| 4C | SHADOW VIDEO BIOS ROM | D8 | SHUTDOWN ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | DA | EXTENDED BLOCK MOVE |
| 52 | TEST KEYBOARD | DC | SHUTDOWN 10 |
| 54 | SET KEYCLICK IF ENABLED | 89 | ENABLE NMI |
| 56 | ENABLE KEYBOARD | 90 | INIT. HDD CONTROLLER |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 5A | DISPLAY "PRESS SETUP" | 92 | JUMP TO USER PATCH 2 |
| 5C | TEST RAM BETWEEN 512K AND 640K | 94 | DISABLE A20 ADDRESS LINE |
| 60 | TEST EXTENDED MEMORY | 96 | CLEAR HUGE ES SEGMENT REG. |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 98 | SEARCH FOR OPTION ROMS |
| 64 | JUMP TO USER PATCH 1 | | |

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	ELECTRONICS
APPROVAL	LIM, J.G	REV	1.0		FWH	PART NO.
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM			BA41-xxxxxx
				PAGE	23	OF 55

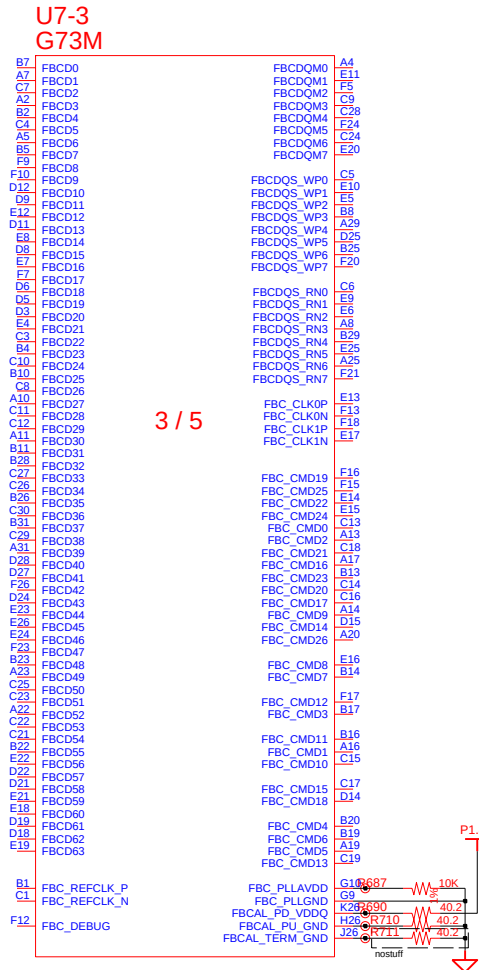
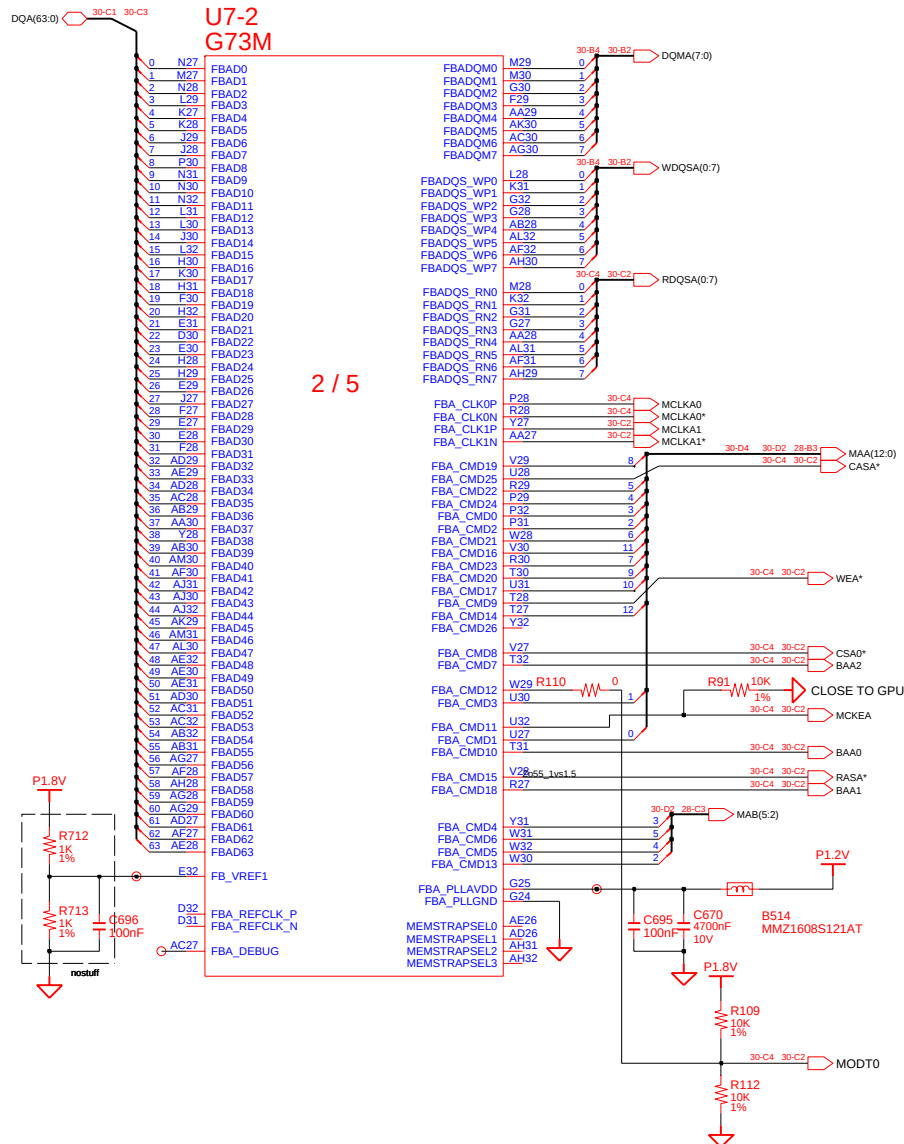
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Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

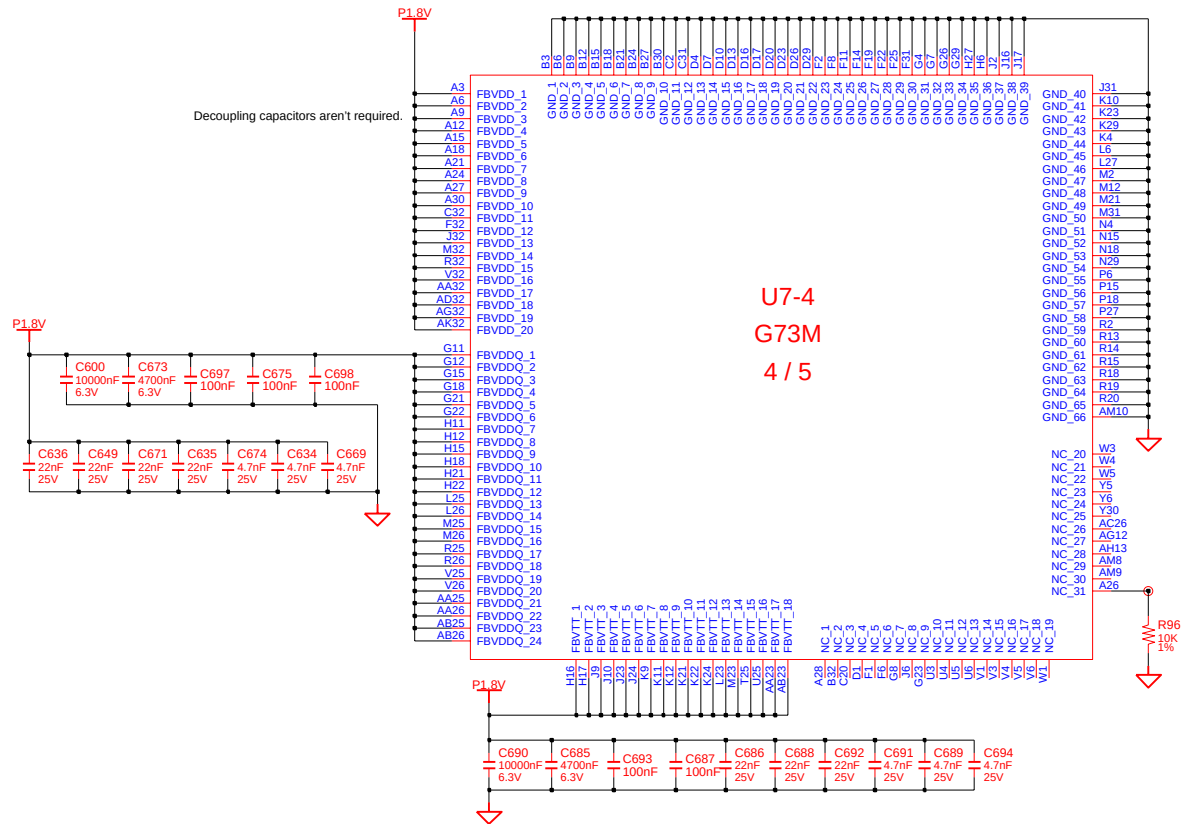
Graphic Memory I/F (Using FBA Channel)

Graphic Memory I/F (Using FBC Channel)



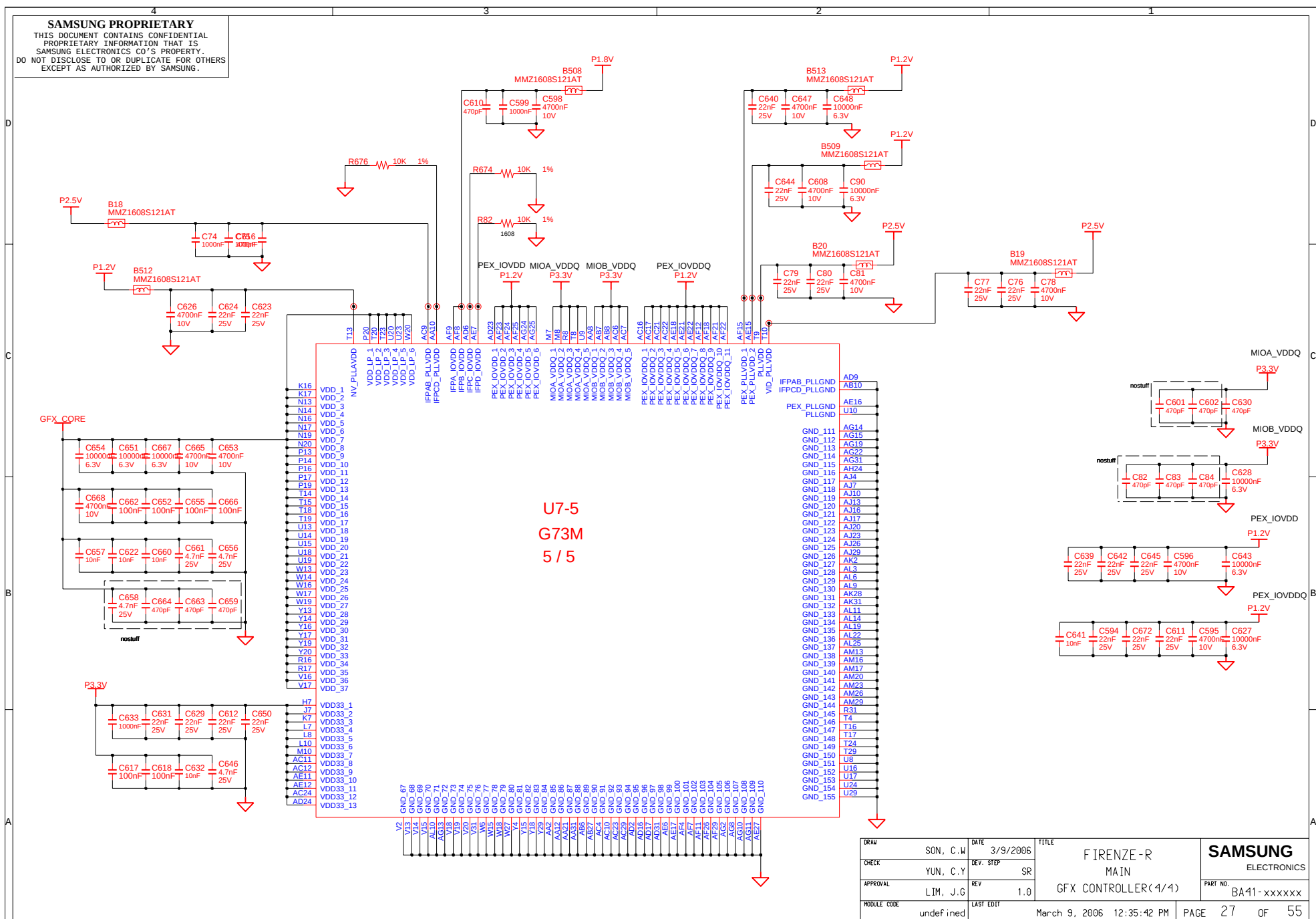
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX CONTROLLER(2/4)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	25 OF 55	

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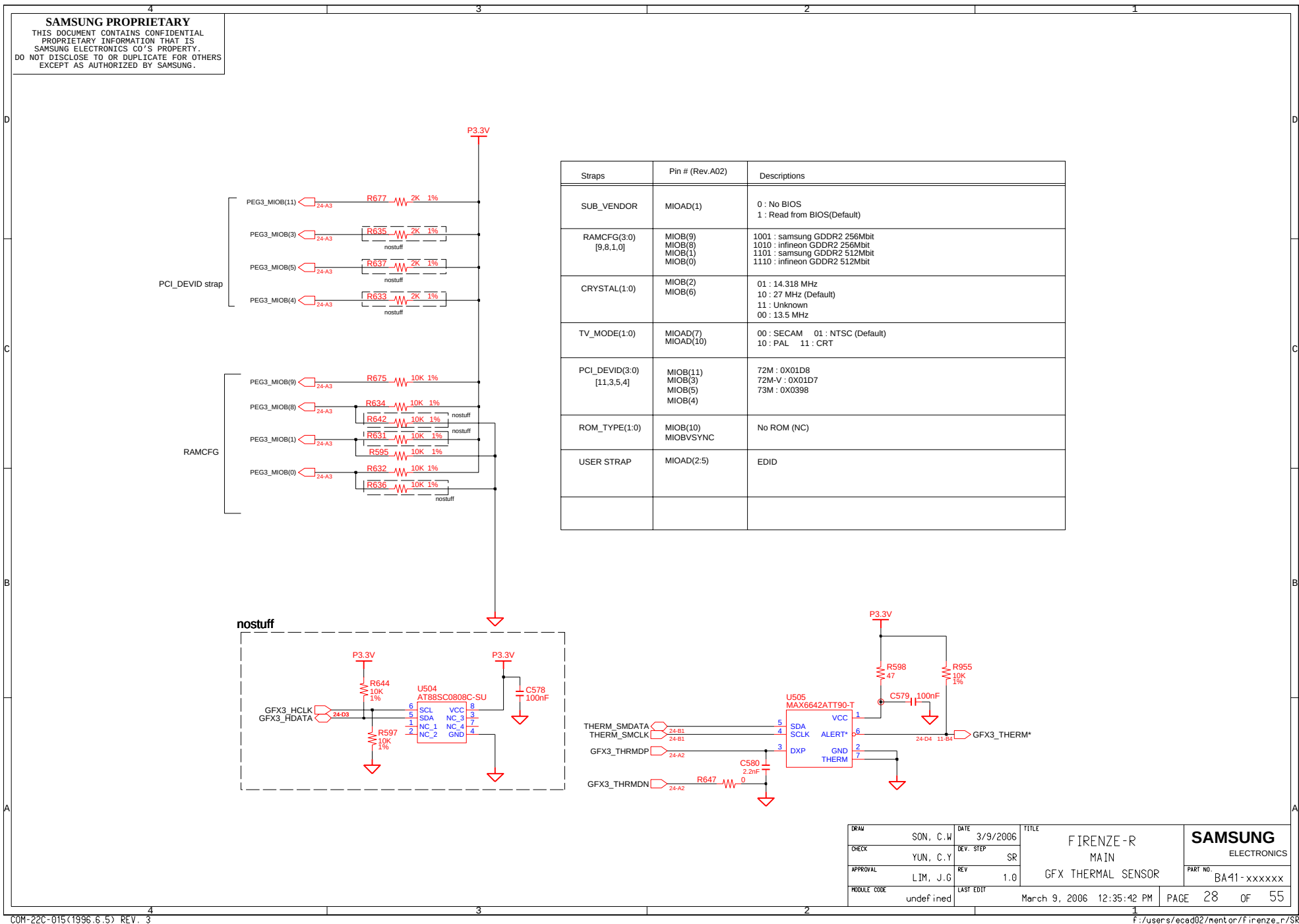


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX CONTROLLER(3/4)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	26	OF 55

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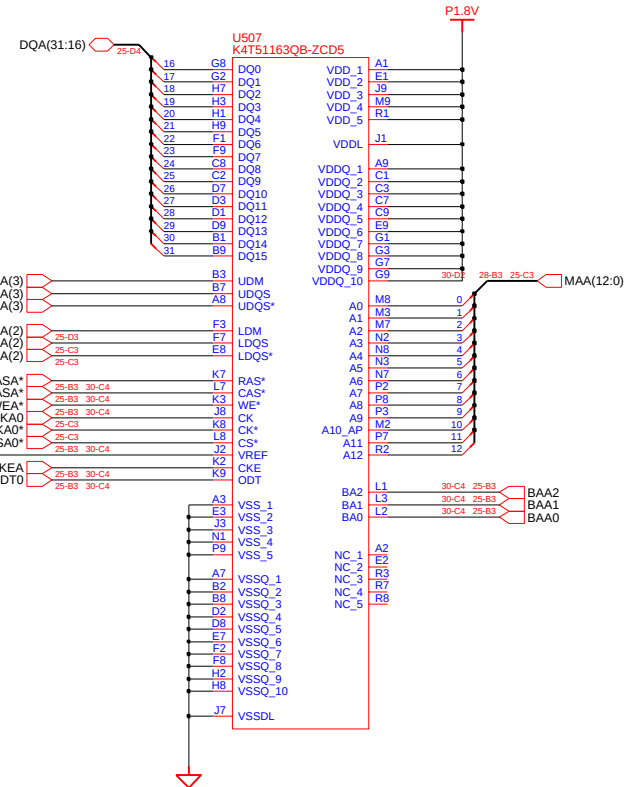
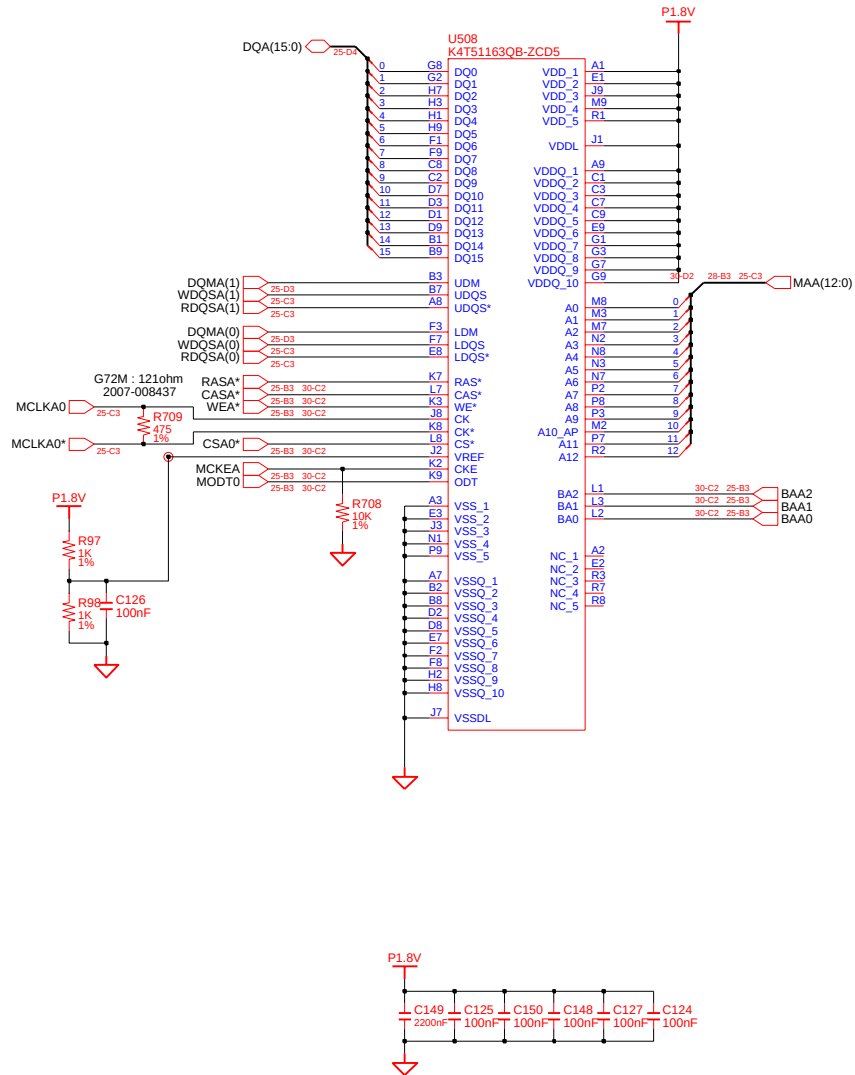


DRAM	SON, C. W.	DATE	3/9/2006		TITLE	FIRENZE-R MAIN GFX CONTROLLER(4/4)	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y.	DEV. STEP	SR				
APPROVAL	LIM, J. G.	REV	1.0				
MODULE CODE		LAST EDIT		March 9, 2006 12:35:42 PM		PAGE	27 OF 55



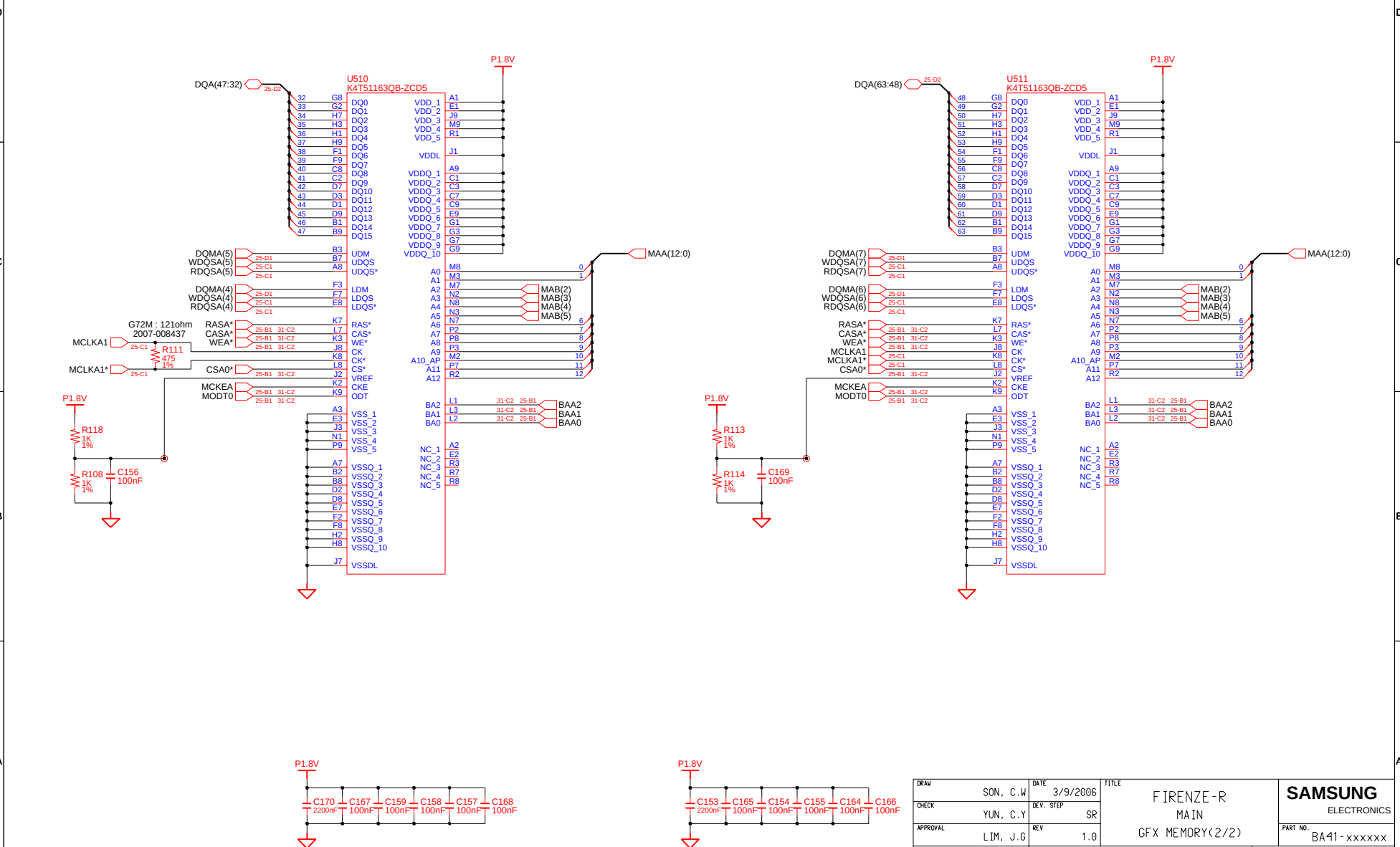
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A-channel

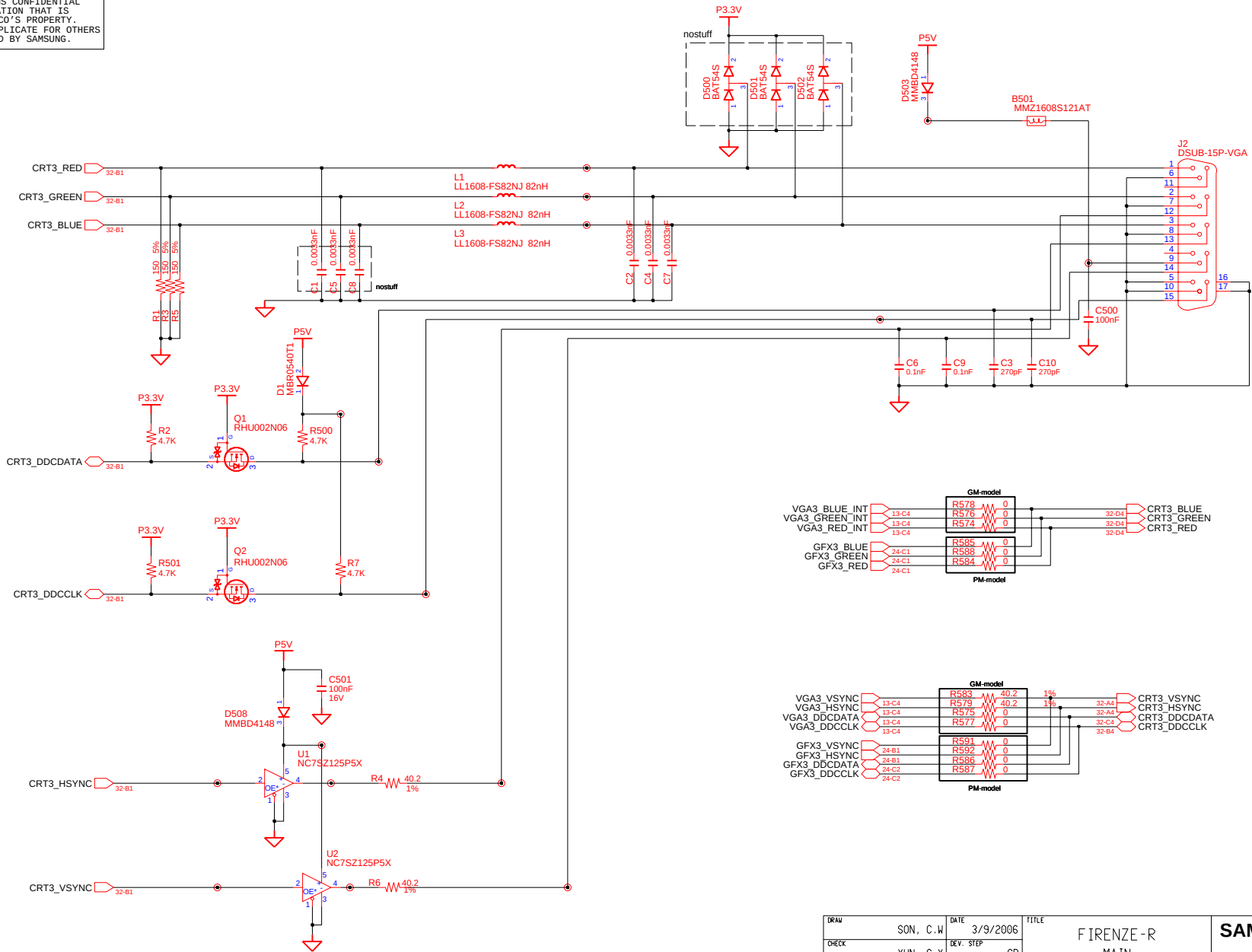


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CHECK	YUN, C.Y	DEV. STEP	SR	MAIN	BA41-xxxxxx	
APPROVAL	LIM, J.G	REV	1.0	GFX MEMORY<1/2>		
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	29	OF 55

A-channel



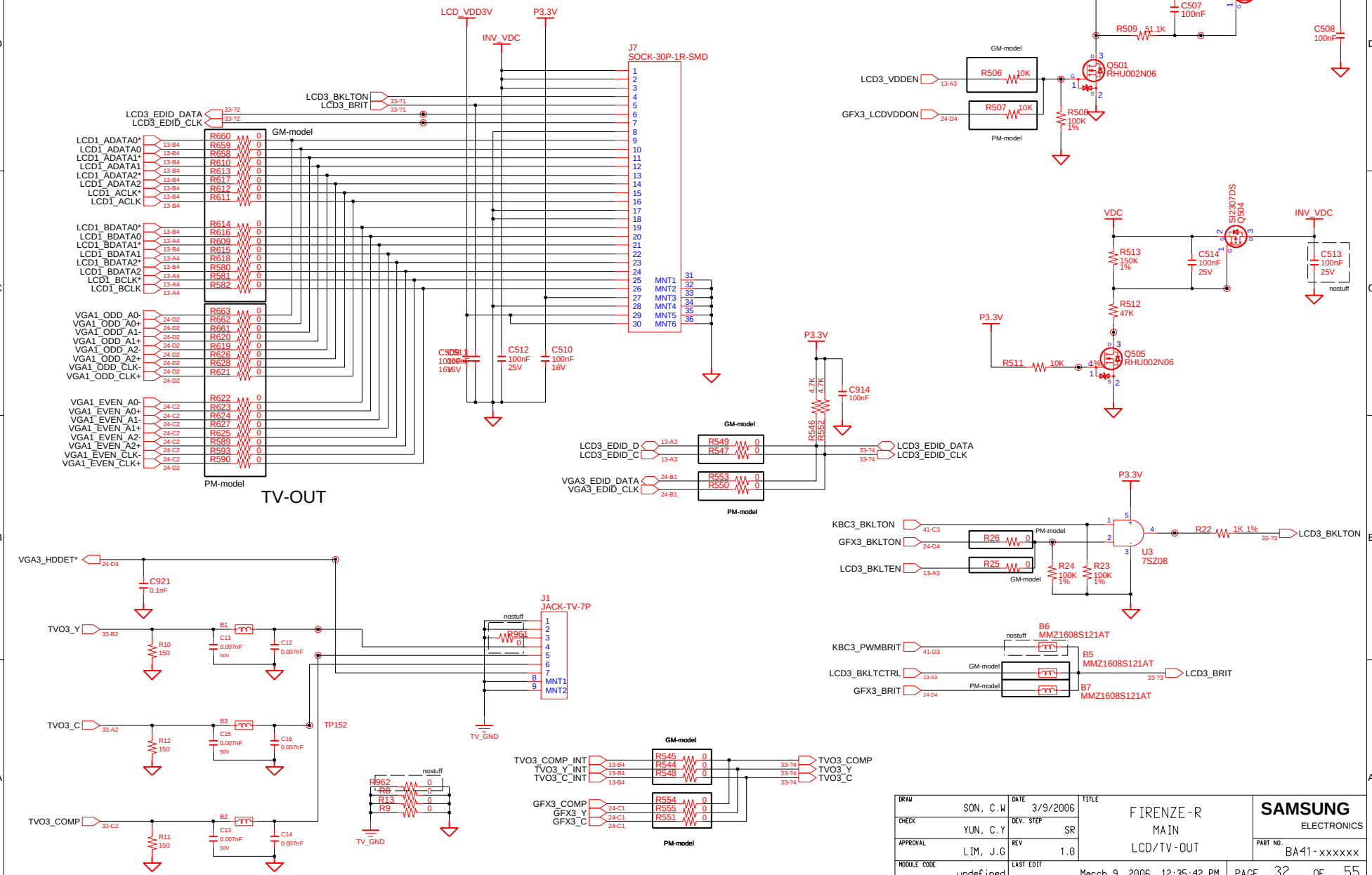
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	31	OF 55

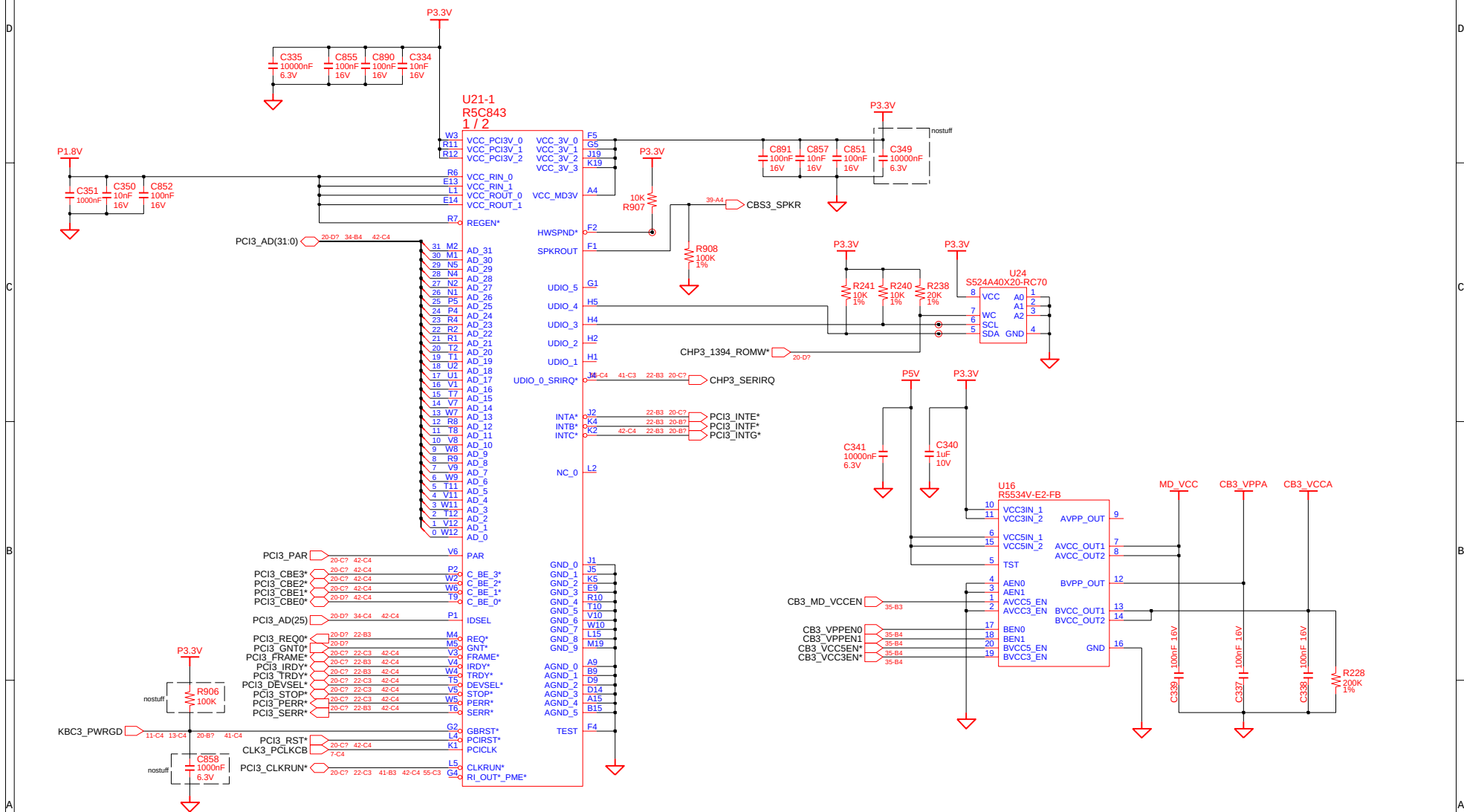
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LCD CONNECTOR

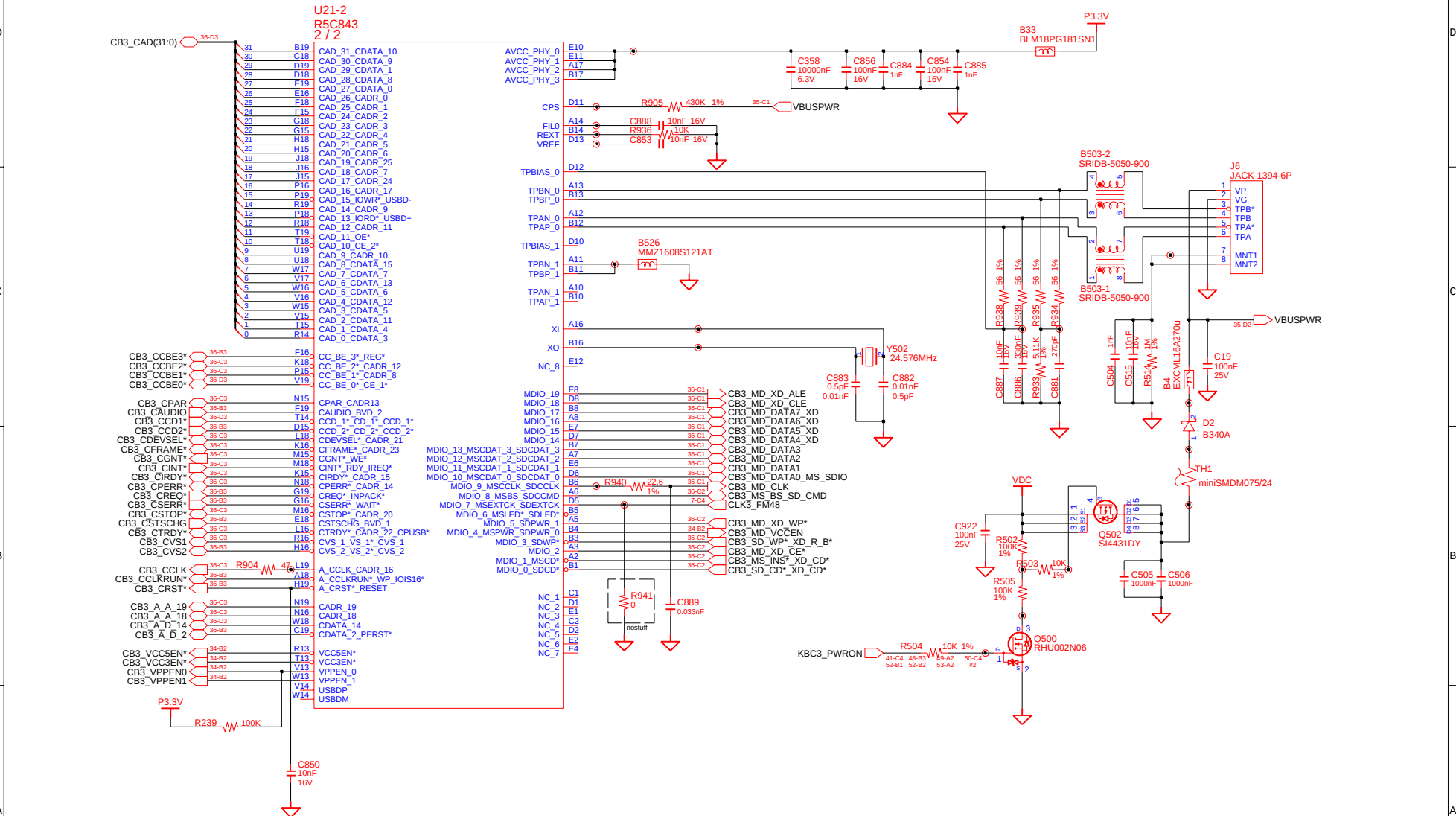


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN LCD/TV-OUT	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	32	OF 55

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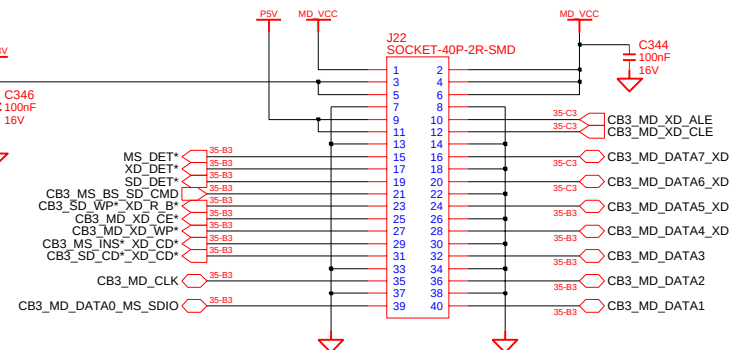
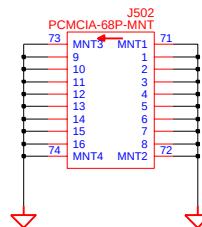
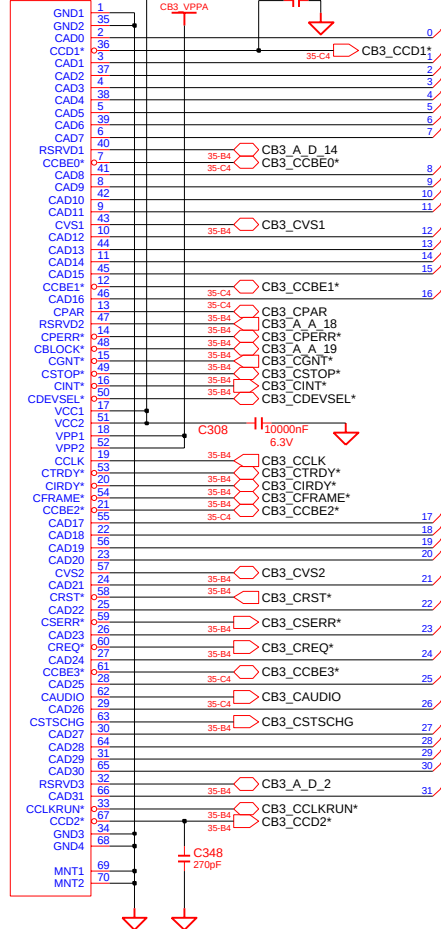
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CARDBUS(1/2)	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	33	OF 55



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		CARDBUS(2/2)	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	34	OF 55

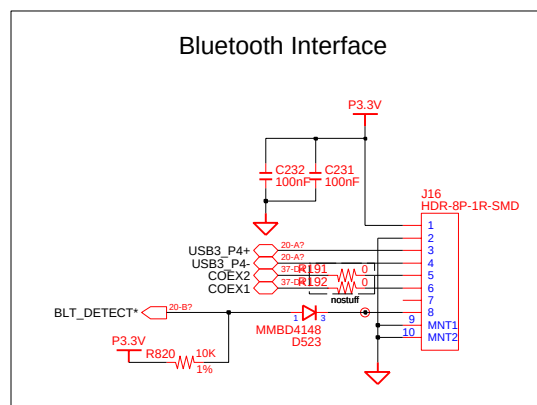
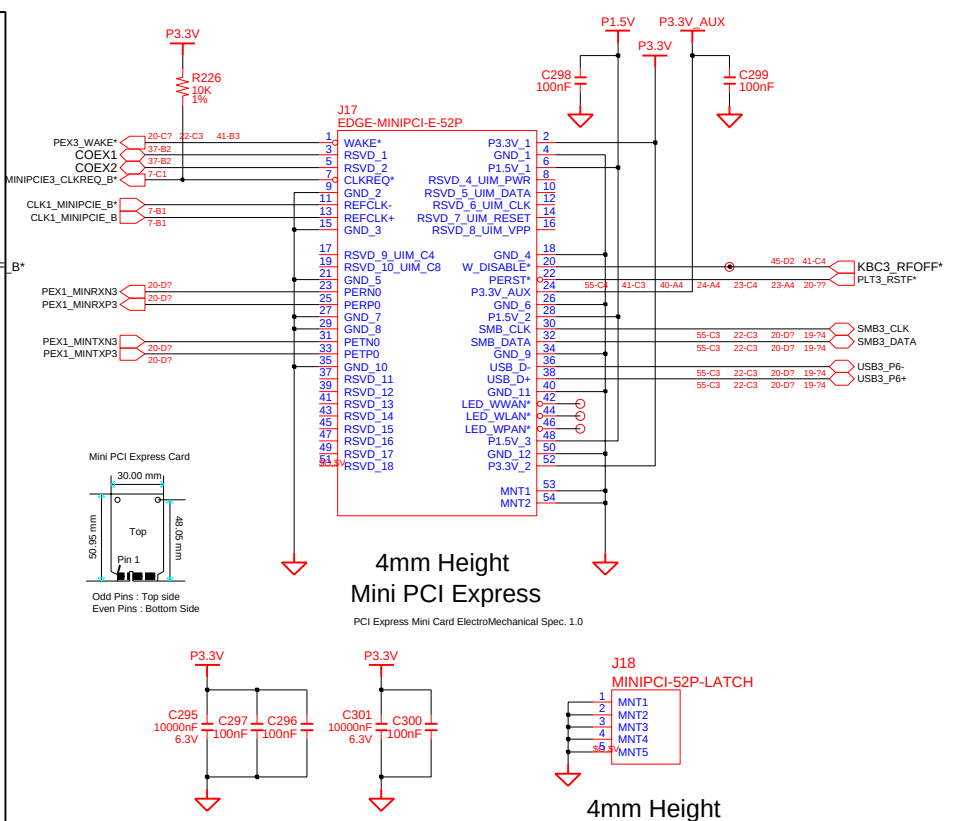
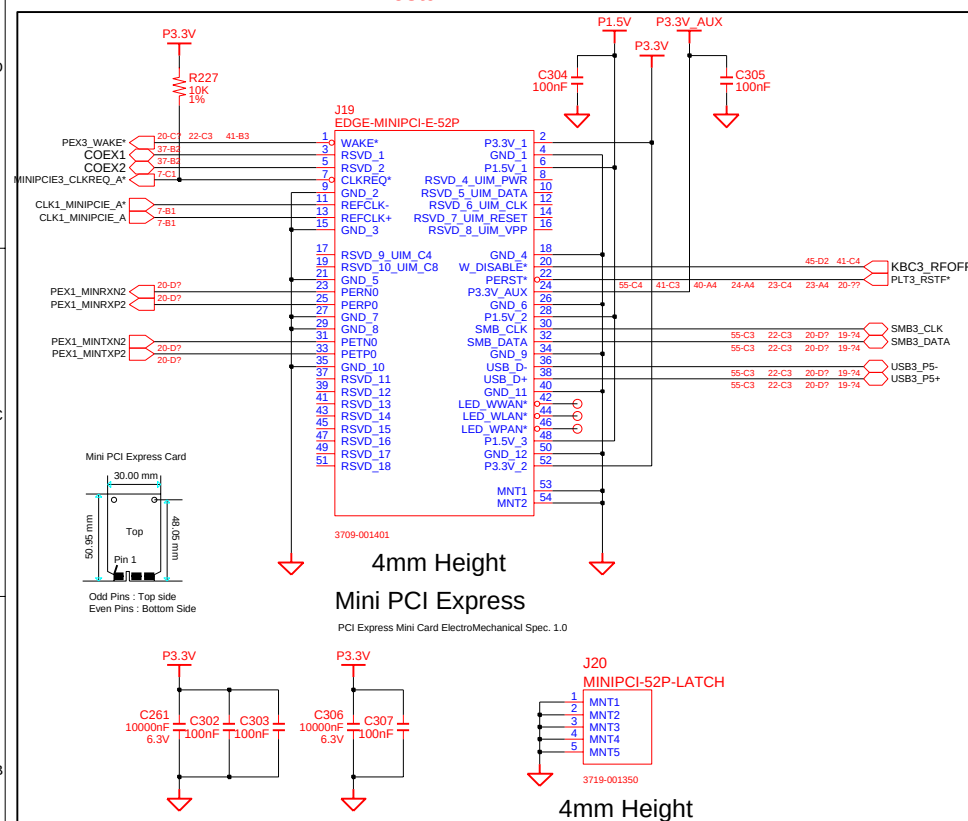
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J501
PCMCIA-68P-REVERSE



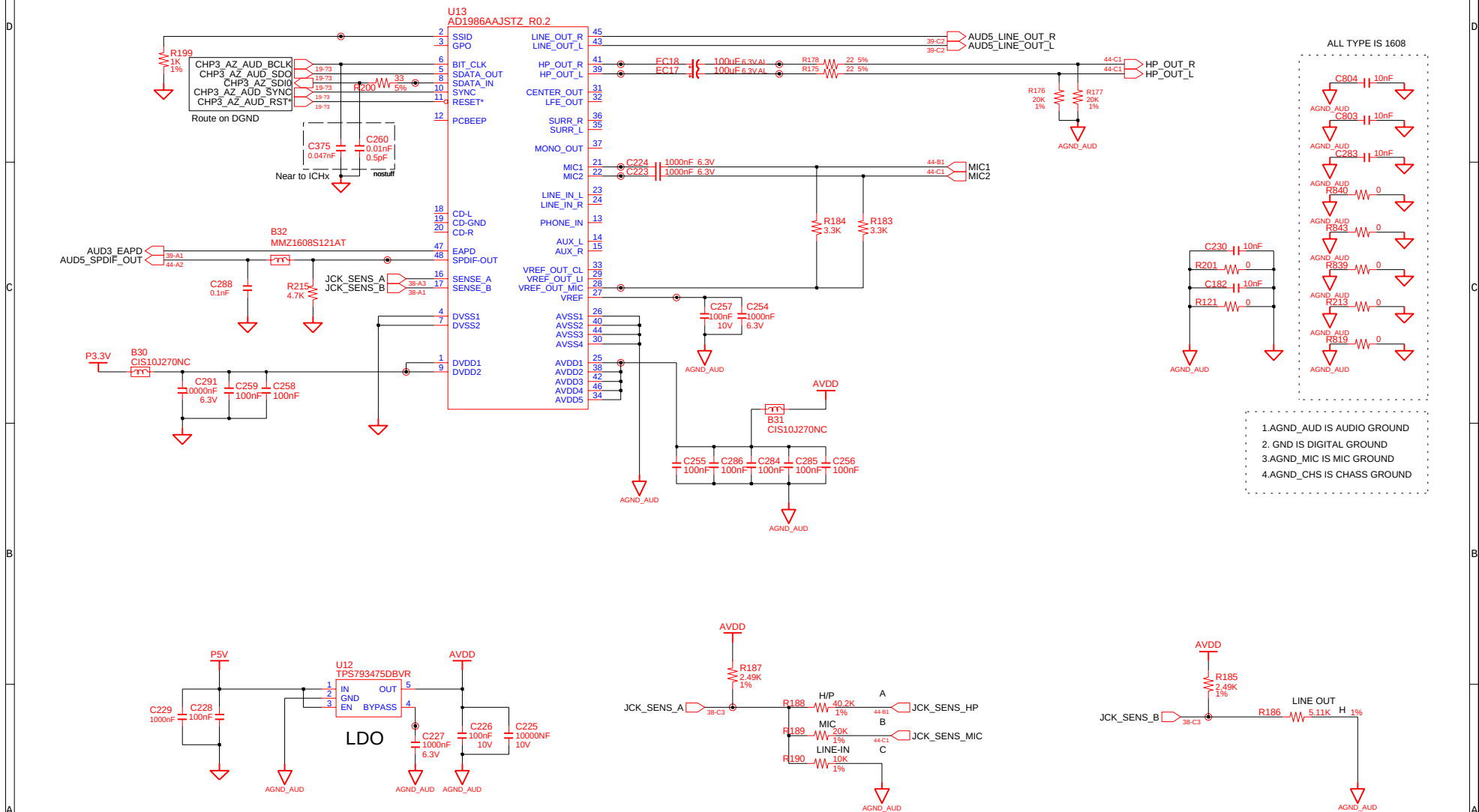
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0		CARDBUS CONN/MEDIA CARD	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	35	OF 55

nostuff



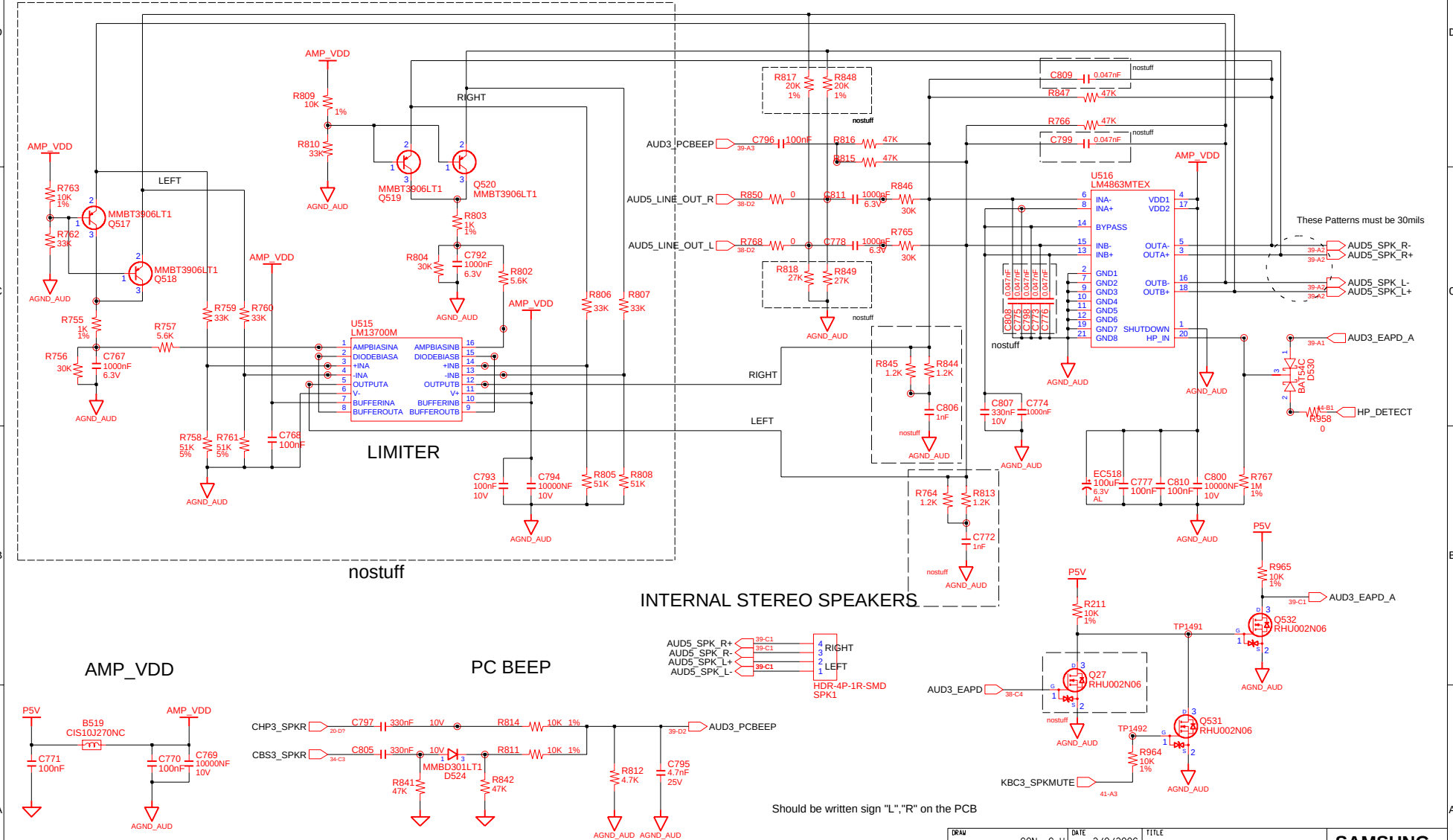
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MINI CARD	SAMSUNG ELECTRONICS		
CHECK	YUN, C.Y	DEV. STEP	SR					
APPROVAL	LIM, J.G	REV	1.0					
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM				PAGE	36
						PART NO.	BA41-xxxxxx	

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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	37 OF 55	

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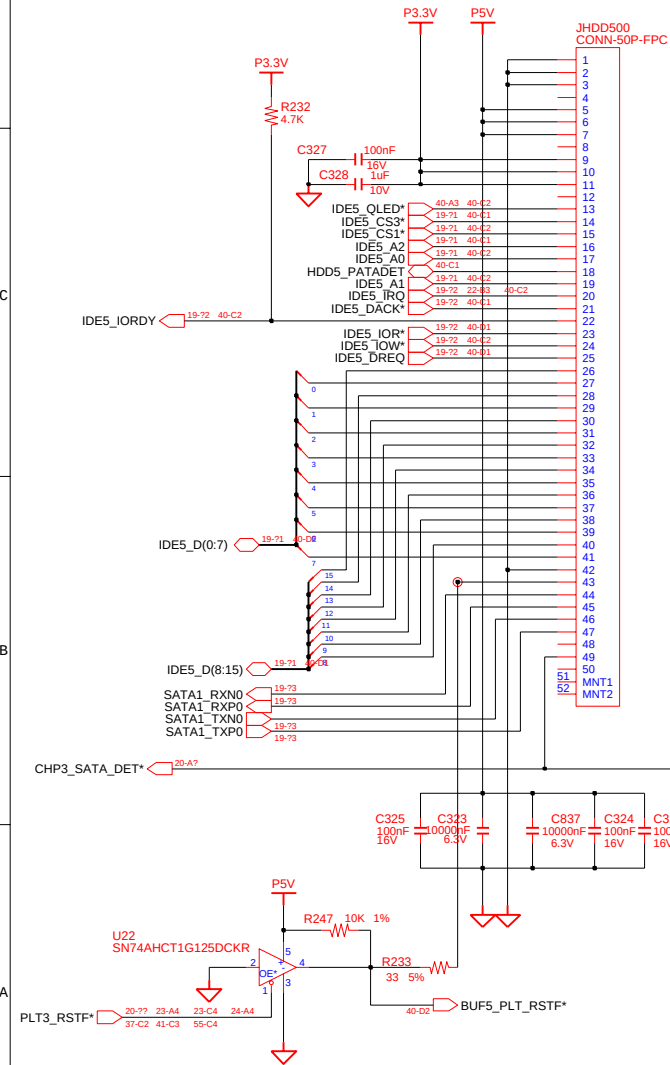
These Patterns must be 30mils

Should be written sign "L", "R" on the PCB

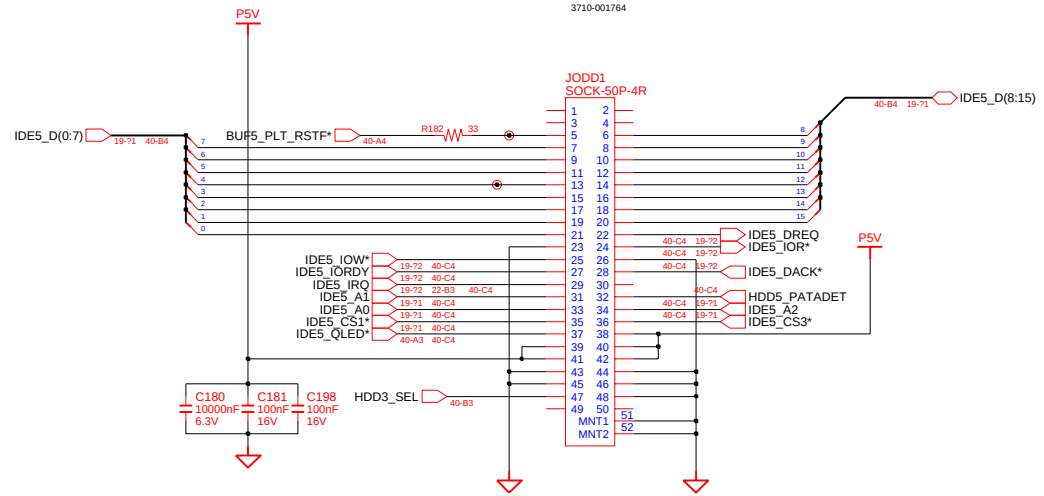
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CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	38	OF 55

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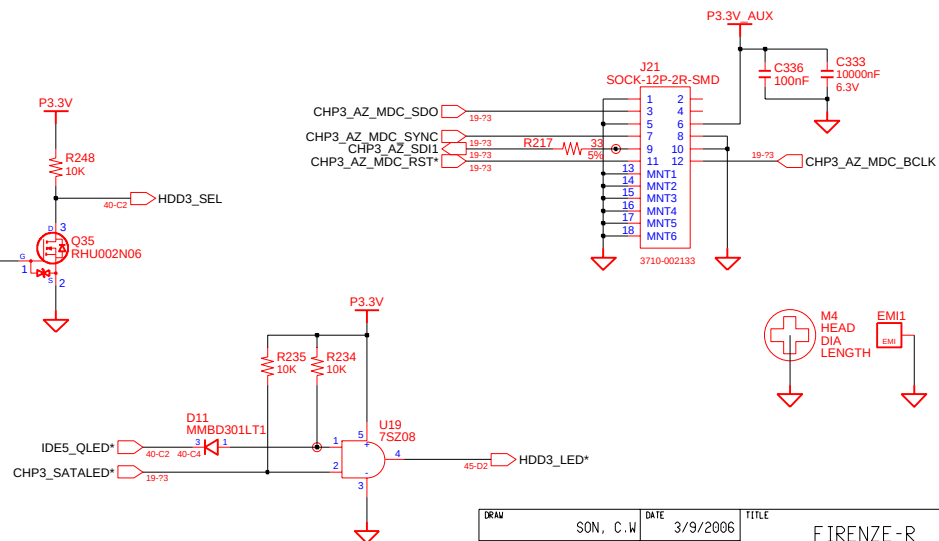
MAIN TO HDD



MAIN TO ODD

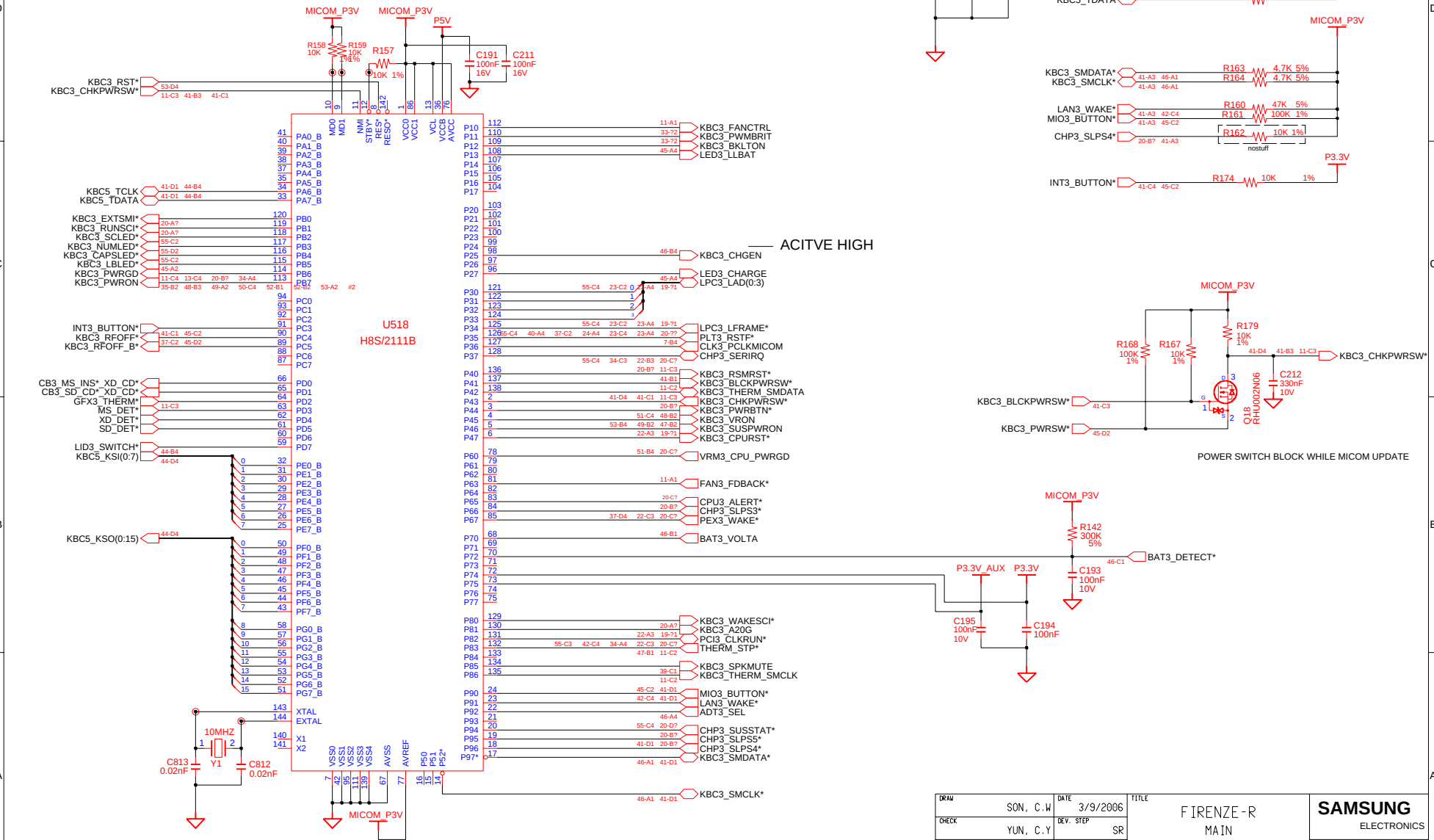


MDC Connector



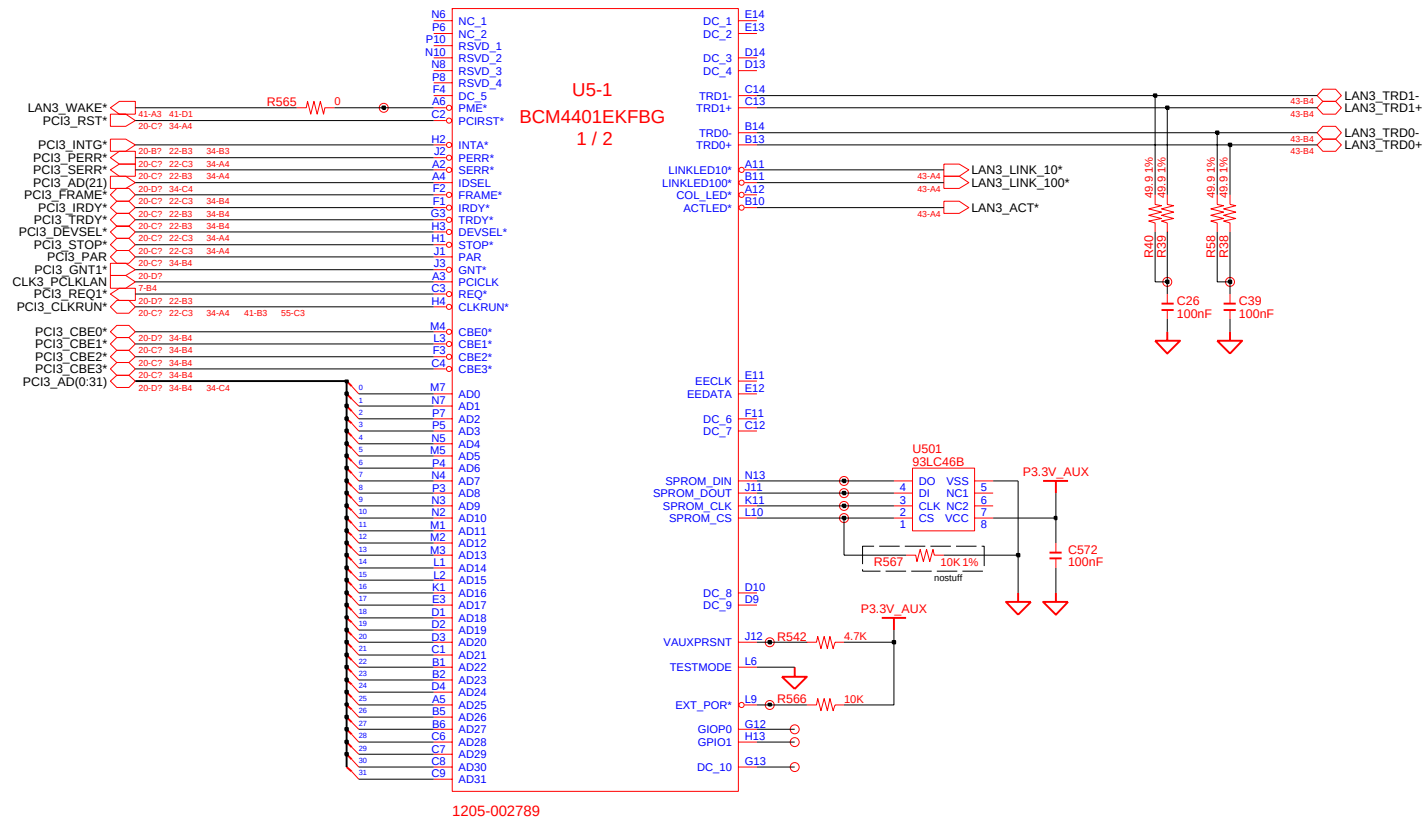
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN HDD/ODD/MDC CONN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	39	OF 55

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DRAW	SON, C. W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MICOM	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J. G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	40	OF 55

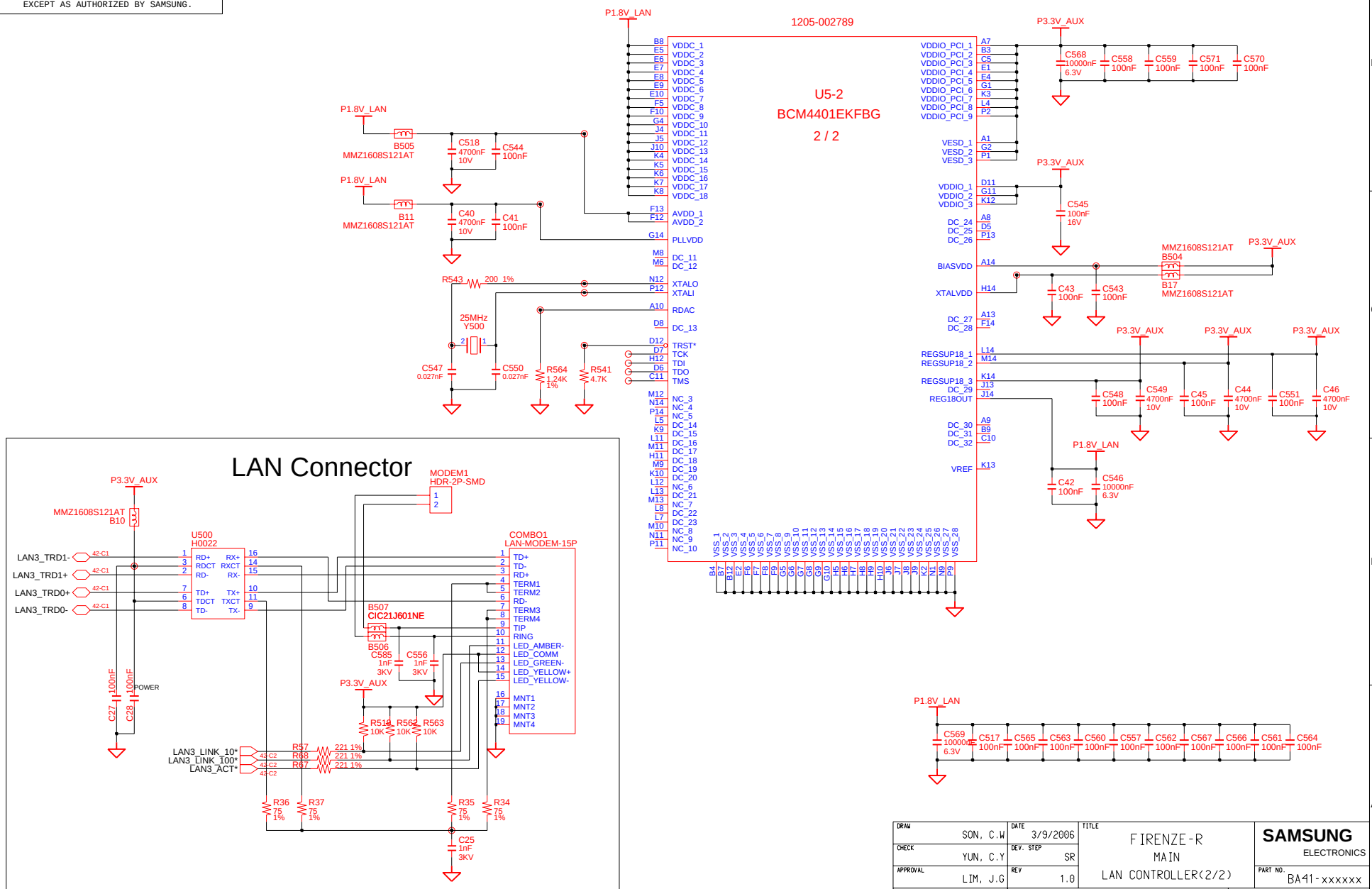
LAN Controller (Only 10/100M)



DRAW	SON, C. W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN LAN CONTROLLER(1/2)	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J. G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	41	OF 55

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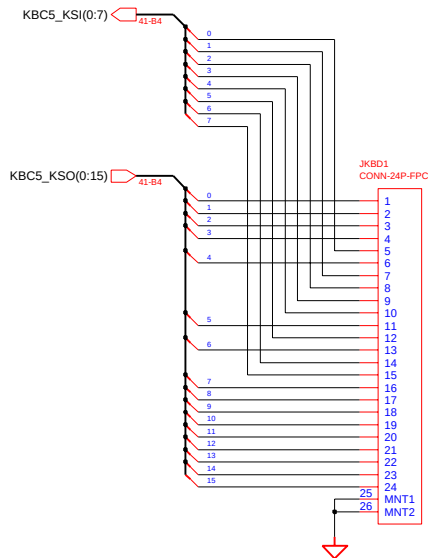
LAN Controller (Only 10/100M)



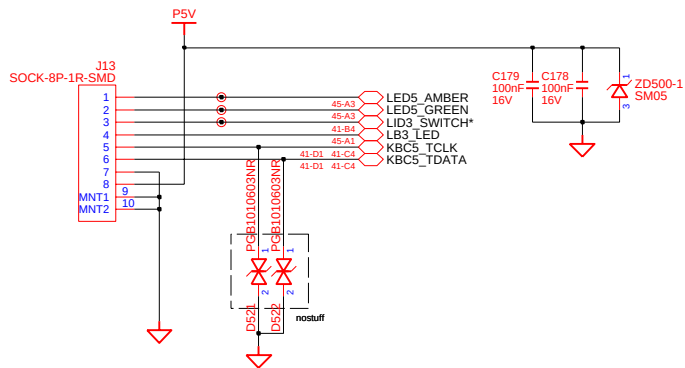
DRAM	SON, C.W	DATE	3/9/2006	FIRENZE-R MAIN LAN CONTROLLER(2/2)		SAMSUNG ELECTRONICS	
CHECK	YUN, C.Y	DEV. STEP	SR				
APPROVAL	LIM, J.G	REV	1.0	PART NO. BA1-xxxxxx		43 OF 56	
MODULE CODE	undefined		LAST EDIT March 9, 2006 12:35:42 PM				

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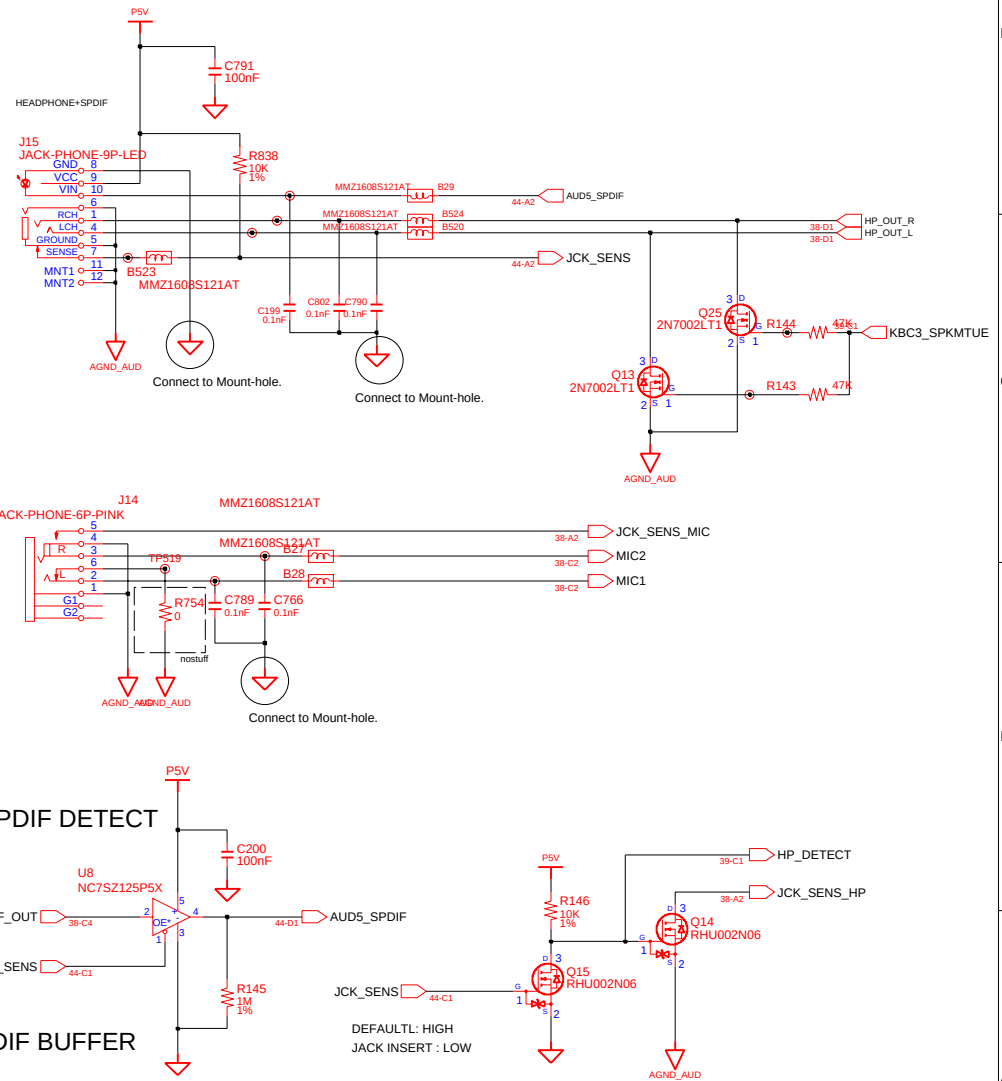
KEYBOARD



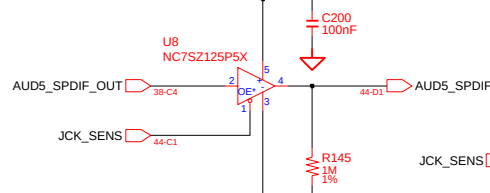
TOUCH PAD



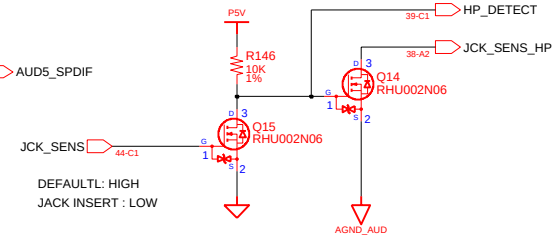
OPTICAL SPDIF OUTPUT & HEADPHONE



SPDIF DETECT



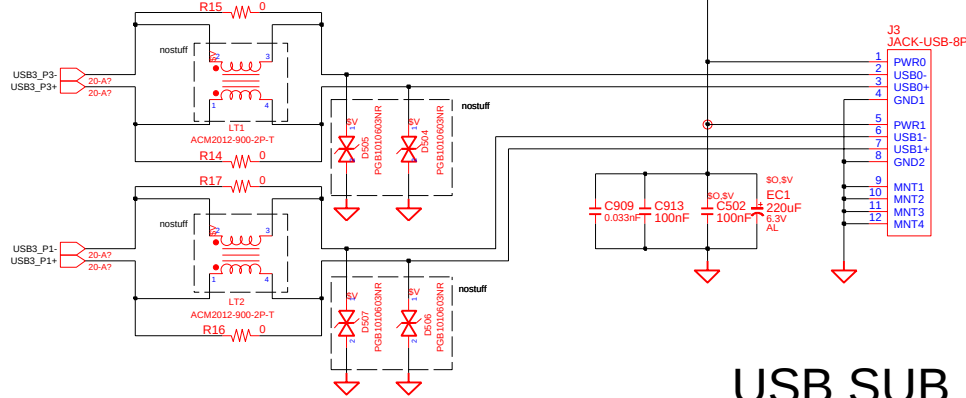
SPDIF BUFFER



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		KBD/TPAD/HP/MIC	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	43 OF 55	

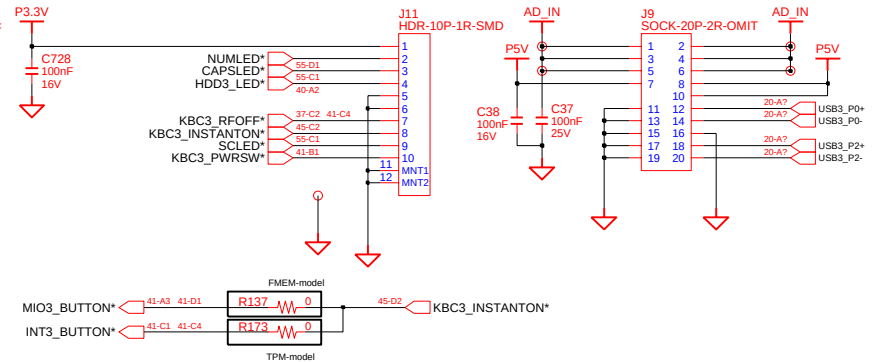
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USB PORT

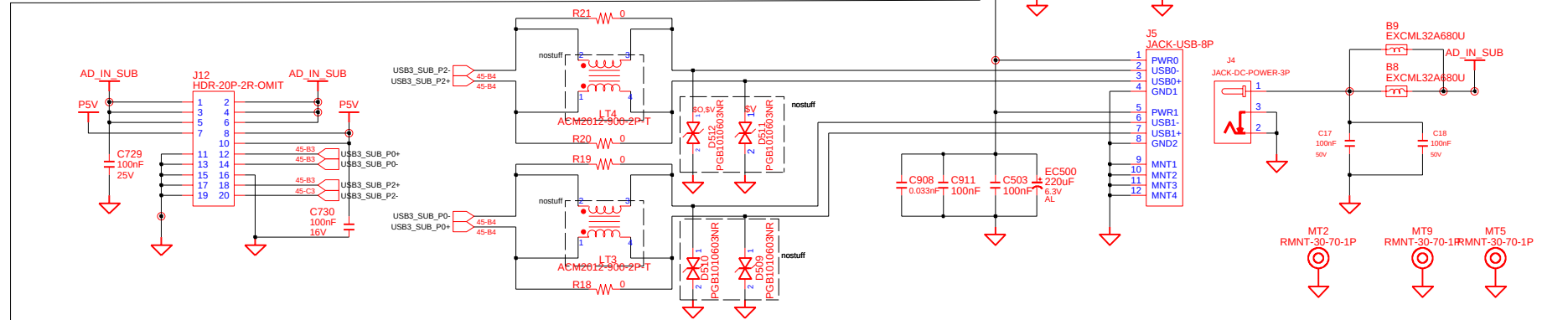


MAIN TO ON-TOP

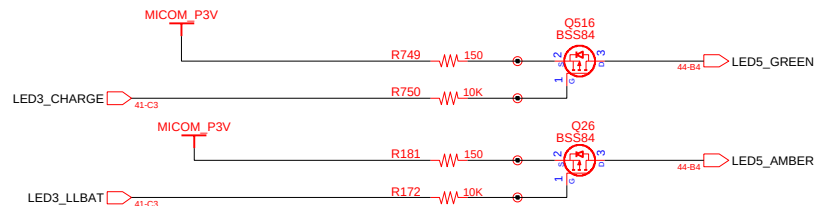
MAIN TO USB



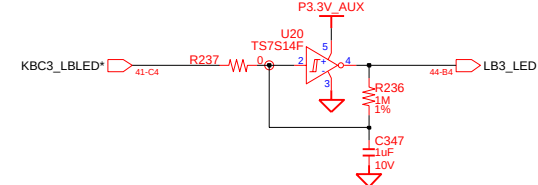
USB SUB B'D



ADAPTER IN / CHARGER LED



POWER ON / LB LED

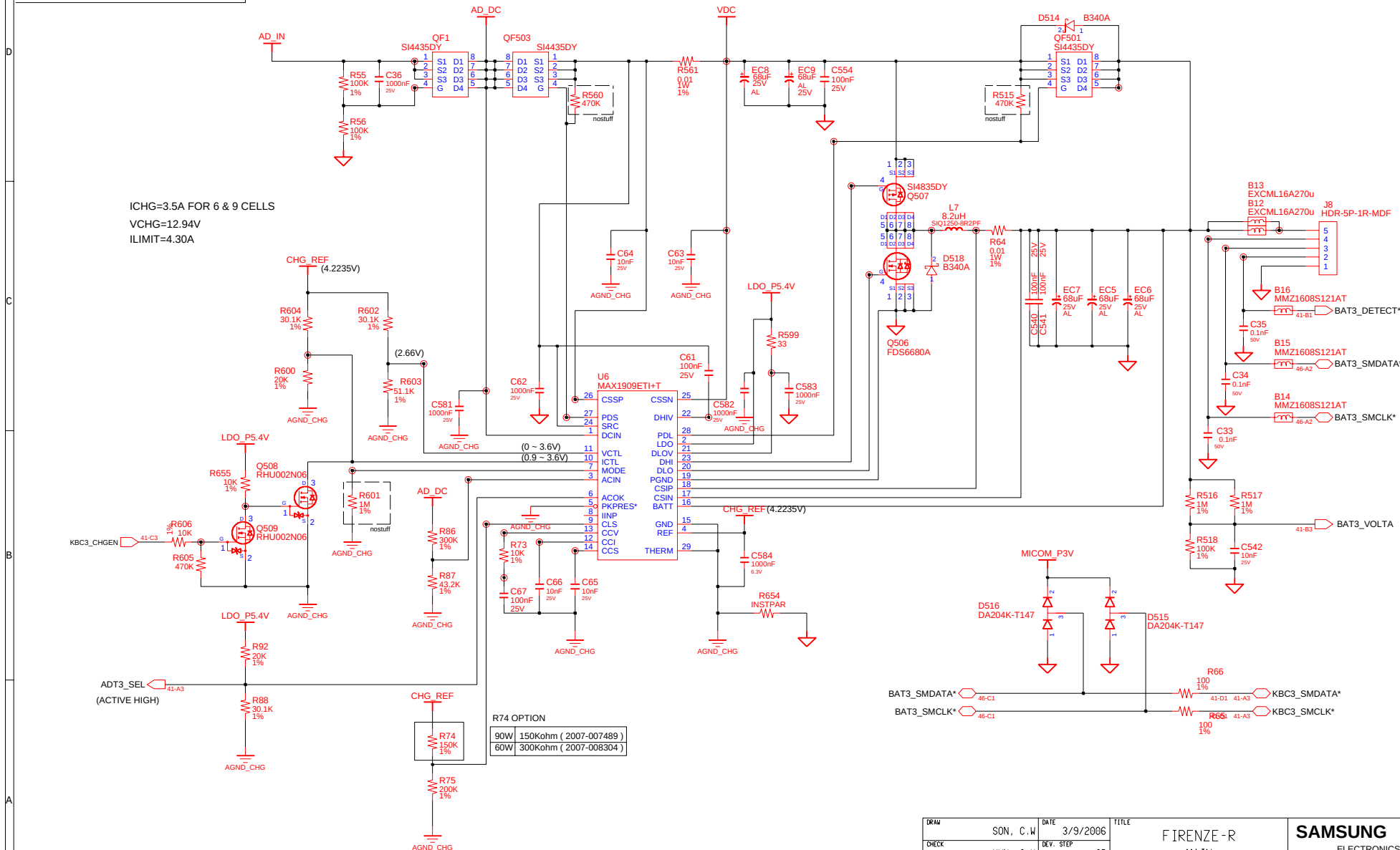


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		USB PORT/LED/ON-TOP	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	44 OF 55	

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CHARGER & POWER MANAGEMENT

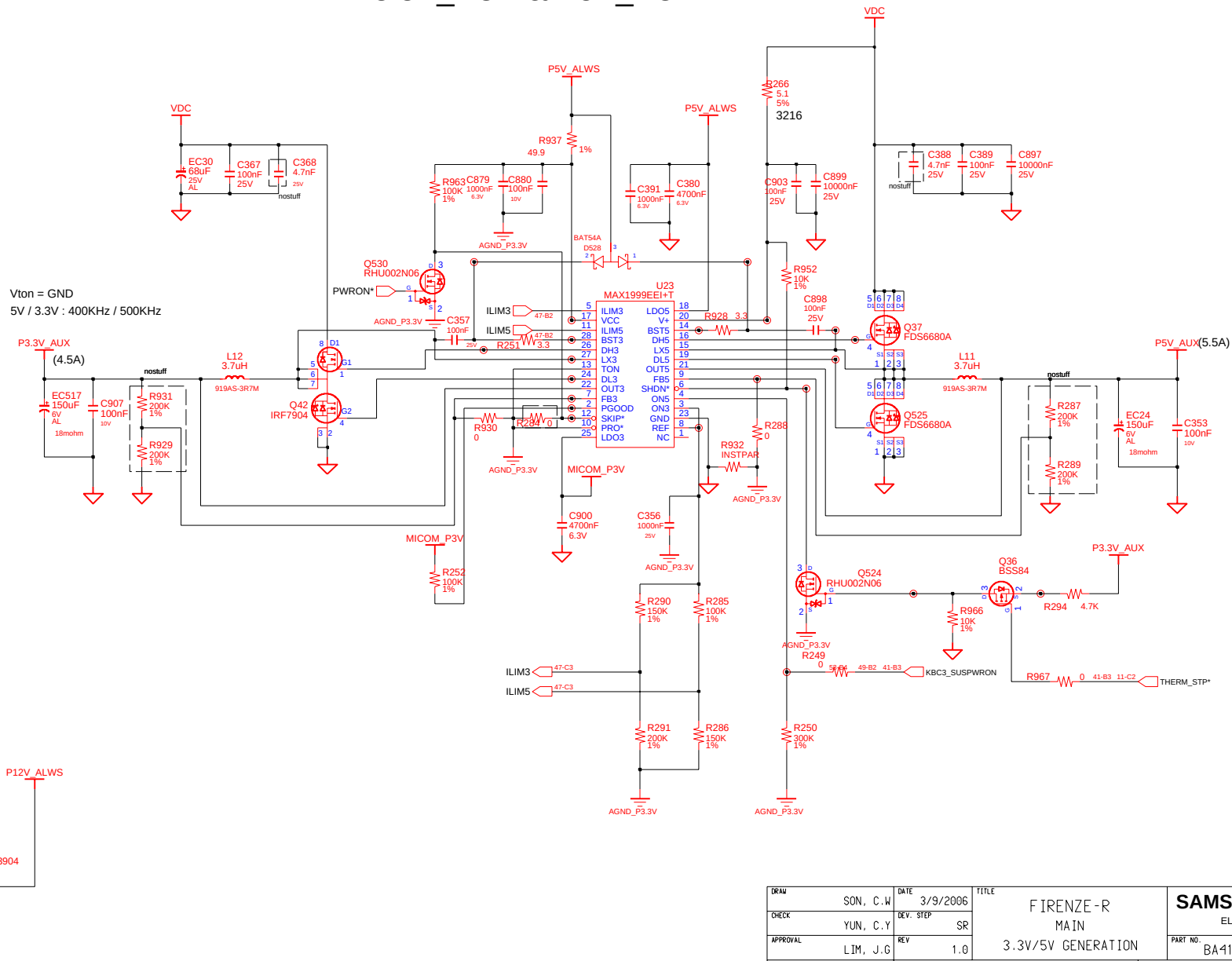
ICHG=3.5A FOR 6 & 9 CELLS
VCHG=12.94V
ILIMIT=4.30A



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	45	OF 55

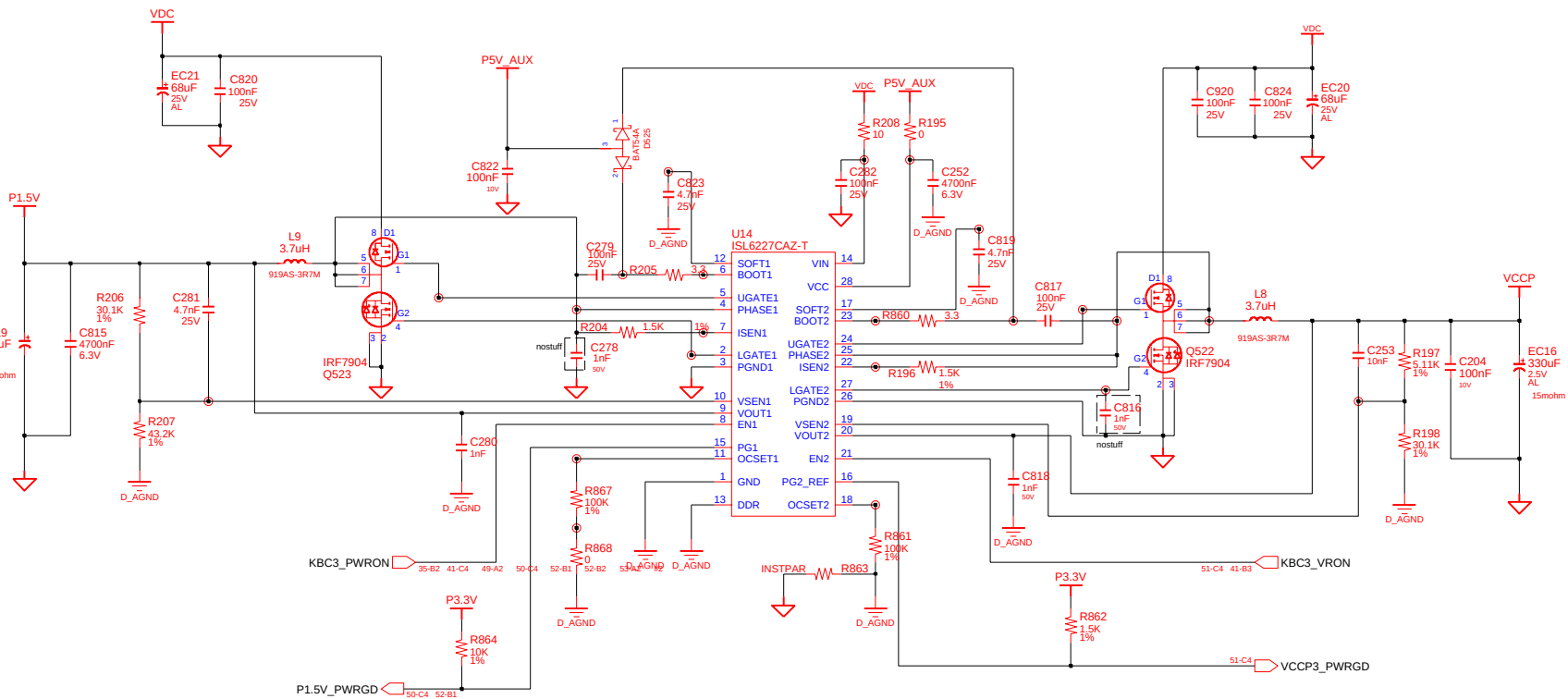
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P3.3V_AUX & P5V_AUX



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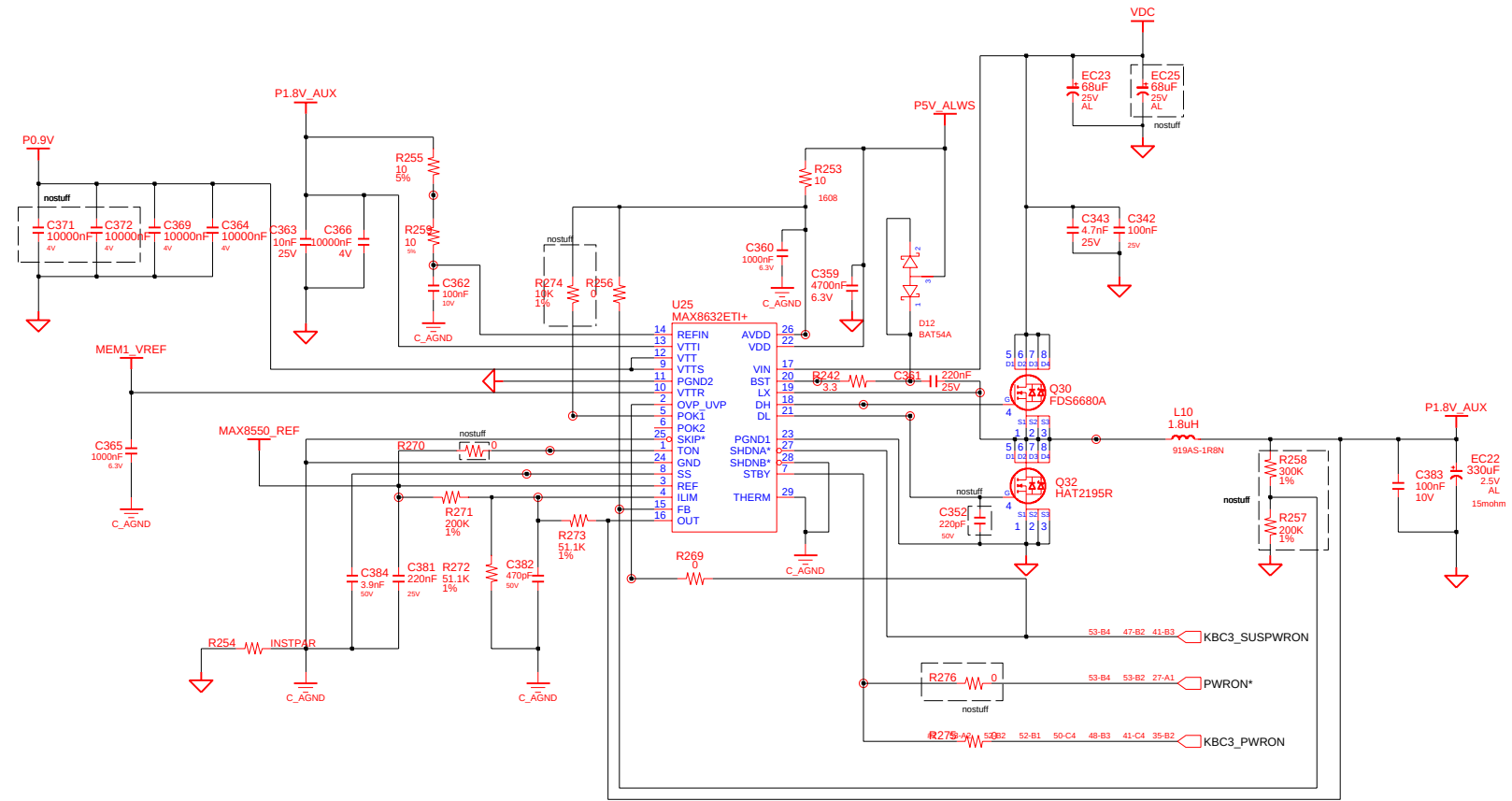
P1.5V & VCCP (1.05V)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 1.5V_AUX/VTT	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	47 OF 55	

DDR2 Power

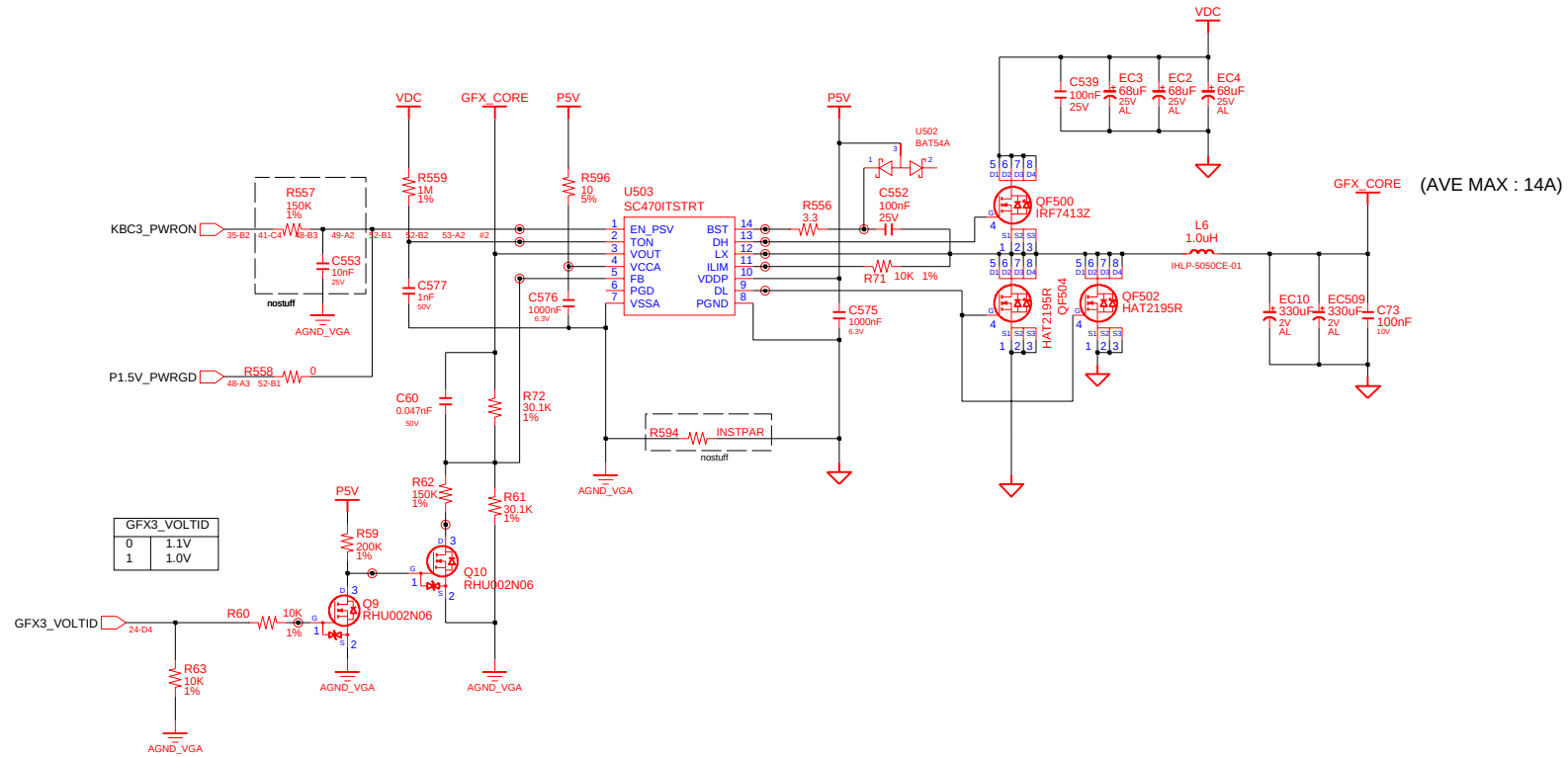
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	48	OF 55

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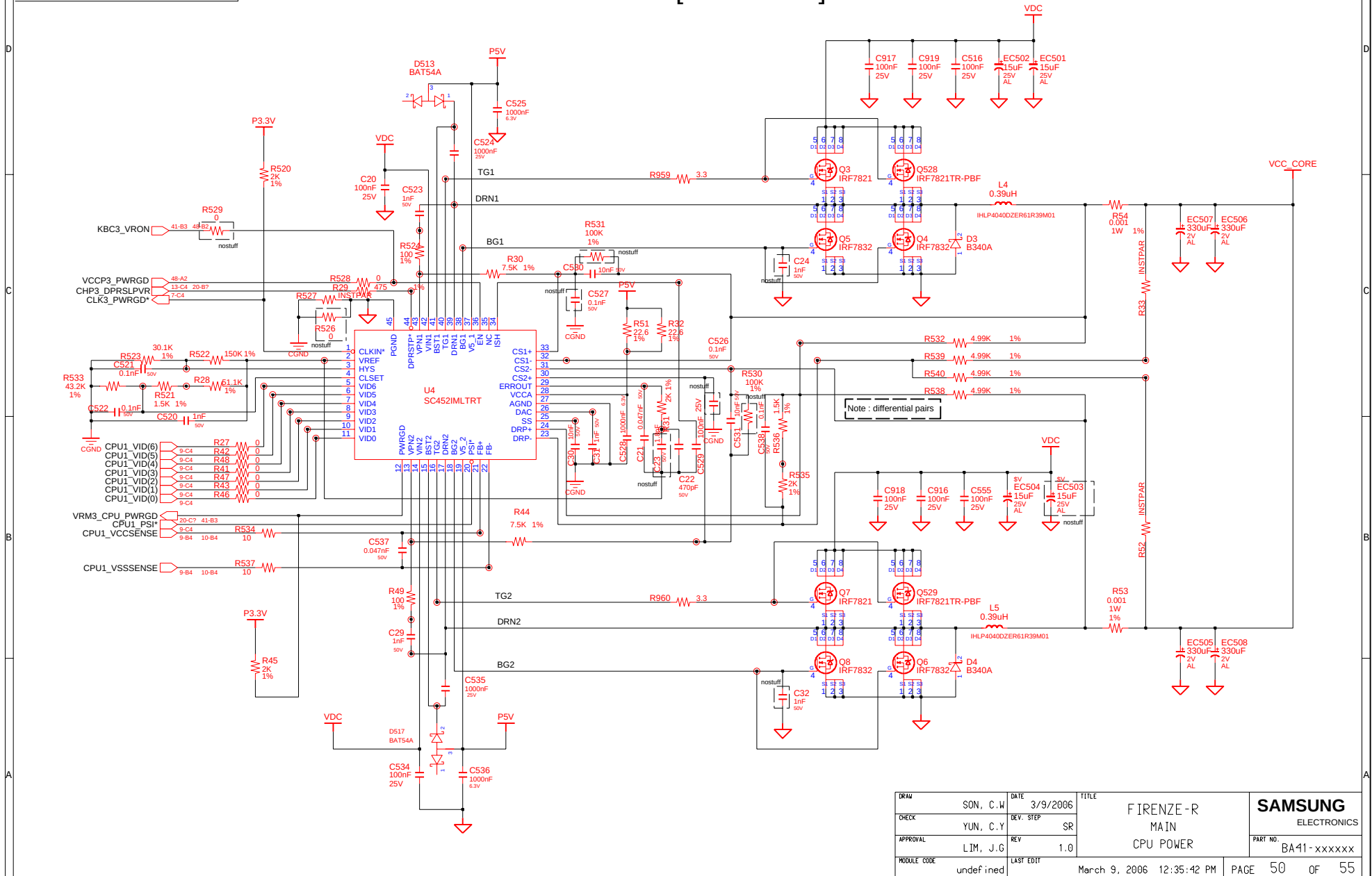
Graphic Core Power



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GRAPHIC CORE POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	49	OF 55

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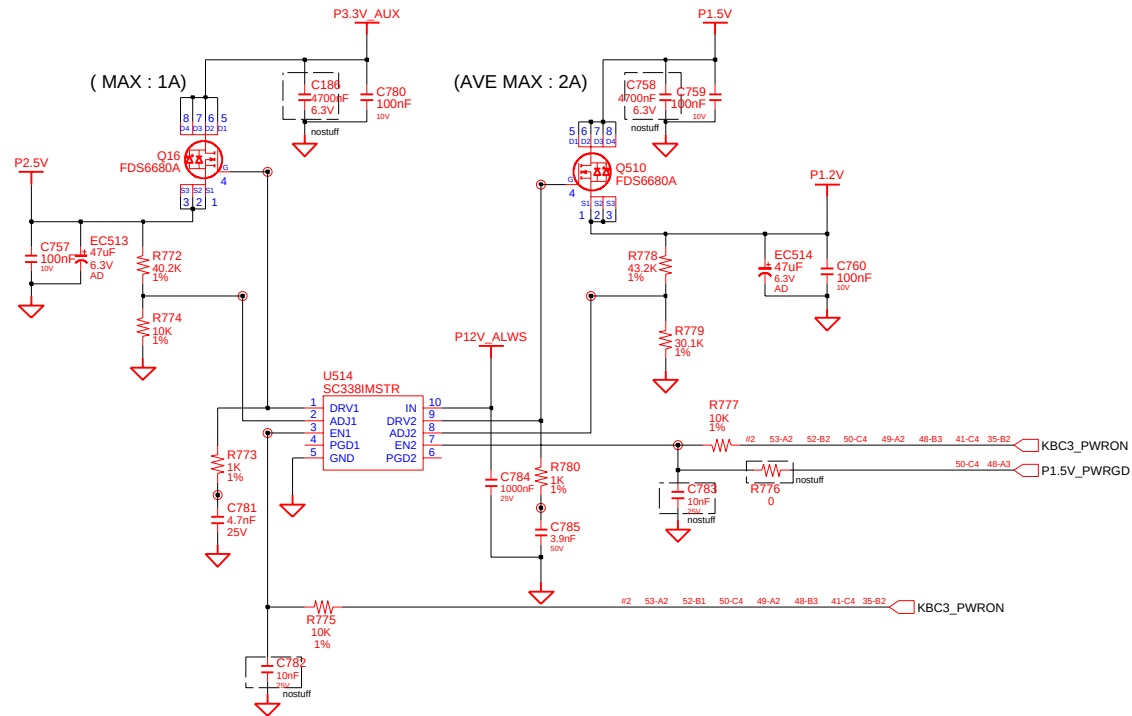
CPU VRM [SEMTECH]



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	50 OF 55	

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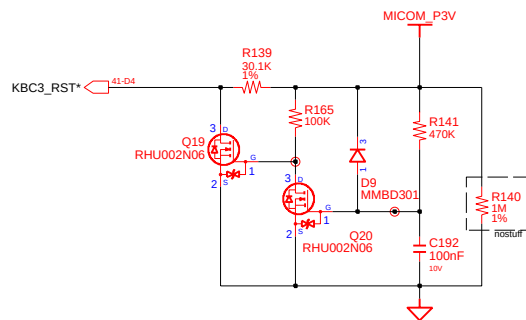
P1.2V / P2.5V POWER



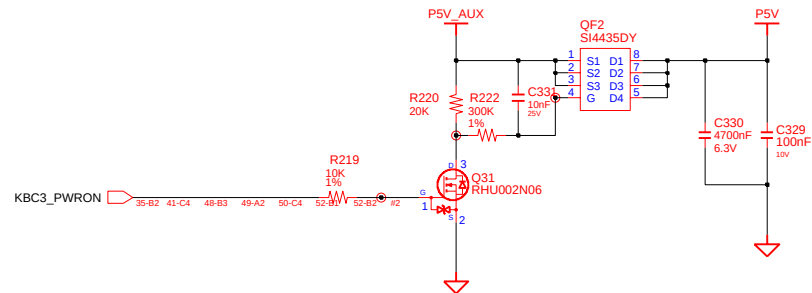
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 1.2V/2.5V POWER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	51 OF 55	

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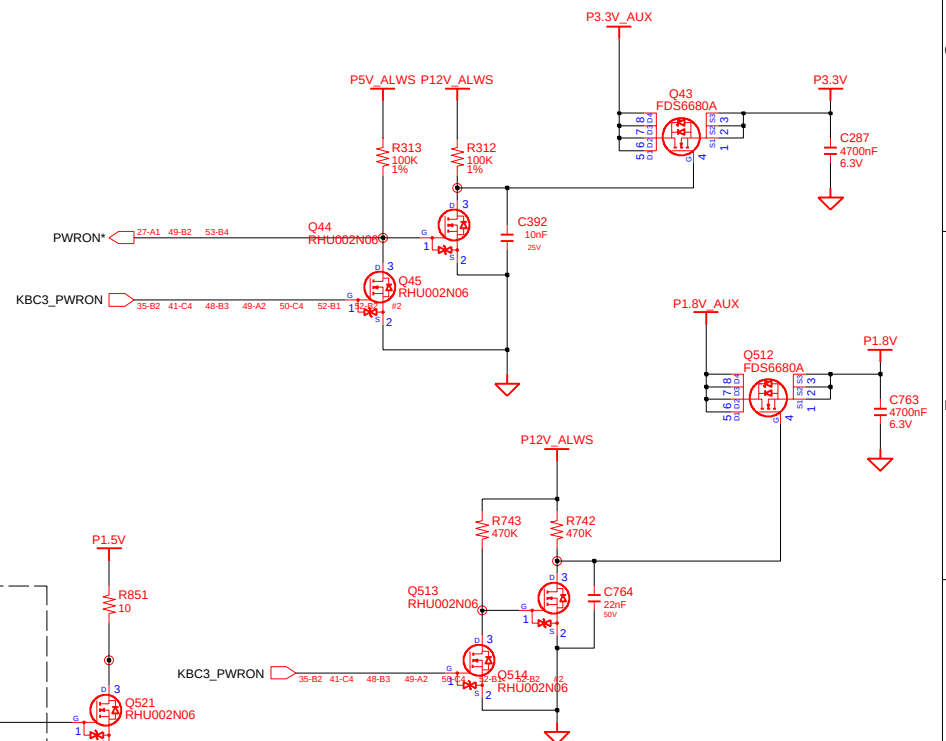
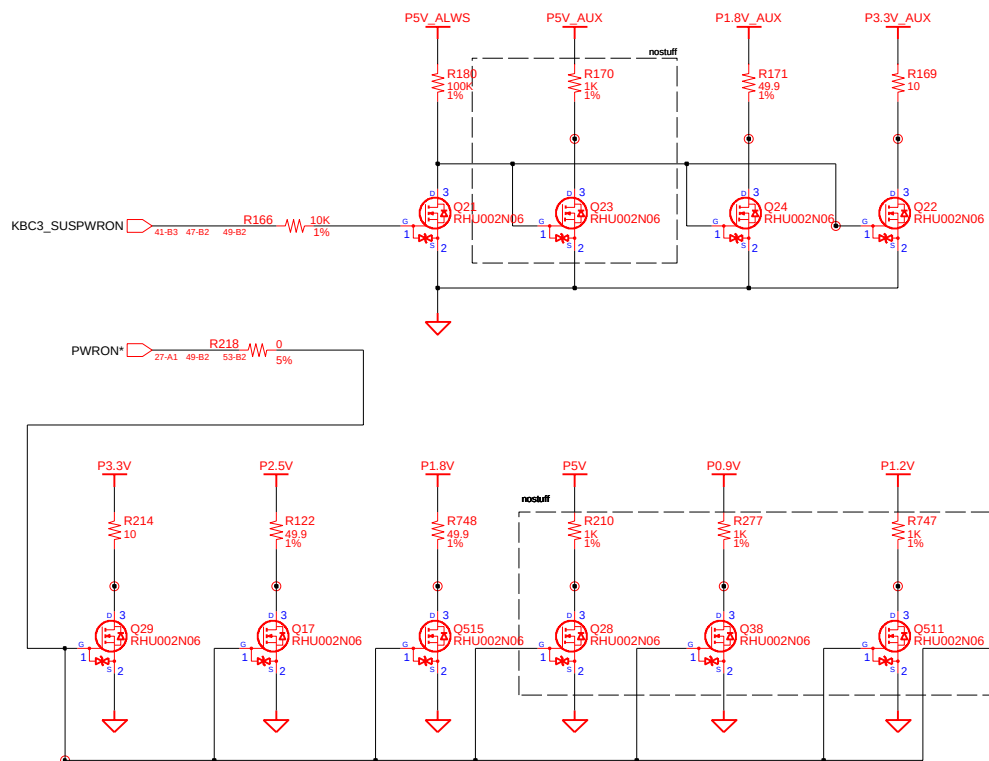
MICOM RESET



Switched Power On (P5V)



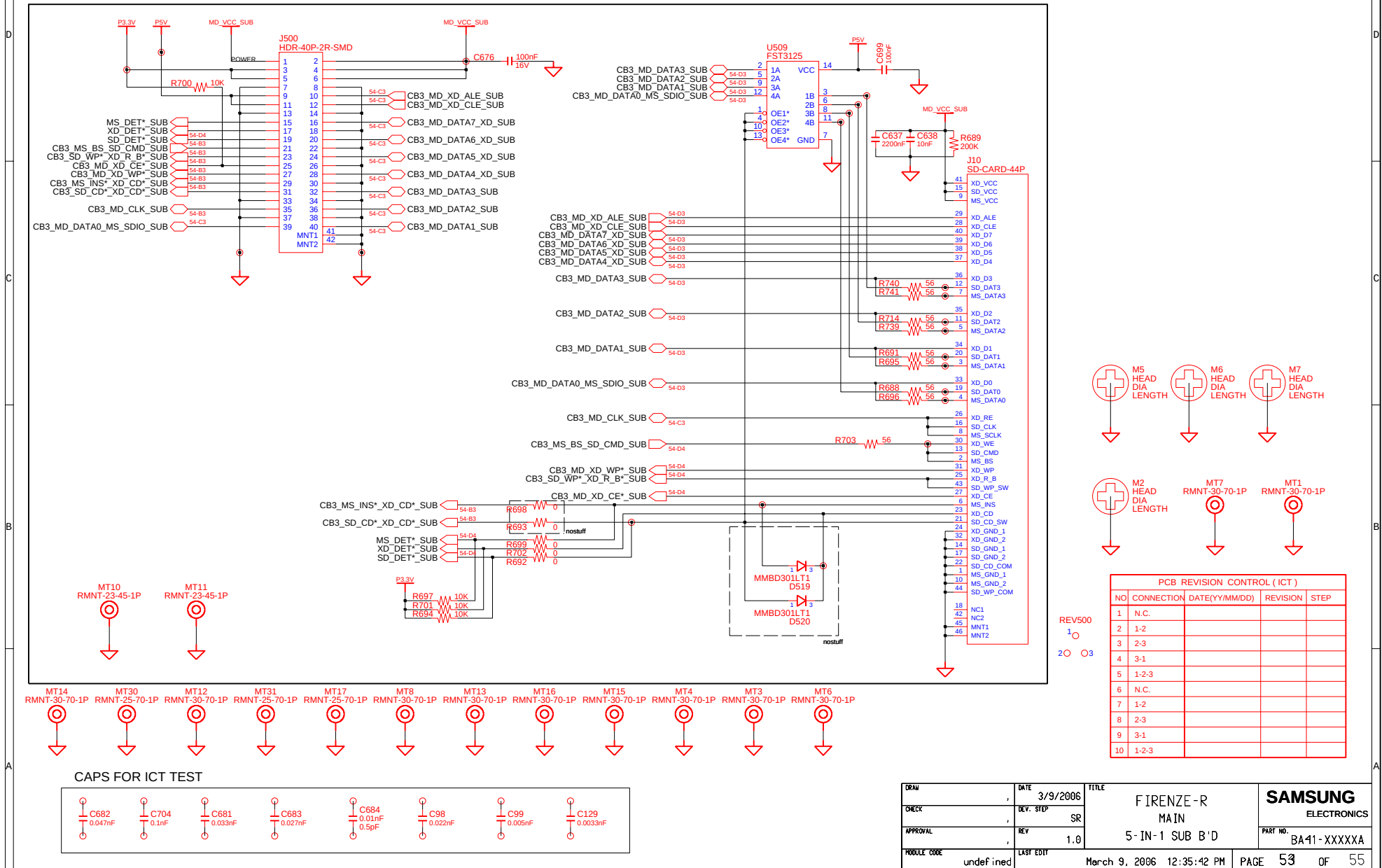
Switched Power On (P3.3V & 1.8V)



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MICOM&SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			PART NO. BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	52	OF 55

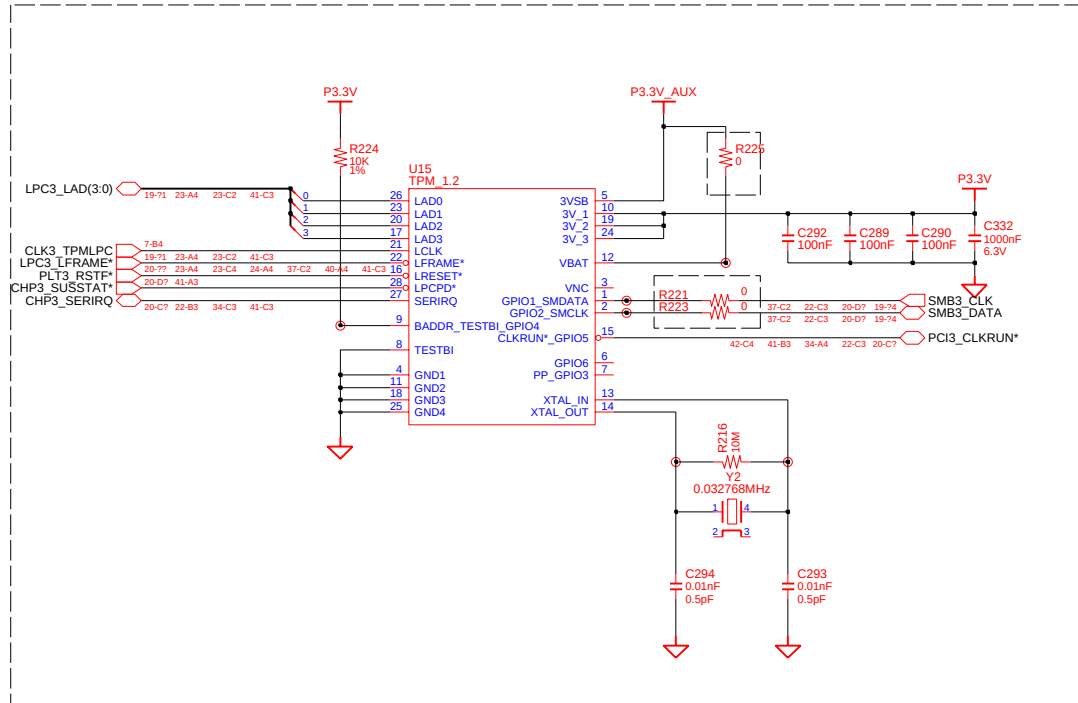
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5-IN-1 SUB B'D

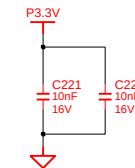
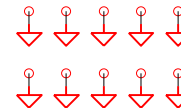
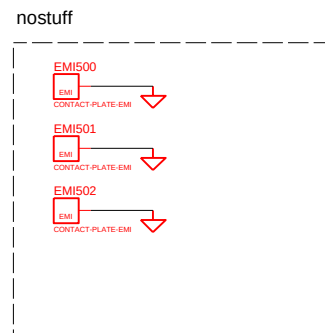
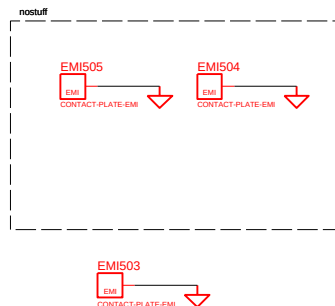
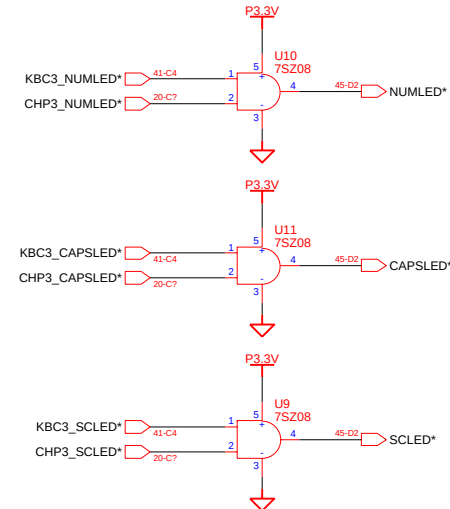


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nostuff



LED SIGNAL



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		TPM	
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	54 OF 55	

4				3				2				1			
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TP913MIC1 TP914MIC2 TP919COXEK1 TP920COXEK2 TP923ILIM3 TP924ILIM5 TP925MCKEA TP911GF3X_C TP912GF3X_Y TP907SCLED* TP908TV03_C TP909TV03_Y TP890IDES_A0 TP891IDES_A1 TP892IDES_A2 TP893OLB3_LED TP898MS_DET* TP873CNUMLED* TP874SD_DET* TP875VBUSPWR TP876XD_DET* TP877ADPT3_SEL TP878CAPSLED* TP879CB3_CCLK TP880CB3_CPAR TP881CB3_CVSD TP882CB3_CVSD TP884CPU1_NMI TP885CPU1_TK TP886CPU1_TDI TP887CPU1_TMS TP888CRT3_RED TP889GF3X_Z TP826GF3X_RED TP827OHDD3_SEL TP828HP_OUT_L TP829HP_OUT_R TP830IDES_IRQ TP831JCK_SENS TP712PCIR_PAR TP723SM83_CLK TP698CB3_A_D_2 TP699CB3_CCD1* TP700CB3_CCD2* TP701CB3_CNT1* TP702CB3_CNT2* TP703CB3_CREQ* TP704CB3_CRS1* TP705CB33_SPKR TP706CHP3_SPKR TP691OCRT3_BLUE TP692GF3X_BLUE TP693GF3X_BRIT TP694GF3X_COMP TP695GF3X_HCLK TP696OHDD3_LED* TP697IDES_CS1* TP627IDES_CS3* TP628IDES_DV0 TP629IDES_DV1 TP630IDES_DV2 TP631IDES_DV3 TP632IDES_DV4 TP633IDES_DV5 TP634IDES_DV6 TP635IDES_DV7 TP636IDES_DV8 TP637IDES_DV9 TP638IDES_DREQ TP639IDES_IOR* TP640IDES_IOW* TP641KBC3_A265 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TP1382CB3_CCBEL* TP1383CB3_CCBEM* TP1384CB3_CCBEN* TP1385CB3_CCBEO* TP1386CB3_CCBEP* TP1387CB3_CCBEL* TP1388CB3_CCBEM* TP1389CB3_CCBEN* TP1390CB3_CCBEO* TP1391CB3_CCBEP* TP1392CB3_CCBEL* TP1393CB3_CCBEM* TP1394CB3_CCBEN* TP1395CB3_CCBEO* TP1396CB3_CCBEP* TP1397CB3_CCBEL* TP1398CB3_CCBEM* TP1399CB3_CCBEN* TP1400CB3_CCBEO* TP1401CB3_CCBEP* TP1402CB3_CCBEL* TP1403CB3_CCBEM* TP1404CB3_CCBEN* TP1405CB3_CCBEO* TP1406CB3_CCBEP* TP1407CB3_CCBEL* TP1408CB3_CCBEM* TP1409CB3_CCBEN* TP1410CB3_CCBEO* TP1411CB3_CCBEP* TP1412CB3_CCBEL* TP1413CB3_CCBEM* TP1414CB3_CCBEN* TP1415CB3_CCBEO* TP1416CB3_CCBEP* TP1417CB3_CCBEL* TP1418CB3_CCBEM* TP1419CB3_CCBEN* TP1420CB3_CCBEO* TP1421CB3_CCBEP* TP1422CB3_CCBEL* TP1423CB3_CCBEM* TP1424CB3_CCBEN* TP1425CB3_CCBEO* TP1426CB3_CCBEP* TP1427CB3_CCBEL* TP1428CB3_CCBEM* TP1429CB3_CCBEN* TP1430CB3_CCBEO* TP1431CB3_CCBEP* TP1432CB3_CCBEL* TP1433CB3_CCBEM* TP1434CB3_CCBEN* TP1435CB3_CCBEO* TP1436CB3_CCBEP* TP1437CB3_CCBEL* TP1438CB3_CCBEM* TP1439CB3_CCBEN* TP1440CB3_CCBEO* TP1441CB3_CCBEP* TP1442CB3_CCBEL* TP1443CB3_CCBEM* TP1444CB3_CCBEN* TP1445CB3_CCBEO* TP1446CB3_CCBEP* TP1447CB3_CCBEL* TP1448CB3_CCBEM* TP1449CB3_CCBEN* TP1450CB3_CCBEO* TP1451CB3_CCBEP* TP1452CB3_CCBEL* TP1453CB3															