

SUZHOU-D

CPU : AMD Caspin
Chip Set : AMD RX881+SB710
Remarks : Tigris Platform

Model Name : Suzhou-D
PBA Name : MAIN
PCB Code : GCE :
 NAN :
 HAN :
Dev. Step : PV
Revision : 1.0
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL
XIE BIN	GUO LEI	BC LEE

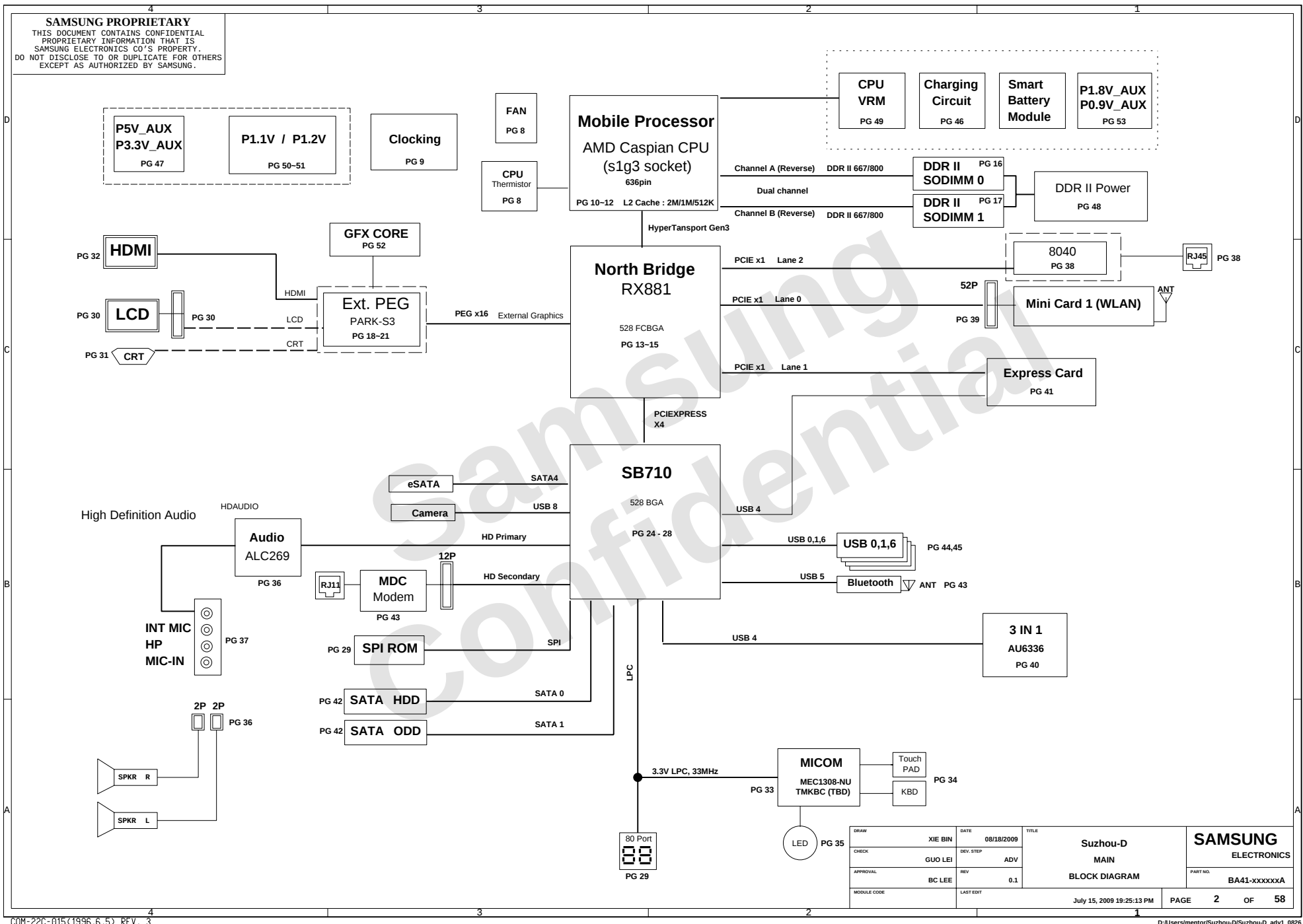
Owner : SEC Mobile R & D Signature : X

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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA
CHECK	GUO LEI	DEV. STEP	ADV		MAIN	
APPROVAL	BC LEE	REV	0.1		COVER	
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	1 OF 58	

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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT				
				July 15, 2009 19:25:13 PM	PAGE 2 OF 58	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE0	Core Voltage for CPU
CPU_CORE1	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for M92, RX881
P1.2V	Core Voltage for SB710
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V_AUX	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MECL308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

I²C / SMB Address

Devices	Address	Hex	Bus
SB710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	EXPRESS CARD

PCI Express Assign

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	EXPRESS CARD
2	LOW
3	NC
4	NC
5	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)
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REVISION HISTORY

See rev notes for more information.

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	BOARD INFORMATION	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	3	OF 58

POWER DIAGRAM

Rev 0.1

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AC Adapter

Battery DC

VDC

P3.3V_MICOM

MICOM LED SB710

P5.0V_STB

USB N Charger

P12.0V_ALW

KBC3_SUSPWR
(CHP3_S4_STATE*)

P1.8V_AUX

AMD S1G3
SODIMM (DDR II)

P5V_AUX

USB connector

P0.9V_AUX

DDR II-Termination

P1.2V_AUX

SB710

P3.3V_AUX

SB710
EXPRESS CARD
WLAN
LAN
MDC
THERMAL
LVDS
LED

P1.2V_LAN

LAN

KBC3_PWRON
(CHP3_SLPS3*)

P1.8V

RX881
PARK
gDDR-3 for PARK
eSATA Reapter
AU6336

P5.0V

THERMAL CRT HDMI
SB710 MICOM AUDIO
ODD HDD CAMERA
TOUCH PAD

EGFX_CORE

PARK

P1.0V

PARK

P1.5V

CK505
WLAN
EXPRESS CARD

P2.5V

S1G3

P3.3V

CK505 THERMAL RX881
DDR2 PARK CRT
LVDS HDMI SB710
SPI WLAN LEDS
LAN AUDIO EXPRESS CARD
HDD BT AU6336

KBC3_VRON

CPU_CORE0,1

S1G3

P1.2V

S1G3
RX881
SB710

P1.1V

RX881
PARK

Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

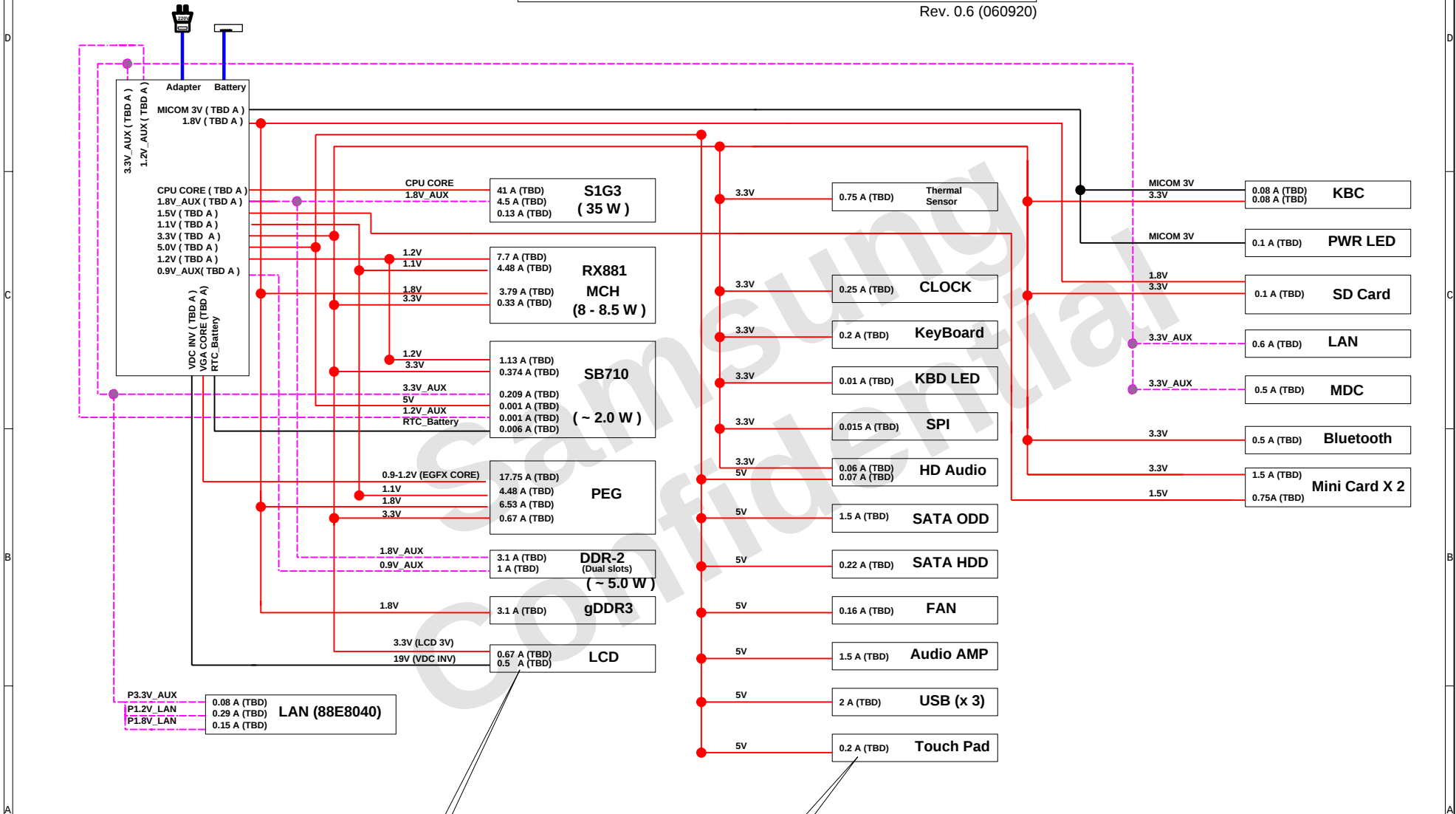
S0

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CHECK	GUO LEI	DEV. STEP	ADV	POWER DIAGRAM		
APPROVAL	BC LEE	REV	0.1			
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POWER RAILS ANALYSIS

Rev. 0.6 (060920)

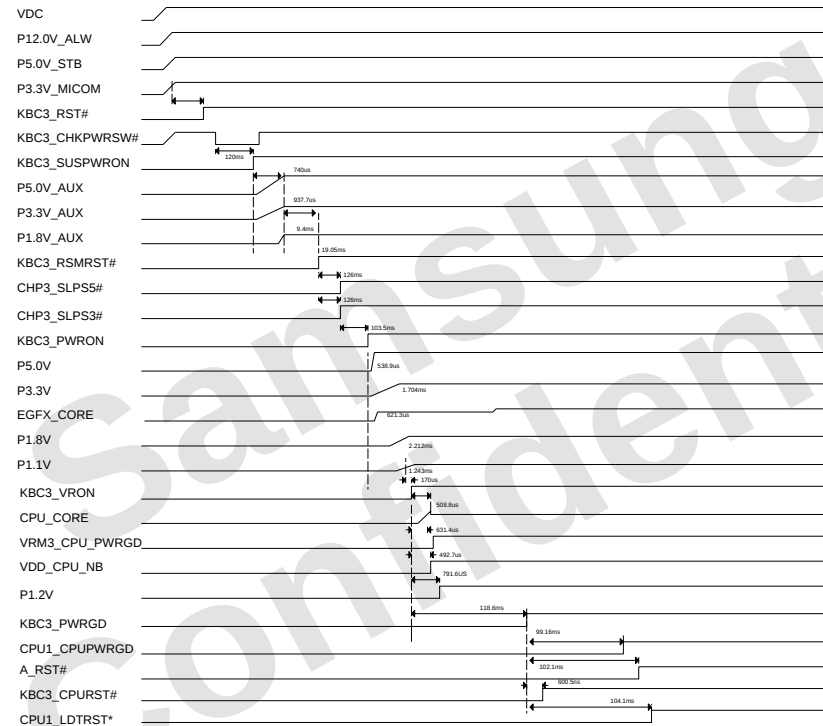


Value by Datasheet/Application notes (Value by measurement)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	POWER RAILS ANALYSIS	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT				
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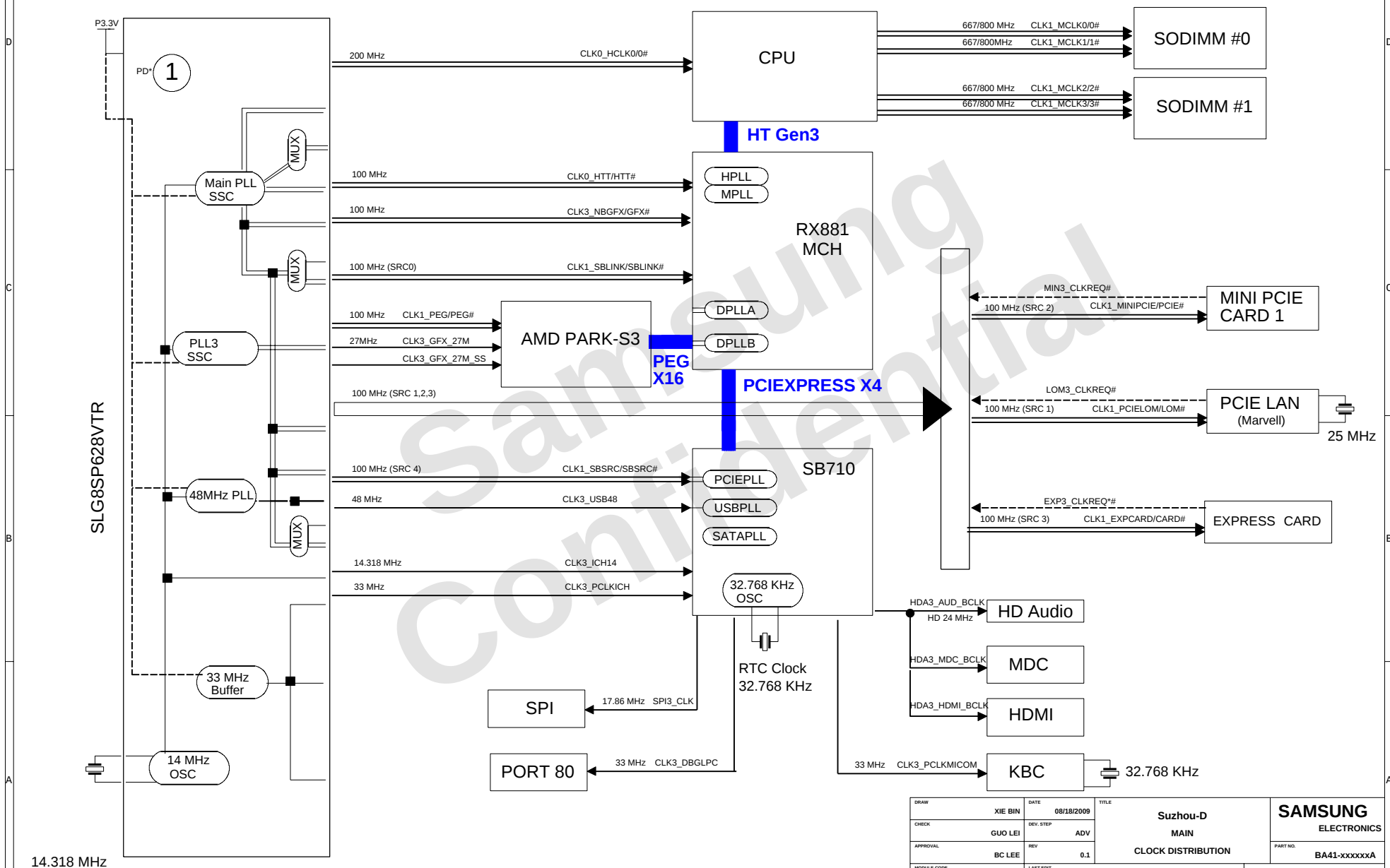
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Timing Diagram, Power ON Rev..1.0 2009-08-27



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CHECK	GUO LEI	DEV. STEP	ADV	MAIN		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	TIMING DIAGRAM		PART NO.
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM			BA41-xxxxxxA
				PAGE	6	OF 58

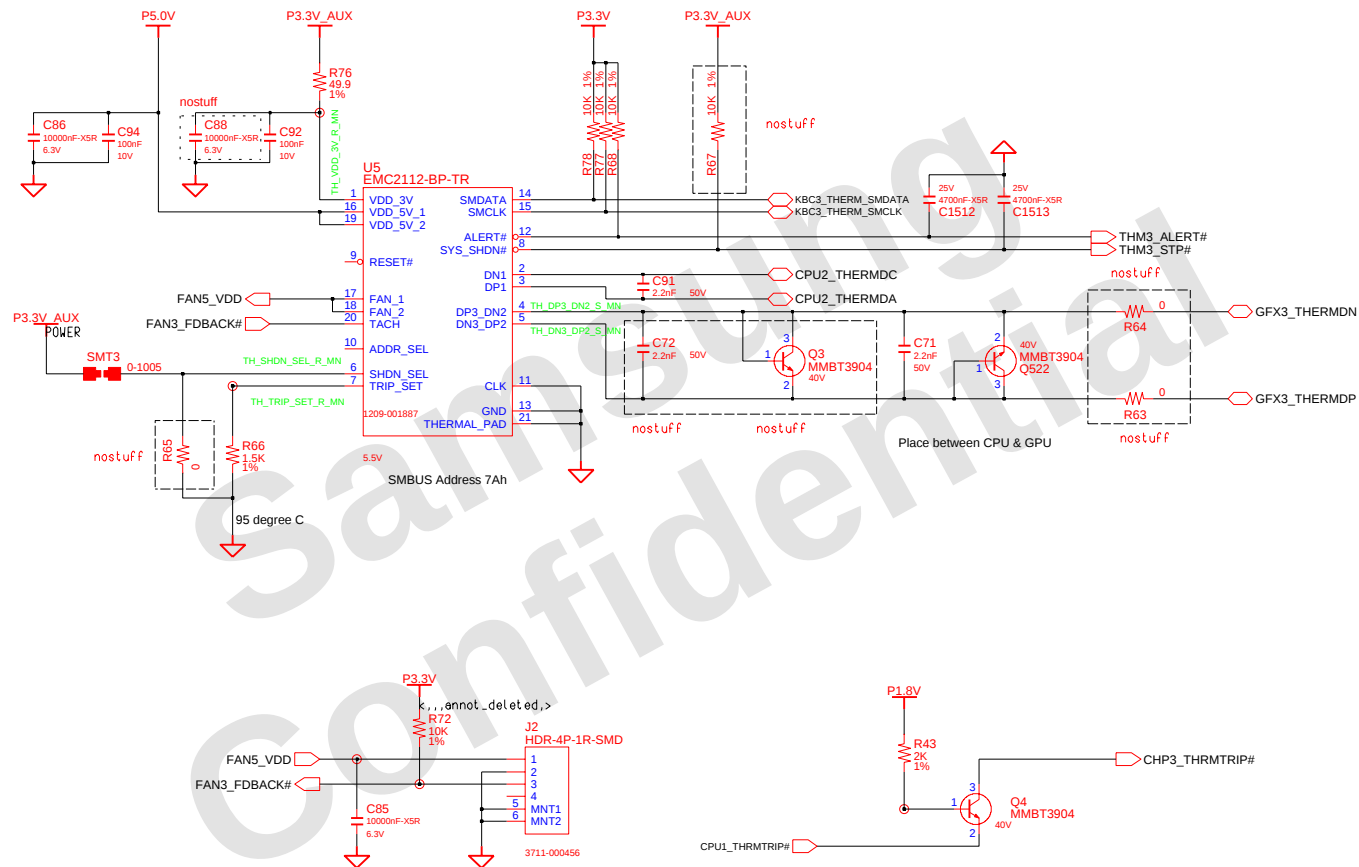
CLOCK DISTRIBUTION



14.318 MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MAIN	MAIN	ELECTRONICS
APPROVAL	BC LEE	REV	0.1	CLOCK DISTRIBUTION	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	7	OF 58

THERMAL SENSOR & FAN CONTROL



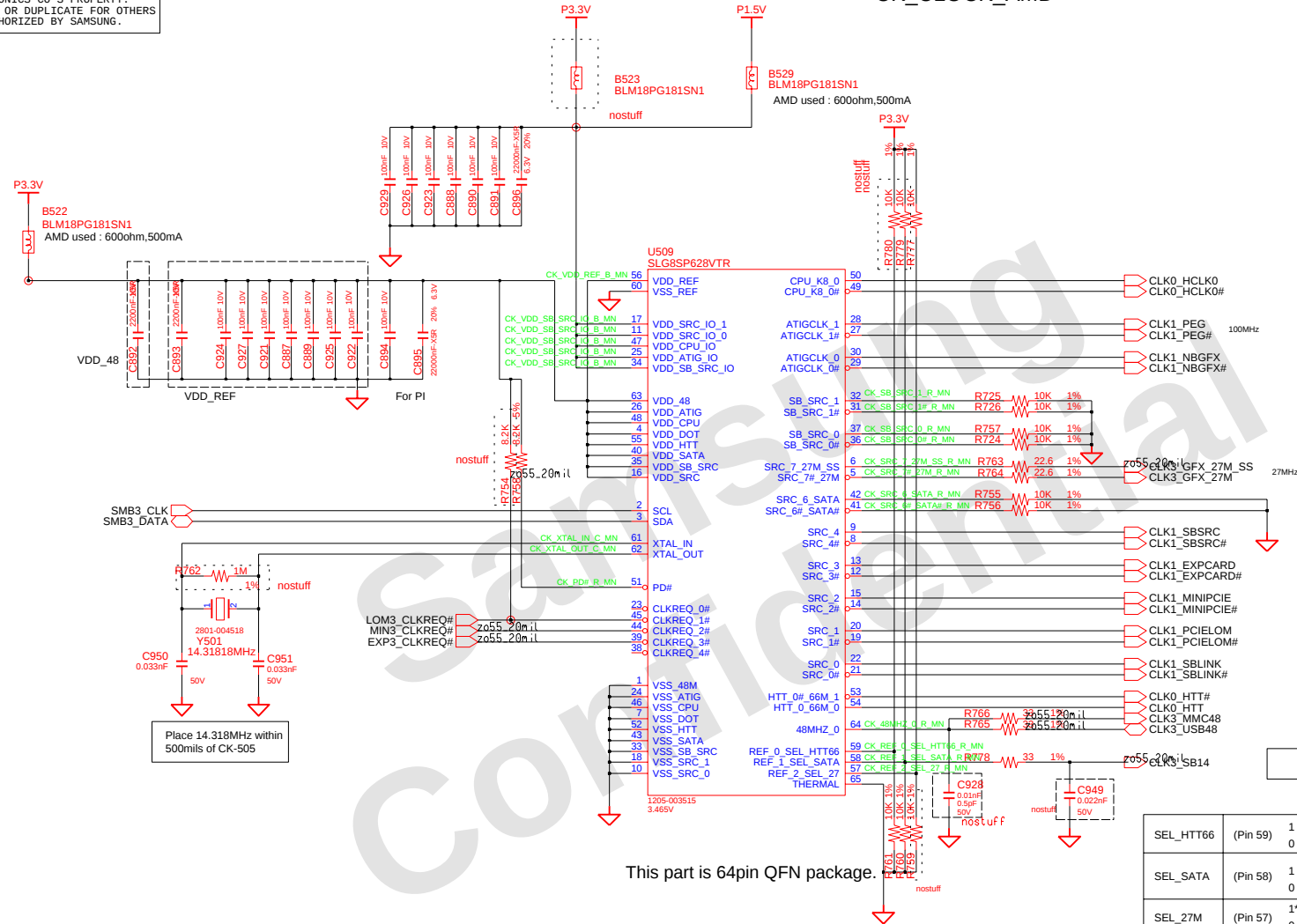
Line Width = 20 mil

SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		THERMAL SENSOR	
APPROVAL	BC LEE	REV	0.1		EMC2112	
MODULE CODE		LAST EDIT				PART NO. BA41-xxxxxxA
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CK_CLOCK_AMD



This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

SEL_HTT66	(Pin 59)	1 0 *	66MHz 3.3V single HTT clock 100MHz differential clock
SEL_SATA	(Pin 58)	1 0 *	SRC6 diff. clock 100MHz spreading diff. clock
SEL_27M	(Pin 57)	1* 0	27MHz/27MHz_SS graphics clock SRC7 diff. clock

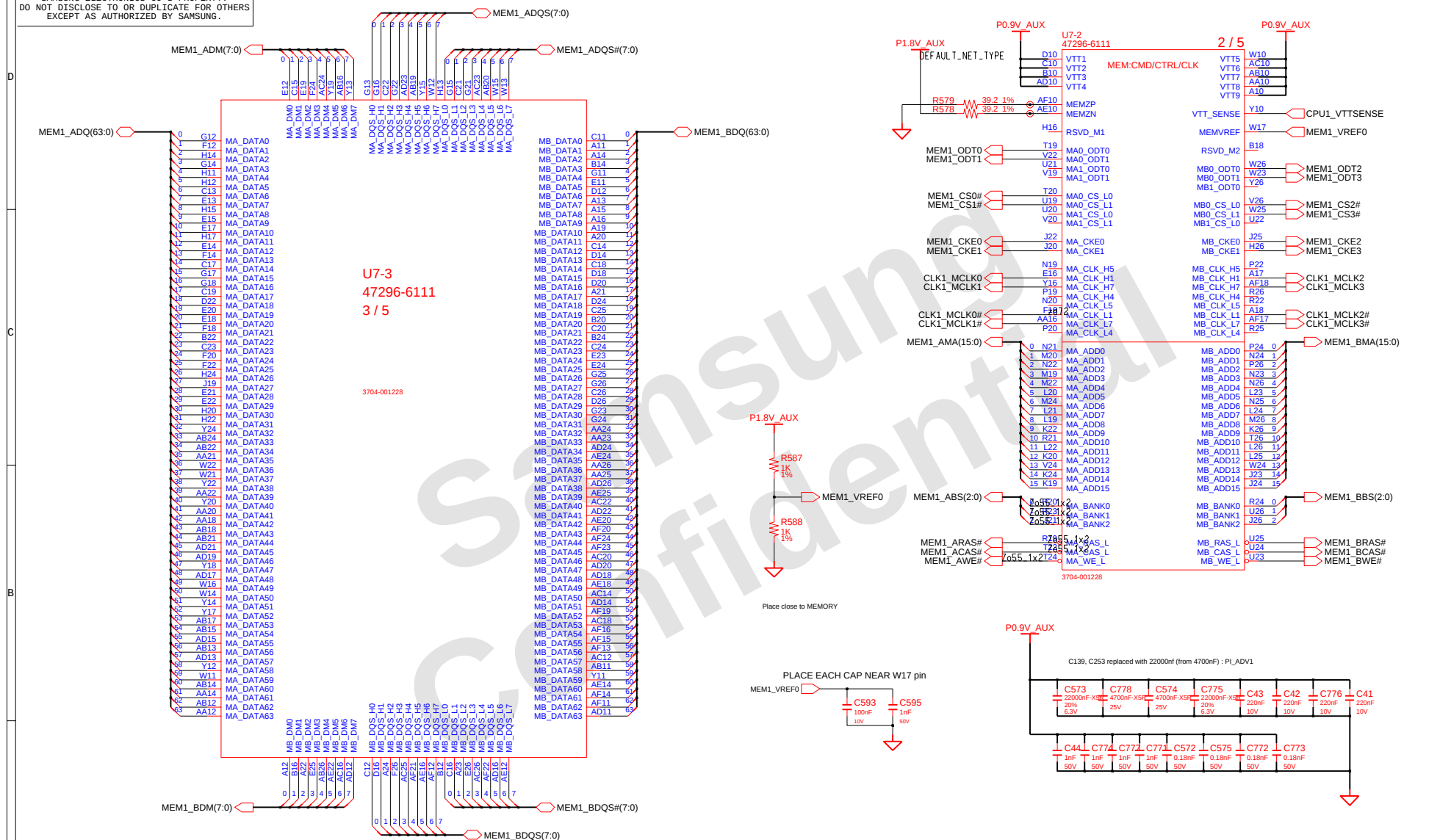
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CHECK		GUO LEI		DEV. STEP		ADV		Main_Clock_Circuit							
APPROVAL		BC LEE		REV		0.1		CK for AMD CPU		PART NO.		BA41-xxxxxxA			
MODULE CODE				LAST EDIT				July 15, 2009 19:25:13 PM				PAGE	9	OF	58

CPU_Caspian



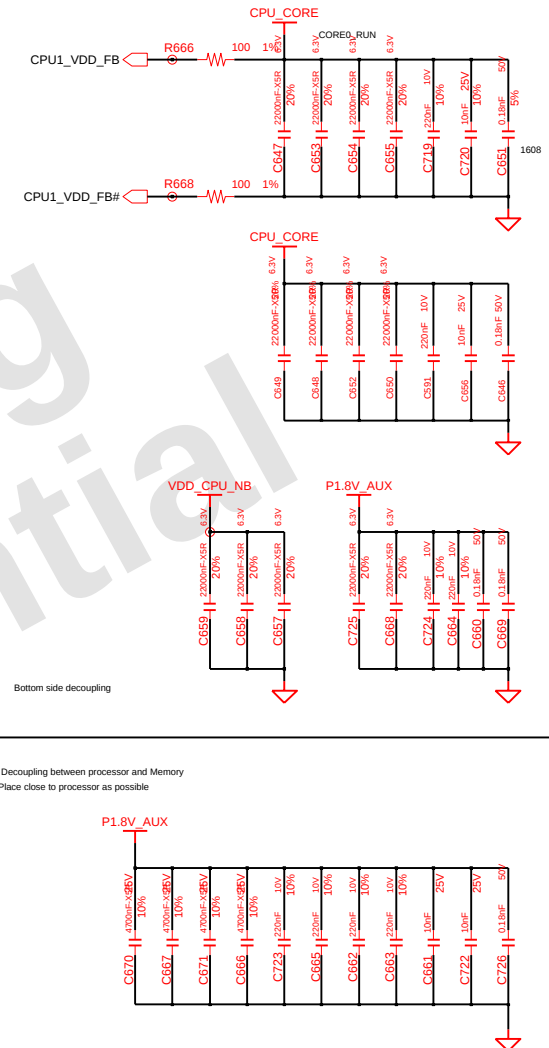
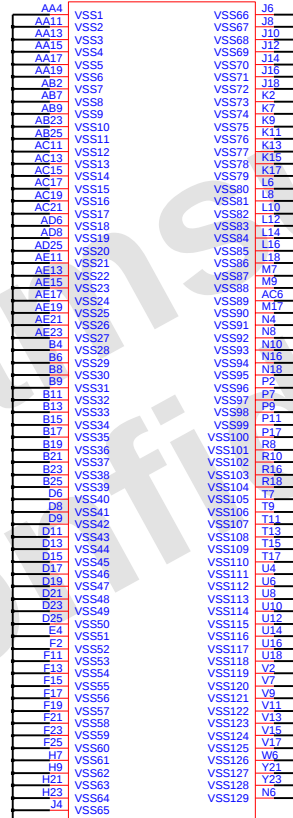
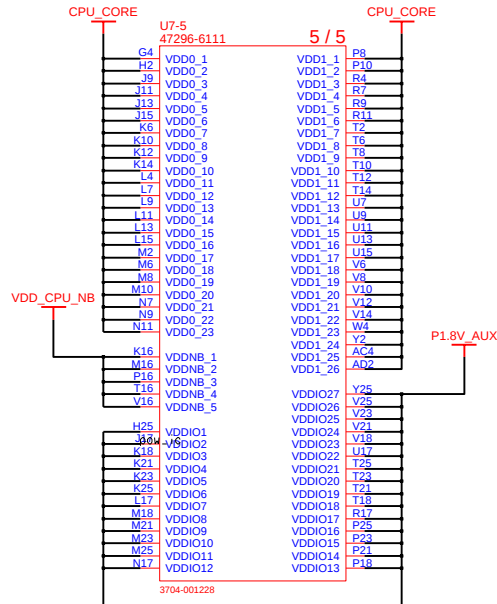
COM-22C-015(1996.6.5) REV. 3

CPU_Caspian



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D Caspian CPU S1G3 CPU (2/3)	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP	ADV				
APPROVAL	REV	0.1					
MODULE CODE	BC LEE	LAST EDIT	July 15, 2009 19:25:13 PM				PAGE
						PART NO.	BA41-XXXXXXA

CPU_Caspian

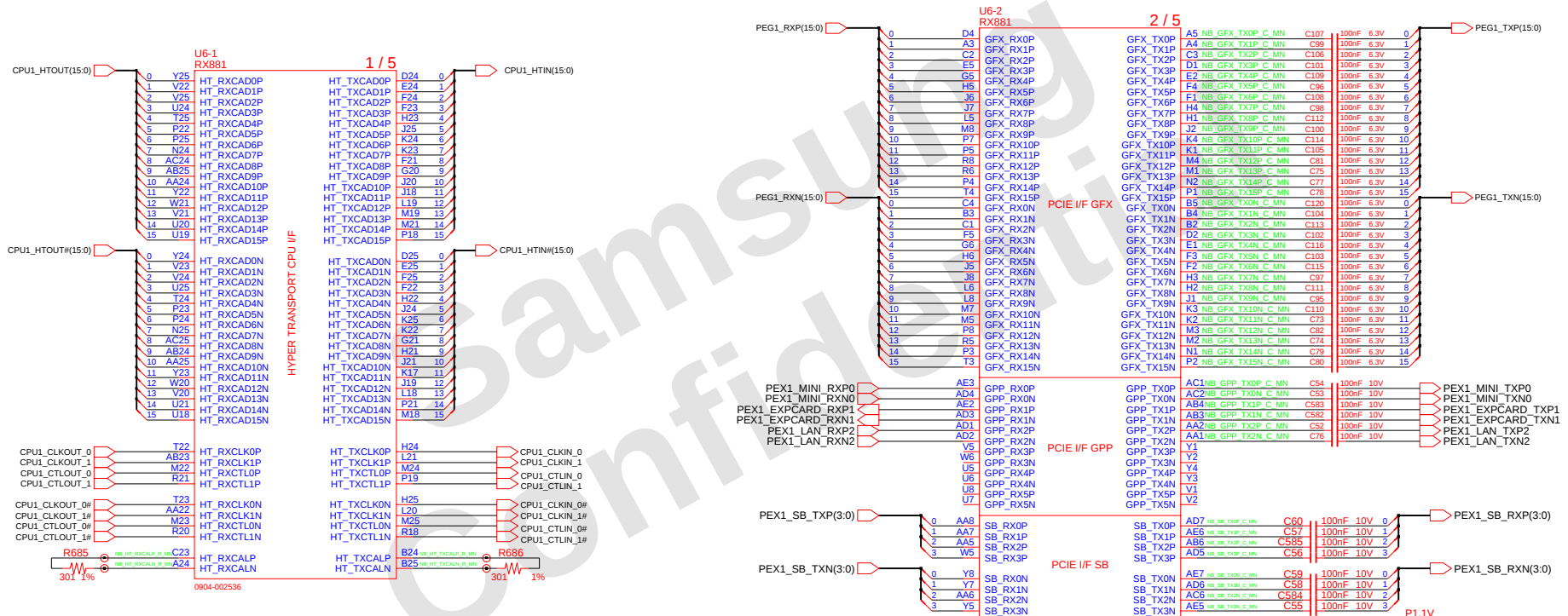


Bottom side decoupling

Decoupling between processor and Memory
Place close to processor as possible

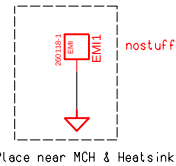
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CHECK	GUO LEI	DEV. STEP	ADV	Caspian CPU	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	S1G3 CPU (3/3)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	12 OF 58

NB_RX881_AMD



* Hyper Transport Calibration resistors

RS780M / RX781 : 301 ohm
RX780 / RD780 : 1.21K ohm (for S3 issue in D/T chipset)

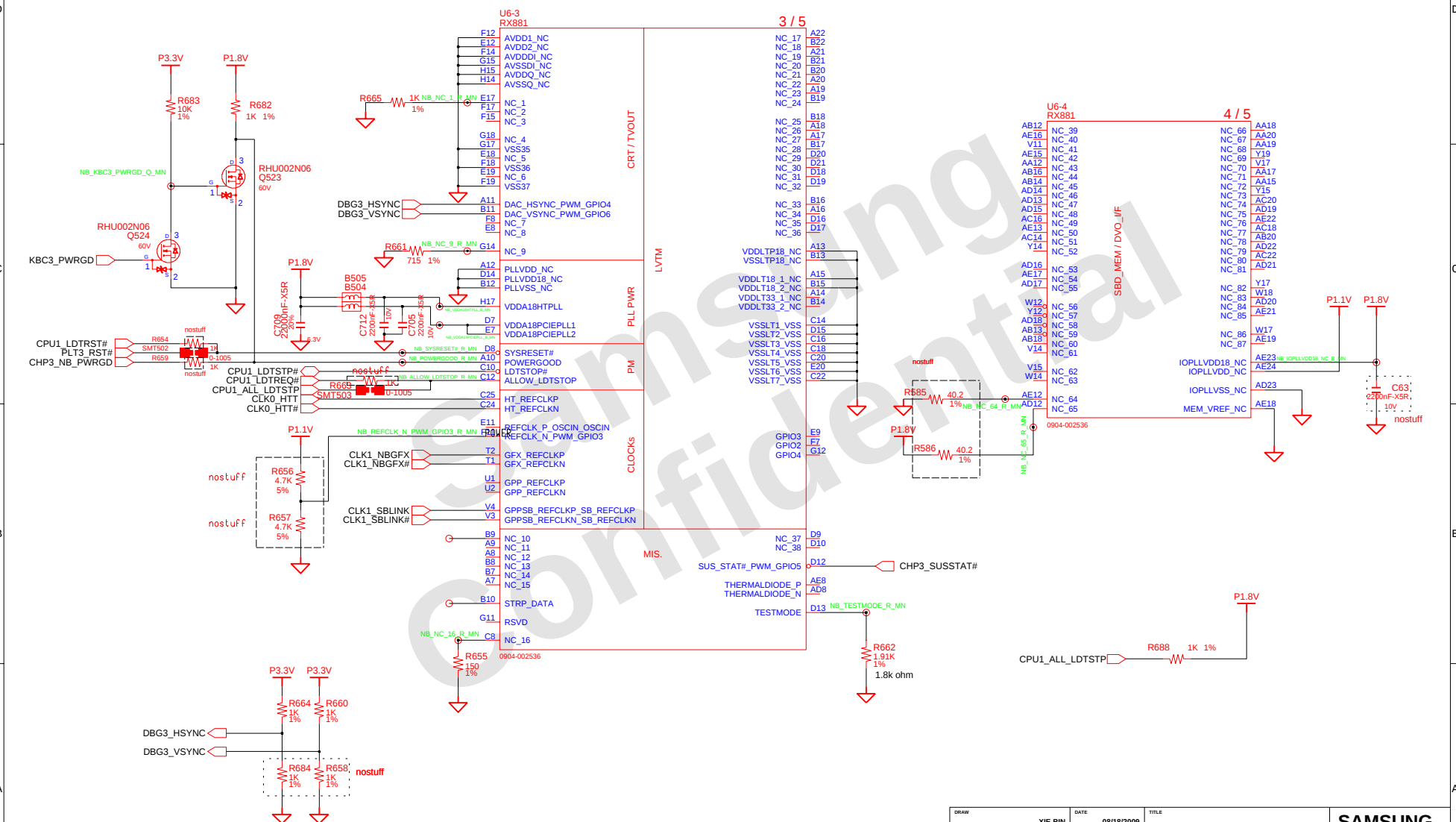


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D
CHECK	GUO LEI	DEV. STEP	ADV		MCH
APPROVAL	BC LEE	REV	0.1		RX881 (1/3)
MODULE CODE		LAST EDIT			

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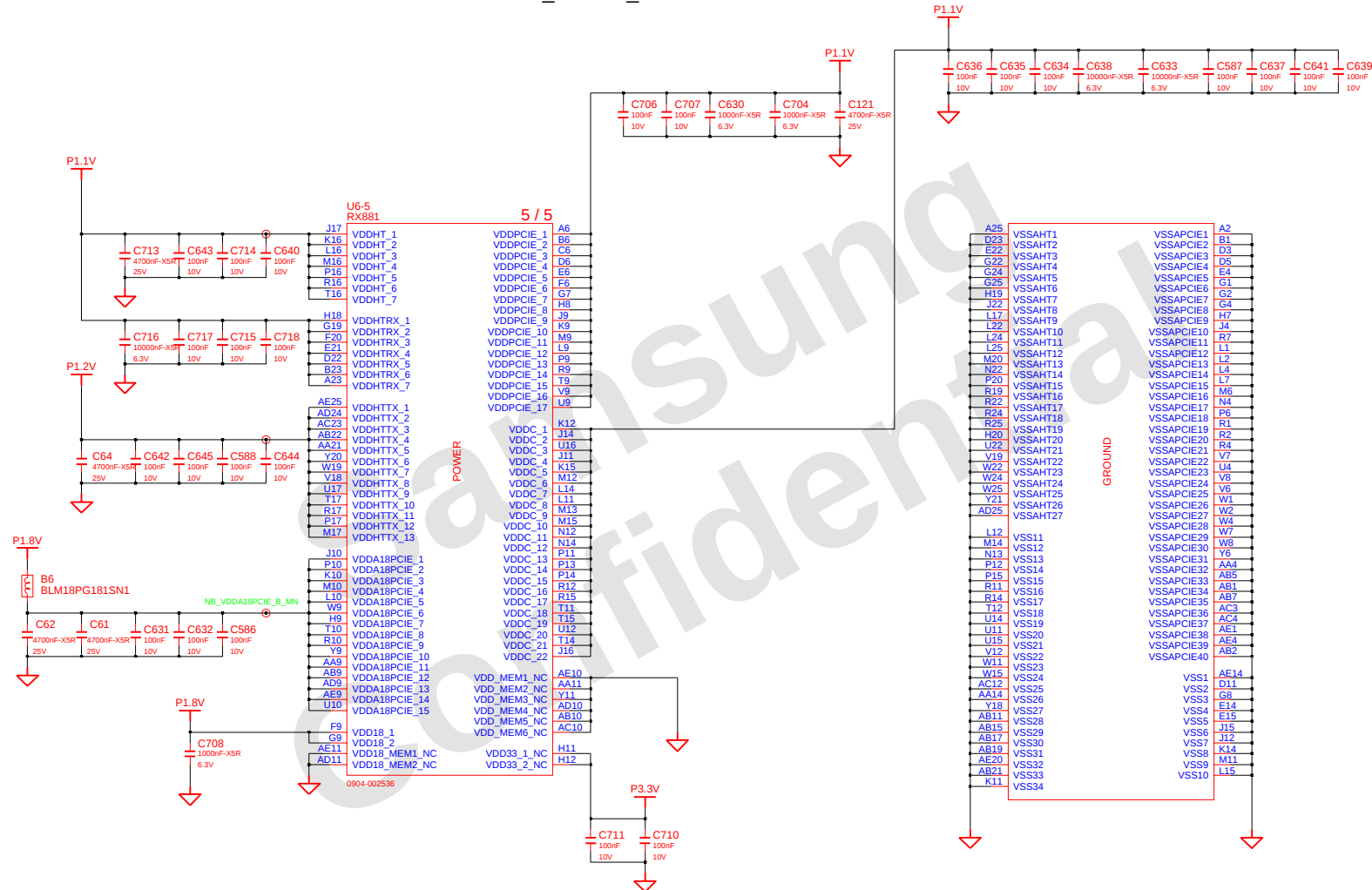
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NB_RX881_AMD

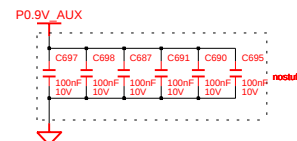


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D MCH RX881 (2/3)	SAMSUNG		
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MODULE CODE	LAST EDIT					July 15, 2009 19:25:13 PM	PAGE	14 OF 58

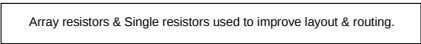
NB_RX881_AMD



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MCH	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	RX881 (3/3)	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	15 OF 58

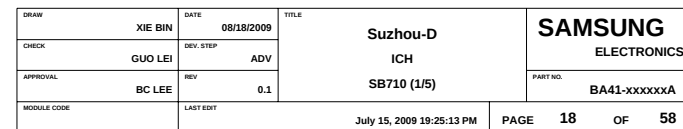


COM-22C-015 (1996.6.5) REV. 3



COM-22C-015(1996.6.5) REV. 3

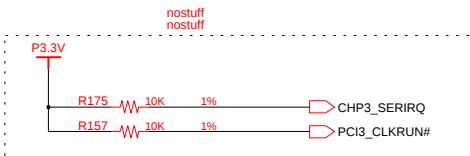
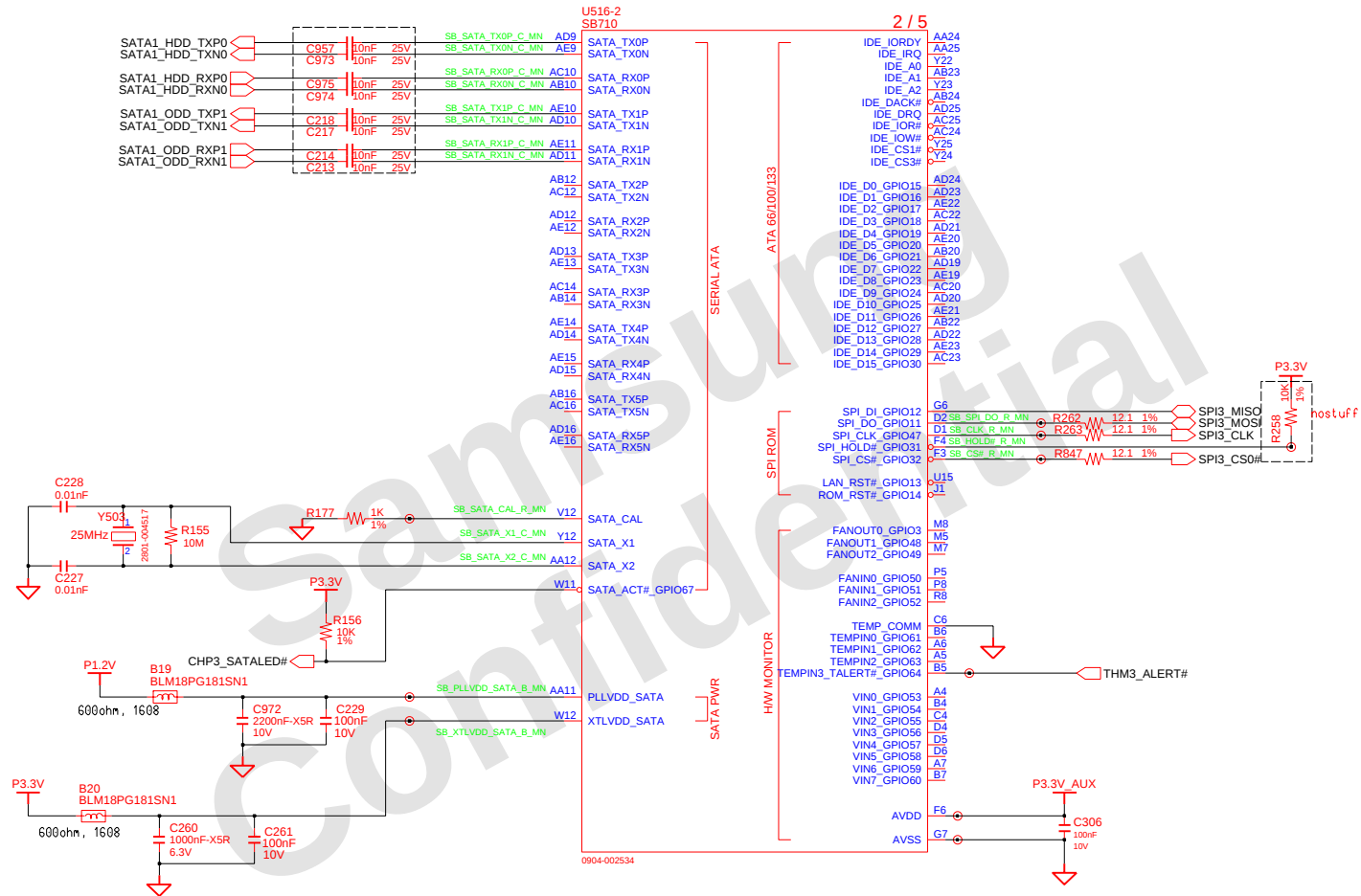
SB 710 AMD



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SB_710_AMD

Route to connector side closely



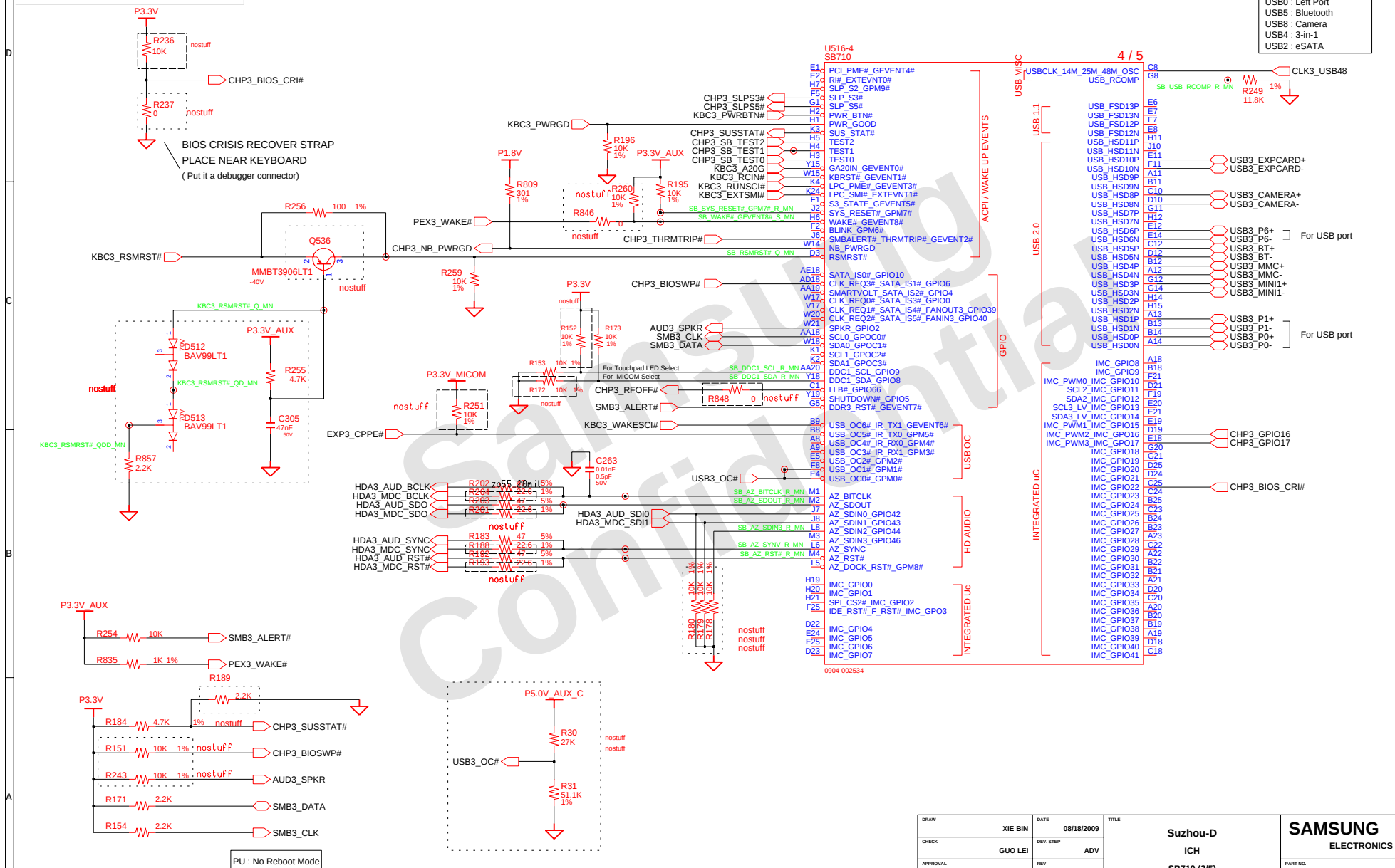
LPC option ; These are used with LPC

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D ICH SB710 (2/5)		SAMSUNG ELECTRONICS				
CHECK	GUO LEI	DEV. STEP	ADV							
APPROVAL	BC LEE	REV	0.1							
				PART NO.		BA41-xxxxxxA				
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM		PAGE	19	OF	58

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SB 710 AMD

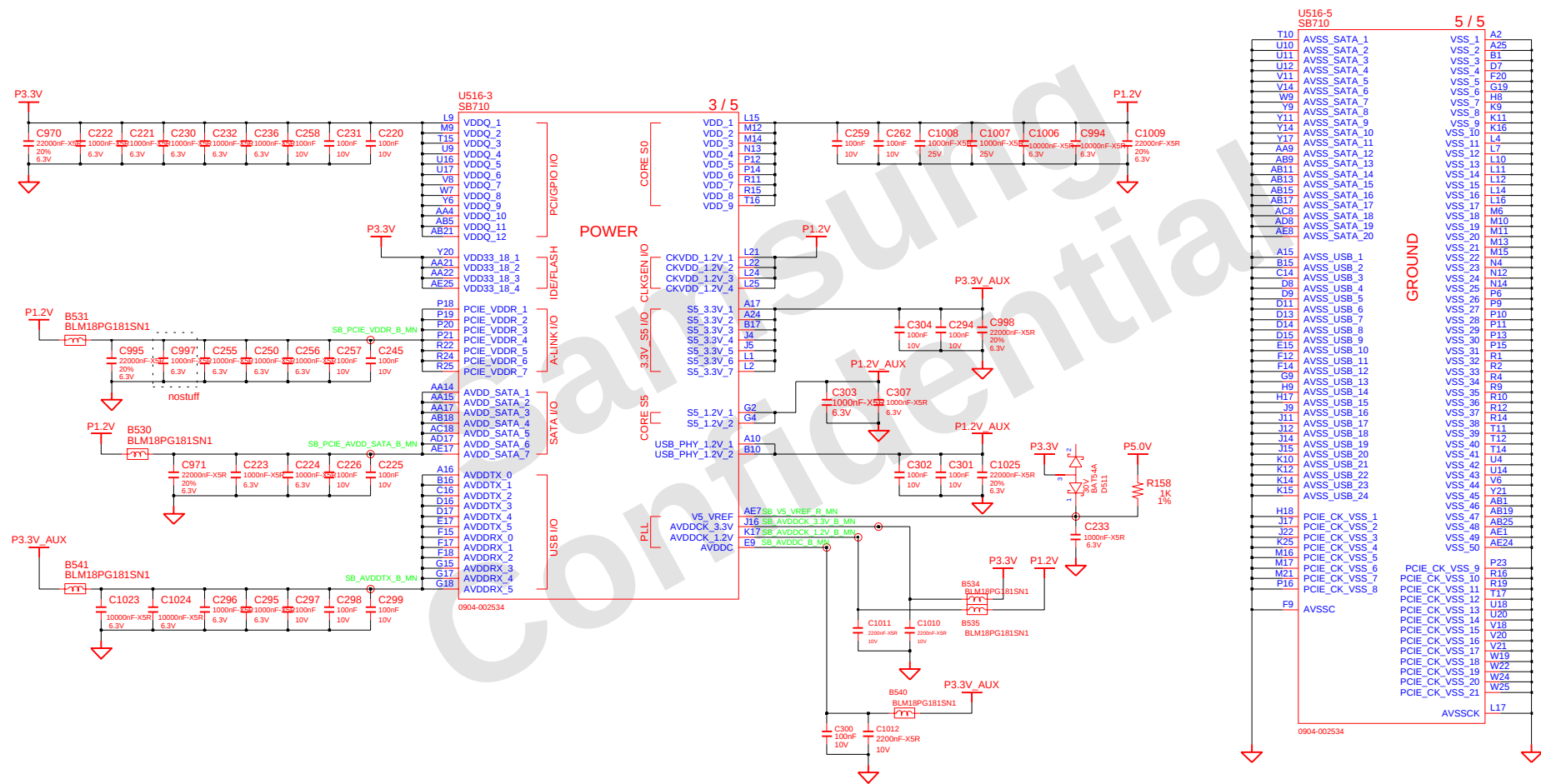
USB1, 6 : Right Port
USB0 : Left Port
USB5 : Bluetooth
USB8 : Camera
USB4 : 3-in-1
USB2 : eSATA



DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D ICH SB710 (3/5)	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV		
APPROVAL	BC LEE	REV	0.1		
MODULE CODE					
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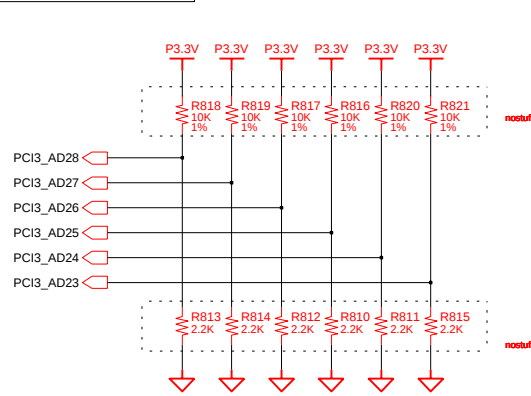
SB_710_AMD



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MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE 21 OF 58

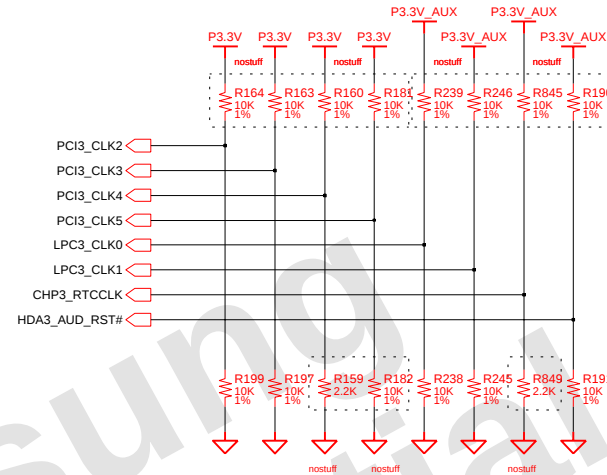
Strap

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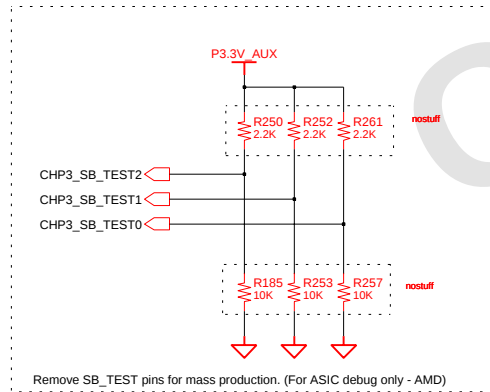


DEBUG STRAPS

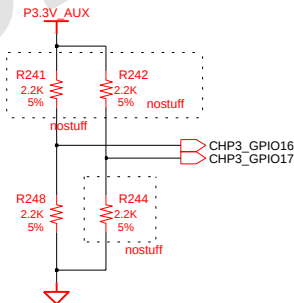
	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT

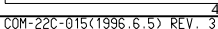


Remove SB_TEST pins for mass production. (For ASIC debug only - AMD)



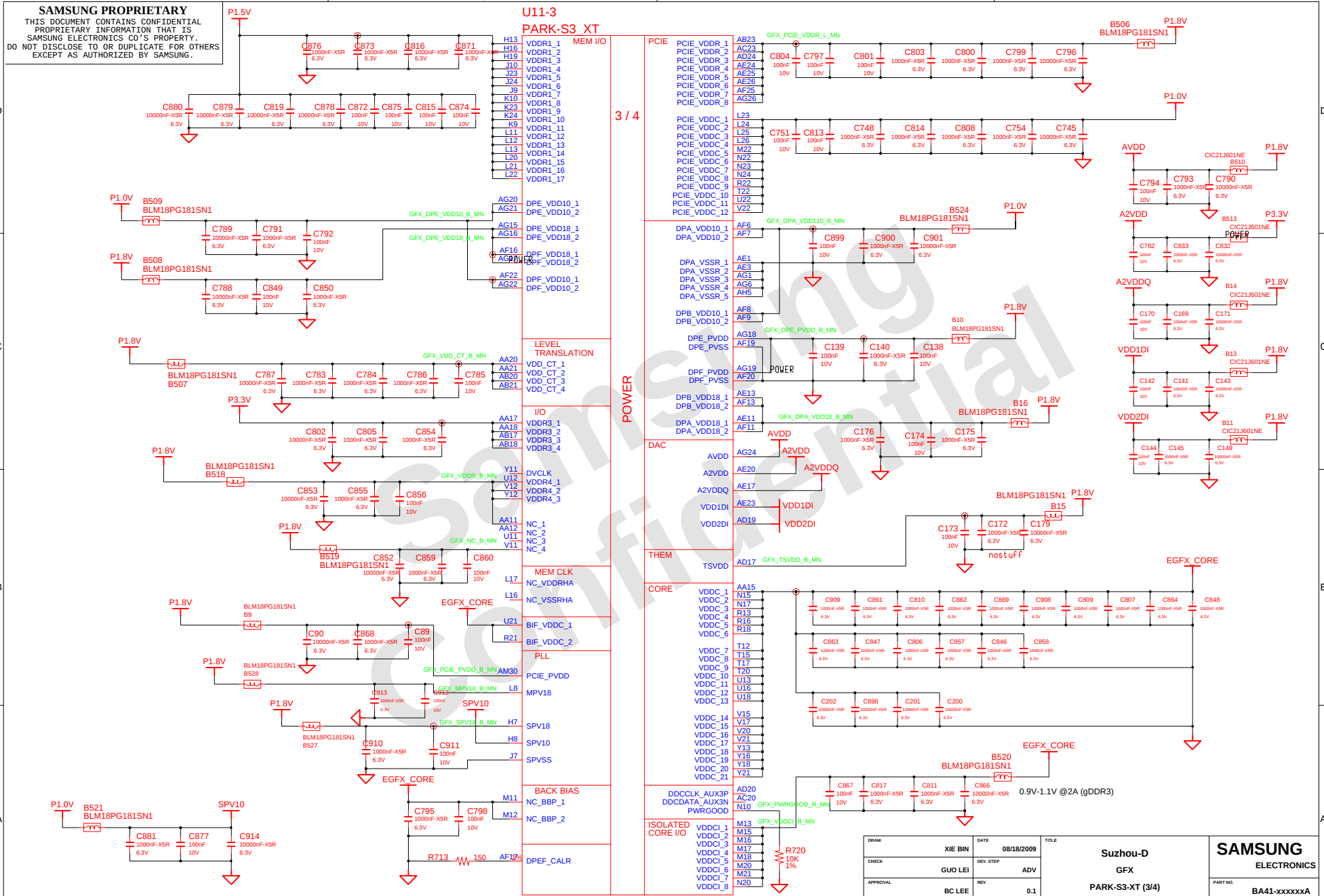
GPI017	GPI016
ROM TYPE	
NC, NC = RSVD	
NC, L = SPI ROM	
L, NC = LPC ROM	
L, L = FWH ROM	

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	ICH		
APPROVAL	BC LEE	REV	0.1	SB710 Strap(5/5)	PART NO. BA41-xxxxxxA	
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 22 OF 58	

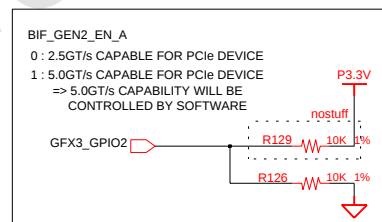
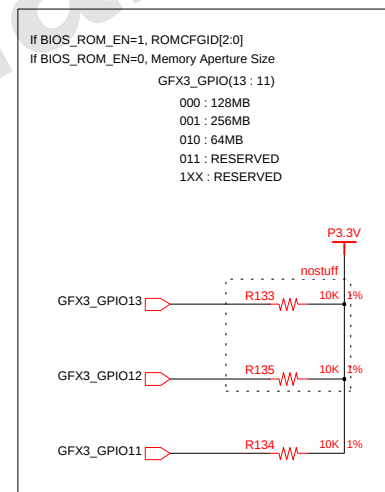
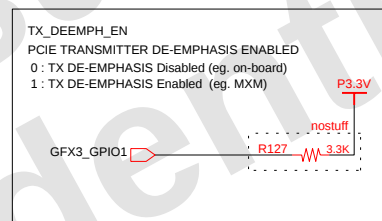
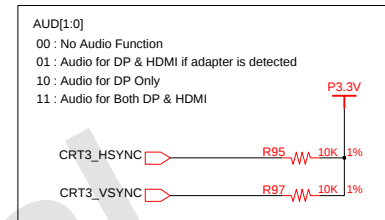
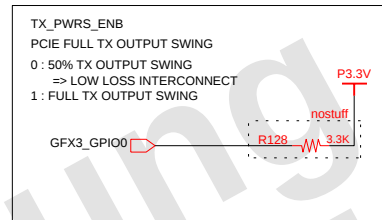
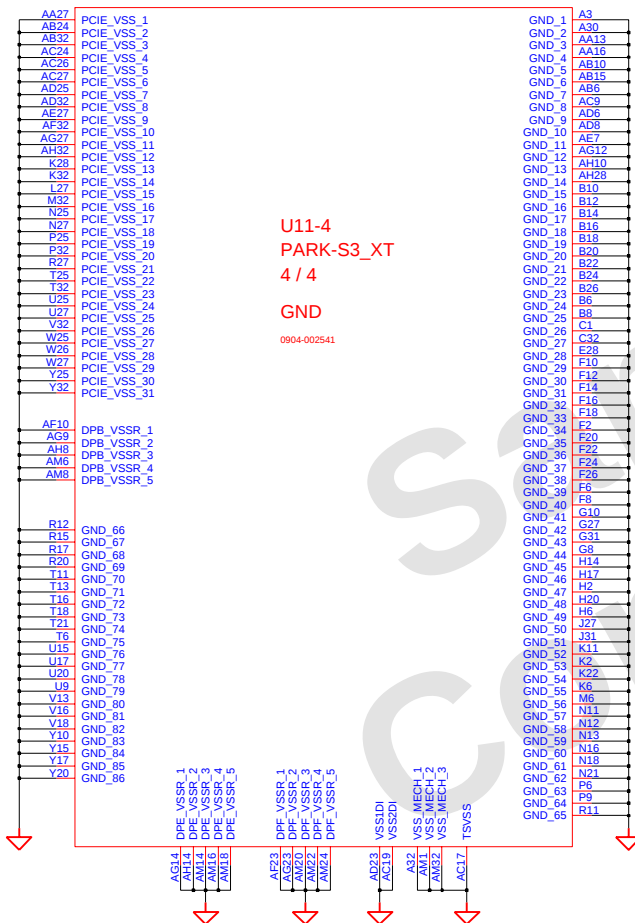


D:/Users/mentor/Suzhou-D/Suzhou-D_adv1_0826

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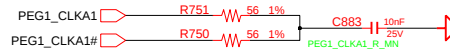
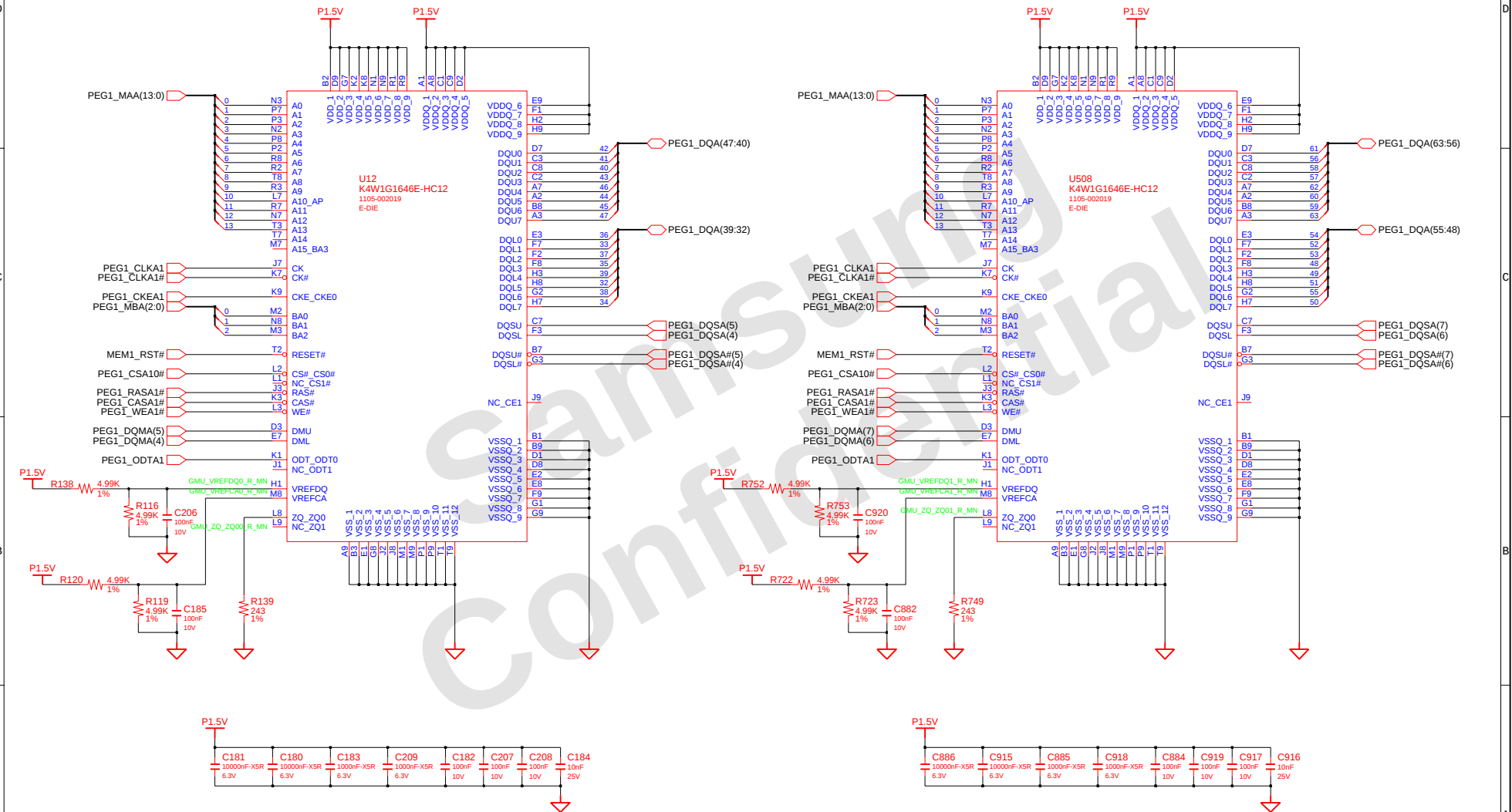


PARK Straps



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	GFX	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	PARK-S3-XT (4/4)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	27	OF 58

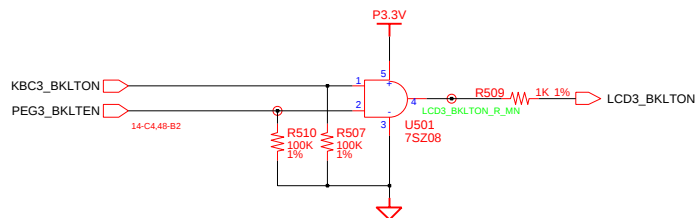
A-channel Upper Data



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_MEMORY		
APPROVAL	BC LEE	REV	0.1	gDDR3 (2/2)		
MODULE CODE		LAST EDIT				
July 15, 2009 19:25:13 PM						PAGE 29 OF 58

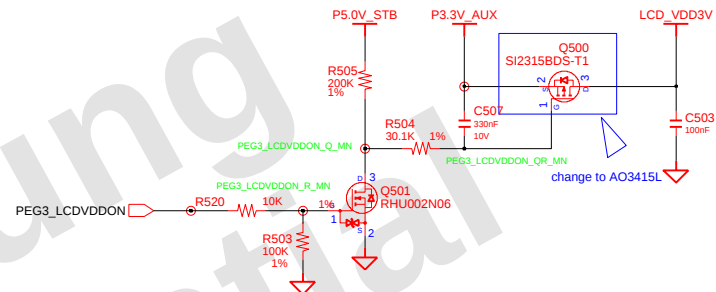
LVDS

Backlight On

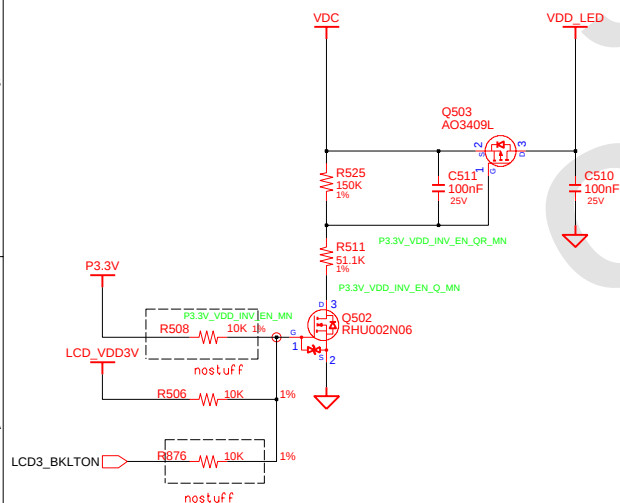


LCD Power

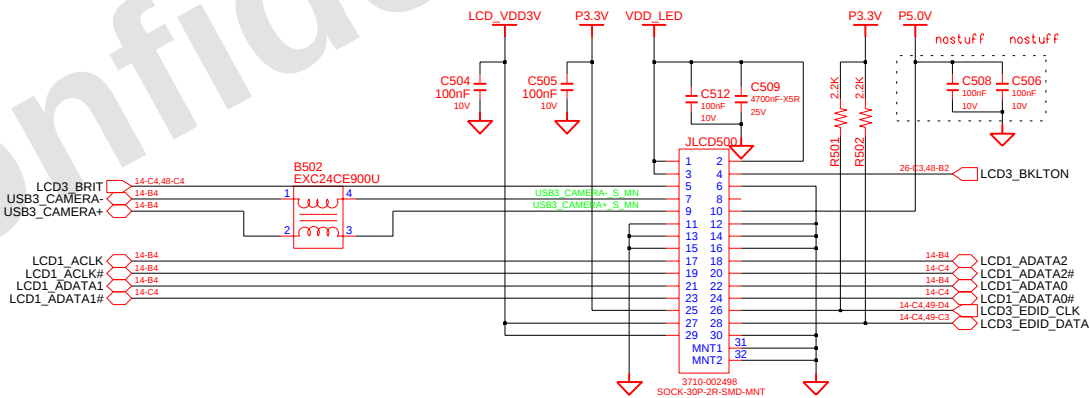
EBL Purpose



Converter Power

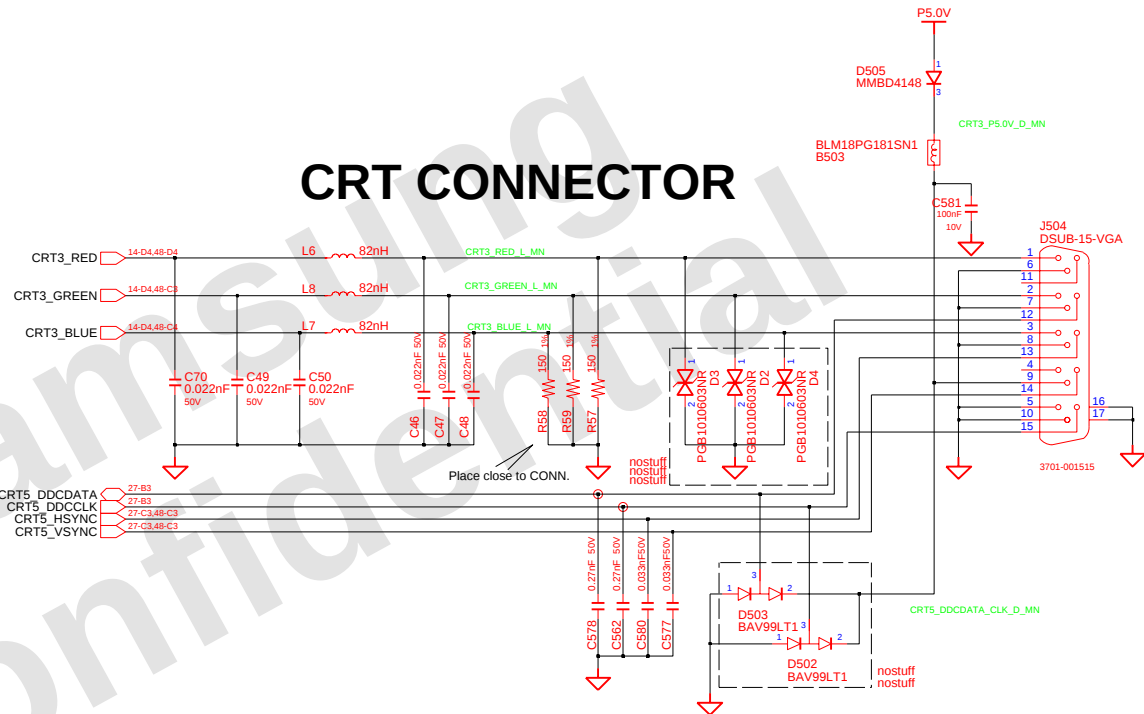
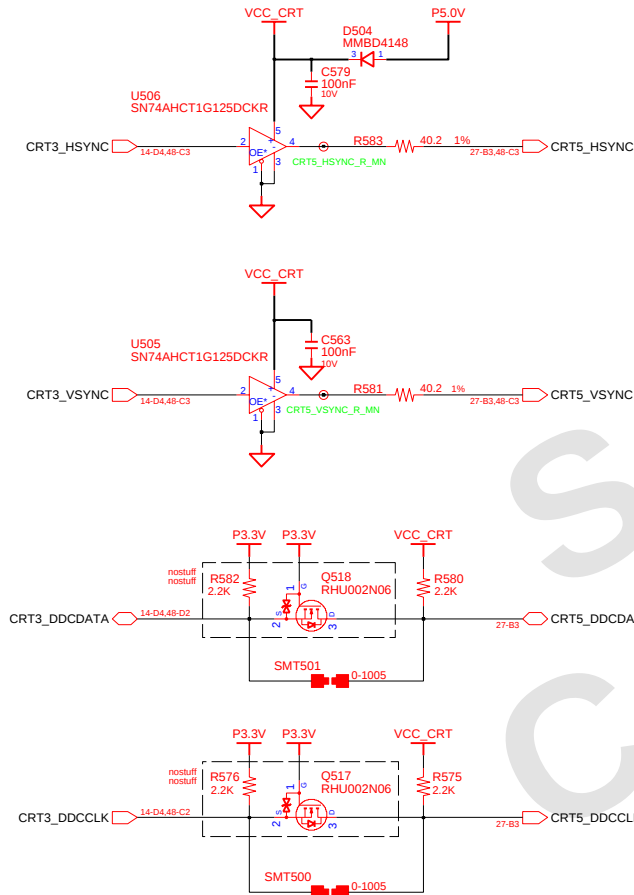


Camera + LCD Connector



CRT

CRT CONNECTOR



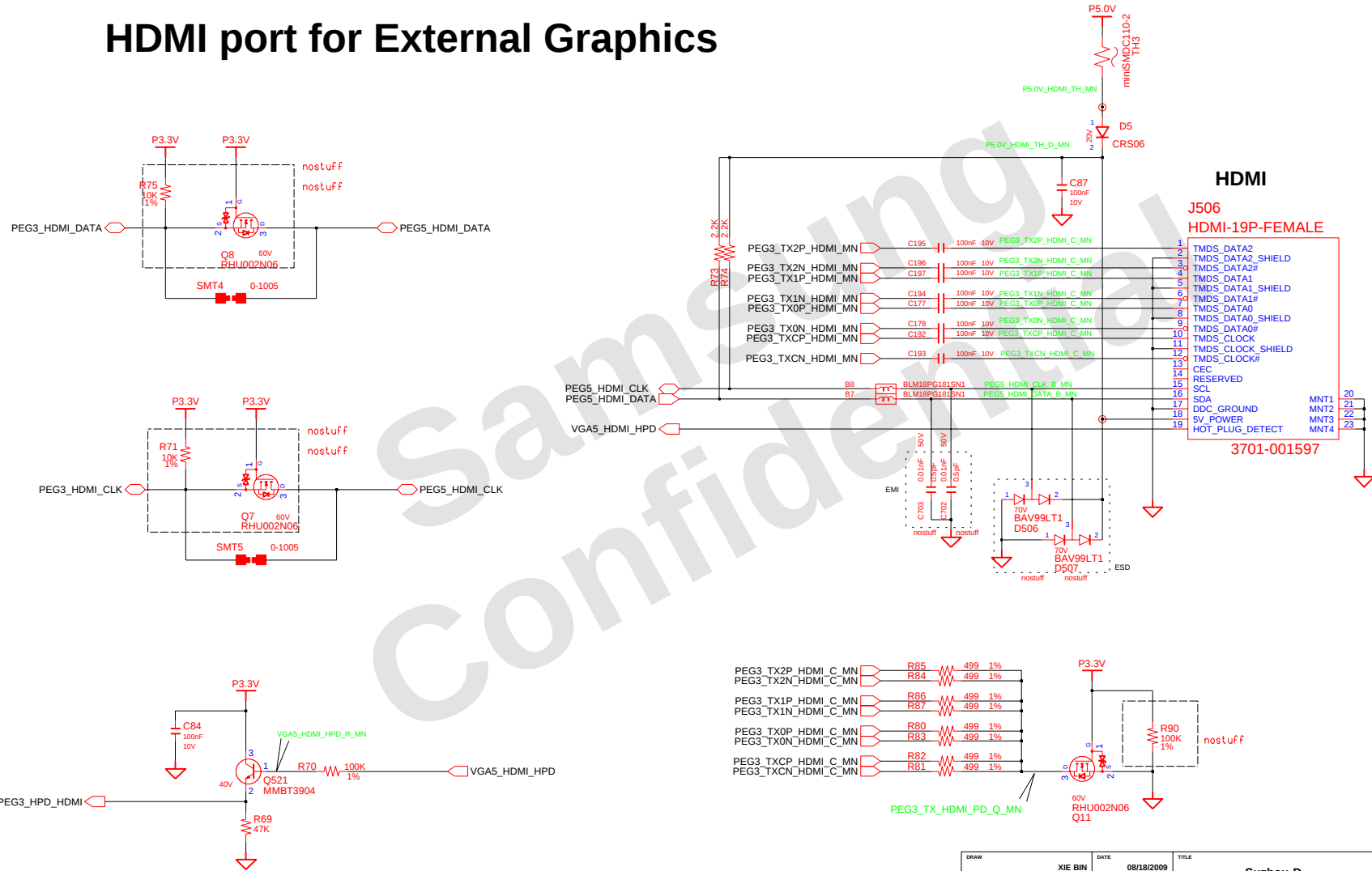
Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV			ELECTRONICS
APPROVAL	BC LEE	REV	0.1	GRAPHICS_IF (2/2)		PART NO.
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM			BA41-xxxxxA
					PAGE	31 OF 58

HDMI

HDMI port for External Graphics

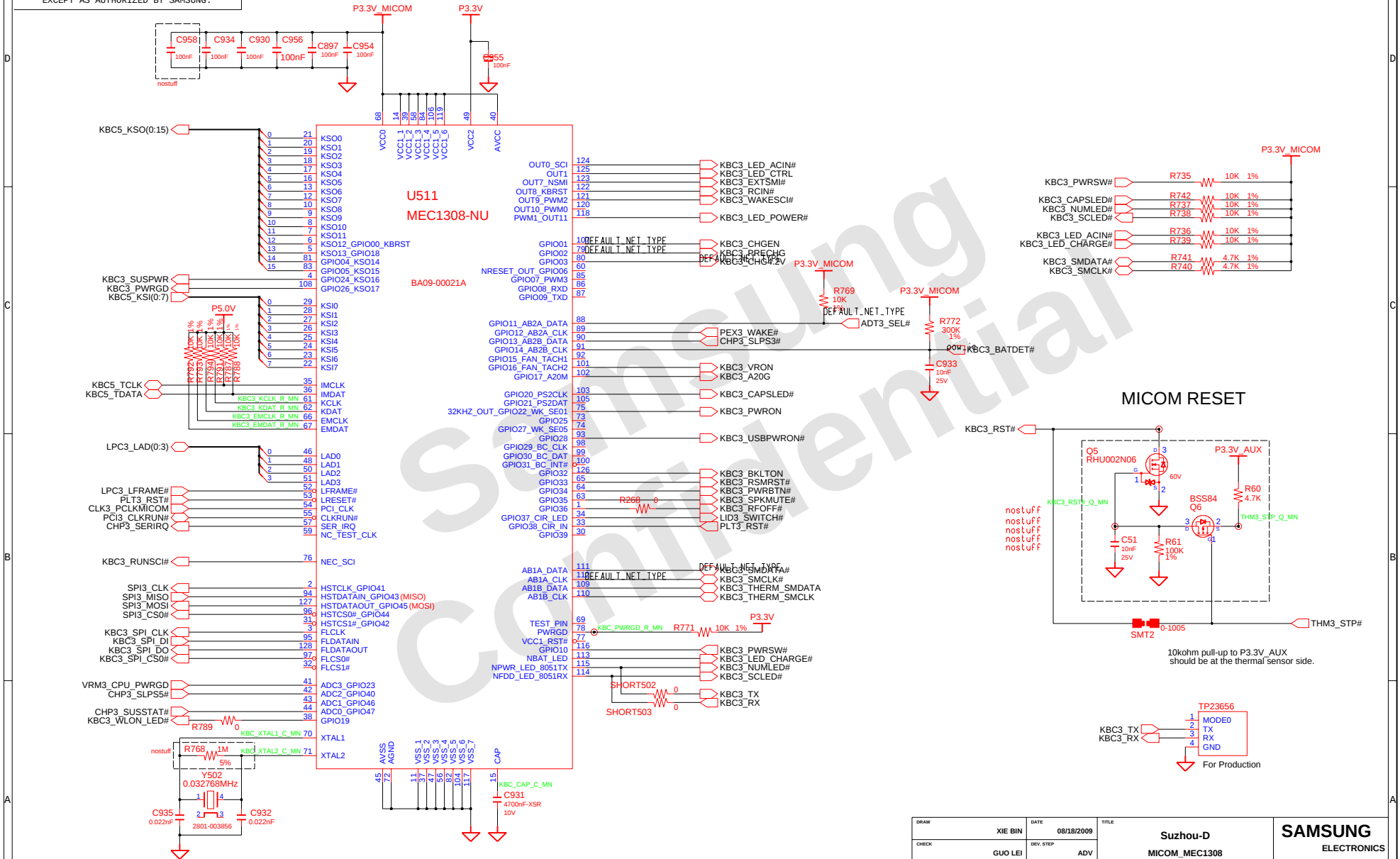
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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	GRAPHICS_IF	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	HDMI	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT				
				July 15, 2009 19:25:13 PM	PAGE	32 OF 58

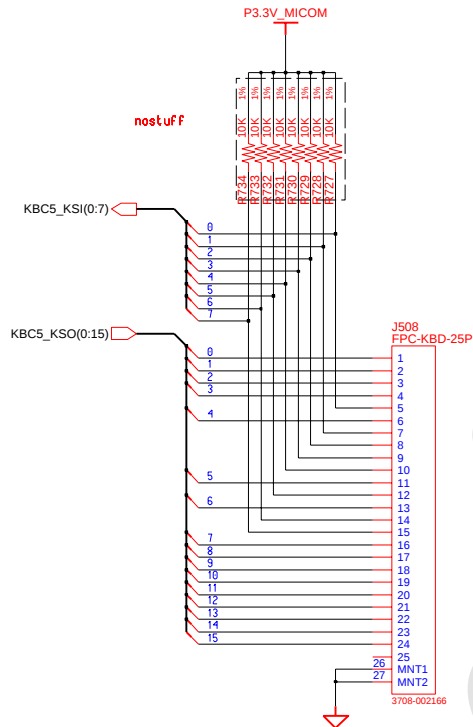
MICOM_MEC1308-NU

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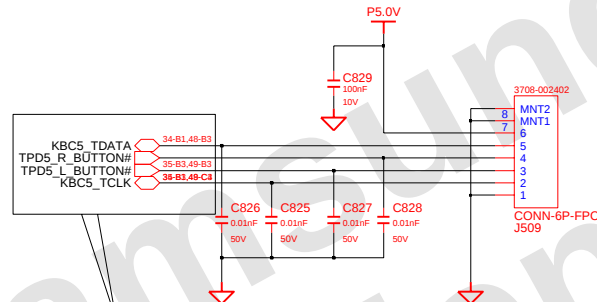


Micom Glue Logic

KEYBOARD

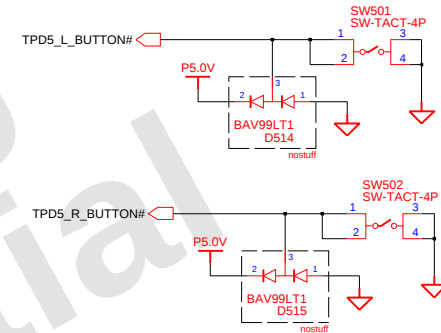


TOUCHPAD

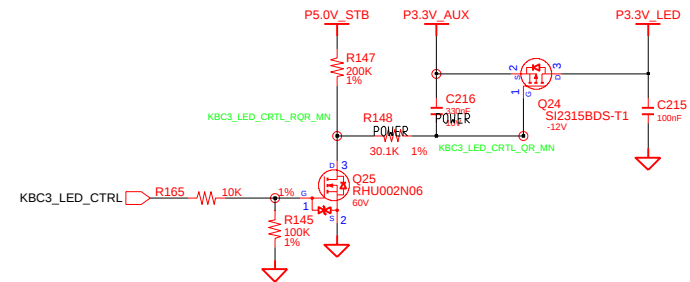


Confirm that there are PU on Touch PAD module side or micom.

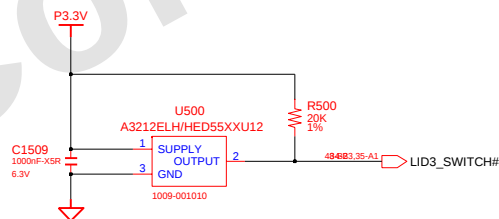
TOUCHPAD BUTTON



TOUCHPAD LED POWER



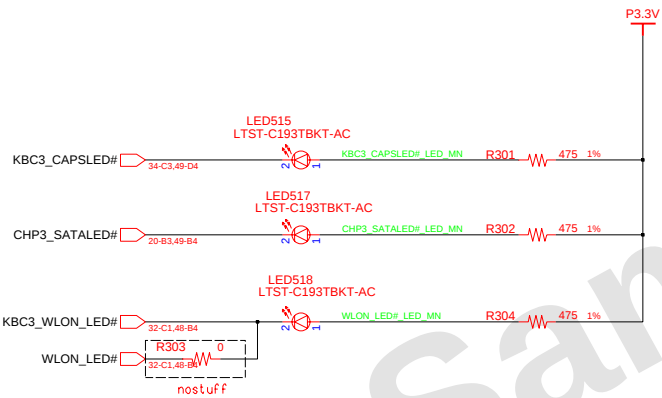
LID SWITCH



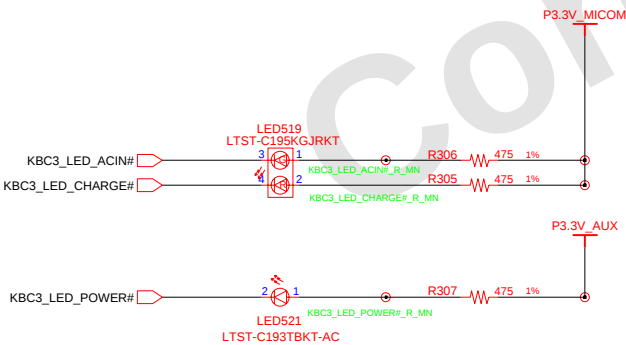
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	MICOM_GLUE		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	34	OF 58

LEDs

FUNCTION KEY LED

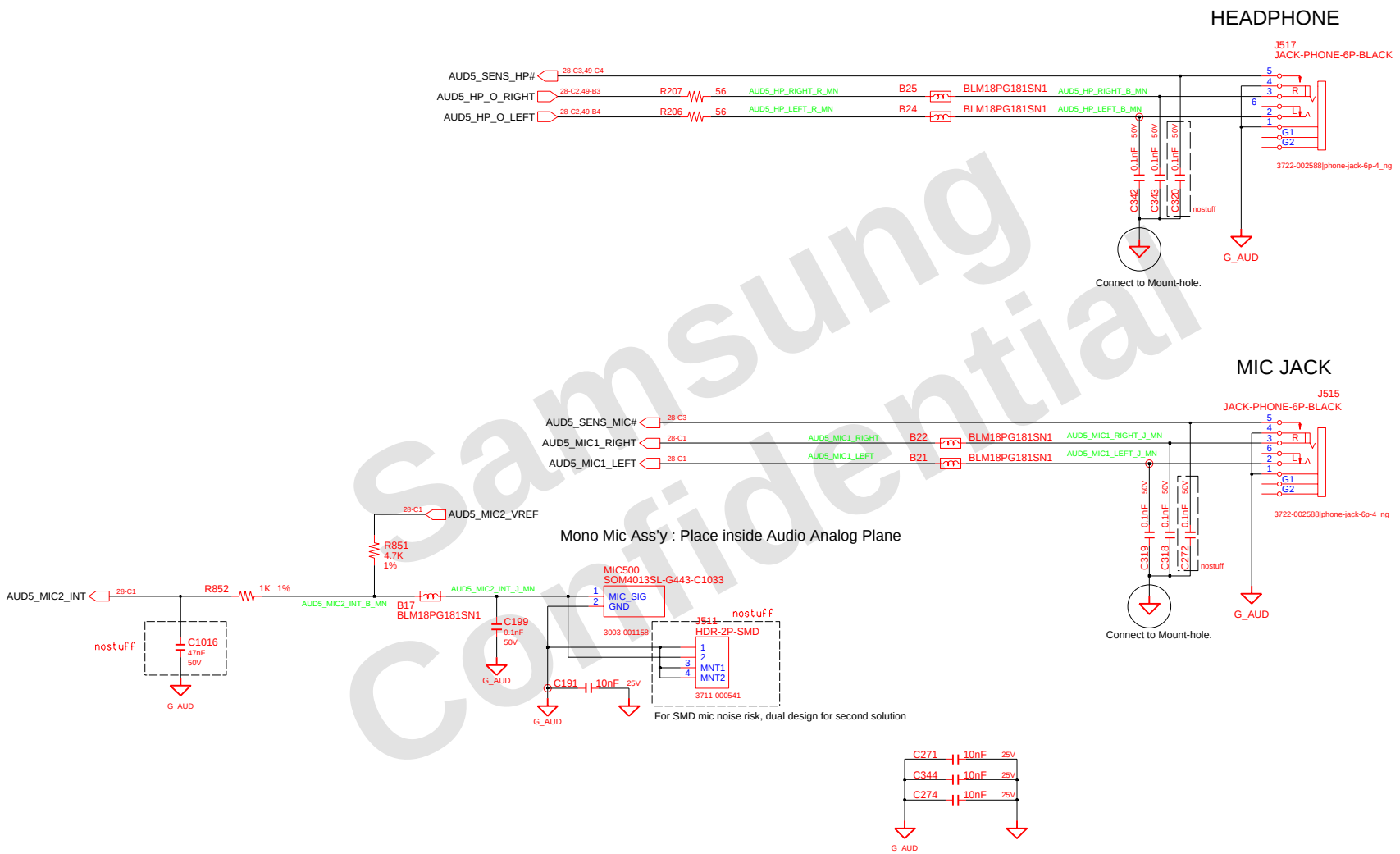


ADAPTERIN/CHARGING LED



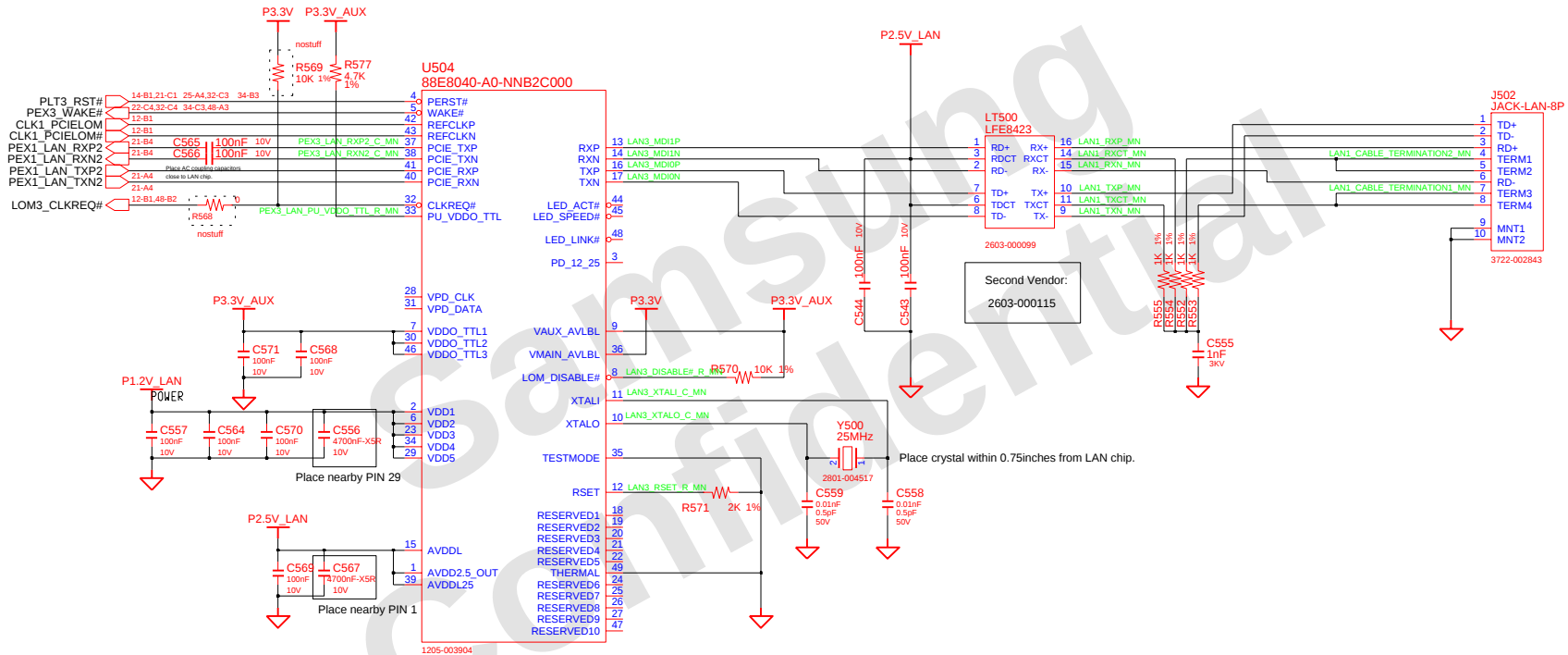
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	LED_SWITCH	LED_SWITCH	ELECTRONICS
APPROVAL	BC LEE	REV	0.1			PART NO.
MODULE CODE		LAST EDIT				BA41-xxxxxxA
				July 15, 2009 19:25:13 PM	PAGE	35 OF 58

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DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	HDA_CODEC	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	AUDIO CODEC ALC269_GR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	37	OF 58

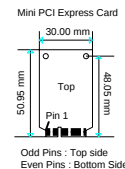
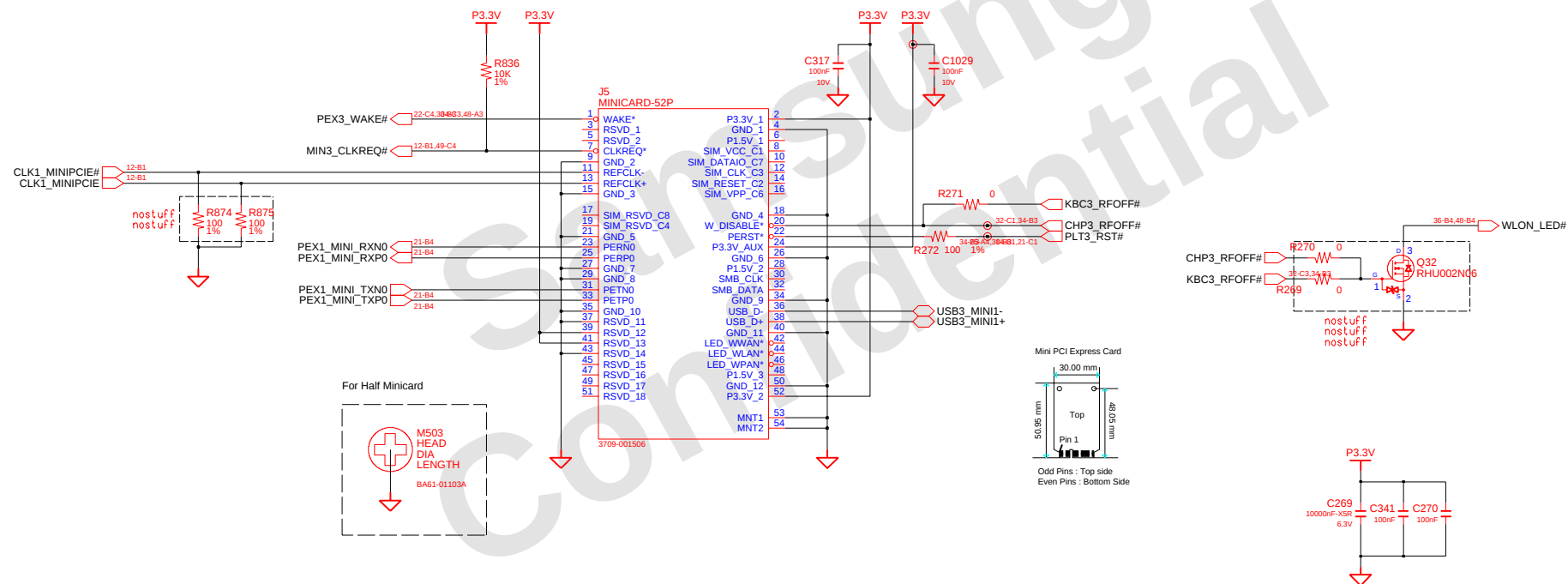
LAN Controller (Marvell 88E8040)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA
CHECK	GUO LEI	DEV. STEP	ADV	LAN		
APPROVAL	BC LEE	REV	0.1	LAN_Marvell 88E8040		
MODULE CODE		LAST EDIT				
				July 15, 2009 19:25:13 PM	PAGE 38 OF 58	

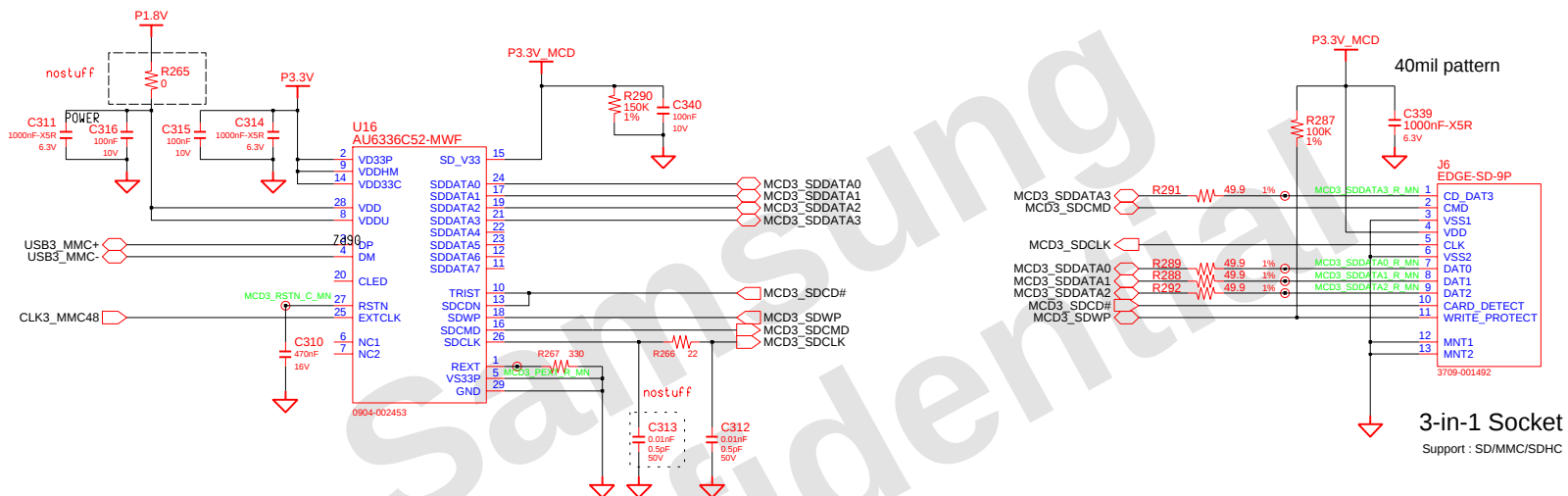
Wireless LAN

WLAN, 4mm



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	MINI_PCIE_CONN	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	Wireless LAN	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	39 OF 58

Card Reader (AU6336)

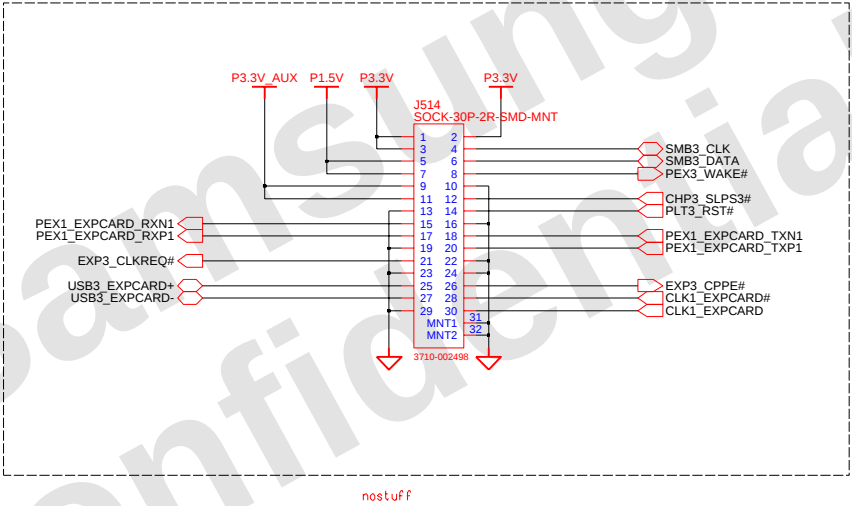


MCD3_SD_SPD	SD v1.0 Clock Option
PU / PD : No Stuff	24 MHz (default)
PU : Stuff, PD : No Stuff	15 MHz

MCD3_CLK_IN	827S Clock Source option
PU : X, PD : X	12MHz, fixed S/N
PU : No Stuff, PD : Stuff	12MHz, no S/N
PU : Stuff, PD : No Stuff	48MHz

DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	MULTICARD		
APPROVAL	BC LEE	REV	0.1	3 IN 1 CARD		
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	40 OF 58	

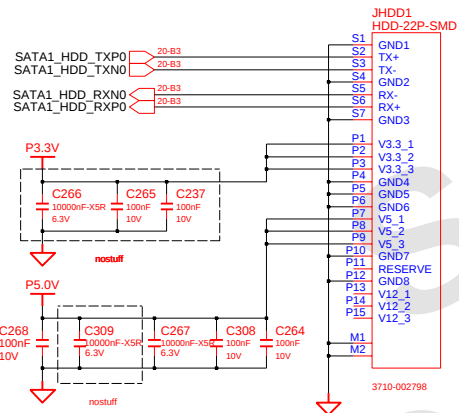
Express Card Connector



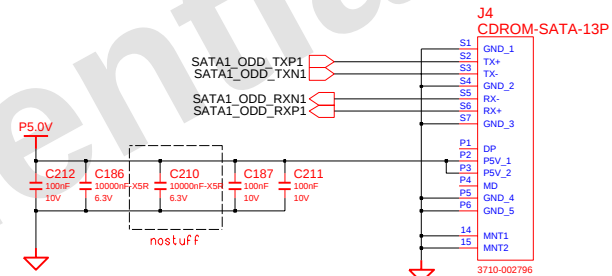
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1	EXPRESS CARD		PART NO. BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	41	OF 58

SATA I/F CONN

SATA HDD CONN



ODD CONN

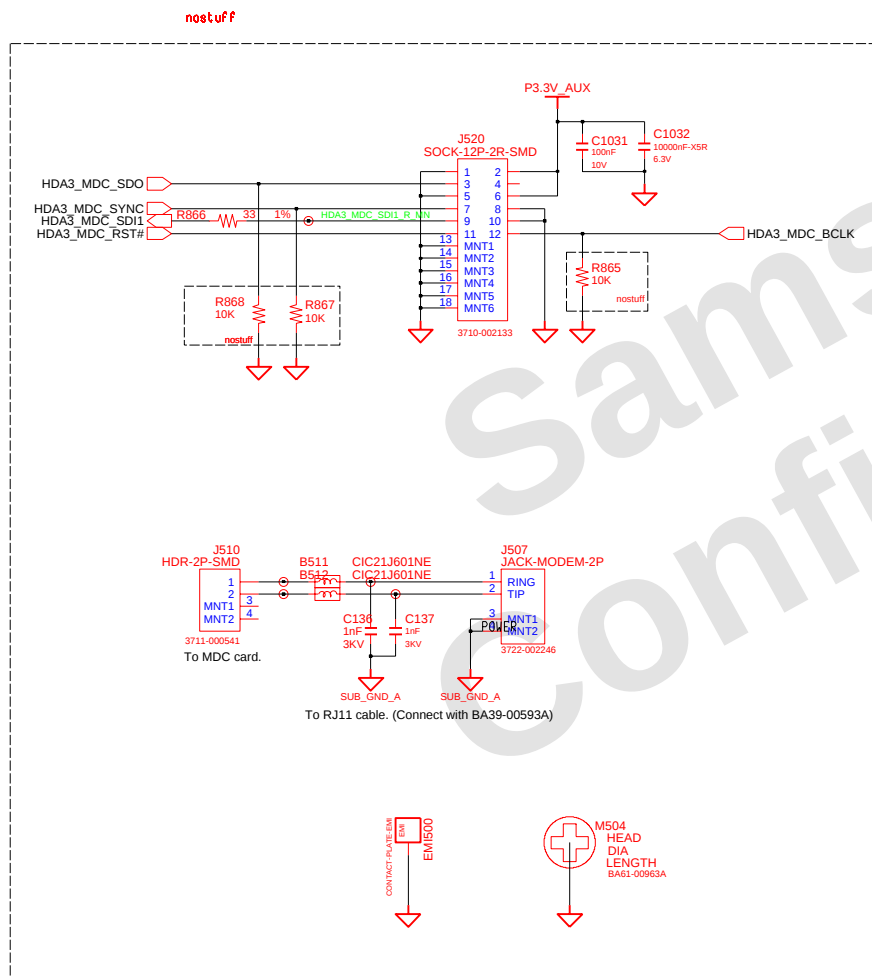


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D SATA_DEVICES HDD & ODD SUB BONNECTOR	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV			PART NO. BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE 42 OF 58	

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MDC Connector

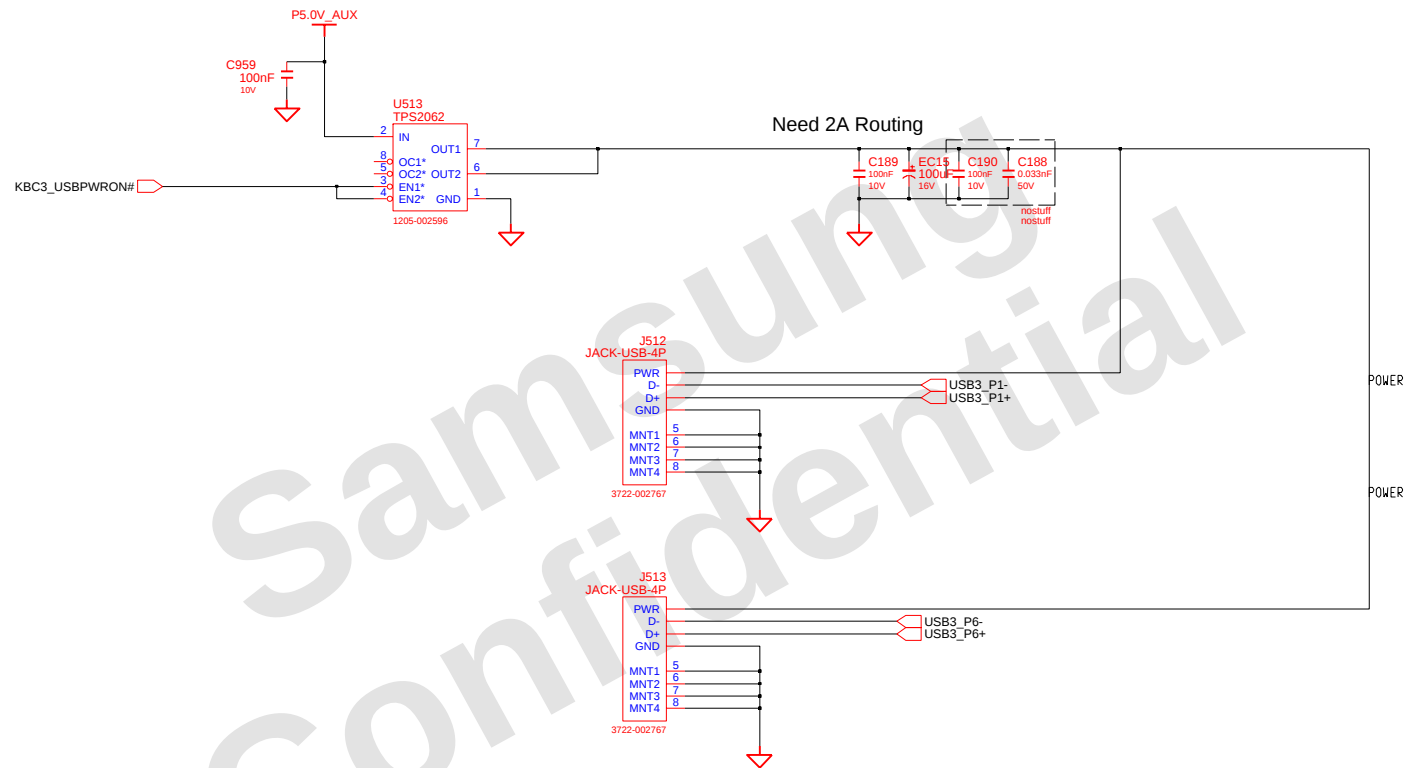
BLUETOOTH



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	HDA_MODEM & BLUETOOTH	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	MODEM & BLUETOOTH	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	43	OF 58

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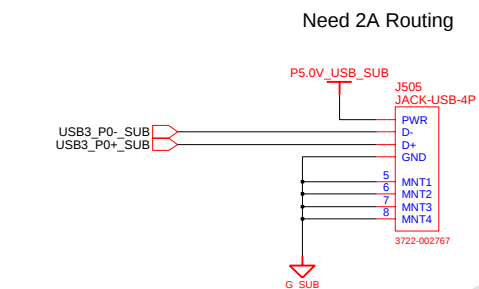
LEFT USB PORT



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (1/2)	PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE 44 OF 58

USB PORT & POWER S/W SUB B'D

TOP RIGHT USB PORT



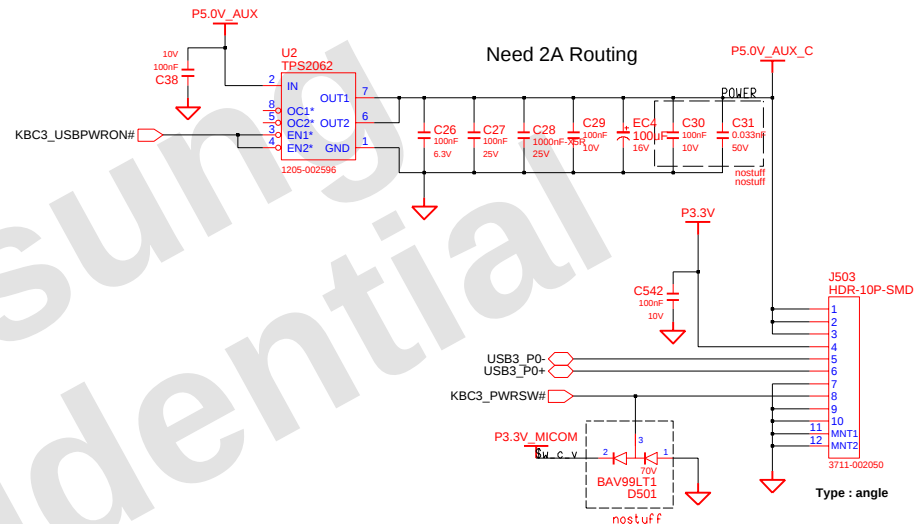
Power Button



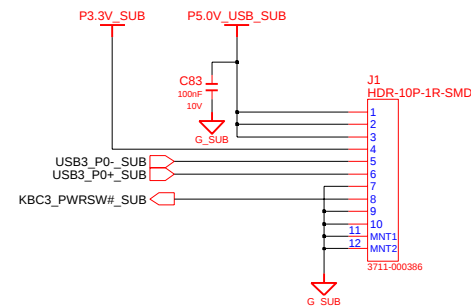
Power ON LED



MAIN TO SUB USB CONN

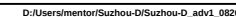


SUB TO MAIN USB CONN

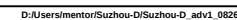


DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG ELECTRONICS
CHECK	GUO LEI	DEV. STEP	ADV	USB_CONNECTOR	USB_CONNECTOR	
APPROVAL	BC LEE	REV	0.1	USB_CONNECTOR (2/2)	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM	PAGE 45 OF 58

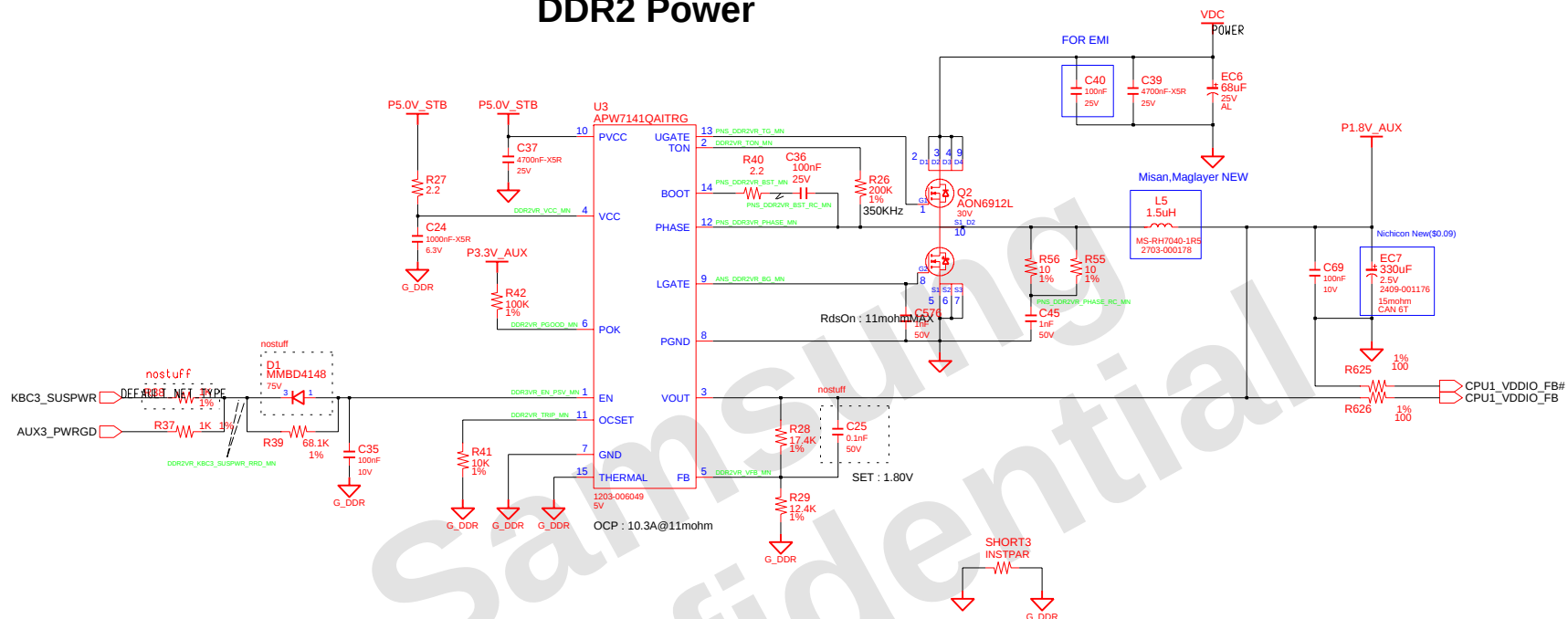
CHARGER & POWER MANAGEMENT



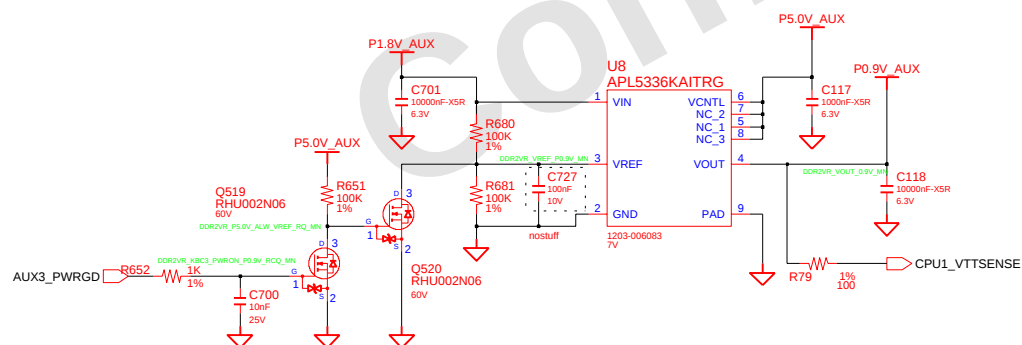
P3.3V_AUX & P5.0V_AUX



DDR2 Power



DDR2 VTT(P0.9V_AUX)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MEMORY	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	DDR2 POWER	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	48 OF 58

$VW \& COMP / 2.33 + 0.29$ uS
 $2.6\text{KHz} @ 6.8\text{Kohm}$
 $1 / ((1.5 \times 10^{-6}) \times Rfsetnb)$ Hz
 $13\text{KHz} @ 22\text{Kohm}$

Place 4700nF like Zigzag

VFXEN VID CODES			
SVC	SVD	VOUT	
0	1	1.4V	
0	1	1.2V	
1	0	1.0V	
1	1	0.8V	

Pre-PWROK Metal VID			
SVC	SVD	VOUT	
0	0	1.1V	
0	1	1.0V	
1	0	0.9V	
1	1	0.8V	

DRAW: XIE BIN, DATE: 08/18/2009, TITLE: Suzhou-D
 CHECK: GUO LEI, DEV. STEP: ADV, PWR_CPU_MV_ISL6265HRT

Figure 10 illustrates the pin configuration for VFIEN and VFIENLPIN. It consists of three tables:

OFS/VFIEN(LPin)	
	OFS VFIEN
3.3V	Disable , Enable
GND	Enable ' Disable
5V	Disable , Disable

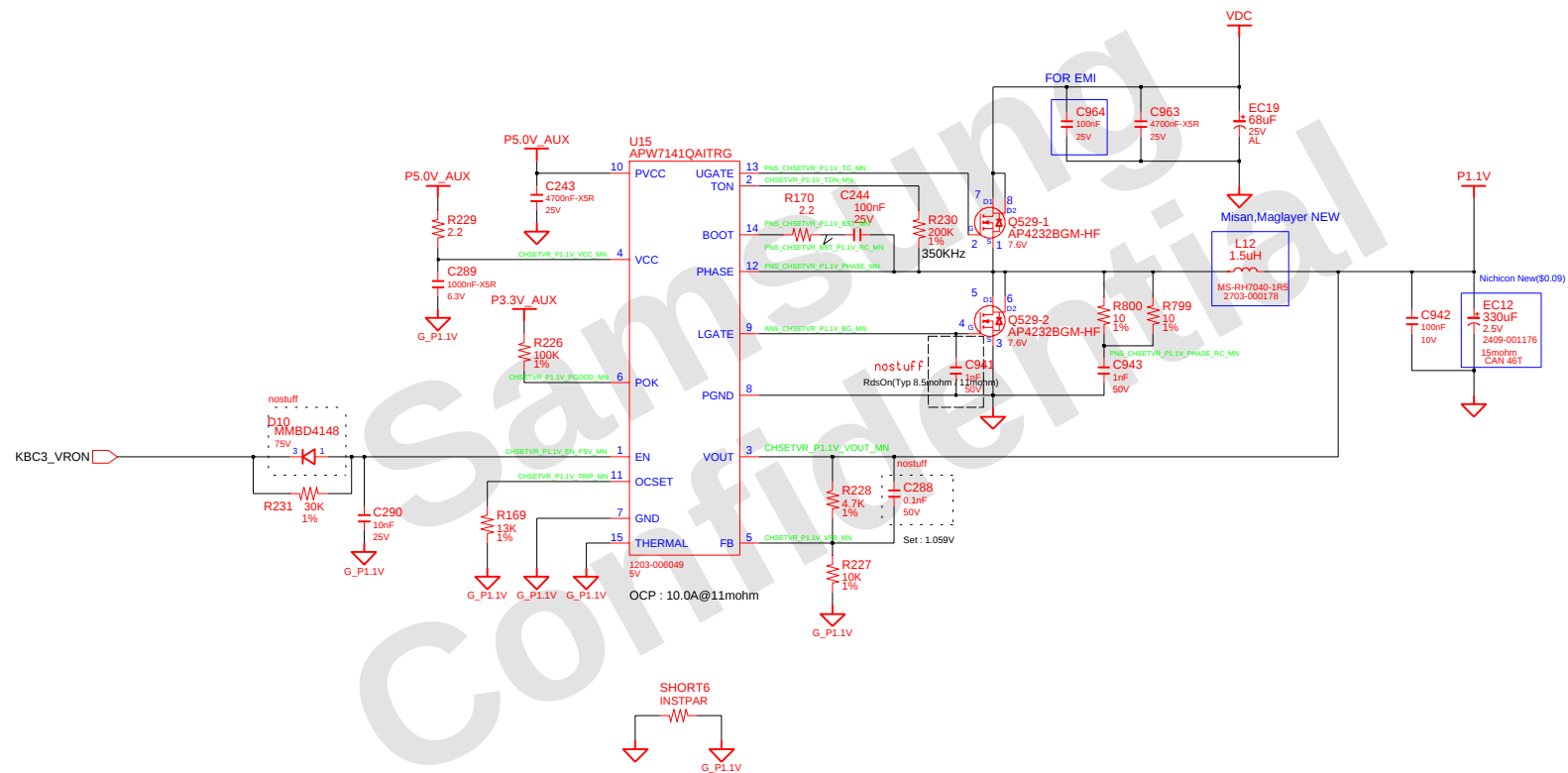
VFIEN VID CODES		
SVC	SVD	VOUT
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

COM-22C-015(1996.6.5) REV. 3

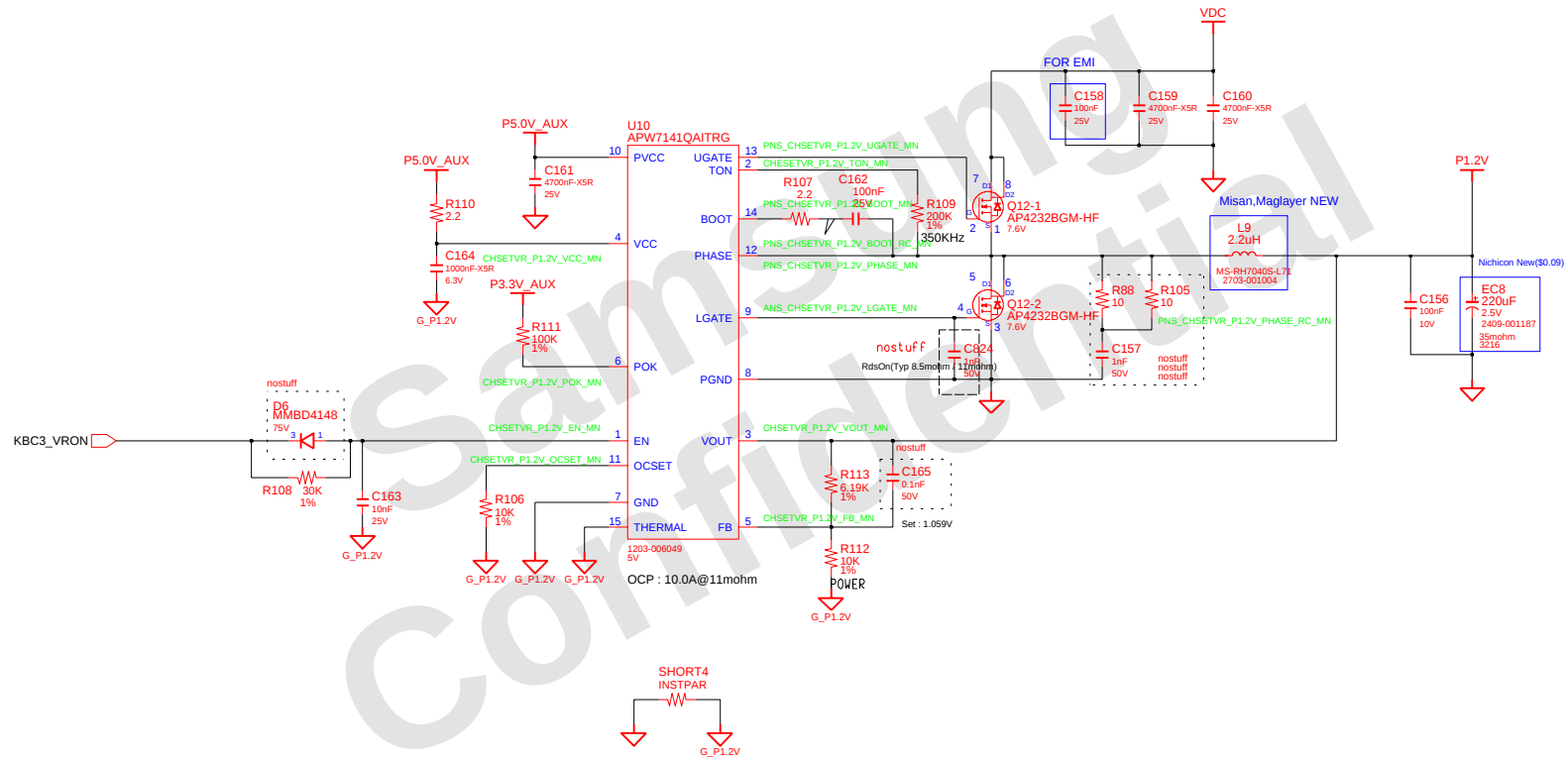
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CHIPSET POWER(P1.1V)



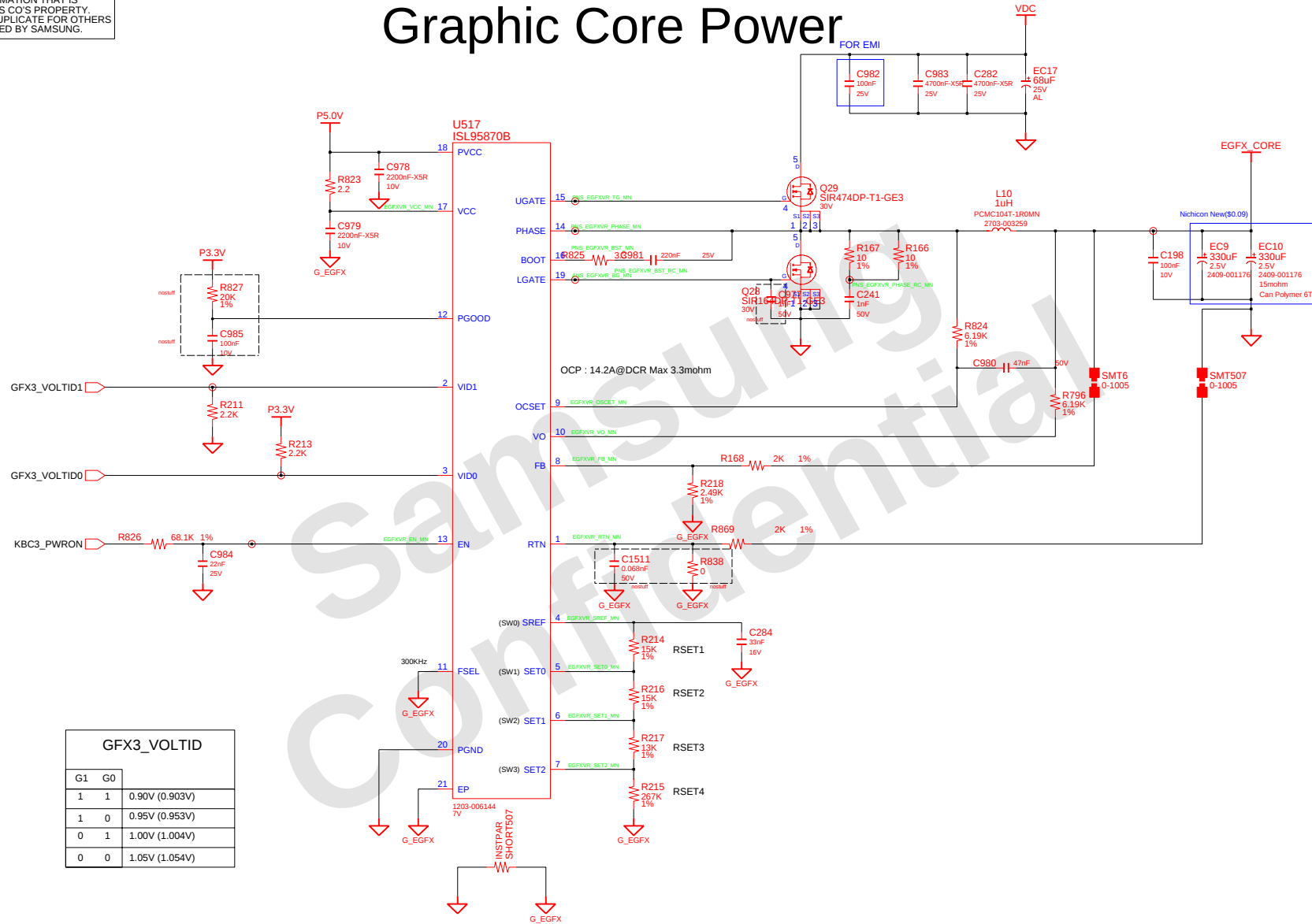
DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	P1.1V	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		July 15, 2009 19:25:13 PM	PAGE	50 OF 58

CHIPSET POWER(P1.2V)



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_MV_RX881	ELECTRONICS	
APPROVAL	BC LEE	REV	0.1	P1.2V	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	51	OF 58

Graphic Core Power



A

3

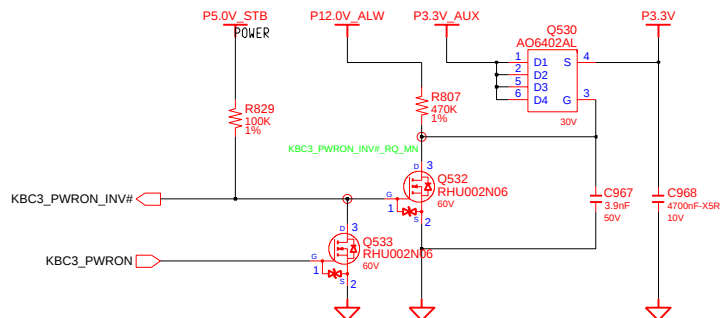


P5

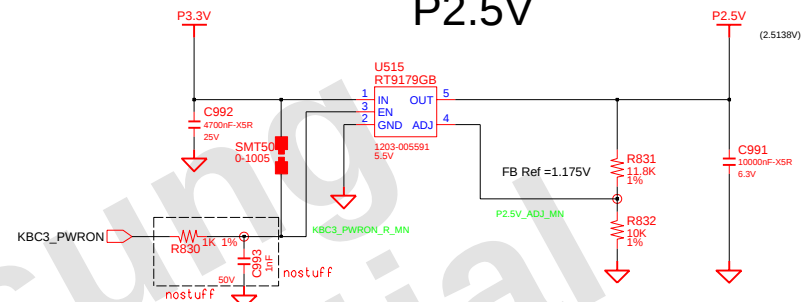
D:/Users/mentor/Suzhou-D/Suzhou-D_adv1_0826

Switched Power

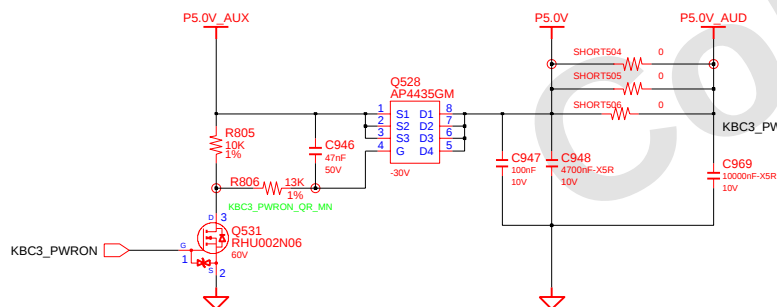
Switched Power On (P3.3V)



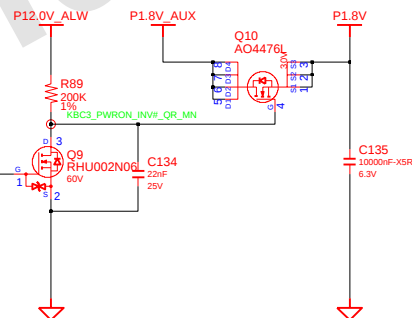
P2.5V



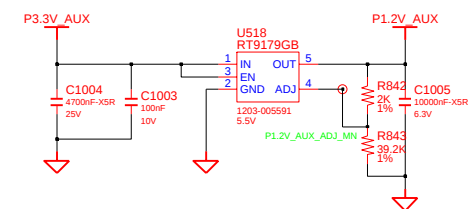
Switched Power On (P5.0V)



Switched Power On (P1.8V)

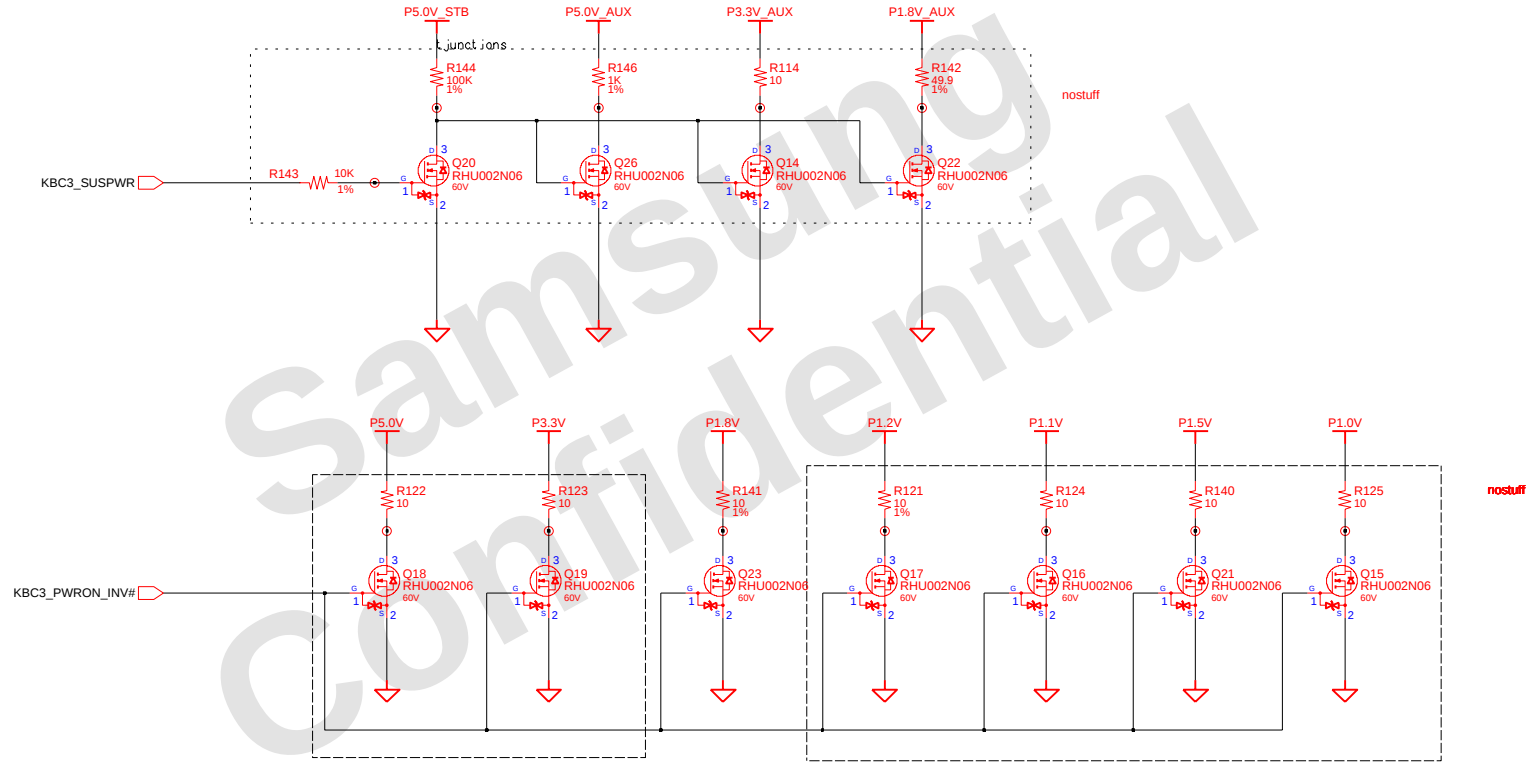


P1.2V AUX



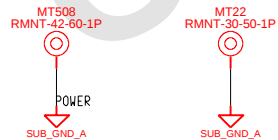
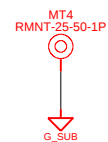
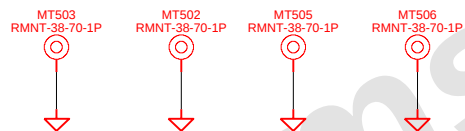
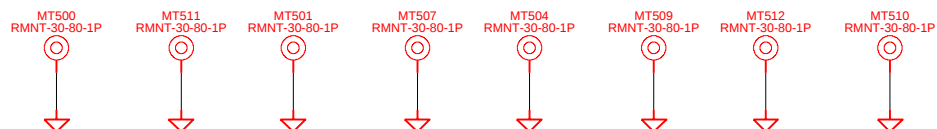
DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D PWR_SWITCH SWITCH POWER		
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1		PART NO.	BA41-xxxxxxA
MODULE CODE	LAST EDIT				July 15, 2009 19:25:13 PM	PAGE 54 OF 58

POWER DISCHARGER



DRAW	XIE BIN	DATE	08/18/2009	TITLE	Suzhou-D	SAMSUNG
CHECK	GUO LEI	DEV. STEP	ADV	PWR_CPU_MV_IDISCHARGER		ELECTRONICS
APPROVAL	BC LEE	REV	0.1	DISCHARGER LOGIC	PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT	July 15, 2009 19:25:13 PM	PAGE	55	OF 58

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DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D MAIN MOUNT HOLE		
CHECK	GUO LEI	DEV. STEP	ADV			
APPROVAL	BC LEE	REV	0.1		PART NO.	BA41-xxxxxxA
MODULE CODE		LAST EDIT			July 15, 2009 19:25:13 PM	PAGE 56 OF 58

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- ☐ VREF0
- ☐ CPU1_SIC
- ☐ CPU1_SID
- ☐ CPU1_SVC
- ☐ CPU1_SVD
- ☐ CR73_RED
- ☐ SM83_CLK
- ☐ SPI3_CLK
- ☐ AD73_SEL#
- ☐ CR73_BLUE
- ☐ KBG3_A20G
- ☐ KBG3_VRON
- ☐ KBG5_TCLK
- ☐ LCD1_ACL
- ☐ LCD1_RIR
- ☐ LPP3_CLK0
- ☐ LPP3_CLK1
- ☐ MCD3_SDWP
- ☐ SM83_DATA
- ☐ SPI3_CS0#
- ☐ SPI3_MISO
- ☐ SPI3_MOSI
- ☐ THM3_STP#
- ☐ WLON_LED#
- ☐ CR73_GREEN
- ☐ CR73_HSYNC
- ☐ CR73_VSYNC
- ☐ CR73_HSYNC
- ☐ CR73_VSYNC
- ☐ DBG3_HSYNC
- ☐ DBG3_VSYNC
- ☐ GF3X_GPI00
- ☐ GF3X_GPI01
- ☐ GF3X_GPI02
- ☐ KBG3_CHGEN
- ☐ KBG3_PWRGD
- ☐ KBG3_PWRON
- ☐ KBG3_RCIN#
- ☐ KBG5_TDATA
- ☐ MCD3_SDCD#
- ☐ MCD3_SDLCK
- ☐ MCD3_SDCMD
- ☐ MEM0_VREF0
- ☐ MEM1_VREF1
- ☐ PEX3_WAKE#
- ☐ SB_X1_C_MN
- ☐ SB_X2_C_MN

- ☐ CHGVR_EN_MN
- ☐ CHP3_GPIO16
- ☐ CHP3_GPIO17
- ☐ CHP3_RTCLK
- ☐ CHP3_SERIRQ
- ☐ CHP3_SLPS3#
- ☐ CHP3_SLPS5#
- ☐ CK_PD#_R_MN
- ☐ CPU1_ALERT#
- ☐ CRT3_DDBCLK
- ☐ GFX_NC_B_MN
- ☐ KBC3_BKLTON
- ☐ KBC3_PRECHG
- ☐ KBC3_PWRSW#
- ☐ KBC3_RFOFF#
- ☐ KBC3_SCLE#
- ☐ KBC3_SMCLK#
- ☐ KBC3_SPL_DI
- ☐ KBC3_SPL_DO
- ☐ KBC5_KSI(0)
- ☐ KBC5_KSI(1)
- ☐ KBC5_KSI(2)
- ☐ KBC5_KSI(3)
- ☐ KBC5_KSI(4)
- ☐ KBC5_KSI(5)
- ☐ KBC5_KSI(6)

KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)
LCD3_BKLTN
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
SMB3_ALERT#
BAT3_DETECT#
CHGVR_ICTM_MN
CHGVR_CSIN_MN
CPU1_LDTRREQ#
CPU1_LDTRDATA#
CPU1_LDTRST#
CPU1_DDCDATA#
EGFXPV_VO_MN
EGFXPV_CLKREQ#
KBC3_BATDET#
KBC3_CHG42V#
KBC3_CHG42V_MN
KBC3_NUMLED#
KBC3_PWRBNT#
KBC3_RSMRST#
KBC3_RSMRST#
KBC3_RST#
KBC3_SPI_CLK
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)
KBC_CAP_C_MN
LPC3_LAD(4)
LPC3_LFRAME#
MCD3_SDDATA0
MCD3_SDDATA1
MCD3_SDDATA2
MCD3_SDDATA3
MCD3_LITTS0#
MCH3_EXTTST#
MIN3_CLKREQ#
PC3_CLKRUN#
PC3_CLKRUN#
PC3_CLKRUN#
CHGVR_CSIN_MN
CHGVR_CSIP_MN
CHGVR_CSON_MN
CHGVR_CSPM_MN
CHGVR_CSPM_MN
CHGVR_CSPM_MN
CHGVR_VADJ_MN
CHGVR_VDDP_MN
CHP3_NB_PWRG#
CHP3_SATALED#
CHP3_TEST0#
CHP3_SB_TEST2
CHP3_SUSTAT#
CPU1_VDDIO_FB
CPU1_VDDNB_FB
CPU1_VDDNB_FB#
CRT3_RDN_L_MN
CRT3_RDN_L_MN
DDR2VR_TON_MN
DDR2VR_VCC_MN
DDR2VR_VFB_MN
DDR2VR_VFB_MN
EGFXVR_VCC_MN
EGFXVR_VCC_MN

[illegible]

GML_VREFDQ0_1_R,M
 GML_ZQ_Q000_R,M
 GML_ZQ_Q001_R,M
 GML_VREFCA0_1_R,M
 GML_VREFCA1_1_R,M
 GML_VREFDQ0_1_R,M
 GML_ZQ_Q000_R,M
 GML_ZQ_Q001_R,M
 GML_ZQ_Q000_R,M
 GML_ZQ_Q001_R,M
 GML_ZQ_Q000_R,M
 KBC3_TSEN_SMLCK
 PMS_CHGVR_BST_MN
 PMS_DRDVR_TG0_MN
 PMS_SYSVR_TG1_MN
 PMS_SYSVR_TG2_MN
 PMS_SYSVR_TG3_MN
 SDI_DC01_SDA_R,M
 SDI_DC01_SDA_R,M
 SDI_SHDN_SLE_R,M
 WLON_LED_LED,MN
 CHGVR_CK0_P000_R,M
 CHGVR_VCOOP_RC,MN
 CPUF_TEST25_H_R,MN
 CPUF_TEST25_L_R,MN
 GFGX_CLKTEST4_C,MN
 GFGX_CLKP0_P000_R,M
 GFGX_TESTEN_2_R,MN
 KBC3_TSEN_SMDATA
 PMS_DRDVR_BST_MN
 PMS_EGFXVR_BST_MN
 PMS_EGFXVR_BST_MN
 GFGX_DPAB_CLK_R,MN
 GFGX_DPAB_VD018_B,MN
 GFGX_DP0_VD010_B,MN
 GFGX_DPRL_VD008_B,MN
 LACI_DP0_VD008_B,MN
 PEGAS_HDMI_CLK_B,MN
 VEGAS_HDMI_HPD_R,MN
 CHESTRV_P12V_EN,MN
 PMS_DRDVR_P12V_EN,MN
 CHESTRV_P12V_VCC,MN
 DRDVR_VIO_P0V9_MN
 GFGX_MEM_CALRPO_R,MN
 GFGX_PCIE_CALRPO_R,MN
 GFGX_PCIE_CALRPO_R,MN
 PEG3_LCDVD0DQ_CR,MN
 PMS_CHGVR_BST_RC,MN
 PMS_DRDVR3_PHASE,MN
 PMS_DRDVR3_BOOT,MN
 AMS_GD03V_BOOT,MN
 CHESTRV_SATALED_LED,MN
 CHESTRV_P11V_TON,MN
 CHESTRV_P11V_VCC,MN
 CHESTRV_P11V_VFE,MN
 CHESTRV_P11V_VFE,MN
 CHESTRV_P12V_VCC,MN
 CHESTRV_P12V_VCC,MN
 DRDVR_VIO_P0V9_MN
 GFGXVR_P10V_P0V9_MN
 GFGXVR_P10V_VOUT,MN
 GFGXVR_P10V_VOUT,MN
 PMS_DRDVR3_BST_RC,MN
 PMS_DRDVR3_PHASE,MN
 PMS_DRDVR3_UGATE,MN
 PMS_DRDVR3_UGATE,MN
 CHESTRV_P11V_TRIP,MN
 KBC3_LED_CHARGER_R,MN
 NM_ALLOW_LDSTOPP_R,MN
 P313V_VDD_INV_EN,MN
 P313V_VDD_INV_EN,MN
 CHESTRV_P11V_PG00D,MN
 CHESTRV_P12V_OSCET,MN
 P313V_VDD_INV_EN_OR,MN
 PMS_DRDVR3_PHASE,R,MN
 PMS_DRDVR3_PHASE,R,MN
 PMS_SYSVR_P3ASE2_RC,MN

ANS_CHESTRV_P11V_BG_MM
 CHGVR_KBC3_PRECHG_RQ_MM
 CHGVR_P33V_MICOM_RQ_MM
 CHESTRV_P11V_EN_PSV_MM
 CREF_G_SEL_HTTB6_R_MM
 CHESTRV_P11V_TC_MM
 PMS_GDDR3VR_PHASE_RC_MM
 CHGVR_KBC3_K8C4_2V_RQ_MM
 PMS_CHESTRV_P11V_BST_MM
 DDPWR_KBC3_SUSPWR_RQ_MM
 EGGFXVR_P10V_P50V_ALW_MM
 PMS_CHESTRV_P12V_BOOT_MM
 PMS_CHESTRV_P12V_LOAD_MM
 NB_REFCLK_N_PWM_GP03_R_MM
 CHESTRV_P11V_PHASE_MM
 PMS_CHESTRV_P12V_PHASE_MM
 PMS_CHESTRV_P12V_UGATE_MM
 DDP2VR_P50V_ALW_VREF_RQ_MM
 PMS_CHESTRV_BST_P11V_RC_MM
 EGGFX_P10V_KBC3_PWRON_R_MM
 PMS_CHESTRV_P12V_BOOT_RC_MM
 PMS_CHESTRV_P11V_PHASE_RC_MM
 DDP2VR_KBC3_PWRON_P09V_RC_MM
 AVDD
 A2VDD
 A2VDDQ
 CPU0_CORE
 CPU0_CORE
 DPC_PVD0
 DPC_VDD18
 G_CHG
 G_CPU
 G_DDR
 G_GSUB
 G_EGFX
 G_P11V
 G_P12V
 G_P15V
 G_P33V
 LCD_VDD3V
 P10V
 P25V
 P50V_AUX
 P12V_AUX
 P12V_LAN
 P18V_AUX
 P20V_REF
 P33V_LAN
 P33V_LED
 P33V_LED
 VDD_LED
 P33V_MCD
 P33V_MCD
 P33V_SUB
 P50V_AUX
 P50V_AUX
 P50V_STB
 P50V_STB
 P120V_ALW
 P120V_ALW
 P475V_AUDD
 P230V_VREF
 P230V_VREF
 P50V_AUX_C
 P50V_USB_SUB
 P50V_USB_SUB
 SPI0
 SUB_GND_A
 VDDC
 VDDC
 VDDIO1DI
 VDDIO2DI
 VCC_CRT

○ VCC_CRT
○ VDD_LED

DRAW	XIE BIN	DATE	08/18/2009	Suzhou-D Test Point	SAMSUNG ELECTRONICS	
CHECK	GUO LEI	DEV. STEP	ADV		PART NO.	BA41-xxxxxxA
APPROVAL	BC LEE	REV	0.1			
MODULE CODE	LAST EDIT					