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# BREMEN-D

CPU : AMD Caspin  
Chip Set : AMD RX881 + SB710  
Remarks : Tigris Platform  
Park-XT M2

Model Name : Bremen-D  
PBA Name : MAIN  
PCB Code : GCE :  
                  NAN :  
                  HAN :  
Dev. Step : PV  
Revision : 1.4  
T.R. Date : 2009.11.10

Design	CHECK	APPROVAL

Owner : SEC Mobile R & D      Signature :      X

## Table of Contents

Page. 1 ---- COVER  
Page. 2 ---- OPERATION BLOCK DIAGRAM  
Page. 3 ---- BOARD INFORMATION  
Page. 4 ---- POWER DIAGRAM  
Page. 5 ---- POWE RAILS ANALYSIS  
Page. 6 ---- TIMING DIAGRAM, POWER ON  
Page. 7 ---- CLOCK DISTRIBUTION  
Page. 8 ---- THERMAL SENSOR&FAN CONTROL  
Page. 9~11 --- CASPIAN S1G3 CPU  
Page. 12 --- CLOCK GENERATOR  
Page. 13~15 - RX881M  
Page. 16~17 - SODIMM DDR2  
Page. 18~22 - MADISON-LP  
Page. 23~27- gDDR3 & MADISON STRAPS  
Page. 25~32- SB710  
Page. 33 ---- SPI\_BIOS\_ROM  
Page. 34 ---- LVDS (LCD CONNECTOR)  
Page. 35 ---- CRT CONNECTOR  
Page. 36 ---- HDMI CONNECTOR  
Page. 37~38 - AUDIO  
Page. 39 ---- LOM(RTL8103EL)  
Page. 40 ---- MEMORY CARD (3 IN 1)  
Page. 41 ---- WLAN  
Page. 42 ---- HDD / ODD  
Page. 43 ---- MICOM  
Page. 44 ---- KBD CONN & TOUCHPAD  
Page. 45 ---- LED LOGIC  
Page. 46 ---- USB CONNECTOR  
Page. 47 ---- BLUETOOTH  
Page. 48 ---- CHARGER  
Page. 49 ---- P3.3V\_AUX / P5.0V\_AUX / P12V\_ALW  
Page. 50 ---- DDR2 POWER / VTT  
Page. 51 ---- CPU VRM  
Page. 52 ---- CHIPSET POWER(P1.1V)  
Page. 53 ---- CHIPSET POWER(P1.2V)  
Page. 54 ---- GFX POWER  
Page. 55 ---- gDDR3 POWER / P1.0V  
Page. 56 ---- SWITCHED POWER  
                  (P5.0V / P3.3V / P2.5V / P1.8V / P1.2\_AUX)  
Page. 57 ---- POWER DISCHARGER  
Page. 58 ---- USB SUB BOARD\_POWER SWITCH  
Page. 59 ---- SUB BOARDS  
Page. 60 ---- MOUNT HOLES  
Page. 61 ---- TEST POINTS

DRAW	XIE, BIN	DATE	10/10/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS
CHECK	GUO, LEI	DEV. STEP	PV	MAIN		
APPROVAL	LEE, BC	REV	1.0	COVER		PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	October, 28, 2009 11:35:37 AM	PAGE	1	OF



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**BOARD INFORMATION**

**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION**

**Voltage Rails**

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.1V	VTT for RX881
P1.2V	Core Voltage for SB710, CPU_VDLT, RX881
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P1.0V	0.9V power rail for DDR (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_STB	5.0V always power rail
P12.0V_ALW	12.0V always power rail

**Crystal / Oscillator**

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB710	Real Time Clock
Crystal	10MHz	MICOM	MEC1308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040
Crystal	25MHz	SATA	SB710

**I<sup>2</sup>C / SMB Address**

Devices	Address	Hex	Bus
S710	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable
Gfx (DTS)		41h	Gfx Thermal SMBUS Slave ID

**USB PORT Assign**

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	NC
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	NC

**PCI Express Assign**

PORT #	ASSIGNED TO
0	Mini Card (WLAN)
1	NC
2	LOM
3	NC
4	NC
5	NC

**LCD Pannel Detect (TBD)**

Devices	Resolution	PANNEL_DETECT_0(strap0)

**REVISION HISTORY**

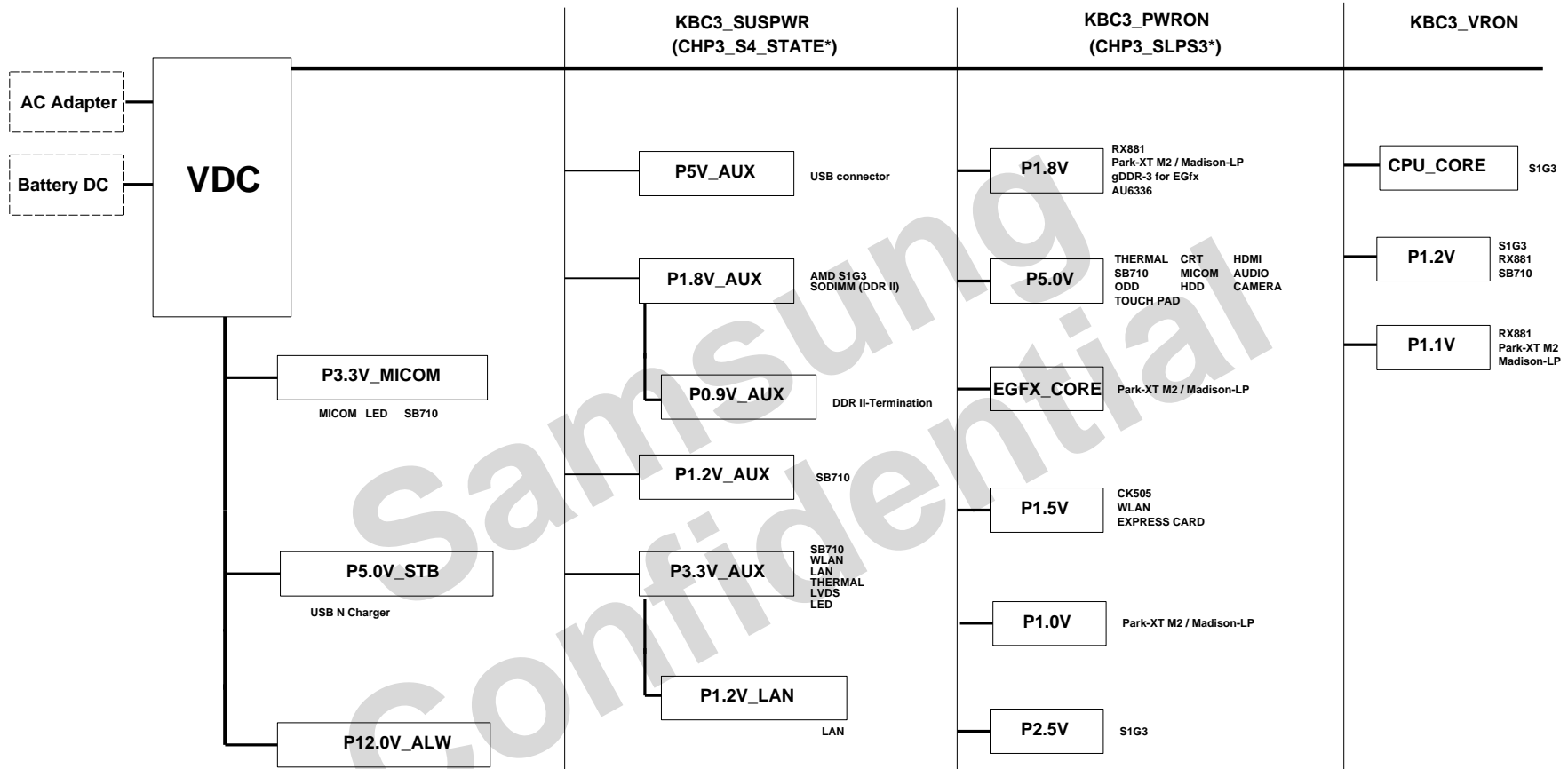
See rev notes for more information.

DRAW	H.J.Ra	DATE	08/18/2009	TITLE	<b>Bremen-D</b> <b>MAIN</b> <b>BOARD INFORMATION</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM			
				PAGE	3	OF 61

# POWER DIAGRAM

Rev 0.3

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Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V_AUX	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—



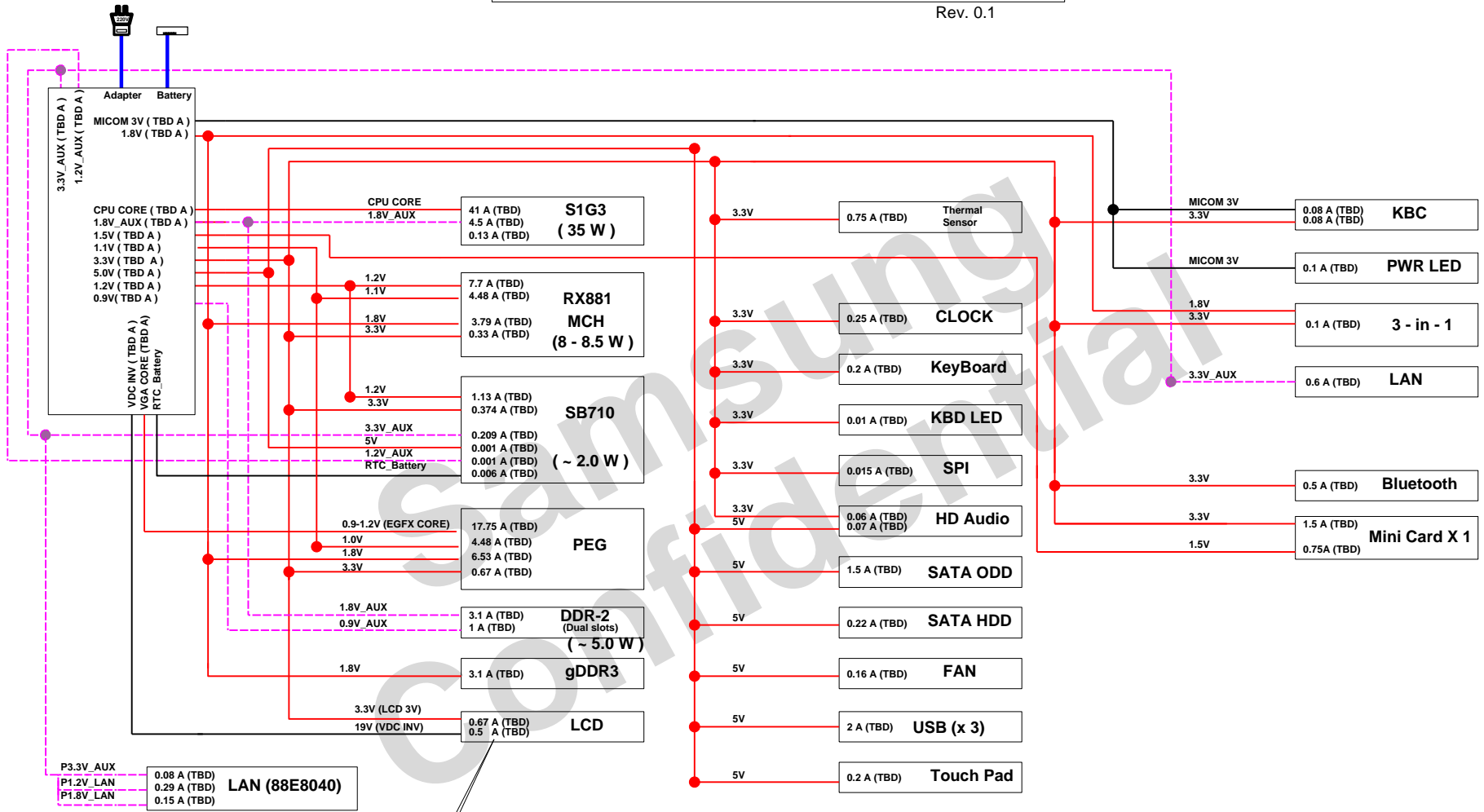
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CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	4 OF 61

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# POWER RAILS ANALYSIS

Rev. 0.1



Value by Datasheet/Application notes (Value by measurement)

DRAW	H.J.Ra	DATE	08/18/2009	TITLE	Bremen-D MAIN POWER RAILS ANALYSIS	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	5 OF 61

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**Host Boot / ME Off**

(SLPS4\* = S4\_STATE\*) > (SLPM\* = SLPS3\*)  
 M-1) KBC3\_DDR\_PWRON (TBD) = 8) KBC3\_SUSPWR  
 M-2) KBC3\_ME\_PWRON = 15) KBC3\_PWRON

**Host / ME Boot**

(SLPS4\* = S4\_STATE\*) > SLPM\* > SLPS3\*

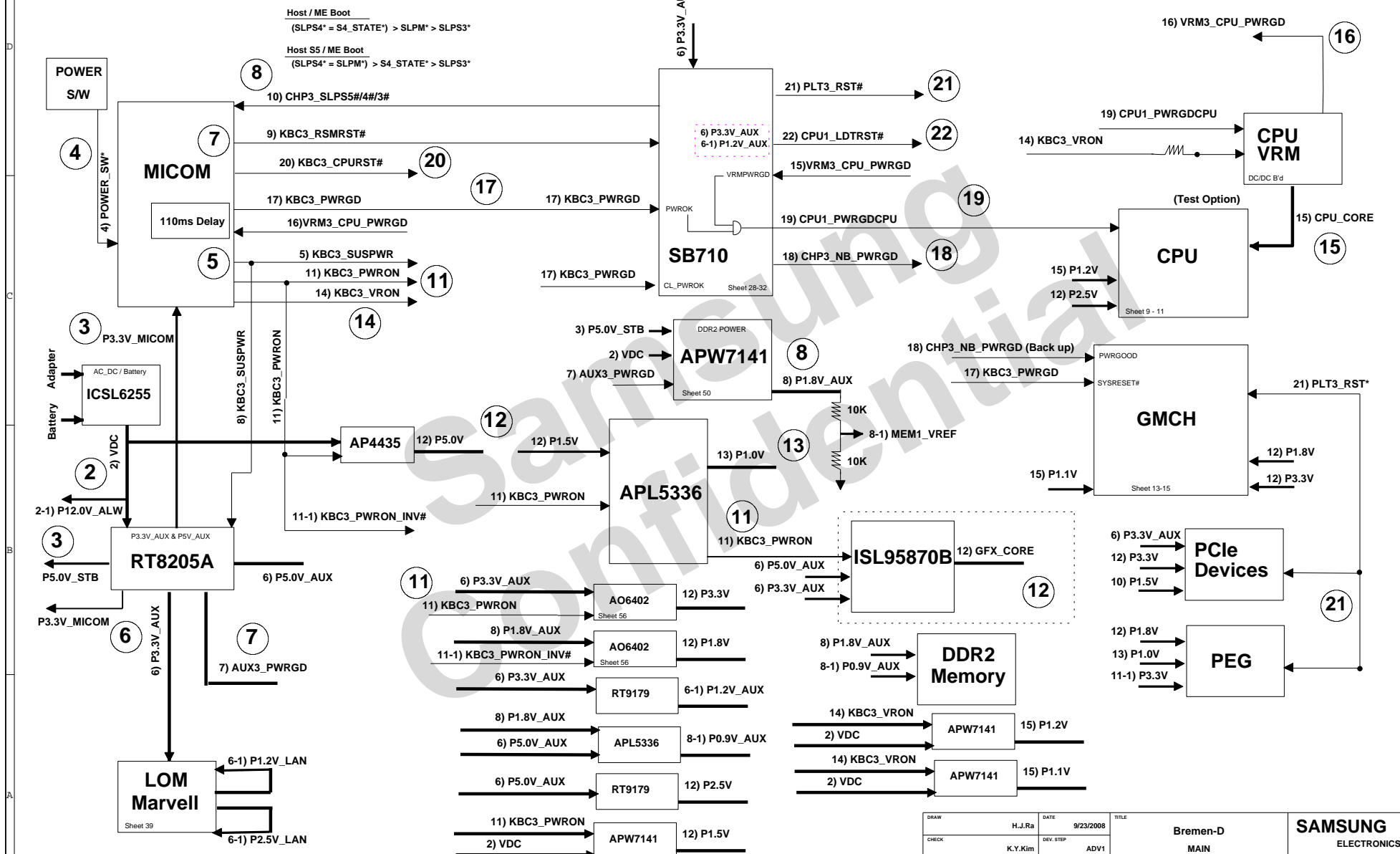
**Host S5 / ME Boot**

(SLPS4\* = SLPM\*) > S4\_STATE\* > SLPS3\*

**RTC Battery** ①  
 PRTC\_BAT  
 CHP3\_RTCRST#

# POWER SEQUENCE

Rev. 0.3

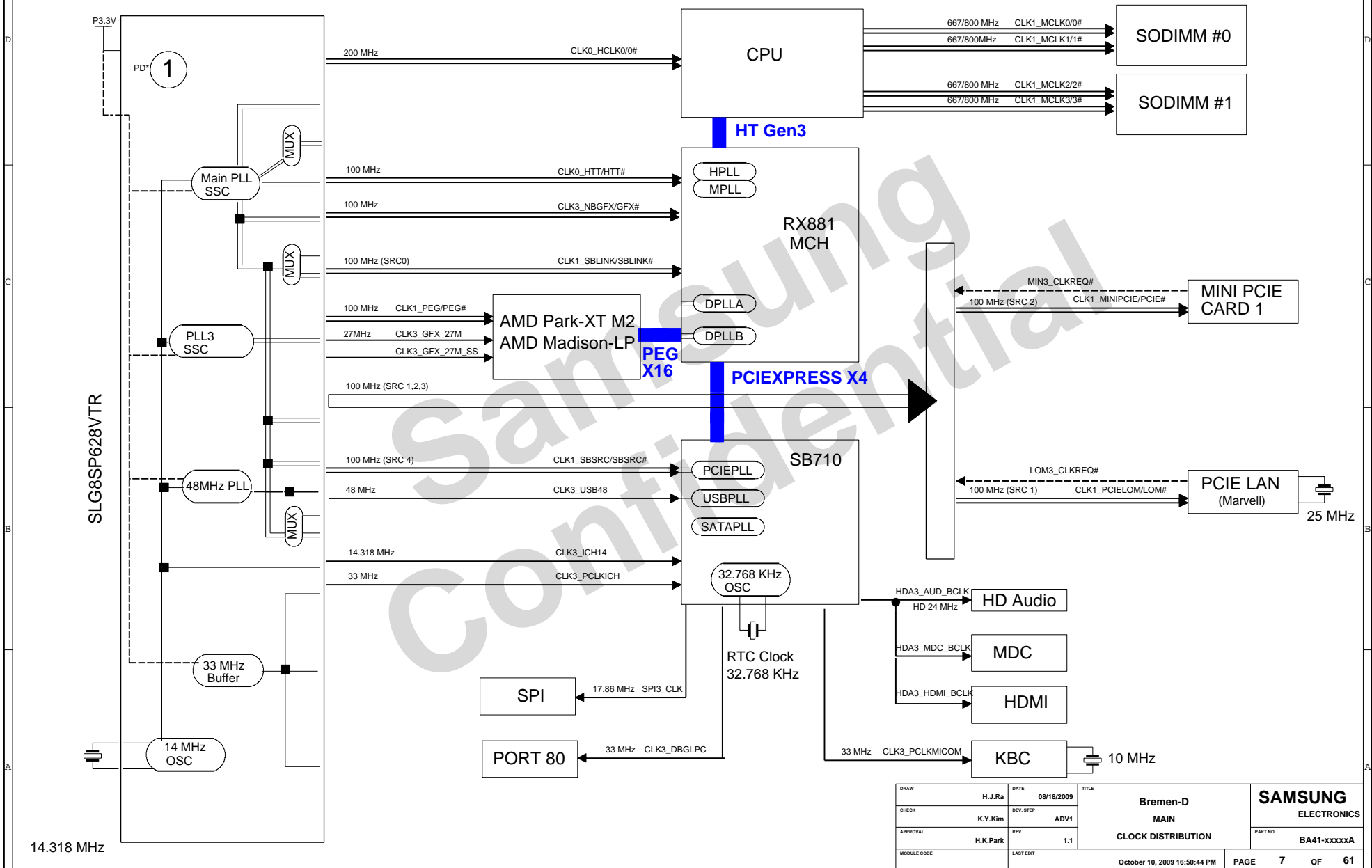


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MAIN POWER SEQUENCE	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT				
October 10, 2009 16:50:44 PM						PAGE 6 OF 61

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# CLOCK DISTRIBUTION

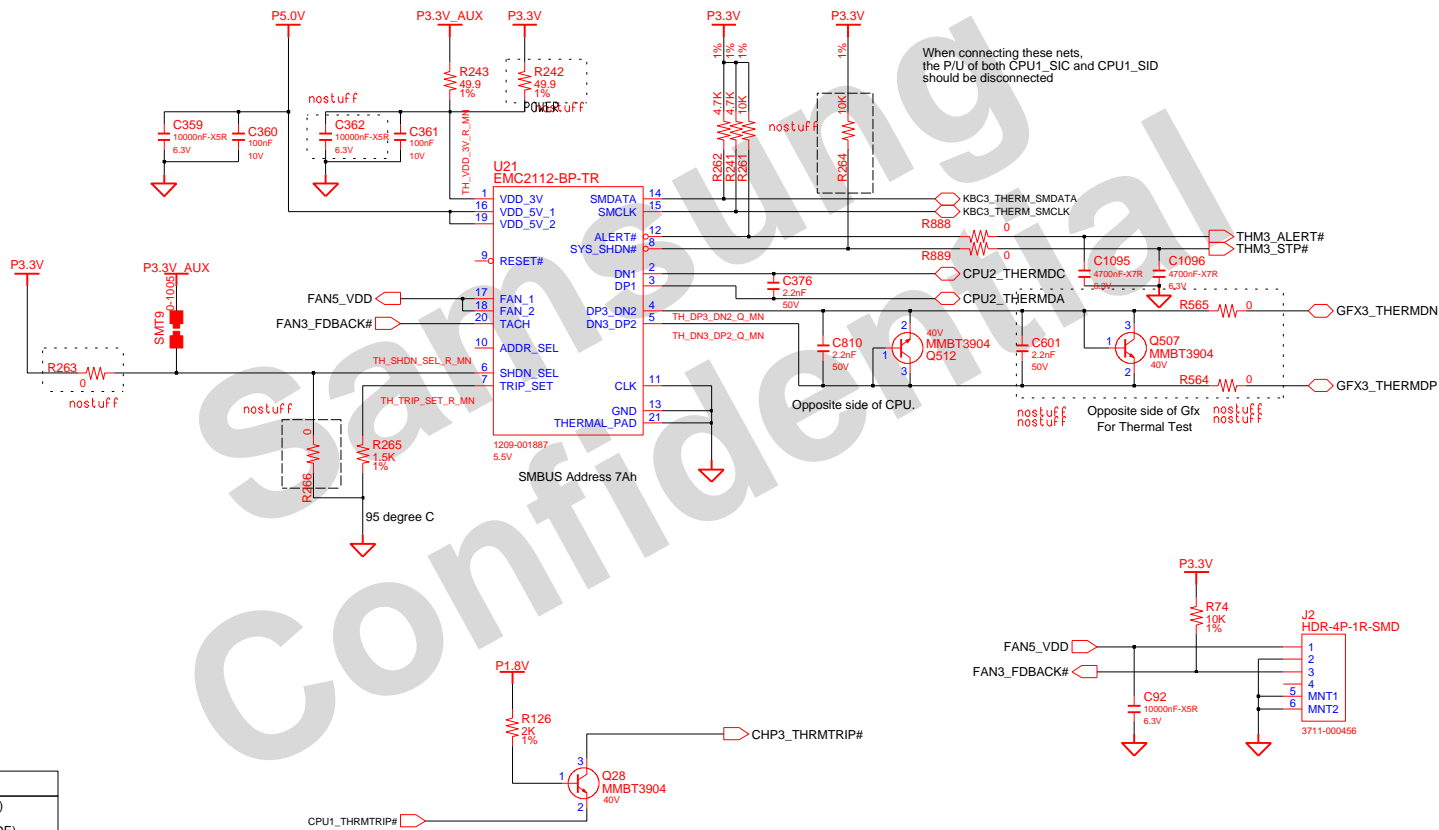


DRAW	H.J.Ra	DATE	08/18/2009	TITLE	Bremen-D MAIN		SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1	CLOCK DISTRIBUTION		PART NO. BA41-xxxxxA	
APPROVAL	H.K.Park	REV	1.1	October 10, 2009 16:50:44 PM		PAGE	7 OF 61
MODULE CODE		LAST EDIT					

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# THERMAL SENSOR & FAN CONTROL

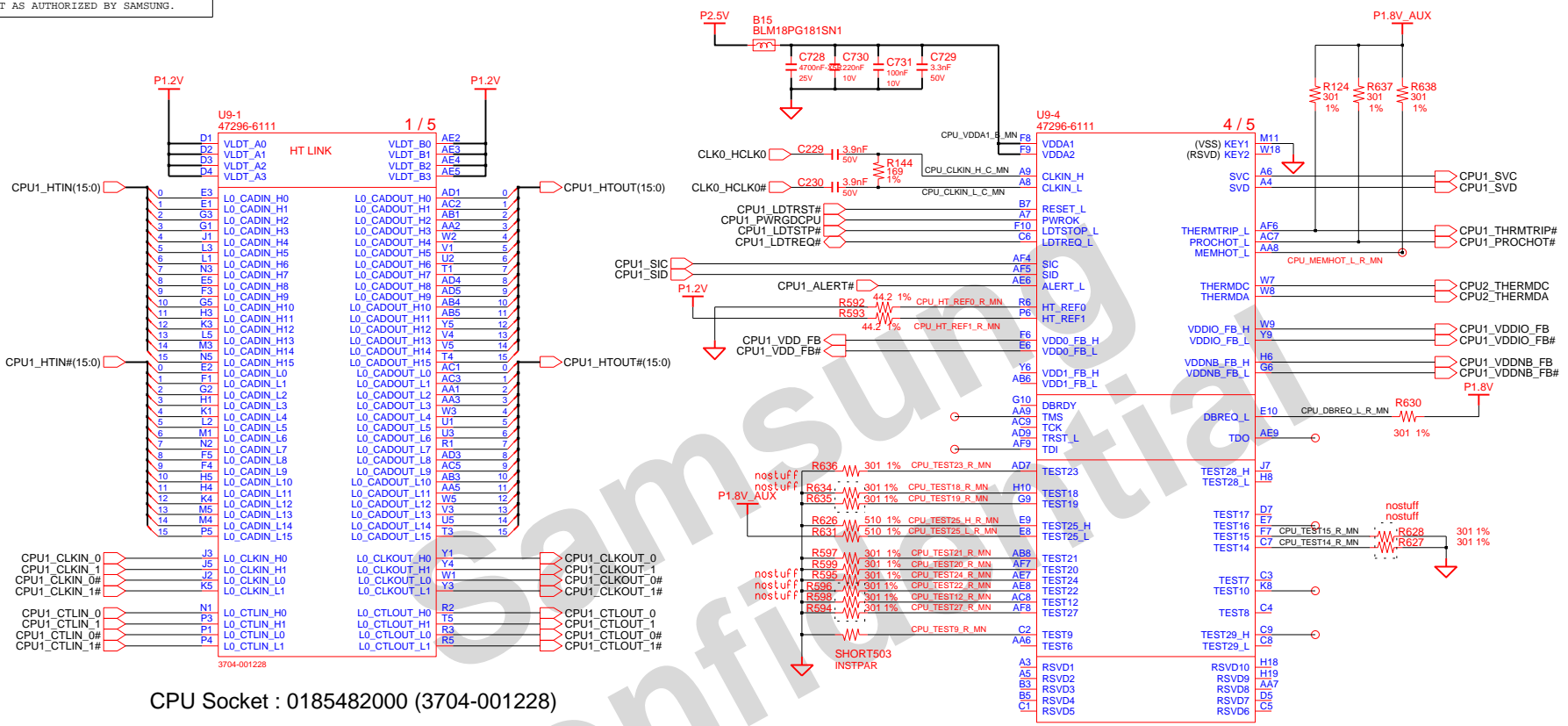


SHDN_SEL MODE	
0	CH1(CPU MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

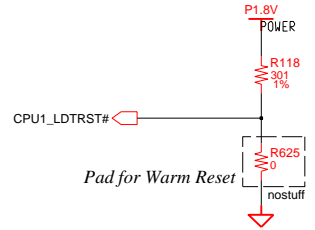
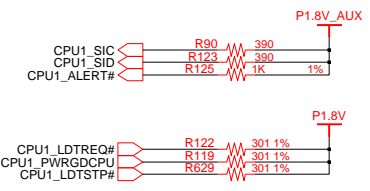
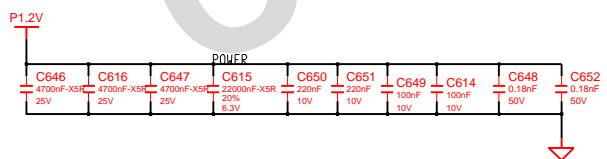
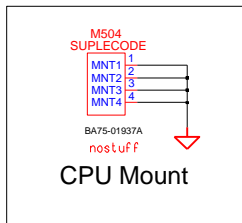
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D THERMAL SENSOR THERMAL SENSOR EMC2112	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE		LAST EDIT				
October 10, 2009 16:50:44 PM						PAGE 8 OF 61

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CPU Socket : 0185482000 (3704-001228)



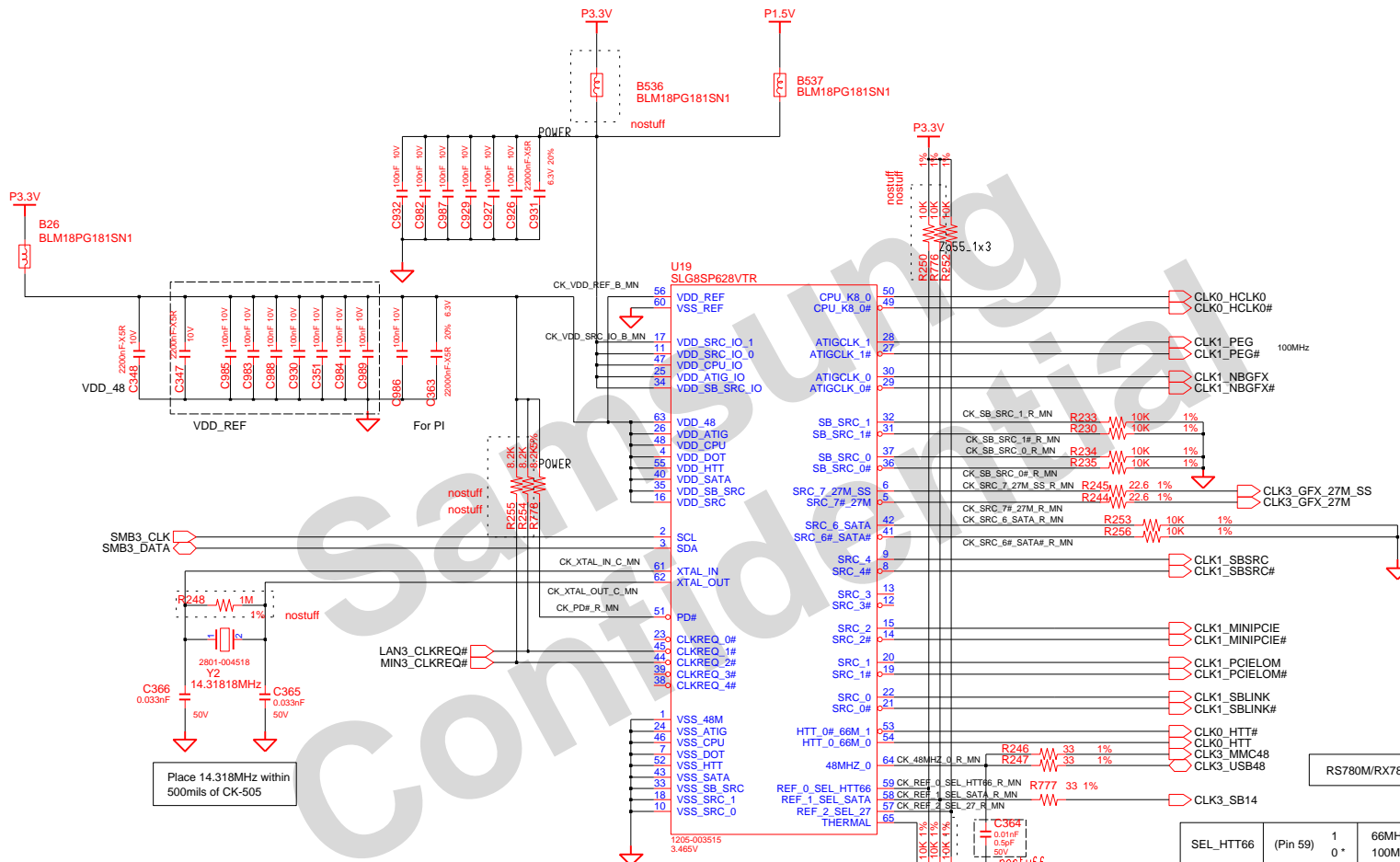
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>CPU</b> <b>Caspian (1/3)</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO: <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT				
October 10, 2009 16:50:44 PM					PAGE	9 OF 61





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Place 14.318MHz within 500mils of CK-505

RS780M/RX781M : 1.1V (OSC\_14MHz)

This part is 64pin QFN package.

SEL_HTT66	(Pin 59)	1	66MHz 3.3V single HTT clock
		0*	100MHz differential clock
SEL_SATA	(Pin 58)	1	SRC6 diff. clock
		0*	100MHz spreading diff. clock
SEL_27M	(Pin 57)	1*	27MHz/27MHz_SS graphics clock
		0	SRC7 diff. clock

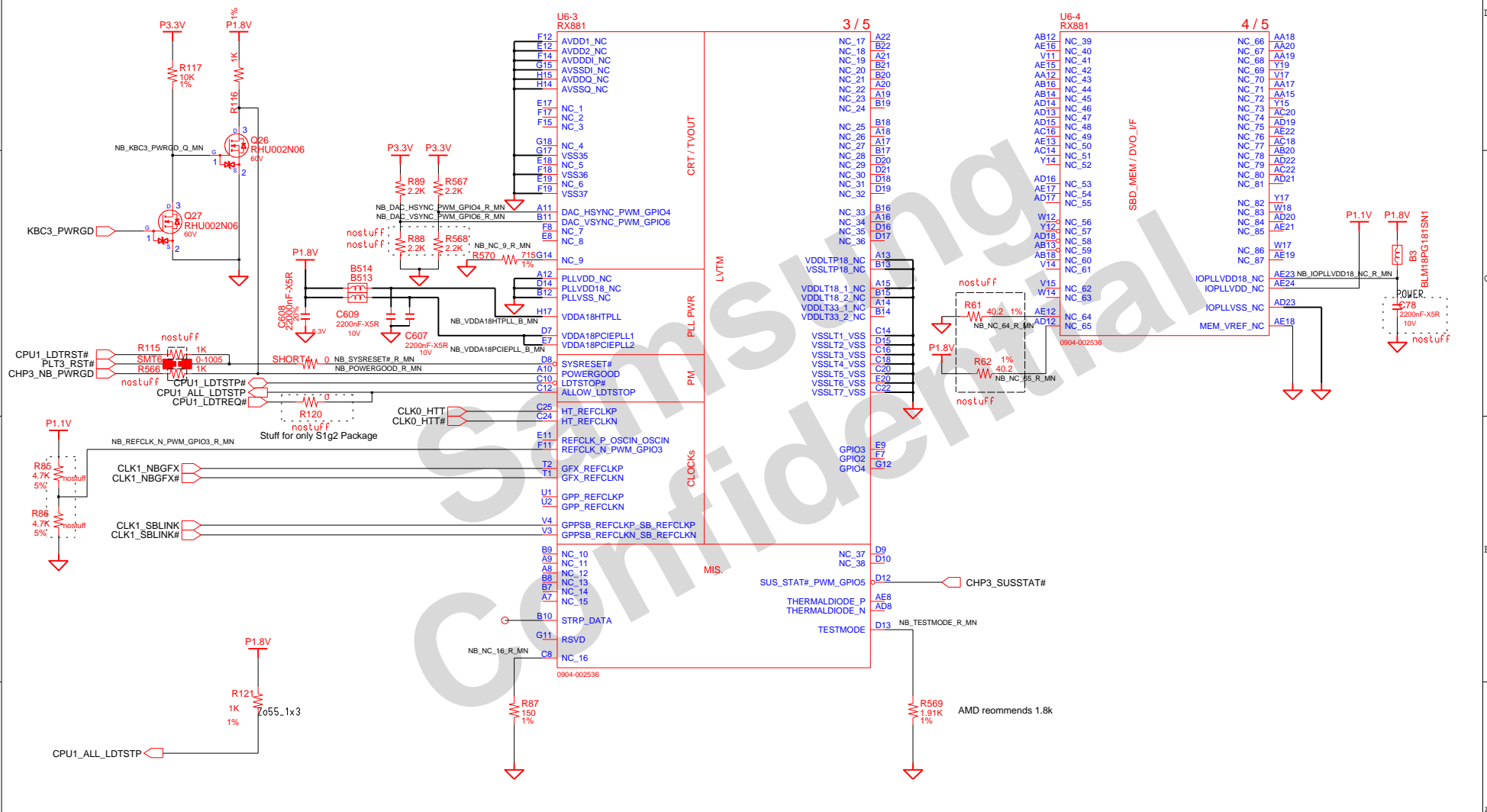
CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	-	-
CLK REQ 4	-	SB_SRC

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>MAIN_CLOCK_CIRCUIT</b> <b>CK_Clock_505M</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO: <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT				
				October 10, 2009 16:50:44 PM		



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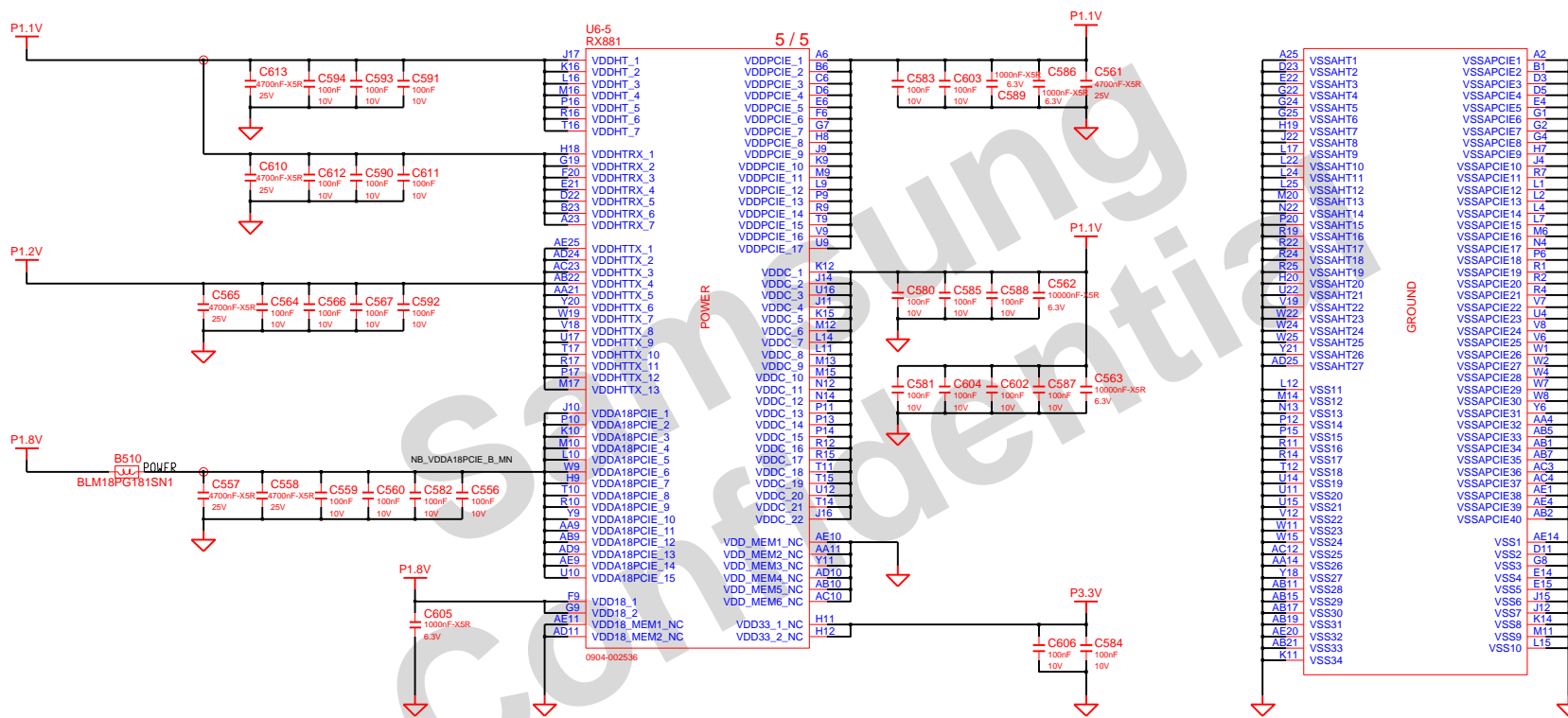
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DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV.STEP	ADV1		MCH_DDR2	
APPROVAL	H.K.Park	REV	1.1		RX881 (2/3)	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	14	OF 61

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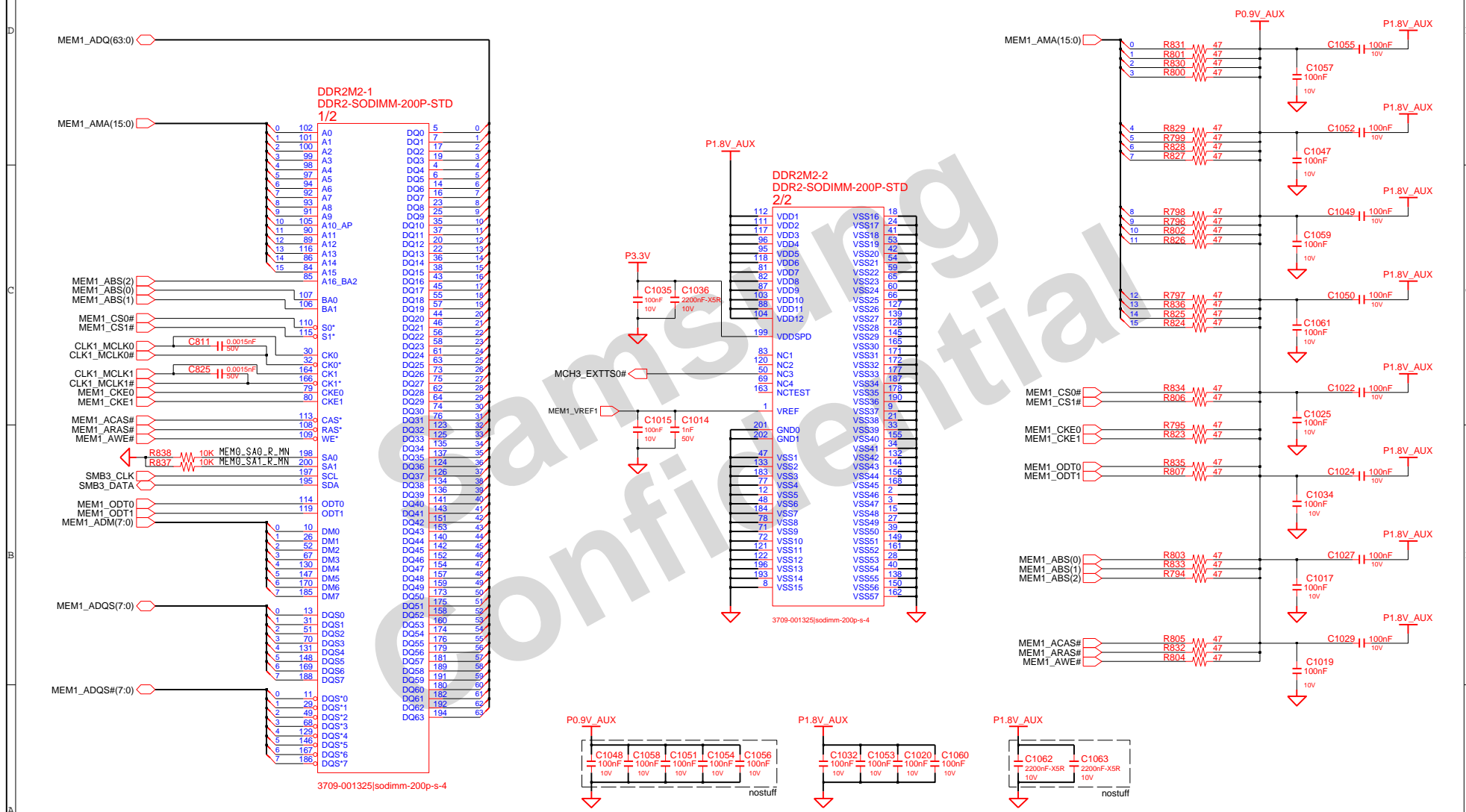


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MCH_DDR2 RX881 (3/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
October 10, 2009 16:50:44 PM						PAGE 15 OF 61

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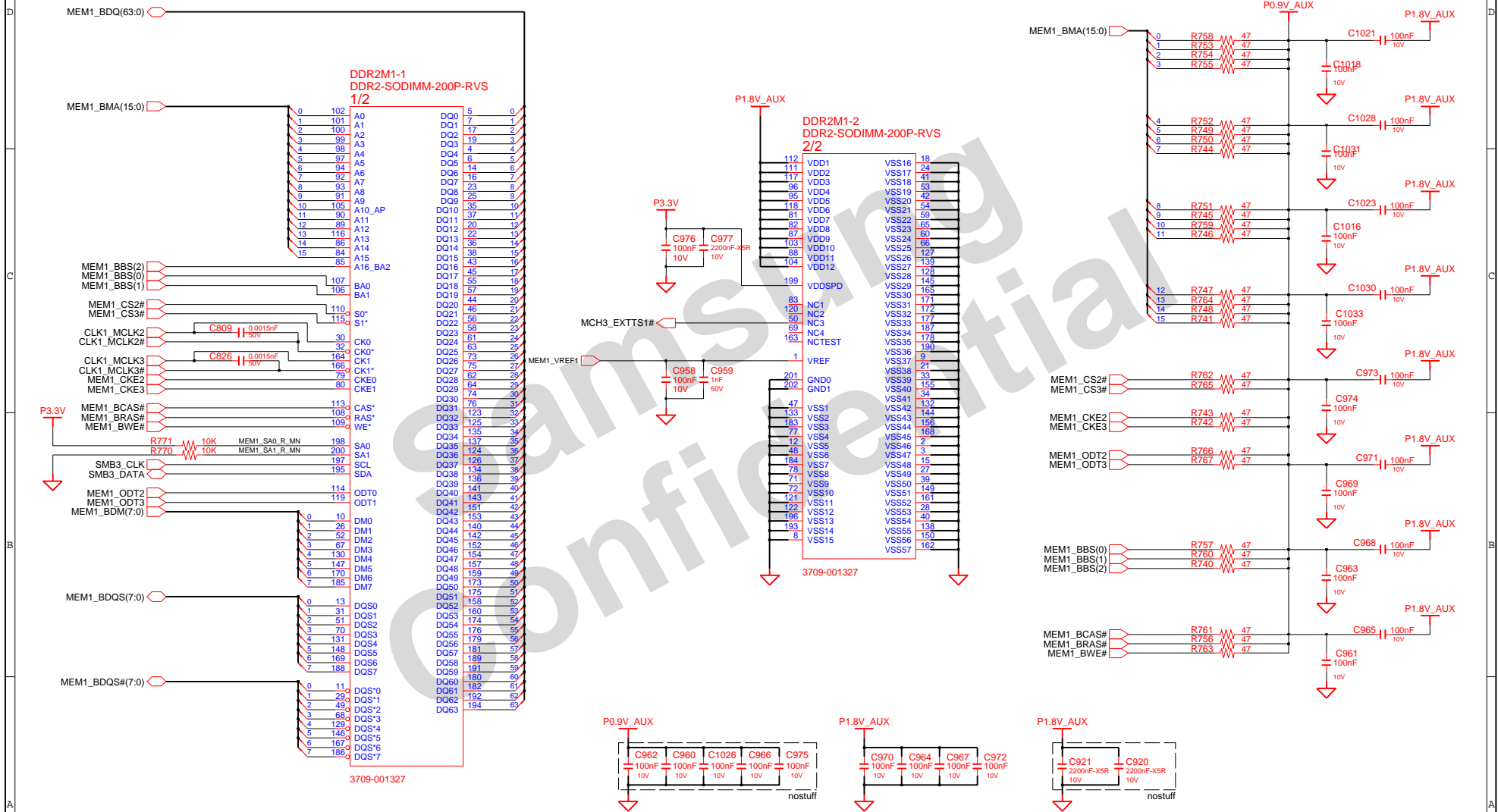
**DDR SO-DIMM #0**



DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1	SODIMM_DDR2		
APPROVAL	H.K.Park	REV	1.1	SODIMM_DDR2 (1/2)		
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM		
				PAGE	16	OF 61

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**DDR SO-DIMM #1**

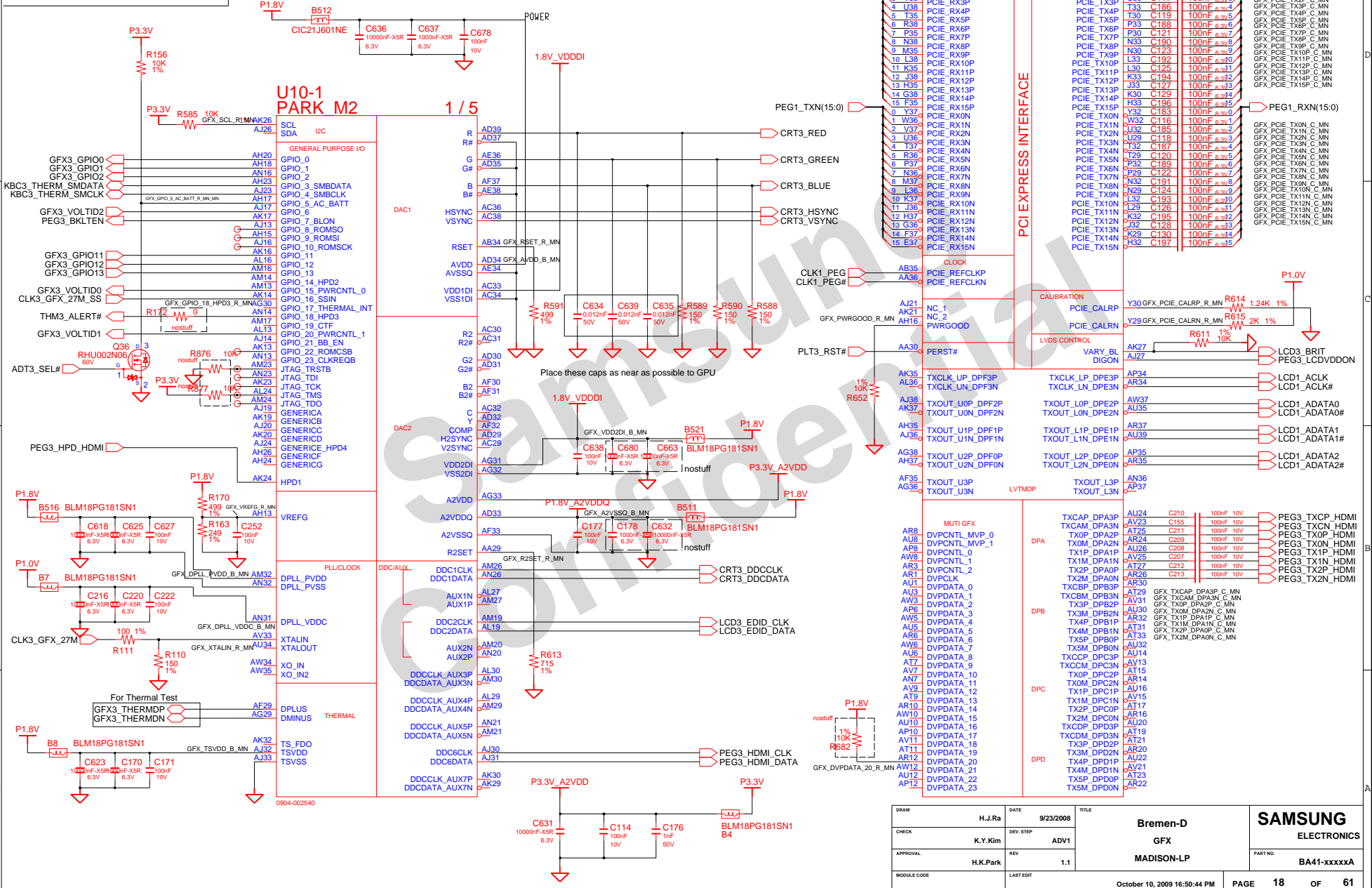


Place near SO-DIMM1

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>SODIMM_DDR2</b> <b>SOCIMM_DDR2 (2/2)</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
October 10, 2009 16:50:44 PM					PAGE	17 OF 61

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DRAW	H.J.Ra	DATE	9/23/2008	TITLE
CHECK	K.Y.Kim	DEV.STEP	ADV1	
APPROVAL	H.K.Park	REV	1.1	
MODULE CODE		LAST EDIT		

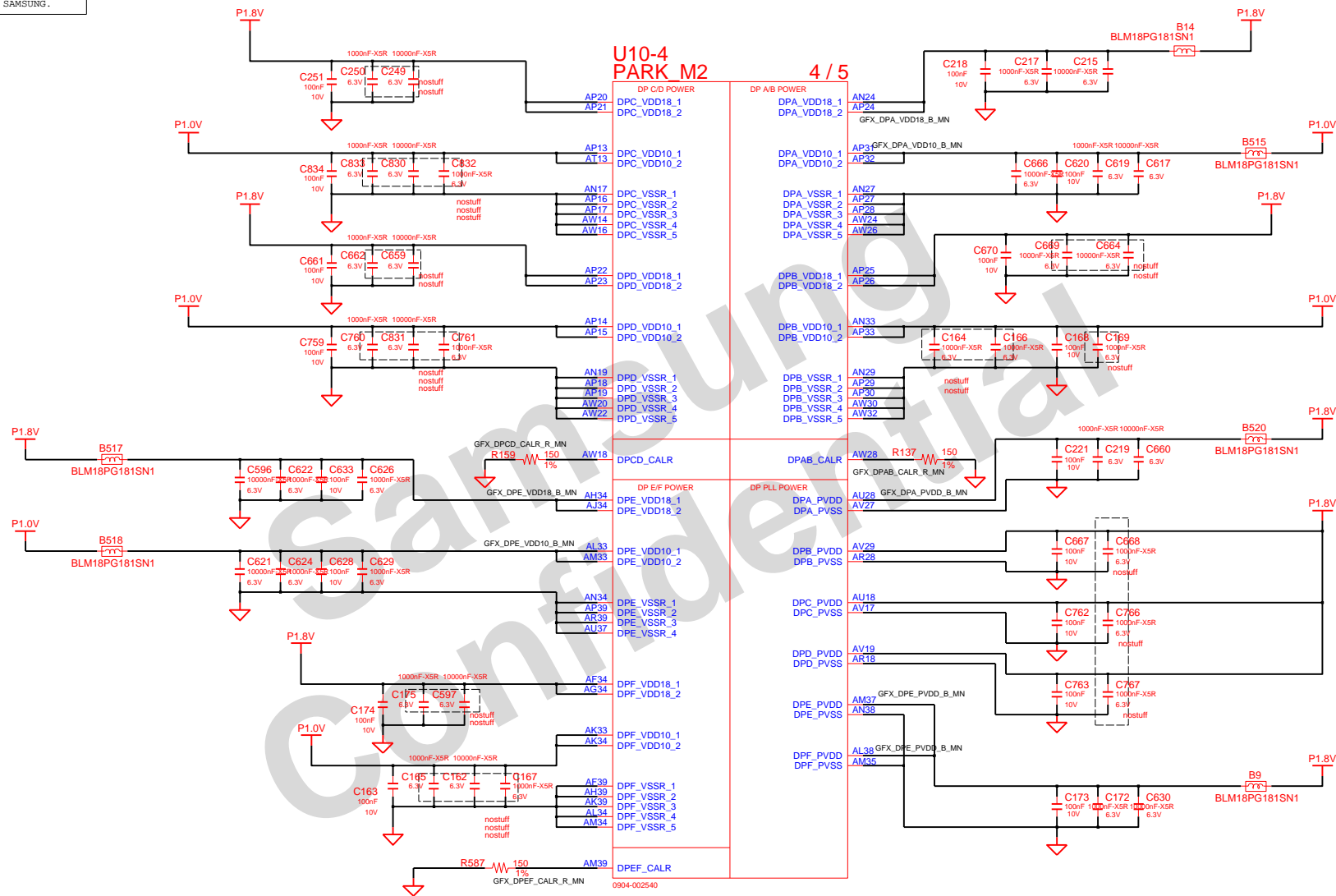
<b>Bremen-D</b>	<b>GFX</b>
<b>MADISON-LP</b>	
October 10, 2009 16:50:44 PM	PAGE 18 OF 61

<b>SAMSUNG</b>	
ELECTRONICS	
PART NO.	BA41-xxxxxA



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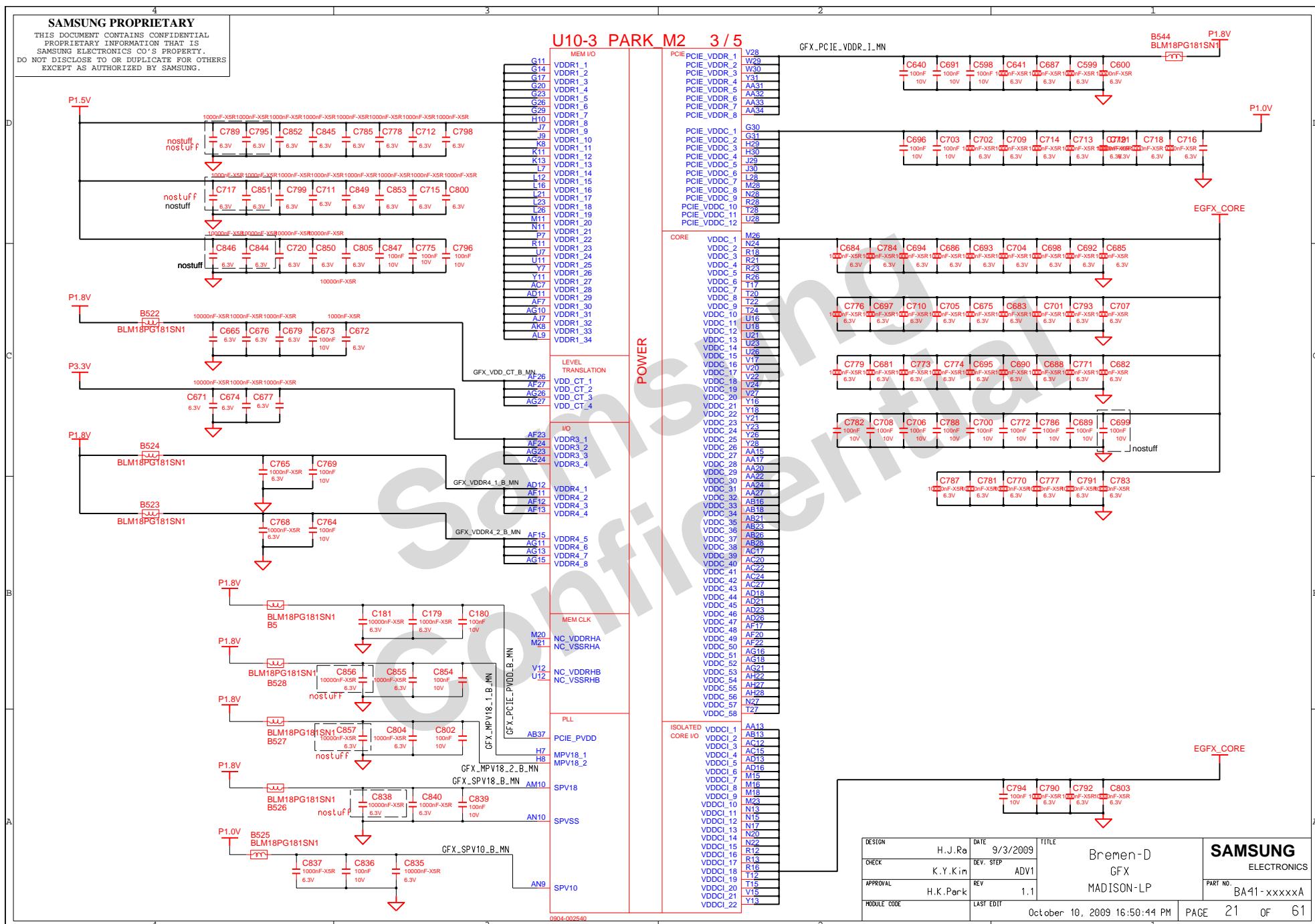


DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GFX MADISON-LP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	20 OF 61	

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U10-3 PARK M2 3/5



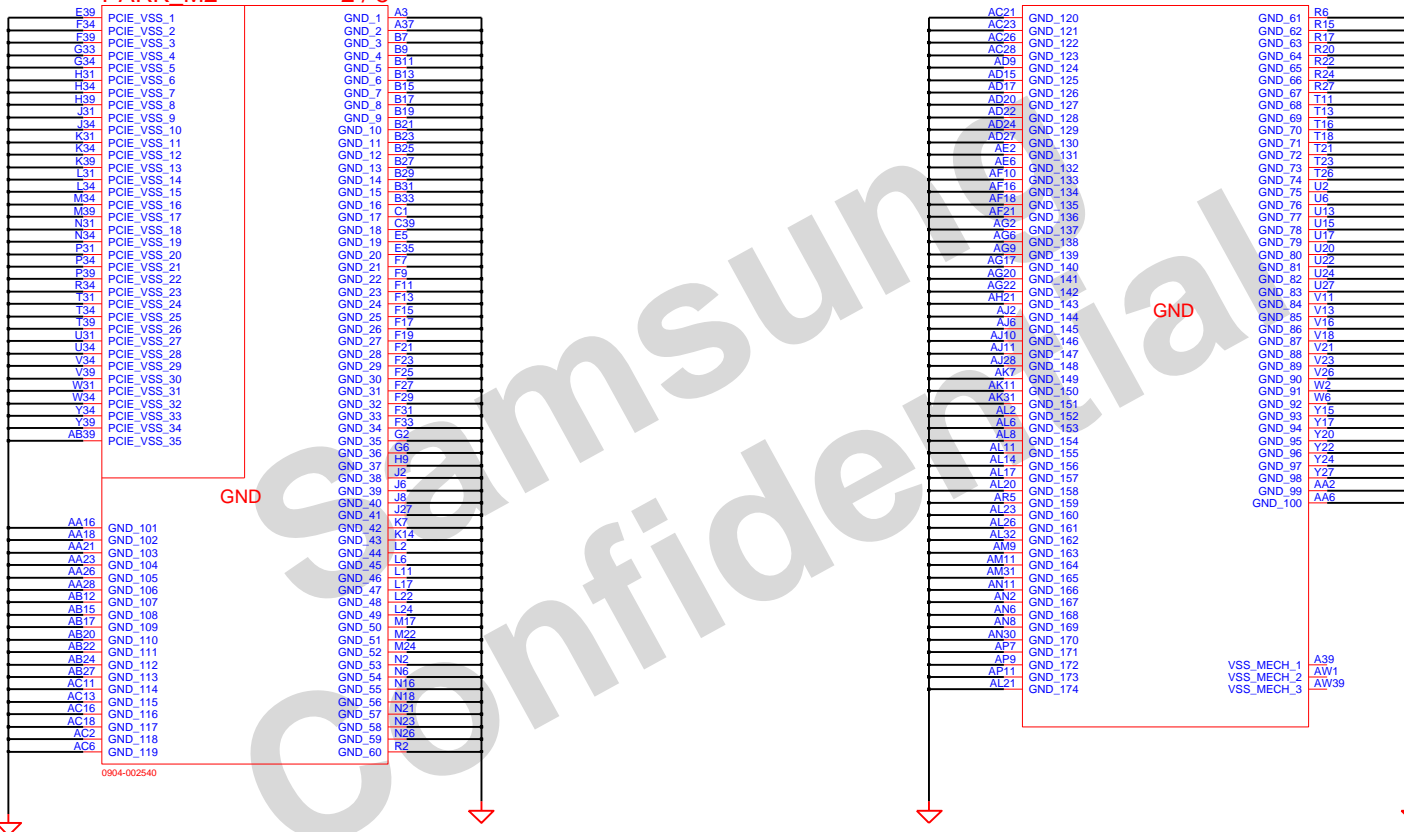
- MEM I/O
  - G11 VDDR1\_1
  - G14 VDDR1\_2
  - G17 VDDR1\_3
  - G20 VDDR1\_4
  - G23 VDDR1\_5
  - G26 VDDR1\_6
  - G29 VDDR1\_7
  - H10 VDDR1\_8
  - J7 VDDR1\_9
  - K8 VDDR1\_10
  - K11 VDDR1\_11
  - K13 VDDR1\_12
  - L7 VDDR1\_14
  - L12 VDDR1\_15
  - L21 VDDR1\_16
  - L23 VDDR1\_18
  - L26 VDDR1\_19
  - M11 VDDR1\_20
  - N11 VDDR1\_21
  - P7 VDDR1\_22
  - R11 VDDR1\_23
  - J7 VDDR1\_24
  - L11 VDDR1\_25
  - Y7 VDDR1\_26
  - Y11 VDDR1\_27
  - AC7 VDDR1\_28
  - AD11 VDDR1\_29
  - AF7 VDDR1\_30
  - AG10 VDDR1\_31
  - AJ7 VDDR1\_32
  - AK8 VDDR1\_33
  - AL9 VDDR1\_34
- POWER
  - LEVEL TRANSLATION
    - AF26 VDD\_CT\_1
    - AF27 VDD\_CT\_2
    - AG26 VDD\_CT\_3
    - AG27 VDD\_CT\_4
  - IO
    - AF23 VDDR3\_1
    - AF24 VDDR3\_2
    - AG23 VDDR3\_3
    - AG24 VDDR3\_4
  - MEM CLK
    - AD12 VDDR4\_1
    - AE11 VDDR4\_2
    - AF12 VDDR4\_3
    - AF13 VDDR4\_4
  - PLL
    - AF15 VDDR4\_5
    - AG11 VDDR4\_6
    - AG13 VDDR4\_7
    - AG15 VDDR4\_8
  - ISOLATED CORE I/O
    - AA13 VDDCI\_1
    - AB13 VDDCI\_2
    - AC12 VDDCI\_3
    - AC12 VDDCI\_4
    - AC15 VDDCI\_5
    - AD13 VDDCI\_6
    - AD16 VDDCI\_7
    - M15 VDDCI\_8
    - M16 VDDCI\_9
    - M18 VDDCI\_10
    - M23 VDDCI\_11
    - N13 VDDCI\_12
    - N15 VDDCI\_13
    - N17 VDDCI\_14
    - N20 VDDCI\_15
    - R12 VDDCI\_16
    - R13 VDDCI\_17
    - R16 VDDCI\_18
    - T12 VDDCI\_19
    - T15 VDDCI\_20
    - V15 VDDCI\_21
    - Y13 VDDCI\_22

DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GFX	<b>SAMSUNG</b> ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		MADISON-LP	
APPROVAL	H.K.Park	REV	1.1			PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	21	OF 61

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U10-2  
 PARK M2 2 / 5



DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GFX MADISON-LP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	22 OF 61	

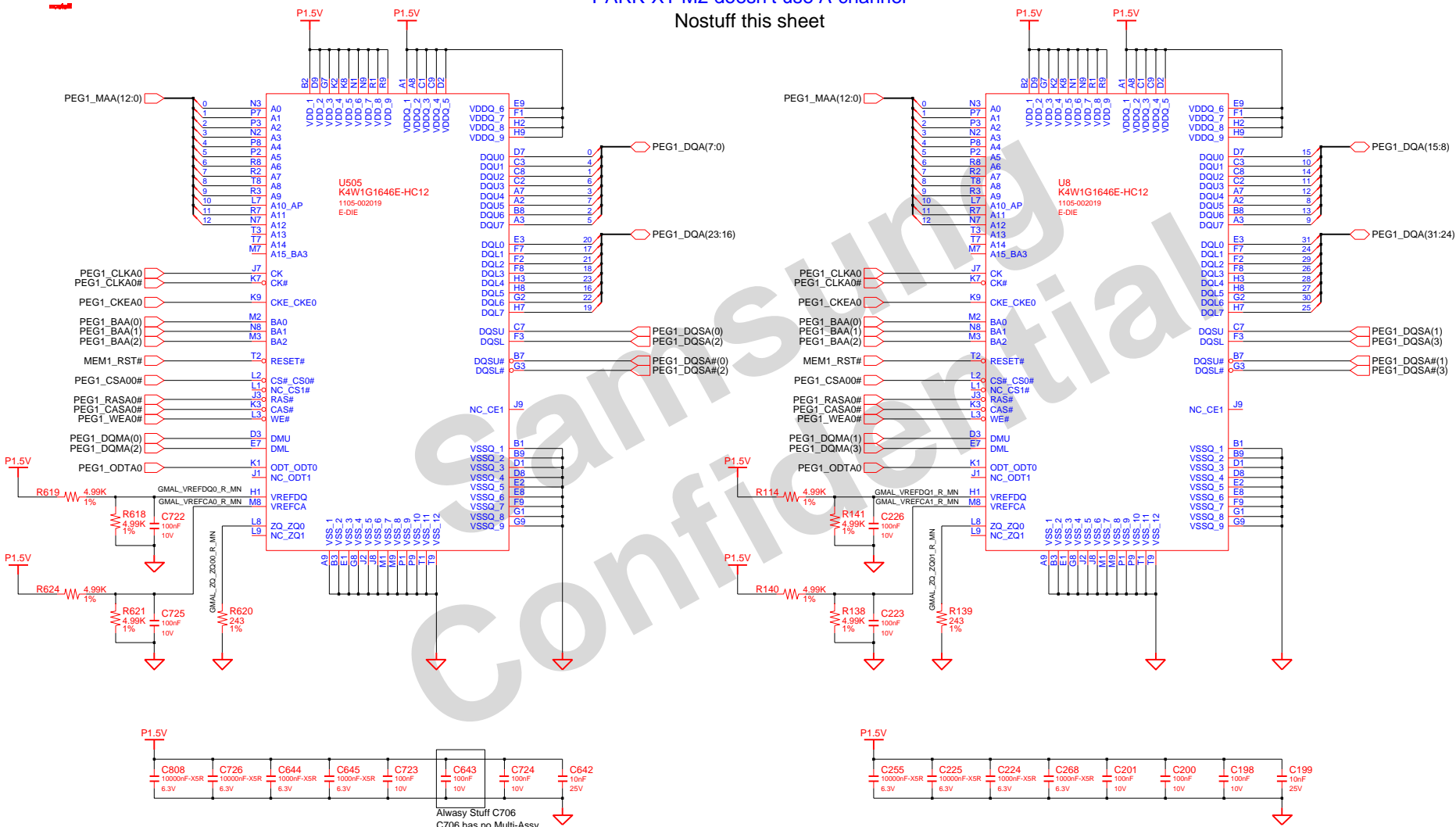
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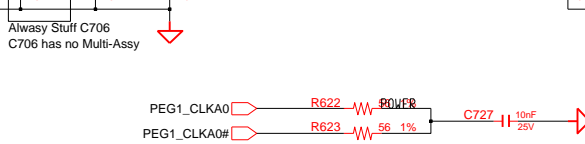
# A-channel Lower Data

PARK-XT M2 doesn't use A-channel

Nostuff this sheet



Confidential



DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1	GRAPHICS MEMORY	
APPROVAL	H.K.Park	REV	1.1	gDDR3	
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	23 OF 61

**SAMSUNG**  
ELECTRONICS  
PART NO. BA41-xxxxxA

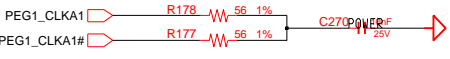
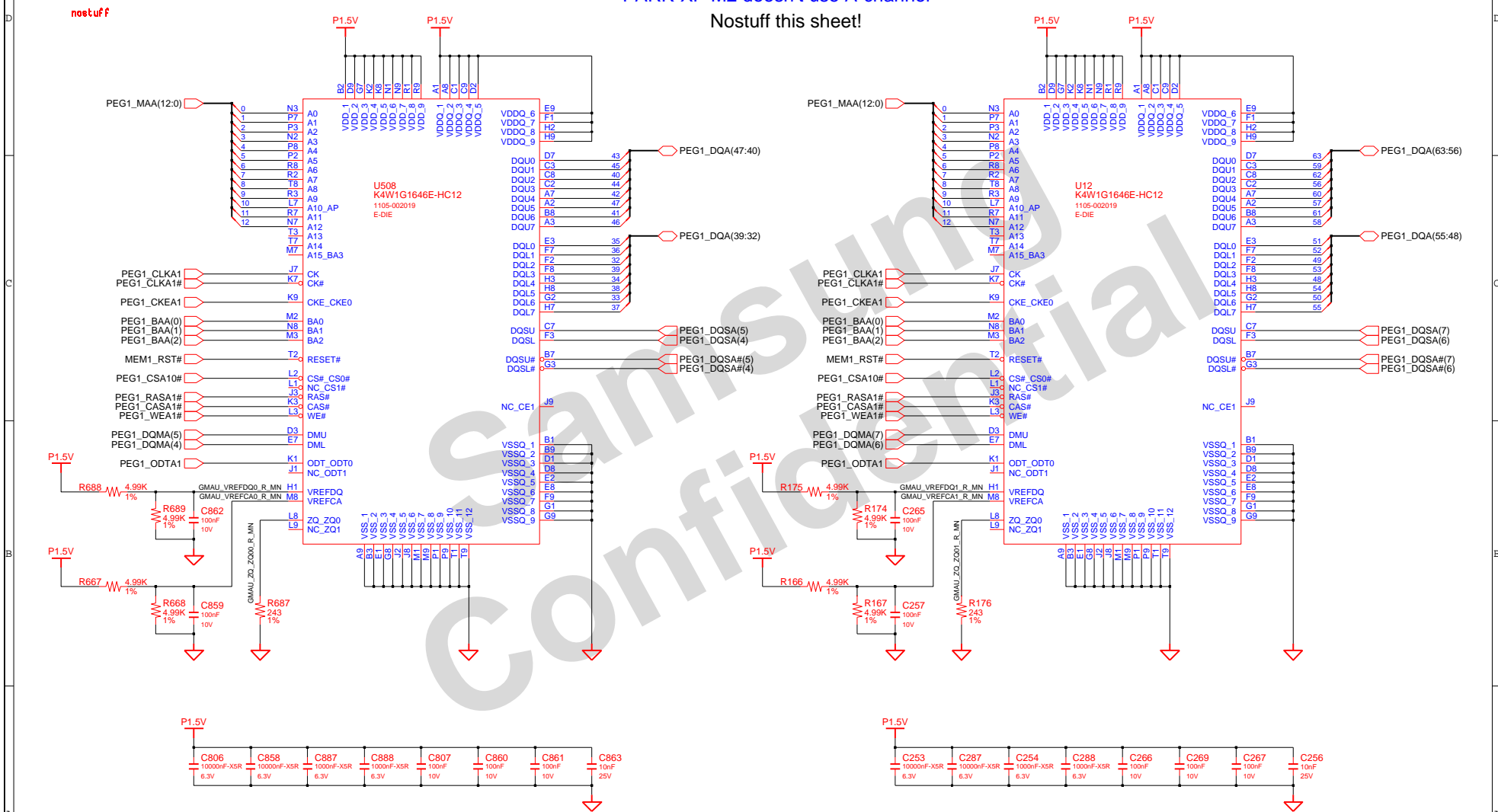
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# A-channel Upper Data

PARK-XP M2 doesn't use A-channel

Nostuff this sheet!



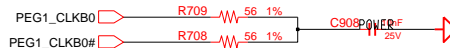
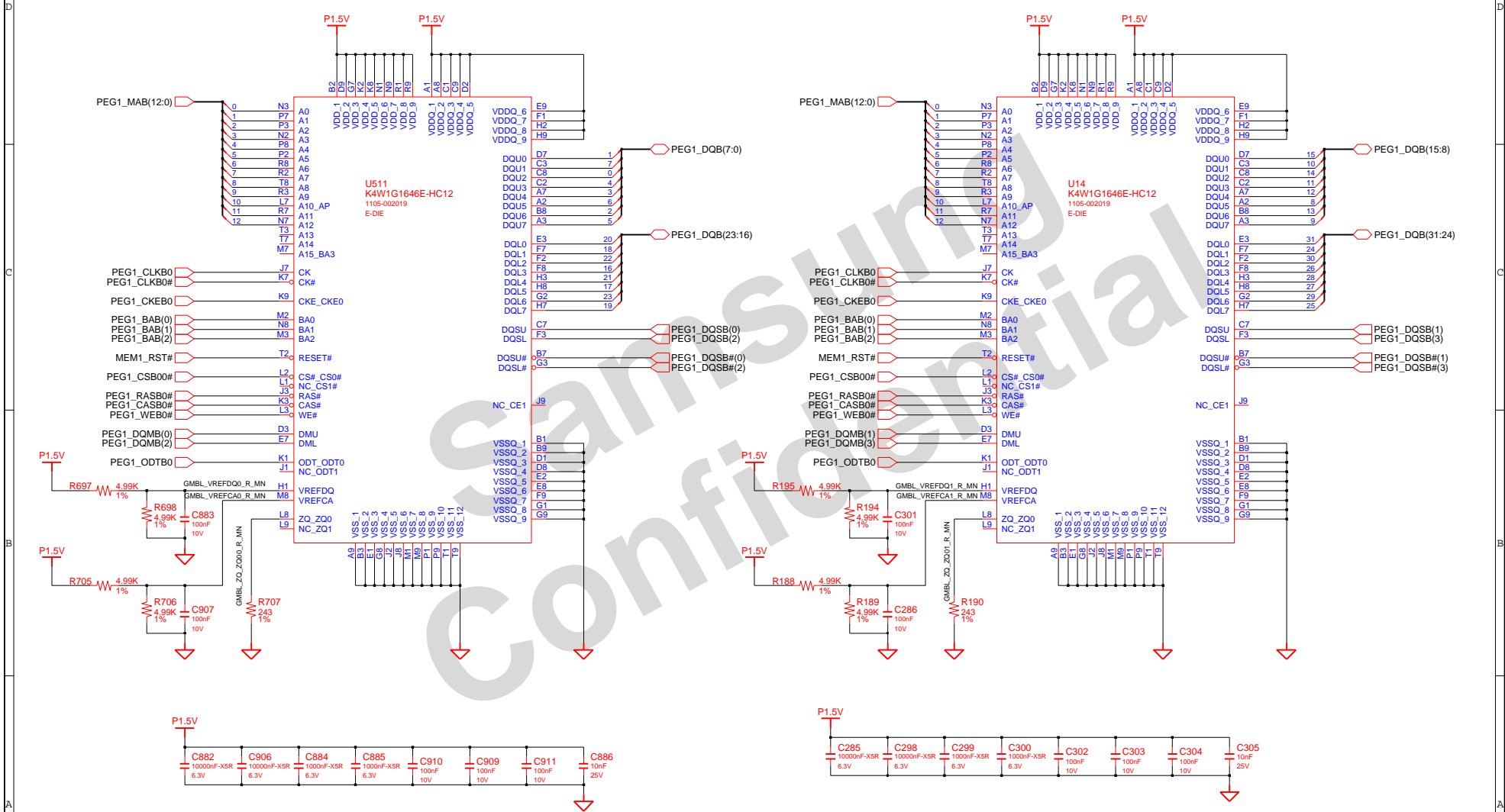
DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D
CHECK	K.Y.Kim	DEV. STEP	ADV1		GRAPHICS MEMORY
APPROVAL	H.K.Park	REV	1.1		gDDR3
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	24 OF 61

**SAMSUNG**  
ELECTRONICS  
PART NO. BA41-xxxxxA

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# B-channel Lower Data

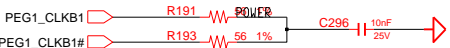
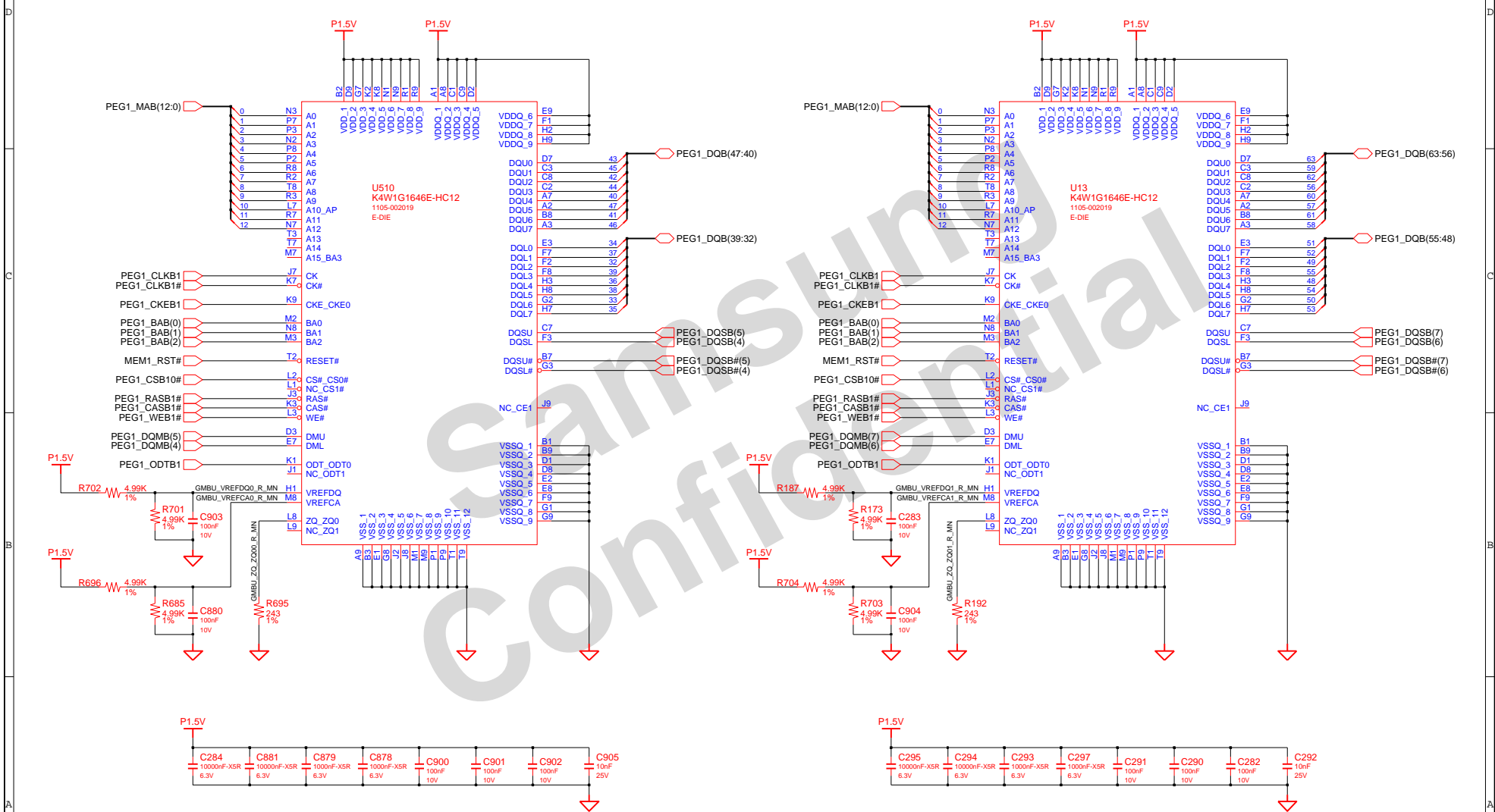


DESIGN	H.J.R	DATE	9/3/2009	TITLE	Bremen-D GTAPHICS MEMORY gDDR3	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	25 OF 61	

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# B-channel Upper Data



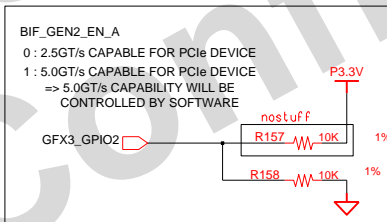
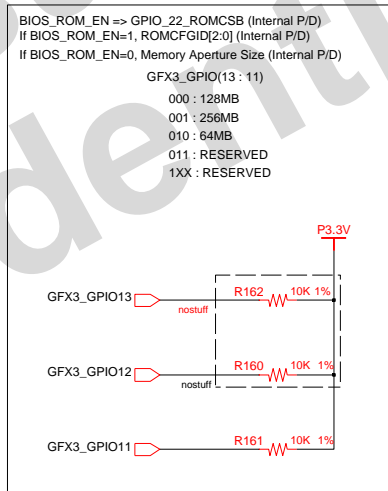
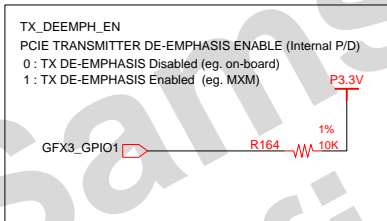
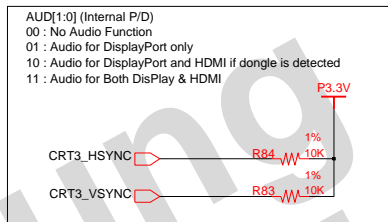
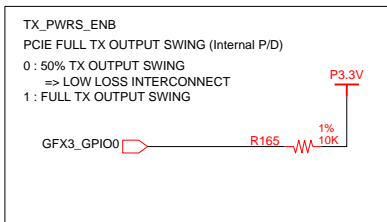
DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GRAPHICS MEMORY gDDR3
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	26 OF 61

<b>SAMSUNG</b> ELECTRONICS
PART NO. BA41-xxxxxA

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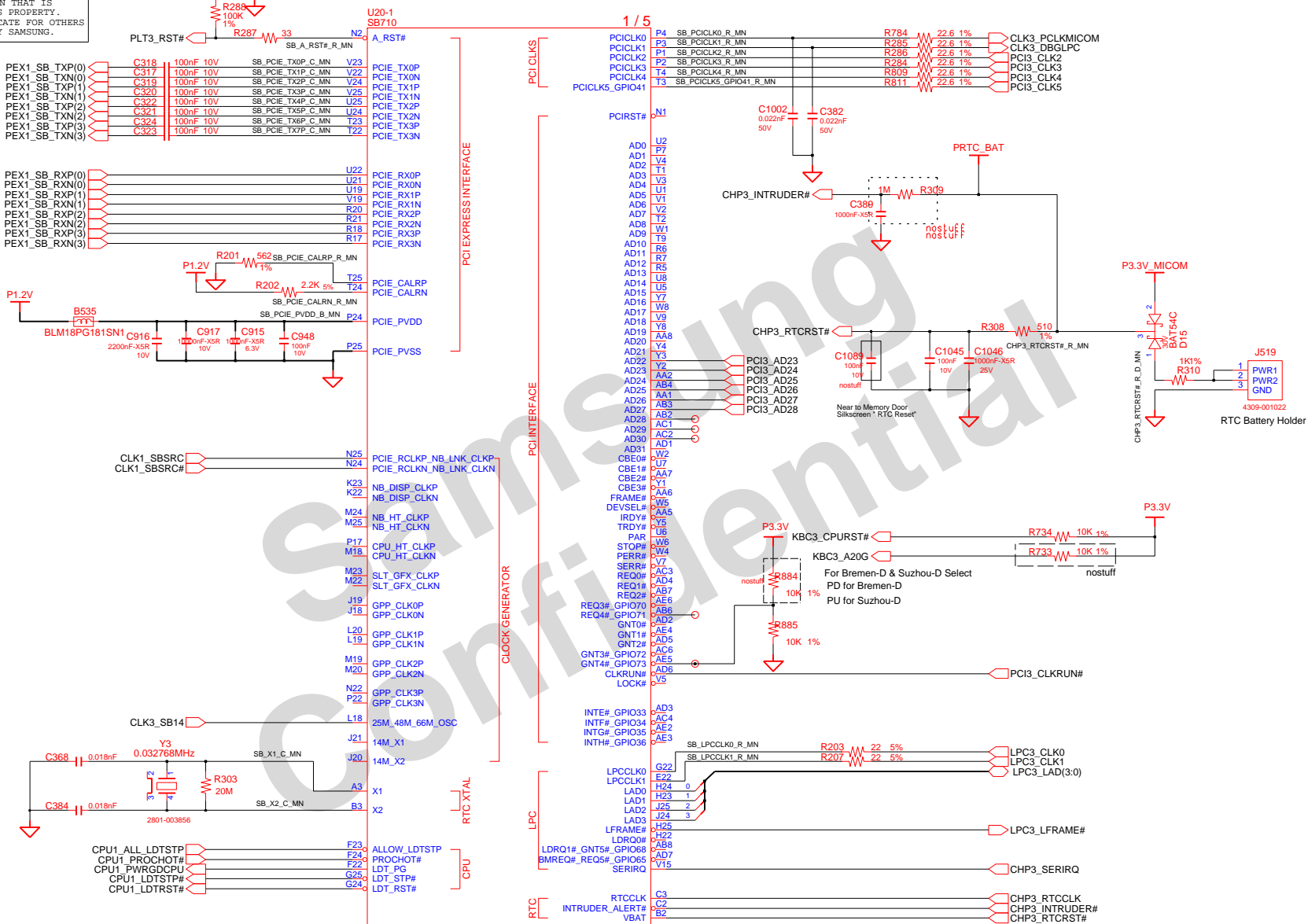
## Park XT Straps



DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D GFX MADISON-LP	<b>SAMSUNG</b> ELECTRONICS	
CHECK	K.Y.Kim	DEV. STEP	ADV1	PART NO.			BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1	PAGE			27 OF 61
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM				

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0904-002534

DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D ICH SB710 (1/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	28 OF 61	

**SAMSUNG PROPRIETARY**

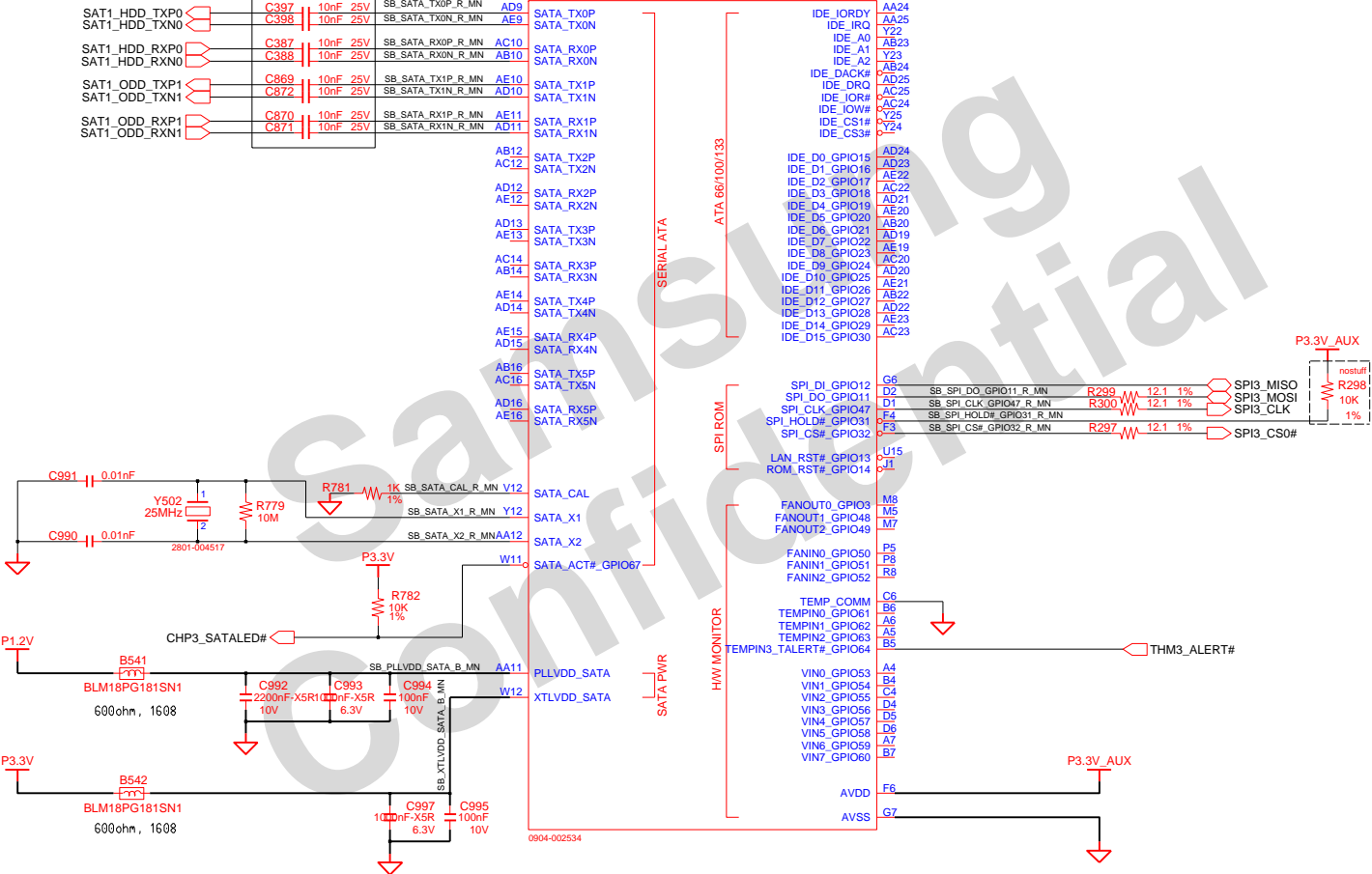
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Rout to connector side closely

SAT1_HDD_TXP0	C397	10nF	25V	SB_SATA_TX0P_R_MN	AD9
SAT1_HDD_TXN0	C398	10nF	25V	SB_SATA_TX0N_R_MN	AE9
SAT1_HDD_RXP0	C387	10nF	25V	SB_SATA_RX0P_R_MN	AC10
SAT1_HDD_RXN0	C388	10nF	25V	SB_SATA_RX0N_R_MN	AB10
SAT1_ODD_TXP1	C869	10nF	25V	SB_SATA_TX1P_R_MN	AE10
SAT1_ODD_TXN1	C872	10nF	25V	SB_SATA_TX1N_R_MN	AD10
SAT1_ODD_RXP1	C870	10nF	25V	SB_SATA_RX1P_R_MN	AE11
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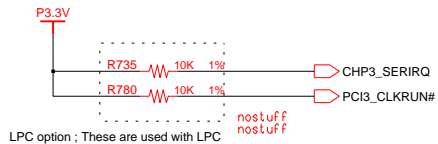
U20-2  
SB710

2/5



P3.3V\_AUX

nostuff	R298	10K
1%		



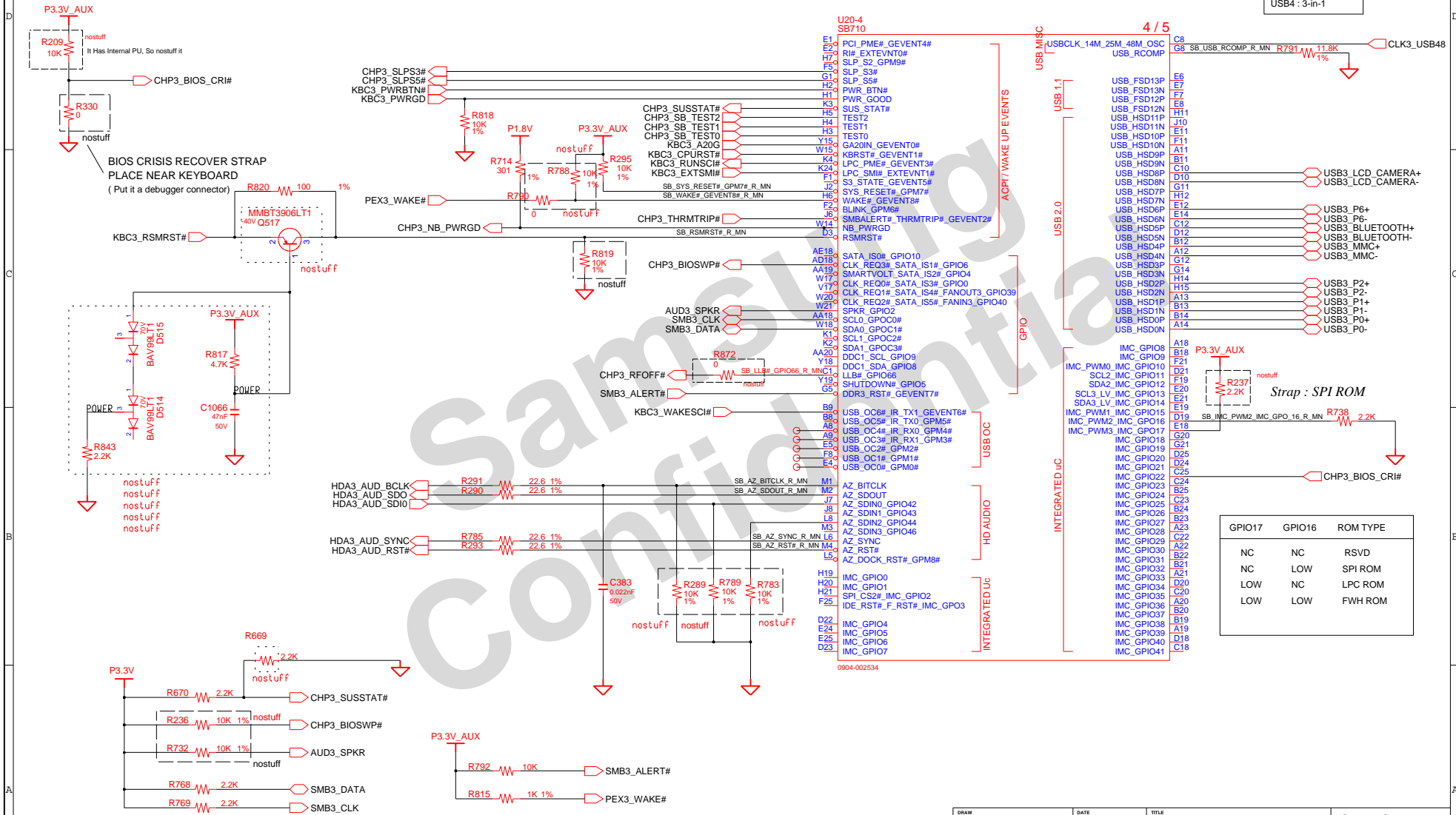
LPC option ; These are used with LPC

DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D ICH SB710 (2/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	29 OF 61	

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USB1\_6 : Right Port  
 USB0 : Left Port  
 USB5 : Bluetooth  
 USB8 : Camera  
 USB4 : 3-in-1

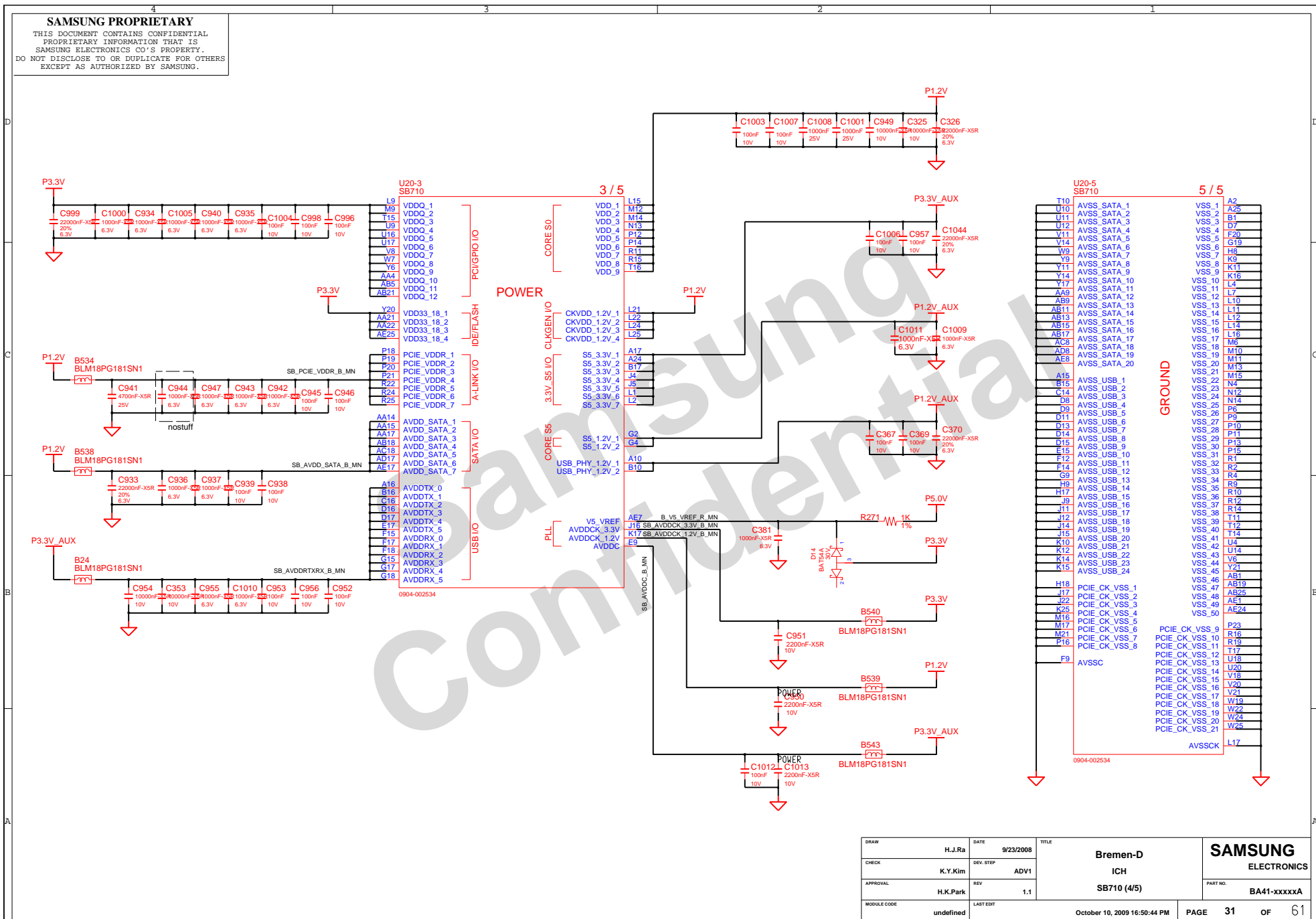


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D ICH SB710 (3/5)
CHECK	K.Y.Kim	DEV. STEP	ADV1		
APPROVAL	H.K.Park	REV	1.1		
MODULE CODE		LAST EDIT			

October 10, 2009 16:50:44 PM PAGE 30 OF 61

**SAMSUNG PROPRIETARY**

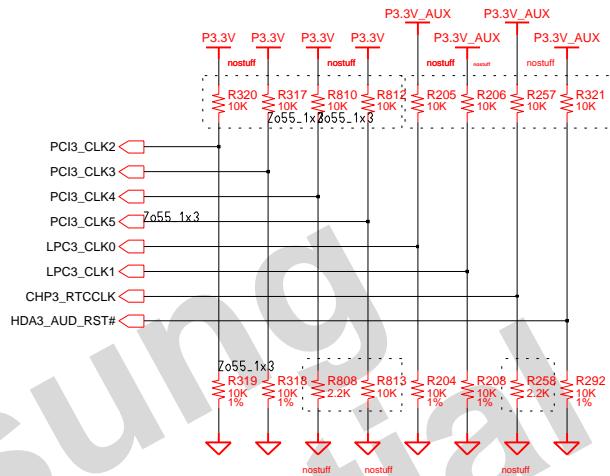
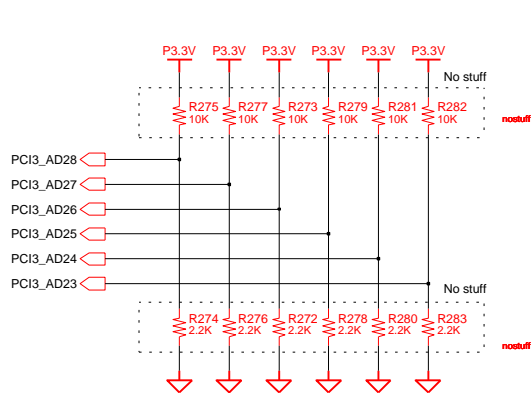
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DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D ICH SB710 (4/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE 31 OF 61	

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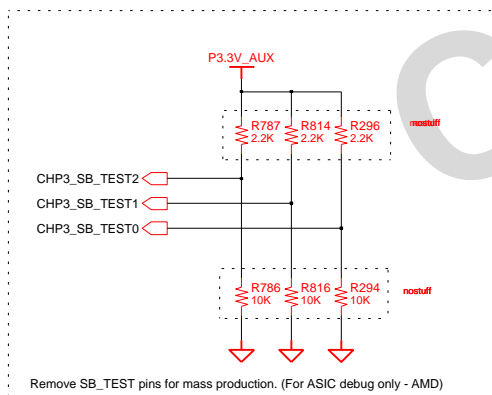
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**DEBUG STRAPS**

STRAP HIGH	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED	
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

STRAP HIGH	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT	
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



Remove SB\_TEST pins for mass production. (For ASIC debug only - AMD)

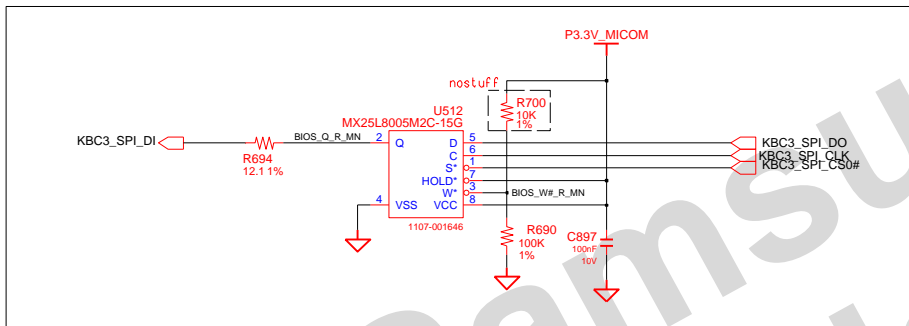
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>ICH</b> <b>SB710 STRAPS (5/5)</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO: <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE 32 OF 61		

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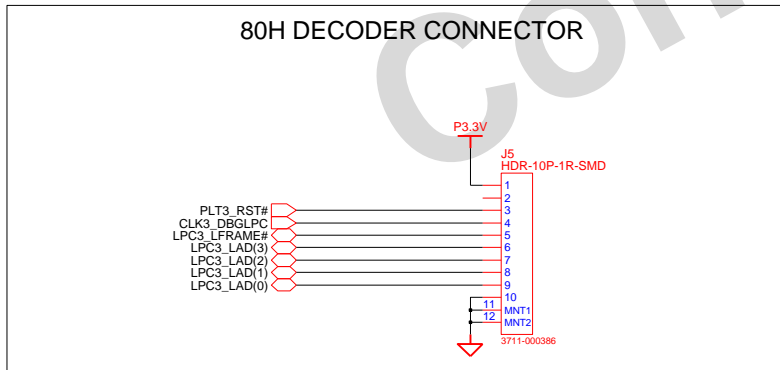
# SPI\_BIOS\_ROM

8MBit

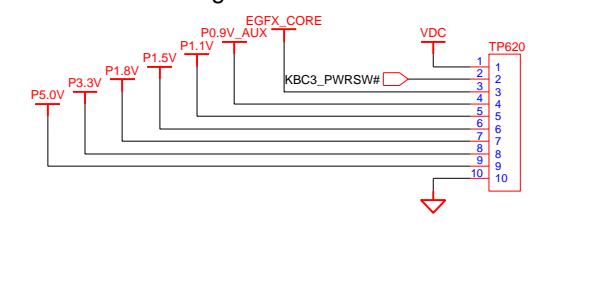


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT SYSTEM HW	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0C	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0E	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0F	INIT I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
10	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
11	INIT_POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
12	LOAD ALTERNATE REG	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT ON-BOARD I/O PORT
	WITH INITIAL POST VALUE	88	INIT BIOS DATA ROM
14	INIT_KEYBOARD CONTROLLER	8A	INIT EXTENDED BIOS DATA AREA
16	CHECK CHECKSUM	8C	INIT_FDD CONTROLLER
18	8254 TIMER INIT	8E	SHADOW OPTION ROMS
1A	8237 DMA CONTROLLER INIT	9A	SETUP POWER MANAGEMENT
1C	RESET INTERRUPT CONTROLLER	9E	ENABLE H/W INTERRUPT
20	TEST DRAM REFRESH	A0	SET TIME OF DAY
22	TEST 8742 KEYBOARD CONTROLLER	A4	INIT_TYPEMATIC RATE
24	SET ES SEGMENT REG. TO 4GB	A8	ERASE F2 PROMPT
26	ENABLE A20	AA	SCAN FOR F2 KEY STROKE
28	AUTO SIZING DRAM	AC	ENTER SETUP
32	COMPUTE THE CPU SPEED	AE	CLEAR IN POST FLAG
34	TEST CMOS RAM	B0	CHECK FOR ERRORS
38	SHADOW SYSTEM BIOS ROM	E2	POST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B4	ONE BEEP
3C	CONFIGURE ADVANCED CHIPSET REG.	B6	CHECK PASSWORD (OPTION)
3D	LOAD ALTER REG WITH CMOS VALUE	B7	ACPI INIT
42	INIT_INTERRUPT VECTOR	BA	DMI INIT
44	INIT BIOS INTERRUPT	BE	CLEAR SCREEN
46	CHECK ROM COPYRIGHT NOTICE	C0	TRY BOOT WITH INT19
47	INIT_I20 SUPPORT IF INSTALLED	D0	INTERRUPT HANDLER ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D2	UNKNOWN INTERRUPT ERROR
49	INIT PCI BUS AND DEVICE	D4	PENDING INTERRUPT ERROR
4A	INIT_ALL VIDEO BIOS ROM	D6	SHUTDOWN 5
4C	SHADOW VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	DISPLAY CPU TYPE AND SPEED	DA	EXTENDED BLOCK MOVE
52	TEST_KEYBOARD	DC	SHUTDOWN 10
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT_HDD CONTROLLER
5A	DISPLAY *PRESS * SETUP	91	INIT_LOCAL BUS HDD CONTROLLER
5C	TEST RAM GETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

## 80H DECODER CONNECTOR



Pins for ICT FREE  
should be rearranged.



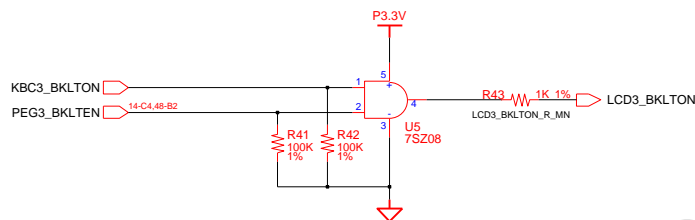
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT				

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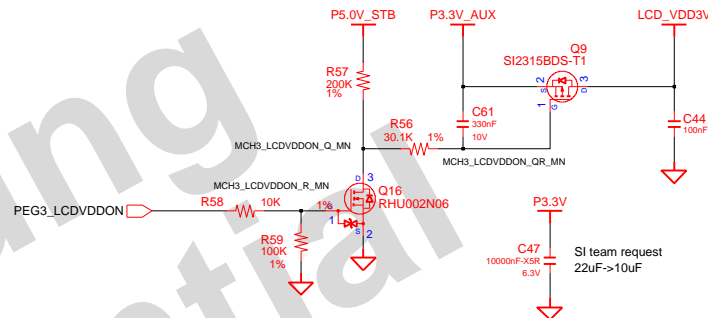
# LVDS

## Backlight On

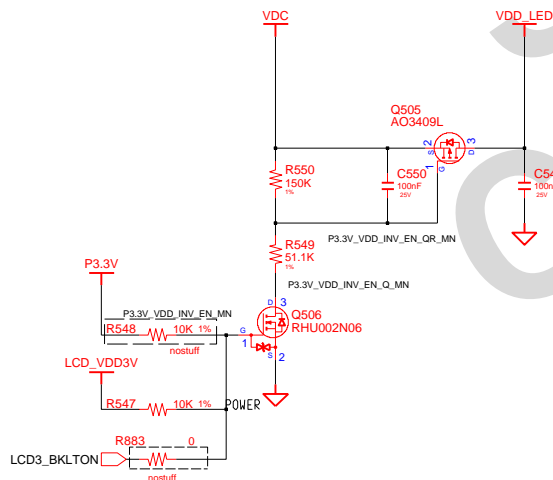


## LCD Power

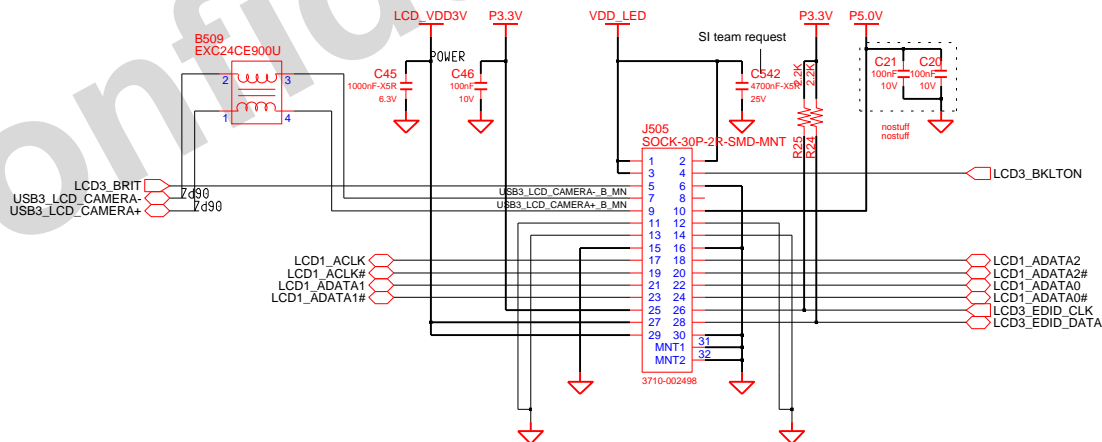
EBL Purpose



## LED Power



## Camera + LCD Connector



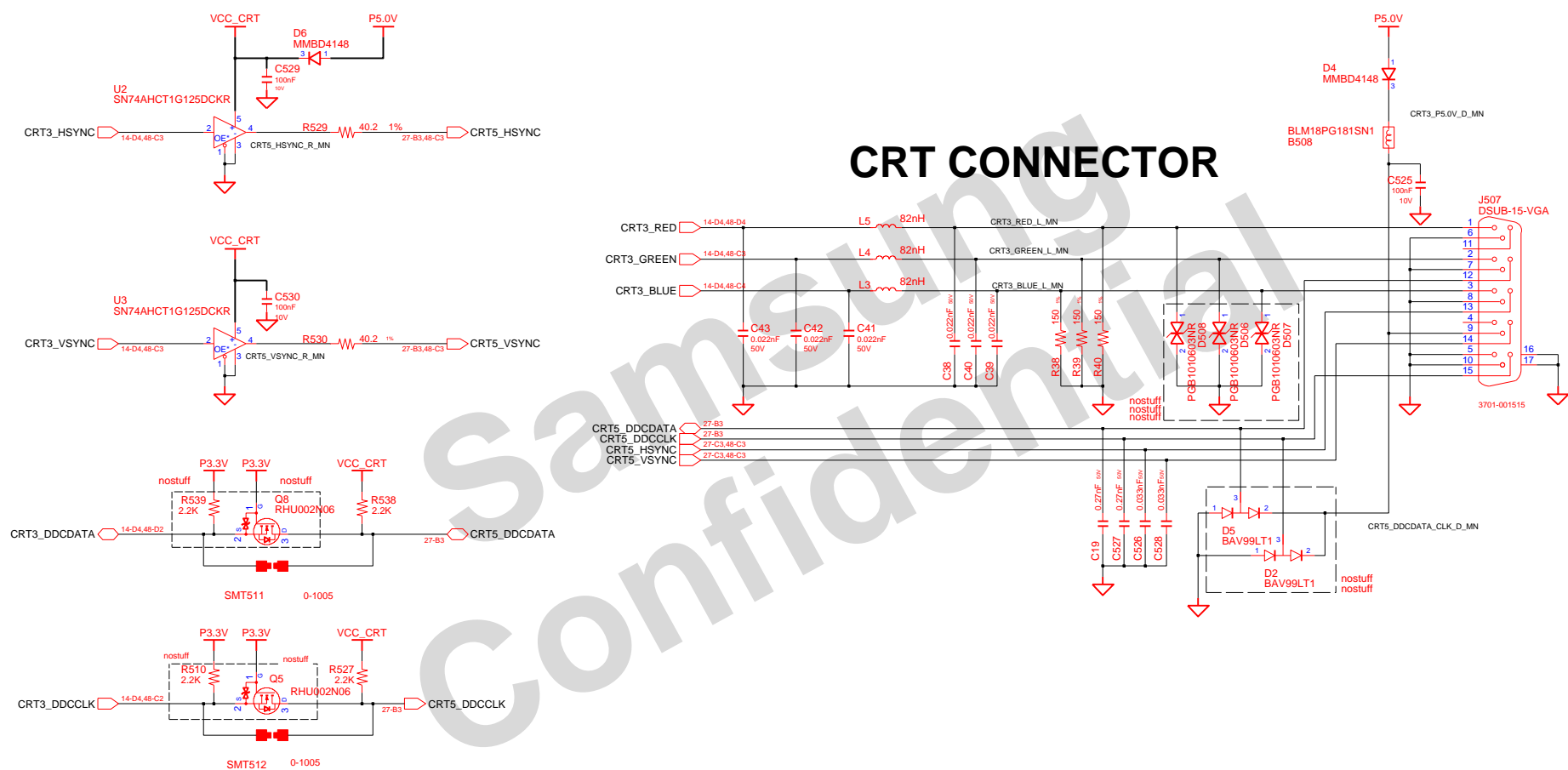
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>GRAPHICS_IF</b> <b>LVDS</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO: <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	34 OF 61

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# CRT

## CRT CONNECTOR



Check "CRT3\_DDCCLK/DATA" Voltage Level  
2N06 Can be replaced with SM6K2

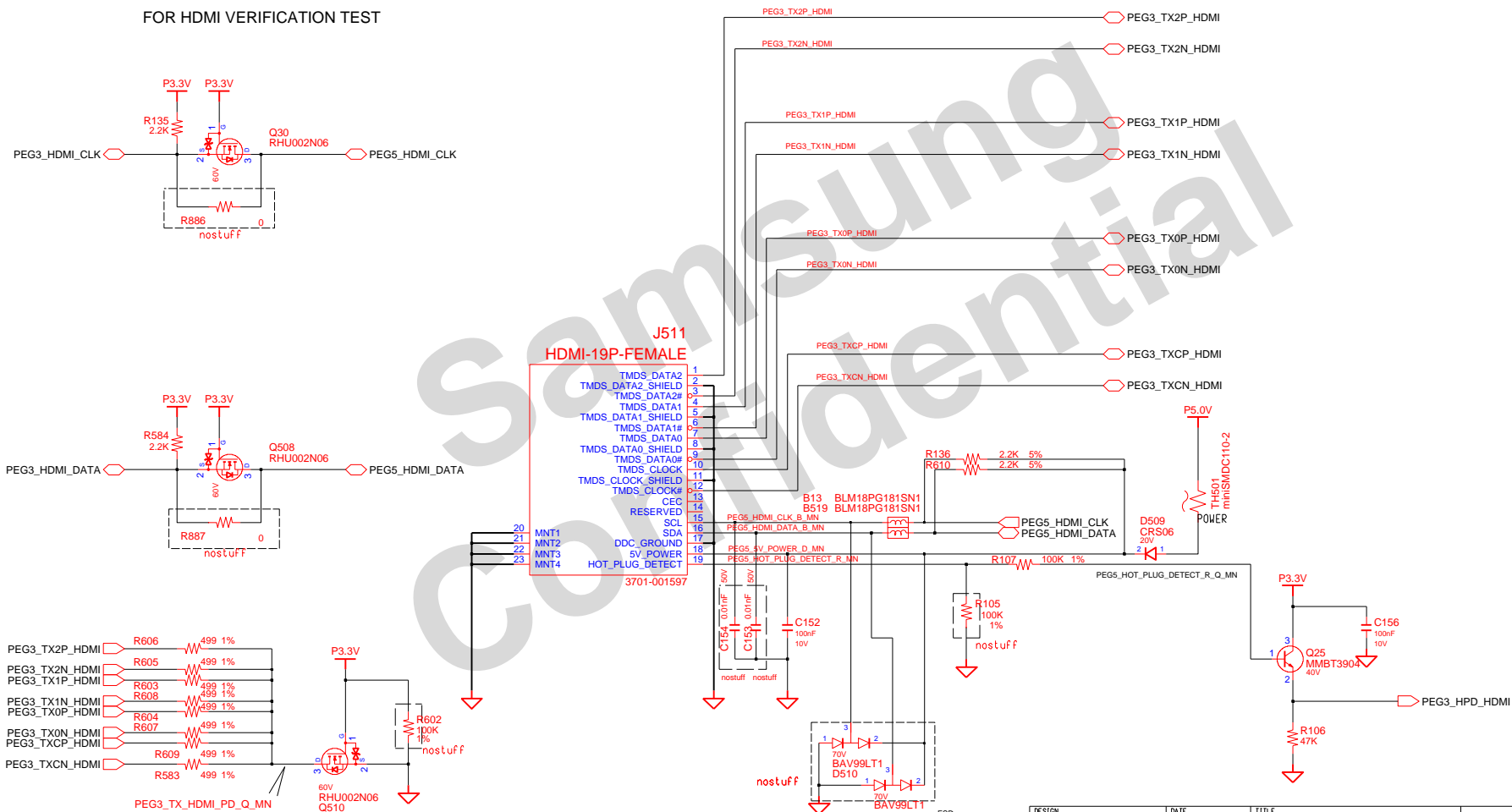
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>GRAPHICS_IF</b> <b>CRT</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	35 OF 61

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# HDMI

FOR HDMI VERIFICATION TEST



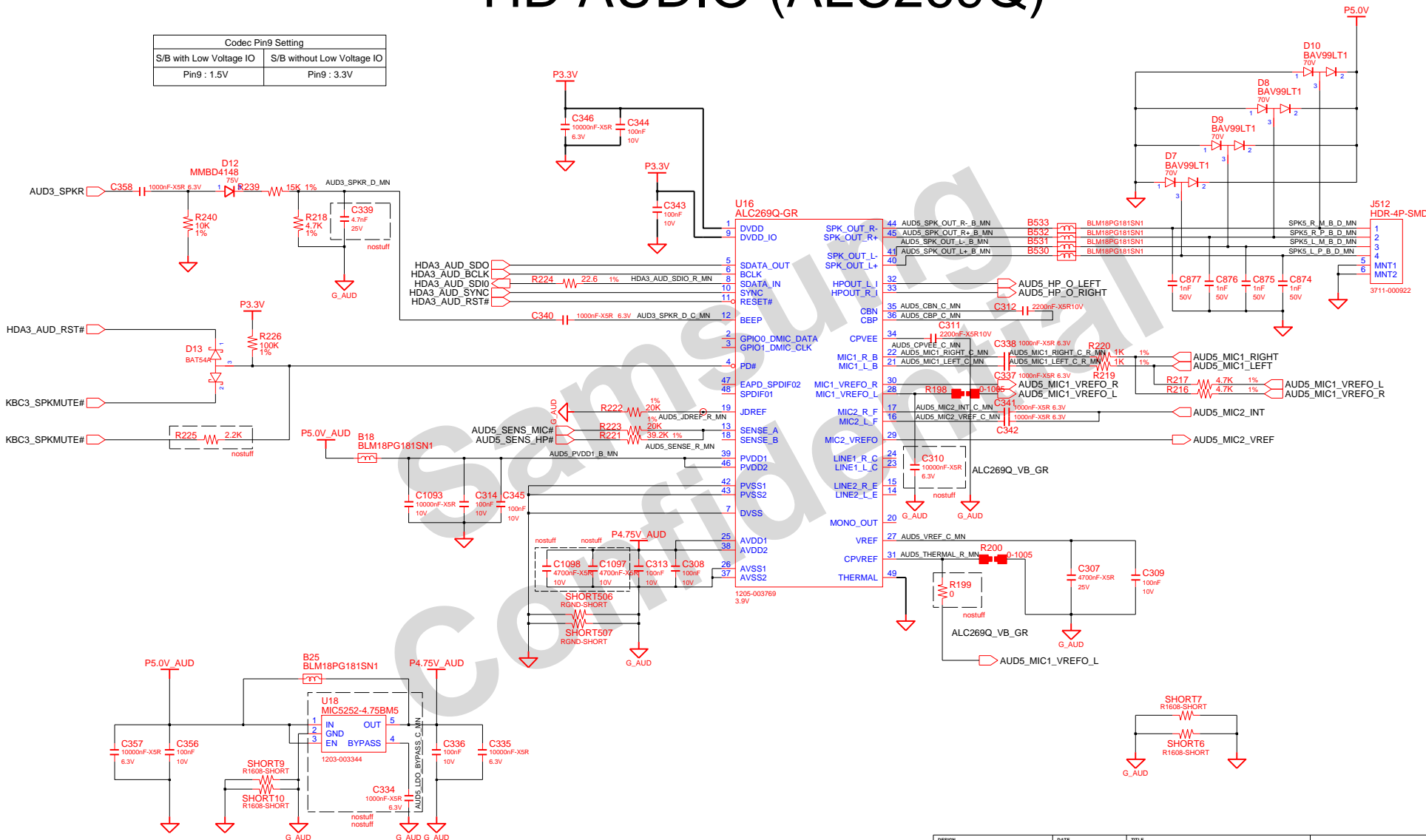
DESIGN	H.J.Ro	DATE	8/14/2009	TITLE	Bremen-D	<b>SAMSUNG</b> ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1	HDMI	HDMI	
APPROVAL	H.K.Park	REV	1.1	HDMI	HDMI	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	36	OF 61

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# HD AUDIO (ALC269Q)

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



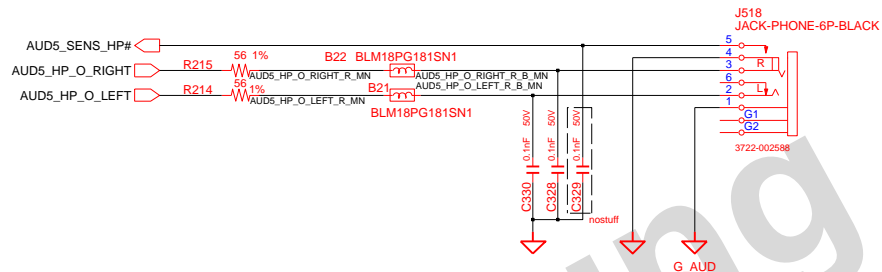
GMT : 1203-005579

DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	SAMSUNG
CHECK	K.Y.Kim	DEV.STEP	ADV1		HDA_CODEC	ELECTRONICS
APPROVAL	H.K.Park	REV	1.1		AUDIO CODEC ALC269Q_GR	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT			October 10, 2009 16:50:44 PM	PAGE 37 OF 61

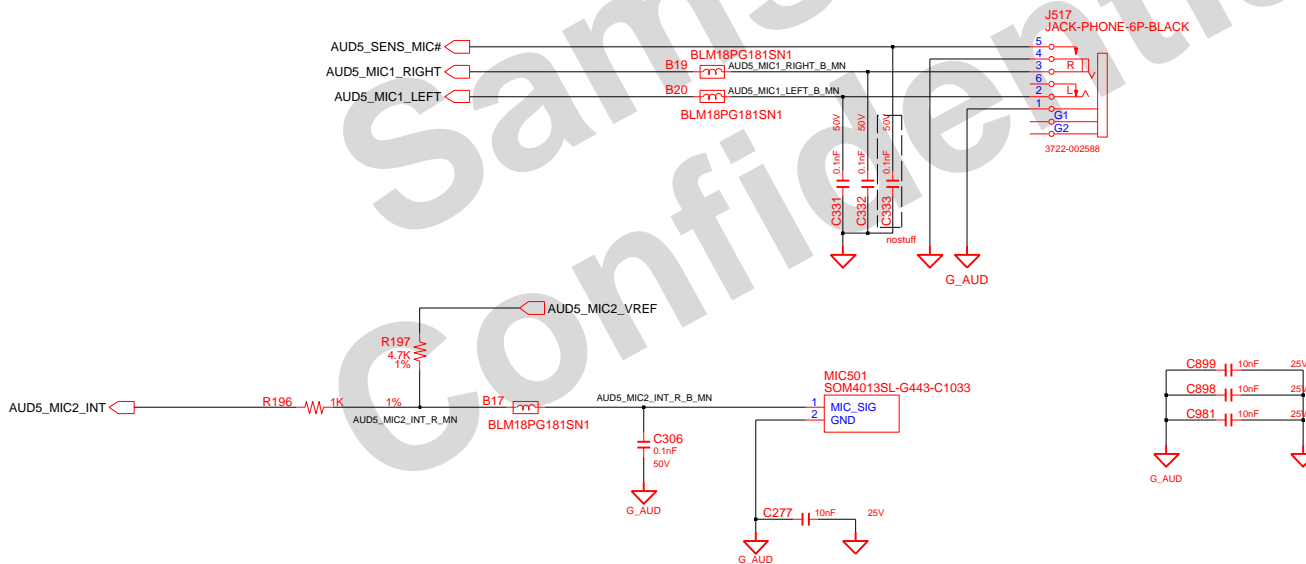
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**HEADPHONE(BLACK)**



**MIC JACK(BLACK)**



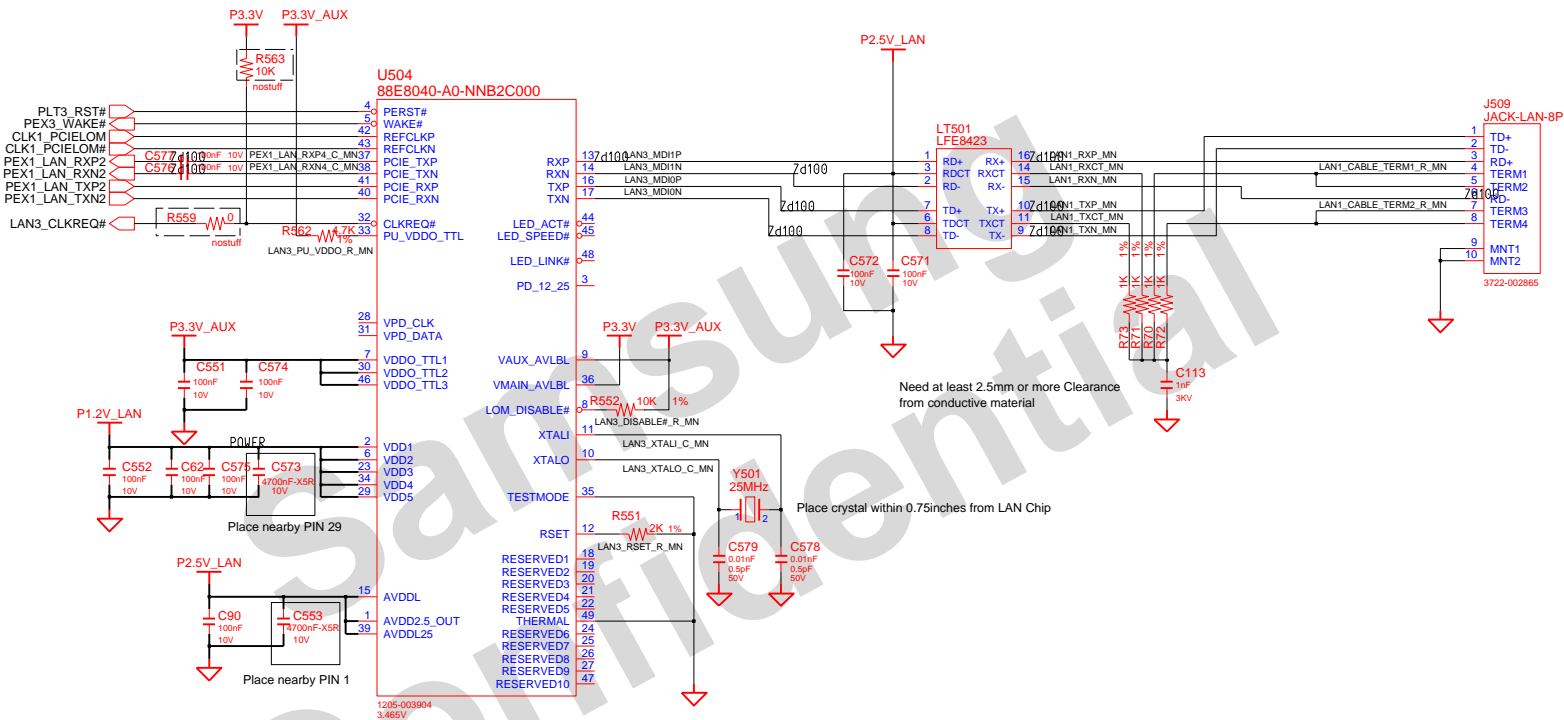
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>HDA_CODEC</b> <b>AUDIO INPUT/OUTPUT</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b>	
CHECK	K.Y.Kim	DEV.STEP	ADV1	PART NO.			BA41-xxxxxA
APPROVAL	H.K.Park	REV	1,1	MODULE CODE			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE			38 OF 61

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# LAN Controller (88E8040)

Place AC coupling capacitors Close to LAN Chip

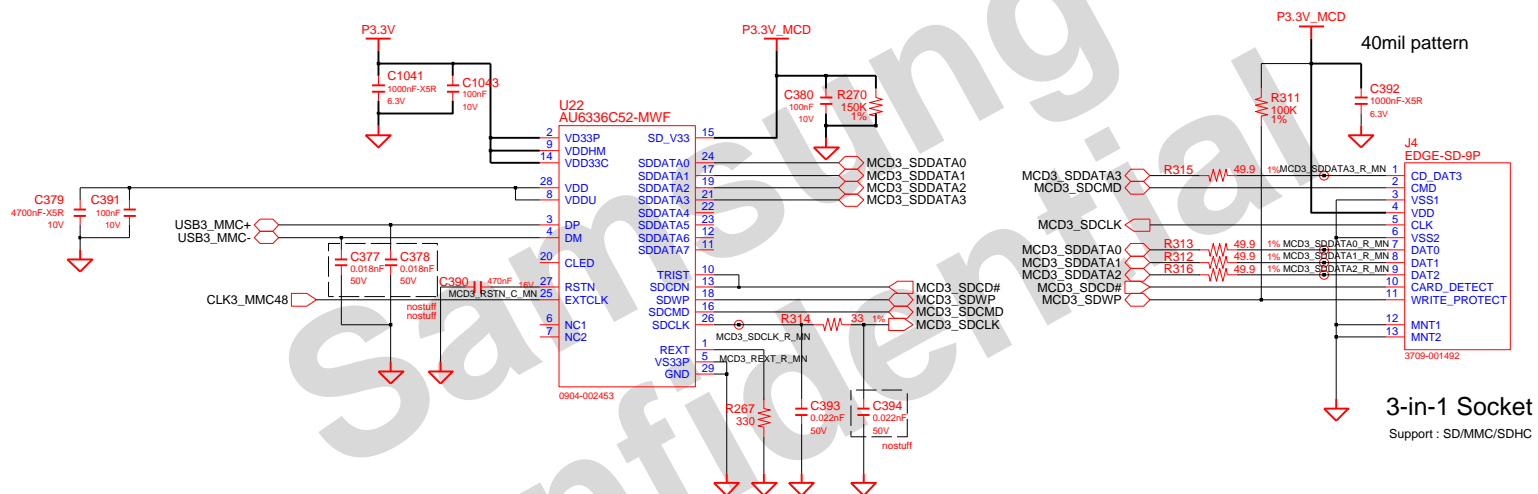


DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D LAN LAN_MARVELL_8040	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	39 OF 61

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# 3 IN 1 CARD (AU6336)



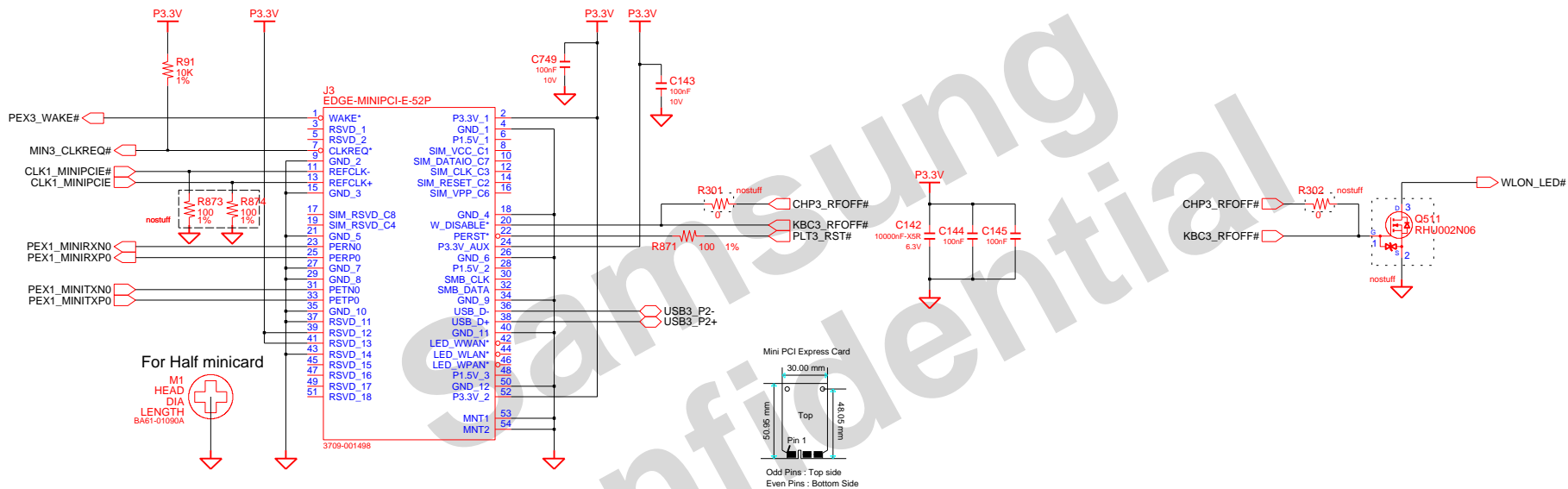
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>MULTICARD</b> <b>3 IN 1 CARD</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	40 OF 61

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# Wireless LAN

## WLAN, 4mm



Confidential

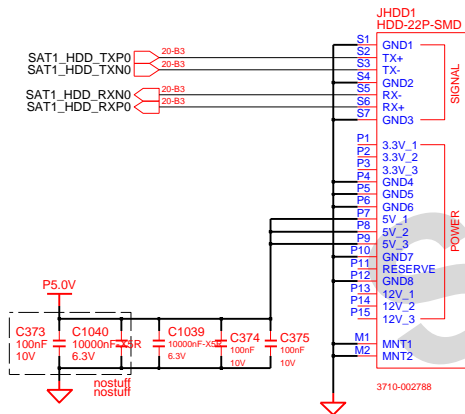
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MINI_PCIE_CONN	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1		WLAN	PART NO. BA41-xxxxxA
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 41 OF 61	

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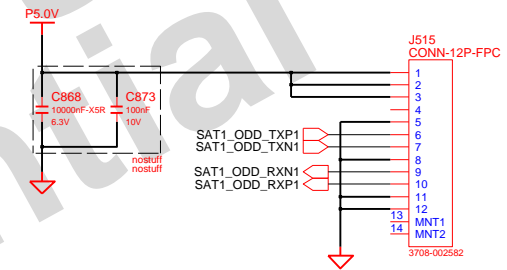
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# SATA I/F CONN

## SATA HDD CONN



## MAIN TO SUB SATA ODD CONN



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>SATA_DEVICES</b> <b>HDD &amp; ODD SUB CONNECTOR</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE 42 OF 61		

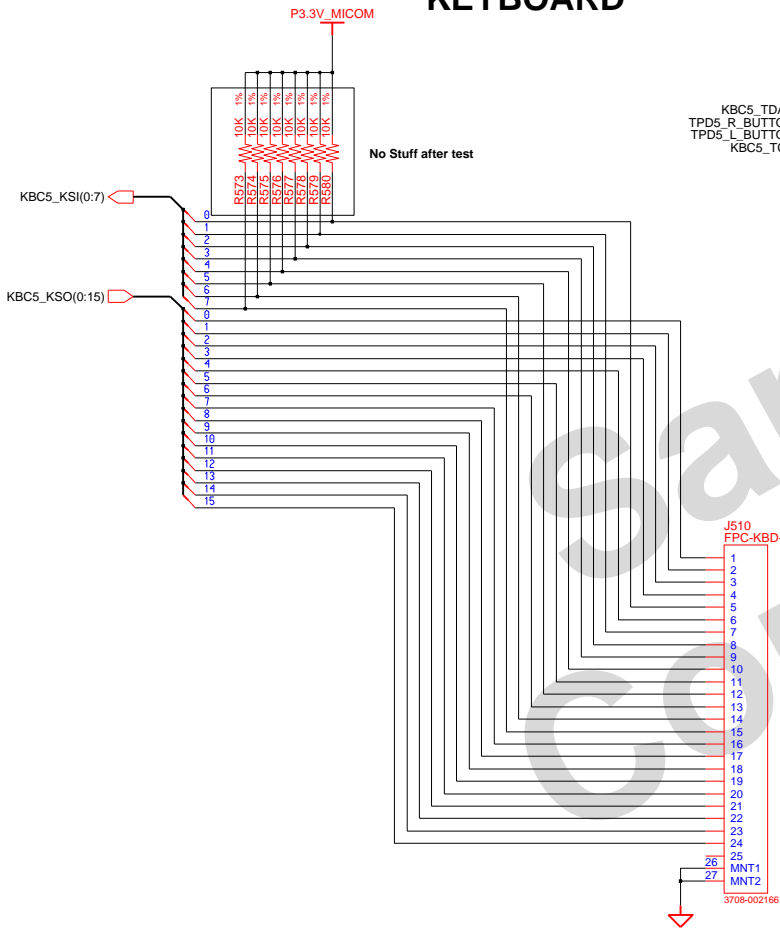


**SAMSUNG PROPRIETARY**

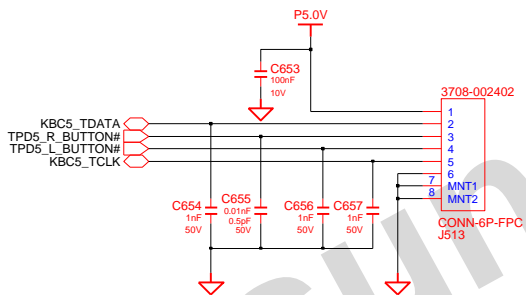
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# Micom Glue Logic

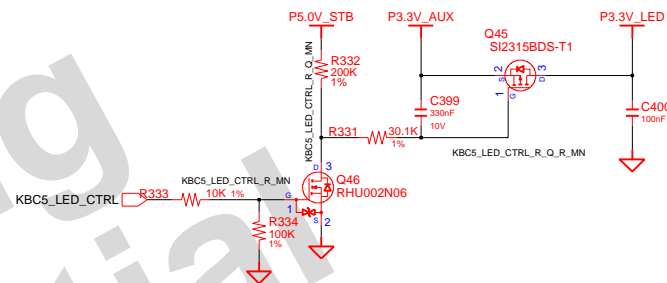
## KEYBOARD



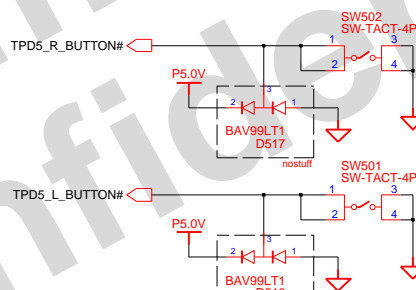
## TOUCHPAD



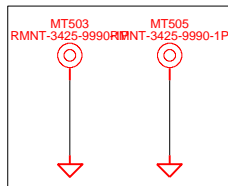
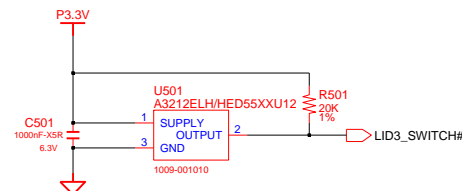
## TOUCHPAD LED



## TOUCHPAD BUTTON



## LID SWITCH



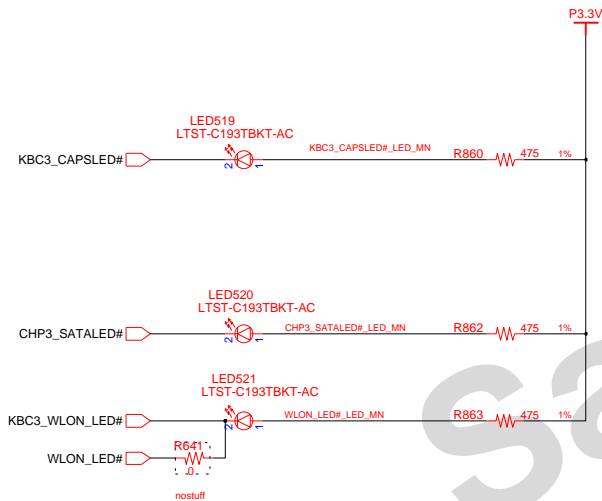
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D MICOM GLUE LOGIC KEYBOARD & TOUCHPAD	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV.STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE 44 OF 61	

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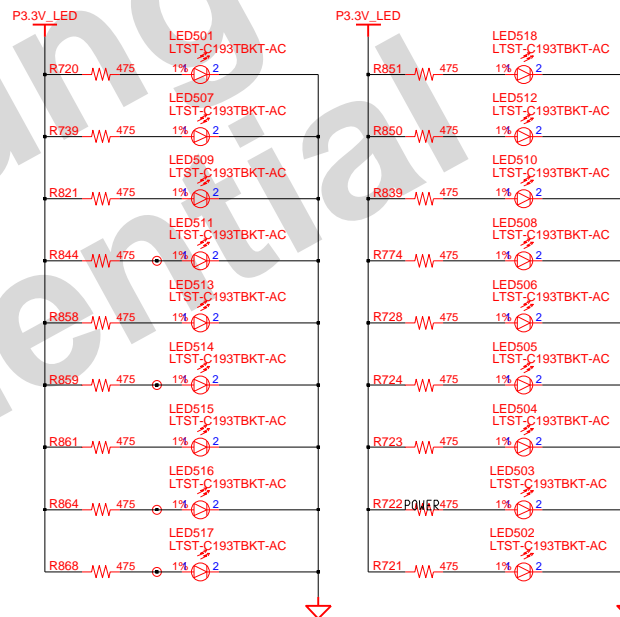
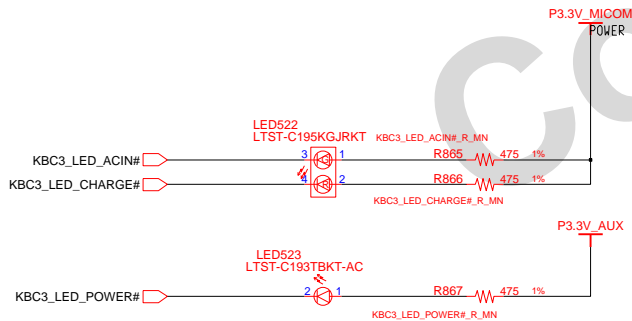
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# LEDs

## FUNCTION KEY LED



## ADAPTERIN/CHARGING LED

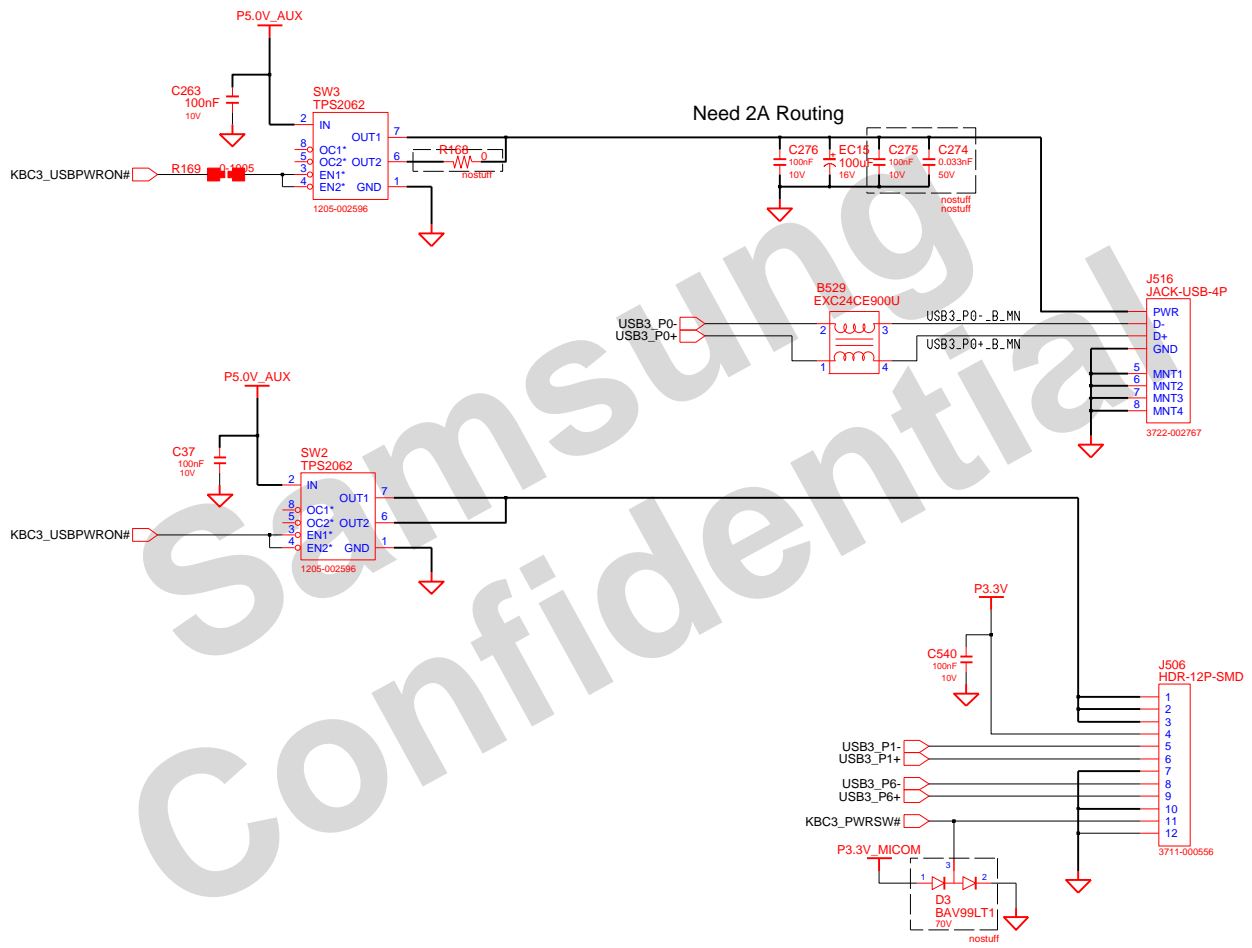


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>LED_SWITCH</b> <b>LED_SWITCH</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	45 OF 61

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# USB Single connector



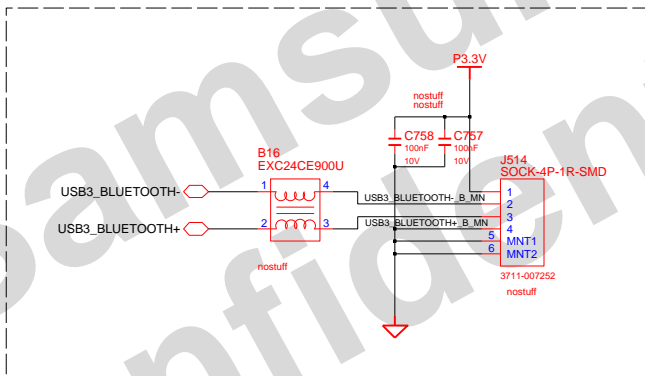
DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>USB_CONN</b> <b>USB</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE <b>46</b> OF <b>61</b>		

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# USB I/F Devices

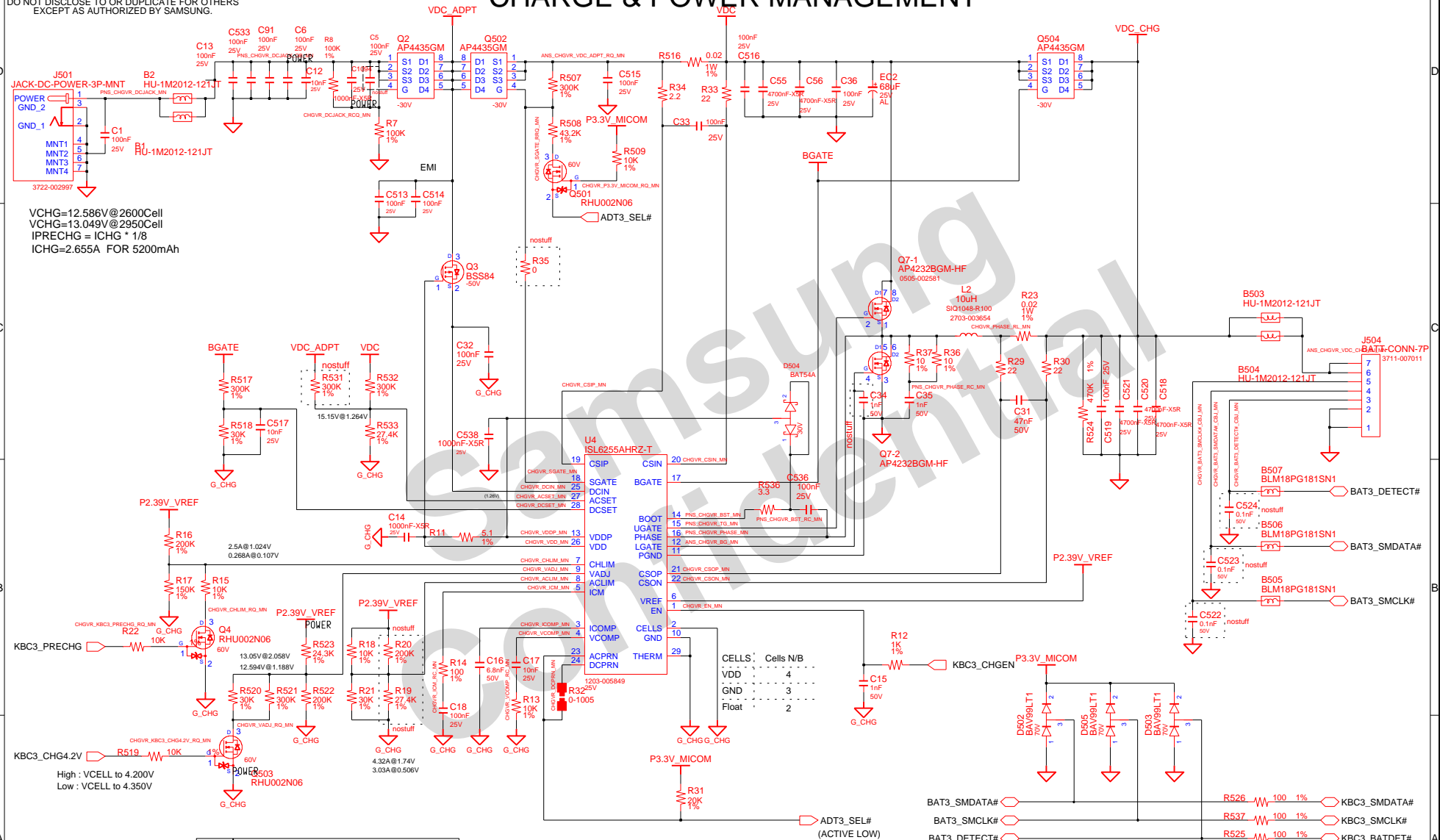
## Bluetooth Interface



DESIGN	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>USB_DEVICES</b> <b>BLUETOOTH</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b>	
CHECK	K.Y.Kim	DEV.STEP	ADV1	PART NO.			BA41-xxxxxA
APPROVAL	H.K.Park	REV	1.1				
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE			47 OF 61

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# CHARGE & POWER MANAGEMENT



VCHG=12.586V@2600Cell  
 VCHG=13.049V@2950Cell  
 IPRECHG = ICHG \* 1/8  
 ICHG=2.655A FOR 5200mAh

Adapter configuration			
	60W / 3.0A / 94.9%	90W / 4.36A / 92.3%	
	Value	SEC Code	Value
Rtop	100K	2007-007107	56.2K 2007-008133
Rbot	43.2K	2007-007108	43.2K 2007-007108

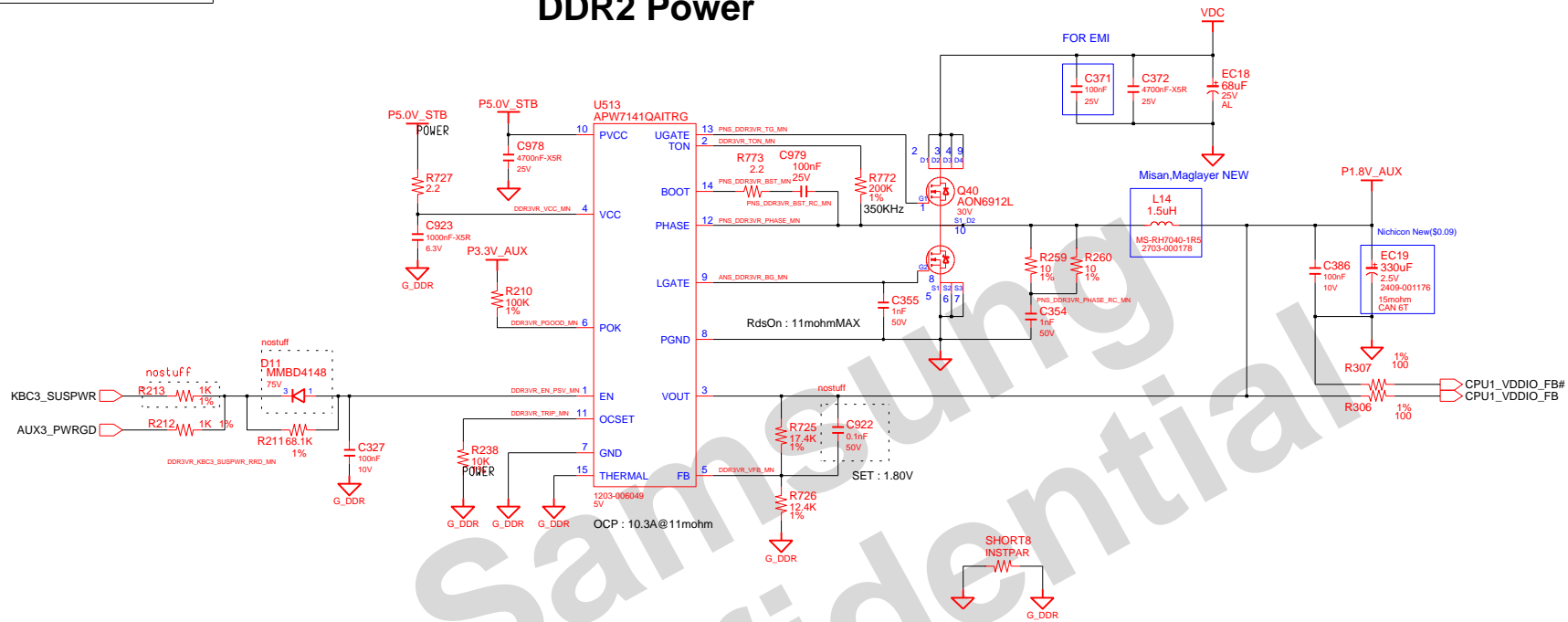
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D Charger	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1	REV	1.1	
APPROVAL	H.K.Park	REV	1.1	MODULE CODE	undefined	PART NO. BA41-xxxxxA
October 10, 2009 16:50:44 PM						PAGE 48 OF 61



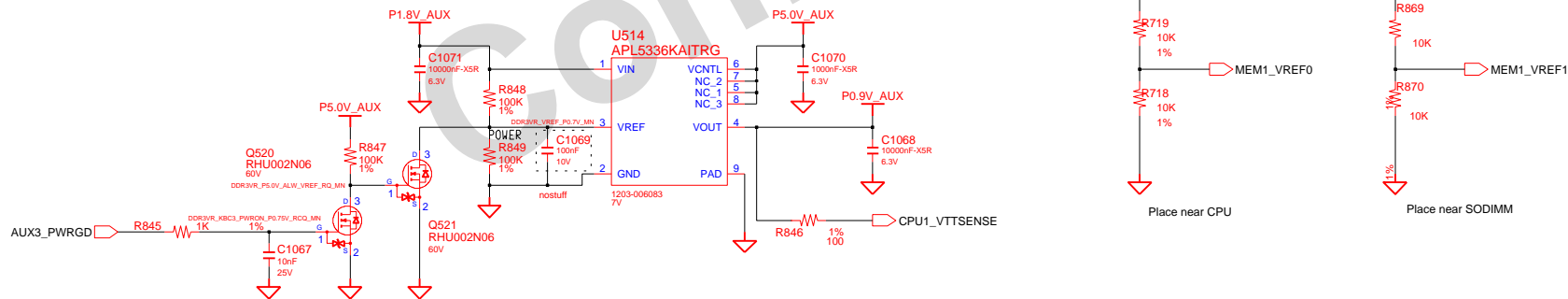
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# DDR2 Power



# DDR2 VTT(0.9V\_AUX)



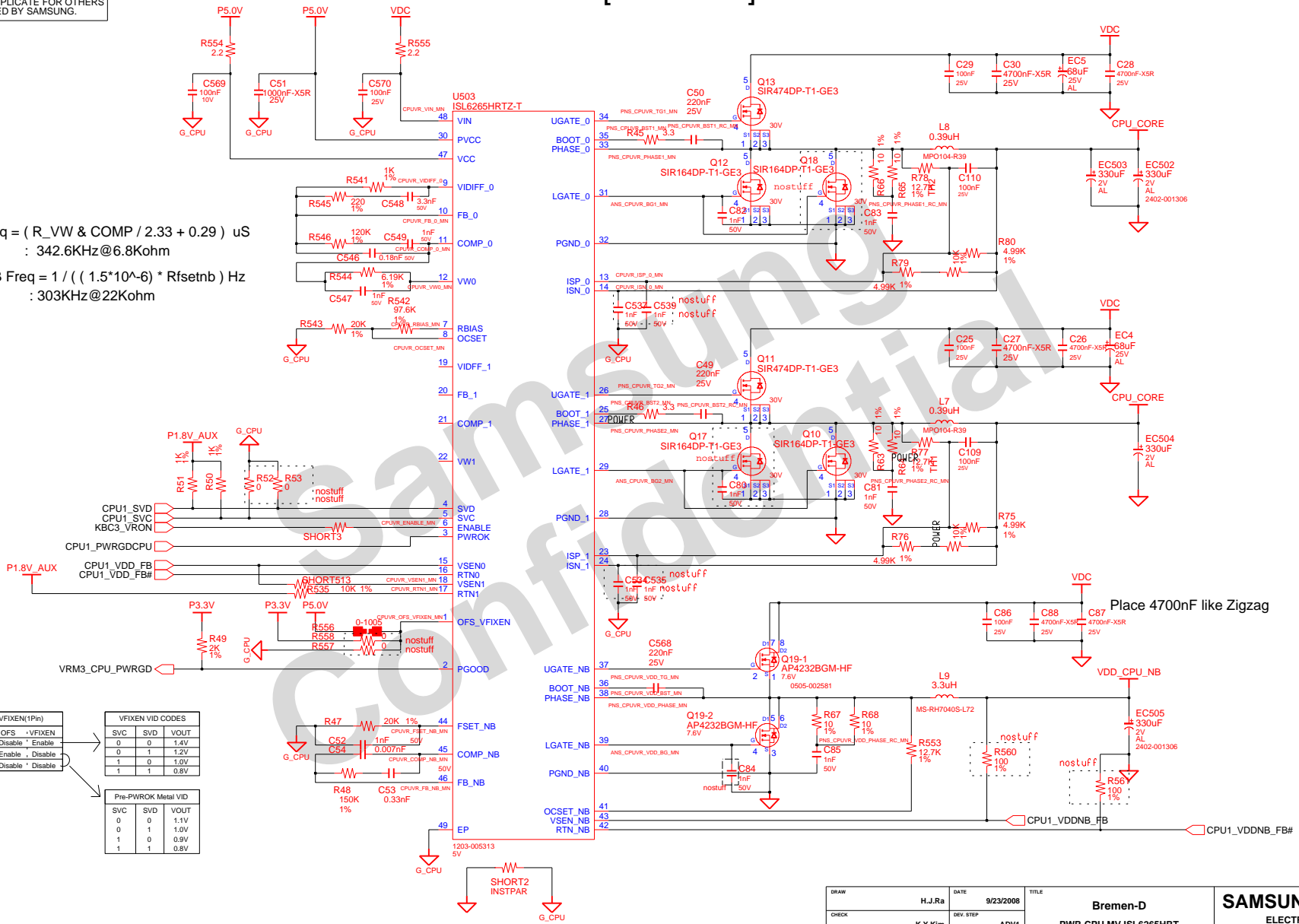
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>PWR_MEMORY</b> <b>DDR2 POWER</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO. <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE <b>50</b> OF <b>61</b>		

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# CPU VRM [INTERSIL]

$VDD \text{ Freq} = (R\_VW \& \text{COMP} / 2.33 + 0.29) \mu\text{S}$   
 : 342.6KHz@6.8Kohm

$VDD\_NB \text{ Freq} = 1 / ((1.5 * 10^{-6}) * R\text{fsetnb}) \text{ Hz}$   
 : 303KHz@22Kohm



Place 4700nF like Zigzag

OFS/VFIXEN(1Pin)		VFIXEN VID CODES		
OFS	VFIXEN	SVC	SVD	VOUT
3.3V	Disable	Enable	0	1.4V
GND	Enable	Disable	0	1.2V
1	1	1	1	0.8V

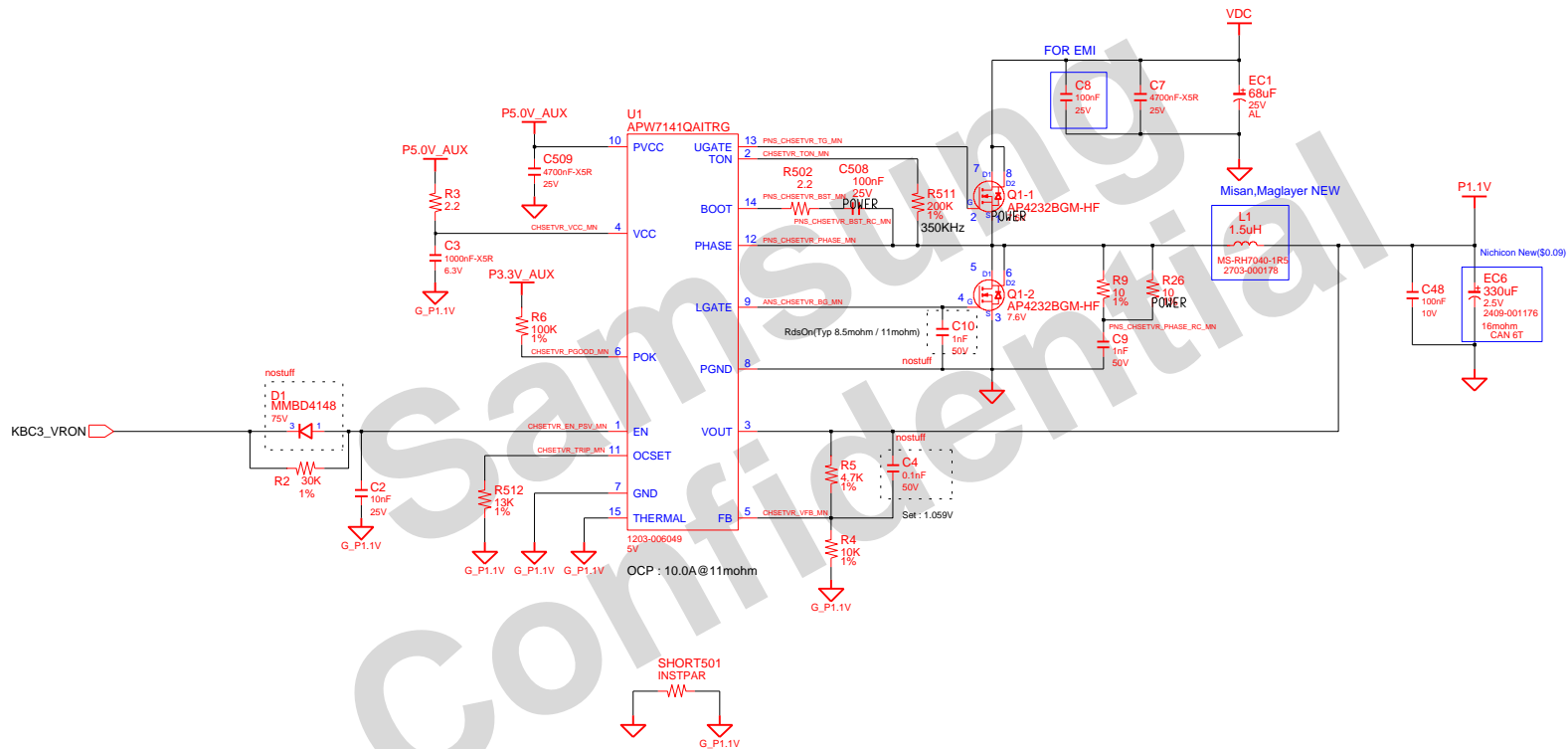
Pre-PWROK Metal VID		VOUT		
SVC	SVD	1.1V	1.0V	0.9V
0	0	1	1	0.8V
1	0	0	1	0.9V
1	1	1	1	0.8V

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	<b>SAMSUNG</b> ELECTRONICS
CHECK	K.Y.Kim	DEV. STEP	ADV1		PWR CPU MV ISL6265HRT	
APPROVAL	H.K.Park	REV	1,1		CPU VRM	PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	51	OF 61

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# CHIPSET POWER(P1.1V)



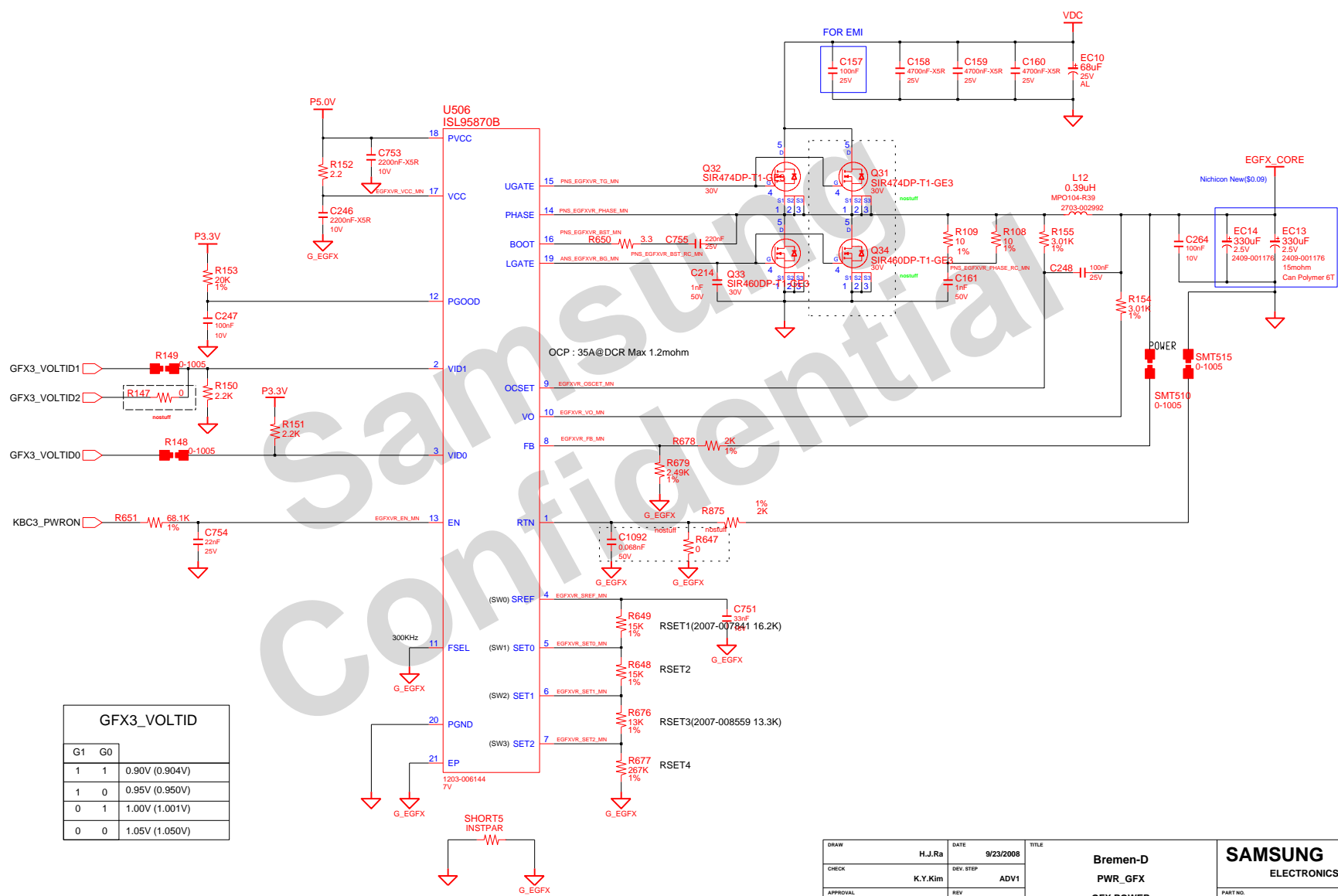
DESIGN	H.J.Ro	DATE	9/3/2009	TITLE	Bremen-D PWR MV RX881 P1.1V	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	52 OF 61	



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# Graphic Core Power



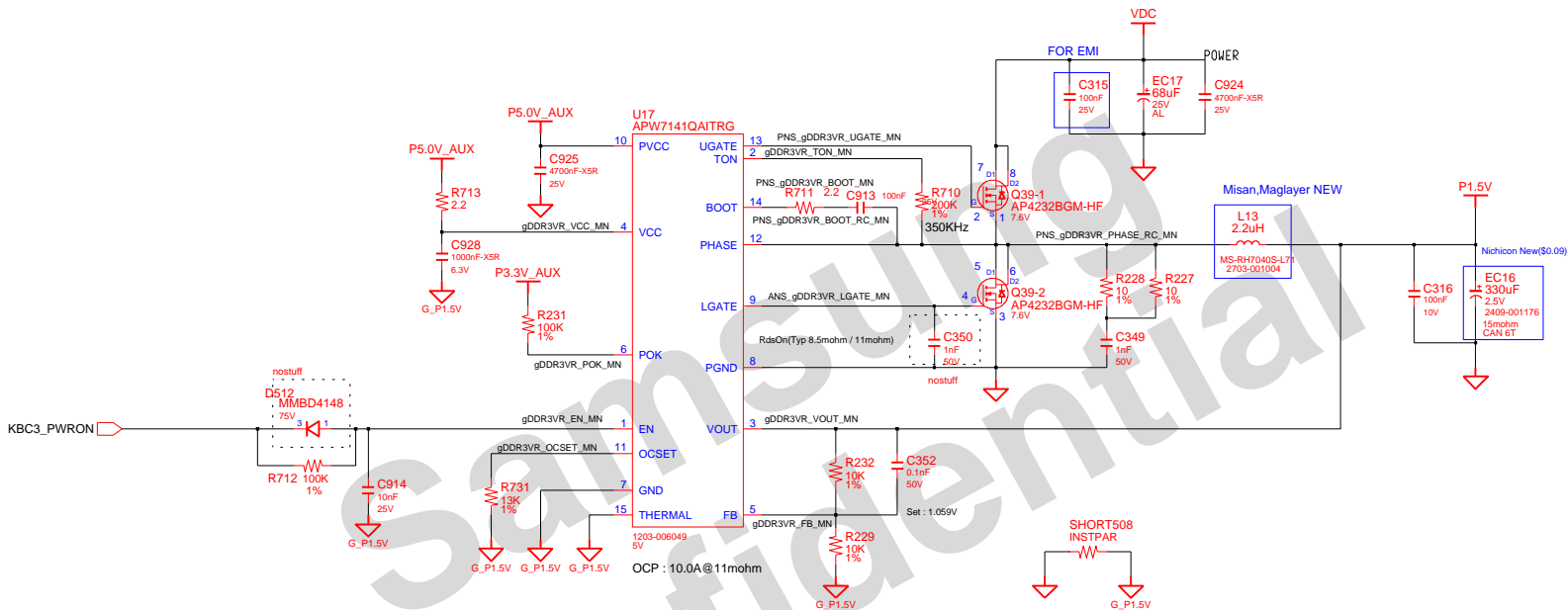
GFX3_VOLTIID			
G1	G0		
1	1	0.90V (0.904V)	
1	0	0.95V (0.950V)	
0	1	1.00V (1.001V)	
0	0	1.05V (1.050V)	

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>PWR_GFX</b> <b>GFX POWER</b>	<b>SAMSUNG</b> <b>ELECTRONICS</b> PART NO: <b>BA41-xxxxxA</b>
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT				
				October 10, 2009 16:50:44 PM	PAGE	54 OF 61

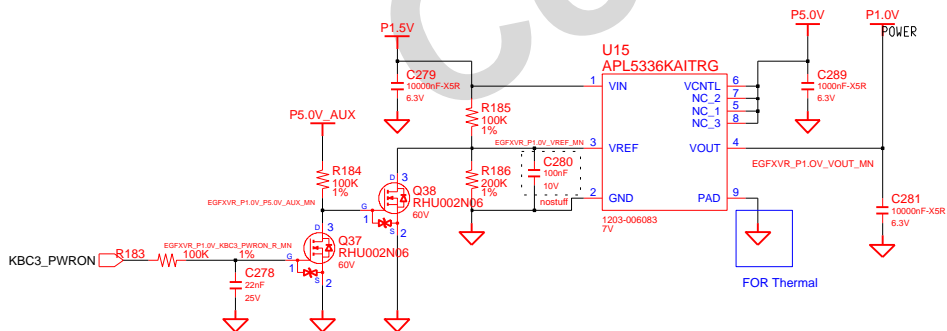
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# gDDR3 POWER(P1.5V)



# P1.0V



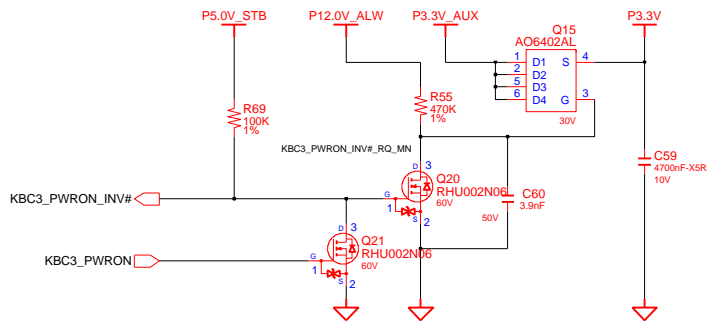
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D	
CHECK	K.Y.Kim	DEV.STEP	ADV1	PWR GFX MEMORY		SAMSUNG ELECTRONICS
APPROVAL	H.K.Park	REV	1.1	gDDR3 POWER		PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	55	OF 61

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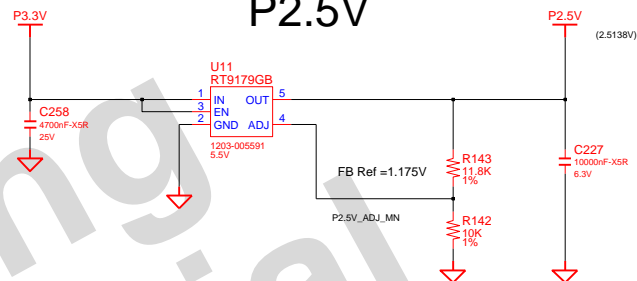
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# Switched Power

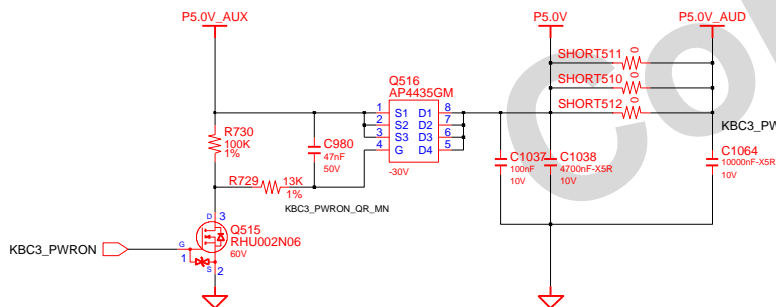
## Switched Power On (P3.3V)



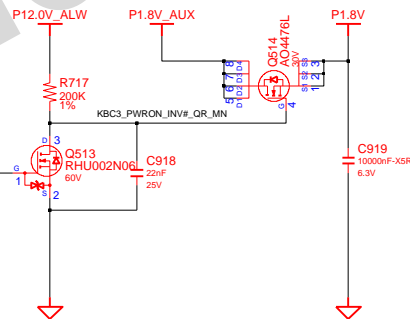
## P2.5V



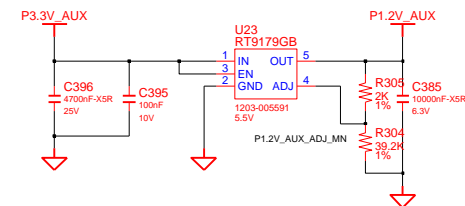
## Switched Power On (P5.0V)



## Switched Power On (P1.8V)



## P1.2V\_AUX

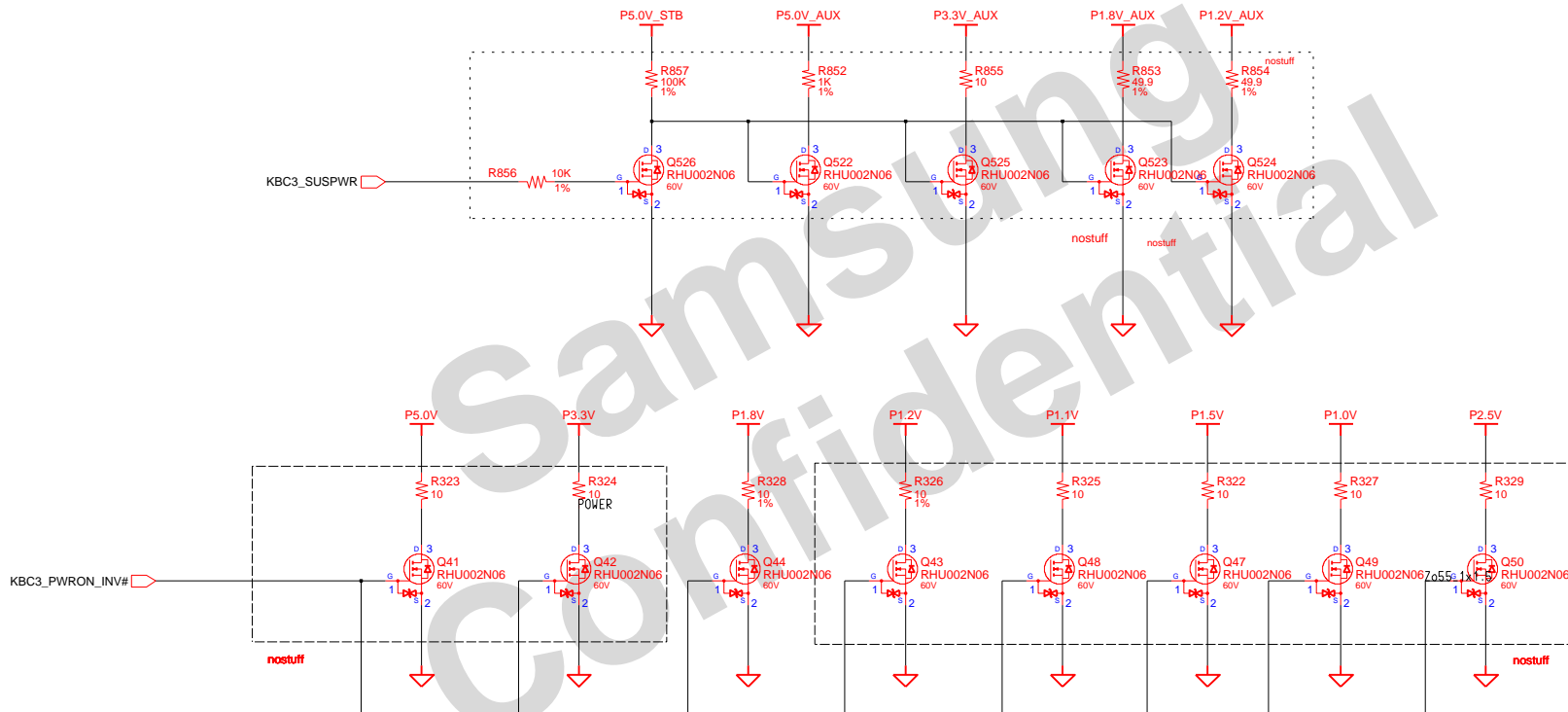


DESIGN	H.J.Ro	DATE	8/22/2009	TITLE	Bremen-D PWR_MV_SWITCHED SWITCHED POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV. STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE	56 OF 61	

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# POWER DISCHARGER



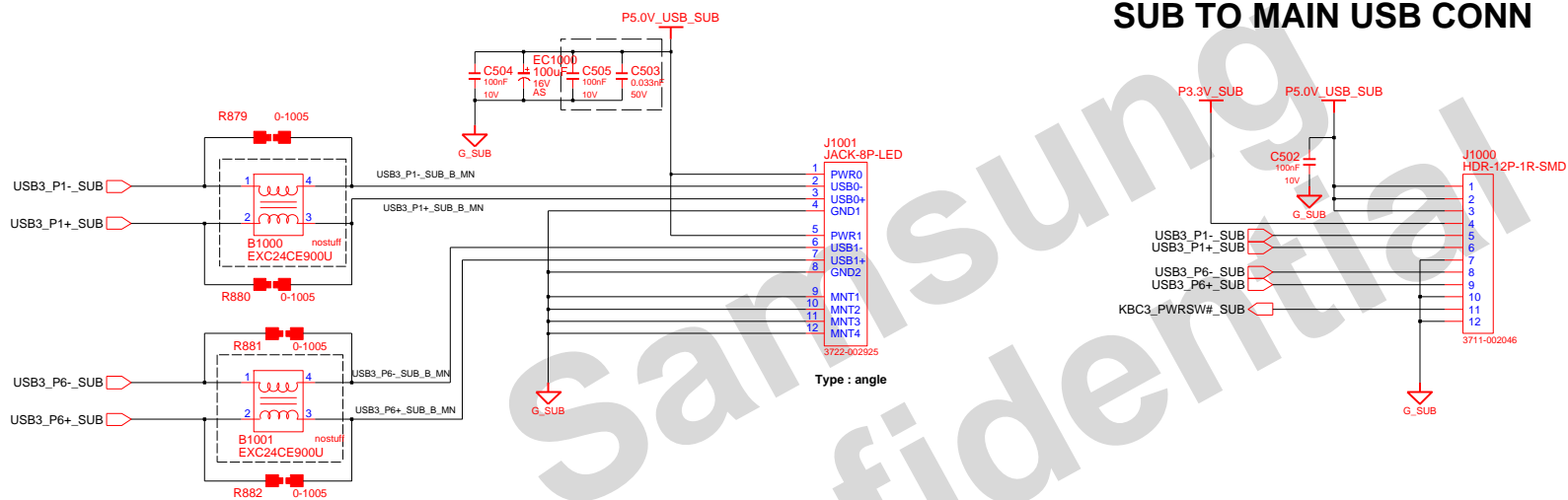
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>PWR_MV_DISCHARGER</b> <b>DISCHARGER LOGIC</b>	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1,1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE 57 OF 61		

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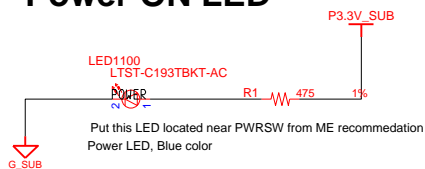
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# 2 USB PORT & POWER S/W SUB B'D

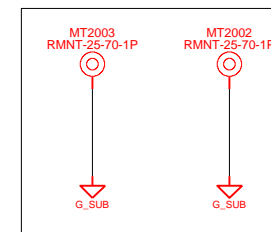
## SUB TO MAIN USB CONN



### Power ON LED



### Power Button



USB sub board mount hole

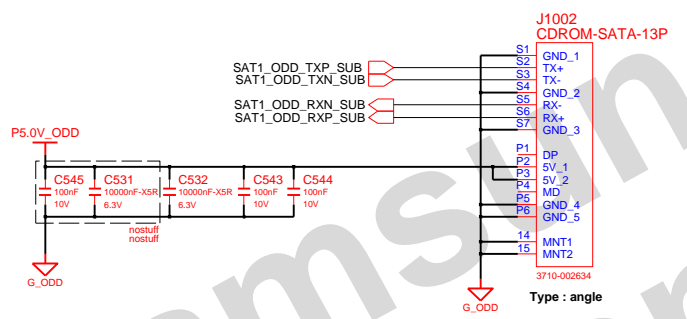
DRAW	H.J.Ra	DATE	9/23/2008	TITLE	Bremen-D SUB BOARD1	SAMSUNG ELECTRONICS
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1	USB PORT, POWER SW SUB BOARD	PART NO.	BA41-xxxxxA
MODULE CODE		LAST EDIT		October 10, 2009 16:50:44 PM	PAGE	58 OF 61

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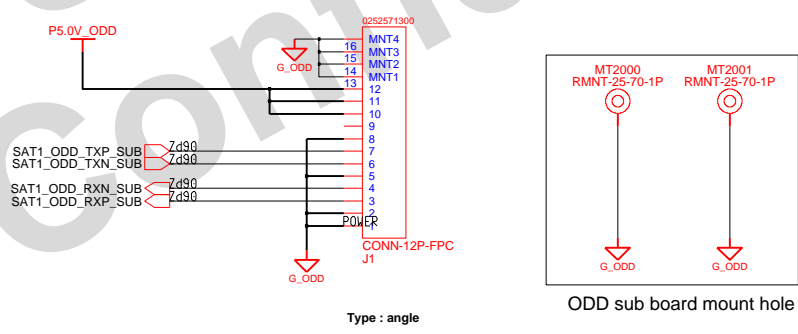
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# SATA ODD SUBBOARD

## SATA ODD CONN



## SUB TO MAIN SATA ODD CONN

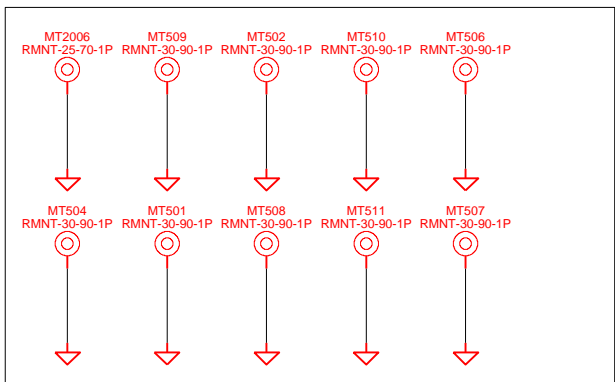


DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D</b> <b>SUB BOARD2</b> <b>SATA ODD SUB BOARD</b>	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxA
CHECK	K.Y.Kim	DEV.STEP	ADV1			
APPROVAL	H.K.Park	REV	1.1			
MODULE CODE	undefined	LAST EDIT	October 10, 2009 16:50:44 PM	PAGE 59 OF 61		

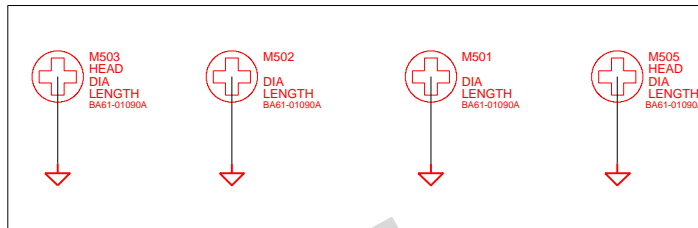
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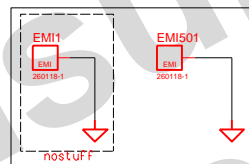
**Mainboard Mount**



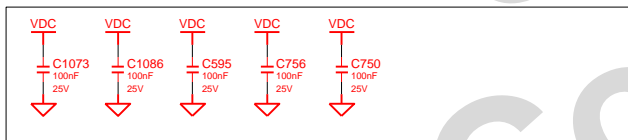
(30,90) x 7, (25,70) x 1



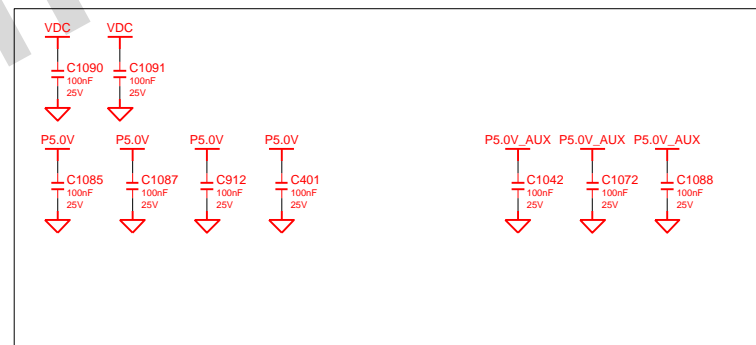
To Support Heatsink



EMI Finger



Add for EMC (Bottom)



Add for EMC (Bottom)

DRAW	H.J.Ra	DATE	9/23/2008	TITLE	<b>Bremen-D MAIN MOUNT HOLE</b>	<b>SAMSUNG ELECTRONICS</b>
CHECK	K.Y.Kim	DEV. STEP	ADV1	PART NO.		
APPROVAL	H.K.Park	REV	1,1	BA41-xxxxxA		
MODULE CODE		LAST EDIT	October 10, 2009 16:50:44 PM	PAGE 60 OF 61		

