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GENEVA 2 EXT

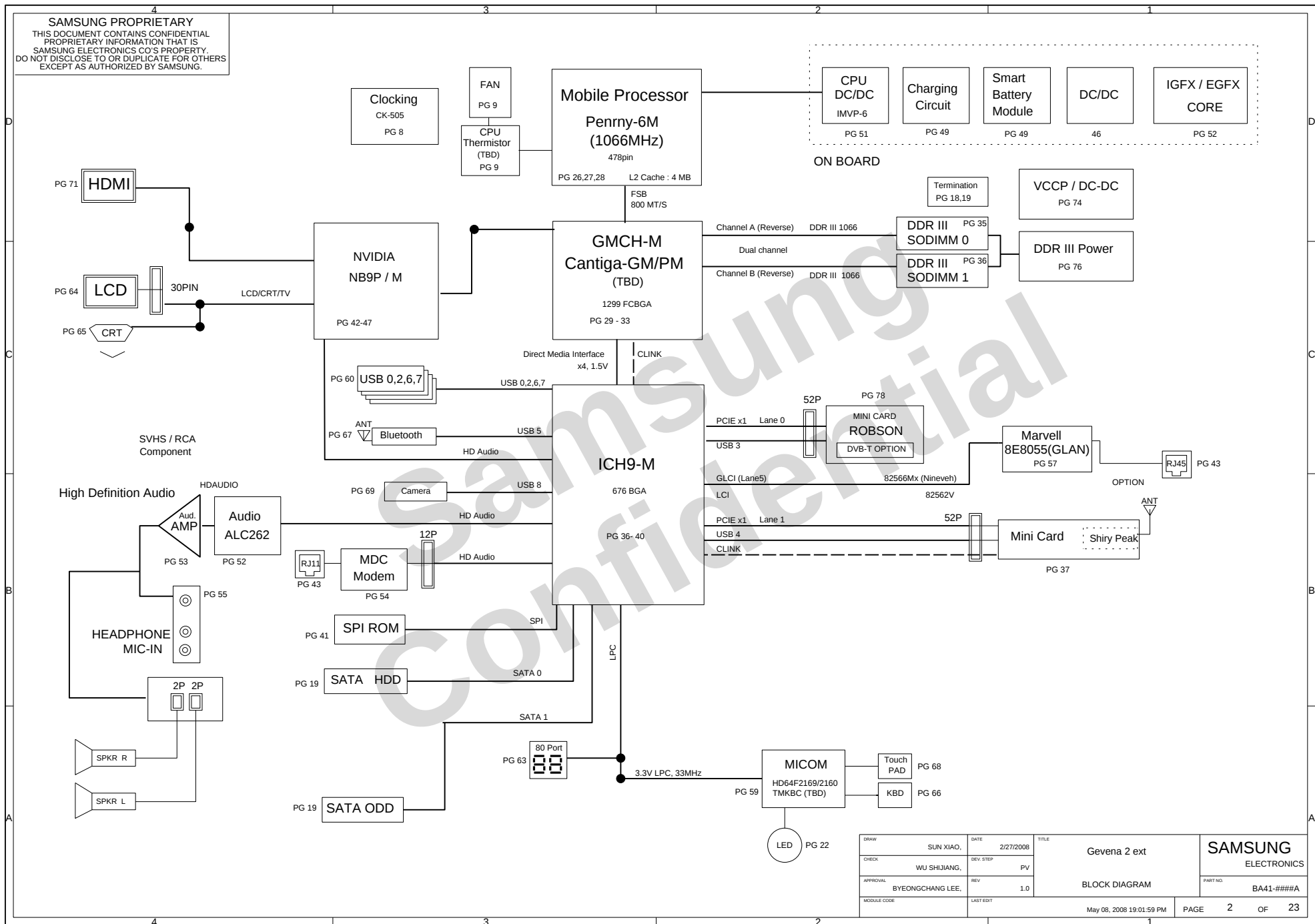
CPU : Penryn
Chip Set : Cantiga + ICH9M
Remarks : Mobility Platform

Model Name : GENEVA 2 EXT
PBA Name : MAIN
PCB Code : SGCE BA41-00930A
NAYA BA41-00936A
Dev. Step : PV1.0
Revision : 1.0
T.R. Date :

DRAW	CHECK	APPROVAL
SUN XIAO	WUSHIJIANG	BC.LEE

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG
CHECK	WU SHIJIANG,	DEV. STEP	PV			ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0	COVER		PART NO.
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1	OF 23

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B,F
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
P5V	5.0V switched off power rail (off in S3-S5)
P5V_AUX	5.0V switched on power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCIE x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect

(TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

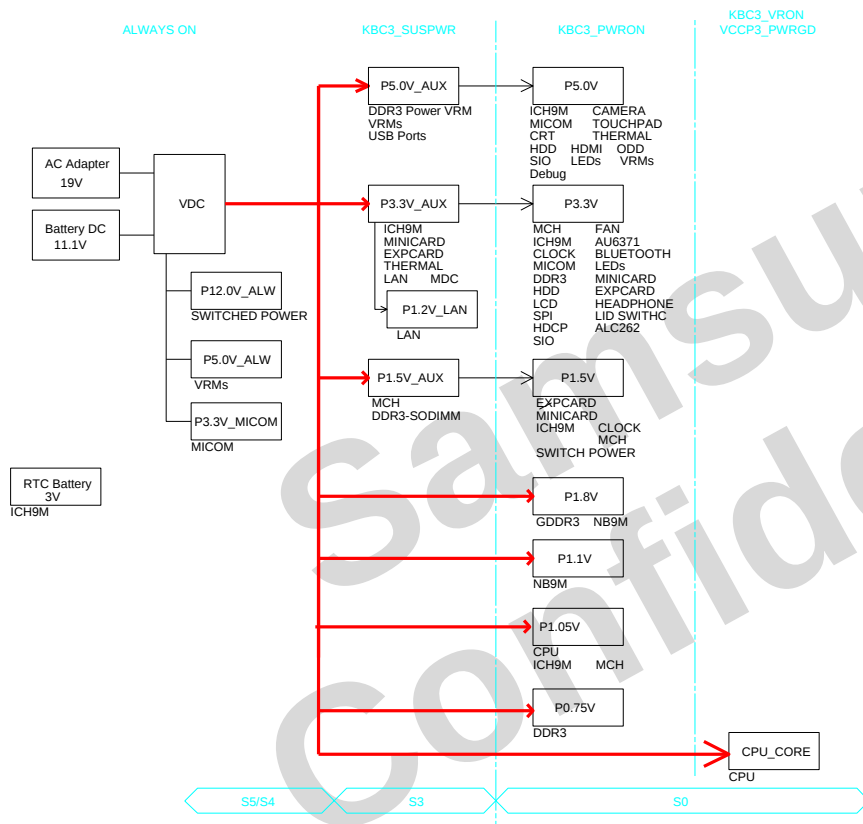
Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

REVISION HISTORY

See rev notes for more information.

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0	BOARD INFO		PART NO. BA41-####A
MODULE CODE		LAST EDIT			May 08, 2008 19:01:59 PM	PAGE 3 OF 23

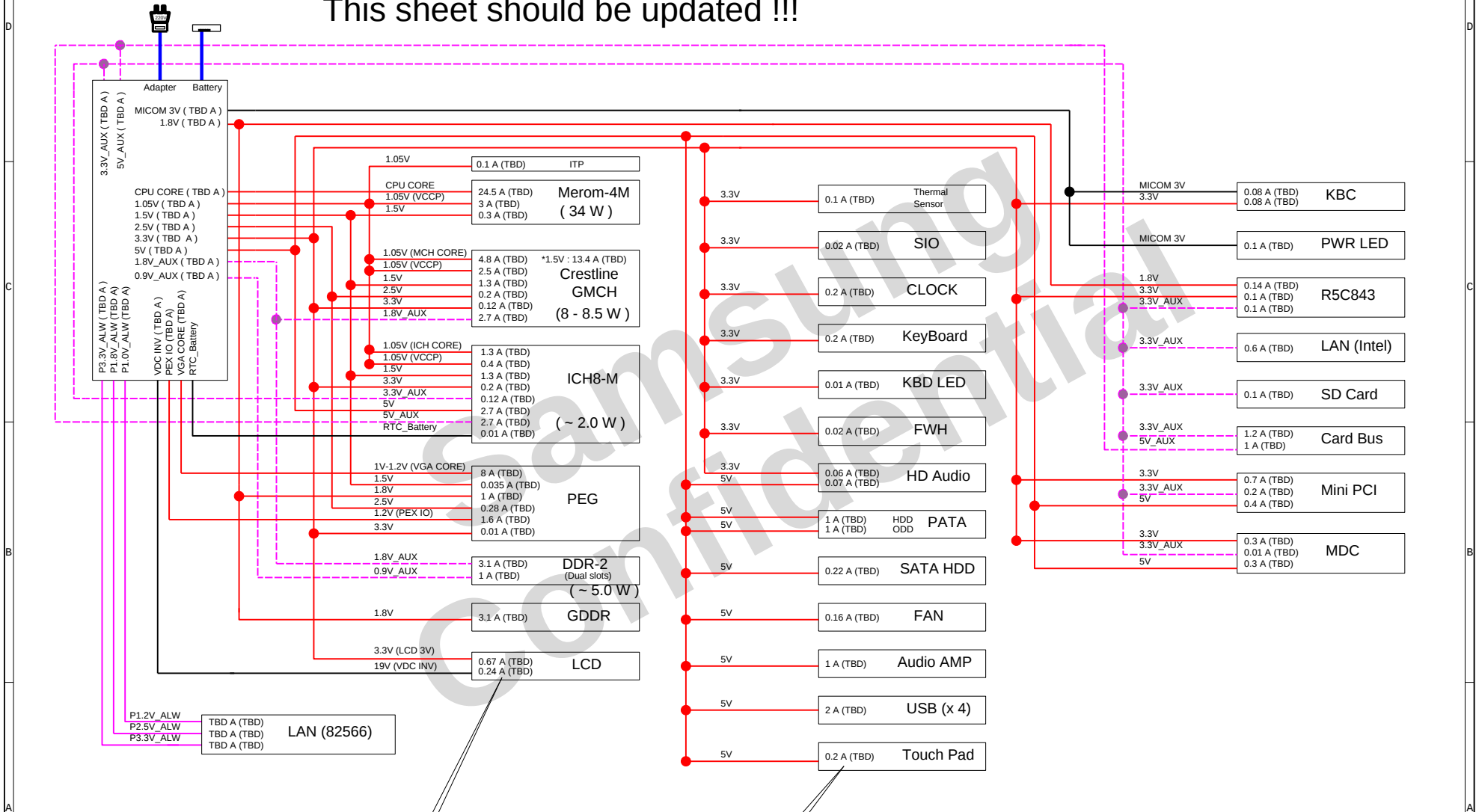
POWER DIAGRAM



State	Rail	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On		ON	ON	ON	H	H	H
S3		ON	ON	OFF	H	L	L
S4		ON	OFF	OFF	H	L	L
S5		ON	OFF	OFF	L	L	L

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG
CHECK	WU SHIJIANG,	DEV. STEP	PV			ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0	POWER DIAGRAM	PART NO.	BA41-####A
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	4	OF 23

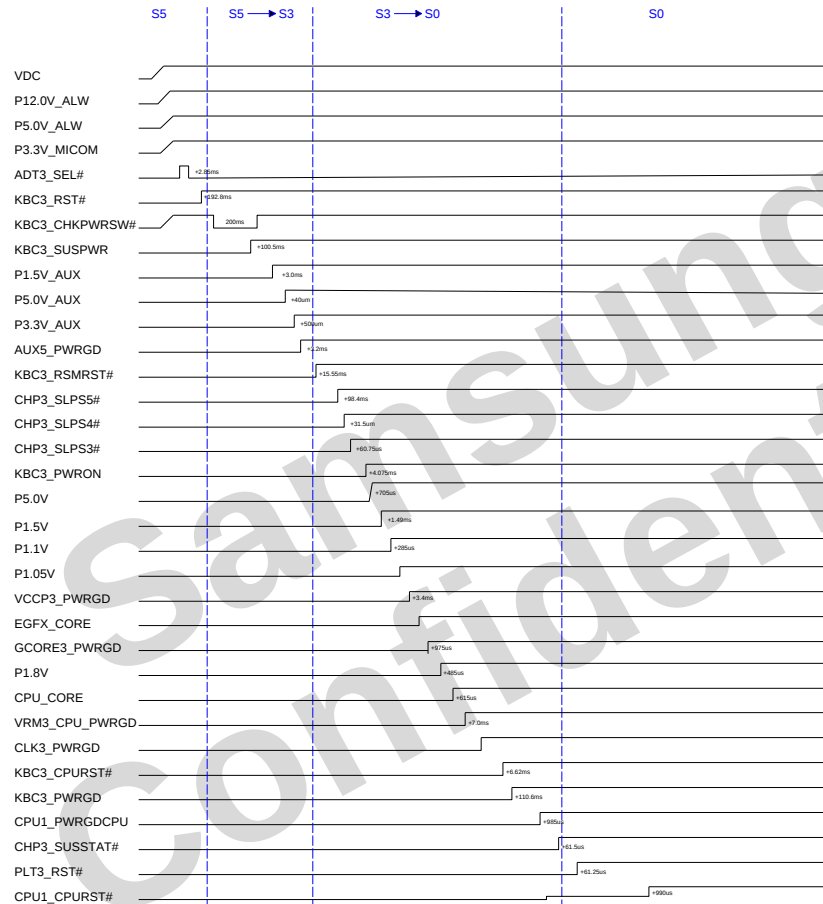
This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

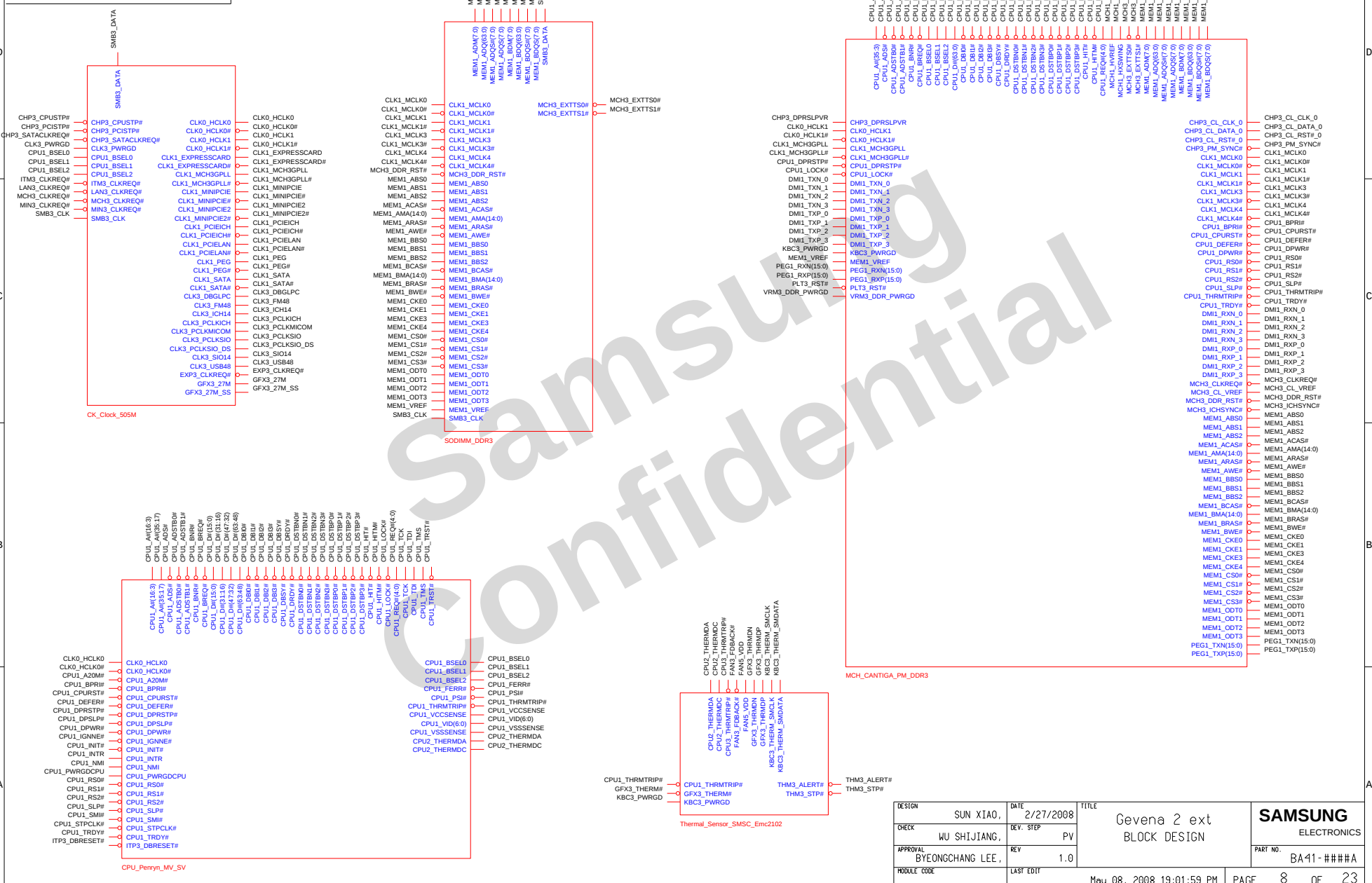
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APPROVAL	BYEONGCHANG LEE,	REV	1.0	POWER RAILS	PART NO.	BA41-####A
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	5	OF 23

Timing Diagram, Power ON Rev. 1.0 2008-05--5

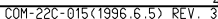


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APPROVAL	BYEONGCHANG LEE,	REV	1.0	CLOCK DIAGRAM		PART NO. BA41-####A
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	7	OF 23

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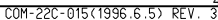


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D:/mentor/Geneva2/Geneva2_ext_PV_050

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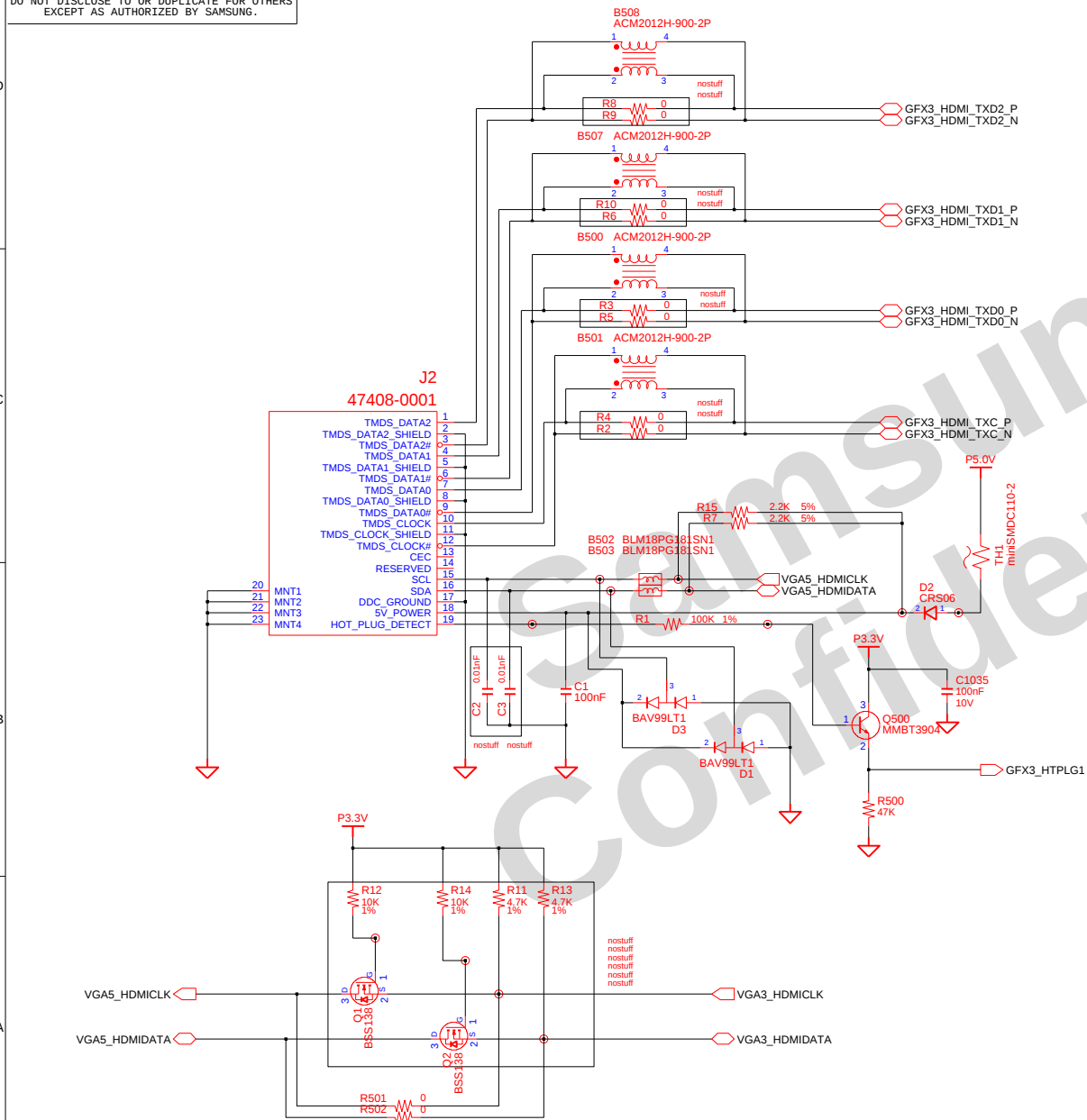
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SRP Sheet Number: 11 of 78

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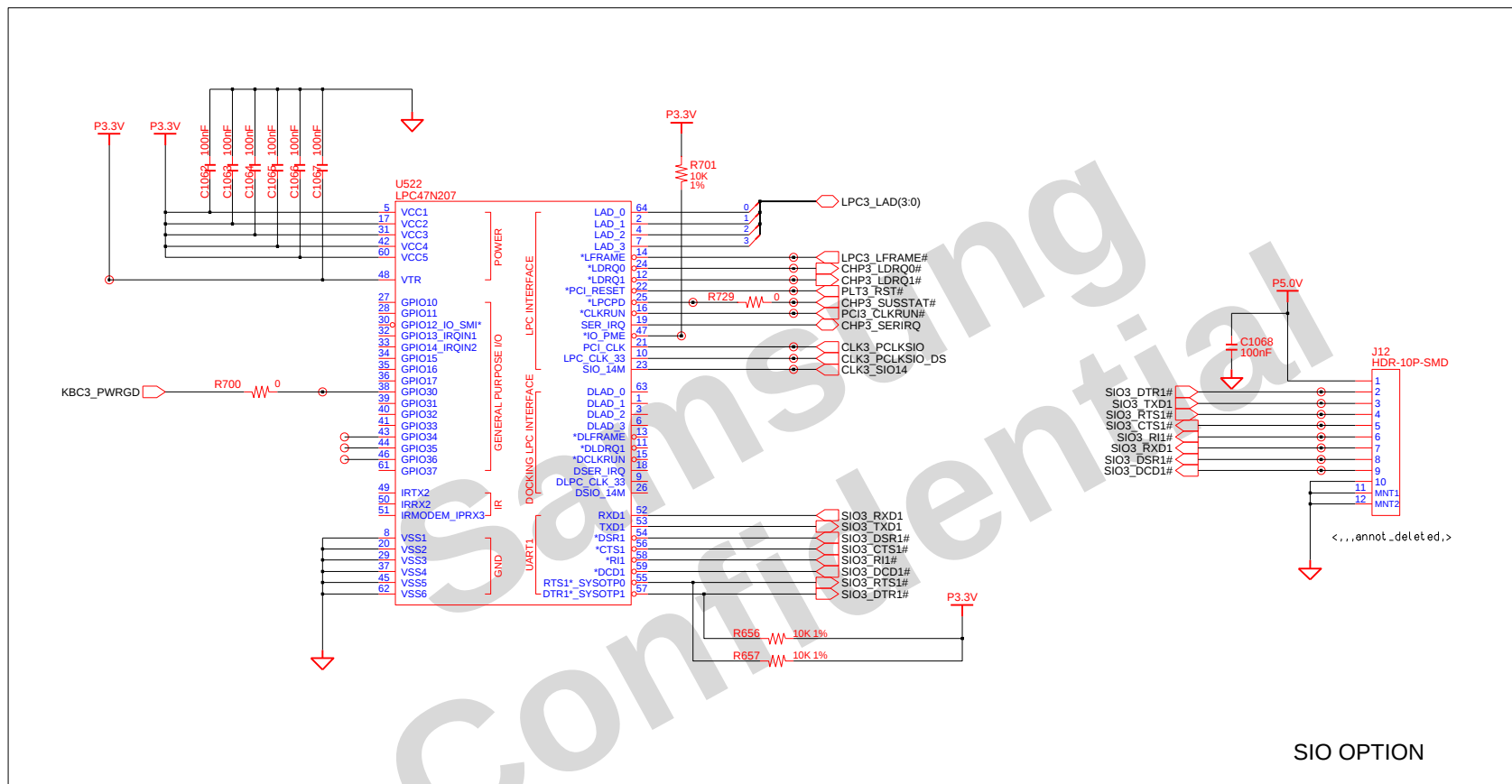
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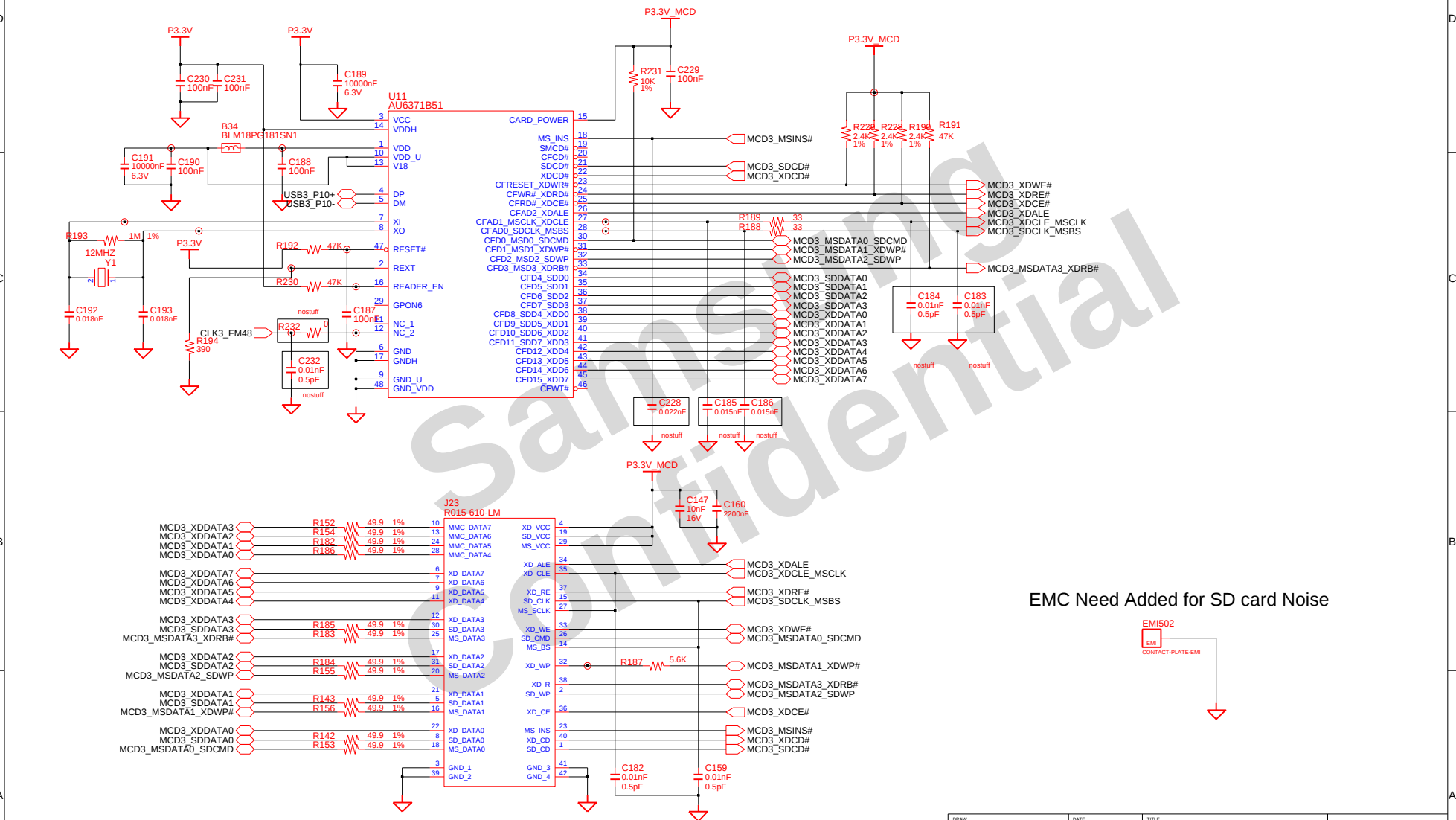
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CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT				
				May 08, 2008 19:01:59 PM	PAGE 30 OF	

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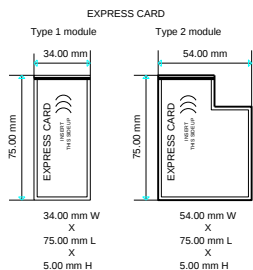
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CHECK	WU SHIJIANG,	REV	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
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DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG
CHECK	WU SHIJIANG,	DEV. STEP	PV		CARDREADER 7 IN 1	ELECTRONICS
APPROVAL	BYEONGCHANG LEE,	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM			BA41-####A
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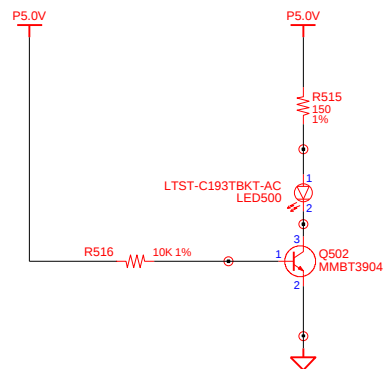
J508
EXPRESS-26P-FRAME

1	MNT1
2	MNT2

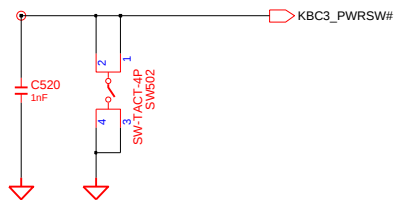
ORAW	SUN XIAO,	DATE	2/27/2008	Gevena 2 ext MIO BOARD EXPRESS CARD			
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO.	
APPROVAL	BYEONGCHANG LEE,	REV	1.0			BA41-####	
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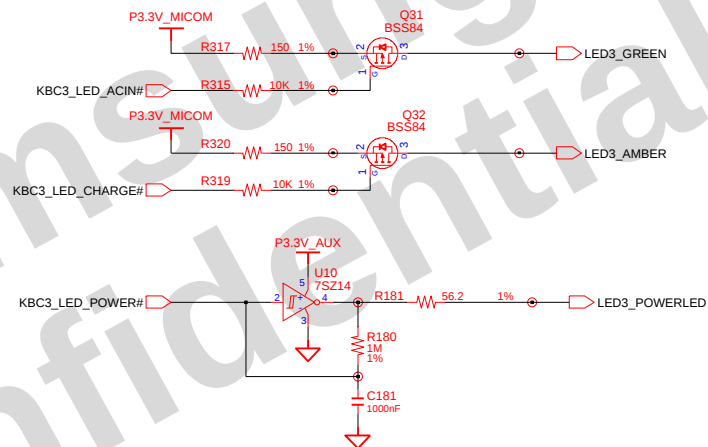
POWER ON LED



POWER ON SW BUTTON



ADAPTERIN/CHARGING LED



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		MICOM	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		MICOM LOGIC SCH	
MODULE CODE		LAST EDIT				PART NO. BA41-####A
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SIGNAL SWITCH

Switched Power On (P5V)

Switched Power On (P3.3V)

Switched Power On (P1.5V)

Table:

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		MAIN	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		SWITCH POWER P1.5V	
MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 18 OF 23

SIGNAL SWITCH

Switched Power On (P5V)

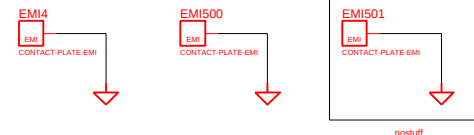
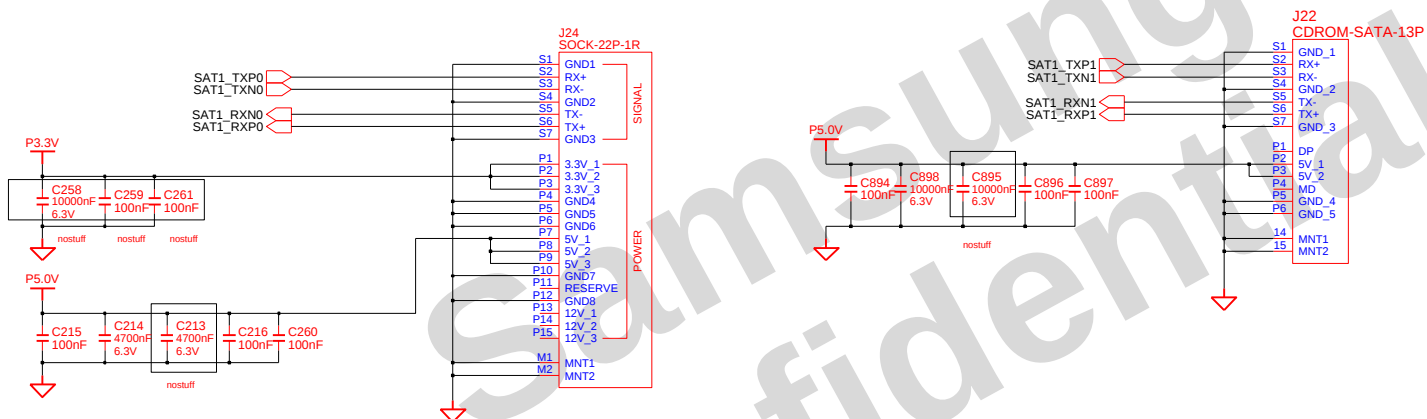
Switched Power On (P3.3V)

Switched Power On (P1.5V)

DRAW		DATE		TITLE		SAMSUNG ELECTRONICS	
SUN XIAO,		2/27/2008					
CHECK		REV. STEP					
WU SHIJIAN,		PV		Gevena 2 ext MAIN SWITCH POWER P1.5V		PART NO.	
APPROVAL		REV				BA41-####A	
BYEONGCHANG LEE,		1.0					
MODULE CODE		LAST EDIT		May 08, 2006 19:01:59 PM		PAGE	18 OF 23

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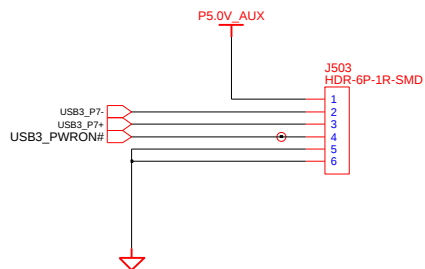
Main to HDD



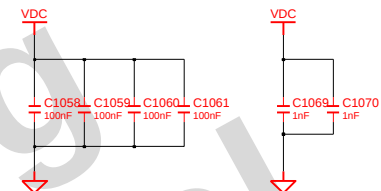
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext CONNECTOR	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDD & ODD CONNECTOR	
MODULE CODE		LAST EDIT		May 08, 2008 19:01:59 PM	PAGE 19 OF 23	

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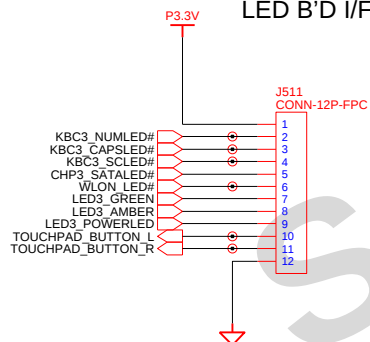
USB I/F B'D



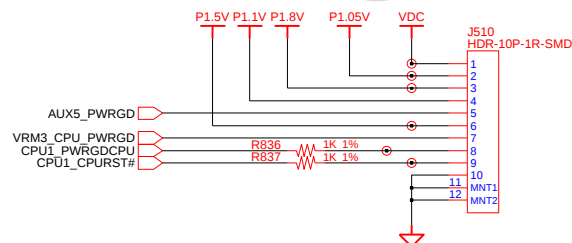
EMC ADD decap CAP



LED B'D I/F



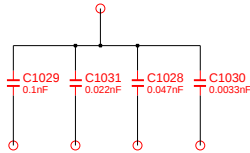
ICT PORT



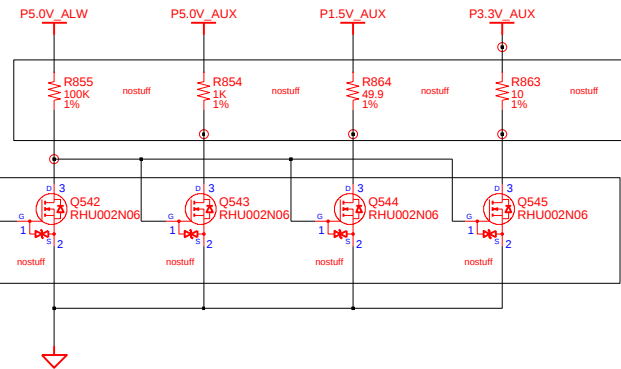
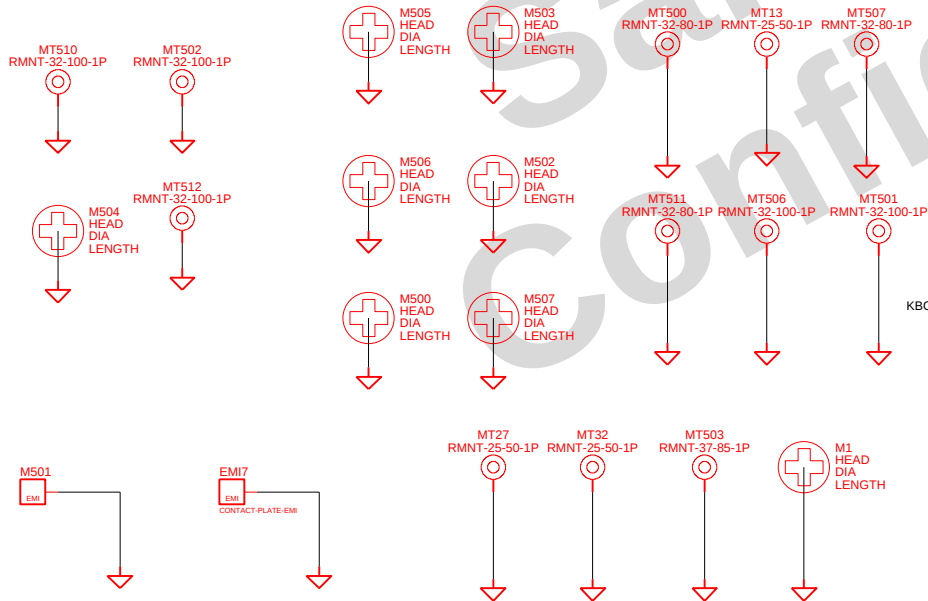
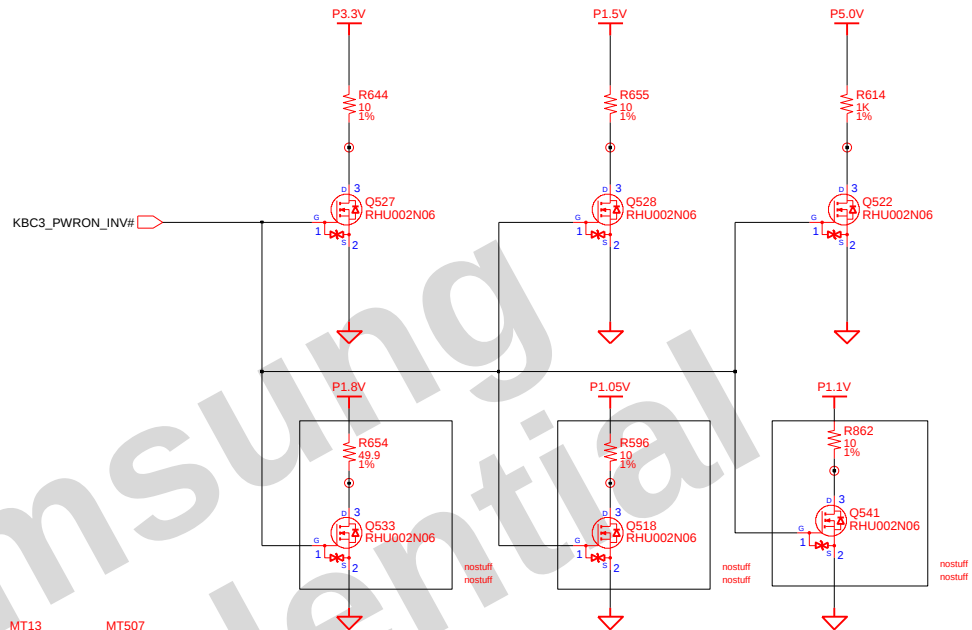
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIAN,	DEV. STEP	PV	KEYBOARD 80PORT ICT PORT		
APPROVAL	BYEONGCHANG LEE,	REV	1.0	LID SWITCH LED B'D USB I/O B'D	PART NO.	BA41-####A
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TOP SIDE



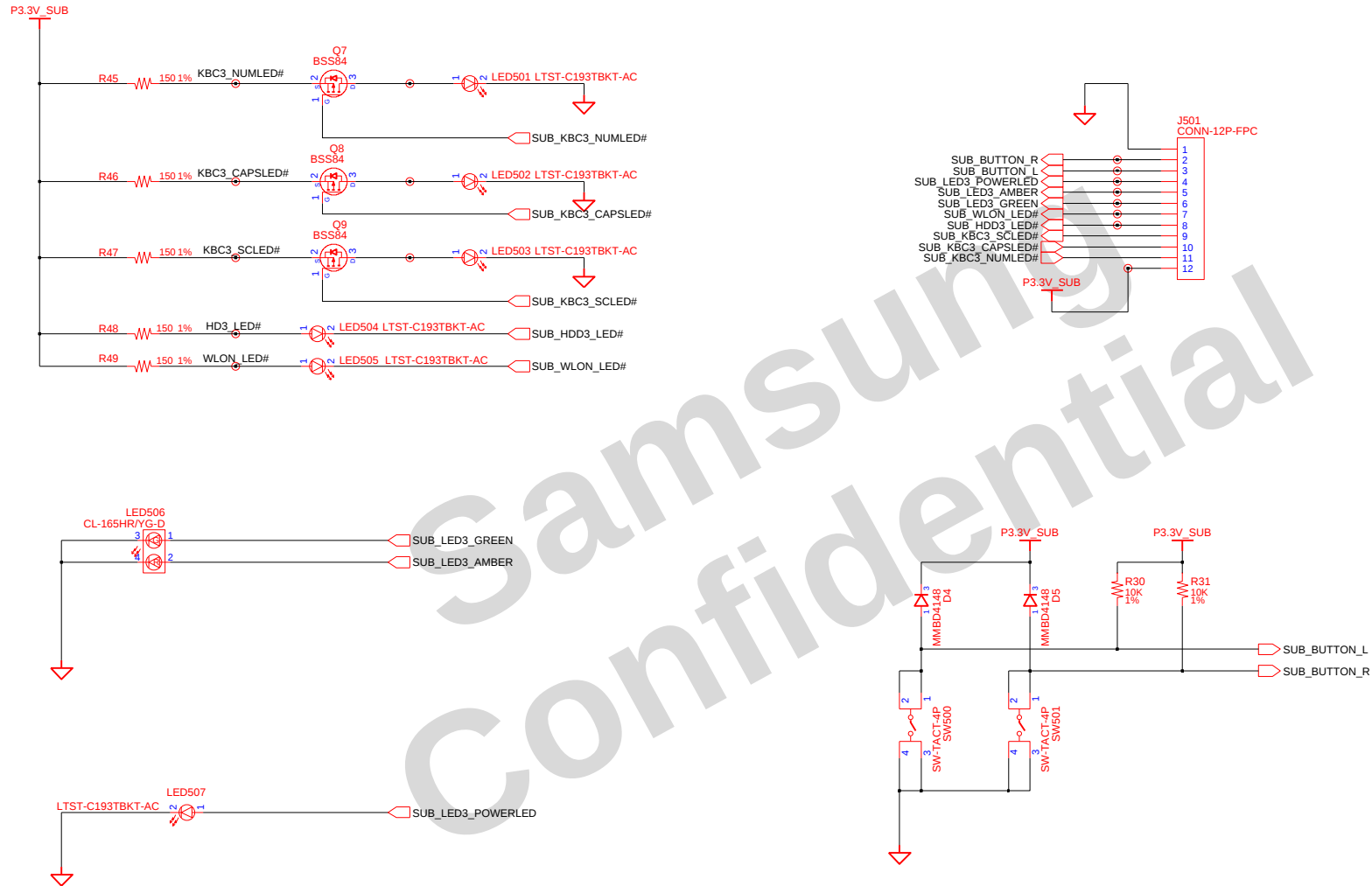
BOTTOM SIDE



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext OTHERS	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	21 OF 23	

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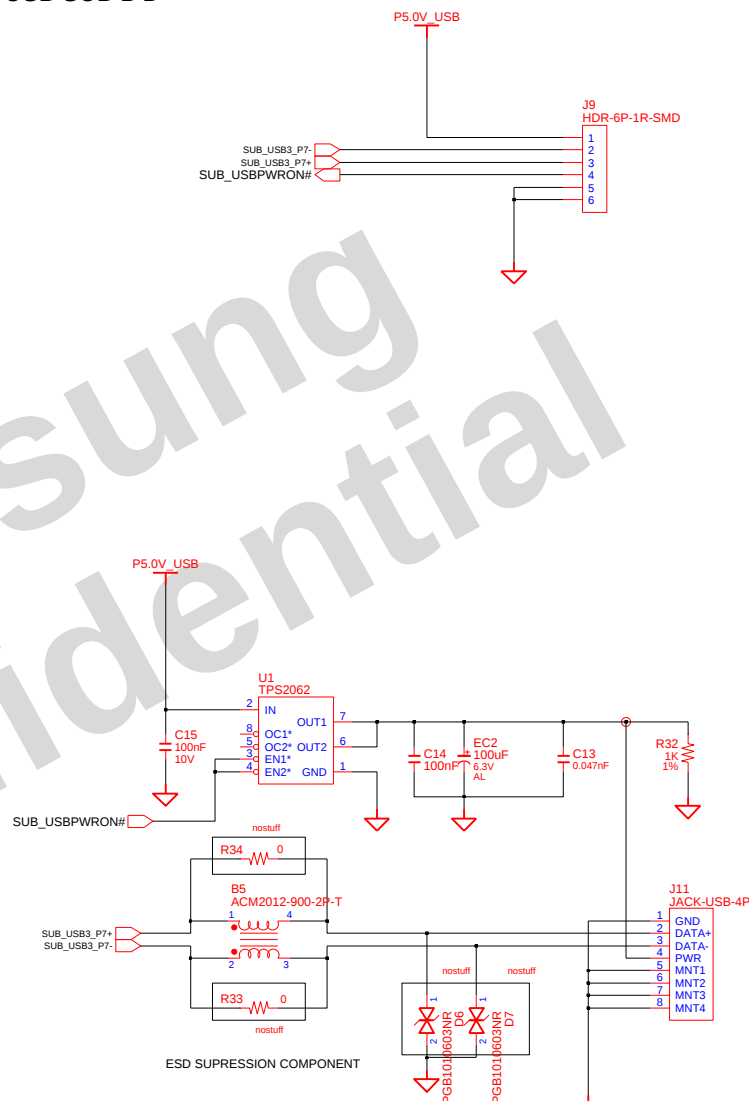
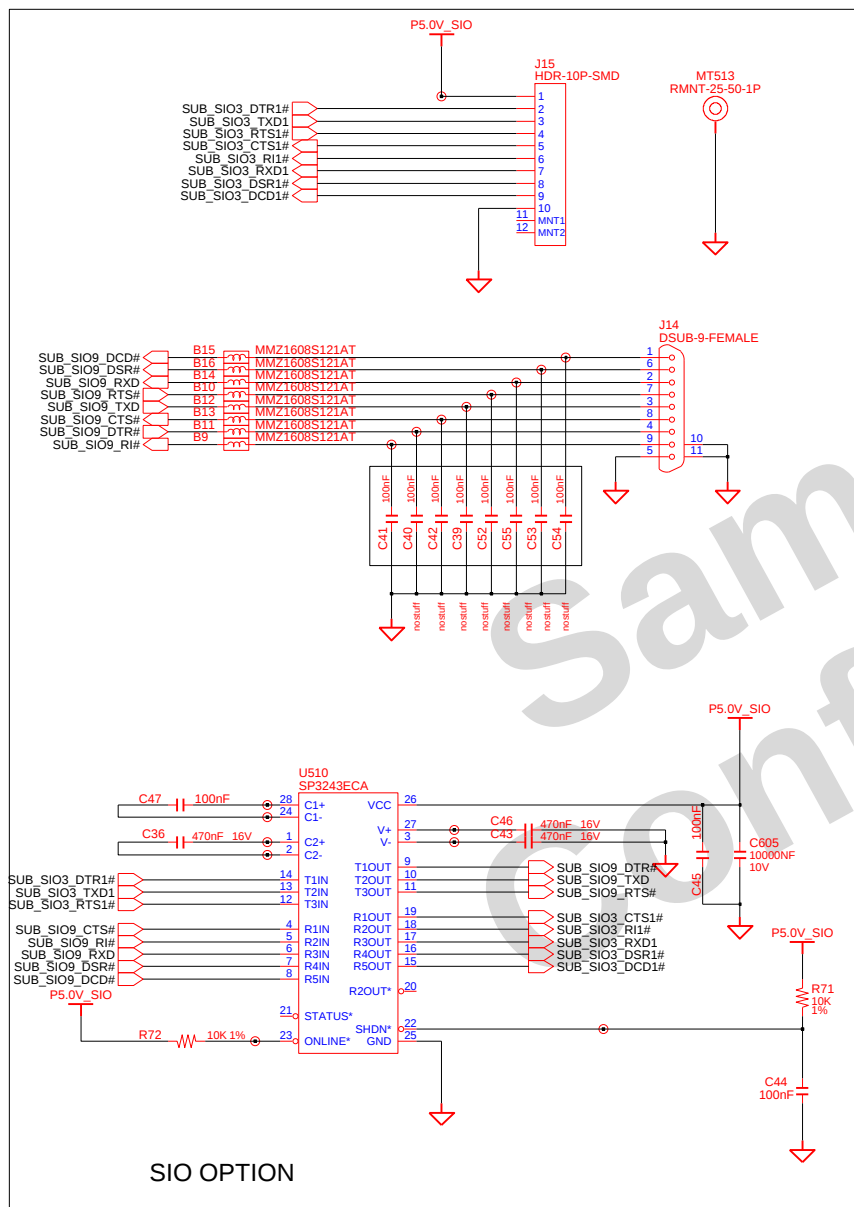
TOUCHPAD AND LED B'D



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext TOUCHPAD AND LED B'D	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT				
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SIO AND USB SUB B'D



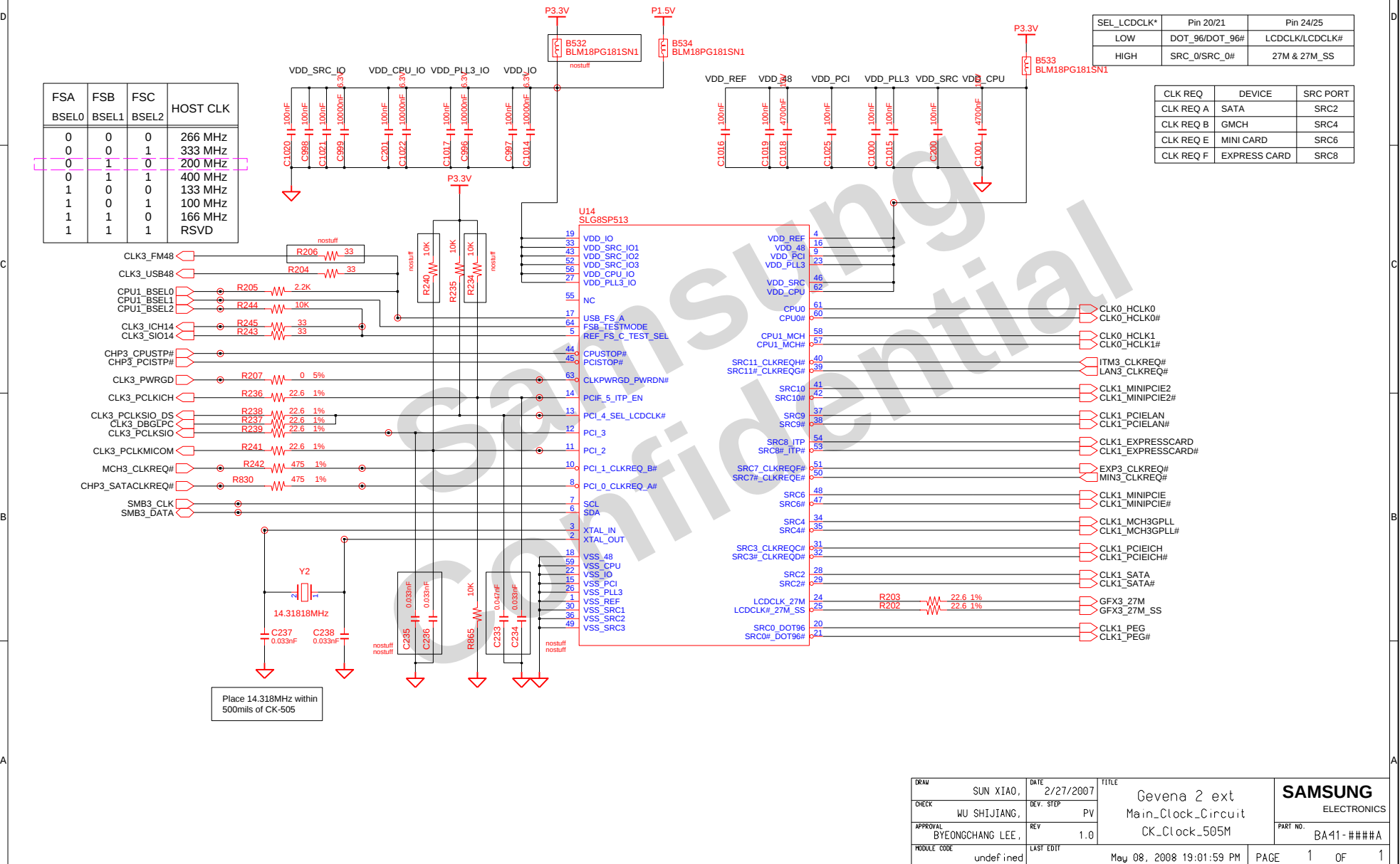
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SUN XIAO,		2/27/2008		Gevena 2 ext		ELECTRONICS	
CHECK		DEV. STEP		MIO BOARD		PART NO.	
WU SHIJIANG,		PV		USB AND SIO SUB B'D		BA141-####A	
APPROVAL		REV					
BYEONGCHANG LEE,		1.0					
MODULE CODE		LAST EDIT		May 08, 2008 19:01:59 PM		PAGE 23 OF 60	

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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

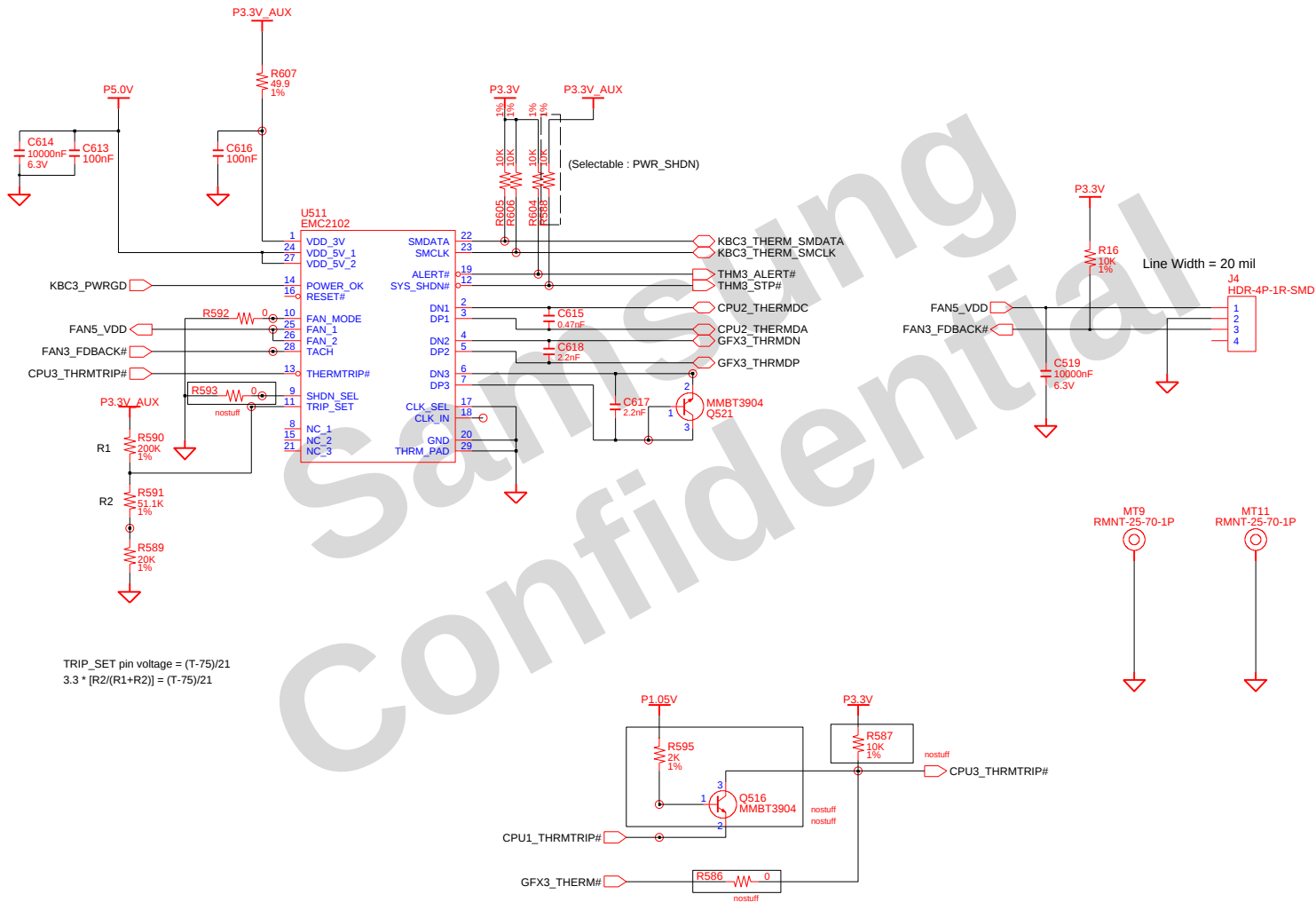
SEL_LCDCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCCLK/LCDCCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



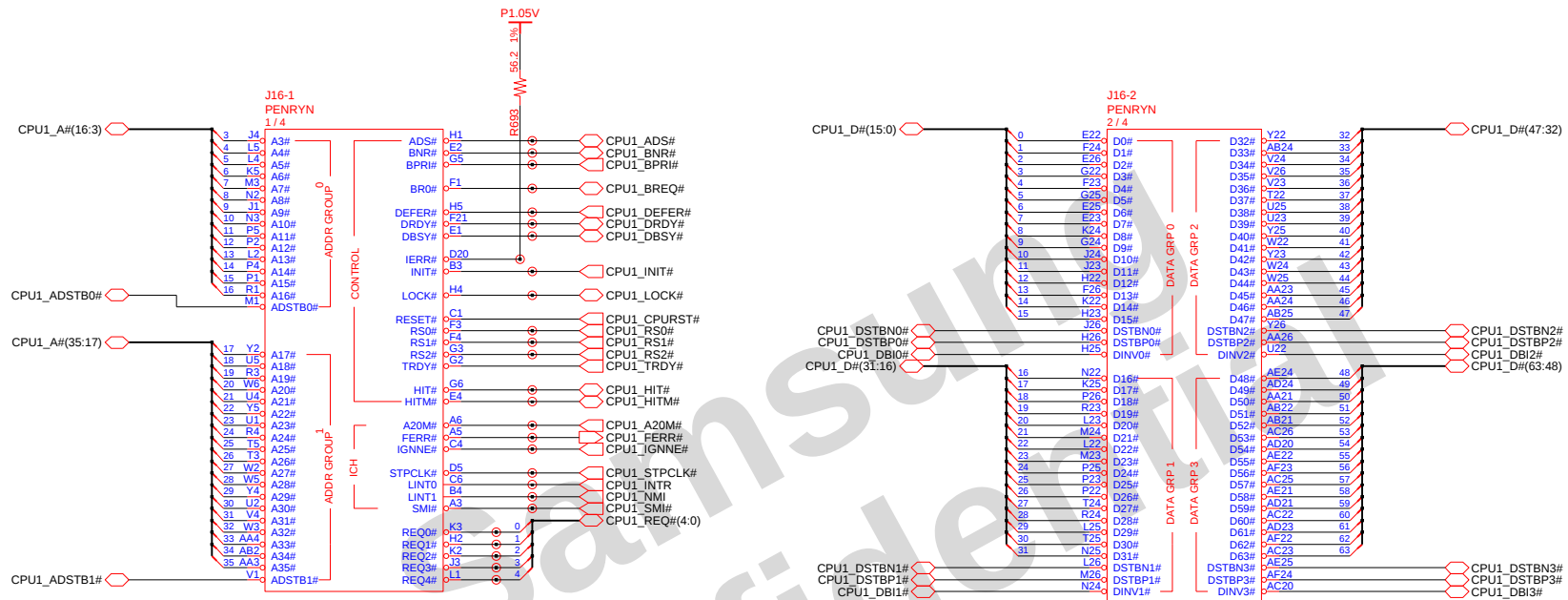
DRAW	SUN XIAO,	DATE	2/27/2007	TITLE	Gevena 2 ext Main_Clock_Circuit CK-Clock_505M	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

THERMAL SENSOR & FAN CONTROL

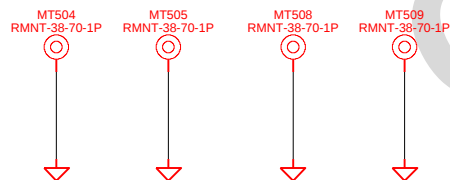


DESIGN	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
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APPROVAL	BYEONGCHANG LEE,	REV	1.0	THERMAL_SENSOR_SMSC_EMC2102		
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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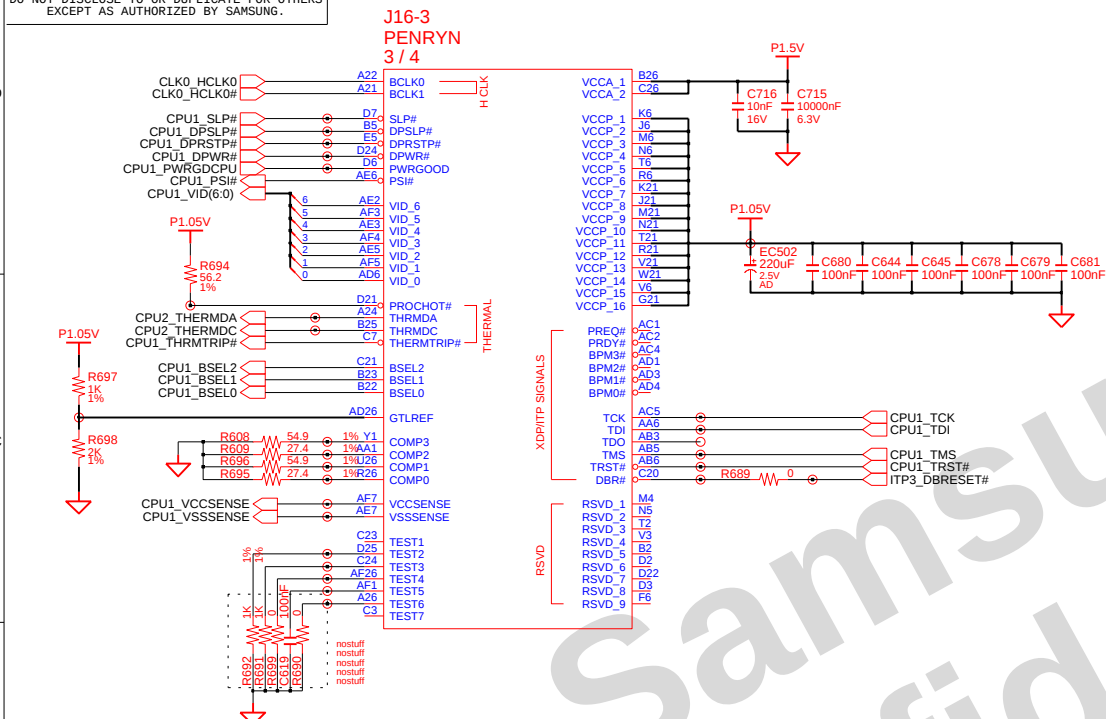


CPU CONNECTOR P/N 3704-001153



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext CPU PENRYN (1/3)	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV			
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 3	

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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 0	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 0 0 0	0.8125 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2125 V
0 0 1 0 1 1 1	1.2125 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 1	0.6125 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 1	0.4875 V	1 1 1 1 0 0 1	0.0000 V
		1 0 1 0 0 1 0	0.4750 V	1 1 1 1 0 1 0	0.0000 V
		1 0 1 0 0 1 1	0.4625 V	1 1 1 1 0 1 1	0.0000 V
		1 0 1 0 1 0 0	0.4500 V	1 1 1 1 1 0 0	0.0000 V
		1 0 1 0 1 0 1	0.4375 V	1 1 1 1 1 0 1	0.0000 V
		1 0 1 0 1 1 0	0.4250 V	1 1 1 1 1 1 0	0.0000 V
		1 0 1 0 1 1 1	0.4125 V	1 1 1 1 1 1 1	0.0000 V
		1 0 1 1 0 0 0	0.4000 V		
		1 0 1 1 0 0 1	0.3875 V		
		1 0 1 1 0 1 0	0.3750 V		
		1 0 1 1 0 1 1	0.3625 V		
		1 0 1 1 1 0 0	0.3500 V		
		1 0 1 1 1 0 1	0.3375 V		
		1 0 1 1 1 1 0	0.3250 V		
		1 0 1 1 1 1 1	0.3125 V		
		1 1 0 0 0 0 0	0.3000 V		
		1 1 0 0 0 0 1	0.2875 V		
		1 1 0 0 0 1 0	0.2750 V		
		1 1 0 0 0 1 1	0.2625 V		
		1 1 0 0 1 0 0	0.2500 V		
		1 1 0 0 1 0 1	0.2375 V		
		1 1 0 0 1 1 0	0.2250 V		
		1 1 0 0 1 1 1	0.2125 V		
		1 1 0 1 0 0 0	0.2000 V		
		1 1 0 1 0 0 1	0.1875 V		
		1 1 0 1 0 1 0	0.1750 V		
		1 1 0 1 0 1 1	0.1625 V		
		1 1 0 1 1 0 0	0.1500 V		
		1 1 0 1 1 0 1	0.1375 V		
		1 1 0 1 1 1 0	0.1250 V		
		1 1 0 1 1 1 1	0.1125 V		
		1 1 1 0 0 0 0	0.1000 V		
		1 1 1 0 0 0 1	0.0875 V		
		1 1 1 0 0 1 0	0.0750 V		
		1 1 1 0 0 1 1	0.0625 V		
		1 1 1 0 1 0 0	0.0500 V		
		1 1 1 0 1 0 1	0.0375 V		
		1 1 1 0 1 1 0	0.0250 V		
		1 1 1 0 1 1 1	0.0125 V		
		1 1 1 1 0 0 0	0.0000 V		
		1 1 1 1 0 0 1	0.0000 V		
		1 1 1 1 0 1 0	0.0000 V		
		1 1 1 1 0 1 1	0.0000 V		
		1 1 1 1 1 0 0	0.0000 V		
		1 1 1 1 1 0 1	0.0000 V		
		1 1 1 1 1 1 0	0.0000 V		
		1 1 1 1 1 1 1	0.0000 V		

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

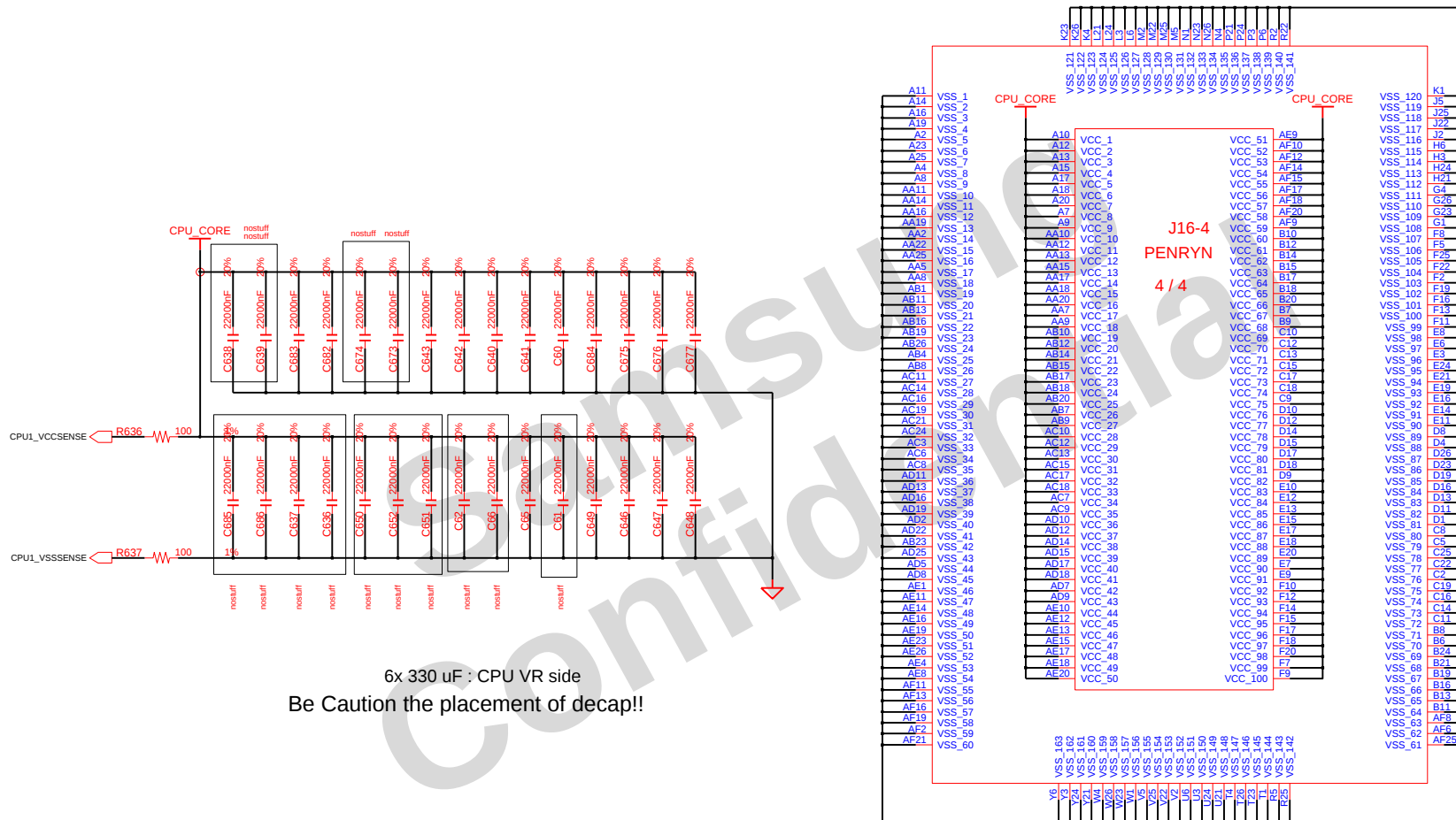
GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF pin with Zo=50ohm trace.
Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(50ohm)
trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSense at the end of the line.
Route the VCC/VSSense as a Zo=50ohm traces with equal length.
Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		CPU	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		PENRYN (<2/3)	
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	2 OF 3	

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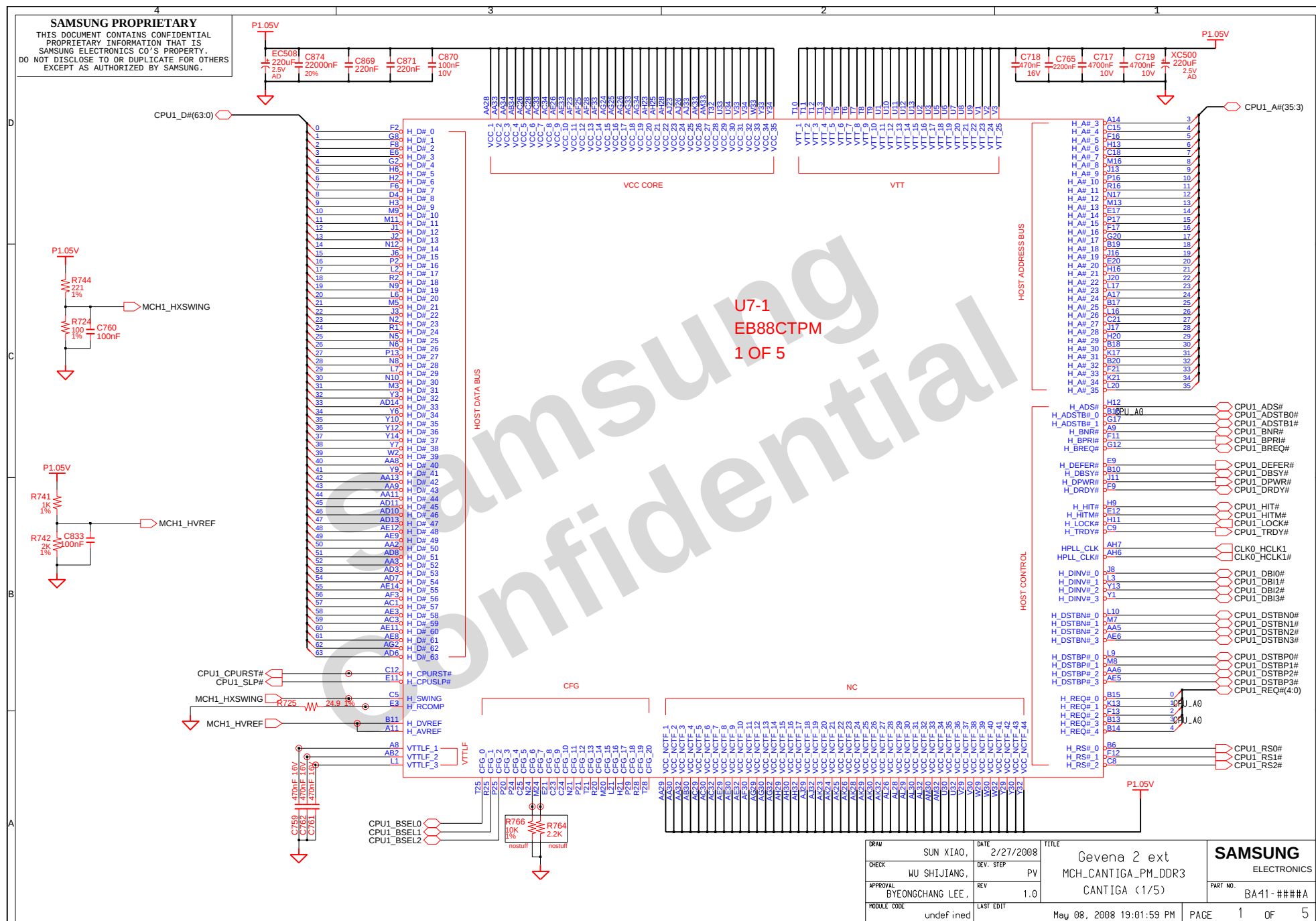


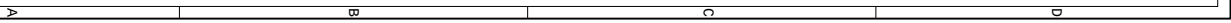
6x 330 uF : CPU VR side
Be Caution the placement of decap!!

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext
CHECK	WU SHIJIANG,	DEV. STEP	PV	CPU	
APPROVAL	BYEONGCHANG LEE,	REV	1.0	PENRYN (3/3)	
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	3 OF 3

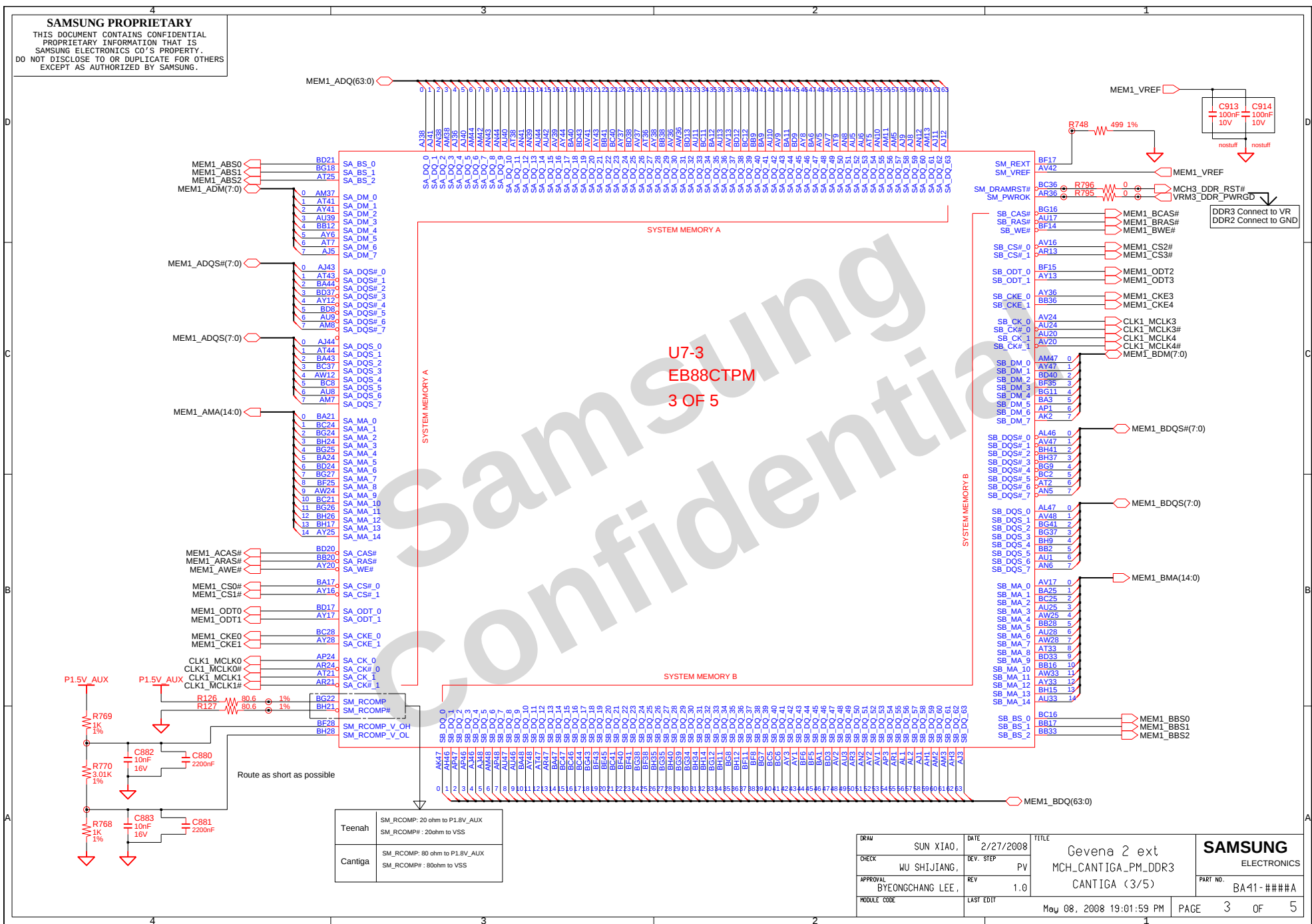
SAMSUNG
ELECTRONICS
PART NO. BA41-####A

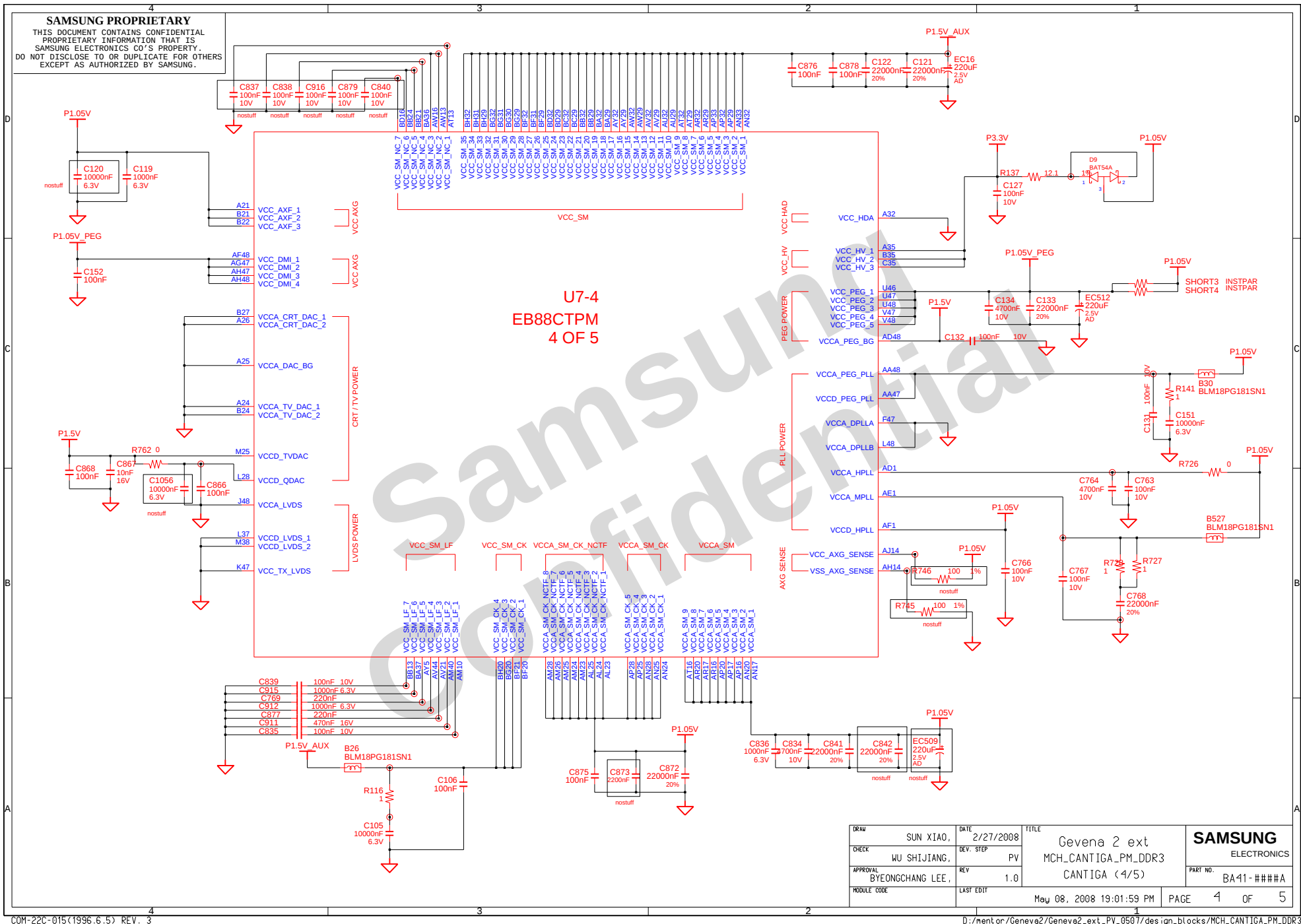
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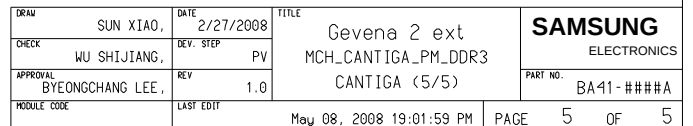


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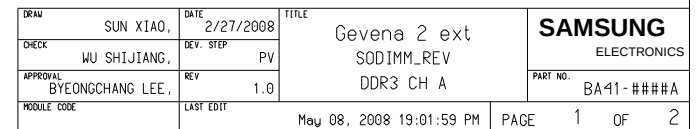


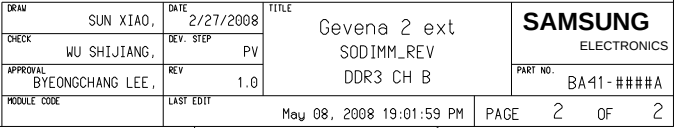


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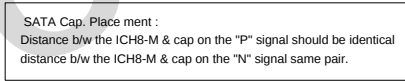


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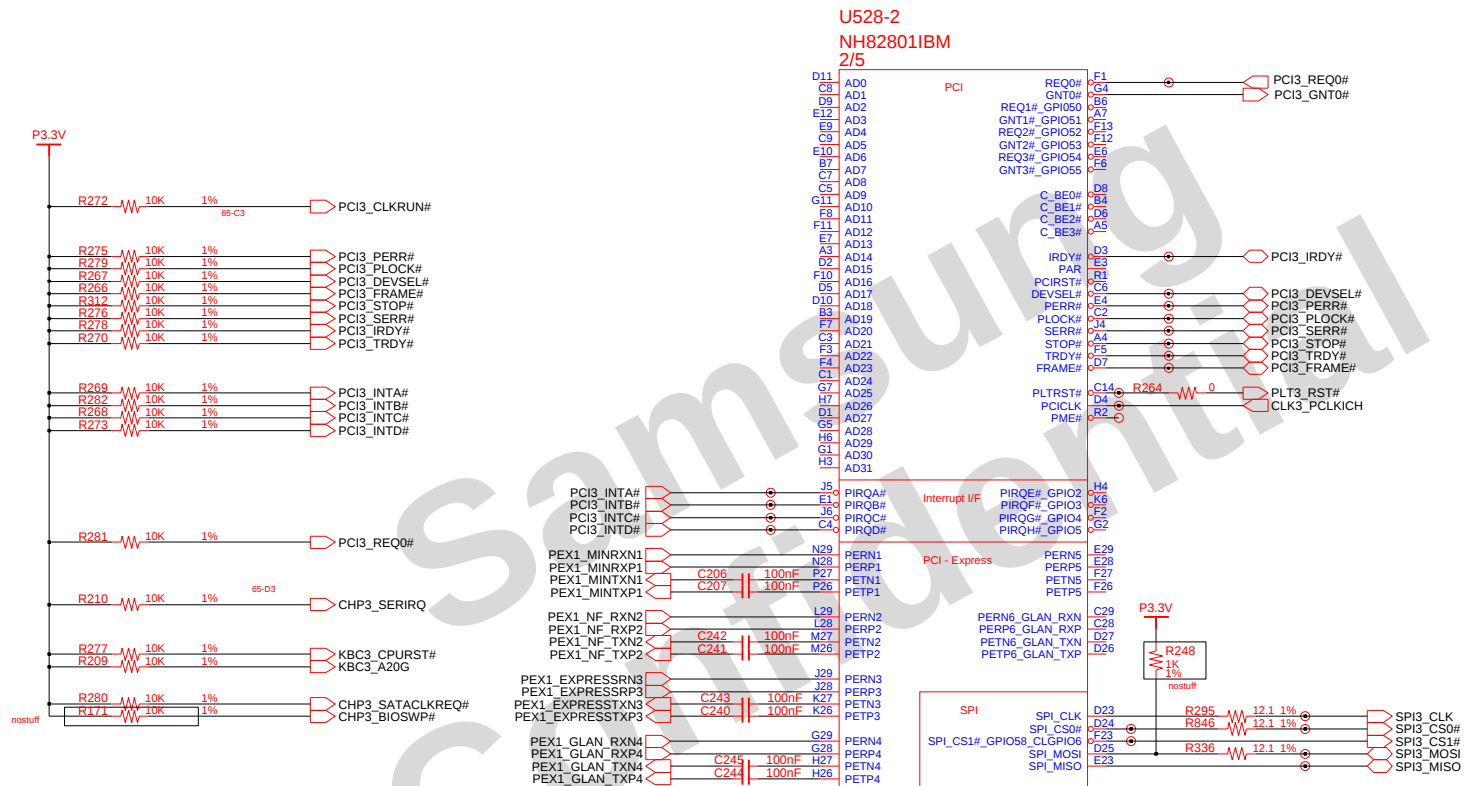


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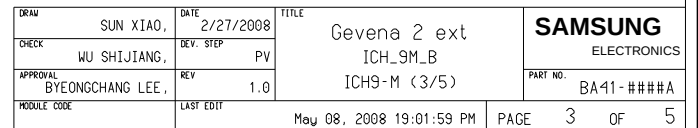
COM-22C-015(1996.6.5) REV. 3

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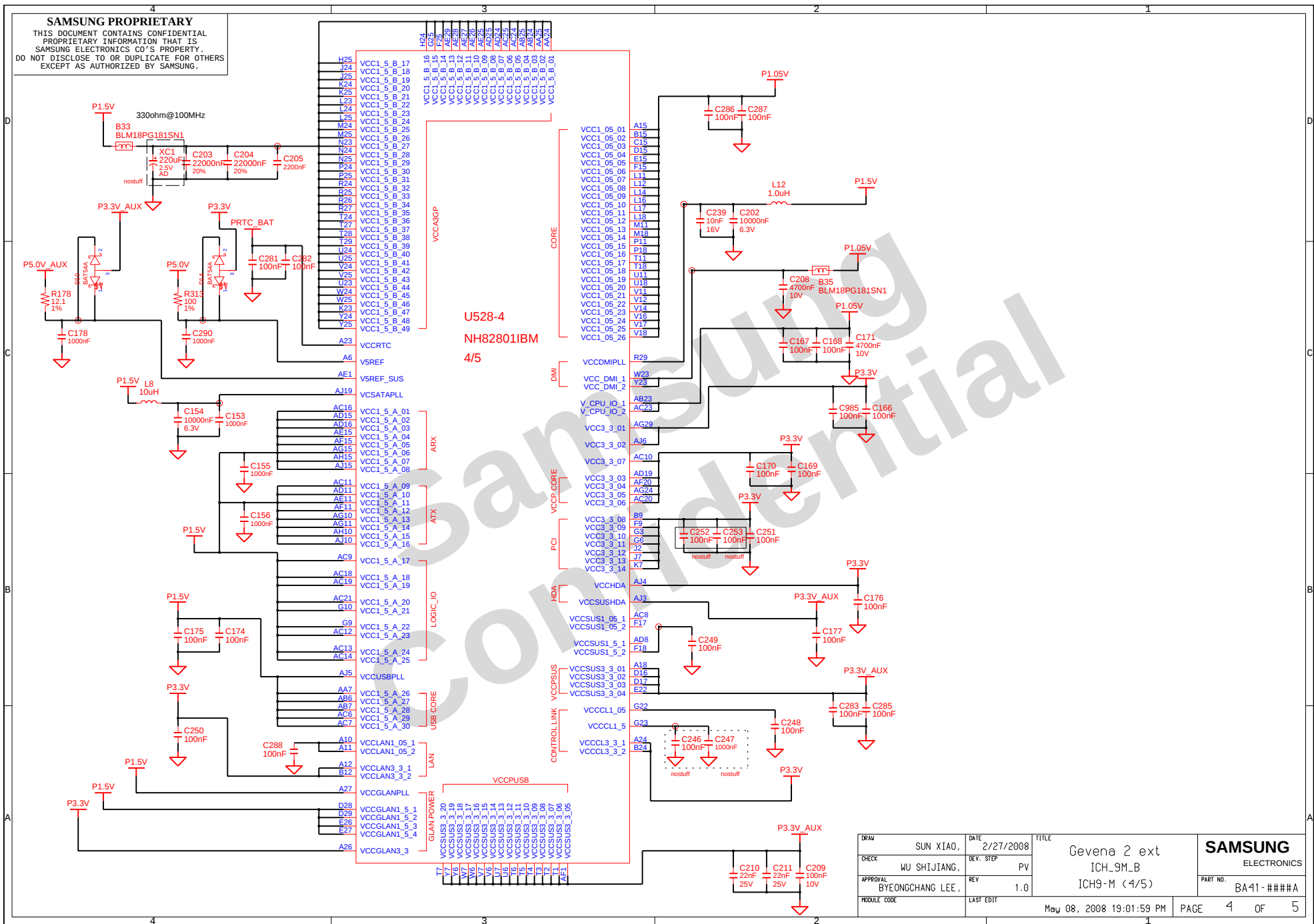


DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext ICH_9M_B	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		ICH9-M (2/5)	PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	2 OF 5	

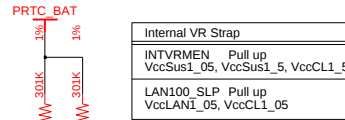
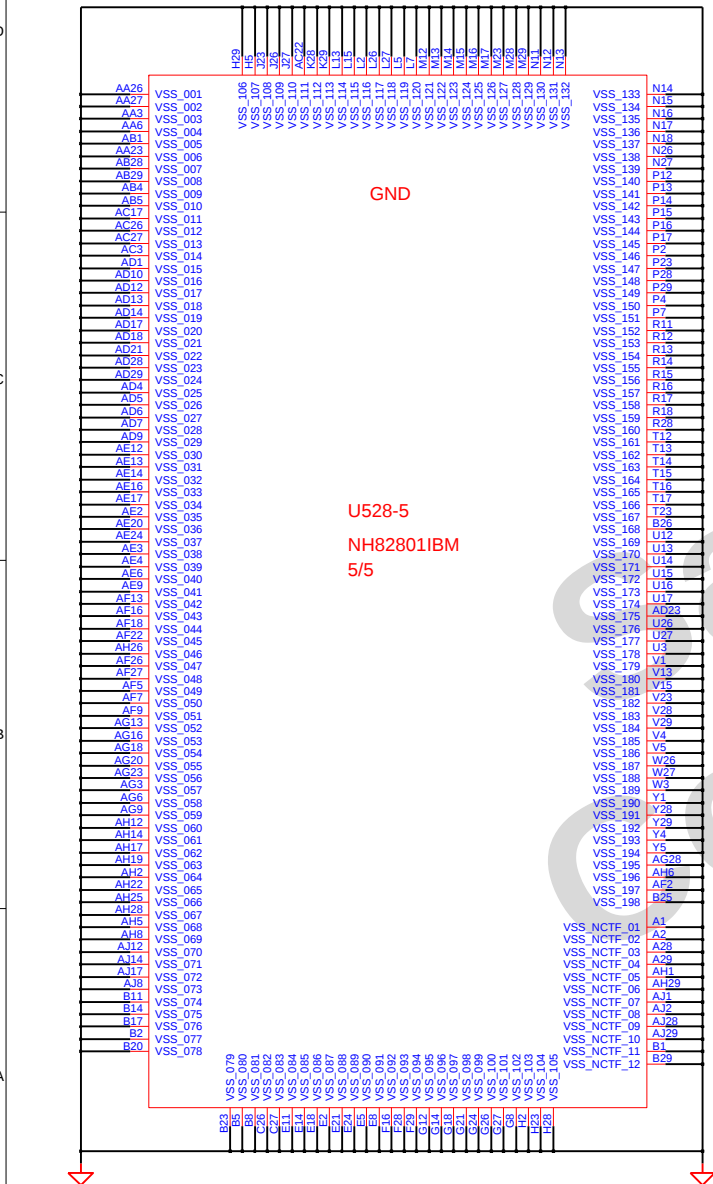
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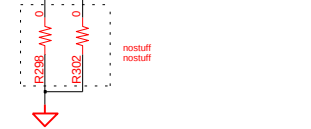
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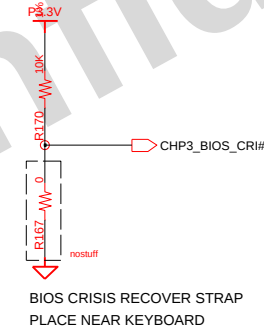
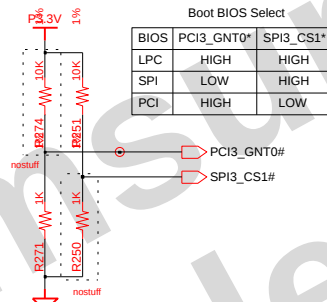
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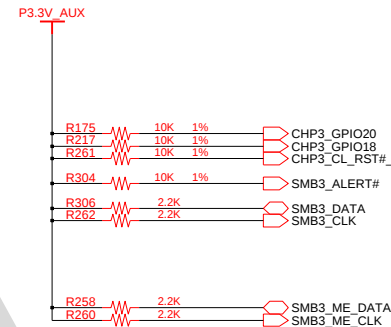
Internal VR Strap
INTVRMEN Pull up
VccSus1_05, VccSus1_5, VccCL1_5
LAN100_SLP Pull up
VccLAN1_05, VccCL1_05



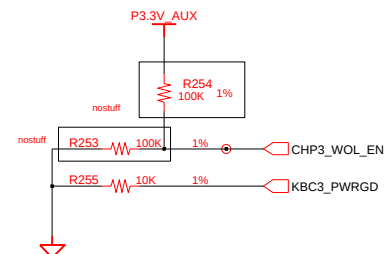
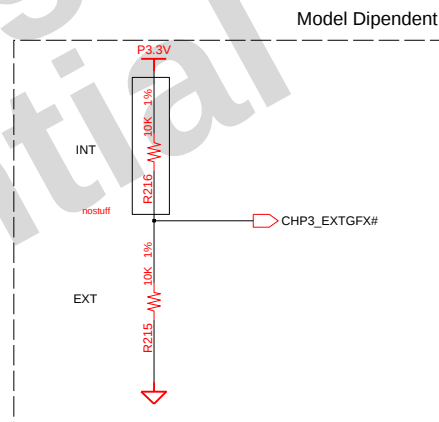
Boot BIOS Select		
BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD



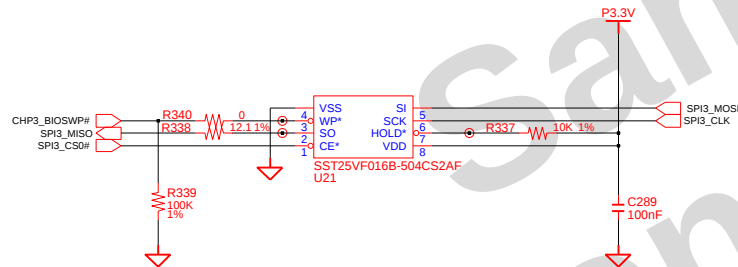
39-C3 38-C2 67-D1 65-C4
39-C3 38-C2 67-C1 65-C4



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Geneva 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		ICH9M_B	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		ICH9-M (5/5)	
MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 5 OF 5

- SPI ROM LIST -

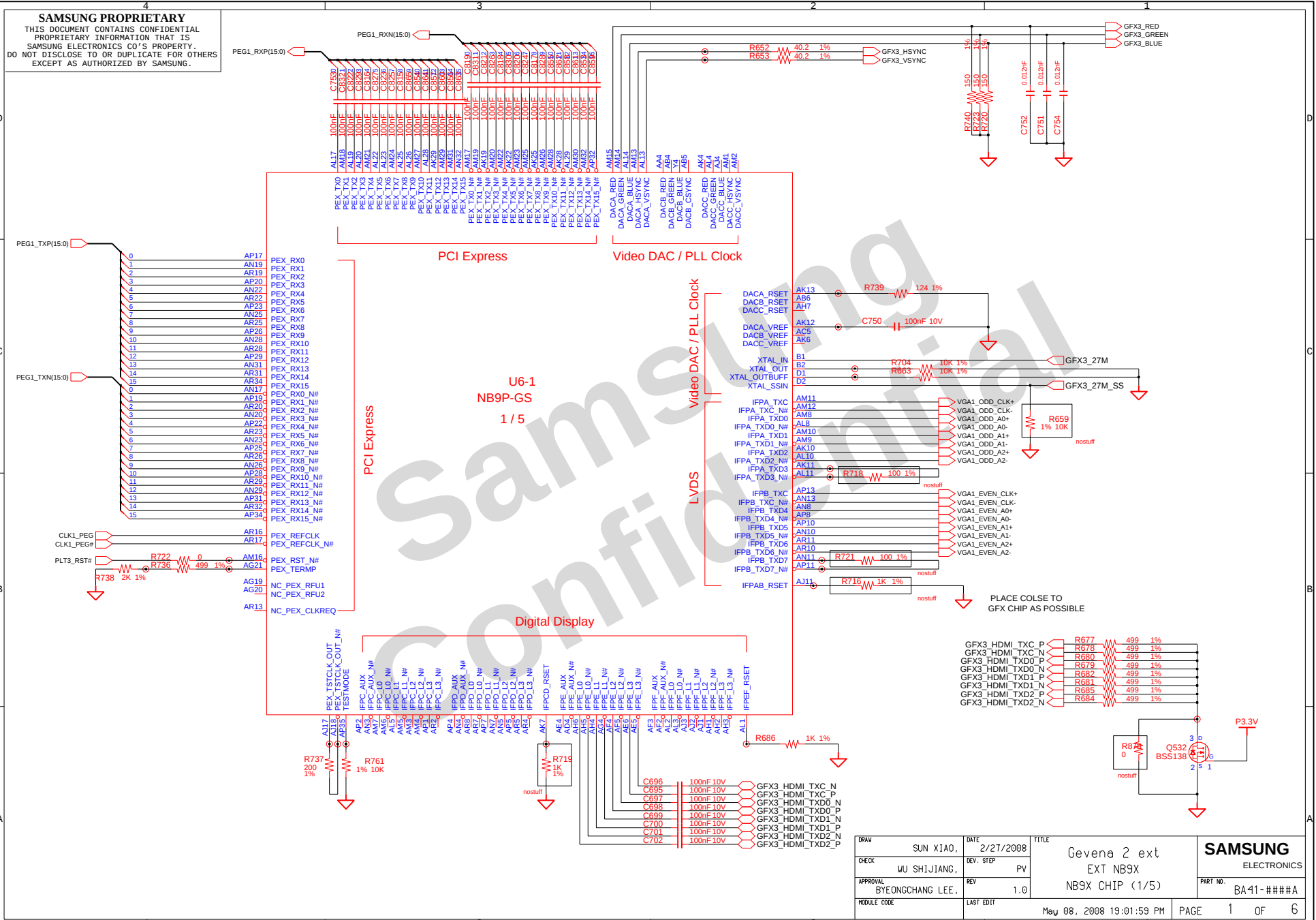
- Macronix - MX25L8005M2C-15G
- STM - M25PE80
- ATMEL - AT26DF081A-SU
- SST - 25VF080B-50-4C-S2AF
- WINBOND - W25X80-VSSI-G



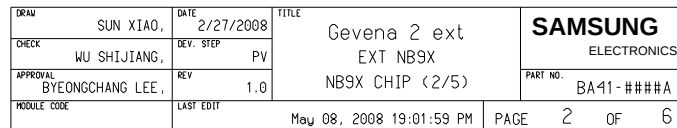
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		SPI1.BIOS_ROM	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		SPI1.BIOS_ROM	
MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 1 OF 1

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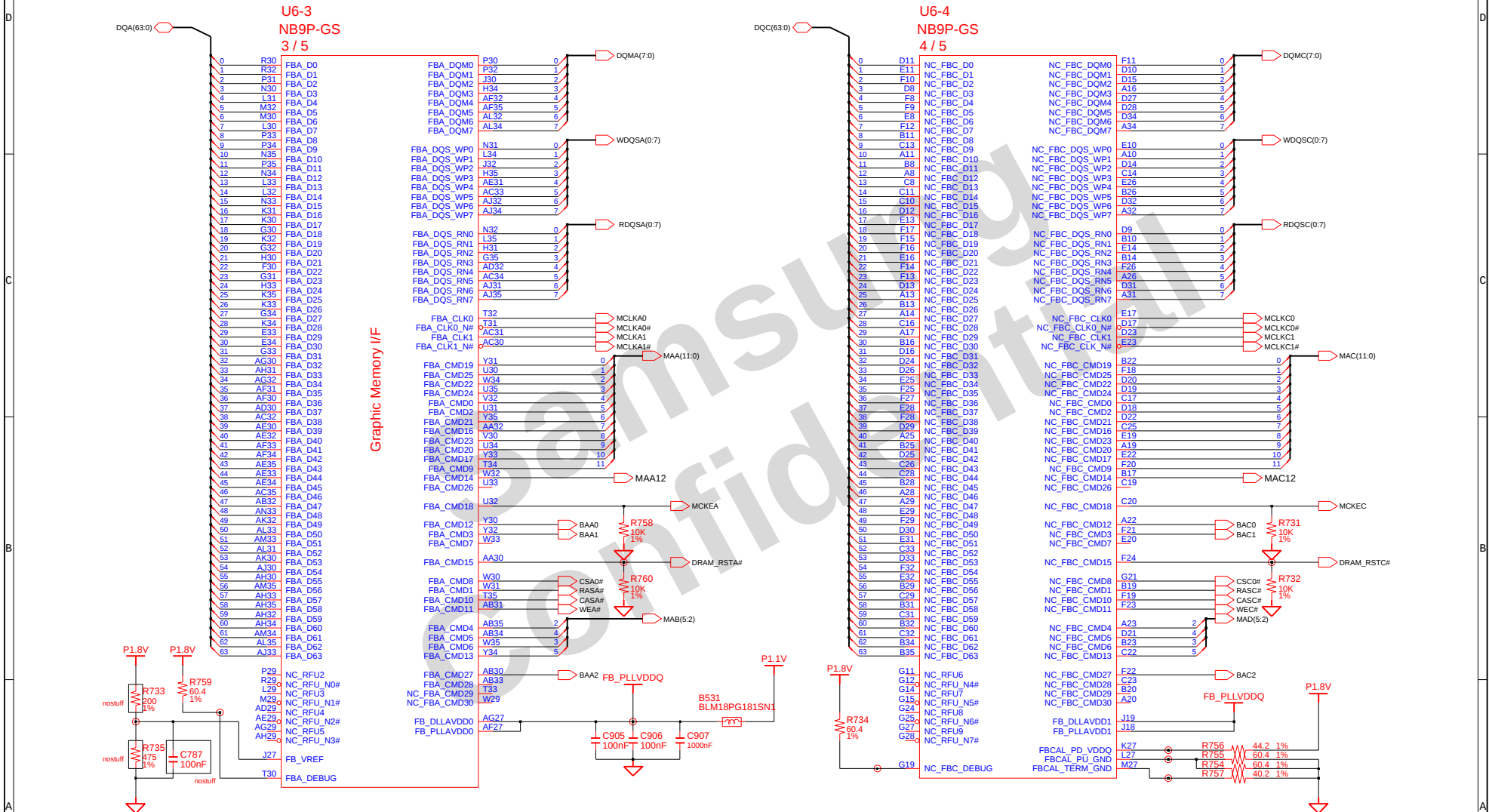
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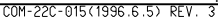


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Graphic Memory I/F (Using FBA Channel)

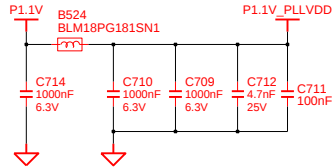
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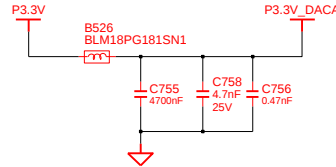


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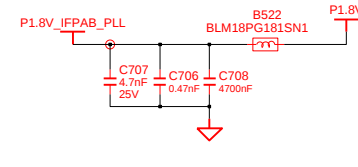
PLL_VDD



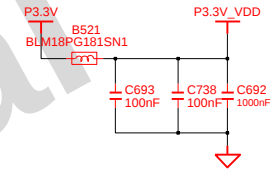
DACA/B/C



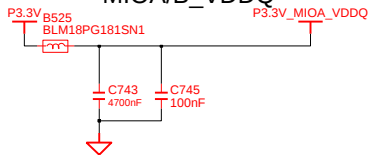
IFPAB_PLLVDD



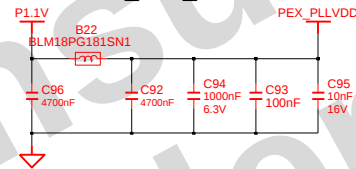
3.3V_VDD



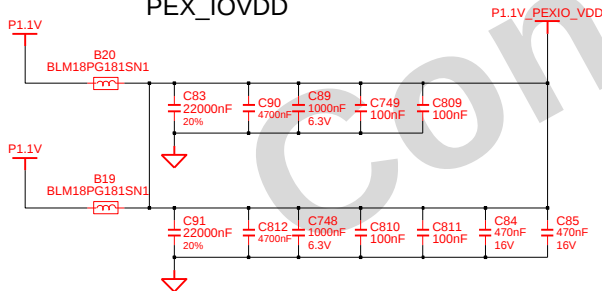
MIOA/B_VDDQ



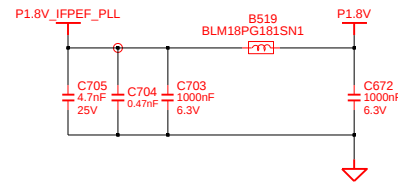
PEX_PLL_VDD



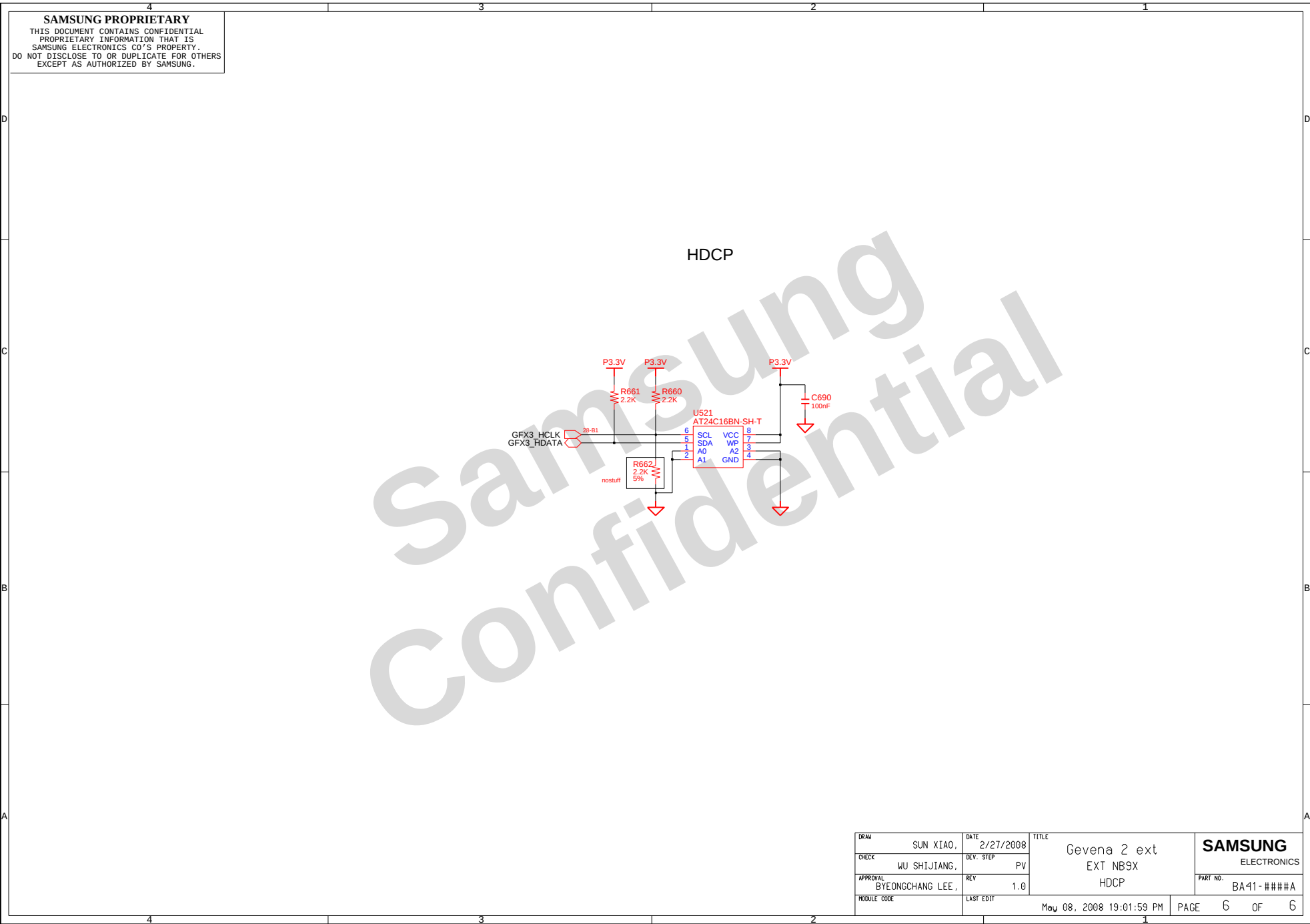
PEX_IOVDD



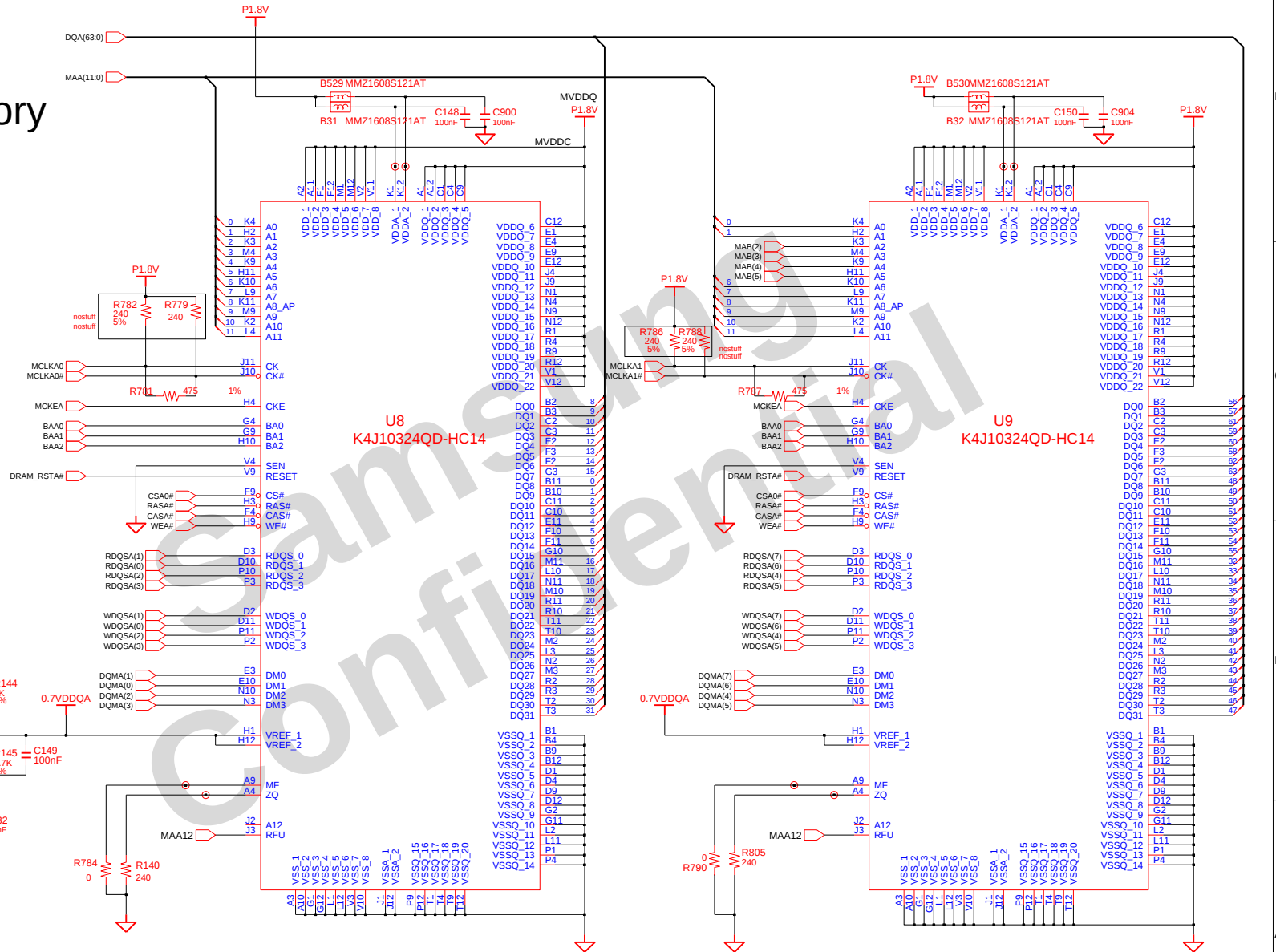
IFPEF_PLLVDD



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CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
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MODULE CODE		LAST EDIT				
				May 08, 2008 19:01:59 PM	PAGE 5 OF 6	

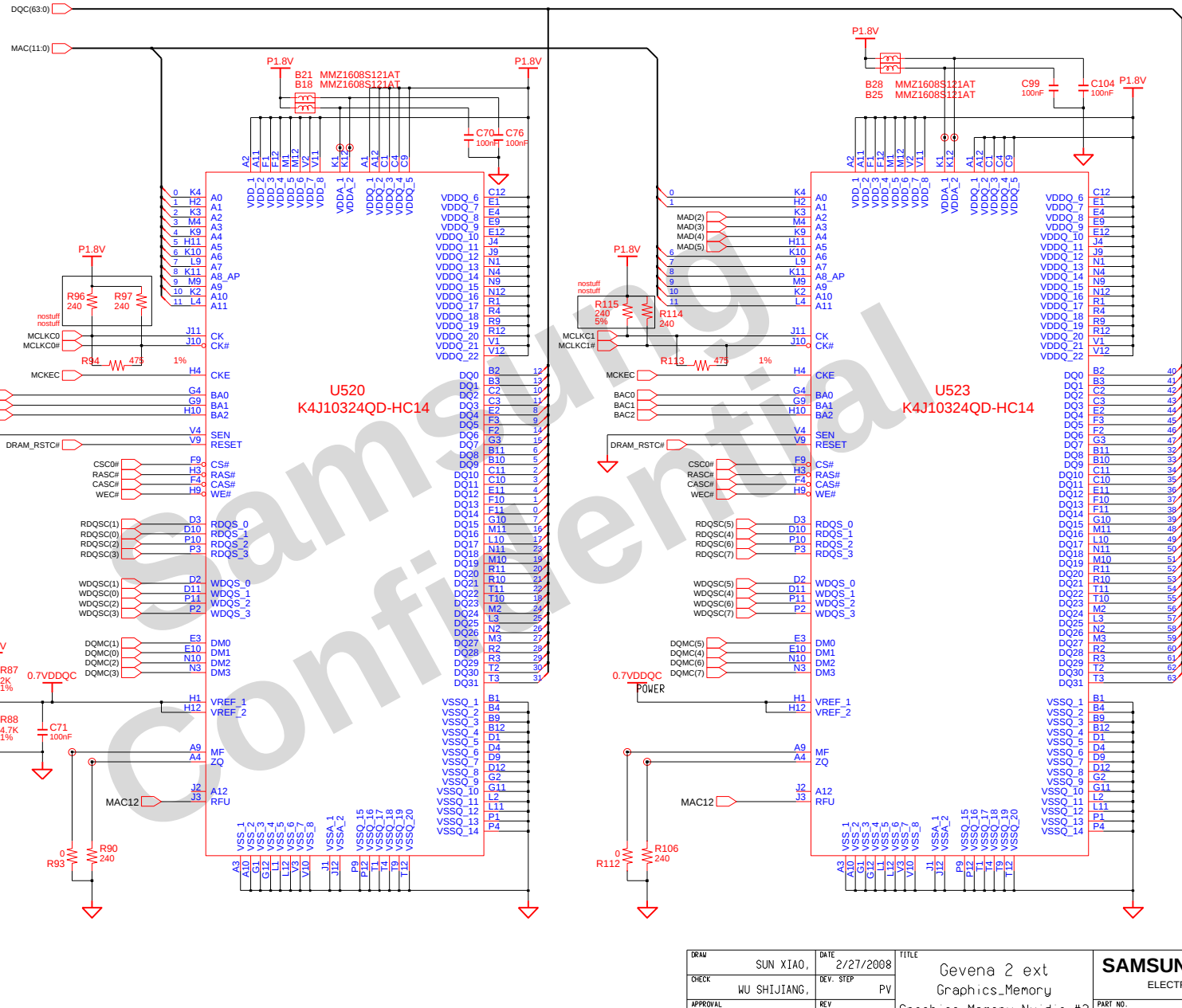


Video Memory (A Channel)



DRAM	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		Graphics_Memory	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		Graphics_Memory.Nvidia #1	
MODULE CODE		LAST EDIT				

Video Memory (C Channel)



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV		Graphics_Memory	
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MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 2 OF 2

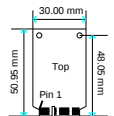
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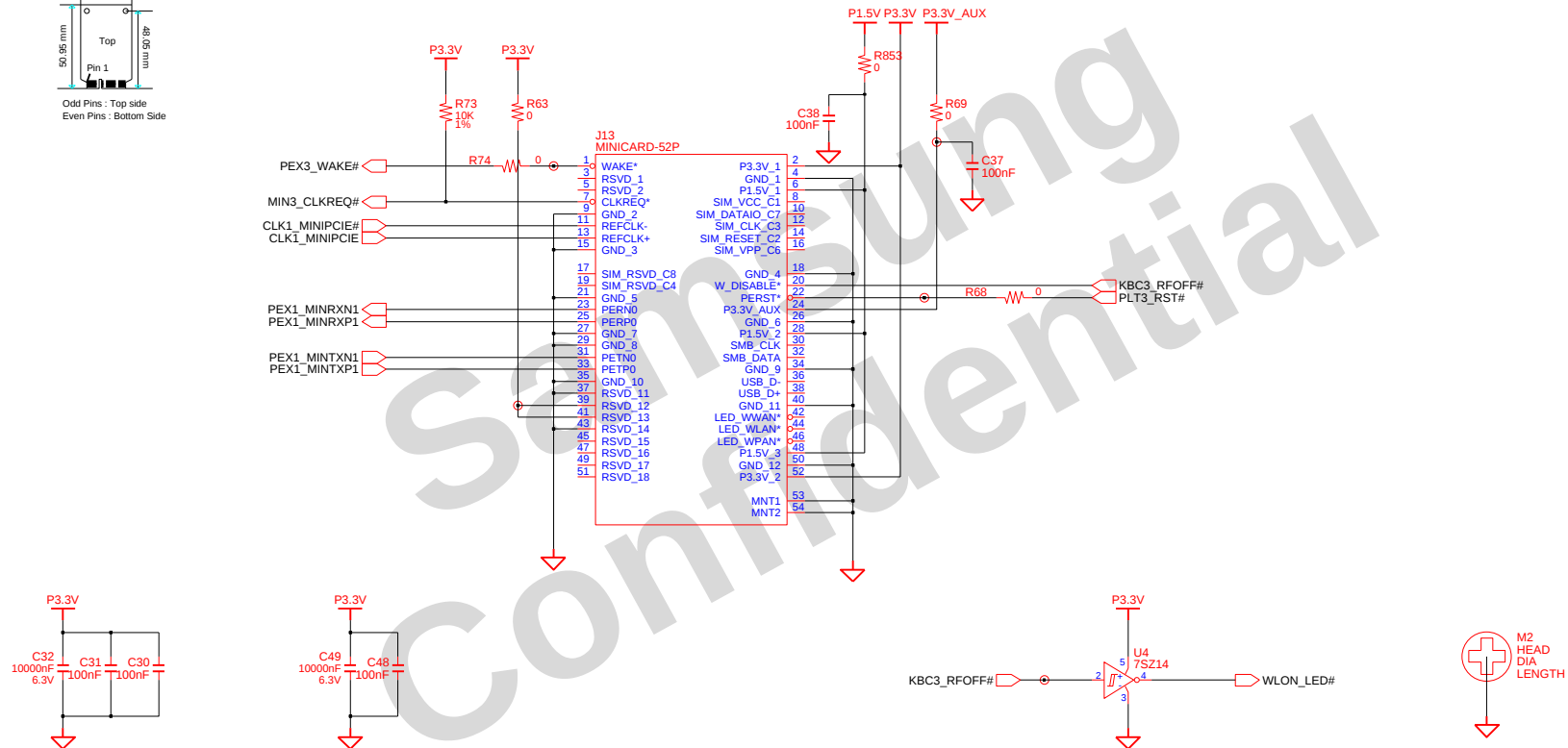
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APPROVAL	BYEONGCHANG LEE,	REV	1.0		
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM		
				PAGE	3 OF 3

Mini Card

Mini PCI Express Card

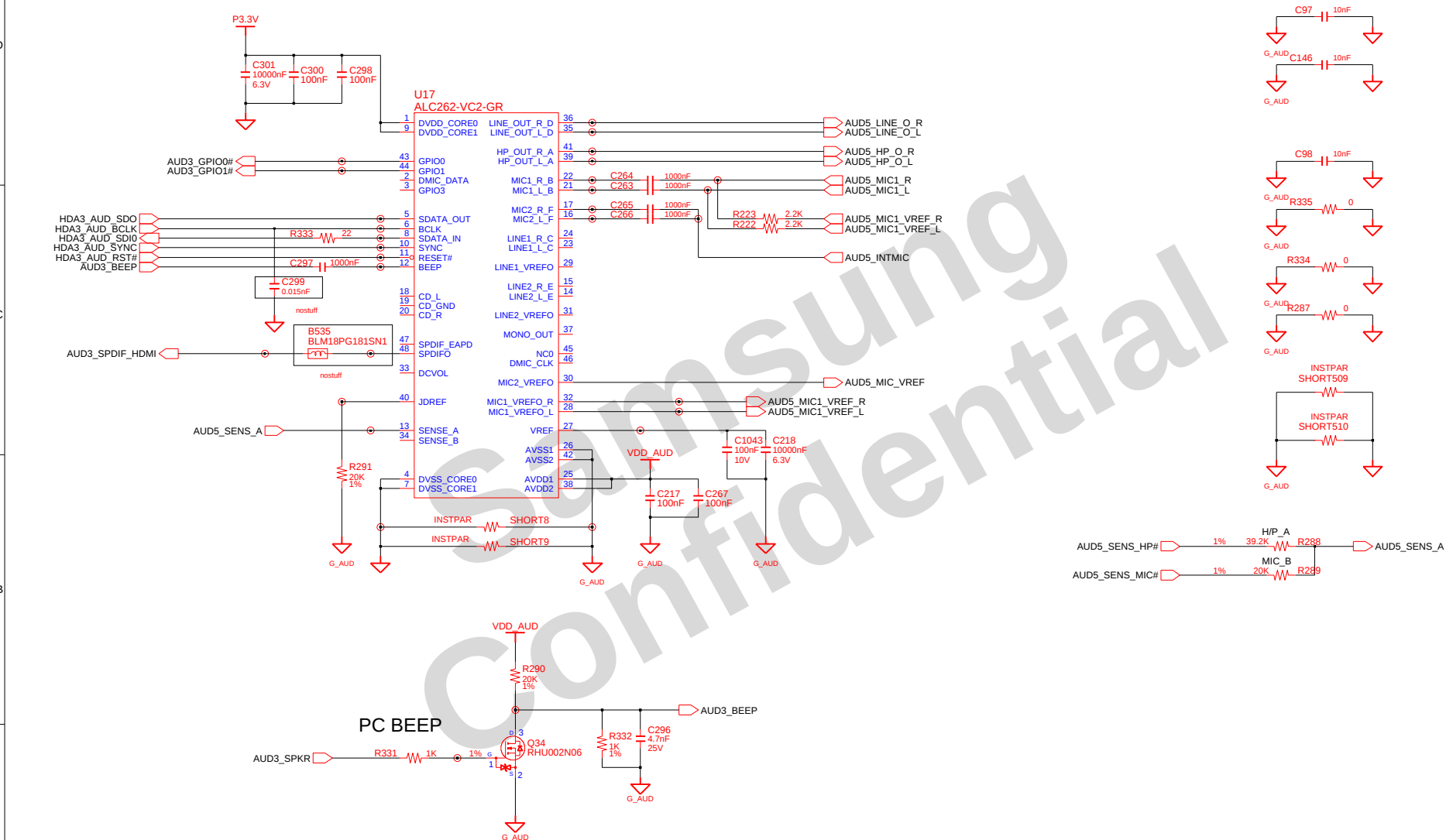


Odd Pins : Top side
Even Pins : Bottom Side



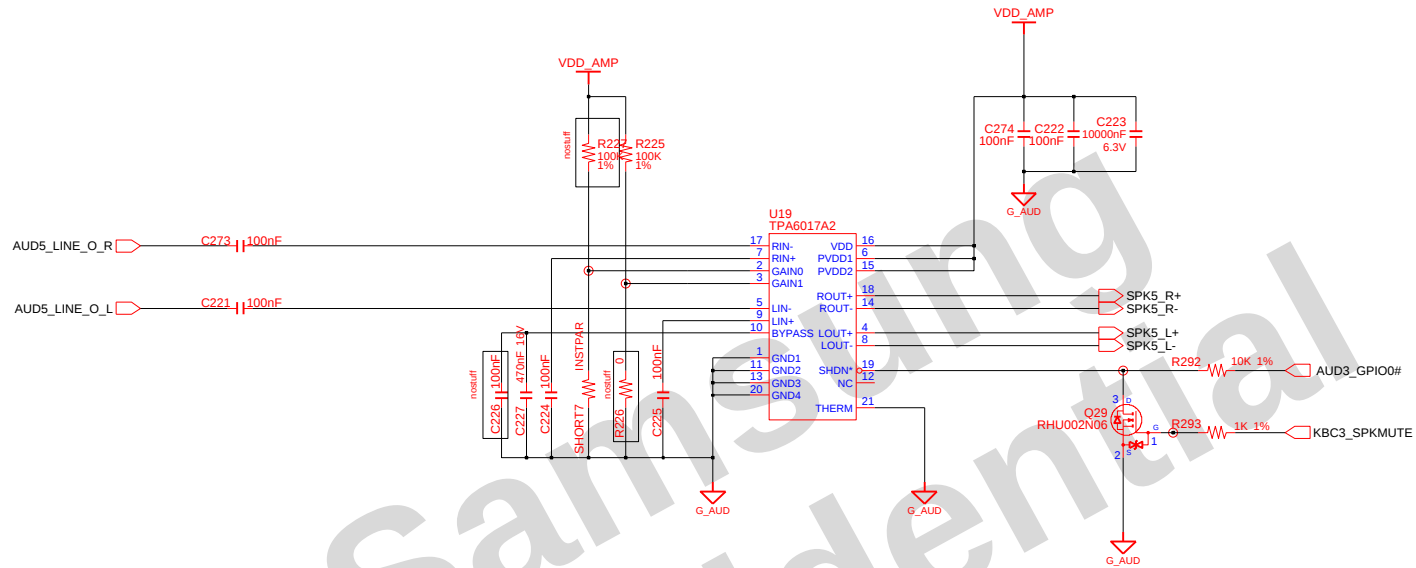
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APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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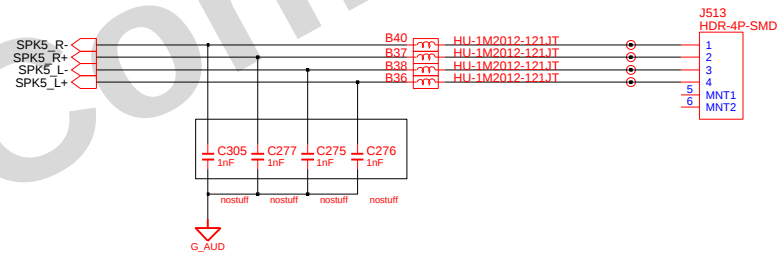


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MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 5	

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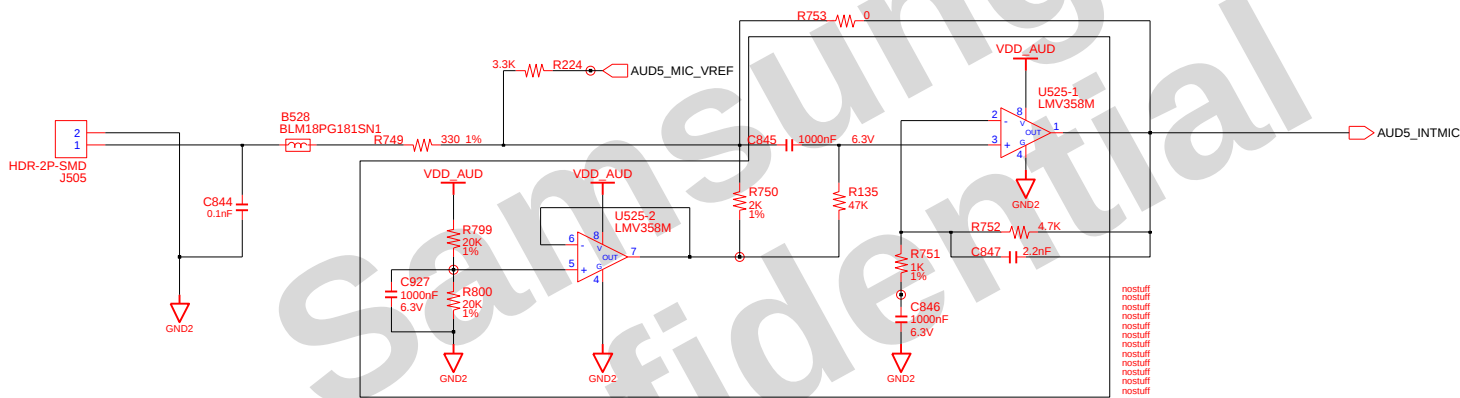
INTERNAL STEREO SPEAKERS



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MODULE CODE		LAST EDIT				
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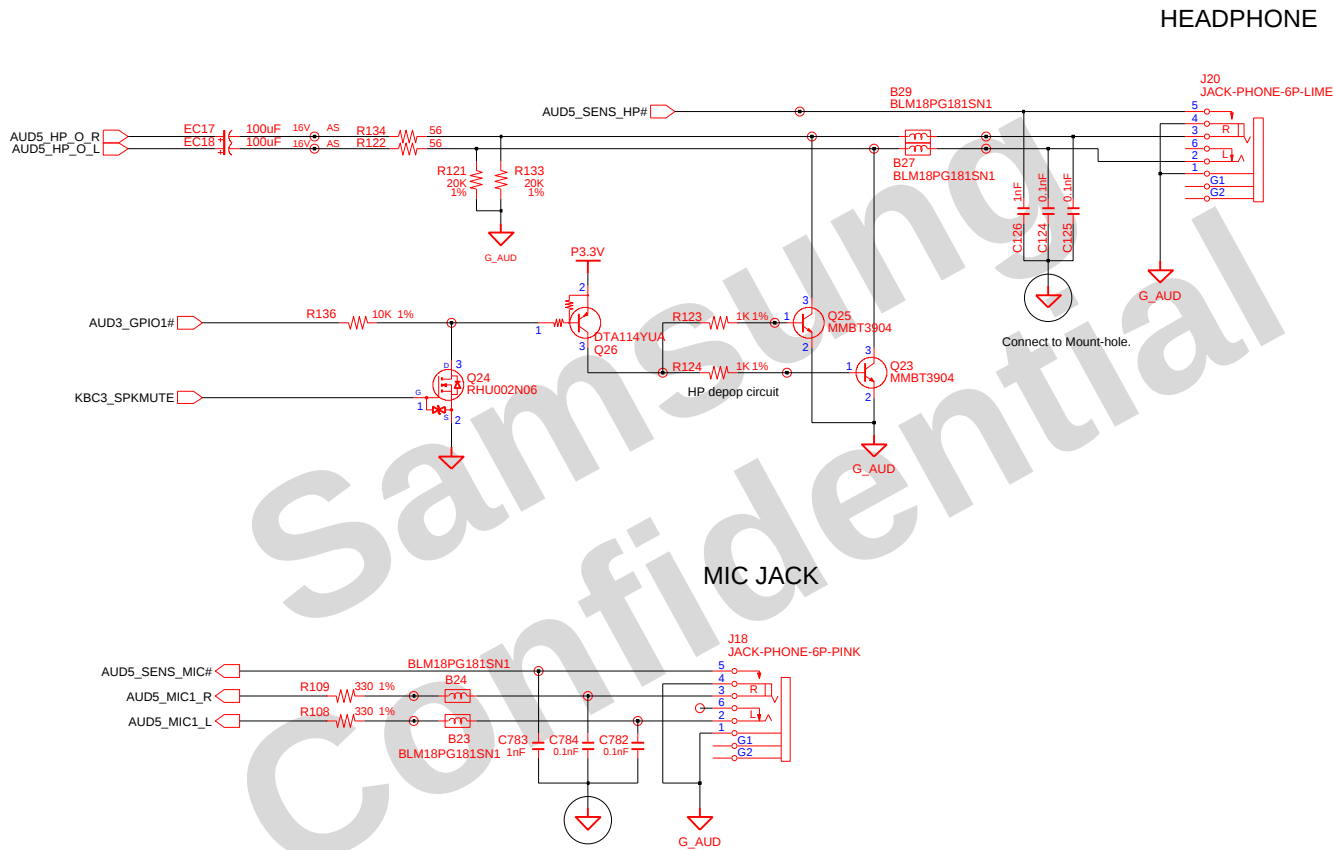
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Internal MIC



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		HDA_Codec_Alc262	
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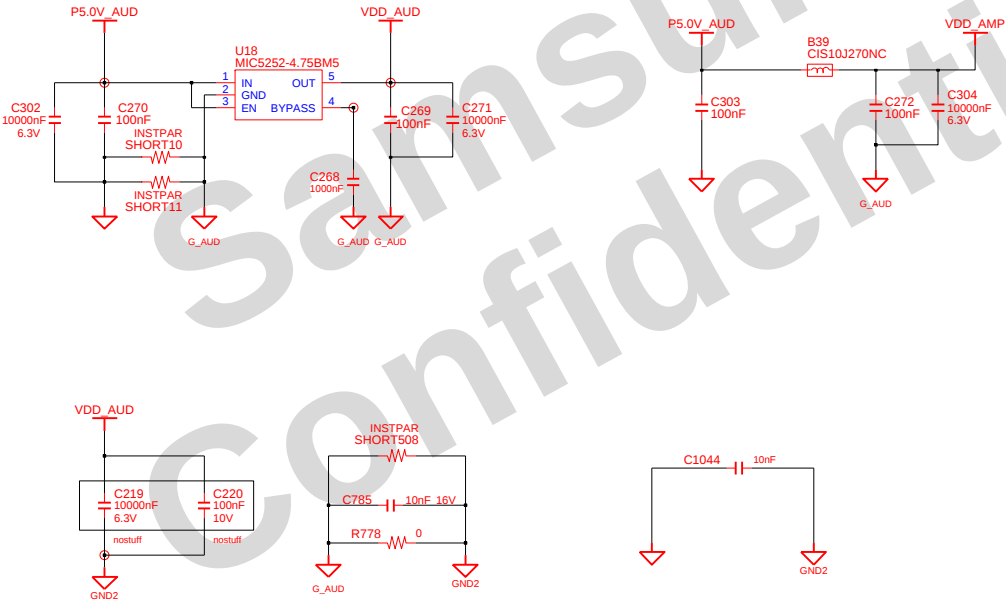
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The traces led to Audio Jacks have the width over 10mil

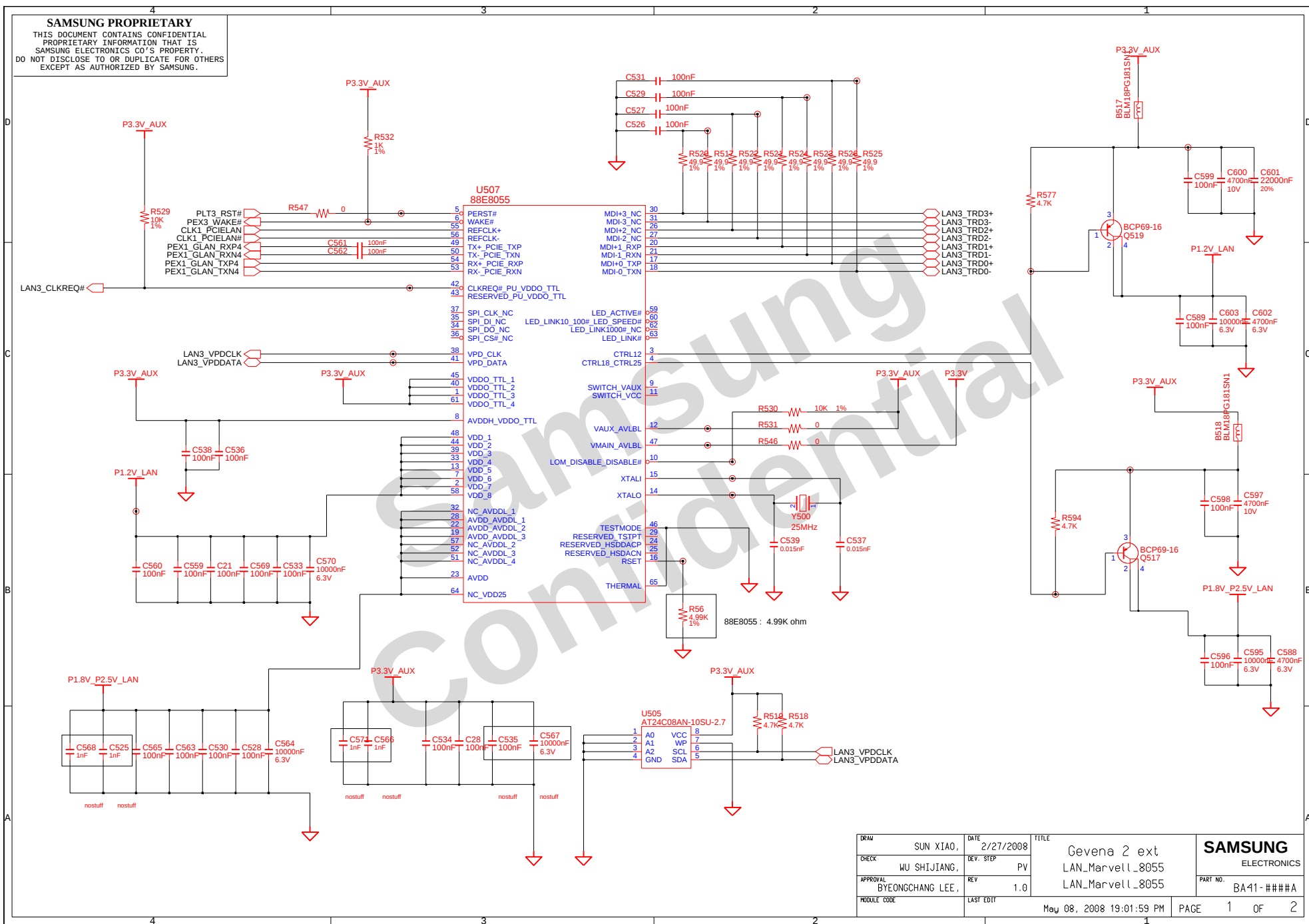
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APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Codec_Alc262 #4	
MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 4 OF 5

AUDIO POWER



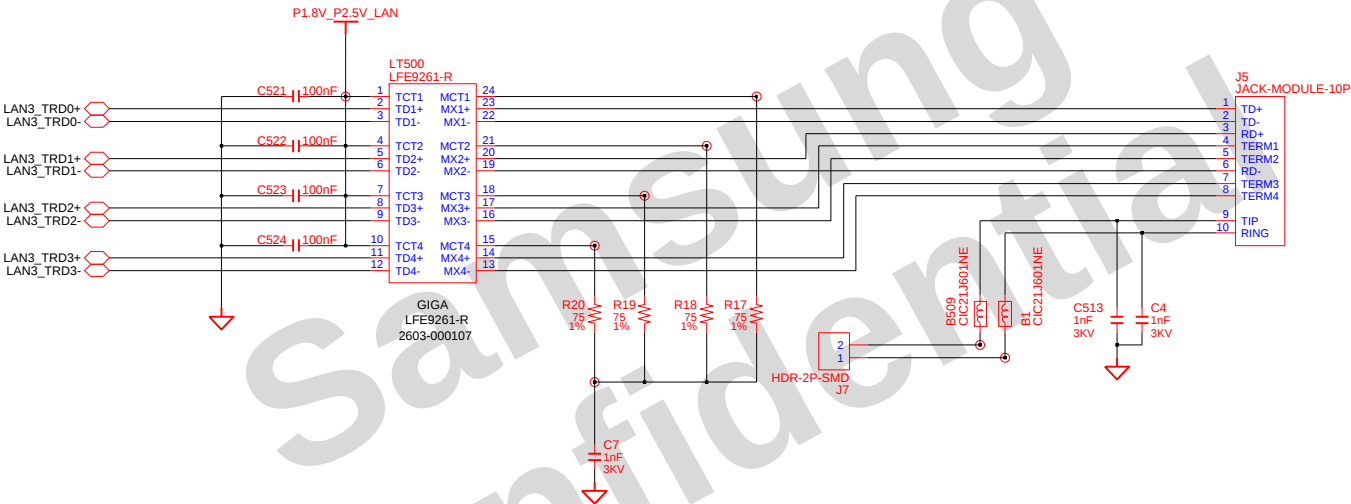
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MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	5 OF 5	

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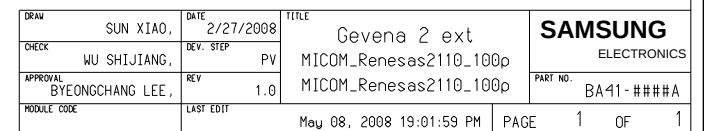
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The distance between LAN controller
and transformer is designed to extend less than two inches.



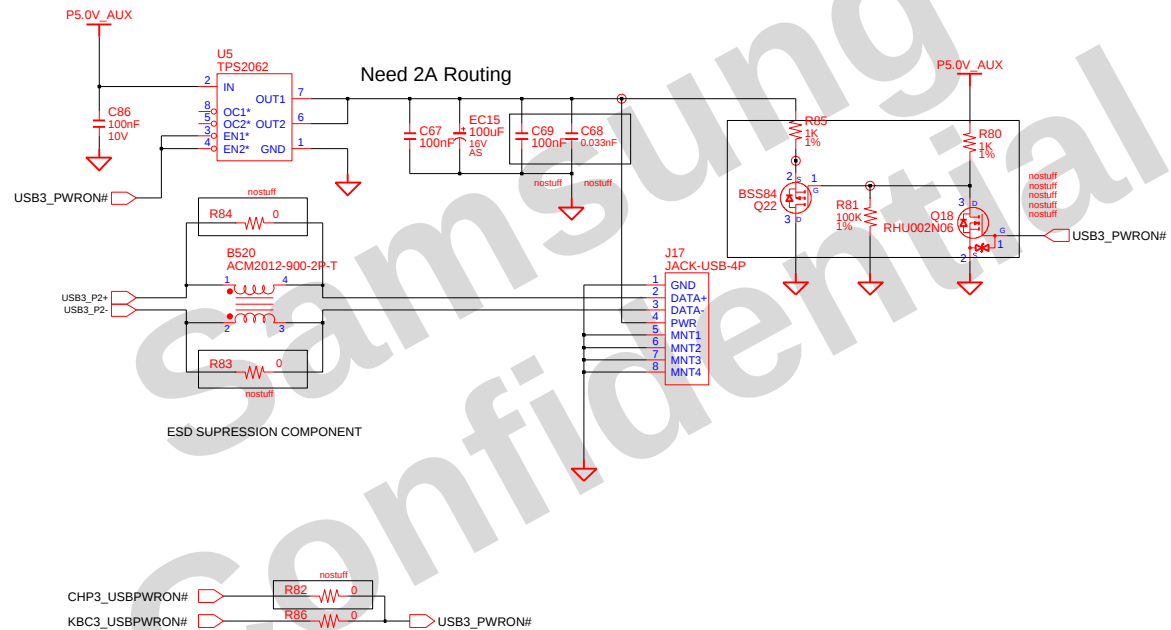
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CHECK	WU SHIJIANG,	DEV. STEP	PV		LAN_Marvell_8055	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		LAN_Marvell_8055	
MODULE CODE		LAST EDIT				
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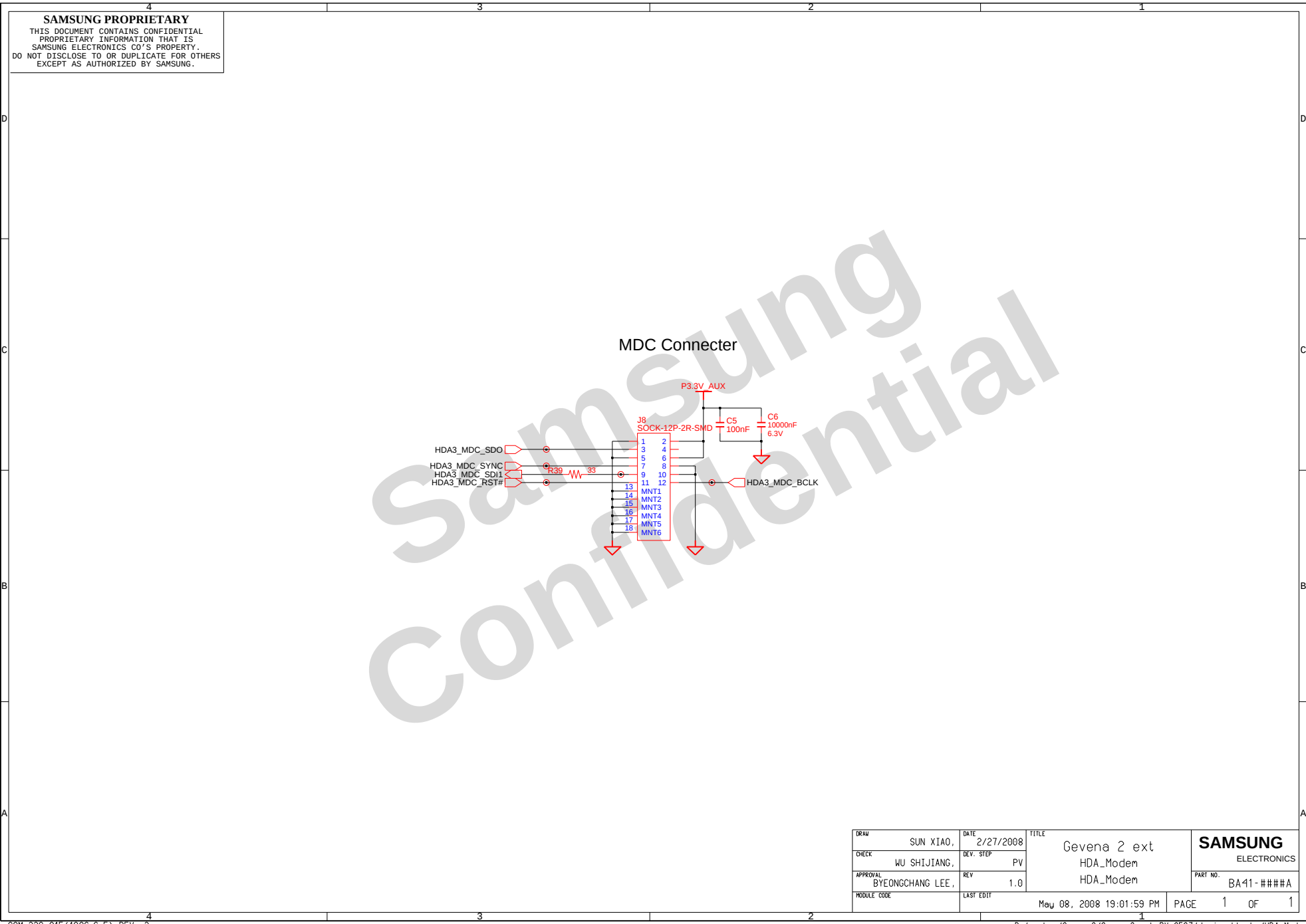
1 PORT USB CONNECTOR



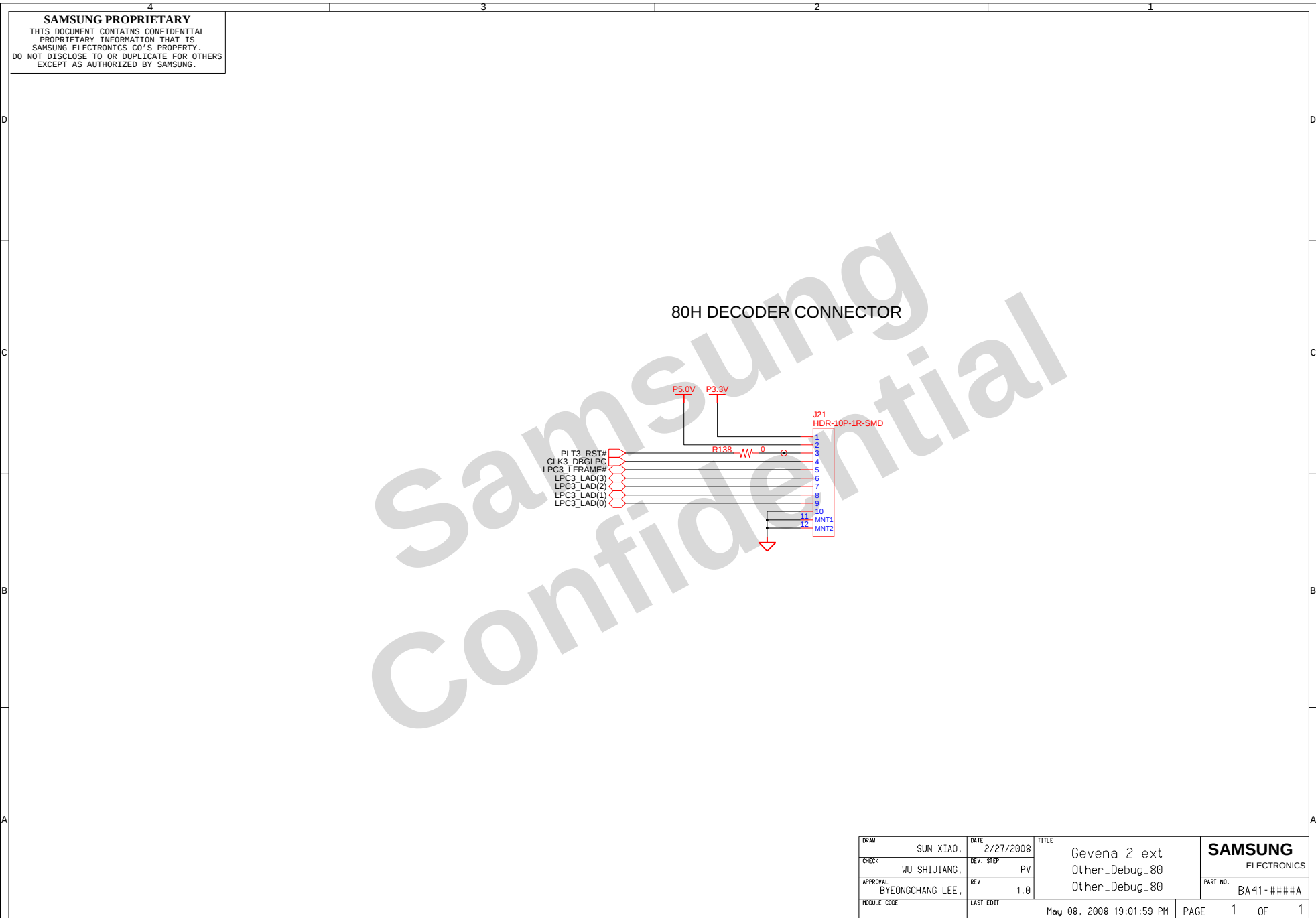
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APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

The schematic diagram illustrates the USB3-PWRON# circuit. It features a P5.0V_AUX supply connected to a U504 TPS2062 level shifter. The level shifter's output (OUT1) is connected to a MOSFET (BSS84 Q3) through a 100nF capacitor (C10). The MOSFET's gate is connected to the USB3_P0+ and USB3_P6+ inputs through a 100nF capacitor (C18). The MOSFET's drain is connected to the USB3_PWRON# output. The circuit also includes a USB3_P0+ and USB3_P6+ input section with resistors R24, R22, R28, and R25, and inductors B3 and B4. A J6 8P-LED-MNT connector is shown with pins 1 through 12. The circuit is labeled "Need 2A Routing".

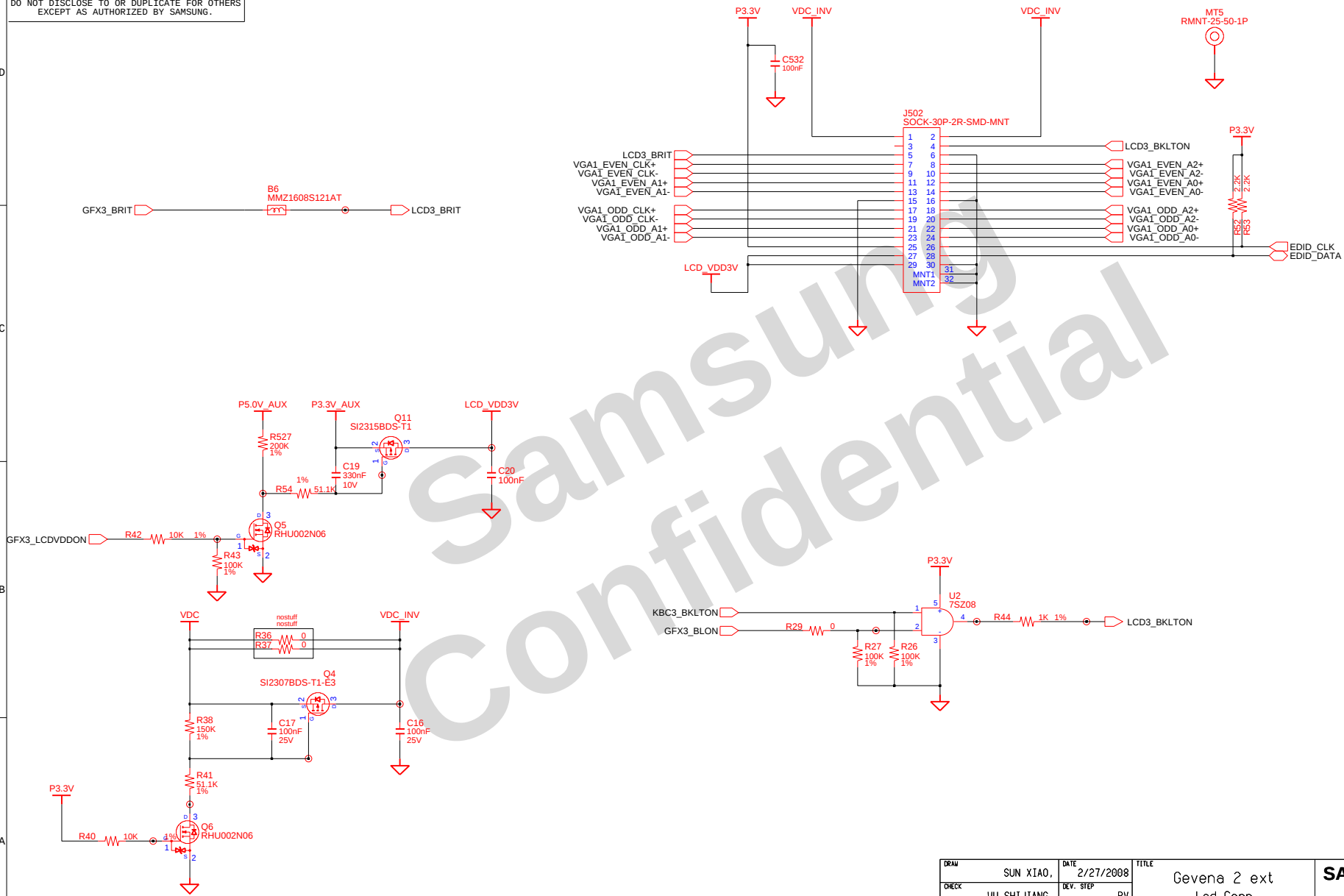
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SRP Sheet Number: 61 of 78



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APPROVAL	BYEONGCHANG LEE,	REV	1.0		HDA_Modem	
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	



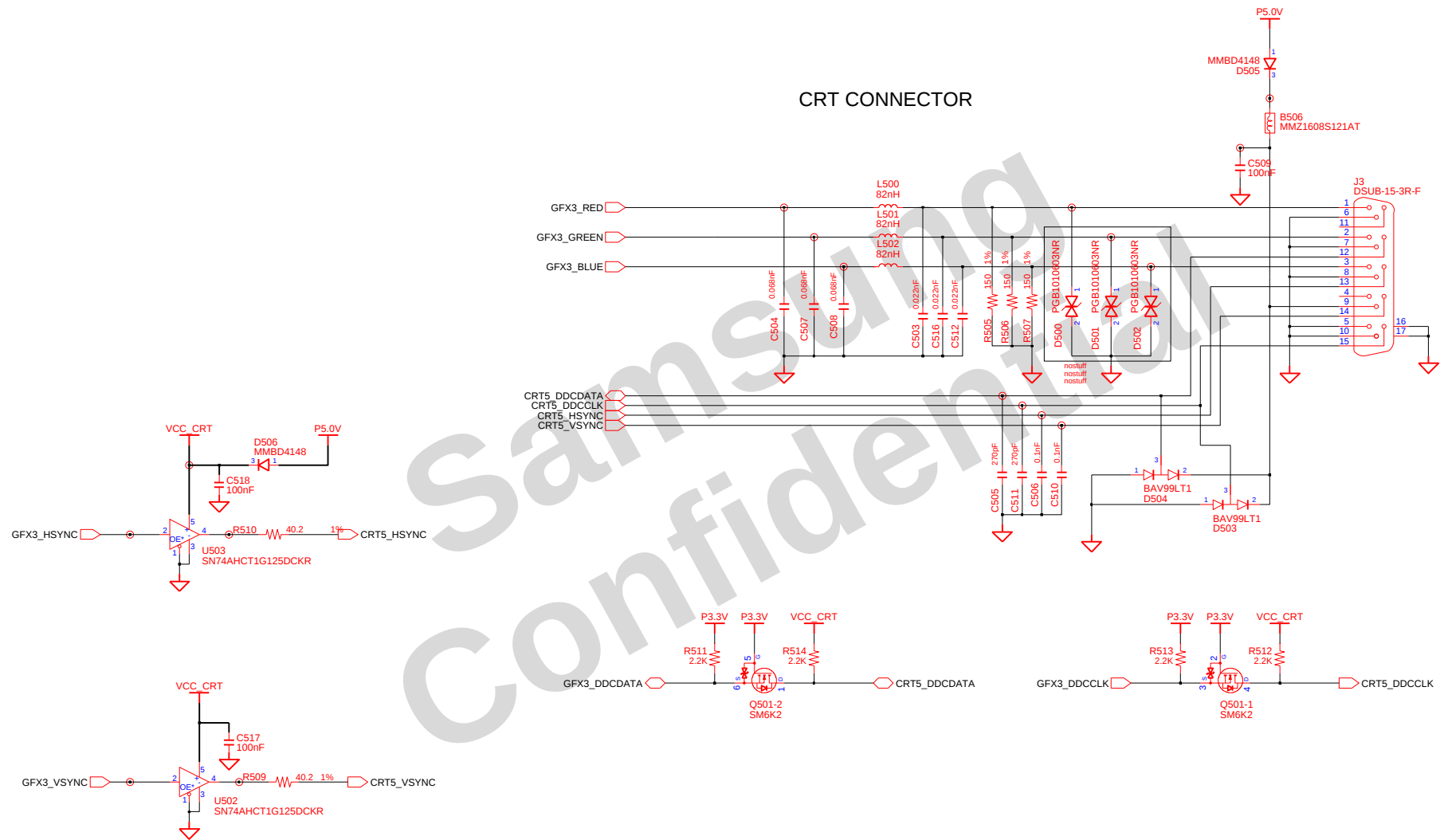
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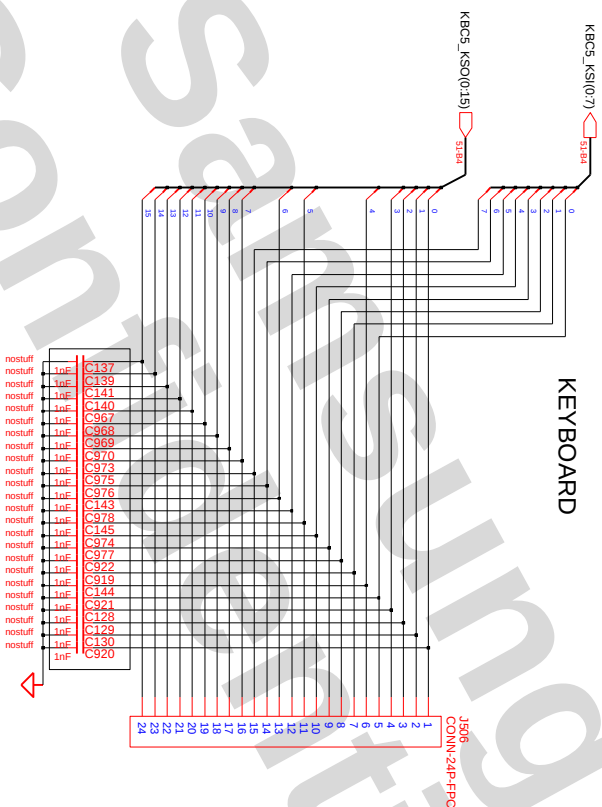
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APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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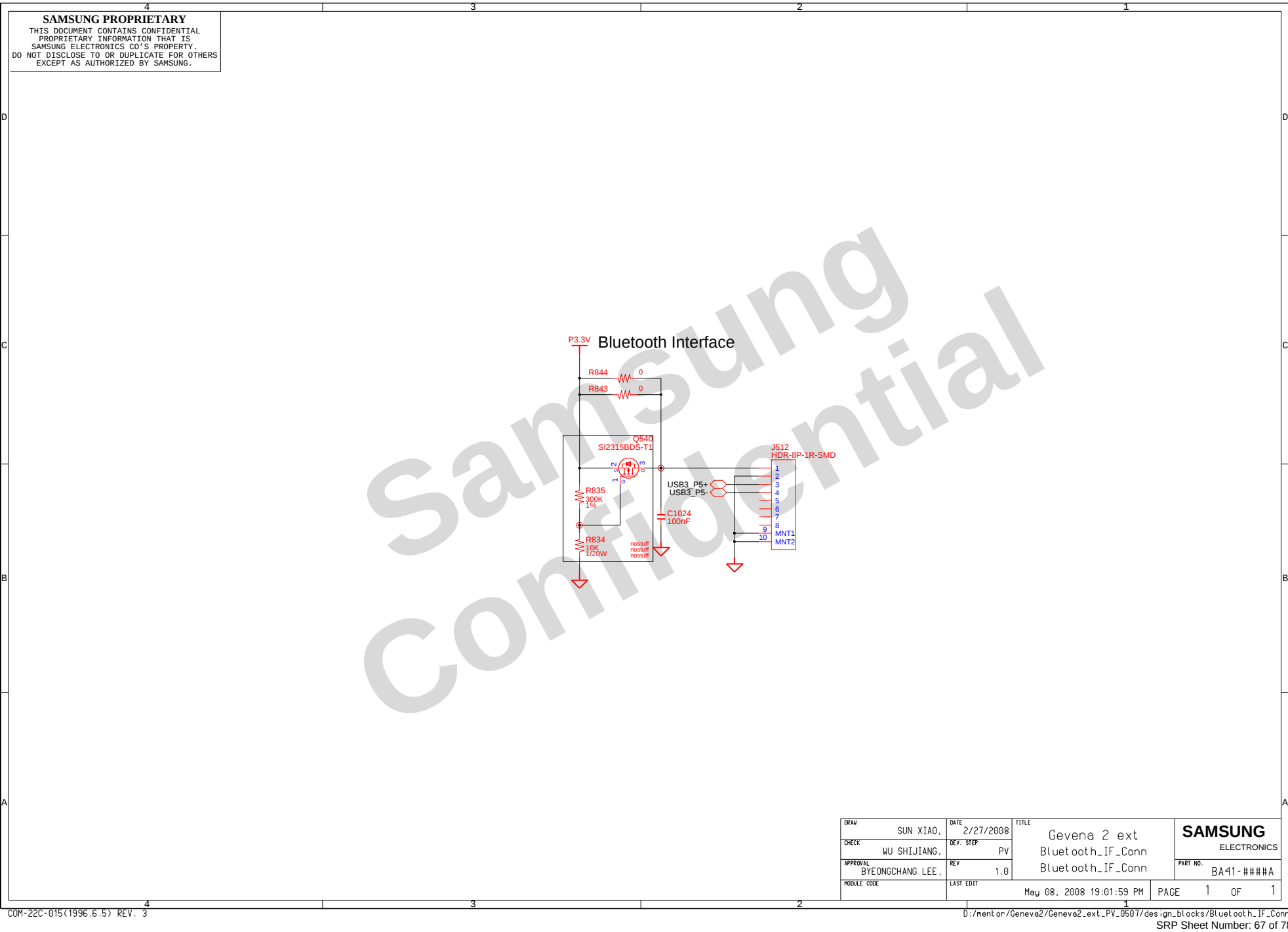
CRT CONNECTOR



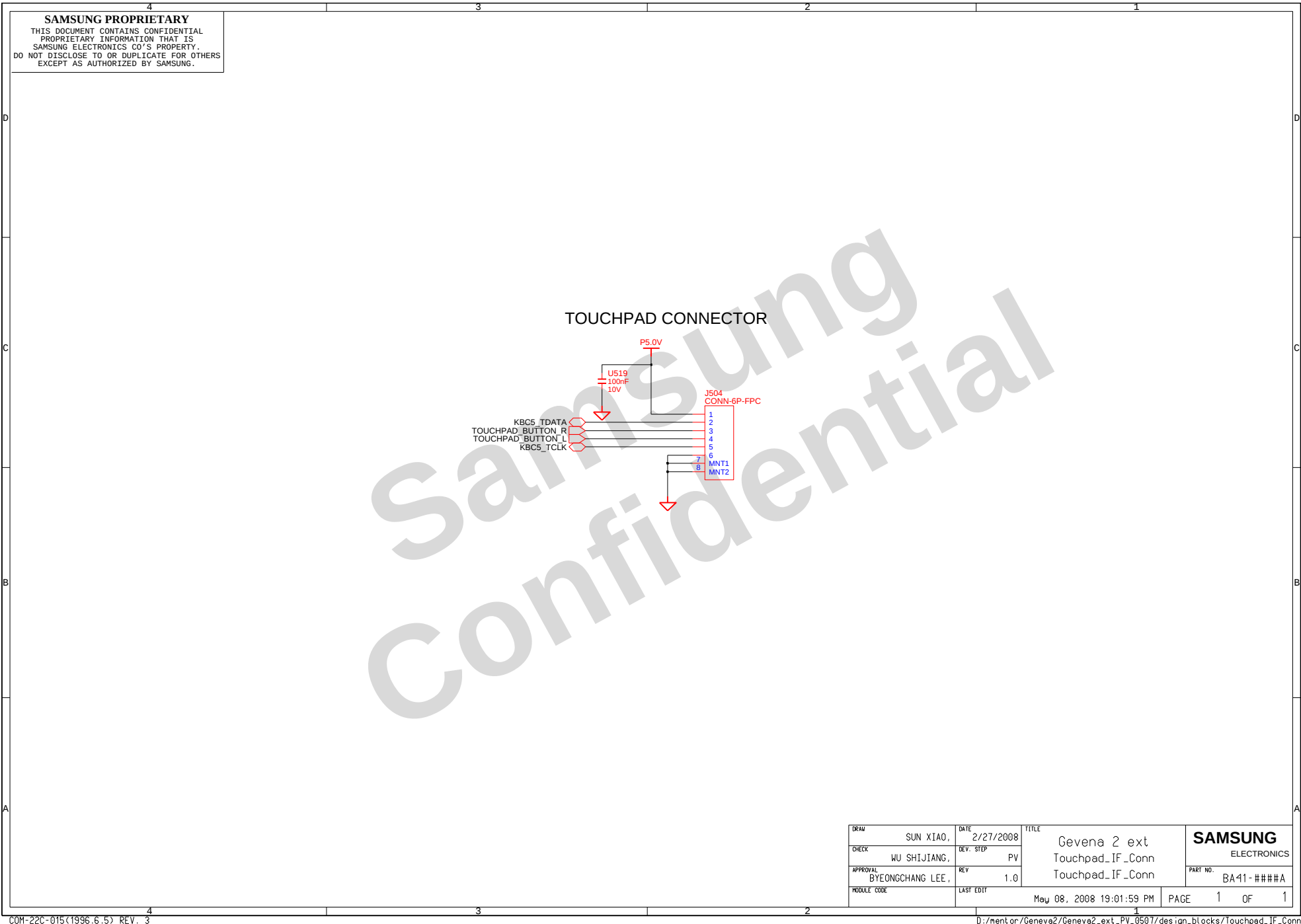
DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
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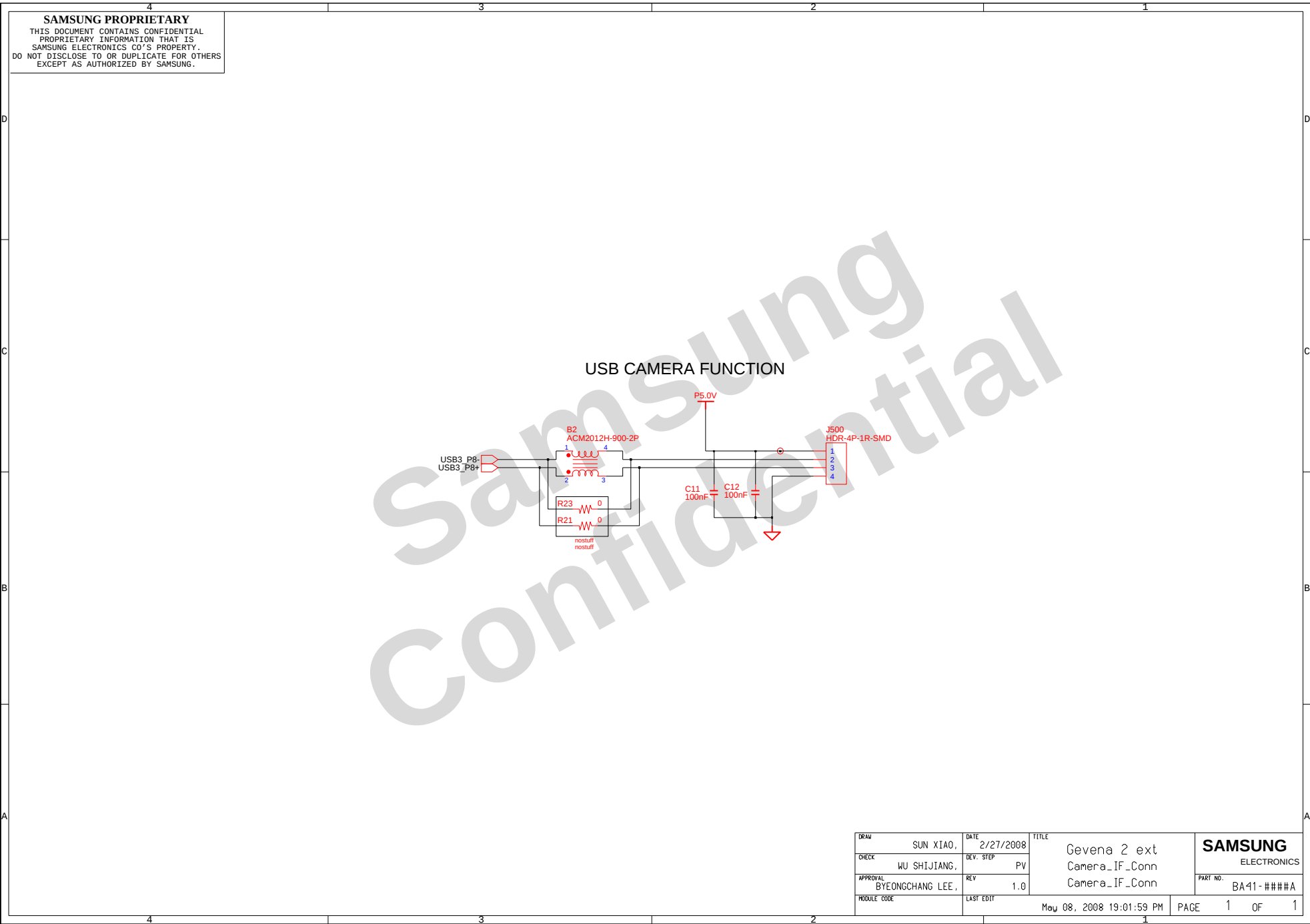


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0091	2/27/2008	KBD_IF_Conn	
0092	2/27/2008	KBD_IF_Conn	
0093	2/27/2008	KBD_IF_Conn	
0094	2/27/2008	KBD_IF_Conn	
0095	2/27/2008	KBD_IF_Conn	
0096	2/27/2008	KBD_IF_Conn	
0097	2/27/2008	KBD_IF_Conn	
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0100	2/27/2008	KBD_IF_Conn	



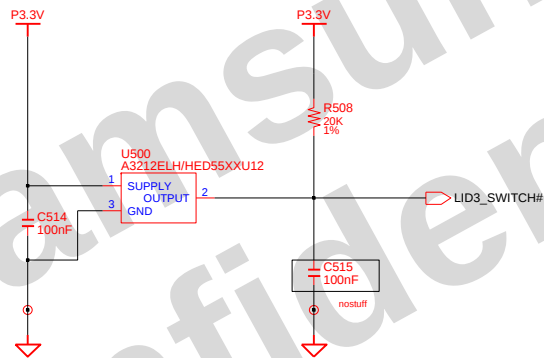
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CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	





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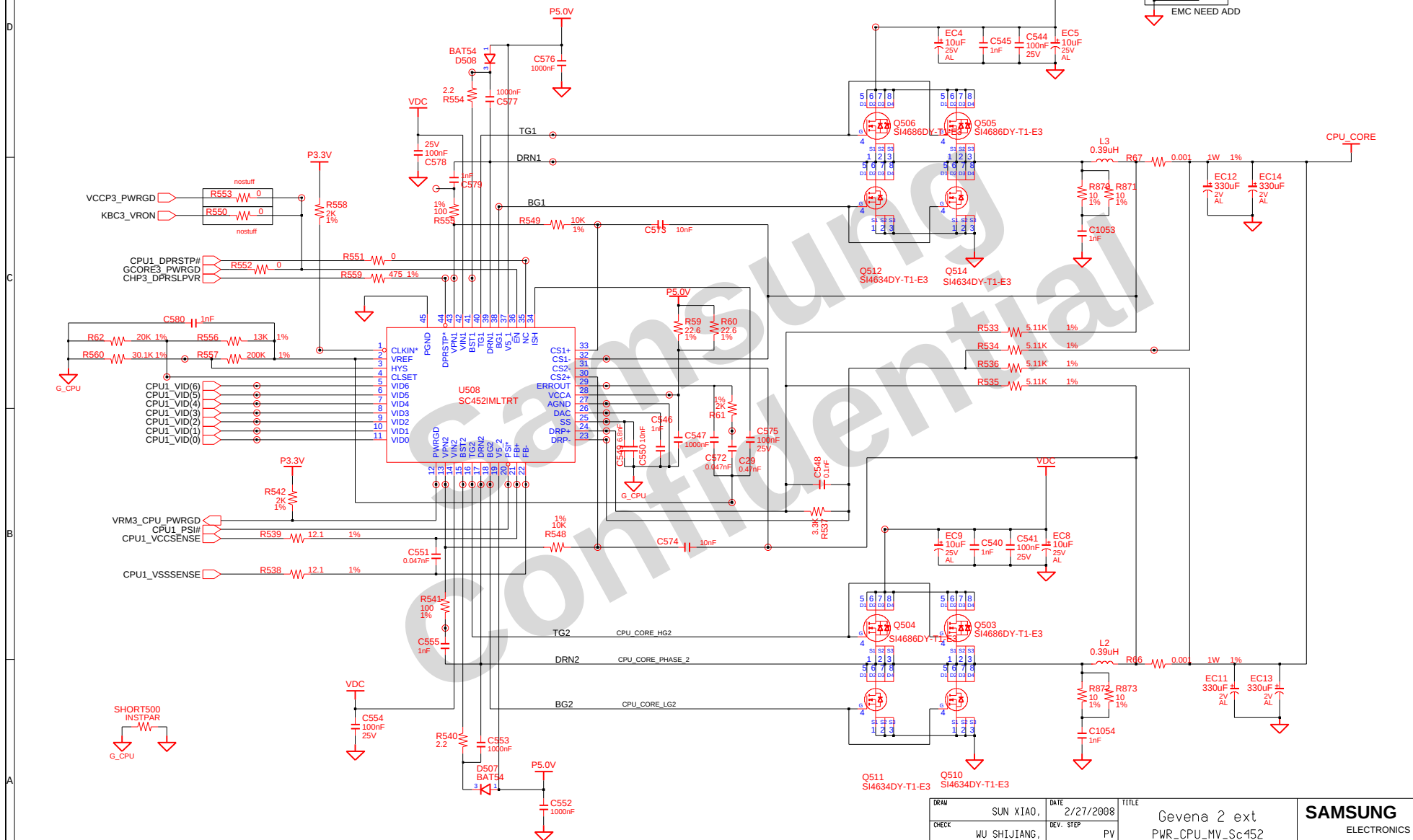
LID_SWITCH



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		LID_Switch	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		LID_Switch	
MODULE CODE		LAST EDIT				
				May 08, 2008 19:01:59 PM	PAGE	1 OF 1

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CPU VRM [SEMTECH]

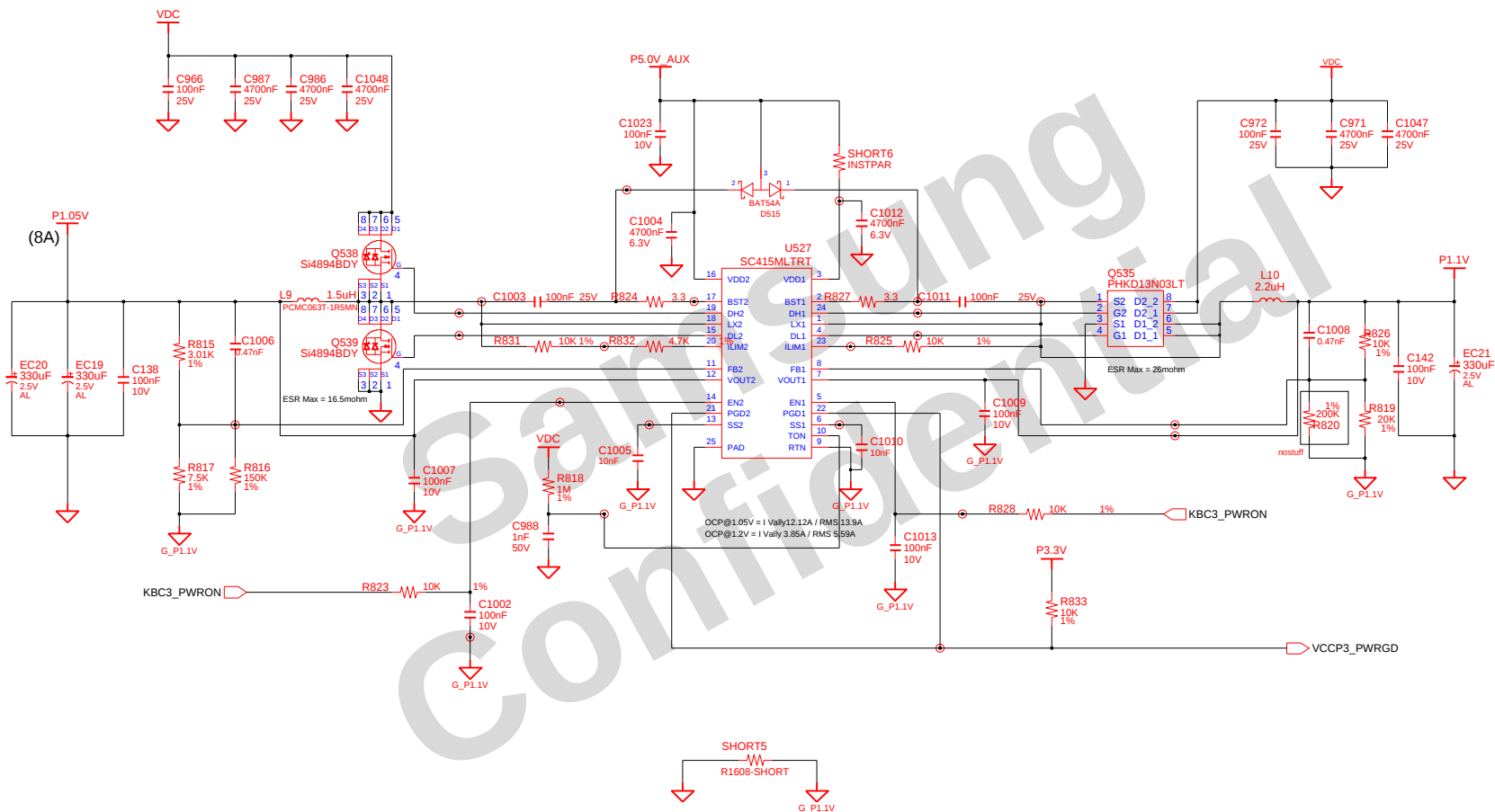


DRAM	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		PWR_CPU_MV_Sc452	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		CPU1 VRM (IMVP6+)	
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	



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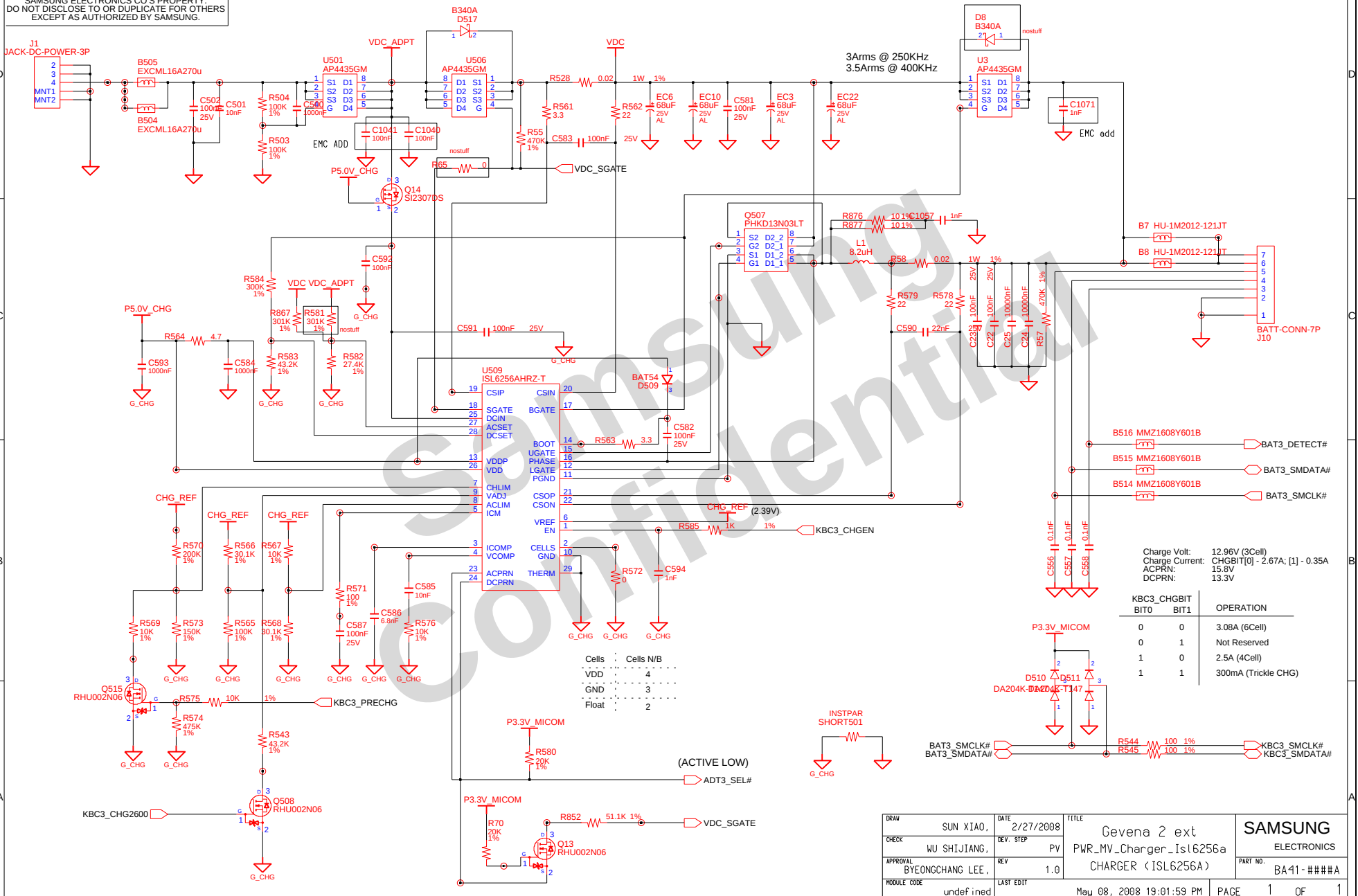
CHIPSET POWER(P1.05V & P1.1V)



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	SAMSUNG ELECTRONICS		
CHECK	WU SHIJIANG,	DEV. STEP	PV	Gevena 2 ext PWR_MV_Cantiga			
APPROVAL	BYEONGCHANG LEE,	REV	1	Chipset Power (P1.05V_M,P1.1V)			
MODULE CODE	undefined	LAST EDIT	May 08, 2008 19:01:59 PM	PART NO. BA41-####A			
				PAGE	1	OF	1

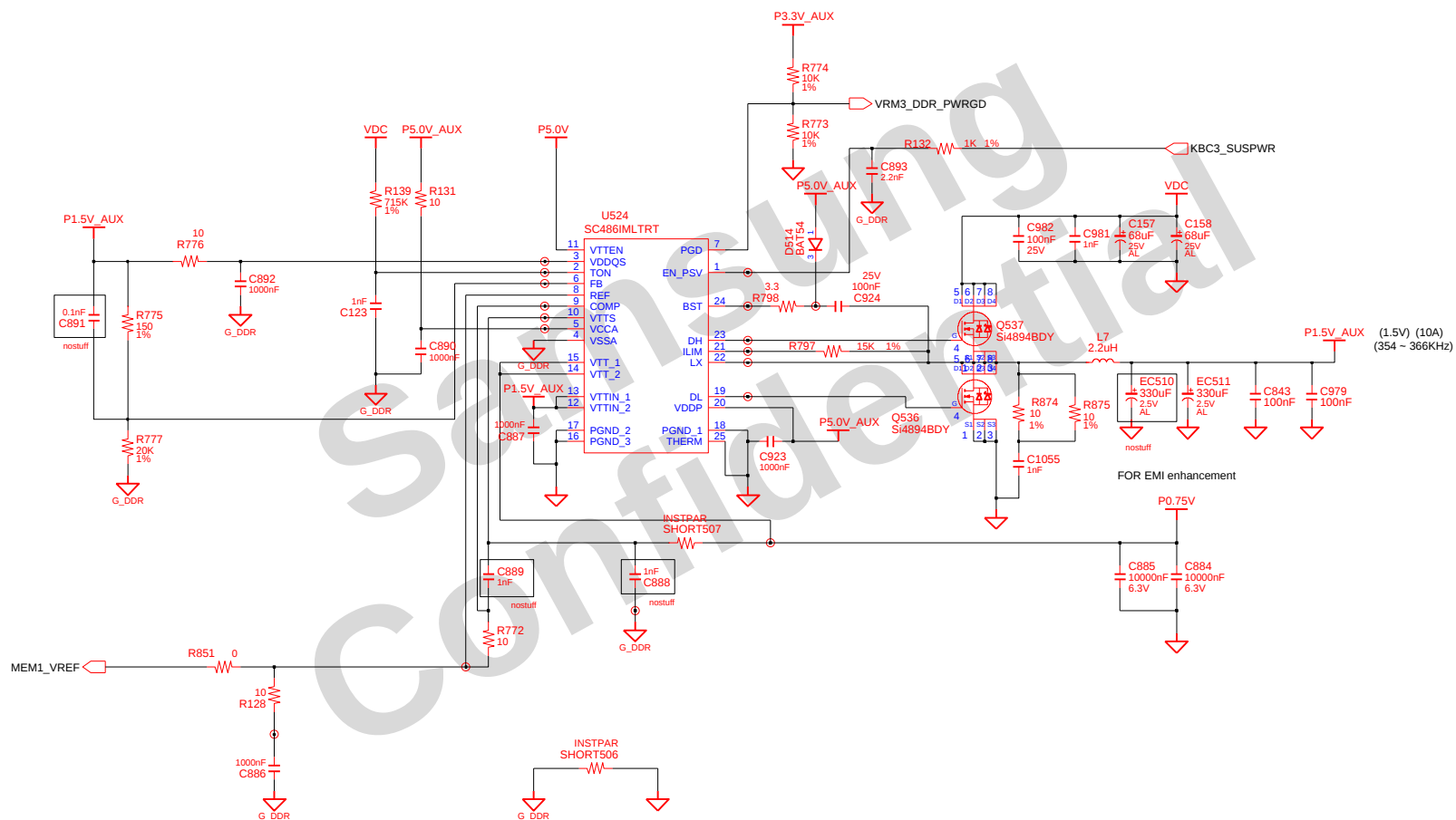
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CHARGER & POWER MANAGEMENT



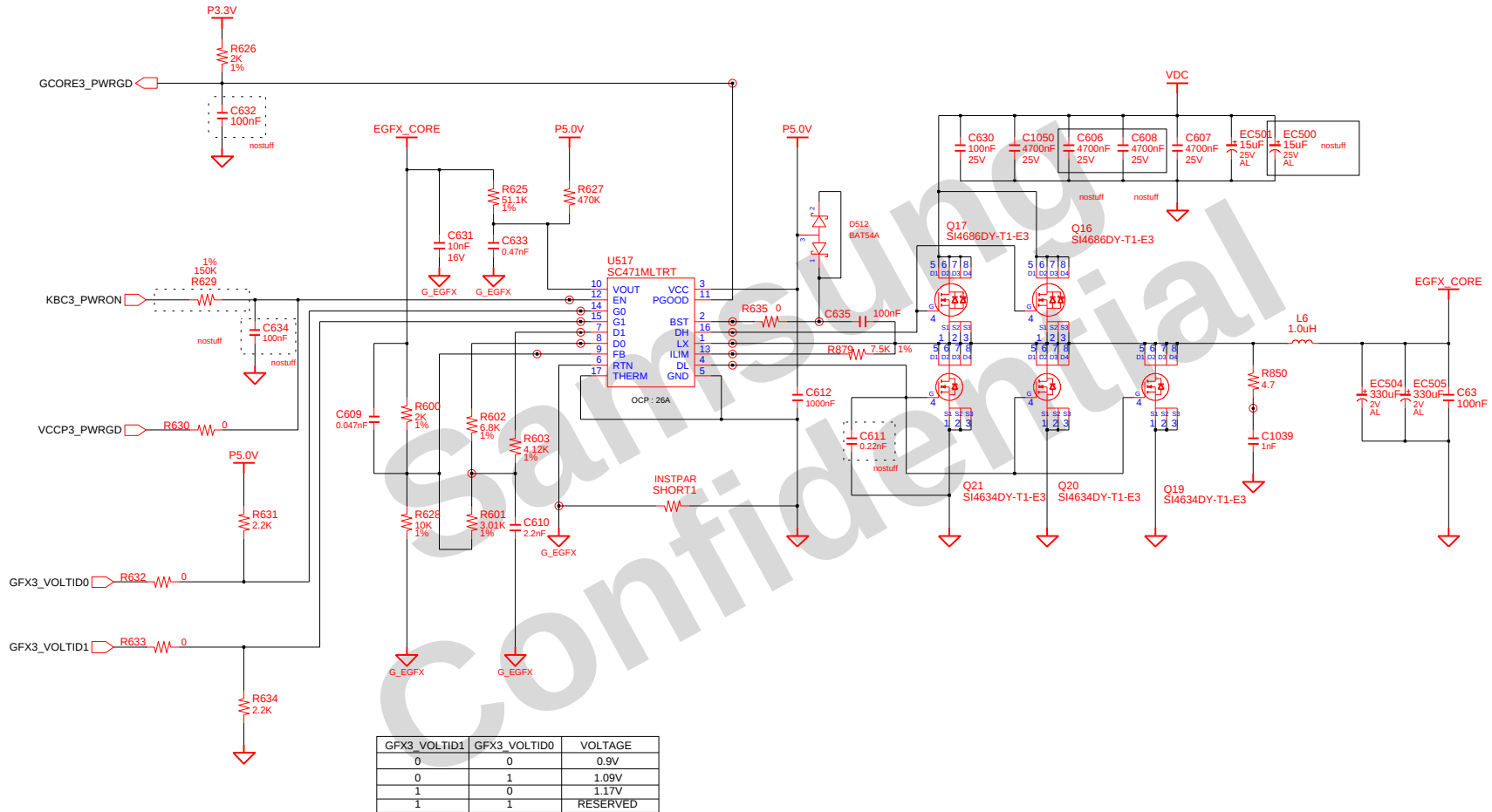
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DDR3 Power



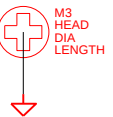
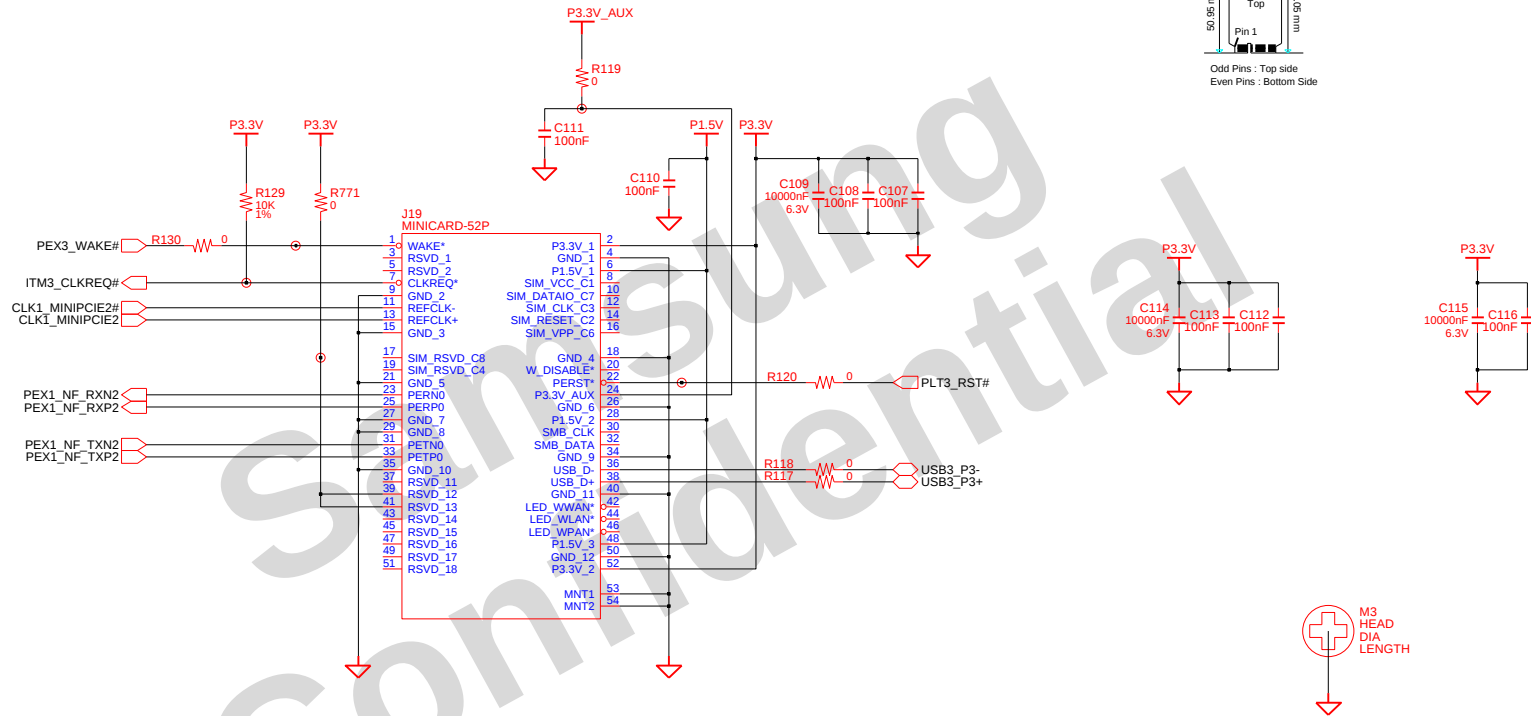
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Graphic Core Power



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	WU SHIJIANG,	DEV. STEP	PV		PWR_Gfx_MV_Ext	
APPROVAL	BYEONGCHANG LEE,	REV	1.0		Ext Gfx Core(SC471)	
MODULE CODE		LAST EDIT				
May 08, 2008 19:01:59 PM						PAGE 2 OF 2

MINI CARD FOR ROBSON



DRAW	SUN XIAO,	DATE	2/27/2008	TITLE	Gevena 2 ext Robson_PCIE Robson_PCIE	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PV			PART NO. BA41-####A
APPROVAL	BYEONGCHANG LEE,	REV	1.0			
MODULE CODE		LAST EDIT	May 08, 2008 19:01:59 PM	PAGE	1 OF 1	

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