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http://laptop-motherboard-schematic.blogspot.com/

Jinmao

CPU : Arrandale PGA
Chip Set : Intel Ibex Peak
GFX : N12M / INT.GFX
Remarks : Calpella Platform

Model Name : Jinmao
PBA Name : MAIN
PCB Code : BA41-01432A (GCE)
BA41-01433A (NY)
BA41-01434A (HAN)
BA41-01435A (GBM)
Dev. Step : PR
Revision : 1.0
T.R. Date : 2010.11.26

Design	CHECK	APPROVAL
MS YANG	*MK KIM*	*BL LEE*

■ ***Owner : SEC IT Solution N/P LAB*** ***Signature : mansu***

sheet01 : Cover
sheet02 : BLOCK DIAGRAM
sheet03 : BOARD INFORMATION
sheet04 : POWER DIAGRAM
sheet05 : POWER RAILS
sheet06 : POWER SEQUENCE
sheet07 : CLOCK DISTRIBUTION
sheet08 : CK505-SHRINK
sheet09 : Thermal Sensor
sheet10 : CPU
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sheet13 : CPU
sheet14 : DDR3 SODIMM #0
sheet15 : DDR3 SODIMM #1
sheet16 : PCH-IbexPeak
sheet17 : PCH-IbexPeak
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sheet21 : 80 port
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sheet23 : N12M-GE2
sheet24 : N12M-GE2
sheet25 : N12M-GE2
sheet26 : GFX memory
sheet27 : GFX memory
sheet28 : LVDS / CAMERA
sheet29 : CRT
sheet30 : HDMI
sheet31 : Audio - ALC269
sheet32 : Audio - HP/MIC WOOFER(2.1CH)
sheet33 : LAN (Realtek 8111E)
sheet34 : WLAN
sheet35 : SATA HDD, IR
sheet36 : MICOM / BIOS
sheet37 : MICOM Glue Logic (KBD)
sheet38 : USB
sheet39 : Power - charger
sheet40 : Power - P3.3V_AUX / P5.0V_AUX
sheet41 : Power - P1.05V (Chipset Power)
sheet42 : Power - DDR3
sheet43 : Power - CPU VRM
sheet44 : Power - IGFX_CORE
sheet45 : Power - EGFX_CORE
sheet46 : Power - Switched Power 1
sheet47 : Power - Power Discharge
sheet48 : 3-in-1 card (AU6437)
sheet49 : ODD Sub B'd
sheet50 : Touchpad & LED
sheet51 : MOUNT HOLE
sheet52 : Power - Switched Power 2

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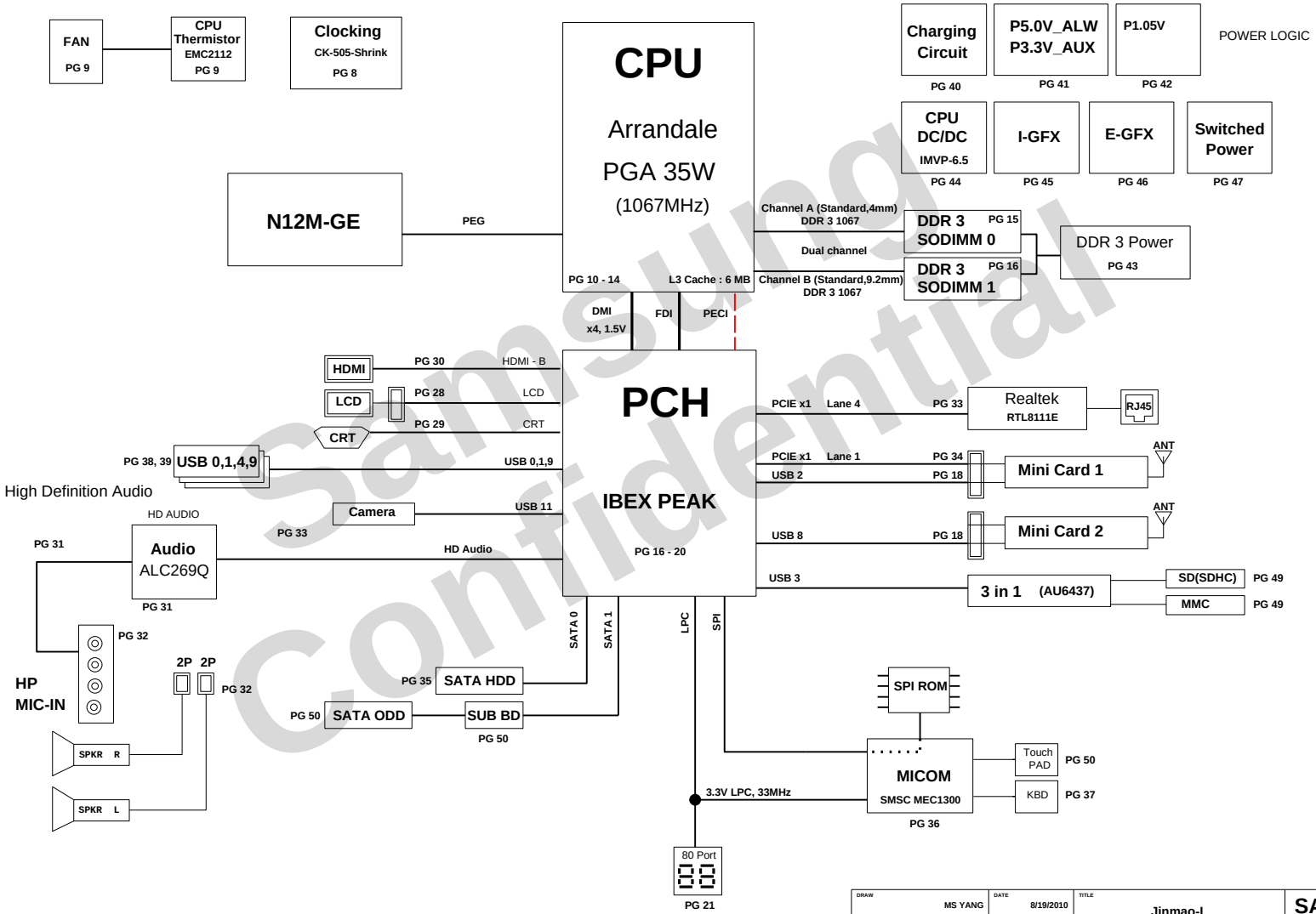
BLOCK DIAGRAM



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC	Primary DC system power supply (7 to 21V)	S4 - S5
P12.0V_ALW	12.0V always power rail	
P3.3V_MICOM	3.3V always power rail (for Micom)	
P5.0V_ALW	5.0V always power rail	
P5.0V_STB	5.0V always power rail	
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)	S3
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)	
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)	
P5.0V	5.0V switched power rail (off in S3-S5)	S0
P3.3V	3.3V switched power rail (off in S3-S5)	
P1.8V	1.8V switched power rail (off in S3-S5)	
P1.5V	1.5V switched power rail (off in S3-S5)	
P1.05V	1.05V power rail for chipset (off in S3-S5)	
P0.75V	0.9V power rail for DDR (off in S3-S5)	
VCC_CORE	Core Voltage for CPU	S0
IGFX_CORE	Core Voltage for IGFX	
EGFX_CORE	Core Voltage for GPU	
P1.05V (VCCP)	VCC for Arrandale & IBEX Peak	

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

LCD Pannel Detect

Devices	Resolution	PANNEL_DETECT_0
LTN140AT17	HD(1366x768)	SEC3250

I²C / SMB Address

Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	Mini PCI Express
3	Multi Memory Card Controller
4	NC
5	NC
6	NC (N/A WITH HM55)
7	NC (N/A WITH HM55)
8	NC
9	SYSTEM PORT 2 (SUB BOARD)
10	Bluetooth
11	Camera
12	NC
13	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	NC
3	NC
4	LAN CONTROLLER
5	NC
6	NC
7	NC (N/A WITH HM55)
8	NC (N/A WITH HM55)

SATA PORT Assign

PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	
5	

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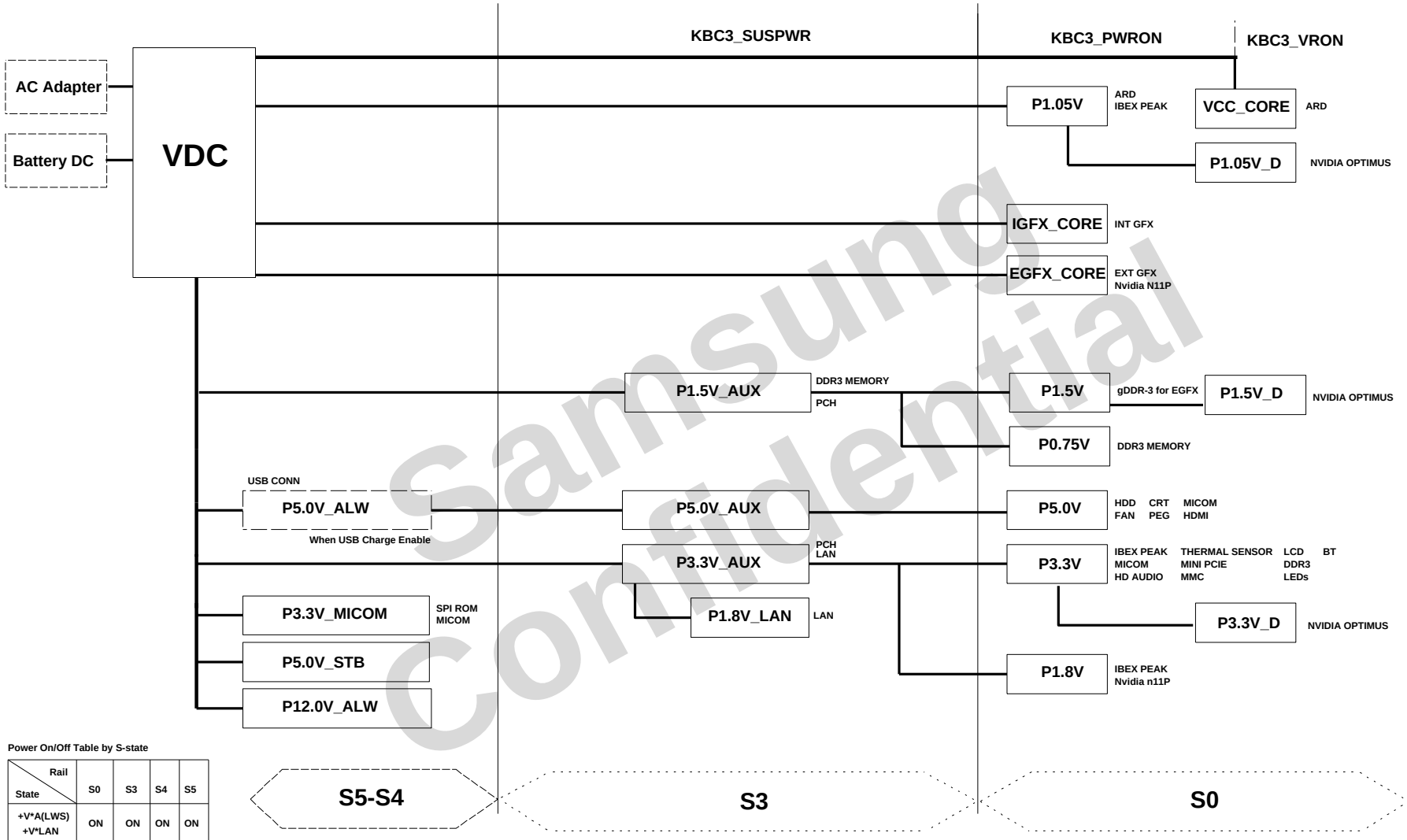
POWER DIAGRAM



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Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

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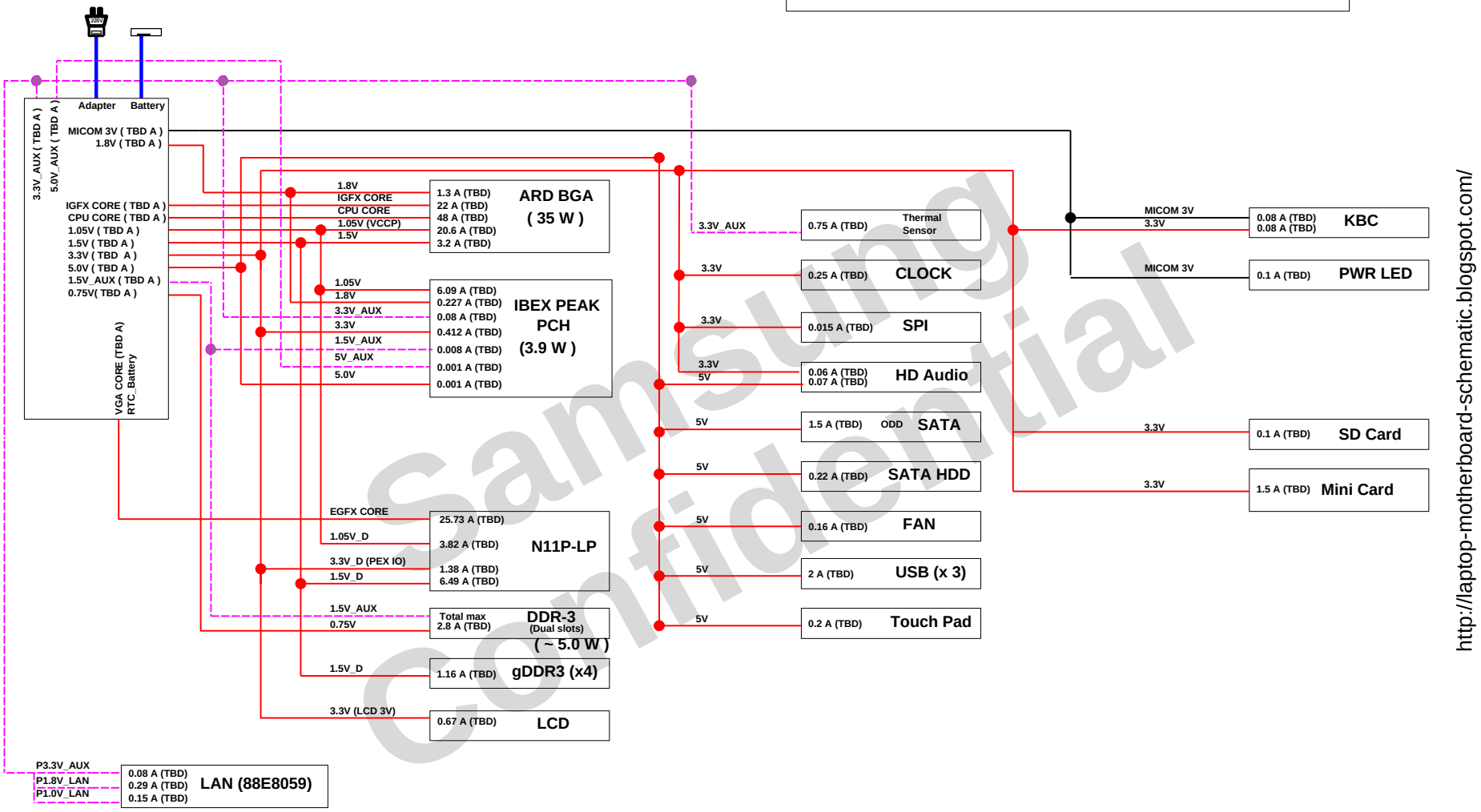
POWER RAILS ANALYSIS



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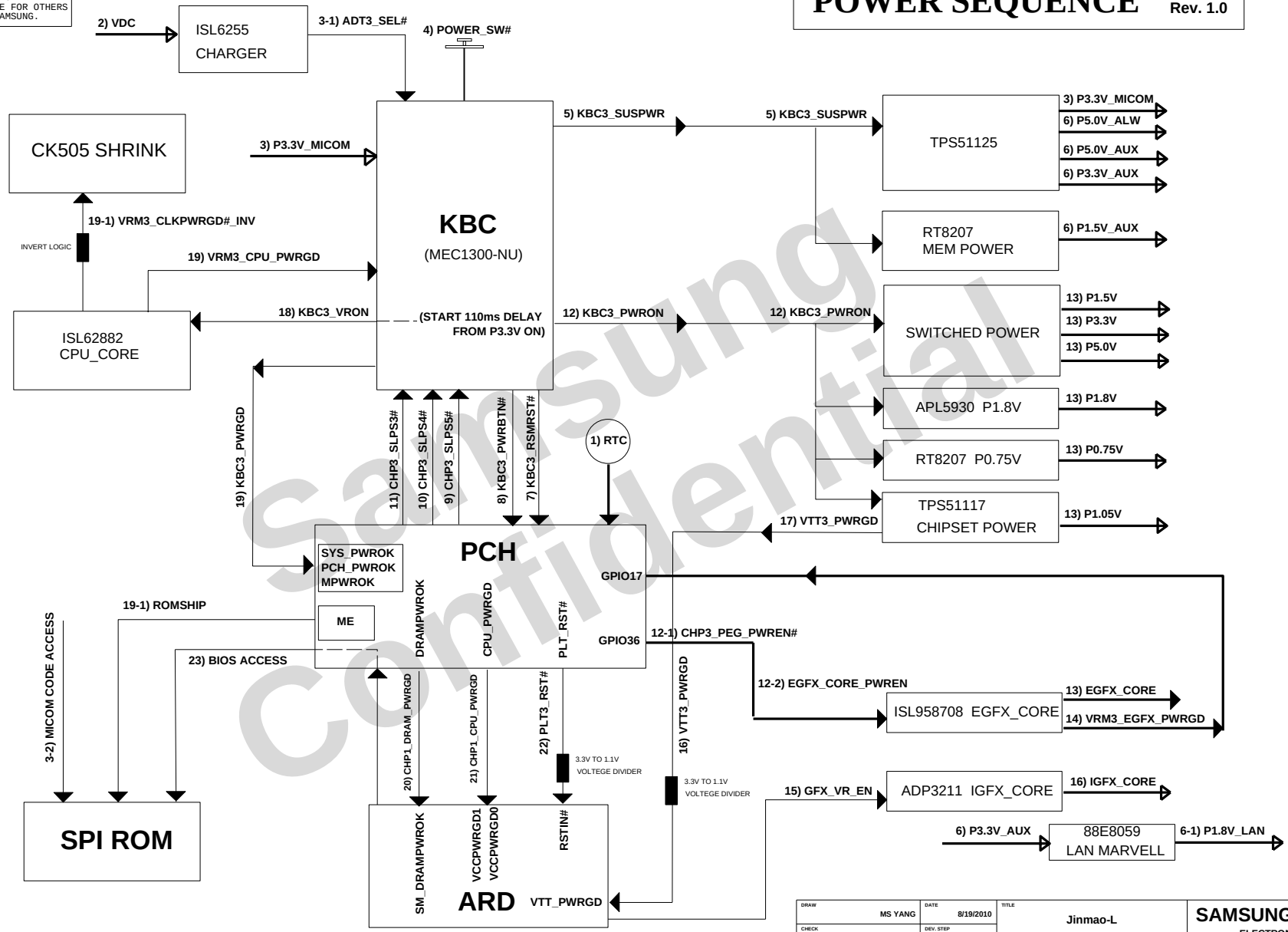
POWER SEQUENCE Rev. 1.0



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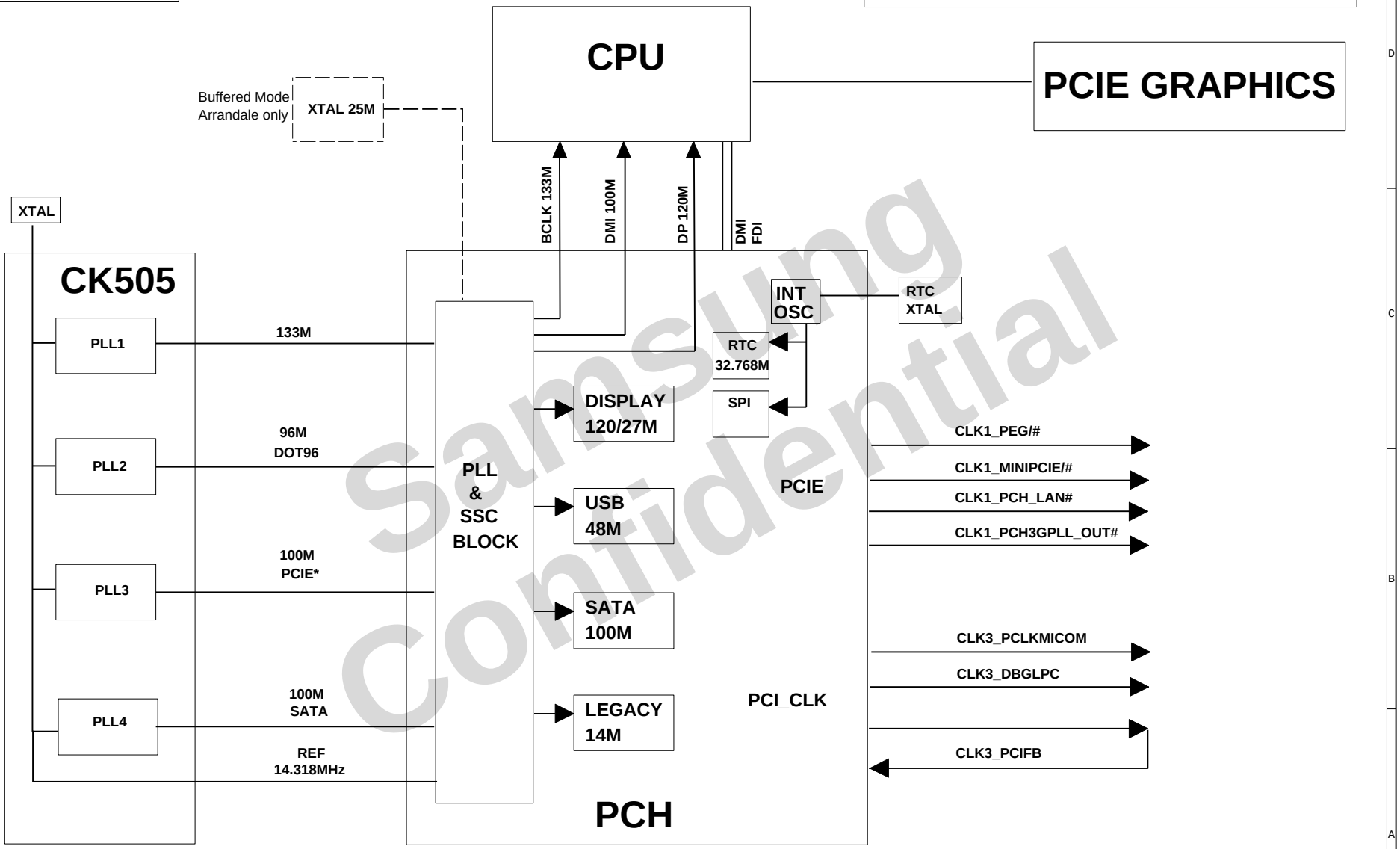
CLOCK DISTRIBUTION Rev. 1.0



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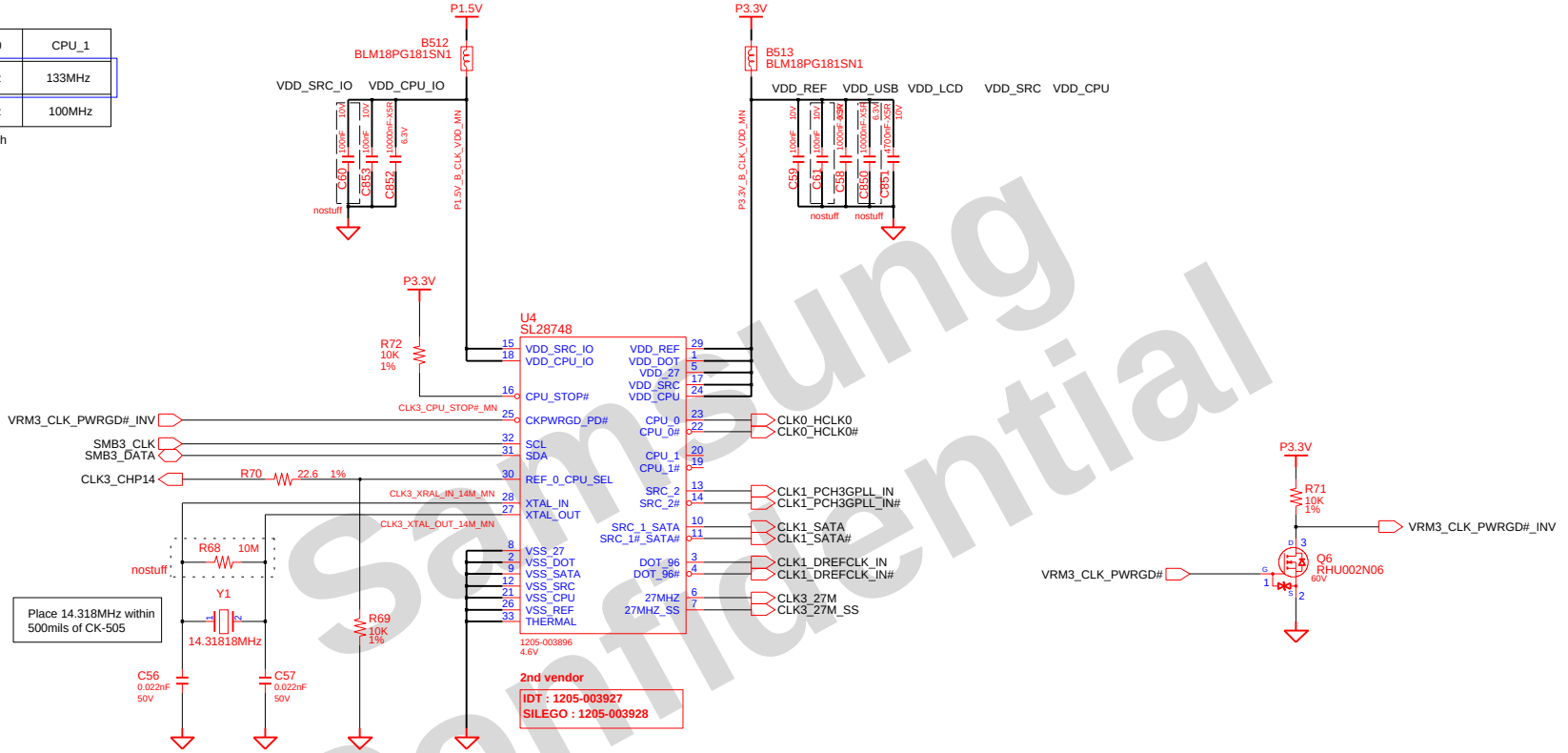
CK505M SHRINK VERSION

CPU_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

*CPU_SEL During CK_PWRGD Latch



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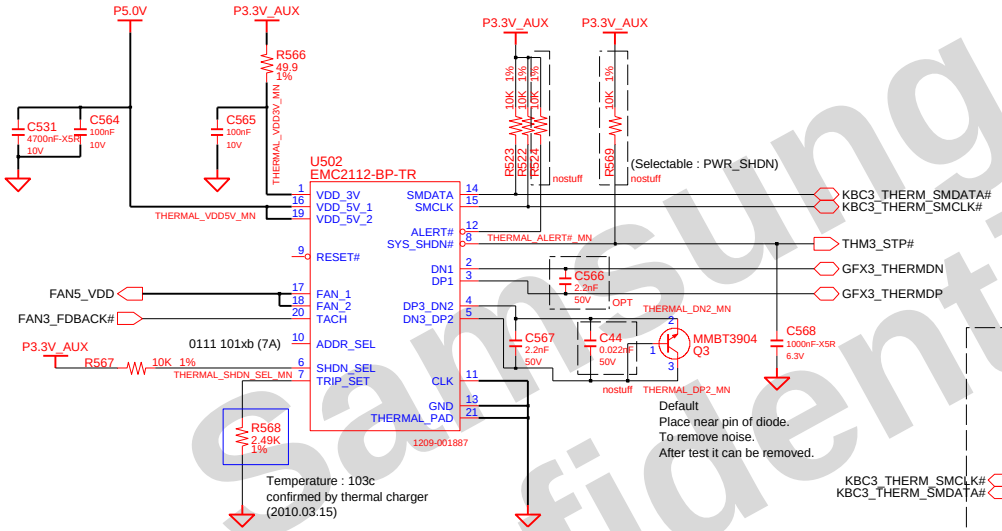
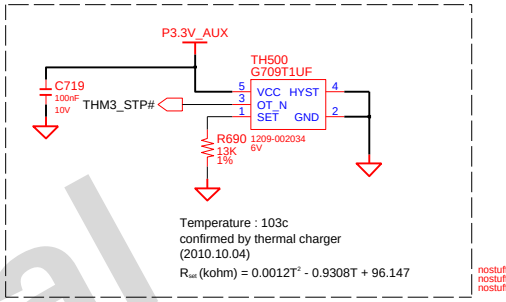
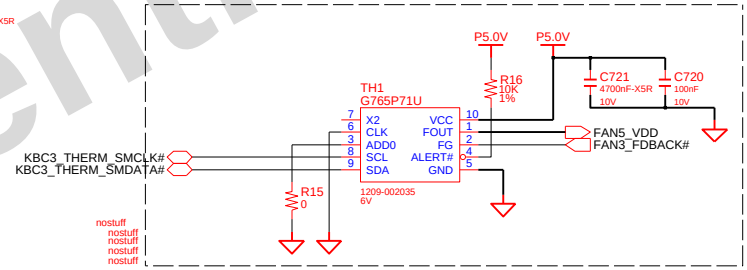
THERMAL SENSOR & FAN CONTROL

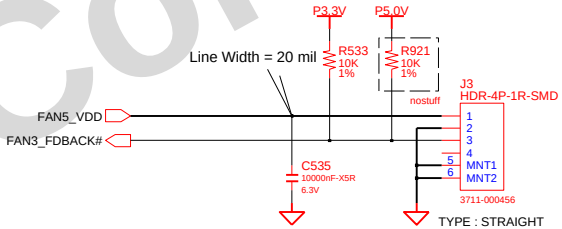
ADDRESSS_SEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

SHDN_SEL MODE	
0	INTEL TR MODE
HIGH Z	AMD CPU/DIODE MODE
✓ 1	EXT.DIODE 2 MODE

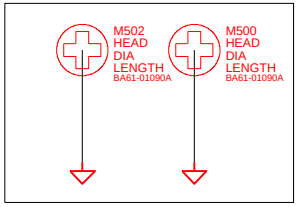








FAN



DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L THERMAL SENSOR THERMAL SENSOR EMC2112	SAMSUNG ELECTRONICS		
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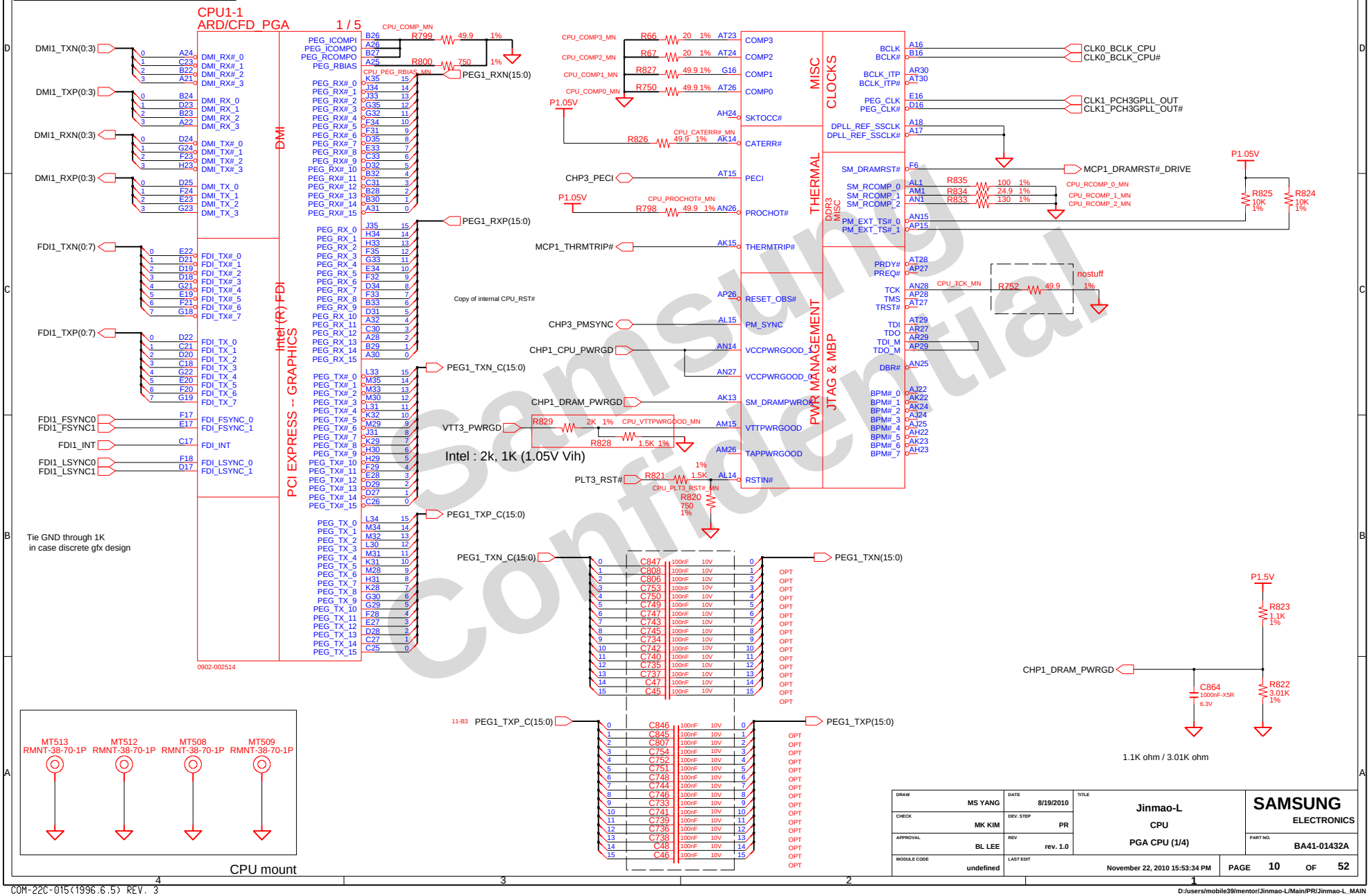
ARRANDALE PROCESSOR (DMI,PEG, FDI)



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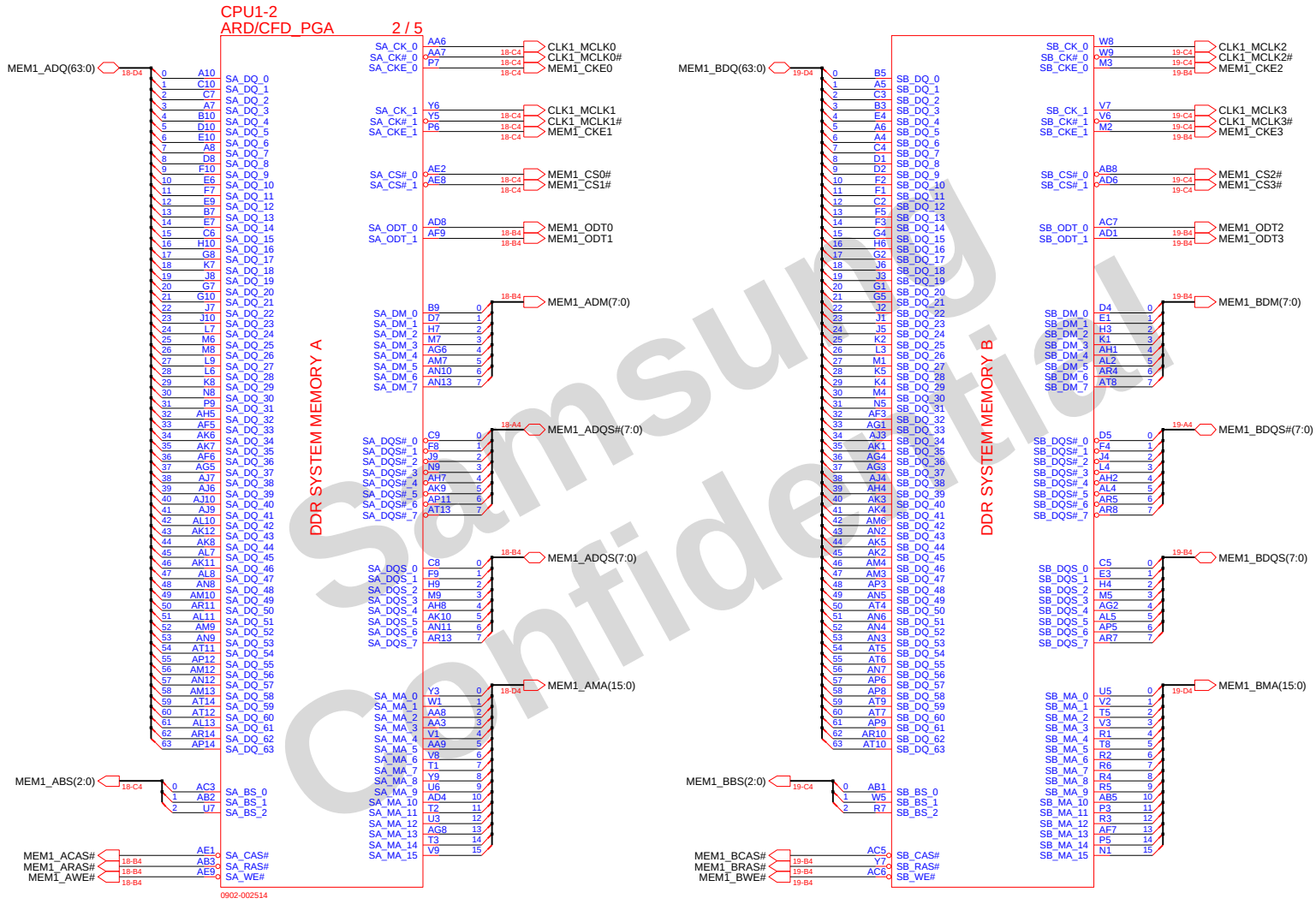

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14x 22 uF : CPU VR side

ALL VTT DECAP IS SHARED

CPU_CORE

CPU1-3 ARD/CFD_PGA 3 / 5

CPU CORE SUPPLY POWER

1.1V RAIL POWER

P1.05V

IGFX_CORE

nostuff

2A ROUTING NEEDED.

CPU VIDS

PSI# → CPU1_PSI#

VID_0 VID_1 VID_2 VID_3 VID_4 VID_5 VID_6 → CPU1_VID(6:0)

PROC_DPRSLPVR → CPU1_DPRSLPVR

VTT_SELECT

VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD

VTT_SEL signal (for CFD/ARD shared)

SENSE LINES

ISENSE → VRM3_IMVP_IMON

VCC_SENSE → CPU1_VCCSENSE

VSS_SENSE → CPU1_VSSSENSE

VTT_SENSE

VSS_SENSE_VTT

R28 100 1%

R29 100 1%

0902-002514

**VTT POWER SELECTION

VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD

CPU1-4 ARD/CFD_PGA 4 / 5

SENSE LINES

VAXG_SENSE → GFX1_VCCSENSE

VSSAXG_SENSE → GFX1_VSSSENSE

GRAPHICS VIDS

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VID_5 GFX_VID_6 → GFX1_VID(6:0)

ADD 1K PD in discrete GFX design

GFX_VR_EN → GFX1_VR_EN

GFX_DPRSLPVR → GFX1_DPRSLPVR

GFX_IMON → GFX1_VR_IMON

GRAPHICS POWER

DDR3 - 1.5V RAILS

P1.5V

FDI

PEG & DMI

1.1V

1.8V

P1.8V

0902-002514

	1uF	10uF	22uF	330uF
w Proddizer	25 pcs	0 pcs	16 pcs	0 pcs
w/o Proddizer	25 pcs	16 pcs	12 pcs	4 pcs

DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L / CPU / PGA CPU (3/4)	SAMSUNG ELECTRONICS
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APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
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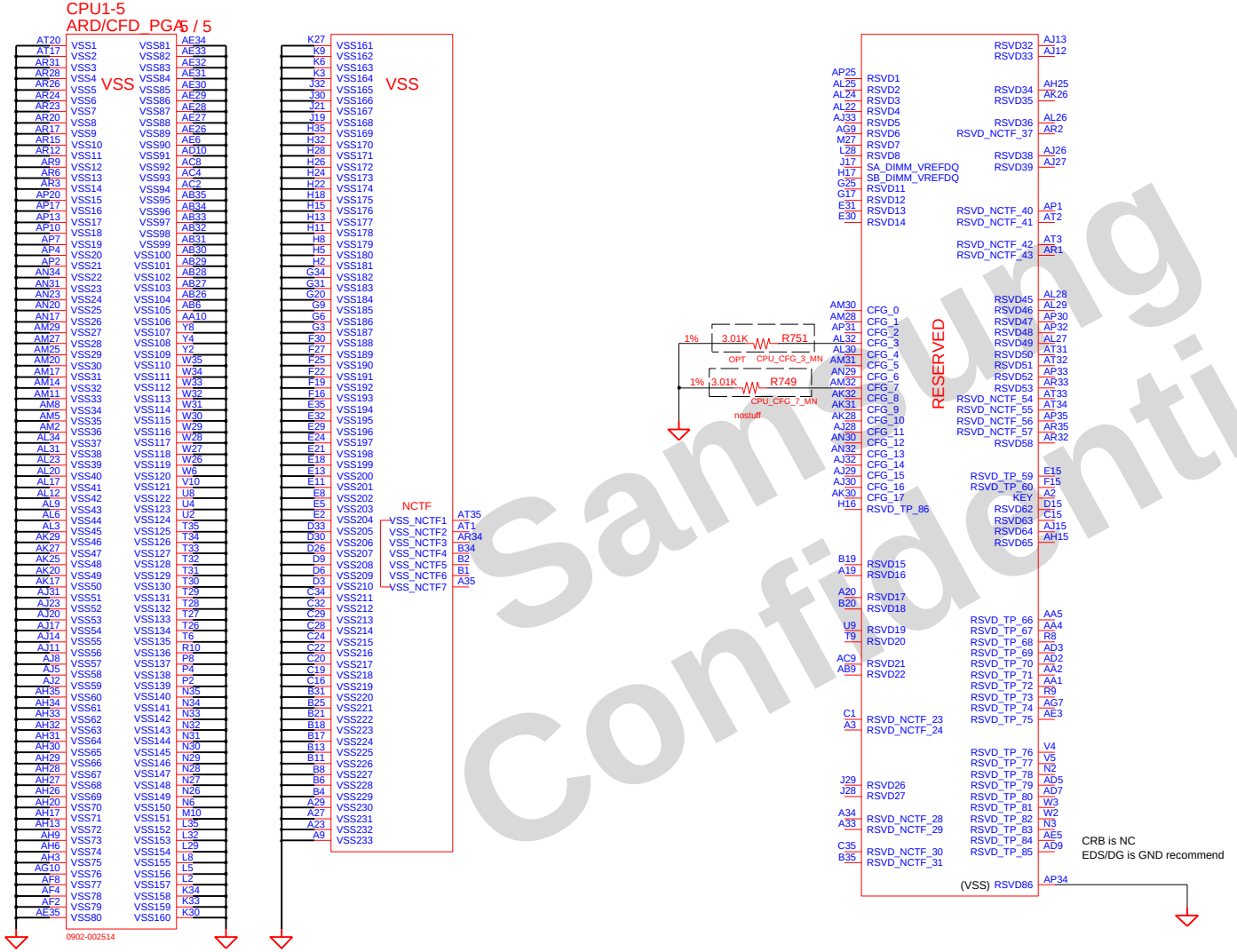

Clarksfield : SA_DIMM_VRREFDQ, 100K PD
SB_DIMM_VRREFDQ, 100K PD

Arrandale : SA_DIMM_VRREFDQ, NC
SB_DIMM_VRREFDQ, NC

CFG Straps for Processor

PCI Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifunction enabled

PCI Express Static Lane Reversal	
CFG3	1 : Normal operation 0 : Lane Reversed

Display Port Presence	
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP

PCIE 2.0 SUPPORT	
CFG7	1 : Normal operation 0 : PCIE2.0 Jitter support

DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L CPU PGA CPU (4/4)	SAMSUNG ELECTRONICS
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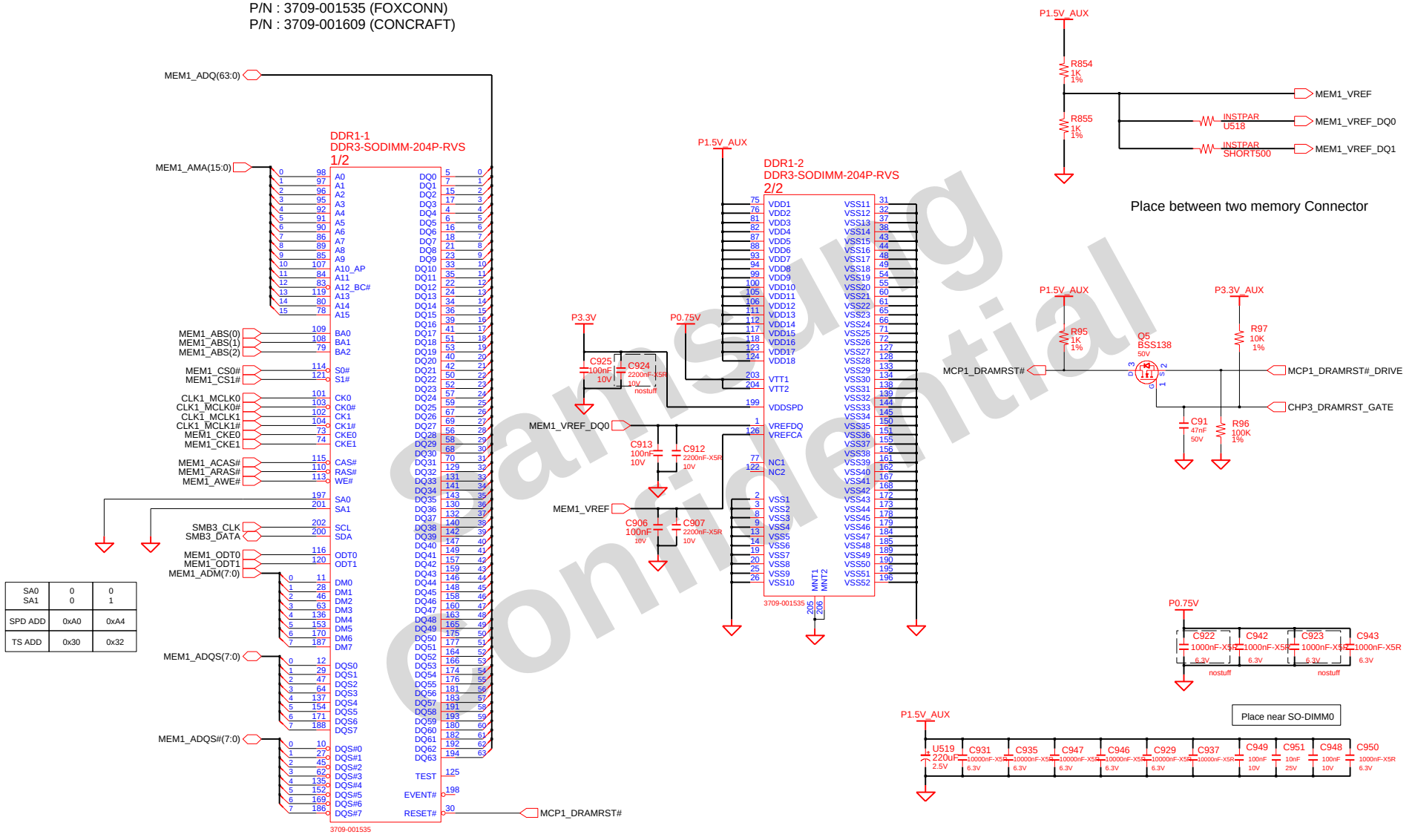
DDR SO-DIMM #0

Height : 9.2 mm (REVERSE)

P/N : 3709-001535 (FOXCONN)
P/N : 3709-001609 (CONCRAFT)



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REV	rev. 1.0	
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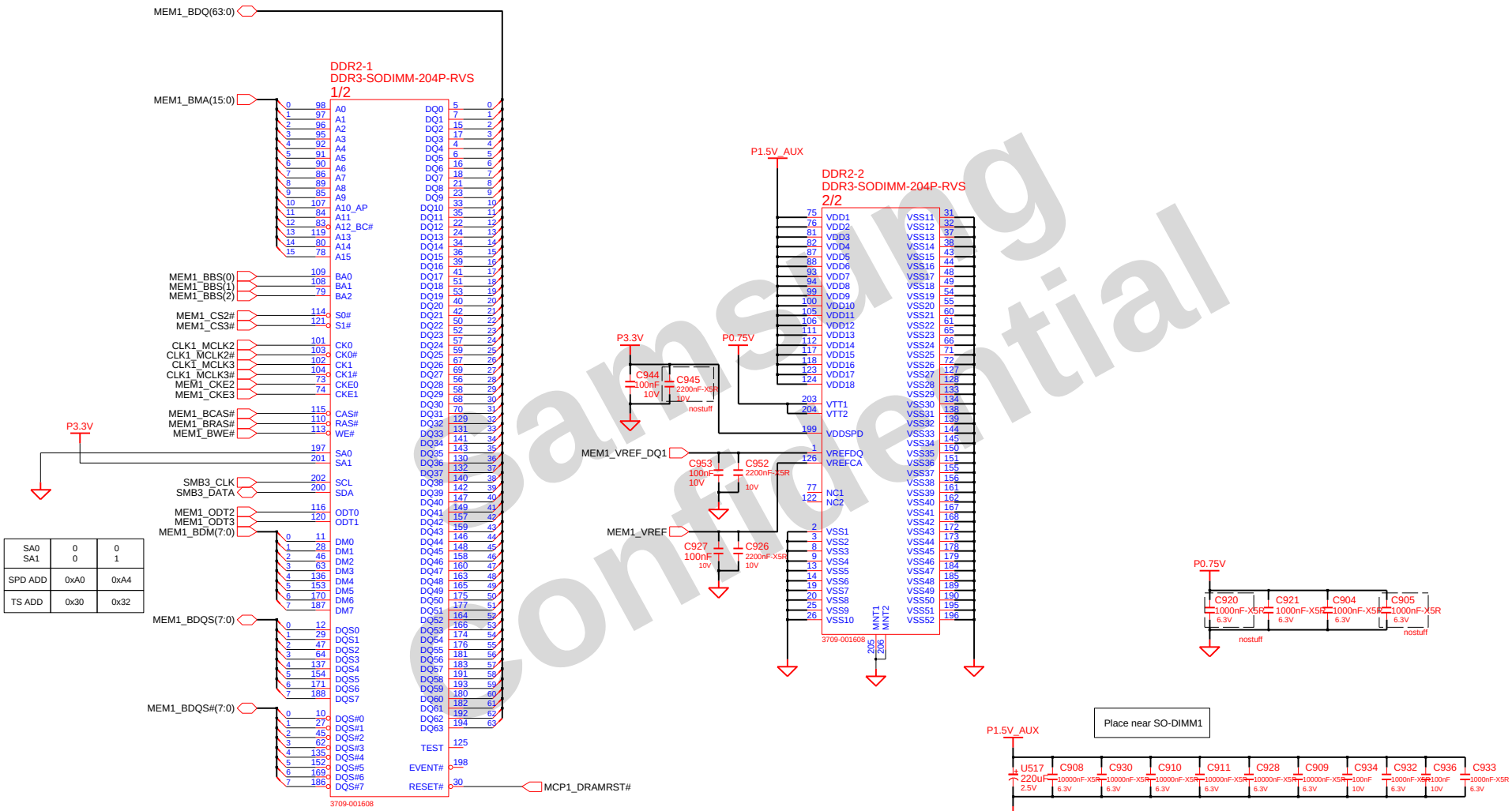
DDR SO-DIMM #1

Height : 4 mm (REVERSE)

P/N : 3709-001608 (CONCRAFT)



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DRAW	MS YANG	
CHECK	MK KIM	
APPROVAL	BL LEE	
MODULE CODE		
DATE	8/19/2010	
DEV. STEP	PR	
REV	rev. 1.0	
LAST EDIT	November 22, 2010 15:53:34 PM	
TITLE	Jinmao-L SODIMM B DDR3	
SAMSUNG ELECTRONICS		
PART NO.	BA41-01432A	

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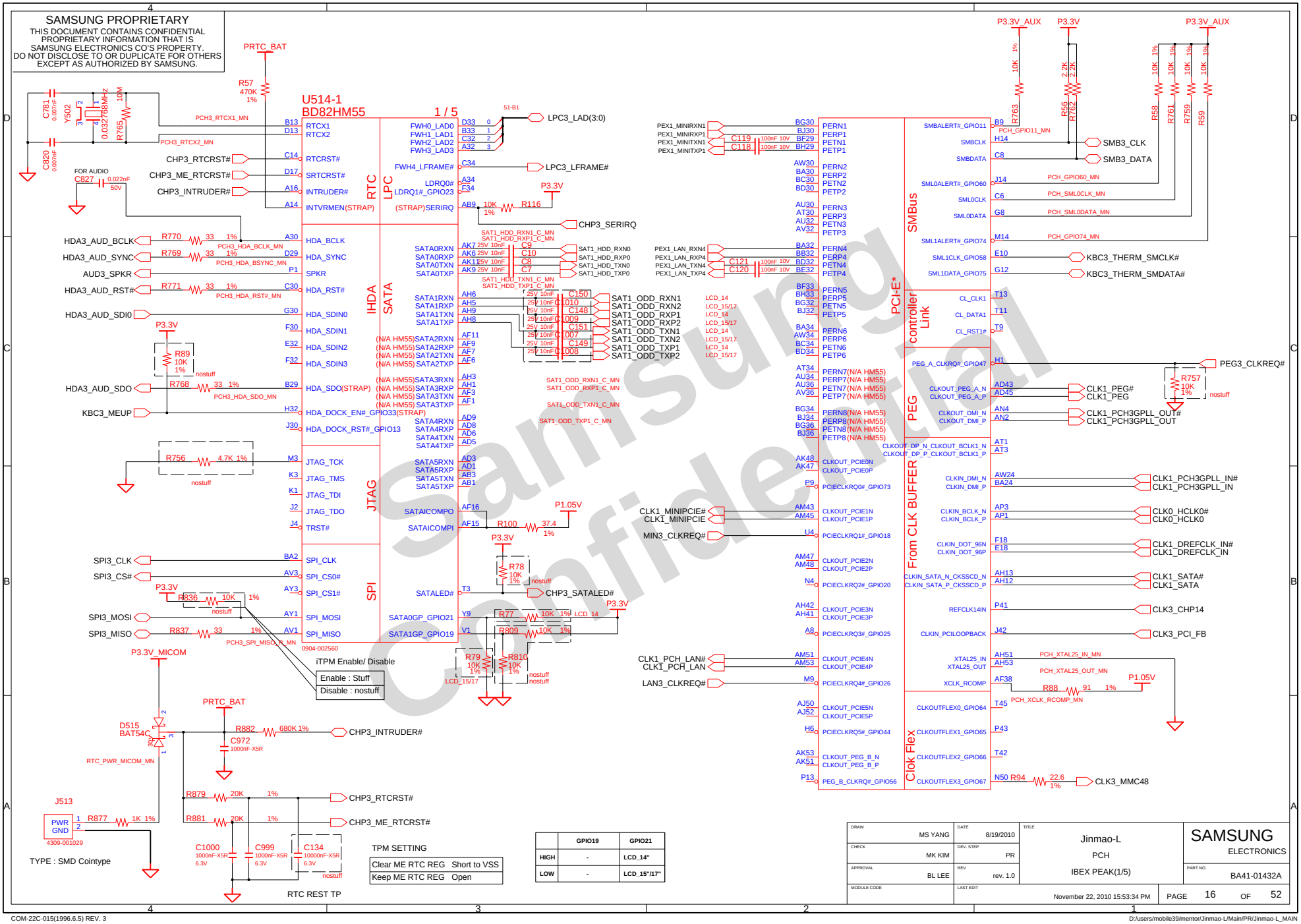

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DRAW	DATE	TITLE	SAMSUNG ELECTRONICS
MS YANG	8/19/2010	Jinmao-L PCH IBEX PEAK(1/5)	
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 16 OF 52	

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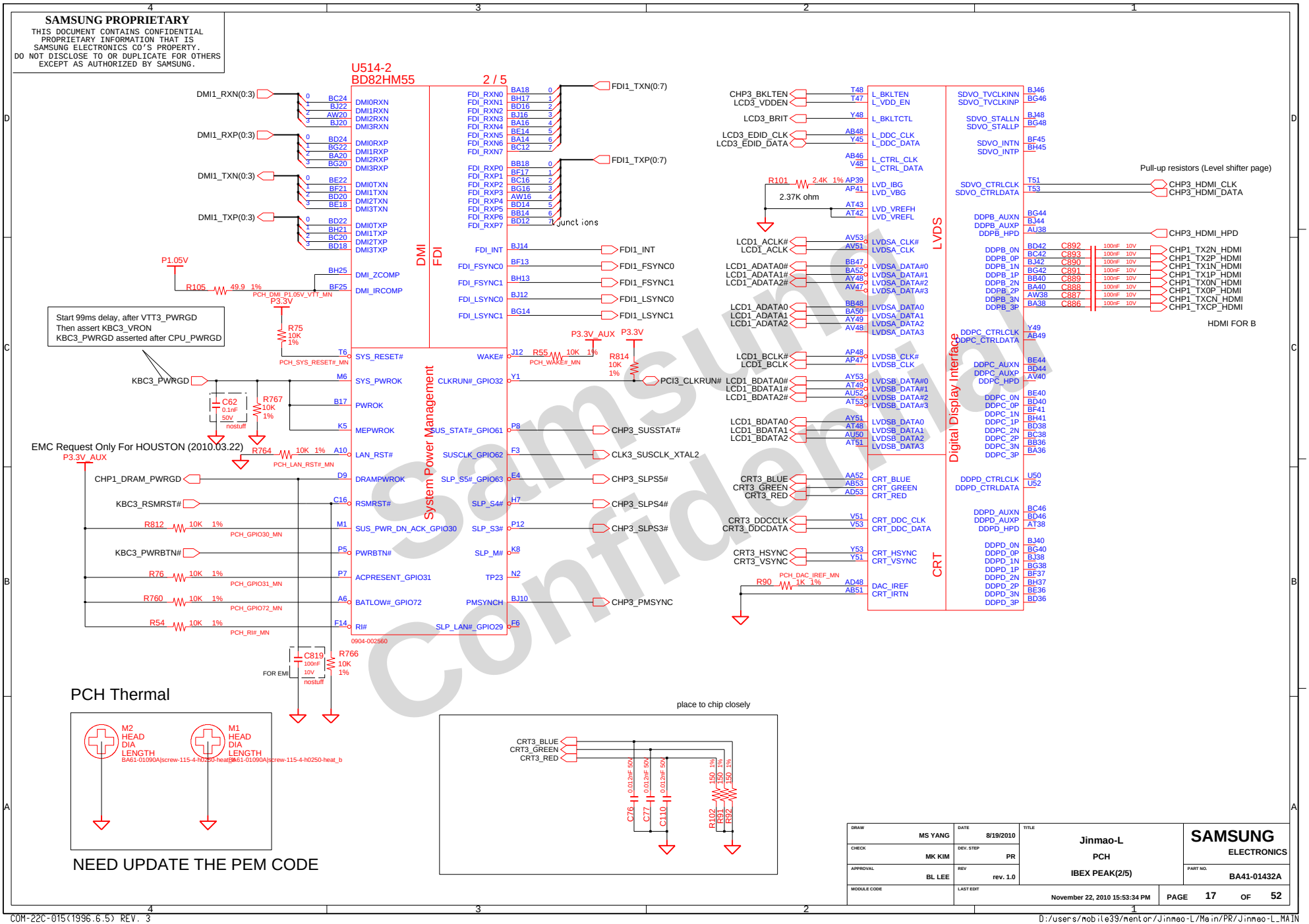

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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PCH IBEX PEAK(2/5)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
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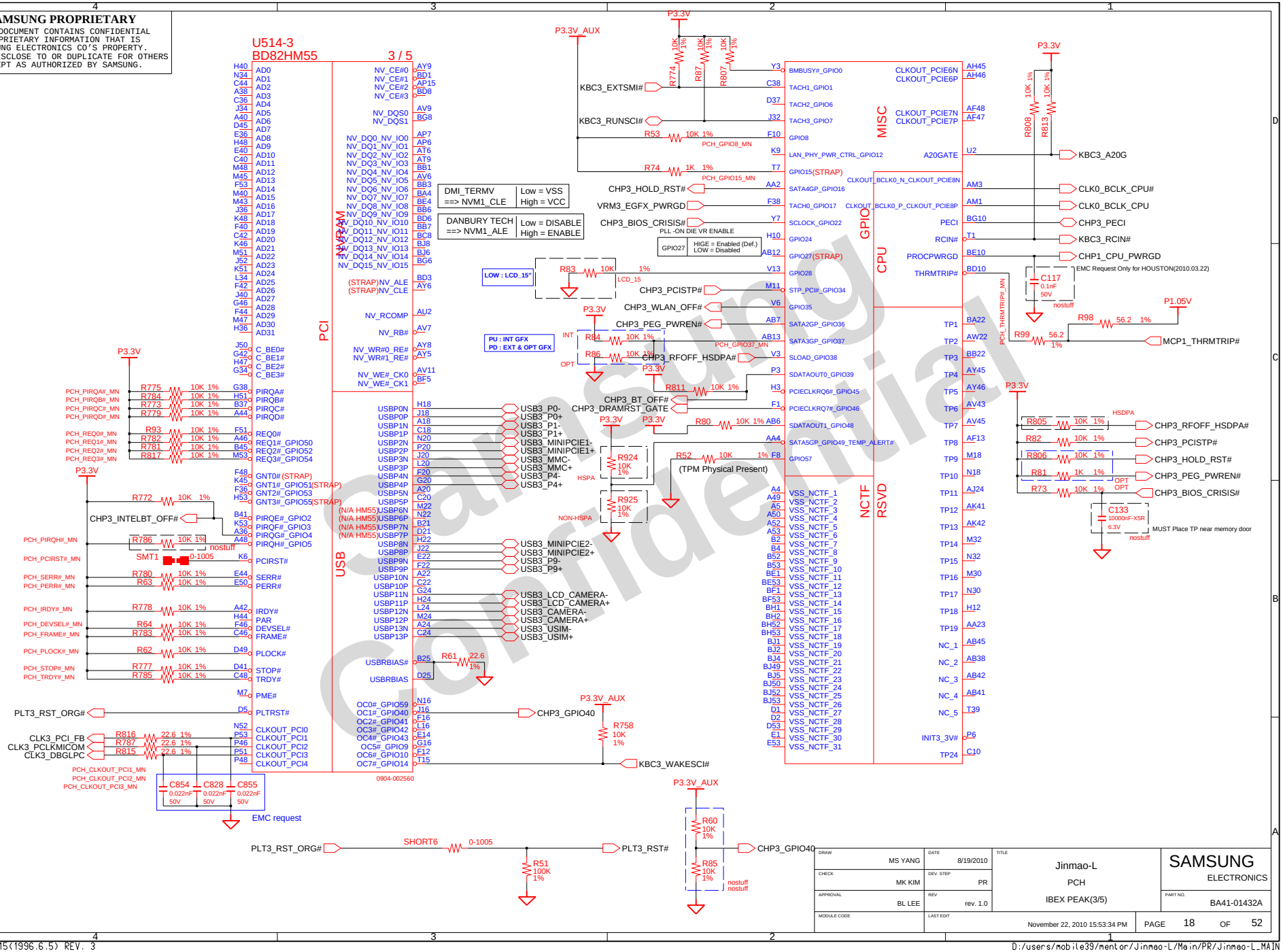

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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PCH IBEX PEAK(3/5)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
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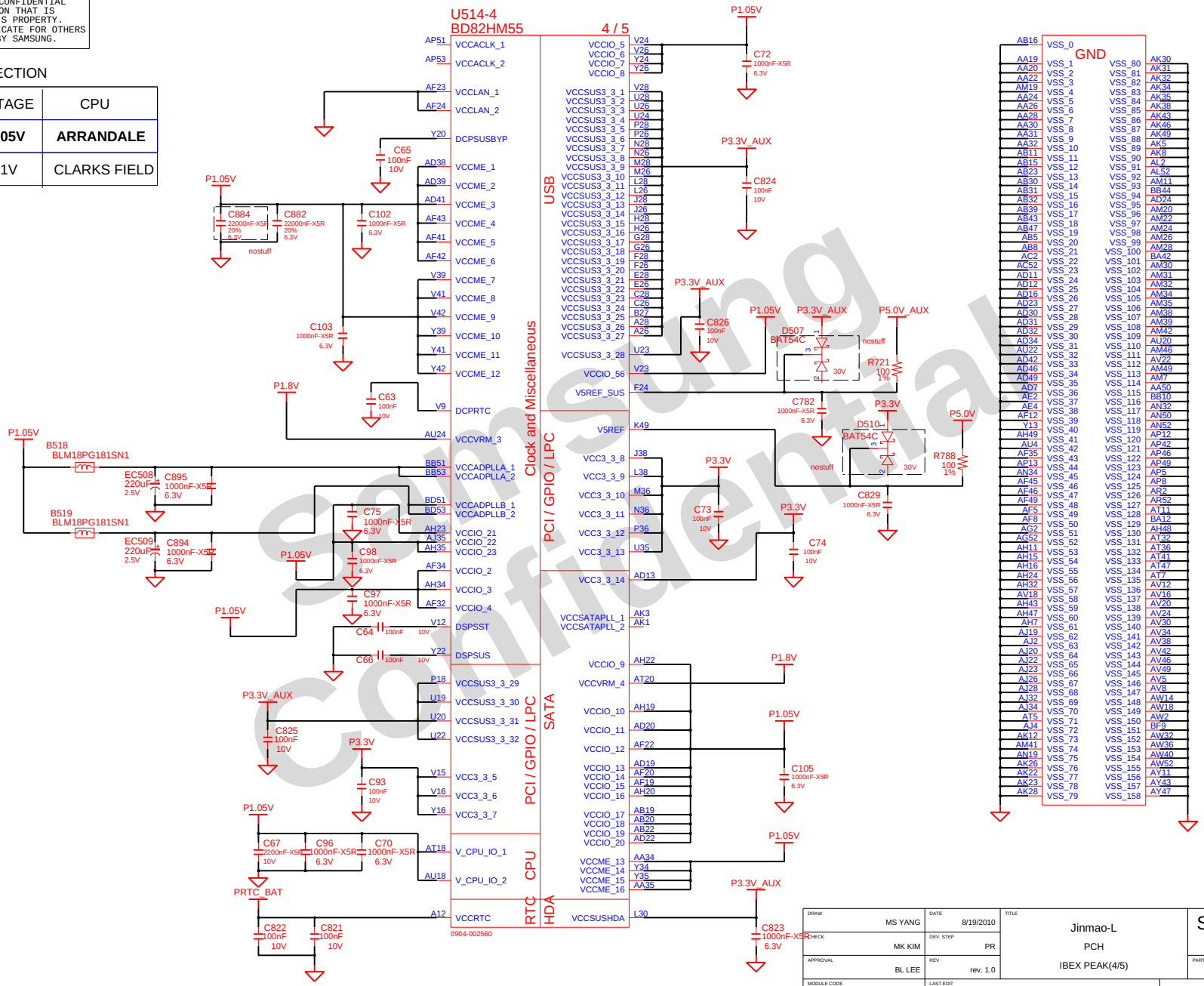
**VTT POWER SELECTION

VTT_SEL	VOLTAGE	CPU
1	**P1.05V**	**ARRANDALE**
0	P1.1V	CLARKS FIELD



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PCH IBEX PEAK(4/5)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE: 52	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 19 OF 60	

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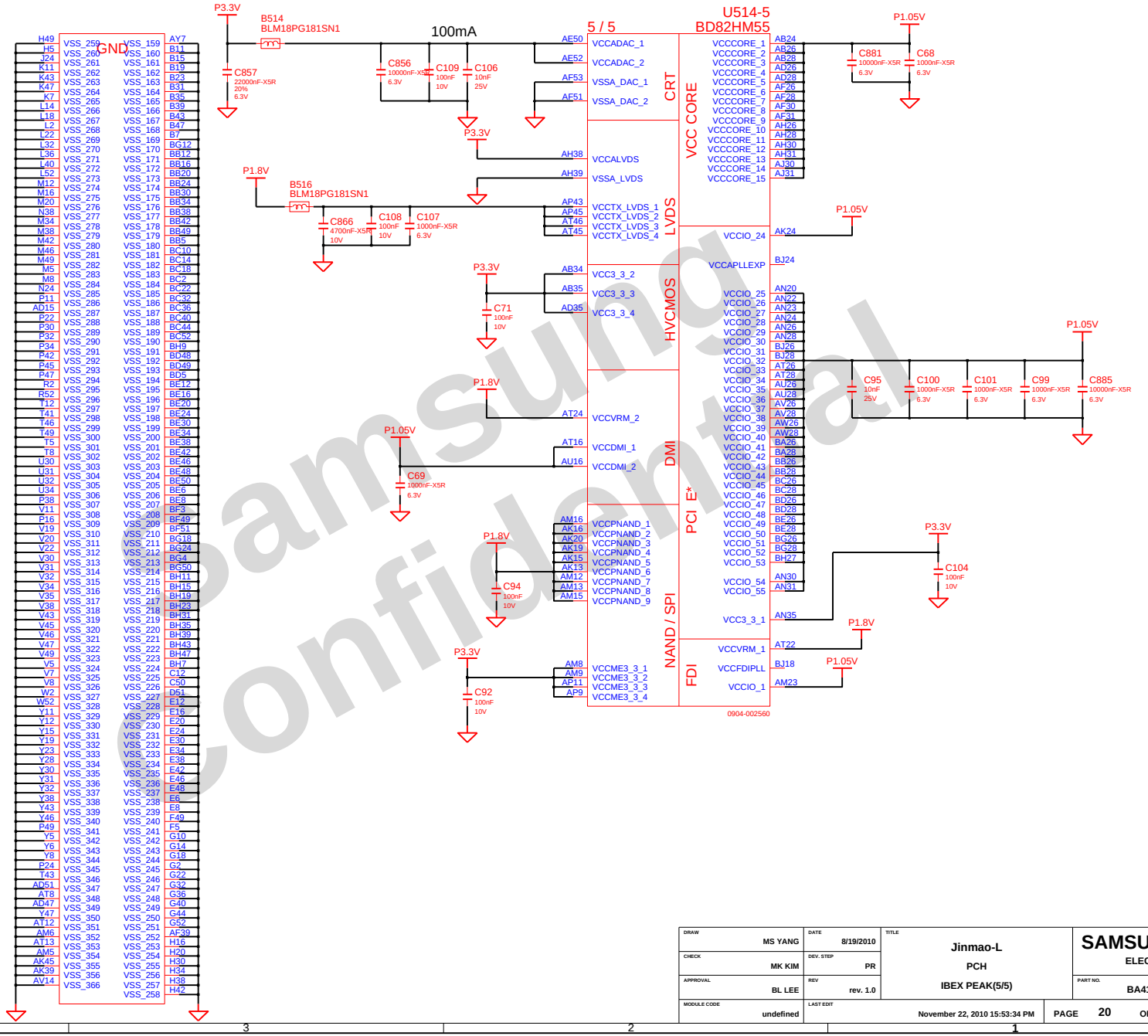

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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PCH IBEX PEAK(5/5)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 20 OF 52	

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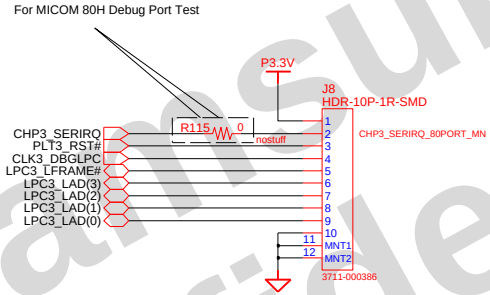
80H PORT DEBUG



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L / DEBUG PORT / 80H DECODER	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 21 OF 52	

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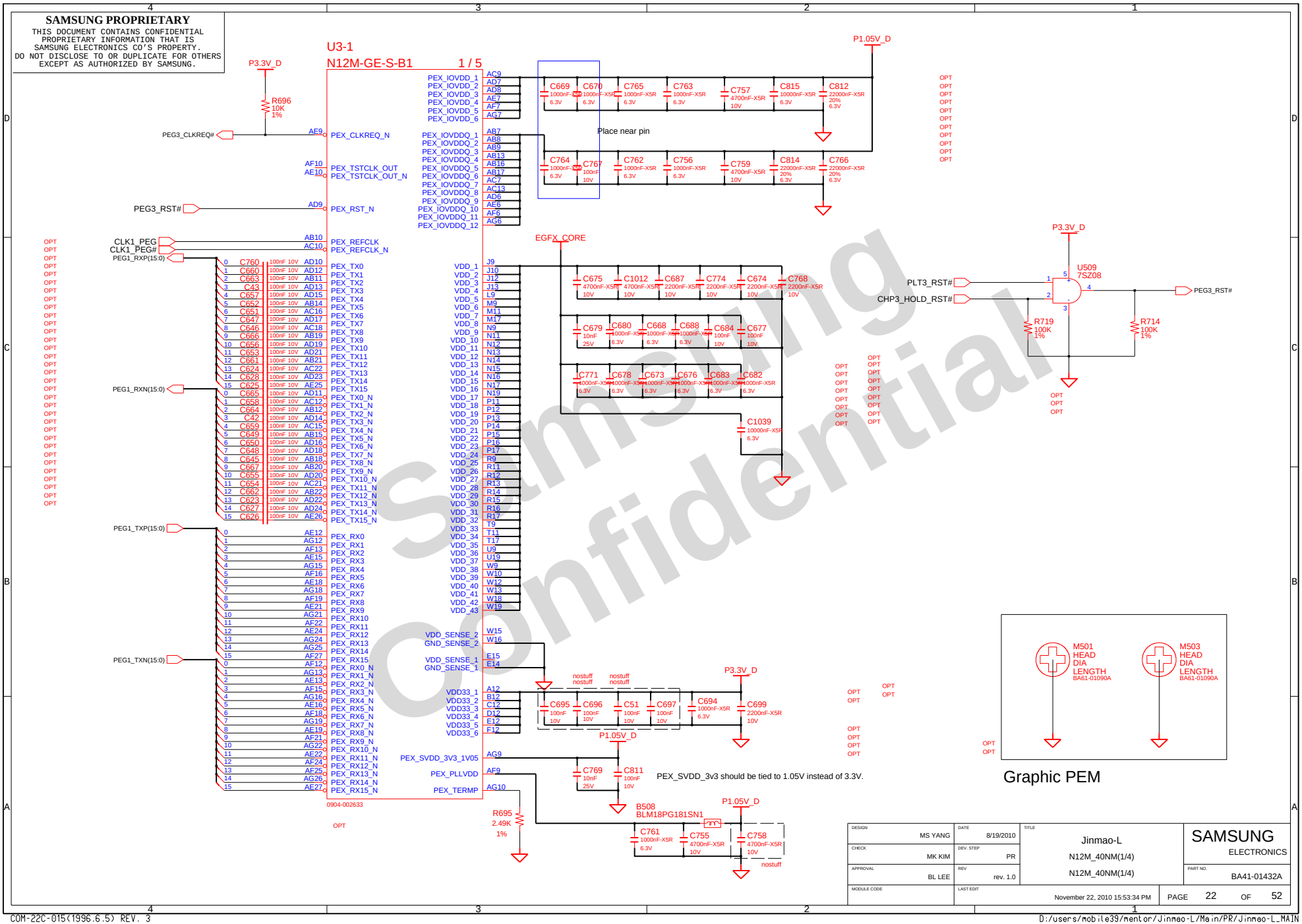

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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L N12M_40NM(1/4) N12M_40NM(1/4)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 22 OF 52	

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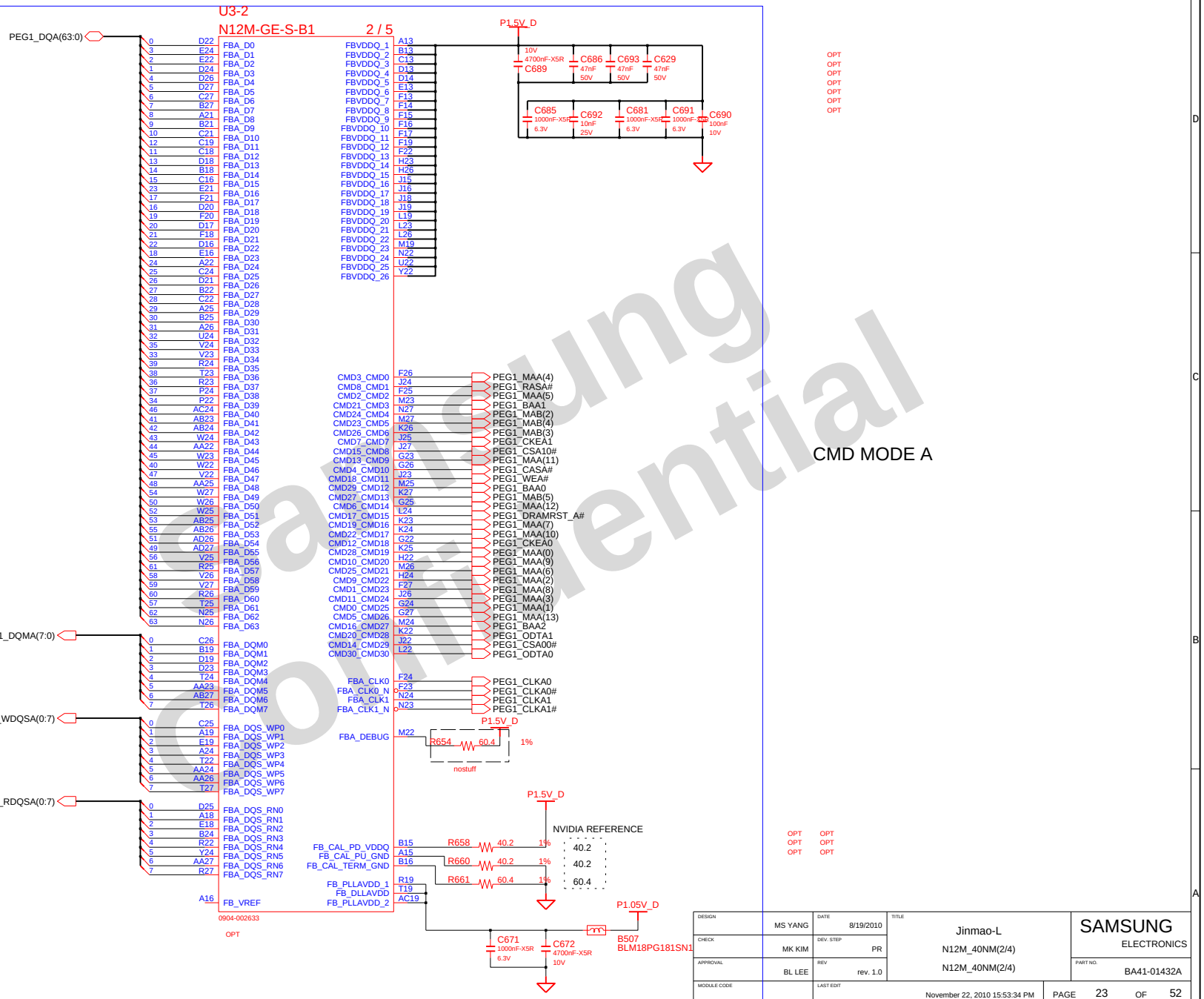

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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L N12M_40NM(2/4) N12M_40NM(2/4)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 23 OF 52	

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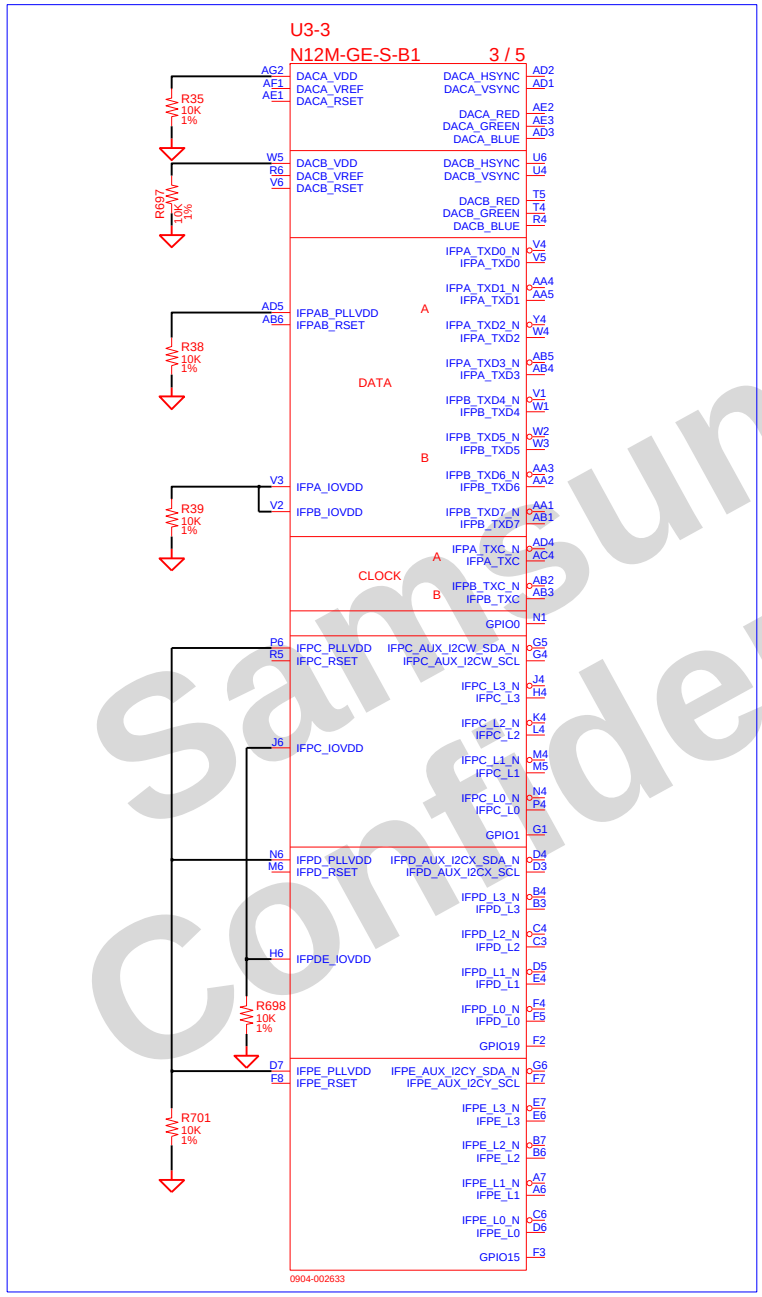

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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L N12M_40NM(3/4) N12M_40NM(3/4)	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 24 OF 52	

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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LCD0_BL_PWM	High
GPIO(3)	LCD0_VDD	High
GPIO(4)	LCD0_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V 10 0.95V
GPIO(6)	GPU VID1	01 0.85V 11 1.03V
GPIO(7)	GPU VID2	NC
GPIO(8)	OVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0 27MHz	
5K ohm	**1000**	**0000**	RAM CFG (SEC)	
10 Kohm	**1001**	**0001**	0011 gDDR3 1Gb	
15K ohm	**1010**	**0010**	USER[3:0]=1111 for EDID	
20K ohm	**1011**	**0011**	PADCFG[3:0]=0110 for NB	
25K ohm	**1100**	**0100**		
30K ohm	**1101**	**0101**		
35K ohm	**1110**	**0110**		
45K ohm	**1111**	**0111**		

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	0	27M
SCLK	1	0	1	0	N11M-GE GFX TPYE
	0	0	1	0	N11M-LP1
SI	0	0	1	1	gDDR3 1Gb
SI	0	1	1	1	gDDR3 2Gb
Strap2	0	0	0	0	N11M-GE2
Strap2	0	1	0	1	N11M-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

U3-4
N12M-GE-S-B1 4 / 5

U3-5
N12M-GE-S-B1
5 / 5

Function Straps

STRAP0	User Strap	
	EDID is used	**1111**
	Customer defined	1000 - 1100
	1024 x 768	0000 - 0001
	1280 x 1024	0010
STRAP1	GPU PCIe Interface Strap	
	GB1	**1110**
	GB2	0110
	DeskTop	0000
ROM_SO	Int PCIe Clock - 277MHz(default)	
	Aperture Size - 256MB(default)	
	I2C Address of GPU - 0x9E(default)	
	Device Type - 3D Device(Optimus)	
ROM_SI	Memory Configuration :	
	Samsung 64M x 16 gDDR3	**0011**
	Samsung 128M x 16 gDDR3	**0111**

Chip Select Straps (N12M-GB1)

GFX3_ROM_SCLK	N12M-GE	15K PU
GFX3_STRAP2	N12M-GE	15K PU

N12M-GE : 0x0A**7A** (1010 / 1010)

Chip Select Straps (N11M-GB1)

GFX3_ROM_SCLK	N11M-GE2	15K PU
GFX3_STRAP2	N11M-GE2	5K PD

N11M-GE2 : 0x0A**70** (1010 / 0000)

nVidia Request
(About Thermal)

Place near chip

DESIGN	MS YANG	DATE	8/19/2010	TITLE: Jinmao-L N12M_40NM(4/4) N12M_40NM(4/4)
CHECK	MK KIM	DEV. STEP	PR	SAMSUNG ELECTRONICS
APPROVAL	BL LEE	REV	rev. 1.0	PART NO. BA41-01432A
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM	PAGE 25 OF 52

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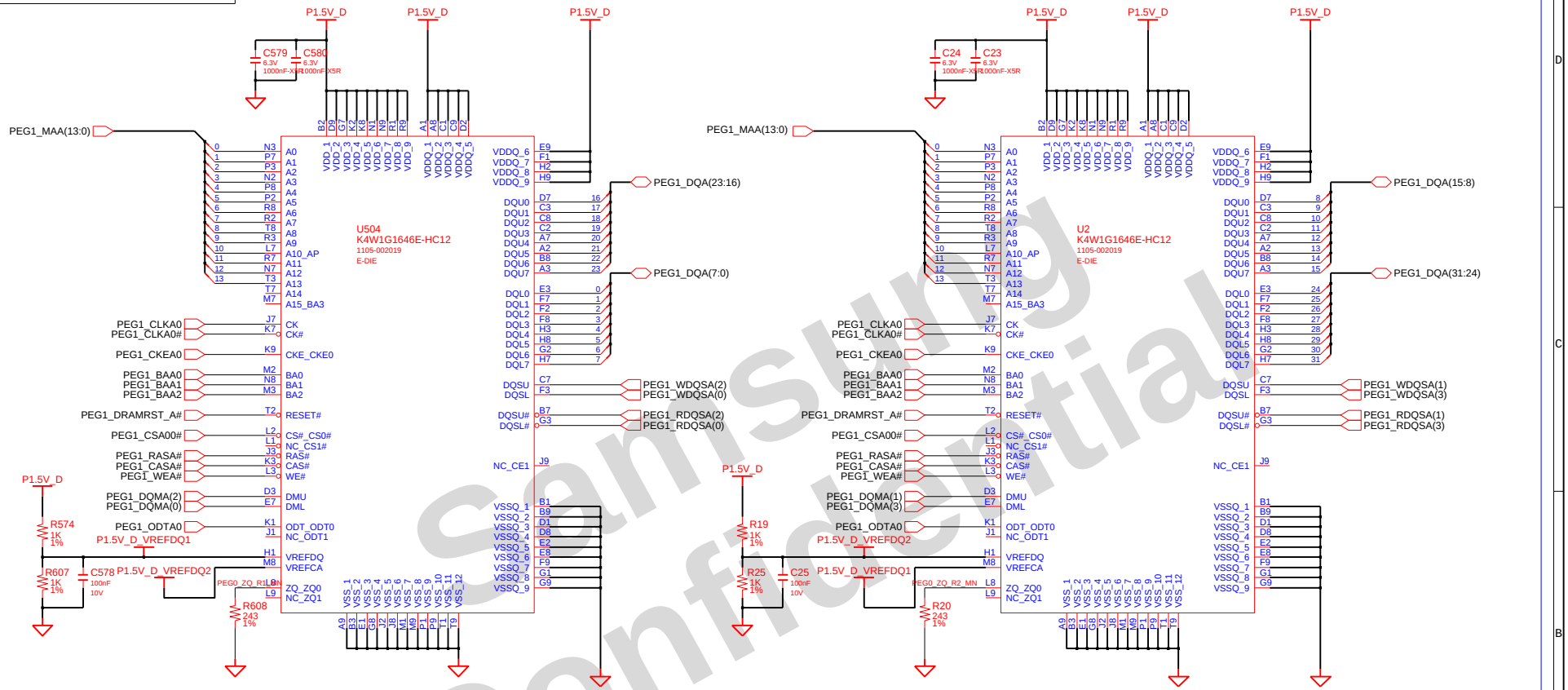
A-Channel #0



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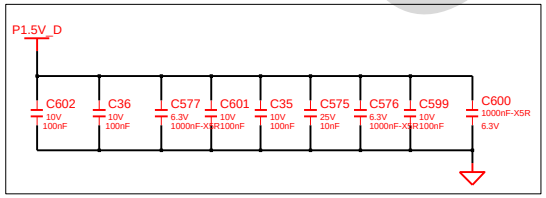
Place near to VDDQ



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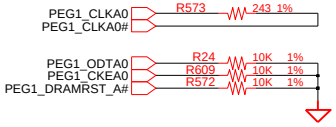
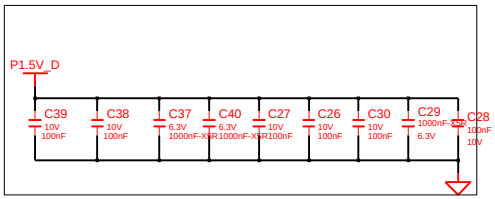


Place near to VDDQ



OPT OPT OPT OPT OPT OPT OPT OPT OPT OPT OPT OPT

DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L GRAPHIC_MEM A#0 GRAPHIC_MEM A#0	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 26 OF 52	

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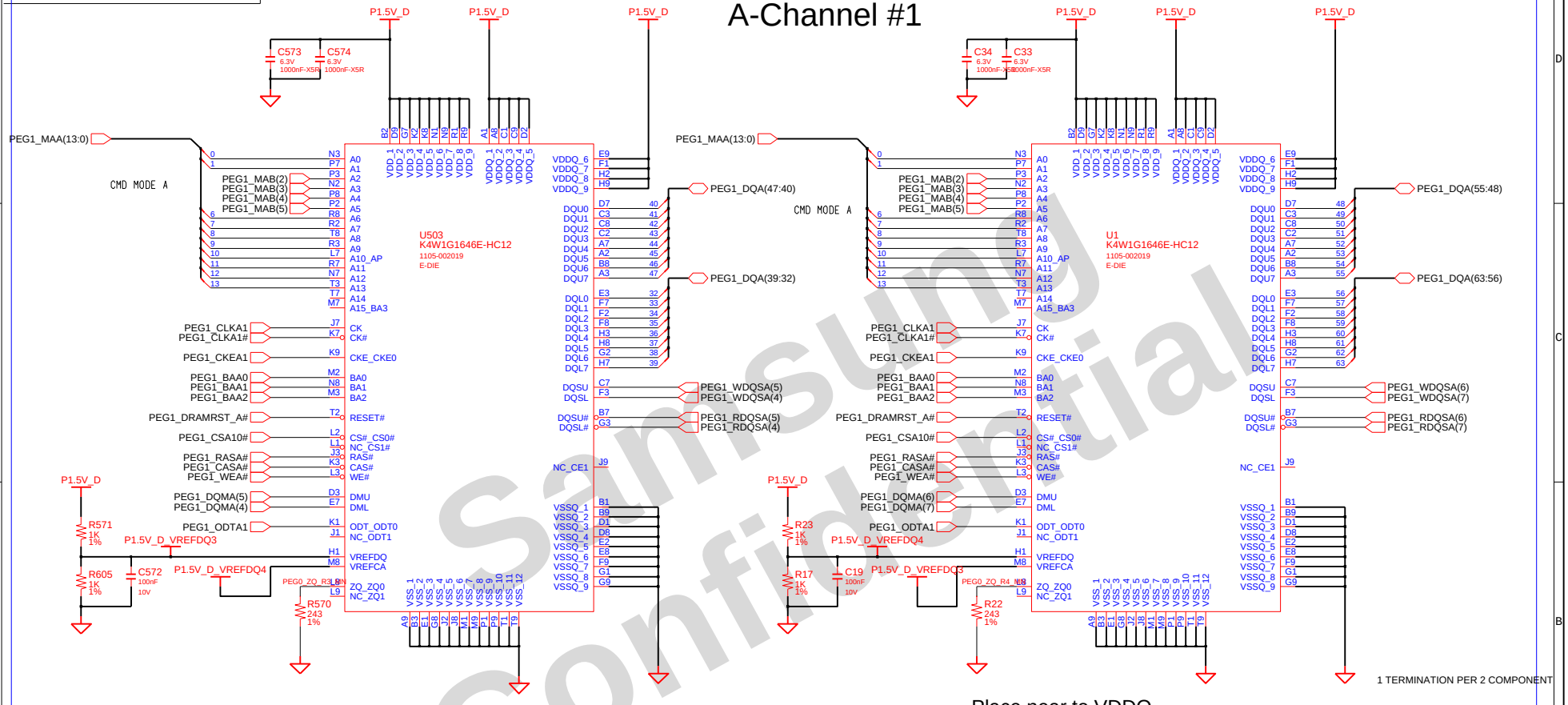
A-Channel #1



DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L GRAPHIC_MEM A#1 GRAPHIC_MEM A#1	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 27 OF 52	

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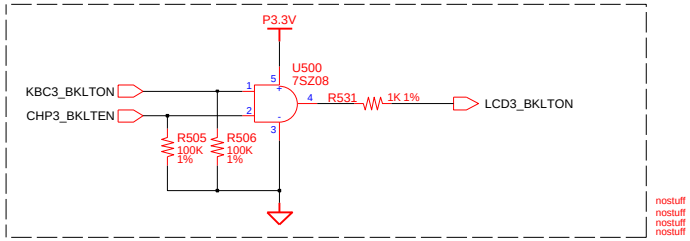
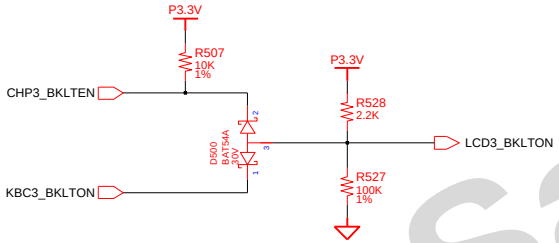
LVDS LOGIC

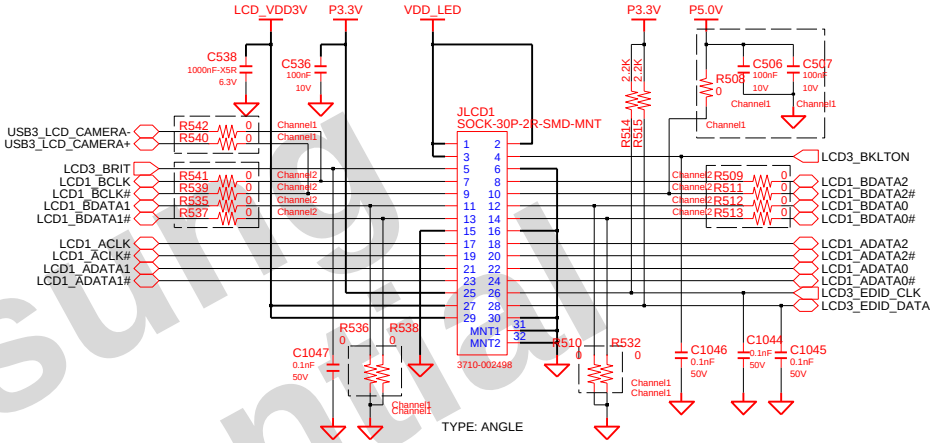
Backlight On



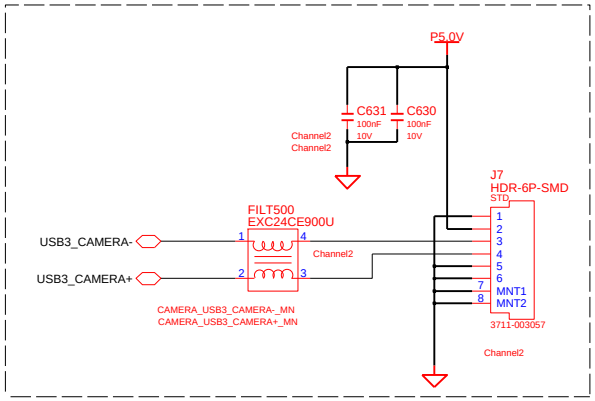


1Ch. LCD Connector + CAMERA

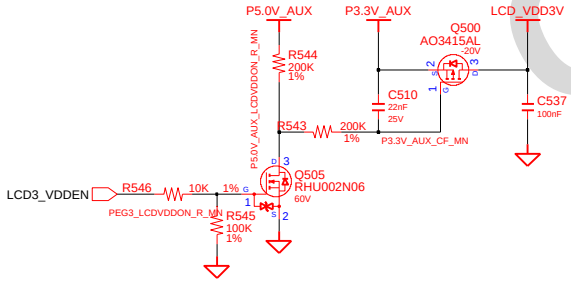
NOTE : Place R20 close to connector to minimize stub



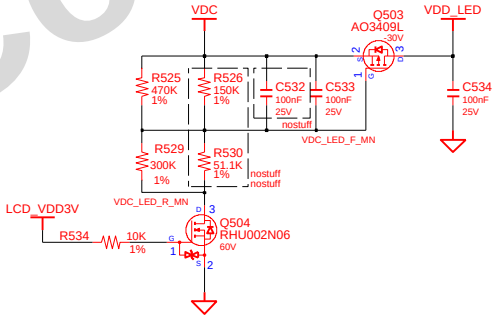
CAMERA CONN FOR 2ch LVDS



LCD Power



LED Power



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 28 OF 52	

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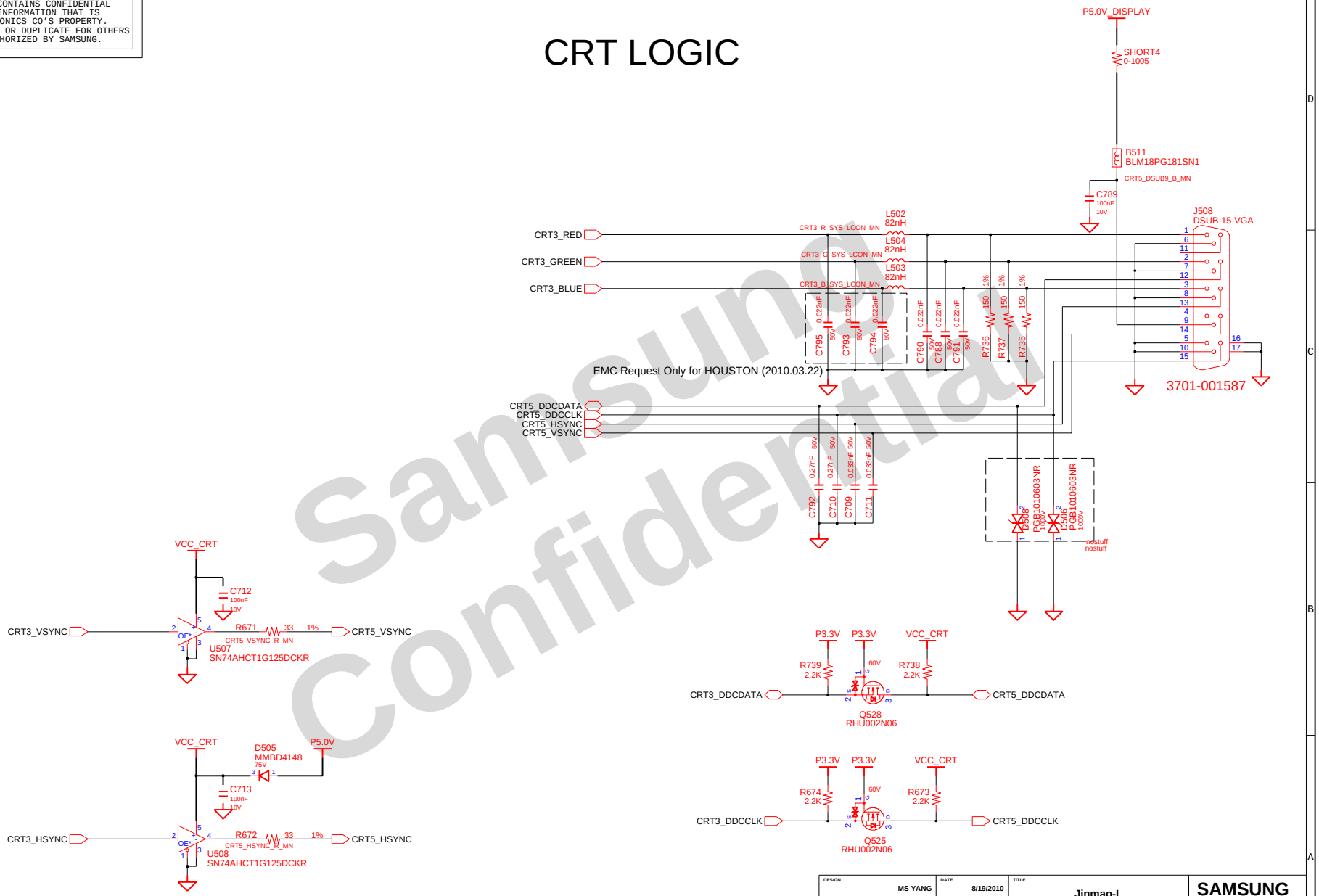
CRT LOGIC



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L GRAPHICS_IF CRT	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 29 OF 52	

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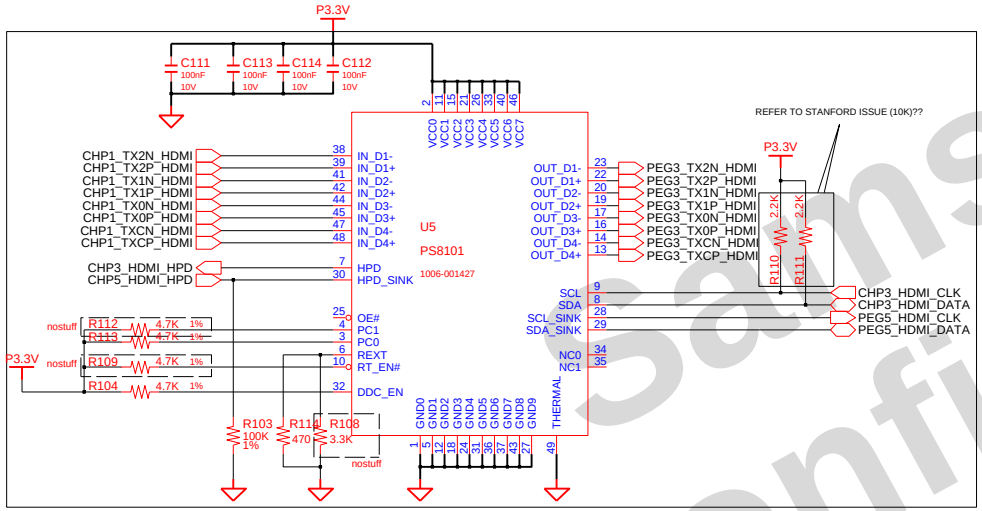
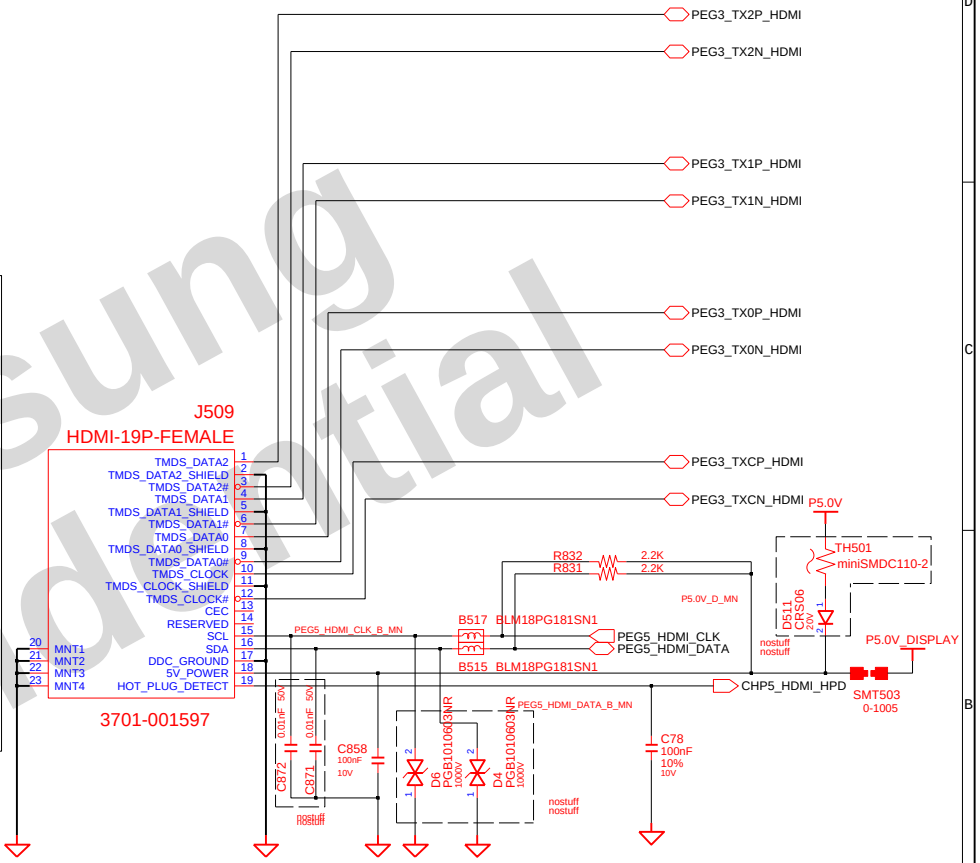
After checking, Houston need to use CMC for each signal.

(EMC request at 2010.04.15)

HDMI Graphic





FOR PS8101

PC1	PC0	
00	8dB	
01	4dB	
10	12dB	←
11	0dB	

FOR ASM1442

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew rate	
0	0	0	450mV	0dB	0dB	
0	0	1	490mV	0dB	-3dB	
0	1	0	450mV	0dB	-3dB	←
0	1	1	460mV	0dB	-4dB	
1	0	0	340mV	0dB	0dB	
1	0	1	400mV	2dB	0dB	
1	1	0	400mV	2dB	0dB	
1	1	1	420mV	0dB	0dB	

N10x/N11x_40nm HDMI/DP/LVDS support only 3.3V voltage tolerance

HDMI Level Shifter	REXT(Pin6)	PC1_CG0(Pin3)	PC1_CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note	4-6 CODE
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC		1006-001427
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing	1006-001471

FOR ASM1442

EQ_1	EQ_0	Equalization	
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	← Internal Default Value

DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 30 OF 52	

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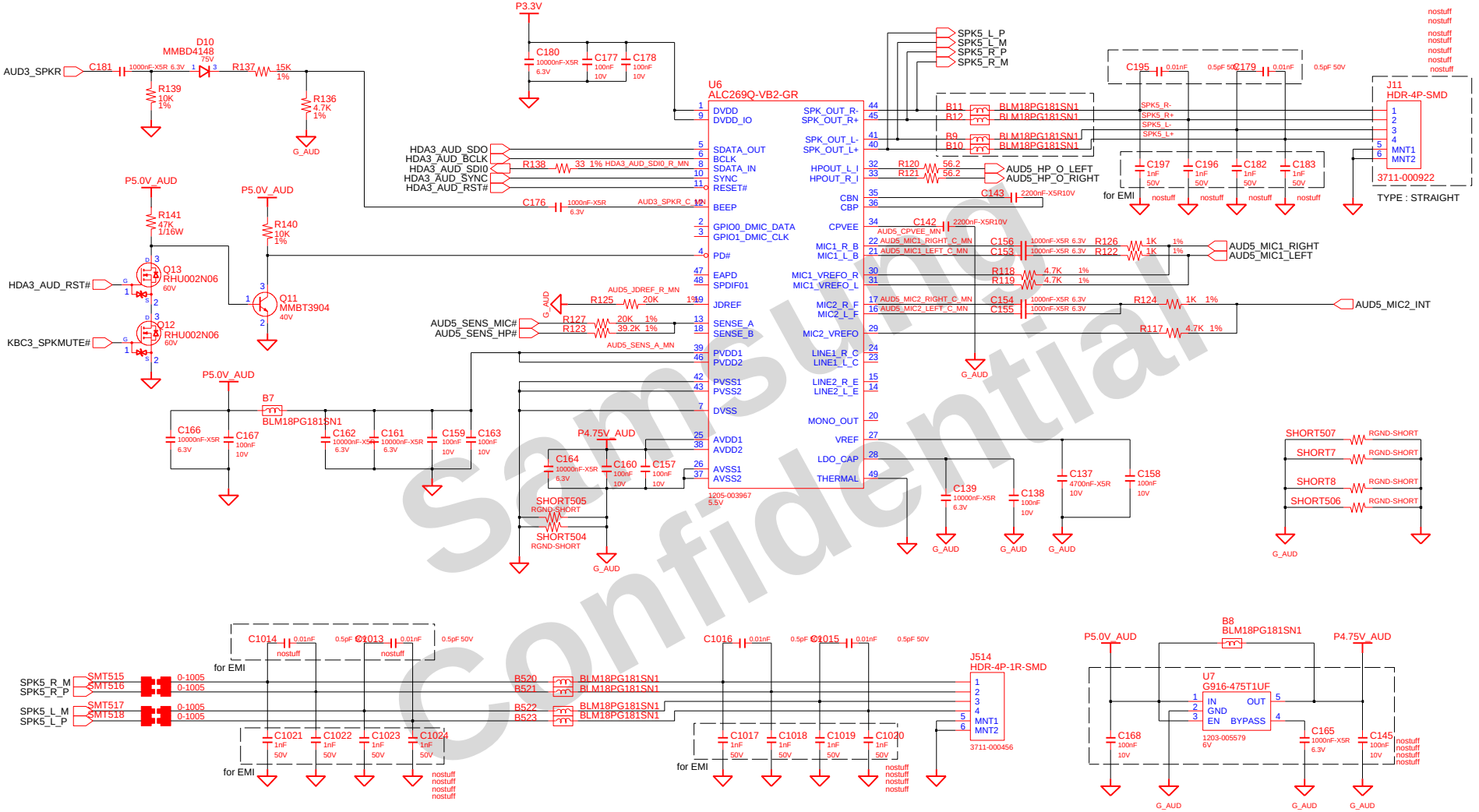
HD AUDIO



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L HDA_CODEC SUB AUDIO CODEC ALC269 SUB	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 31 OF 52	

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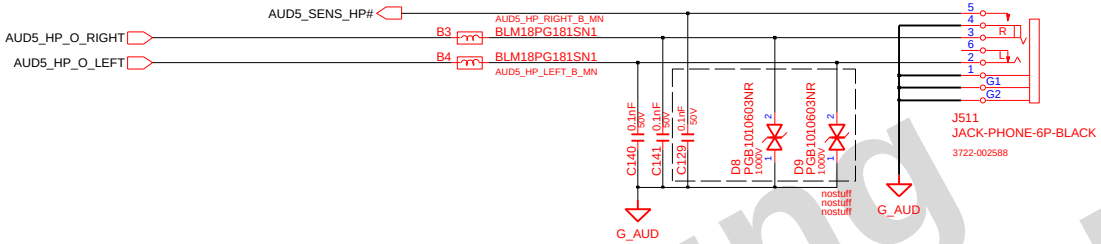
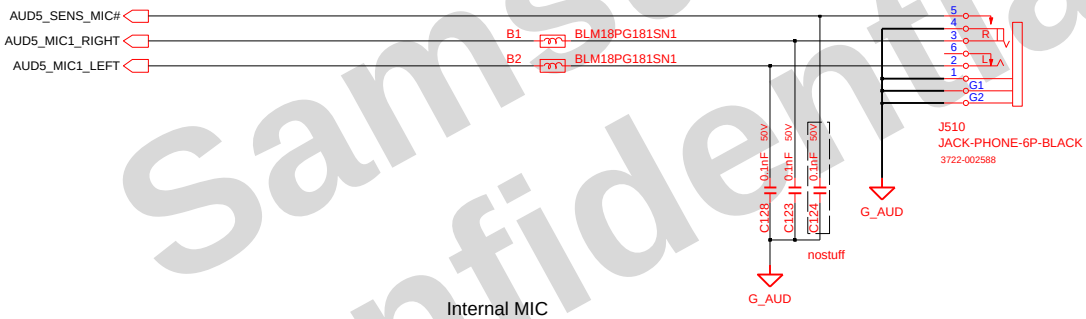
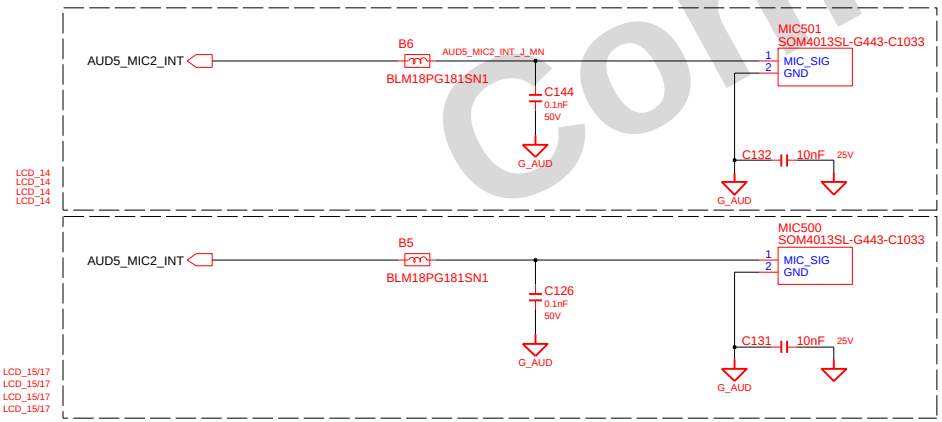
HEADPHONE

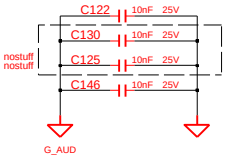


MIC JACK



Internal MIC





DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L HDA_CODEC & LED SUB AUDIO JACK & LED SUB	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 32 OF 52	

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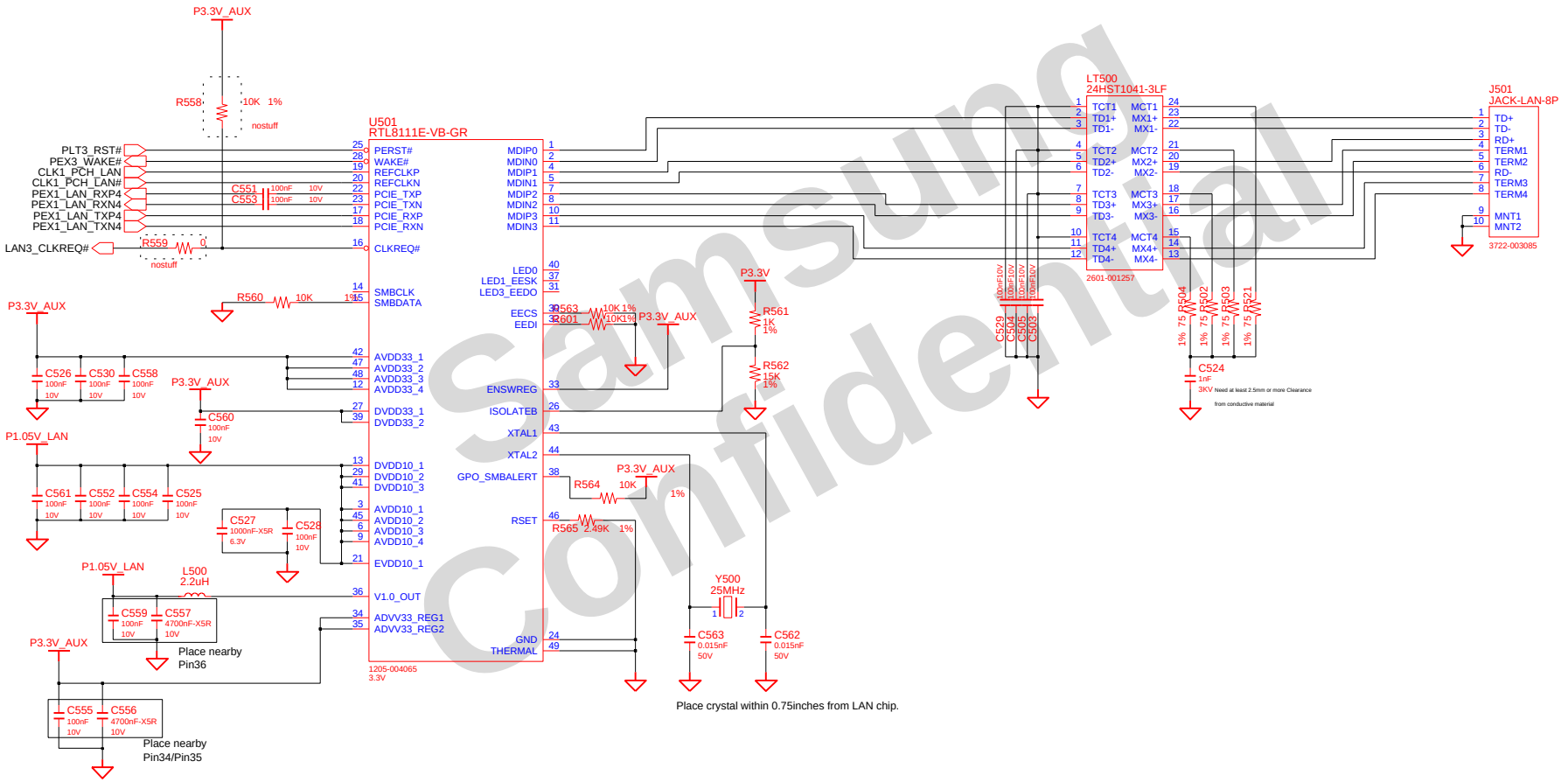
Reatek RTL8111E



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L / LAN / LAN_Realtek_RTL8111	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 33 OF 52	

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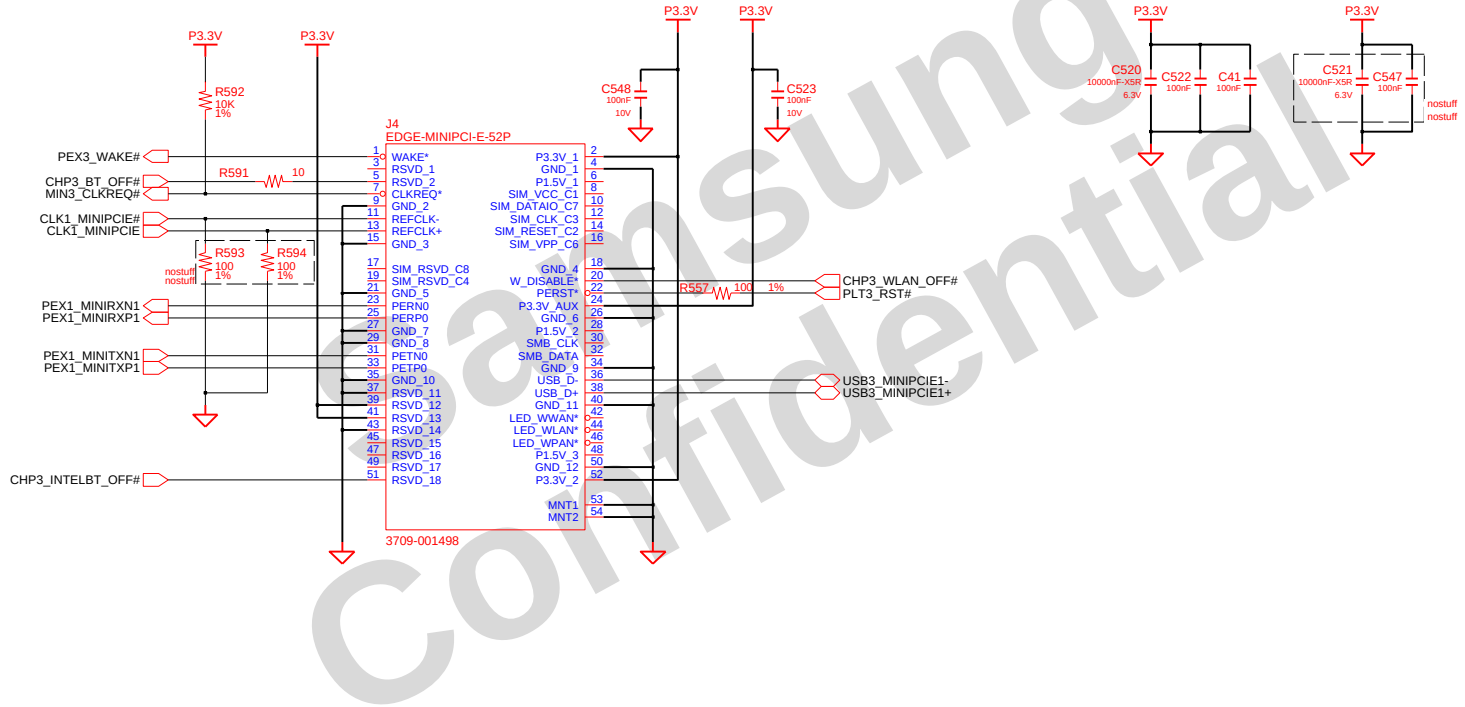
WLAN
Height : 4.0mm



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L WLAN WLAN	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 34 OF 52	

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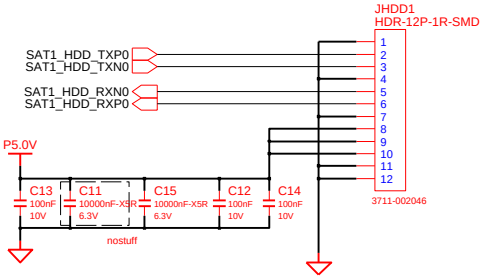
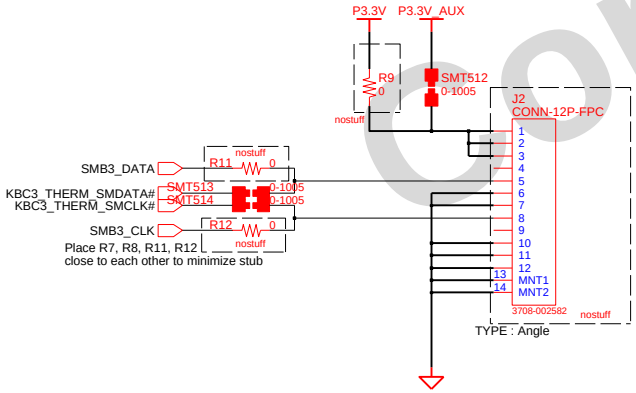
SATA HDD CONN

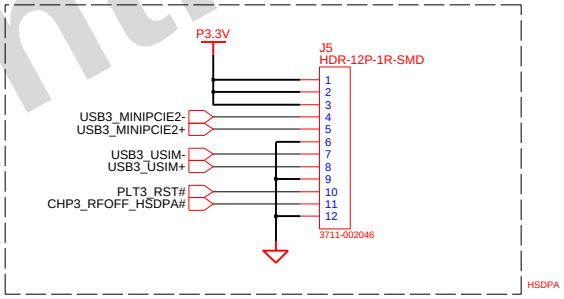
Cable Connector Type



FOR IR



MAIN to HSDPA SUB



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L SATA HDD & IR SATA HDD & IR	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 35 OF 52	

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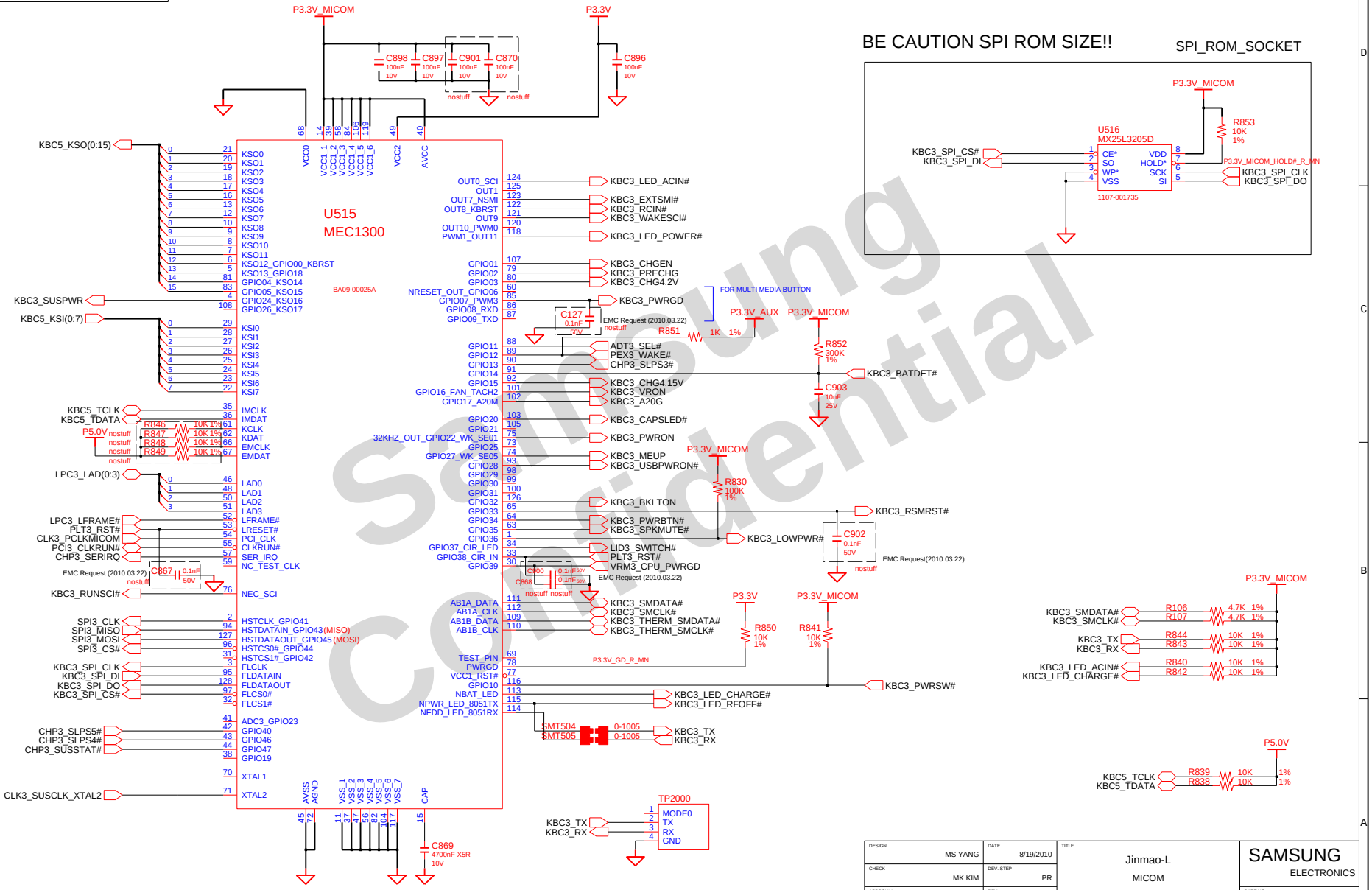
MAIN BOARD (MICOM)



BE CAUTION SPI ROM SIZE!!

SPI_ROM_SOCKET

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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L MICOM SMSC MEC1300	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 36 OF 52	

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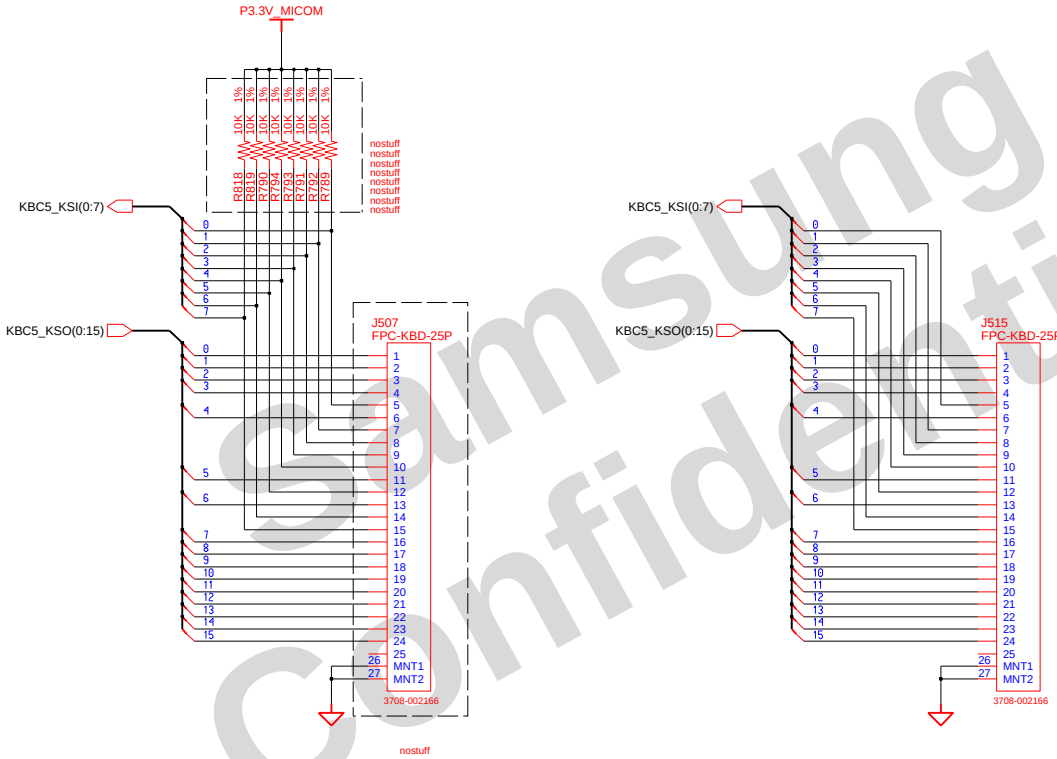
Micom Glue Logic

KEYBOARD



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR	MICOM GLUE LOGIC	
APPROVAL: BL LEE	REV: rev. 1.0	MICOM GLUE LOGIC	PART NO.: BA41-01432A
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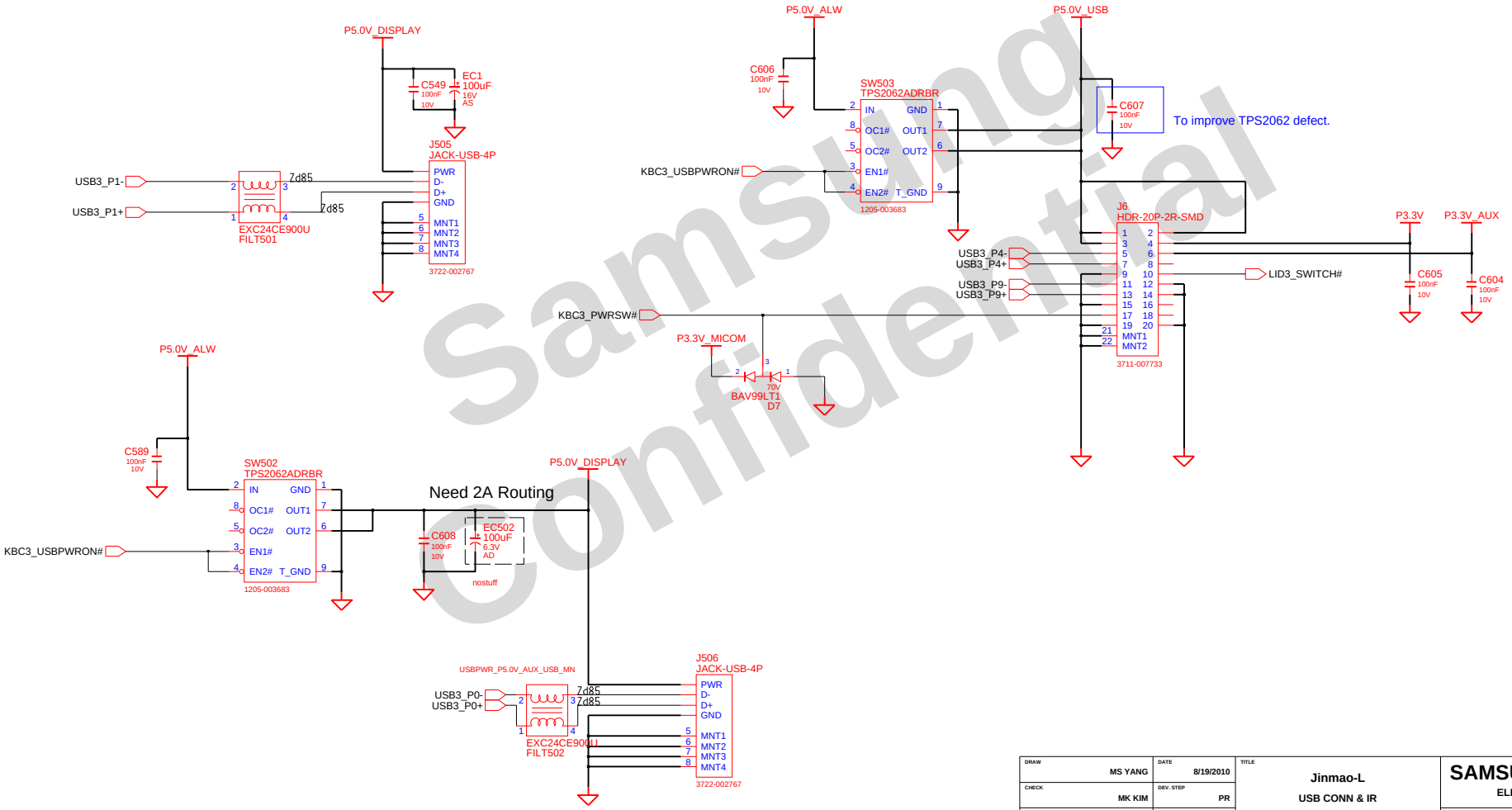
POWER S/W SUB B'D CONNECTOR

MAIN to SUB



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L USB CONN & IR USB & IR	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 38 OF 52	

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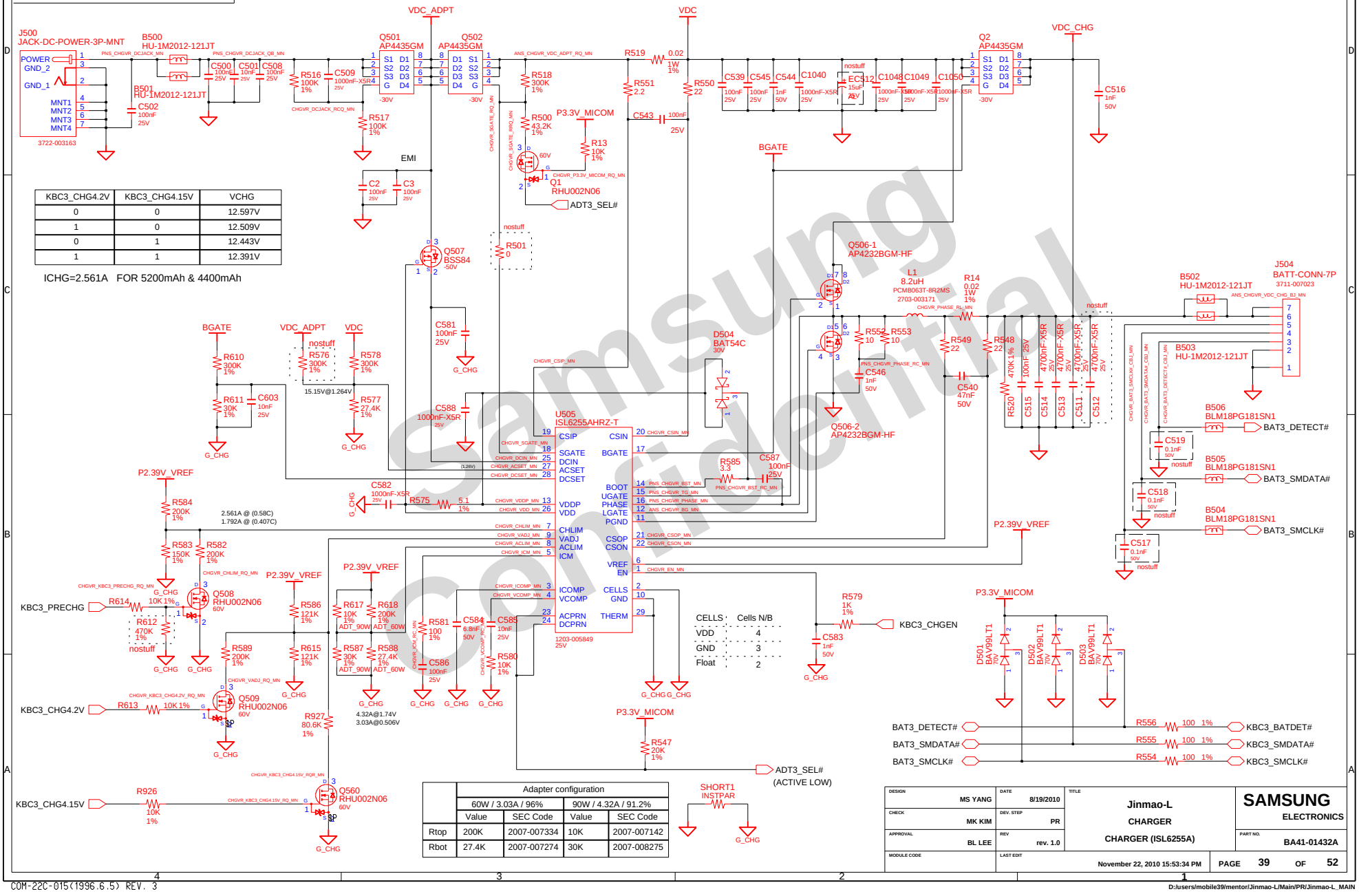
CHARGER & POWER MANAGEMENT



KBC3_CHG4.2V	KBC3_CHG4.15V	VCHG
0	0	12.597V
1	0	12.509V
0	1	12.443V
1	1	12.391V

ICHG=2.561A FOR 5200mAh & 4400mAh

CELLS	Cells N/B
VDD	4
GND	3
Float	2

	Adapter configuration			
	60W / 3.03A / 96%		90W / 4.32A / 91.2%	
	Value	SEC Code	Value	SEC Code
Rtop	200K	2007-007334	10K	2007-007142
Rbot	27.4K	2007-007274	30K	2007-008275

DESIGN	MS YANG	DATE	8/19/2010
CHECK	MK KIM	DEV. STEP	PR
APPROVAL	BL LEE	REV	rev. 1.0
MODULE CODE		LAST EDIT	November 22, 2010 15:53:34 PM

TITLE: Jinmao-L CHARGER CHARGER (ISL6255A)

SAMSUNG ELECTRONICS

PART NO. BA41-01432A

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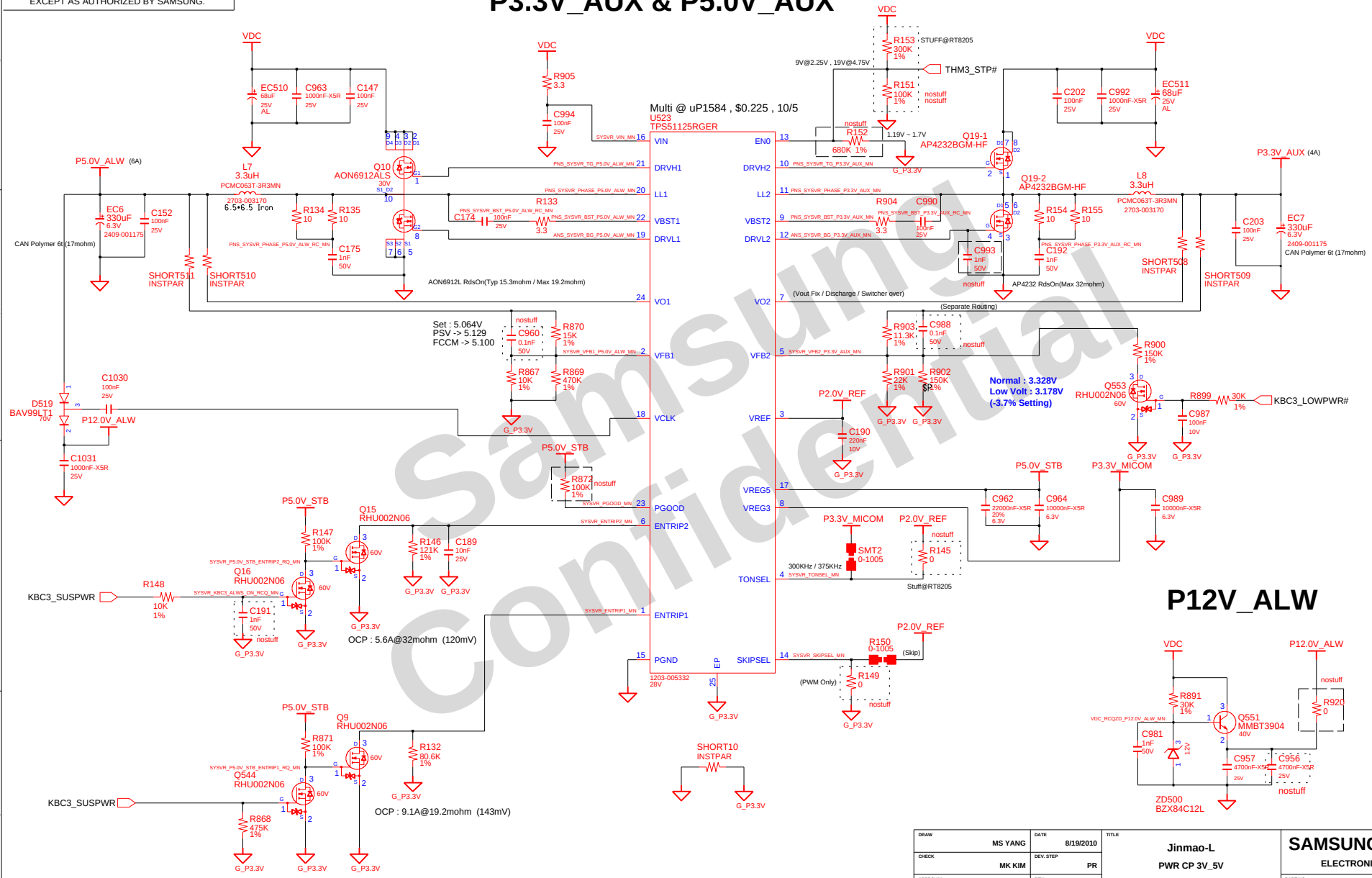
P3.3V_AUX & P5.0V_AUX



P12V_ALW

DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PWR CP 3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 40 OF 52	

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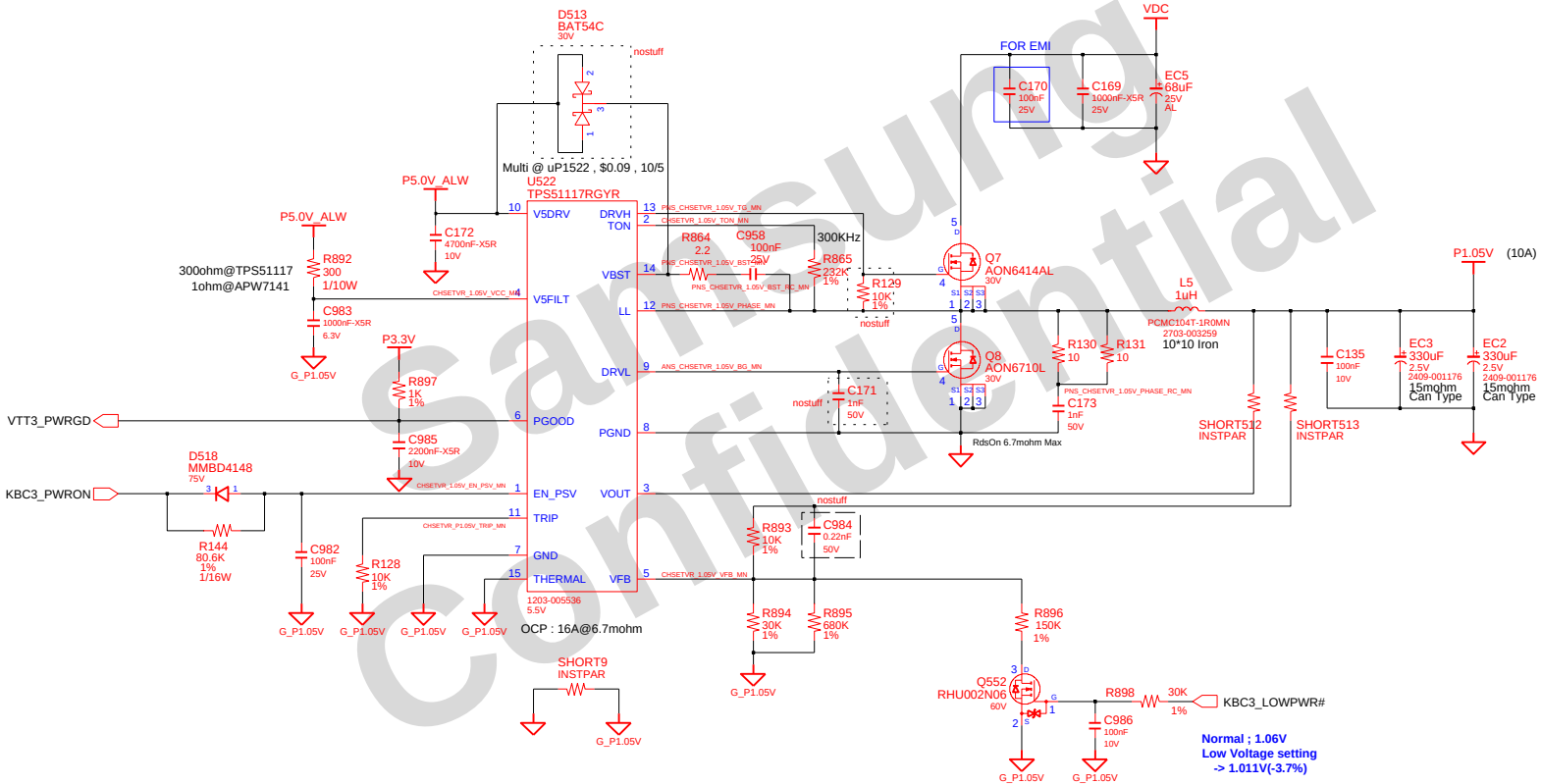
CHIPSET POWER(P1.05V)



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L / P1.05V / TI TPS51117R	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 41 OF 52	

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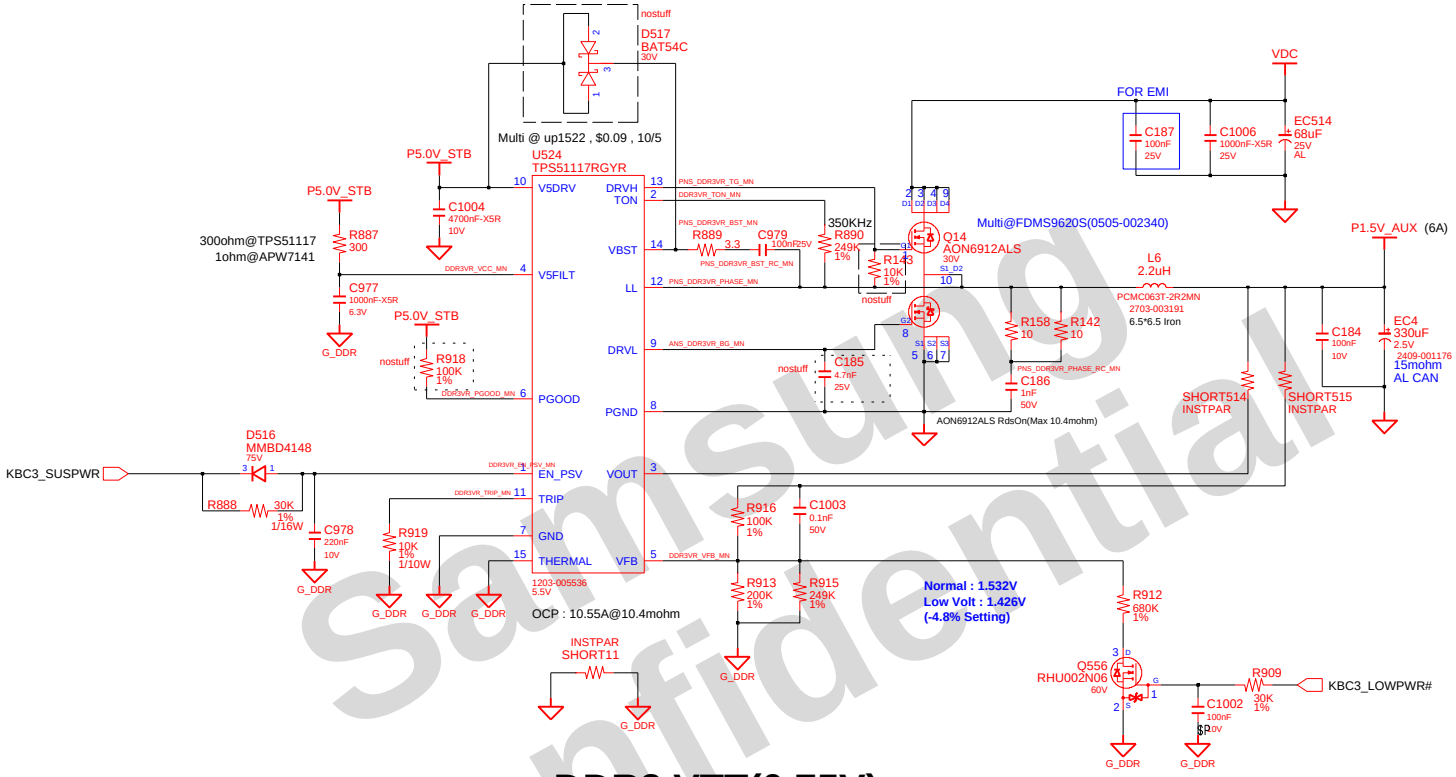
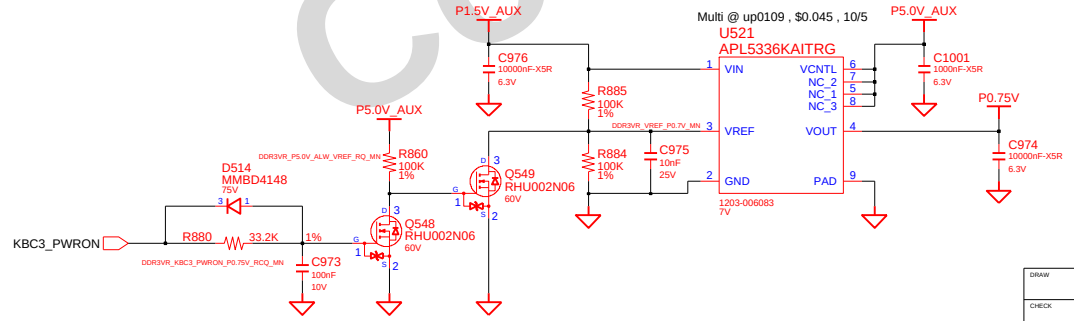
DDR3 Power



DDR3 VTT(0.75V)



DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PWR MEMORY RT8207	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 42 OF 52	

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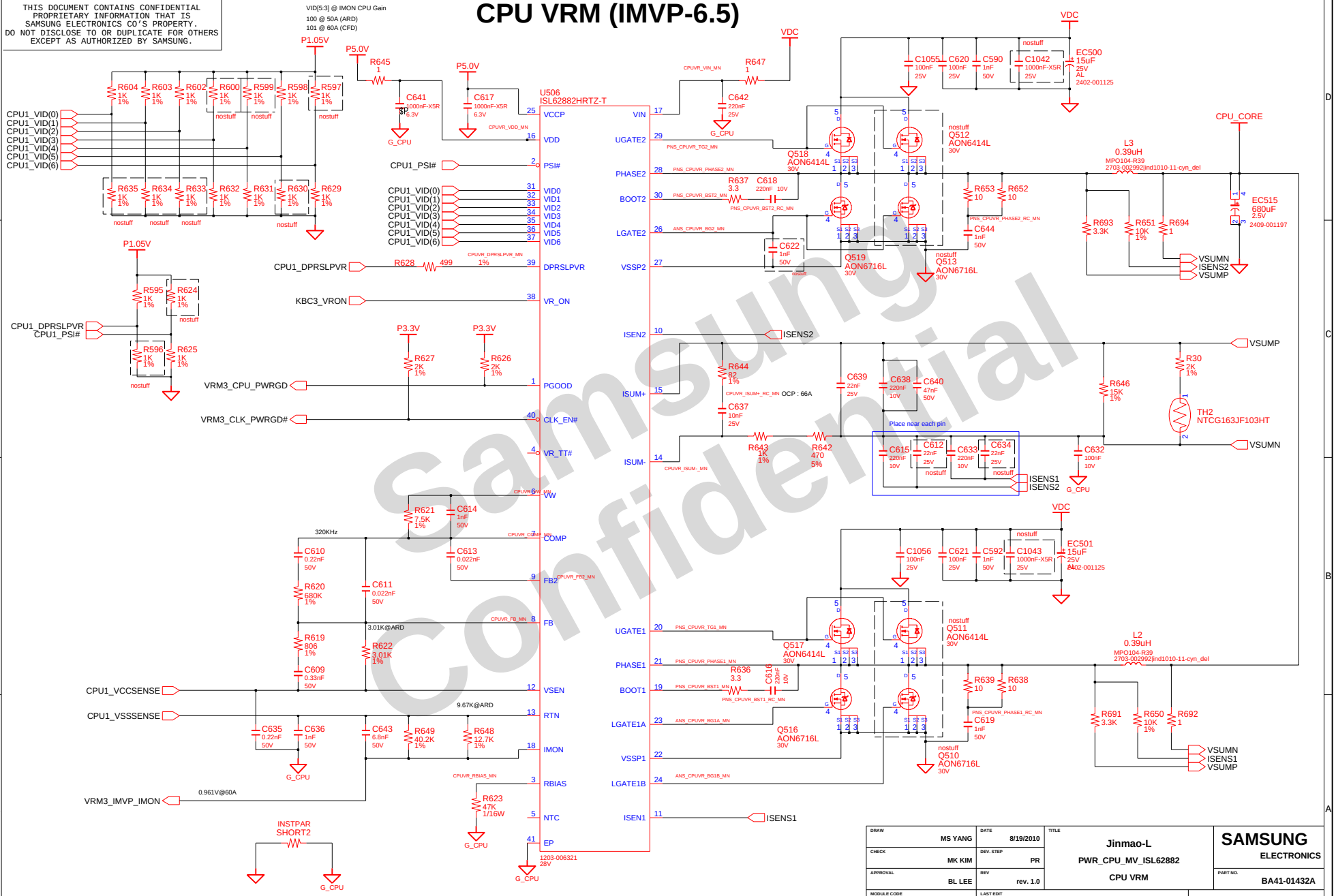
CPU VRM (IMVP-6.5)



DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PWR_CPU_MV_ISL62882 CPU VRM	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 43 OF 52	

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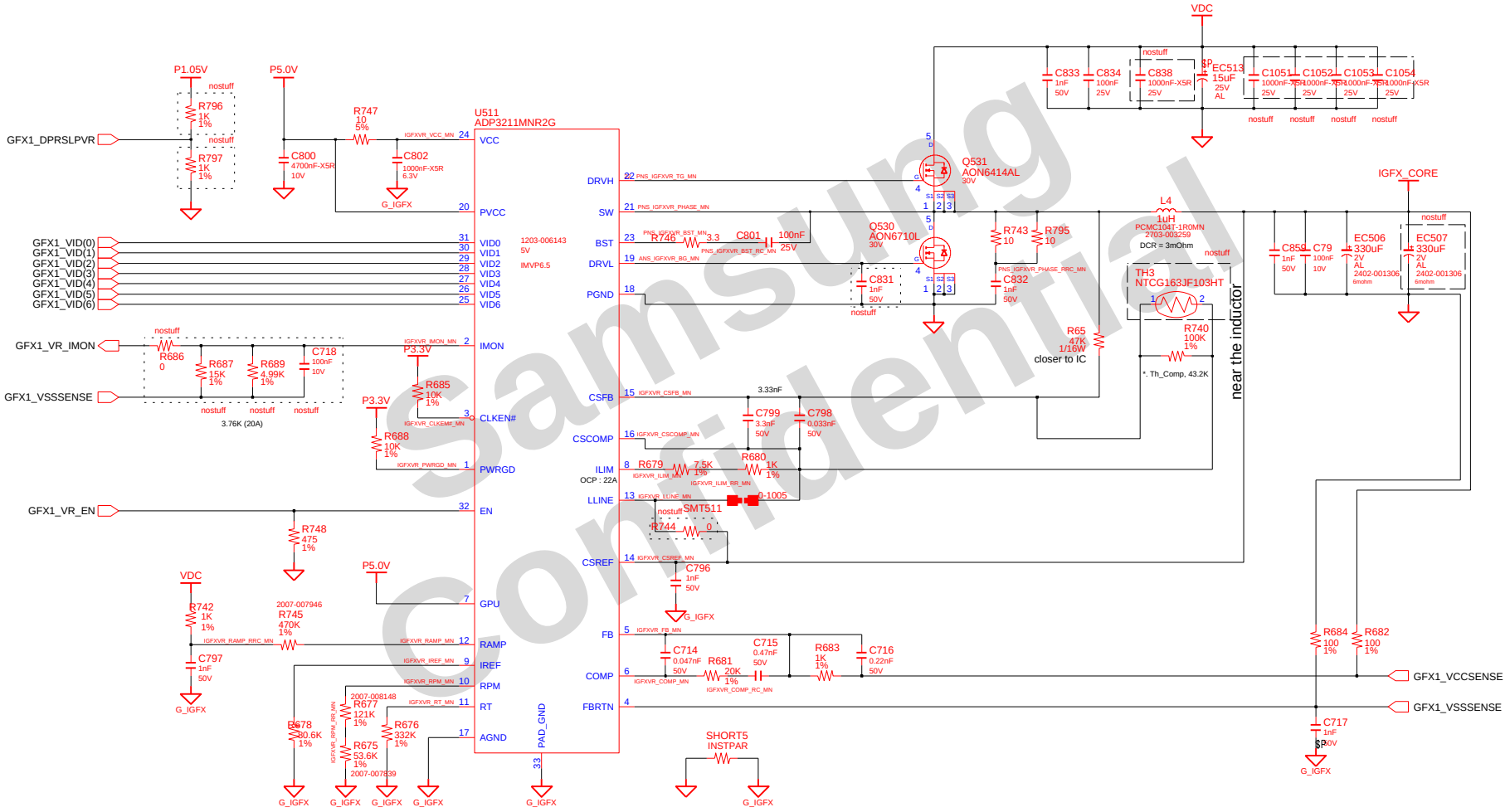
Internal GFX Core Power



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PWR_GFX_INT_ Internal Graphic Power	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 44 OF 52	

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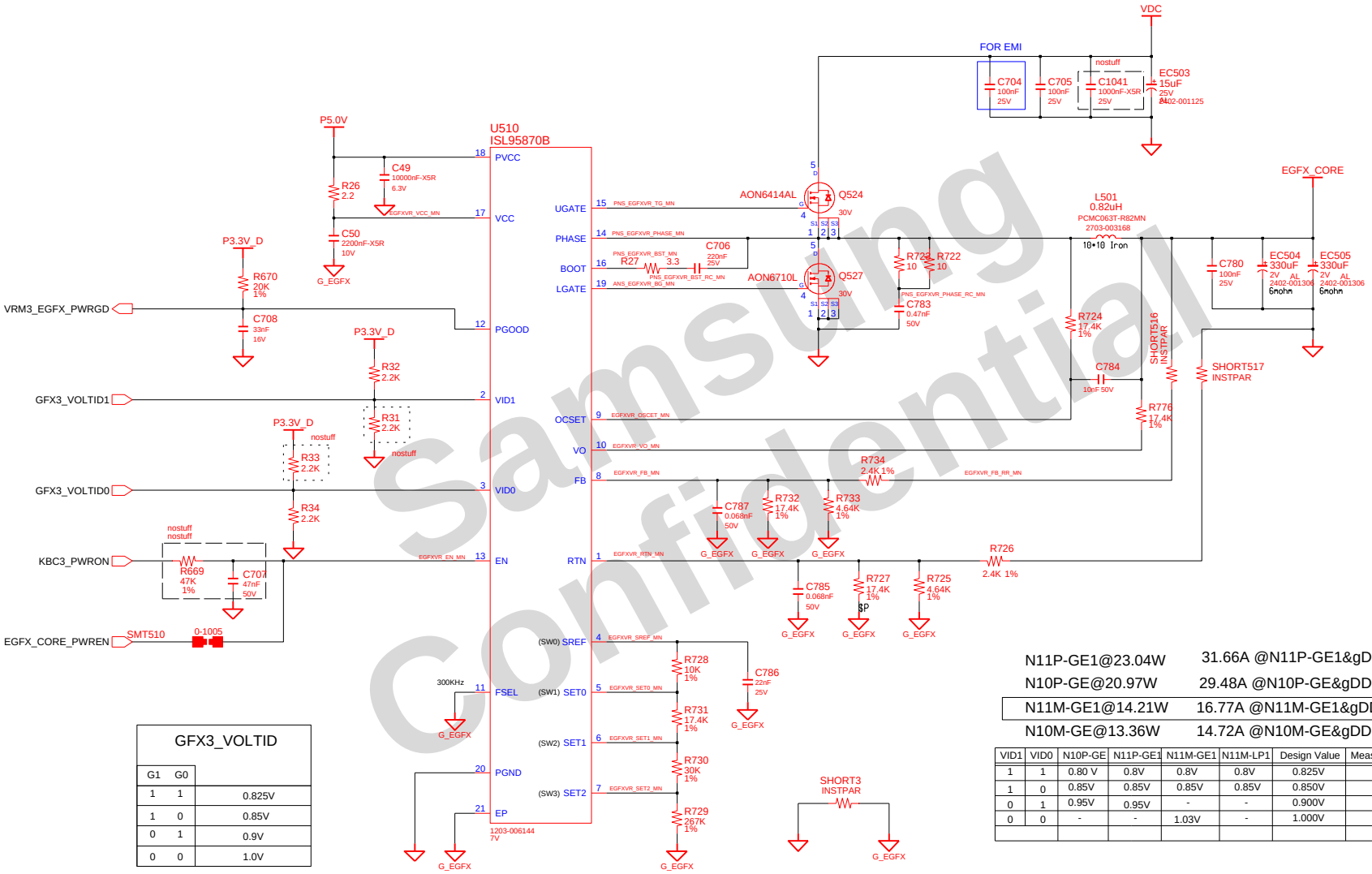
External GFX Core Power



GFX3_VOLTID		
G1	G0	
1	1	0.825V
1	0	0.85V
0	1	0.9V
0	0	1.0V

N11P-GE1@23.04W	31.66A @N11P-GE1&gDDR3
N10P-GE@20.97W	29.48A @N10P-GE&gDDR3
N11M-GE1@14.21W	16.77A @N11M-GE1&gDDR3
N10M-GE@13.36W	14.72A @N10M-GE&gDDR3

VID1	VID0	N10P-GE	N11P-GE1	N11M-GE1	N11M-LP1	Design Value	Measured Value
1	1	0.80 V	0.8V	0.8V	0.8V	0.825V	
1	0	0.85V	0.85V	0.85V	0.85V	0.850V	
0	1	0.95V	0.95V	-	-	0.900V	
0	0	-	-	1.03V	-	1.000V	

OPT OPT OPT OPT **OPT**
OPT OPT OPT OPT **OPT**
OPT OPT OPT OPT OPT
OPT OPT OPT OPT OPT OPT
OPT OPT OPT OPT OPT
OPT OPT OPT OPT OPT
OPT OPT OPT OPT OPT
OPT OPT
OPT
OPT

DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR	PWR_GFX_MV_EXT	
APPROVAL: BL LEE	REV: rev. 1.0	External Graphic Power	PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 45 OF 52	

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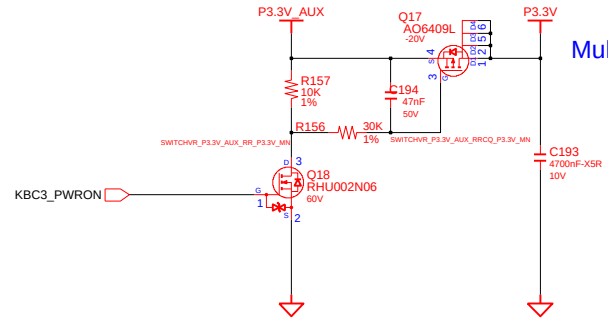
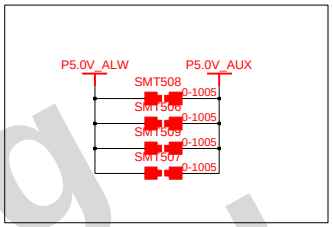
Switched Power

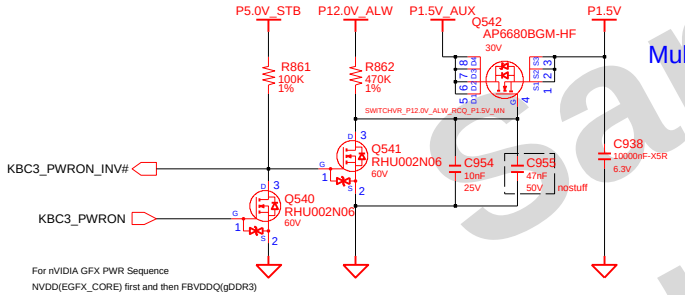
Switched Power On (P3.3V)



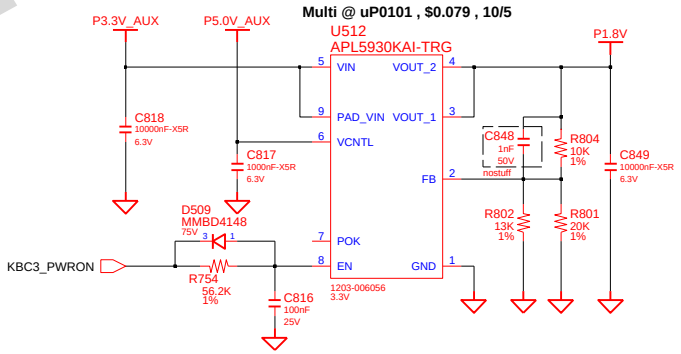
P5.0V_AUX



Switched Power On (P1.5V)

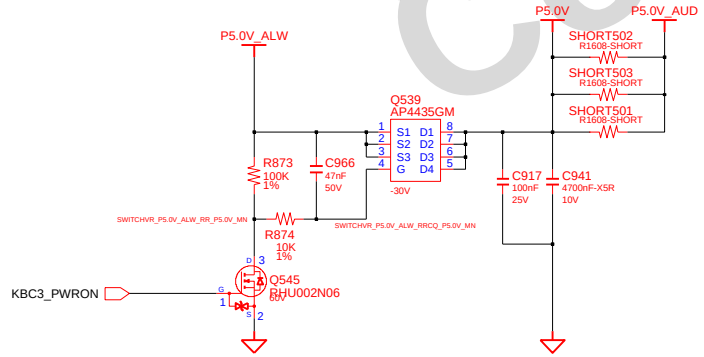


P1.8V(LDO)



Switched Power On (P5.0V)

Multi@Si4435DDY



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR	PWR_MV_SWITCHED	
APPROVAL: BL LEE	REV: rev. 1.0	SWITCHED POWER	PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 46 OF 52	

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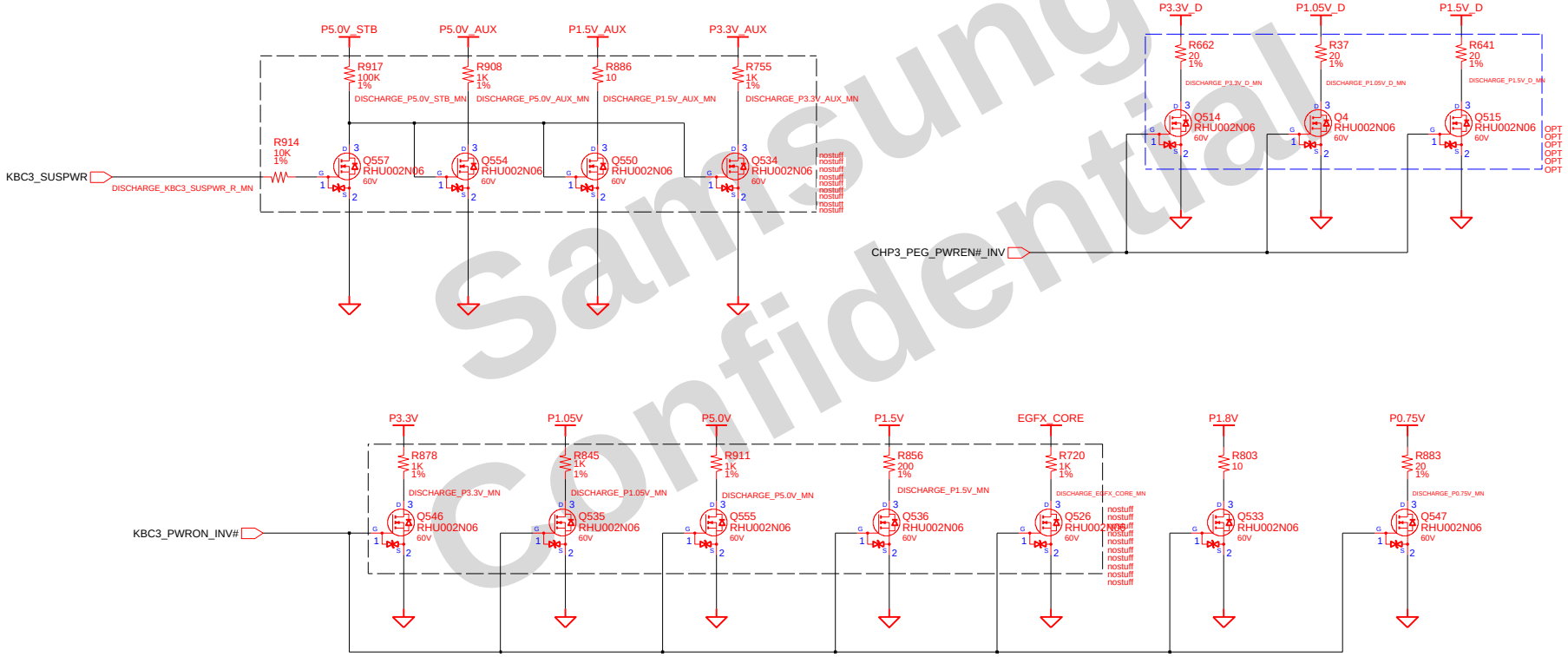
POWER DISCHARGER



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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L PWR_MV_DISCHARGER DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE: undefined	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 47 OF 52	

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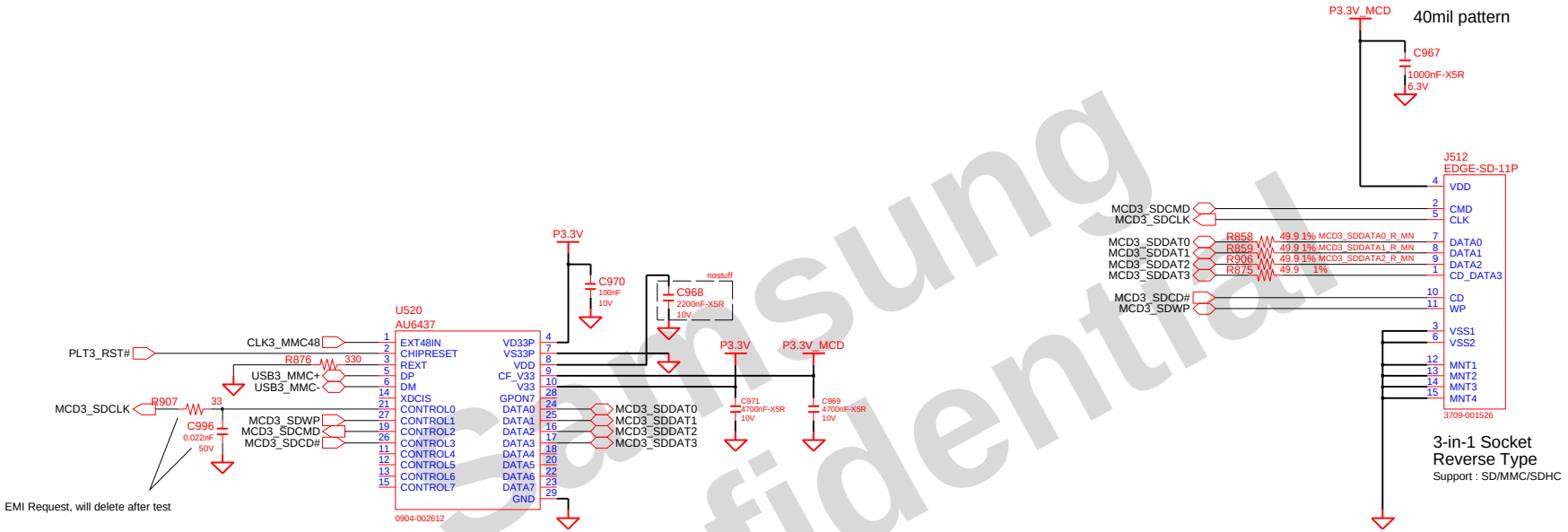
AU6437 (4-in-1)



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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L AU 6437 AU 6437	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 48 OF 52	

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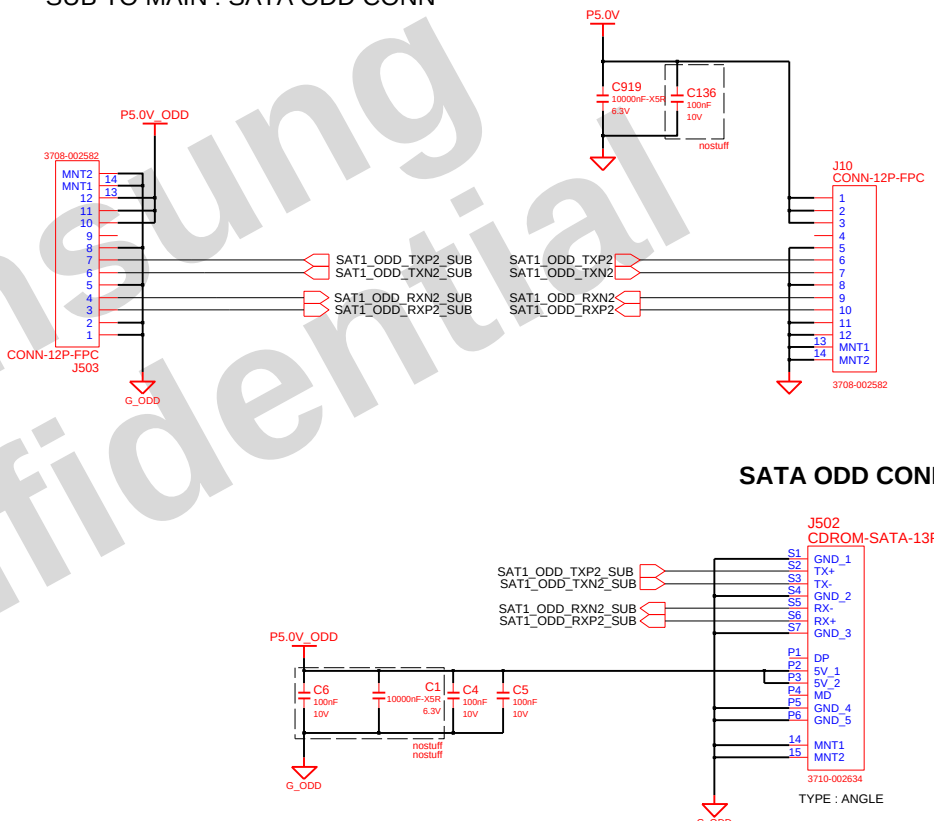
SATA ODD SUB BOARD

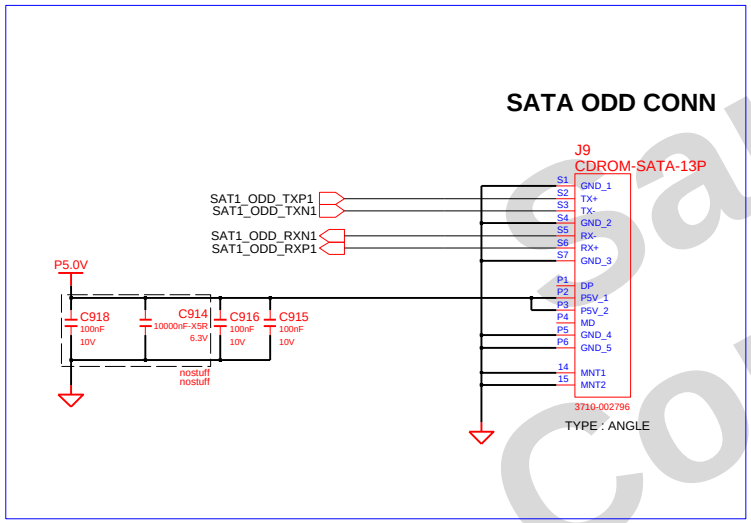
15.6" & 17.3"

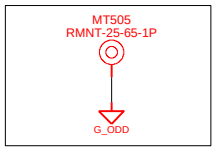
MAIN TO SUB : SATA ODD CONN

SUB TO MAIN : SATA ODD CONN



14"





ODD sub board mount hole

DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L SATA ODD SATA ODD	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 49 OF 52	

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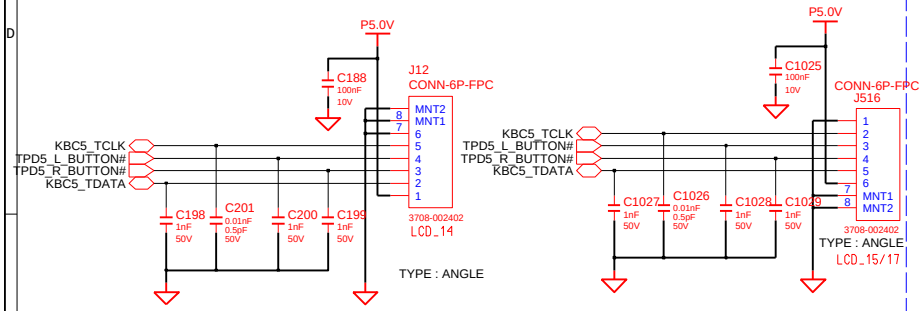
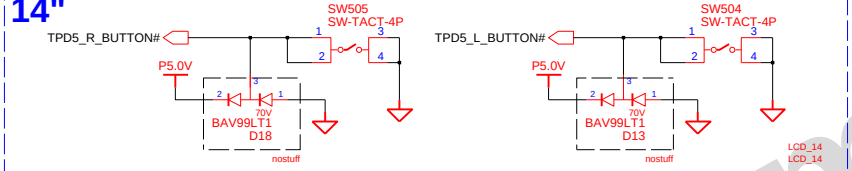
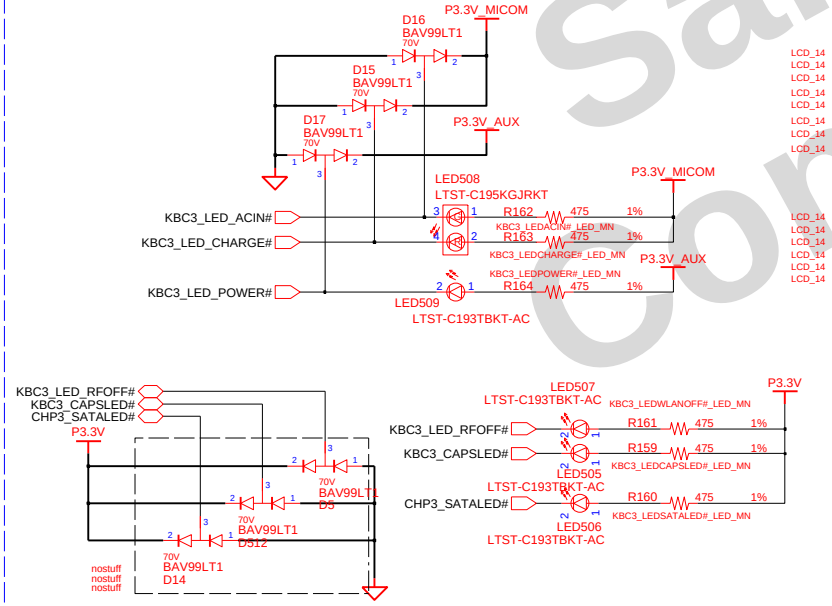
TOUCHPAD



14"

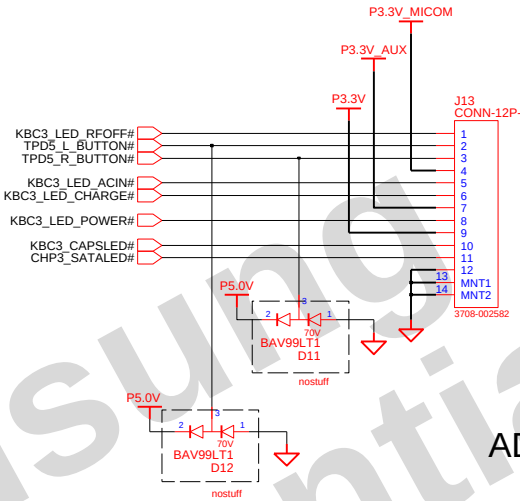


ADAPTERIN/CHARGING LED

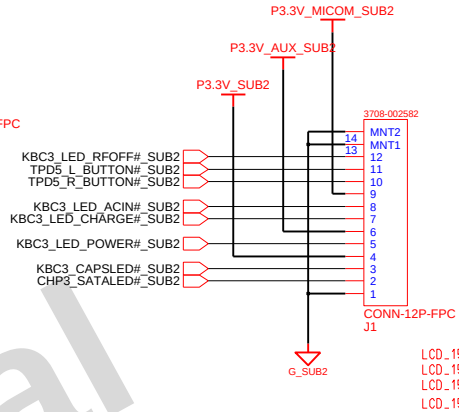


15.6" & 17.3"

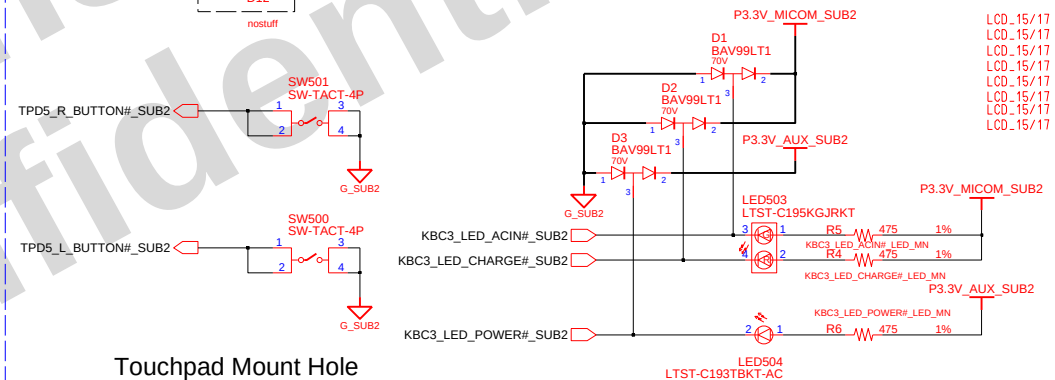
TOUCHPAD MAIN TO SUB



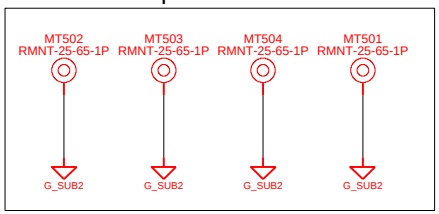
TOUCHPAD SUB TO MAIN

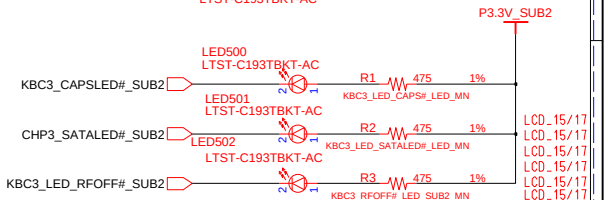


ADAPTERIN/CHARGING LED



Touchpad Mount Hole





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DRAW: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L Touchpad Touchpad	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 50 OF 52	

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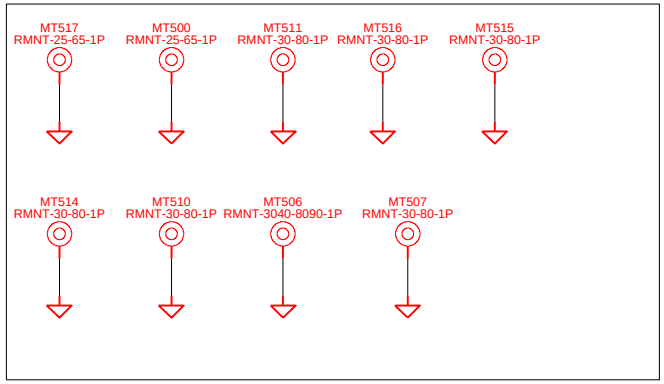
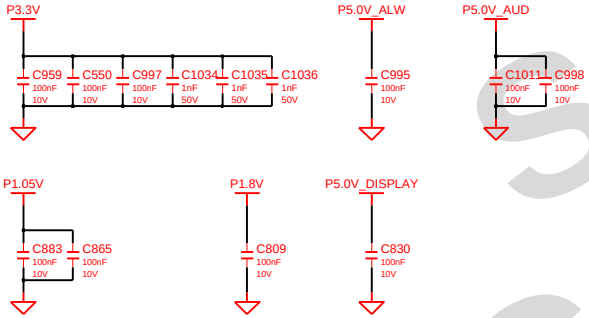
Mainboard Mount ((25-65)X2EA, (30-80)X7EA)





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DESIGN: MS YANG	DATE: 8/19/2010	TITLE: Jinmao-L MNT hole MNT hole	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		
APPROVAL: BL LEE	REV: rev. 1.0		PART NO.: BA41-01432A
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 51 OF 52	

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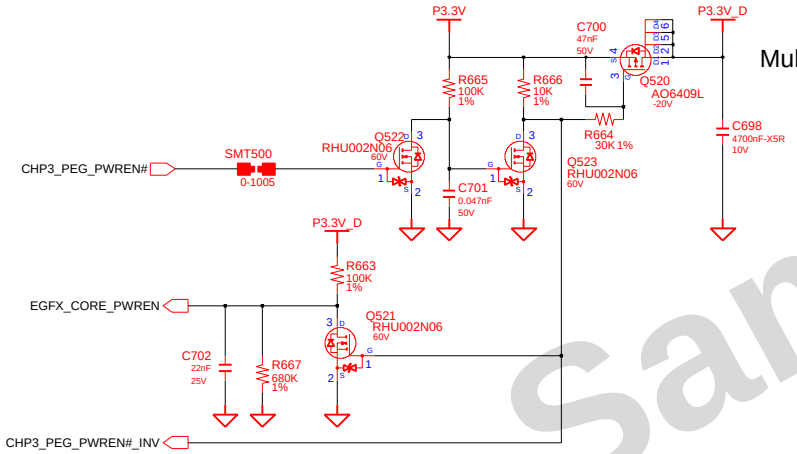
Switched Power 2 (For nVidia GFX Power Sequence)

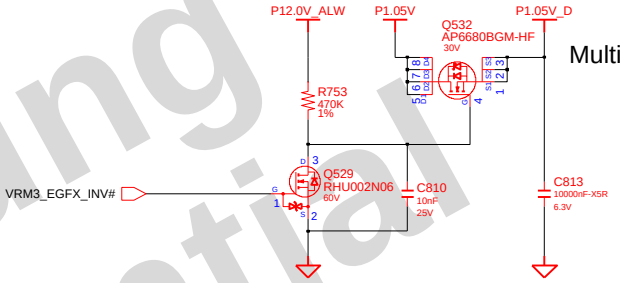
Sequence (D3.3V -> GFX Core -> D1.8V -> D1.5V -> D1.05V)

Discrete Switched Power (D3.3V : Max_1.2A)



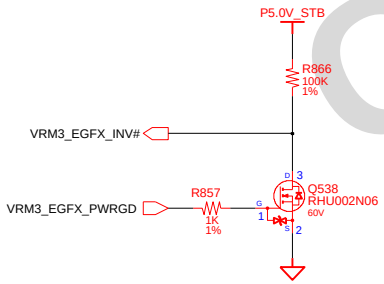
Multi@AP2607GY

Discrete Switched Power (D1.05V : Max 3.6A)

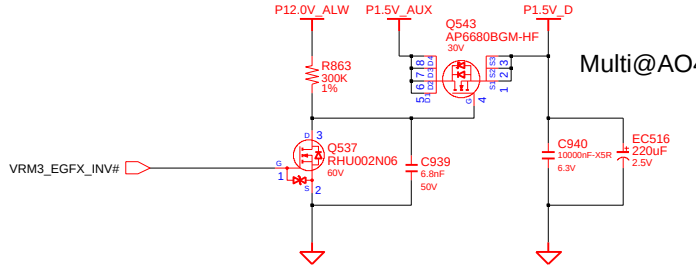


Multi@AO4476L

Discrete Switched Power (D1.8V : Max 0.5A)



Discrete Switched Power (D1.5V : Max 5.0A)



Multi@AO4476L

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DRAW: MS YANG	DATE: 5/10/2010	TITLE: Jinmao-L Switched PWR 2 FOR OPTIMUS PWR	SAMSUNG ELECTRONICS
CHECK: MK KIM	DEV. STEP: PR		PART NO.: BA41-01432A
APPROVAL: BL LEE	REV: rev. 1.0		
MODULE CODE:	LAST EDIT: November 22, 2010 15:53:34 PM	PAGE 52 OF 52	

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