

MODEL NAME : *PALB0*
PCB NO : *LA-6801P (DAB000000400)*
BOM P/N : *46198531L01*
46198531L02

Dell/Compal Confidential

Schematic Document

Specter (Huron River)

Sandy Bridge (PGA) + Cougar Point (standard)

DISCRETE VGA N12E-GE-B (optimus)

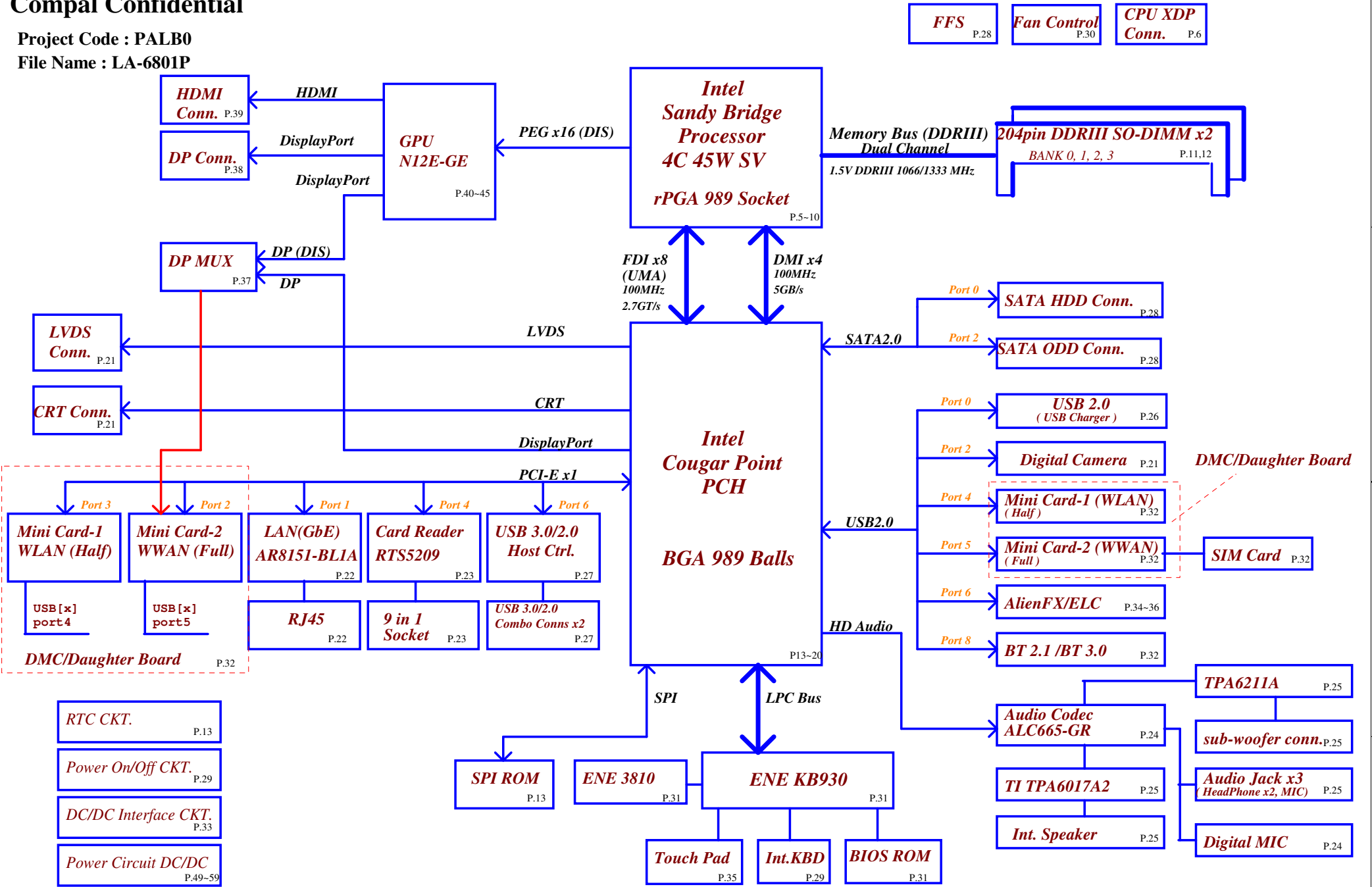
2010-12-06

Rev: 0.3

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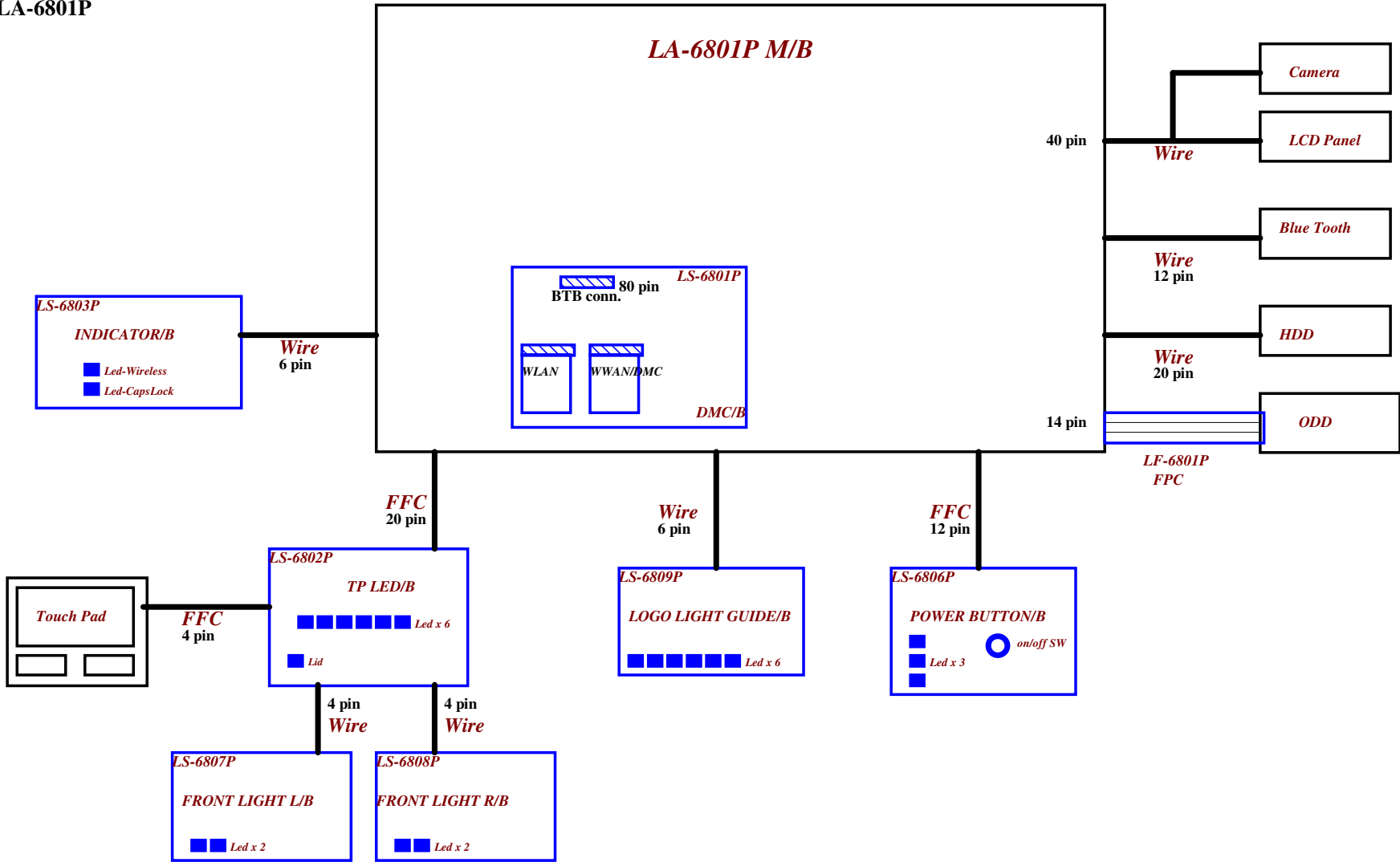
Project Code : PALB0
File Name : LA-6801P



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Project Code : PALB0
File Name : LA-6801P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

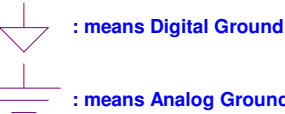
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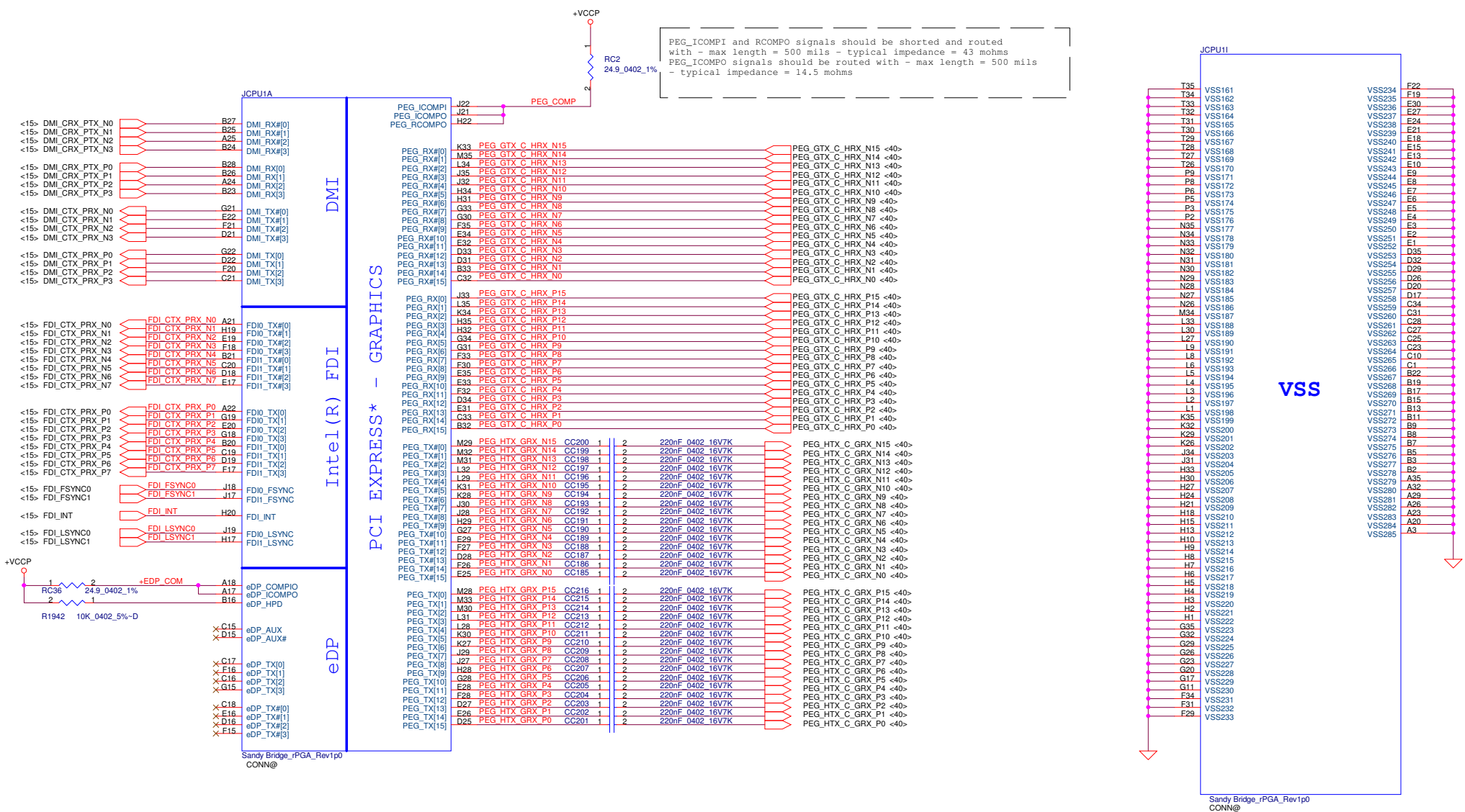
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

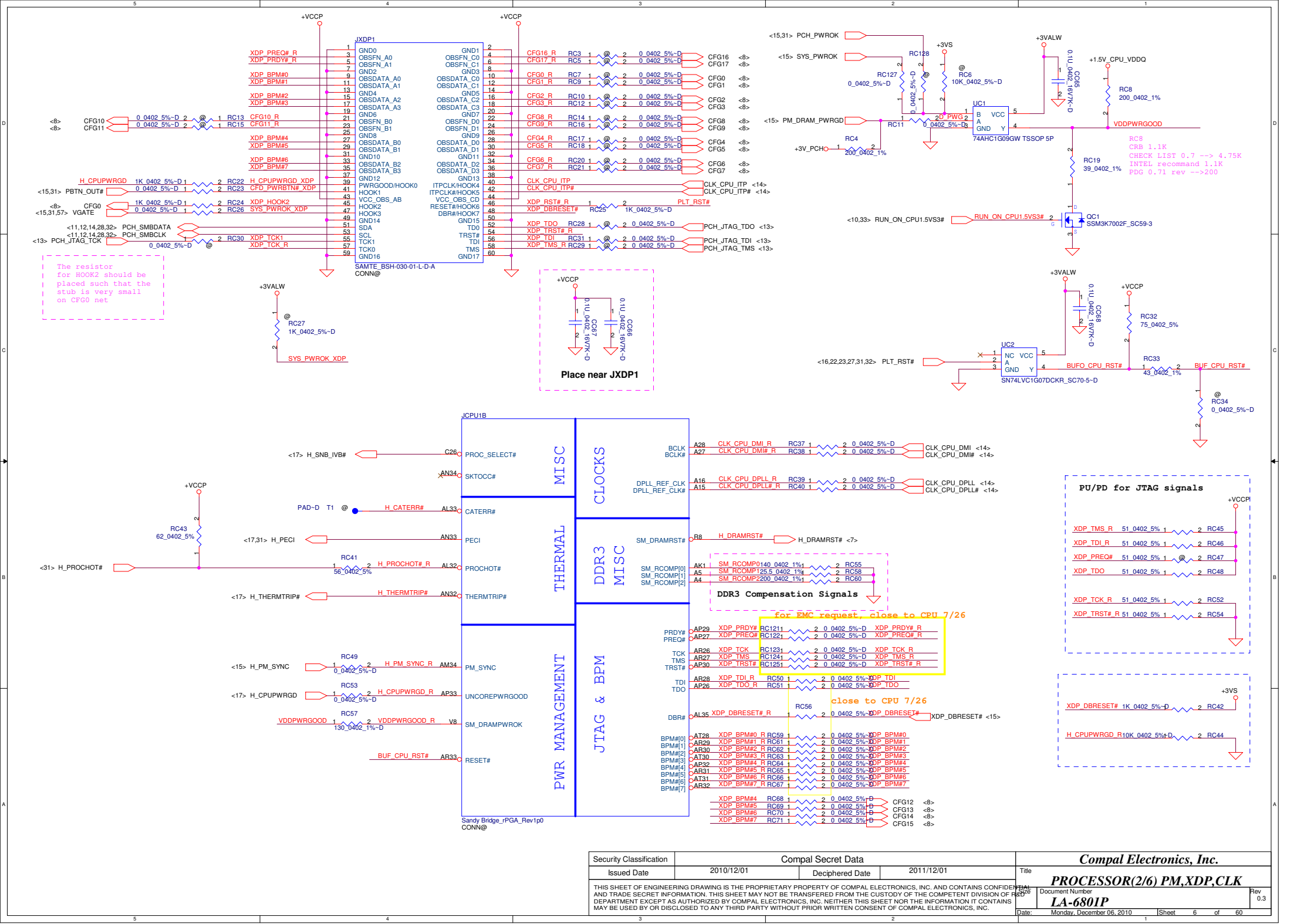
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

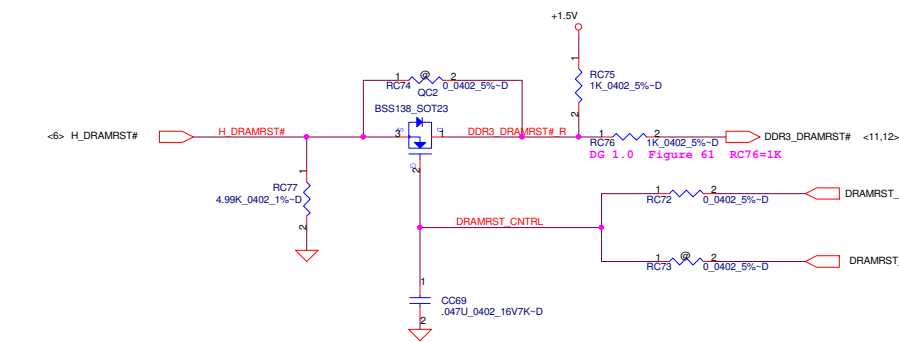
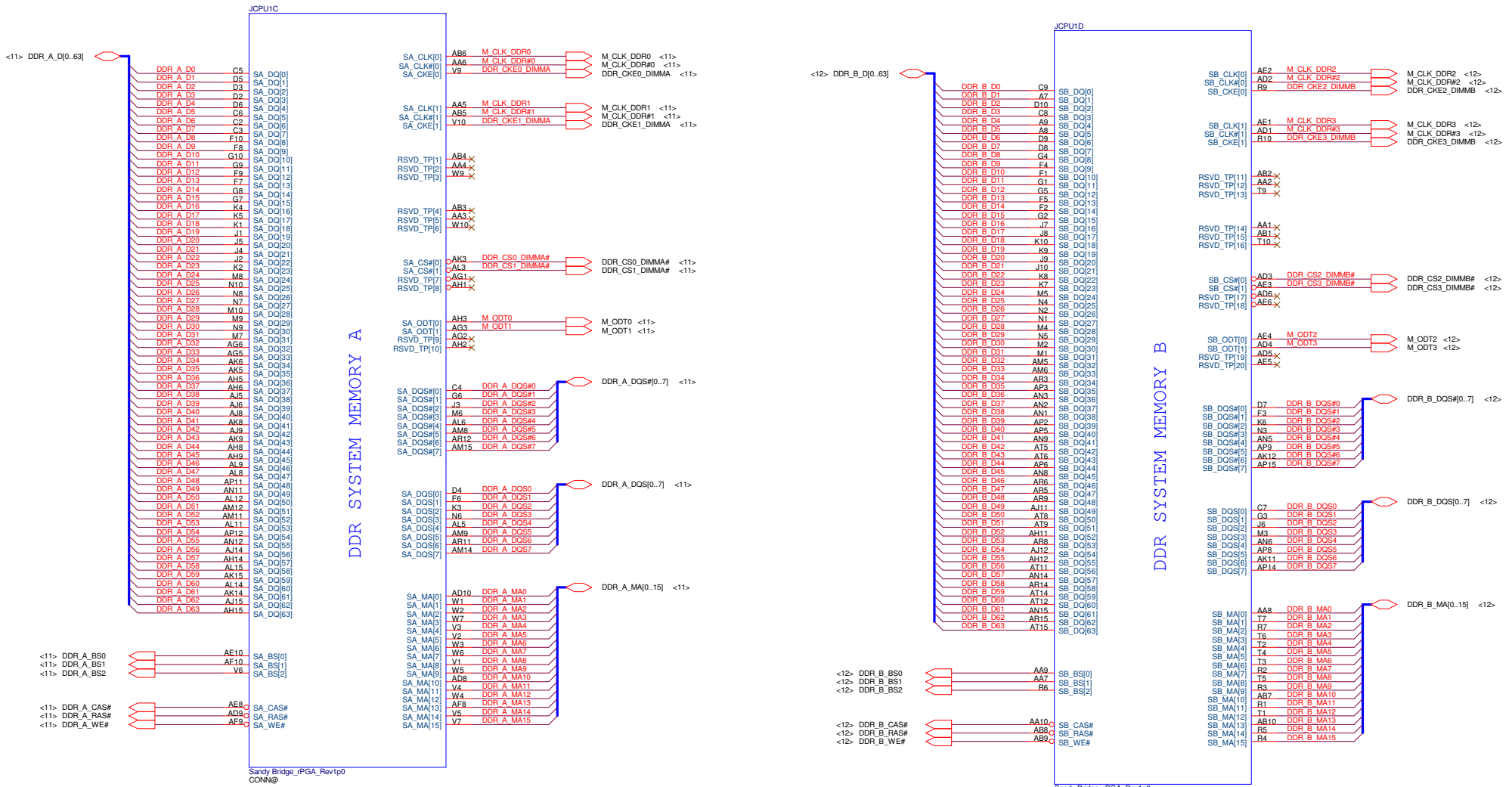
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

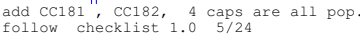
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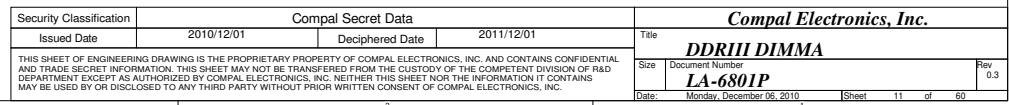
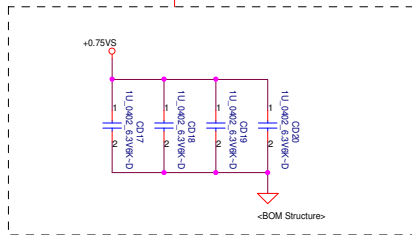
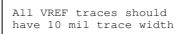


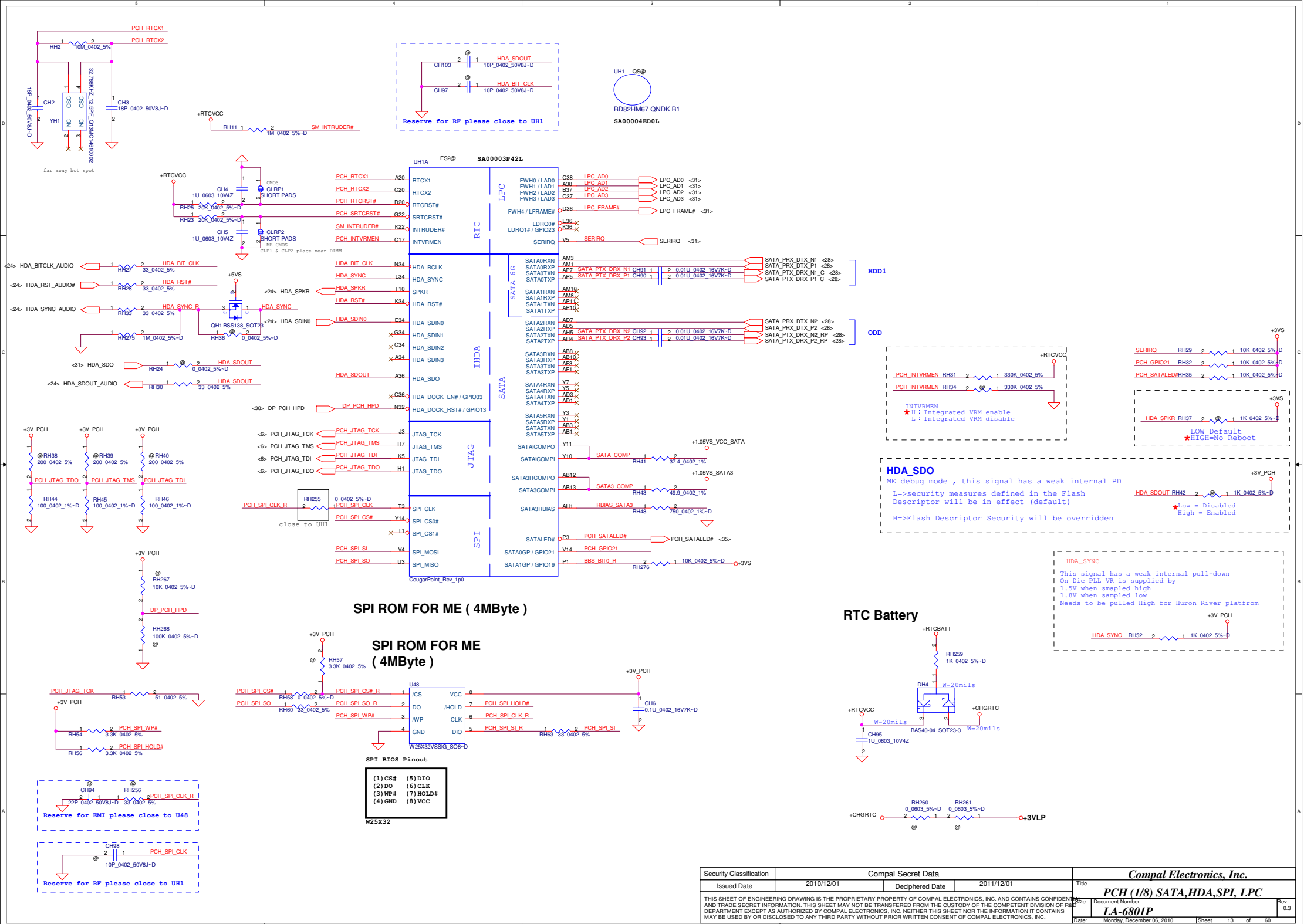




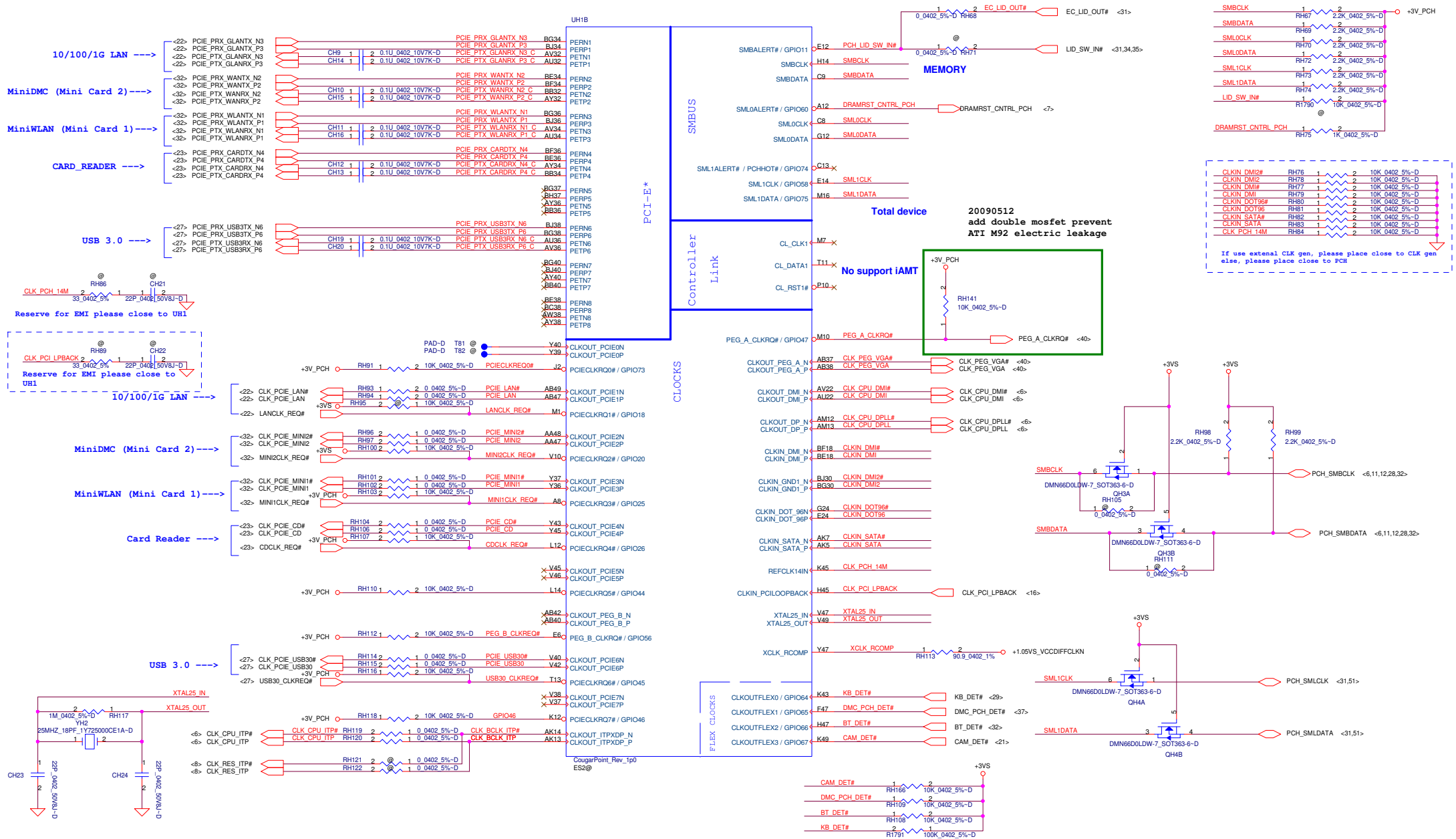




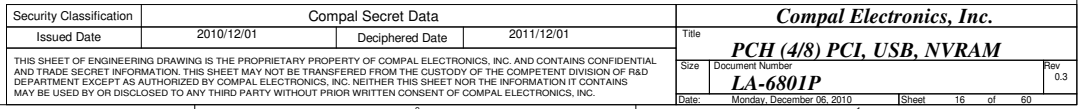


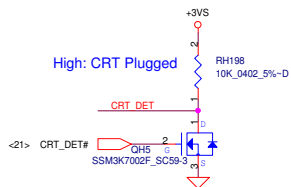
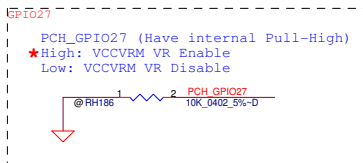
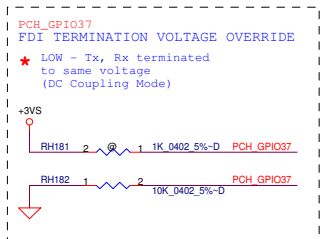
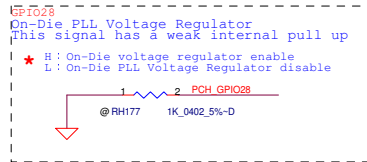


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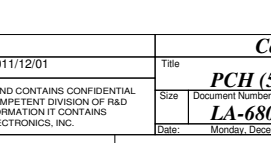
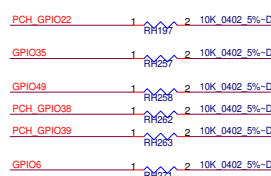
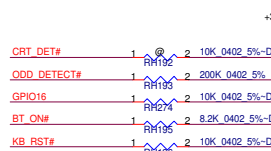
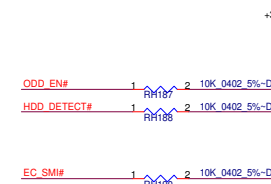
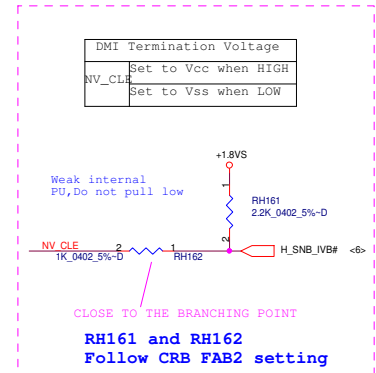
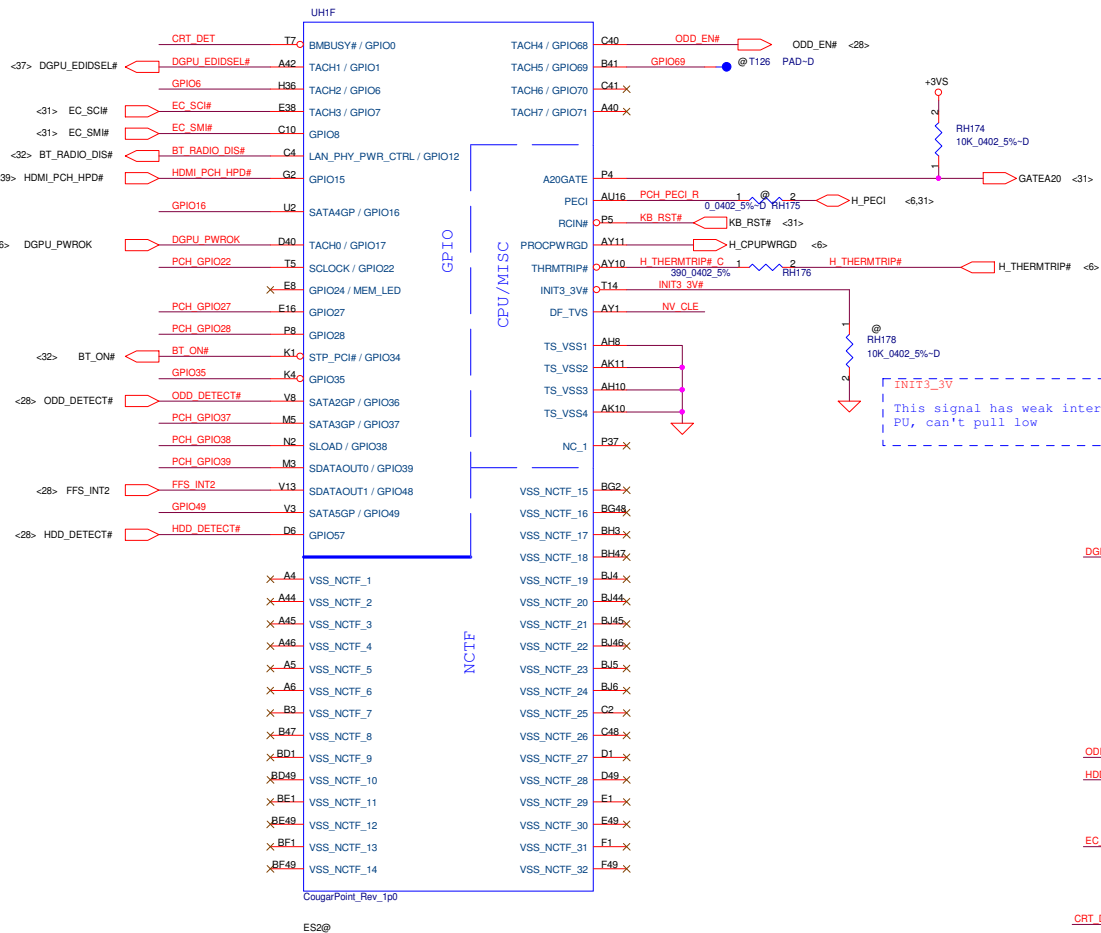
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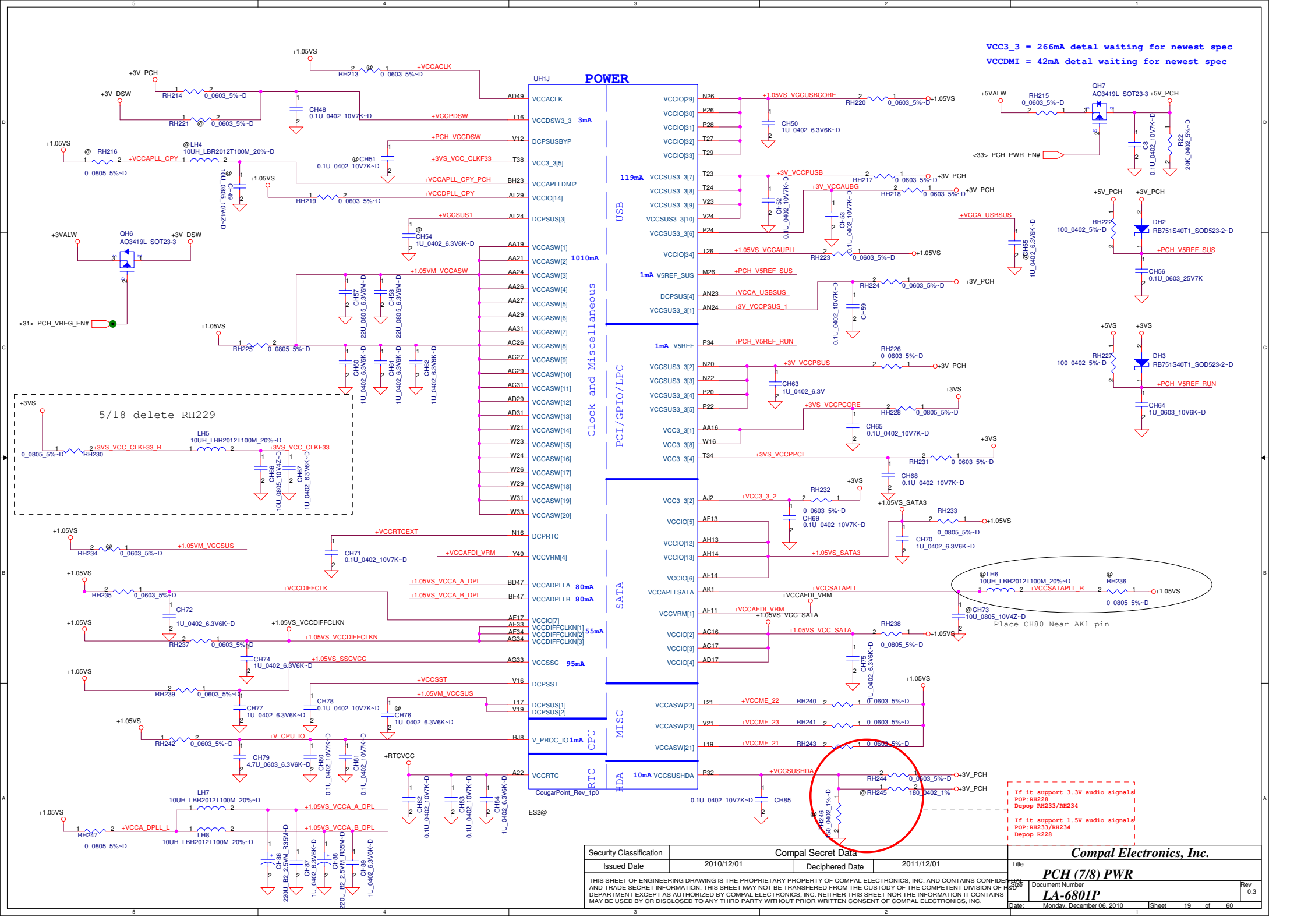


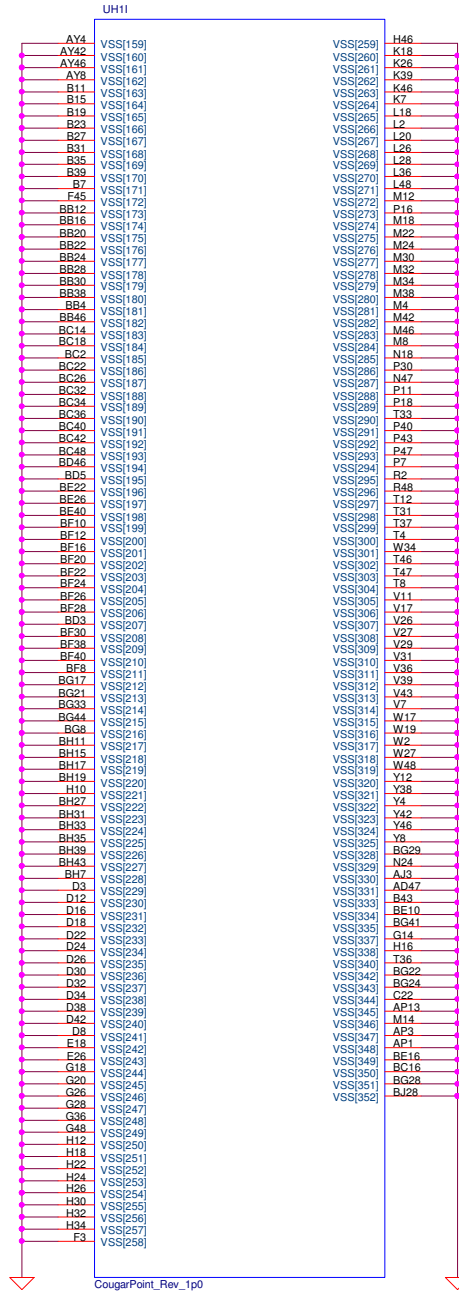
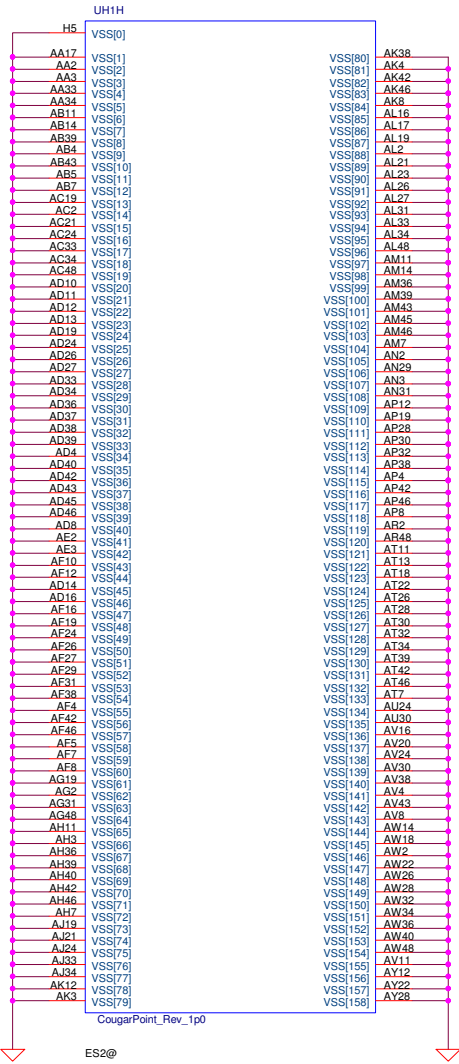
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

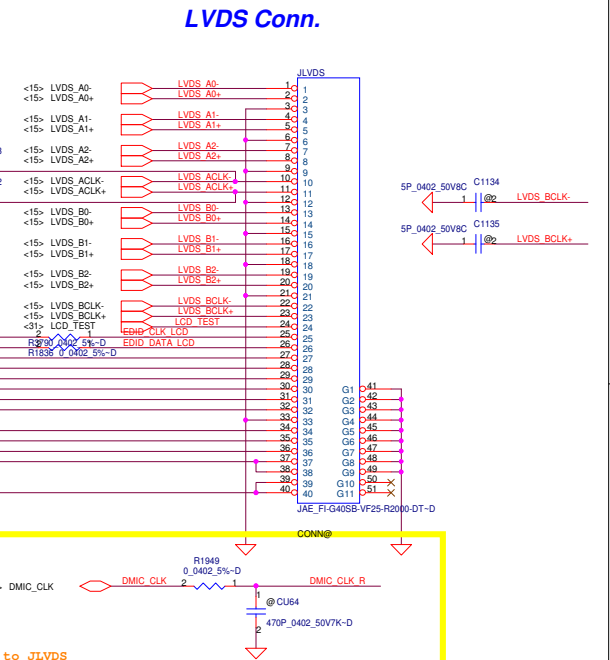
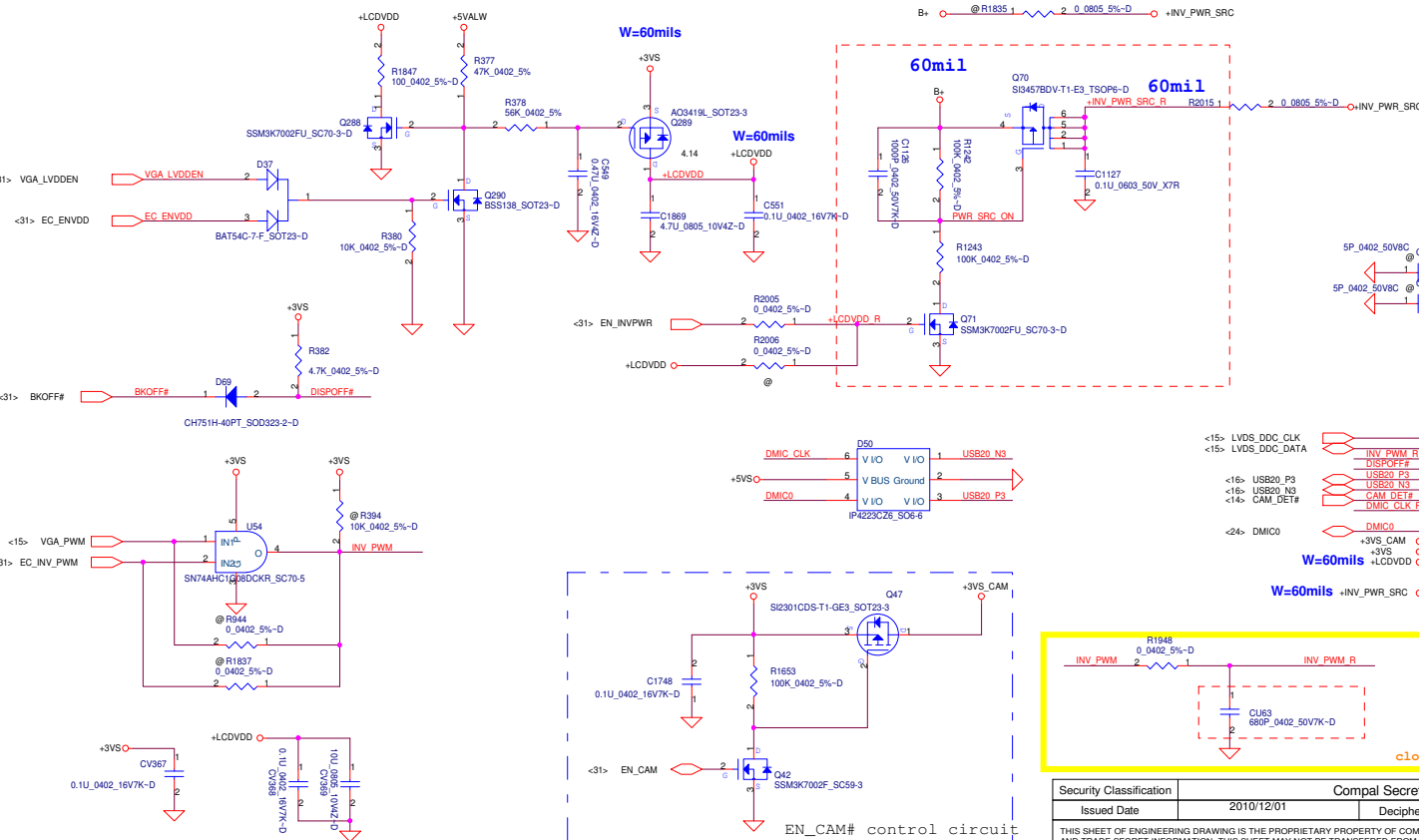
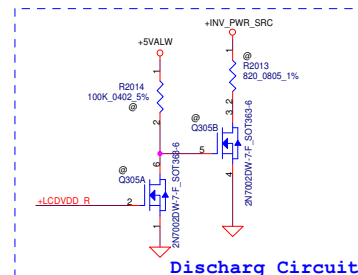
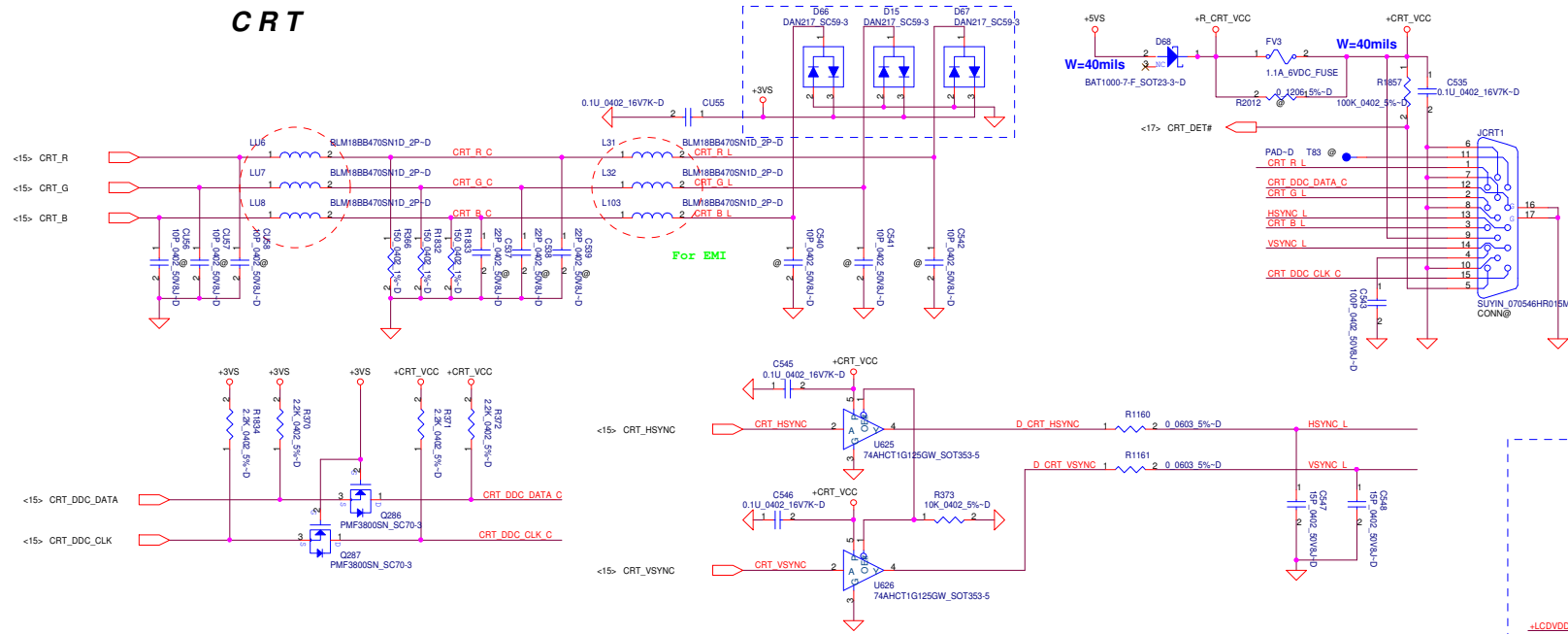


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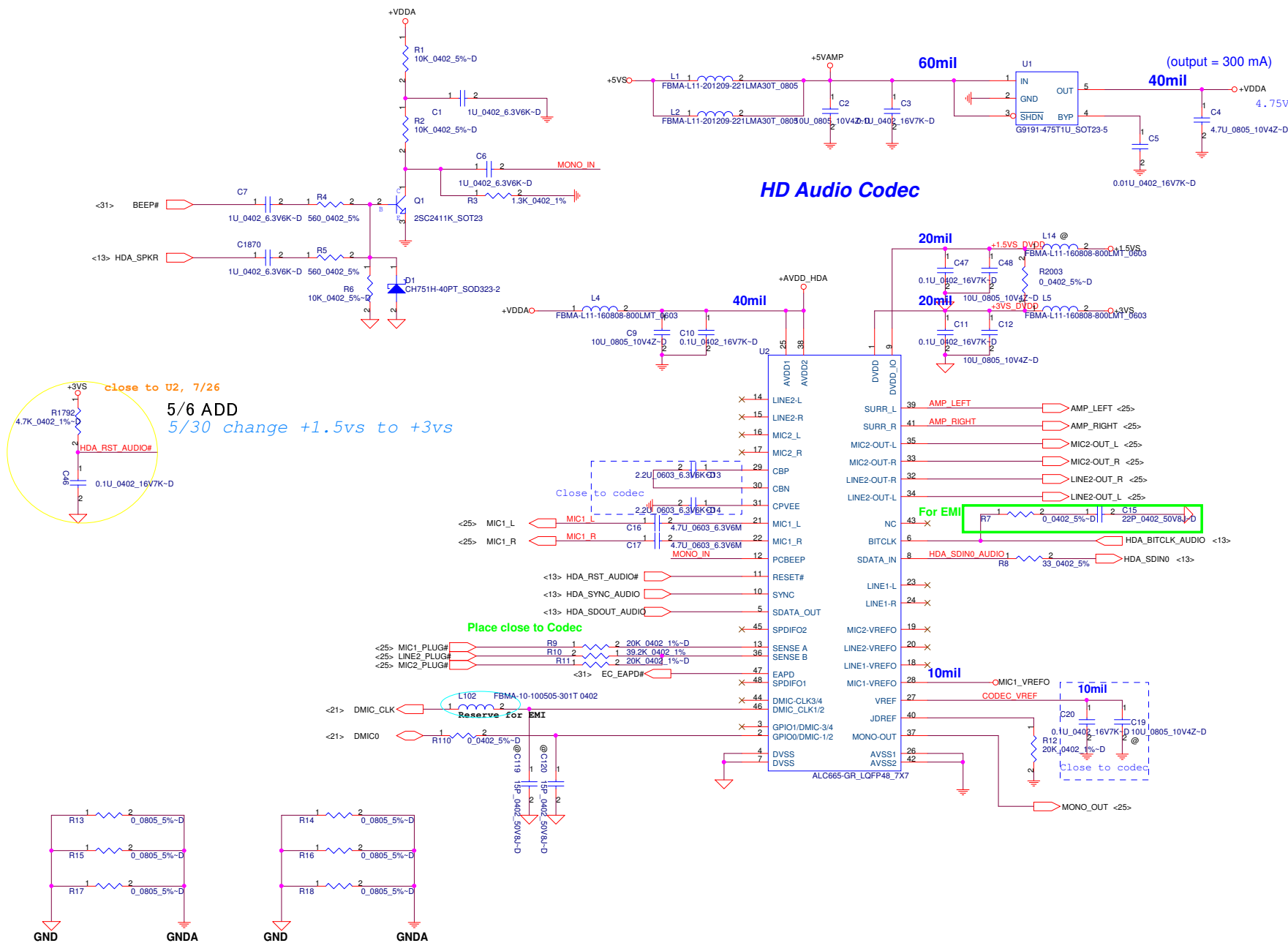




CRT

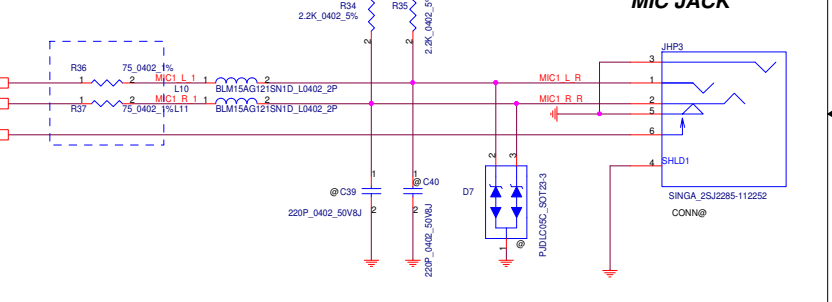
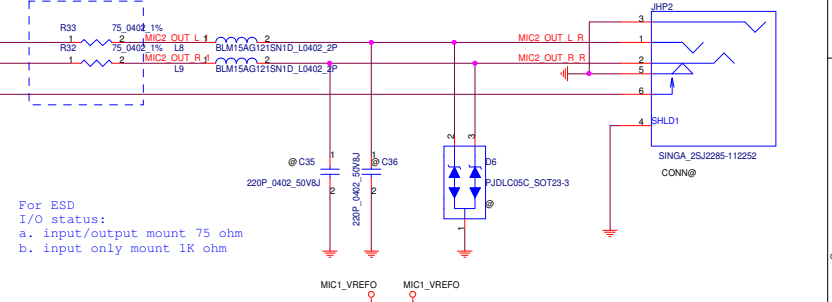
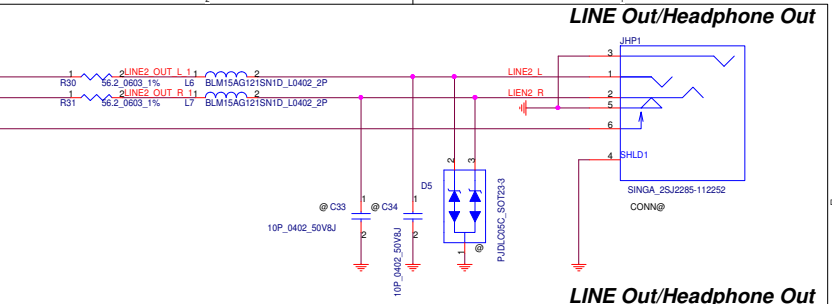
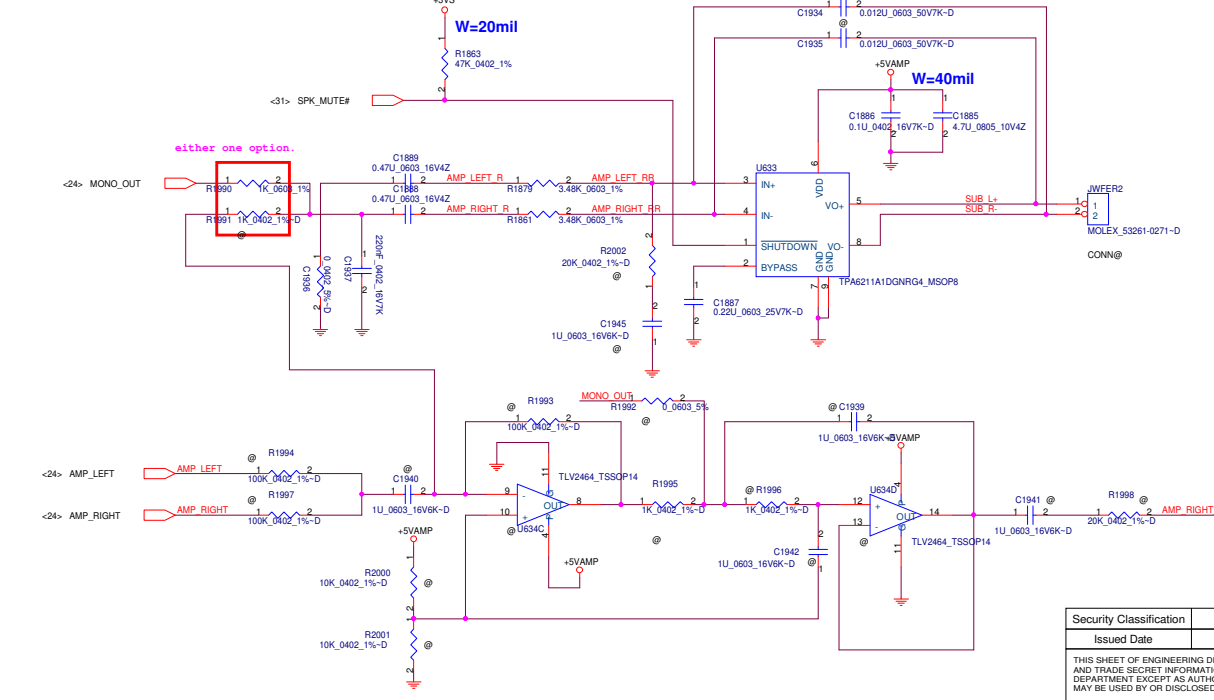
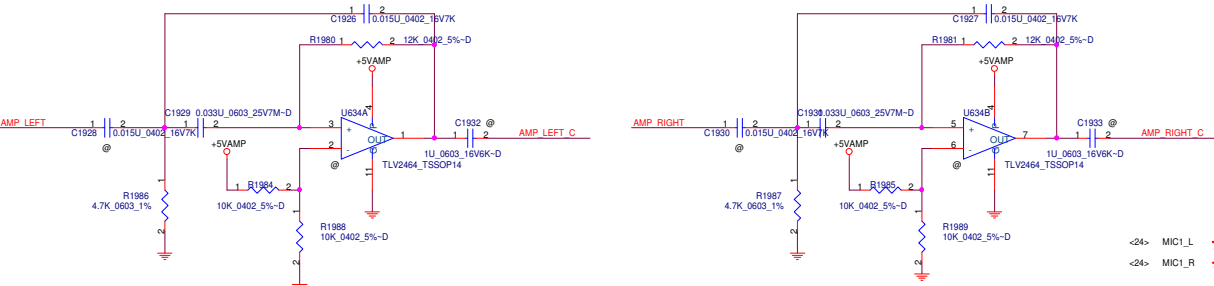
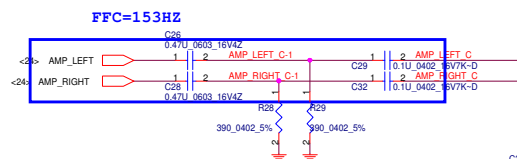


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						VGA / LVDS /camera conn.				
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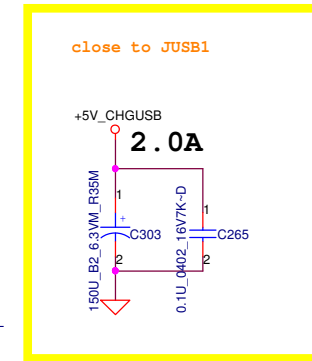
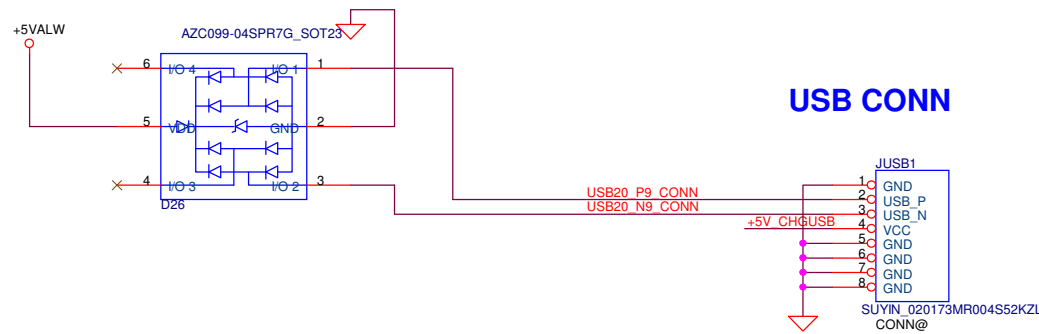
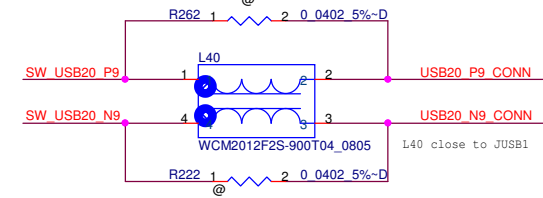
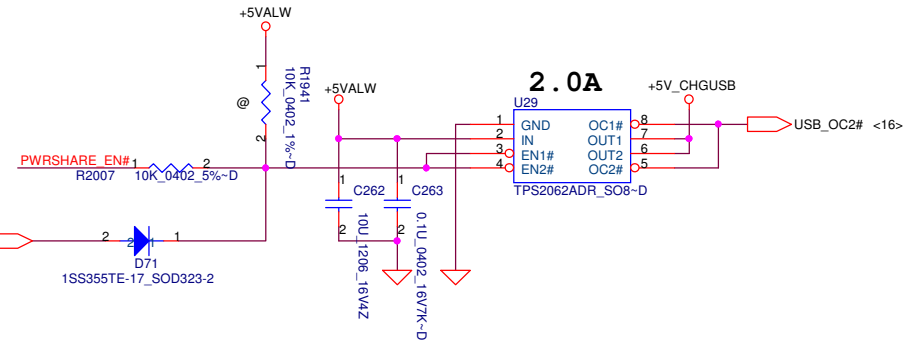
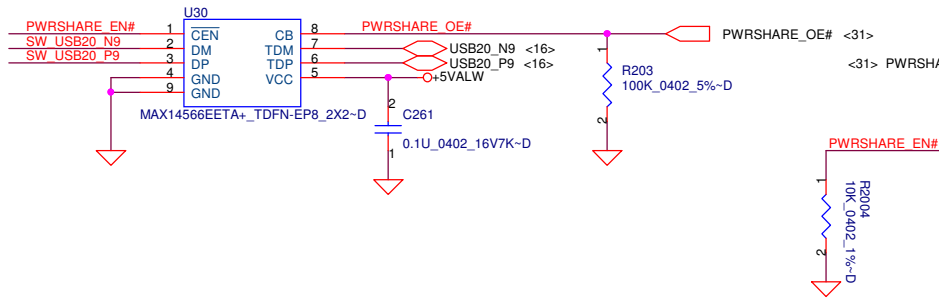
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GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

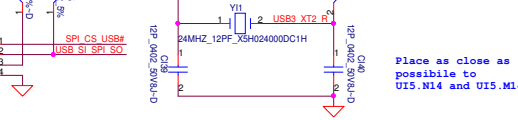
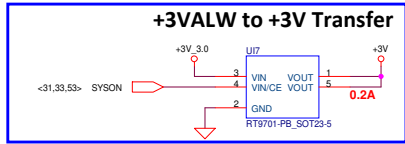


Power share

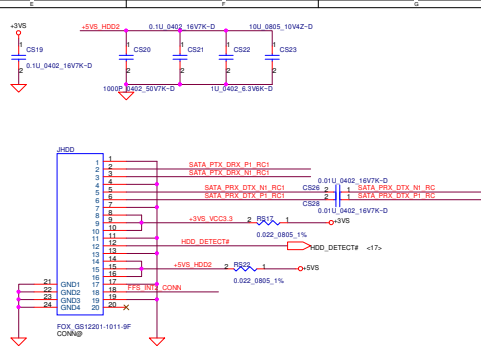
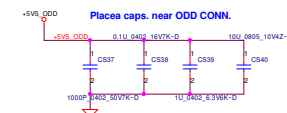
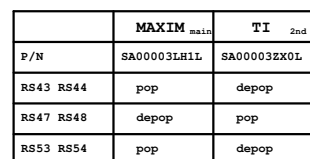
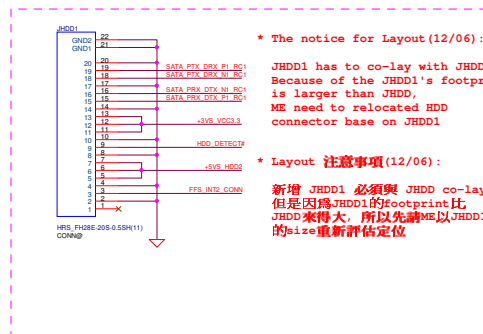
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



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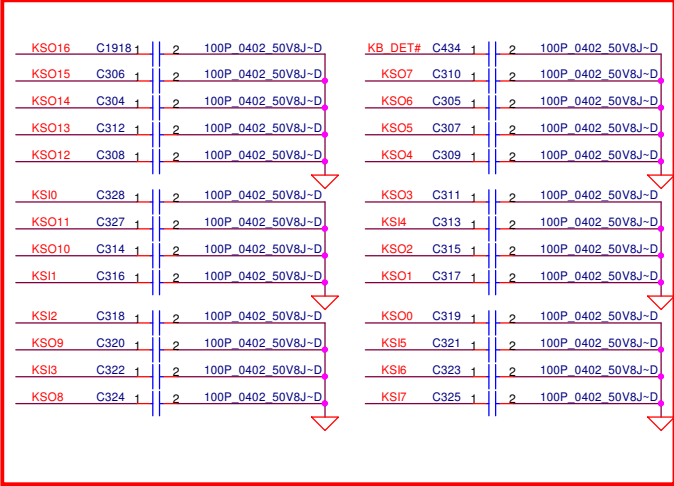
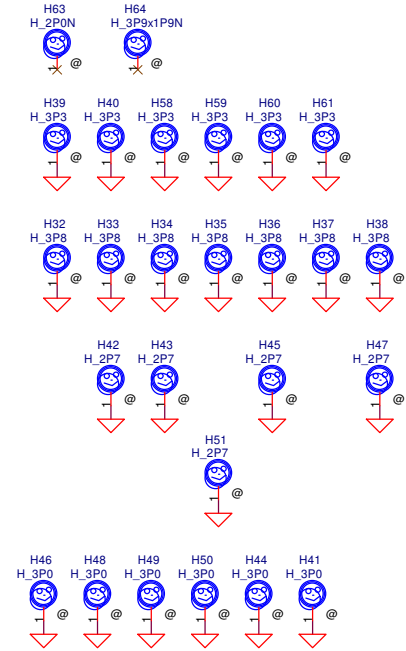
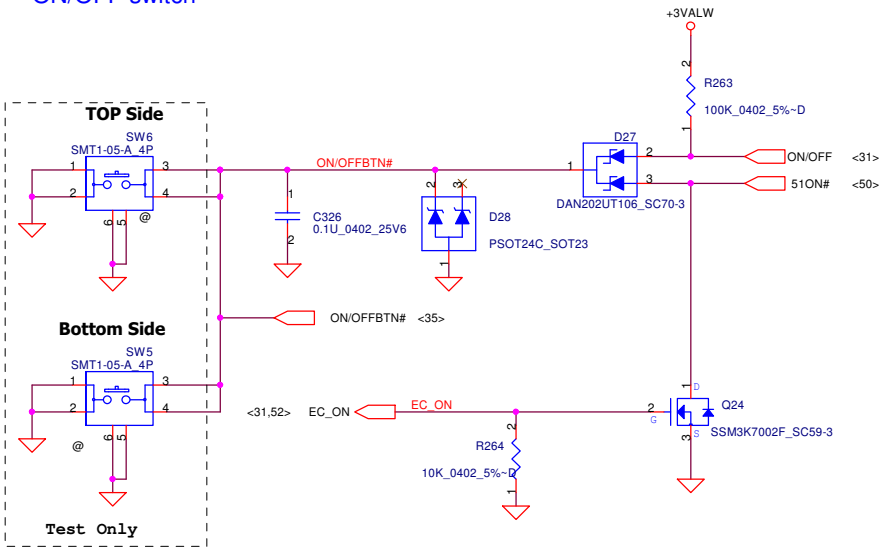


	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

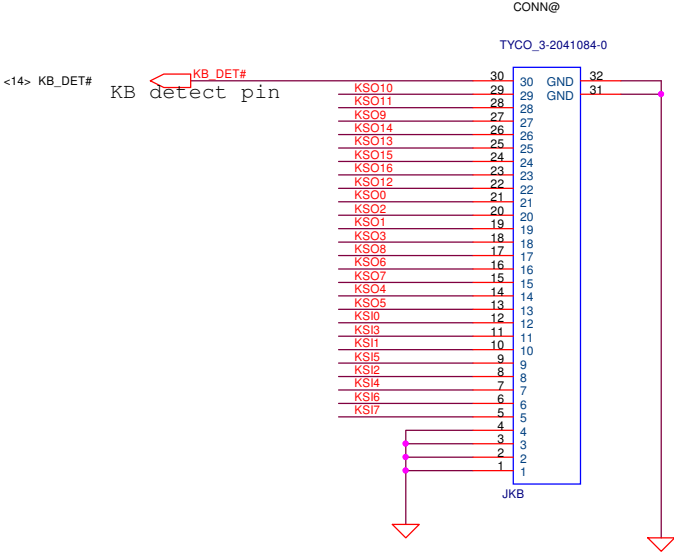
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ON/OFF switch Power Button



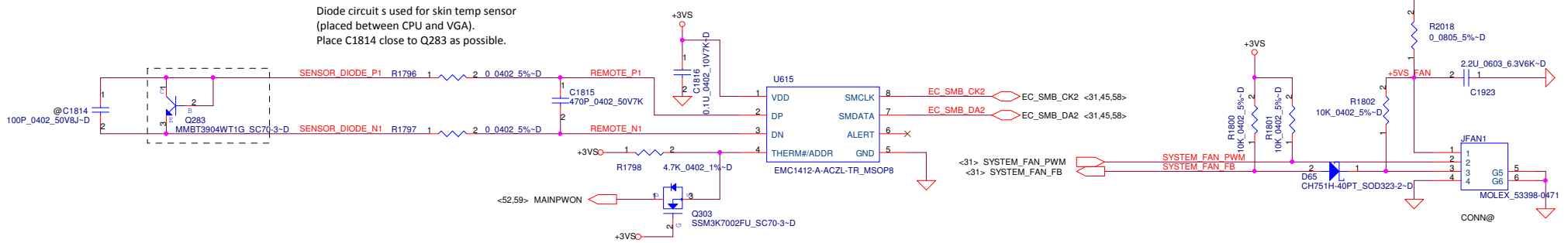
INT_KBD Conn.



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				0.3	

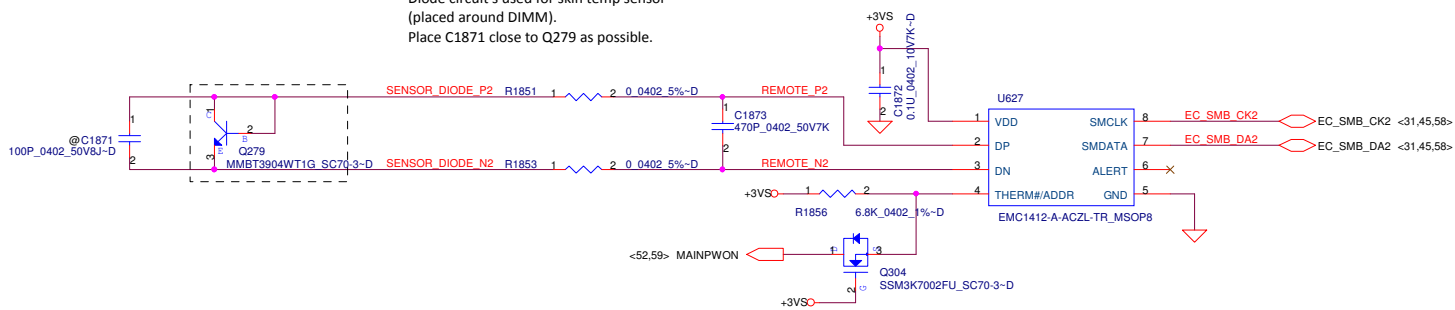
System Thermal Sensor 1

Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.

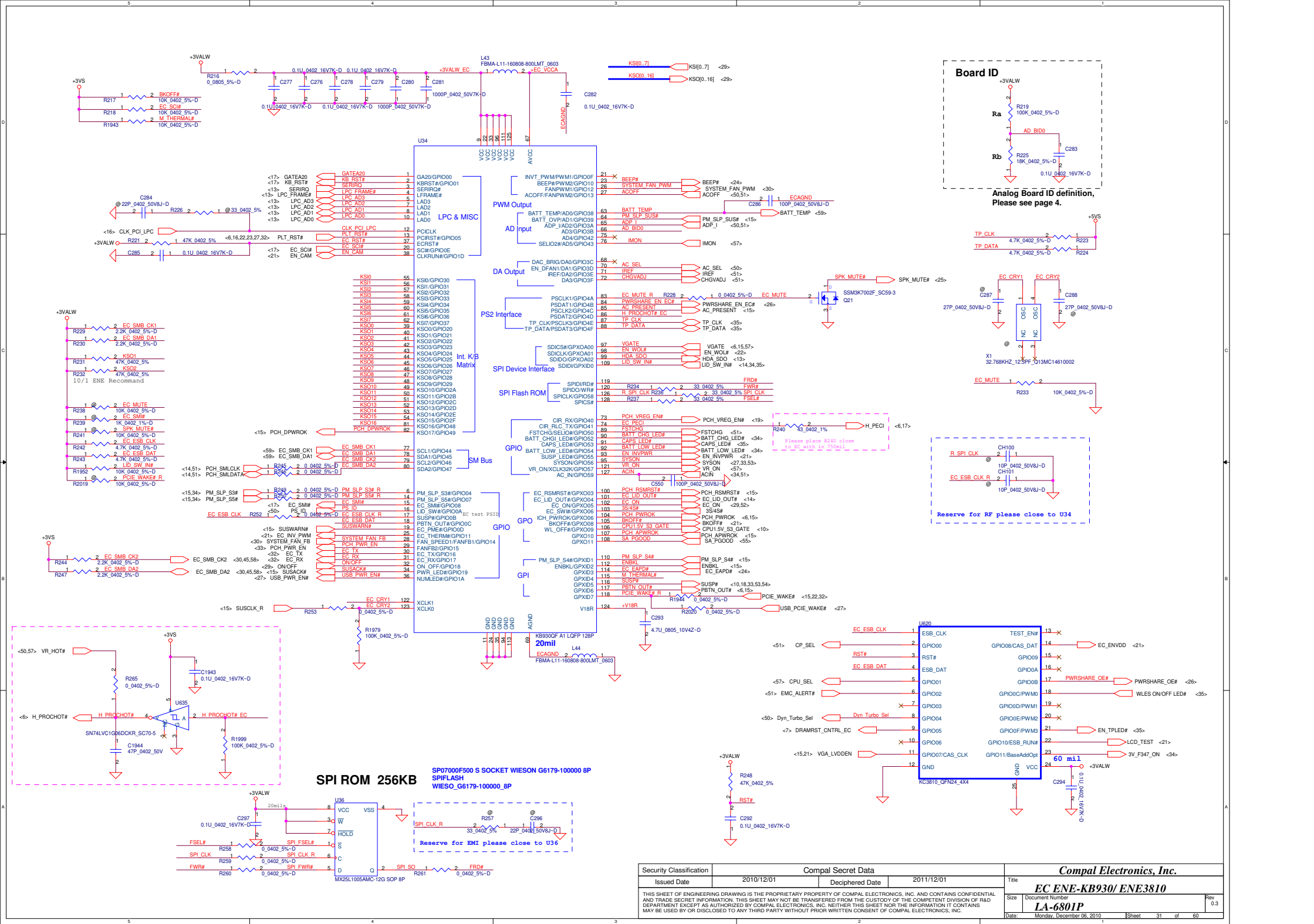


System Thermal Sensor 2

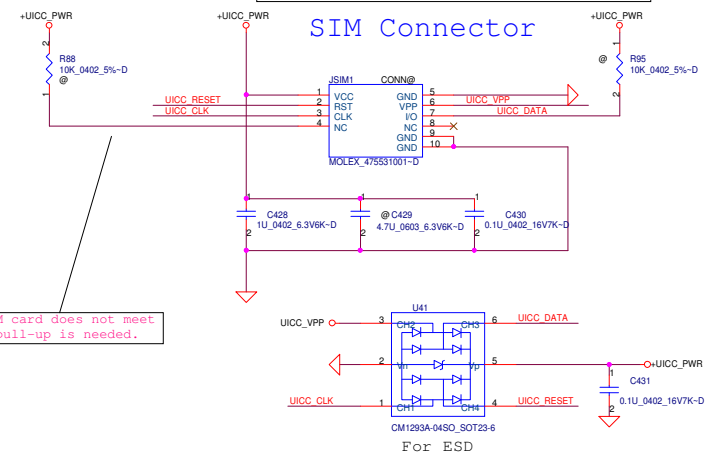
Diode circuit s used for skin temp sensor (placed around DIMM).
Place C1871 close to Q279 as possible.



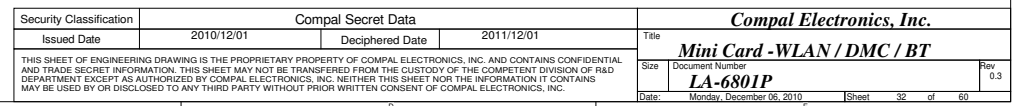
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Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title	
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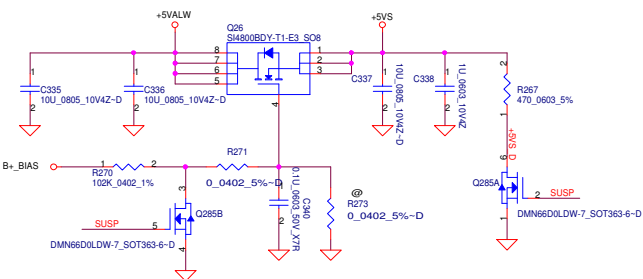
The schematic diagram illustrates the internal circuitry of a 3V5 BT module. It starts with a 3V5 power supply connected to a series of components: capacitor CU1 (0.1uF, 0402, 16V7K-D), resistor RU1 (10K, 0402, 5%-D), and capacitor CU3 (0.1uF, 0402, 16V7K-D). The signal path then splits. One branch goes through capacitor CU4 (4.7uF, 0805, 10V4Z-D) to the gate of MOSFET QU1 (A03419L_SOT23-3). The other branch goes through capacitor CU2 (1uF, 0603, 10V4Z) to the gate of MOSFET QU2 (SSM3K7002F_SC59-3). The gates of both MOSFETs are also connected to the 3V5 supply. The drain of QU1 is connected to the gate of QU2. The source of QU1 is connected to ground. The source of QU2 is connected to the 3V5 supply. The output of the module is taken from the drain of QU2, labeled '3V5_BT'. A note 'W=40mils' indicates the width of the traces. The input signal is labeled 'BT_ON#' and the output is '3V5_BT'.



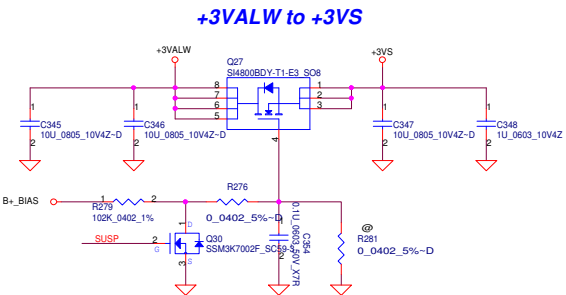
For ESD



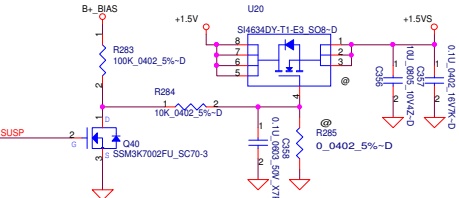
+5VALW to +5VS



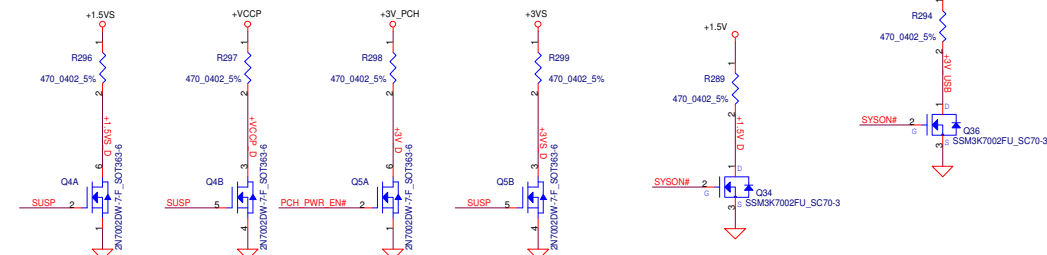
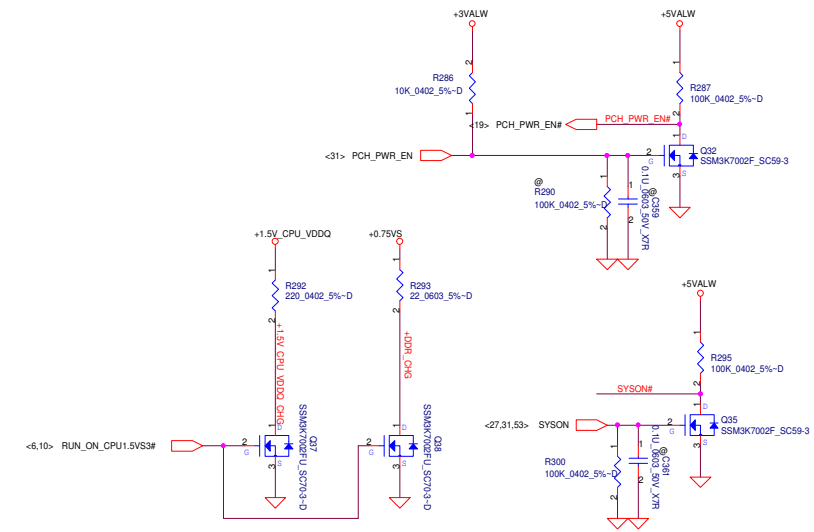
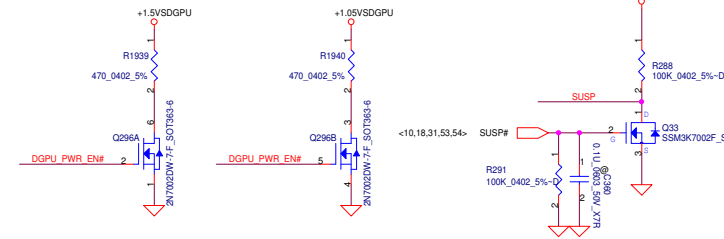
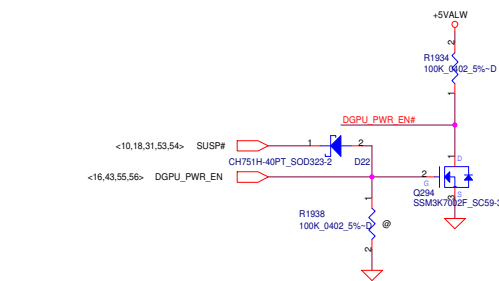
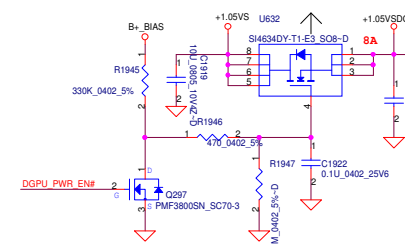
+3VALW to +3V_PCH



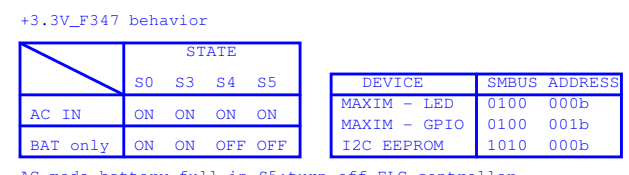
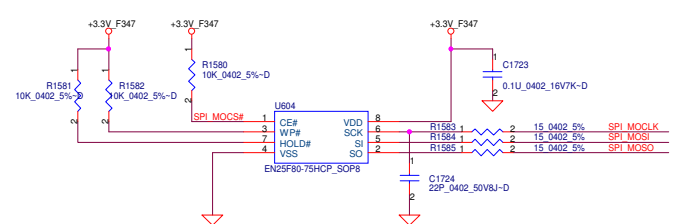
+1.5V To +1.5VS

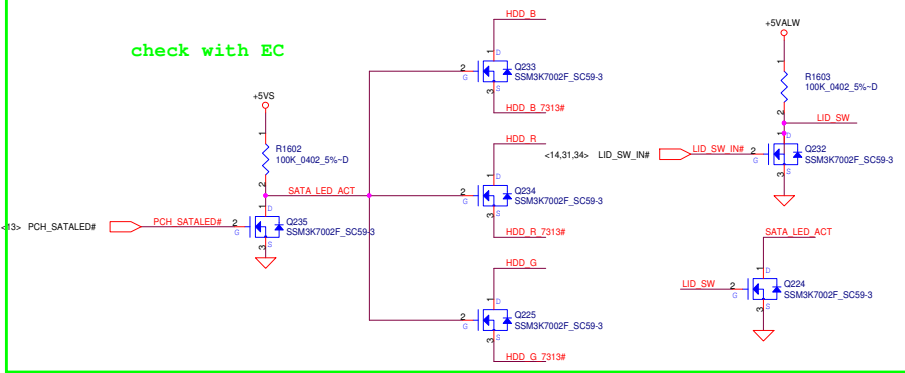
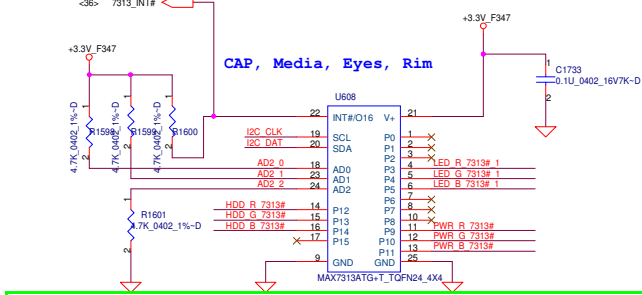
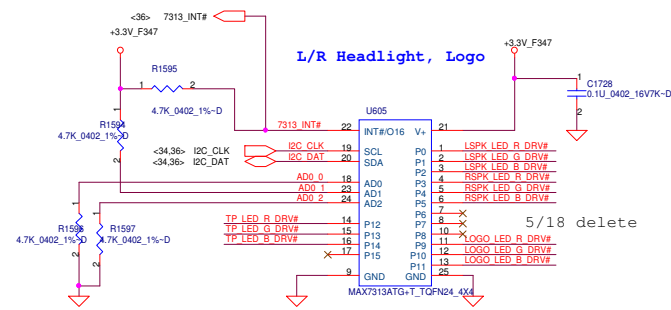


+1.05V to +1.05VSDGPU Transfer

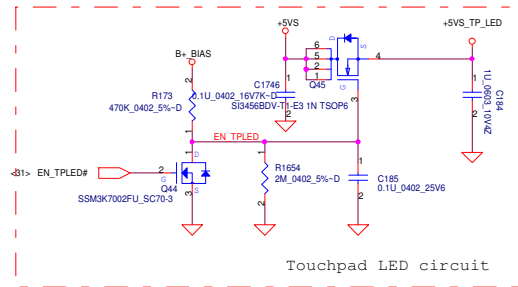


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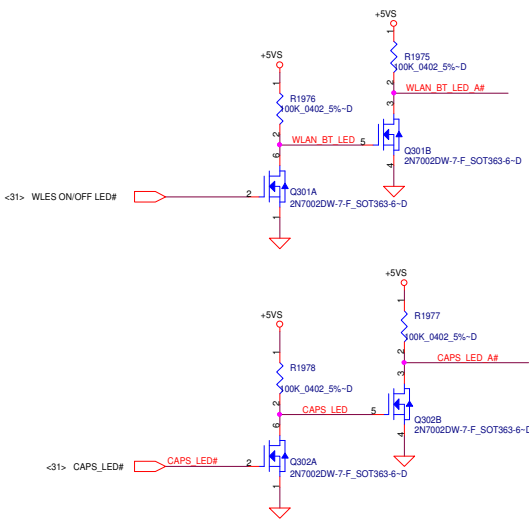
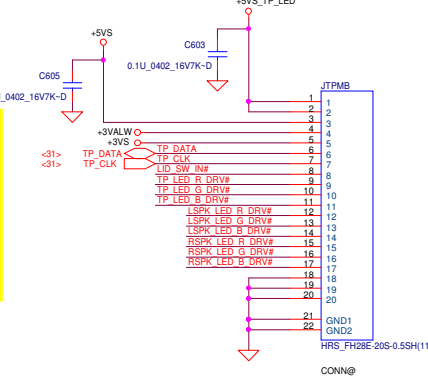




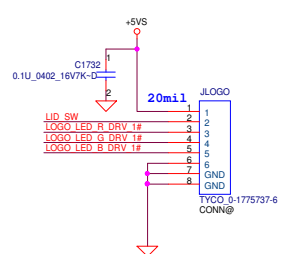
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight , Logo, TP
U608	0	1	1	Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim



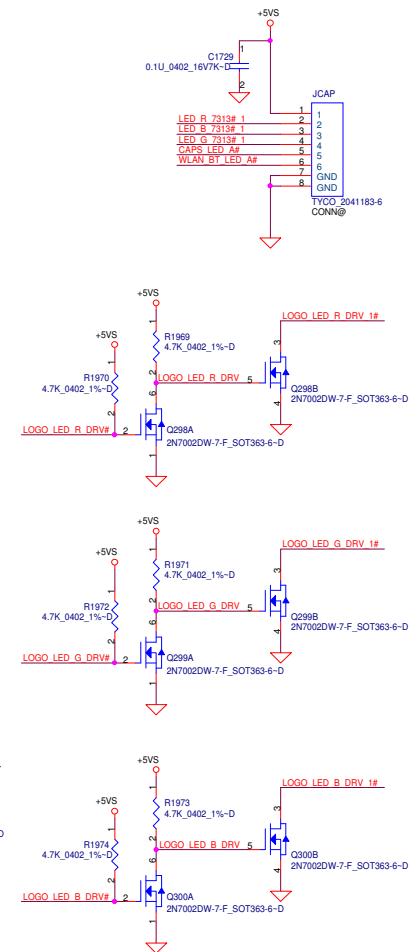
Touchpad LED CONN



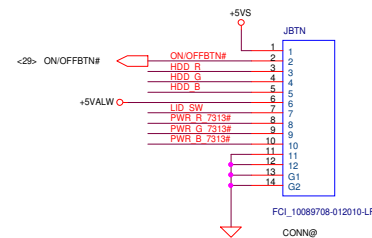
LOGO Board CONN

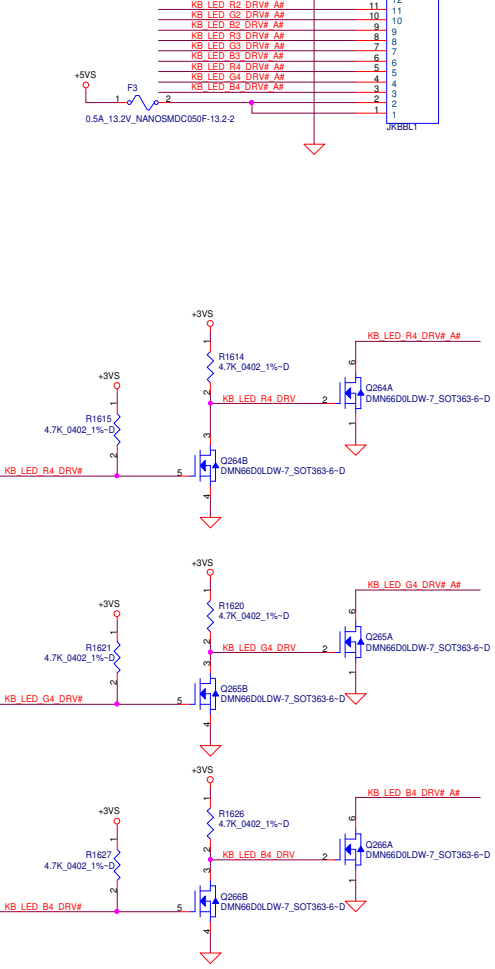
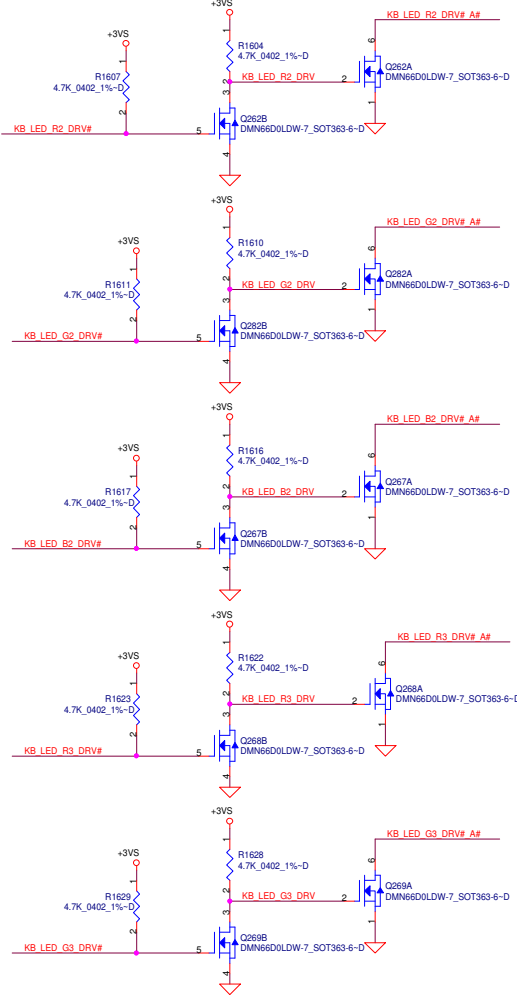
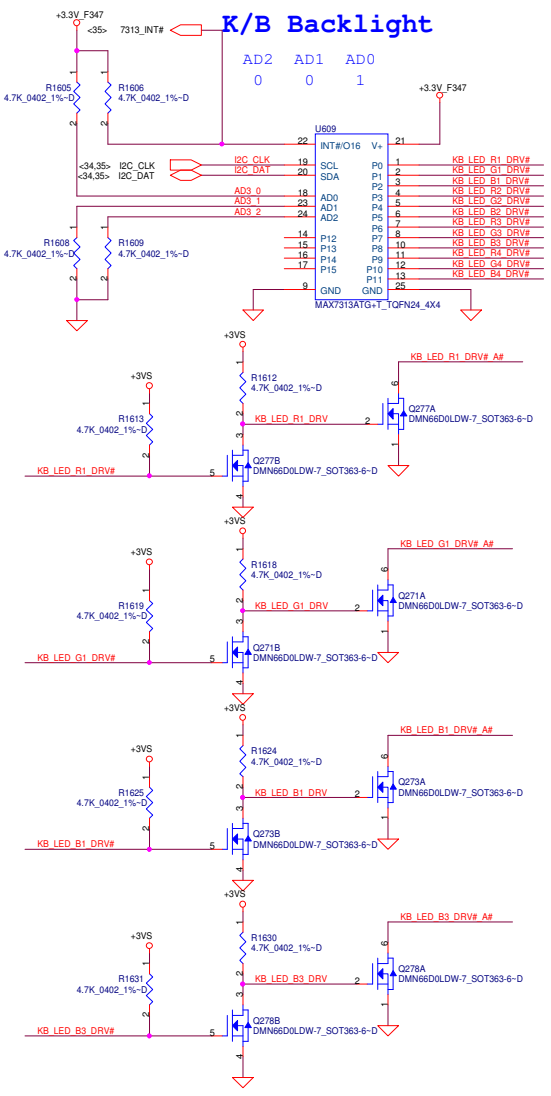


Indicator CONN

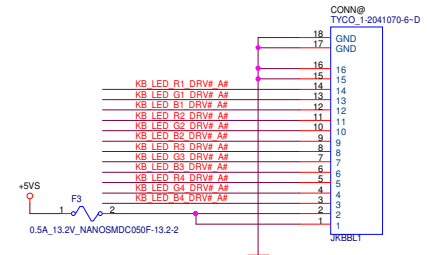


PWR BTN Board CONN

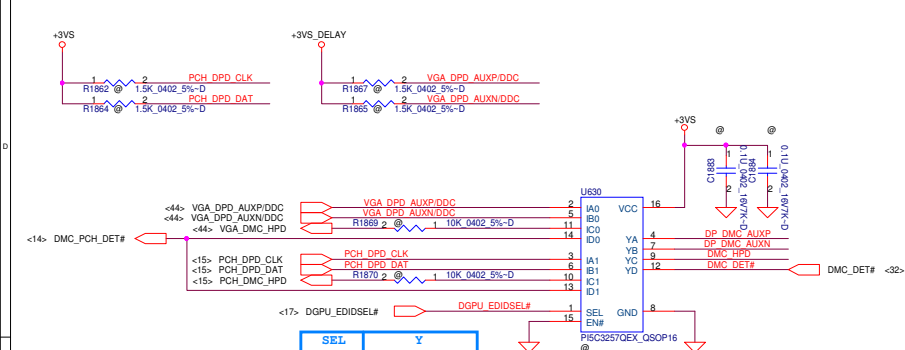




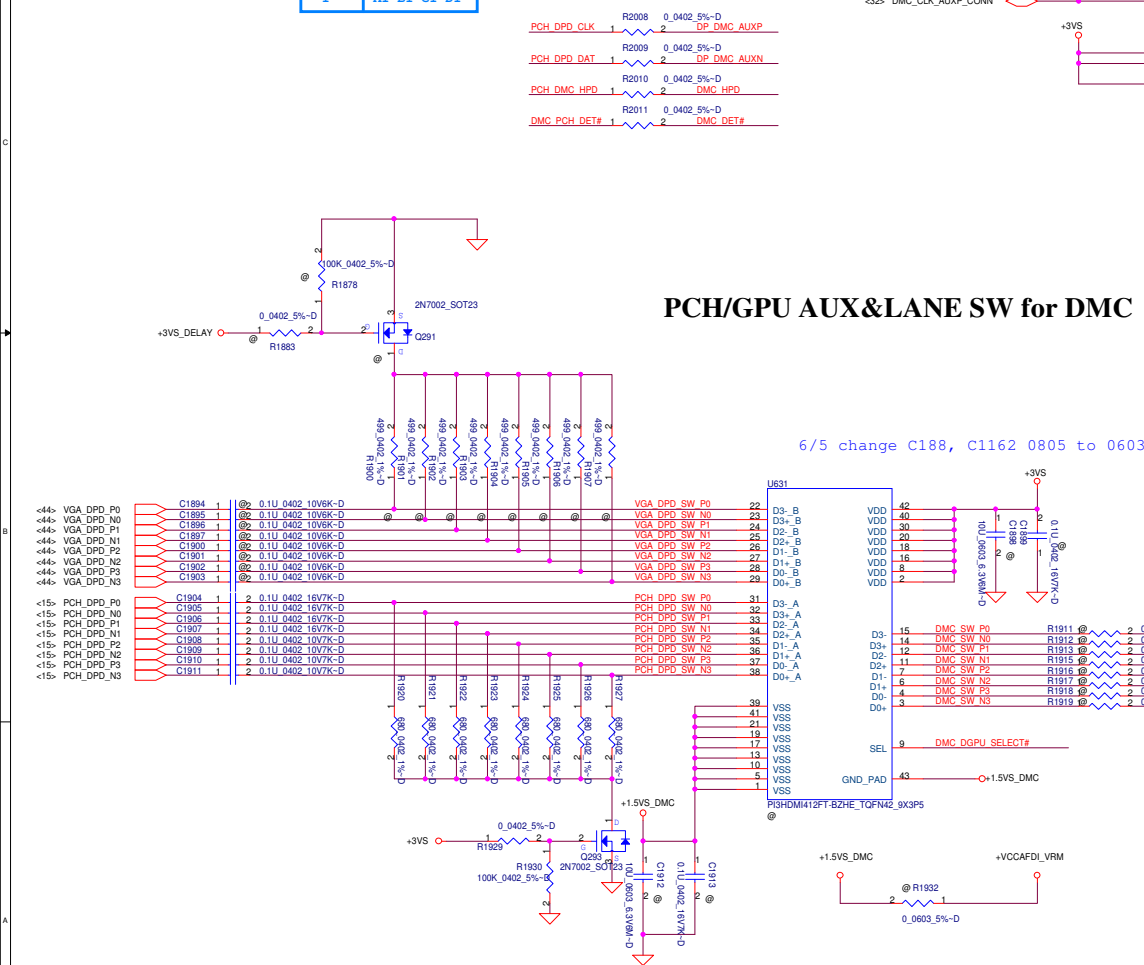
K/B Backlight CONN



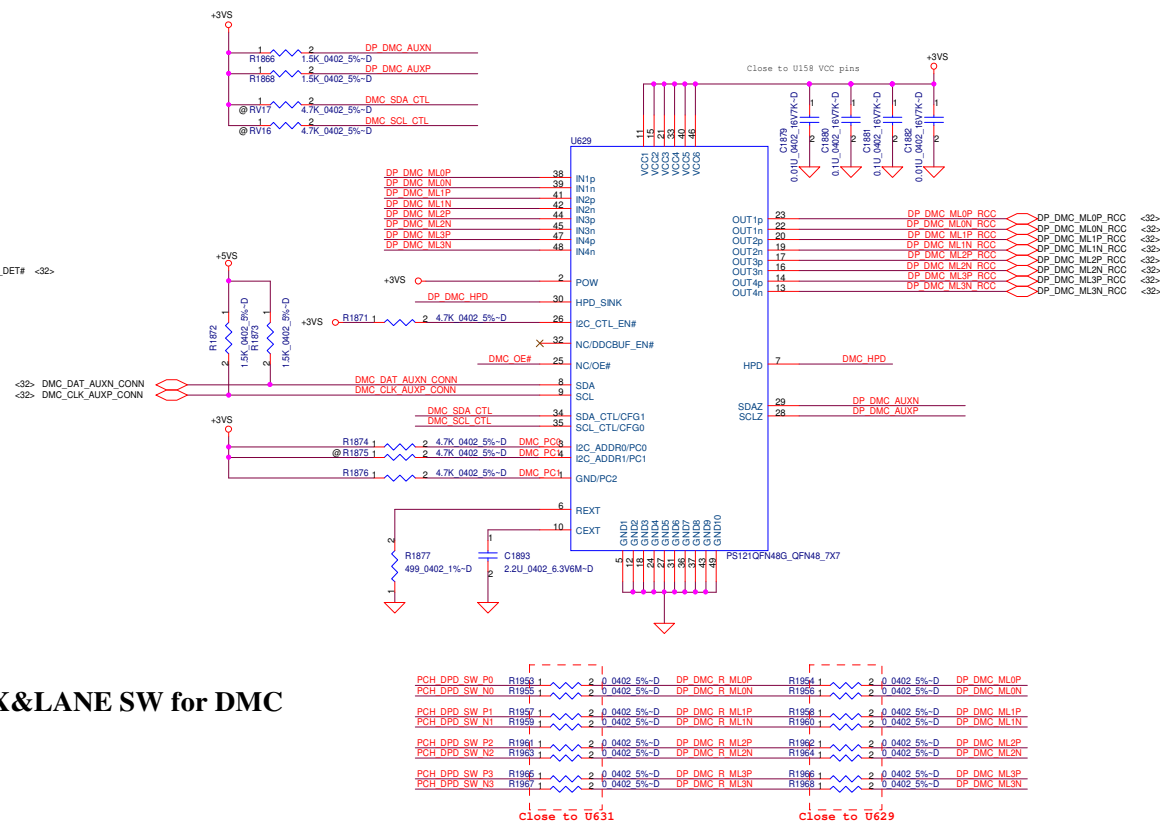
PCH/GPU DDC SW for DMC



PCH/GPU AUX&LANE SW for DMC



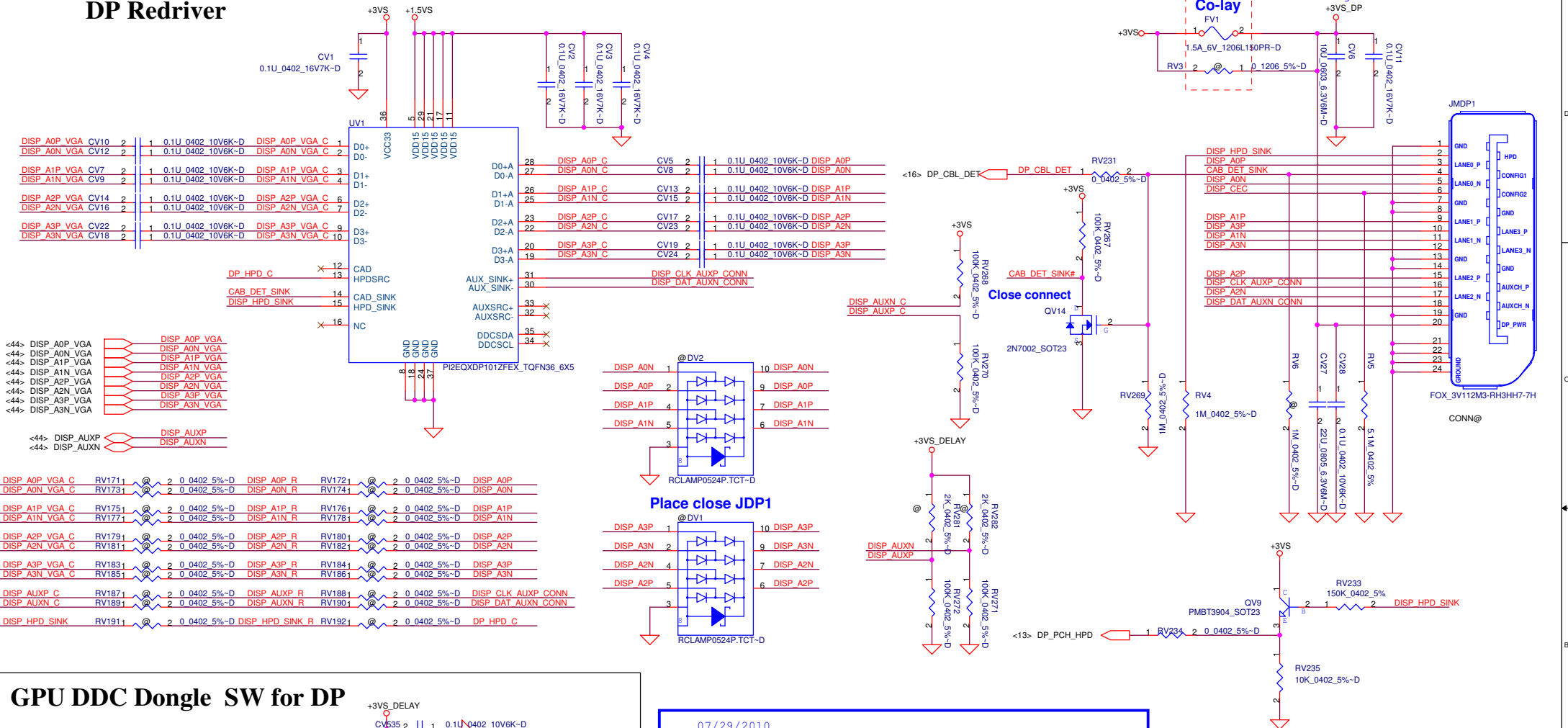
DMC Redriver



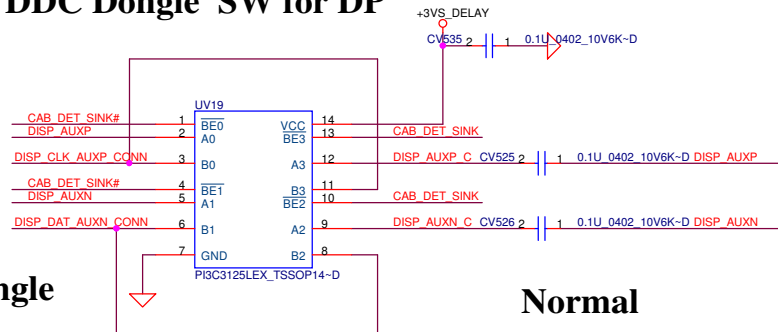
AUX_SEL/SEL1&2	Chanel	Source
0	A	GPU
1	B	PCH

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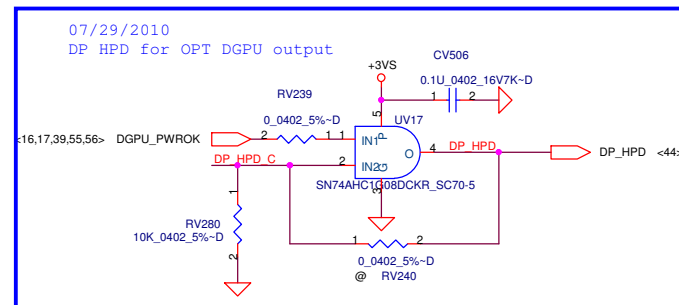
DP Redriver



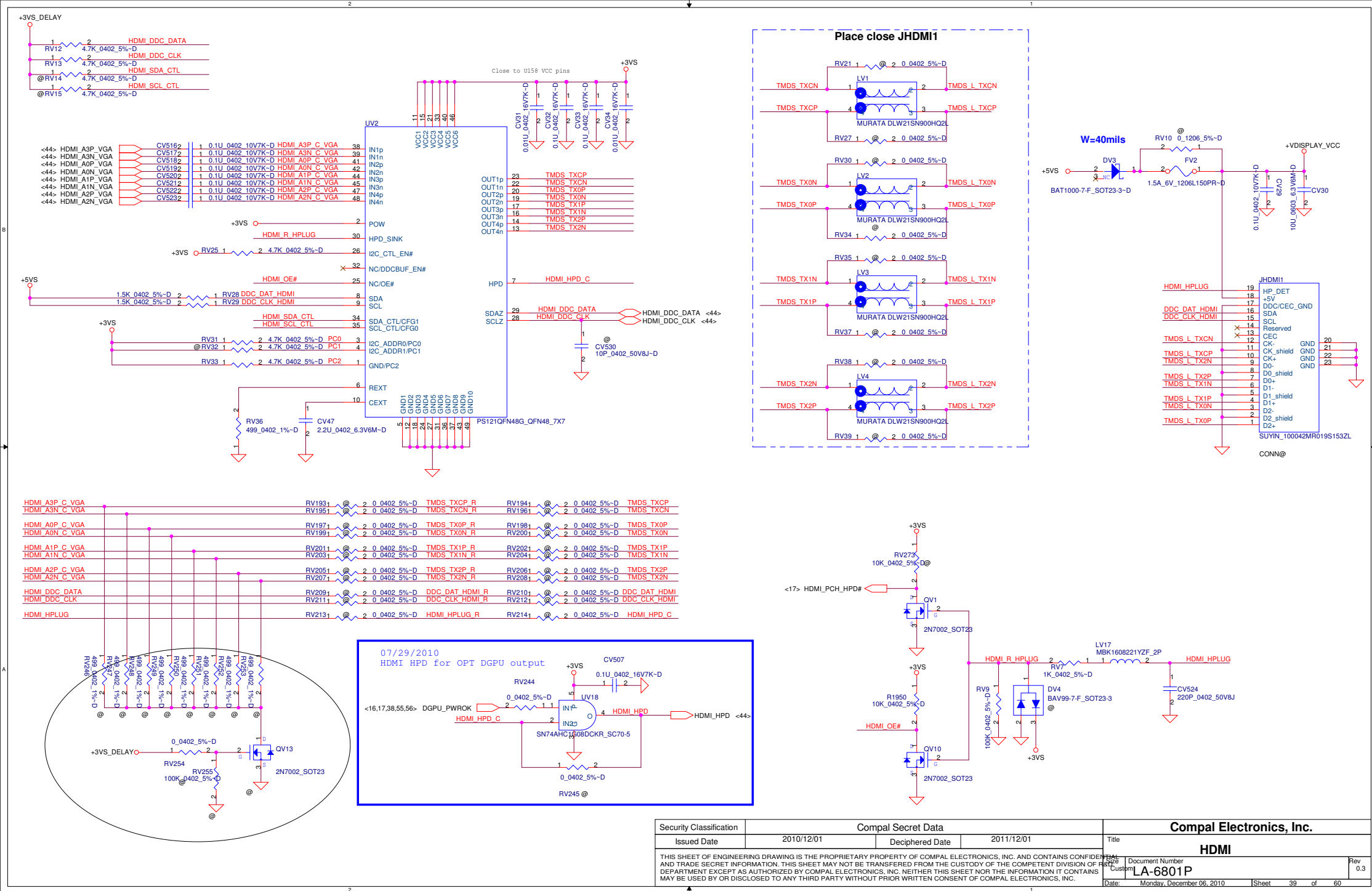
GPU DDC Dongle SW for DP

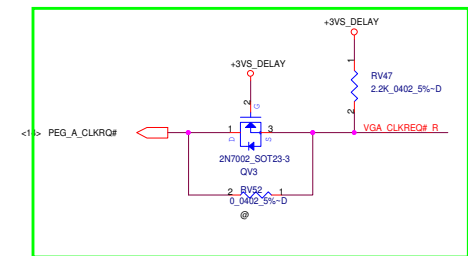
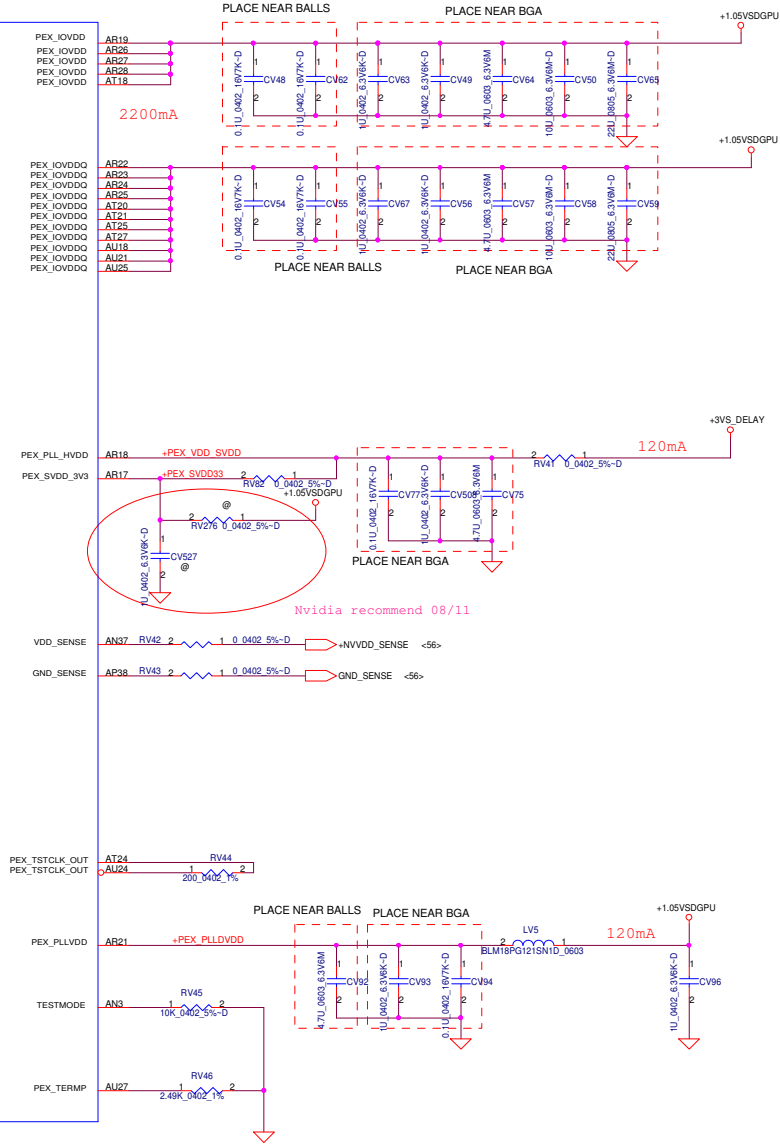
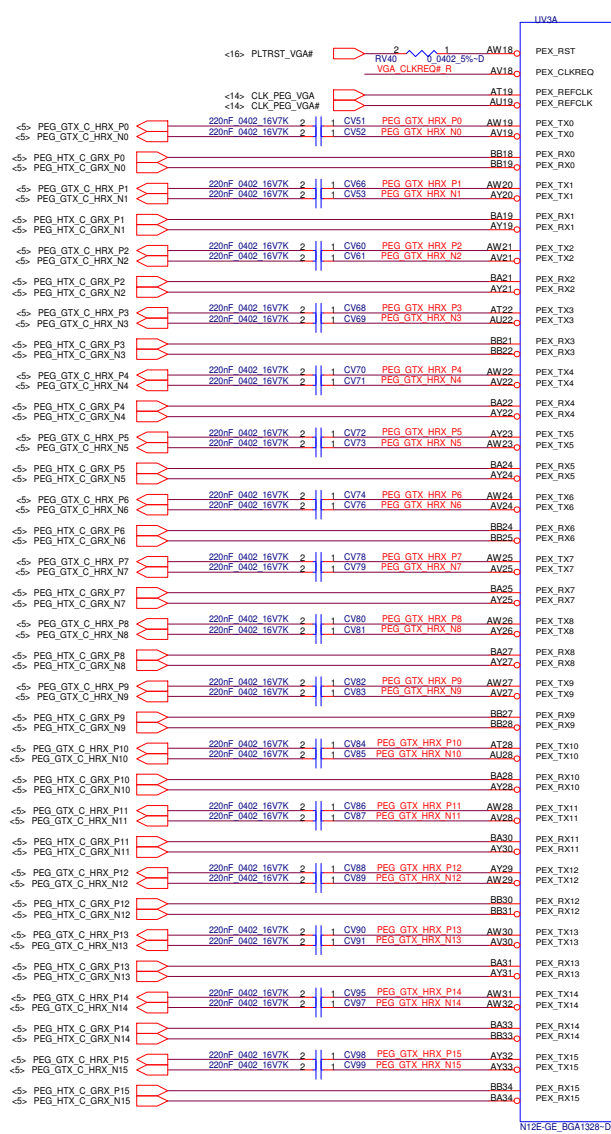


Normal

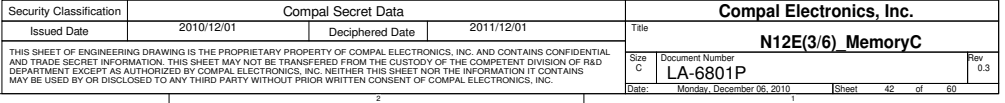


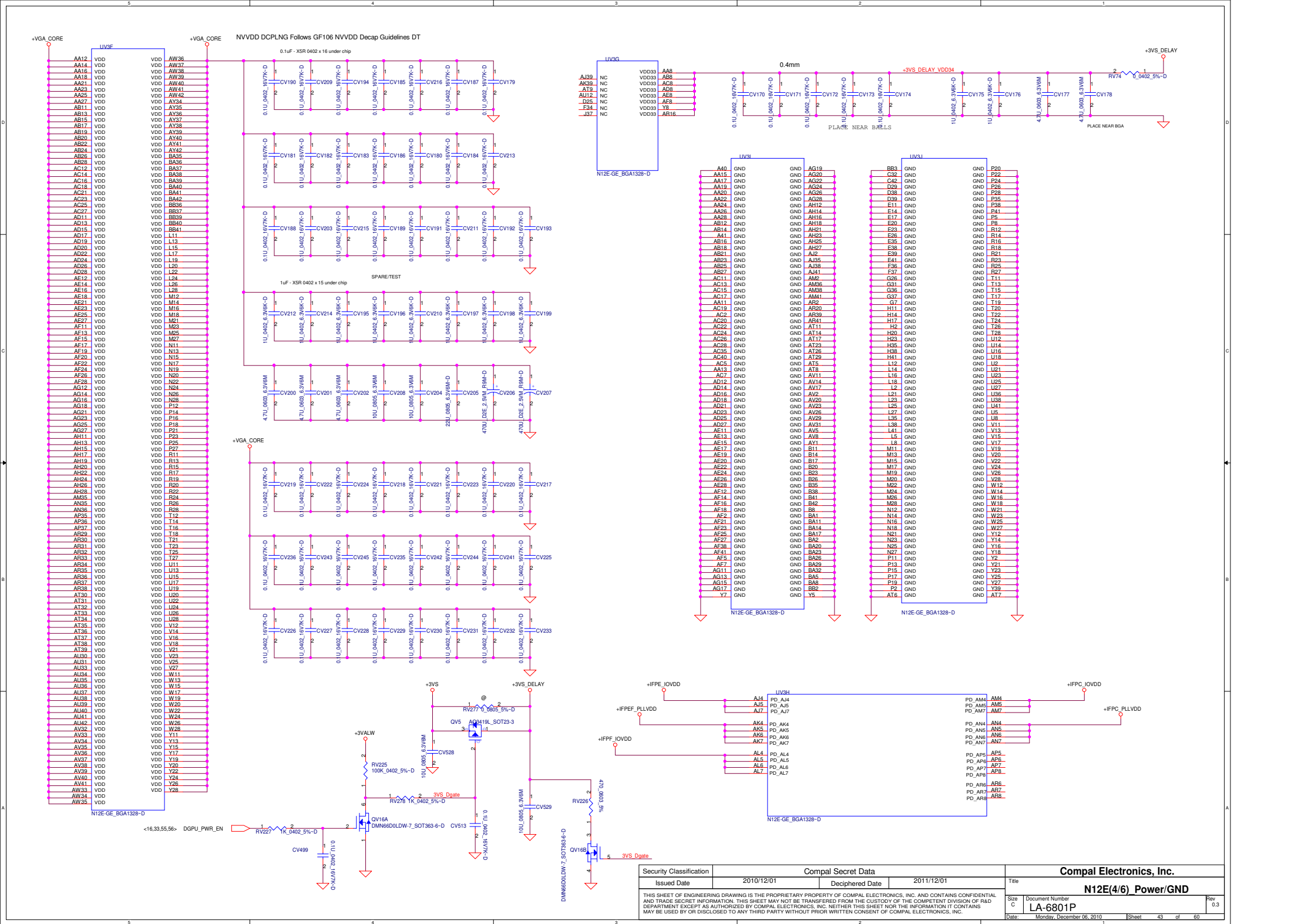
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/12/01	Deciphered Date	2011/12/01	Title		
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				Size	Document Number	Rev
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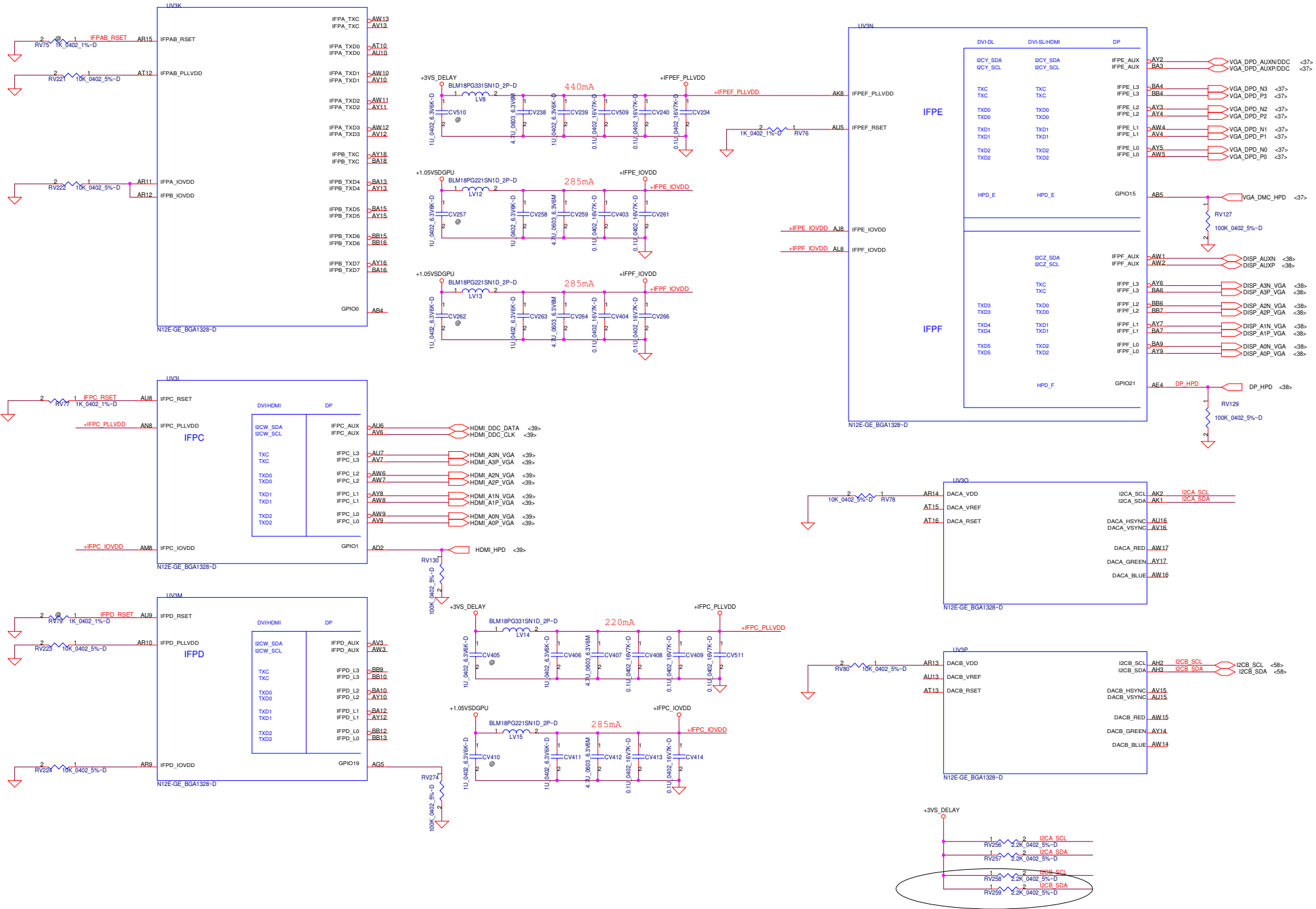


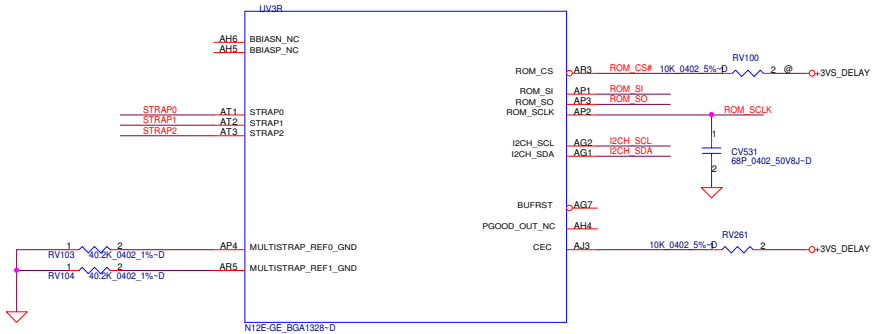
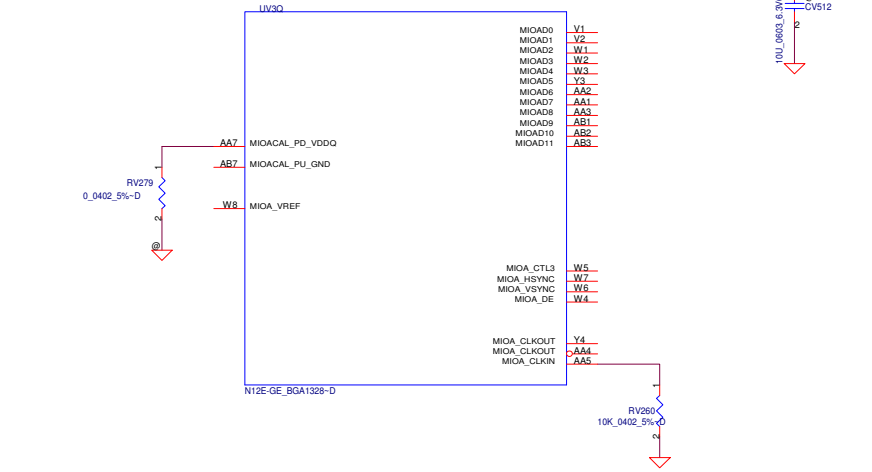


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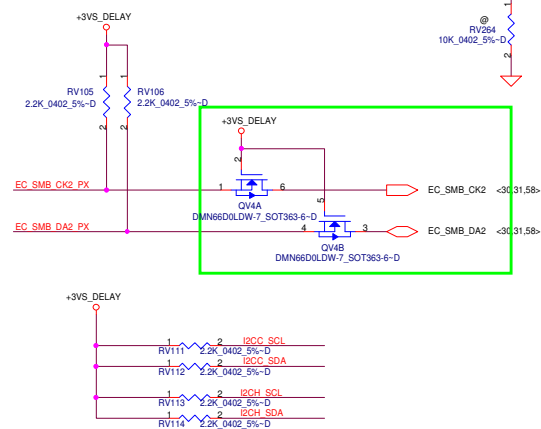
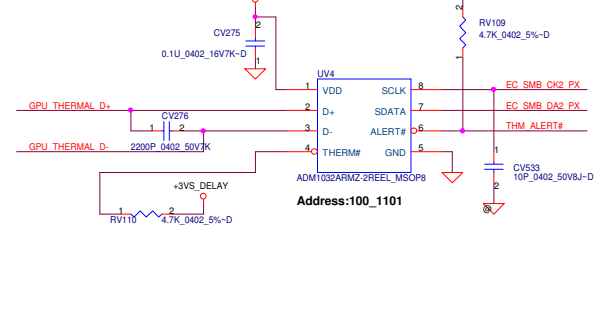




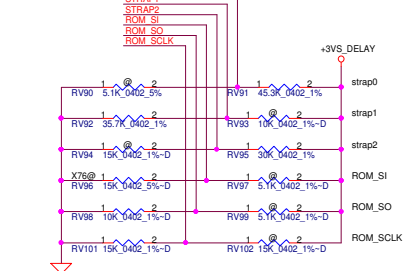


VGA Thermal Sensor ADM1032ARMZ

Closed to GPU



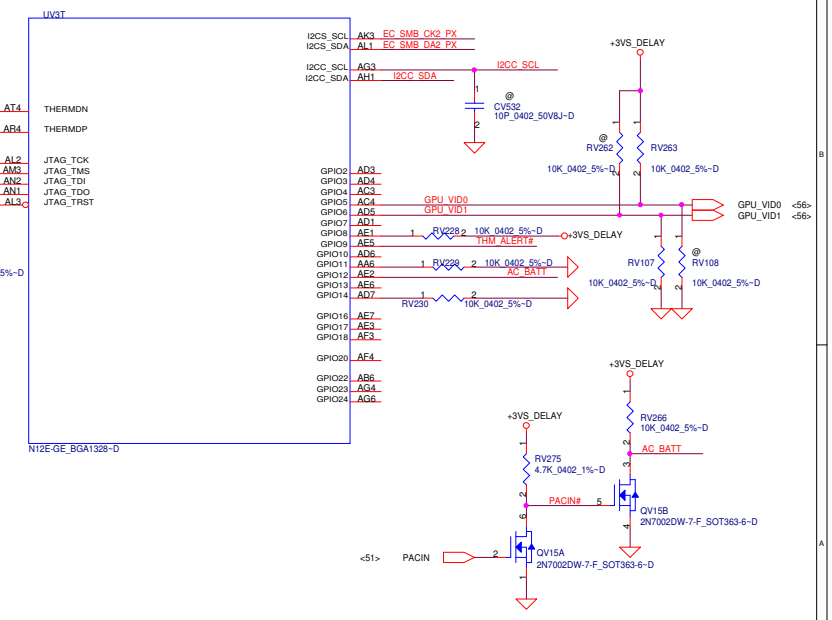
Straps

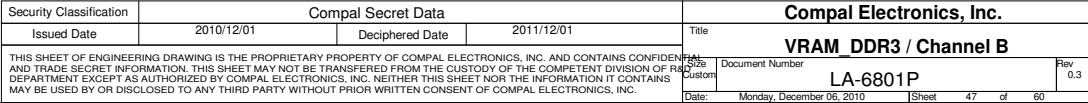


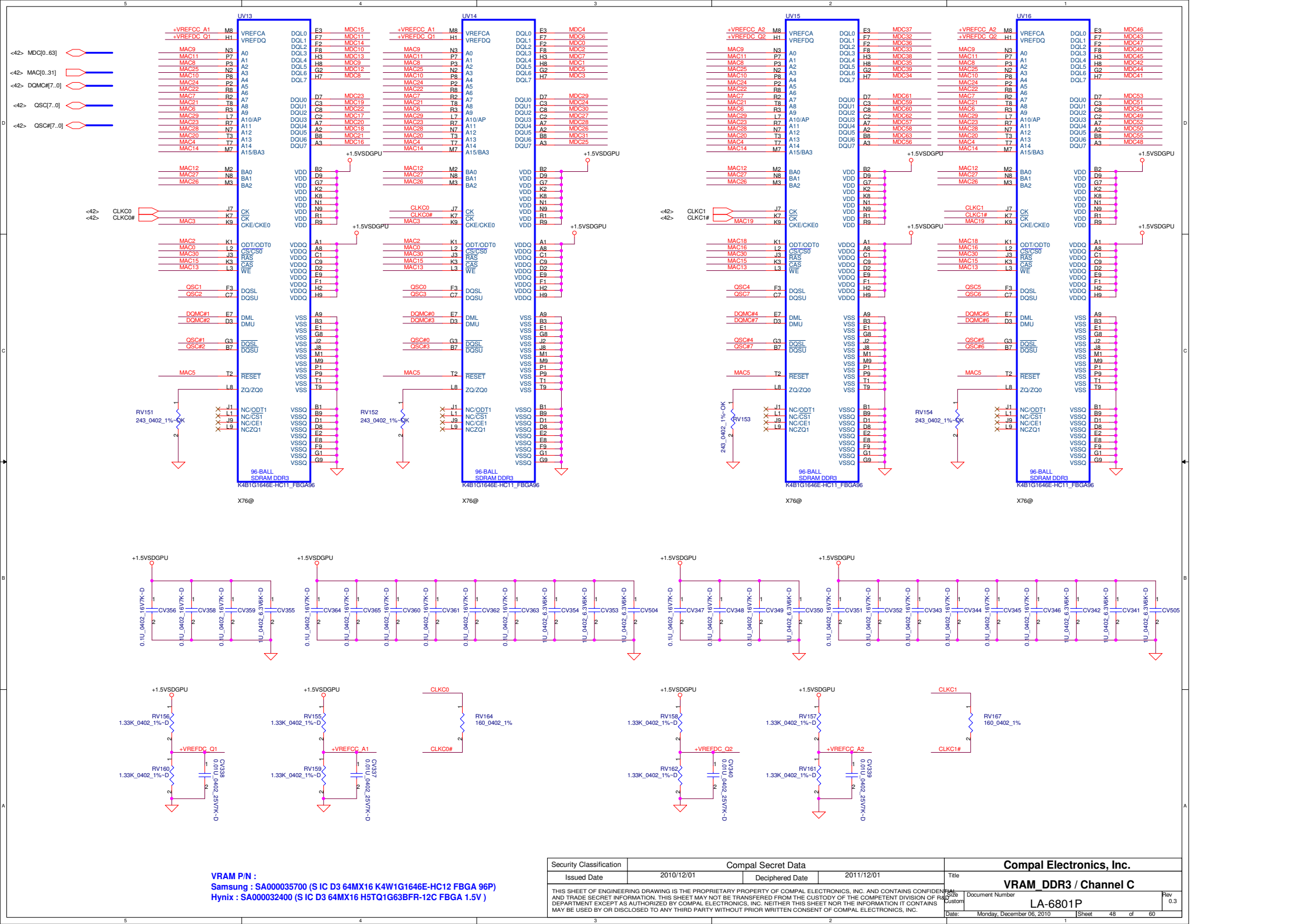
MULTI LEVEL STRAPS

	ROM_SI
64MX16 Samsung	Pull low with RV96=20K
64MX16 Hynix	Pull low with RV96=15K
128MX16 Samsung	Pull low with RV96=45K
128MX16 Hynix	Pull low with RV96=35K

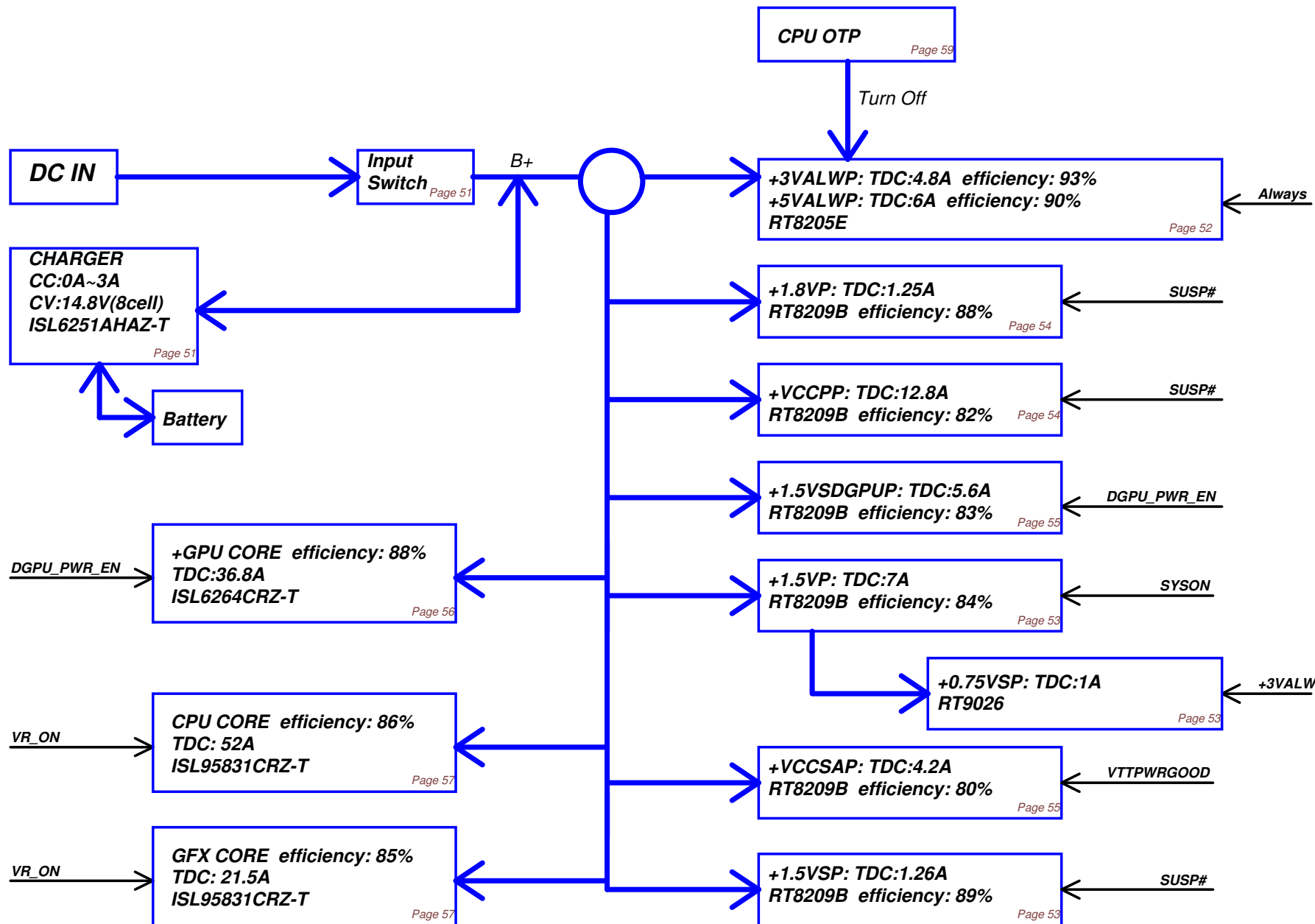
SSI --> Hynix







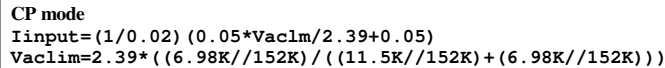
Power block



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$$CP = 90\% \cdot I_{ada} ; CP = 6.92A$$
$$CP = 90\% \cdot I_{ada} ; CP = 6.92A$$

add 10/20
for EMI request



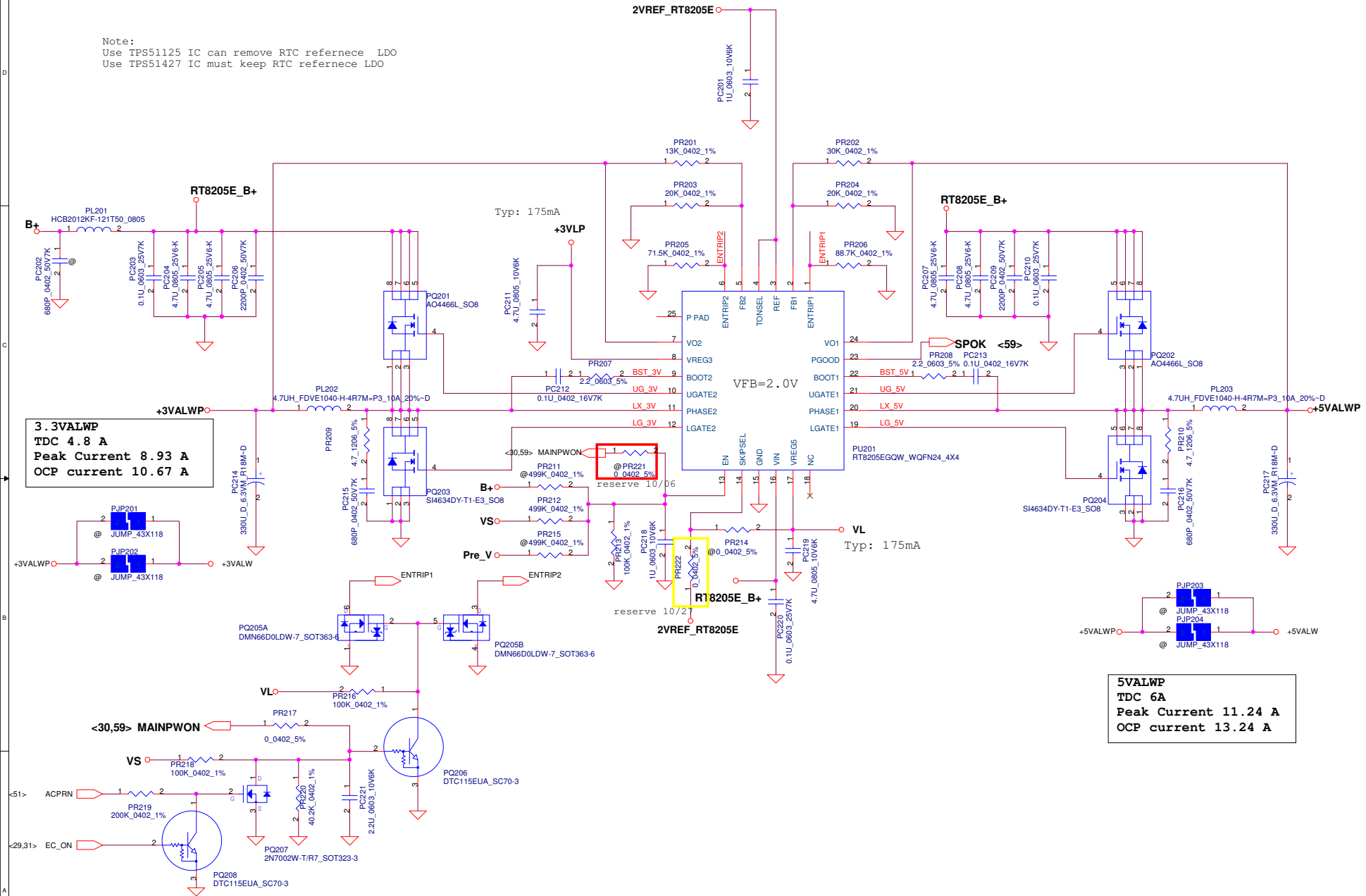
IREF=1*Icharge
IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

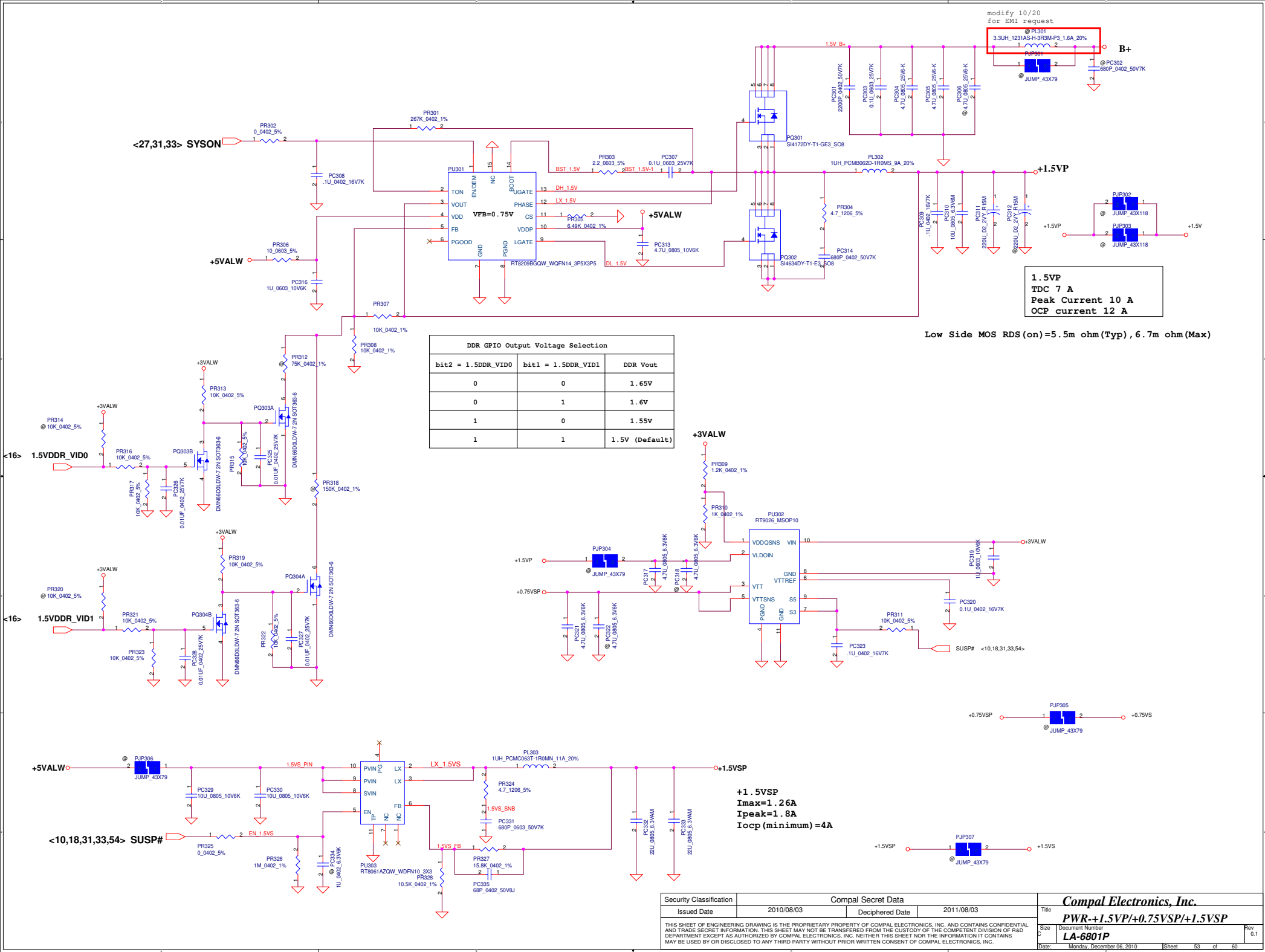
Compal Electronics, Inc.

ENTR Size Rev Custom s	PWR-CHARGER Document Number LA-6801P	Rev 0.1
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Note:
Use TPS51125 IC can remove RTC reference LDO
Use TPS51427 IC must keep RTC reference LDO

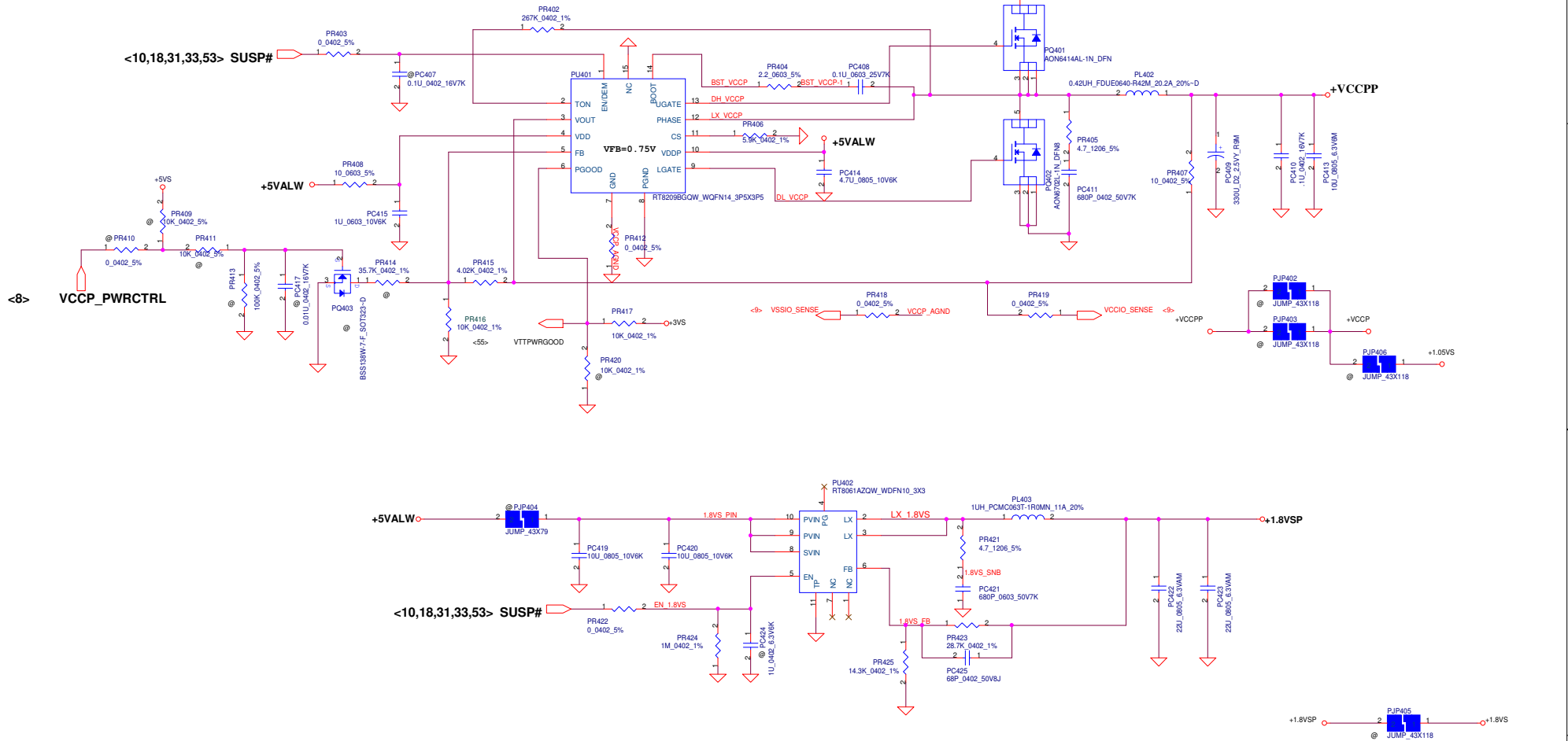


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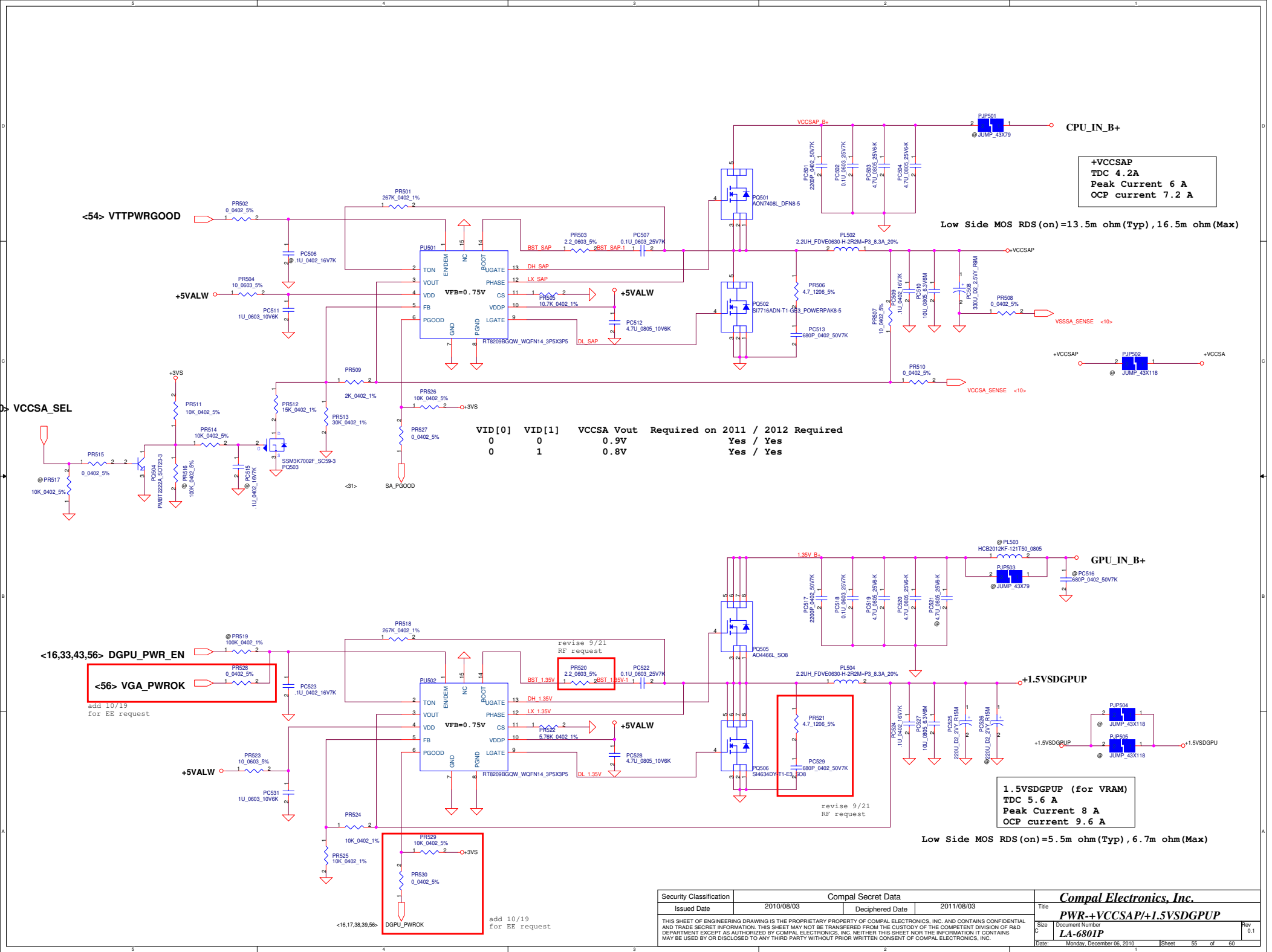


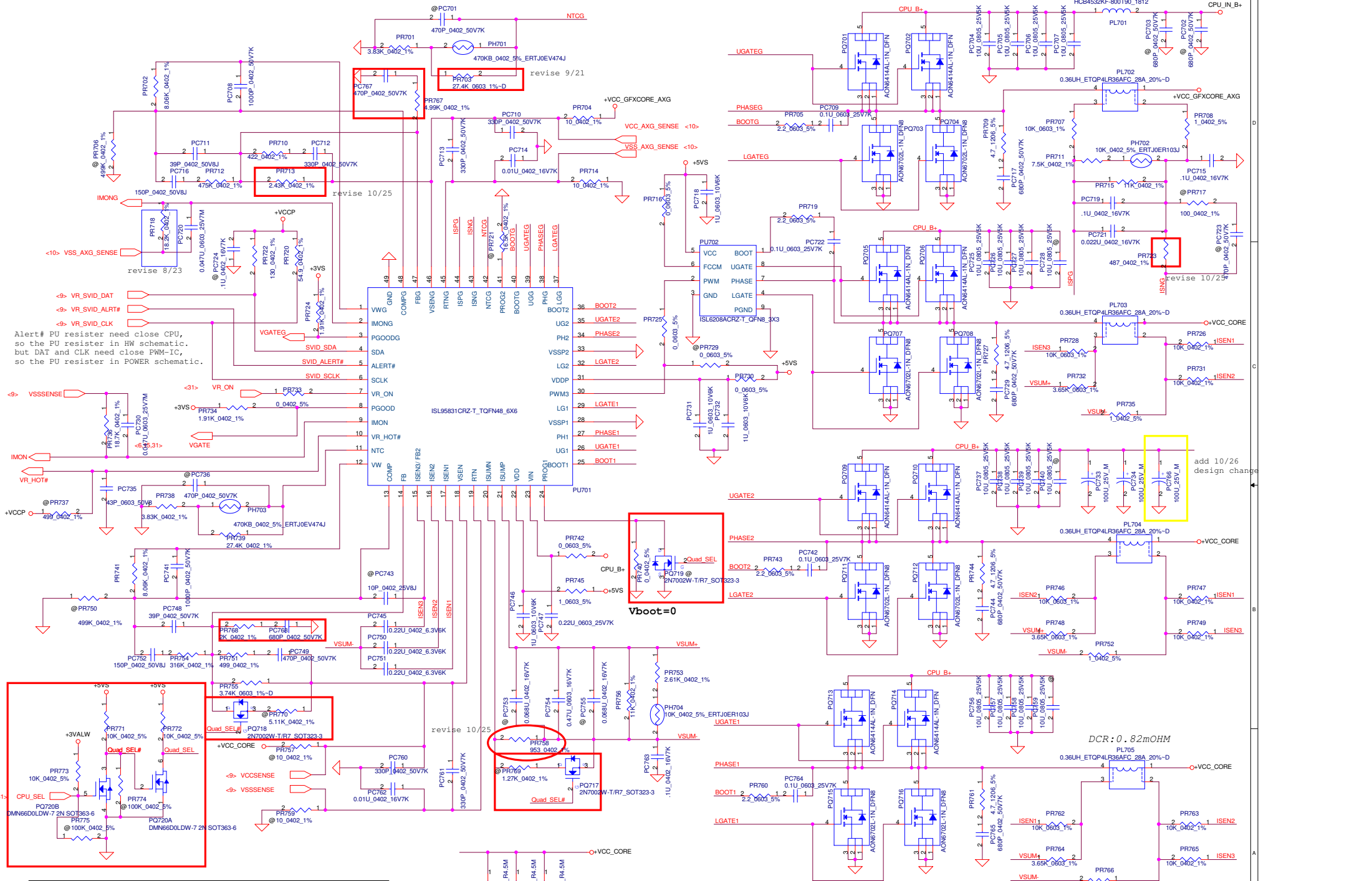
VCCPP
TDC 12.8 A
Peak Current 18.3 A
OCP current 22.4 A

Low Side MOS RDS(on)=2.6m ohm(Typ) , 3.2m ohm(Max)



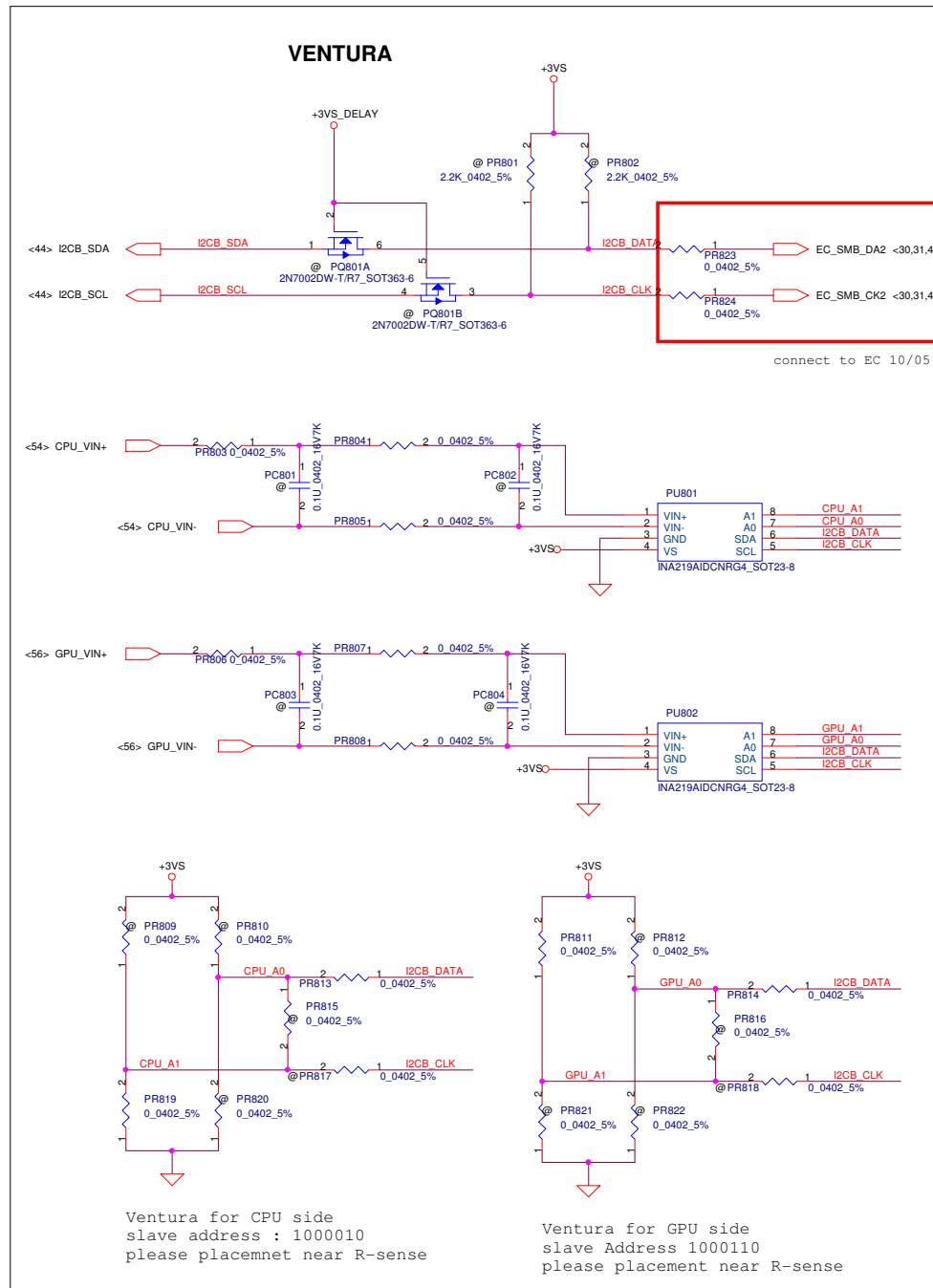
1.8VSP
TDC 1.25 A
Peak Current 1.75 A
OCP current 4 A





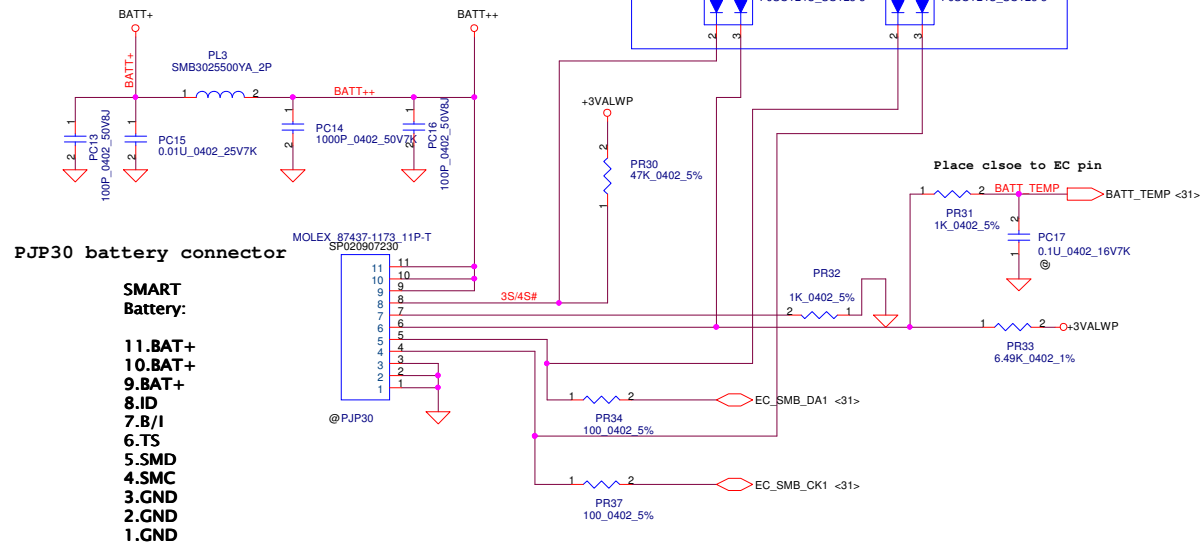
Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

Quad & Dual CORE selection						
CORE	CPU_SEL	Quad_SEL	Quad_SEL#	PR758//PR769	PR755//PR770	PROG1
Dual	L	L	H	TBD	TBD	4.32k
Quad (Default)	H	H	L	953	3.74k	0



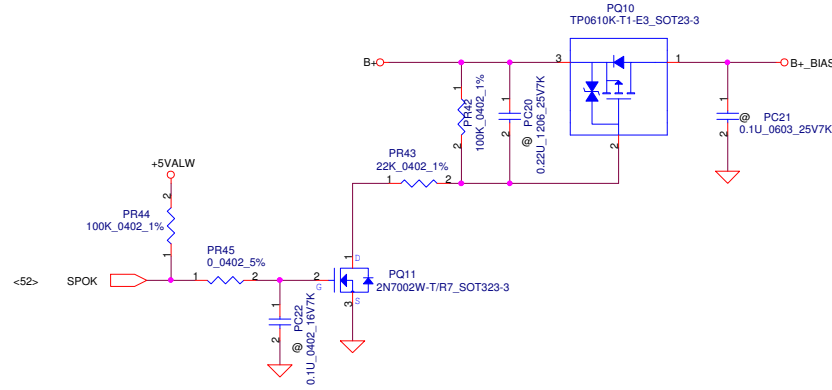
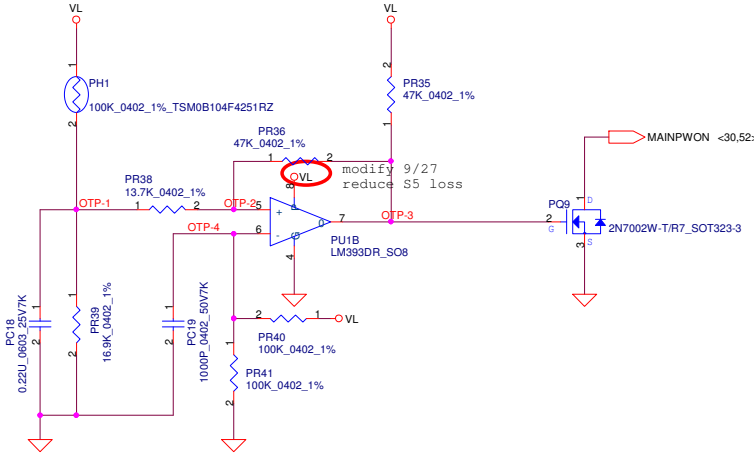
PJP30 battery connector

- SMART Battery:**
- 11.BAT+
 - 10.BAT+
 - 9.BAT+
 - 8.ID
 - 7.B/I
 - 6.TS
 - 5.SMD
 - 4.SMC
 - 3.GND
 - 2.GND
 - 1.GND



Battery Connect/OTP

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



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