

MODEL NAME : *PALB0*
PCB NO : *LA-6801P (DAB00000410)*
BOM P/N : *46198531L01 -->R3*
46198531L02 -->R1
46198531L03 -->R3
46198531L04 -->R1

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Schematic Document

Specter (Huron River)

Sandy Bridge(PGA) + Cougar Point(standard)

DISCRETE VGA N12E-GE-B (optimus)

2011-01-25

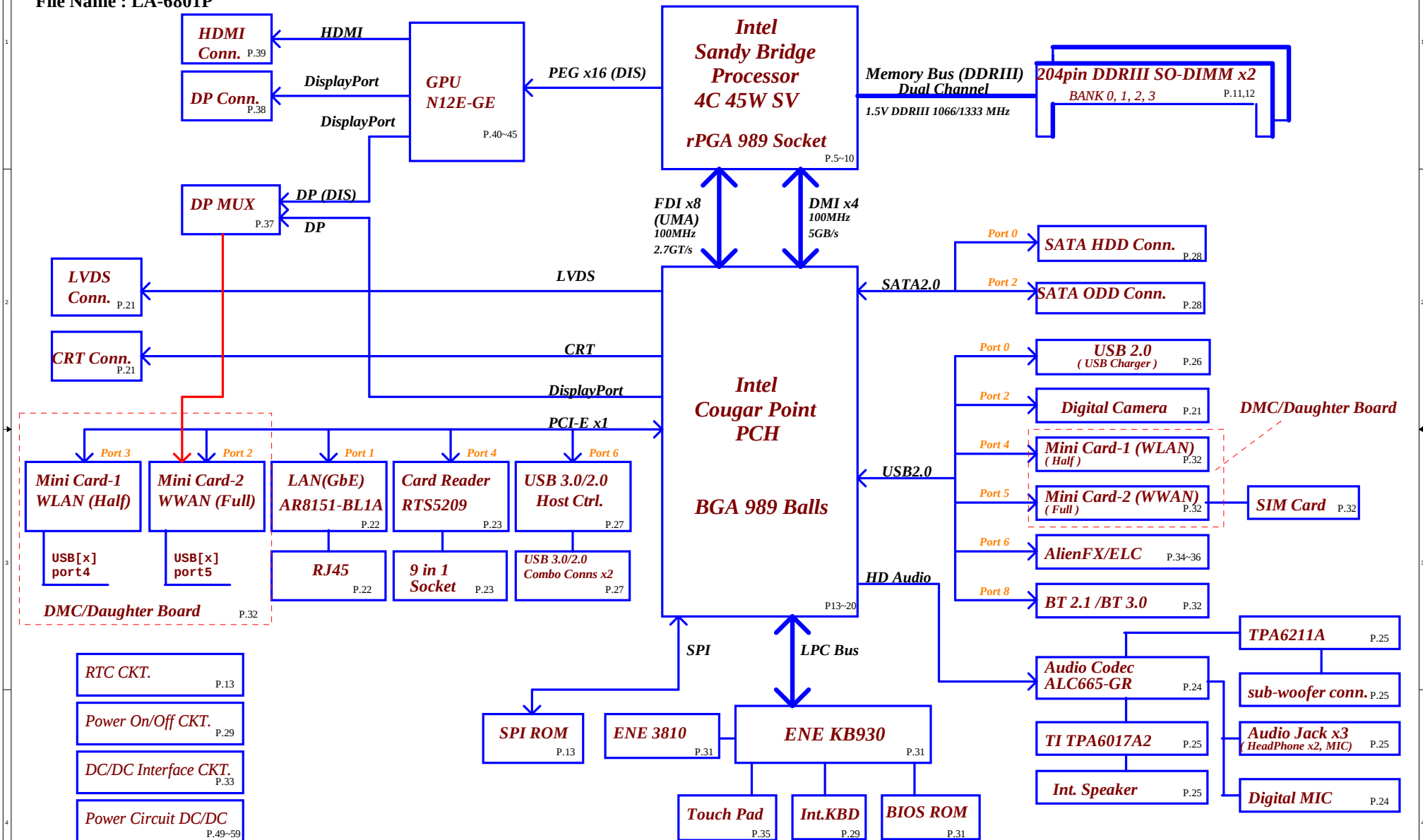
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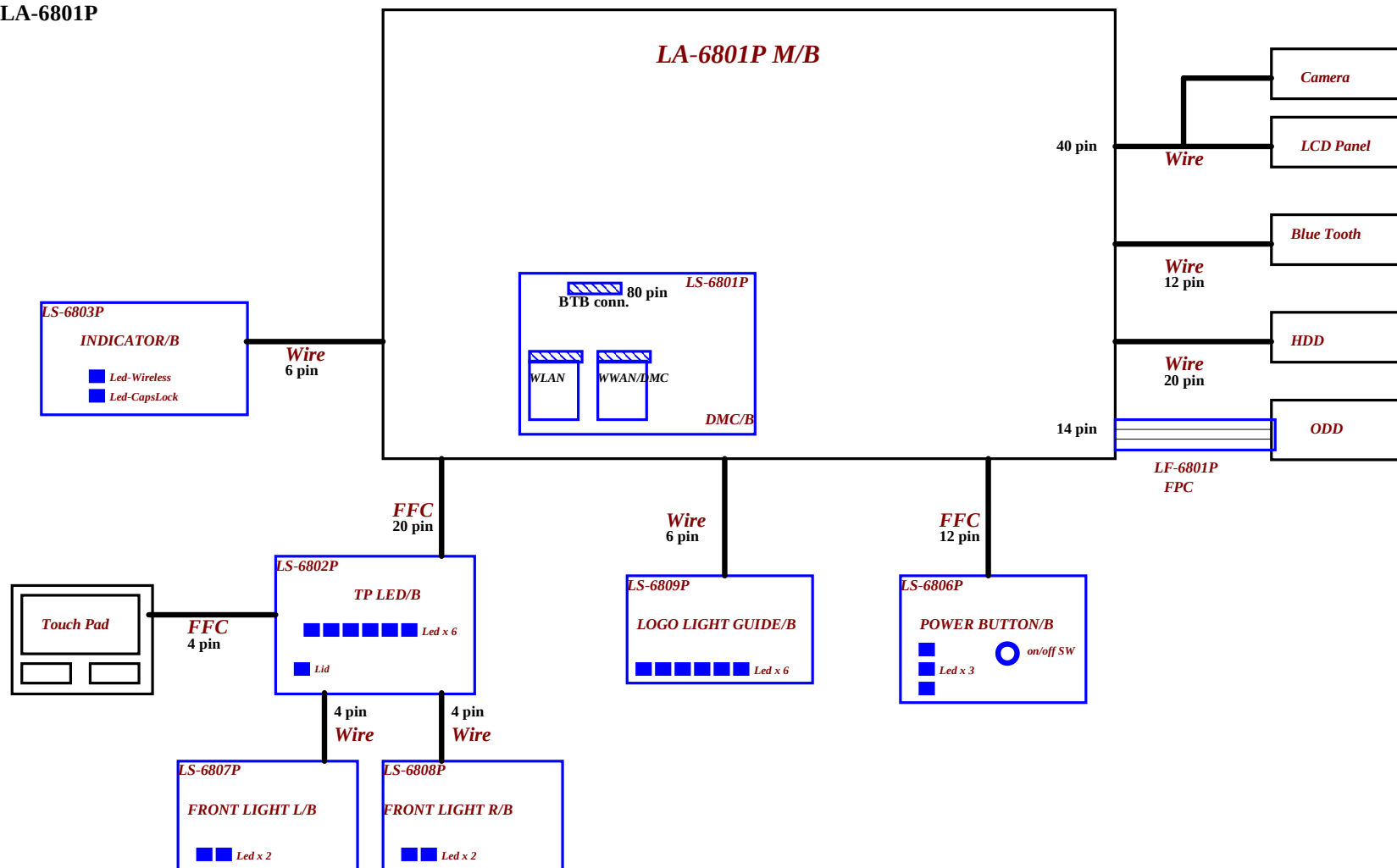


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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

PCH

USB PORT#	DESTINATION
0	None
1	JUSB1 (2.0 Ext Left Side)
2	Bluetooth
3	CAMERA
4	JMINI1 (WLAN)
5	JMINI2 (WWAN/DMC)
6	ELC 8051
7	None
8	None
9	None
10	None
11	None
12	None
13	None

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

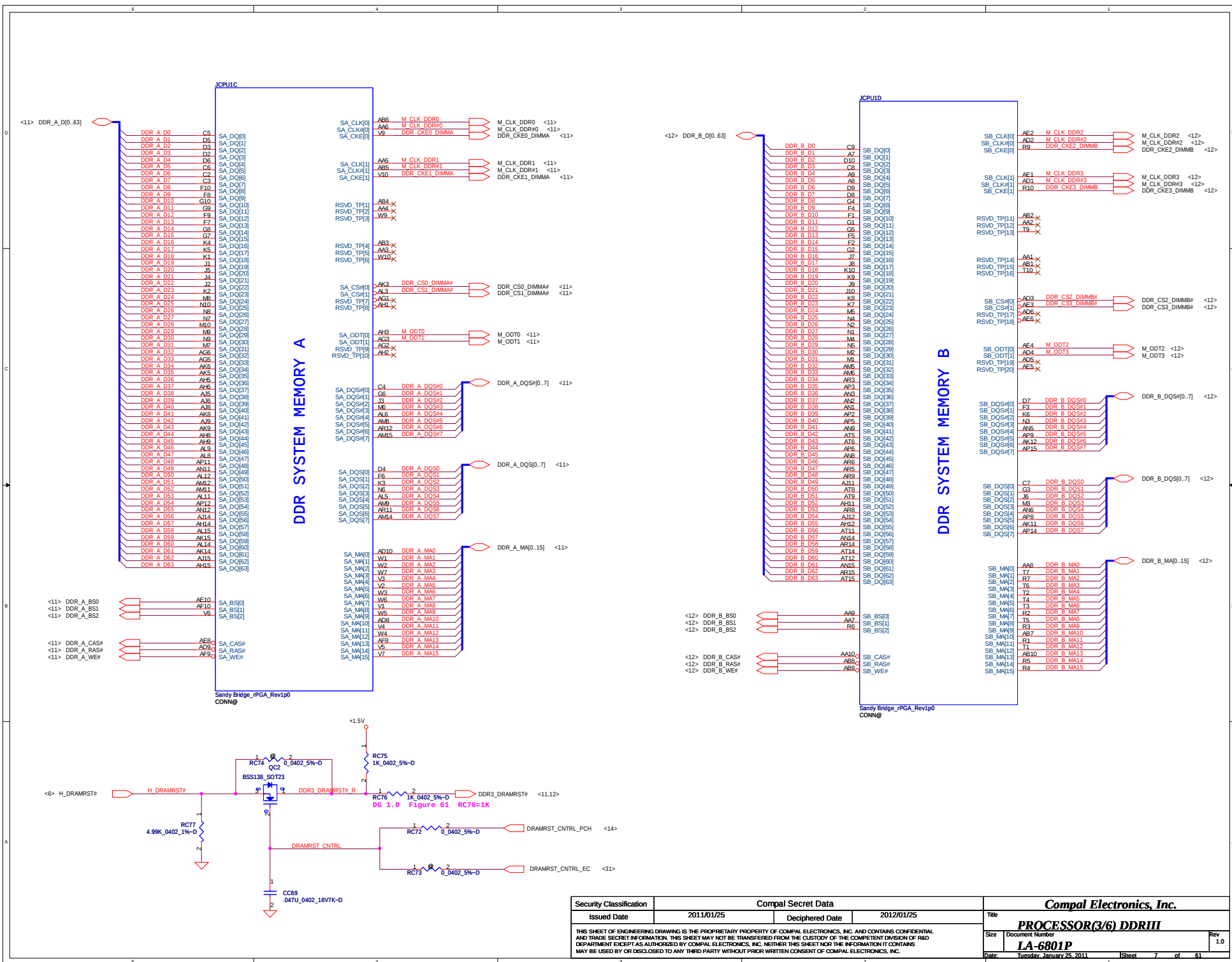
SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

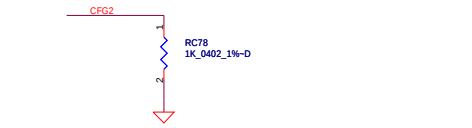
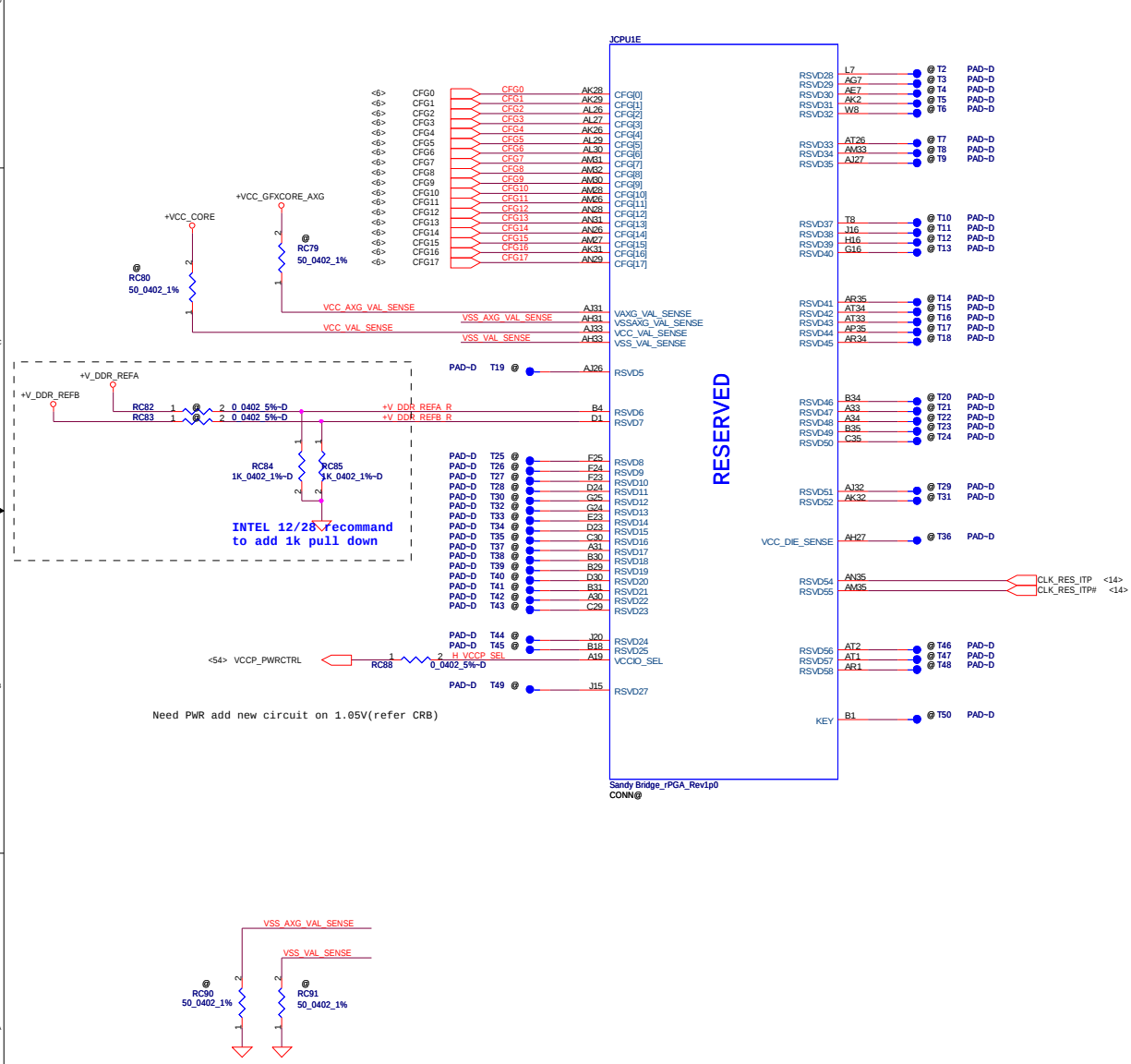
Symbol Note :



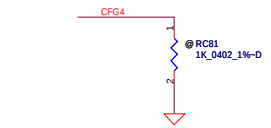
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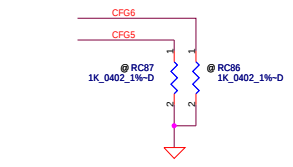
CFG Straps for Processor



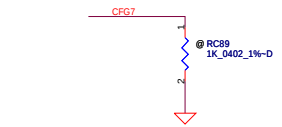
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

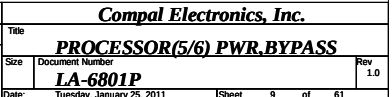


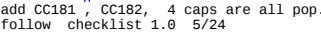
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



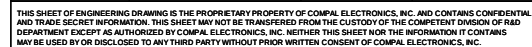
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

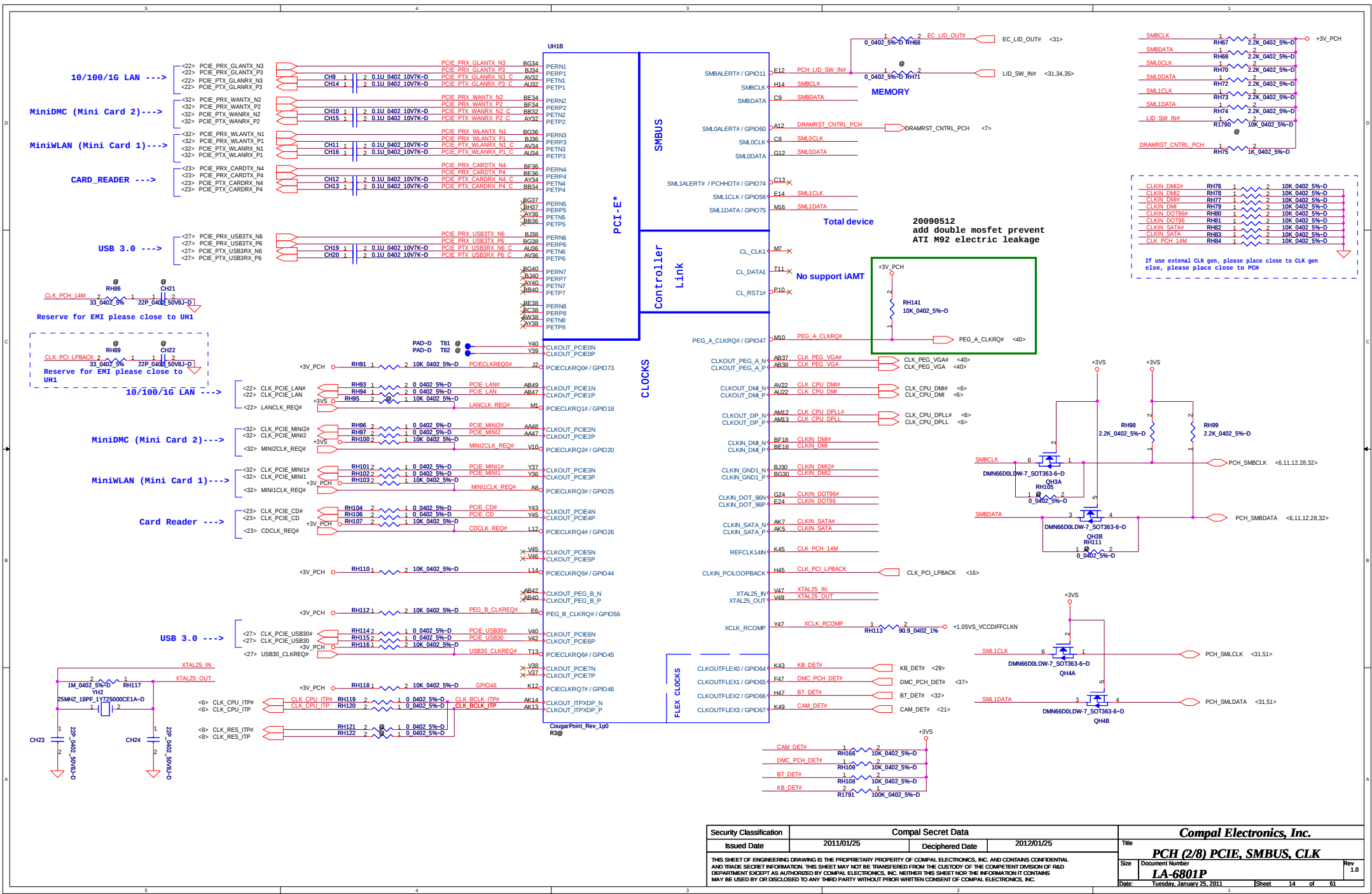
INTEL 12/28 recommend to add RC120, RC121, RC122, RC123 Please place as close as JCPU1



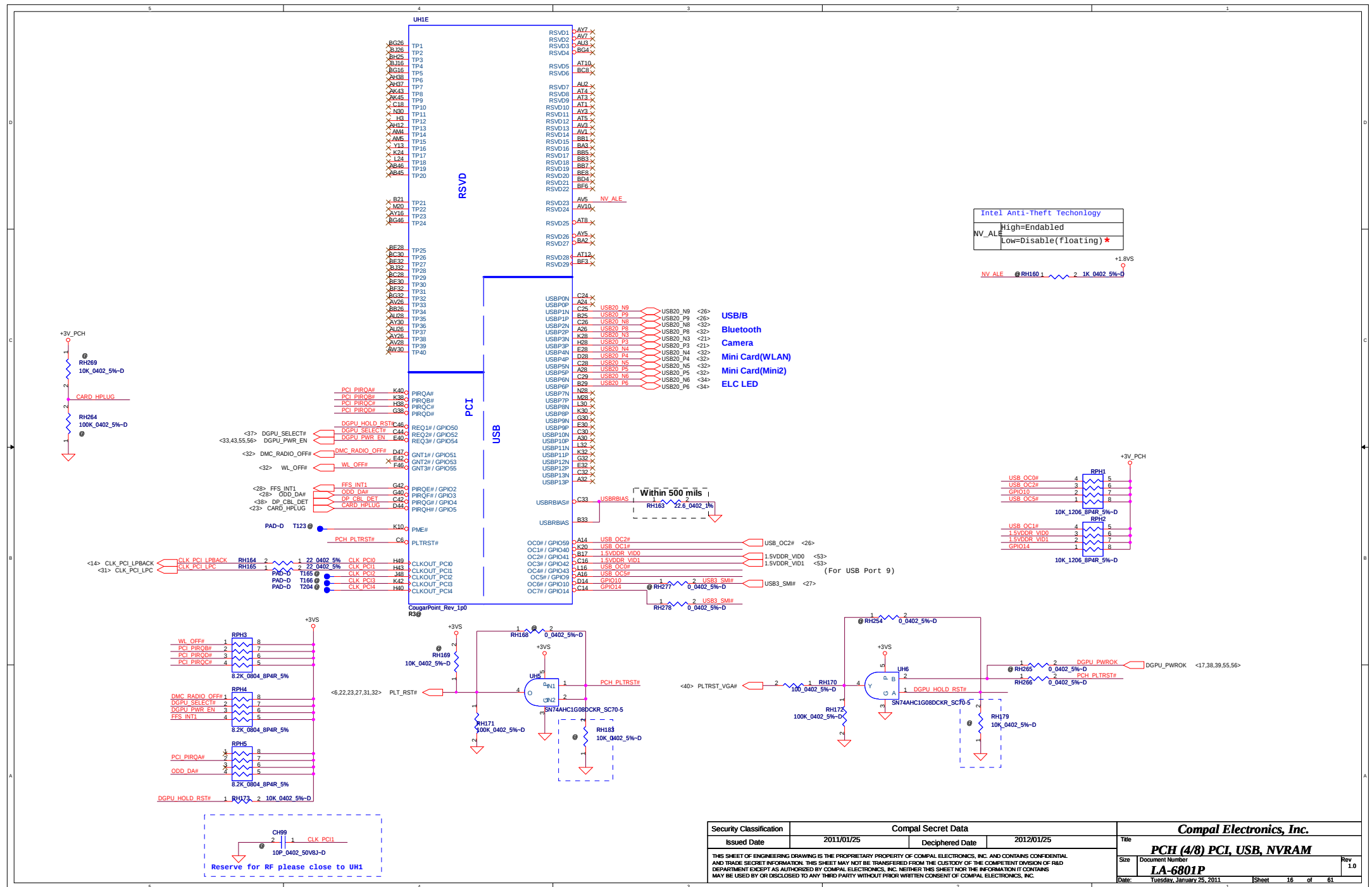


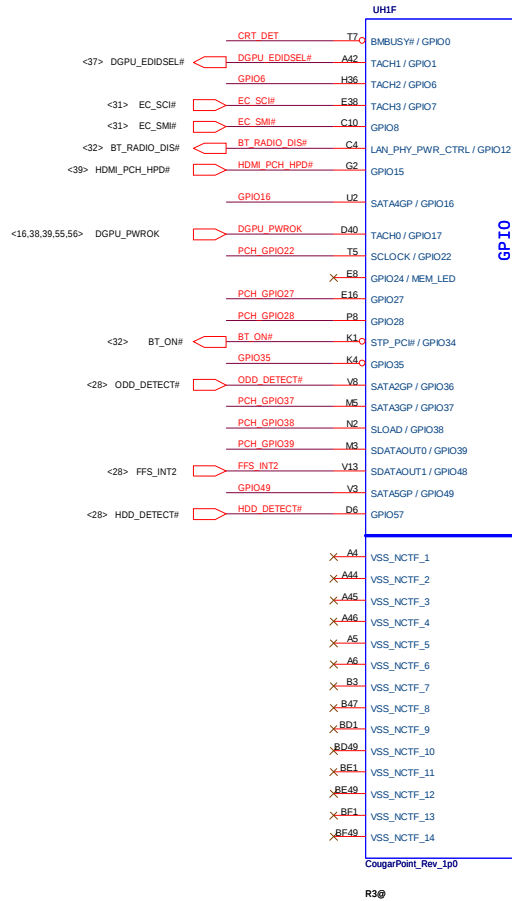
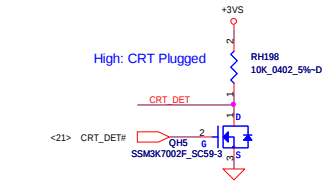
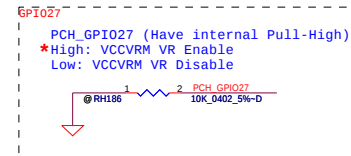
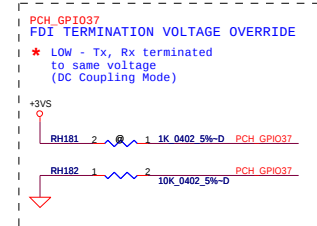
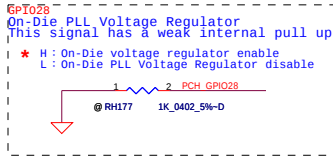
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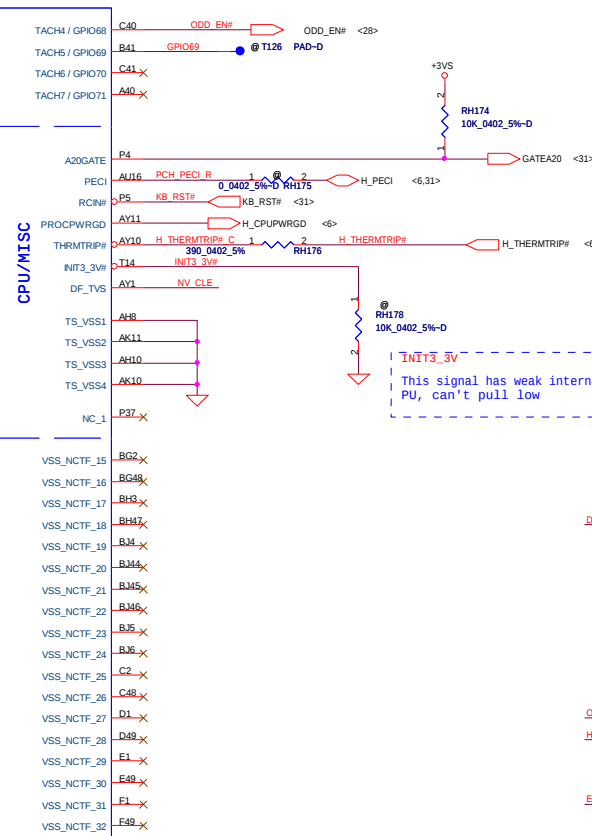


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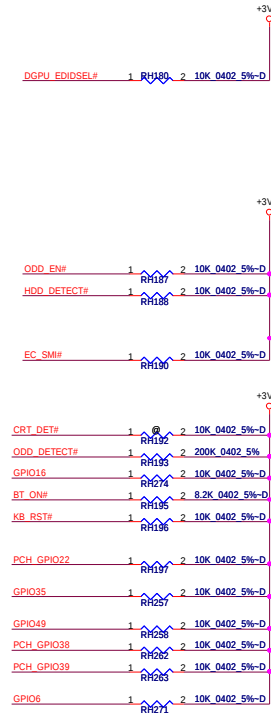
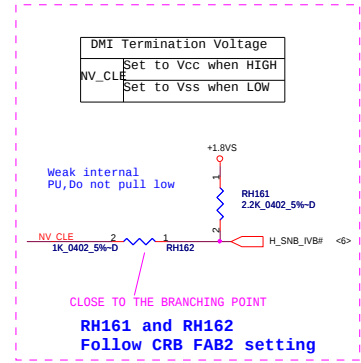




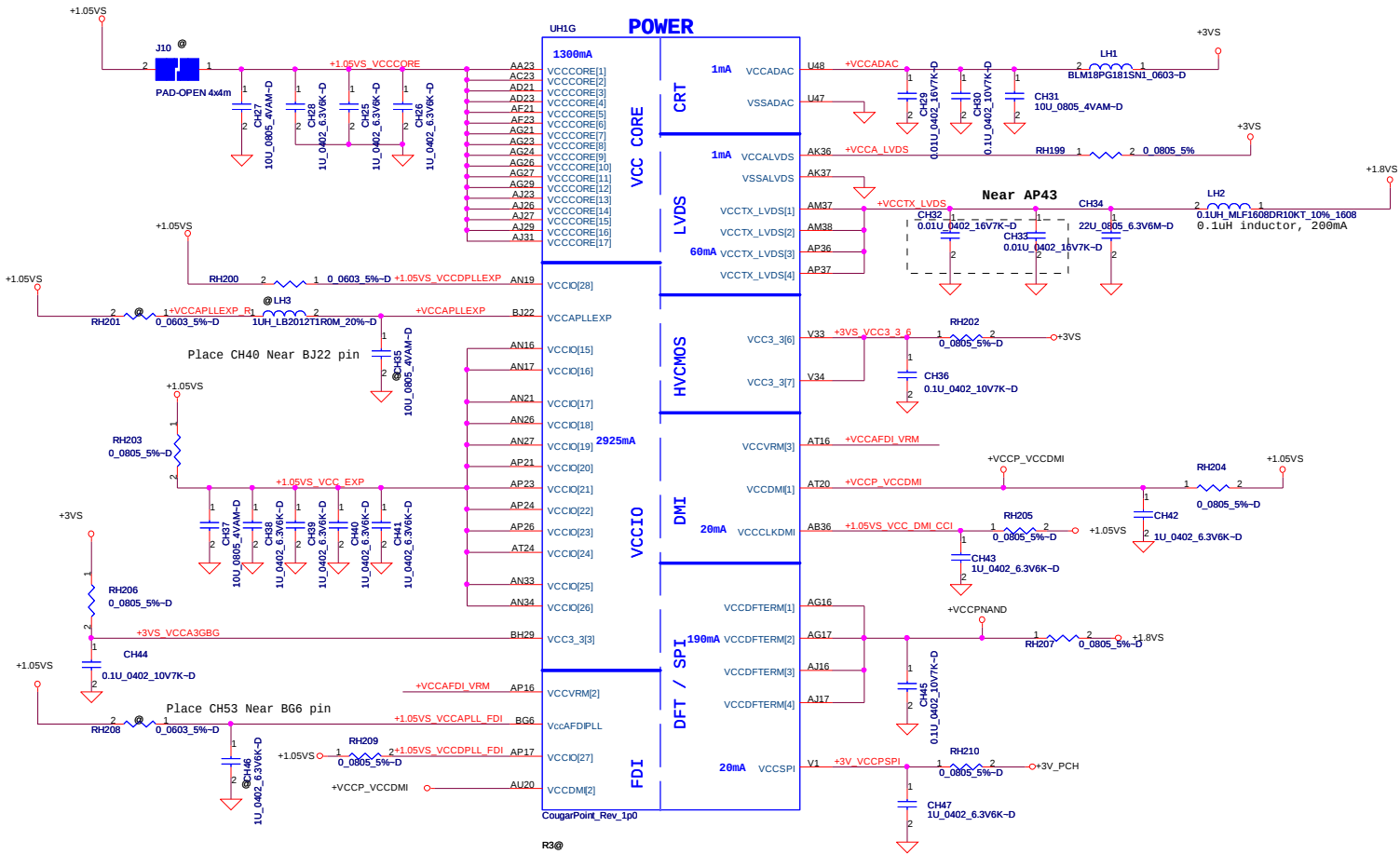
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5



INIT3_3V
This signal has weak internal
PU, can't pull low

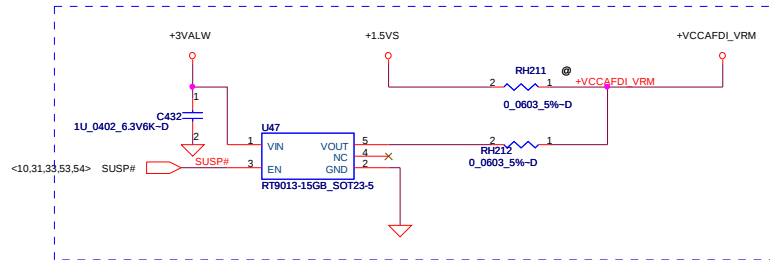


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				PCH (5/8) GPIO, CPU, MISC			
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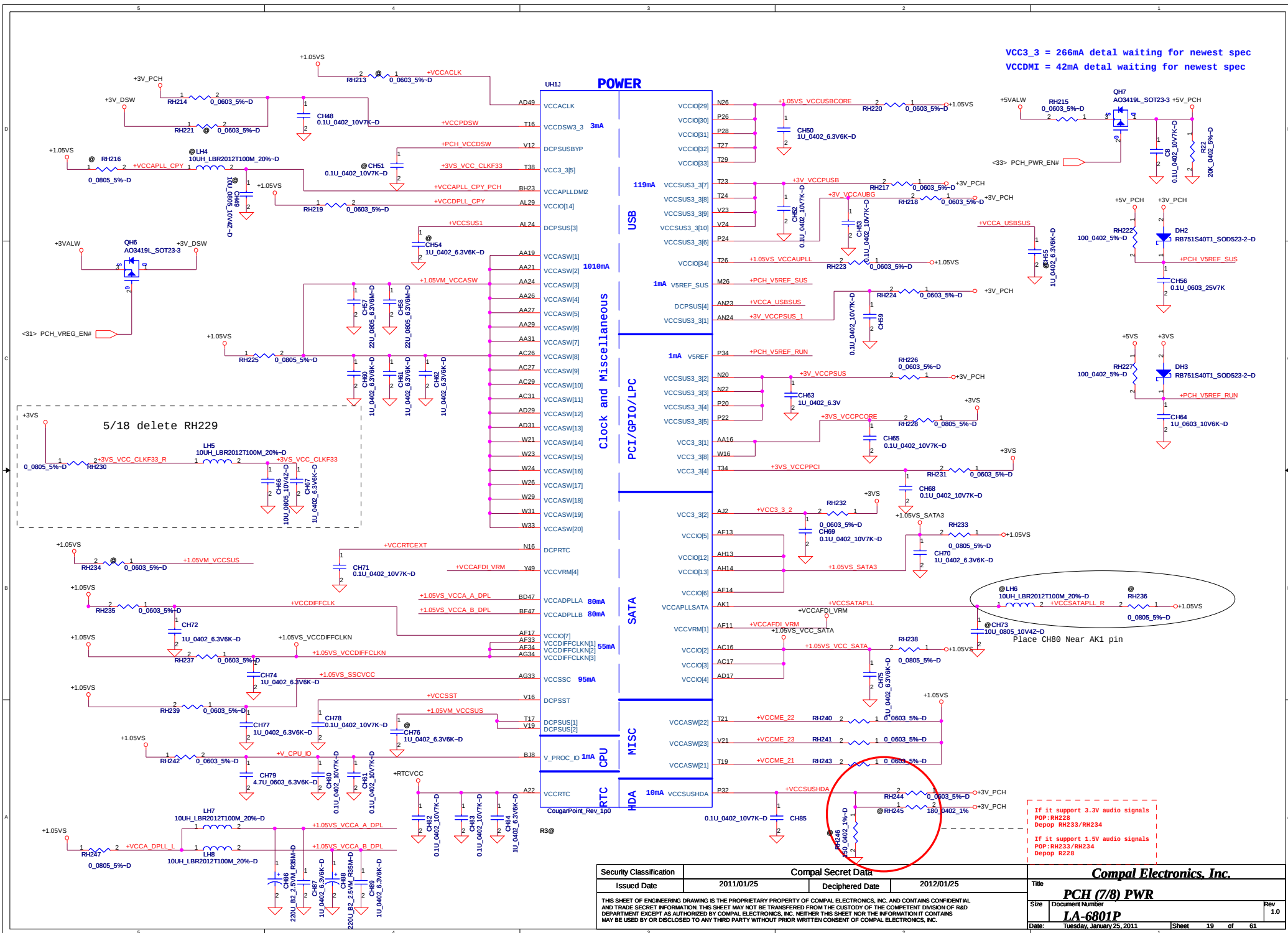


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detail waiting for newest spec



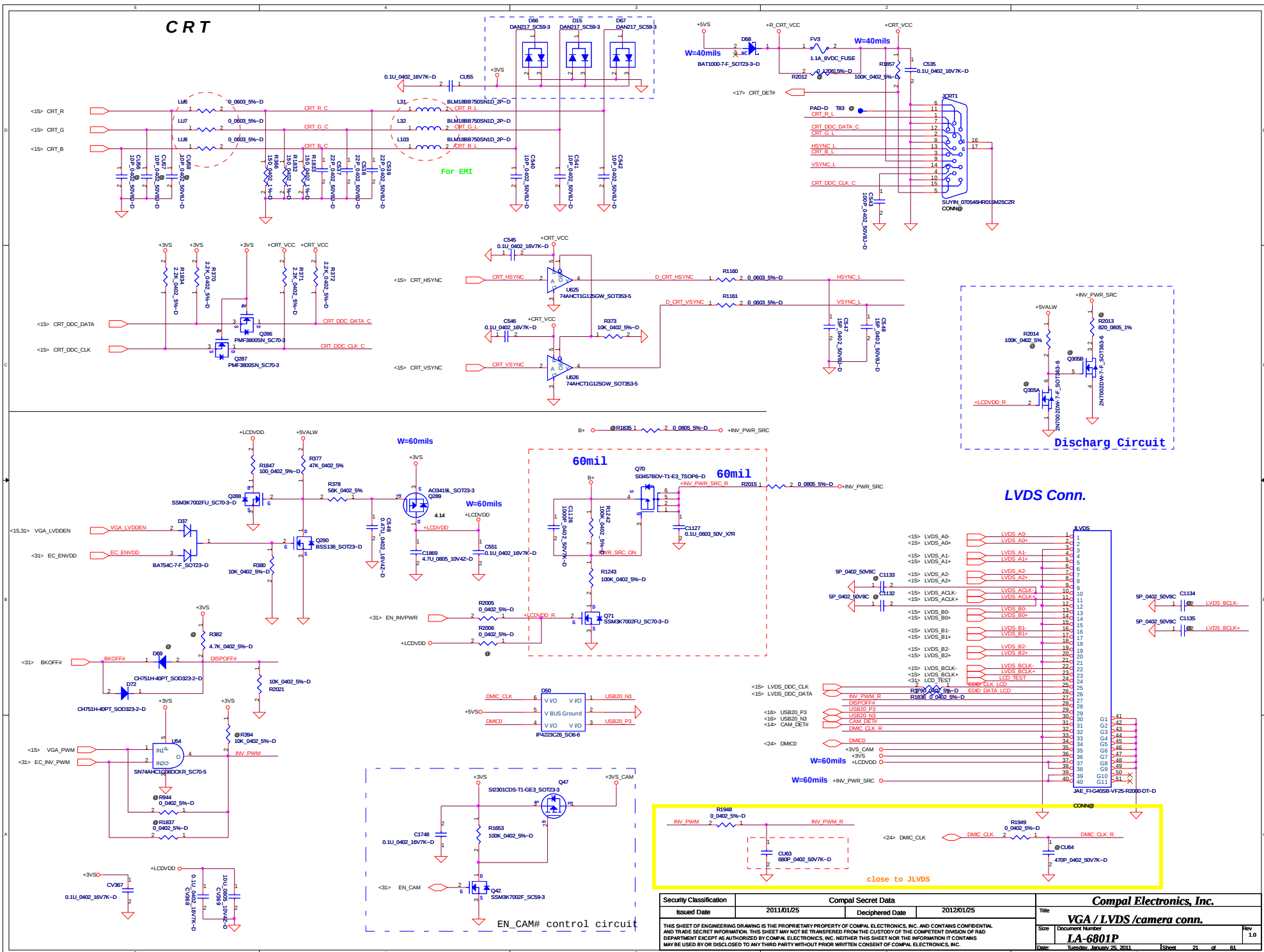
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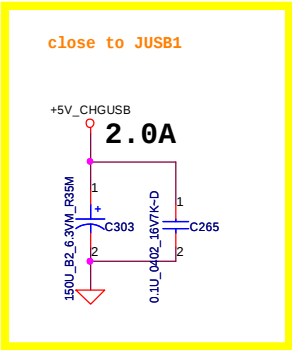
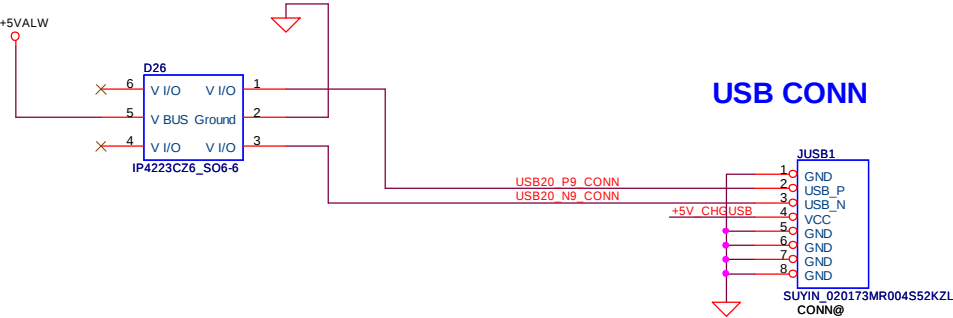
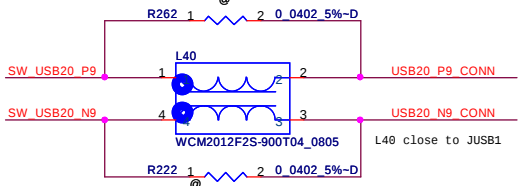
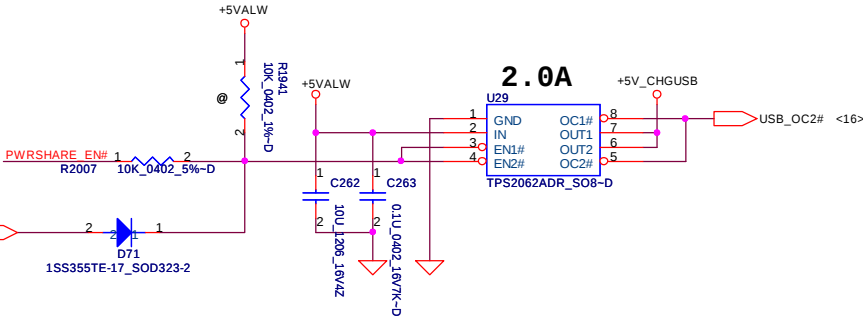
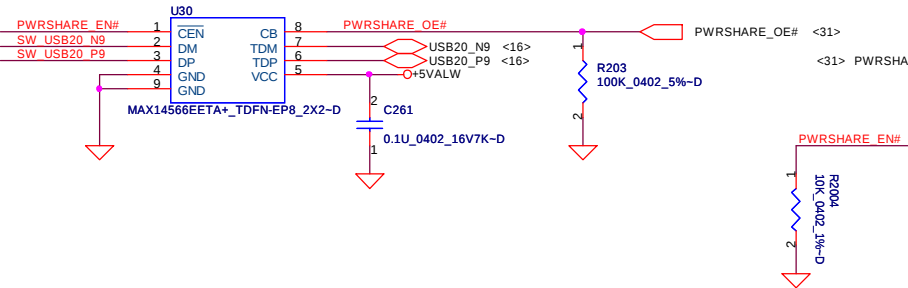
CRT



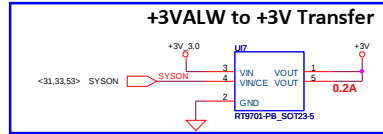
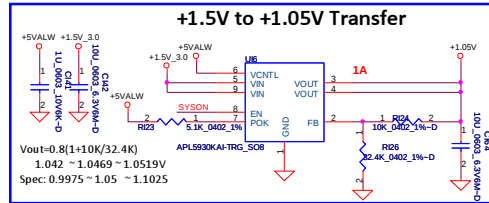
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Power share

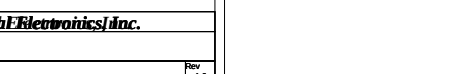
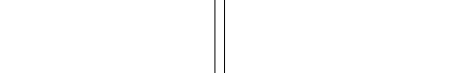
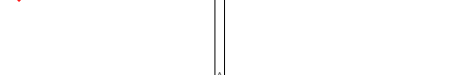
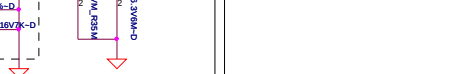
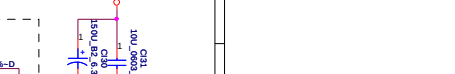
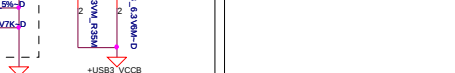
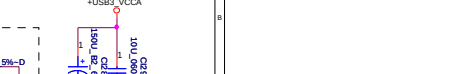
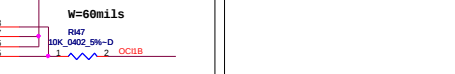
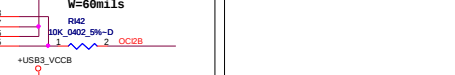
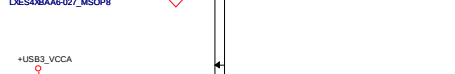
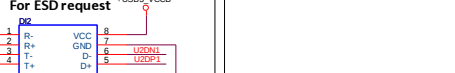
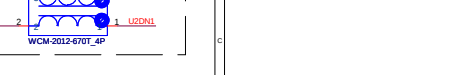
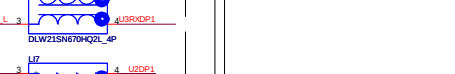
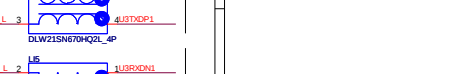
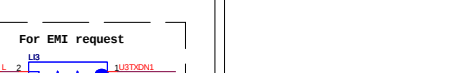
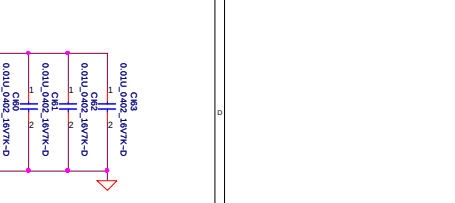
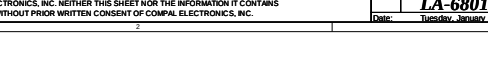
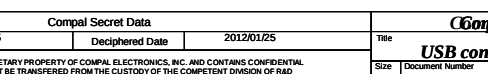
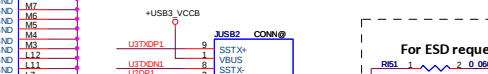
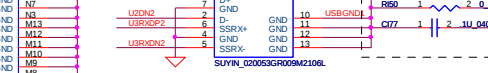
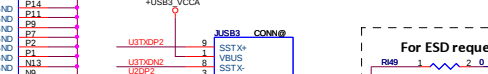
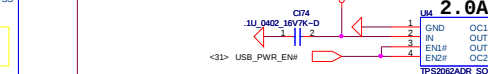
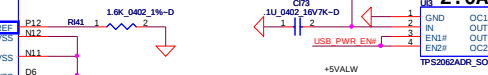
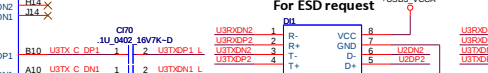
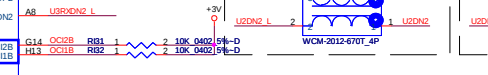
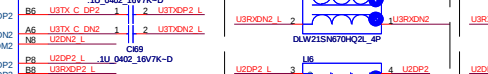
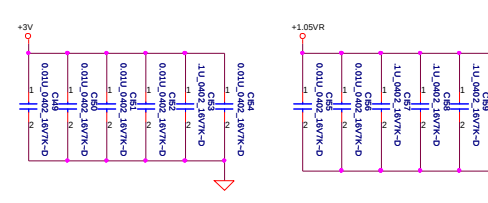
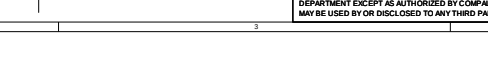
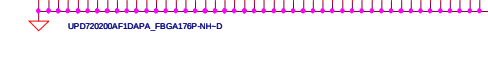
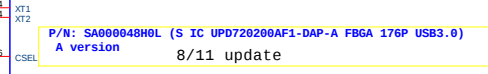
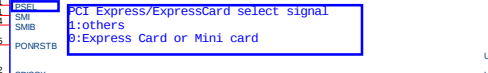
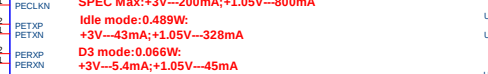
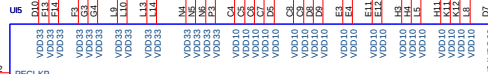
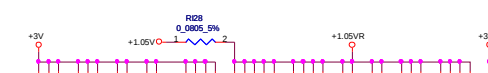
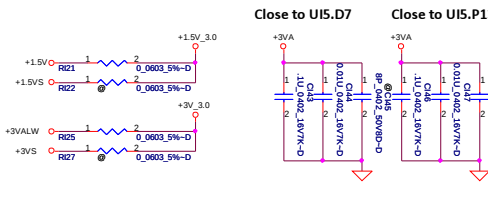
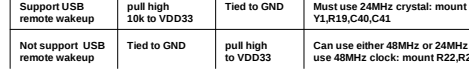
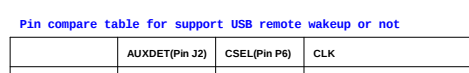
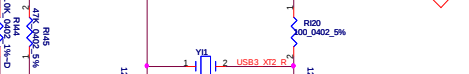
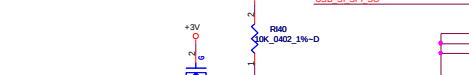
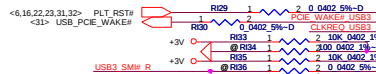
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



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- <14> CLK_PCIE USB30
- <14> CLK_PCIE USB30#
- <14> PCIE_PRX_USB3TX_P6
- <14> PCIE_PRX_USB3TX_N6
- <14> PCIE_PTX_USB3RX_P6
- <14> PCIE_PTX_USB3RX_N6



SPEC Max: +3V--200mA; +1.05V--800mA
 Idle mode: 0.489W;
 +3V--43mA; +1.05V--328mA
 D3 mode: 0.066W;
 +3V--5.4mA; +1.05V--45mA

can be attach to EC, either.

PCIE Express/Expresscard select signal
 1: others
 0: Express Card or Mini card

As short as possible

P/N: SA000048H0L (S IC UPD720200AF1-DAP-A FBGA 176P USB3.0)
 A version 8/11 update

Place as close as
 possible to
 UI5.N14 and UI5.M14

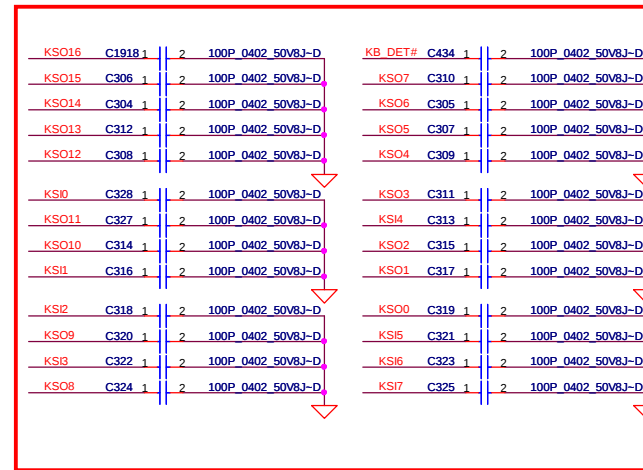
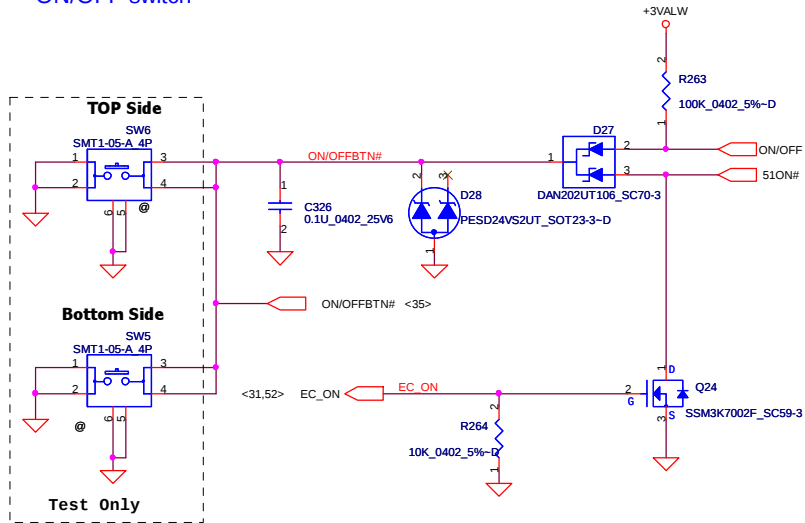
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

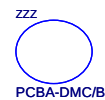
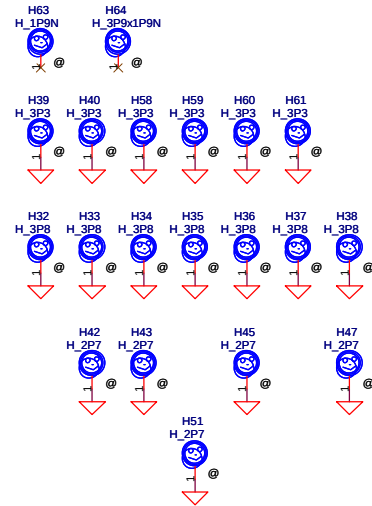
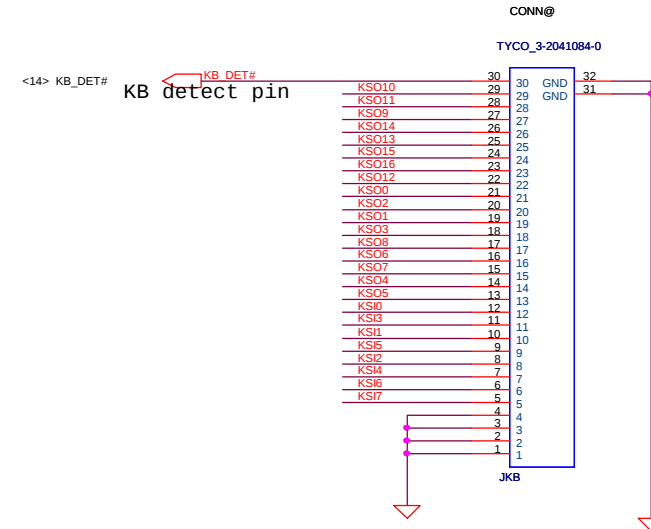
Security Classification	Compal Secret Data		Title	
Issued Date	201101/25	Deciphered Date	201201/25	USB conn.
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ON/OFF switch

Power Button



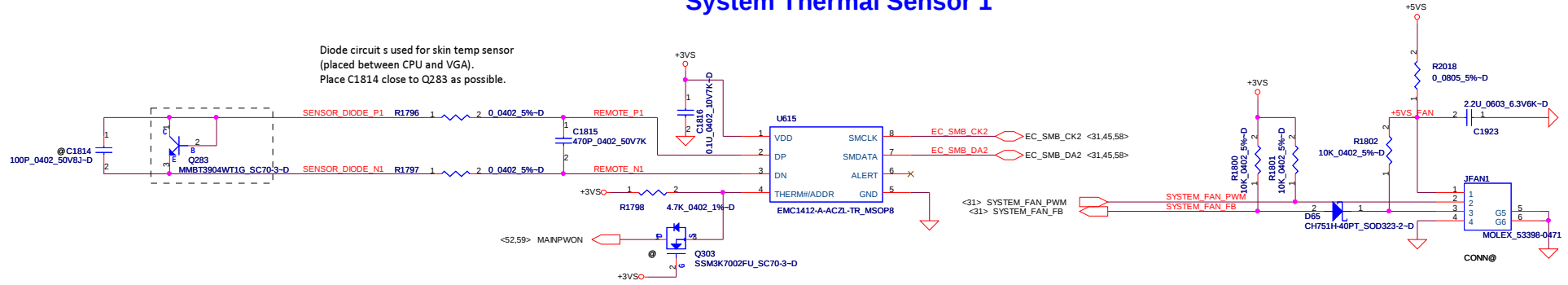
INT_KBD Conn.



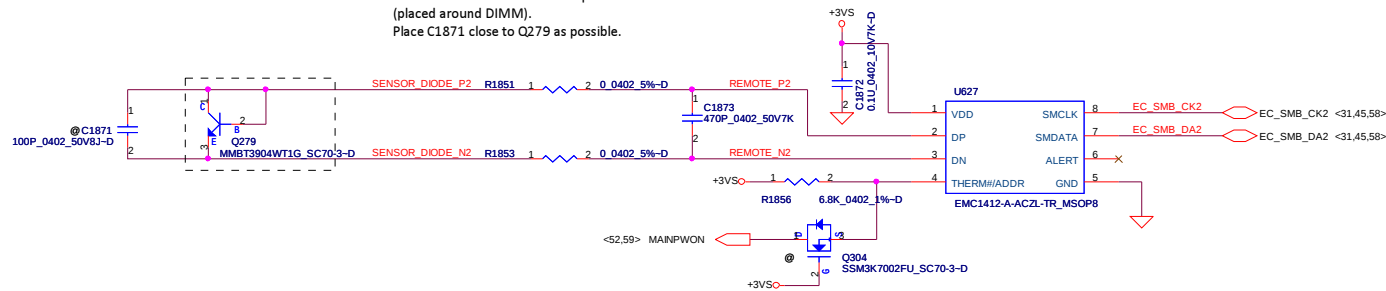
45@

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				Date:	Tuesday, January 25, 2011
				Sheet	29 of 61
				Rev	1.0

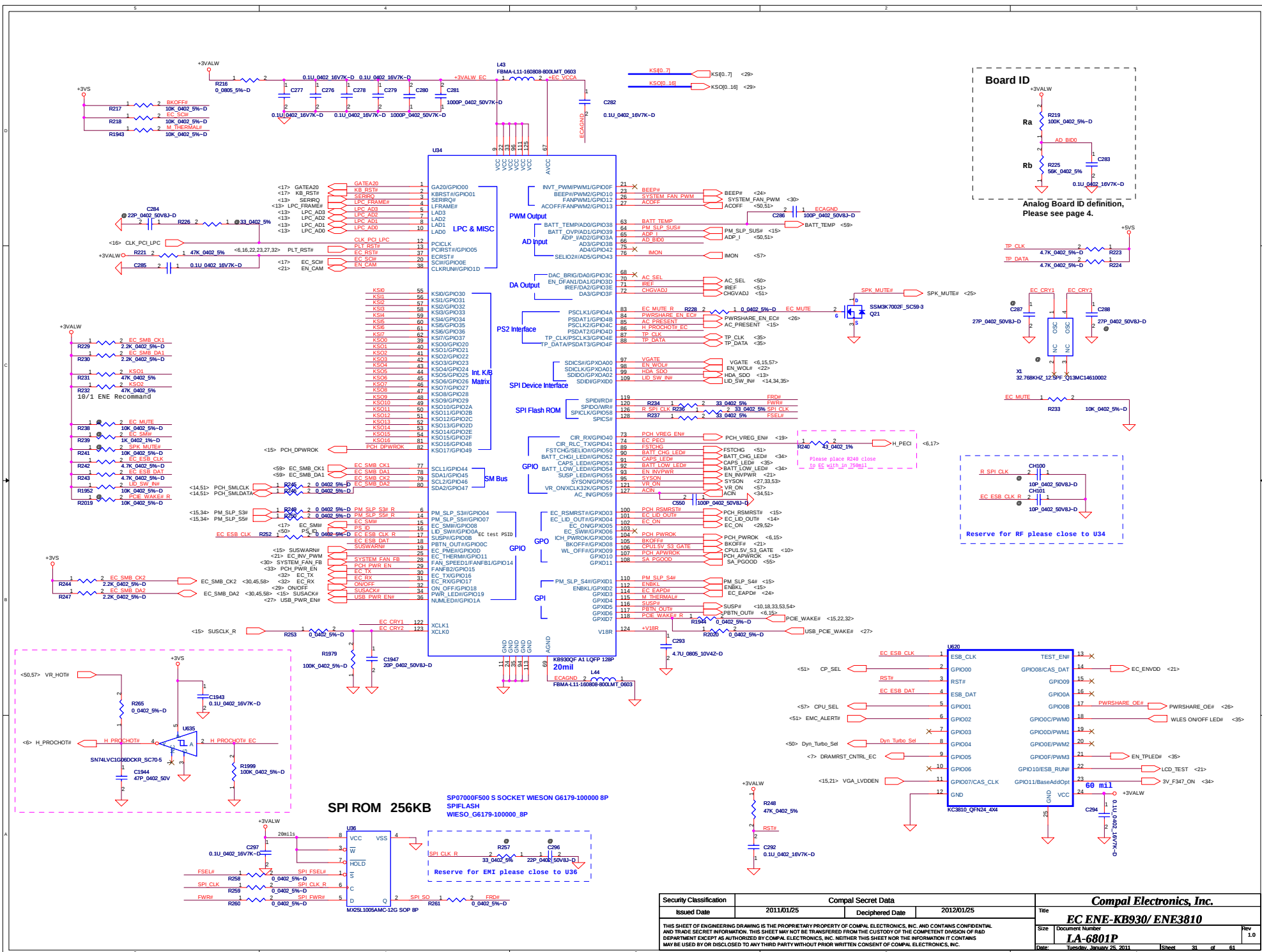
Diode circuit s used for skin temp sensor
(placed between CPU and VGA).
Place C1814 close to Q283 as possible.



Diode circuit s used for skin temp sensor (placed around DIMM).
Place C1871 close to Q279 as possible.

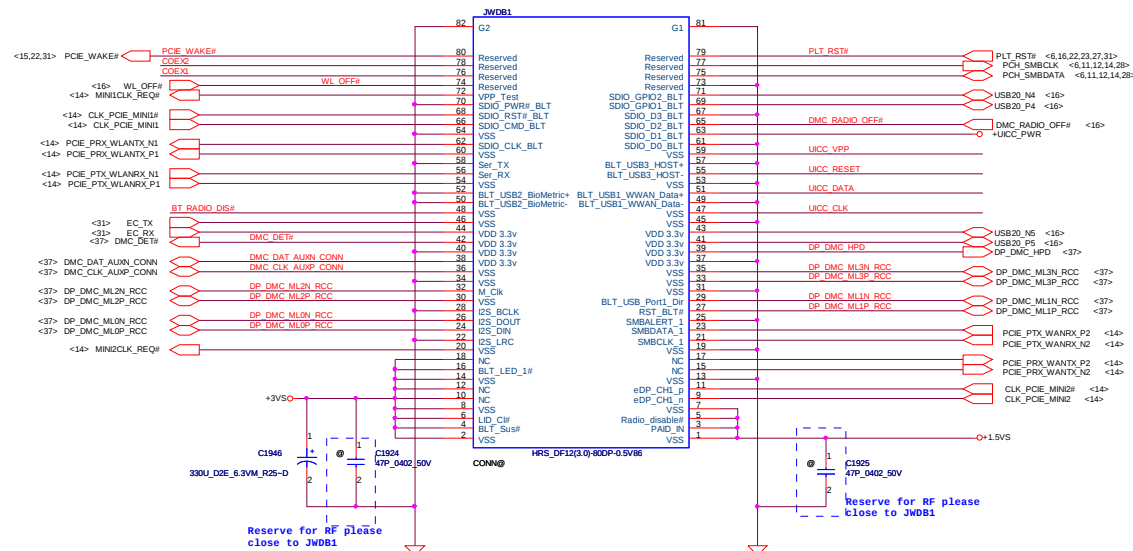


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				LA-6801P		
				Date:	Tuesday, January 25, 2011	Sheet

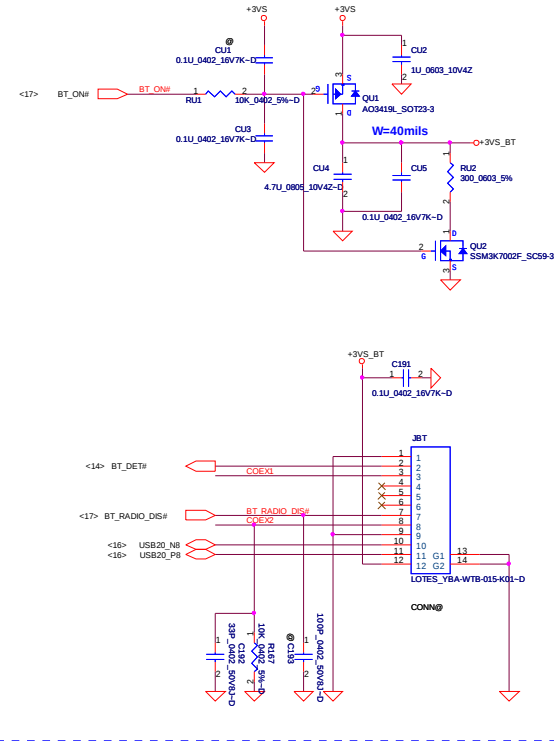


Security Classification	Compal Secret Data		Title	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Size
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			Documents Number LA-6801P	
			Date: <u>January 25, 2011</u> Sheet <u>31</u> of <u>61</u>	

To DMC PCB connector

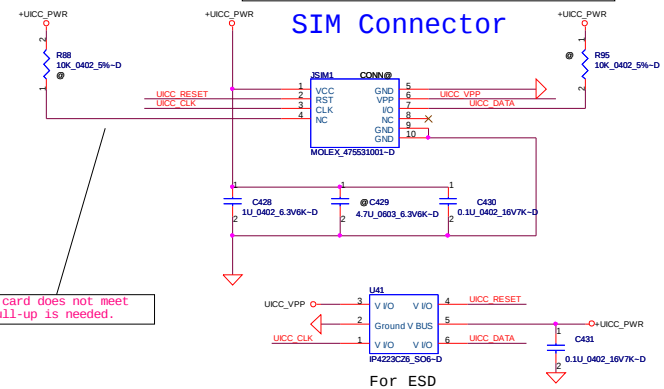


BlueTooth



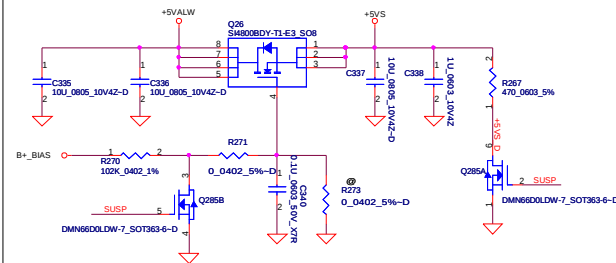
SIM card board 4.7uF change to 1uF for Tiger detect issue.

SIM Connector

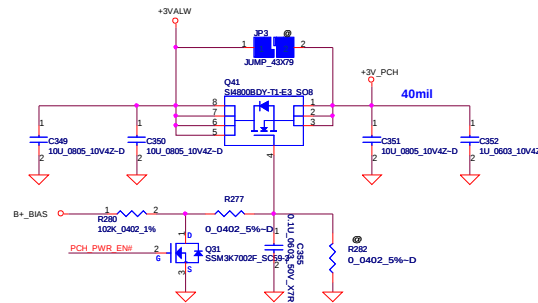
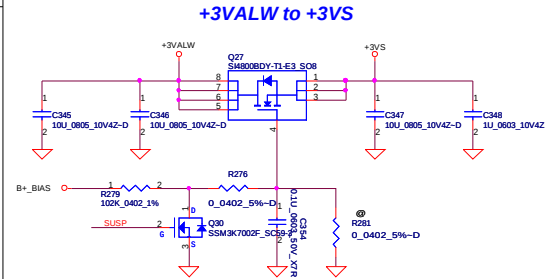


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Issued Date	2011/01/25	Deciphered Date	2012/01/25	Mini Card - WLAN / DMC / BT
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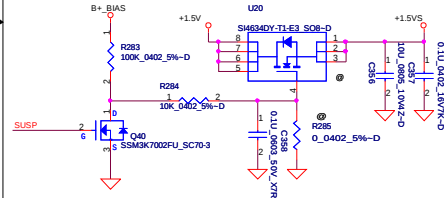
+5VALW to +5VS



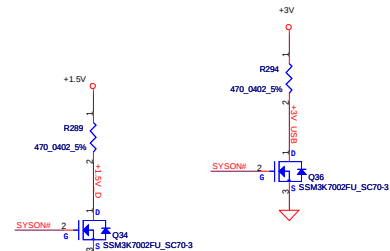
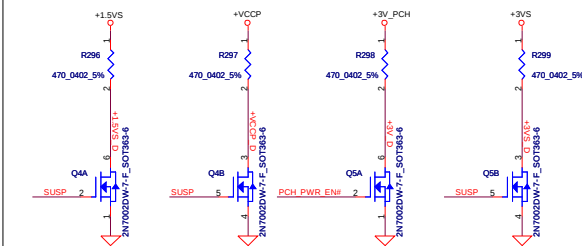
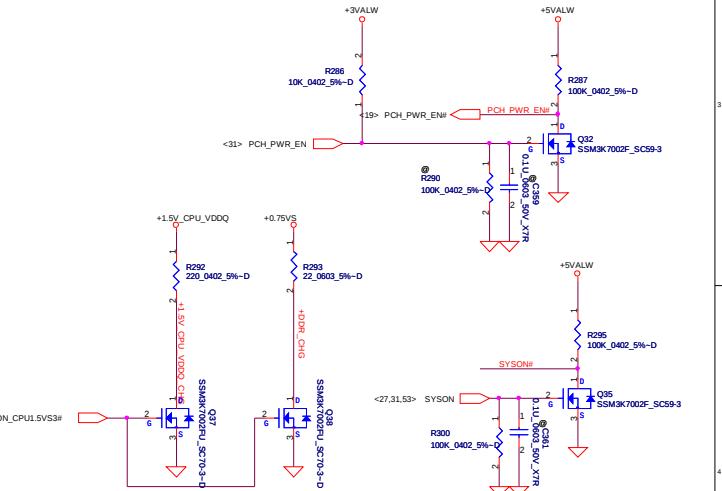
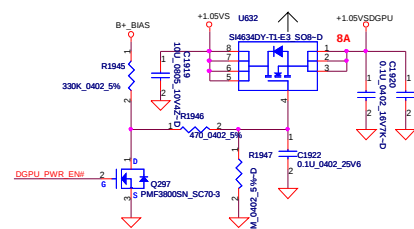
+3VALW to +3V_PCH



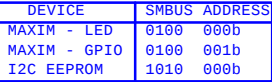
+1.5V To +1.5VS



+1.05V to +1.05VSDGPU Transfer



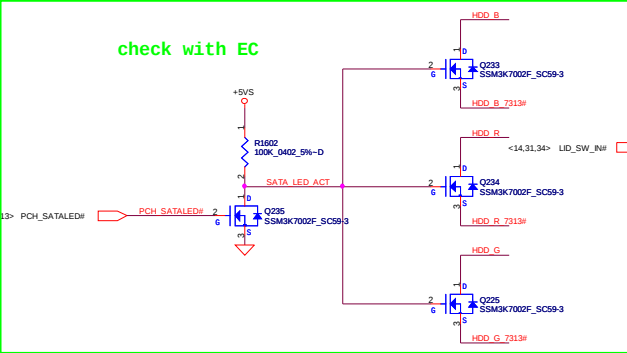
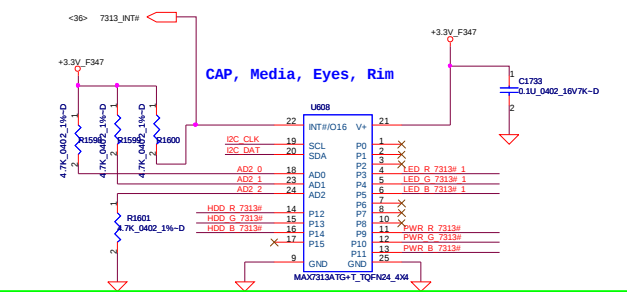
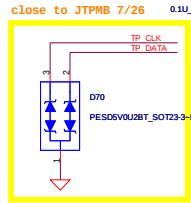
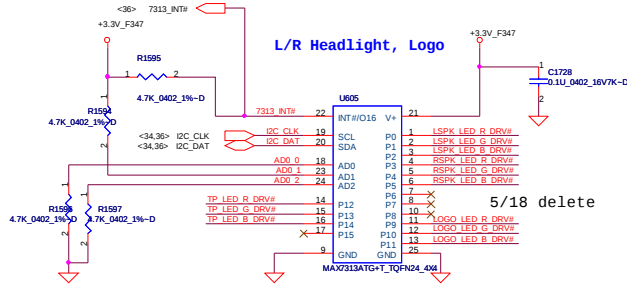
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Issued Date	2011/01/25	Deciphered Date	2012/01/25	Size	Document Number
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Date: Tuesday, January 25, 2011				Sheet	33 of 61



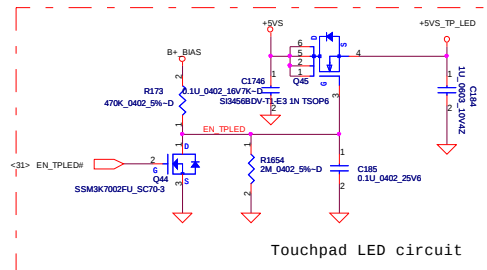
AC mode battery full in S5:turn off ELC controller

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				Date:	Tuesday, January 25, 2011
				Sheet	34 of 61

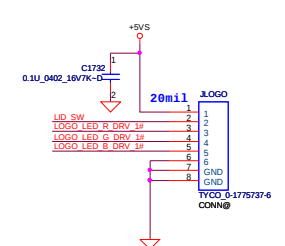
Touchpad LED CONN



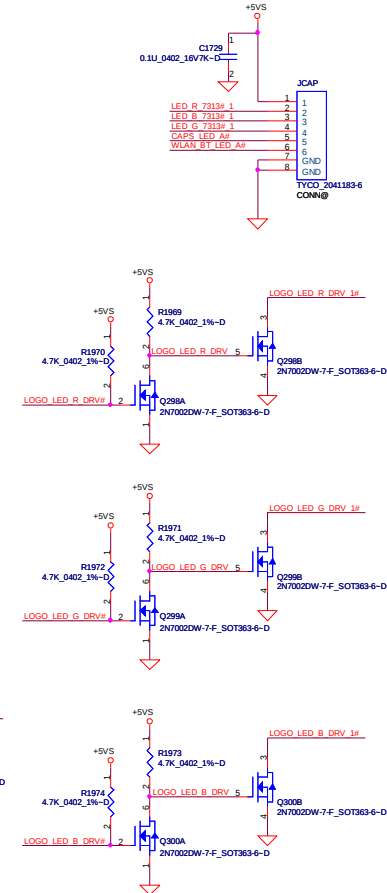
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight , Logo, TP
U608	0	1	1	Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim



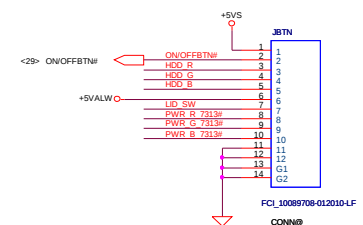
LOGO Board CONN



Indicator CONN

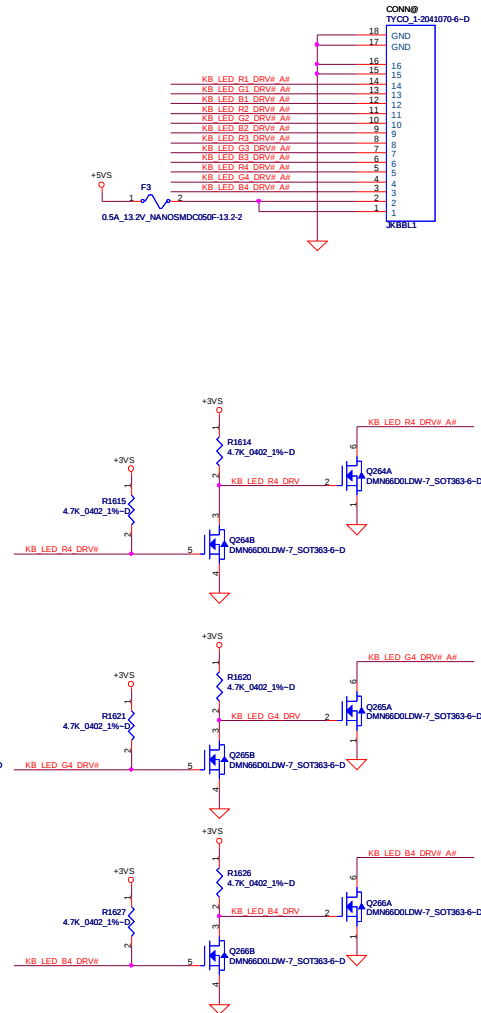
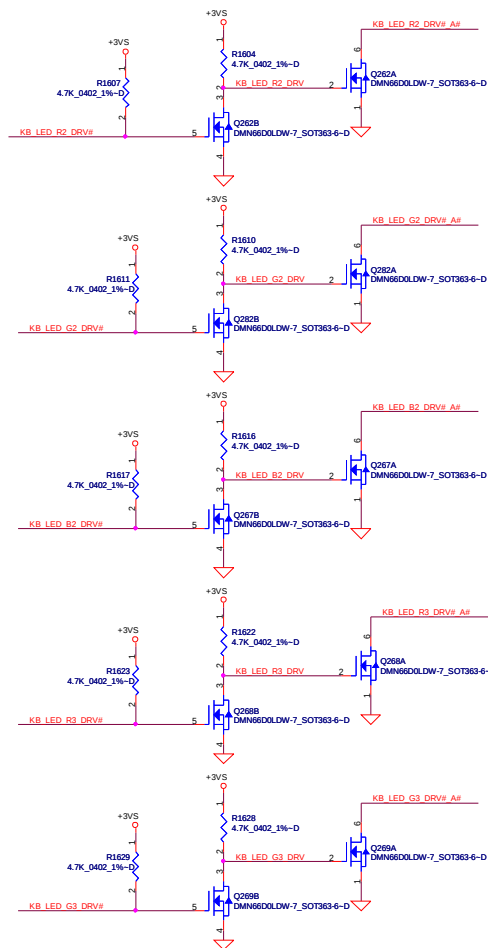


PWR BTN Board CONN



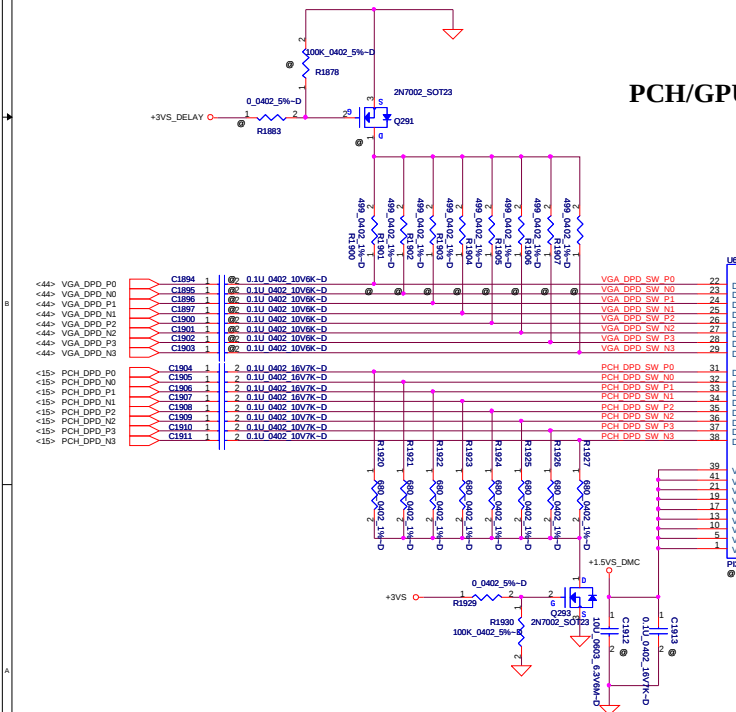
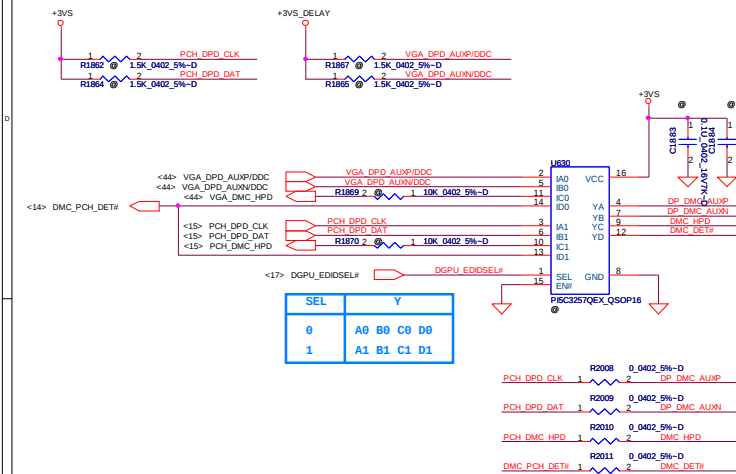
Security Classification	Compal Secret Data		Title	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	ELC (2)
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K/B Backlight

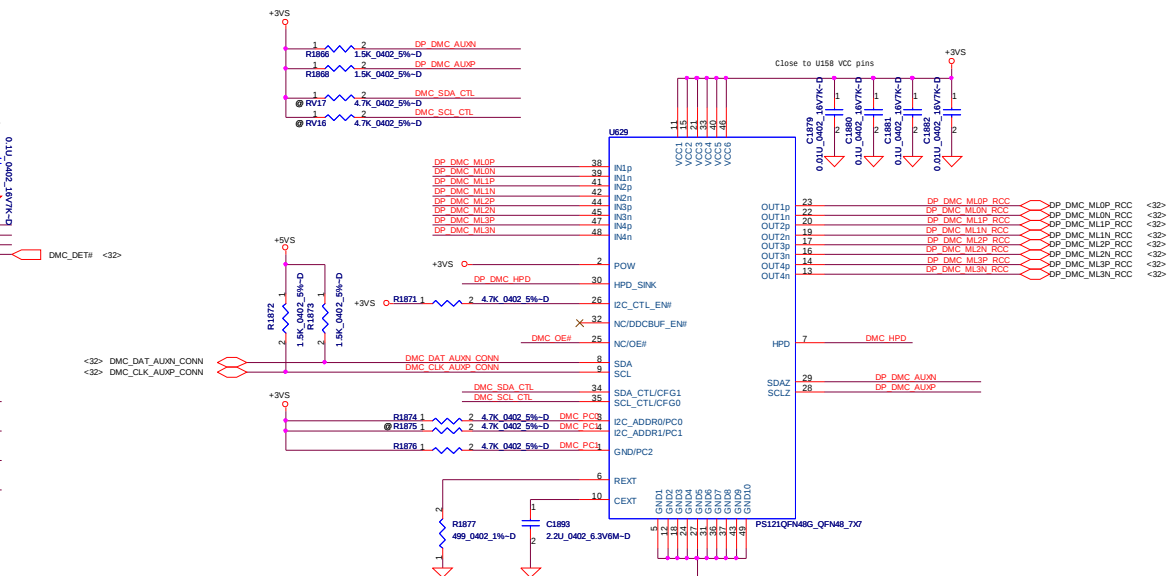


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		Deciphered Date				
2011/01/25		2012/01/25		ELC (3)		
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				LA-6801P		
Date:				Tuesday, January 25, 2011	Sheet	36 of 61

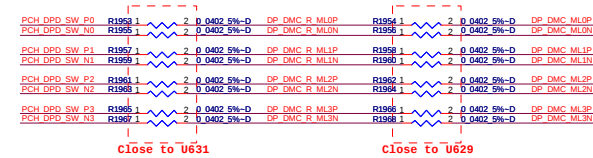
PCH/GPU DDC SW for DMC



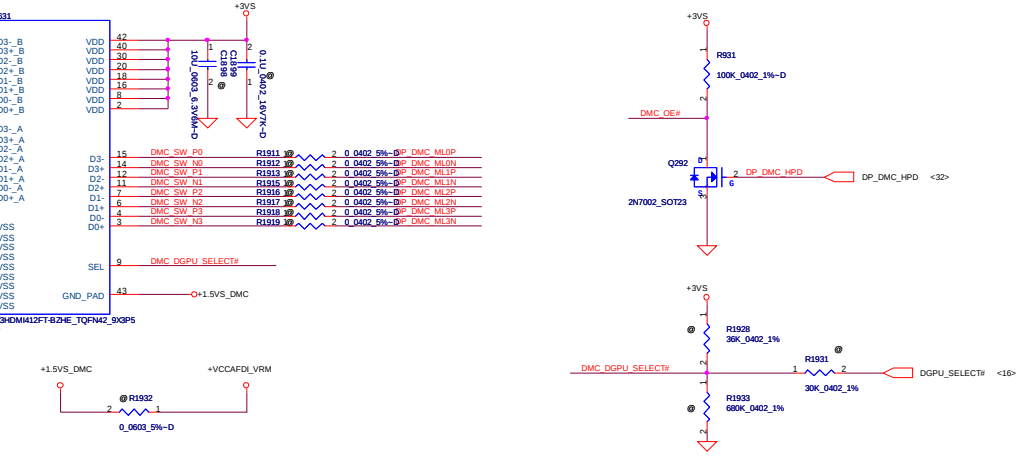
DMC Redriver



PCH/GPU AUX&LANE SW for DMC



6/5 change C188, C1162 0805 to 0603

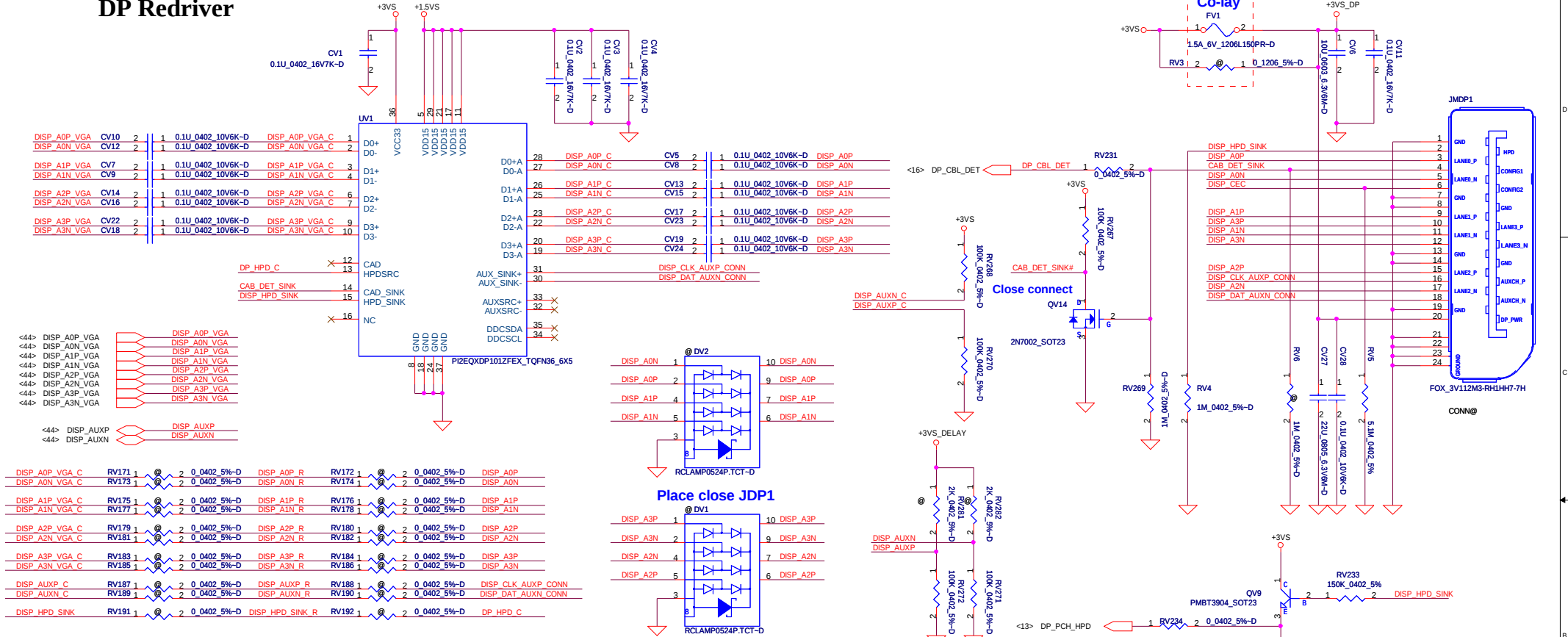


AUX_SEL/SEL1&2	Chanel	Source
0	A	GPU
1	B	PCH

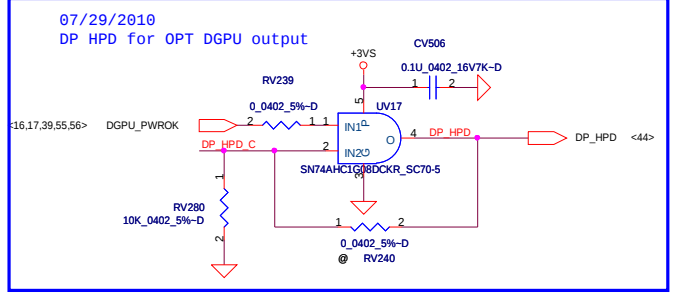
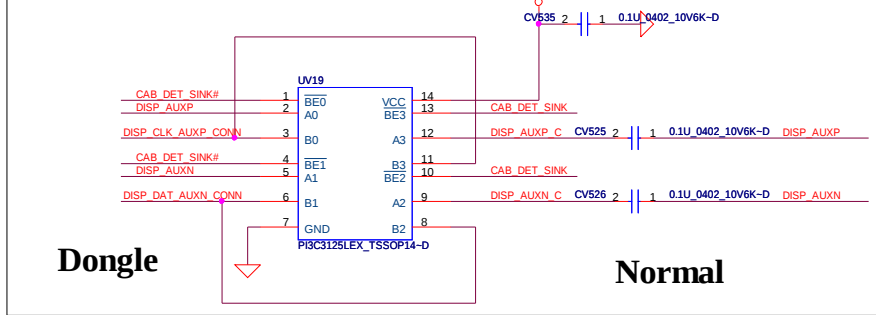
Security Classification		Compal Secret Data		2012/01/25		Compal Electronics, Inc. DMC MUX/Redriver	
Issued Date		2011/01/25		Deciphered Date		Size Doc Number Rev	
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Date		Transferred		Deciphered		3/8/2011 37 of 61	

DP Redriver

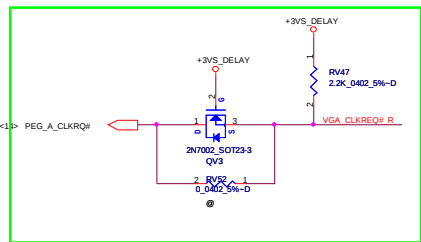
6/5 change C61 0805 to 0603



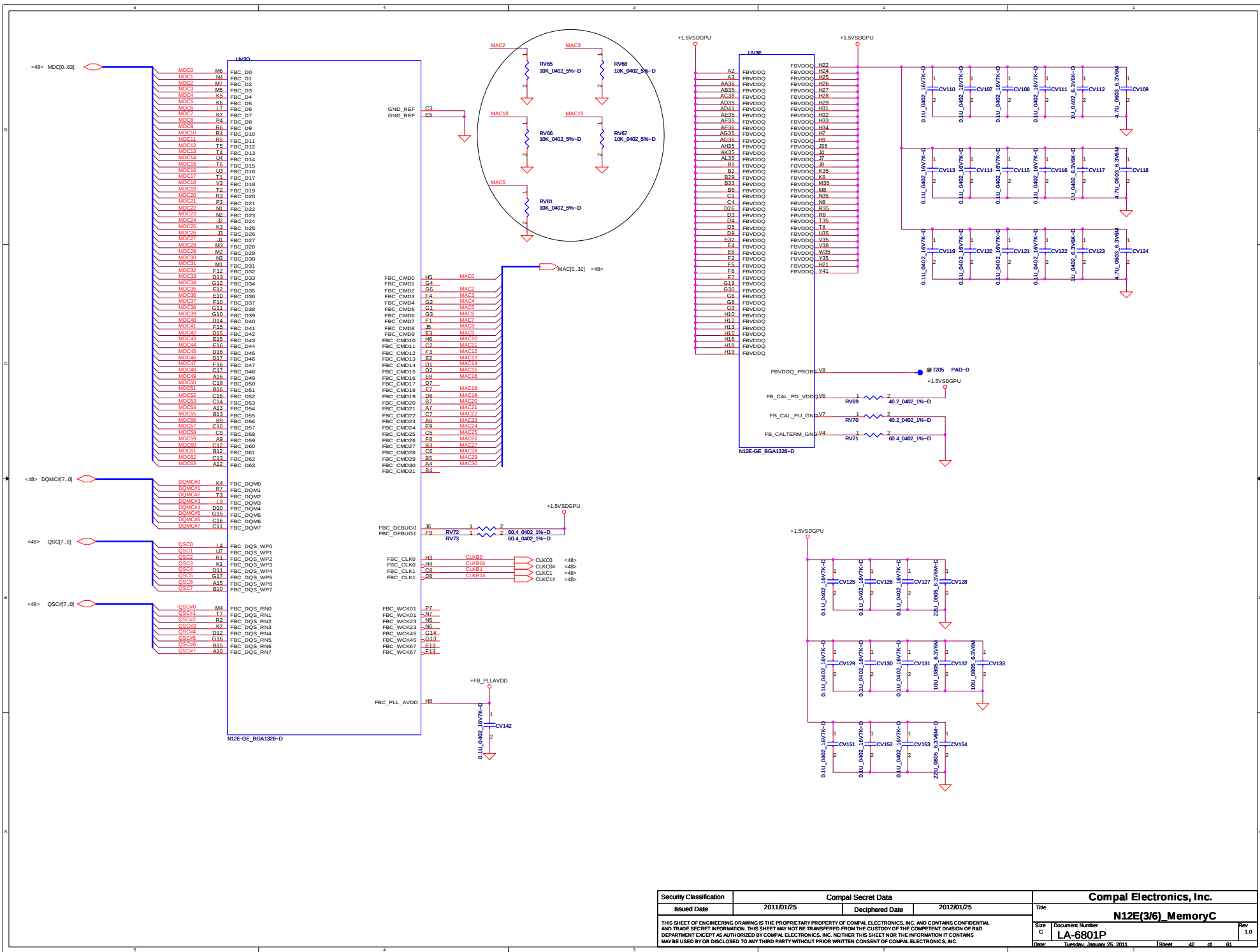
GPU DDC Dongle SW for DP

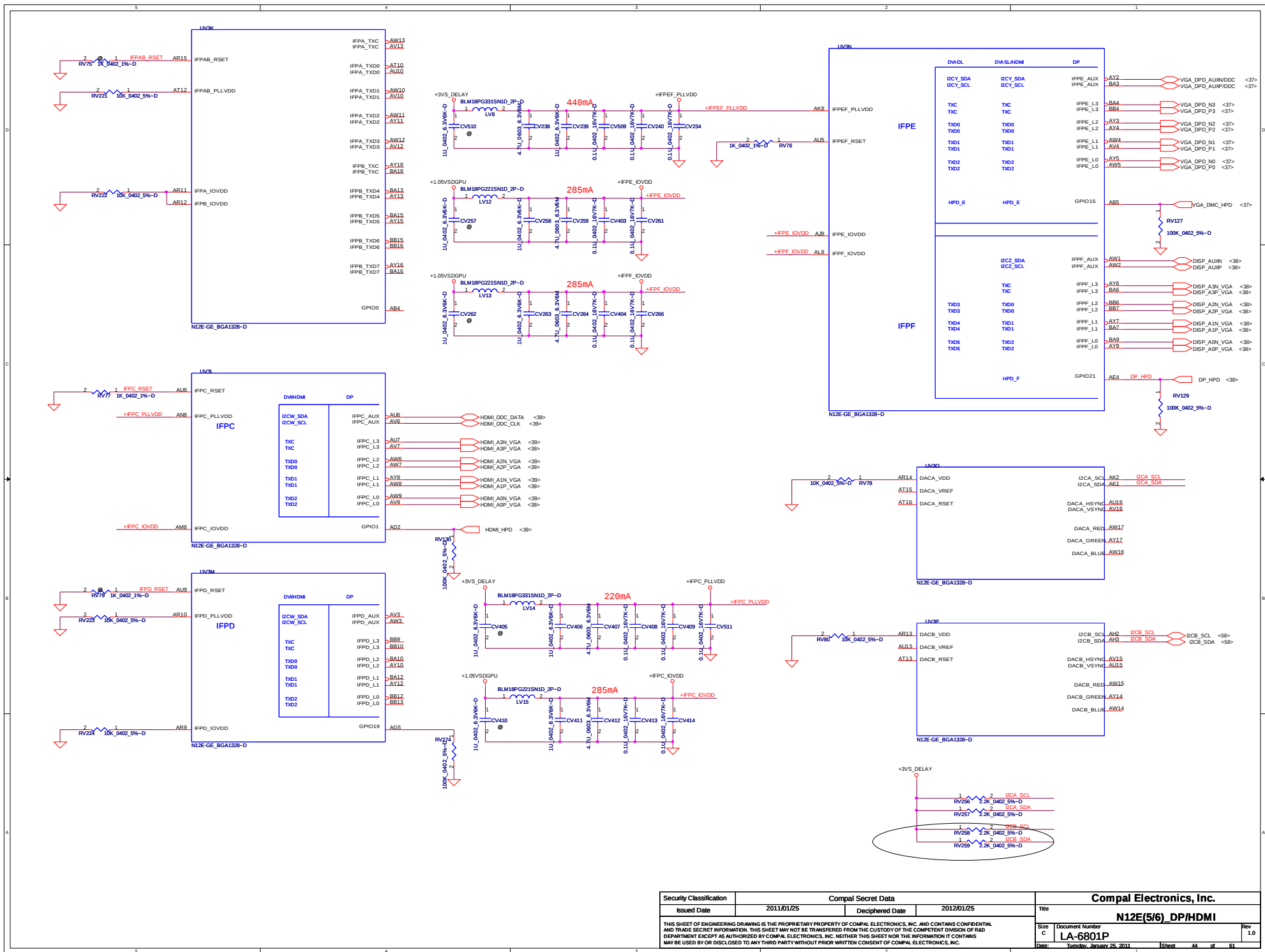


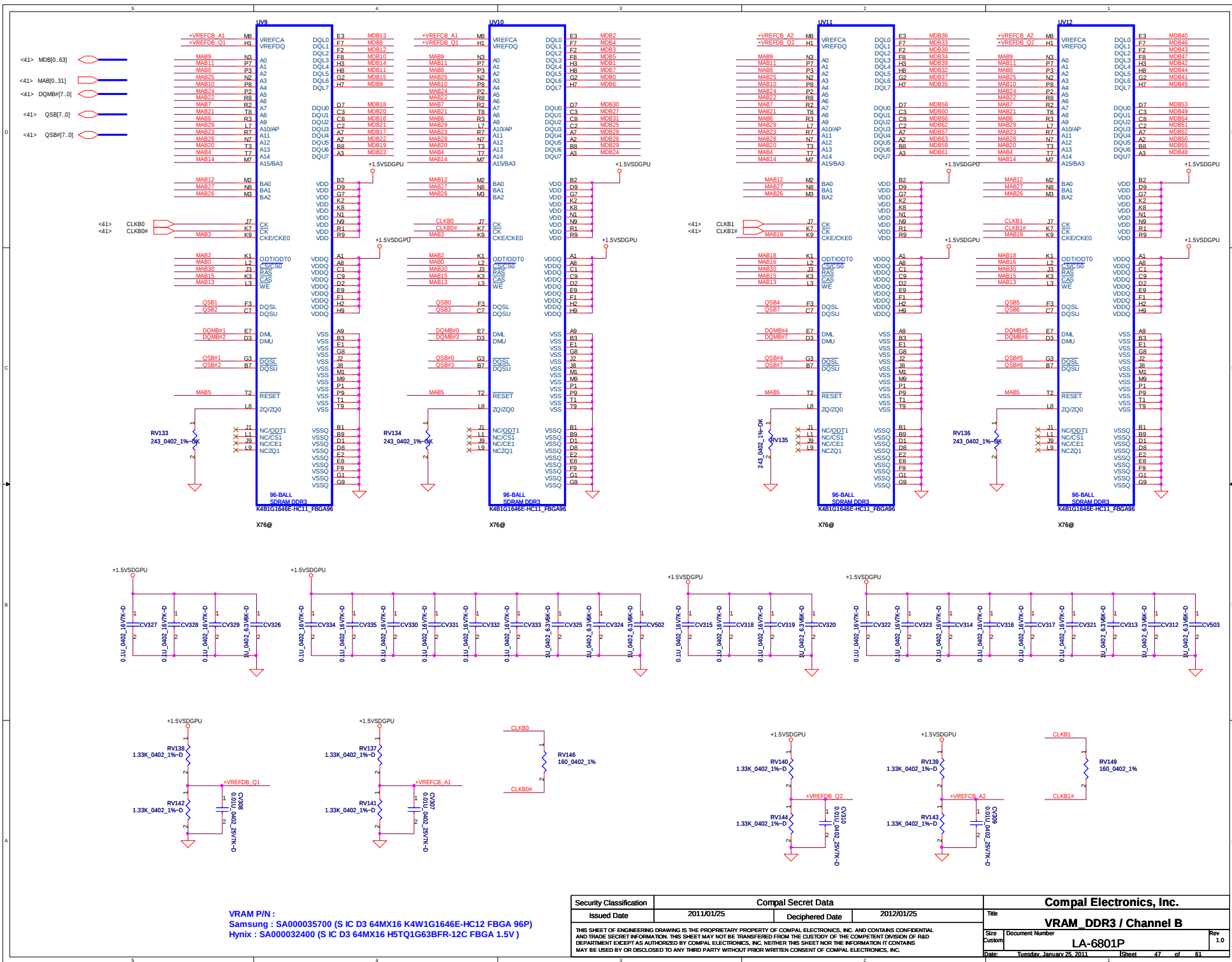
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	
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38		61			



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	N12E(1/6) PCIE	
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				C	LA-6801P	1.0
				Date	Tuesday, January 25, 2011	Sheet 40 of 61

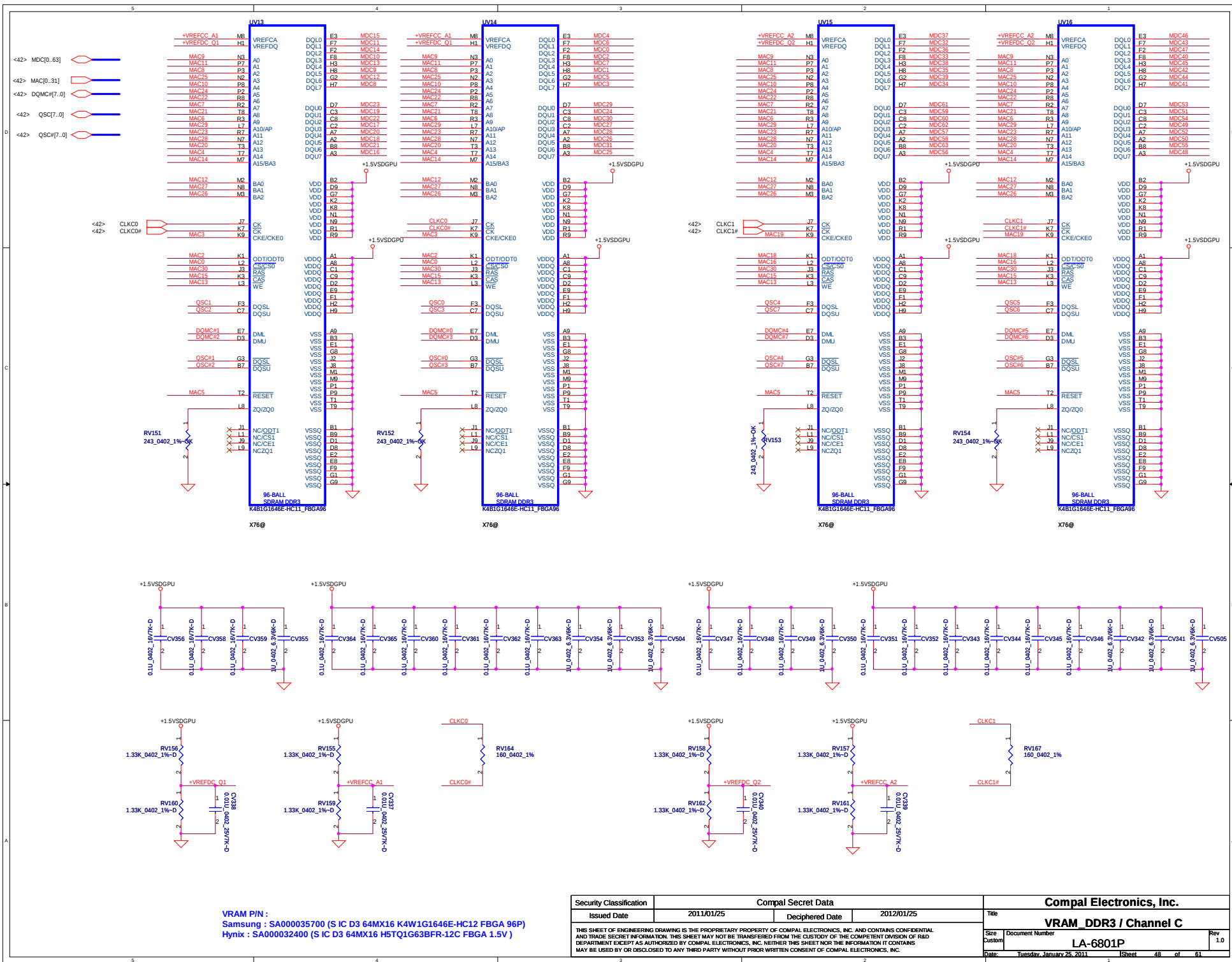






VRAM PIN :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

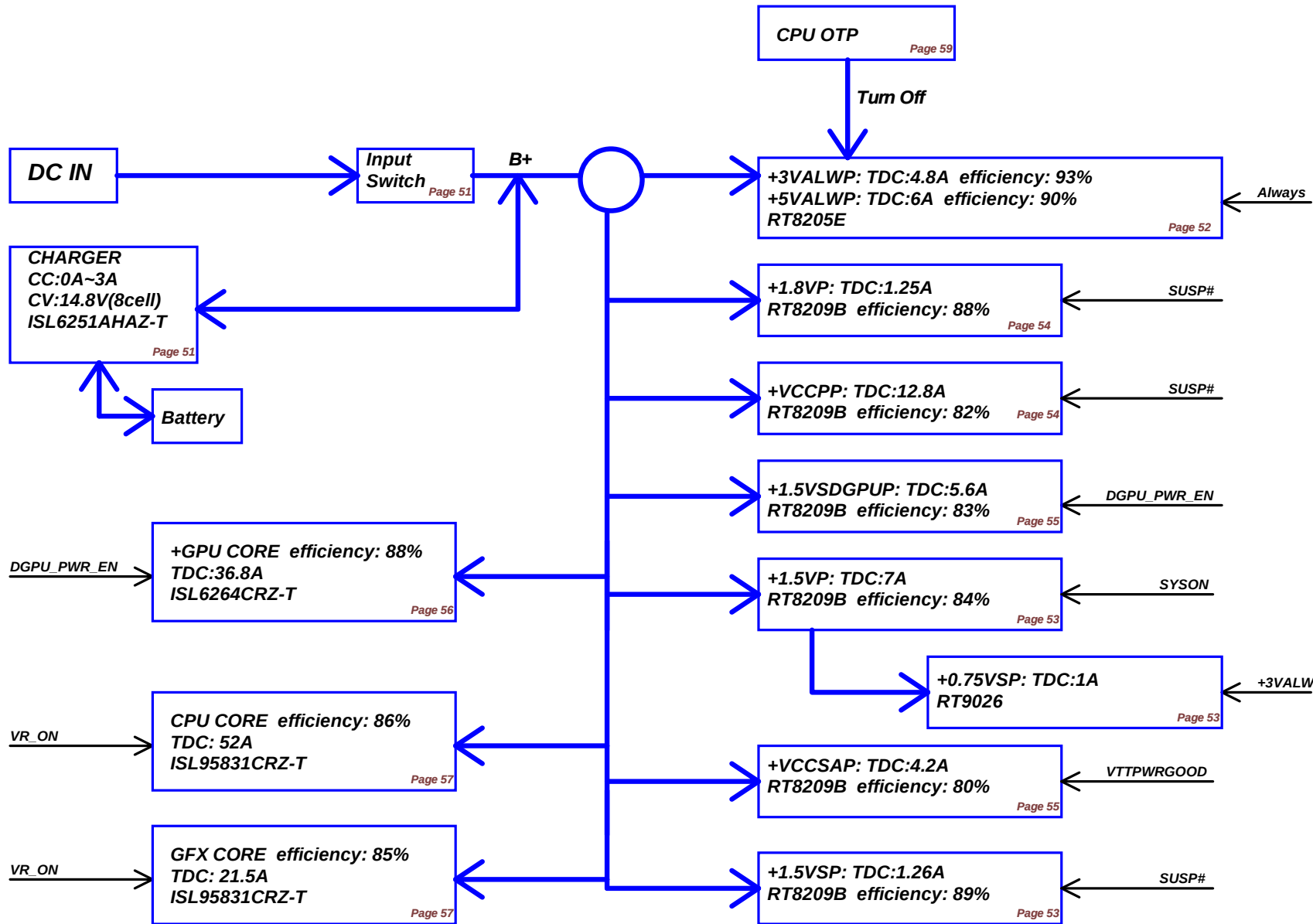
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	VRAM_DDR3 / Channel B
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-6801P
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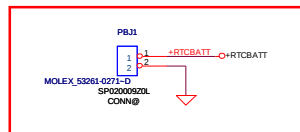
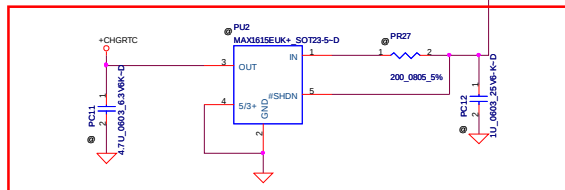
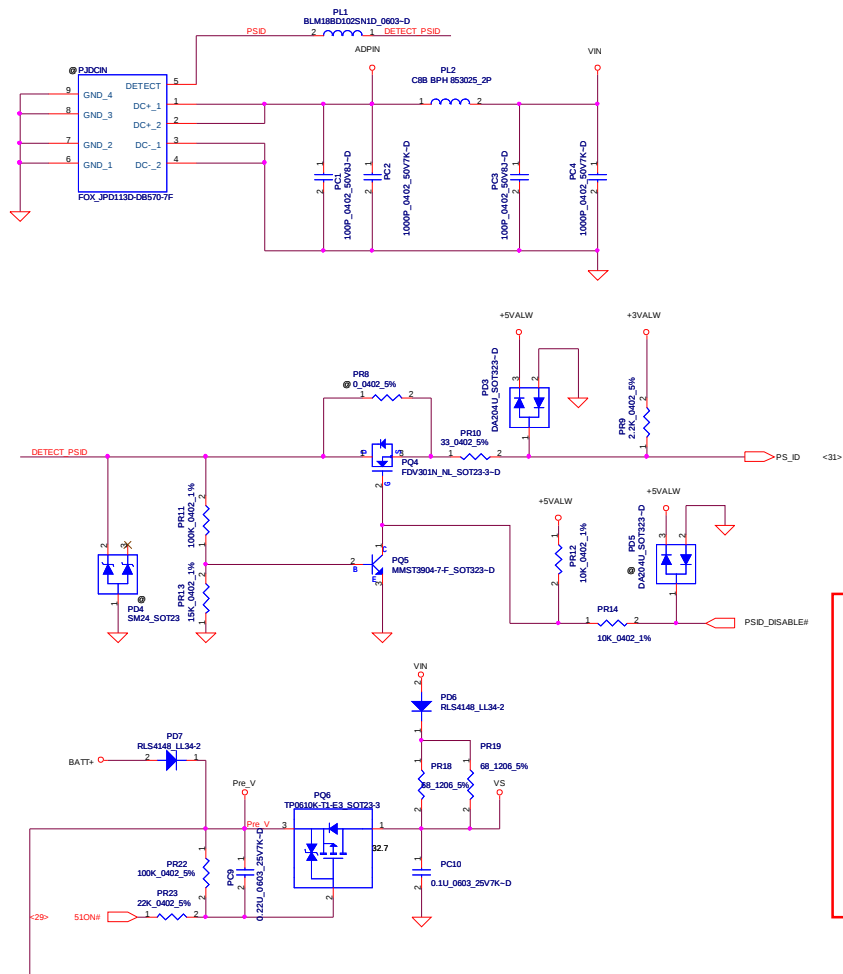
VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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				Size	Document Number	Rev
					LA-6801P	1.0
				Date:	Tuesday, January 25, 2011	Sheet 48 of 61

Power block

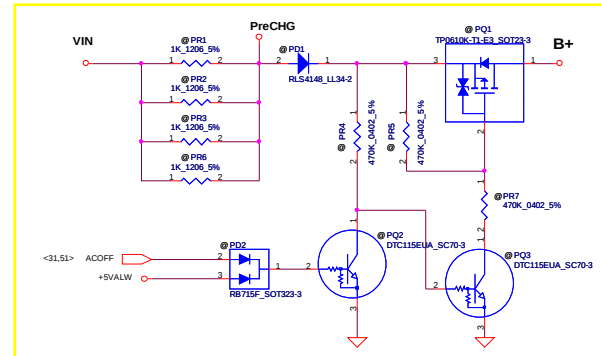


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Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	POWER BLOCK DIAGRAM
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				Custom	LA-6801P
				Date	Tuesday, January 25, 2011
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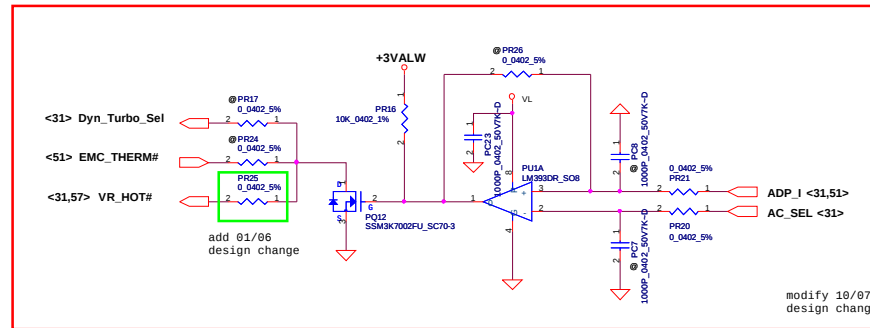


revise 9/17
reduce SS loss

modify 10/21
for ME request



del 12/13
design change



modify 10/07
design change

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	PWR-DCIN / Vin Detector
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				Document Number	LA-6801P
				Date	Tuesday, January 25, 2011
				Sheet	50 of 61

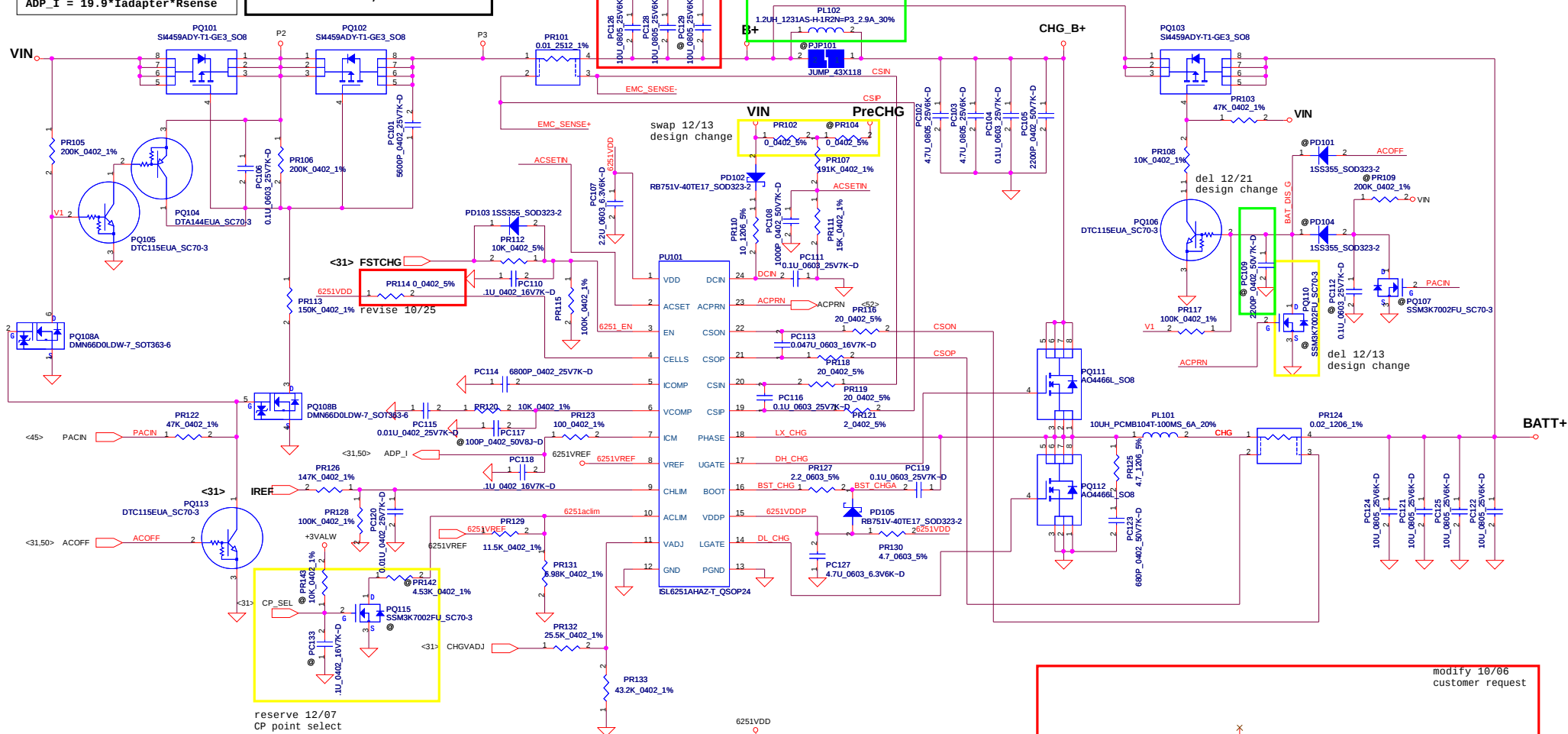
Iada=0-7.693A(150W/19.5V=7.693A)

ADP_I = 19.9*Iadapter*Rsense

CP = 90%*Iada ; CP = 6.92A

add 10/19
for EMI request

add 01/20
for EMI request



CP mode

$I_{input} = (1/0.02) * (0.05 * V_{ac1m} / 2.39 + 0.05)$
 $V_{ac1m} = 2.39 * ((6.98K / 152K) / ((11.5K / 152K) + (6.98K / 152K)))$

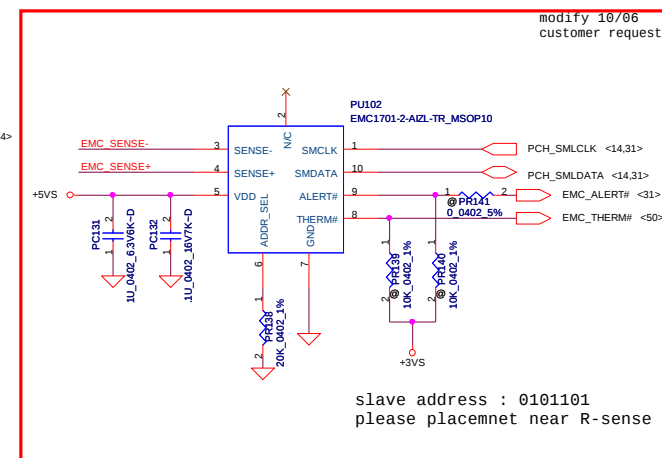
CC=3.3A

IREF=1*Icharge

IREF=0.25V~3.3V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date	Tuesday, January 25, 2011
				Sheet	51 of 61

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO

add 01/20
for EMI request

12UH_12B1AS-H1R2N=P3_9A_30%

PL201

HCB2012KF-121T50_0805

PL204

RT8205E_B+

0.1u_0603_25V7K-D

4.7u_0805_25V6K-D

220P_0402_50V7K-D

PC203

PC204

PC205

PC206

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PC211

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<27,31,33> SYSON

+5VALW

1U_0603_10V6K-D

PC308

10K_0402_5%

PR302

0.0402_5%

PR301

267K_0402_1%

PR303

2.2_0603_5%

PC307

0.1U_0603_25V7K-D

BST 1.5V

ABST 1.5V+1

PC309

10K_0402_1%

PR304

4.7U_0805_10V6K

PC313

4.7U_0805_10V6K

DL 1.5V

PC302

SM634DY-T1-E3_S08

PC304

4.7_1206_5%

PL302

1UH_PCB0802D-180MS_9A_20%

PC301

SM172DY-T1-GE3_S08

PC303

0.1U_0603_25V7K-D

PC304

4.7U_0805_25V6K-D

PC305

4.7U_0805_25V6K-D

PC306

4.7U_0805_25V6K-D

PC307

0.1U_0603_25V7K-D

PC308

10K_0402_5%

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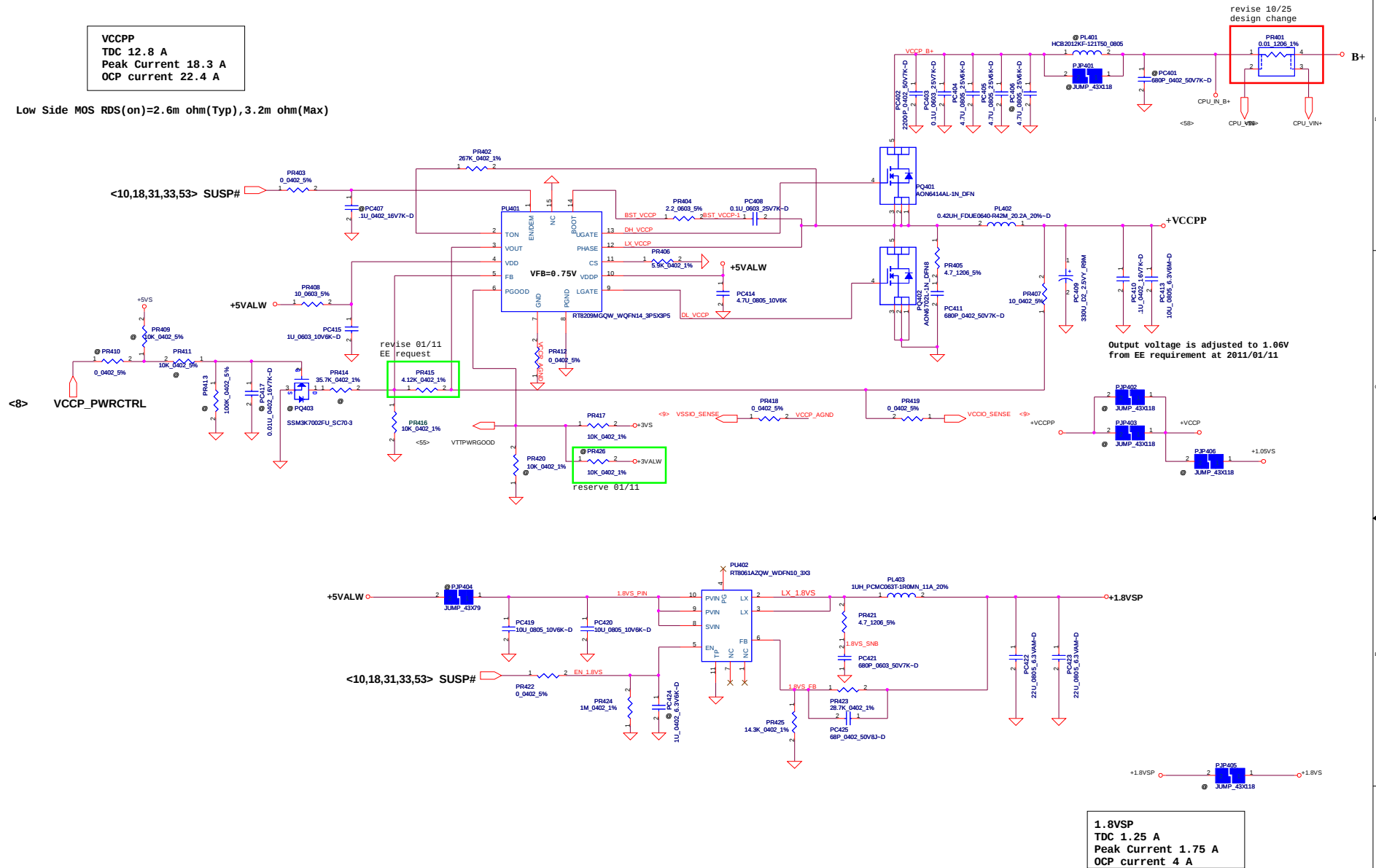
10K_0402_5%

PC434

10K_0402_5%

VCCPP
TDC 12.8 A
Peak Current 18.3 A
OCP current 22.4 A

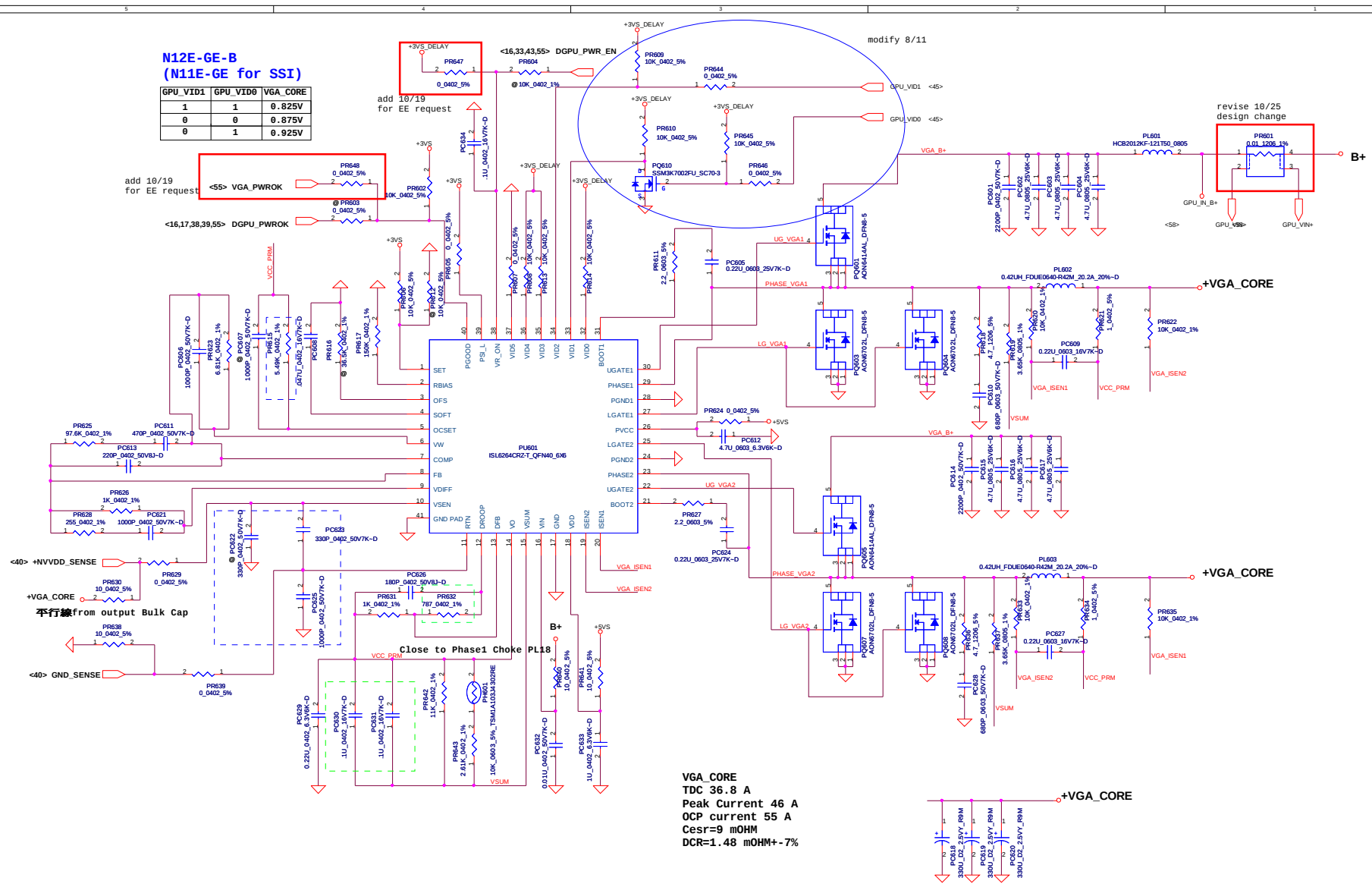
Low Side MOS RDS(on)=2.6m ohm(Typ), 3.2m ohm(Max)



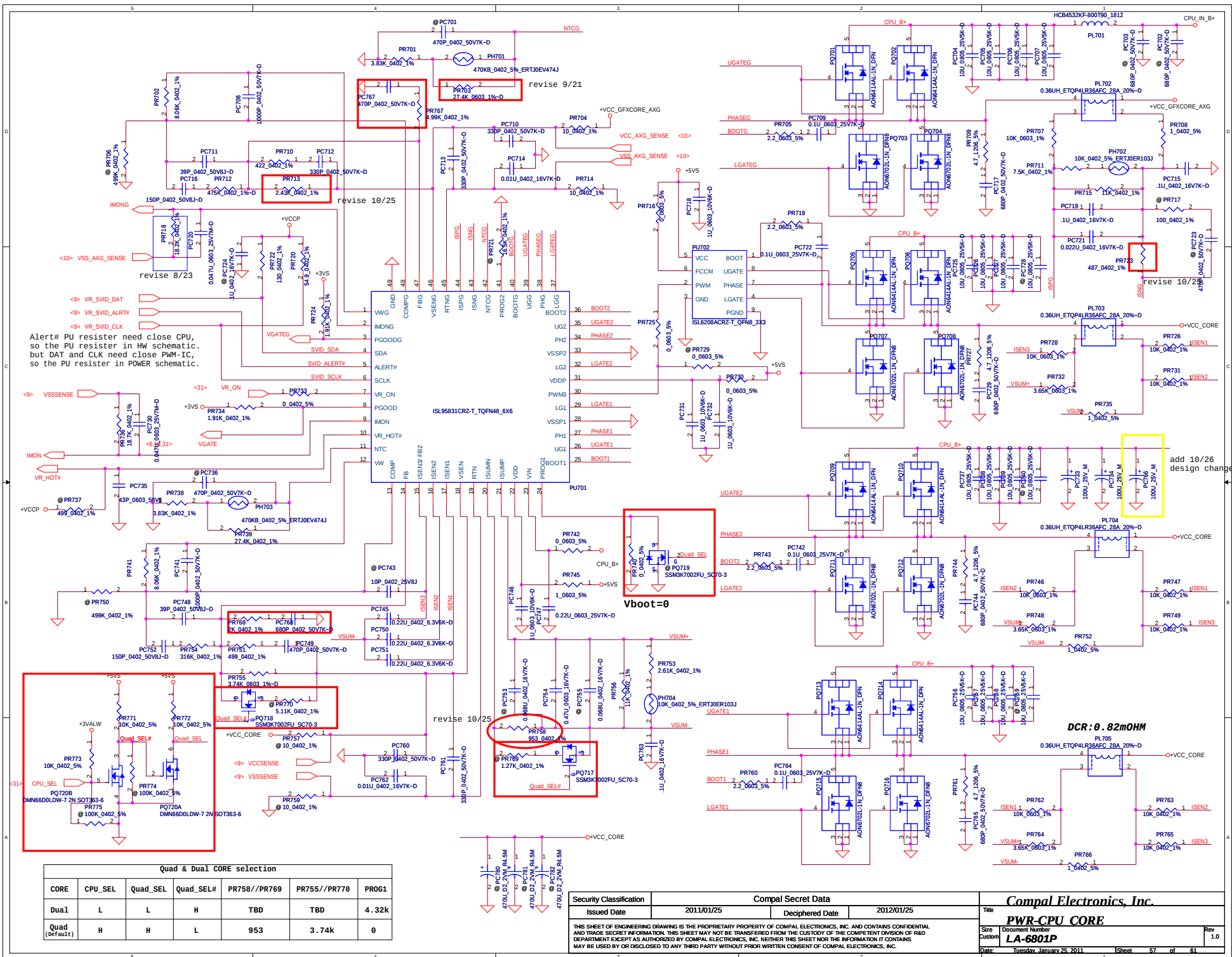
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/25	Deciphered Date	2012/01/25	Title	PWR+VCCPP+1.8VSP
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				C	LA-6801P
				Date	Tuesday, January 25, 2011
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N12E-GE-B
(N11E-GE for SSI)

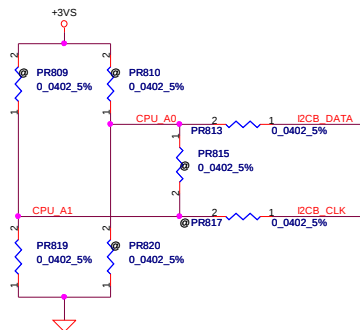
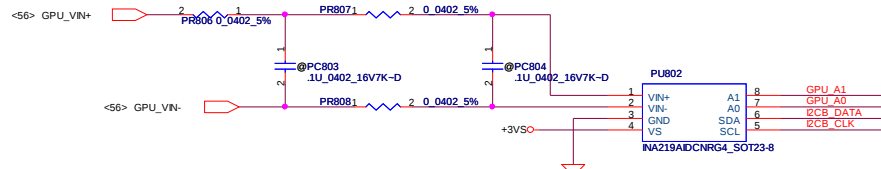
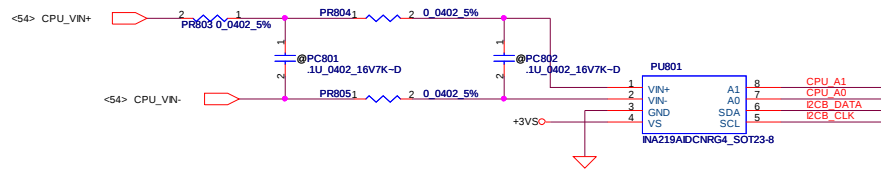
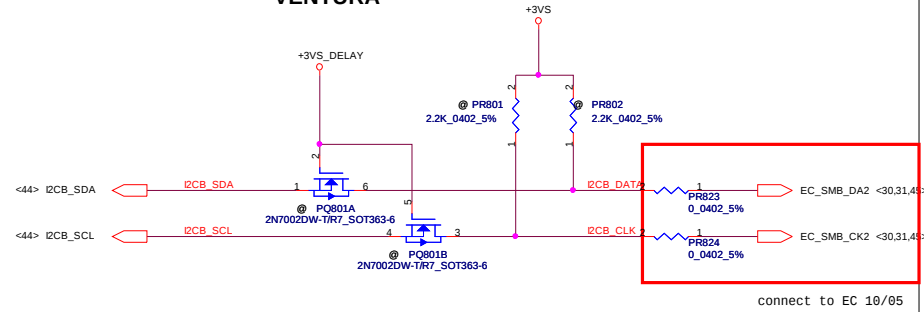
GPU_VID1	GPU_VID6	VGA_CORE
1	1	0.825V
1	0	0.875V
0	1	0.925V



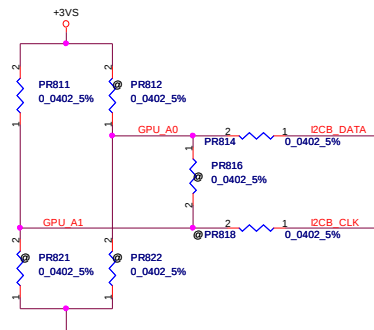
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VENTURA



Ventura for CPU side
slave address : 1000010
please placemnet near R-sense



Ventura for GPU side
slave Address 1000110
please placement near R-sense

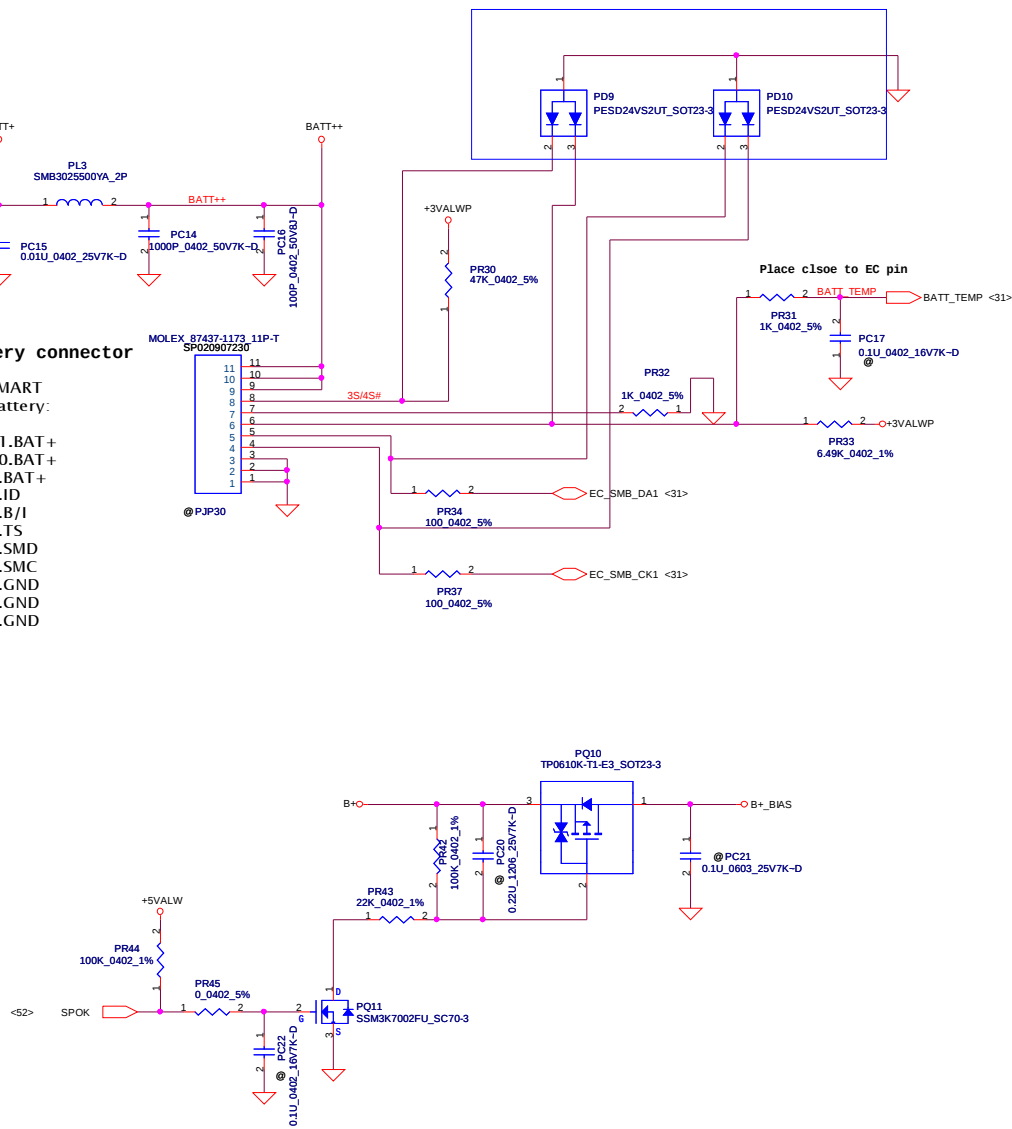
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revise 8/09
ESD request

PJP30 battery connector

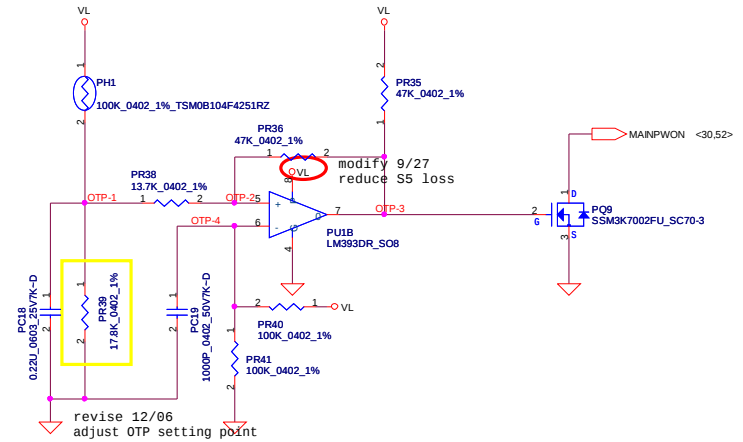
SMART
Battery:

- 11.BAT+
- 10.BAT+
- 9.BAT+
- 8.ID
- 7.B/I
- 6.TS
- 5.SMD
- 4.SMC
- 3.GND
- 2.GND
- 1.GND



Battery Connect/OTP

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



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Version Change List (P. I. R. List)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	50	PWR-DCIN / Vin Detector	10/09/17	COMPAL	reduce SS loss	add PU2;PR27;PC11;PC12	0.2
2	55	+VCCSAP/+1.5VSDGUP	10/09/21	COMPAL	RF request	add PR521;PC529 change PR520 from 0 to 2.2	0.2
3	57	+CPU_CORE	10/09/21	COMPAL	design change	change PR703 from 0 to 27.4K	0.2
4	51	CHARGER	10/10/06	COMPAL	design change	change PC131 from 0.1u to 1u	0.2
5	50	PWR-DCIN / Vin Detector	10/10/07	COMPAL	design change	add PQ12;PC23	0.2
6	54	+VCCPP/+1.8VSP	10/10/07	COMPAL	design change	modify 1.8VSP solution	0.2
7	51	CHARGER	10/10/19	COMPAL	EMI request	add PC126;PC128	0.2
8	55	+VCCSAP/+1.5VSDGUP	10/10/19	COMPAL	EE request	add PR528;PR529;PR530 del PR519	0.2
9	56	+VGA_CORE	10/10/19	COMPAL	EE request	add PR647;PR648 del PR603;PR604	0.2
10	51	CHARGER	10/10/25	COMPAL	design change	change PR114 from 47K to 0	0.2
11	54	+VCCPP/+1.8VSP	10/10/25	COMPAL	design change for use ventura curcuit	change PR401 from 0 to 0.01	0.2
12	56	+VGA_CORE	10/10/25	COMPAL	design change for use ventura curcuit	change PR601 from 0 to 0.01	0.2
13	57	+CPU_CORE	10/10/25	COMPAL	change CPU OCP setting	change PR758 from 887 to 953	0.2
14	57	+CPU_CORE	10/10/25	COMPAL	change GFX OCP & LL setting	change PR723 from 442 to 487 change PR713 from 2.61K to 2.43K	0.2
15	57	+CPU_CORE	10/10/25	COMPAL	quad & dual core CPU switch setting design	add PQ717;PQ718;PQ720;PR771;PR772;PR773;PR767;PR768;PC767;PC768	0.2
16	58	VENTURA	10/10/25	COMPAL	add ventura connect to EC	add PU801;PU802;PR803;PR804;PR805;PR806;PR807;PR808	0.2
						;PR811;PR813;PR814;PR819;PR823;PR824	0.2
17	57	+CPU_CORE	10/10/26	COMPAL	design change for solve acoustic issue	add PC766	0.3
18	52	3VALWP/5VALWP	10/10/27	COMPAL	design change for reserve adjust working frequency	add PR222	0.3
19	59	BATTERY CONN	10/12/06	COMPAL	adjust OTP setting point	change PR39 from 16.9K to 17.8K	0.3
20	50	PWR-DCIN / Vin Detector	10/12/13	COMPAL	design change for delete prechange circuit	del PR1;PR2;PR3;PR4;PR5;PR6;PR7;PD1;PD2;PQ1;PQ2;PQ3	0.3
21	51	CHARGER	10/12/13	COMPAL	design change for delete prechange circuit	del PR104;PQ110 add PR102	0.3
22	53	+1.5VP/+0.75VSP/+1.5VSP	10/12/13	COMPAL	EE request for use memory over clocking circuit	add PR312;PR318	0.3
23	53	+1.5VP/+0.75VSP/+1.5VSP	10/12/20	COMPAL	design change for adjust original output voltage	swap PR314;PR317 and PR320;PR323	0.4
24	51	CHARGER	10/12/21	COMPAL	design change for delete prechange circuit	del PC109	0.4
25	50	PWR-DCIN / Vin Detector	11/01/06	COMPAL	design change for add AC peak power function	add PR25	0.4
26	54	+VCCPP/+1.8VSP	11/01/11	COMPAL	EE request for adjust output voltage	change PR415 from 4.02K to 4.12K	0.4
27	55	+VCCSAP/+1.5VSDGUP	11/01/11	COMPAL	EE request for adjust output voltage	change PR524 from 10K to 10.5K	0.4
28	51	CHARGER	11/01/20	COMPAL	EMI request	add PL102	0.4
29	52	3VALWP/5VALWP	11/01/20	COMPAL	EMI request	add PL204	0.4

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