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P. Leader	Check by	Design by

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TitleIndex Page

SizeCustom

Document NumberMS51(MBX-152)

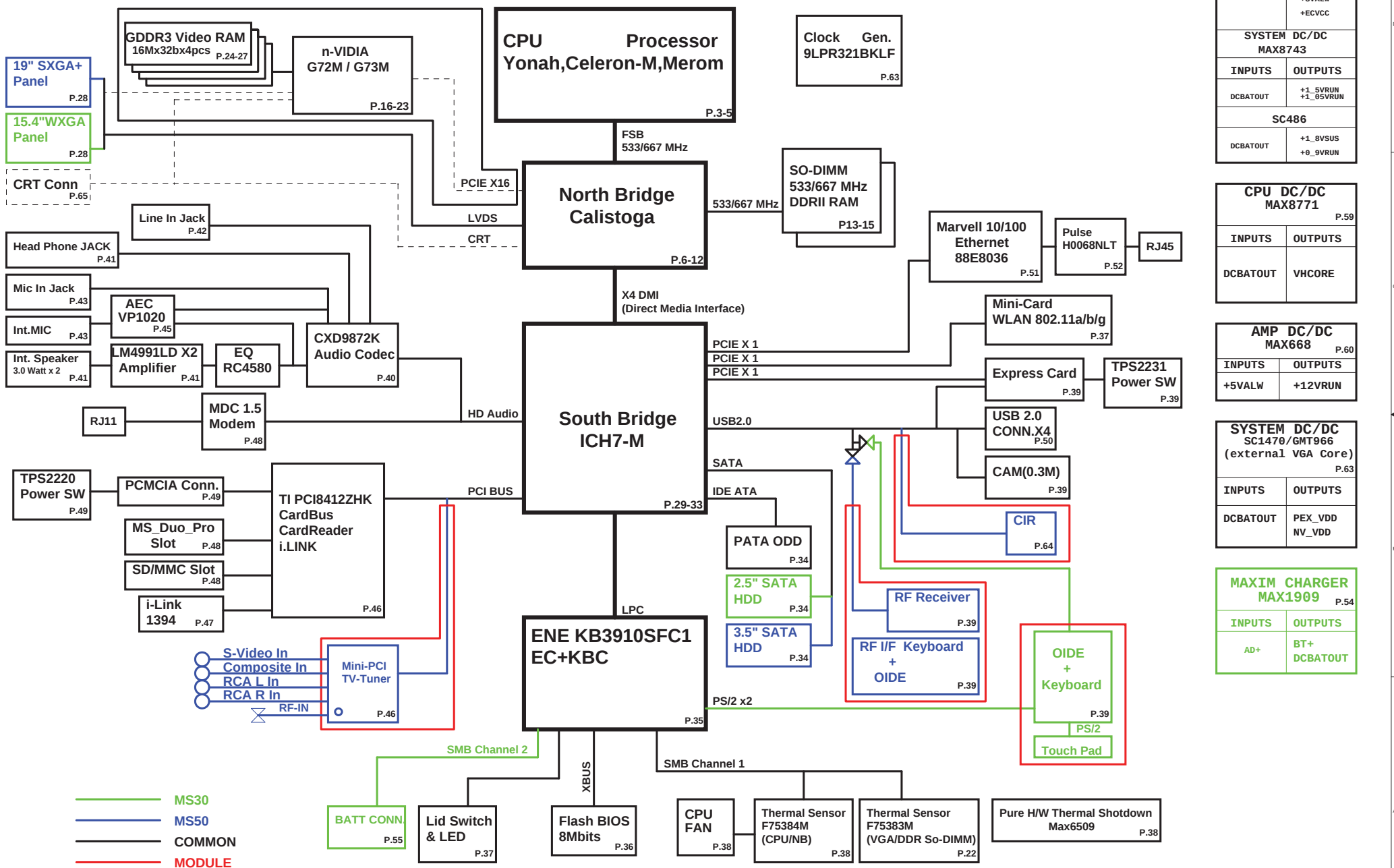
Rev0.30

DateThursday, July 27, 2006Sheet1 of 67

PCB P/N: - - SA
 - - SA
 - - SA

Project Code & Schematics Subject: MS31/51 Main Board

MBX-152(CALISTOGA PM/GM+Gfx Block Diagram



SYSTEM DC/DC MAX8734A P.56	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC
SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486	
DCBATOUT	+1_8VSUS +0_9VRUN

CPU DC/DC MAX8771 P.59	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX668 P.60	
INPUTS	OUTPUTS
+5VALW	+12VRUN

SYSTEM DC/DC SC1470/GMT966 (external VGA Core) P.63	
INPUTS	OUTPUTS
DCBATOUT	PEX_VDD NV_VDD

MAXIM CHARGER MAX1909 P.54	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

- MS30
- MS50
- COMMON
- MODULE

Layout note:
no stub on
H_STPCLK#

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL --- -0.5V ~ 0.8V
VIH --- 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL --- -0.1V ~ 0.3*VCCP
VIH --- 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU, IMVP and MCH, pull-up
resistor has to be 75 ohm +-5%

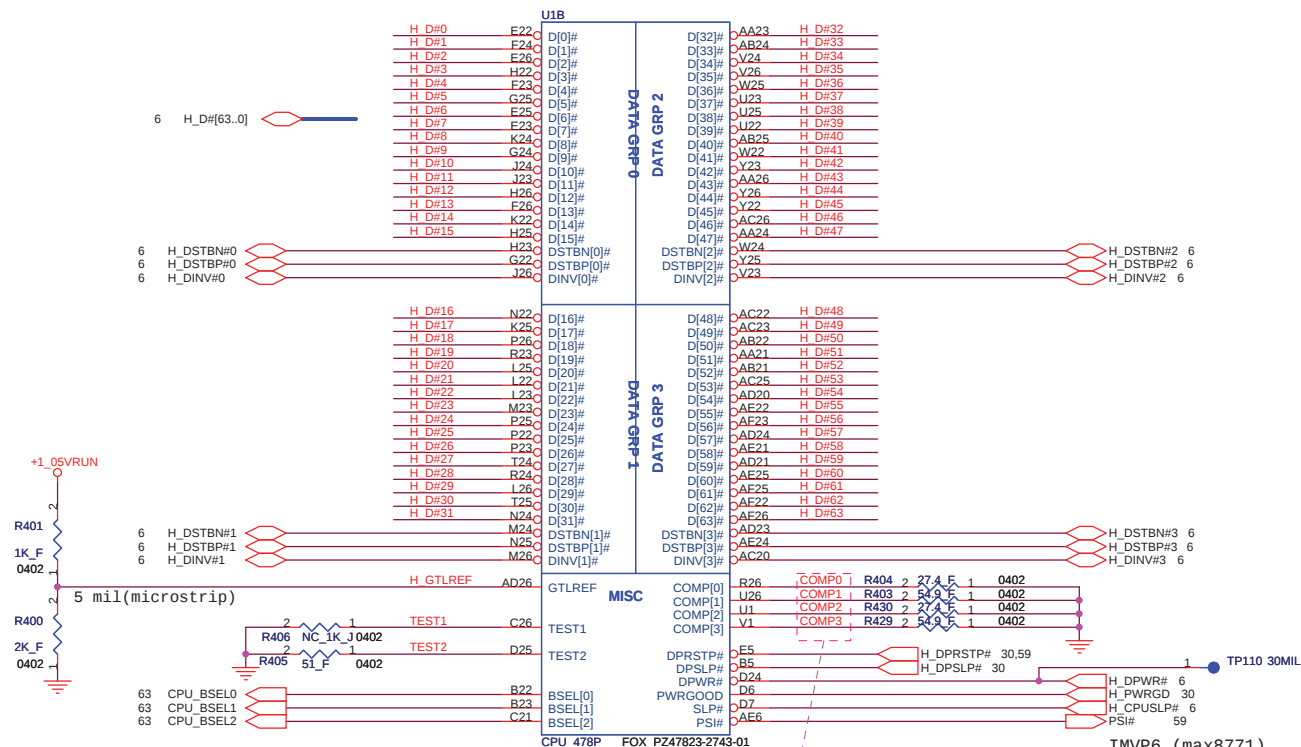
DVT (change to 2N7002)

Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

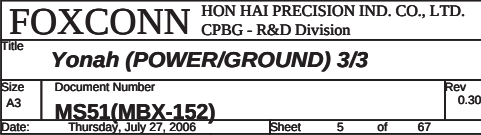
FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

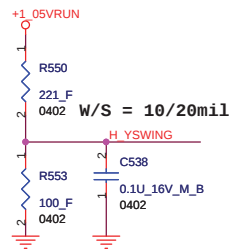
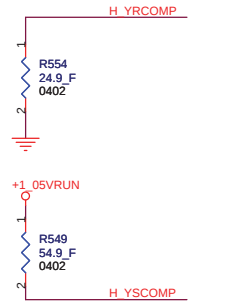
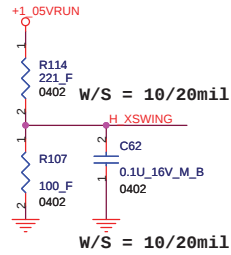
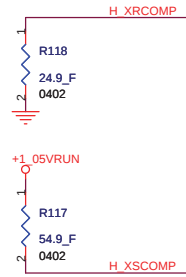


Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

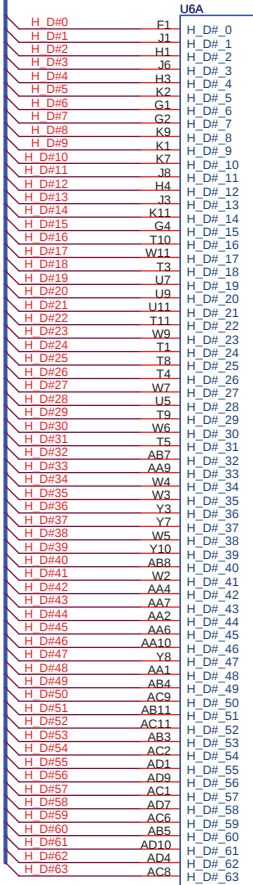
IMVP6 (max8771)
cpu PSI# <-> max8771 PSI#
max8771: VIHmin=0.67V
VILmax=0.33V
(ref. max8771 datasheet)



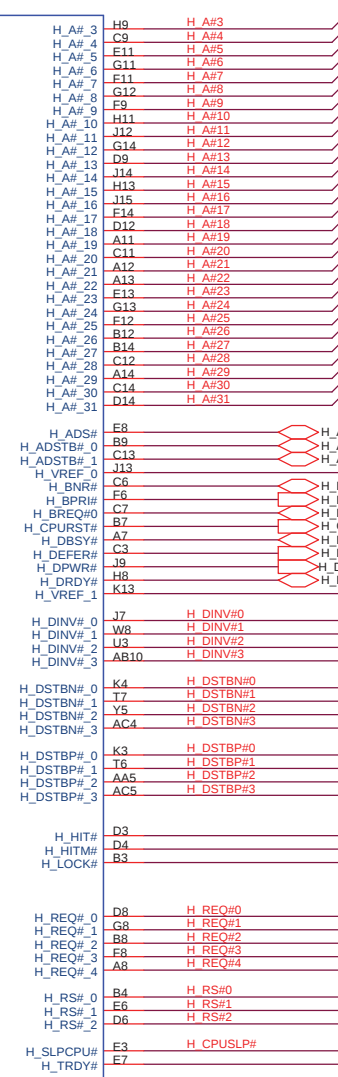
W/S = 10/20mil



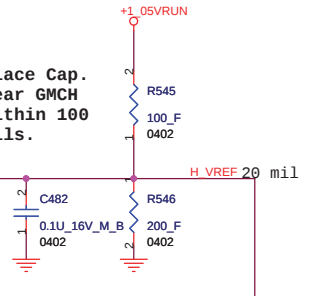
4 H_D#[63..0]



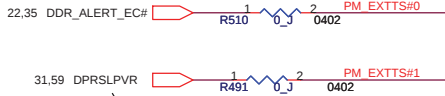
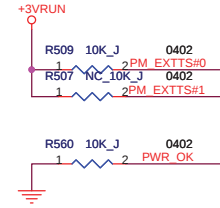
HOST



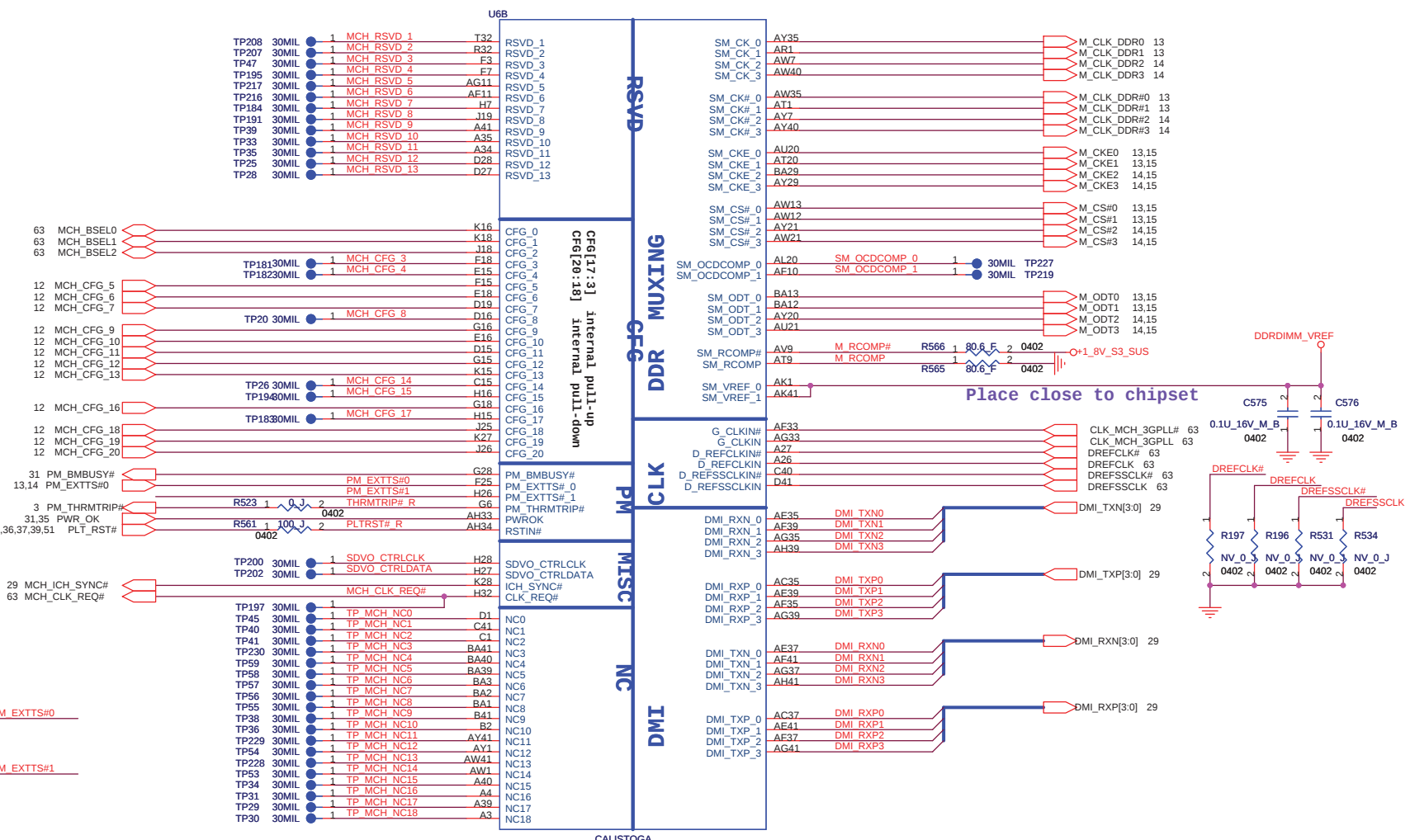
Place Cap.
near GMCH
within 100
mils.

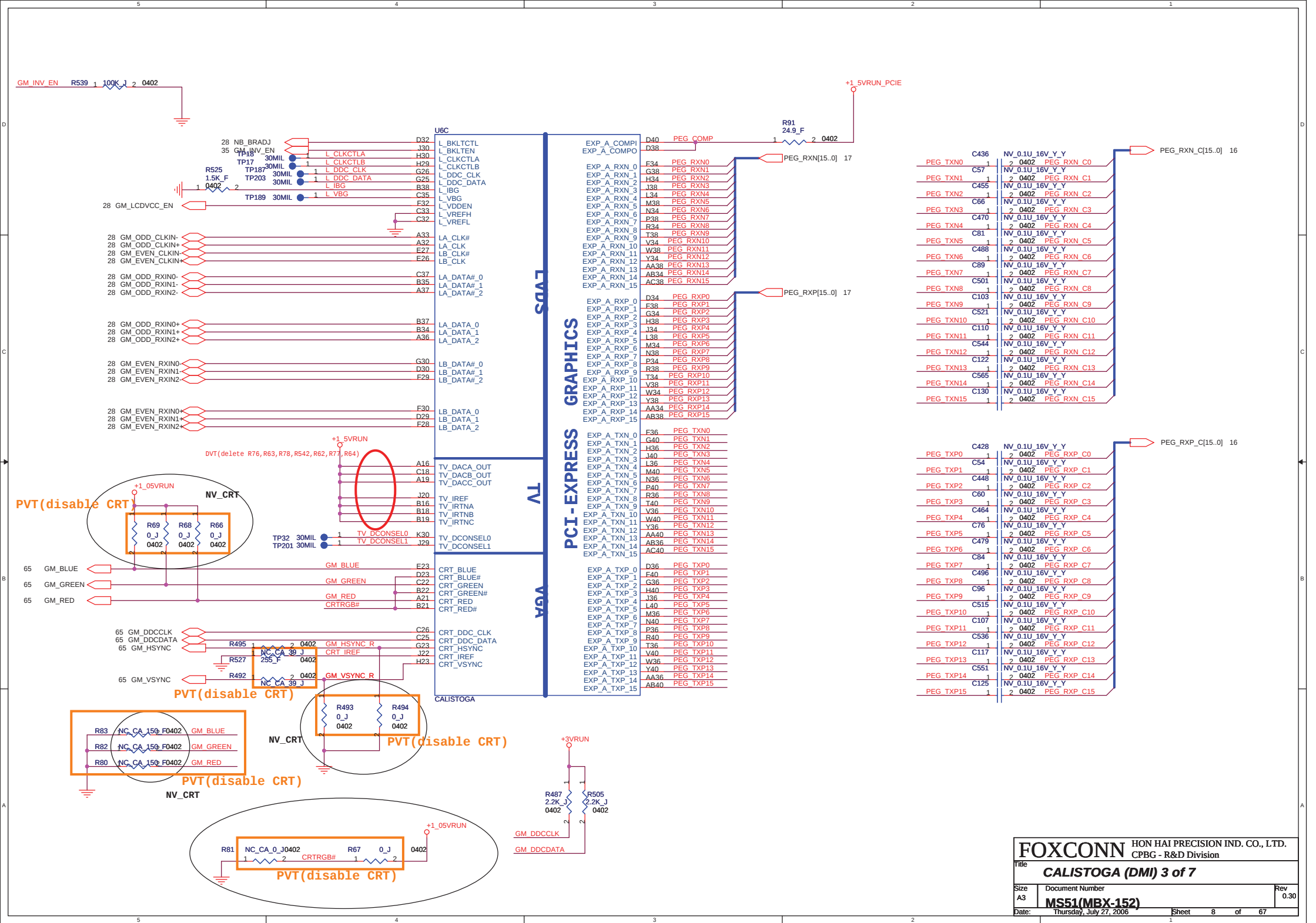


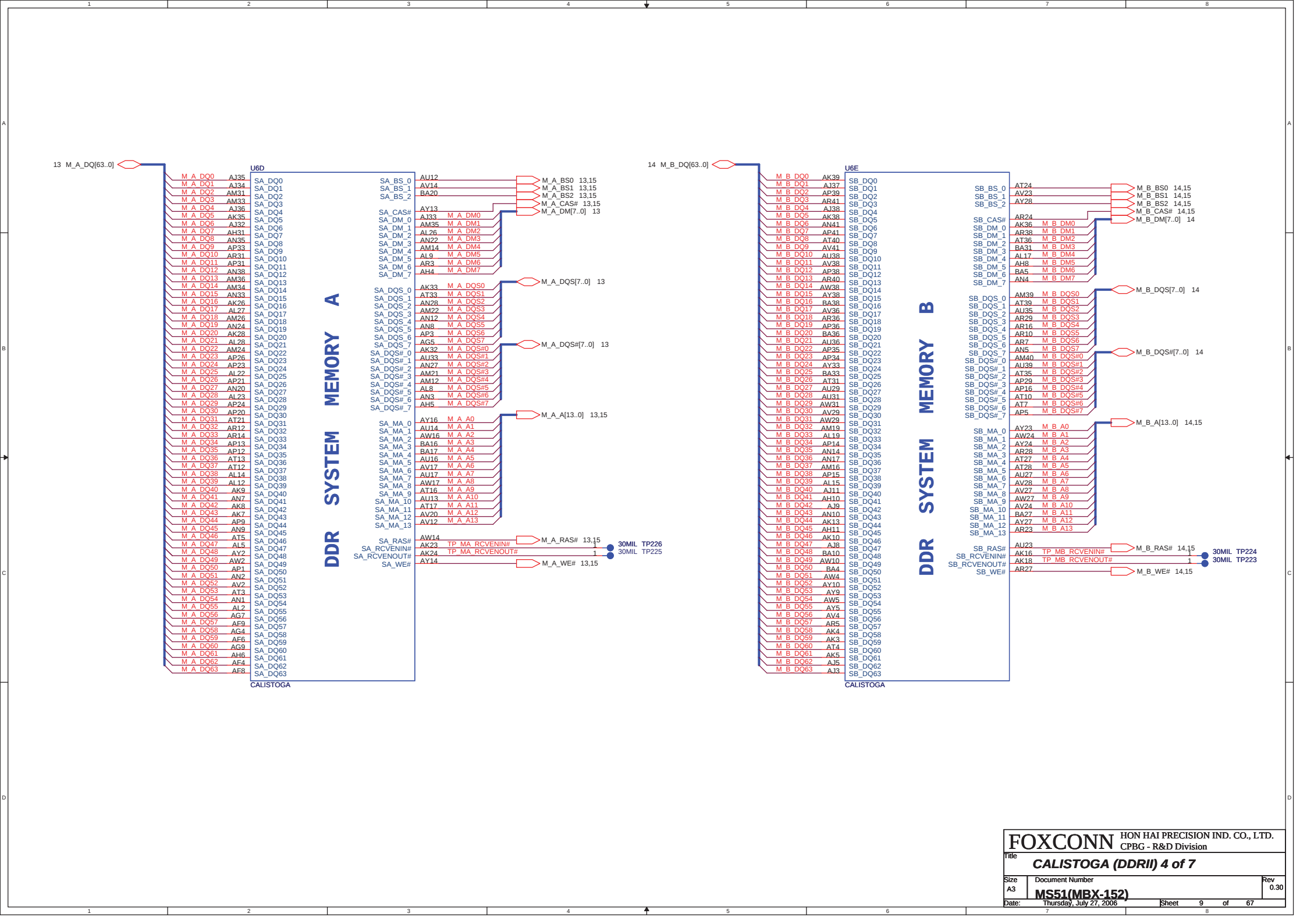
GM QG88CGM 12-0688CGM-0000
PM QG88CPM 12-0688CPM-0000
GM QG82945GM-A3 12-0682945-A300 for MP

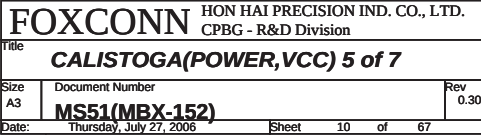


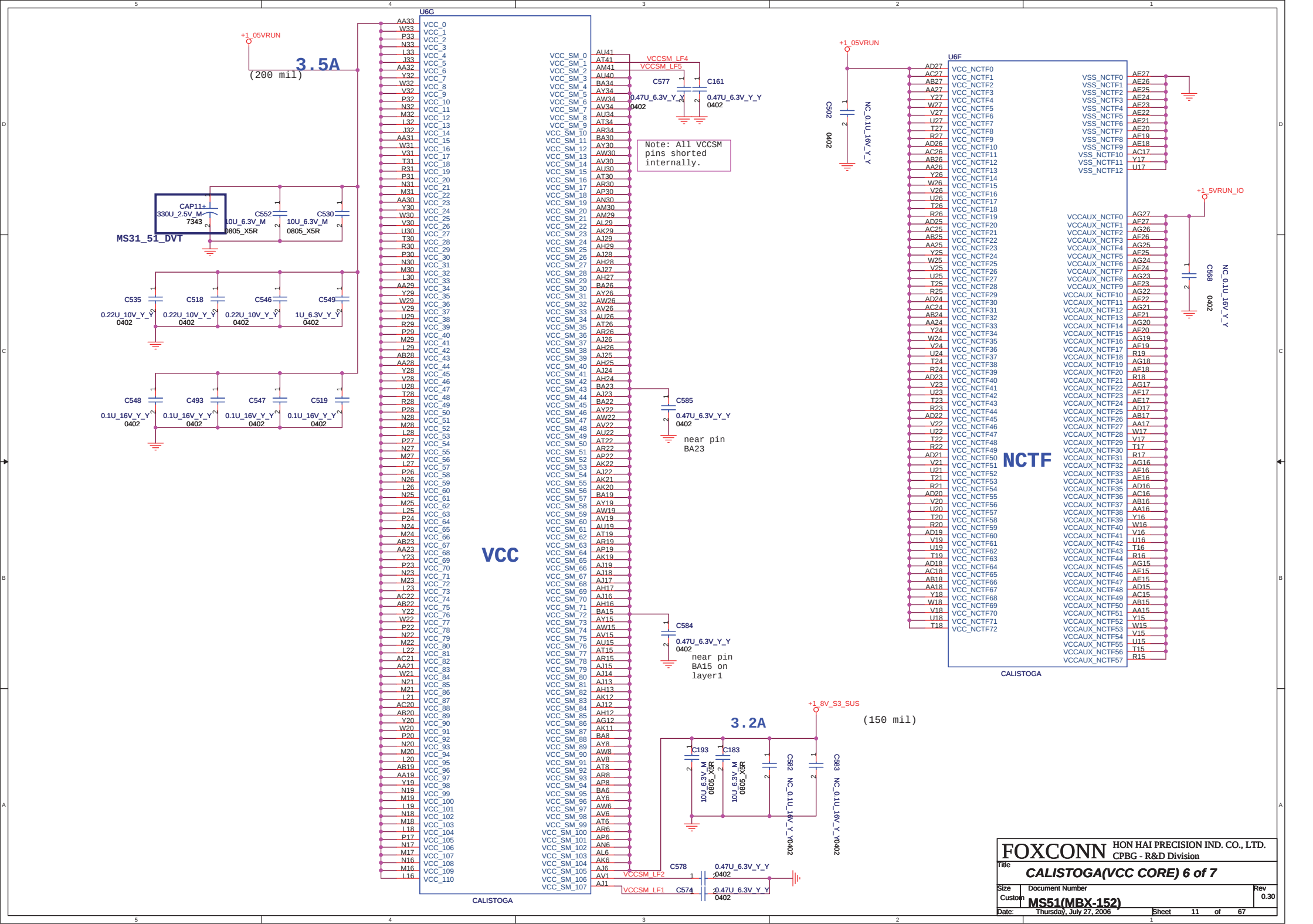
CRB rev:1.301 update











7 MCH_CFG_5 1 30MIL TP193

MCH_CFG_5 Low = DMIX2
High = DMIX4

7 MCH_CFG_6 1 30MIL TP180

MCH_CFG_6 Low = Moby Dick
High = Calistoga
DDR2 select (default high)

7 MCH_CFG_7 1 30MIL TP15

MCH_CFG_7 (CPU Strap) Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 1 30MIL TP250

MCH_CFG_9 (PCIe Graphics Lane) Low = Reverse Lane
High = Normal operation

For layout convenience

7 MCH_CFG_10 1 30MIL TP192

MCH_CFG_10 (HOST PLL VCC SELECT) Low = RESERVED
High = MOBILITY

7 MCH_CFG_11 1 30MIL TP205

MCH_CFG_11 (PSB 4x CLK ENABLE) Low = Reserved
High = Calistoga

7 MCH_CFG_12 1 30MIL TP185

7 MCH_CFG_13 1 30MIL TP205

MCH_CFG [13:12] (XOR/ALLZ) 00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 1 30MIL TP178

MCH_CFG_16 (FSB Dynamic ODT) Low = Dynamic ODT Disabled
High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select) Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_18 1 30MIL TP248

DTV (delete R508, add TP)

MCH_CFG_19 (DMI LANE REVERSAL) Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_19 1 30MIL TP249

DTV (delete R541, add TP)

DTV (delete R514, add TP)

MCH_CFG_20 (PCIe Backward Interoperability mode) Low = Only SDVO or PCIe x1 is operational (defaults)
High = SDVO and PCIe x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 1 30MIL TP204

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub



Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U6I	AC41	VSS_0	AK34
	AA41	VSS_1	AG34
	WA1	VSS_2	AF34
	TA1	VSS_3	AE34
	PA1	VSS_4	AC34
	MA1	VSS_5	C34
	JA1	VSS_6	AW33
	FA1	VSS_7	AV33
	AV40	VSS_8	AR33
	AP40	VSS_9	AE33
	AN40	VSS_10	AE33
	AK40	VSS_11	Y33
	AH40	VSS_12	V33
	AG40	VSS_13	T33
	AF40	VSS_14	R33
	AE40	VSS_15	M33
	AD40	VSS_16	H33
	AV39	VSS_17	G33
	AW39	VSS_18	F33
	AX39	VSS_19	D33
	AY39	VSS_20	B33
	BA39	VSS_21	AL32
	AB39	VSS_22	AH32
	AC39	VSS_23	AG32
	AD39	VSS_24	AF32
	AE39	VSS_25	AE32
	AF39	VSS_26	AC32
	AG39	VSS_27	K21
	AH39	VSS_28	J21
	AI39	VSS_29	H21
	AJ39	VSS_30	C21
	AK39	VSS_31	B32
	AL39	VSS_32	Y31
	AM39	VSS_33	AB30
	AN39	VSS_34	E30
	AO39	VSS_35	AT29
	AP39	VSS_36	AN29
	AQ39	VSS_37	AB29
	AR39	VSS_38	T29
	AS39	VSS_39	N29
	AT39	VSS_40	K29
	AU39	VSS_41	G29
	AV39	VSS_42	E29
	AW39	VSS_43	C29
	AX39	VSS_44	B29
	AY39	VSS_45	A29
	BA39	VSS_46	BA28
	AB39	VSS_47	AM28
	AC39	VSS_48	AP28
	AD39	VSS_49	AM28
	AE39	VSS_50	AD28
	AF39	VSS_51	AC28
	AG39	VSS_52	W28
	AH39	VSS_53	J28
	AI39	VSS_54	E28
	AJ39	VSS_55	AP27
	AK39	VSS_56	AM27
	AL39	VSS_57	AK27
	AM39	VSS_58	J27
	AN39	VSS_59	L15
	AO39	VSS_60	G27
	AP39	VSS_61	F27
	AQ39	VSS_62	C27
	AR39	VSS_63	B27
	AS39	VSS_64	AN26
	AT39	VSS_65	M26
	AU39	VSS_66	K26
	AV39	VSS_67	AA24
	AW39	VSS_68	D26
	AX39	VSS_69	AK25
	AY39	VSS_70	P25
	BA39	VSS_71	K25
	AB39	VSS_72	H25
	AC39	VSS_73	E25
	AD39	VSS_74	D25
	AE39	VSS_75	A25
	AF39	VSS_76	BA24
	AG39	VSS_77	AU24
	AH39	VSS_78	P13
	AI39	VSS_79	D13
	AJ39	VSS_80	AW23
	AK39	VSS_81	
	AL39	VSS_82	
	AM39	VSS_83	
	AN39	VSS_84	
	AO39	VSS_85	
	AP39	VSS_86	
	AQ39	VSS_87	
	AR39	VSS_88	
	AS39	VSS_89	
	AT39	VSS_90	
	AU39	VSS_91	
	AV39	VSS_92	
	AW39	VSS_93	
	AX39	VSS_94	
	AY39	VSS_95	
	BA39	VSS_96	

VSS

U6J	AT23	VSS_180	J11
	AN23	VSS_181	D11
	AM23	VSS_182	B11
	AH23	VSS_183	AV10
	AC23	VSS_184	AP10
	W23	VSS_185	AL10
	K23	VSS_186	AJ10
	J23	VSS_187	AG10
	F23	VSS_188	AC10
	C23	VSS_189	W10
	AA22	VSS_190	U10
	Y33	VSS_191	BA9
	G22	VSS_192	AW9
	F22	VSS_193	AR9
	E22	VSS_194	AH9
	D22	VSS_195	AB9
	A22	VSS_196	R9
	BA21	VSS_197	G9
	AV21	VSS_198	E9
	AR21	VSS_199	A9
	AN21	VSS_200	AG8
	AL21	VSS_201	AD8
	AB21	VSS_202	AA8
	Y21	VSS_203	U8
	P21	VSS_204	K8
	K21	VSS_205	C8
	J21	VSS_206	BA7
	H21	VSS_207	AV7
	C21	VSS_208	AP7
	AW20	VSS_209	AL7
	AR20	VSS_210	AJ7
	AM20	VSS_211	AH7
	AK20	VSS_212	AG7
	B20	VSS_213	AD6
	A20	VSS_214	AB6
	AN19	VSS_215	Y6
	E30	VSS_216	U6
	W19	VSS_217	N6
	K19	VSS_218	K6
	G19	VSS_219	H6
	C19	VSS_220	G6
	AH18	VSS_221	AG6
	K29	VSS_222	AD6
	H18	VSS_223	AB6
	D18	VSS_224	Y6
	A18	VSS_225	U6
	AY17	VSS_226	N6
	AR17	VSS_227	K6
	AP17	VSS_228	H6
	AM17	VSS_229	AG6
	AK17	VSS_230	AD6
	AV16	VSS_231	AB6
	AN16	VSS_232	Y6
	AL16	VSS_233	U6
	J16	VSS_234	N6
	F16	VSS_235	K6
	W28	VSS_236	H6
	C16	VSS_237	AG6
	AN15	VSS_238	AD6
	AM15	VSS_239	AB6
	AK15	VSS_240	Y6
	N15	VSS_241	U6
	M15	VSS_242	N6
	L15	VSS_243	K6
	G27	VSS_244	H6
	F27	VSS_245	AG6
	C27	VSS_246	AD6
	B27	VSS_247	AB6
	AN26	VSS_248	Y6
	M26	VSS_249	U6
	K26	VSS_250	N6
	AA24	VSS_251	K6
	D26	VSS_252	H6
	AK25	VSS_253	AG6
	P25	VSS_254	AD6
	K25	VSS_255	AB6
	H25	VSS_256	Y6
	E25	VSS_257	U6
	D25	VSS_258	N6
	A25	VSS_259	K6
	BA24	VSS_260	H6
	AU24	VSS_261	AG6
	P13	VSS_262	AD6
	D13	VSS_263	AB6
	AW23	VSS_264	Y6
		VSS_265	U6
		VSS_266	N6
		VSS_267	K6
		VSS_268	H6
		VSS_269	AG6
		VSS_270	AD6
		VSS_271	AB6
		VSS_272	Y6

VSS

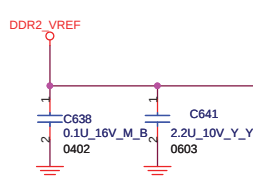
CALISTOGA

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Title CALISTOGA(VSS) 7 of 7

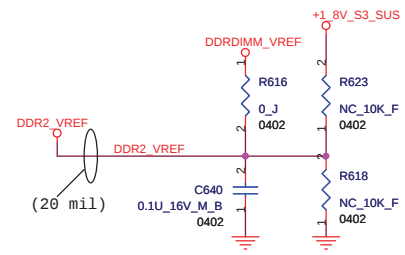
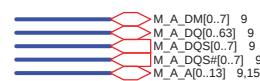
Size A3 Document Number MS51(MBX-152) Rev 0.30

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0.1 uF and 2.2 uF placed close to VREF pins

1.8V per DIMM=3.08A



Close to DIMM

7,15 M_CKE0

9,15 M_A_BS2

9,15 M_A_BS0

9,15 M_A_WE#

9,15 M_A_CAS#

7,15 M_CS#1

7,15 M_ODT1

M_A A12

M_A A9

M_A A8

M_A A5

M_A A3

M_A A1

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

M_A A10

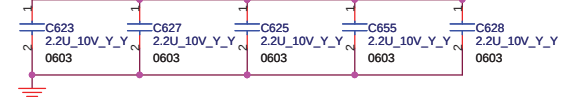
PC2-4300 DDR2
SDRAM SO-DIMM
(200P)
9.2mm

DIMM_0

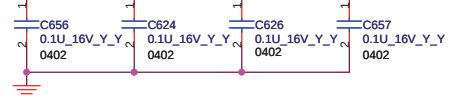
PM_EXTTS#0 7,14

SMBus Address: A0(W)/A1(R)

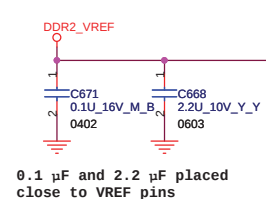
Place these Caps near So-Dimm0.



Place these Caps near So-Dimm0.

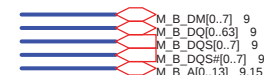


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Title DDR(II)SO-DIMM_0			
Size A3	Document Number	Rev 0.30	
MS51(MBX-152)			
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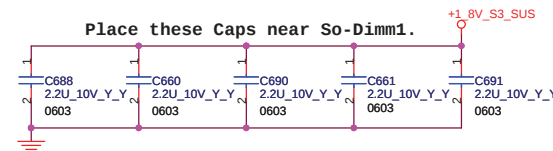


0.1 uF and 2.2 uF placed close to VREF pins

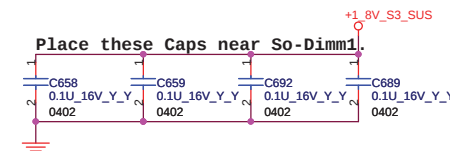
1.8V per DIMM=3.08A



Place these Caps near So-Dimm1.

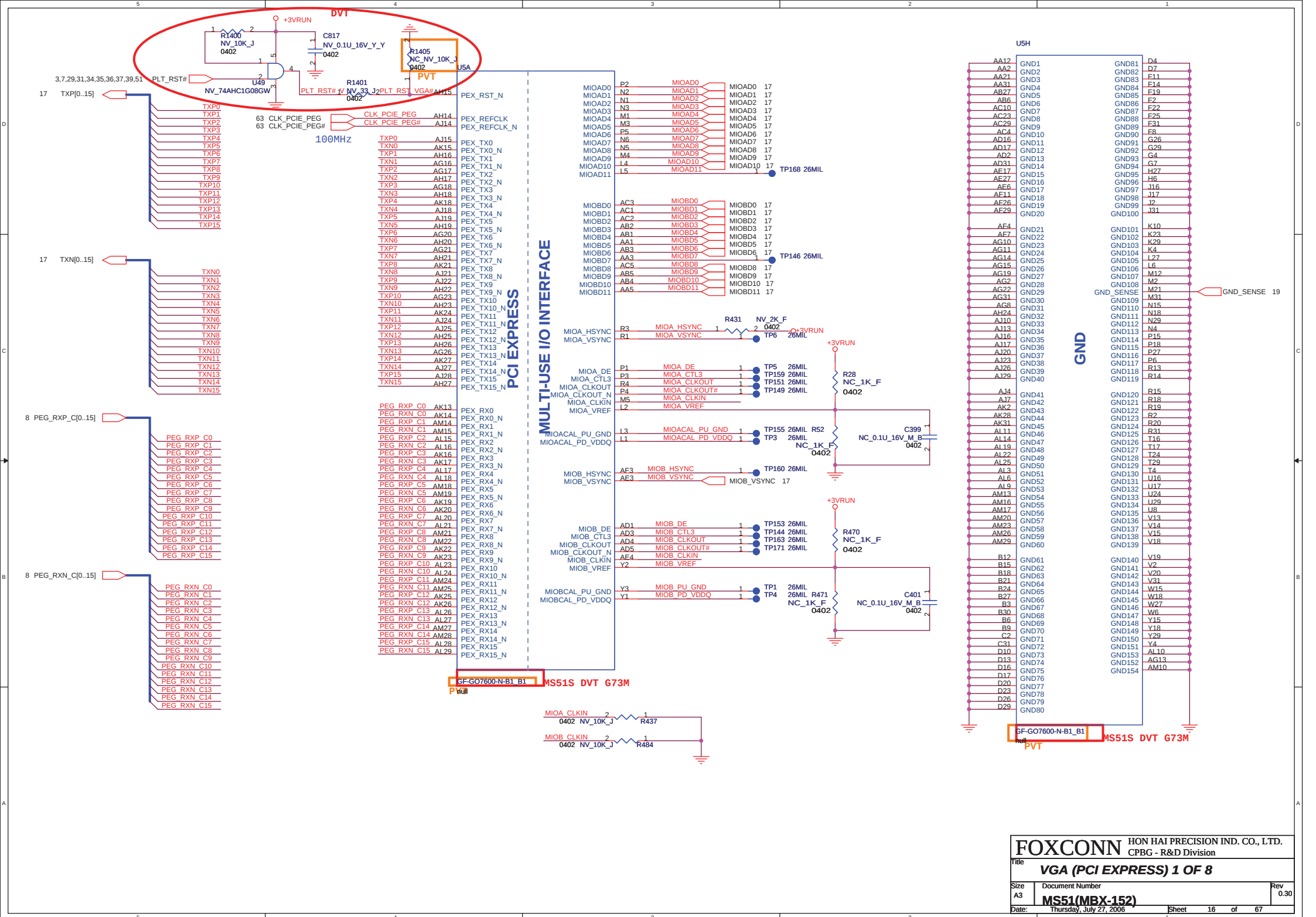


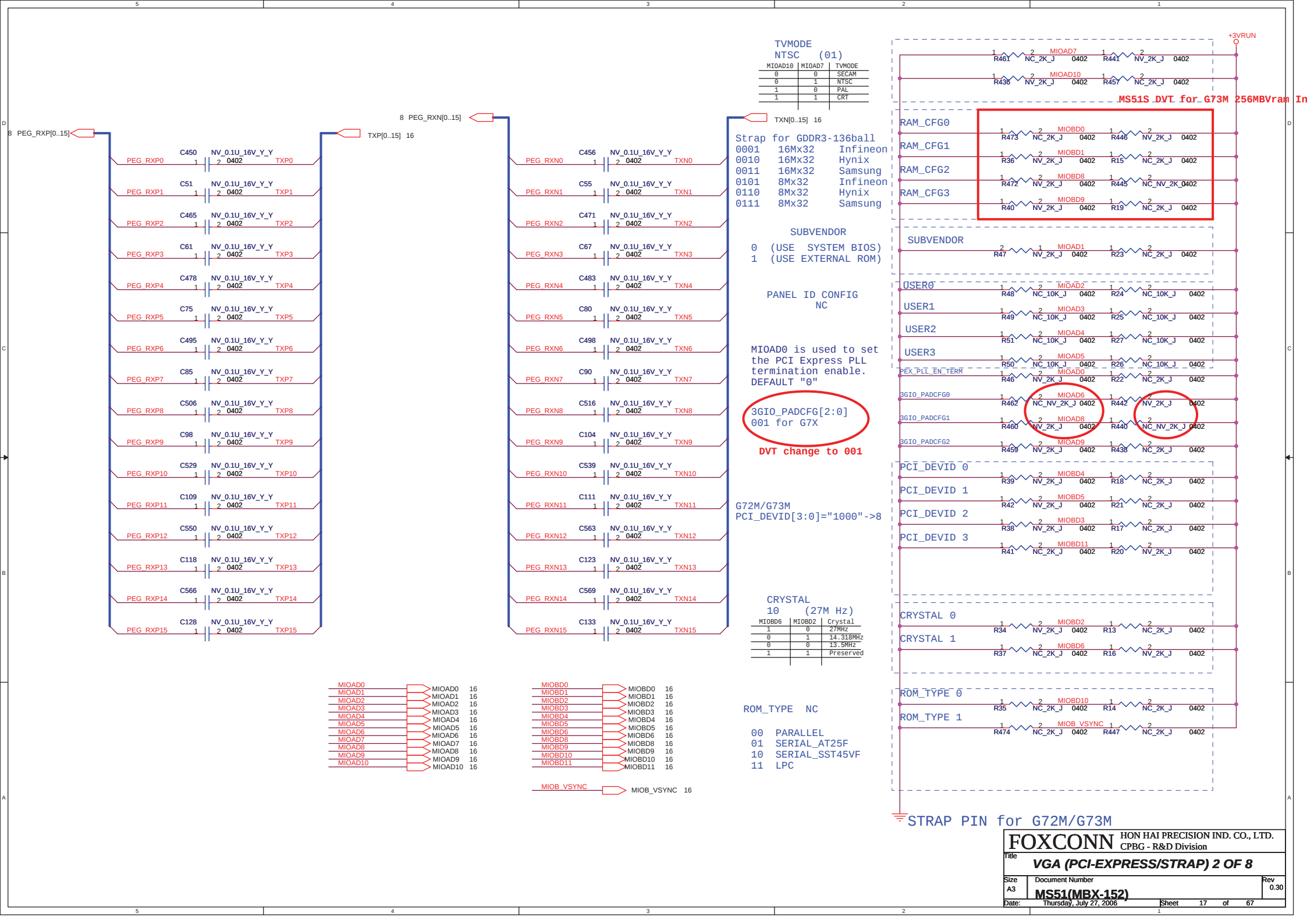
Place these Caps near So-Dimm1.



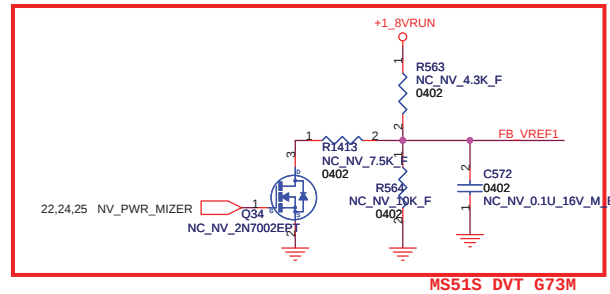
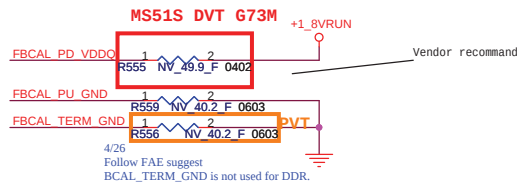
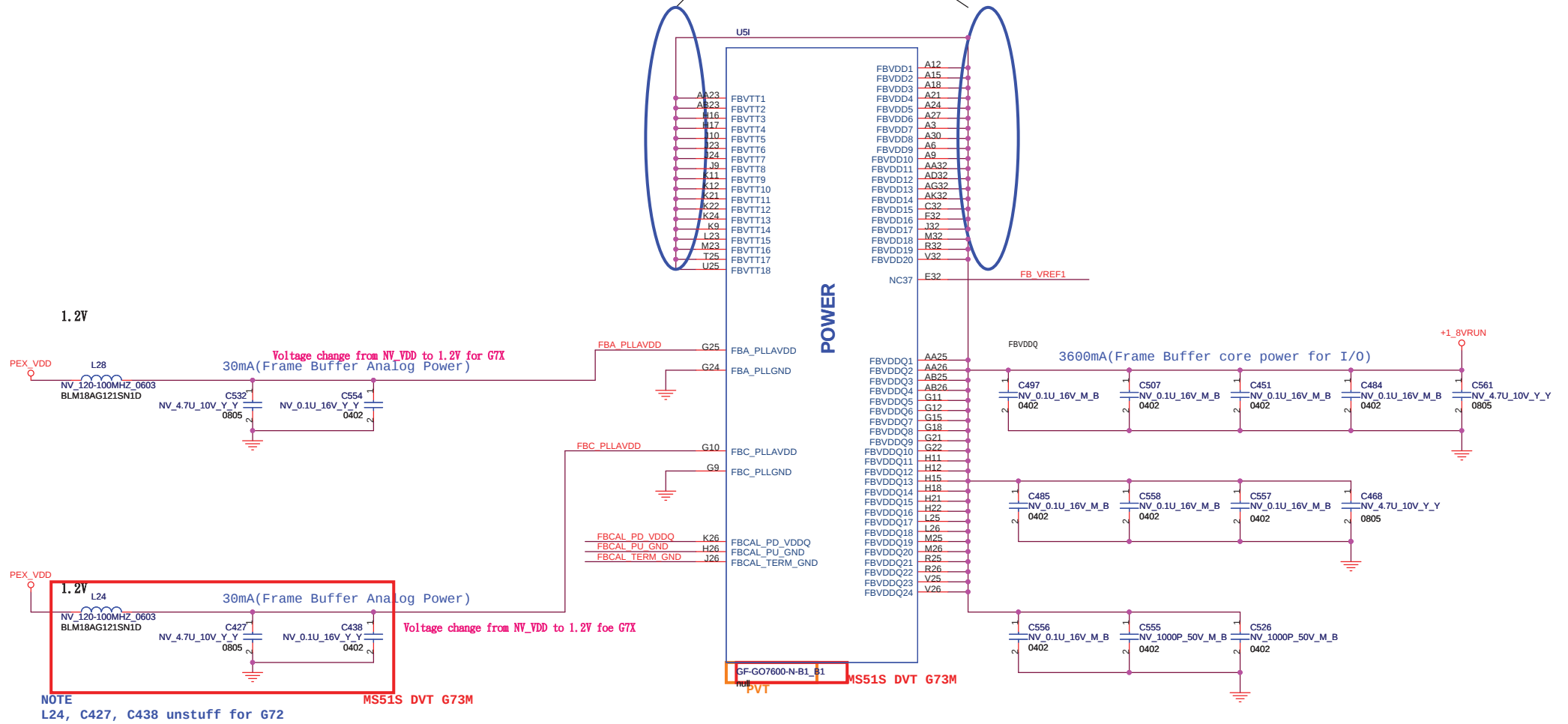
SMBus Address: A4(W)/A5(R)

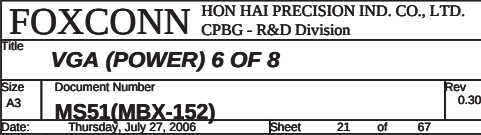
DIMM_1

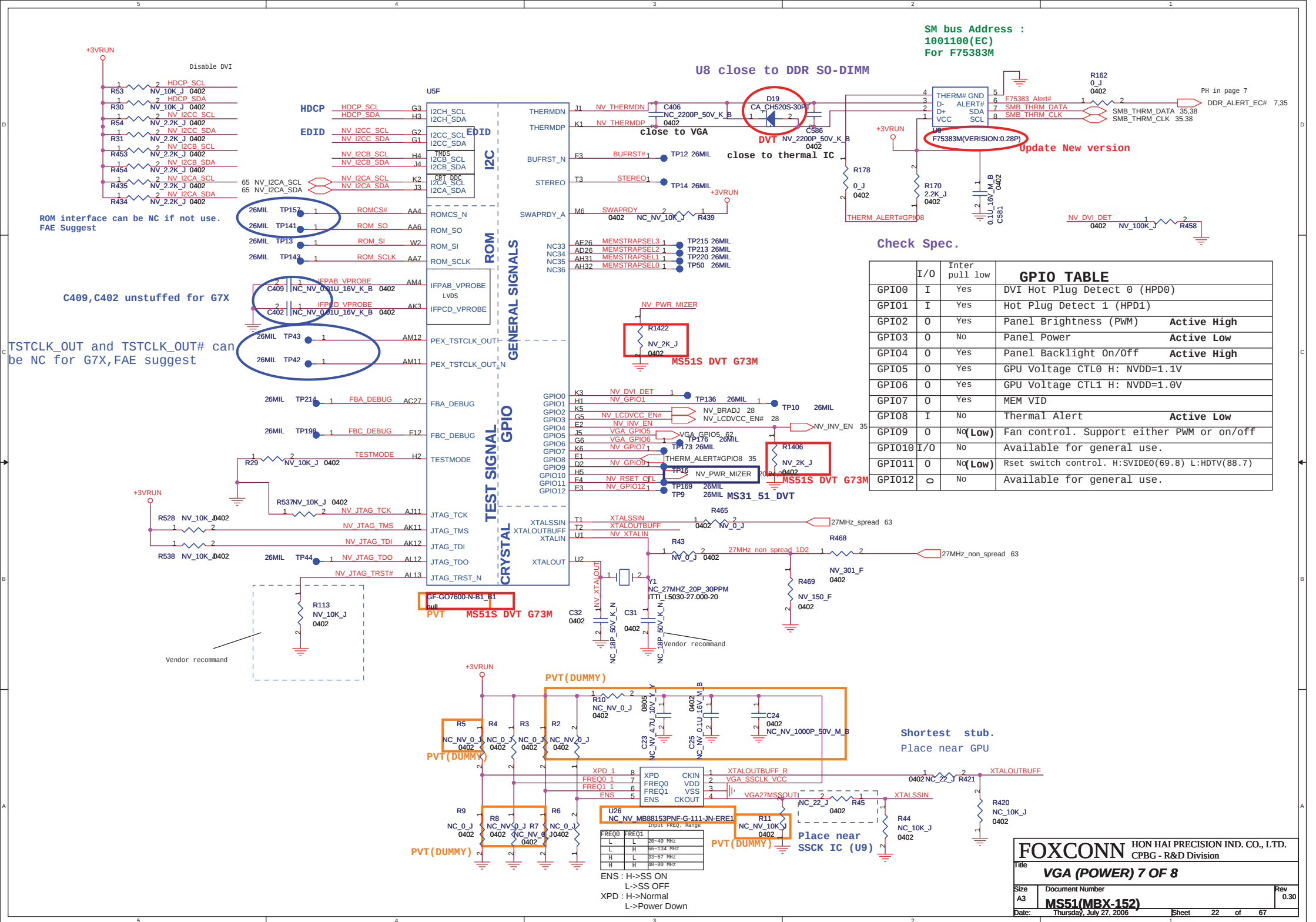


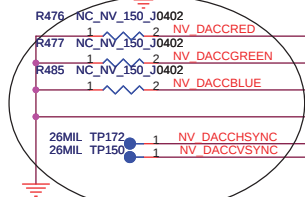


Follow FAE suggest the design guide table 4-4 and 4-5.
 DDR1 undermined solution,so FBVTT/FBVDQ/FBVDQ can connect together.
 for the power rails decoupling,FBVTT/FBVDQ do not require caps decoupling.
 only FVDDQ power rail required.



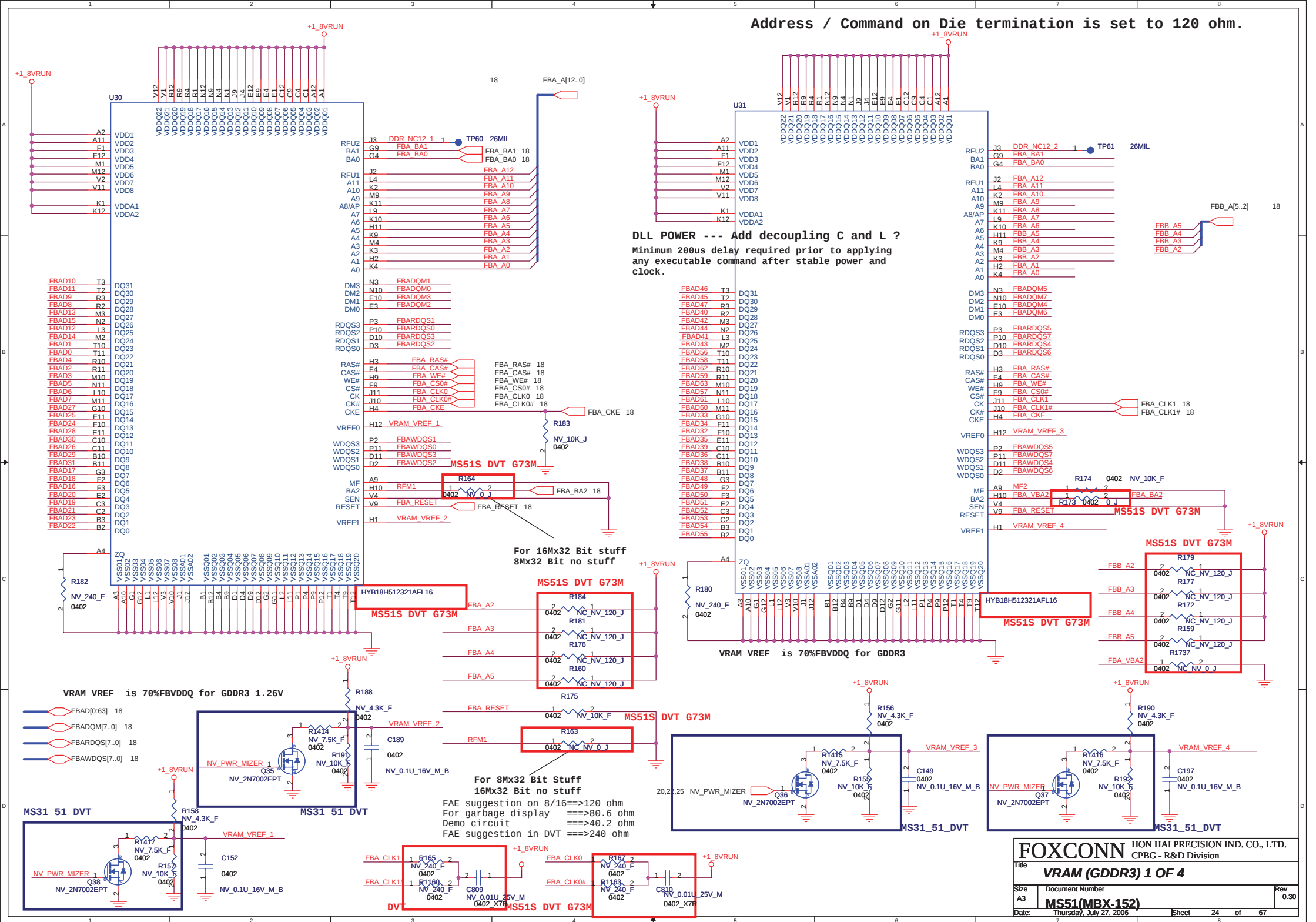


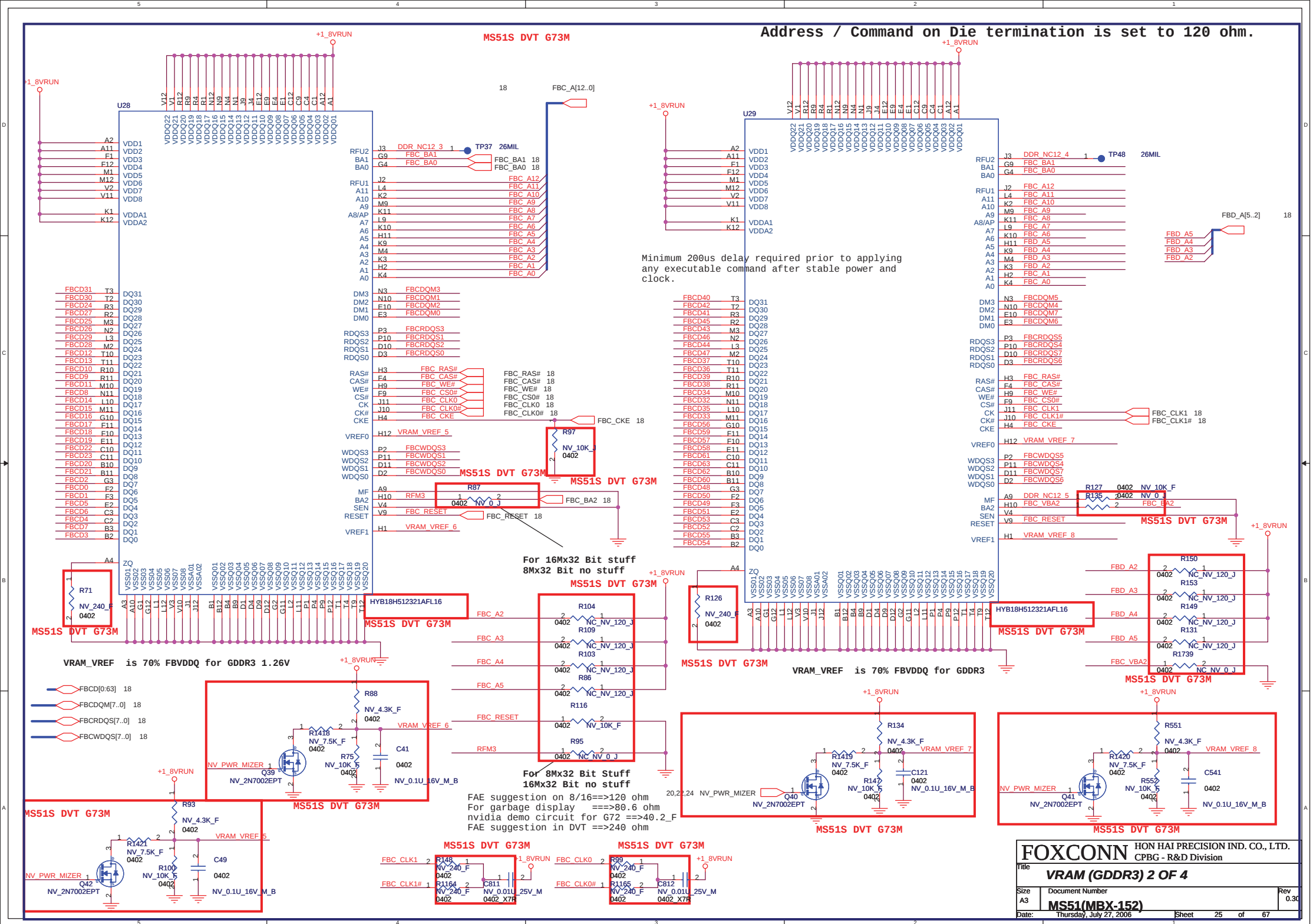


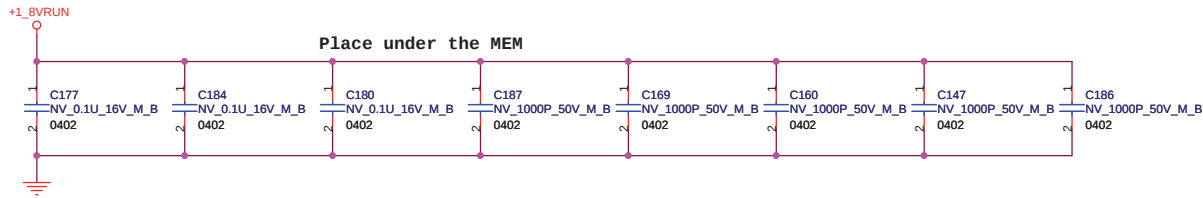
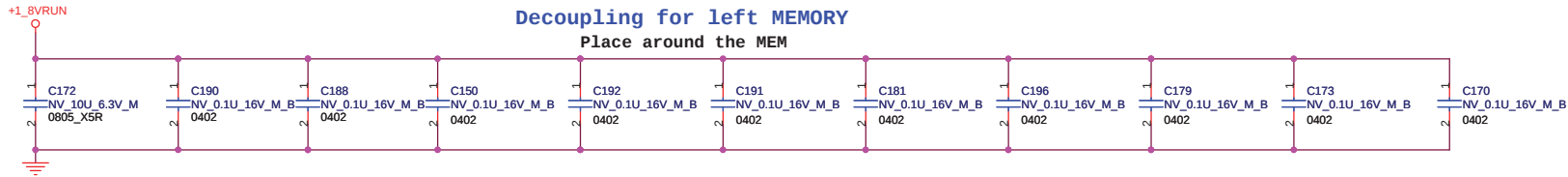
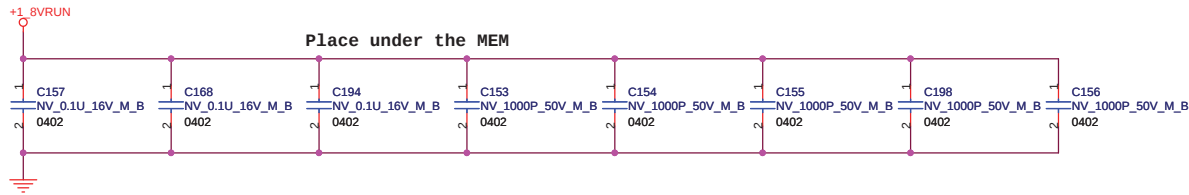
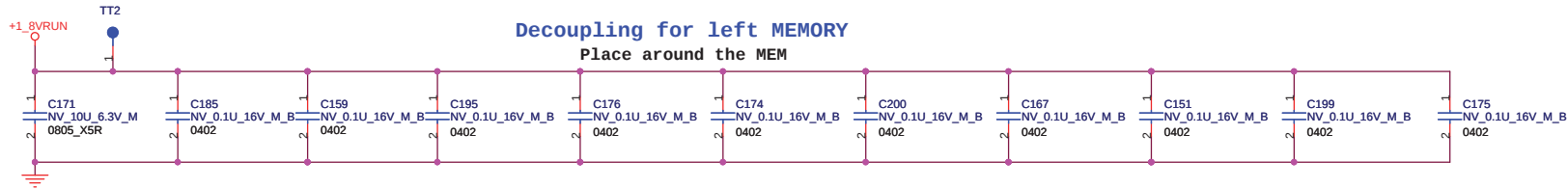


DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDBCLK			SCL
	VGA-DDBDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CB
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITEB		
			LINE1	
			LINE2	SCL
			LINE3	SDA
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDBCLK			SCL
	DVI-DDBDATA			SDA

Address / Command on Die termination is set to 120 ohm.

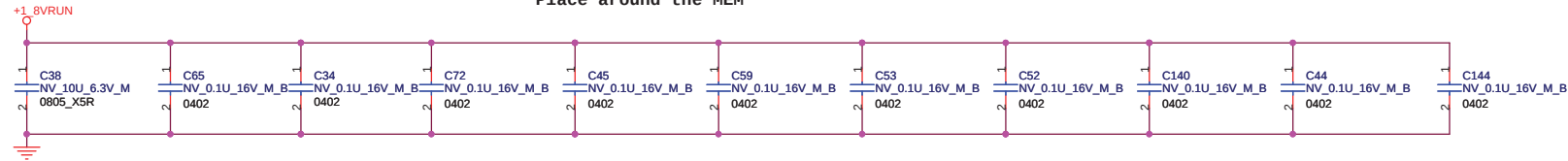






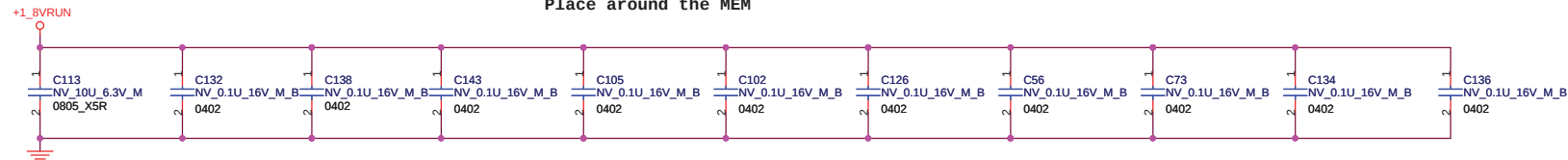
Decoupling for right MEMORY

Place around the MEM

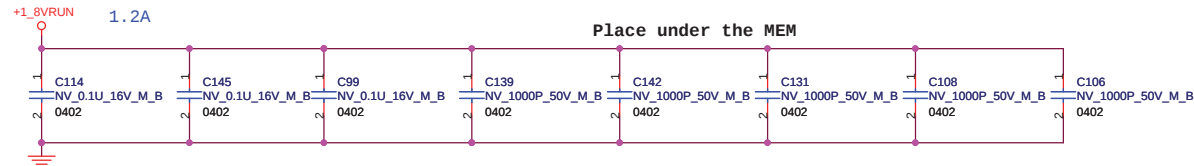


Decoupling for right MEMORY

Place around the MEM

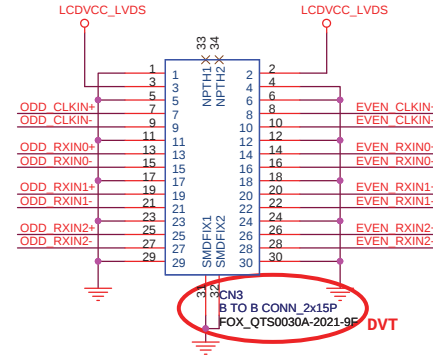
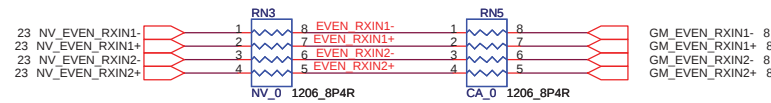
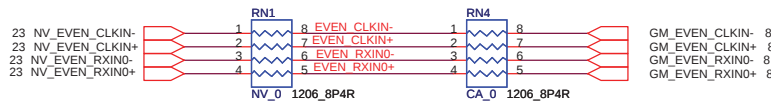
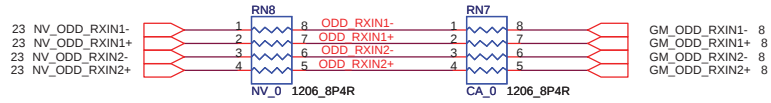


Place under the MEM

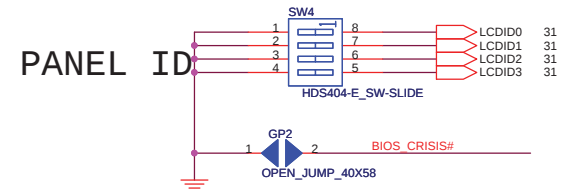
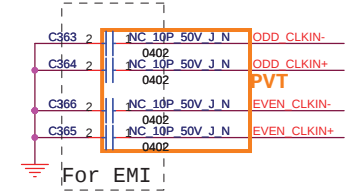


MS51S DVT 673M

LVDS

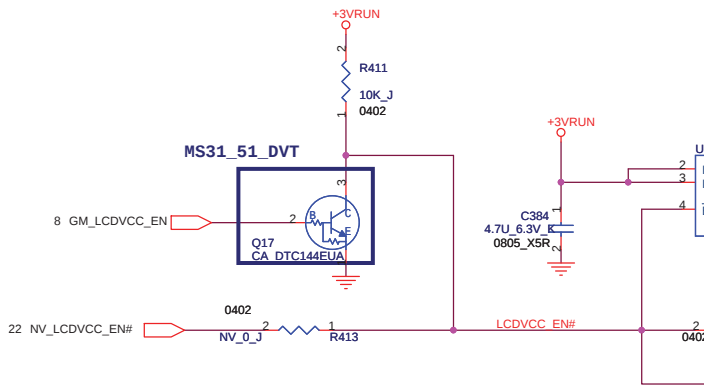


LVDS CONNECTOR

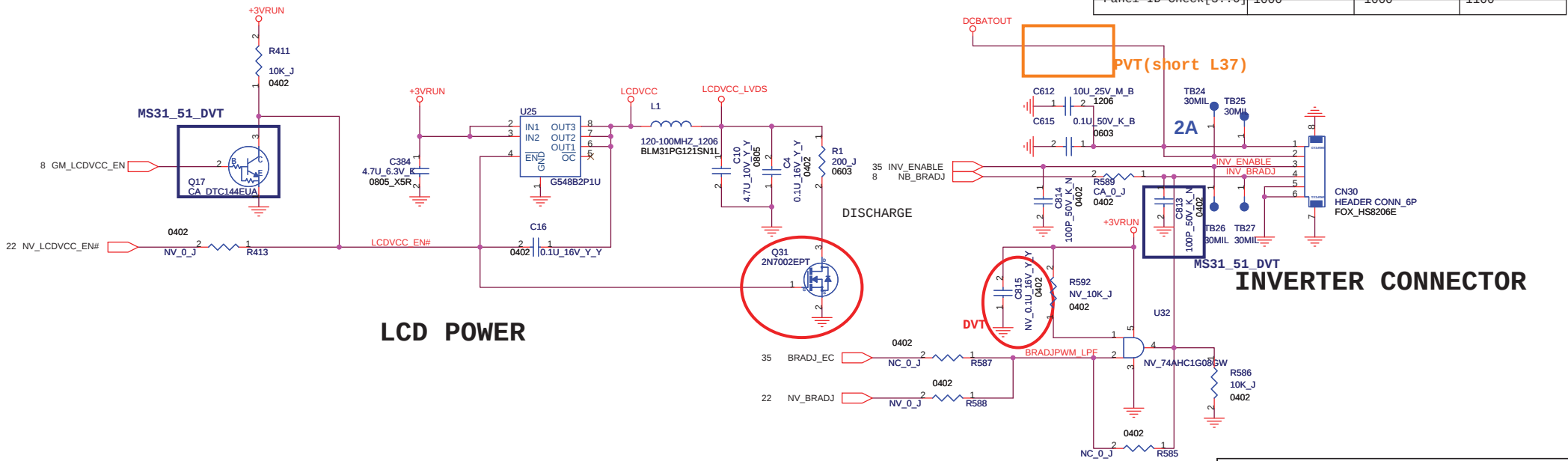


ON=0

Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vendor	Hitachi	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC16AA	TX39D90VC1GAA
Panel ID Check[3..0]	1000	1000	1100



LCD POWER

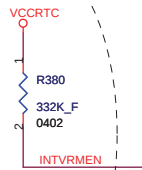
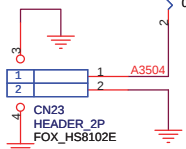
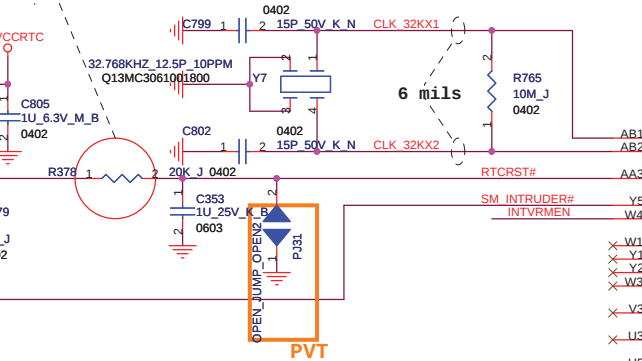
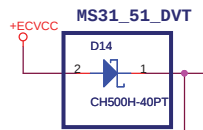


RTCRST#

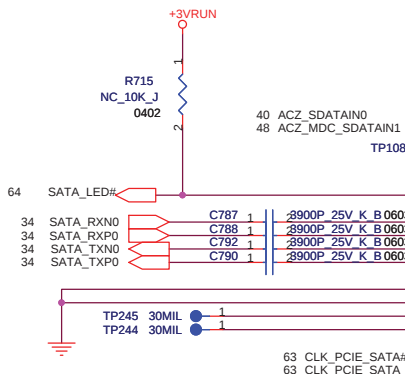
VccRTC

Min :
5ms

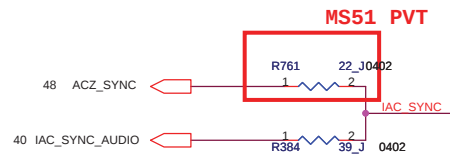
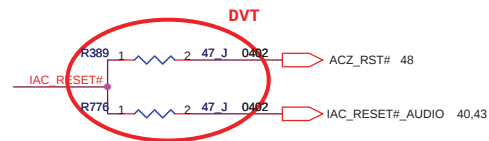
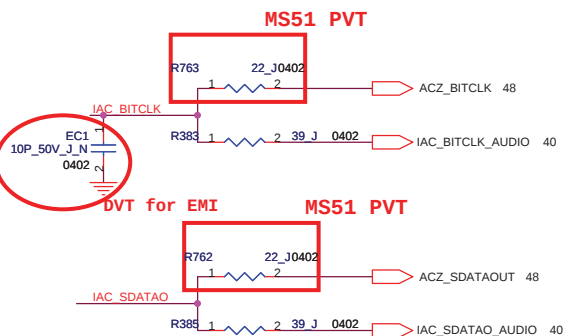
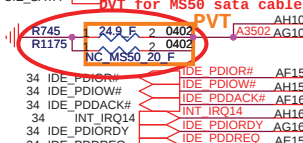
The traces inside this
block should be wider.
No digital signals routed
under XTAL



Pull-up to enable
internal VccSus1_05
regular
Pull-Low to disable



Distance between the ICH-7M
and C on the "p" signal
should be identical distance
between the ICH-7M and C on
the "N" signal for same pair



U44A

RTCX1
RTCX2

RTCRST#

INTRUDER#
INTVRMEN

EE_CS
EE_SHCLK
EE_DOUT
EE_DIN

LAN_CLK

LAN_RSTSYNC

LAN_RXD0
LAN_RXD1
LAN_RXD2

LAN_TXD0
LAN_TXD1
LAN_TXD2

ACZ_BIT_CLK
ACZ_SYNC

IAC_RESET#

ACZ_RST#

ACZ_SDAIN0
ACZ_MDC_SDAIN1
TP ACZ_SDIN2

IAC_SDATA0

SATALED#

SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0

SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP

SATA_CLKN
SATA_CLKP

SATARBIAISN
SATARBIAISP

IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT IRQ14
IDE_PDIORDY
IDE_PDDREQ

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DIOH#
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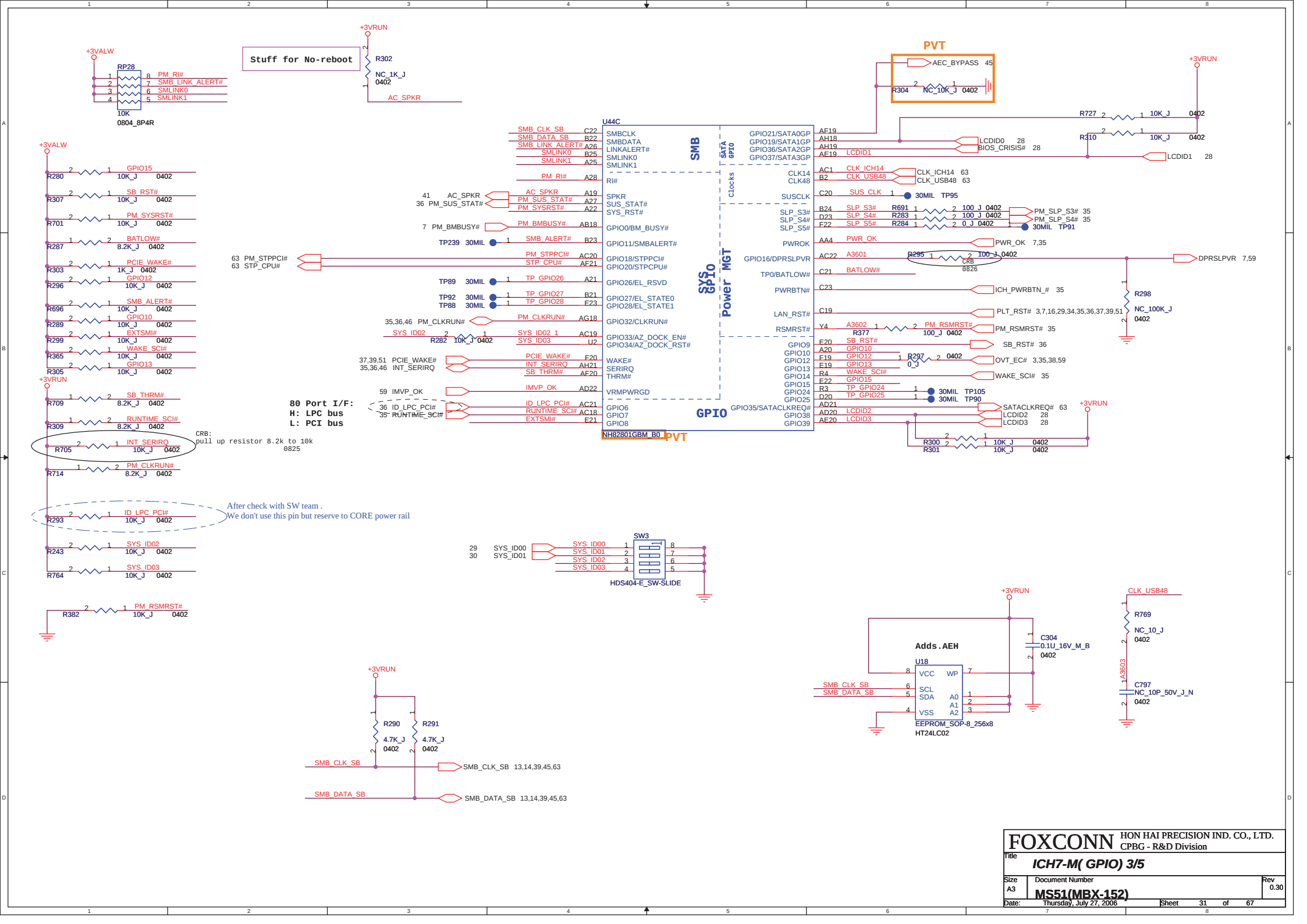
DIOR#
DIOH#
DIOH#
DIOH#
DIOH#
DIOH#

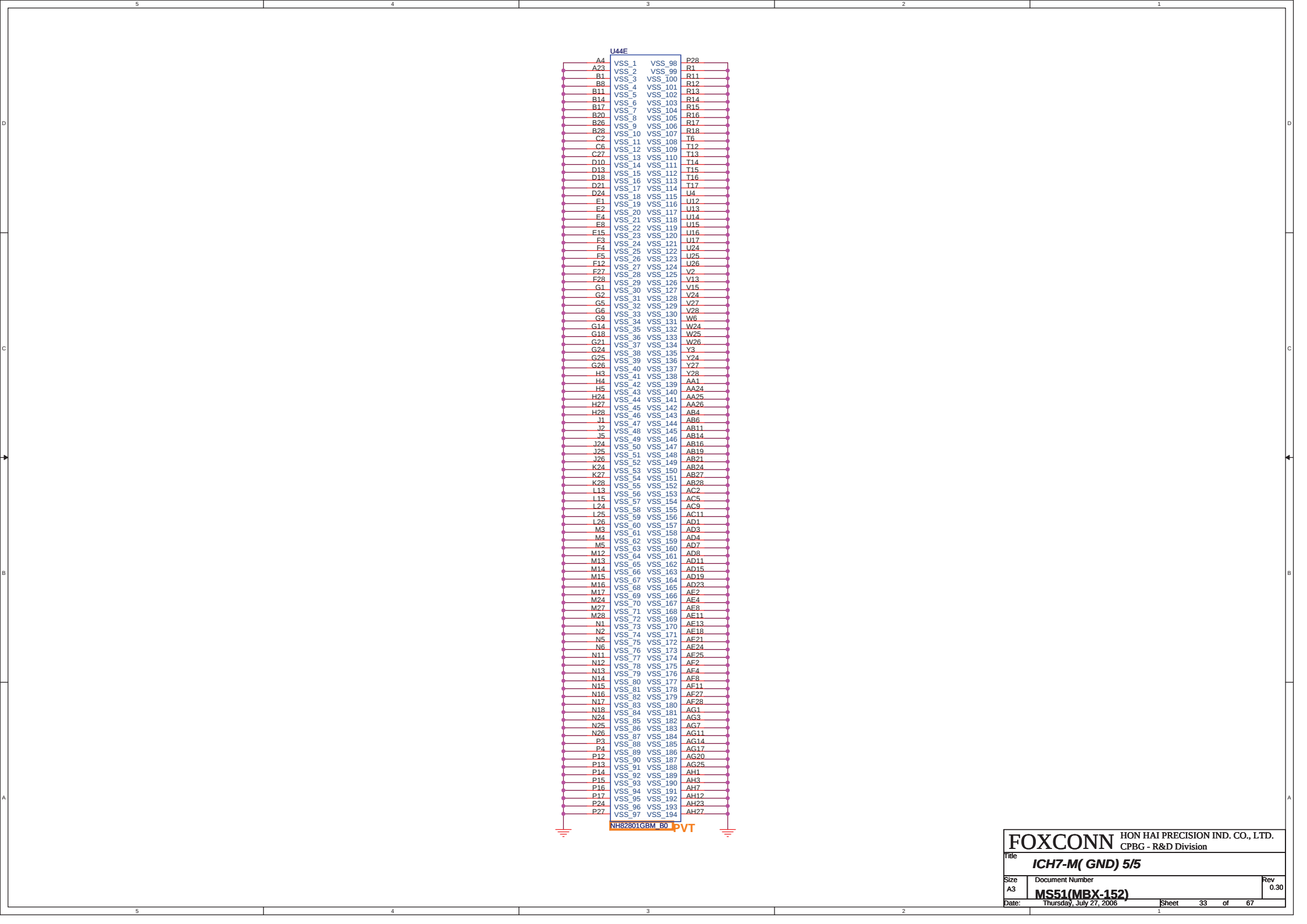
DIOR#
DIOH#
DIOH#
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DIOR#
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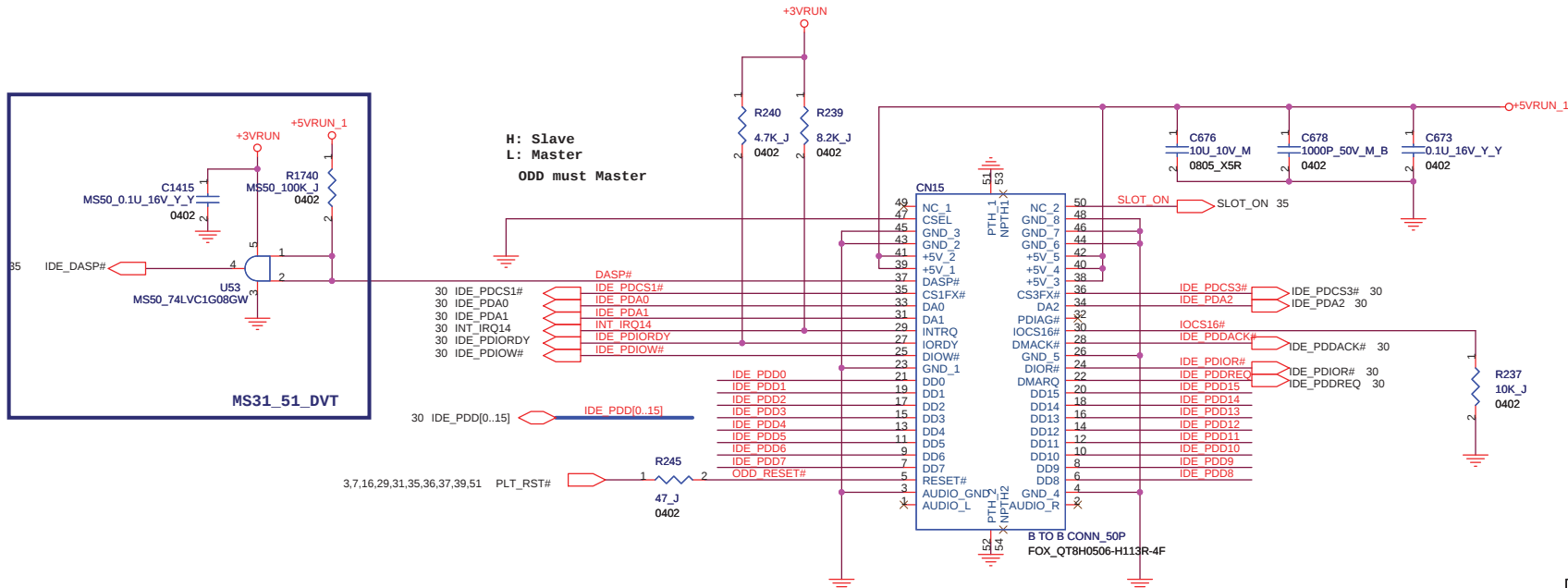
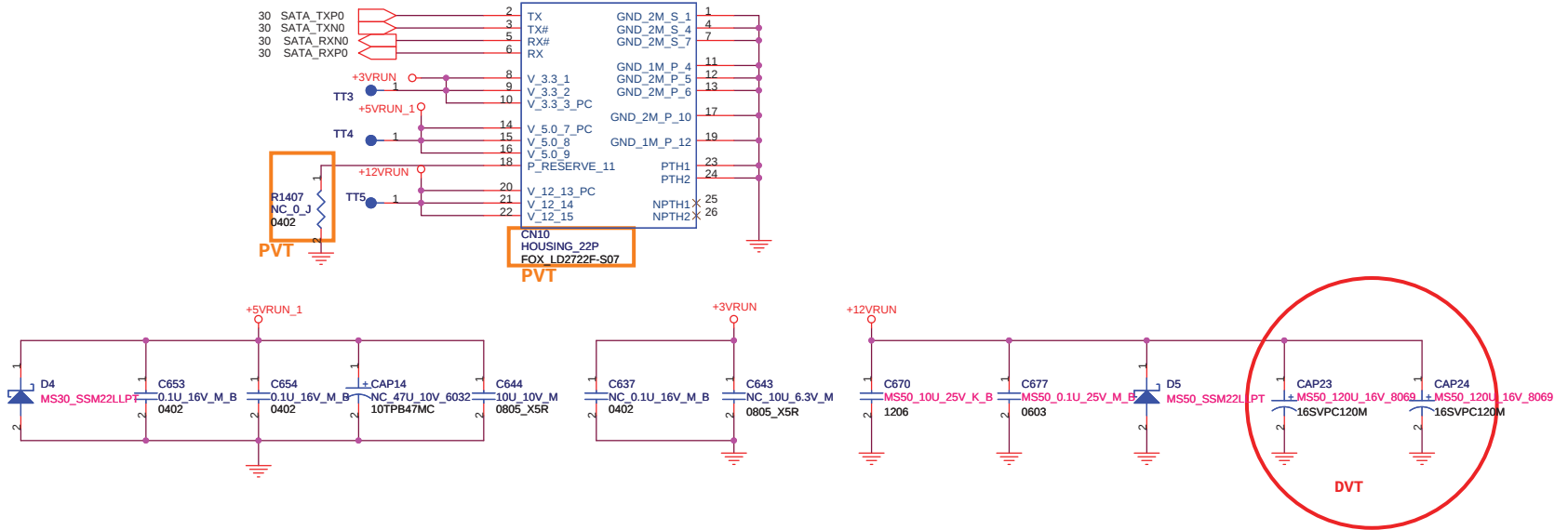
DIOR#
DIOH#
DIOH#
DIOH#
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DIOR#
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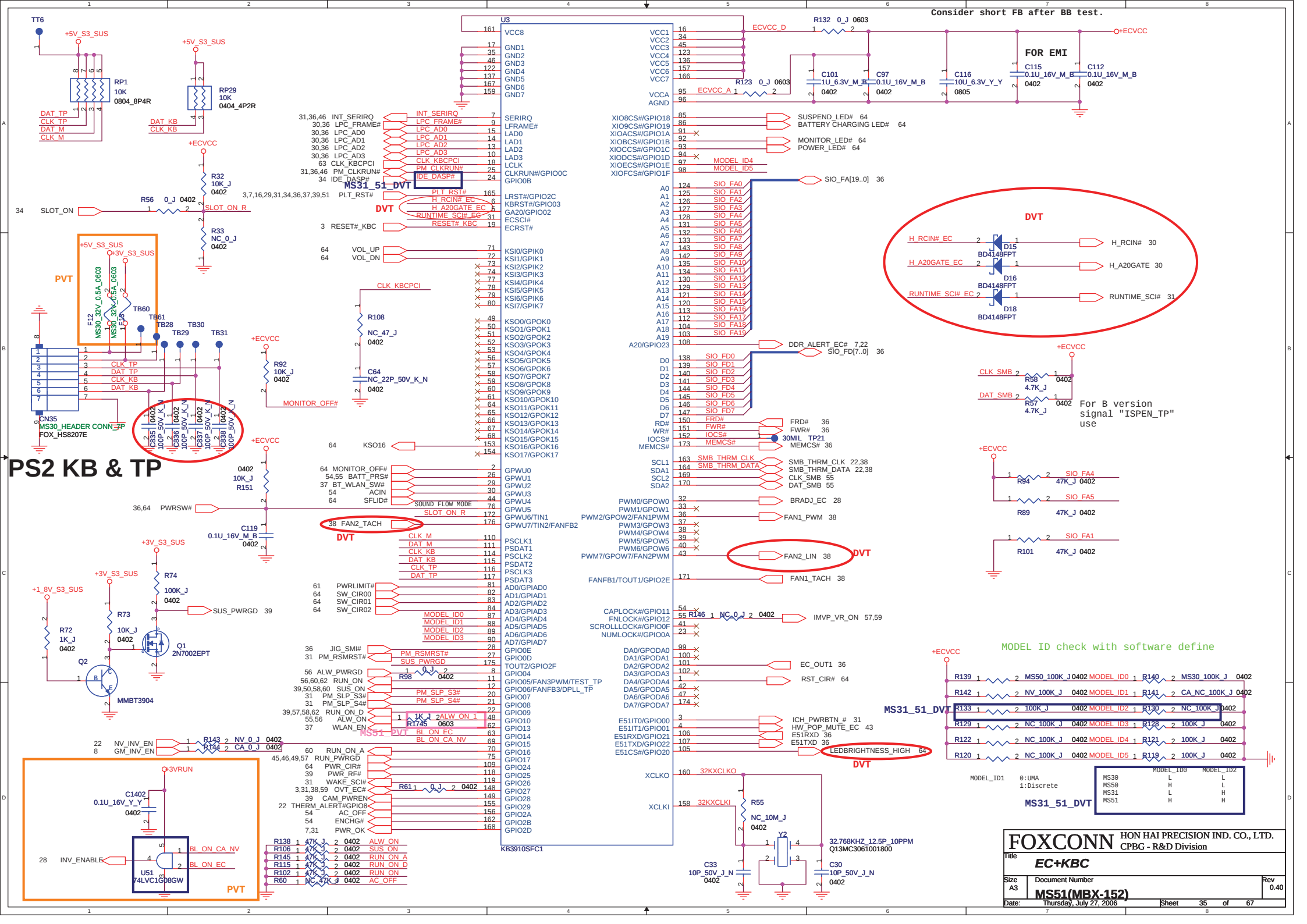


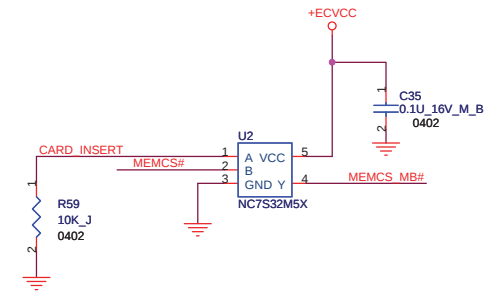
SATA HDD CONN



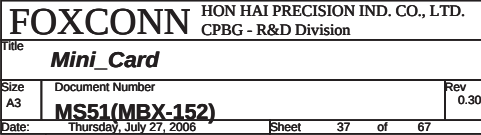
CD-ROM CONN

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		SATA HDD/CD-ROM	
Size		Document Number	
A3		MS51(MBX-152)	
Date:		Thursday, July 27, 2006	
Sheet		34 of 67	
Rev		0.30	

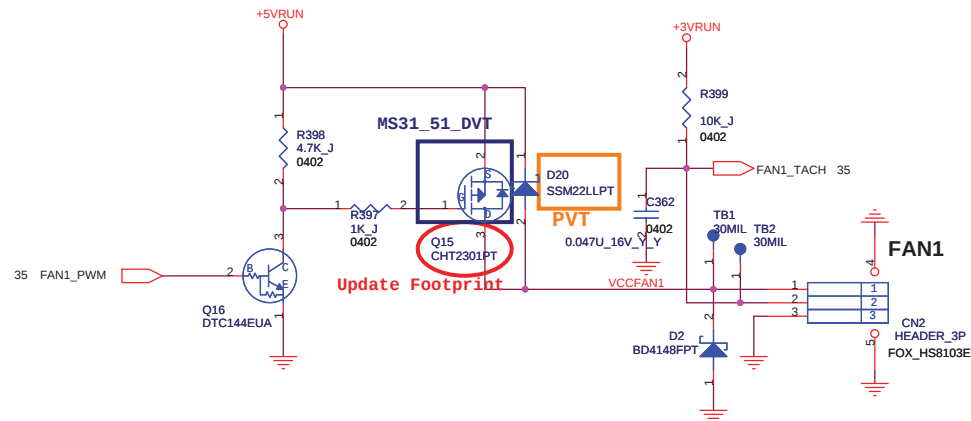




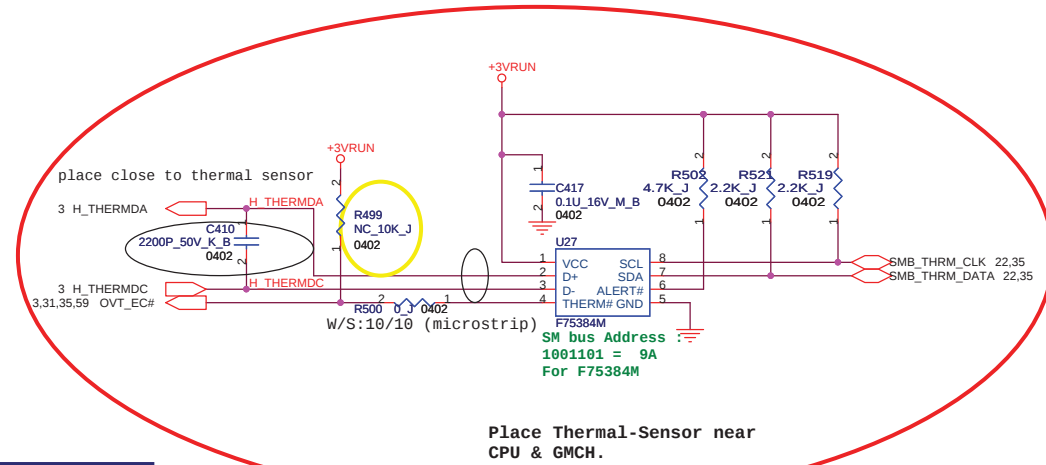
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
File		CPBG - R&D Division	
Flash ROM/X-Bus CONN			
Size A3	Document Number MS51(MBX-152)	Rev 0.40	
Date: Thursday, July 27, 2006	Sheet 36	of 67	



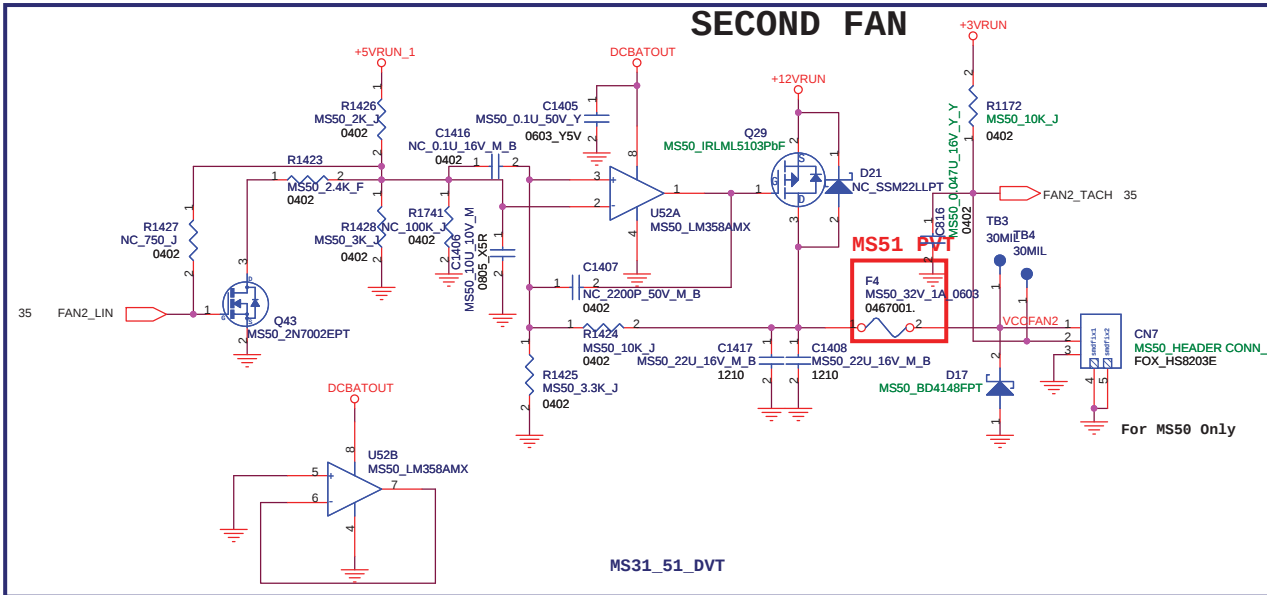
FAN



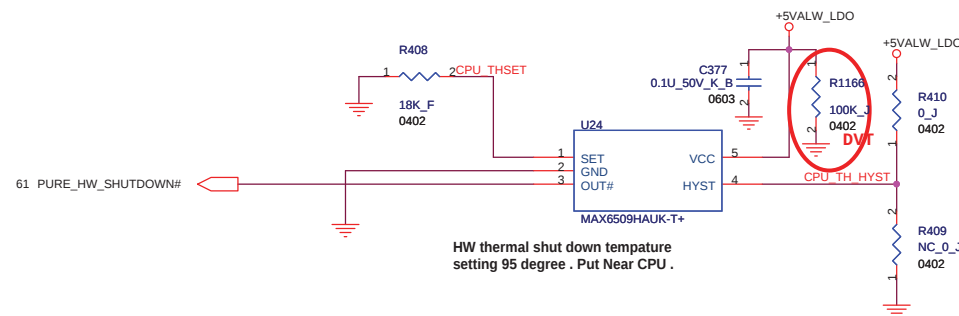
CPU SENSOR



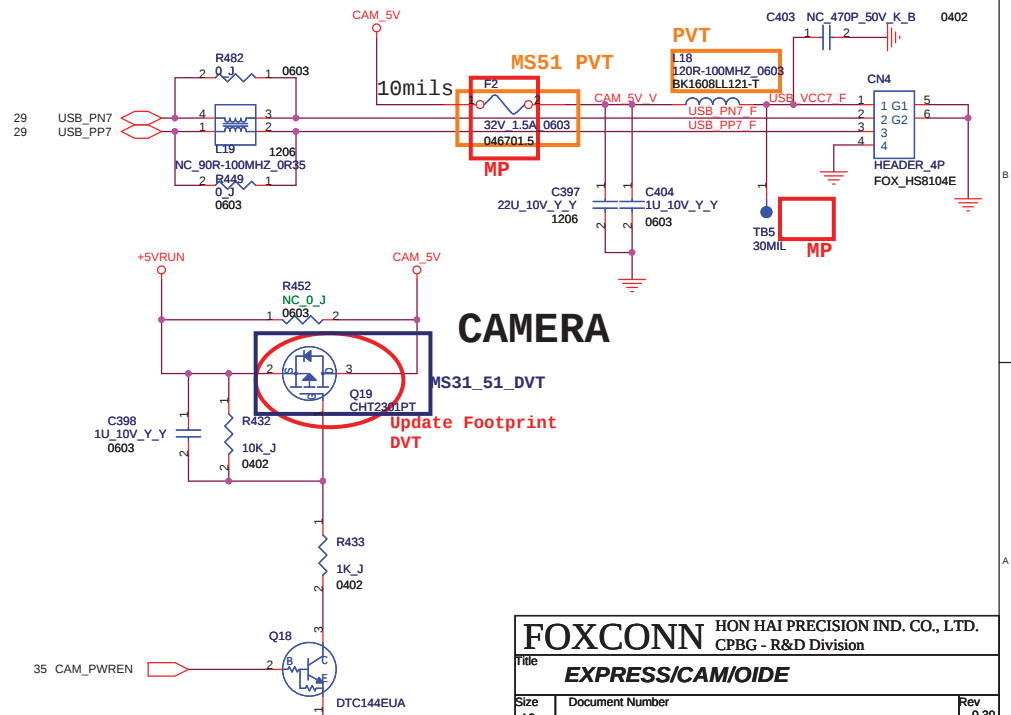
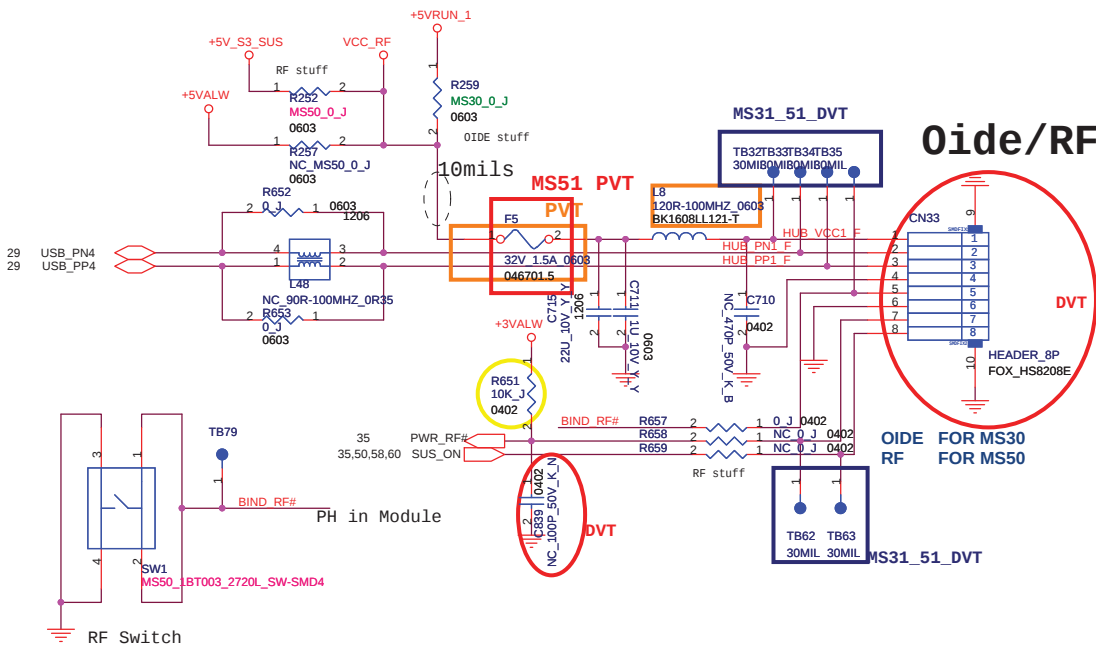
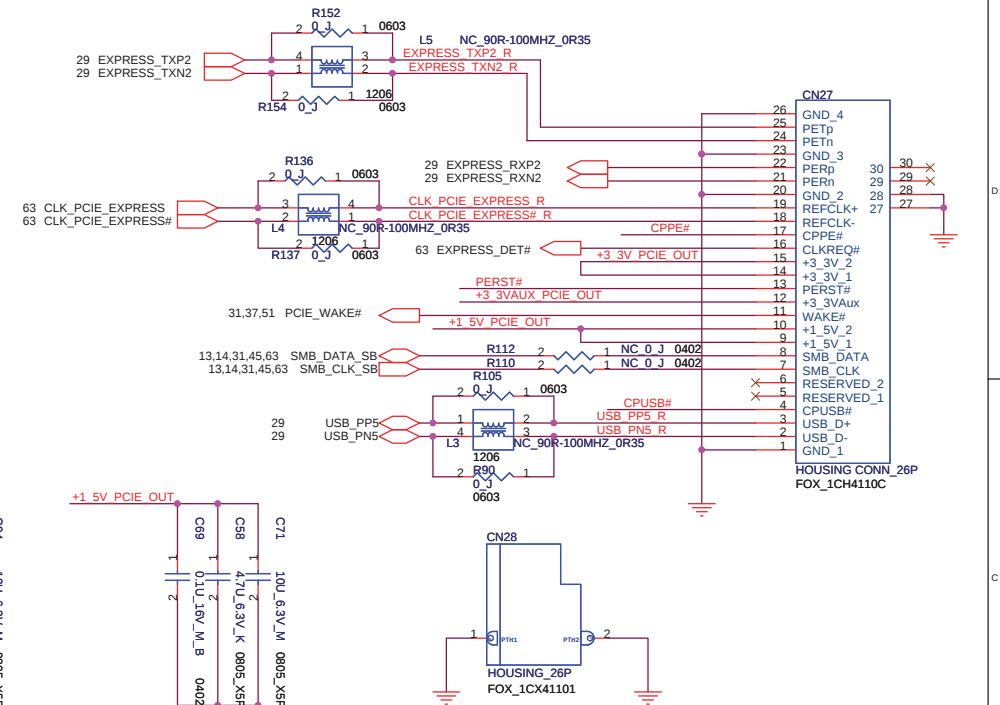
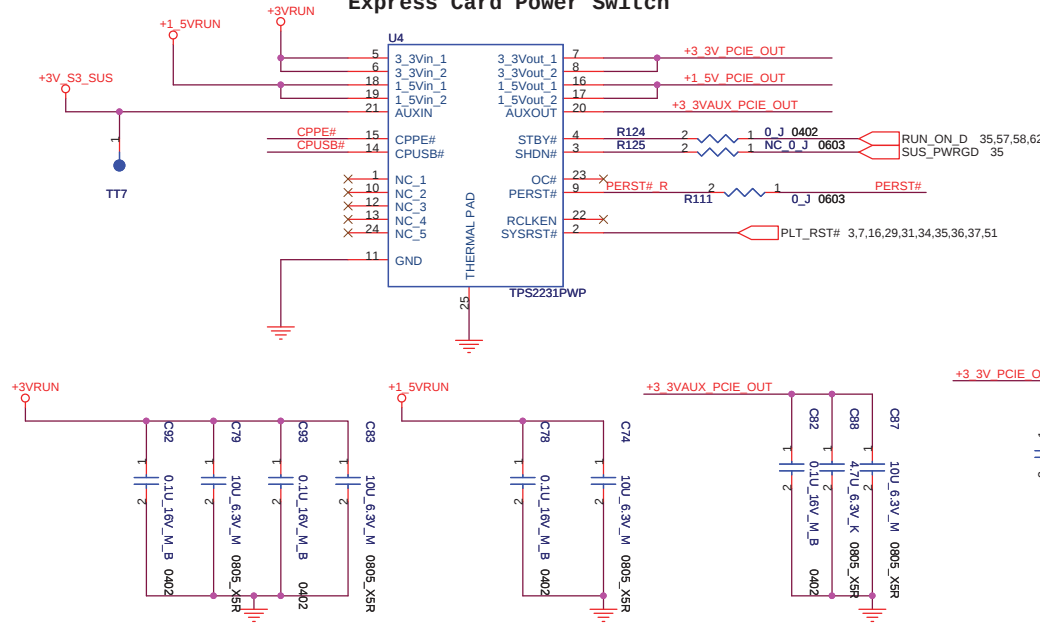
SECOND FAN

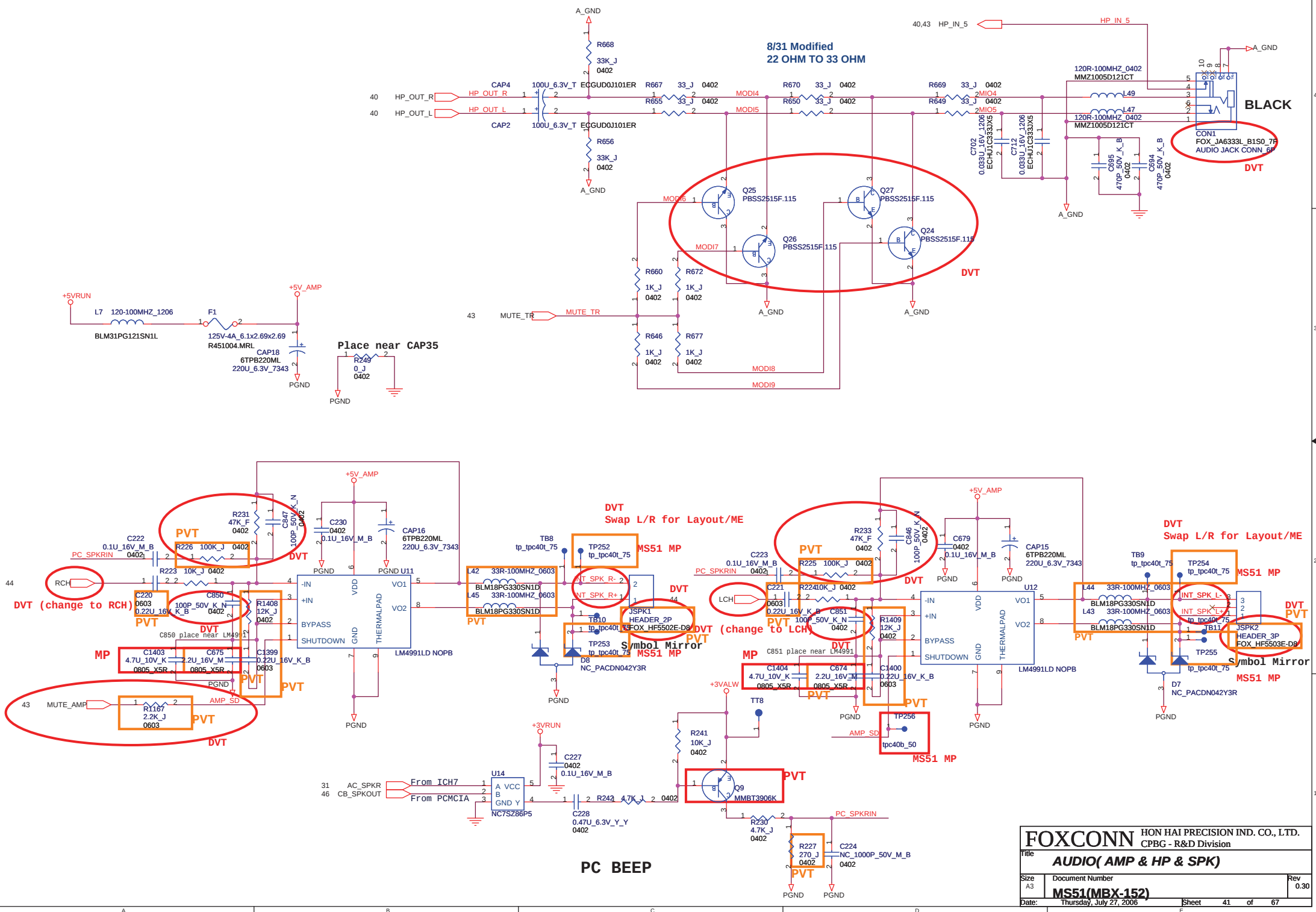


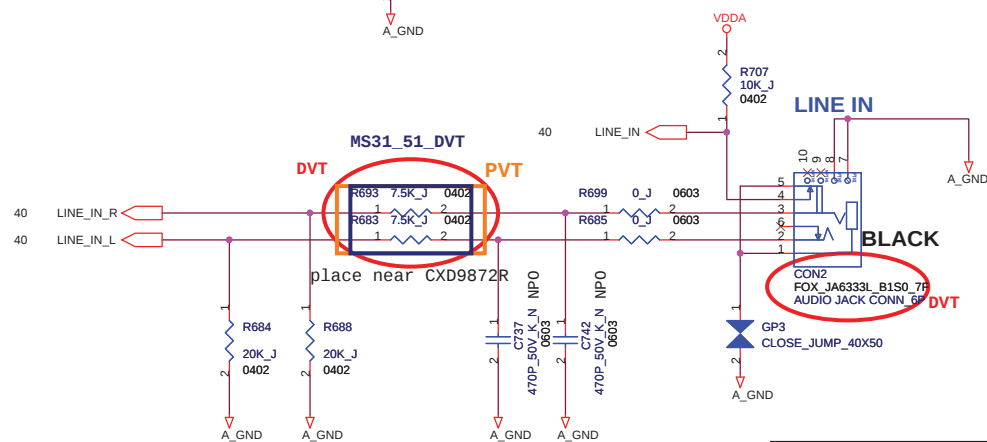
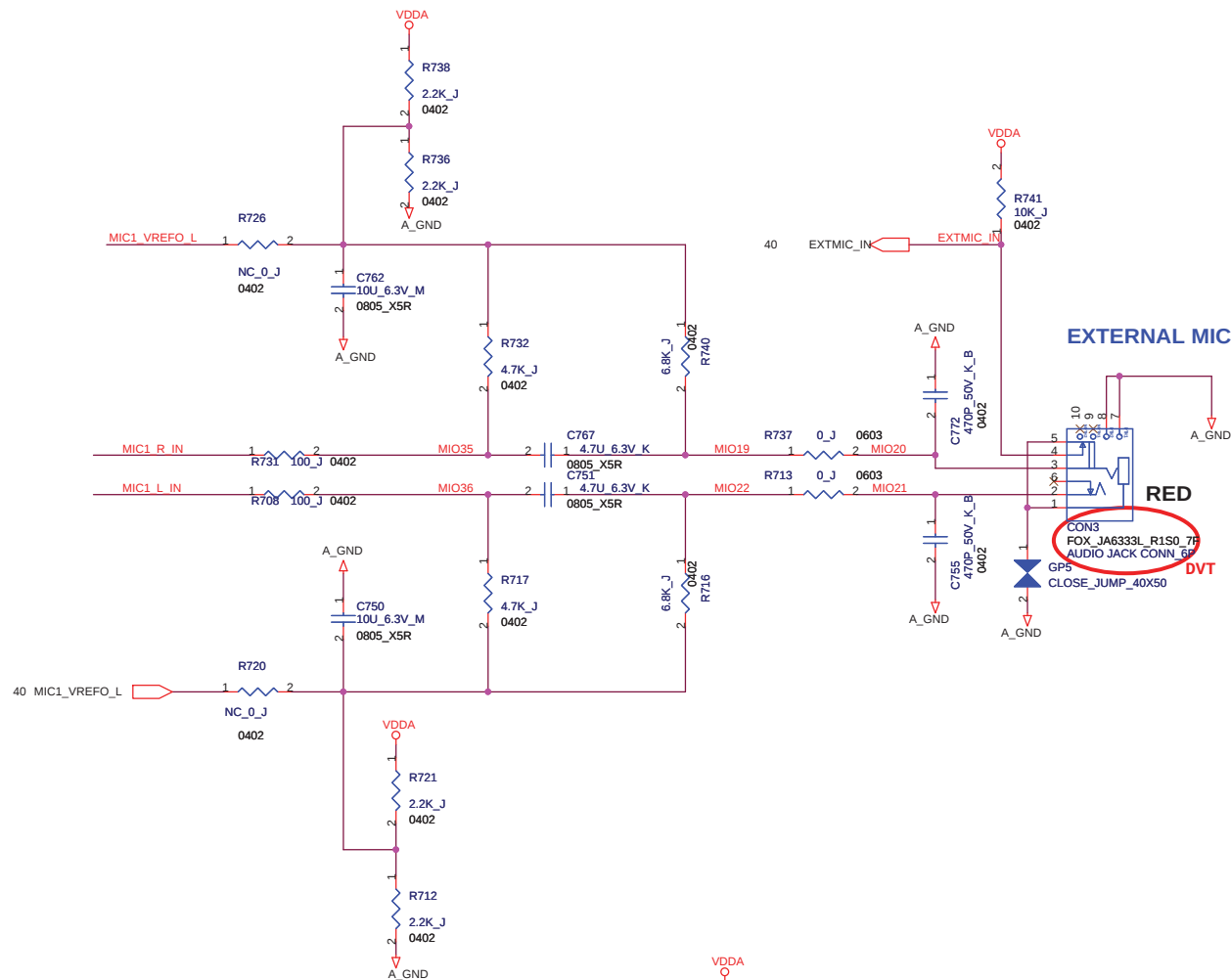
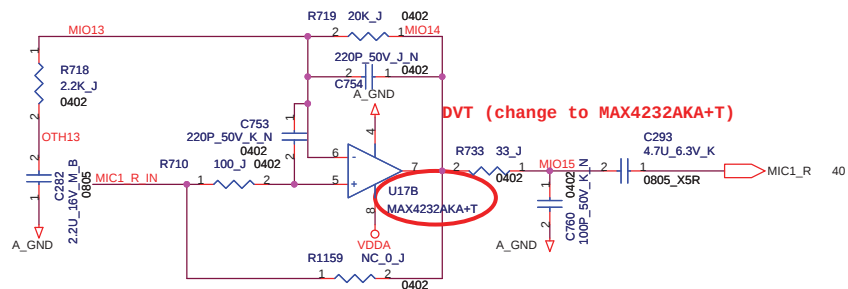
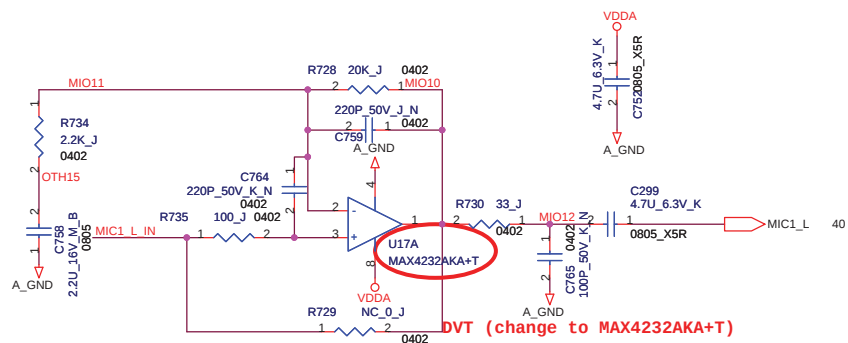
HW THERMAL PROTECTION

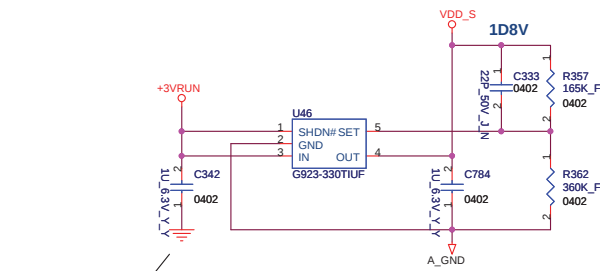


Express Card Power Switch

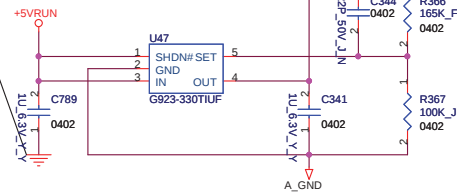




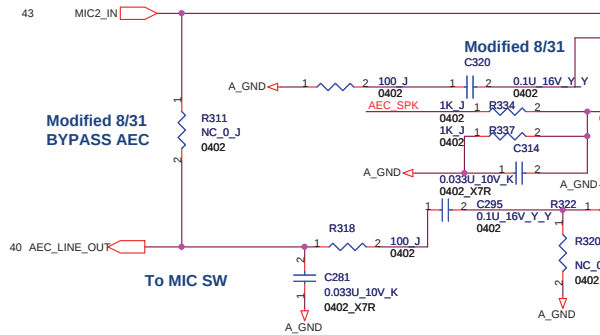




8/31 Modified
CHANGE TO D-GND



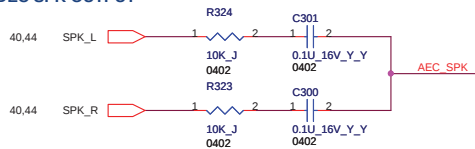
Modified 8/31
From MIC



Modified 8/31
BYPASS AEC

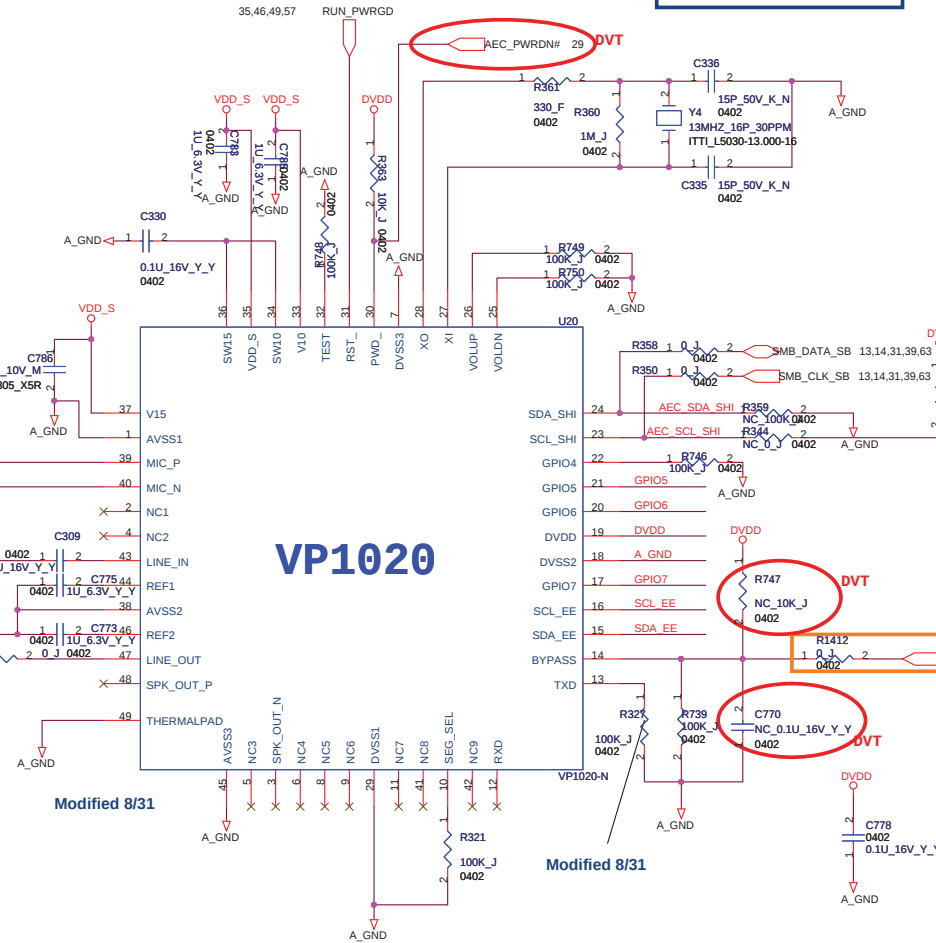
To MIC SW

To CODEC SPK OUTPUT

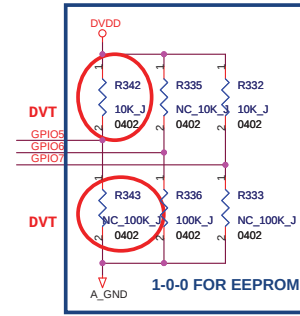


Modified 8/31

VP1020

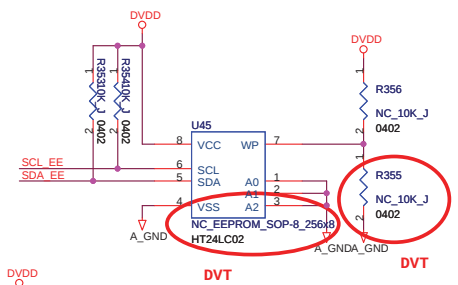


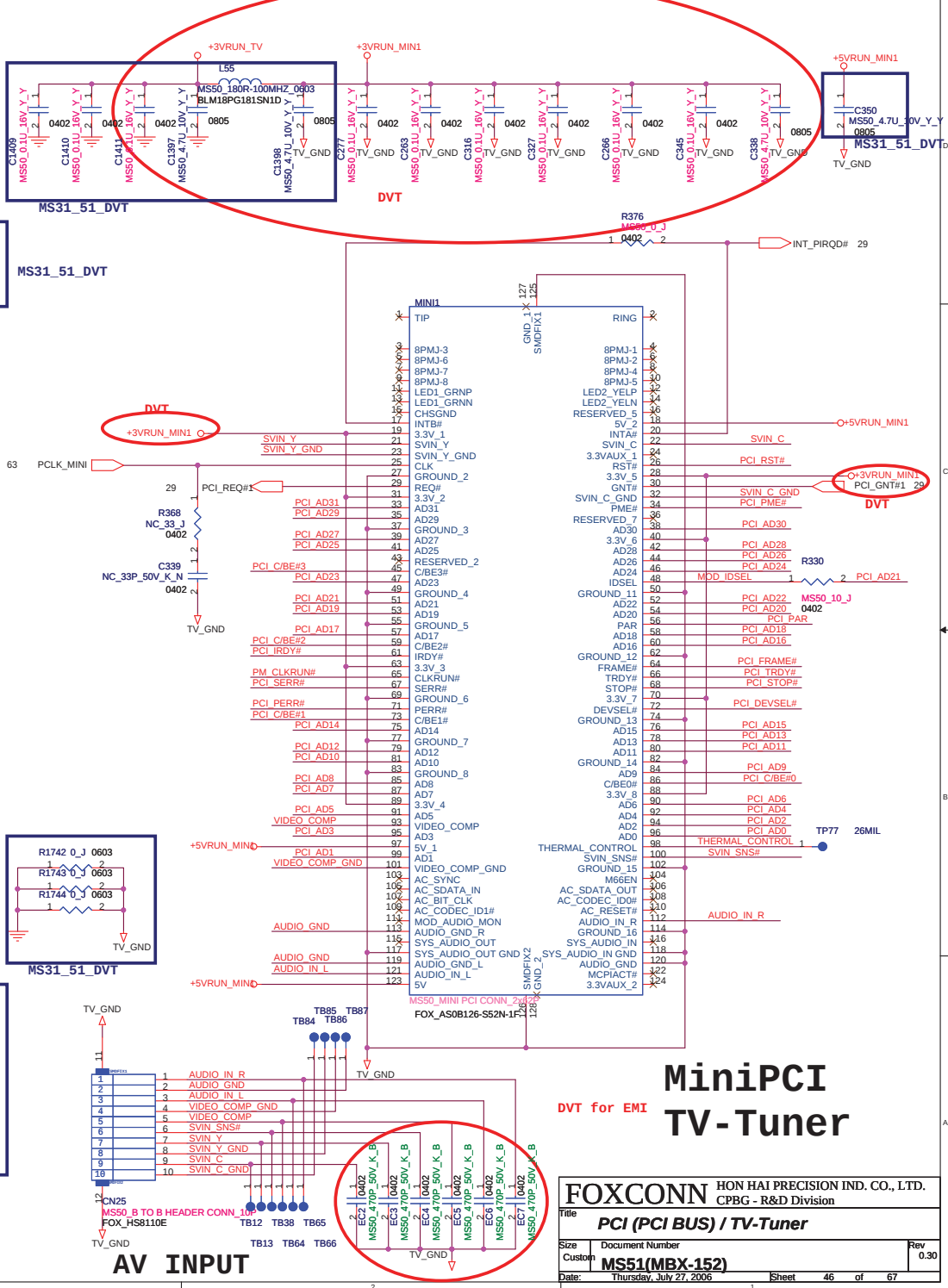
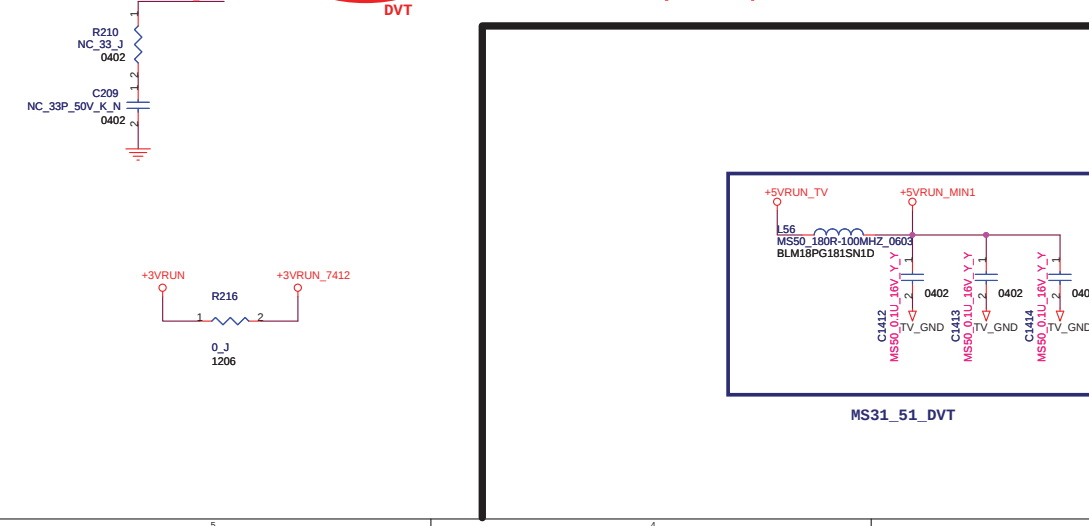
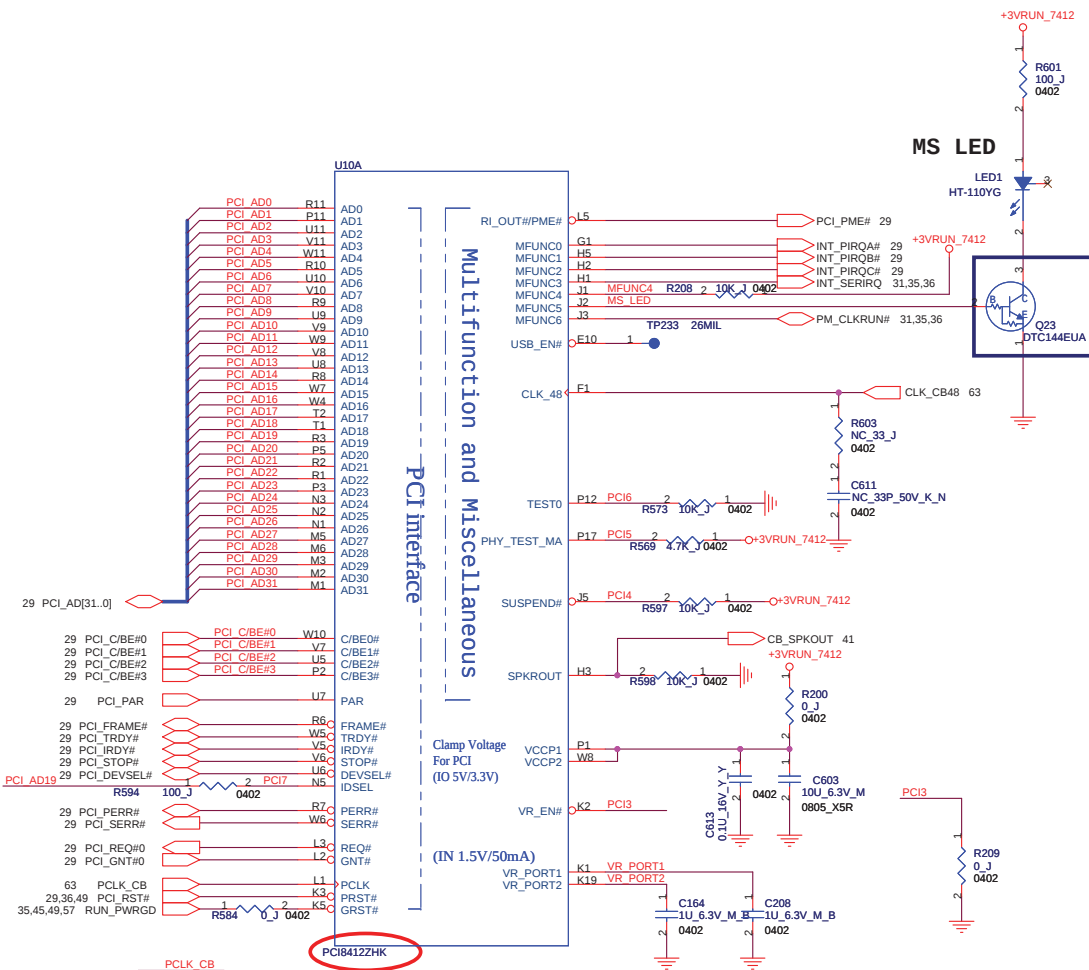
Modified 8/31

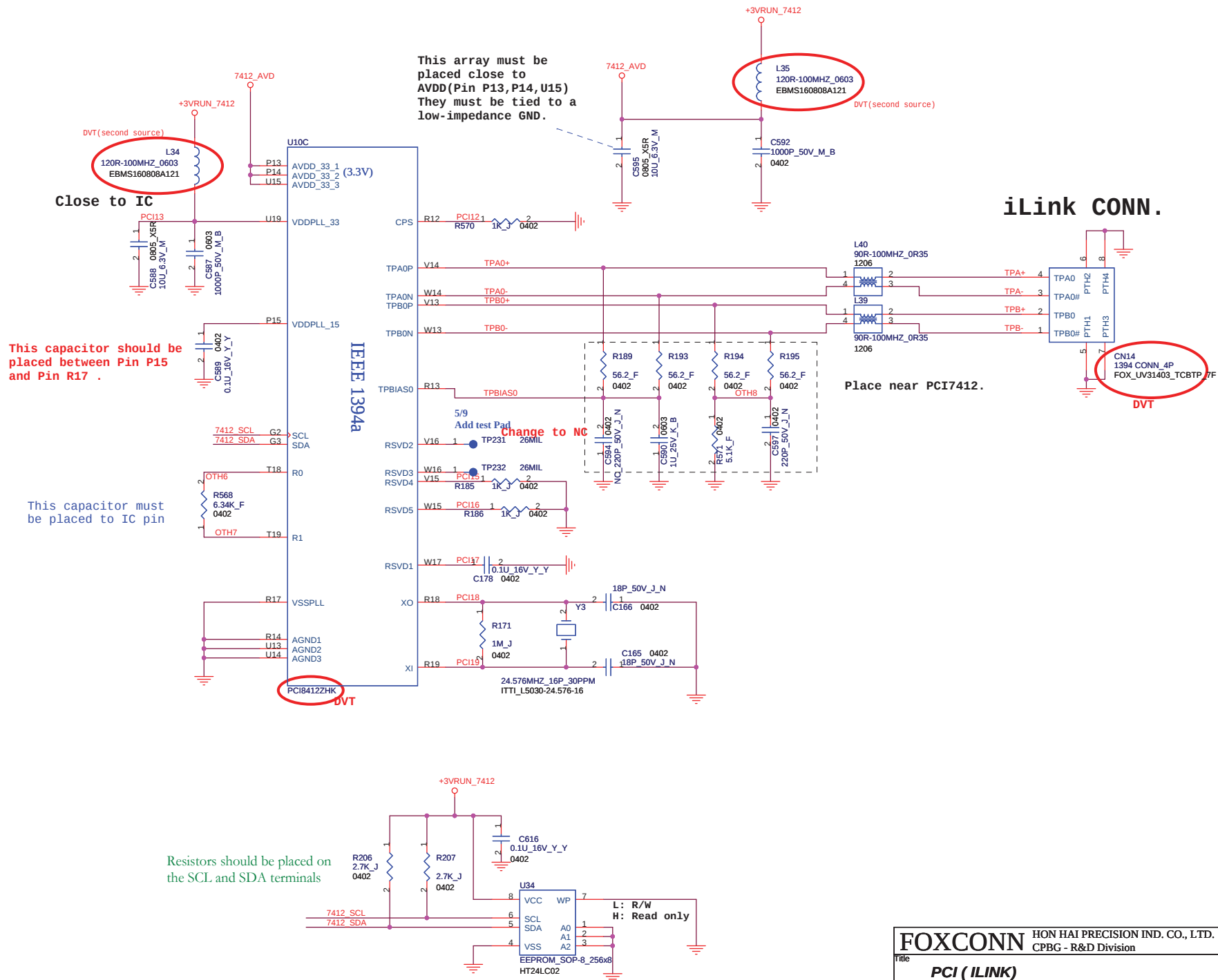


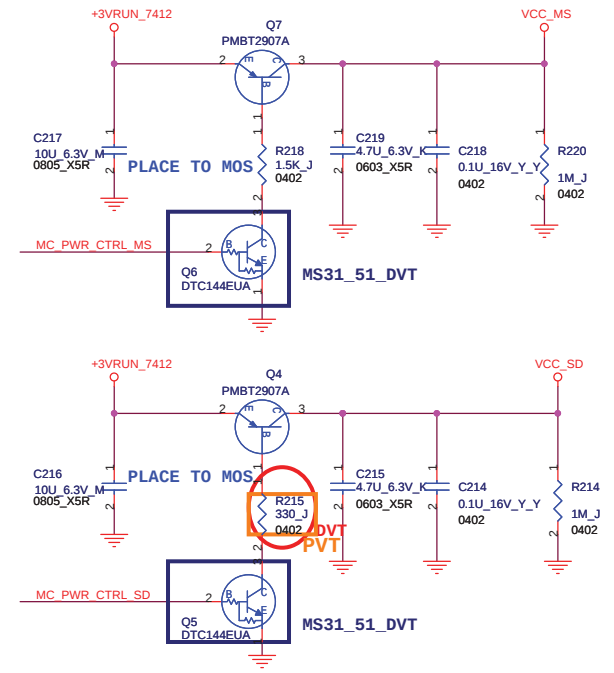
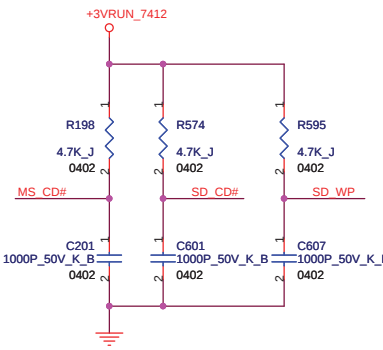
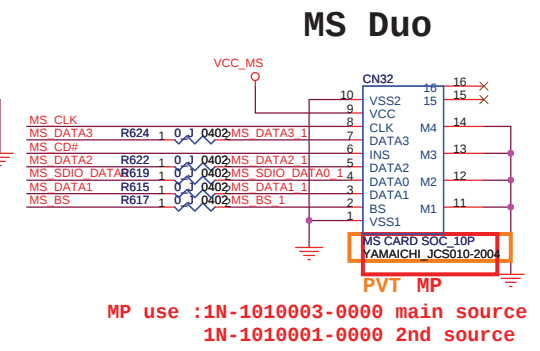
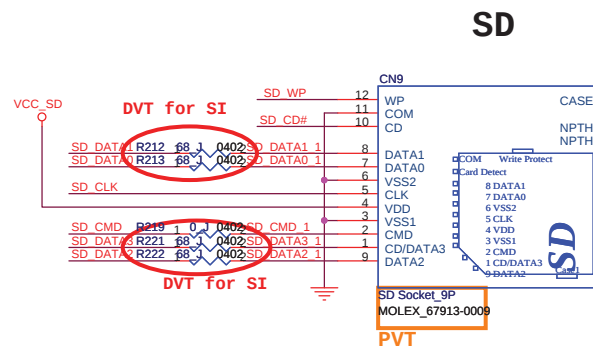
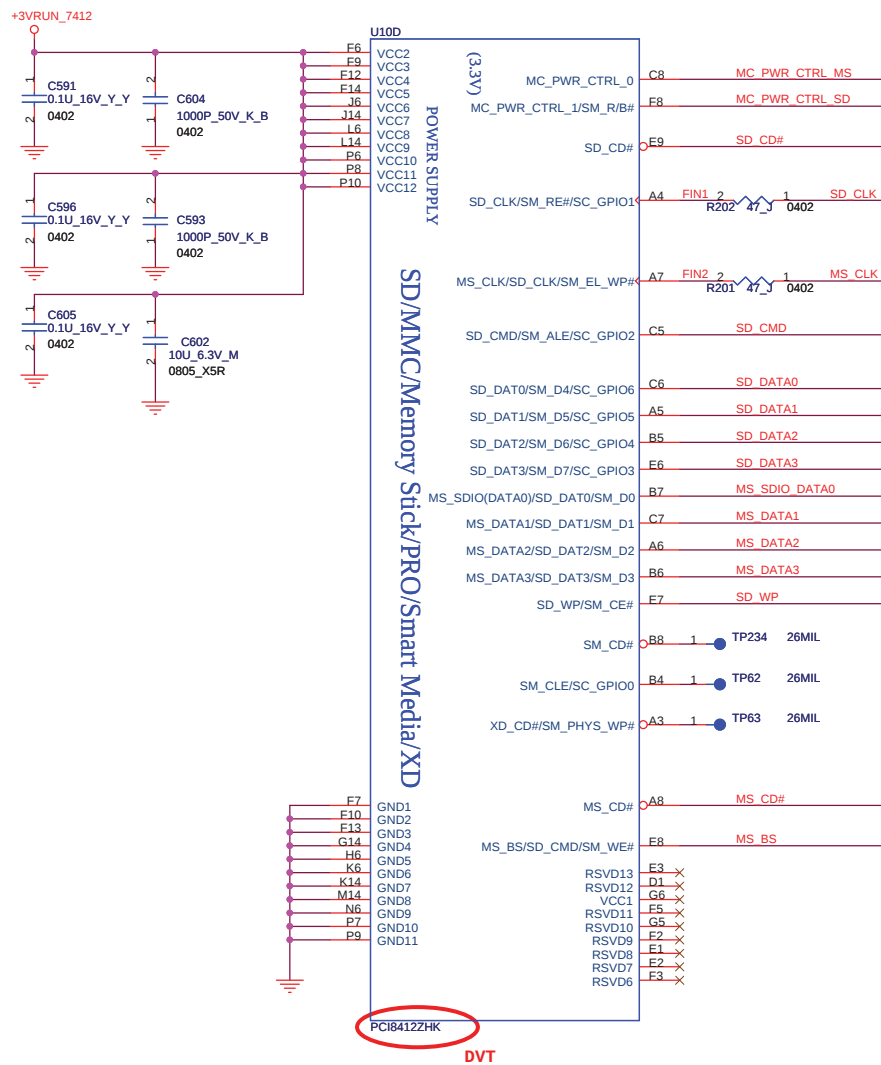
MODE	GPIO7	GPIO6	GPIO5
INTERNAL	0	0	X
RESERVED	0	1	X
EEPROM 256B	1	0	0
EEPROM 1KB	1	1	0
SHI	1	0	1
UART	1	1	1

8/31 Modified

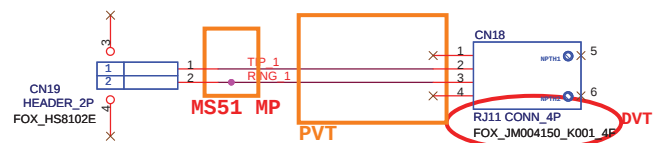
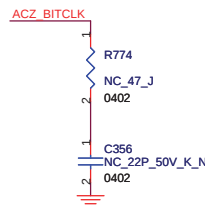
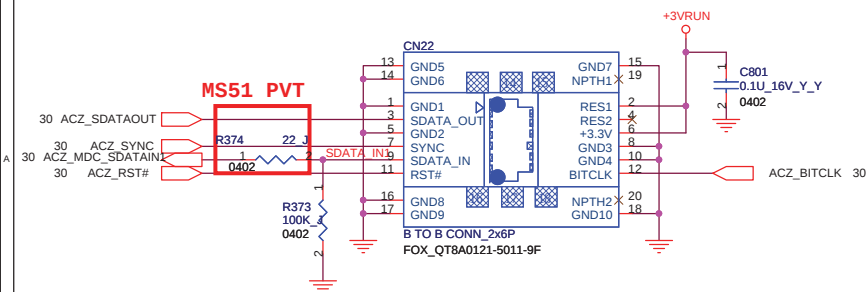








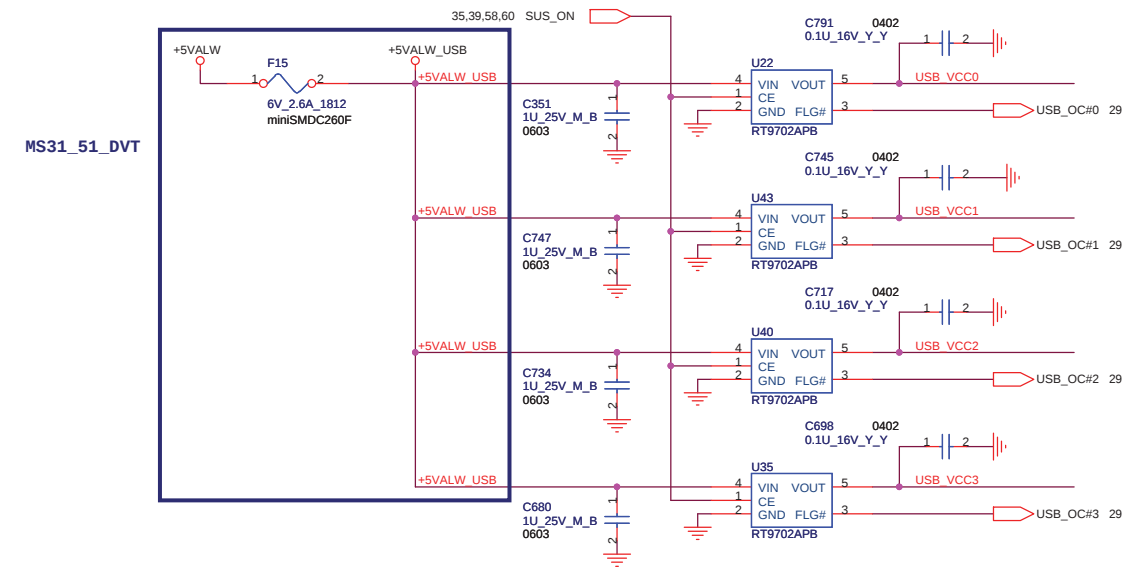
MDC CONN.



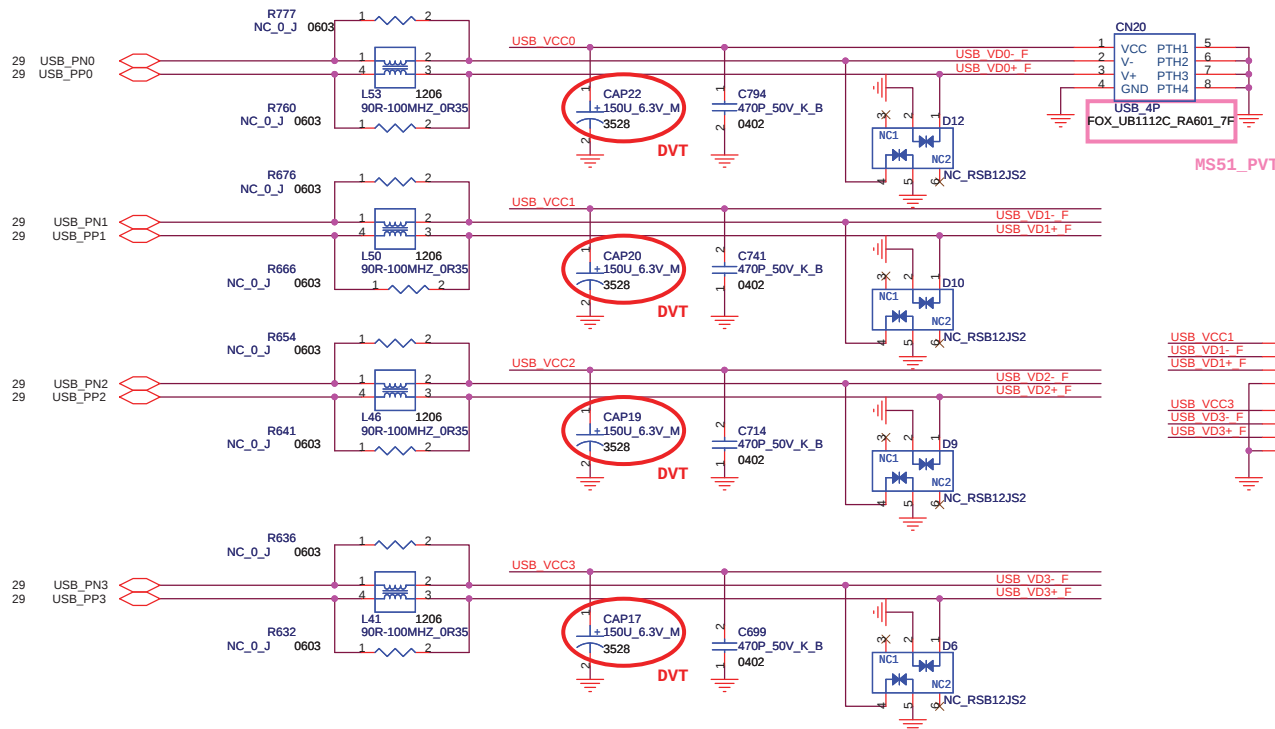
RJ11 CONN.

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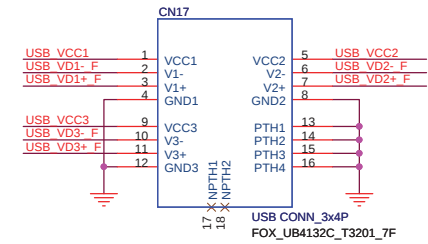
MS31_51_DVT

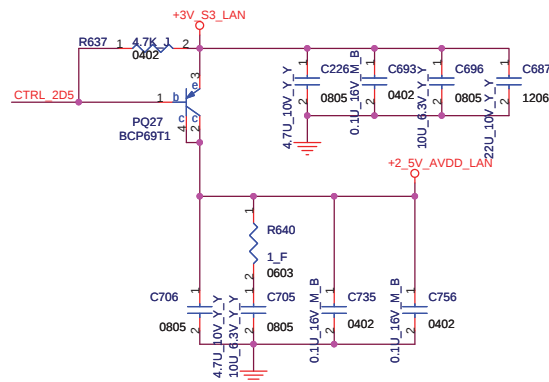
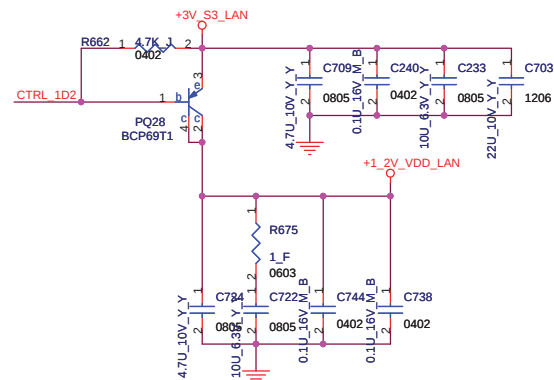
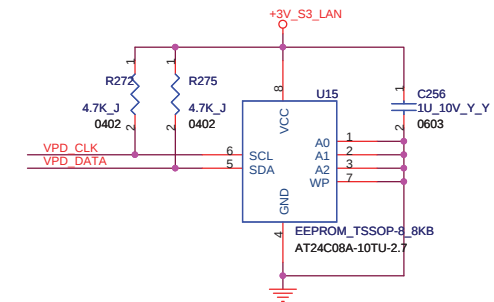
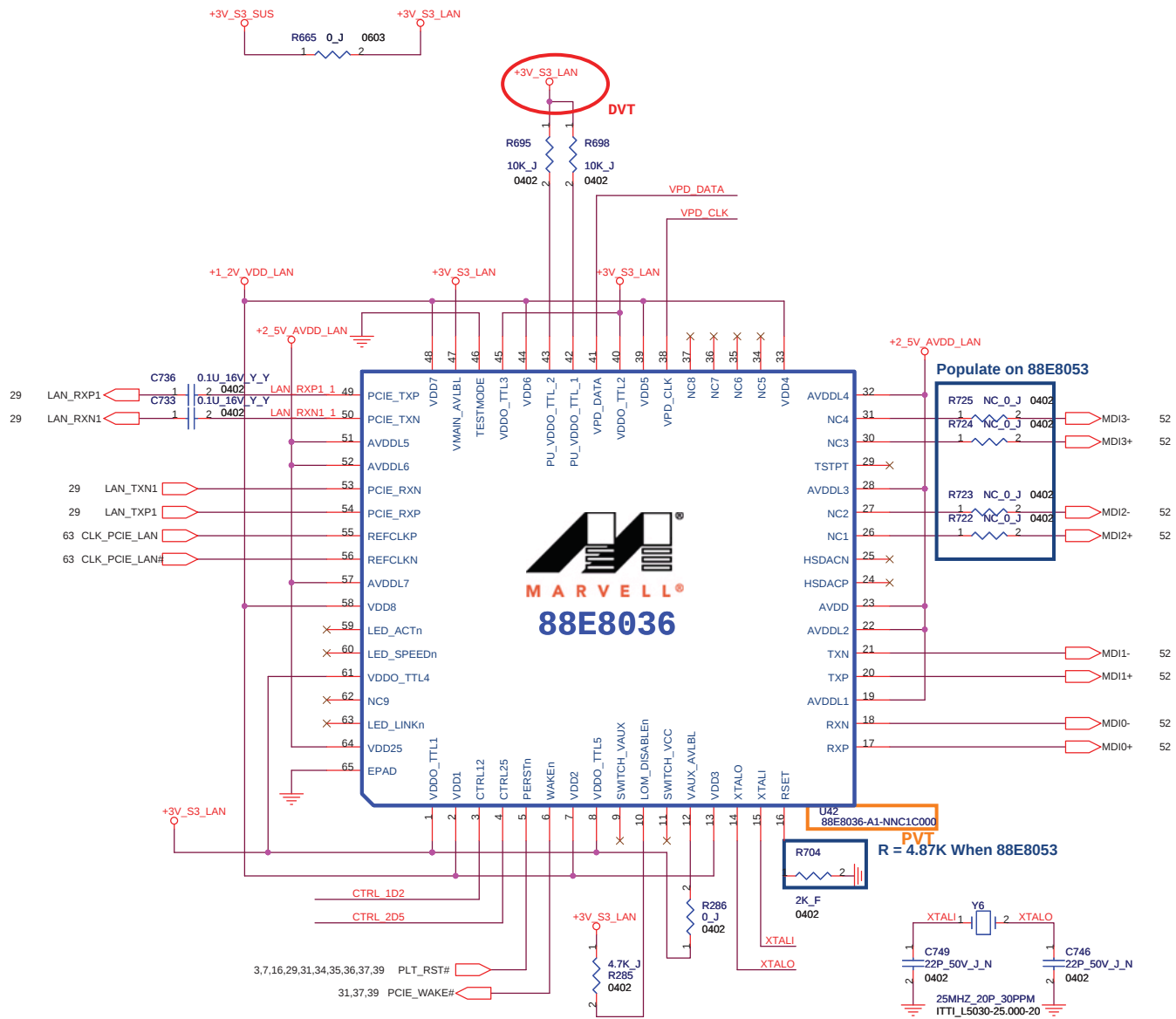


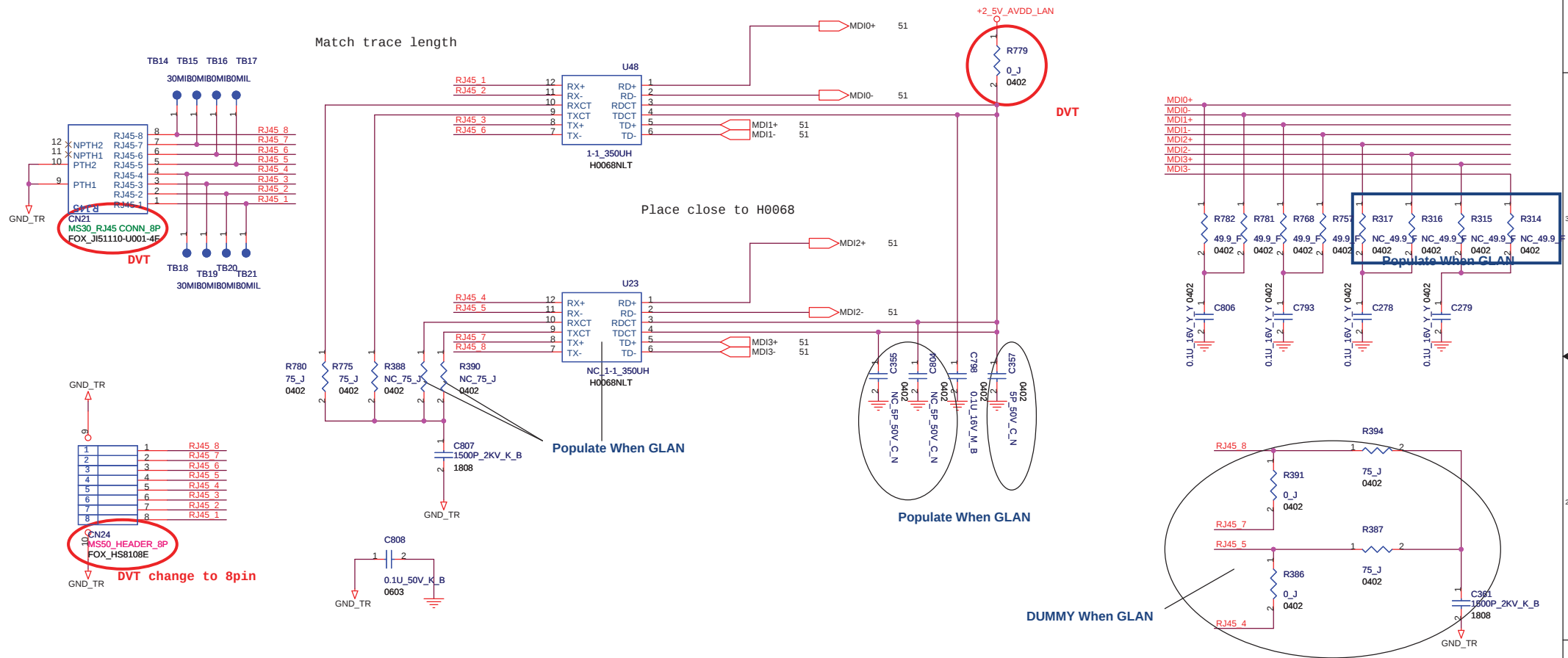
Use Power Switch



USB CONN X 4







Adaptor
19.5V
90W or 120W

MS30 ONLY
MAXIM
MAX1909ETI+
Battery Charger
Switch Mode

MS30 ONLY
Battery
BPS2
Li-Ion
12.6V
4800mAh

ENCHG#

DCBATOUT

DCBATOUT

DCBATOUT

DCBATOUT

DCBATOUT

MAXIM
MAX8734A+
Switch Mode
For System

Semtech
SC486
Switch Mode
For DDR2

MAXIM
MAX8743+
Switch Mode
For System

MAXIM
MAX8771+
Switch Mode
For CPU Core

Semtech
SC1470
Switch Mode
For VGAcure

System

+5VALW/9.5A

System

+3VALW/9.5A

+1_8VSUS/14A

+0_9VRUN/2.0A

+1_05VRUN/6.5A

+1_5VRUN/7.0A

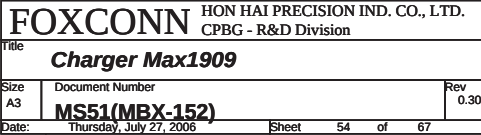
VHORE/44A

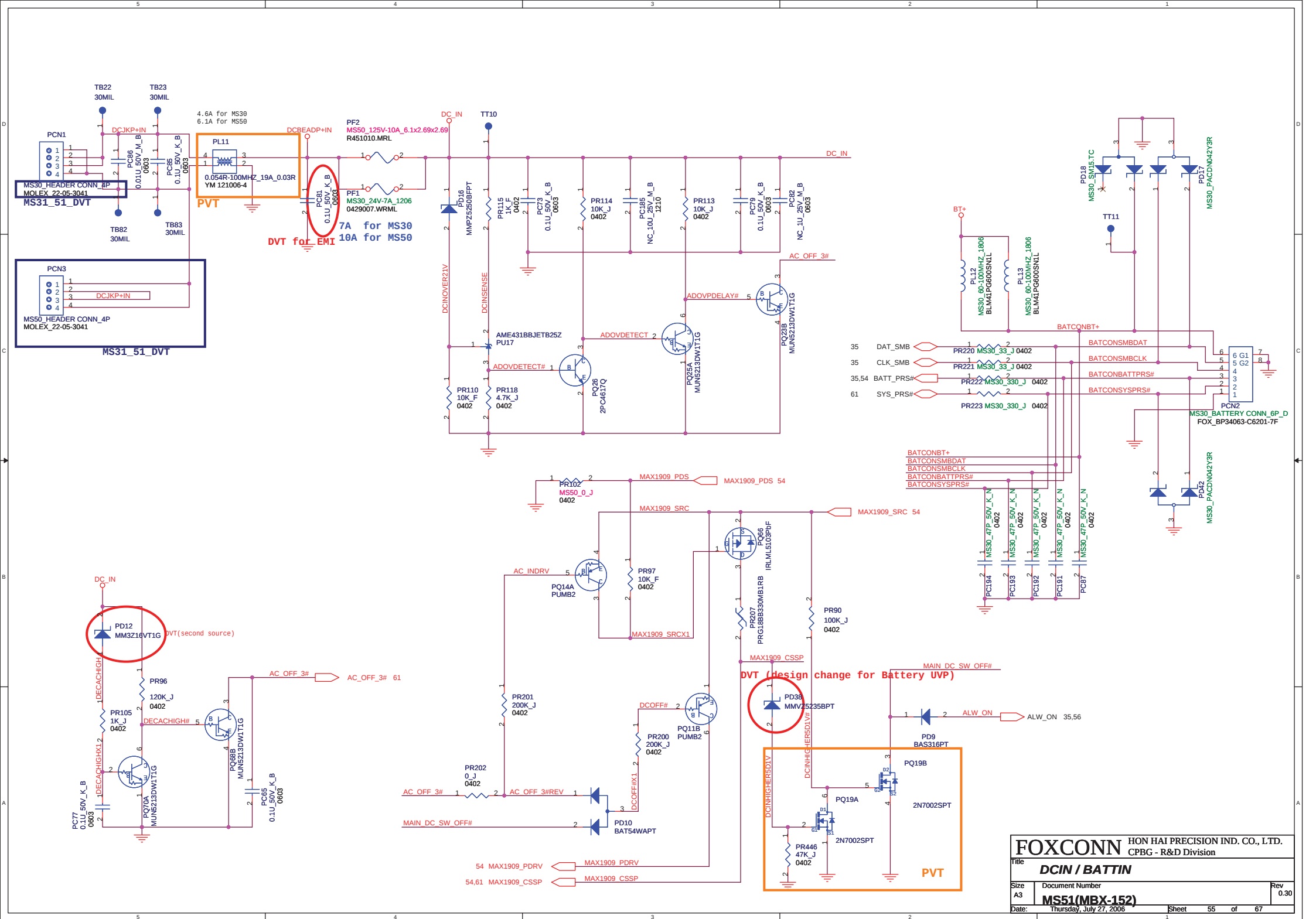
NV_VDD(1.025V)/16A

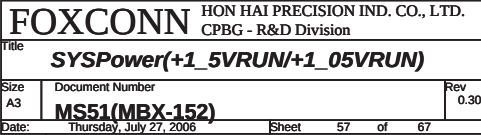
+5VALW

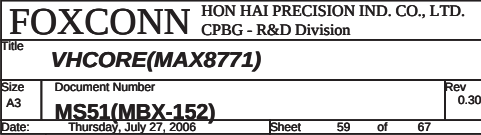
MAXIM
MAX668
Switch Mode
For 12V

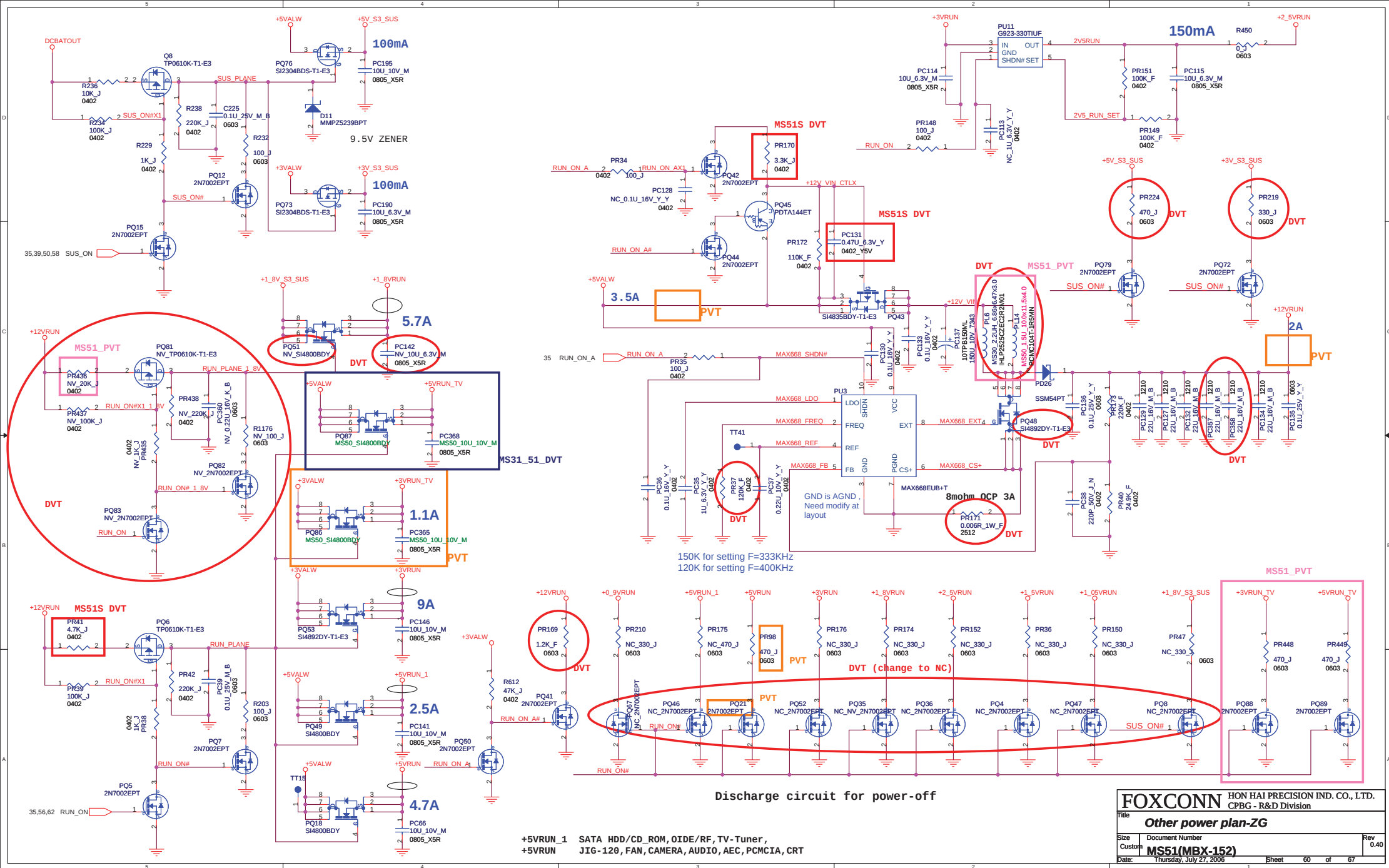
+12VRUN/1.2A

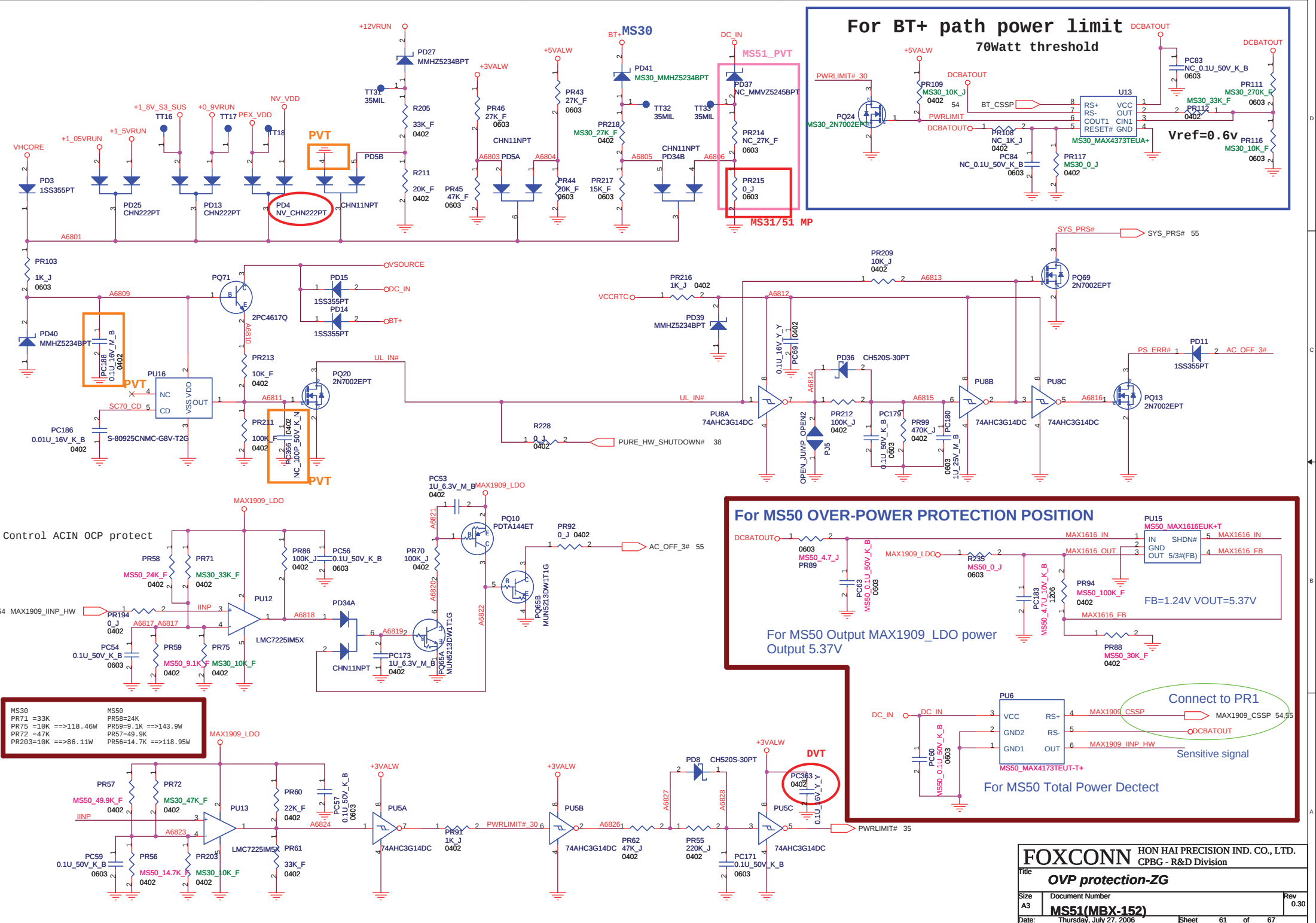




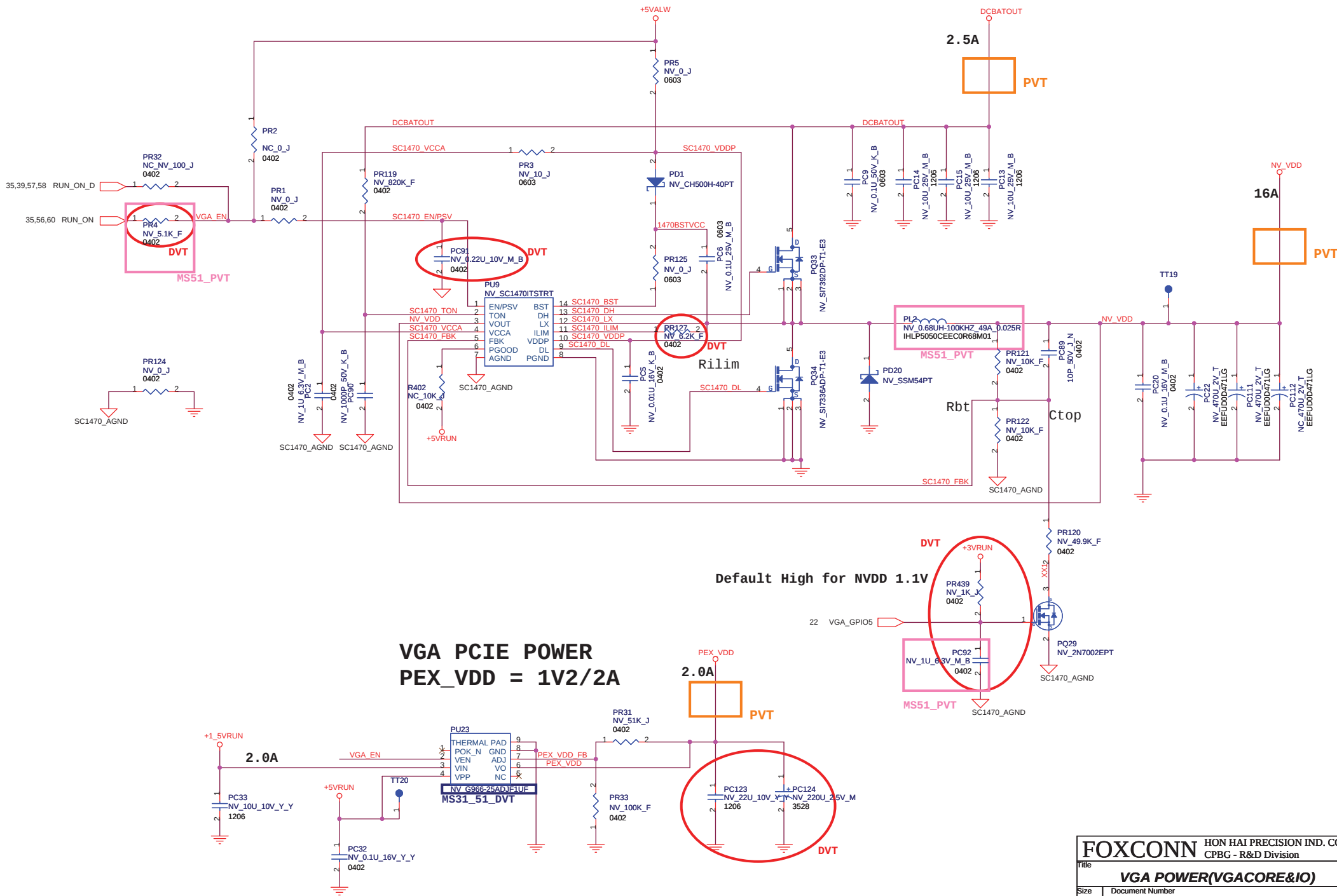


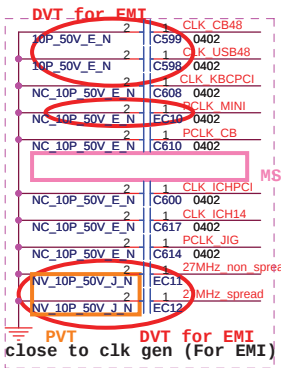






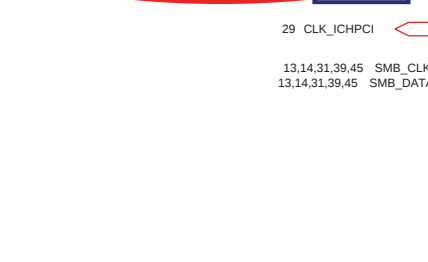
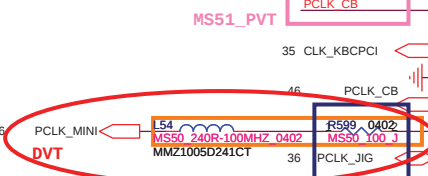
MS30	MS50
PR71 =33K	PR58=24K
PR75 =10K ==>118.46W	PR59=9.1K ==>143.9W
PR72 =47K	PR57=49.9K
PR203=10K ==>86.11W	PR56=14.7K ==>118.95W





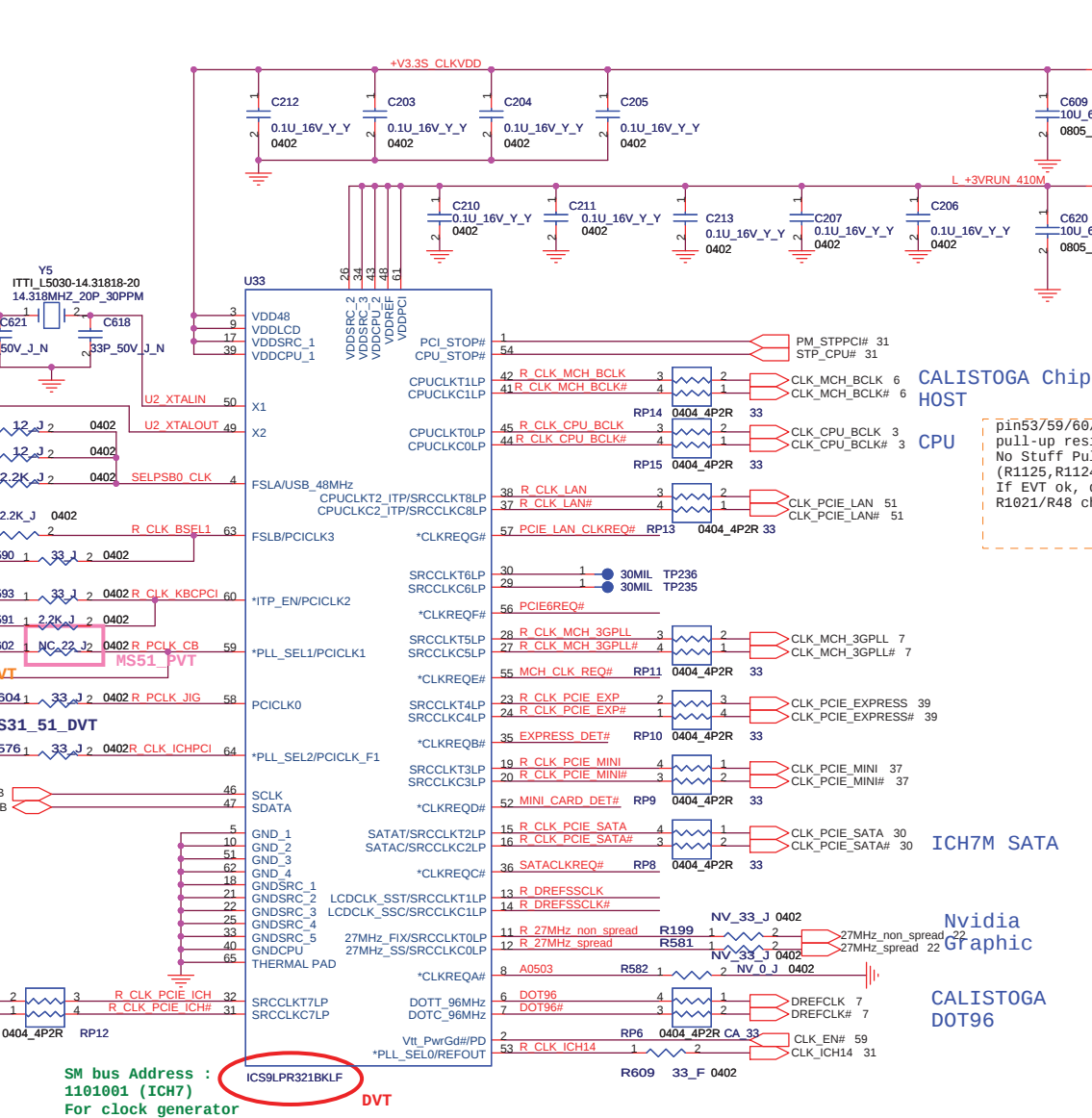
Length as short as possible.

31 CLK_USB48 R578 12K 0402 CPU_BSEL0 R577 2.2K 0402 SELPSB0 CLK



FSB Frequency Table:

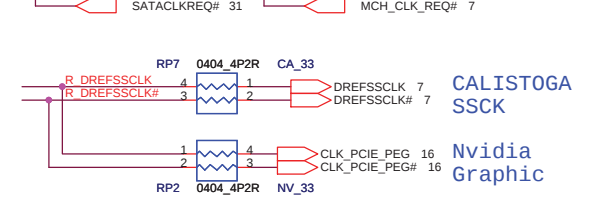
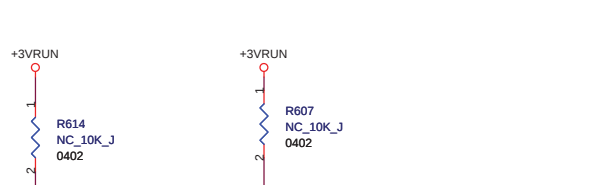
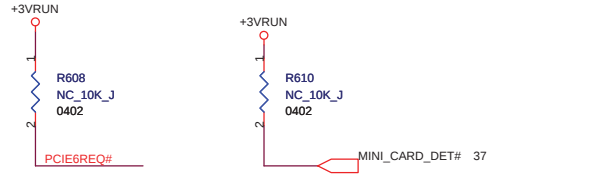
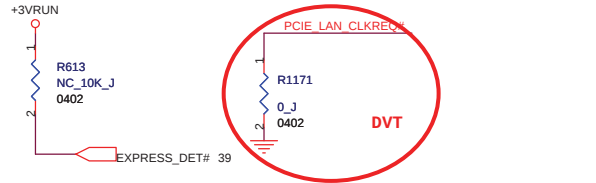
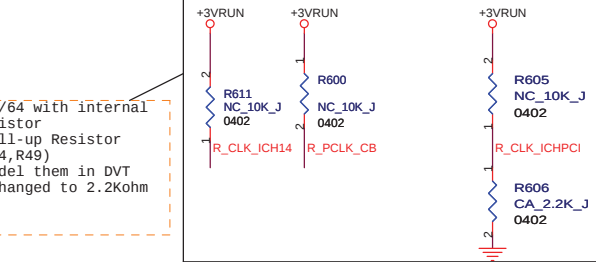
FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33



CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
If EVT ok, del them in DVT

Pin Straps

pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)



CALISTOGA SSCK

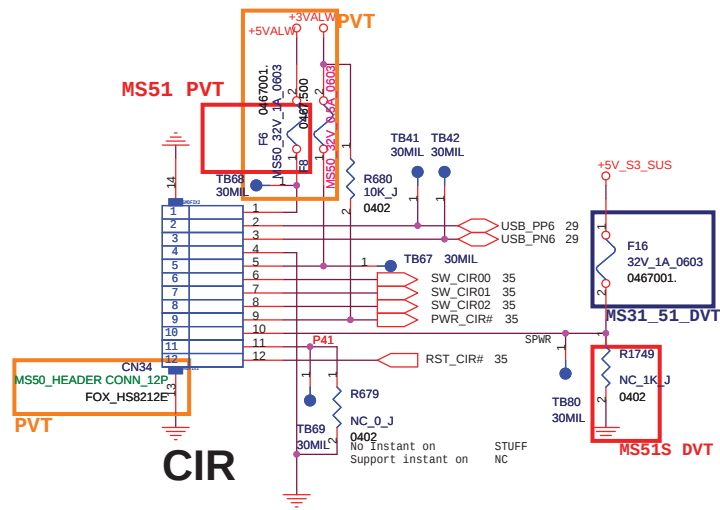
Nvidia Graphic

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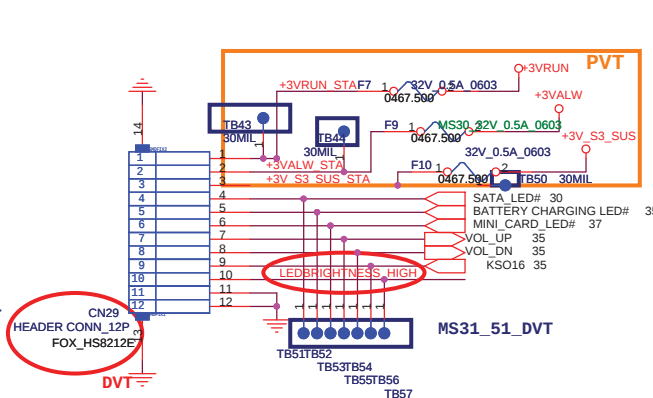
CLOCK GEN

Size A3 Document Number MS51(MBX-152) Rev 0.40

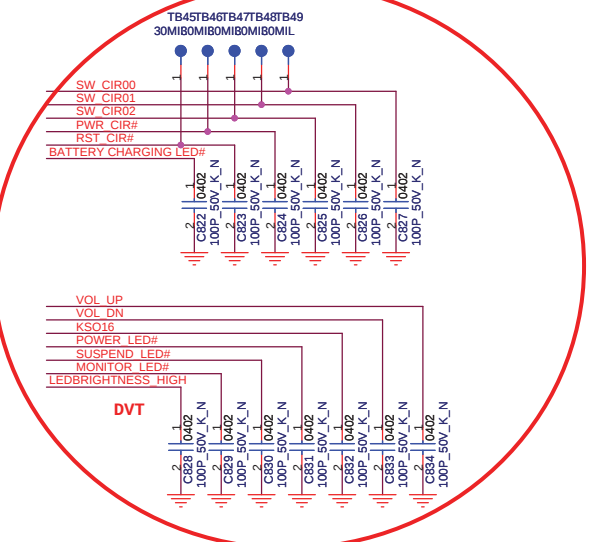
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CIR

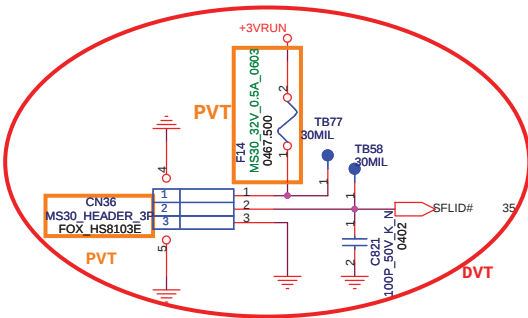


STATUS LED CONN

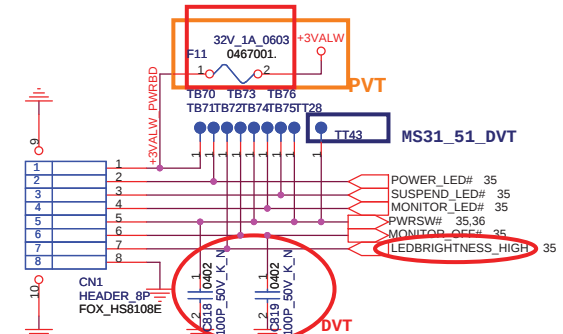


DVT

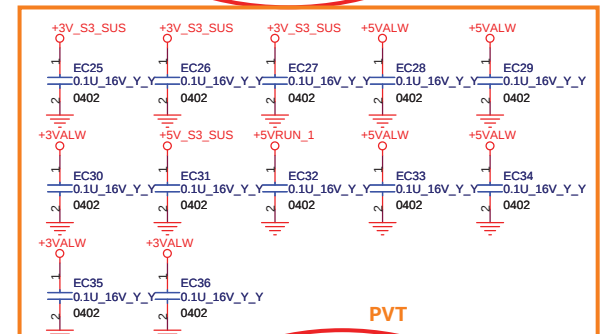
DVT



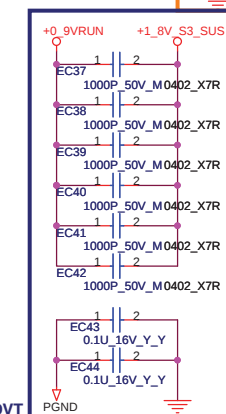
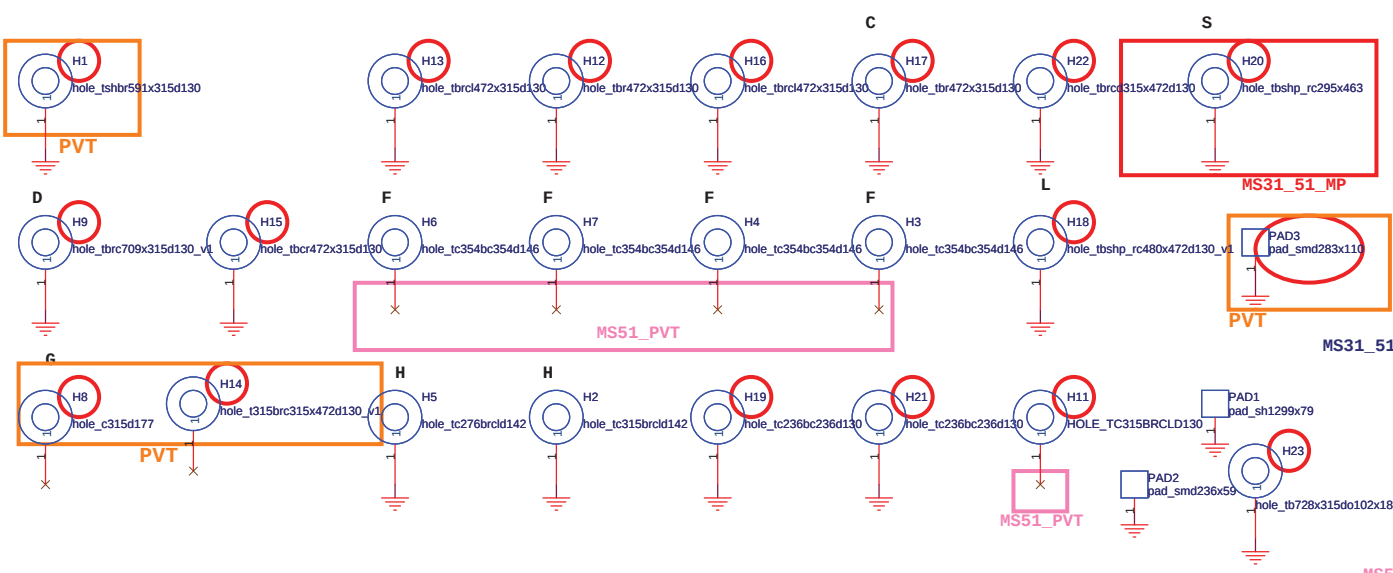
Cover SW CONN



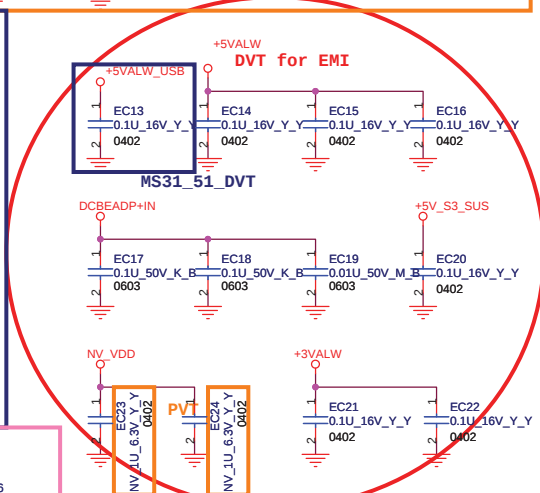
Power LED/Power BTN



PVT

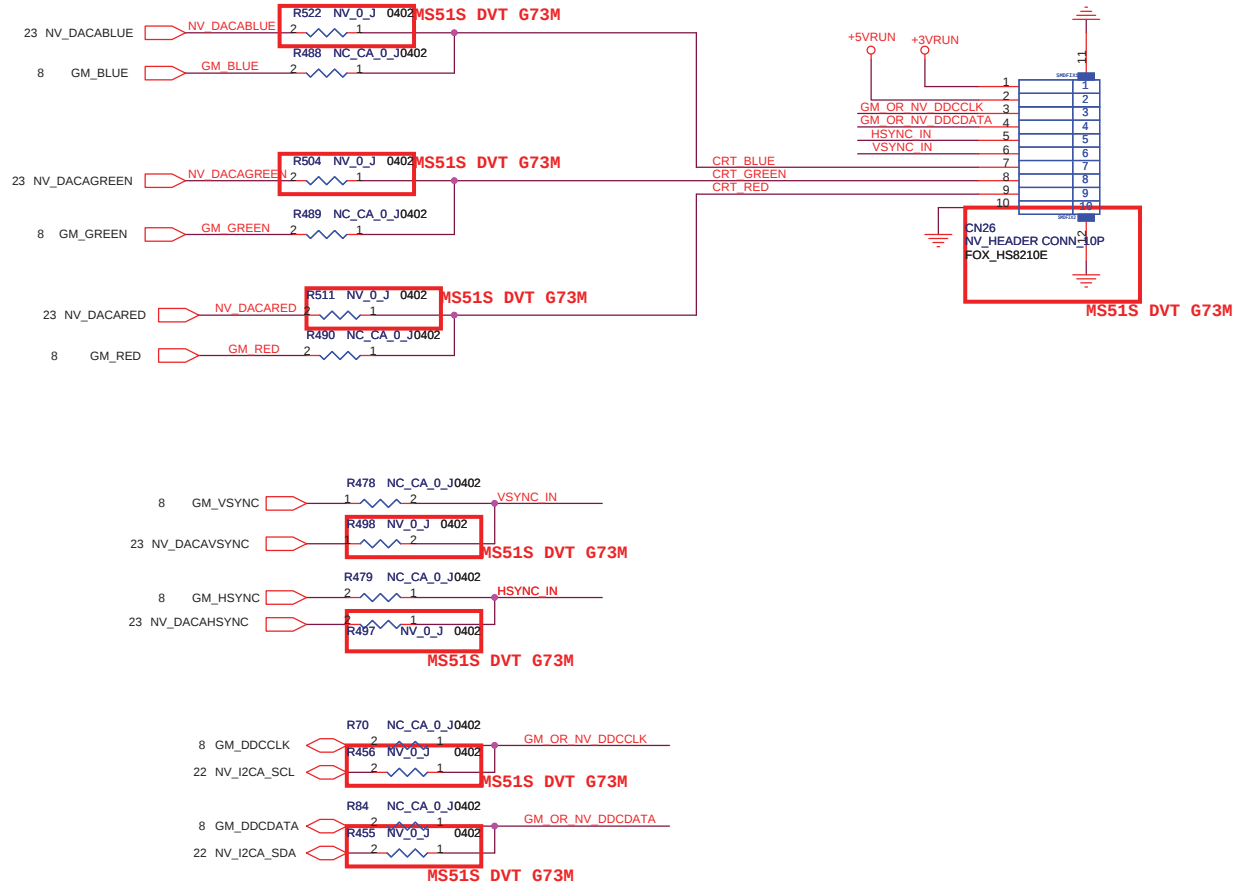


MS31_51_DVT



DVT for EMI

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P51 CN1 pin1 change to +3VALW for leakage
P52 mount R779 for lan get ip fail
P40 net name HW_POP_MUTE_CODEEC change to HW_POP_MUTE_CODEEC
P43 (1)net name HW_POP_MUTE_CODEEC change to HW_POP_MUTE_CODEEC
(2)change Q11 from MMBT3996 to MMBT3994
P60 mount PR224 for +5V_S3_SUS discharge too slow
P57 (1)change PR164 from 0ohm to 3.3 ohm for decrease 1.5V/1.05 noise
(2)mount PD21,PD24 for decrease 1.5V/1.05 noise
P59 mount PC278,PC279; mount PC38,PC109 for decrease Vcore noise
P62 mount PC32 for decrease VGA power noise
P40 (1)mount R682,R694 for sense_B,sense_A detect
(2)NC R388
P44 NC R643,R647
P43 mount R381 for amp abnormal be mute
P41 change J5PK1,J5PK2 from 2N-0002900-M00 to 2N-0002901-M10
P39 change CN33 from 2N-0008000-M10 to 2N-0008001-M10
P64 change CN36 from 2N-0002901-M10 to 2N-0002900-M10
P46-A9 change U10 to PC184122WK
P59 change PQ3,PQ8 to 17-514324D-VY00
P40 U19 change to CXD9872AR
P20-PQ3 change R172 to 12-CA1157B-A300(GM)
P41,P42 CNW1,2,3 change to 2N-0006062-FKX0
P22 R567 change to 16-CHS2853-0P00
P59 R568 change to 17-514324D-VY00
P58 PR193 change to 6.2K_F,PR136 change to 82K_F
P62 PR127 change to 6.2K_F
P60 PR37 change to 120K_F,PR171 change to 5mohm, P16 change to 2.2uH
P24,P25 Change R99,R148,R165,R167 from 120 Ohm to 60 Ohm
P60 change PQ31,PC142,PQ35 value to NV_
P43 add Q12,R172,R173 for adding EC to control mute function
P45 (1)add R342,NC R343 for Change VP1020 initialization to SHT mode
(2)NC U45,R355
P59 NC PD2,PD19
P60 add PC219,PR169
P24 change R165 to 40.2_F and add R1160,C809,
R1163,C810 for nvidia latest demo board for G72
P25 change R148,R99 to 40.2_F and add R1164,R165,
C811,C812 for nvidia latest demo board for G72
P43 change U21 to W74VNC1G732DF276 for shortage of toshiba parts
P41 change Q24,Q25,Q26,Q27 to PBSS2515F.115 for toshiba parts shortage
P16 add U49 for PLT_RST# to VGA
P28 add C815,C813,C814
P29,45 connect GP1017 to AEC pin30 powerdown
P35 (1)add D15,D16,D17 for preventing leakage from EC before power on
(2)reserved U3 pin 176 for second fan FB,pin43 for second fan PWM
(3)add U3 P105 as EC_LED to control LED brightness
P36 change CN12 pin1,pin21 to +ECVCC
P38 (1)add R1166 for discharge path of +SVALW_LDO
P59 update Q19 footprint
P43 change Q11 to MMT3994
P34 add CAP23,CAP24
P62 add PR439,delete PR123,NC PC92 for preventing VGA_GPIOS floating
P63 delete R294,add R1171 for PCIE_LAN_CLKREQ# pull low
P45 delete PQ77
P48 change CN18 to smaller size
P47 change CN14 to 1394 normal type
P42 change CN03 to Red color
P41 J5KP1 change to 3 pin for manufacture
P43 delete R306,R308,C350,R305,C360
P54 add PC340
P59 change PQ38 to MMV252538PT for battery in UVP fail
P38 change second fan to adjustable
P56 add PC347,PC346,PC341,PC158 for +SVALW
P57 add PC349,PC359,PC342 for +1.VRUN
P58 add PC351,PC352,PC343 for +1.8V_S3_SUS
P59 add PC353,PC354,PC344,PC355,PC356,PC345,PC278,PC279 for VCORE
P57 add PC348,PC196,PC197,PC359
P59 change PD2,PD19 to NC.SPL1849PT (18A)
P60 (1)change PQ48 to 514802DV-T1-E3
(2)add PL14 for MS50,PL6 for MS30
(3)add PC357,PC358 for +12VRUN
P34 add CAP23,CAP24 for MS50 HDD
P30 add R1175 for MS50 SATA Cable
P64 (1) delete R783
(2) CN1 add EC_LED to control LED brightness
(3)CN1 pin 1 change to +SVALW
P60 add PR436,PR437,P081,PR435,P083,PR438,PC380,P082,R1176 for +1.8VRUN timing
P54 (1)add PR442,P084,U50 and connect PR182 pin2 to +ECVCC for preventing leakage of charger LDO
P56,S7,S8,S9,S0 Update PL6,PL9,PL7,PL8,PL2,PL4,PL5,PL14,PL1,PL3 footprint for shaking test

1201
P40,41 Swap SPK_L,SPK_R at source and speaker cnn side
P46 add C818,C819 for ESD
P40 CN15 change to CXD9872AK
1202
P40 Follow FAE suggestions
(1)add C820(180.10V_M) for AVDD
(2)change C305 to 100.6.3V for VREFILT
(3)change R752 to 1% tolerance
1205
P29 change GP4 to R1402
P51 add R1403,NC R665 for LAN S4 wake up
P54 add PC362
P57 add PR440,PR441 for balance 2 caps voltage
P22 U9 update new version
1206
P22 rename R567 to D19
P45 NC C770
P51 change R665 value to MS30_0_J,R1403 value to MS50_0_J
P60 NC P067,P046,PQ21,PQ52,PQ35,PQ36,PQ4,PQ47,PQ6
P62 change PC123 to 22U.10V_Y,PC124 to 220U.2.5V_M for reduce PEX_VDD ripple
P64 add C321-C334 for protecting EC from ESD
P54 add C835-C838 for protecting EC from ESD
P40 add C839 for protecting EC from ESD
P30 add C840-C844 for protecting EC from ESD
P41 change R233,R231 to 47K_F,addC850,C847,C851,C846
P44 (1)R261,R255 change to 56K_F
(2)R248,R254 change to 2.4K_F
(3)R246,R251 change to 2.2K_J
Add TB1-T777,T11-20 for manufacture TE test
P44 add GP7,GP8,GP9 for MIC quality
P57 mount PR159
1206-1
P3 change Q21 to 2N7002
1206-2
P59 PC4,PC12,PC18,PC19,PC98,PC105 change to 330U.2.5V_M
1207
P28 change CN3 to 1N-0030000-FW00
P42 change R693,R683 from 11K_F to 7.5K_F
P30 change second fan(CN7) source(R173,Q9) to +12VRUN
1208
P52 CN24 change from 10pin to 8pin
P51 change R665 value to 0_J,dummy R1403
1209
P59 add TT21-TT27 for manufacture
P61 add PC363 for PUS power bypass
P38 add R1403 for reserve 12V path to second fan
P42 update U17 to MAX4232AKA+T
P59 delete PR14-PR20 ,and short
P08 delete R76,R63,R78,R542,R62,R77,R64,and short
P10 delete R544,R535,R65,R355,R79,R543 ,and short
P12 delete R514,R508,R541,add TP248,TP249,TP250
P30 delete R782,R697 and short
P41 (1)change R225,R226 from 22K_J to 47K_J
(2)change TB8-TB11 to 40m1
P46 (1)add R1404,C1397(NC),C1398(NC) for separate power for reduce
noise of tv-tuner
P60 add R1415,C1400(NC),C1401(NC) for separate power for reduce
noise of tv-tuner
P63 change R599 to 100_J,add L54 for PCLK_MIN1
P57 change PR440,PR441 from 2.2K_J to 100K_J
P54 (1)PQ03 change to 514825
(2)mount P07
1212
P63 mount C596,C509 for EMI
P55 mount PC81 for EMI
P39,P46,P56,P63,P64 add EC1-EC24 for EMI solution
P59 reserve PR444,P085,PR445,PC364,PR443 for max8771 CLKEN# abnormal
P29 change R389,R776 from 99_J to 47_J for SI
1213
P28 add Q31 for LCD_VDD discharge path
P46 change EC2-EC7 value to MS50_
P43 mount R778,Q14
P44 (1)change R248,R254 from 2.4K_F to 1.5K_J
(2)change R246,R251 from 2.2K_J to 2.4K_F
P48 (1)change R212,R213,R221,R222 from 0_J to 60_J for SI
(2)change R215 from 1.5K_J to 1K_J from customer suggestion
P54 (1)change PR183 from 15.4K_F to 20K_F
(2)change PR49 from 20K_F to 24K_F
to set constant power to 4.09A(87%)
P57 (1)NC PC196,PC197
(2)change PR440,PR441 to NC.27K_J
1214
P60 change CAP17,CAP19,CAP20,CAP22 to 100U.6.3V_M for vendor
P54 add PD43
P59 change PR7,PR126 to 3.3_J
1215
P61 change PD4 value to NV_

1219
P54 change PD7,PD43 from 16-MMP2525-3B00 to 16-MMP2525-1B00
P43 change EC11,EC12 to 10P.50V_3_N
P61 change CN21 to MS30_
1227
P42,P59 Update C282,C758,PC94,PC102
0110 for PVT BOM
P50 change CAP17,CAP19,CAP20,CAP22 to 150U.6.3V_M(NEC/TOKIM)
P54 (1)change PQ63 to A04407
(2)NC PC382 for battery issue
P41 change L42,L43,L44,L45 to BLH18PG330SNI0
P20 (1)change R555 to 49.9 ohm 1%
(2)mount R556
P24 (1)change R165,R1160,R1163,R167 to 240_F
(2)change C809,C810 to 0.01U
P25 (1)change R148,R1164,R1165,R99 to 240_F
(2)change C811,C812 to 0.01u
P16-P23 update U6 P/N to 12-67PMA20-A200
P43 NC K773 for +VRUN leakage
P42 change C831,EC24 value to NV_ *
(2)change CN36 value to MS30_ *
P60 mount PR08,PQ21 for +VRUN leakage
P50 change PR80 to 102K_F for meet TV-tuner power spec
P59 change PQ3,PQ30 for better Vcore design
0120
P37 add Q32 for wireless led always on
P38 add D20,D21 for +VRUN current to damage Q5
P40 update CN6,CNS footprint
P55 add PR446,combine PQ22A/PQ198 to PQ19(2N7002DW) for abnormal ALW.ON
P44 add PQ8 for improve rf quality
P43 add Q33,and change Q14 to MMBT3904 for leakage
P37 change SW2 to SSS0U1700_SW-DIP3
P48 change CNW to MOLEX.67913-0009 for factory repair
0121
P64 change CIR connector value to MS58_ * for ms50 only
P39 change L8,L18 to 1200-100M1Z R693 for curren rating
P8 mount R69,R68,R65,R493,R494 _NC R540,C453,D3,R548,L21,L23,C414 for disable CRP4
P10 mount R547,R518,C454 _NC R540,C453,D3,R548,L21,L23,C414 for disable CRP4
0123
P8 change R87 value to 0_J,dummy R485,R492,R81 for CRT disable
P65 dummy R488,R489,R490,R476,R479,R70,R84 for CRT disable
P10 dummy R558 for G73M
P61 change PC188 to X50 type
P27 dummy R5,R2,R6,R7,R10,C23,C25,C24,U26,R11
P63 change R659 to 100ohm 0402 1%
P30 add P331 for RCTCRST#
P61 add PC366 for reserve ;P05B pin 4 connect to GND for preventing floatin
0125
P64 change PADS to pad_smd203x10
P54 update PL1,PL11 footprint for cold solder issue
P63 update L54 vendor to TKD
P30 delete L37 and short for inverter fuse current rating
P42 change PQ06,PC385 value to MS50_ *
P56-62 delete P31-P34,PJ6-PJ27,P29,PJ30 and shot
P54,P56-61 add TT29-41 for power test
0207
P48 change CN32 to 1N-1010003-0000
P34 change CN10 to 2N-0022000-MK00(shorter pin length)
P41 (1)change J5PK1 to 2N-0002902-M10(shorter pin length)
(2)change J5PK2 to 2N-0003001-M10(shorter pin length)
P39 add F2 for protection
P16 reserve R1405 for new G72M
P22 reserve R1406 for new G73M
0208
P38 mount R1403,dummy Q30,R1173,R1174,Q29,D21 for fix mode by customer suggestion
P54 change H1,H0,H14 footprint
P59 add TT42 for power test
P63 change R590 from 100ohm to 47ohm(1R-000470-J200)
P30 change F2 to 1M-F24V042-0000(24V-0.2A.120V)
P34 reserve R1407 for Staggered spin-up disable by customer suggestion
P43 add C1401 by customer suggestion
P41 (1)change C220,C221 from 0.47u to 0.22u
(2)change C676,C674 from 1u to 6.8u
(3)change R1167 from 1K to 2.2K
(4)add R1408,C1399,R1409,C1400 by customer suggestion
P48 NC CN18 pin1,4 and remove R742,R743,L51,L52 by customer suggestion
P22 mount R1406
P40 change U19 to CXD9872K
0209
P56 reserve R1410 for discharge path
0210
P20 mount C363,C364,C365,C366 for EMI
P41 (1)change R225,R226 from 47K to 100K,
(2)change R227 from 2.2k to 270 ohm
P65 add EC25-EC30 for EMI
P44 add GP10 for EMI
P35 add U51,C1402 by customer suggestion
P55 change PQ19 to 17-2N70025-P100
P30 (1)change R745 value from MS30_24.9_F to 24.9_F
(2)dummy R1175
P48 change R215 from 1K_J to 330_J for SD card power drop

0214
P44 change GP10 to R1411(MS50_0_J) for EMI
P38 add F3,F4 for cable short protection
P39 add F5 for cable short protection
P64 add F6-F11 for cable short protection
P31 (1)connect GP1021 to U20 pin14 for bypass AEC
(2)dummy R304 for double pull low
P45 connect U20 pin14 to SB GP1021 for bypass AEC
P54 add PR447,PC367(snubber circuit) for dc.in inrush voltage/current
0214
P38 delete F3,F4
P44 add F5 for cable short protection
P35 add F12,F13 for cable short protection
P45 add R1412 for hardware disable
0214.1
P38 add F4
P60 correct PQ6,PQ81,Q0 part number(TP610K-T1-E3) to TP0610K-T1-E3
P56 correct PQ65,PQ66 value to S174040N-T1-E3
P57 correct PQ37,PQ38,PQ39,PQ40 to S174040N-T1-E3
0215
P39,P38,P35,P64 change F2,F4-F14 size from 1206 to 0603
P60 correct PQ6,PQ81,Q0 vendor part number(TP610K-T1-E3) to TP0610K-T1-E3
0216
P39,P38,P35,P64 change F2,F4-F14 to 1M-F32V0A5-F001 FUSE,Littelfuse,0467.750,32V,0.75A
0223.SMT
P28 dummy C363,C364,C365,C366 for LVDS timing by customer
P38 add D20,D21 for +VRUN current to damage Q5
P39 change F5 to 32V.1A.0603,F2 to 32V.0.5A.0603
P29-P33 update U44 part number to NH828010BM.00
P54 update PR447 to 1_F.0805,1R-0008010-F500
P39,P38,P35,P64 change F2,F4-F14 to 1M-F32V0A5-F000 FUSE Littelfuse,0467.500,32V,0.5A
NP
0302
P48 change CN32 to Yamaichi_JCS810.2005_1 for vendor shortage
0303
P44 (1)change C675,C674 to 1C-2B70225-M000 for 6.8U.6.3V_M shortage
(2)add C1403,C1404(1C-2B70475-K201) for 6.8U.6.3V_M shortage
P39 remove TB6,TB7 for manufacture test issue
0311
P39 change F2 to 32V.1A.0603 for current rating
P41,43 change Q8,Q13,Q28 from 17-MMBT390-6K00 to 17-MMBT390-6K00
P57 change PR105 to 1K_F,PC30 to 2.2uF,16V for adjusting 1005V power on/off sequence
MS31_51.DVT
U4/26
P19 change L26,L27 to 10uH inductor(CS0603-10N1-S) by vendor suggestion
P24 add GP10 NV.PWR.MIZER
(1)add R1416,Q37,R1415,R1414,Q35,R1417,Q30,Q36
P25 add GP10 NV.PWR.MIZER
(1)add R1420,Q41,R1419,Q40,R1418,Q39,R1421,Q42
P20 add GP10 NV.PWR.MIZER
(1)change R563 to NV.4.3K_F,R564 to NV.10K_F
(2)add Q34,R1413
P22 add GP10 NV.PWR.MIZER
(1) add USF GP1010 to NV.PWR.MIZER and PL R1412
P64 replace R578 with F50(32V.1A.0603)
P63 change R509 to 100_J for tv-tuner quality
P64 add EC37-EC44 for EMI
P50 add F15 for USB EU standard
0427 for G72M
P28 change R555 to 60.4_F by vendor suggestion for G72M
P24 (1)dummy R184,R181,R176,R160,R179,R177,R172,R159 for G72M
(2)change R165,R167,R1160,R1163 to 60.4_F for G72M
(3)change C800,C810 to 0_J for G72M
P42,P25 cahnge U28,U29,U30,U31 to HYB18H256321AFL20(256Mbit) for G72M
P25 dummy all parts for G72M
P27 dummy all parts for G72M
P20 dummy L24,C427,C438 for G72M
P19 mount R558 for G72M
P16-23 change US to G72M (12-0FG0740-A300)
0428
P64 EC13 power rail change to +SVALW_USB
P35,34 connect CN15 pin 37 to U3 pin 24 to detect 000 operation for 2nd fan control
0502
P31 (1)delete Q30,R1173,R1174,R1403,D21
(2) add R1426,R1428,R1423,R1427,Q43,C1406,C1405,C1407,C1425,R1424,U52,C1408 for 2nd fan control
0503
P42 change R693,R693 to 7.5K for CXD9872M.4TW+ Line in FSIV
P24 mount R163,add R1737,dummy R174,R164 for 8M X32 Vram
P25 reserve R1739 for 8M X 32 Vram support
P35 change netname FAN2_PWM to FAN2_LIN
P60 add PQ87,PC368 for TV
P46 add C1409,C1410,C1411,R1738,C1412,C1413,C1414 for TV
P55 reserve PCN3 for new TV card ME interference 0504
P55 change PCN1 value to MS30_ *