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PCB P/N:

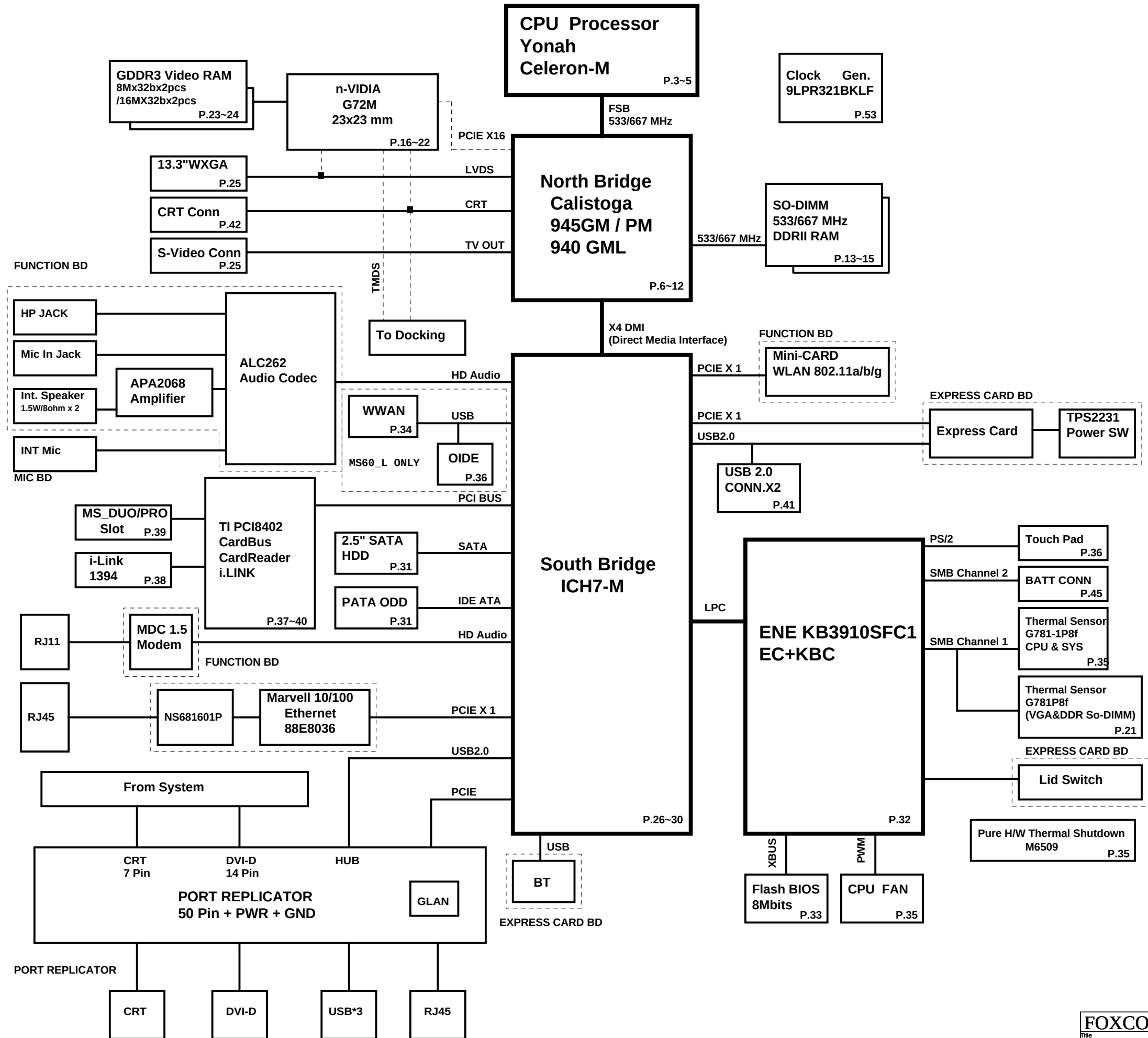
1P-0066700-8010 - Unimicro
1P-0066201-8010 - NANYA

Project Code & Schematics Subject: MS60 Main Board

P. Leader	Check by	Design by

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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MS60 (CALISTOGA PM/GM+Gfx Block Diagram)



SYSTEM DC/DC	
MAX8734 P.46	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC
SYSTEM DC/DC	
MAX8743 P.47	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486 P.52	
DCBATOUT	+1_8V_S3_SUS +0_9VRUN

CPU DC/DC	
ISL6262 P.48	
INPUTS	OUTPUTS
DCBATOUT	VHCORE

AMP DC/DC MAX1616		P.49
INPUTS	OUTPUTS	
DCBATOUT	+8V_{RUN}	

SC411		P.51
INPUTS	OUTPUTS	
DCBATOUT	NV_VDD	
GMT966		P.51
+1_5VRUN	PEX_VDD	

MAXIM CHARGER MAX1909	
P.45	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

Layout note:
no stub on
H_STPCLK#

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU, IMVP and MCH, pull-up
resistor has to be 75 ohm +-5%

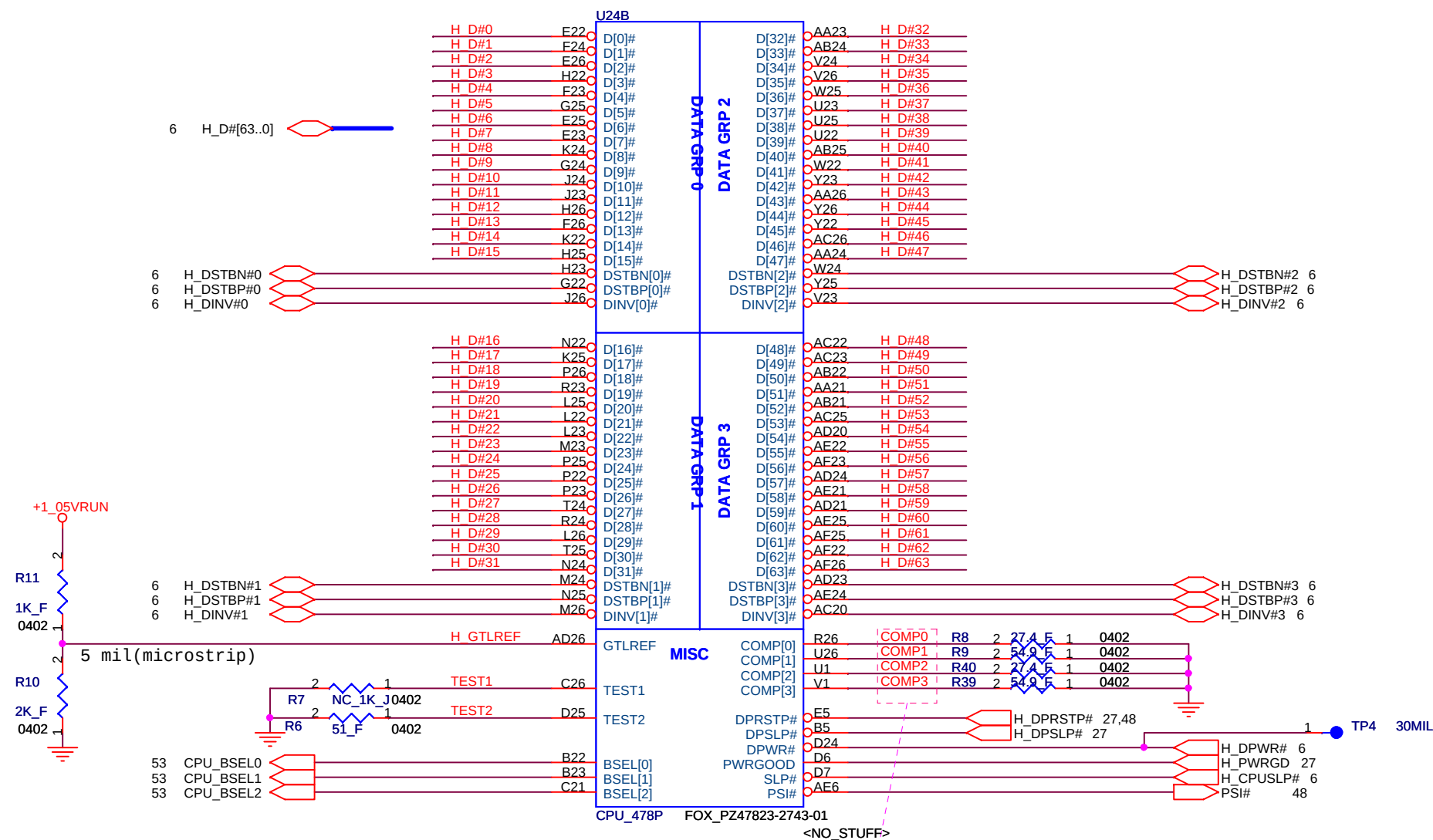
Place close to CPU

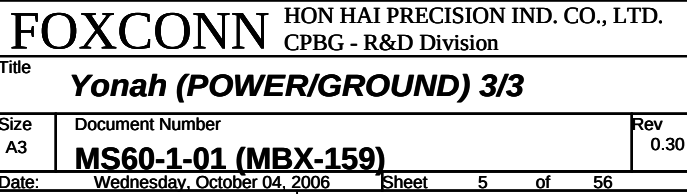
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

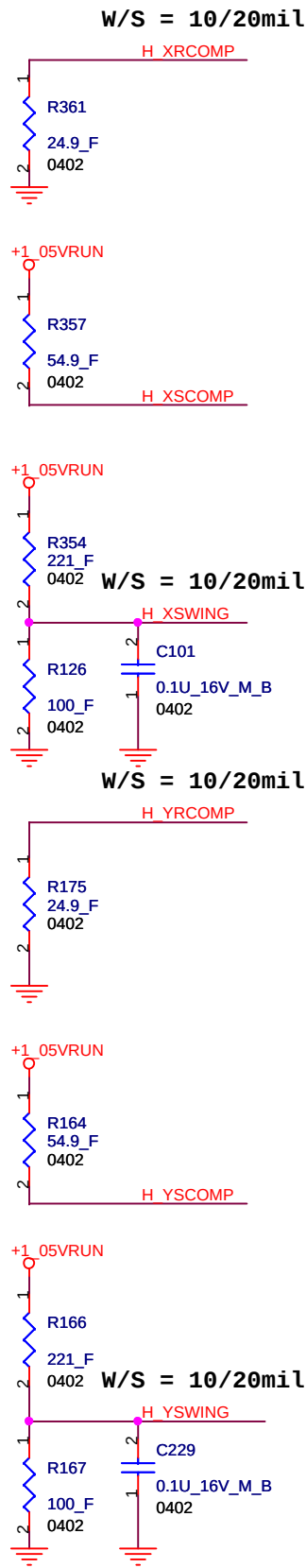
FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

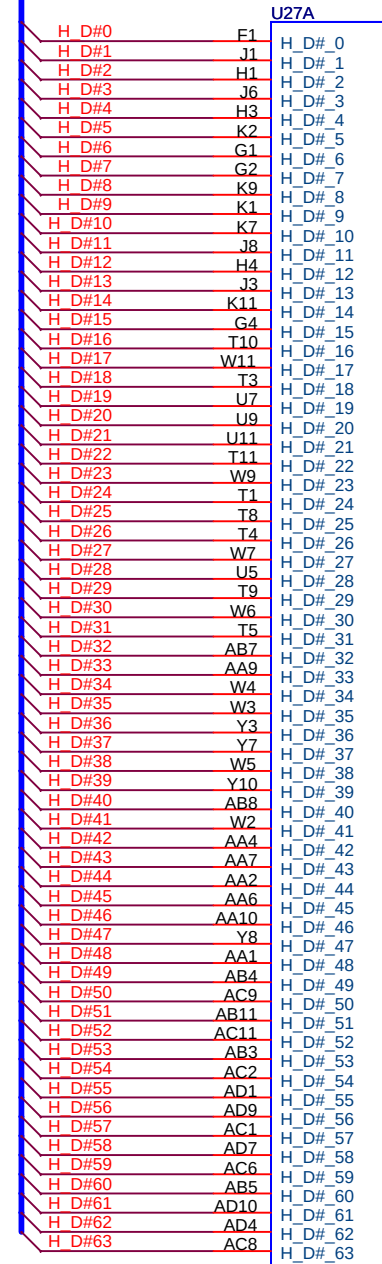
Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".



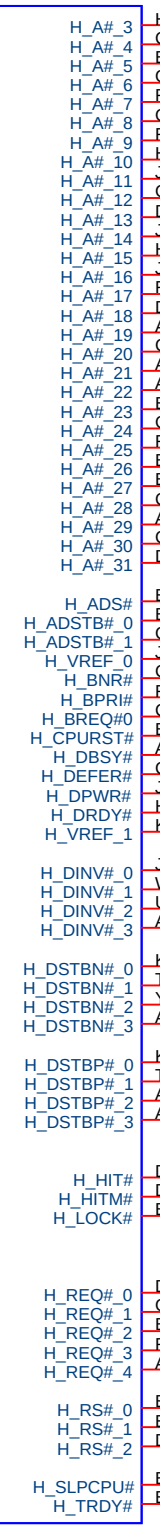




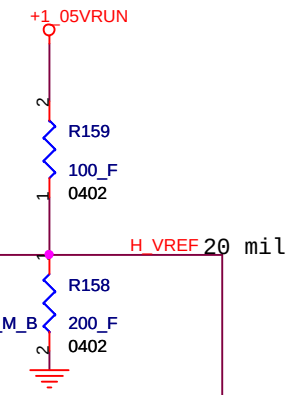
4 H_D#[63..0] H_D#[63..0]



HOST



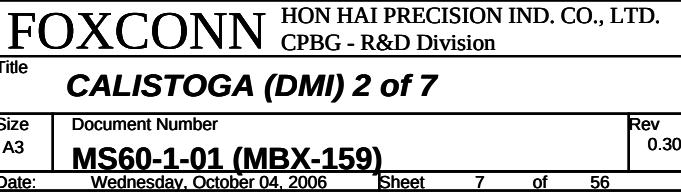
Place Cap.
near GMCH
within 100
mils.

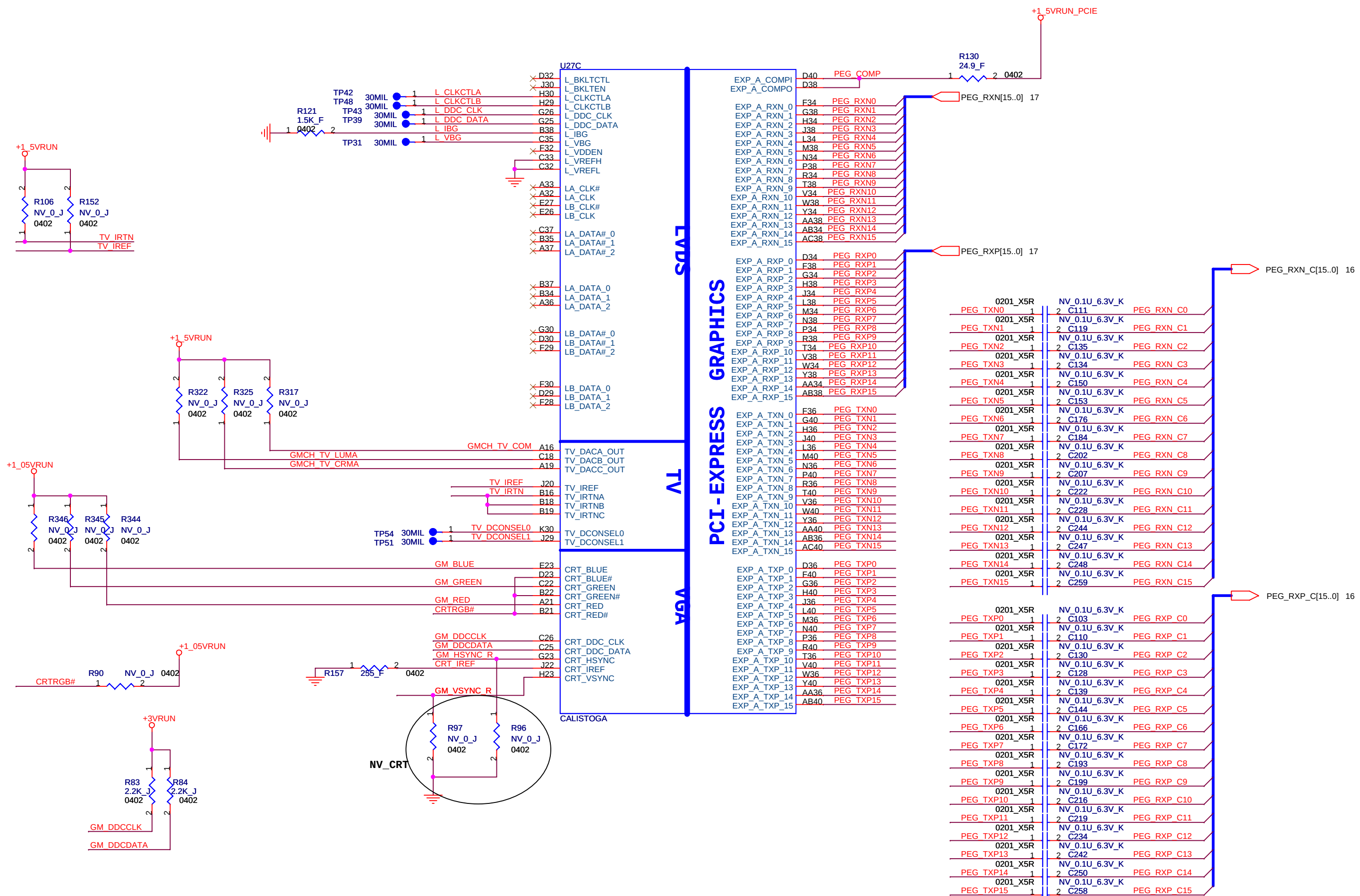


GM Q688CGM 12-0688CGM-0000

PM Q688CPM 12-0688CPM-0000

GML 940GML-QK60-A3 12-940GML0-A300





13 M_A_DQ[63..0]

M A DQ0	AJ35
M A DQ1	AJ34
M A DQ2	AM31
M A DQ3	AM33
M A DQ4	AJ36
M A DQ5	AK35
M A DQ6	AJ32
M A DQ7	AH31
M A DQ8	AN35
M A DQ9	AP33
M A DQ10	AR31
M A DQ11	AP31
M A DQ12	AN38
M A DQ13	AM36
M A DQ14	AM34
M A DQ15	AN33
M A DQ16	AK26
M A DQ17	AL27
M A DQ18	AM26
M A DQ19	AN24
M A DQ20	AK28
M A DQ21	AL28
M A DQ22	AM24
M A DQ23	AP26
M A DQ24	AP23
M A DQ25	AL22
M A DQ26	AP21
M A DQ27	AN20
M A DQ28	AL23
M A DQ29	AP24
M A DQ30	AP20
M A DQ31	AT21
M A DQ32	AR12
M A DQ33	AR14
M A DQ34	AP13
M A DQ35	AP11
M A DQ36	AT13
M A DQ37	AT12
M A DQ38	AL14
M A DQ39	AL12
M A DQ40	AK9
M A DQ41	AN7
M A DQ42	AK8
M A DQ43	AK7
M A DQ44	AP9
M A DQ45	AN9
M A DQ46	AT5
M A DQ47	AL5
M A DQ48	AY2
M A DQ49	AW2
M A DQ50	AP1
M A DQ51	AN2
M A DQ52	AV2
M A DQ53	AT3
M A DQ54	AN1
M A DQ55	AL2
M A DQ56	AG7
M A DQ57	AF9
M A DQ58	AG4
M A DQ59	AF6
M A DQ60	AG9
M A DQ61	AH6
M A DQ62	AF4
M A DQ63	AF8

U27D

DDR SYSTEM MEMORY A

SA_BS_0	AU12
SA_BS_1	AV14
SA_BS_2	BA20
SA_CAS#	AY13
SA_DM_0	AJ33 M A DM0
SA_DM_1	AM35 M A DM1
SA_DM_2	AL26 M A DM2
SA_DM_3	AN22 M A DM3
SA_DM_4	AM14 M A DM4
SA_DM_5	AL9 M A DM5
SA_DM_6	AR3 M A DM6
SA_DM_7	AH4 M A DM7
SA_DQS_0	AK33 M A DQS0
SA_DQS_1	AT33 M A DQS1
SA_DQS_2	AN28 M A DQS2
SA_DQS_3	AM22 M A DQS3
SA_DQS_4	AN12 M A DQS4
SA_DQS_5	AN8 M A DQS5
SA_DQS_6	AP3 M A DQS6
SA_DQS_7	AG5 M A DQS7
SA_DQS#_0	AK32 M A DQS#0
SA_DQS#_1	AU33 M A DQS#1
SA_DQS#_2	AN27 M A DQS#2
SA_DQS#_3	AM21 M A DQS#3
SA_DQS#_4	AM12 M A DQS#4
SA_DQS#_5	AL8 M A DQS#5
SA_DQS#_6	AN3 M A DQS#6
SA_DQS#_7	AH5 M A DQS#7
SA_MA_0	AY16 M A A0
SA_MA_1	AU14 M A A1
SA_MA_2	AW16 M A A2
SA_MA_3	BA16 M A A3
SA_MA_4	BA17 M A A4
SA_MA_5	AU16 M A A5
SA_MA_6	AV17 M A A6
SA_MA_7	AU17 M A A7
SA_MA_8	AW17 M A A8
SA_MA_9	AT16 M A A9
SA_MA_10	AU13 M A A10
SA_MA_11	AT17 M A A11
SA_MA_12	AV20 M A A12
SA_MA_13	AV12 M A A13
SA_RAS#	AW14
SA_RCVENIN#	AK23 TP MA RCVENIN#
SA_RCVENOUT#	AK24 TP MA RCVENOUT#
SA_WE#	AY14

M_A_BS0 13,15
M_A_BS1 13,15
M_A_BS2 13,15
M_A_CAS# 13,15
M_A_DM[7..0] 13

M_A_DQS[7..0] 13

M_A_DQS#[7..0] 13

M_A_A[13..0] 13,15

M_A_RAS# 13,15 30MIL TP60

M_A_WE# 13,15 30MIL TP62

14 M_B_DQ[63..0]

M B DQ0	AK39
M B DQ1	AJ37
M B DQ2	AP39
M B DQ3	AR41
M B DQ4	AJ38
M B DQ5	AK38
M B DQ6	AN41
M B DQ7	AP41
M B DQ8	AT40
M B DQ9	AV41
M B DQ10	AU38
M B DQ11	AV38
M B DQ12	AP38
M B DQ13	AR40
M B DQ14	AW38
M B DQ15	AY38
M B DQ16	BA38
M B DQ17	AY36
M B DQ18	AR36
M B DQ19	AP36
M B DQ20	BA36
M B DQ21	AU36
M B DQ22	AP35
M B DQ23	AP34
M B DQ24	AY33
M B DQ25	BA33
M B DQ26	AT31
M B DQ27	AU29
M B DQ28	AU31
M B DQ29	AW31
M B DQ30	AV29
M B DQ31	AW29
M B DQ32	AM19
M B DQ33	AL19
M B DQ34	AP14
M B DQ35	AN14
M B DQ36	AN17
M B DQ37	AM16
M B DQ38	AP15
M B DQ39	AL15
M B DQ40	AJ11
M B DQ41	AH10
M B DQ42	AJ9
M B DQ43	AN10
M B DQ44	AK13
M B DQ45	AH11
M B DQ46	AK10
M B DQ47	AJ8
M B DQ48	BA10
M B DQ49	AW10
M B DQ50	BA4
M B DQ51	AW4
M B DQ52	AY10
M B DQ53	AY9
M B DQ54	AW5
M B DQ55	AY5
M B DQ56	AV4
M B DQ57	AR5
M B DQ58	AK4
M B DQ59	AK3
M B DQ60	AT4
M B DQ61	AK5
M B DQ62	AJ5
M B DQ63	AJ3

U27E

DDR SYSTEM MEMORY B

SB_BS_0	AT24
SB_BS_1	AV23
SB_BS_2	AY28
SB_CAS#	AR24
SB_DM_0	AK36 M B DM0
SB_DM_1	AR38 M B DM1
SB_DM_2	AT36 M B DM2
SB_DM_3	BA31 M B DM3
SB_DM_4	AL17 M B DM4
SB_DM_5	AH8 M B DM5
SB_DM_6	BA5 M B DM6
SB_DM_7	AN4 M B DM7
SB_DQS_0	AM39 M B DQS0
SB_DQS_1	AT39 M B DQS1
SB_DQS_2	AU35 M B DQS2
SB_DQS_3	AR29 M B DQS3
SB_DQS_4	AR16 M B DQS4
SB_DQS_5	AR10 M B DQS5
SB_DQS_6	AR7 M B DQS6
SB_DQS_7	AN5 M B DQS7
SB_DQS#_0	AM40 M B DQS#0
SB_DQS#_1	AU39 M B DQS#1
SB_DQS#_2	AT35 M B DQS#2
SB_DQS#_3	AP29 M B DQS#3
SB_DQS#_4	AP16 M B DQS#4
SB_DQS#_5	AT10 M B DQS#5
SB_DQS#_6	AT7 M B DQS#6
SB_DQS#_7	AP5 M B DQS#7
SB_MA_0	AY23 M B A0
SB_MA_1	AW24 M B A1
SB_MA_2	AY24 M B A2
SB_MA_3	AR28 M B A3
SB_MA_4	AT27 M B A4
SB_MA_5	AT28 M B A5
SB_MA_6	AU27 M B A6
SB_MA_7	AV28 M B A7
SB_MA_8	AV27 M B A8
SB_MA_9	AW27 M B A9
SB_MA_10	AV24 M B A10
SB_MA_11	BA27 M B A11
SB_MA_12	AY27 M B A12
SB_MA_13	AR23 M B A13
SB_RAS#	AU23
SB_RCVENIN#	AK16 TP MB RCVENIN#
SB_RCVENOUT#	AK18 TP MB RCVENOUT#
SB_WE#	AR27

M_B_BS0 14,15
M_B_BS1 14,15
M_B_BS2 14,15
M_B_CAS# 14,15
M_B_DM[7..0] 14

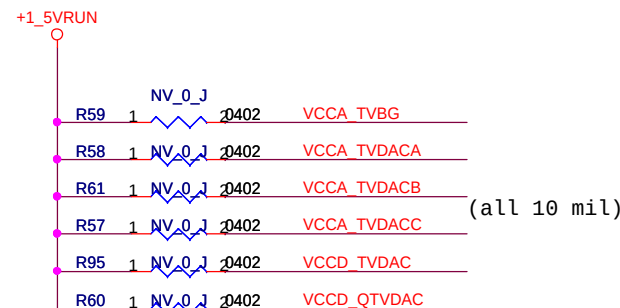
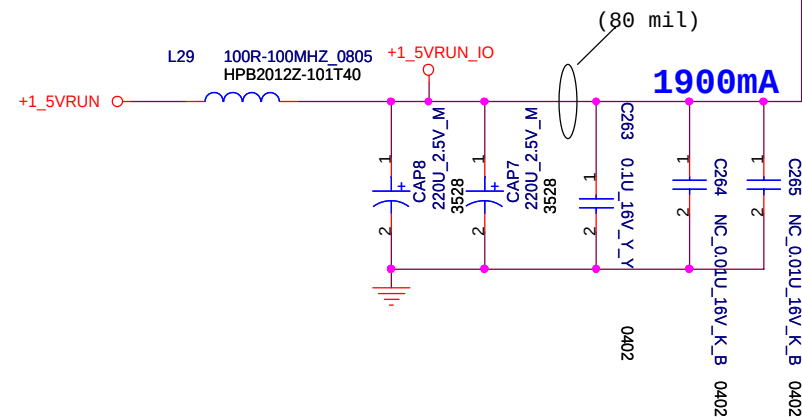
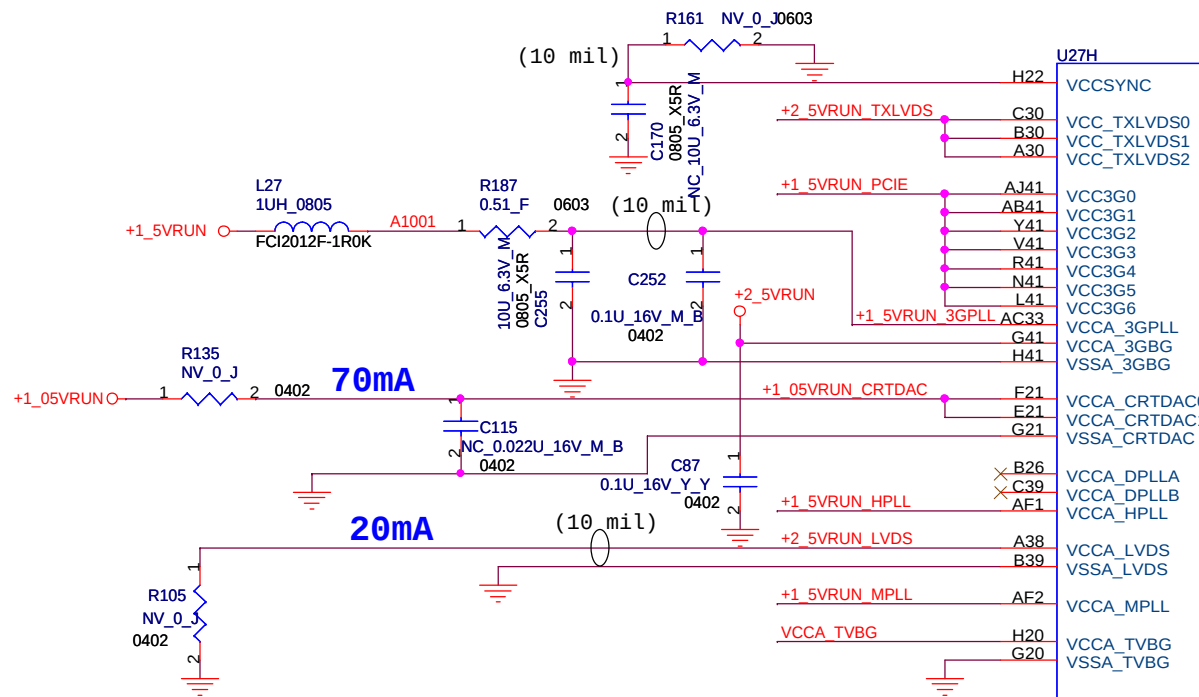
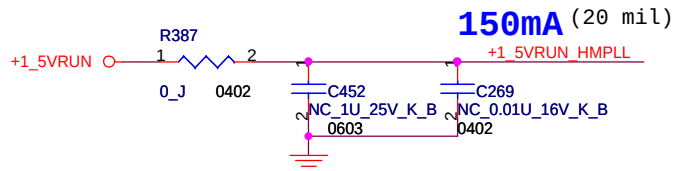
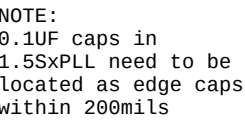
M_B_DQS[7..0] 14

M_B_DQS#[7..0] 14

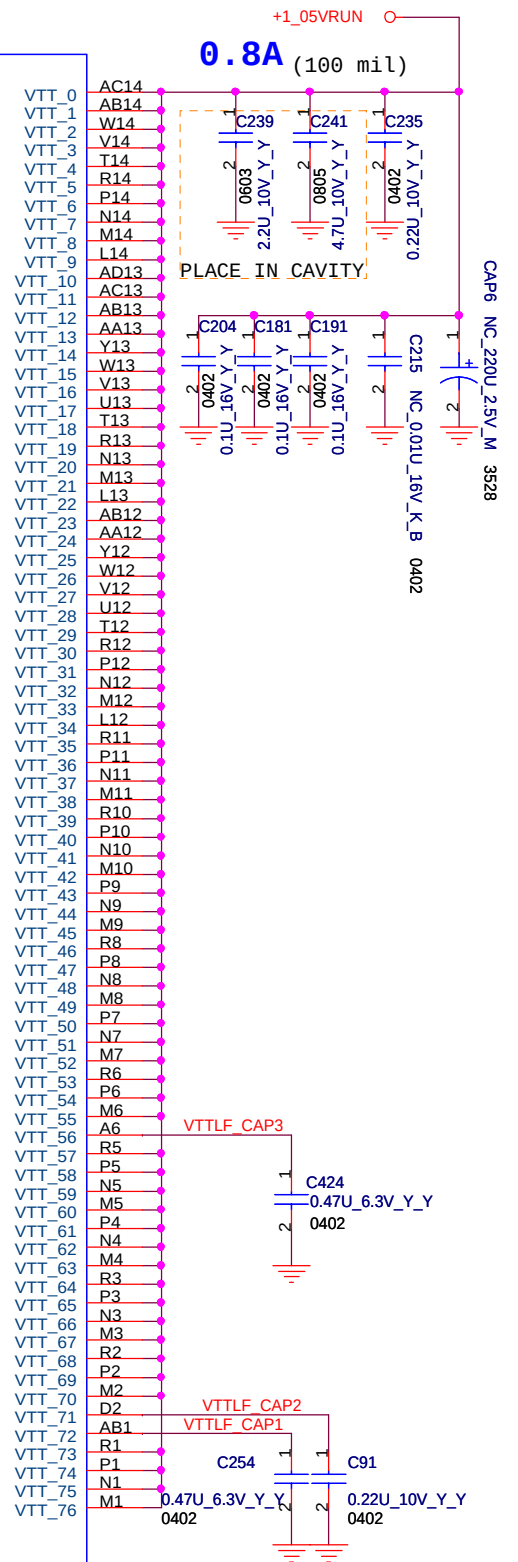
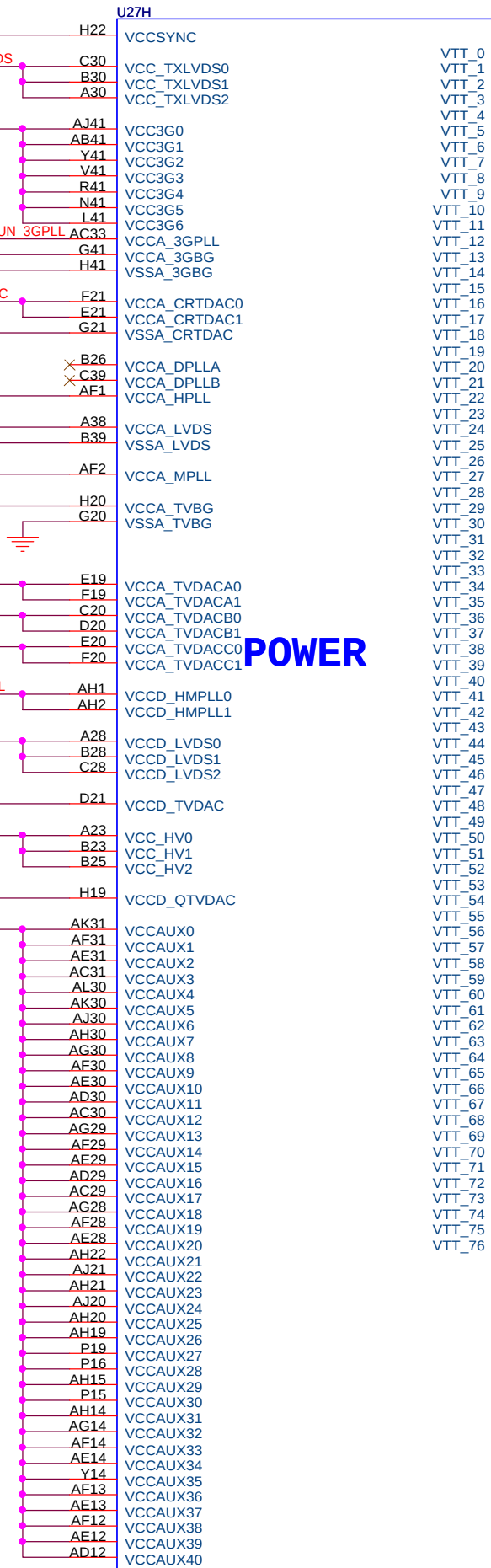
M_B_A[13..0] 14,15

M_B_RAS# 14,15 30MIL TP59

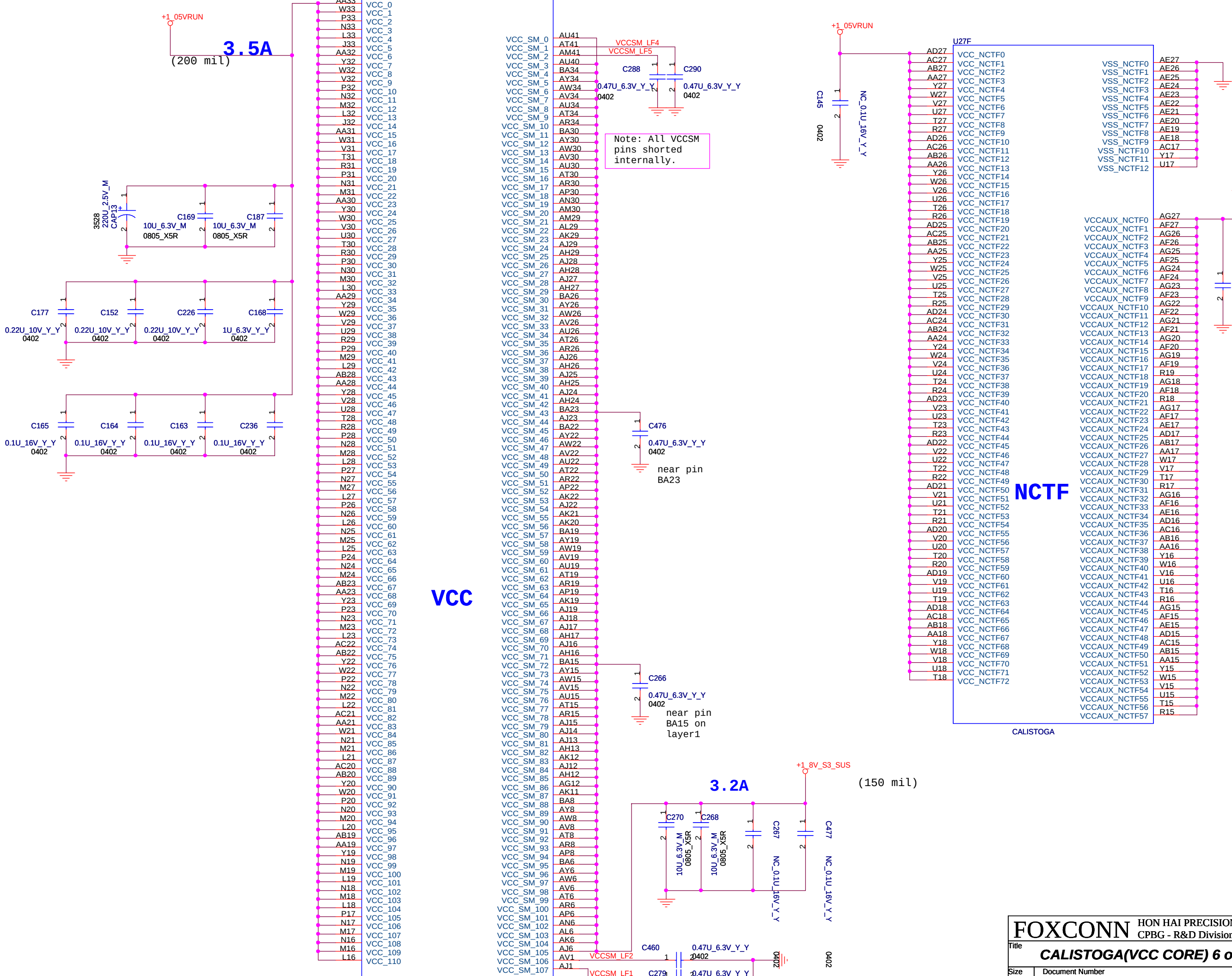
M_B_WE# 14,15 30MIL TP61



VCCA_TVDACA	E19	VCCA_TVDACA
	F19	VCCA_TVDACA
VCCA_TVDACB	C20	VCCA_TVDACB
	D20	VCCA_TVDACB
VCCA_TVDACC	E20	VCCA_TVDACC
	F20	VCCA_TVDACC
+1_5VRUN_HMPLL	AH1	VCCD_HMPLL0
	AH2	VCCD_HMPLL1
+1_5VRUN_LVDS	A28	VCCD_LVDS0
	B28	VCCD_LVDS1
	C28	VCCD_LVDS2
VCCD_TVDAC	D21	VCCD_TVDAC
+3VRUN_HV	A23	VCC_HV0
	B23	VCC_HV1
	B25	VCC_HV2
VCCD_QTVDAC	H19	VCCD_QTVDAC



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7 MCH_CFG_5 1 30MIL TP45

MCH_CFG_5	Low = DMIX2 High = DMIX4
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7 MCH_CFG_6 1 30MIL TP40

MCH_CFG_6	Low = Moby Dick High = Calistoga
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DDR2 select (default high)

7 MCH_CFG_7 1 30MIL TP36

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
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7 MCH_CFG_9 1 30MIL TP36

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation
---	--

For layout convenience

7 MCH_CFG_10 1 30MIL TP35

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
--	-----------------------------------

7 MCH_CFG_11 1 30MIL TP35

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga
--------------------------------------	-----------------------------------

7 MCH_CFG_12 1 30MIL TP47
7 MCH_CFG_13 1 30MIL TP55

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---

7 MCH_CFG_16 1 30MIL TP44

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
------------------------------------	---

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------

7 MCH_CFG_18 1 30MIL TP40

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
--------------------------------------	--

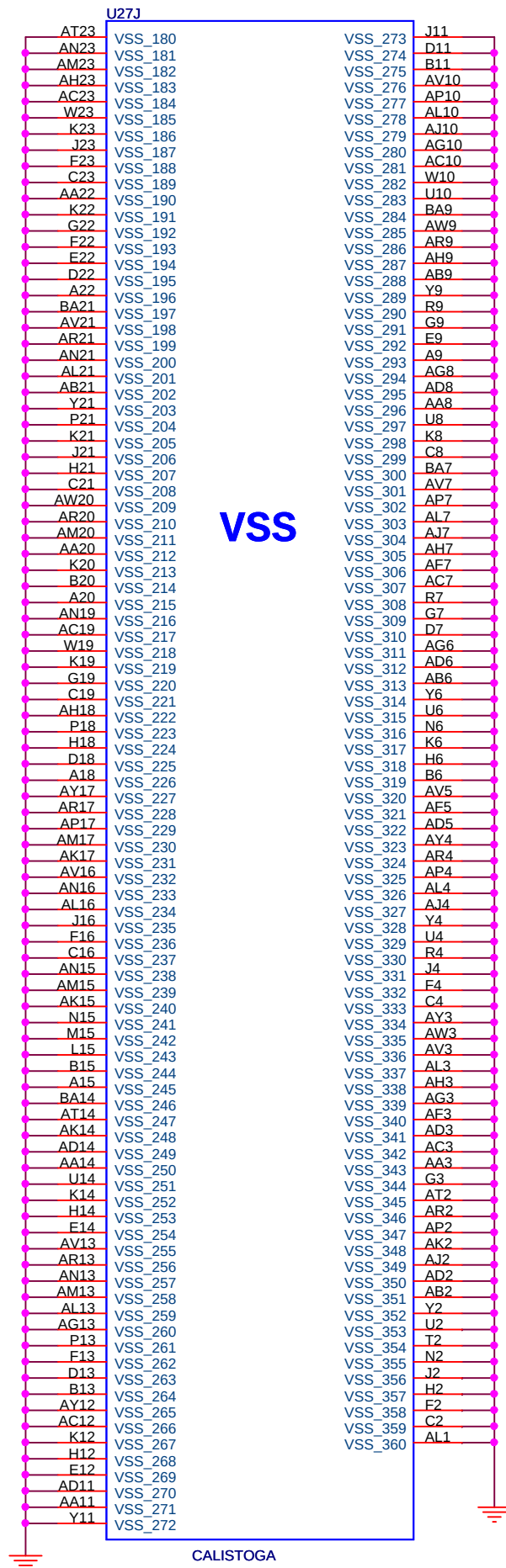
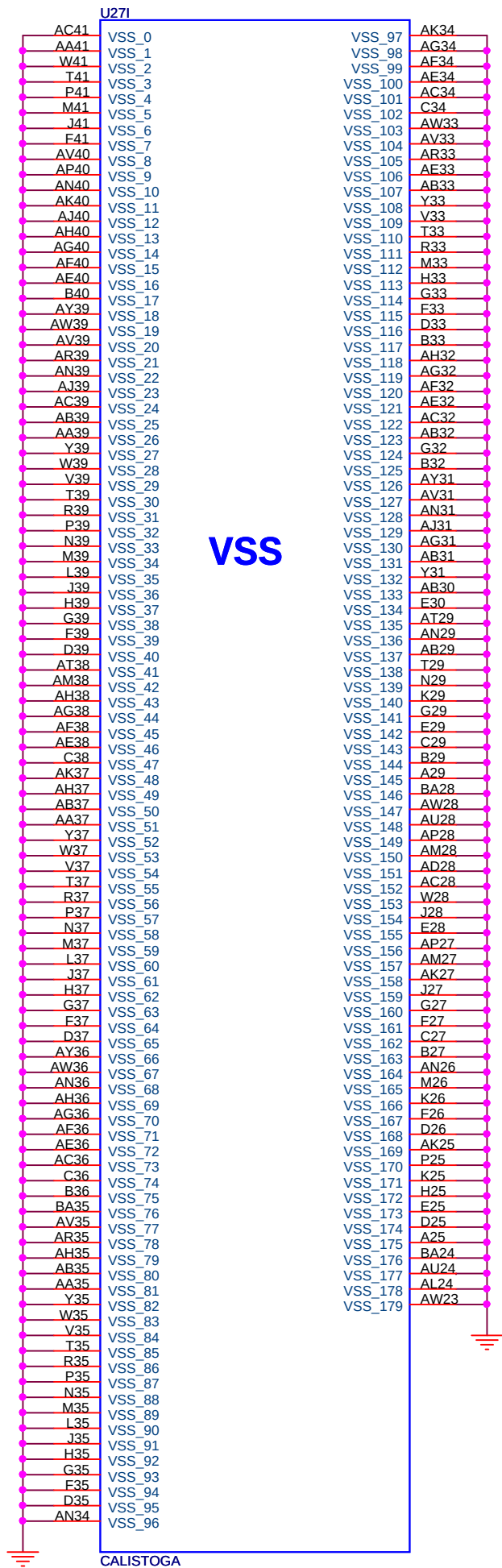
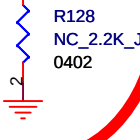
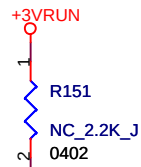
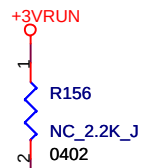
7 MCH_CFG_19 1 30MIL TP36

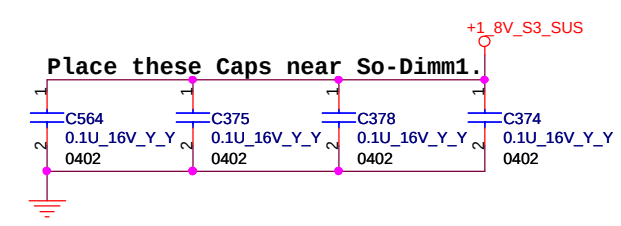
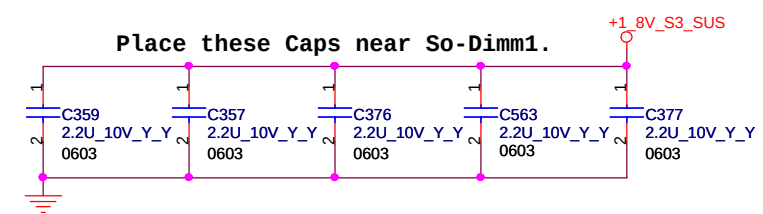
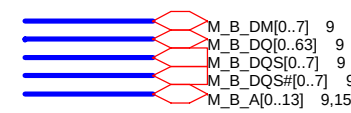
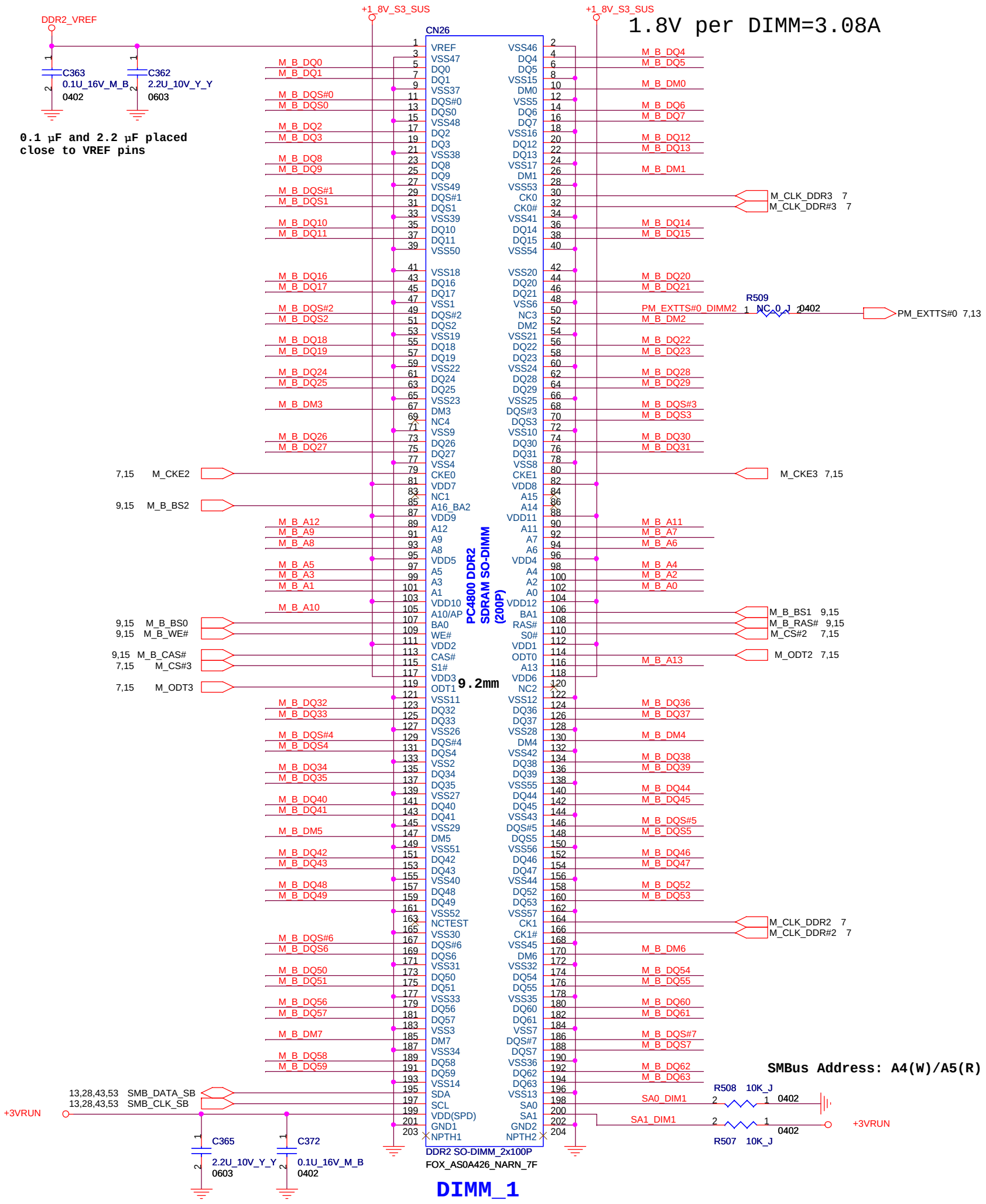
MCH_CFG_20 (PCIE Backward Interpoerability mode)	Low = Only SDV0 or PCIE x1 is operational (defaults)) High = SDV0 and PCIE x1 are operating simultaneously via the PEG port
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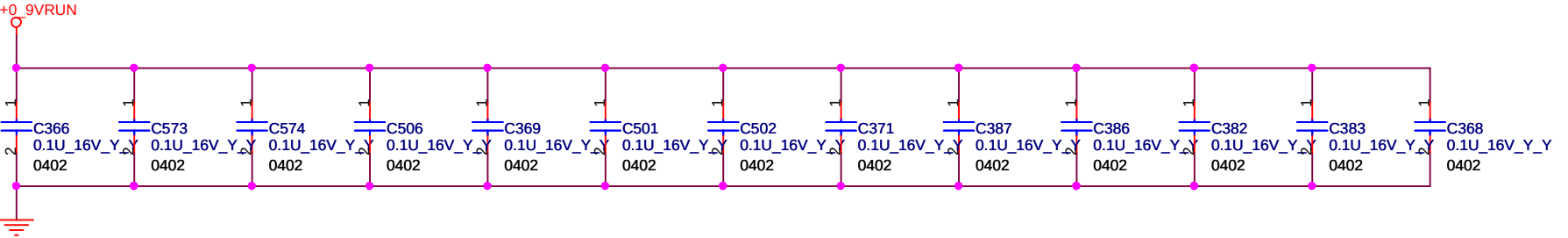
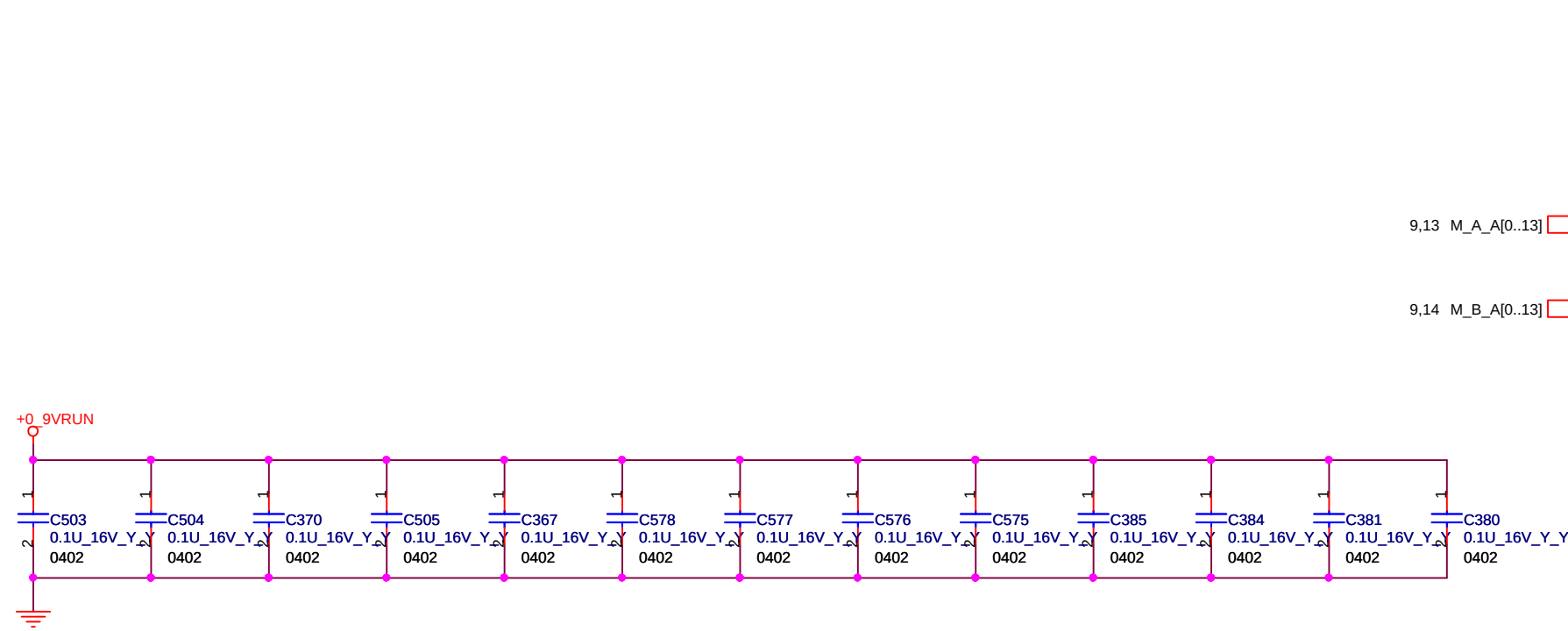
7 MCH_CFG_20 1 30MIL TP52

Layout Noe:
Location of all MCH_CFG strap resistors
needs to be close to trace to minimize
stub

Check CALISTOGA version , after A2 version , if
sysfec can't boot up then NC the pull low R

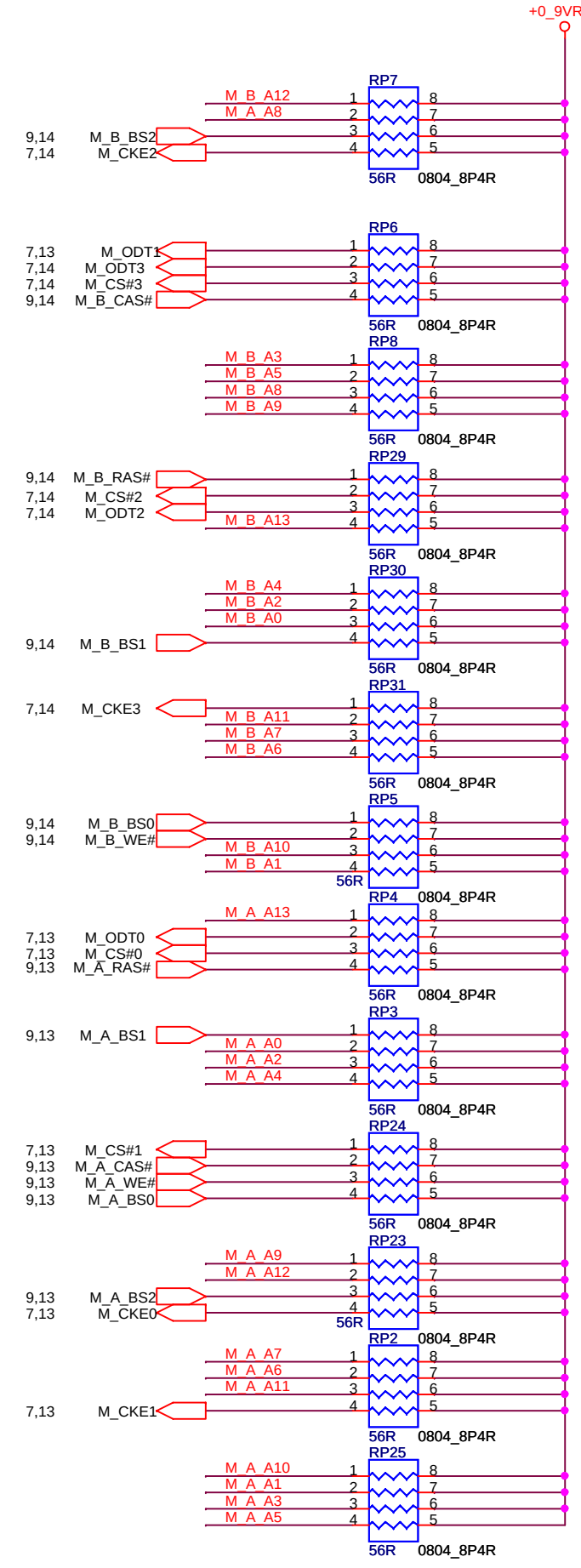


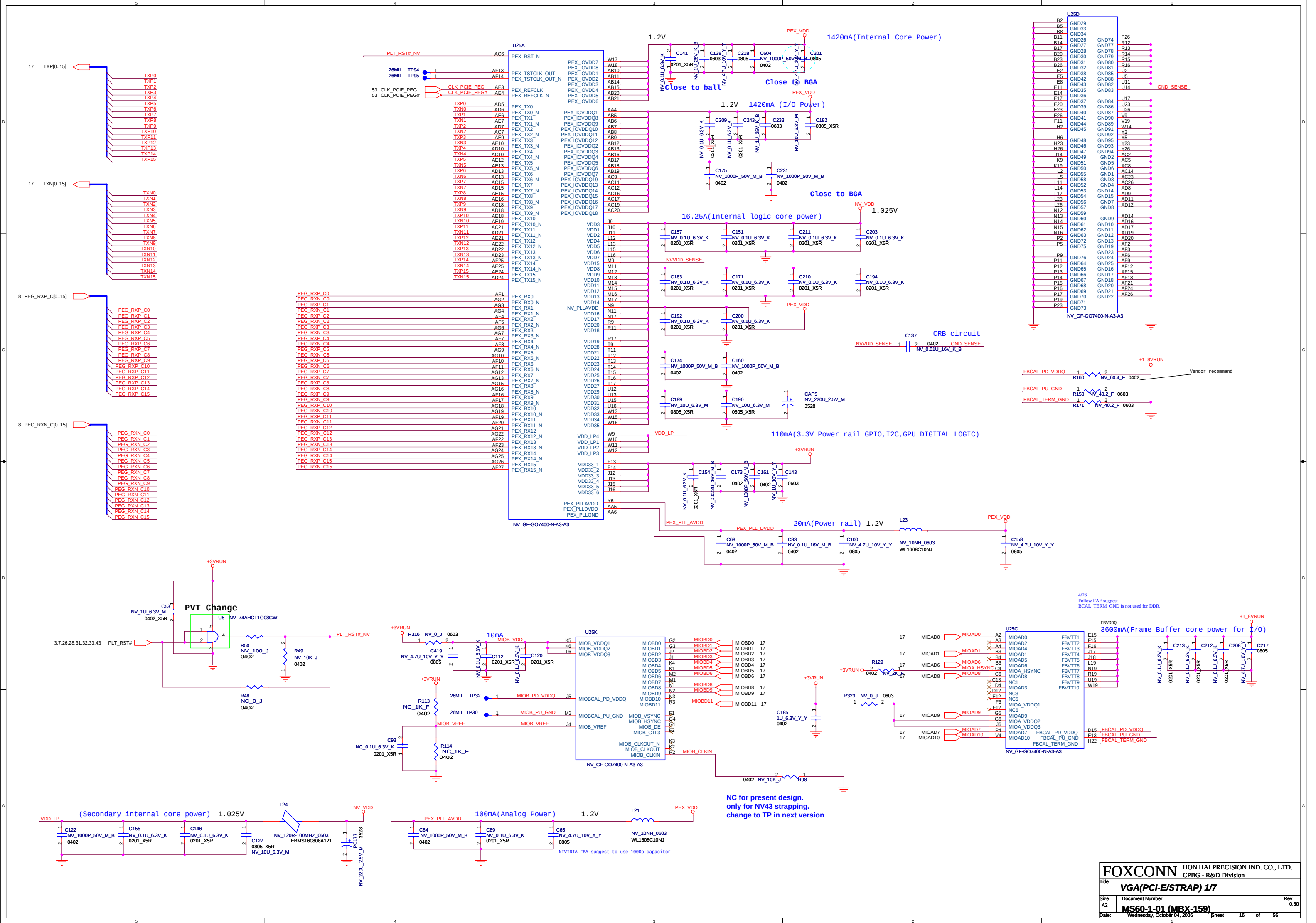


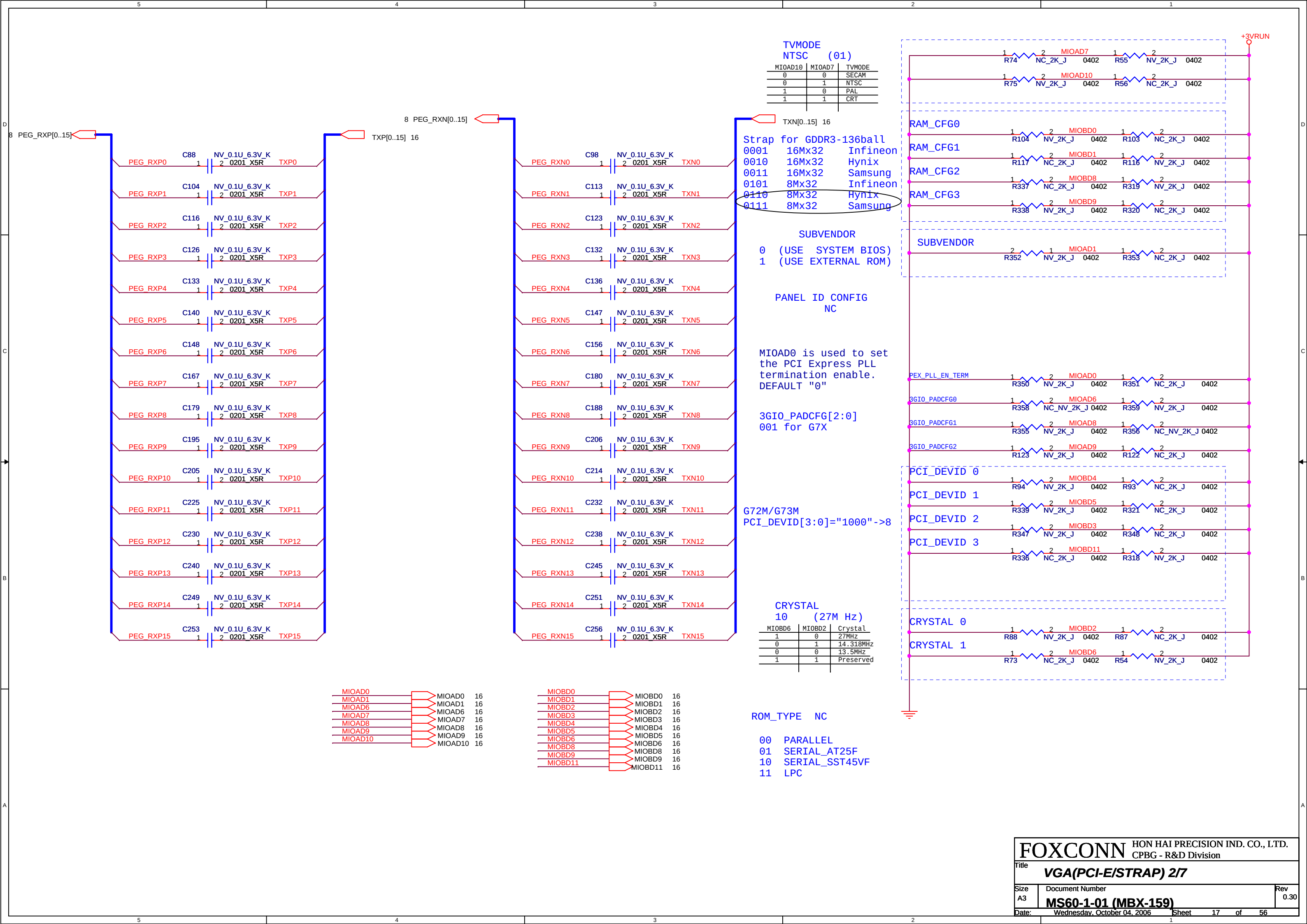


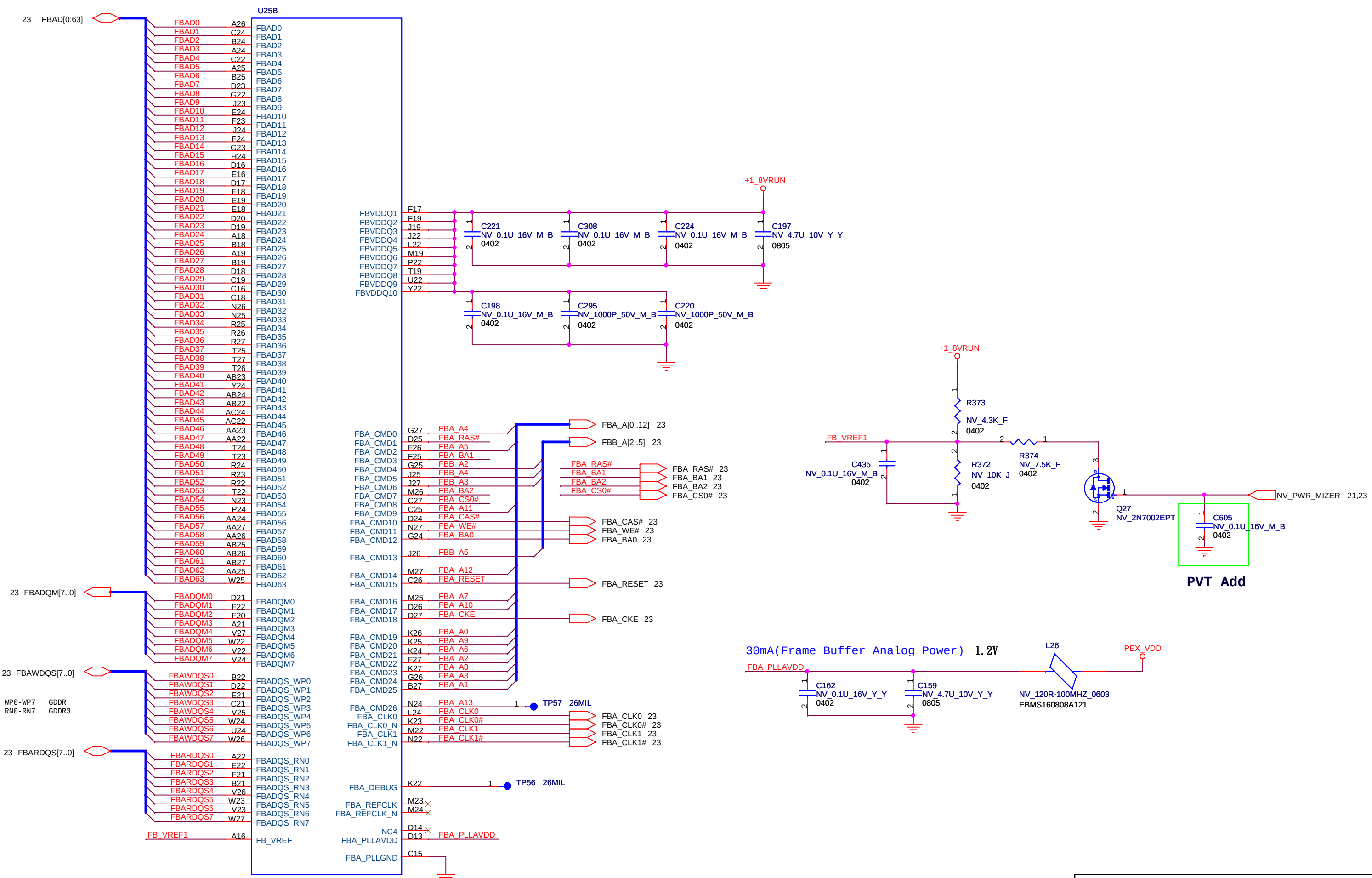
9,13 M_A_A[0..13]

9,14 M_B_A[0..13]

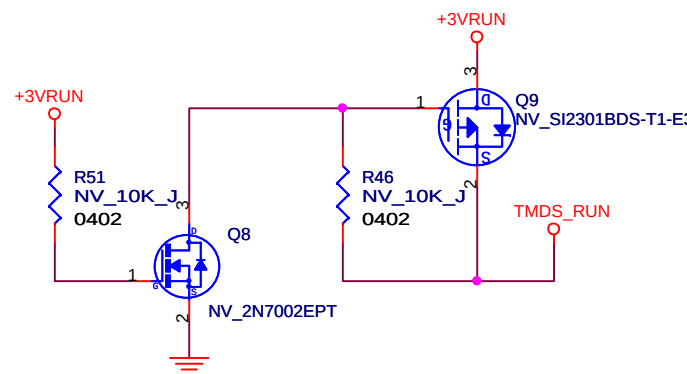
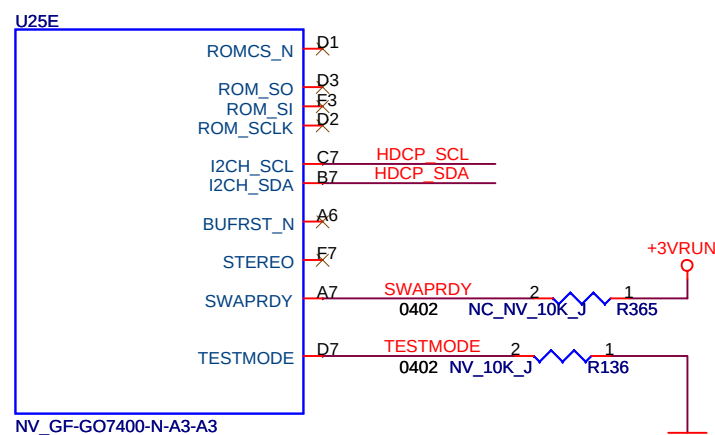
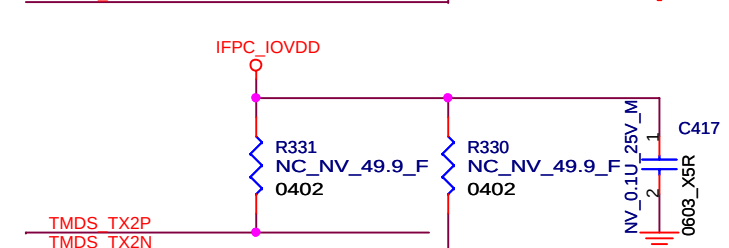
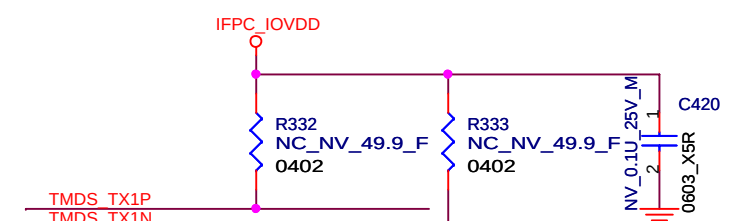
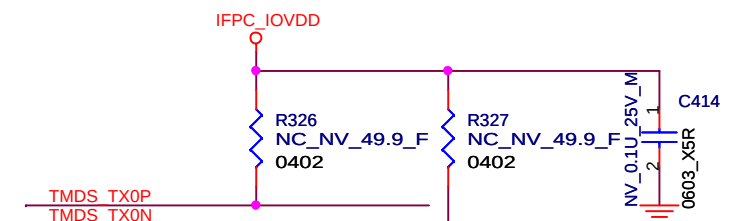
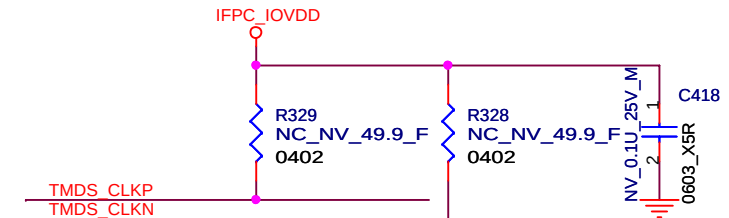
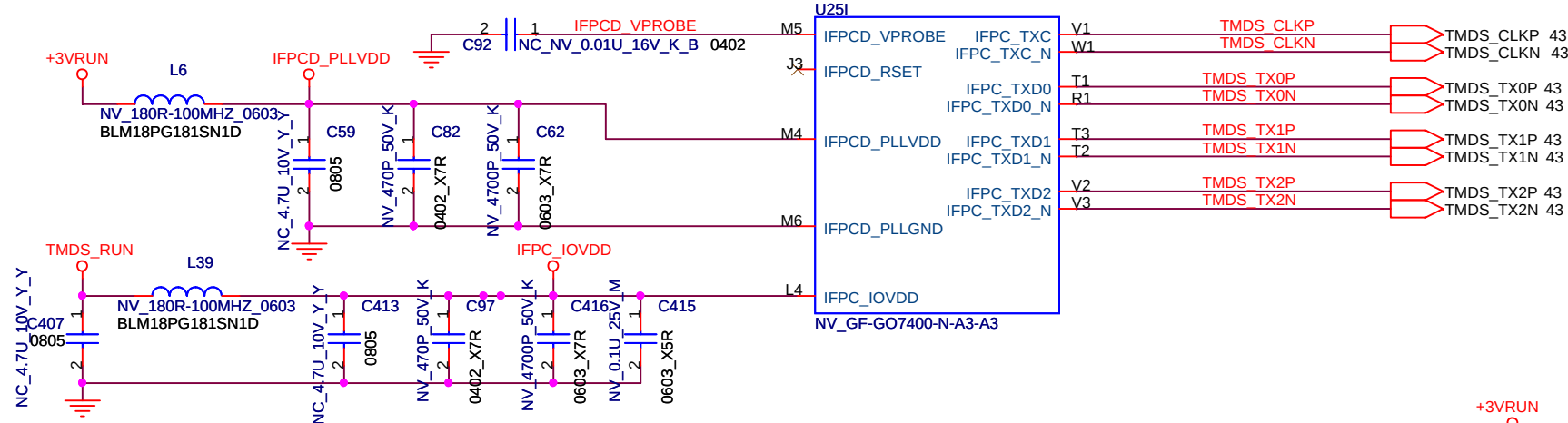
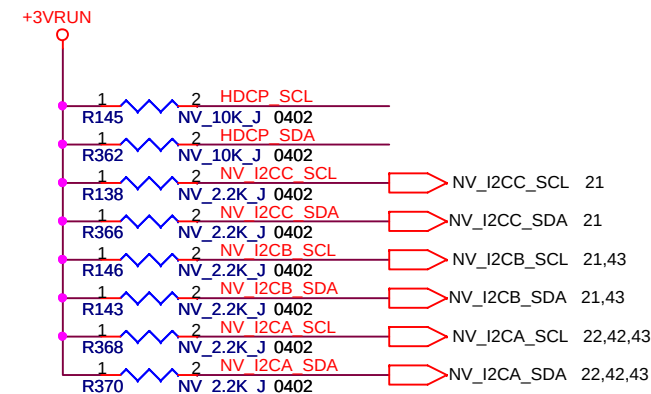
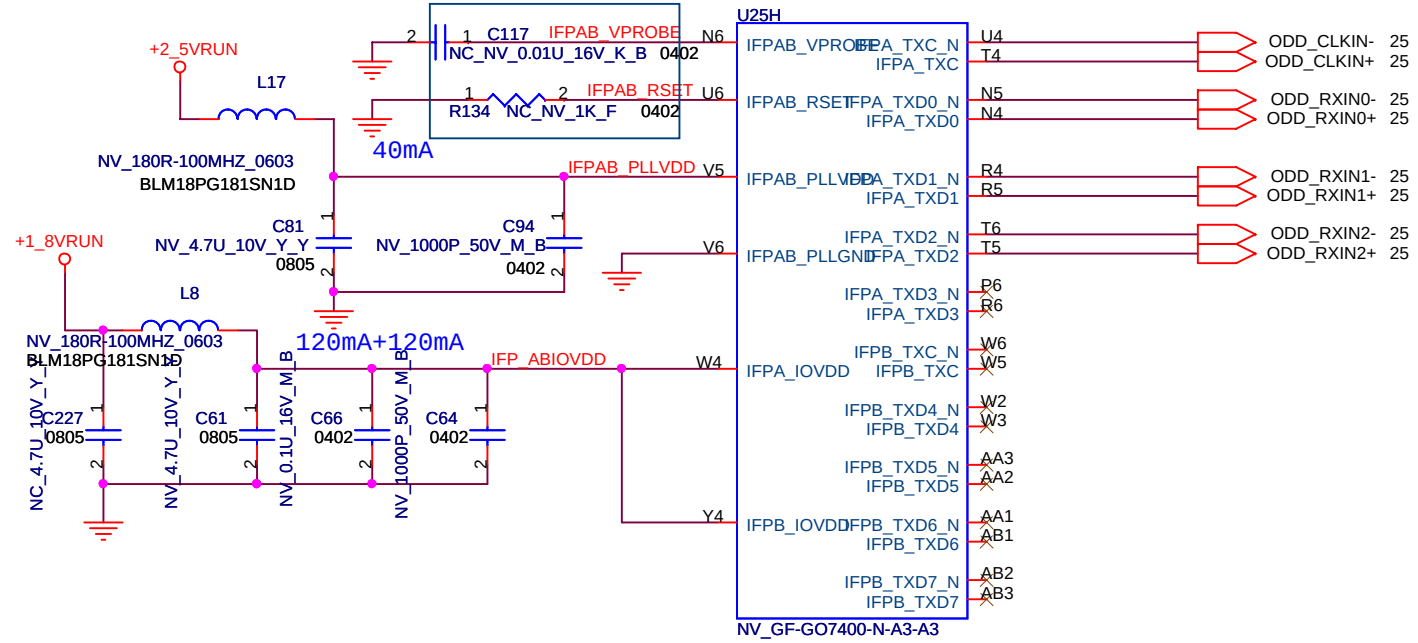


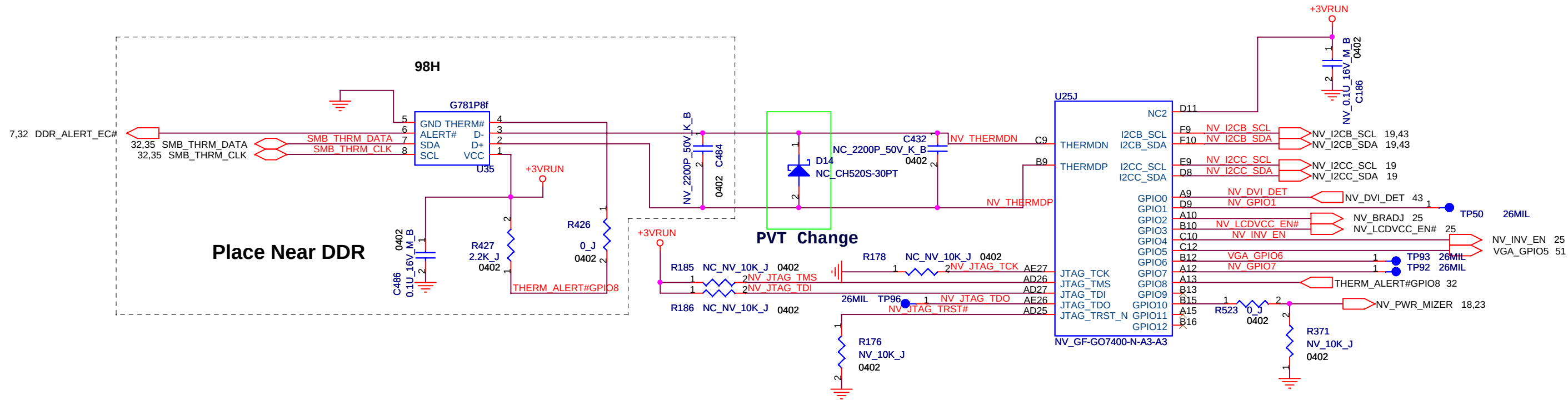






UN STUFF FOR G7X

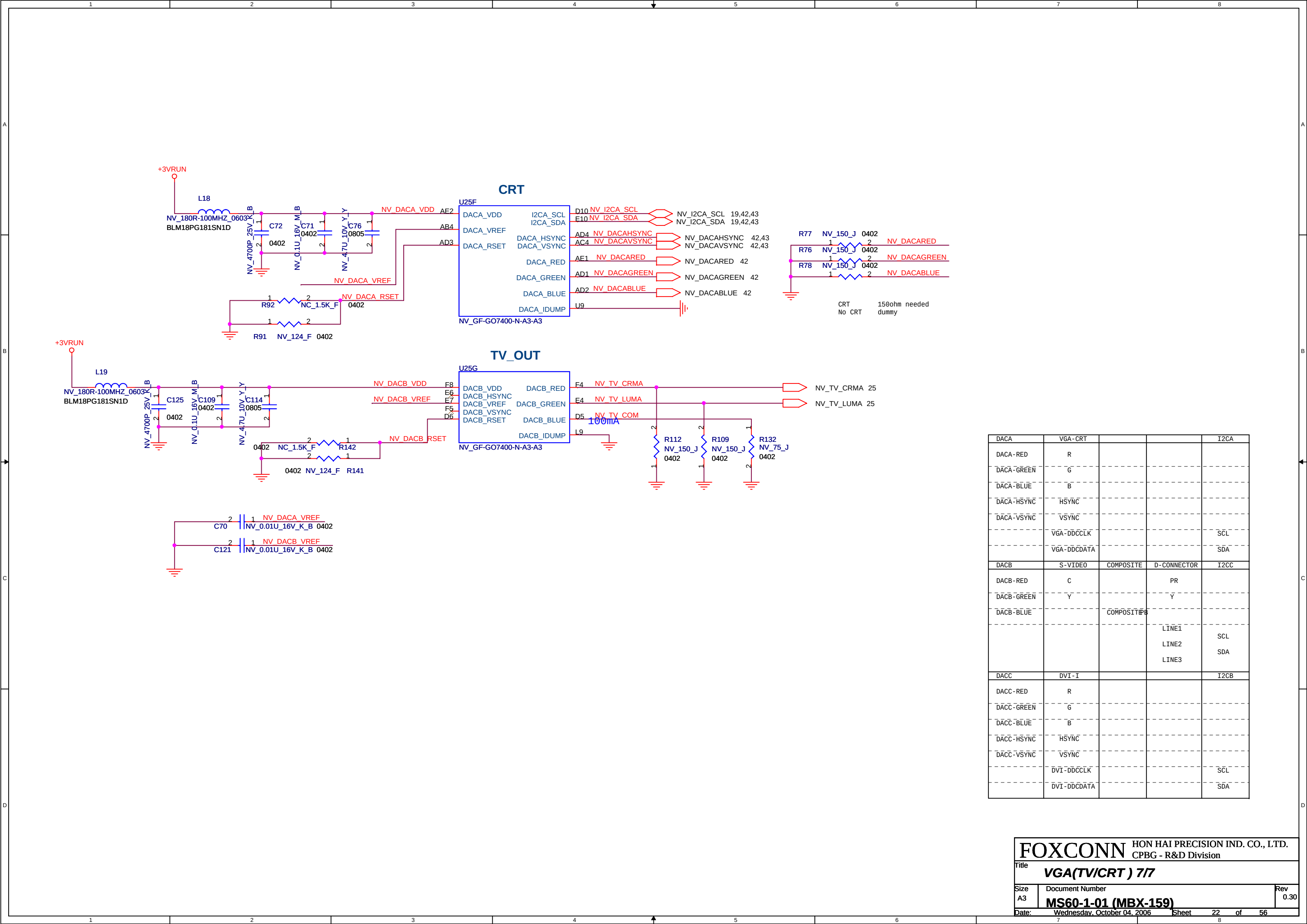




Check Spec.

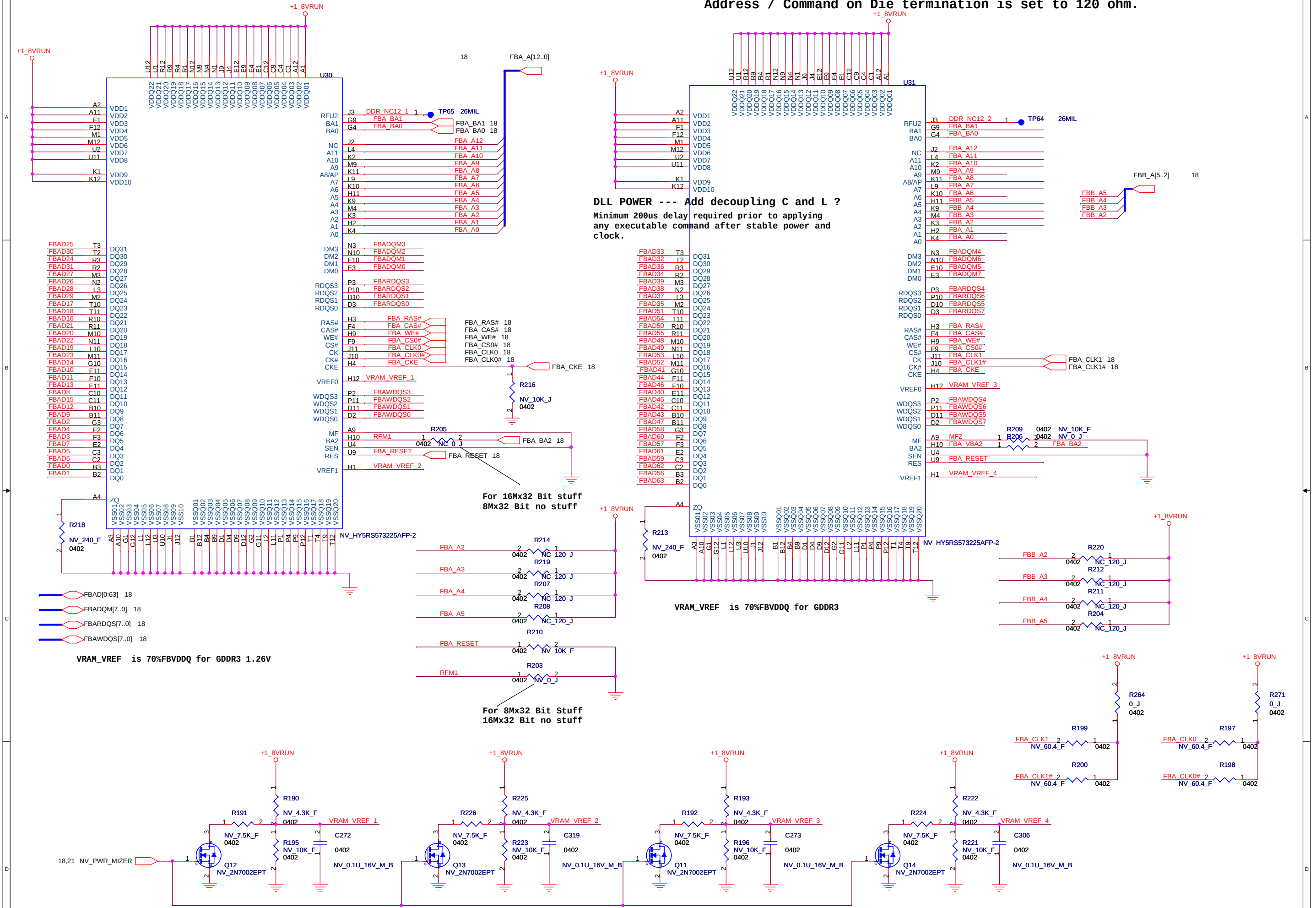
	I/O	Inter pull low	GPIO TABLE
GPI00	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPI01	I	Yes	Hot Plug Detect 1 (HPD1)
GPI02	0	Yes	Panel Brightness (PWM) Active High
GPI03	0	No	Panel Power Active Low
GPI04	0	Yes	Panel Backlight On/Off Active High
GPI05	0	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPI06	0	Yes	
GPI07	0	Yes	MEM VID
GPI08	I	No	Thermal Alert Active Low
GPI09	0	No (Low)	Fan control. Support either PWM or on/off
GPI010	I/O	No	Power Mizer control signal
GPI011	0	No (Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPI012	0	No	Available for general use.

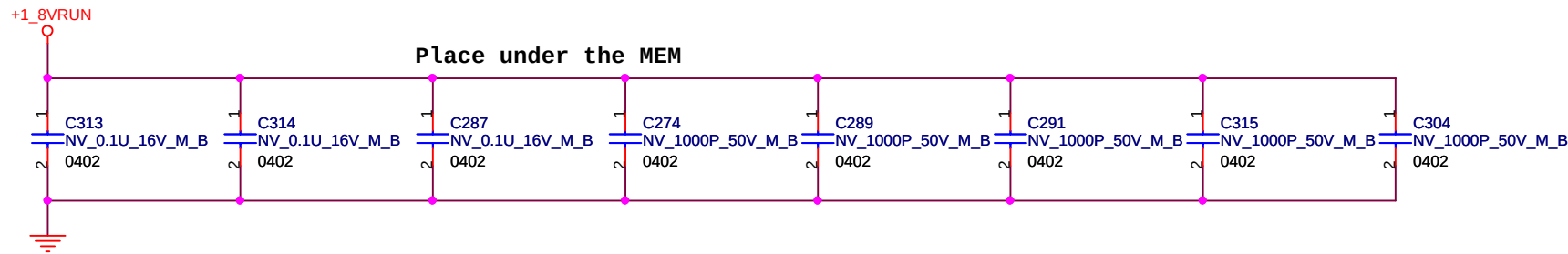
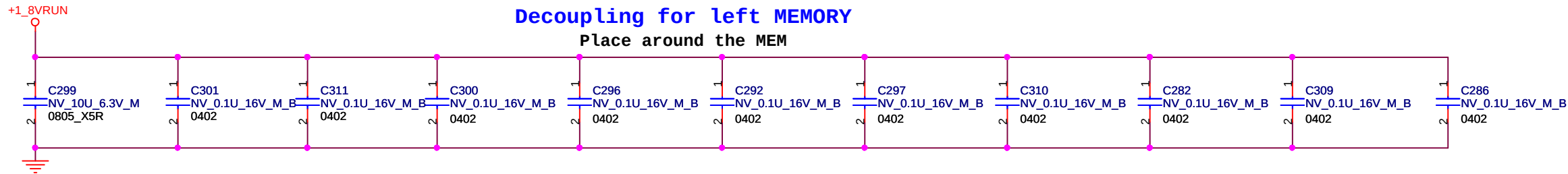
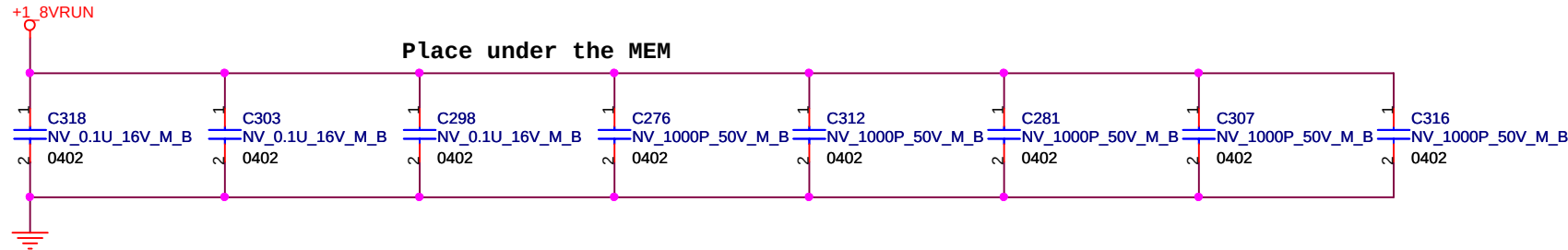
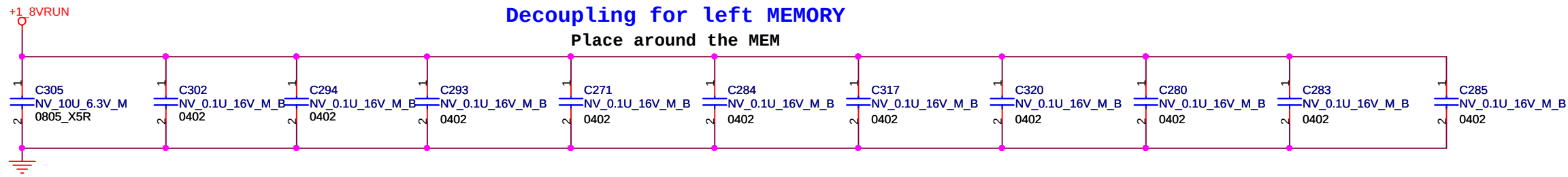
PWR_MIZER LEVEL	H	L
Vref	50% FBVDDQ	70% FBVDDQ



DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCLK			SCL
	VGA-DDCDATA			SDA
DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CB
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	DVI-I			I2CB
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCLK			SCL
	DVI-DDCDATA			SDA

Address / Command on Die termination is set to 120 ohm.



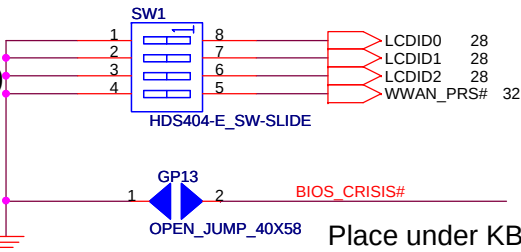


LVDS

19 ODD_RXIN1-
19 ODD_RXIN1+
19 ODD_CLKIN-
19 ODD_CLKIN+

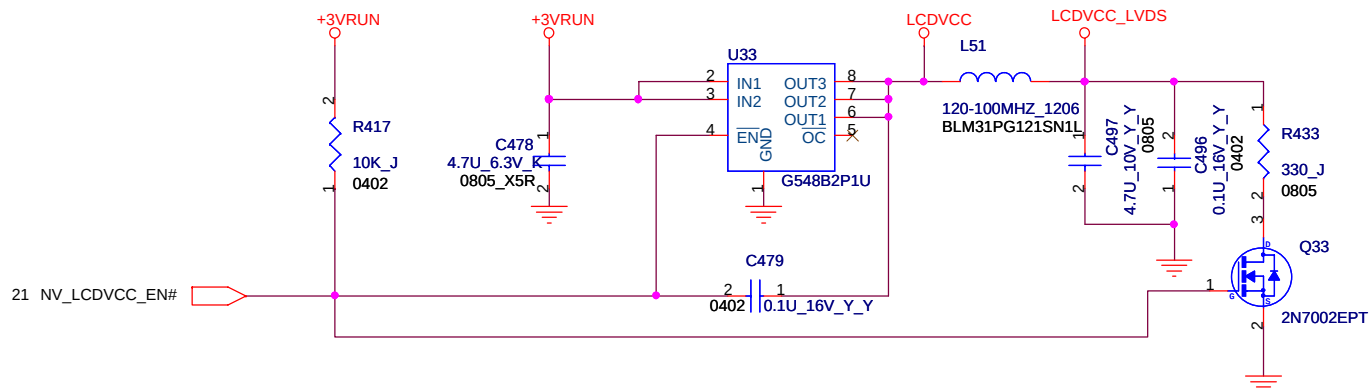
19 ODD_RXIN0-
19 ODD_RXIN0+
19 ODD_RXIN2-
19 ODD_RXIN2+

PANEL ID

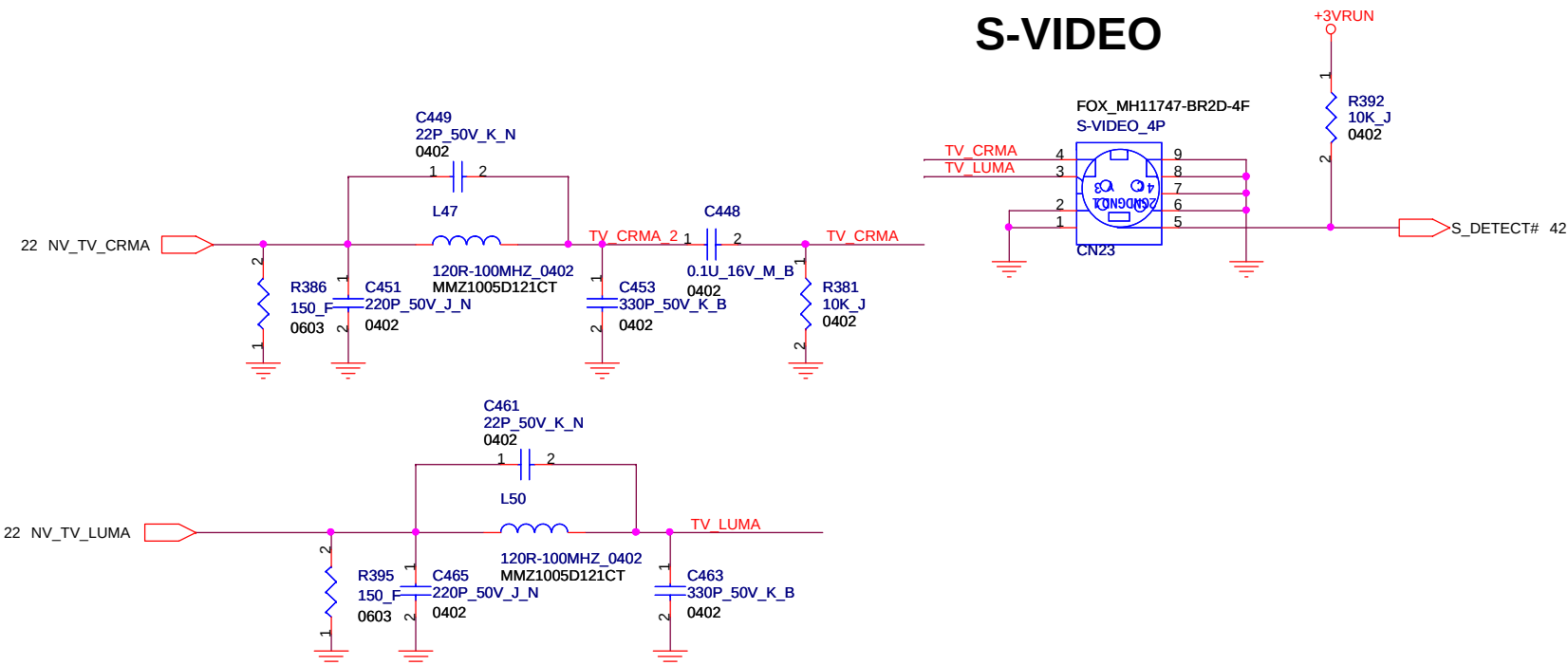


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

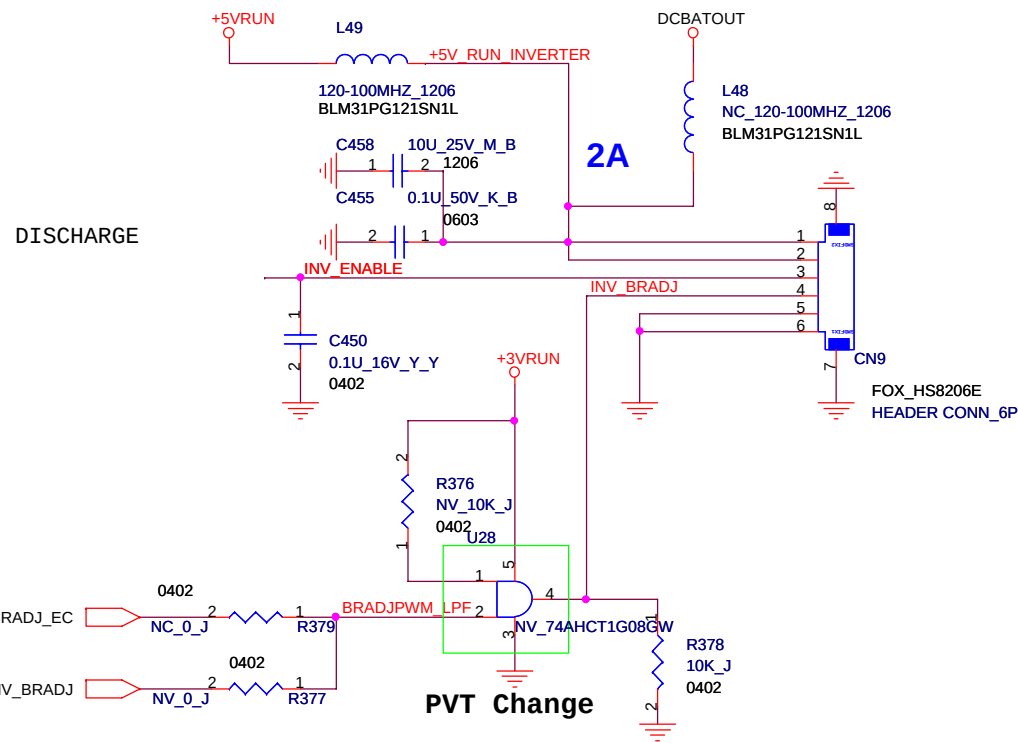
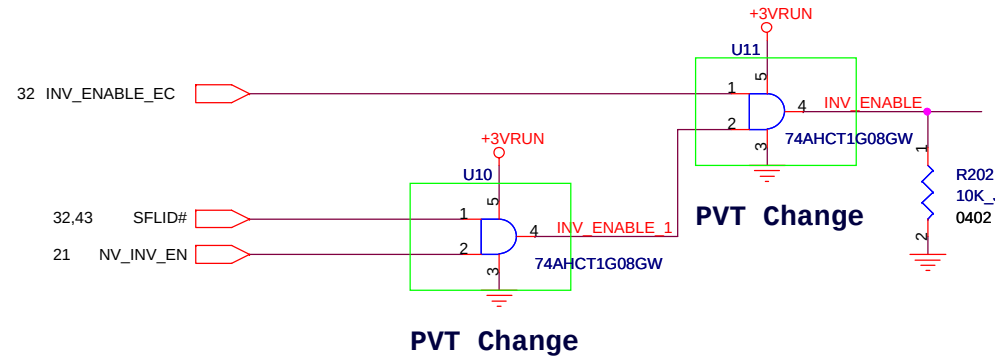
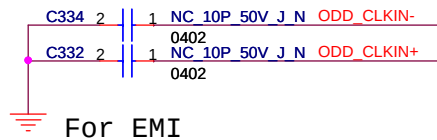
LCD POWER



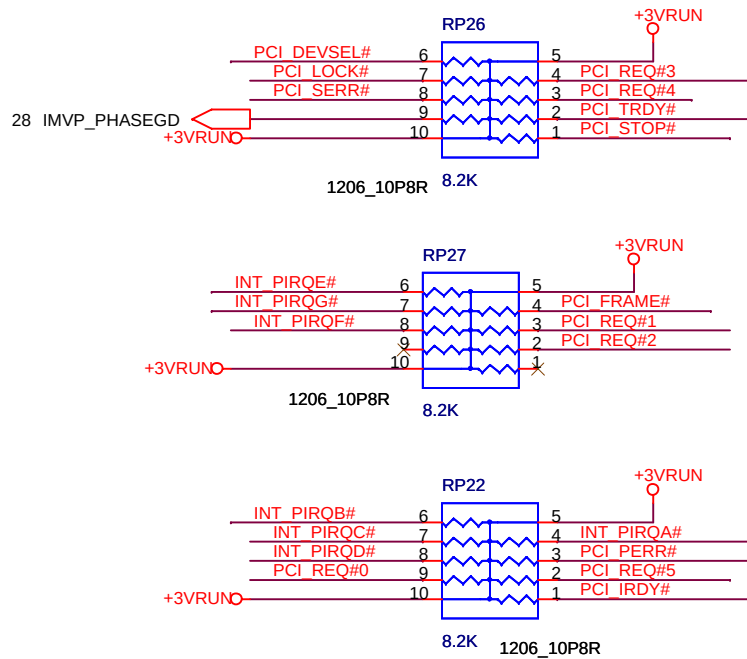
S-VIDEO



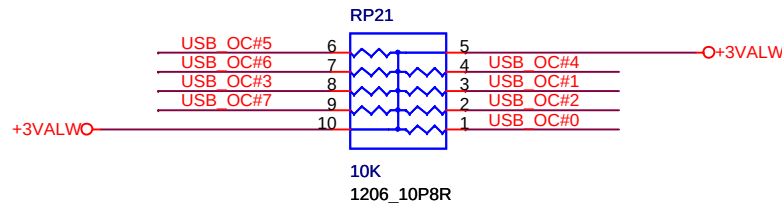
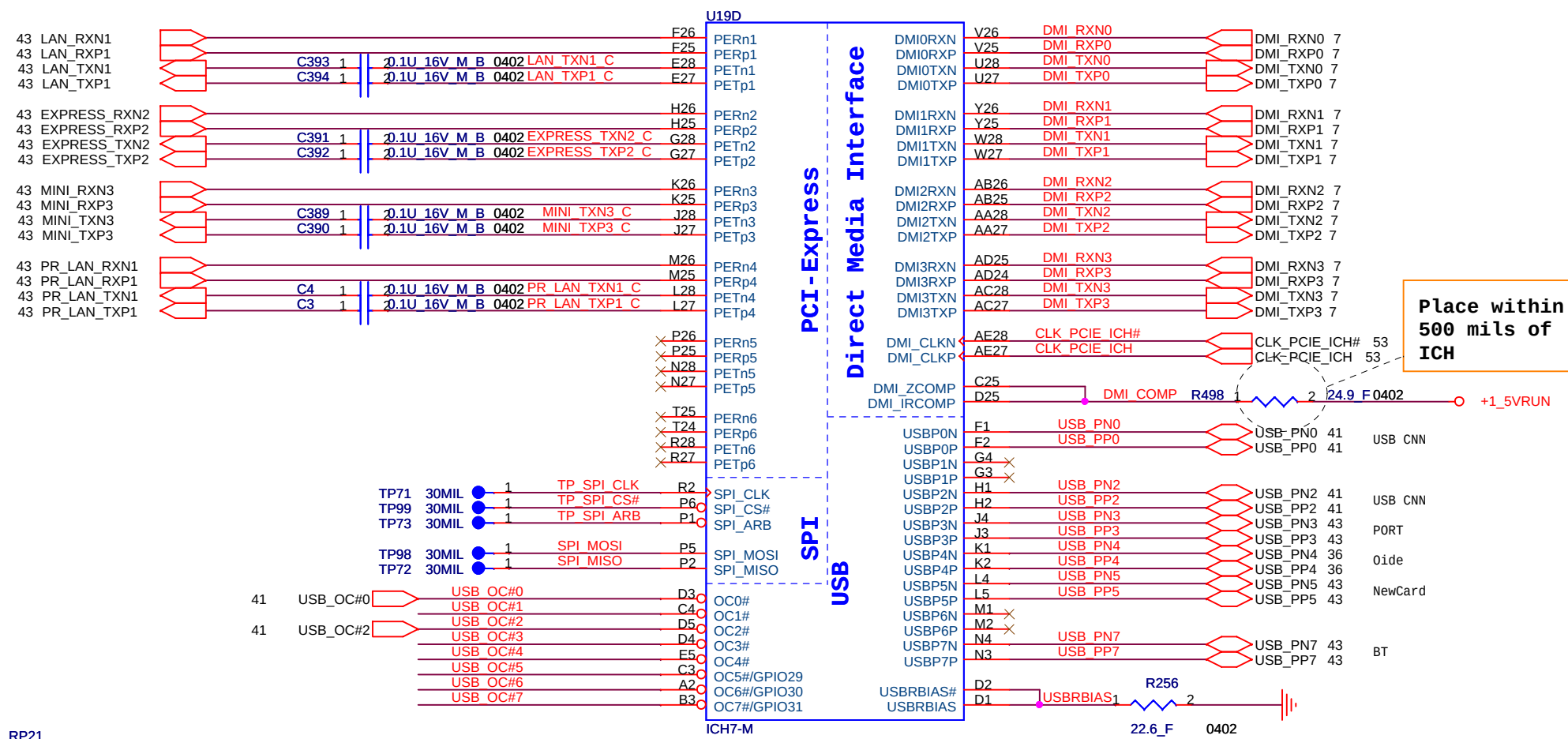
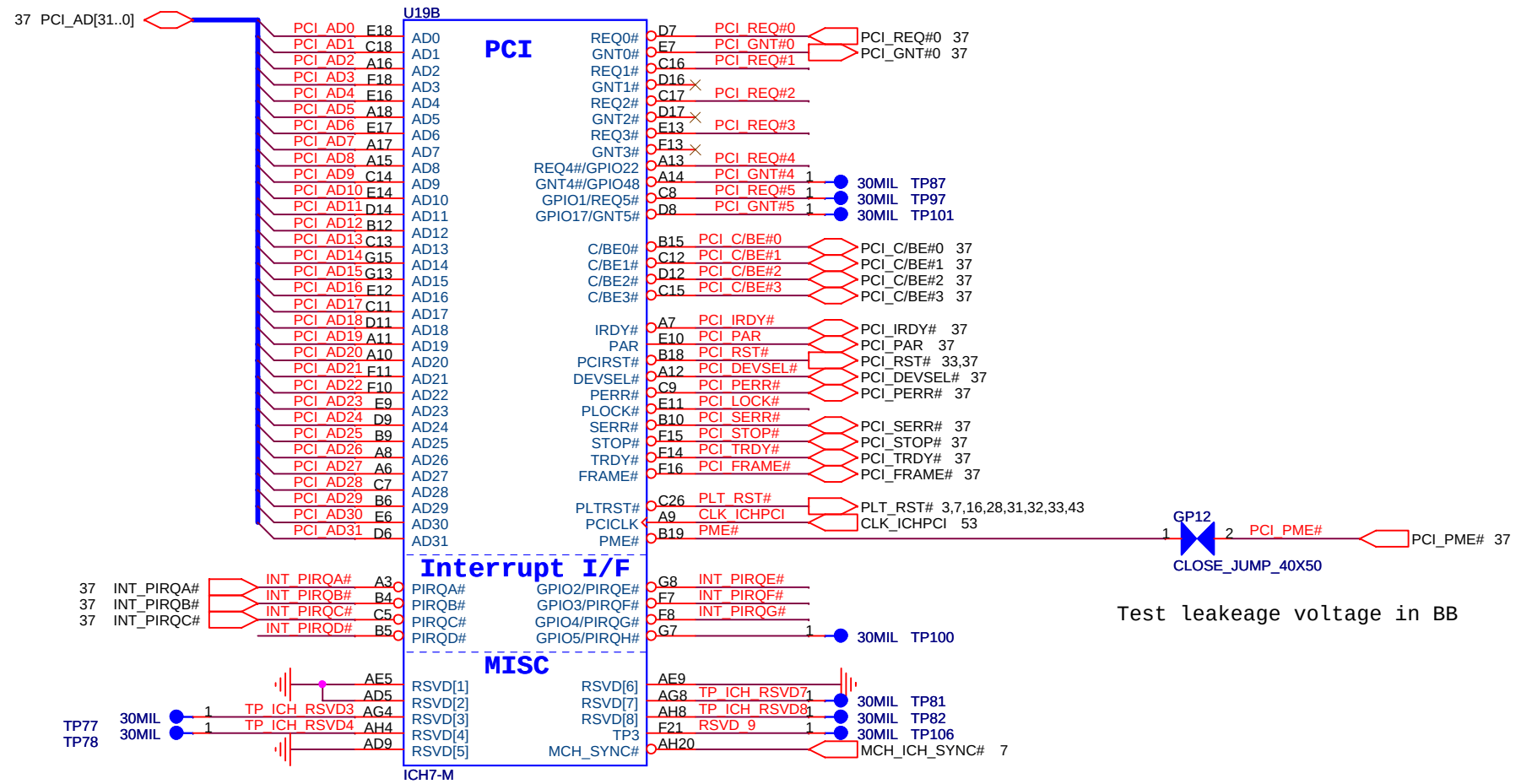
LVDS CONNECTOR



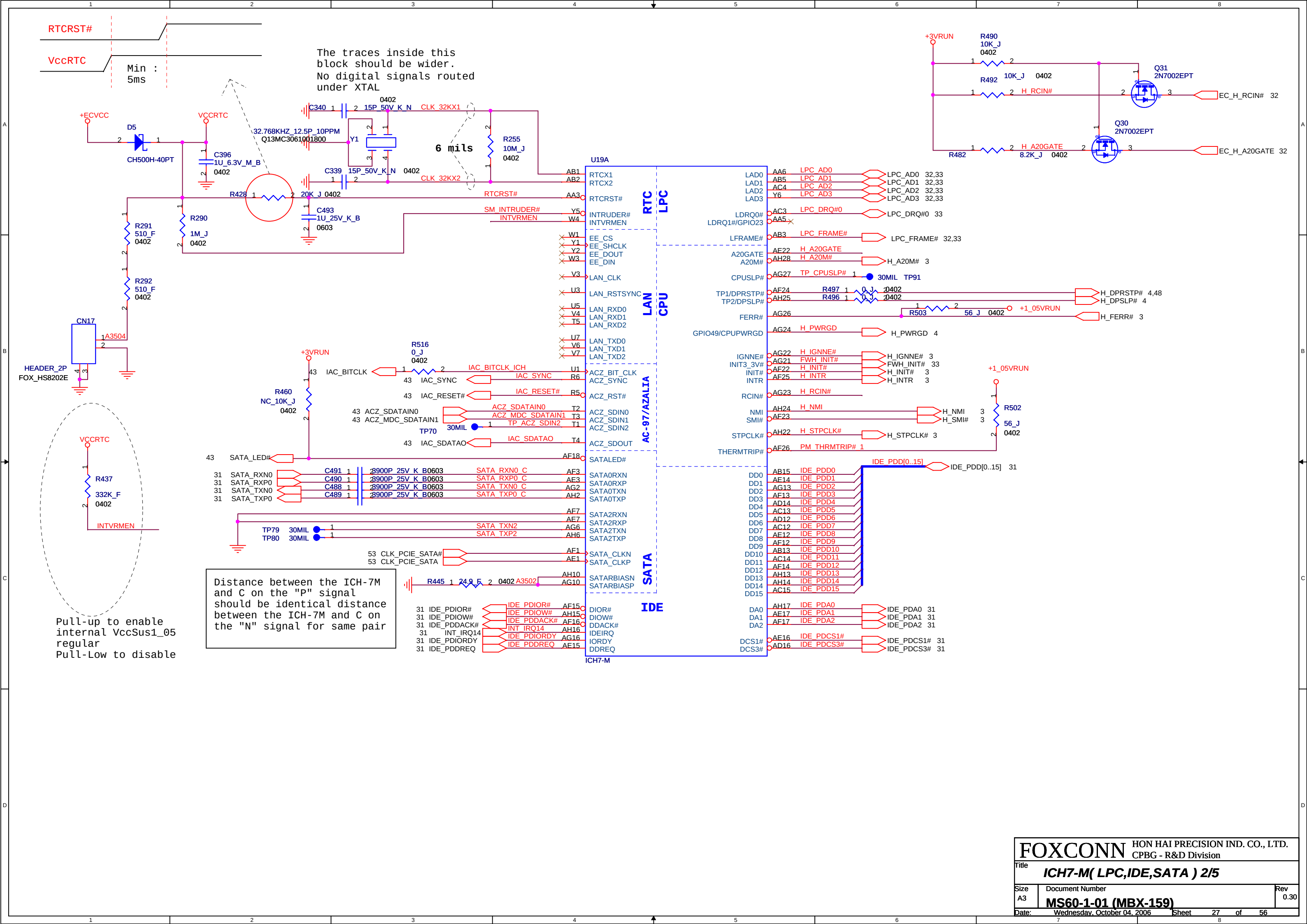
INVERTER CONNECTOR

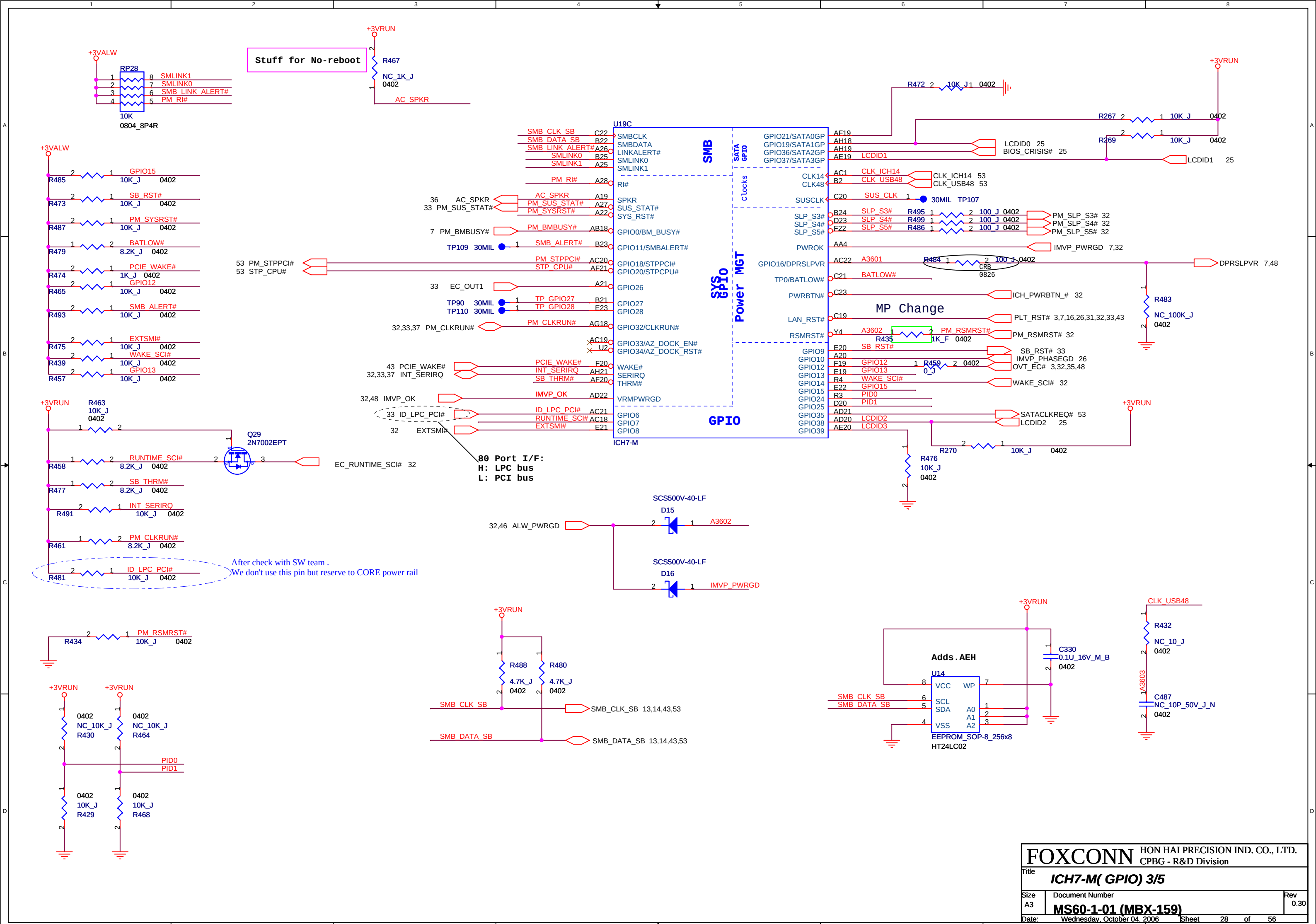


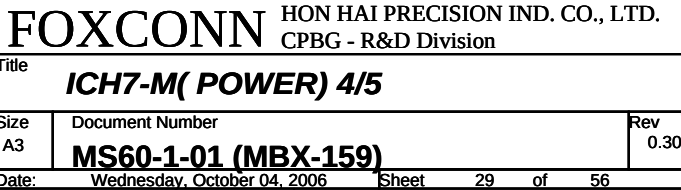
PCI Pullups

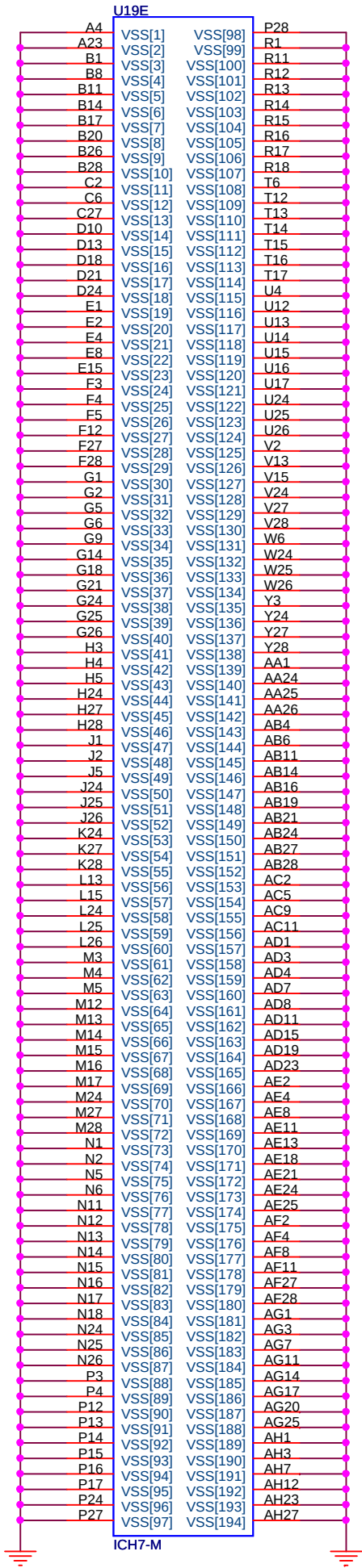


Place within 500 mils of ICH and don't routing next to high speed signals

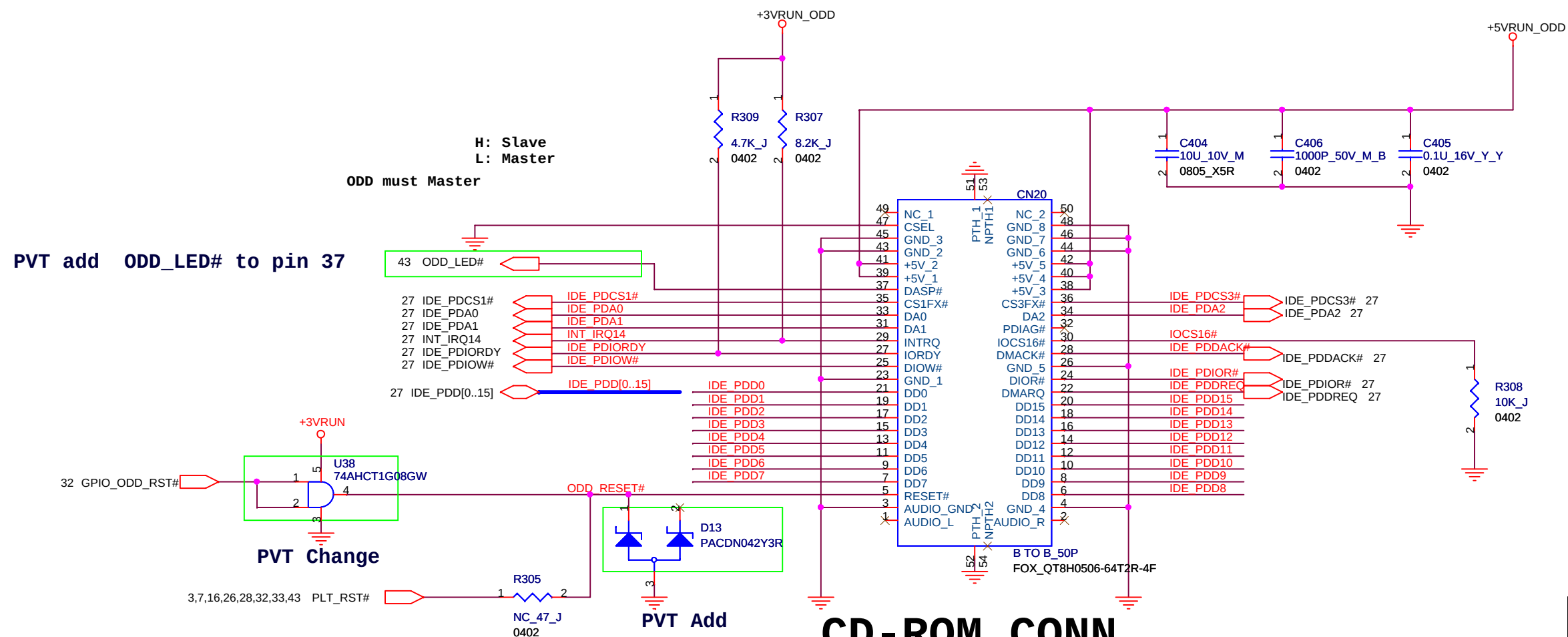
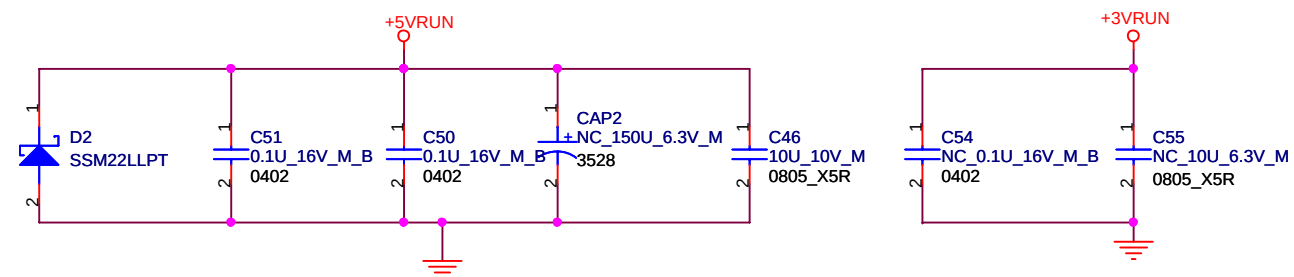
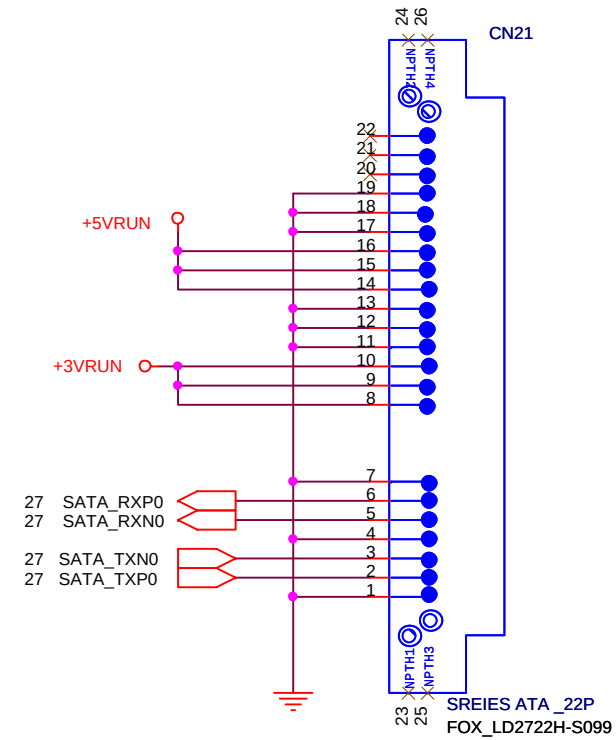








SATA HDD CONN



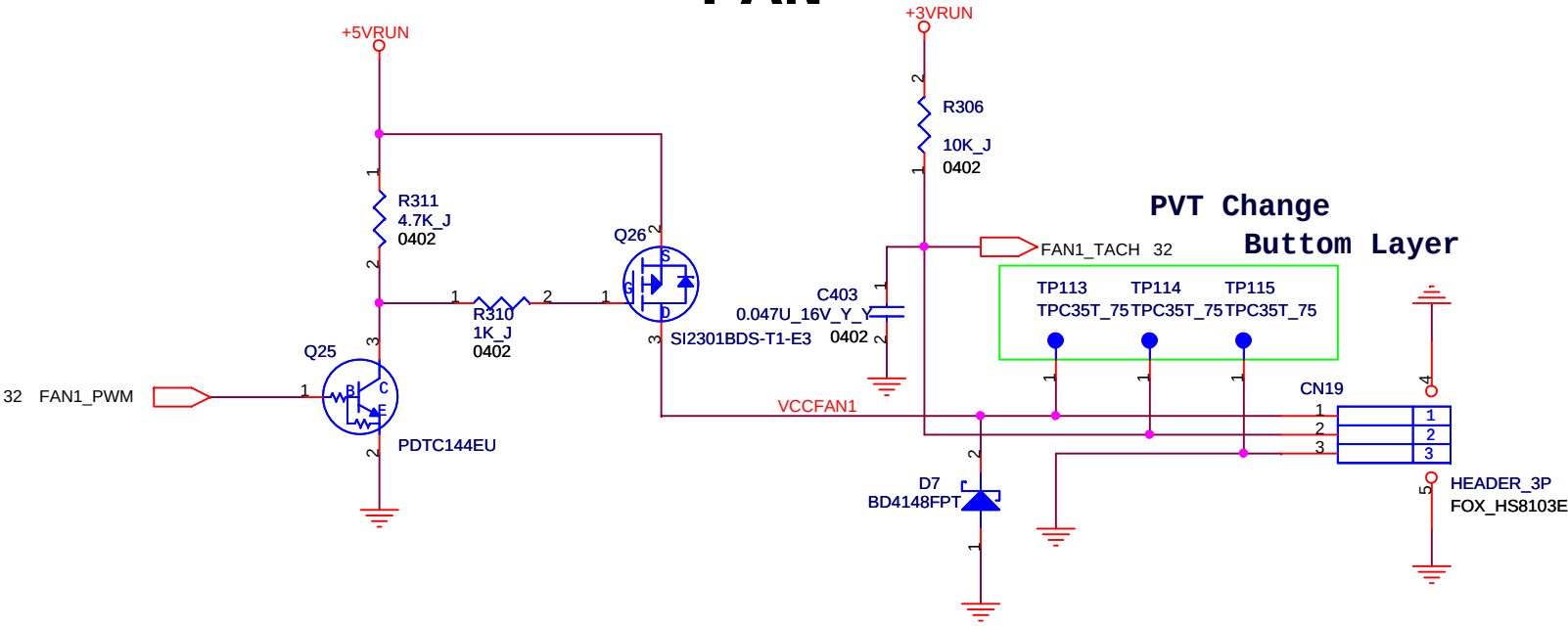
CD-ROM CONN

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
SATA HDD/CD-ROM			
Size	Document Number	Rev	
A3	MS60-1-01 (MBX-159)	0.30	
Date:	Wednesday, October 04, 2006	Sheet	31 of 56

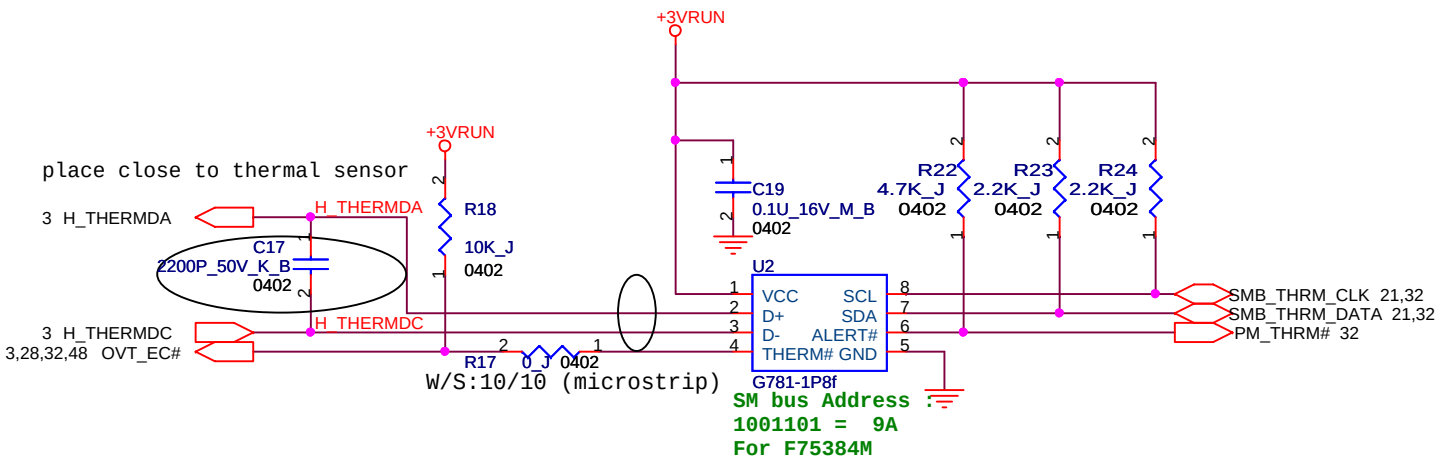
WWAN FOR MS60-L ONLY !!

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title		WWAN	
Size	Document Number		Rev
Custom	MS60-1-01 (MBX-159)		0.30
Date:	Wednesday, October 04, 2006		Sheet 34 of 56
		1	

FAN

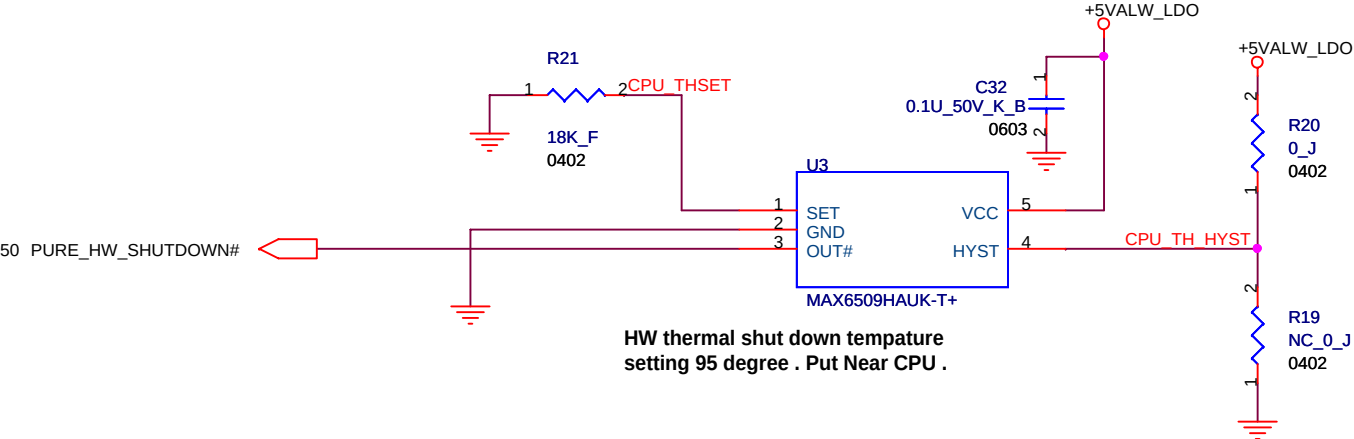


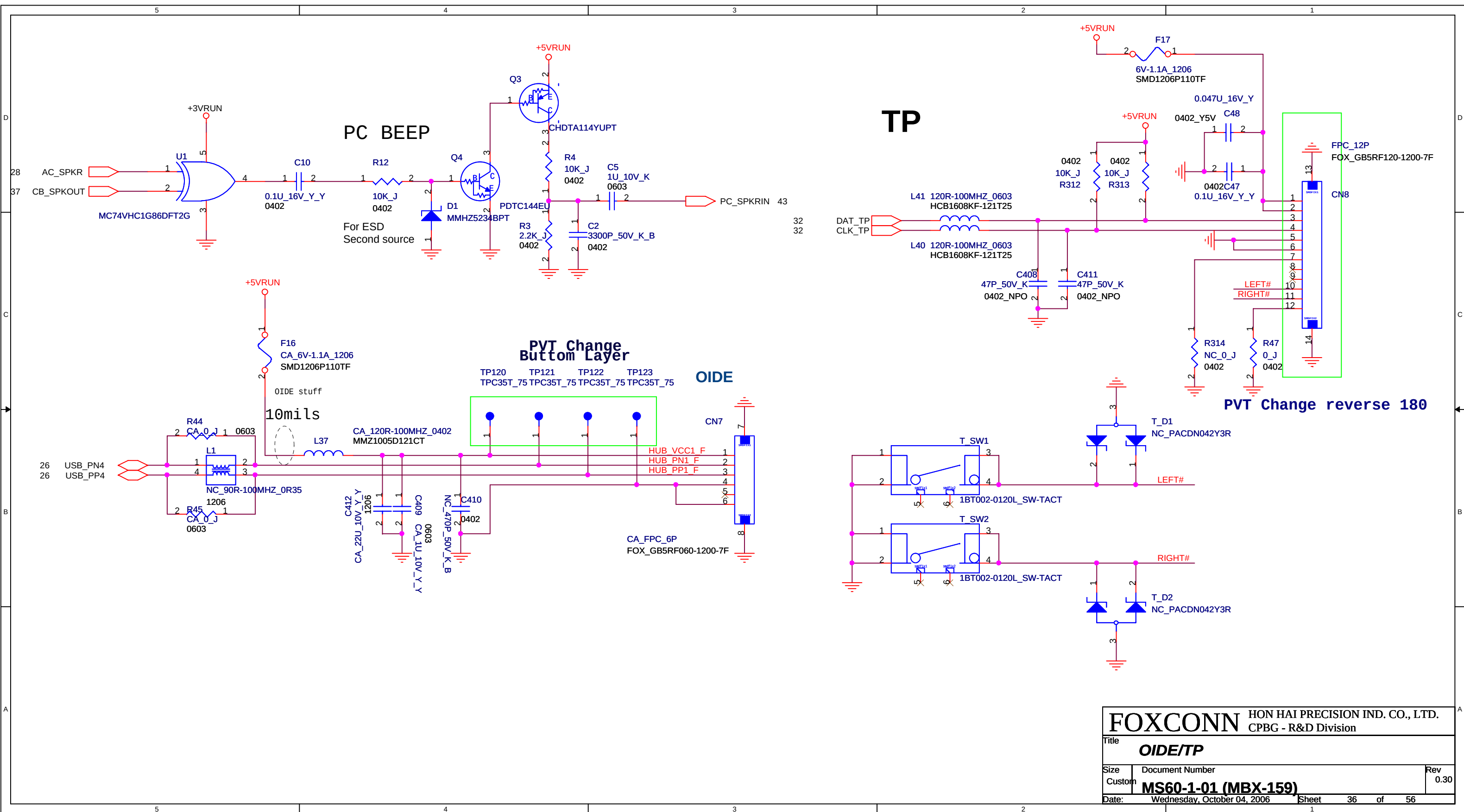
CPU SENSOR

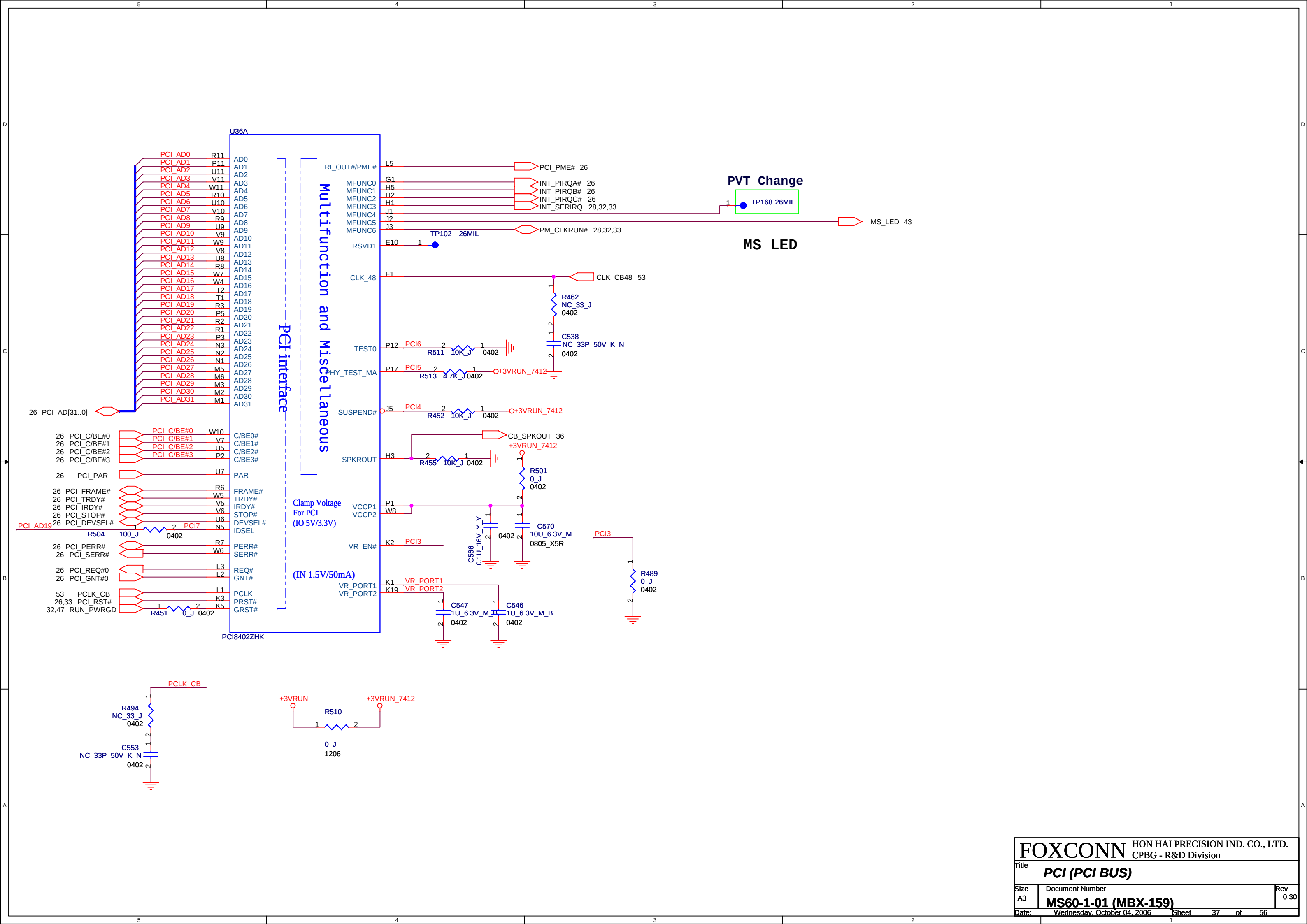


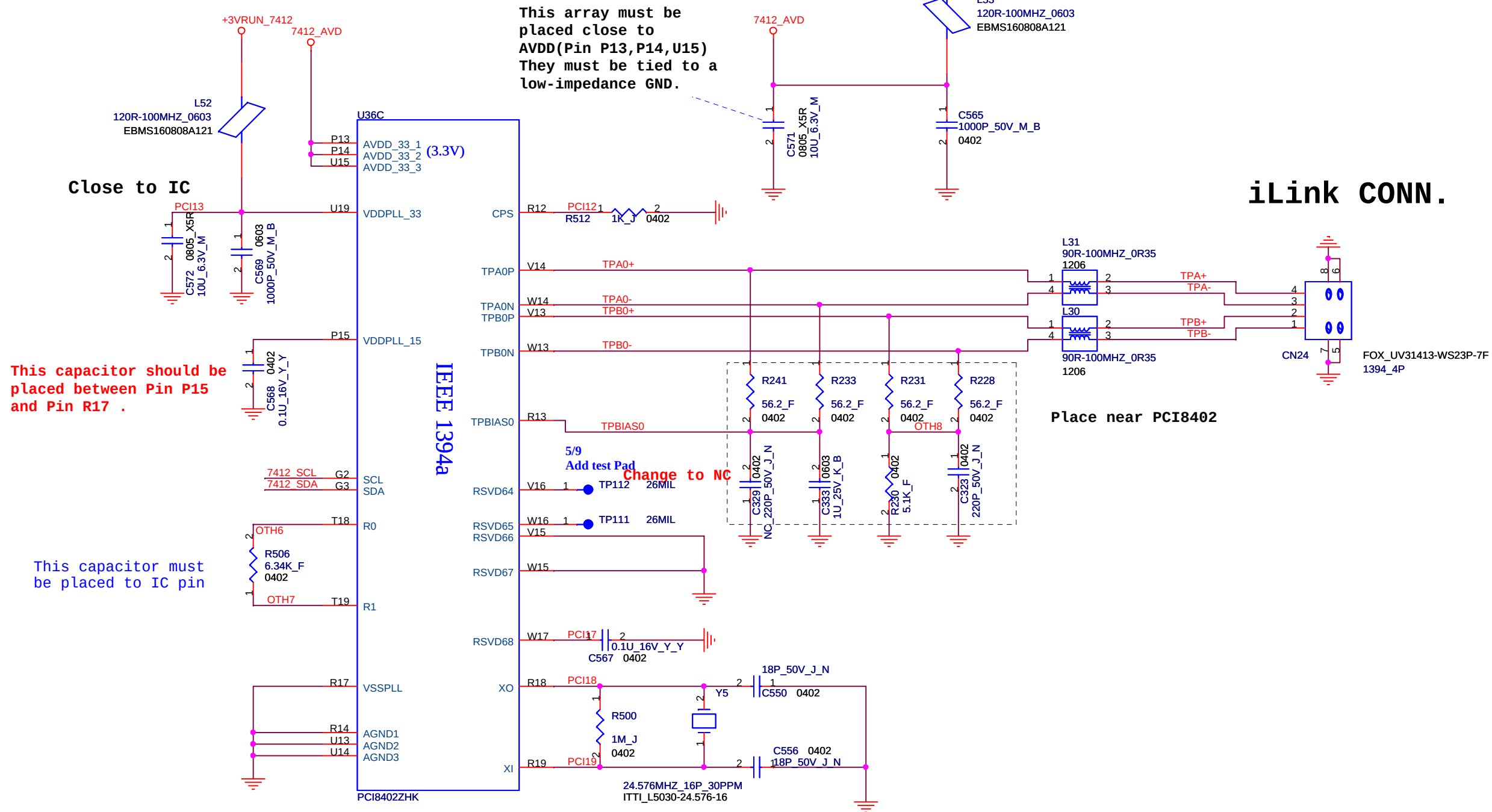
Place Thermal-Sensor near CPU & GMCH.

HW THERMAL PROTECTION









Close to IC

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

This array must be placed close to AVDD(Pin P13,P14,U15) They must be tied to a low-impedance GND.

IEEE 1394a

5/9 Add test Pad Change to NC

Place near PCI8402

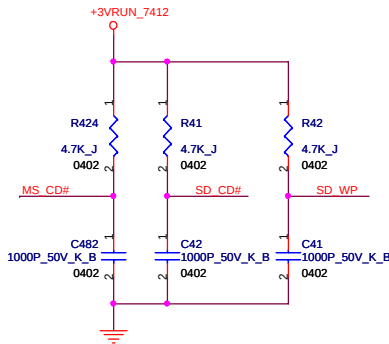
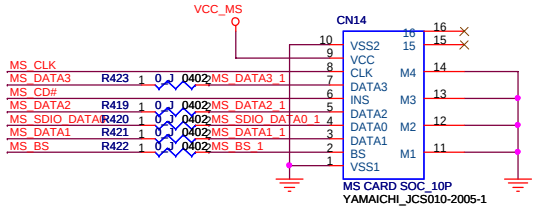
iLink CONN.

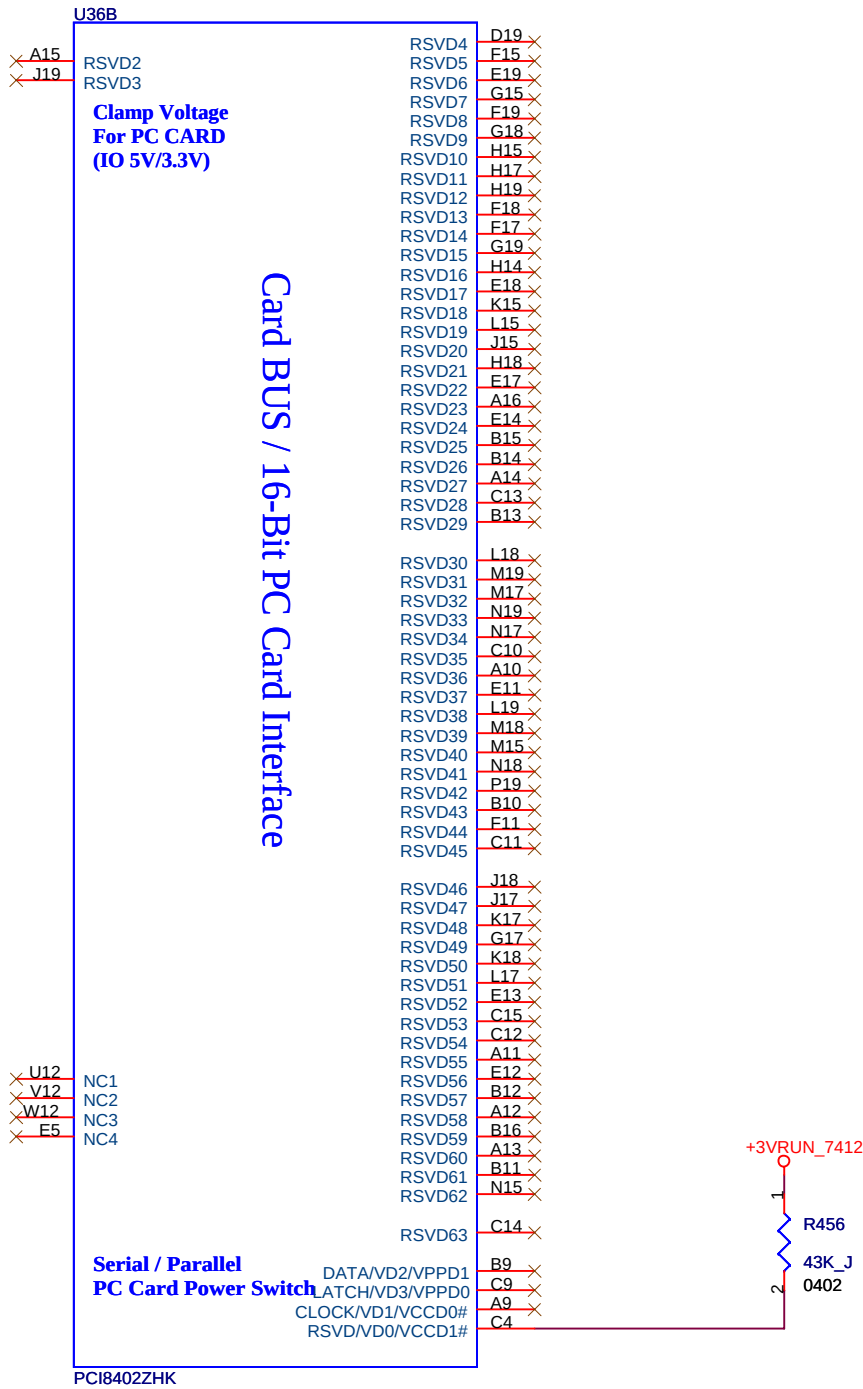
Resistors should be placed on the SCL and SDA terminals

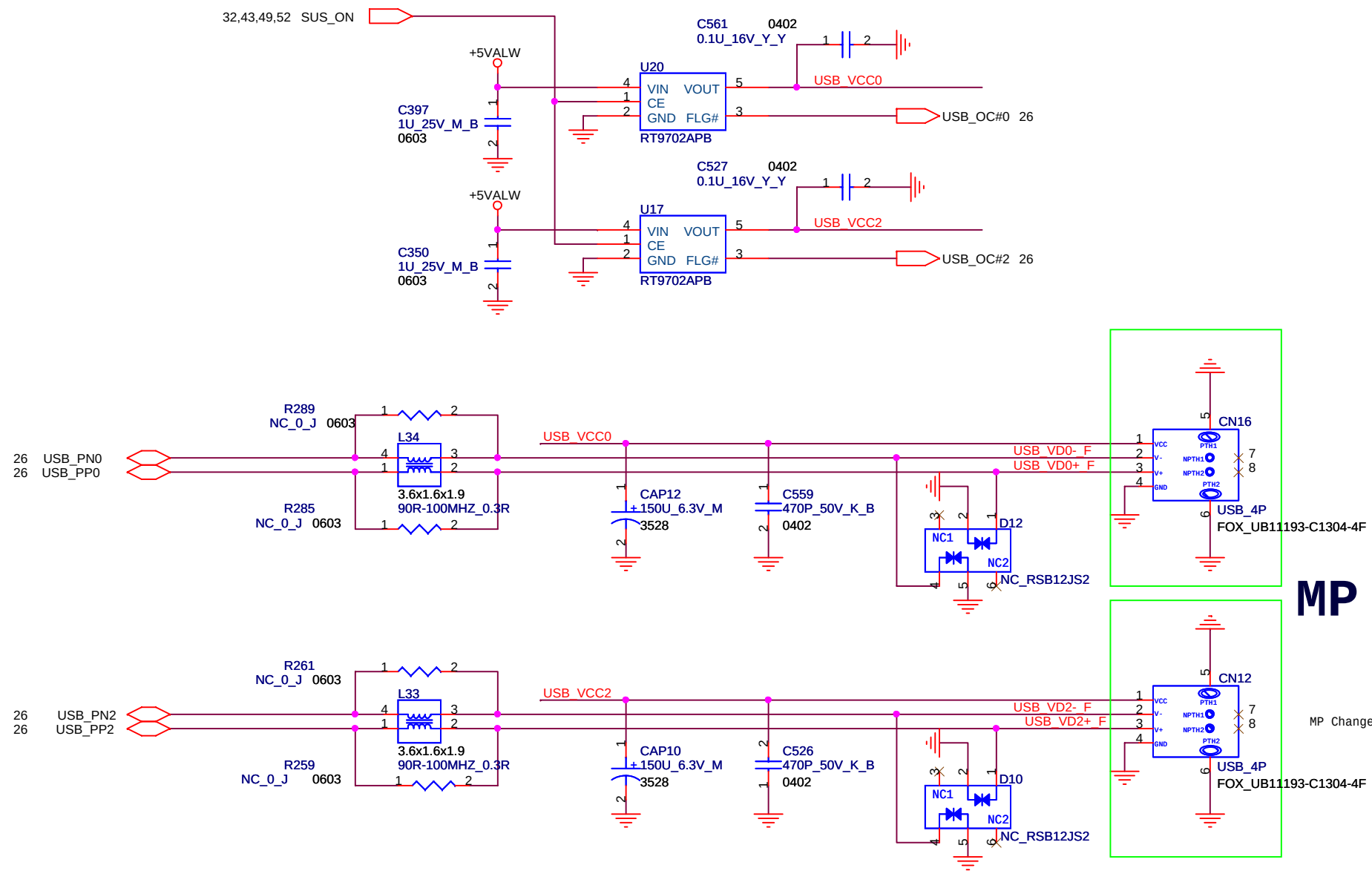
L: R/W
H: Read only



PVT Change to test point

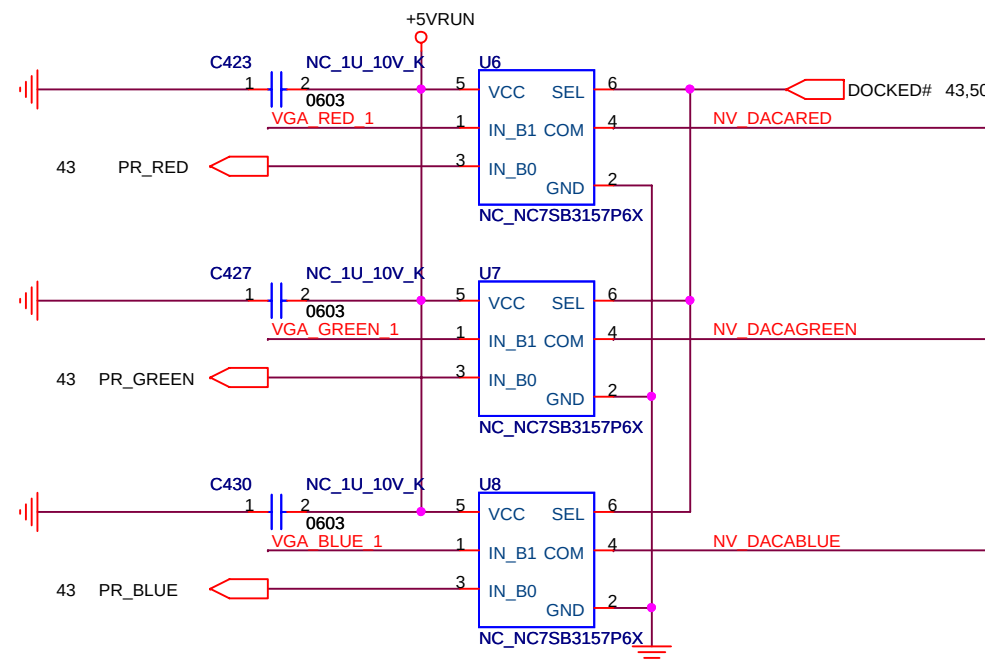
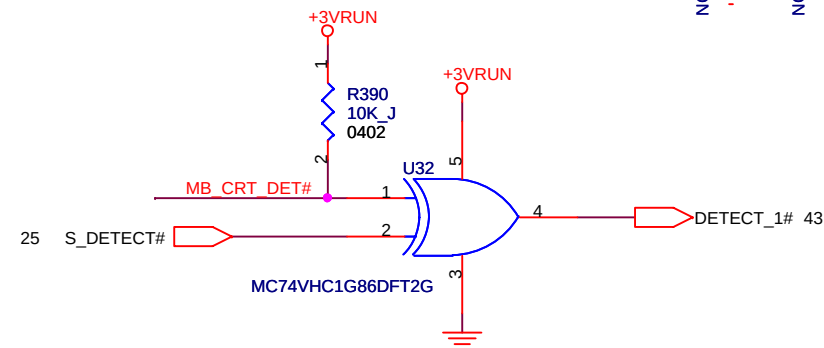
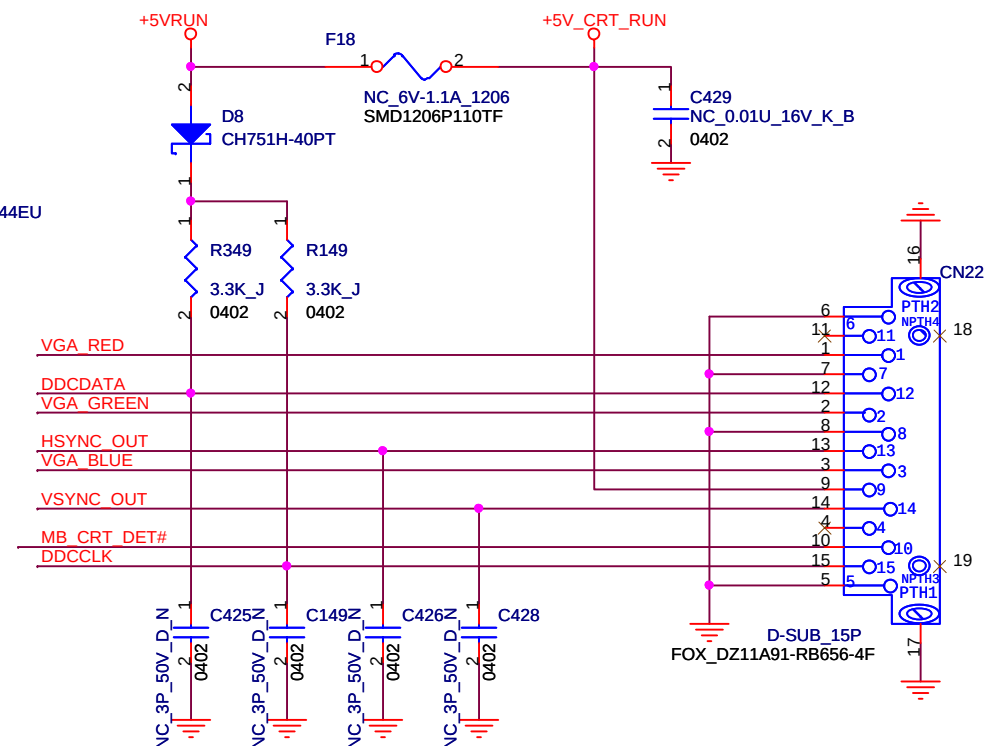
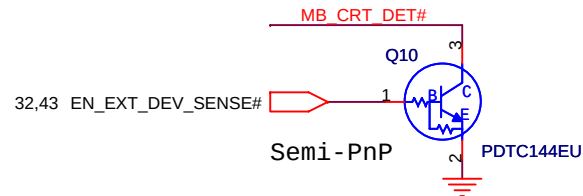


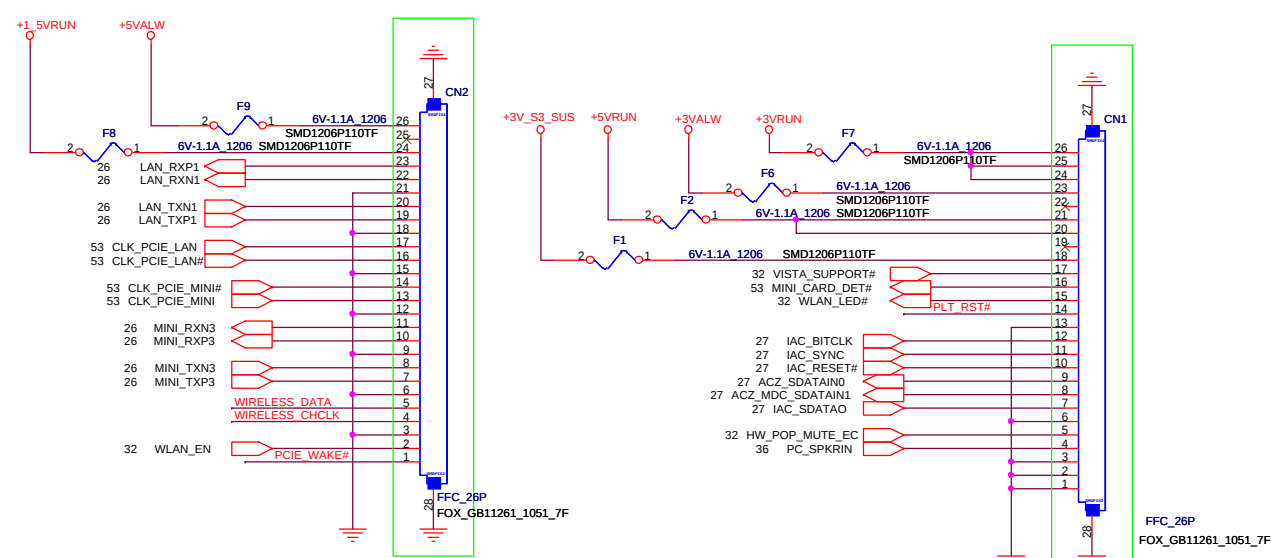
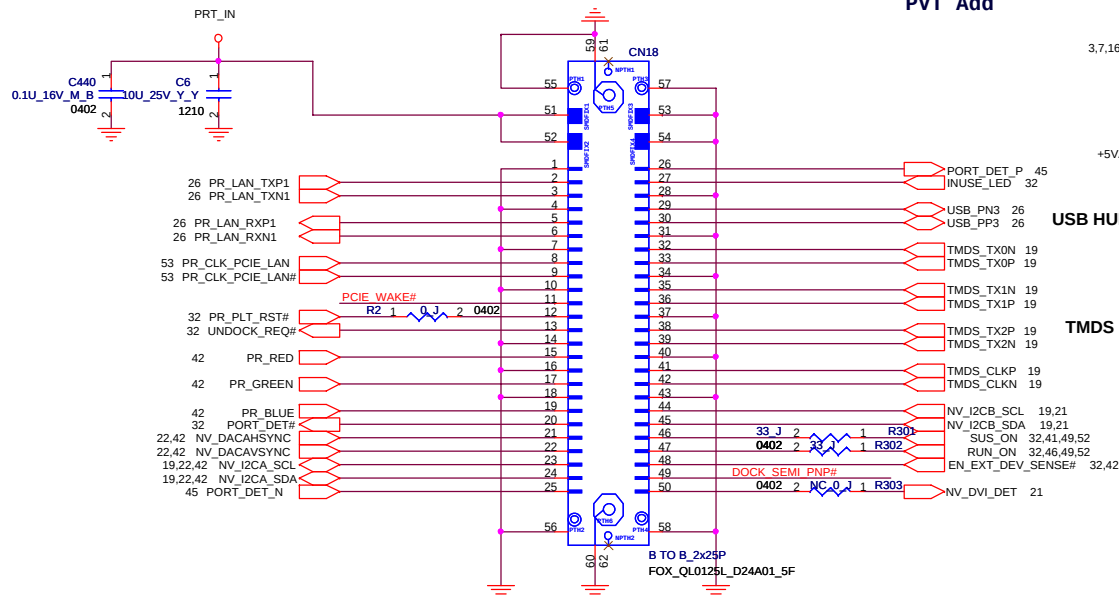
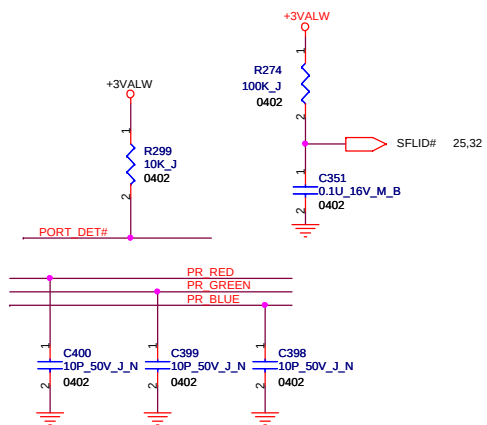
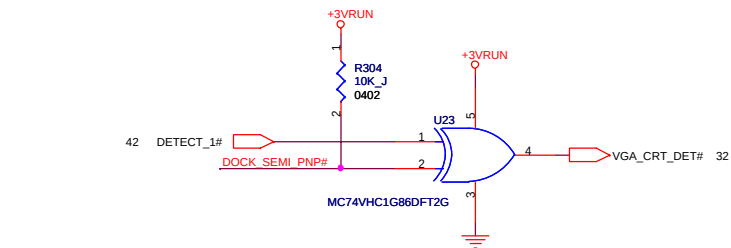
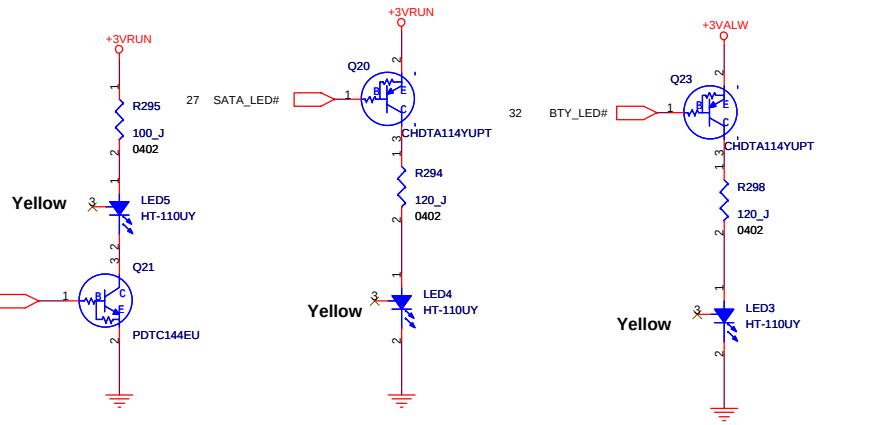
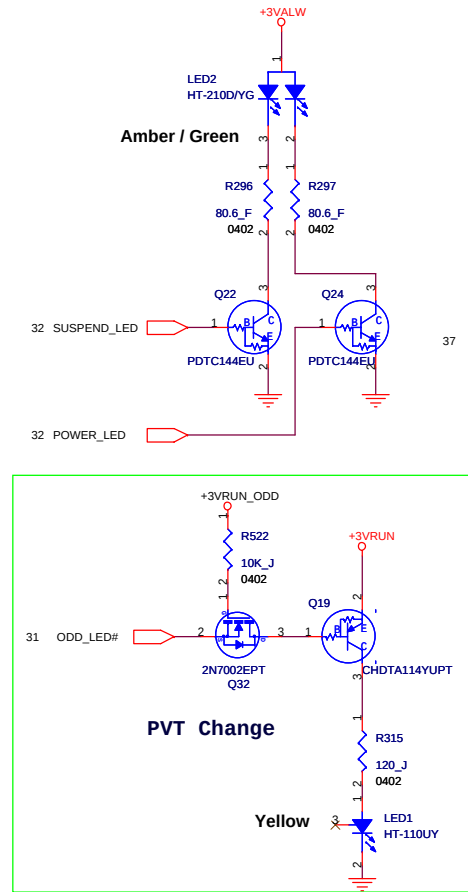




MP Change

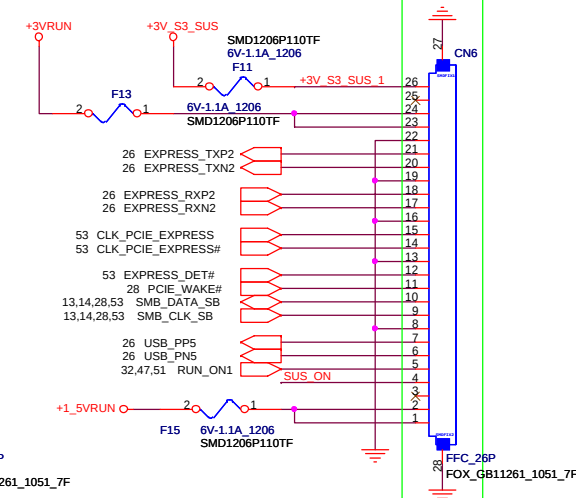
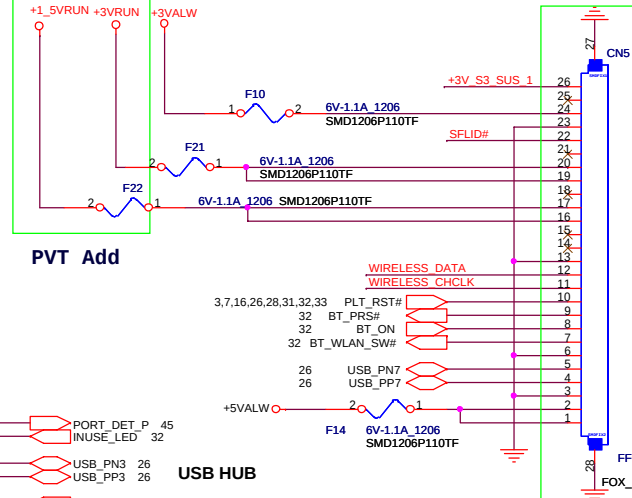
MP Change





PVT Change to GB11261_1051_7F

PVT Change to NC

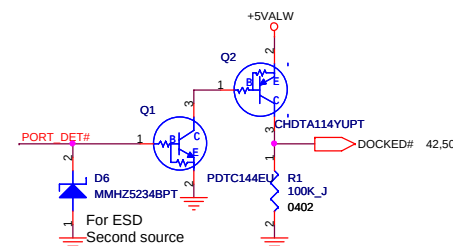


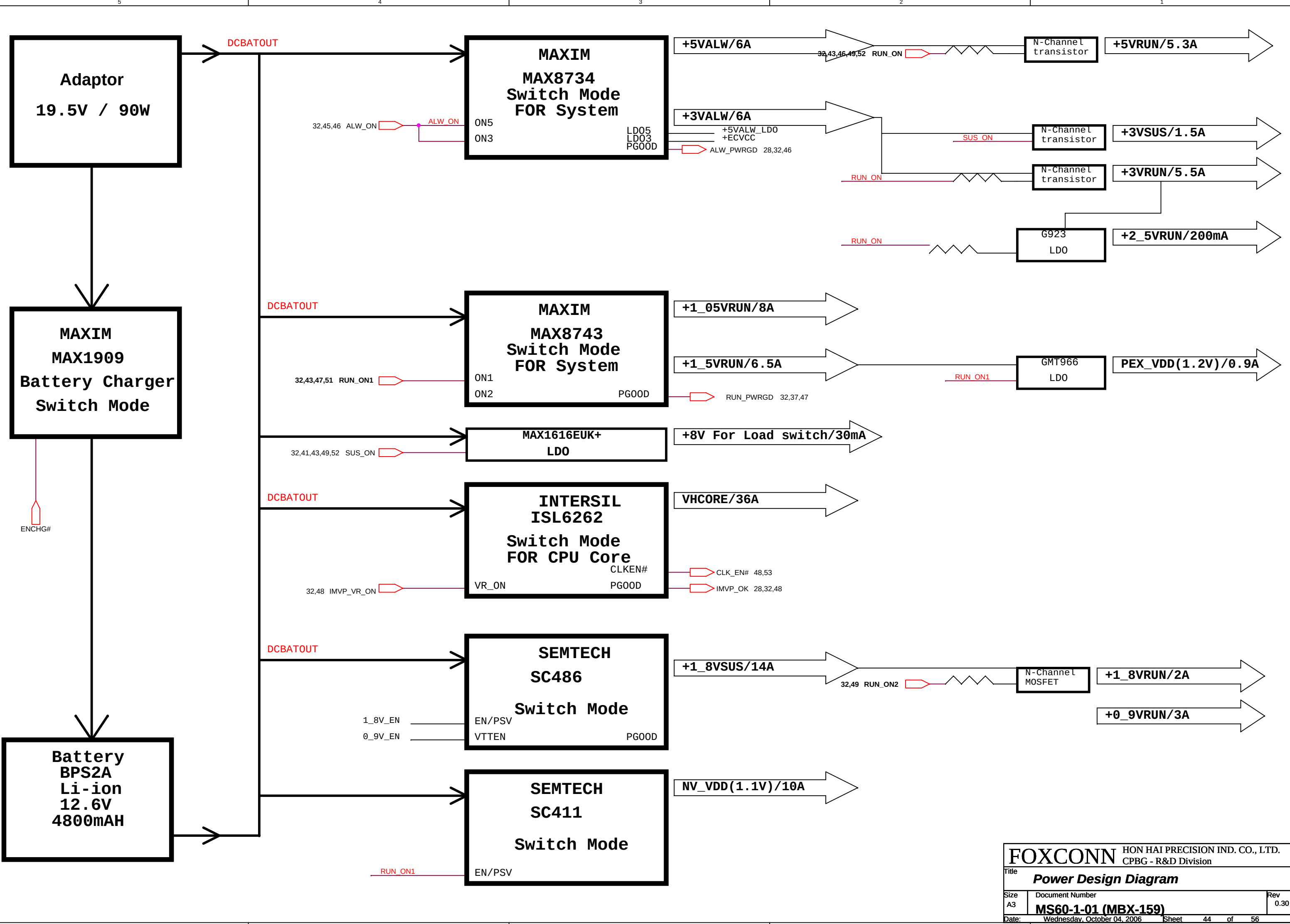
USB HUB

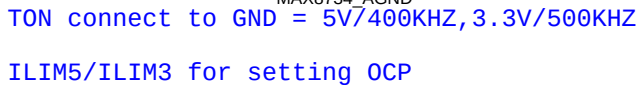
TMDS

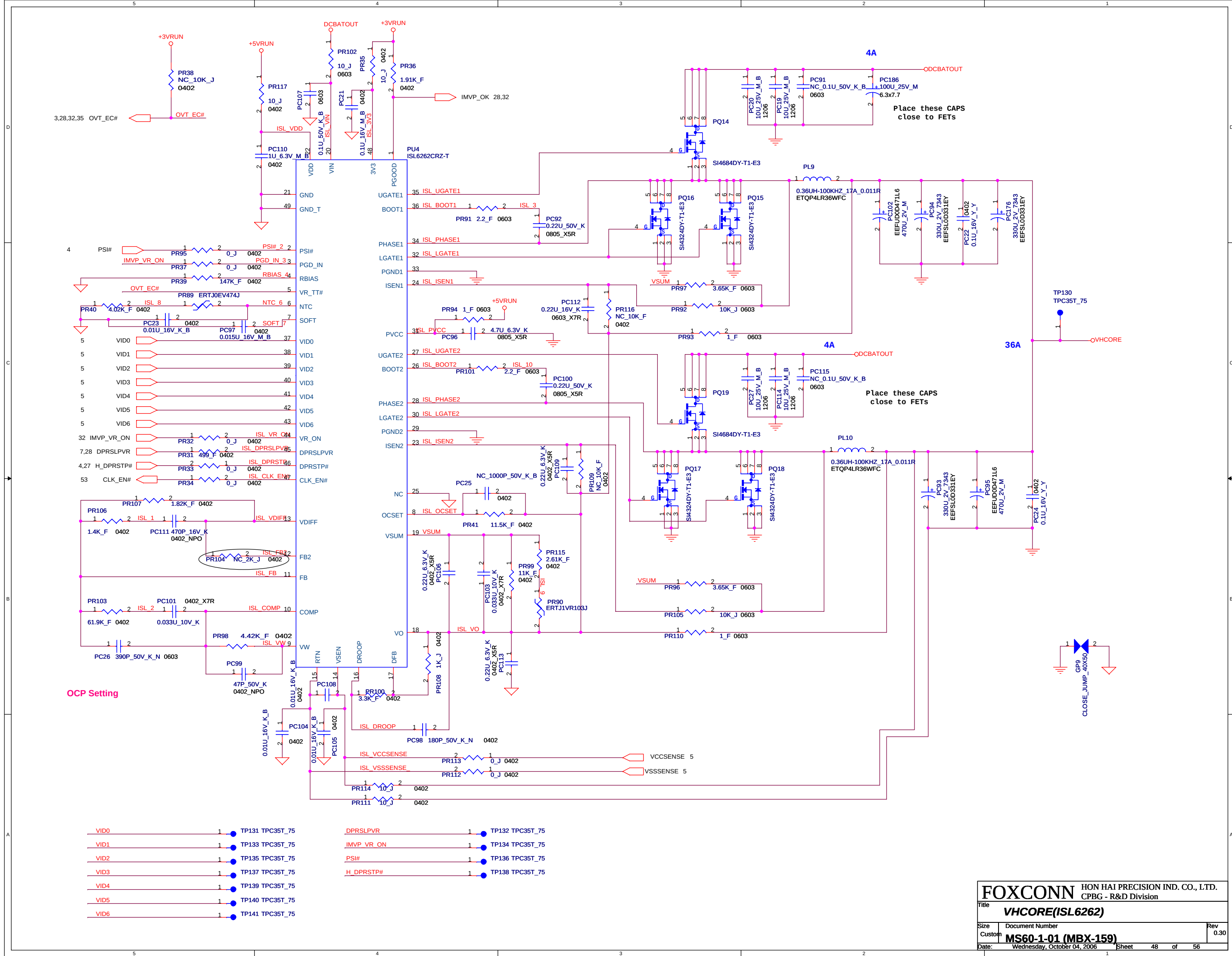
PVT Change to GB11261_1051_7F

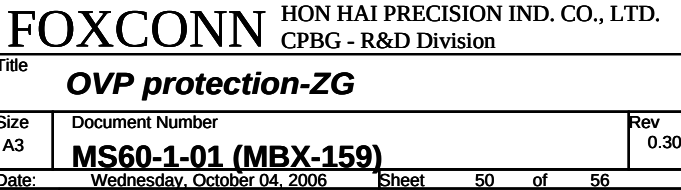
PVT Change to GB11261_1051_7F

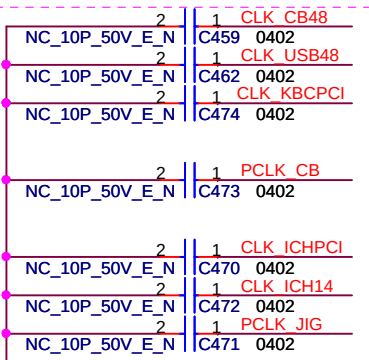






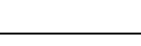
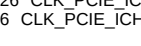
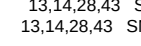
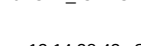
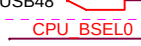
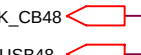
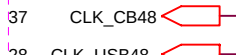






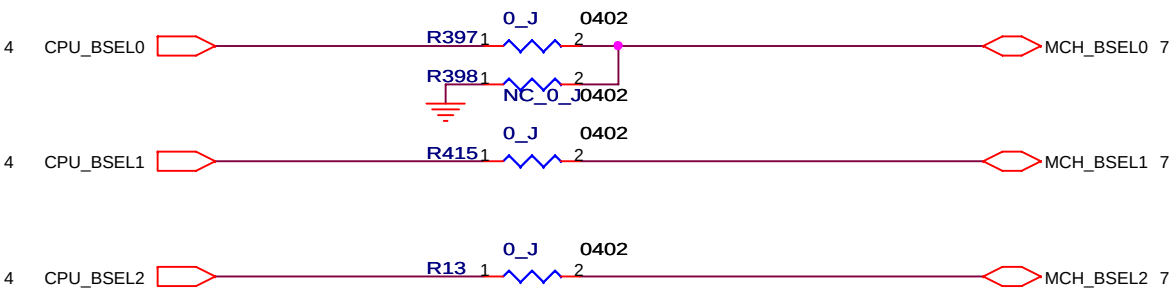
close to clk gen (For EMI)

Length as short as possible.



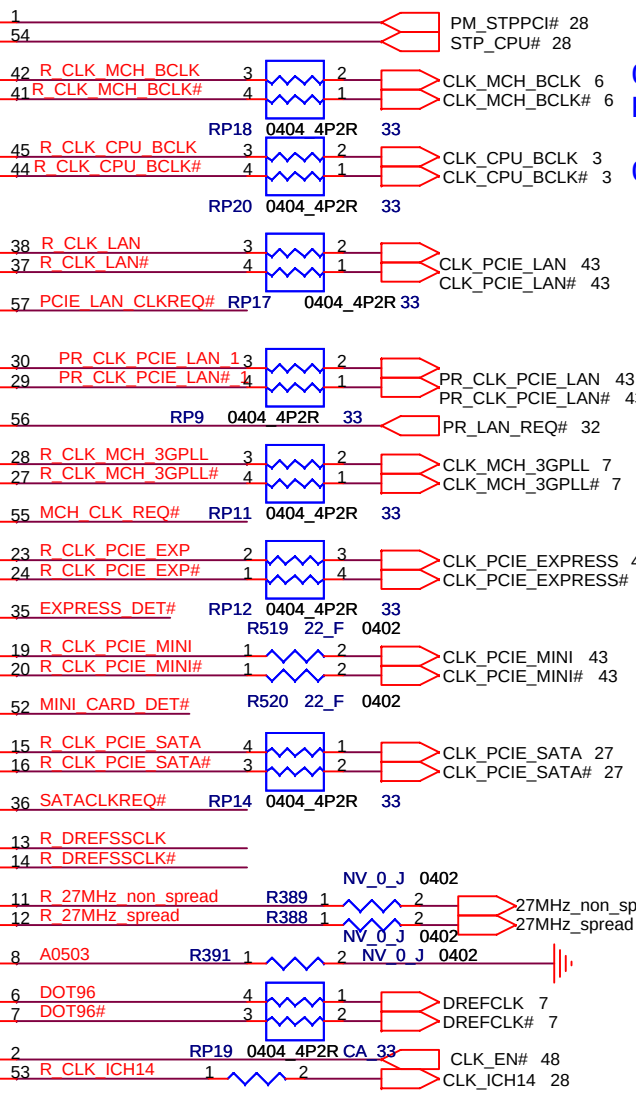
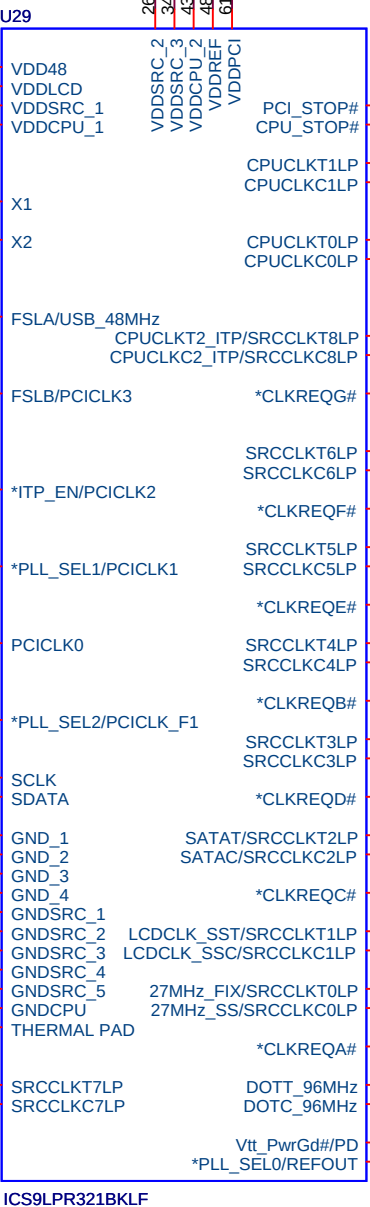
FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33



SM bus Address : 1101001 (ICH7)
For clock generator

CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
If EVT ok, del them in DVT



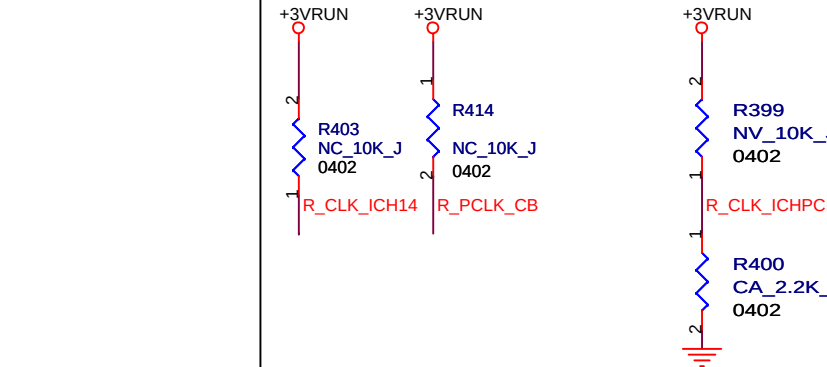
CALISTOGA chip HOST

CPU

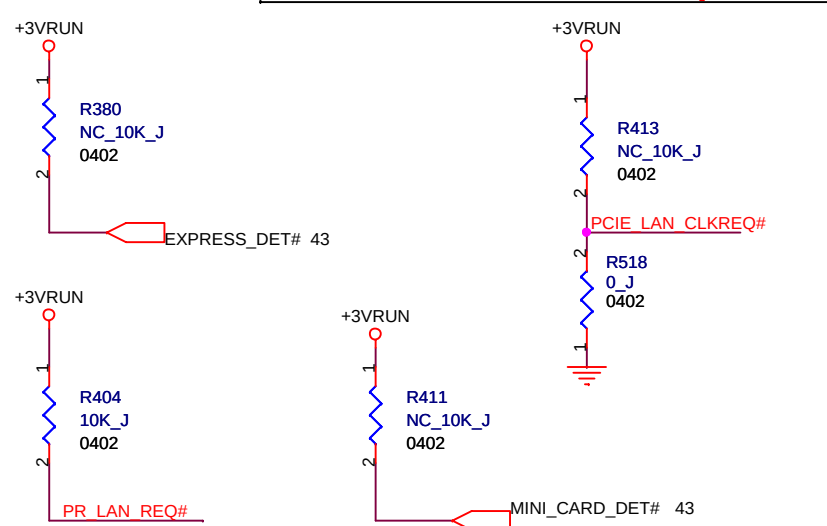
ICH7M SATA

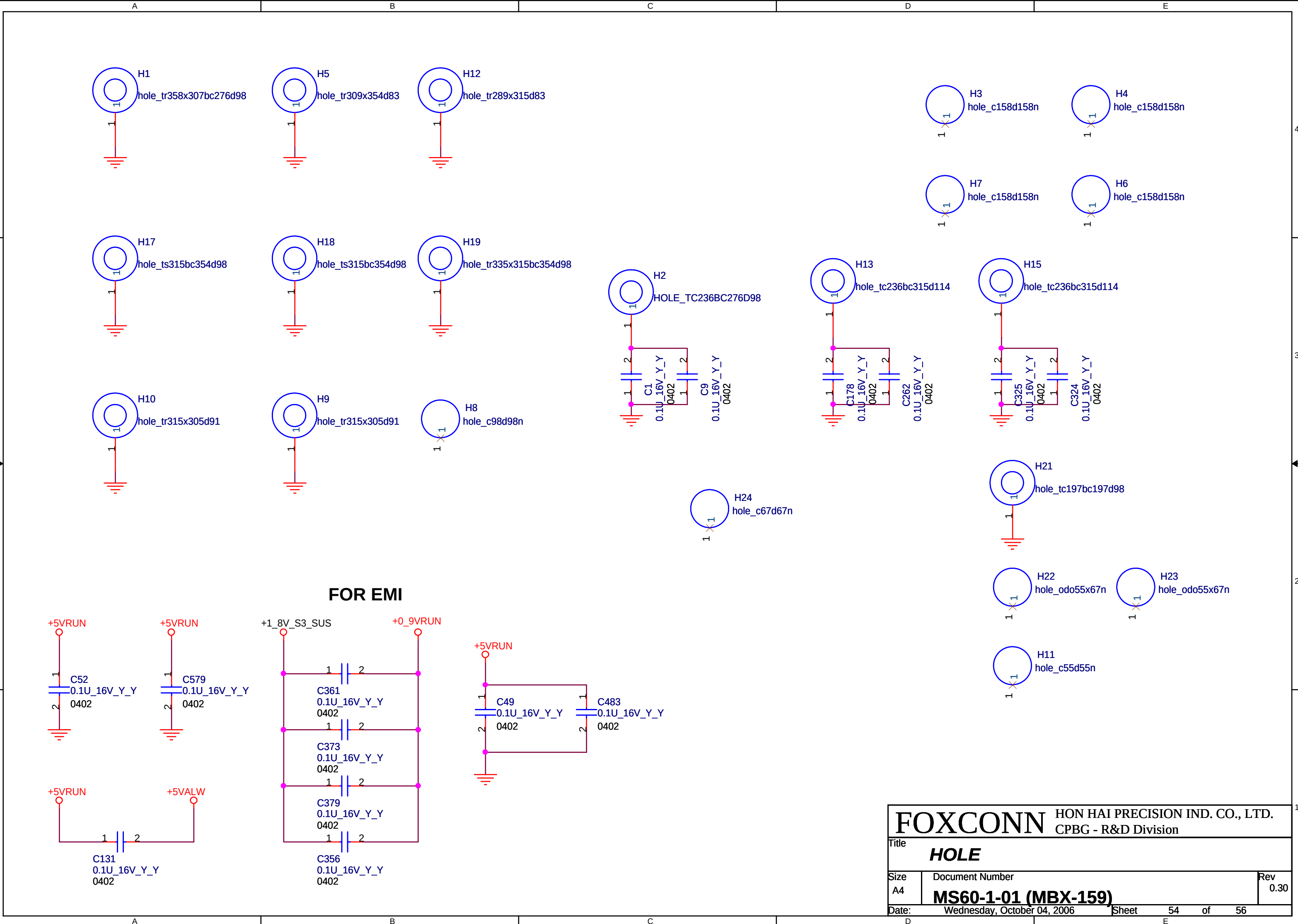
Nvidia Graphic

CALISTOGA DOT96



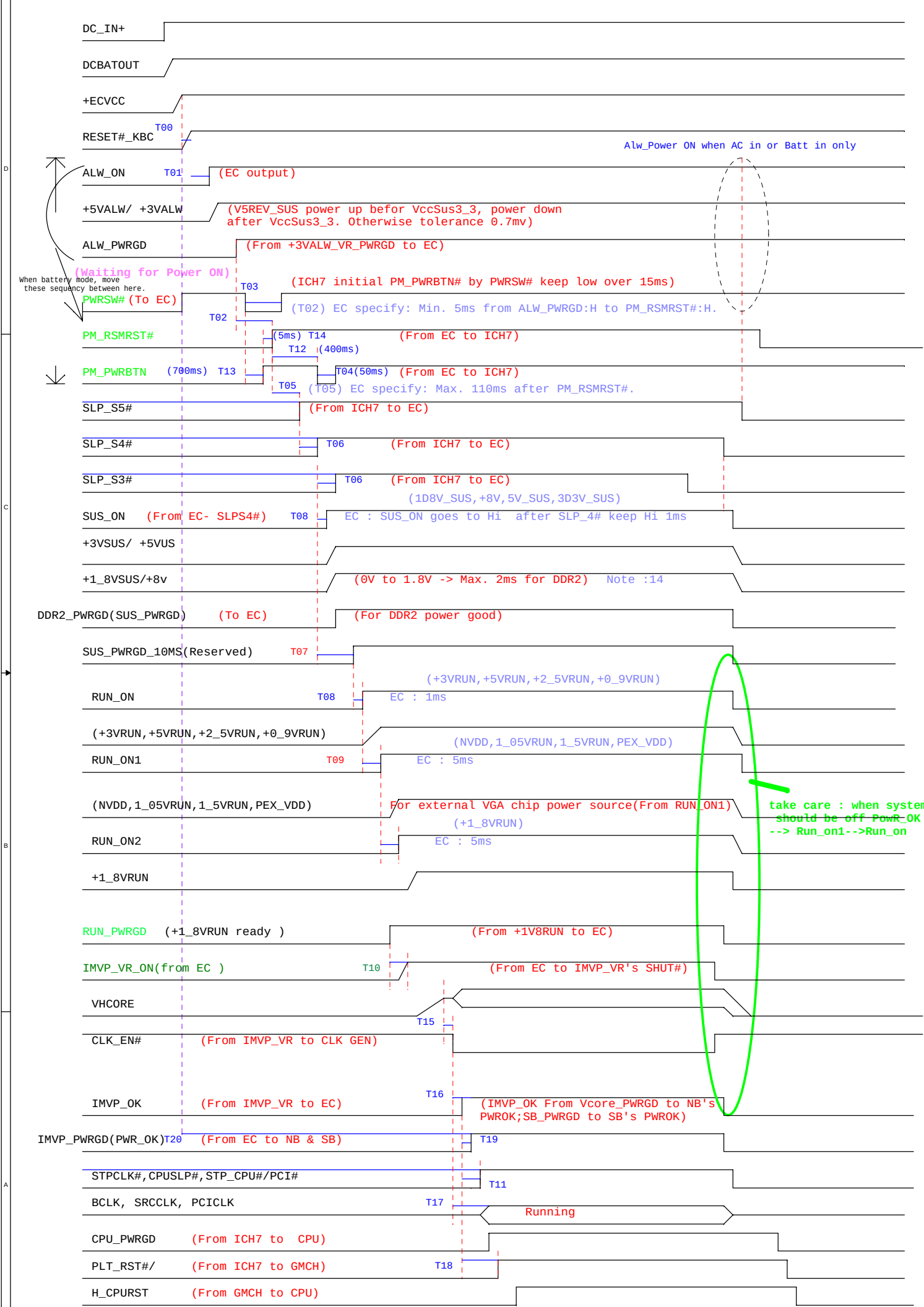
Pin Straps	
Pin 53/59/60/64 100K ohm pull-up	
pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)





MS60 Power On Sequerce Timing

Version : 0.0
Modified date : 2/14/2006

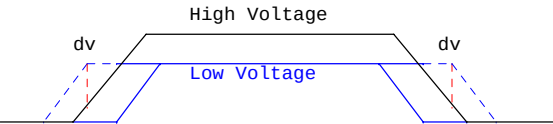


NOTE : (EC KB3910 Min. response time is 1ms)

- 1. T00 : R=47K, C = 0.1uF is ENE recomment value please refer to KB3910B0-AN4A-200
- 2. T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- 3. T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
- 4. T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- 5. T05 : RSMRST# active High to SLP_S5# avtive High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
- 6. T06(Please reference Intel 16971 Page 301 of t234 timing)
- 7. T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
- 8. T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- 9. T09 : For MS01 current SPEC
- 10.T10 :Please refer to Intel 16971 Page 300 of t214 timing
- 11.T11 :Please refer to Intel 16971 Page 303 of t216 timing
- 12.T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
- 13. T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- 14.T14 : For MS01 current SPEC Min. is 5 ms
- 15.DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- 16.IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
- 17.In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
- 18.T15 : Please refer to MAX8771 datasheet
- 20.T16: Please refer to MAX8771 datasheet
- 21.T17 : Please refer to Intel CK410(14690) page 53
- 22. T18 : The ICH7 drives PLTRST# active a mininum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- 23. CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- 24. T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- 1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- 2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- 3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- 4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
- 5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
- 6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- 7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV



R/C delay
(47K/
0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns~2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min :1s	

<1>-2006/3/28 Remove USB_SW no need to program for present application.	<21>-2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.	<46>-2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component : P9273 P/N : 1R-0000103-F200	<84>-2006/7/18 Change TP connector to reverse 180.	<140>-2006/9/04 Change R189 to 1R-0000103-F200.
<2>-2006/3/28 Change PR5 from 13K to common parts 10KOhm.	<22>-2006/4/4 D6,D7 D8 change to Q59 Q60 Q61 P/N : 1T-2N7002E-PT00	PR773 P/N : 1R-0004992-F200 PQ208 P/N : 1T-2N7002E-PT00	<85>-2006/7/18 add ODD_LED to pin37	<141>-2006/9/05 del TP1,T2,TP3,TP5,TP6,TP7,TP8,TP9
<3>-2006/3/28 Change USB CONN. CN16 & CN40 for ID requirement. P/N : FOX_USB1193-C1301-4F	<23>-2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate. P/N : 1R-0000121-J200	PR774 P/N : 1R-0000102-J200 PC873 P/N : 1C-2Y20105-Y000	<86>-2006/7/18 Remove SD signal for Jugar comment.	<142>-2006/9/05 del TP10,TP11,TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19
<4>-2006/3/29 Change ODD CONN. CN21 for ID requirement. P/N : FOXCONN_Q78H959_8472R_4F	<24>-2006/4/4 new add Q62 for WLAN LED Logic P/N : 1T-2N7002E-PT00	<47>-2006/4/10 add H21-H24.	<87>-2006/7/18 add RS21	<143>-2006/9/05 del TP20,TP21,TP22,TP23,TP25,TP26,TP27,TP28,TP29
<5>-2006/3/29 Change PC359,PC360 to 10uF P/N : 1C-2B70106-M100	<25>-2006/4/4 NC F1 and C859 according to customer's feedback.	<48>-2006/4/10 Rename Schematic Part retireme. new version since 411	<88>-2006/7/19 change PD1 from SM15.7C to PESD15V52UT_215(16-PESD15V-S200).	<145>-2006/9/06 Change PR136 to 1R-0007152-F200.
<6>-2006/3/29 update new HDD CONN CN24. P/N : 2N-9022002-F050	<26>-2006/4/4 delete R482,R483 according to customer's feedback.	<49>-2006/4/11 change R68,R133,R100 P/N : 1R-0000151-F200	<89>-2006/7/19 del one test point in P+ and P- (place on bottom side).	<146>-2006/9/09 add RS27 to 100K
<7>-2006/3/29 update new DC-IN CONN PCN1. P/N : FOX_CSS3620-00598-7F	<27>-2006/4/6 add H3 ~ H20	<50>-2006/4/11 PR111,PR114 change to NC according to PWR team's suggestion in EVT.	<90>-2006/7/19 add test points in net +ECVCC and +5VALW_LDO.	<147>-2006/9/09 add RS28 to 10K
<8>-2006/3/29 update new BTY CONN PCN2. P/N : FOXCONN_BP34963_86013_7F	<28>-2006/4/6 Update BTY Connector PCN2 for ME requirement. P/N : 2N-0006001-MKX0	<51>-2006/4/11 Modify ODD reset circuit as customer's feedback. Add U37 P/N : 1S-MA-X8095-0000 Add RS16 P/N : 1R-0000104-J200 NC R305	<91>-2006/7/19 remove P31,P32,P33,P34,P35,P36,P39	<148>-2006/9/11 Change R296,R297 to 1R-000806X-F200
<9>-2006/3/30 U18,U19,U21,R277,R300,R315change to NC according to Customer's feedback.	<29>-2006/4/6 R278,R289,R270 change to 75Ohm and circuit modified as customer's feedback. P/N : 1R-0000750-F200	<52>-2006/4/11 Remove C257 for EMI comment.	<92>-2006/7/20 add test points TP173,TP174 in net +5VRUN_ODD and +3VRUN_ODD.	<149>-2006/9/11 Change PC106,PC109,PC113 TO 1C-2B20224-K101
<10>-2006/3/30 R269,R271,R276,R286,R287,R300 change to Populate according to Customer's feedback.	<30>-2006/4/6 RS43 change to 75Ohm as customer's feedback. P/N : 1R-0000750-F300	<53>-2006/4/11 add ODD Reset RC. Add RS17 P/N : 1R-0000103-J200 Add C380 P/N : 1C-2Y20104-Y000	<93>-2006/7/25 add PD37 and PR203 for Power improvement.	<150>-2006/9/11 Change PC89 to 1C-2B30224-K000.
<11>-2006/3/30 New add INV_ENABLE_EC logic due to BIOS Code merge issue.add new component : US3,U54 P/N : 14-74AHCT1G-0800 R762 P/N : 1R-0000103-J200 R763 P/N : 1R-0000000-J200 R764 P/N : 1R-0000104-J200 Delete R176,R177	<31>-2006/4/6 R99,R94,R97,R109,R67,R64,R65,R75 change to NC as customer's feedback. and R66,R69,R98,R101 change to 120Ohm. P/N : 1R-0000121-J200	<54>-2006/4/14 change P197,R198,R199,R200 to 60.4Ohm P/N : 1R-0000604X-F200	<94>-2006/7/27 change PC89 to 1C-2B30224-M000.	
<12>-2006/3/31 Add C20,C21,C22,C31,C38 for EMI slution. P/N : 1C-2Y20104-Y000	<33>-2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.	<55>-2006/4/14 add RS18 for 0Ohm P/N : 1R-0000000-J200	<95>-2006/7/27 add C605 for NV_PWR_MIZER.	
<13>-2006/3/31 Add R5 for Customer feedback. P/N : 1R-0000000-J200	<34>-2006/4/6 CN31 Pin1,2 change to +3V_S3_SUS as customer's feedback.	<56>-2006/4/14 CN7,C49,C412,L37,F16,R44,R45 change to CA from NV to fit configuration.	<96>-2006/8/01 add C606 and C607 to 1C-2N20030-D000.	
<14>-2006/3/31 Dummy R482,R483 for Customer feedback.	<35>-2006/4/6 add 1A Fuse F4,F5,F9,F11,F15,F17,F18,F19 P/N : 1M-F32V1A0-F000	<57>-2006/4/27 PR111,PR114 change to Populate from NC according to PWR team's suggestion in EVT. P/N : 1R-0000100-J200	<97>-2006/8/01 change R263 and R265 to 1R-0000222-J200.	
<15>-2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component : US5,US6 P/N : 1S-RT9702A-0000 CS21,CS22 P/N : 1C-2Y20104-Y000 R569,R573 P/N : 1R-0000105-J200 C870,C871 P/N : 1C-2Y20225-Y000 CS35,C751 P/N : 1C-2B70106-M100 Deleted Component : Q162,Q193,Q200,Q201,CS35,CS27,CS21,C753,C752,R486,R476,R568,R569	<36>-2006/4/6 add 0.5A Fuse F2,F3,F6,F7,F8,F10,F12,F13,F14,F16,F18 P/N : 1M-F32V0A5-F000	<58>-2006/5/24 PWR/SUS LED control signal swap to fit the correct definition.	<98>-2006/8/01 add PCB and PC7 to 1C-2N20030-D000.	
<16>-2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.	<37>-2006/4/6 add C872 according to MS20 lesson learn. P/N : 1C-2B20102-M000	<59>-2006/5/24 DC_IN connector connection swap to fit the correct definition.	<99>-2006/8/01 add D13 to 16-PACDM04-2Y00 for ESD protector.	
<17>-2006/4/3 CN20,CN32,CN33 Pin assignment modified due to Customer's concern.	<38>-2006/4/6 CN34 Pin23,24 change to +3VRUN.	<60>-2006/5/24 WWAN Connector remark with "CA".	<100>-2006/8/01 add PC186 to 1C-10X0107-M403 for PWR.	
<18>-2006/4/3 CN31,CN32,CN33 CN34 Connector change. P/N : GB11261_1051_7F	<39>-2006/4/6 add C71,C74,C87 for EMI. P/N : 1C-2Y20104-Y000	<61>-2006/5/24 add more 12pcs 10uF capacitor for CPU usage reseving. P/N : 1C-2B70226-M100	<101>-2006/8/01 Change PC186 P/N:1C-10X0107-M403 to 1C-1XX0107-M400 for PWR.	
<19>-2006/4/3 L17 & L19 updated according to Customer feedback P/N : 1L-DCS0603-1000	<40>-2006/4/6 add C89,C188,C199,C208,C213,C214 P/N : 1C-2Y20104-Y000	<62>-2006/5/24 R47 change to populate for TTP rotation.	<102>-2006/8/02 Change R189 to 1R-0000102-J200.	
<20>-2006/4/4 Add PWR_MIZER circuit. UG2 GPCD10 with new signal "TV_PWR_MIZER" new Components added and modified as below : 10K Ohm ~ R130,R766 ~ P/N : 1R-0000103-J200 7.5K Ohm ~ R765,R767,R768,R769,R770 ~ P/N : 1R-0000752-F200 4.3K Ohm ~ R128 ~ P/N : 1R-0000432-F200 2N7002EPT ~ Q54,Q55,Q56,Q57,Q58 ~ P/N : 1T-2N7002E-PT00	<41>-2006/4/7 R118,R119,R361 change to populate as customer's feedback.	<63>-2006/5/24 L21,L23 change to 1L-DWL10-C100 from 1L-DCS0603.	<103>-2006/8/03 remove R425.	
	<42>-2006/4/7 Y1,C104,C107,C492,C497,C501,R433,R434,R427,R428,R429,R430,R132, R133,R134,R136,R117 change to NC as customer's feedback.	<64>-2006/5/24 add new GPIO07 VISTA SUPPORT for Audio mute concern as customer's comment.	<104>-2006/8/03 add D14 to 16-HCS2053-OP00.	
	<43>-2006/4/7 R439,R440 change to 0 Ohm as customer's feedback. P/N : 1R-0000000-J200	<65>-2006/6/1 change both USB connector according to ME requirement. P/N : 1N-0004000-FEG0	<105>-2006/8/03 add GP14 to OPEN_JUMP_40X58.	
	<44>-2006/4/7 update Net name EN_EXT_SENSER as customer's feedback.	<66>-2006/6/1 change both INV connector according to ME requirement. P/N : 1N-0006001-M1T0	<106>-2006/8/03 Change US,U10,U11,U22,U28,U38 to 14-74AHCT1-G000.	
	<45>-2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component : PQ183 P/N : 1T-2N70020-M000 PR115 P/N : 1R-0000101-J200 PR103,PR114 P/N : 1R-0000104-F100 PC87 P/N : 1C-2B20103-M000 Q238 P/N : 1T-S14800B-QY00 PC76 P/N : 1C-2B70106-M000	<67>-2006/6/1 change TP connector according to ME requirement. P/N : 1N-0012001-F0T0	<107>-2006/8/03 Change H2 to HOLE000-0282.	
		<68>-2006/6/1 change ODE connector according to ME requirement. P/N : 1N-0006000-F0T0	<108>-2006/8/03 add H24.	
		<69>-2006/6/1 change ODE connector according to ME requirement. P/N : 1N-0006000-F0T0	<109>-2006/8/04 add RS22 to 1R-0000103-J200.	
		<70>-2006/6/2 Delete GPIO08 and GPIO18 CN3 Pin1 for WWAN removing.	<110>-2006/8/04 add Q32 to 1T-2N7002E-PT00.	
		<71>-2006/6/2 Delete H14 & H16 for WWAN removing.	<111>-2006/8/04 Change CN1,CN2,CN5,CN6 to GB11261_1051_7F.	
		<72>-2006/6/2 Delete R264,R271 for Debug BD LED.	<112>-2006/8/07 add CN1,Pin3 to 3VRUN.	
		<73>-2006/6/5 Delete RST_IC circuit and replace with PLT_RST#.	<113>-2006/8/07 add Q33.	
		<74>-2006/6/5 Delete all GM VGA related circuit in Page81,1025&42.	<114>-2006/8/07 Change Battery Conn Vender Pin to BP34067-86012-7F.	
		<75>-2006/6/8 change PORT_DET# from EC Pin81 to Pin176 for Noise decreasing.	<115>-2006/8/08 Change R433 to 330.	
		<76>-2006/6/9 PC127 change to Populate to improve VGA power feedback.	<116>-2006/8/08 add CN5 Pin26 to +3V_S3_SUS.	
		<77>-2006/6/9 add +3VRUN_ODD for ODD connector.also new power plane control for this.	<117>-2006/8/08 add CN5 Pin19,20 to 3VRUN.	
		<78>-2006/6/9 add R323 & C185 for VGA improvement.	<118>-2006/8/08 add CN5 Pin16,17 to 1SVRUN.	
		<79>-2006/6/9 add R238 1K ohm for customer's comment. P/N : 1R-0000102-J200	<119>-2006/8/08 Change R98 to 19.1K.	
		<80>-2006/6/13 remove RP13 and replace with RS19RS20 for WLAN issue improving. P/N : 1R-0000220-F200	<120>-2006/8/08 Change PR181 to 100K.	
		<81>-2006/6/15 reserve R264,R271 for VRAM. P/N : 1R-0000000-J200	<121>-2006/8/08 Change PR183 to 127K.	
		<82>-2006/6/15 Change PQ32 for VGA Power modification. P/N : 1T-S17114D-H700	<122>-2006/8/08 add F20,F21,F22 to 1M-F06V1A1-F000.	
		<83>-2006/6/15 Change USB connector footprint to FOX_USB11193_C1301_4F, but actually will populate with BOM Connector that is FOX_USB11193_C1304_4F	<123>-2006/8/08 del F20	
			<124>-2006/8/08 add RS23.	
			<125>-2006/8/08 Would R303 NC,DVI Hot Plug Detect# is implemented by not Gfx but EC as usual.	
			<126>-2006/8/08 Change R98 to 22.1K.	
			<127>-2006/8/11 Change PR15 to 1R-0000203-F100.	
			<128>-2006/8/11 Change RR183 to 1R-0002153-F200.	
			<129>-2006/9/04 add D15,D16 to 16-SCS500V-4000.	
			<130>-2006/9/04 add Q34 to 1T-PMV65XP-0000	
			<131>-2006/9/04 add Q35 to 1T-POTC144-EL00	
			<132>-2006/9/04 add RS24 to 1R-0004773-J200	
			<133>-2006/9/04 add RS25 to 1R-0000102-J200.	
			<134>-2006/9/04 add F23 to 1M-F06A35-F000	
			<135>-2006/9/04 add U39 to 1S-TPS2055-0000.	
			<136>-2006/9/04 add U40 to 1S-MAX4798-0000.	
			<137>-2006/9/04 add RS26,RS27 to 1R-0000103-J200.	
			<138>-2006/9/04 del RS21,U34.	
			<139>-2006/9/04 Change CN12,CN16 to 1N-0004000-FEG0.	