

MODEL NAME : *QBLB0*
PCB NO : *LA-8381P*
BOM P/N : *4319H631L01 (Samsung 1G)*
4319H631L02(Samsung 2G)
4319H631L03(Hynix 1G)
4319H631L04(Hynix 2G)

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Schematic Document

Specter MLK (Chief River)

Ivy Bridge (PGA) + Panther Point (standard)

DISCRETE VGA N13P-GT (optimus)

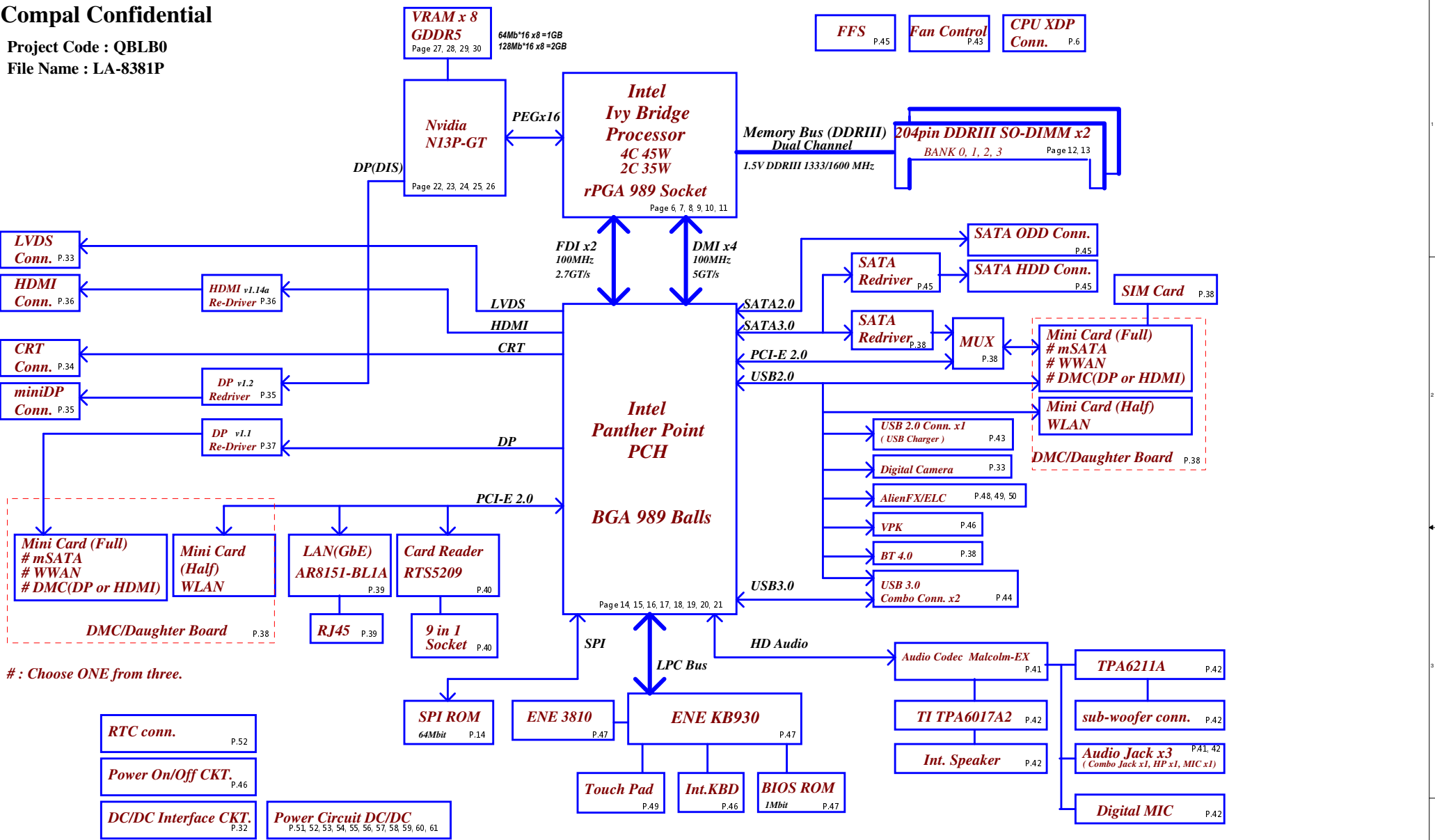
2011-10-26

Rev: X01

Highlight the short pad for 0 ohm

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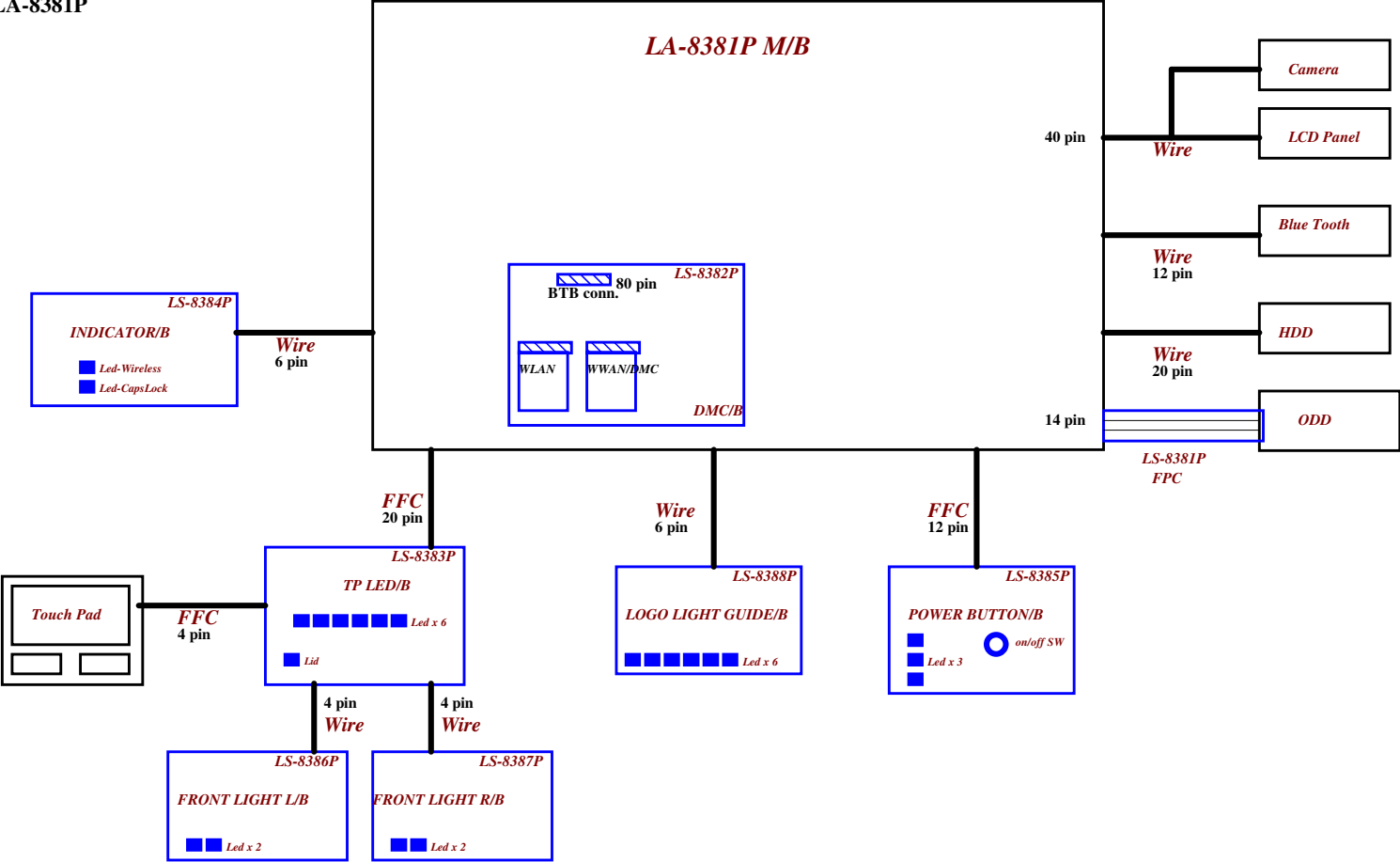
Project Code : QBLB0
File Name : LA-8381P

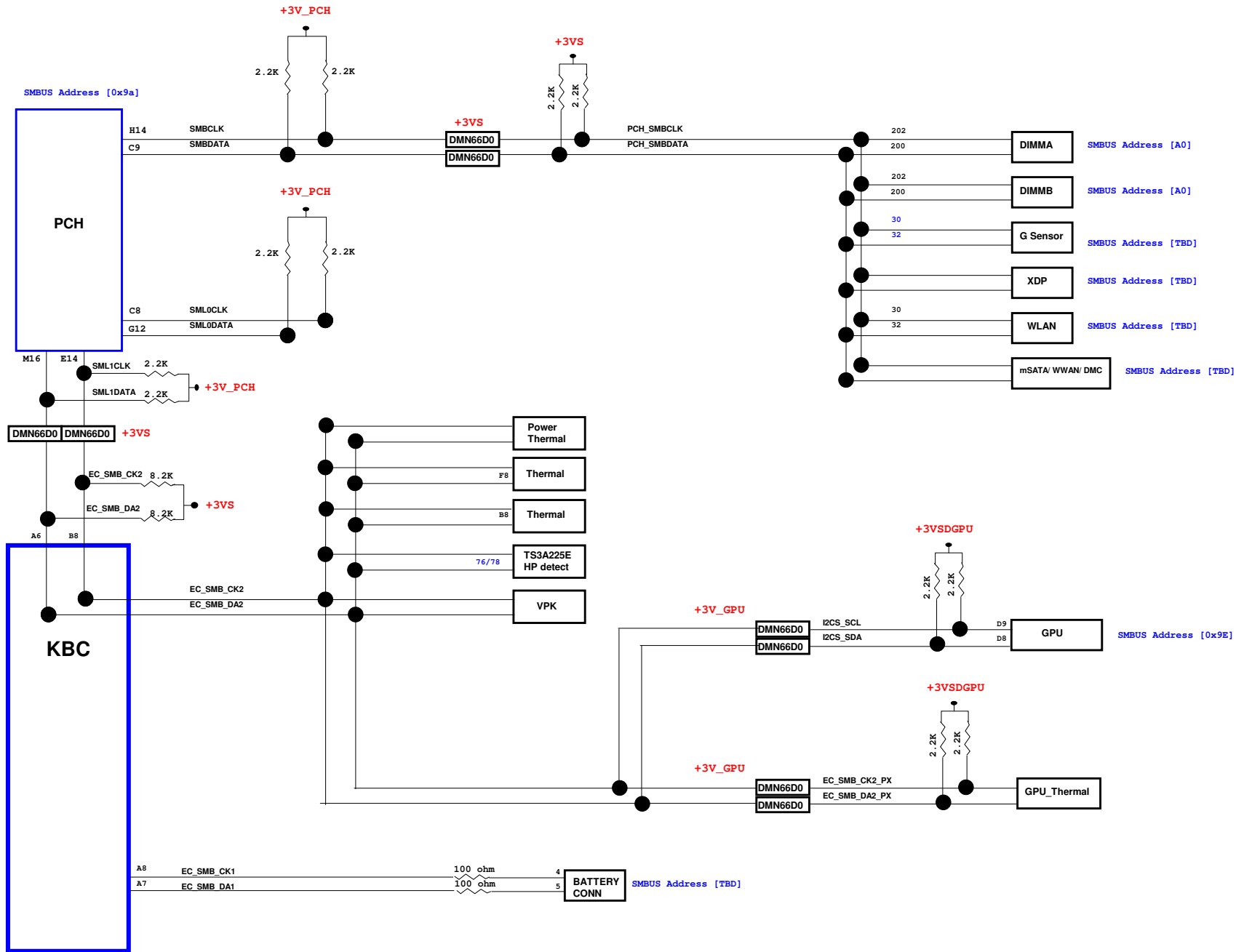


: Choose ONE from three.

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Vcc	3.3V +/- 5%	Board ID Table for AD channel				BOARD ID Table	
Ra	100K +/- 5%						
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	Board ID	PCB Revision
0	0	0 V	0 V	0.155 V	0x00-0x0C	0	
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C	1	
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30	2	
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49	3	
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69	4	SSI_X00
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E	5	PT_X01
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB	6	ST_X02
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF	7	QT_A00

SMBUS Control Table

	SOURCE	MINI1 (WLAN)	MINI2 (DMC)	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	XDP	Charger	HP detect
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V	V		V	V
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V			V		

Link

PCH

USB PORT#	DESTINATION
0	JUSB2 (v3.0 Ext Right Side)
1	JUSB3 (v3.0 Ext Right side)
2	None
3	None
4	JMINI1 (WLAN)
5	JMINI2 (WWAN/DMC)
6	ELC 8051
7	None
8	Bluetooth
9	JUSB1 (2.0 Ext Left Side)
10	None
11	None
12	CAMERA
13	VPK

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

power plane			+5VS +3VS +1.8VS +1.5VS +1.5V_CPU_VDDQ +VCCP = +1.05VS +VCC_CORE +VCC_GFXCORE_AXG +VCCSA +0.75VS +3VSDGPU +1.5VSDGPU +VGA_CORE
State	+5VALW +3VALW +3VLP +3V_PCH	+1.5V	
S0			
S3	ON	ON	ON
	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION		
	CLKOUT_PCIE0	None		
	CLKOUT_PCIE1	10/100/1G LAN		
	CLKOUT_PCIE2	MINI CARD-2 WWAN		
	CLKOUT_PCIE3	MINI CARD-1 WLAN		
	CLKOUT_PCIE4	CARD READER	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE5	None	CLKOUTFLEX0	None
	CLKOUT_PCIE6	None	CLKOUTFLEX1	None
	CLKOUT_PCIE7	None	CLKOUTFLEX2	None
	CLKOUT_PEG_B	None	CLKOUTFLEX3	None

Symbol Note :



: means Digital Ground



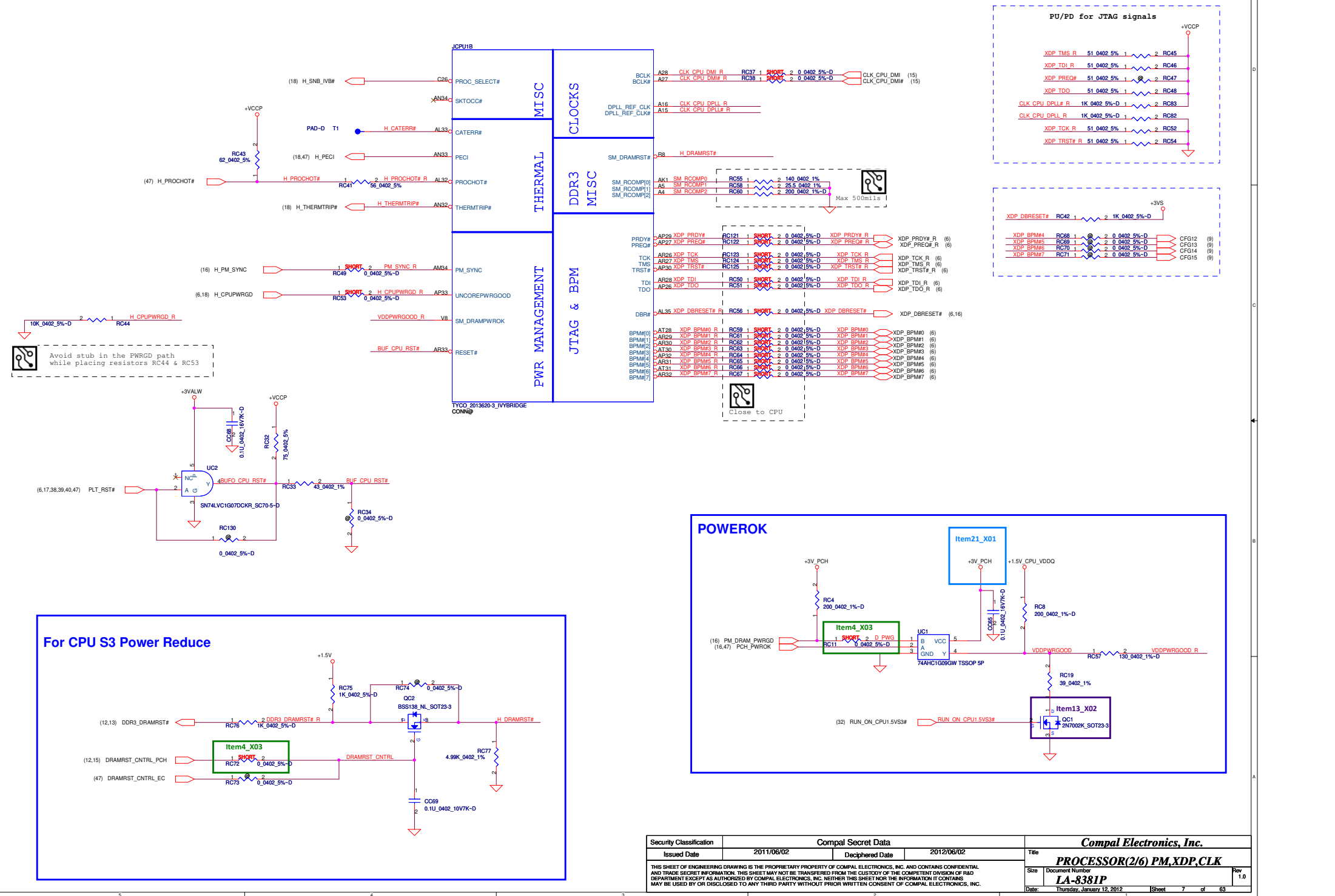
: means Analog Ground

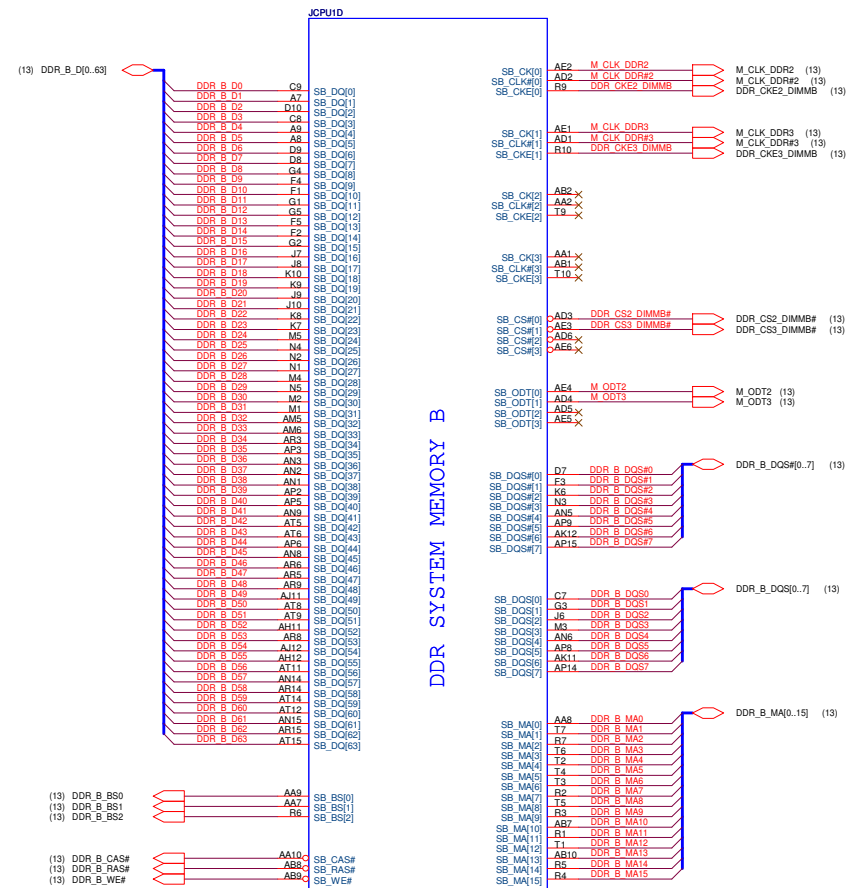
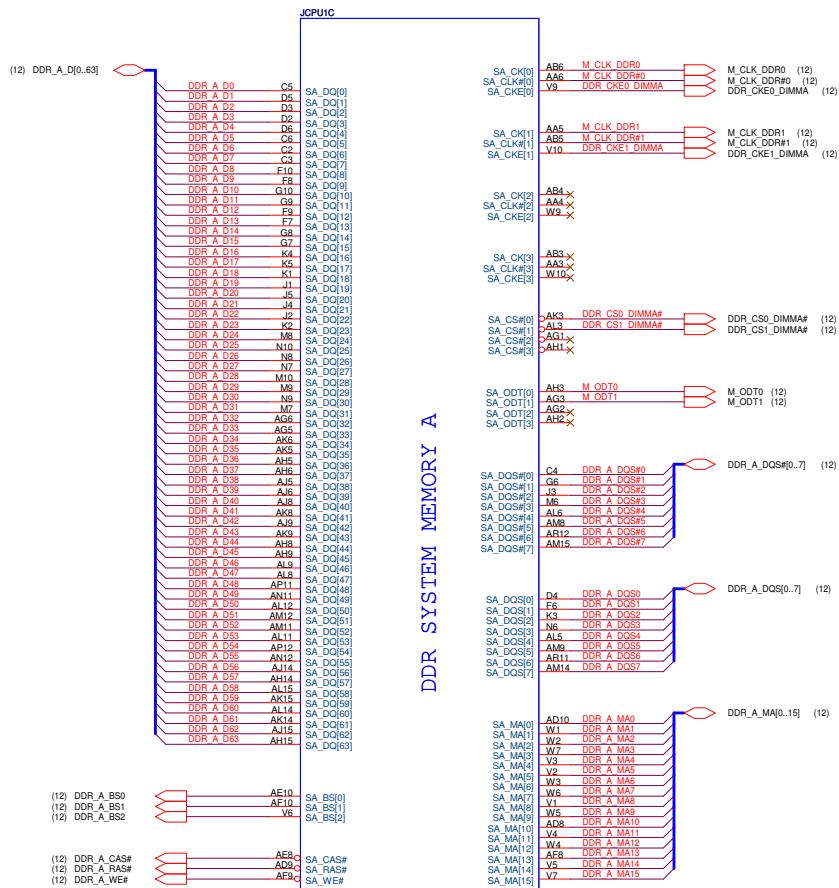
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	m-SATA
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

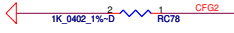
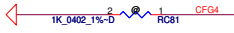
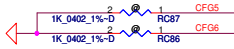
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				Rev 1.0

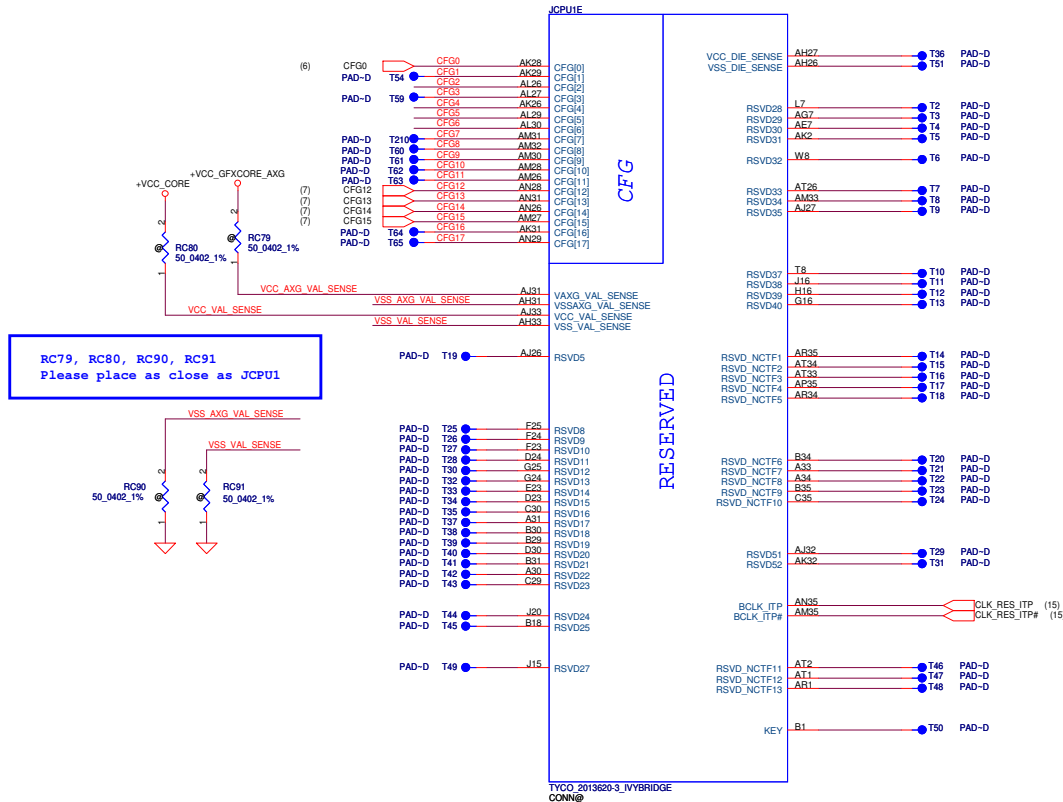
PM, XDP, CLK, S3 Reduce, PLTRST

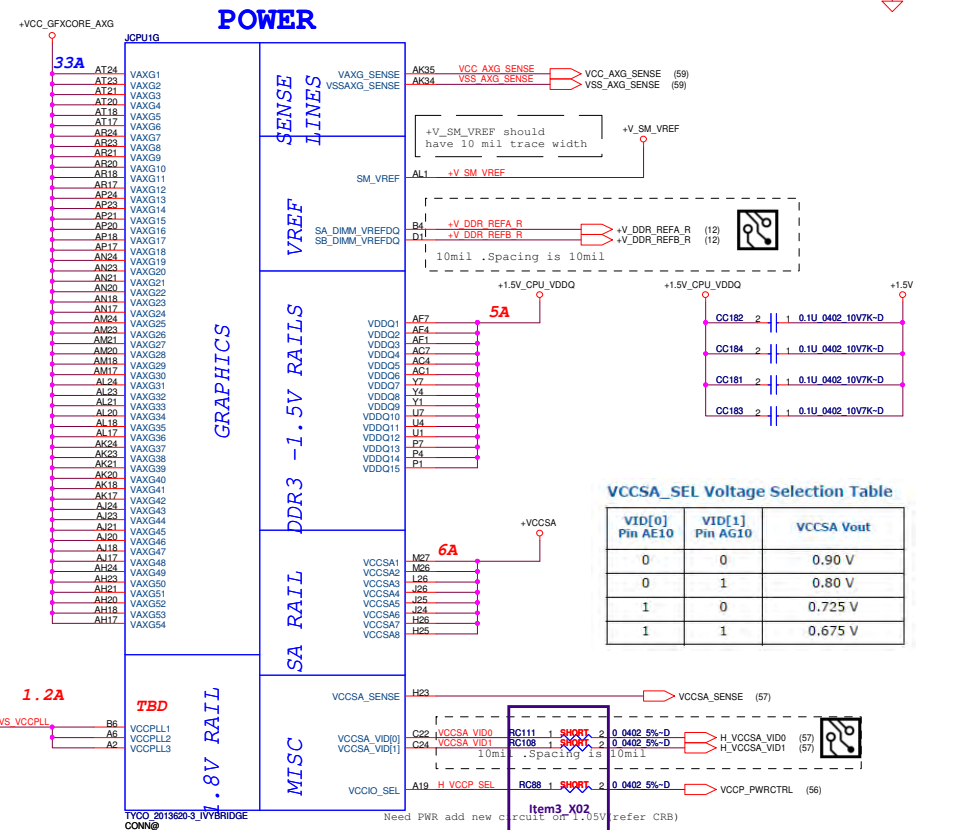
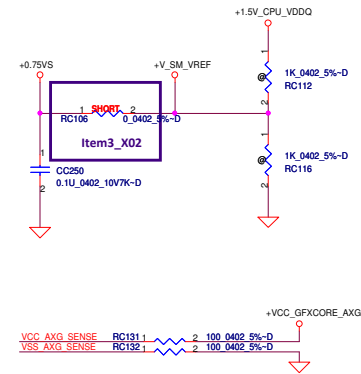
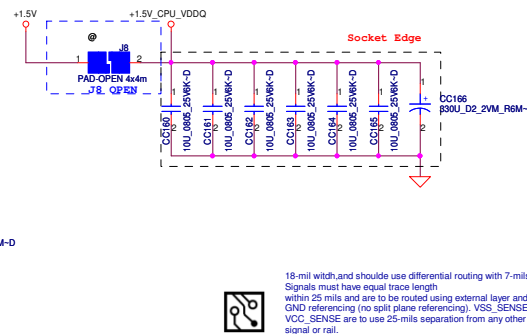




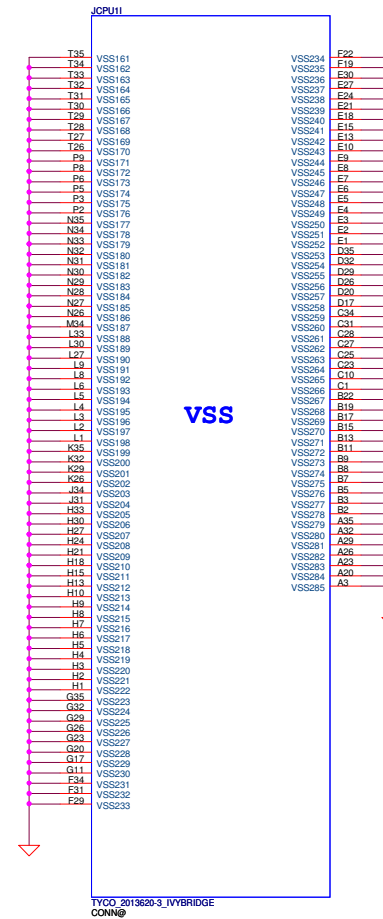
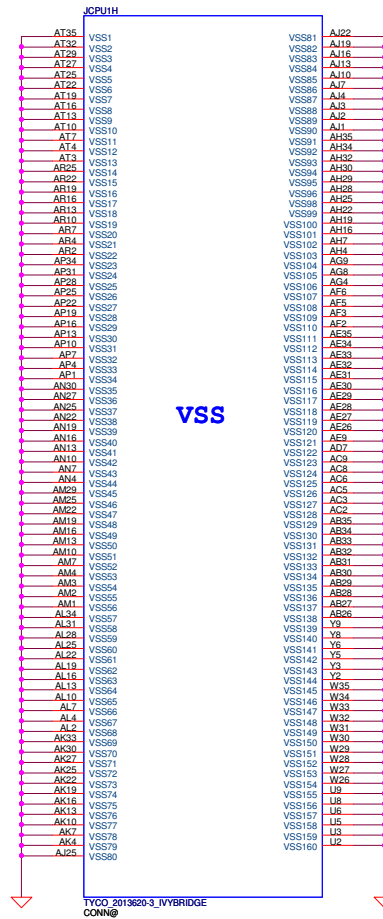
CFG Straps for Processor

	
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
	
Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	
PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, 8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

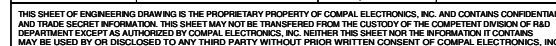


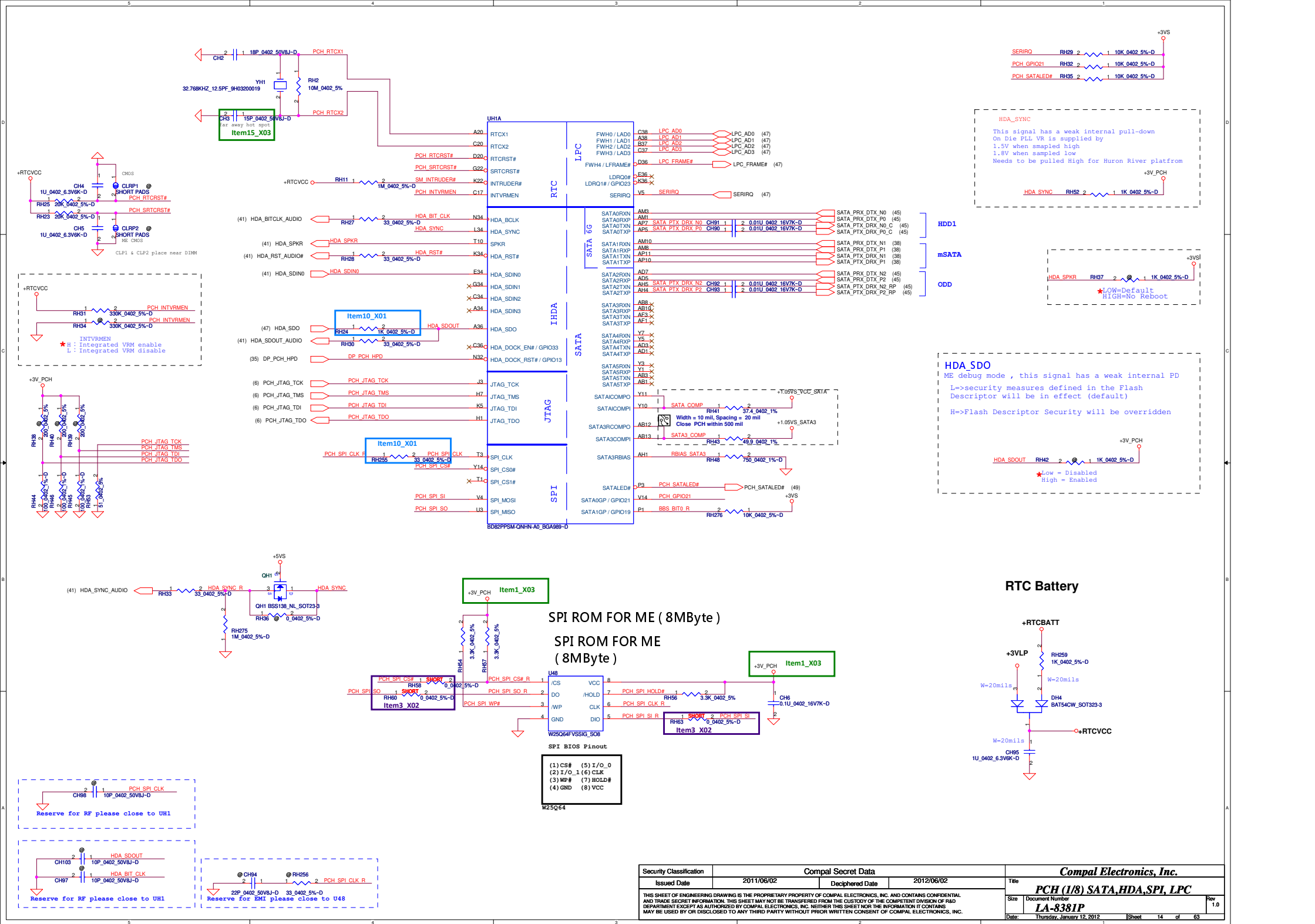


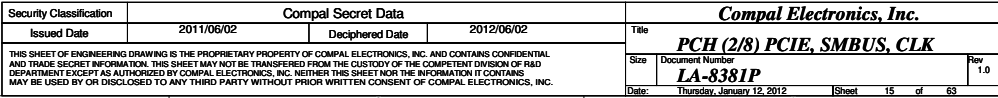
VID[0] Pin AE10	VID[1] Pin AG10	VCCSA Vout
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

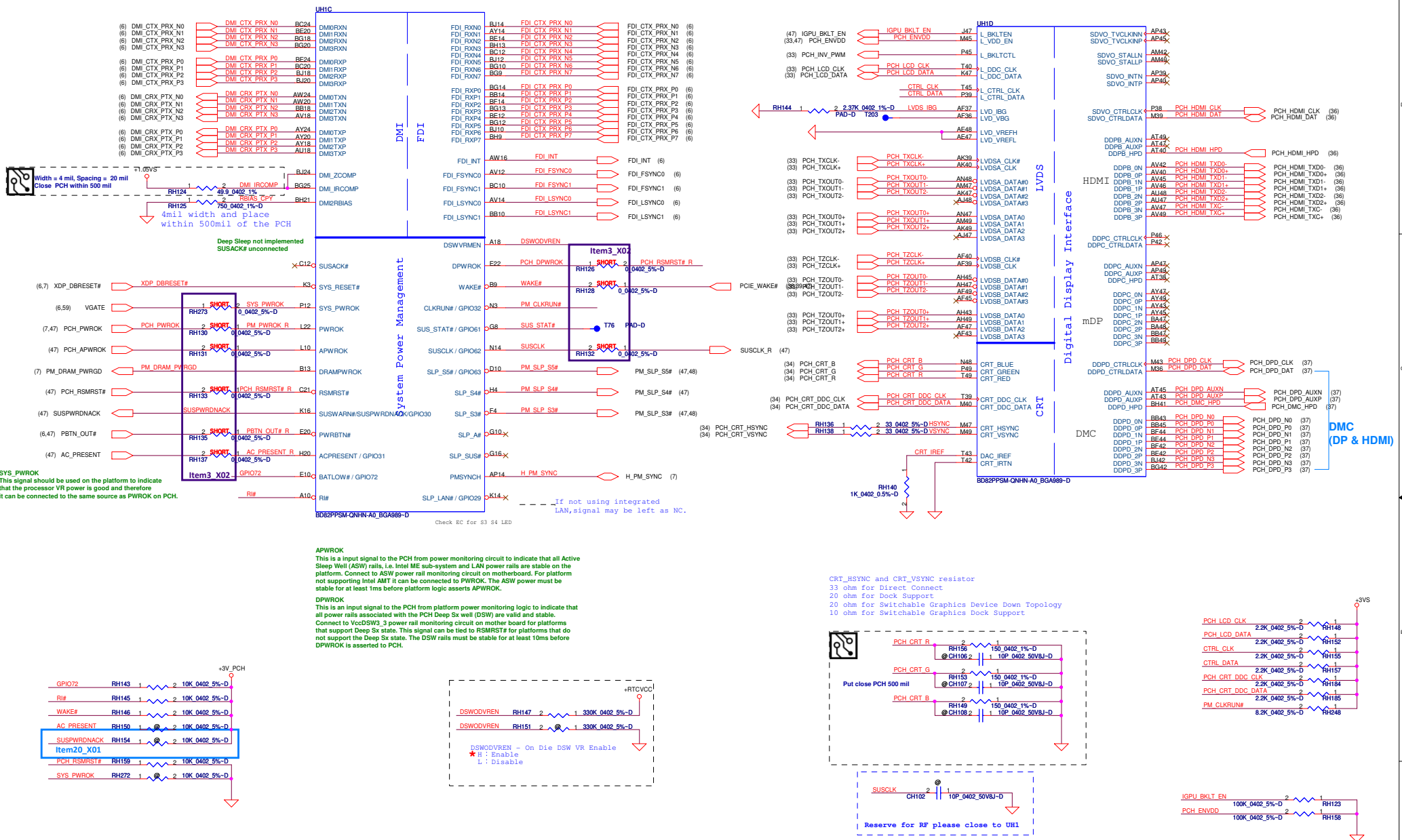


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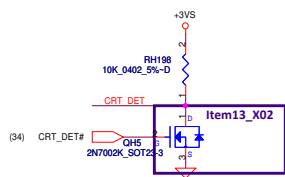




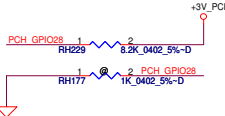




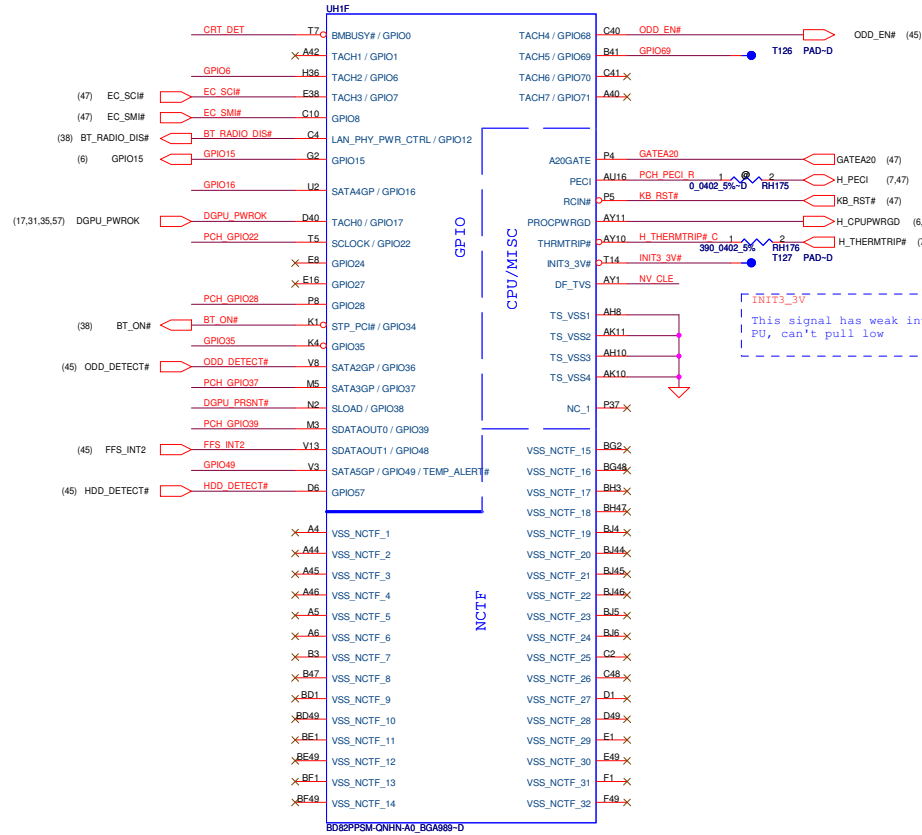
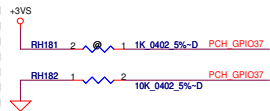
High: CRT Plugged



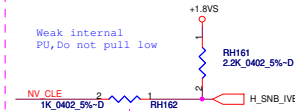
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



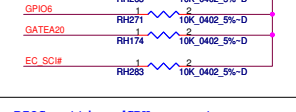
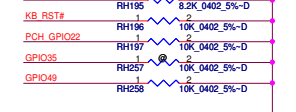
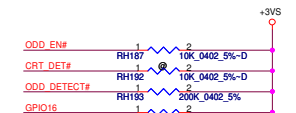
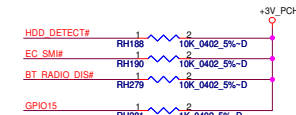
PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated
to same voltage
(DC Coupling Mode)



DMI Termination Voltage	
NV_CLS#	Set to Vcc when HIGH
	Set to Vss when LOW

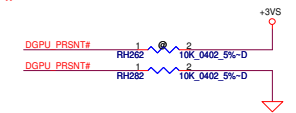


CLOSE TO THE BRANCHING POINT
RH161 and RH162
Follow CRB FAB2 setting



For BIOS setting dGPU present

★ LOW - dGPU exist



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				Size	Document Number
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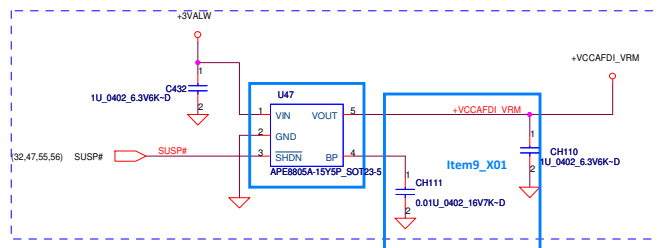
The image shows a complex PCB layout for a power supply section, primarily for a 1300mA power source. The layout is organized into several functional blocks, each with its own set of components and connections.

Power Input and Regulation:

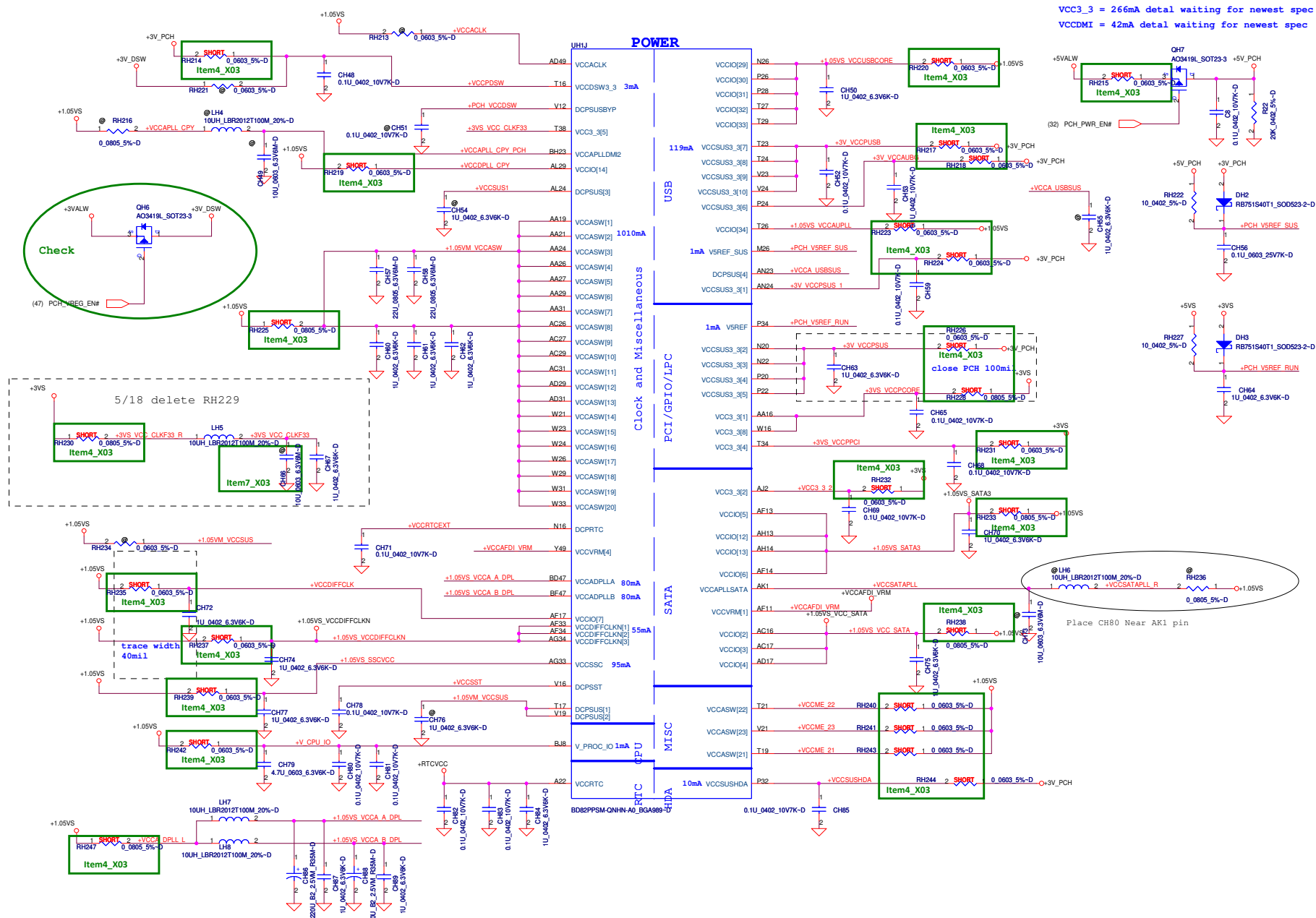
- 1.05VDS Input:** Connected to J10 (PAD-OPEN 4x4mm). The signal passes through a series of capacitors (CH27, CH28, CH29, CH30, CH31) and a resistor (RH201) to the VCCCORE plane.
- 3VDS Input:** Connected to J11 (PAD-OPEN 4x4mm). The signal passes through a series of capacitors (CH32, CH33, CH34, CH35) and a resistor (RH202) to the VCCCORE plane.
- 1.8VDS Input:** Connected to J12 (PAD-OPEN 4x4mm). The signal passes through a series of capacitors (CH36, CH37, CH38, CH39) and a resistor (RH203) to the VCCCORE plane.

Power Planes and Connections:

- VCC CORE:** The main power plane for the 1300mA source. It is connected to the VCCCORE[1] through VCCCORE[17] pins. The plane is populated with numerous capacitors (CH27, CH28, CH29, CH30, CH31, CH32, CH33, CH34, CH35, CH36, CH37, CH38, CH39) and resistors (RH201, RH202, RH203).
- LVDS:** The LVDS power plane is connected to the LVDS[1] through LVDS[4] pins. It is populated with capacitors (CH40, CH41, CH42, CH43, CH44, CH45) and resistors (RH204, RH205, RH206, RH207, RH208, RH209).
- HVCMOS:** The HVCMOS power plane is connected to the HVCMOS[1] through HVCMOS[4] pins. It is populated with capacitors (CH46, CH47, CH48, CH49) and resistors (RH210, RH211, RH212, RH213, RH214, RH215, RH216, RH217, RH218, RH219, RH220, RH221, RH222, RH223, RH224, RH225, RH226, RH227, RH228, RH229, RH230, RH231, RH232, RH233, RH234, RH235, RH236, RH237, RH238, RH239, RH240, RH241, RH242, RH243, RH244, RH245, RH246, RH247, RH248, RH249, RH250, RH251, RH252, RH253, RH254, RH255, RH256, RH257, RH258, RH259, RH260, RH261, RH262, RH263, RH264, RH265, RH266, RH267, RH268, RH269, RH270, RH271, RH272, RH273, RH274, RH275, RH276, RH277, RH278, RH279, RH280, RH281, RH282, RH283, RH284, RH285, RH286, RH287, RH288, RH289, RH290, RH291, RH292, RH293, RH294, RH295, RH296, RH297, RH298, RH299, RH300, RH301, RH302, RH303, RH304, RH305, RH306, RH307, RH308, RH309, RH310, RH311, RH312, RH313, RH314, RH315, RH316, RH317, RH318, RH319, RH320, RH321, RH322, RH323, RH324, RH325, RH326, RH327, RH328, RH329, RH330, RH331, RH332, RH333, RH334, RH335, RH336, RH337, RH338, RH339, RH340, RH341, RH342, RH343, RH344, RH345, RH346, RH347, RH348, RH349, RH350, RH351, RH352, RH353, RH354, RH355, RH356, RH357, RH358, RH359, RH360, RH361, RH362, RH363, RH364, RH365, RH366, RH367, RH368, RH369, RH370, RH371, RH372, RH373, RH374, RH375, RH376, RH377, RH378, RH379, RH380, RH381, RH382, RH383, RH384, RH385, RH386, RH387, RH388, RH389, RH390, RH391, RH392, RH393, RH394, RH395, RH396, RH397, RH398, RH399, RH400, RH401, RH402, RH403, RH404, RH405, RH406, RH407, RH408, RH409, RH410, RH411, RH412, RH413, RH414, RH415, RH416, RH417, RH418, RH419, RH420, RH421, RH422, RH423, RH424, RH425, RH426, RH427, RH428, RH429, RH430, RH431, RH432, RH433, RH434, RH435, RH436, RH437, RH438, RH439, RH440, RH441, RH442, RH443, RH444, RH445, RH446, RH447, RH448, RH449, RH450, RH451, RH452, RH453, RH454, RH455, RH456, RH457, RH458, RH459, RH460, RH461, RH462, RH463, RH464, RH465, RH466, RH467, RH468, RH469, RH470, RH471, RH472, RH473, RH474, RH475, RH476, RH477, RH478, RH479, RH480, RH481, RH482, RH483, RH484, RH485, RH486, RH487, RH488, RH489, RH490, RH491, RH492, RH493, RH494, RH495, RH496, RH497, RH498, RH499, RH500, RH501, RH502, RH503, RH504, RH505, RH506, RH507, RH508, RH509, RH510, RH511, RH512, RH513, RH514, RH515, RH516, RH517, RH518, RH519, RH520, RH521, RH522, RH523, RH524, RH525, RH526, RH527, RH528, RH529, RH530, RH531, RH532, RH533, RH534, RH535, RH536, RH537, RH538, RH539, RH540, RH541, RH542, RH543, RH544, RH545, RH546, RH547, RH548, RH549, RH550, RH551, RH552, RH553, RH554, RH555, RH556, RH557, RH558, RH559, RH560, RH561, RH562, RH563, RH564, RH565, RH566, RH567, RH568, RH569, RH570, RH571, RH572, RH573, RH574, RH575, RH576, RH577, RH578, RH579, RH580, RH581, RH582, RH583, RH584, RH585, RH586, RH587, RH588, RH589, RH590, RH591, RH592, RH593, RH594, RH595, RH596, RH597, RH598, RH599, RH600, RH601, RH602, RH603, RH604, RH605, RH606, RH607, RH608, RH609, RH610, RH611, RH612, RH613, RH614, RH615, RH616, RH617, RH618, RH619, RH620, RH621, RH622, RH623, RH624, RH625, RH626, RH627, RH628, RH629, RH630, RH631, RH632, RH633, RH634, RH635, RH636, RH637, RH638, RH639, RH640, RH641, RH642, RH643, RH644, RH645, RH646, RH647, RH648, RH649, RH650, RH651, RH652, RH653, RH654, RH655, RH656, RH657, RH658, RH659, RH660, RH661, RH662, RH663, RH664, RH665, RH666, RH667, RH668, RH669, RH670, RH671, RH672, RH673, RH674, RH675, RH676, RH677, RH678, RH679, RH680, RH681, RH682, RH683, RH684, RH685, RH686, RH687, RH688, RH689, RH690, RH691, RH692, RH693, RH694, RH695, RH696, RH697, RH698, RH699, RH700, RH701, RH702, RH703, RH704, RH705, RH706, RH707, RH708, RH709, RH710, RH711, RH712, RH713, RH714, RH715, RH716, RH717, RH718, RH719, RH720, RH721, RH722, RH723, RH724, RH725, RH726, RH727, RH728, RH729, RH730, RH731, RH732, RH733, RH734, RH735, RH736, RH737, RH738, RH739, RH740, RH741, RH742, RH743, RH744, RH745, RH746, RH747, RH748, RH749, RH750, RH751, RH752, RH753, RH754, RH755, RH756, RH757, RH758, RH759, RH760, RH761, RH762, RH763, RH764, RH765, RH766, RH767, RH768, RH769, RH770, RH771, RH772, RH773, RH774, RH775, RH776, RH777, RH778, RH779, RH780, RH781, RH782, RH783, RH784, RH785, RH786, RH787, RH788, RH789, RH790, RH791, RH792, RH793, RH794, RH795, RH796, RH797, RH798, RH799, RH800, RH801, RH802, RH803, RH804, RH805, RH806, RH807, RH808, RH809, RH810, RH811, RH812, RH813, RH814, RH815, RH816, RH817, RH818, RH819, RH820, RH821, RH822, RH823, RH824, RH825, RH826, RH827, RH828, RH829, RH830, RH831, RH832, RH833, RH834, RH835, RH836, RH837, RH838, RH839, RH840, RH841, RH842, RH843, RH844, RH845, RH846, RH847, RH848, RH849, RH850, RH851, RH852, RH853, RH854, RH855, RH856, RH857, RH858, RH859, RH860, RH861, RH862, RH863, RH864, RH865, RH866, RH867, RH868, RH869, RH870, RH871, RH872, RH873, RH874, RH875, RH876, RH877, RH878, RH879, RH880, RH881, RH8



PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



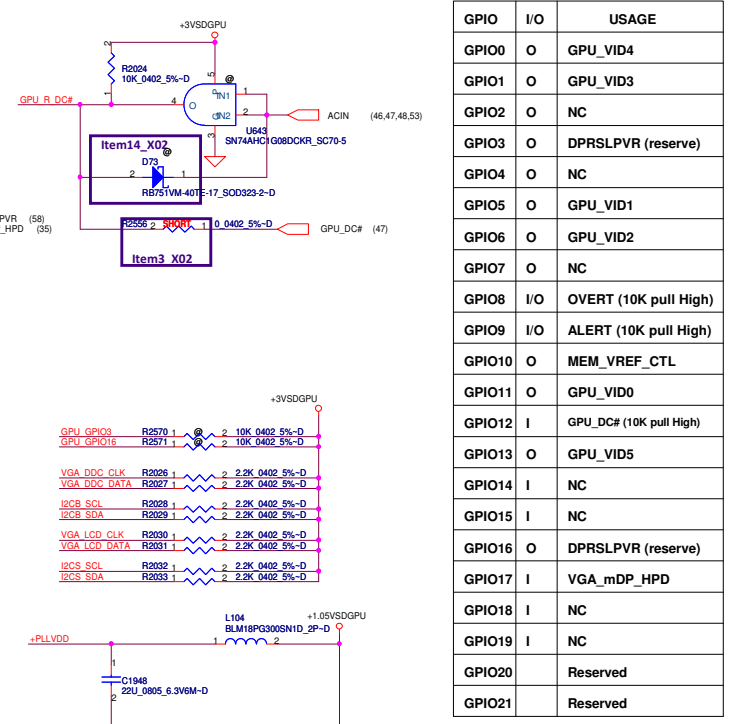
UH1H	
H5	VSS[0]
AA17	VSS[80]
AA2	VSS[81]
AA3	VSS[82]
AA33	VSS[83]
AA34	VSS[84]
AB11	VSS[85]
AB14	VSS[86]
AB39	VSS[87]
AB4	VSS[88]
AB43	VSS[89]
AB5	VSS[90]
AB7	VSS[91]
AC2	VSS[92]
AC19	VSS[93]
AC2	VSS[94]
AC21	VSS[95]
AC33	VSS[96]
AC34	VSS[97]
AD10	VSS[98]
AD11	VSS[99]
AD12	VSS[100]
AD13	VSS[101]
AD19	VSS[102]
AD24	VSS[103]
AD25	VSS[104]
AD27	VSS[105]
AD33	VSS[106]
AD34	VSS[107]
AD36	VSS[108]
AD37	VSS[109]
AD38	VSS[110]
AD39	VSS[111]
AD4	VSS[112]
AD40	VSS[113]
AD41	VSS[114]
AD42	VSS[115]
AD43	VSS[116]
AD45	VSS[117]
AD46	VSS[118]
AE2	VSS[119]
AE3	VSS[120]
AE10	VSS[121]
AE12	VSS[122]
AE13	VSS[123]
AE14	VSS[124]
AE16	VSS[125]
AE19	VSS[126]
AE24	VSS[127]
AE26	VSS[128]
AE27	VSS[129]
AE30	VSS[130]
AE31	VSS[131]
AE34	VSS[132]
AE42	VSS[133]
AE46	VSS[134]
AE5	VSS[135]
AE7	VSS[136]
AF3	VSS[137]
AG19	VSS[138]
AG2	VSS[139]
AG48	VSS[140]
AG49	VSS[141]
AH3	VSS[142]
AH36	VSS[143]
AH39	VSS[144]
AH40	VSS[145]
AH42	VSS[146]
AH46	VSS[147]
AH7	VSS[148]
AJ19	VSS[149]
AJ21	VSS[150]
AJ24	VSS[151]
AJ33	VSS[152]
AJ34	VSS[153]
AK12	VSS[154]
AK3	VSS[155]
AK3	VSS[156]
AK3	VSS[157]
AK3	VSS[158]

BD82PPSM-QNH-N-A0_BGA089-D

UH1	
AY4	VSS[159]
AY42	VSS[160]
AY46	VSS[161]
AY8	VSS[162]
B11	VSS[163]
B15	VSS[164]
B18	VSS[165]
B23	VSS[166]
B27	VSS[167]
BA42	VSS[168]
B35	VSS[169]
B39	VSS[170]
B7	VSS[171]
F45	VSS[172]
BB12	VSS[173]
BB16	VSS[174]
BB20	VSS[175]
BB22	VSS[176]
BB24	VSS[177]
BB28	VSS[178]
BB38	VSS[179]
BB4	VSS[180]
BB46	VSS[181]
BC14	VSS[182]
BC18	VSS[183]
BC2	VSS[184]
BC22	VSS[185]
BC26	VSS[186]
BC32	VSS[187]
BC34	VSS[188]
BC36	VSS[189]
BC40	VSS[190]
BC42	VSS[191]
BC48	VSS[192]
BD46	VSS[193]
BD5	VSS[194]
BE22	VSS[195]
BE26	VSS[196]
BE32	VSS[197]
BE40	VSS[198]
BF10	VSS[199]
BF12	VSS[200]
BF16	VSS[201]
BF20	VSS[202]
BF22	VSS[203]
BF24	VSS[204]
BF26	VSS[205]
BF28	VSS[206]
BD3	VSS[207]
BF30	VSS[208]
BF38	VSS[209]
BF40	VSS[210]
BF4	VSS[211]
BG17	VSS[212]
BG21	VSS[213]
BG33	VSS[214]
BG44	VSS[215]
BH11	VSS[216]
BH15	VSS[217]
BH17	VSS[218]
BH19	VSS[219]
BH27	VSS[220]
BH31	VSS[221]
BH33	VSS[222]
BH35	VSS[223]
BH39	VSS[224]
BH43	VSS[225]
BH7	VSS[226]
D3	VSS[227]
D12	VSS[228]
D16	VSS[229]
D18	VSS[230]
D22	VSS[231]
D24	VSS[232]
D26	VSS[233]
D30	VSS[234]
D32	VSS[235]
D34	VSS[236]
D38	VSS[237]
D42	VSS[238]
D8	VSS[239]
E18	VSS[240]
E26	VSS[241]
E18	VSS[242]
G20	VSS[243]
G22	VSS[244]
G26	VSS[245]
G28	VSS[246]
G38	VSS[247]
G48	VSS[248]
H12	VSS[249]
H18	VSS[250]
H22	VSS[251]
H24	VSS[252]
H26	VSS[253]
H30	VSS[254]
H32	VSS[255]
H34	VSS[256]
F3	VSS[257]
F3	VSS[258]

BD82PPSM-QNH-N-A0_BGA089-D

H46	VSS[259]
K18	VSS[260]
K26	VSS[261]
K39	VSS[262]
K46	VSS[263]
K7	VSS[264]
L18	VSS[265]
L2	VSS[266]
L26	VSS[267]
L28	VSS[268]
L28	VSS[269]
L36	VSS[270]
L48	VSS[271]
M12	VSS[272]
P18	VSS[273]
M18	VSS[274]
M22	VSS[275]
M30	VSS[276]
M32	VSS[277]
M34	VSS[278]
M38	VSS[279]
M4	VSS[280]
M46	VSS[281]
M46	VSS[282]
M48	VSS[283]
M8	VSS[284]
M8	VSS[285]
P30	VSS[286]
P30	VSS[287]
P11	VSS[288]
P18	VSS[289]
P30	VSS[290]
P43	VSS[291]
P40	VSS[292]
P43	VSS[293]
P47	VSS[294]
R2	VSS[295]
R48	VSS[296]
T12	VSS[297]
T31	VSS[298]
T37	VSS[299]
T4	VSS[300]
W34	VSS[301]
T46	VSS[302]
T47	VSS[303]
T8	VSS[304]
V11	VSS[305]
V17	VSS[306]
V26	VSS[307]
V27	VSS[308]
V31	VSS[309]
V38	VSS[310]
V39	VSS[311]
V43	VSS[312]
V7	VSS[313]
W17	VSS[314]
W19	VSS[315]
W2	VSS[316]
W27	VSS[317]
W48	VSS[318]
X12	VSS[319]
X4	VSS[320]
Y42	VSS[321]
Y46	VSS[322]
Y8	VSS[323]
Y4	VSS[324]
Y4	VSS[325]
Y4	VSS[326]
Y4	VSS[327]
Y4	VSS[328]
Y4	VSS[329]
Y4	VSS[330]
Y4	VSS[331]
Y4	VSS[332]
Y4	VSS[333]
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Y4	VSS[347]
Y4	VSS[348]
Y4	VSS[349]
Y4	VSS[350]
Y4	VSS[351]
Y4	VSS[352]



04/06 : Add 6bit VID Function.

N13P-PE5-A1

N13P-GT boot voltage: confirm Nvidia

3VSDGPU

N13P-GT boot voltage: confirm Nvidia

Item3 X02

GPU_VID_0 (56)

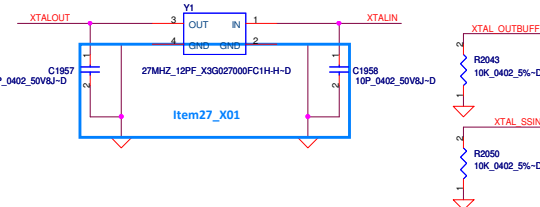
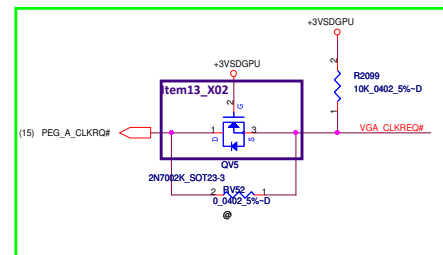
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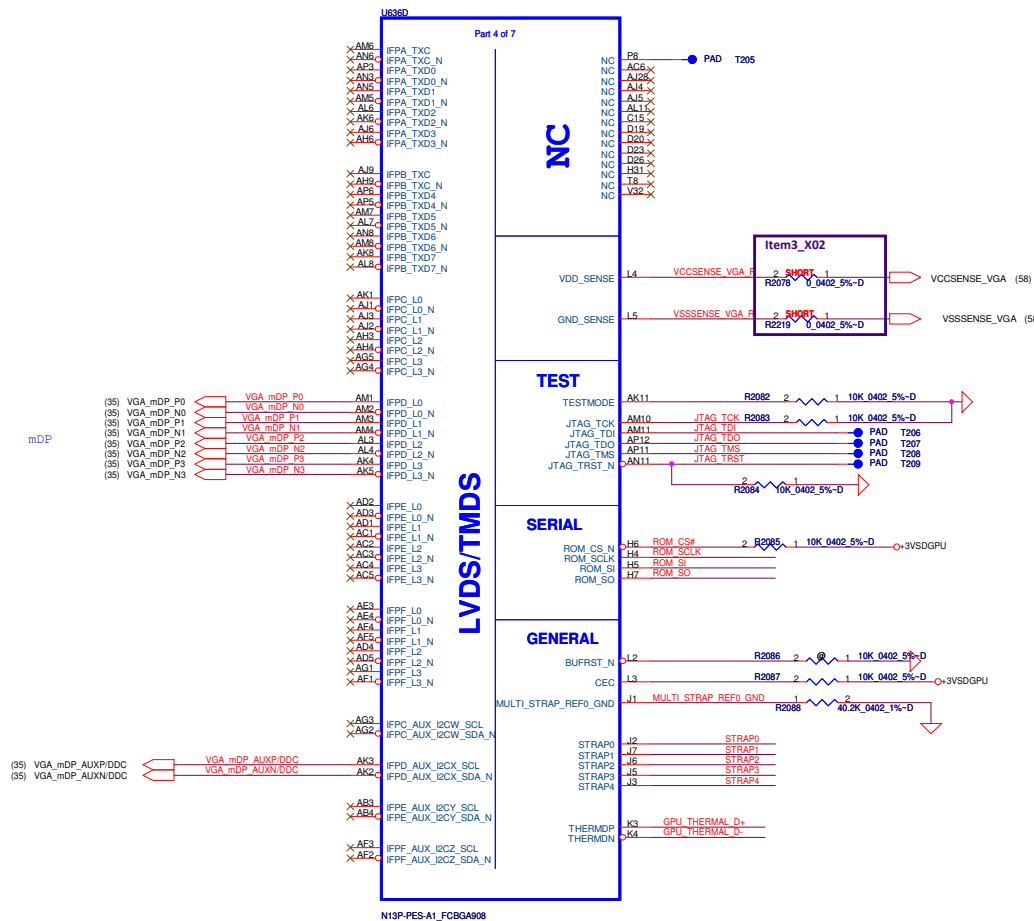
GPU_VID_2 (56)

GPU_VID_3 (56)

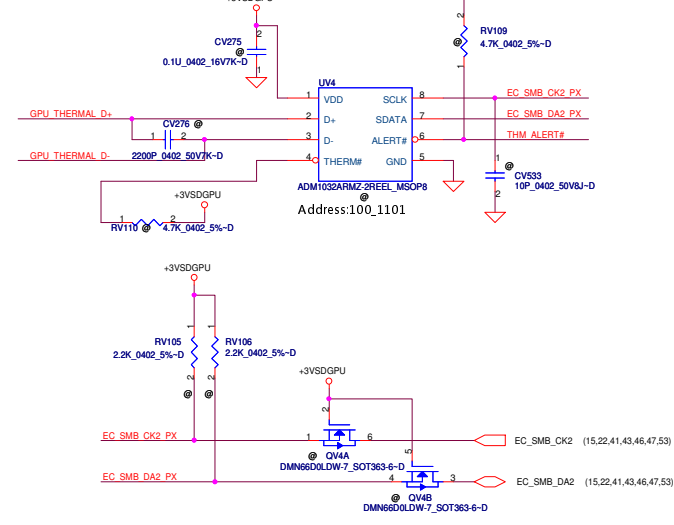
GPU_VID_4 (56)

GPU_VID_5 (56)

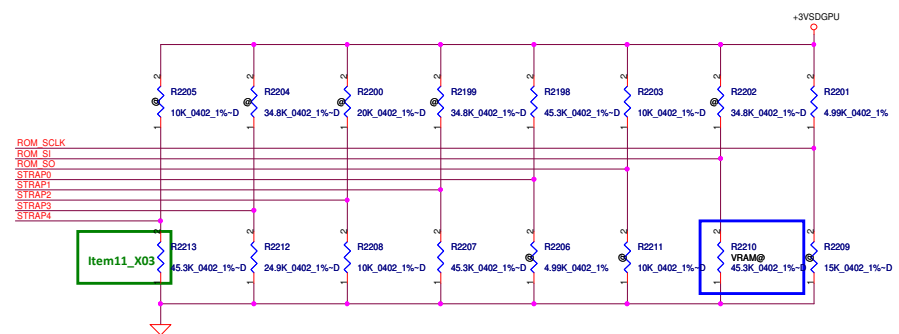




VGA Thermal Sensor ADM1032ARMZ Closed to GPU

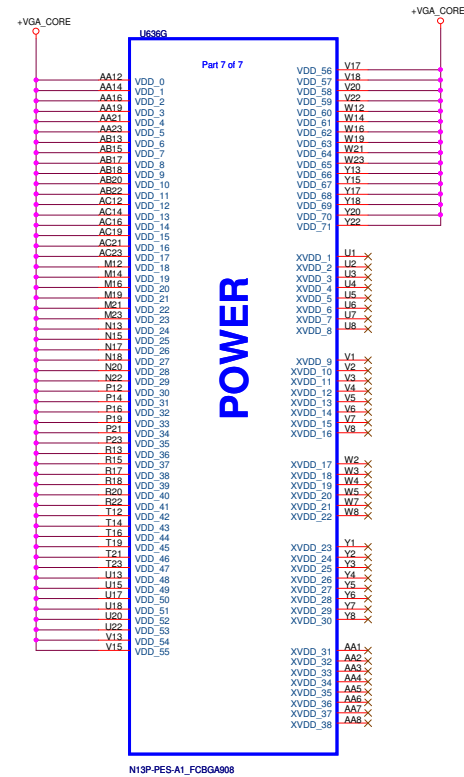
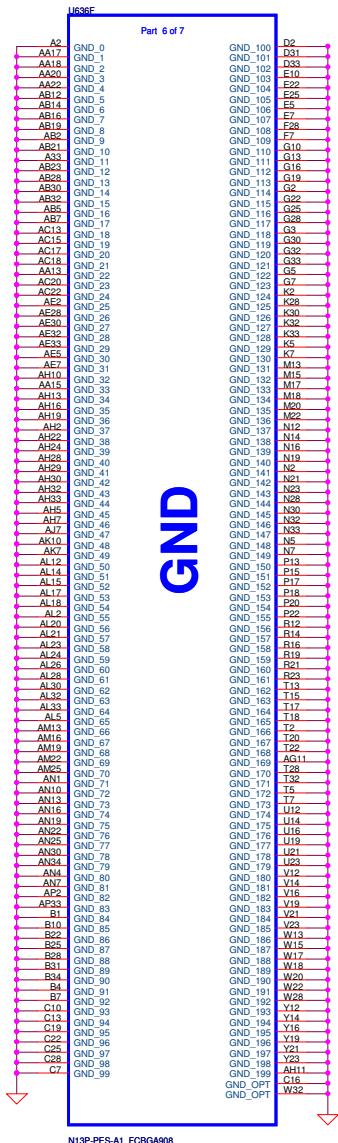


MULTI LEVEL STRAPS



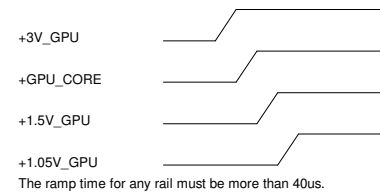
For N13P-GT strap table

GPU	Freq.	Memory Size	Memory Config	ROM_SCLK	ROM_SI	ROM_SO	STRAP0	STRAP1 (PCle driving)	STRAP2 (ES PH20K)	STRAP3	STRAP4
N13P-GT	2500 Mhz	64M* 16* 8 1GB	Samsung SA00003RS0L	PH 5K	PL 45.3K SD03445328L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 Mhz	64M* 16* 8 1GB	Hynix SA00003WL0L	PH 5K	PL 34.8K SD03434828L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 Mhz	128M* 16* 8 2GB	Samsung SA000048E0L	PH 5K	PL 30.1K SD03430128L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K
N13P-GT	2500 Mhz	128M* 16* 8 2GB	Hynix SA00004GD0L	PH 5K	PL 24.9K SD03424928L	PH 10K	PH 45K	PL 45K	PL 10K	PL 25K	PL 10K

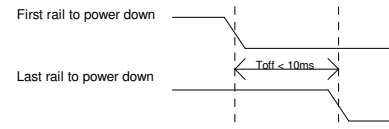


SEQUENCE

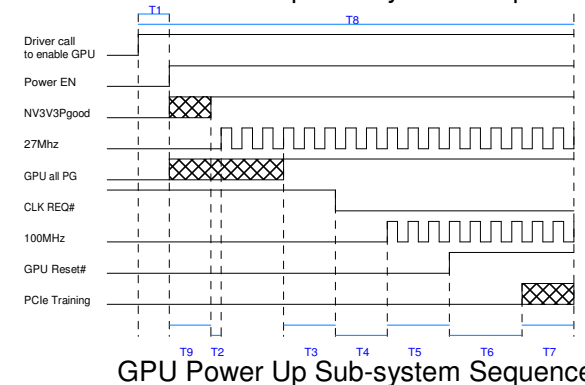
GPU Power Up Power Rail Sequence



GPU Power Down Sequence



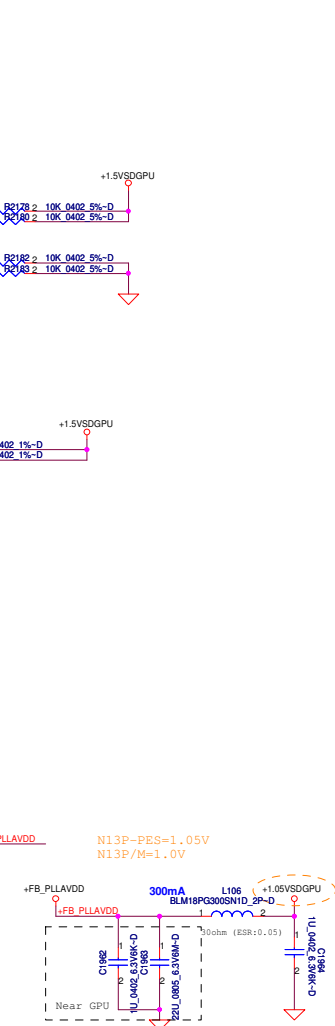
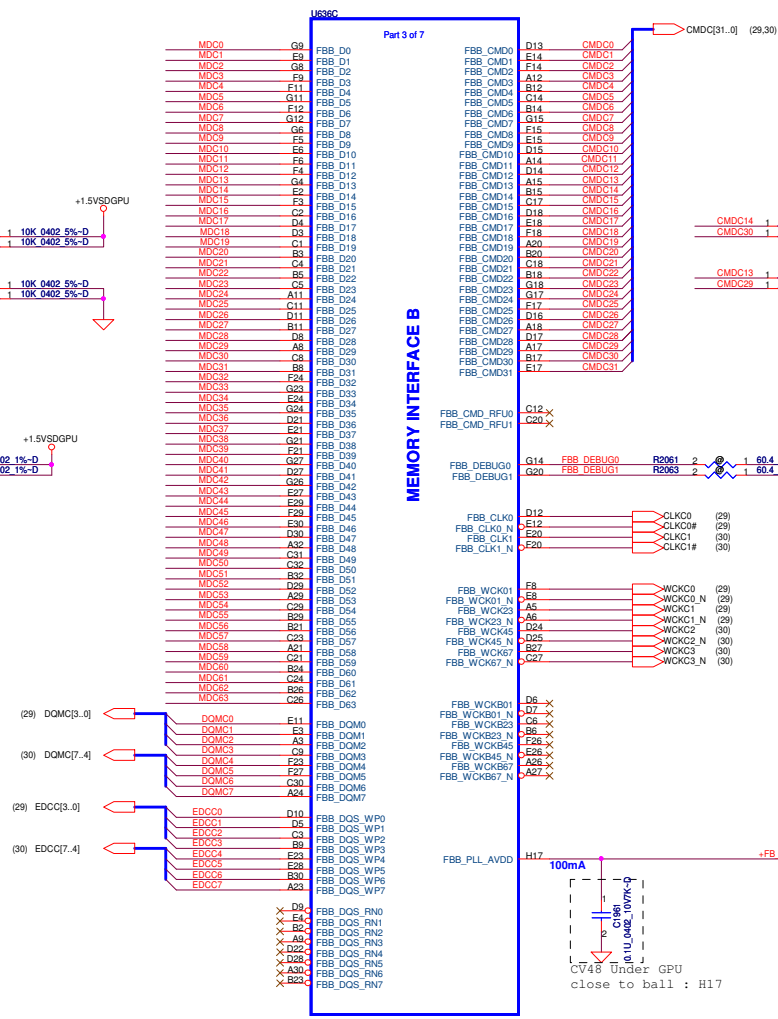
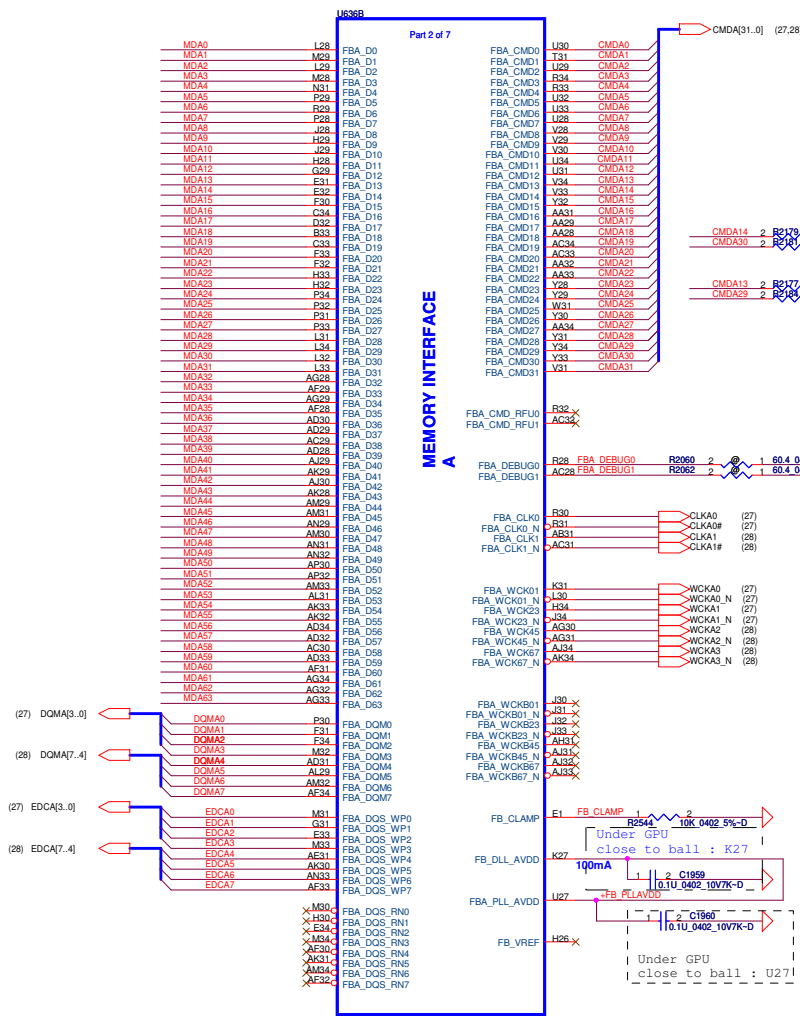
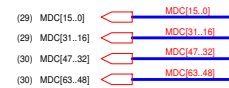
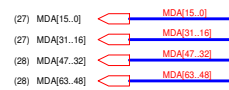
GPU Power Up Sub-system Sequence



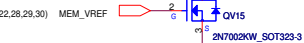
GPU Power Up Sub-system Sequence

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				N13P (4/10) POWER & GND	
Size	Document Number			Rev	
	LA-8381P			0.1	
Date:		Thursday, January 12, 2012		Sheet	25 of 63

VRAM Interface

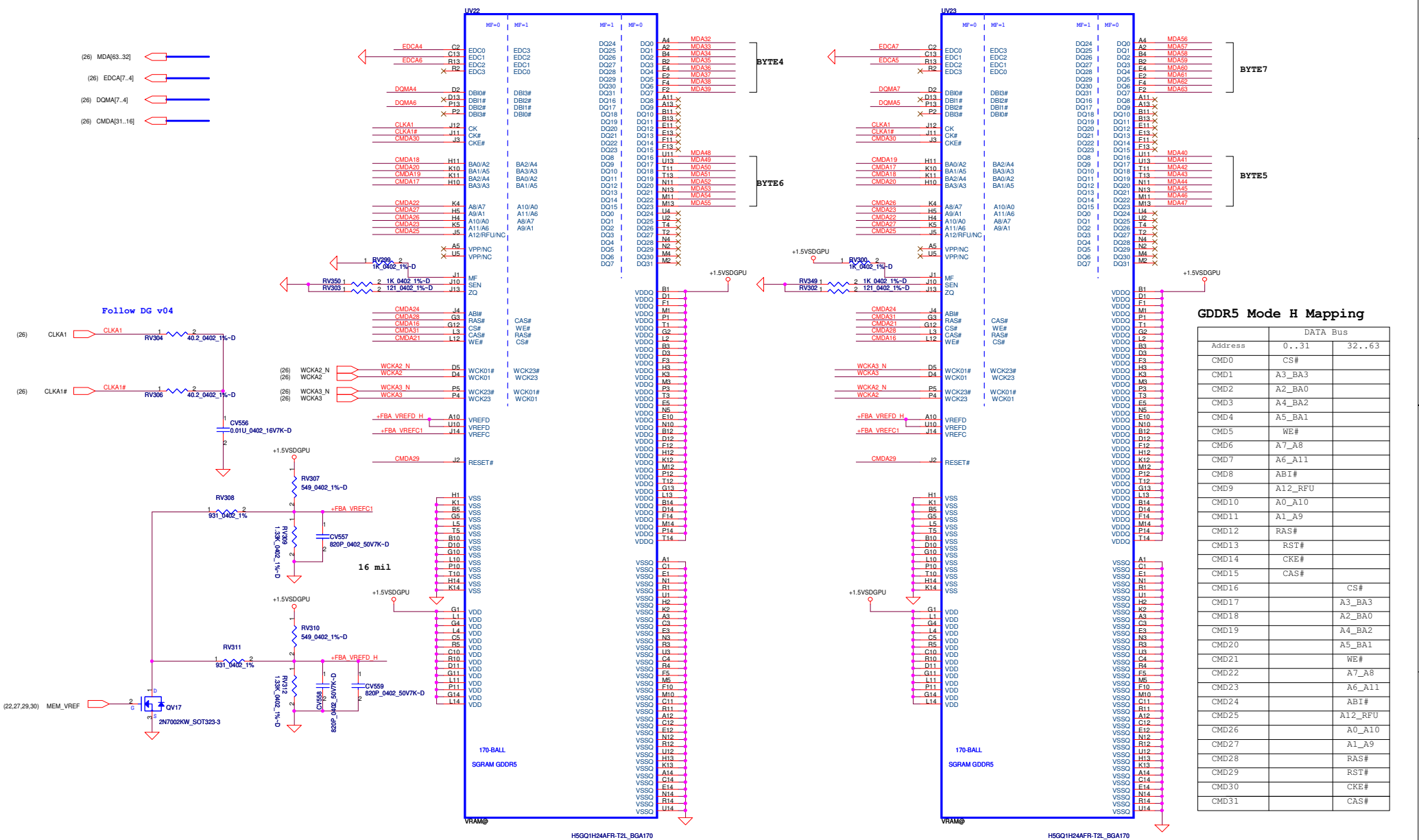


22,28,29,30) MEM_VREF 2 G QV15
2N7002KW_SOT323-3



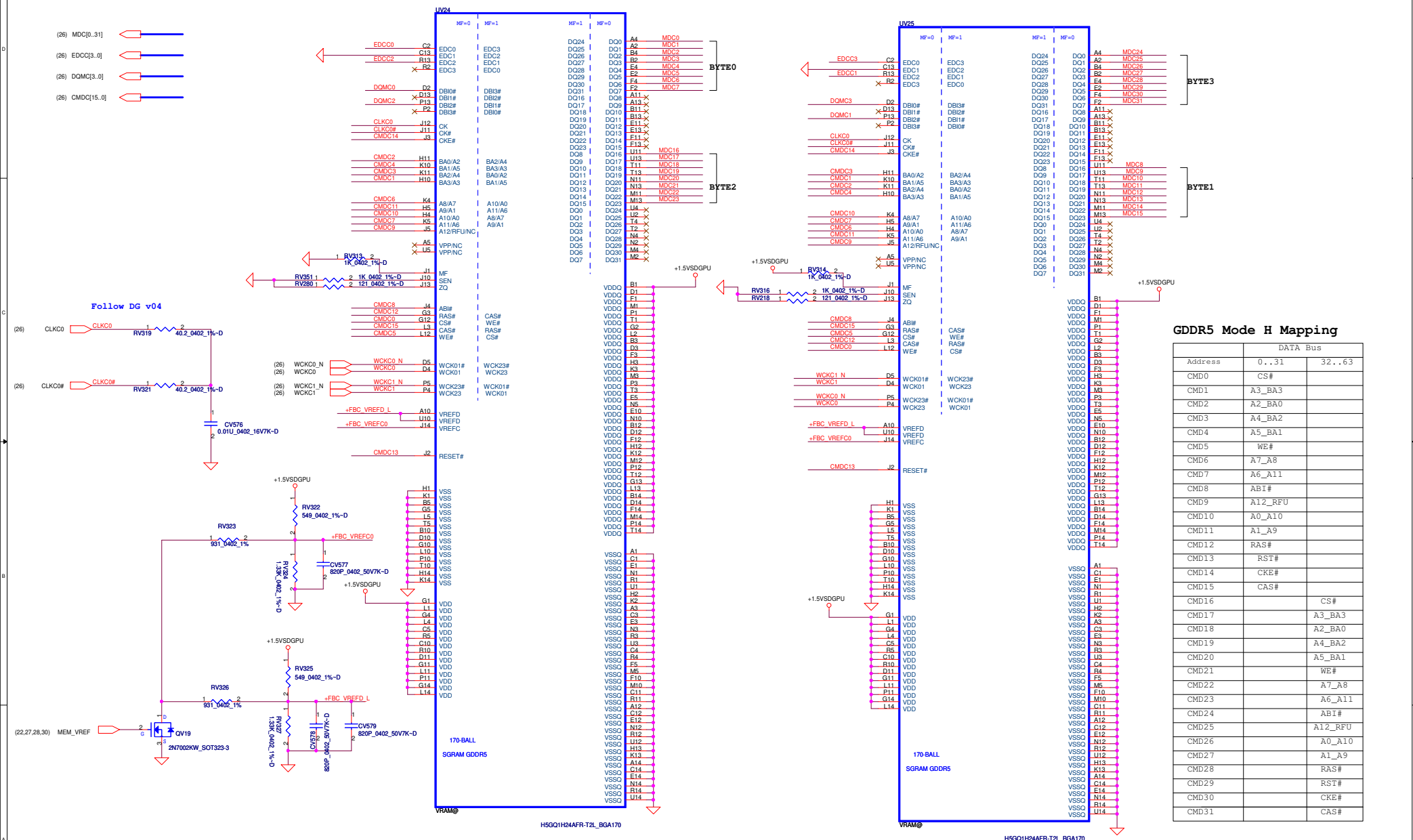
	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Memory Partition A - Upper 32 bits

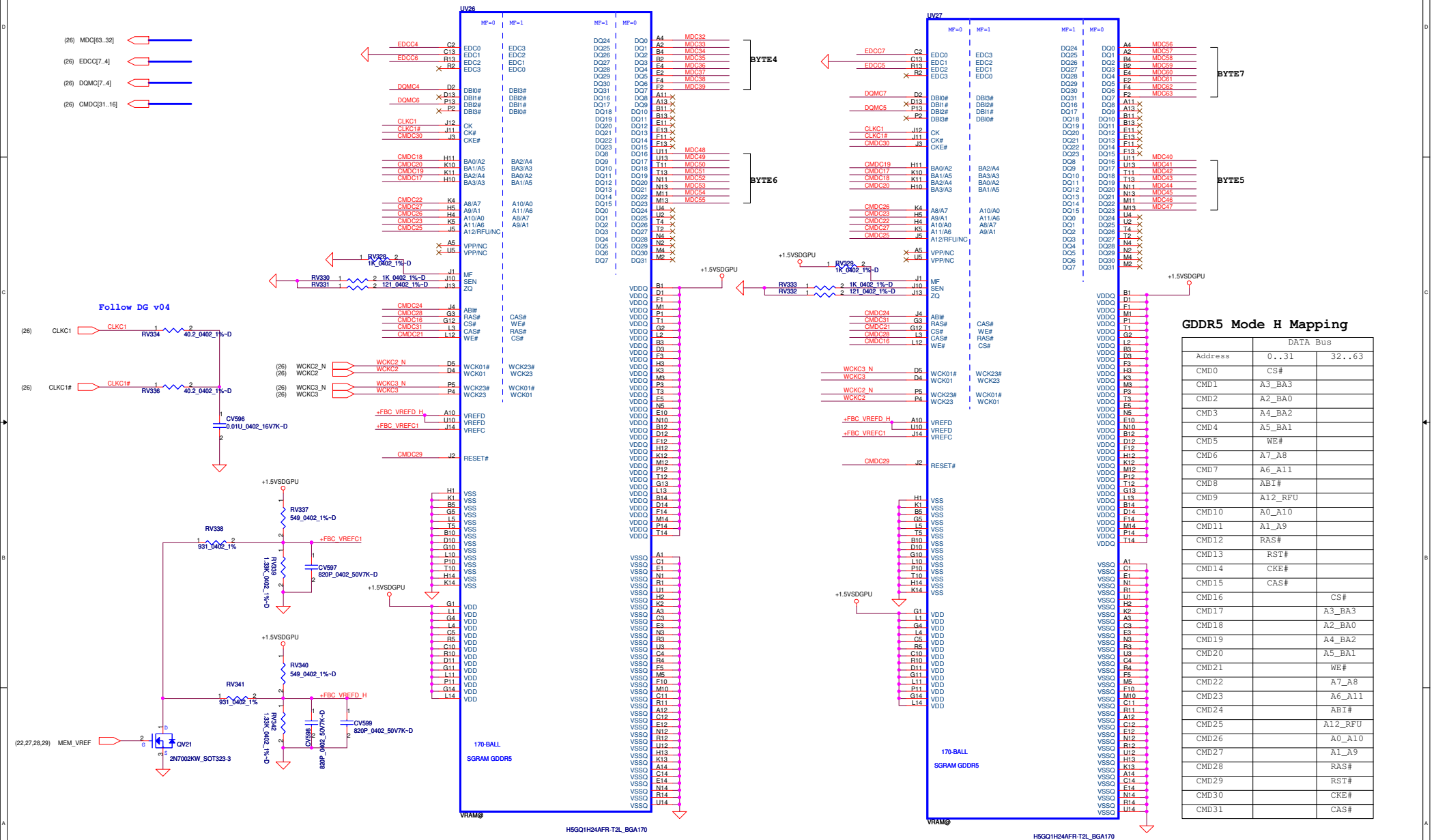


	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

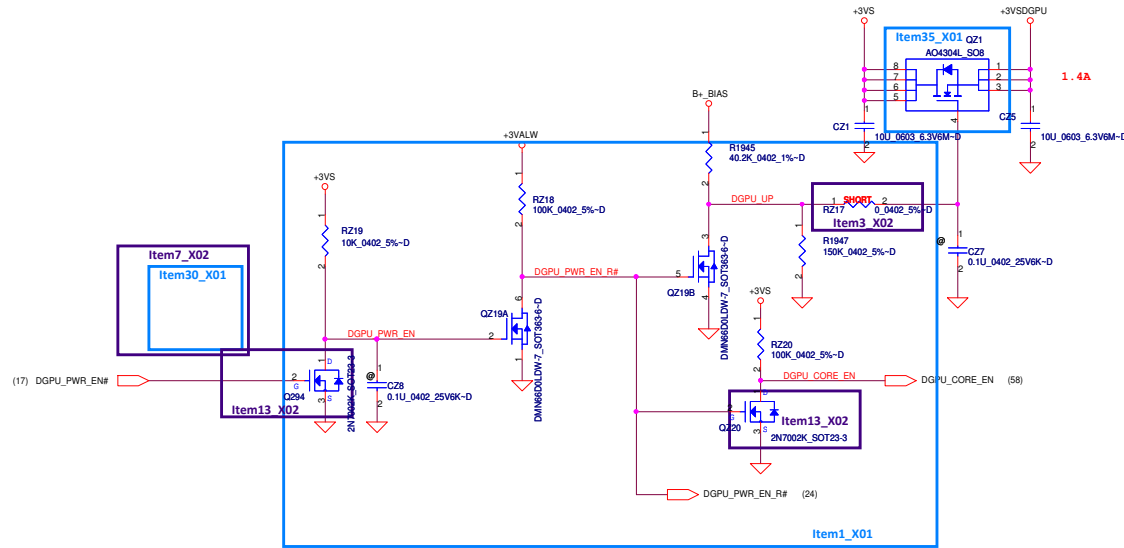
Memory Partition C - Lower 32 bits



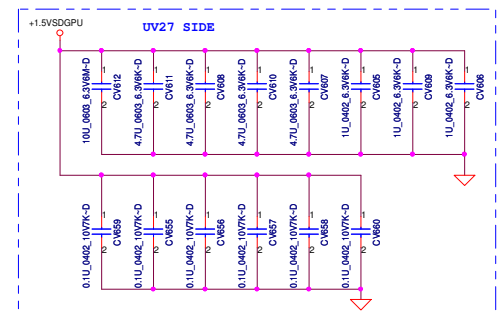
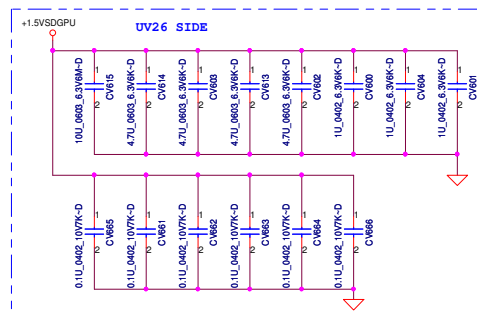
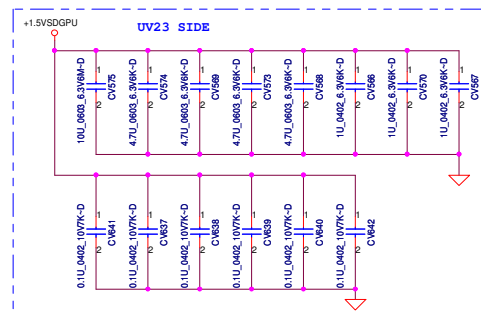
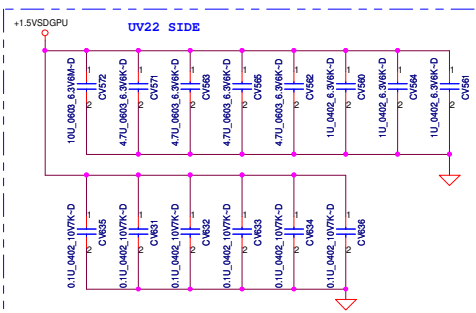
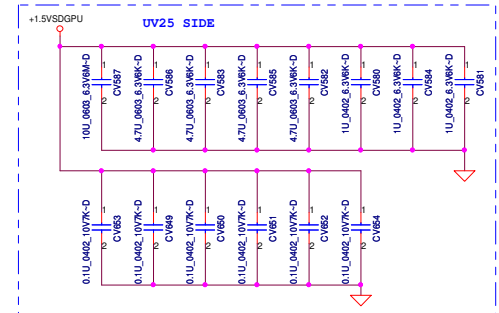
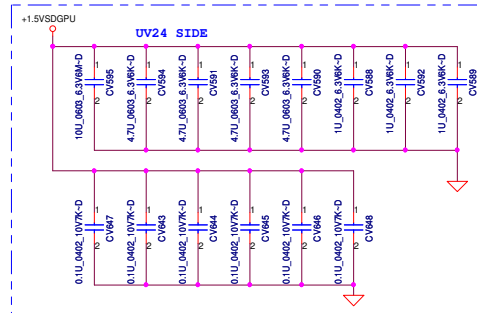
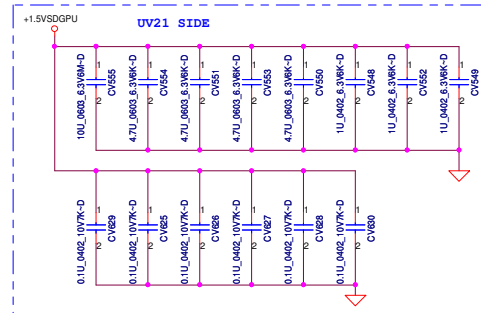
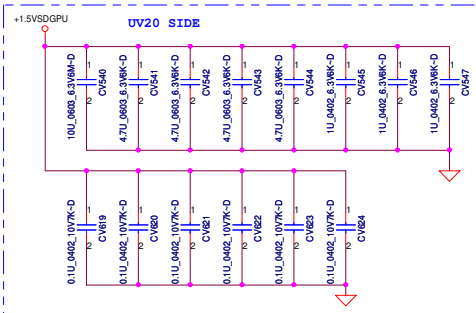
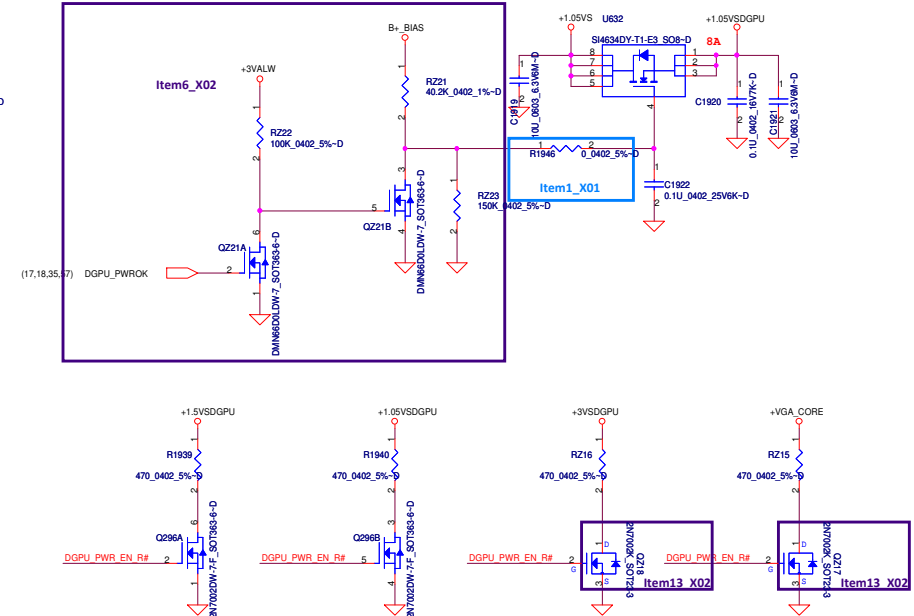
Memory Partition C - Upper 32 bits



+3VS to +3VSDGPU

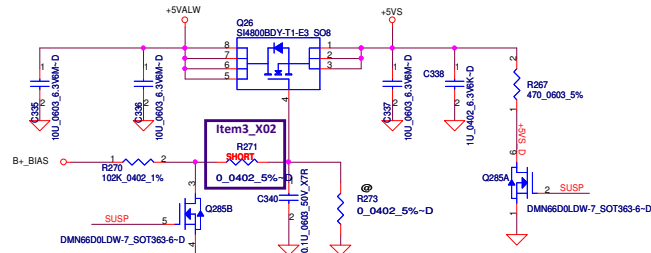


+1.05V to +1.05VSDGPU Transfer

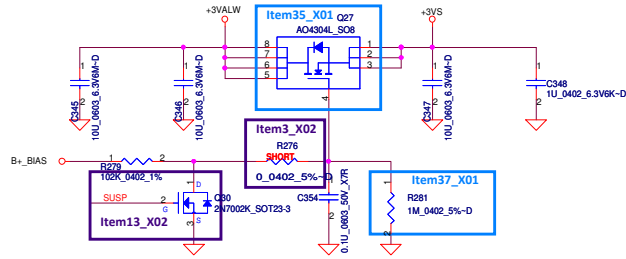


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				LA-8381P	Rev 1.0
				Date	Thursday, January 12, 2012
				Sheet	31 of 63

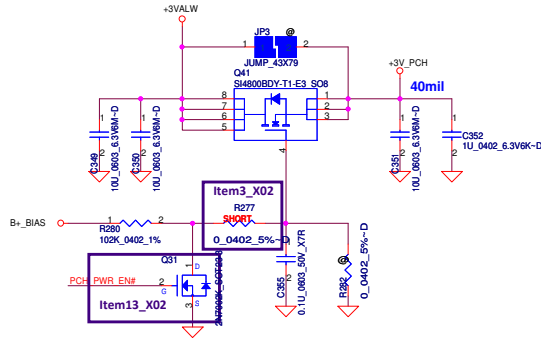
+5VALW to +5VS



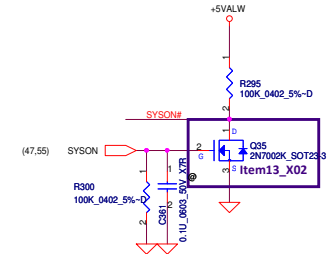
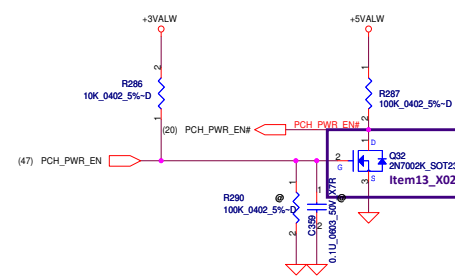
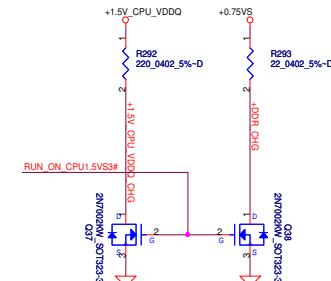
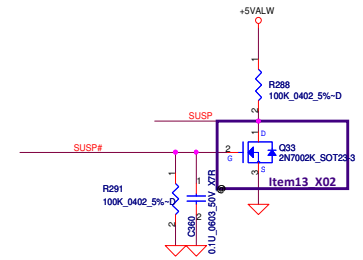
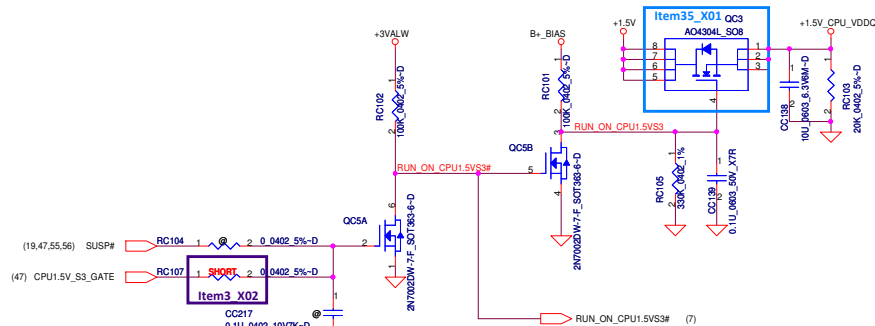
+3VALW to +3VS



+3VALW to +3V_PCH

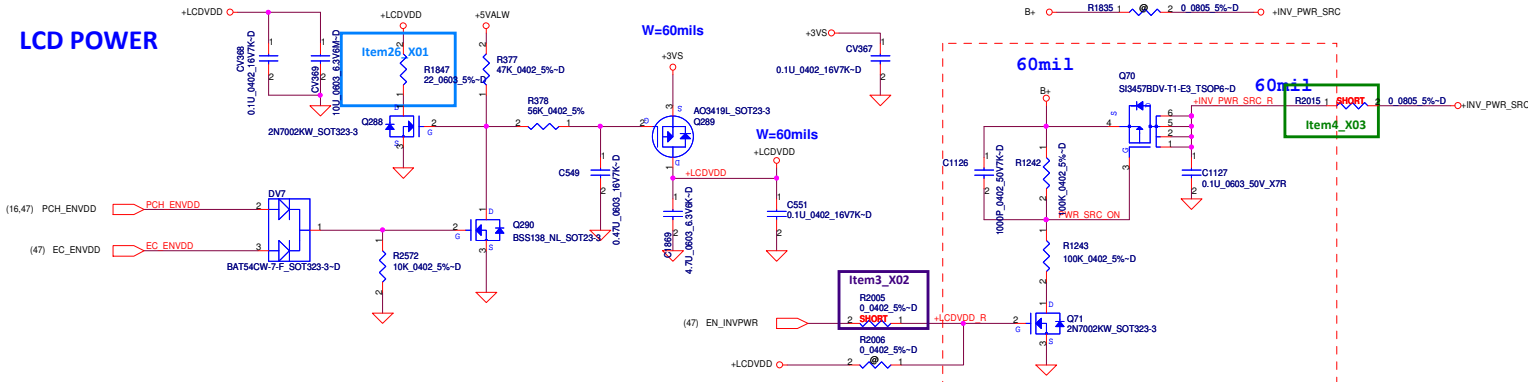


+1.5V to +1.5V_CPU_VDDQ

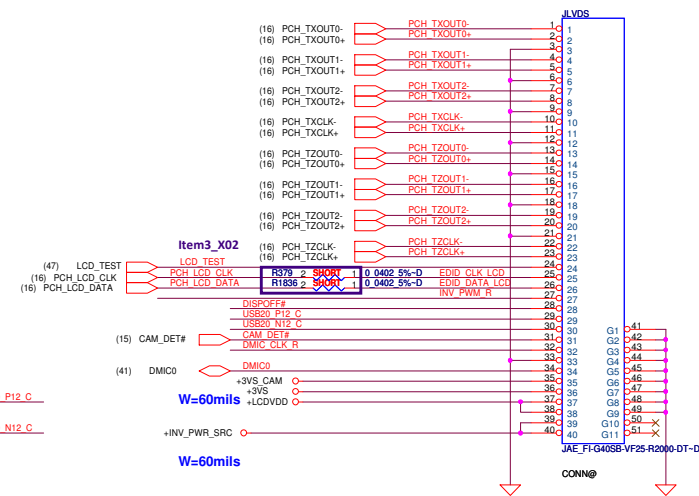


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Issued Date	2011/06/02	Deciphered Date	2012/06/02	Document Number
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				LA-8381P
				Rev
				1.0
				Date: Thursday, January 12, 2012
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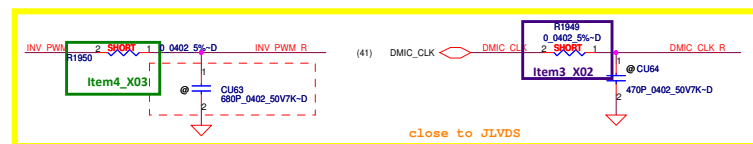
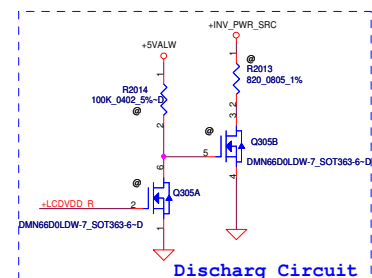
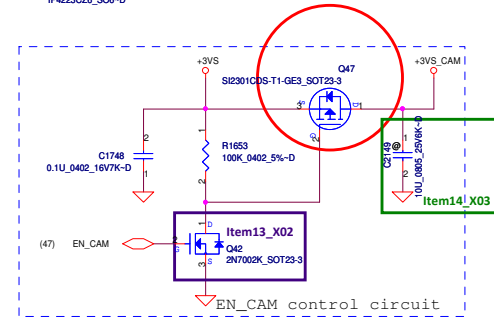
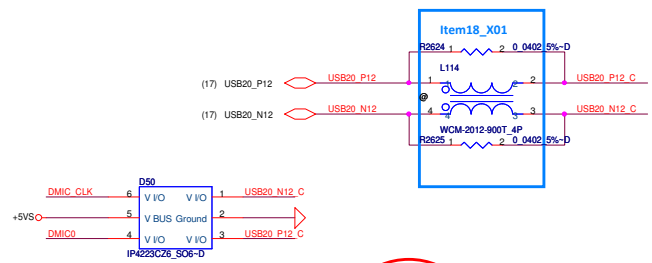
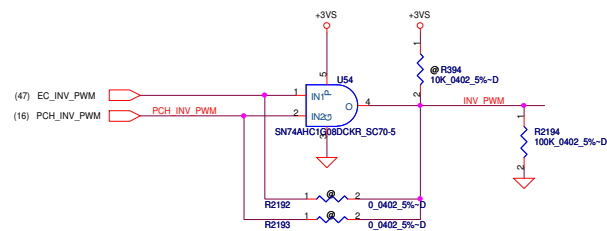
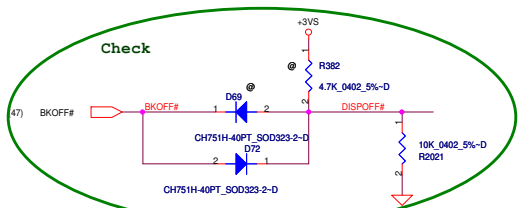
LCD POWER



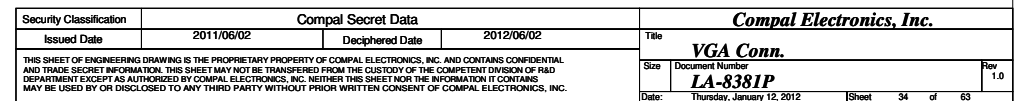
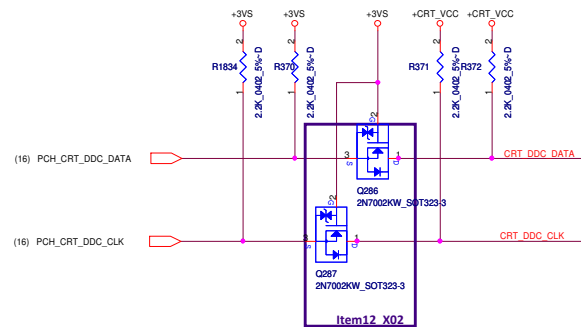
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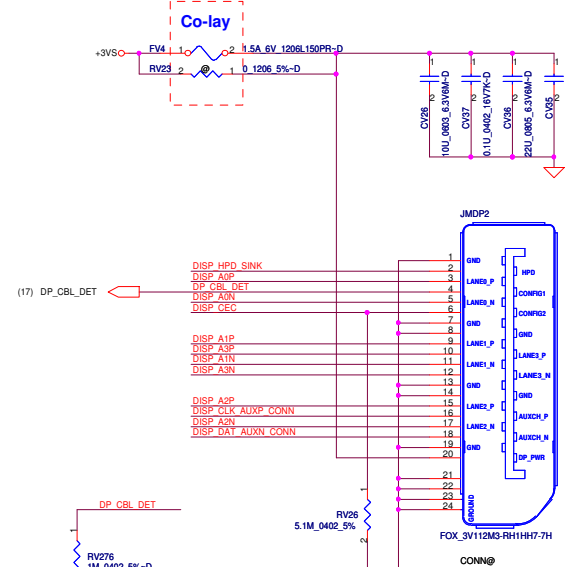
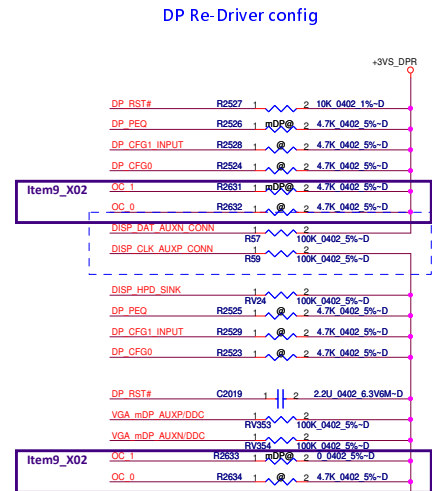
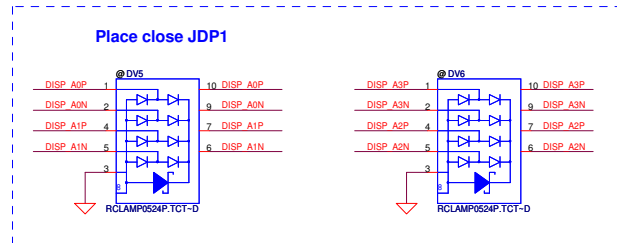
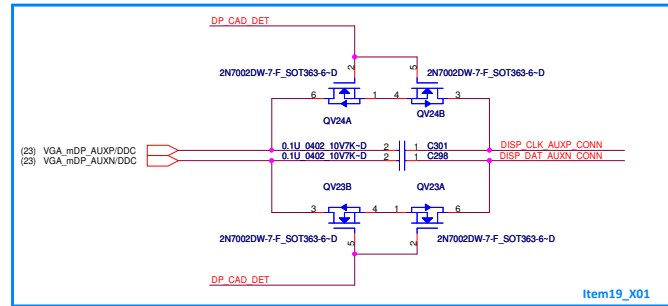
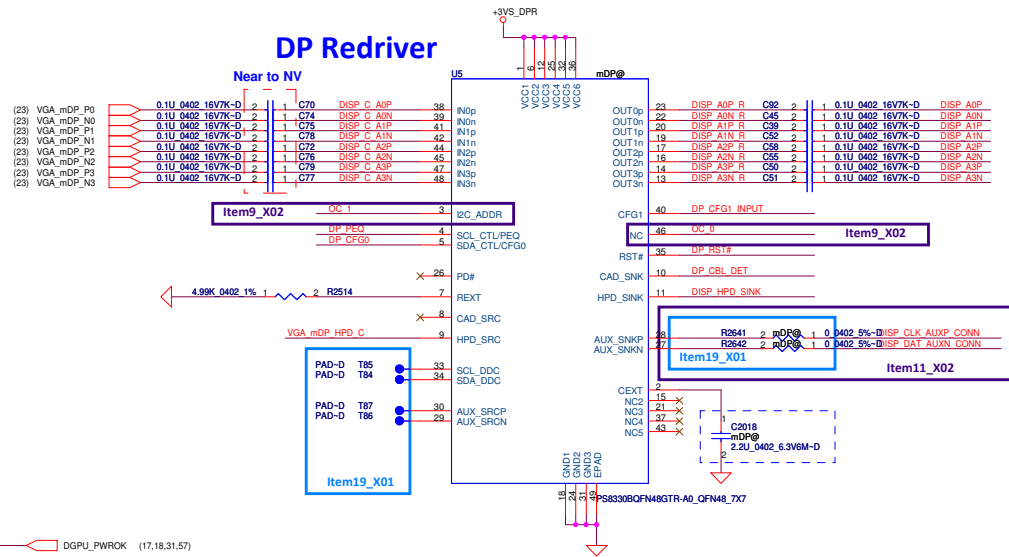
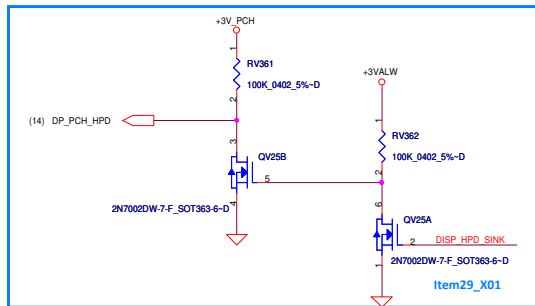
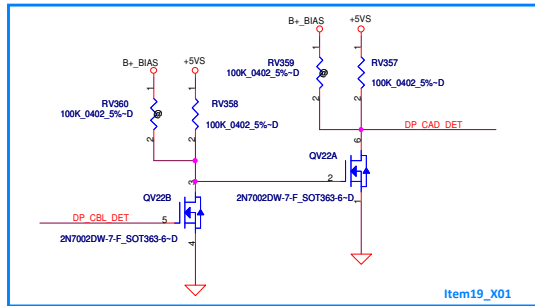
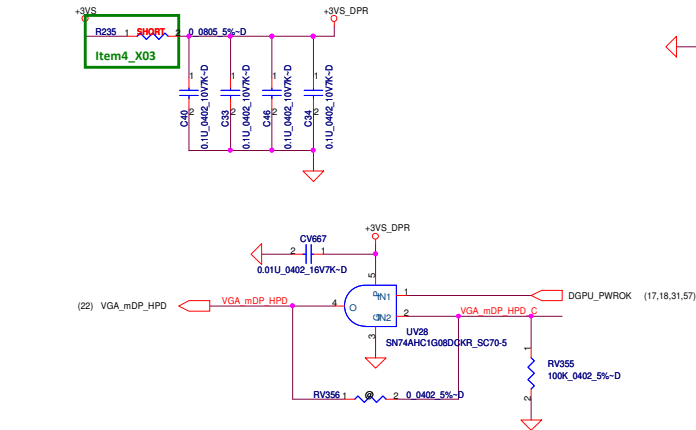


LCD Backlight Selector

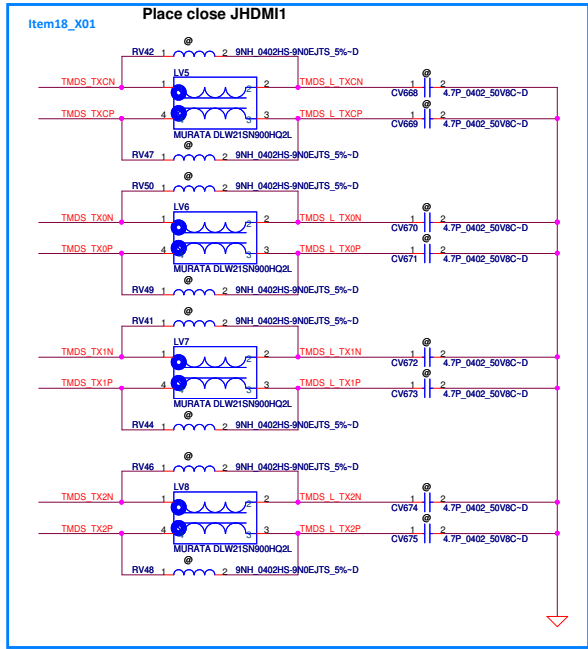
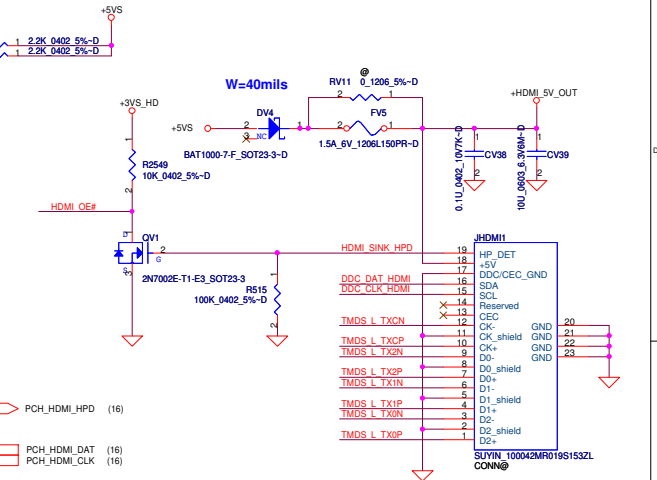
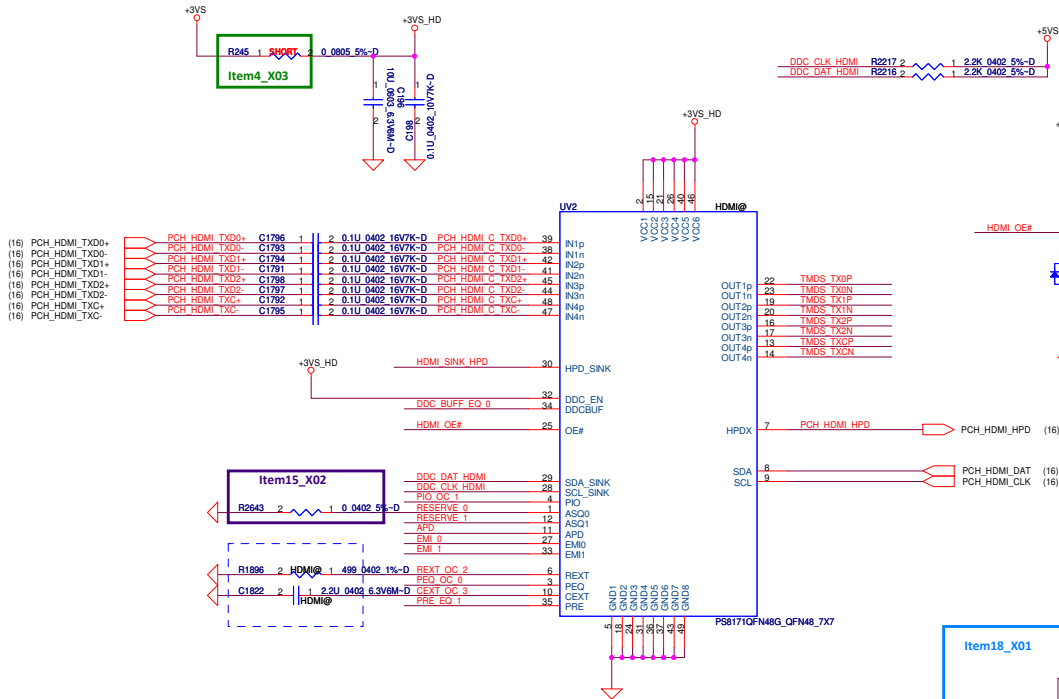
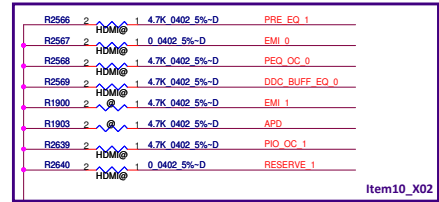
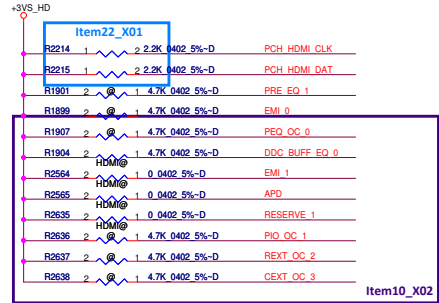


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		Size	1.0
		Date	Thursday, January 12, 2012
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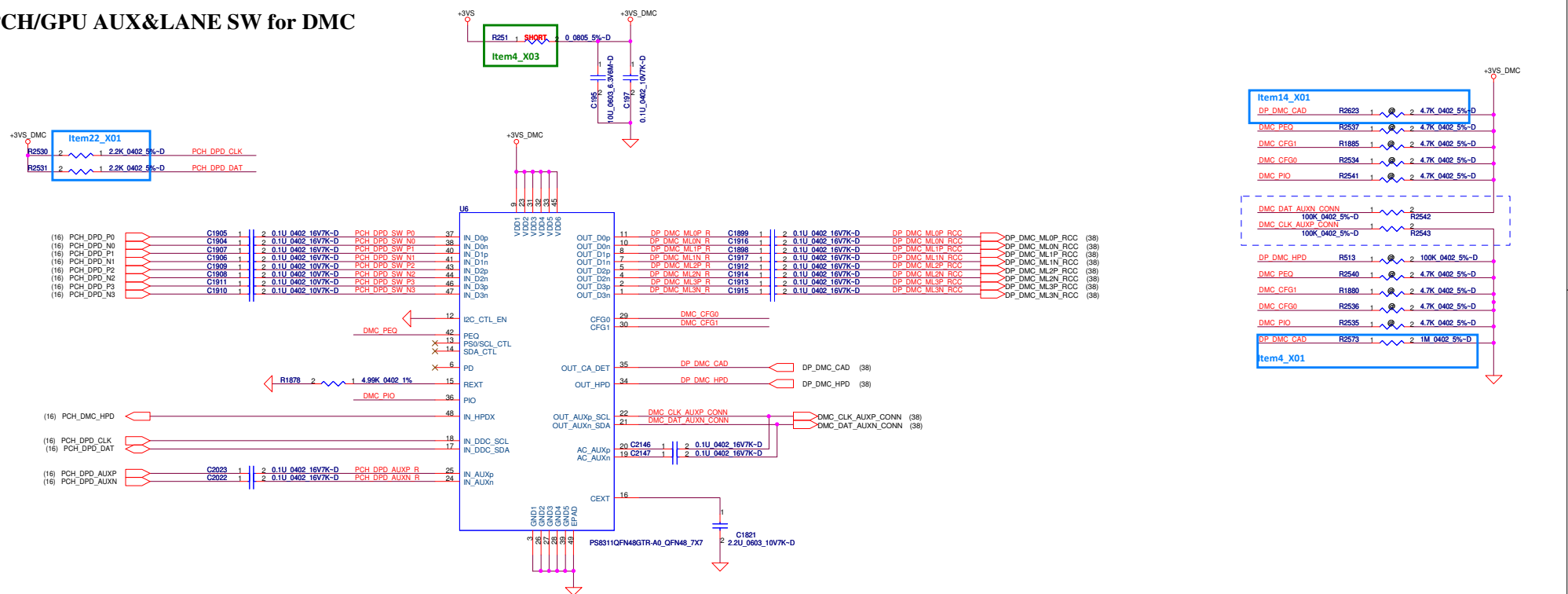




X76 BOM option table	
PARADE:	
UV2	= SA00003VV00
R1896	= SD03449908L (499 ohm)
C1822	= SE00000888L (2.2U 6.3V)
R1904	= SD02847018L (4.7K ohm)
R2635	= SD02800008L (0 ohm)
Other	= NC*
PERICOM:	
UV2	= SA000005K000
R1896	= SD02847018L (4.7K ohm)
C1822	= SD02847018L (4.7K ohm)
R2566	= SD02847018L (4.7K ohm)
R2568	= SD02847018L (4.7K ohm)
R2569	= SD02847018L (4.7K ohm)
R2639	= SD02847018L (4.7K ohm)
R2564	= SD02800008L (0 ohm)
R2565	= SD02800008L (0 ohm)
R2567	= SD02800008L (0 ohm)
R2640	= SD02800008L (0 ohm)
Other	= NC*



PCH/GPU AUX&LANE SW for DMC



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								Size C	Document Number	Rev 1.0	
								LA-8381P			
Date:		Thursday, January 12, 2012				Sheet		37	of 63		

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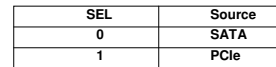
X7E BOM option table

PERICOM (PI3EQX6741):
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RS318 = SD028000008L (0 ohm)
Other = NC*

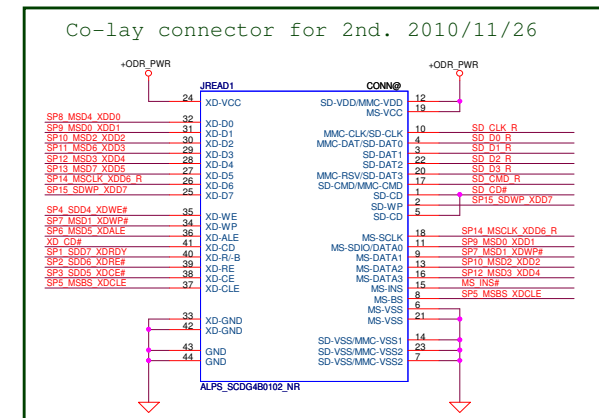
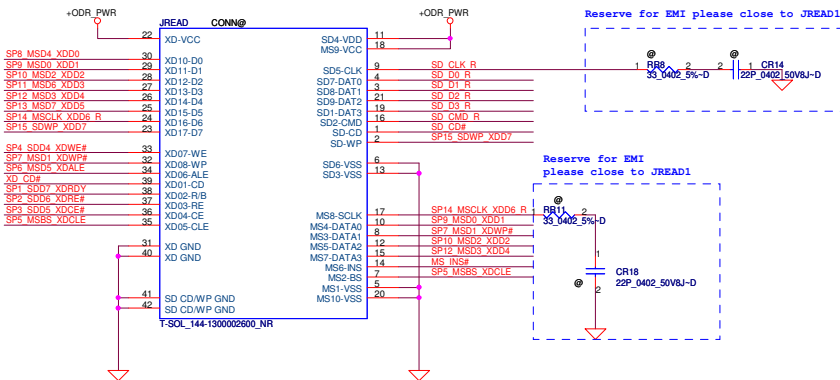
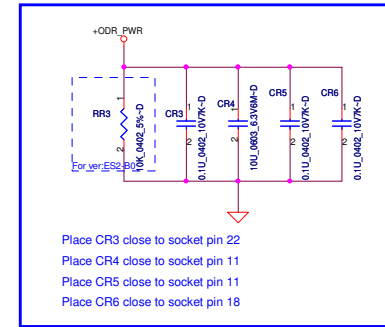
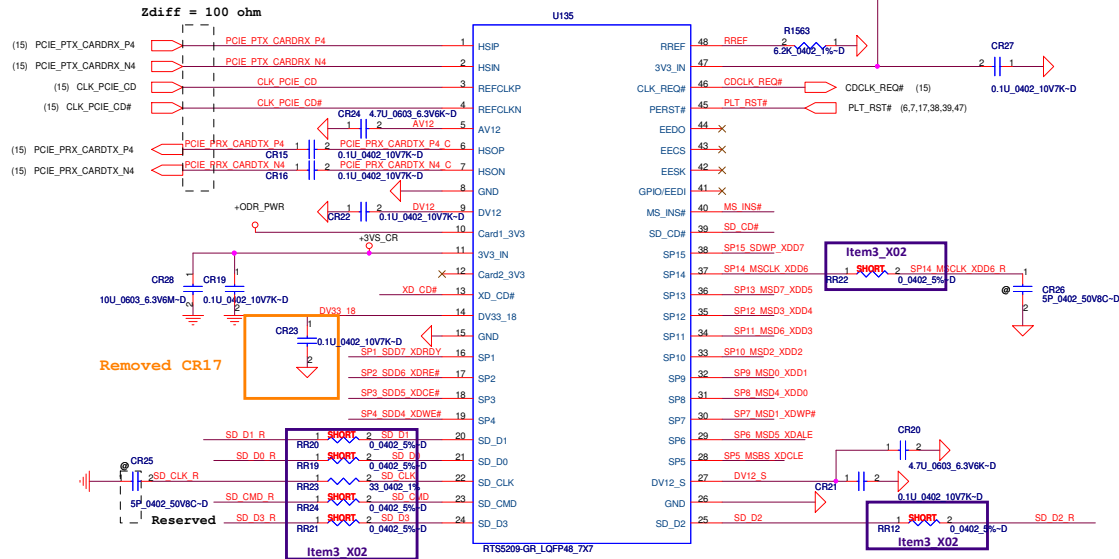
PARADE (PS8520B):
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RS317 = SD028000008L (0 ohm)
RS320 = SD028000008L (0 ohm)
RS321 = SD028000008L (0 ohm)
Other = NC*

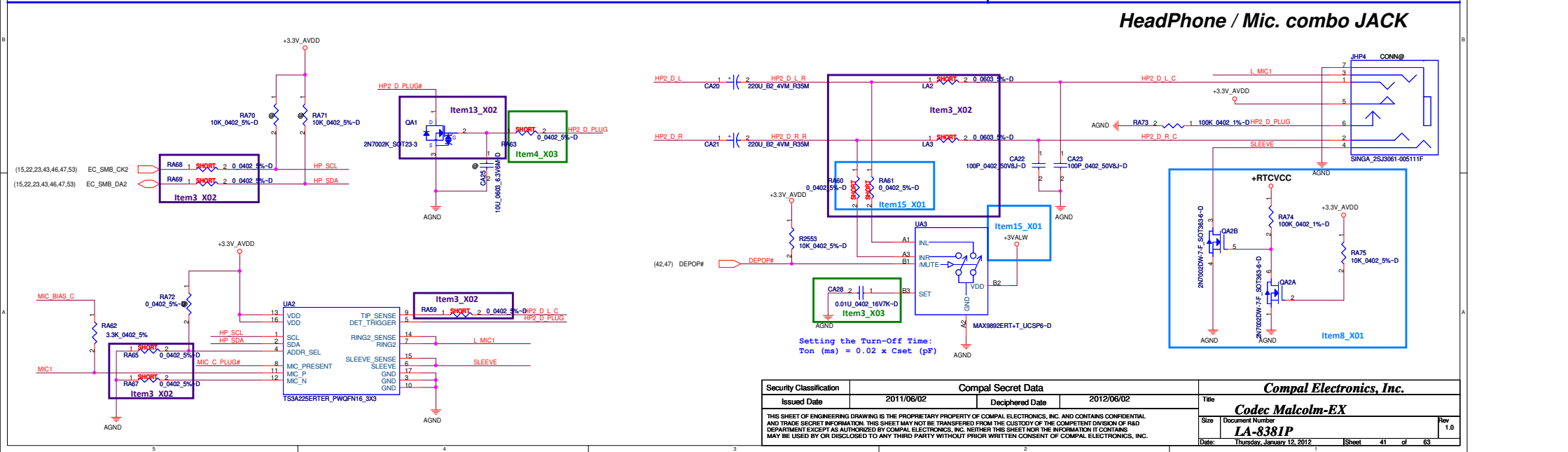
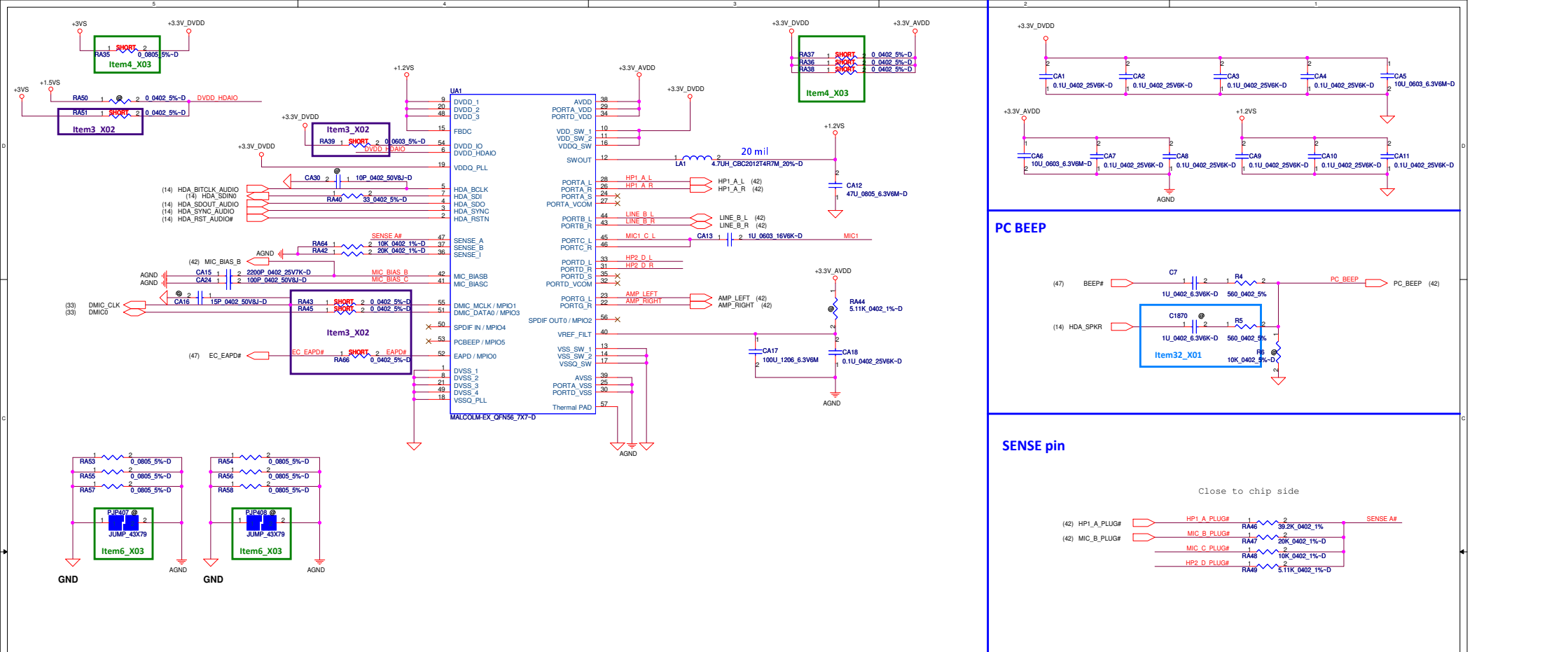
TI (SN75LVPC601RTJR):
U637 = SA00003ZX0L
RS310 = SD028000008L (0 ohm)
RS318 = SD028000008L (0 ohm)
RS320 = SD028000008L (0 ohm)
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Other = NC*

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[illegible]

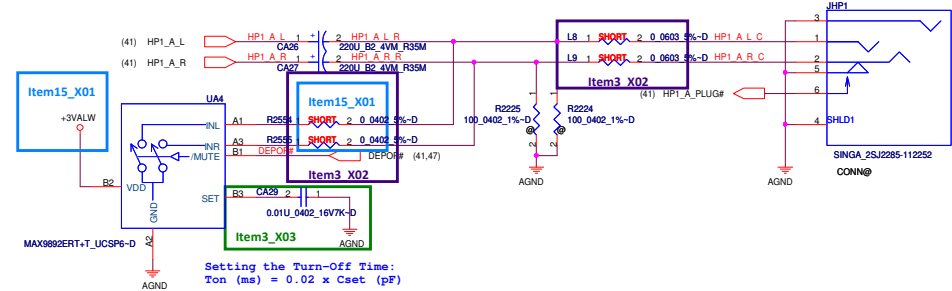
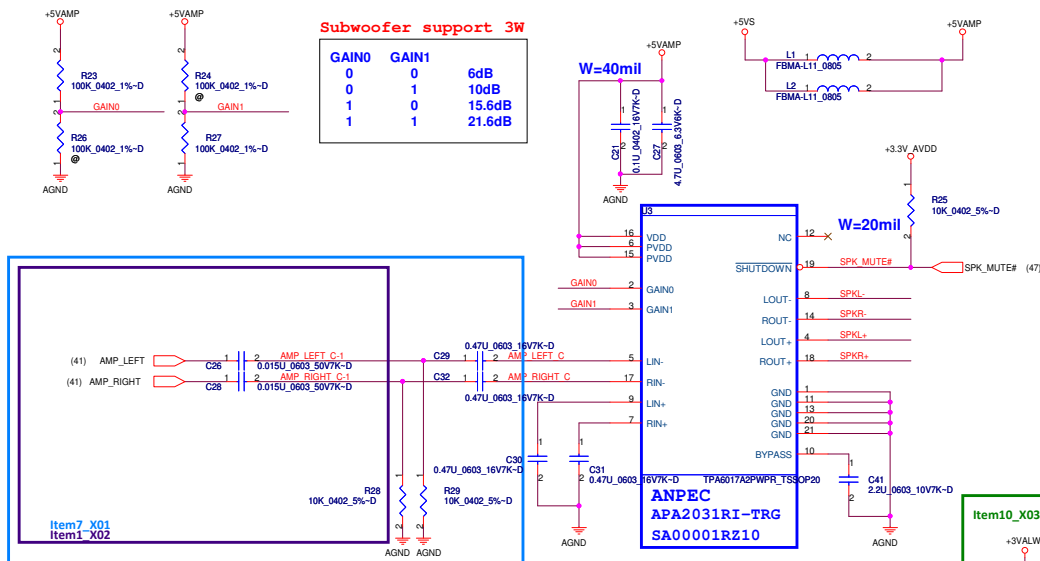
check IC support 9 in 1 function



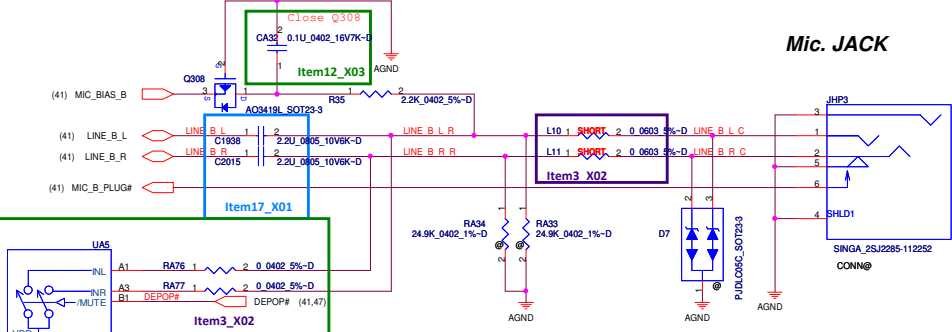


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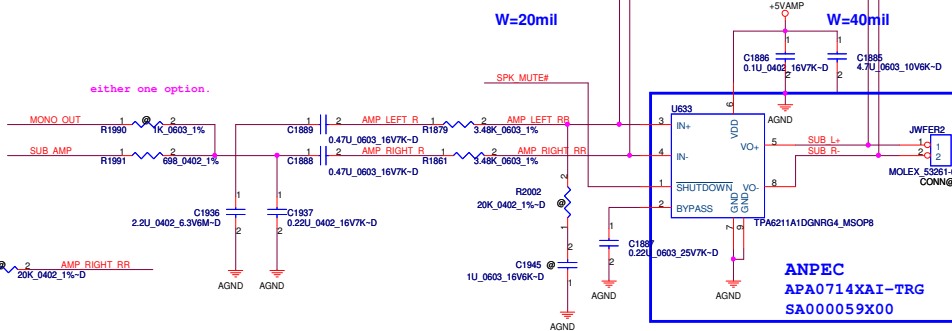
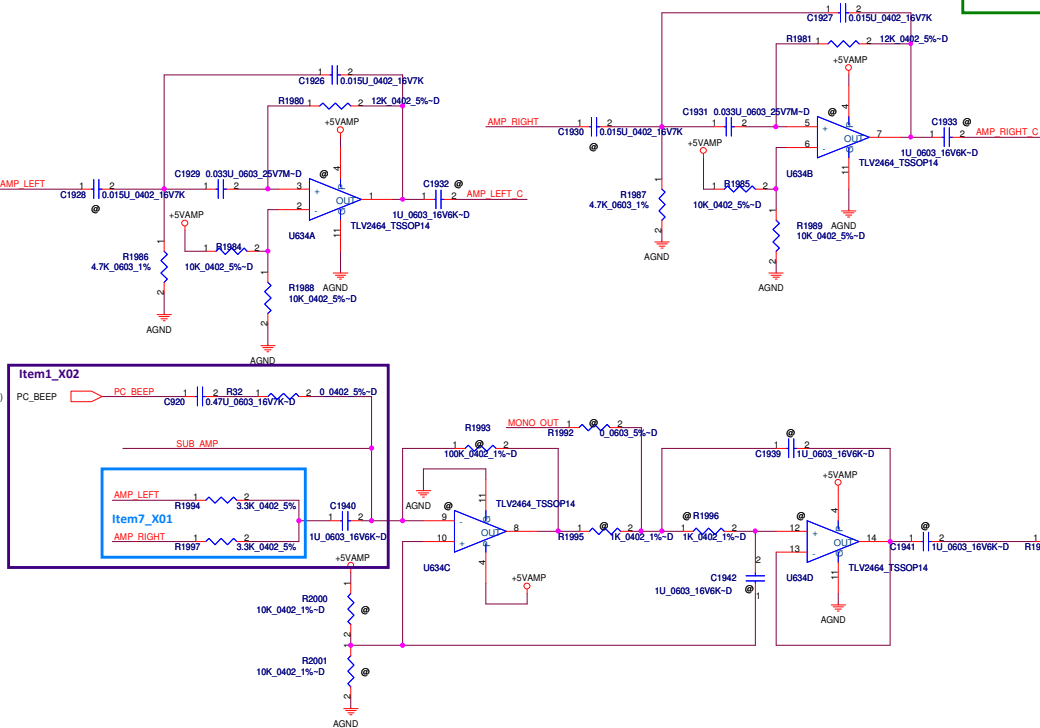
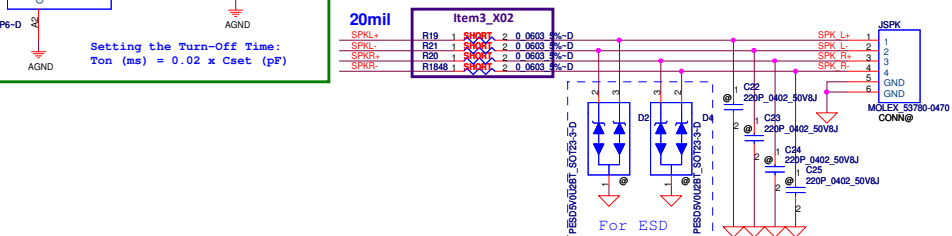
Line Out/HeadPhone



Mic. JACK



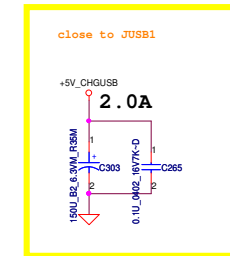
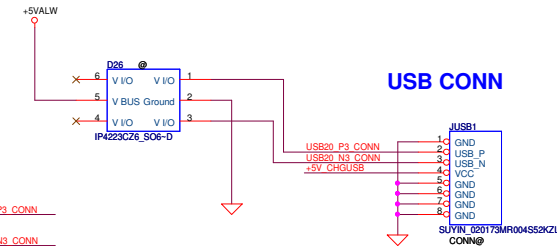
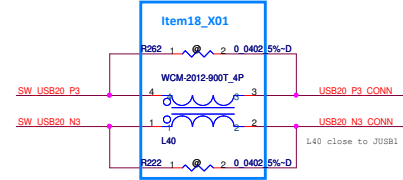
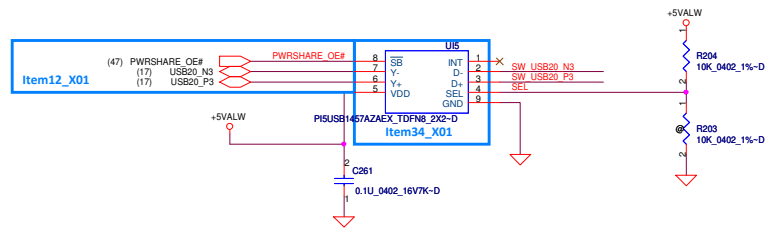
Int. Speaker Connector



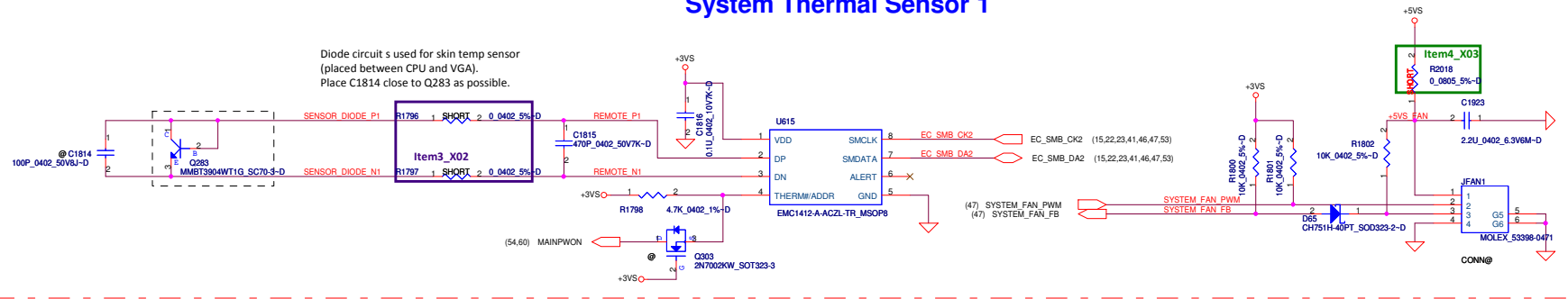
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Power share

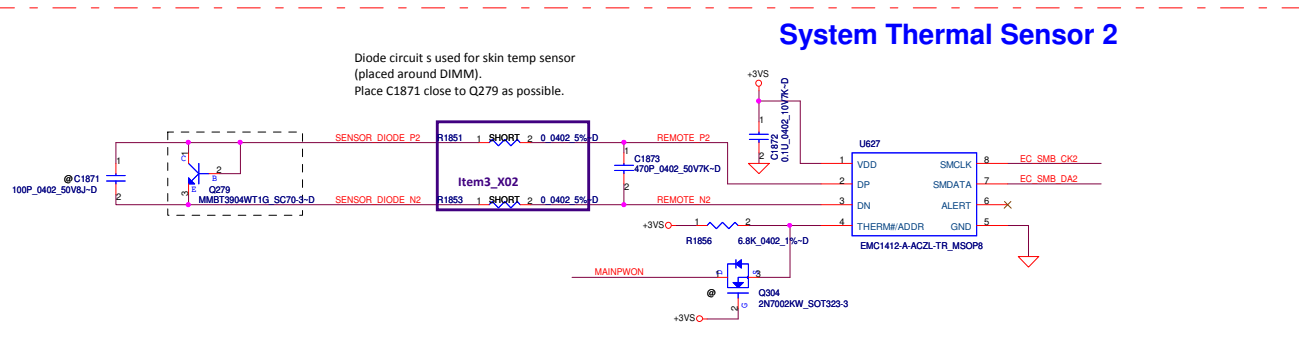
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM



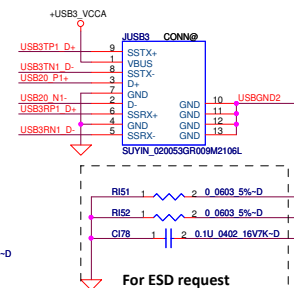
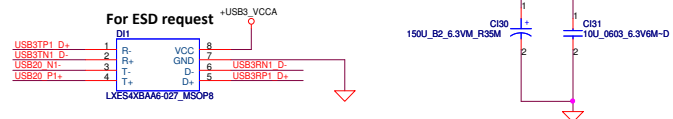
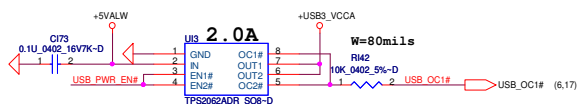
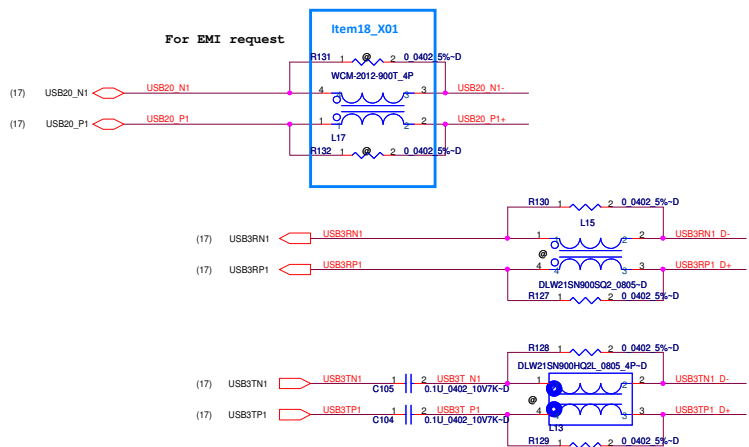
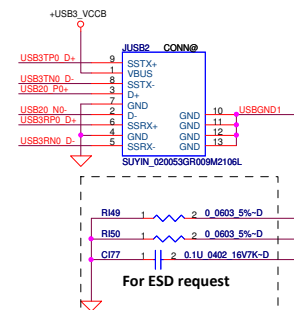
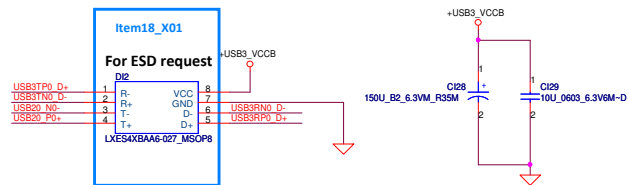
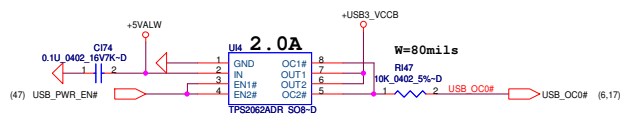
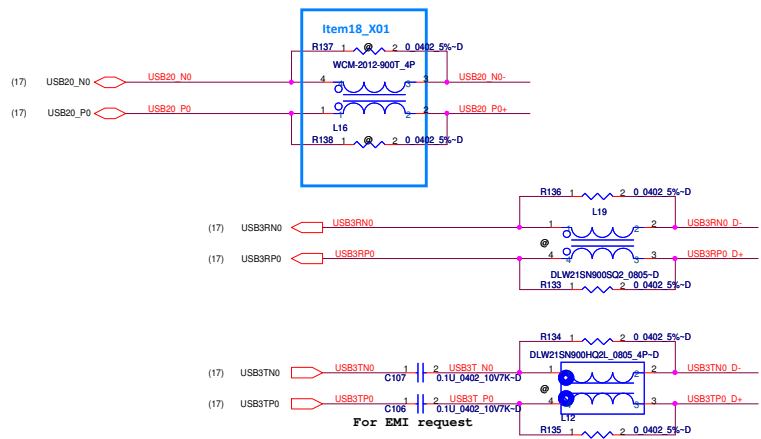
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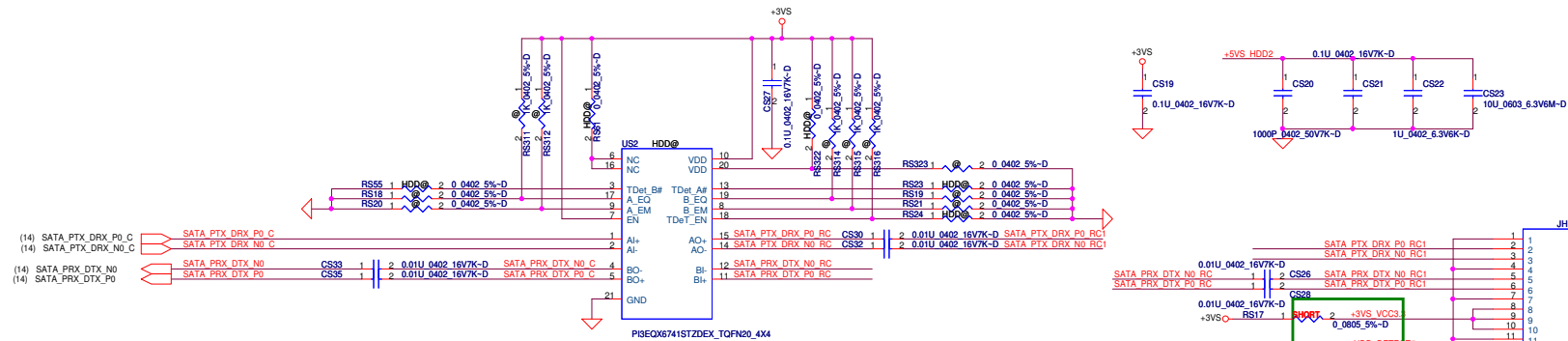
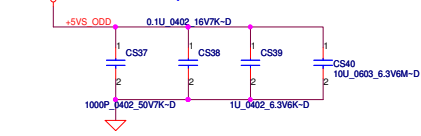
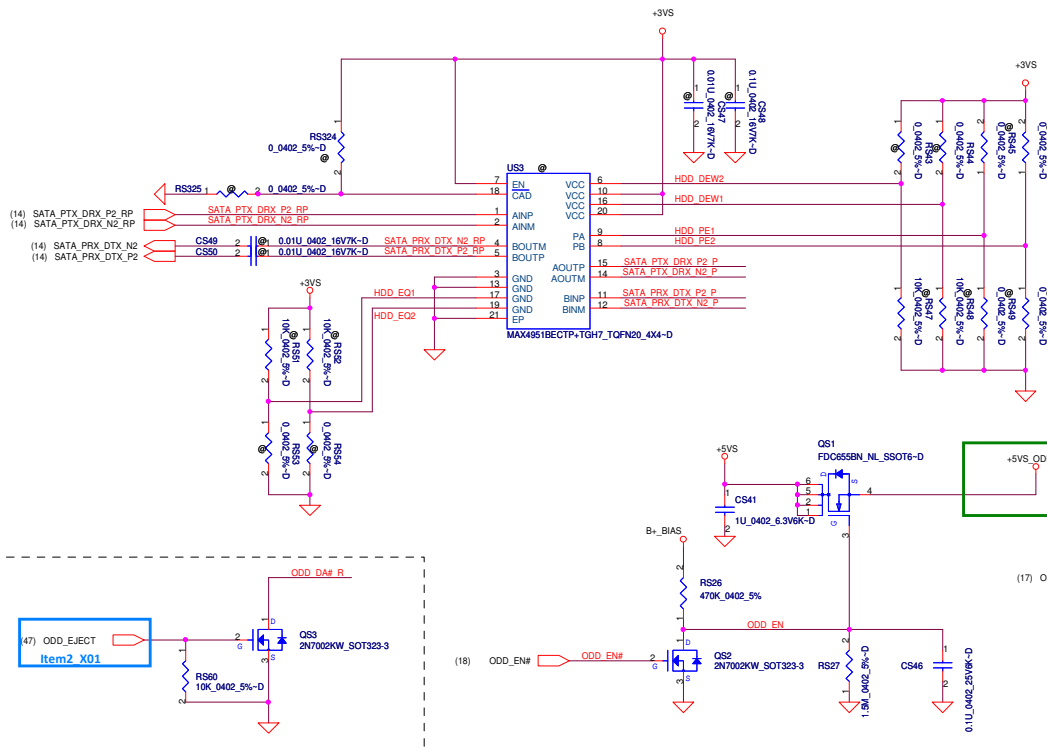


System Thermal Sensor 2

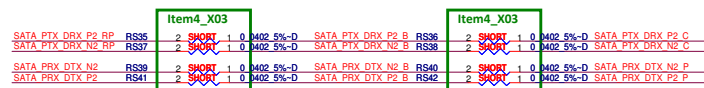


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[illegible]

	MAXIM _{main}	TI _{2nd}
P/N	SA00003LH1L	SA00003ZX0L
RS43 RS44	pop	depop
RS47 RS48	depop	pop
RS53 RS54	pop	depop

[illegible]

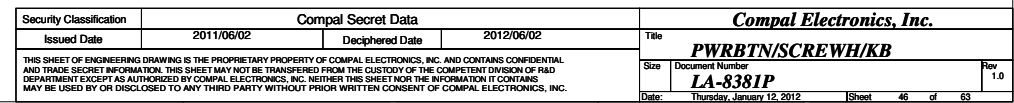
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						Size	Document Number				Rev 1.
						LA-8381P					
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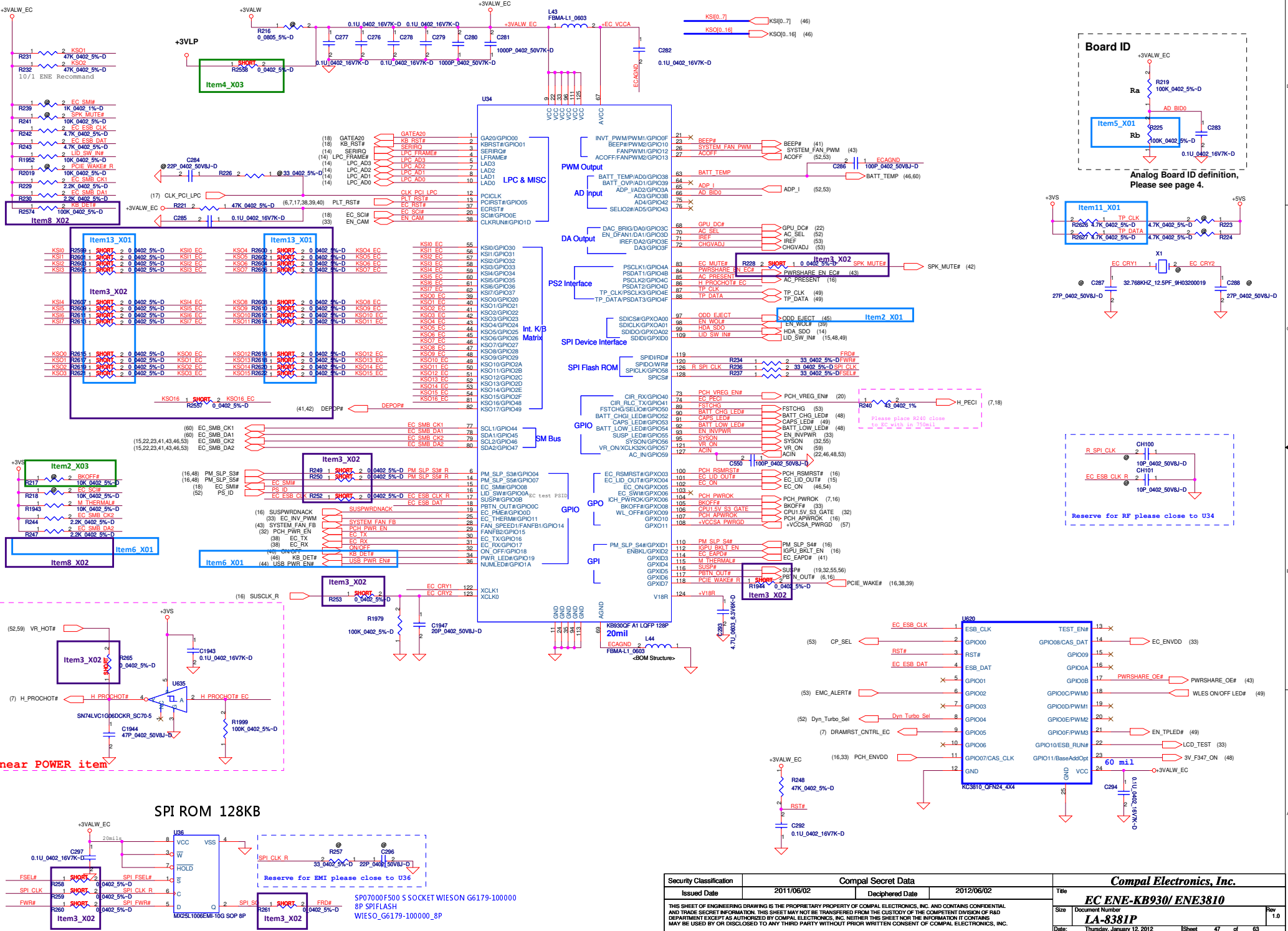
Power Button



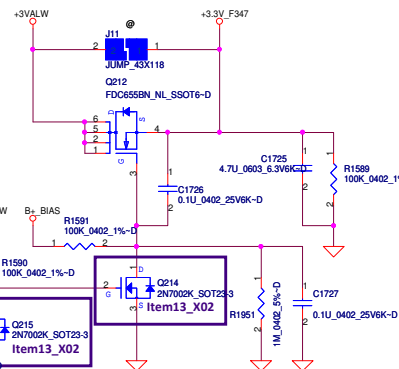
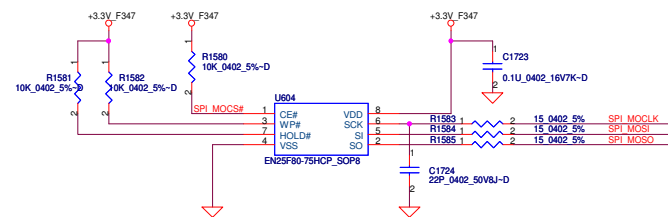
K/B Backlight CONN (co-lay VPK)

- 1, Analog keys connector and F/P temporary use.
- 2, check pin assignment.
- 3, check VPK K/B layout.





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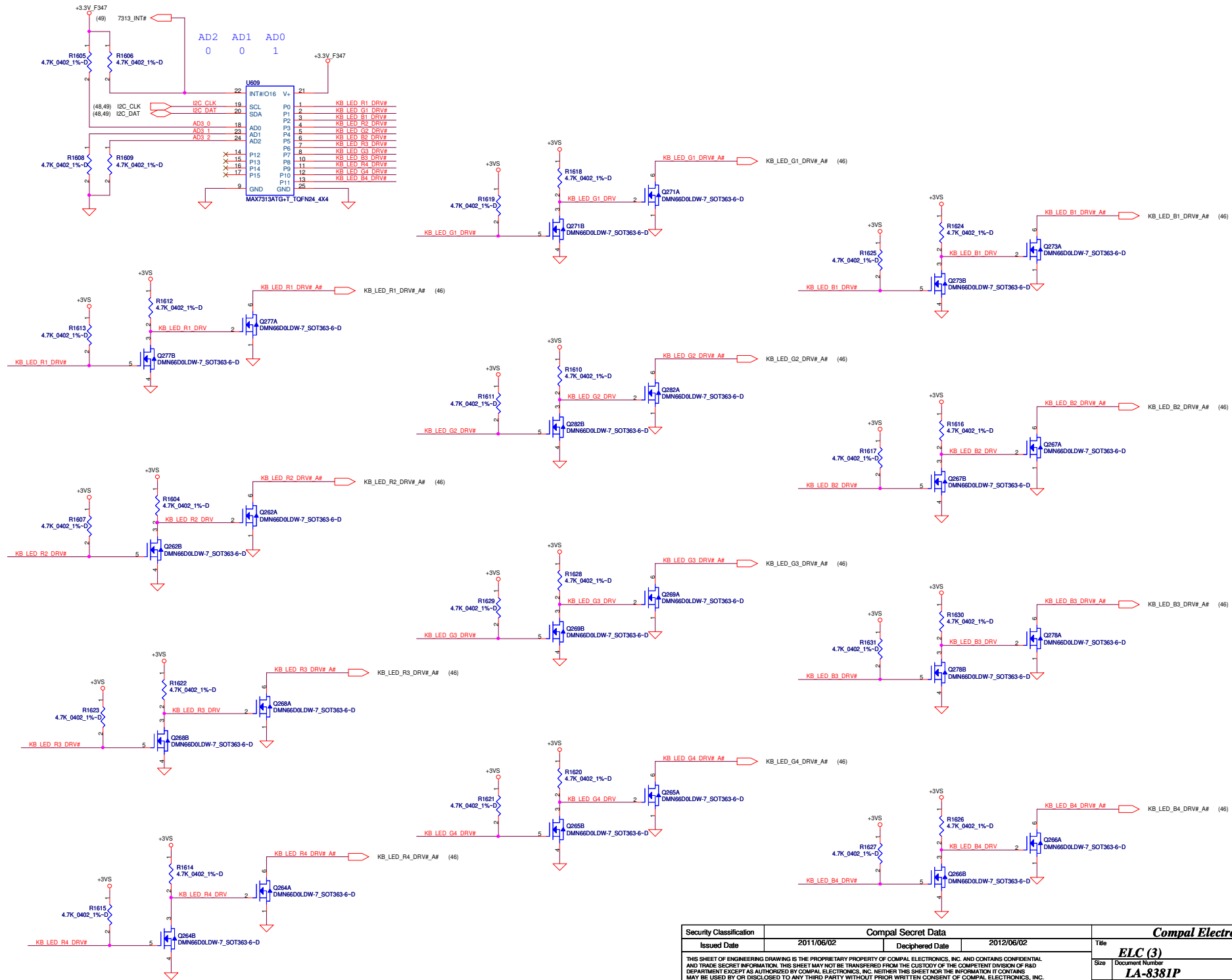


	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

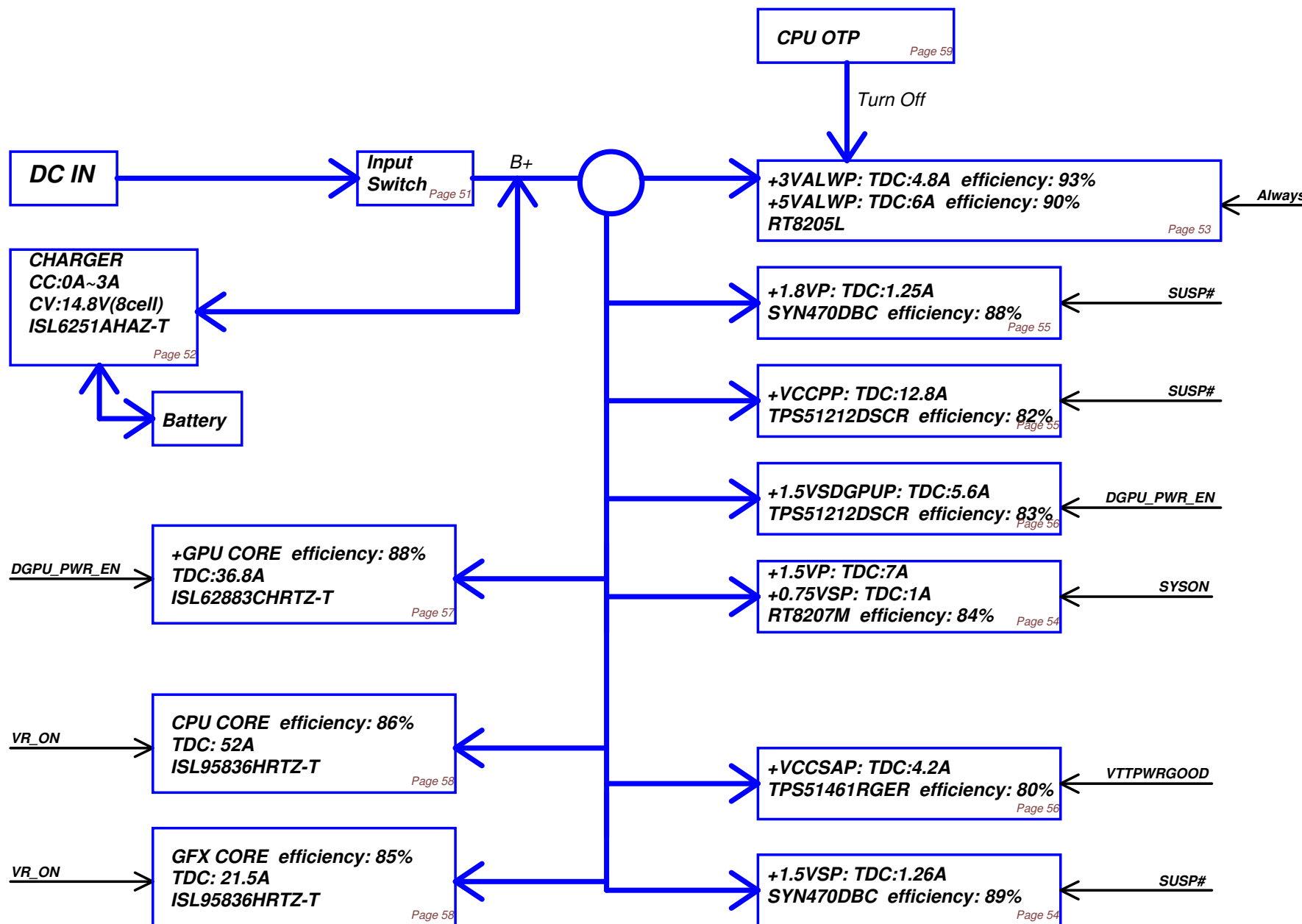
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

K/B Backlight



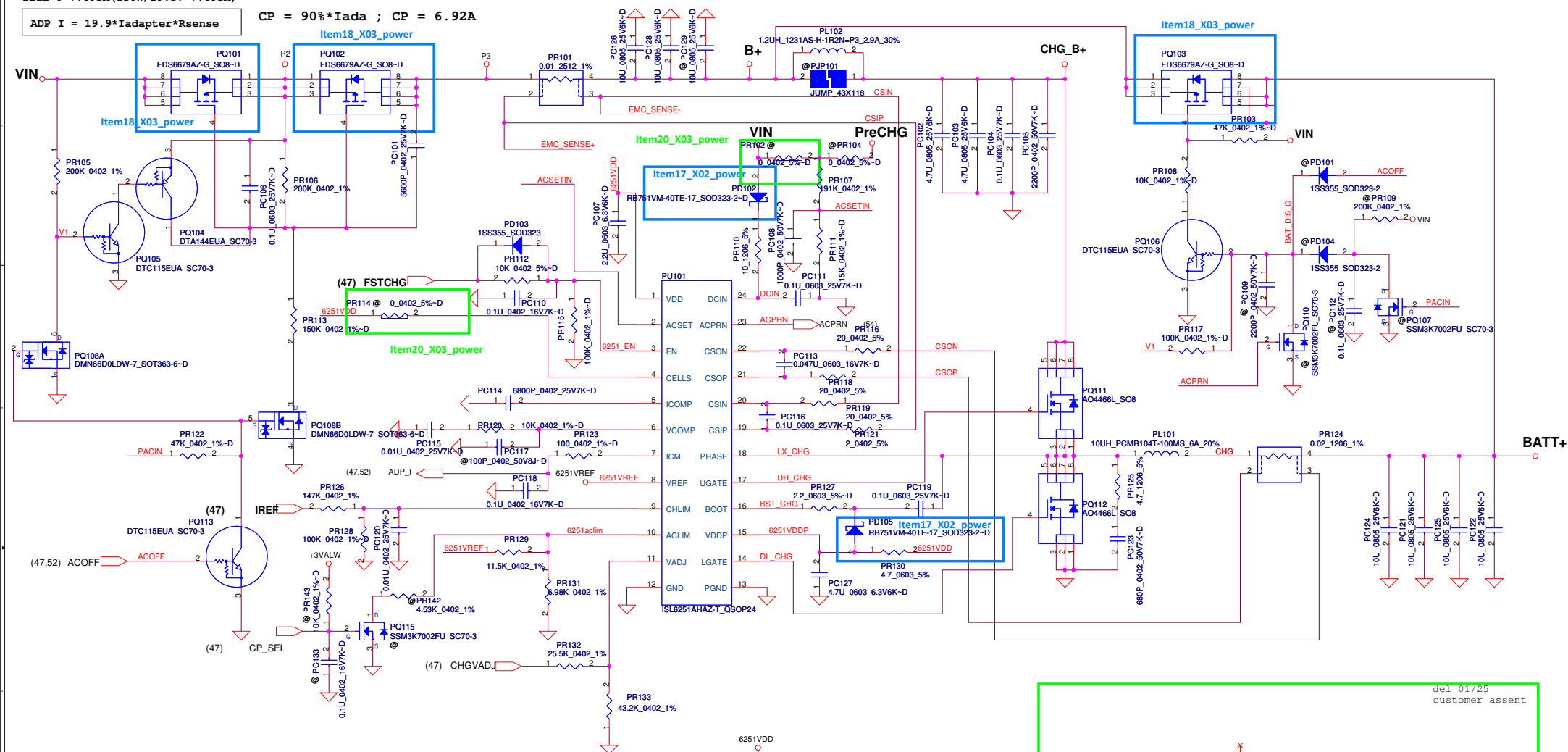
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				Size Document Number
				LA-8381P
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Power block



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title	POWER BLOCK DIAGRAM	
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				Date:	Thursday, January 12, 2012	Sheet 51 of 63

$I_{ada}=0\sim 7.693A(150W/19.5V=7.693A)$

$$\text{ADP I} = 19.9 \cdot \text{Iadapter} \cdot \text{Rsense}$$
$$CP = 90\% \cdot I_{ada} ; CP = 6.92A$$


CP mode

```
Iinput=(1/0.02) (0.05*Vaclm/2.39+0.05)
Vaclim=2.39* ((6.98K/152K)/(11.5K/152K)+(6.98K/152K))
```

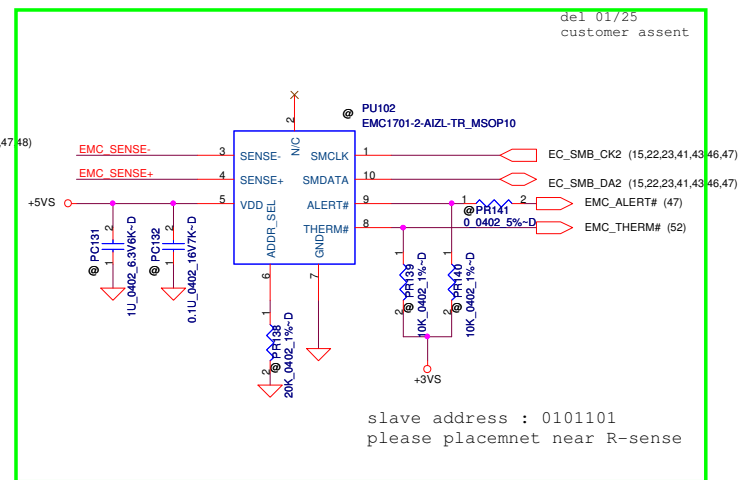
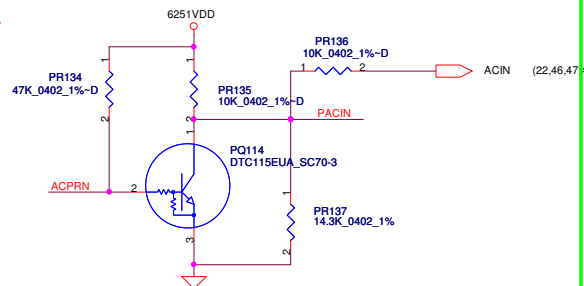
CC=3.3A

IREF=1*Icharge

IREF=0.25V~3.3V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 4S LI-ON Cells	14800mV	14.80V

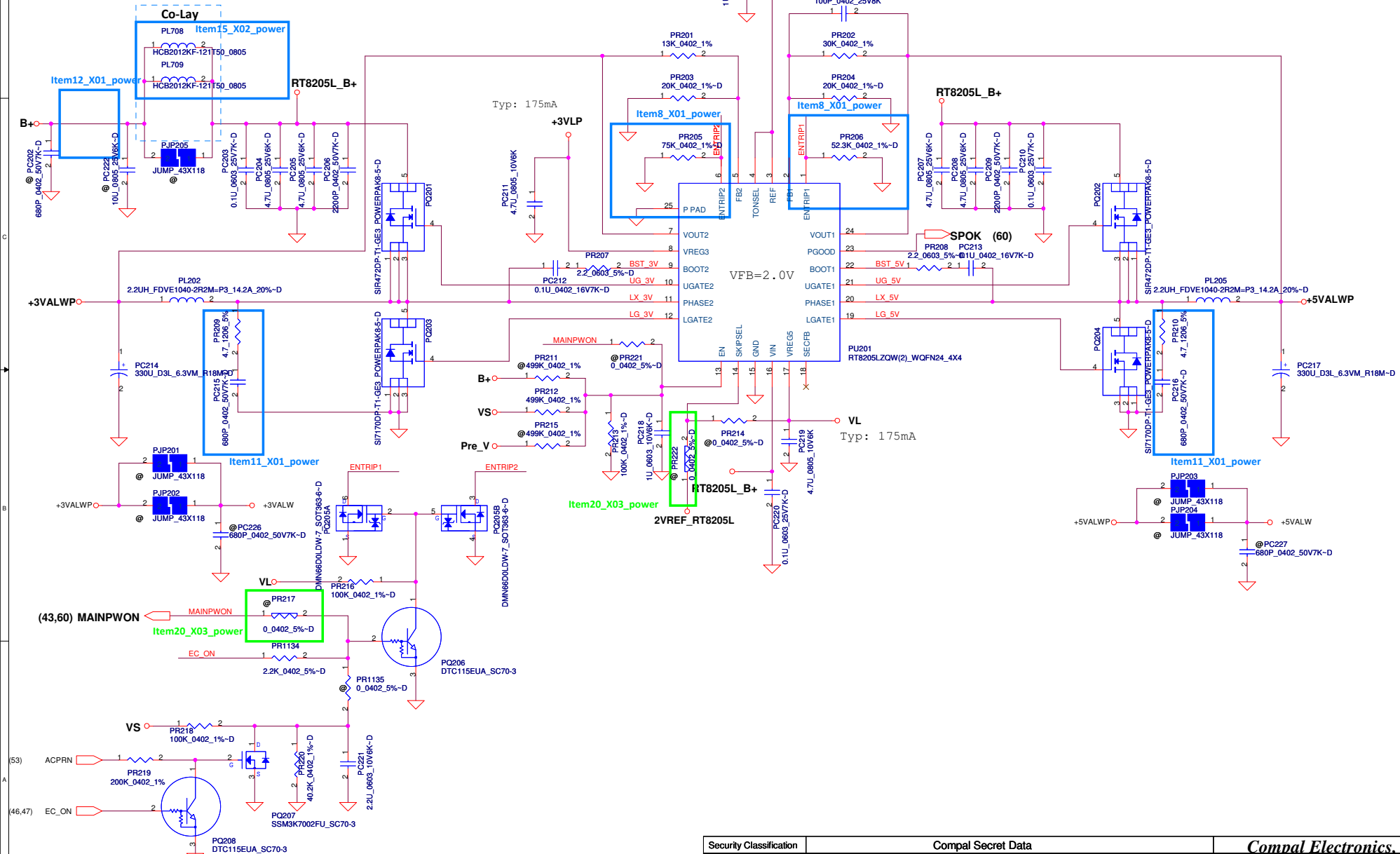
CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell



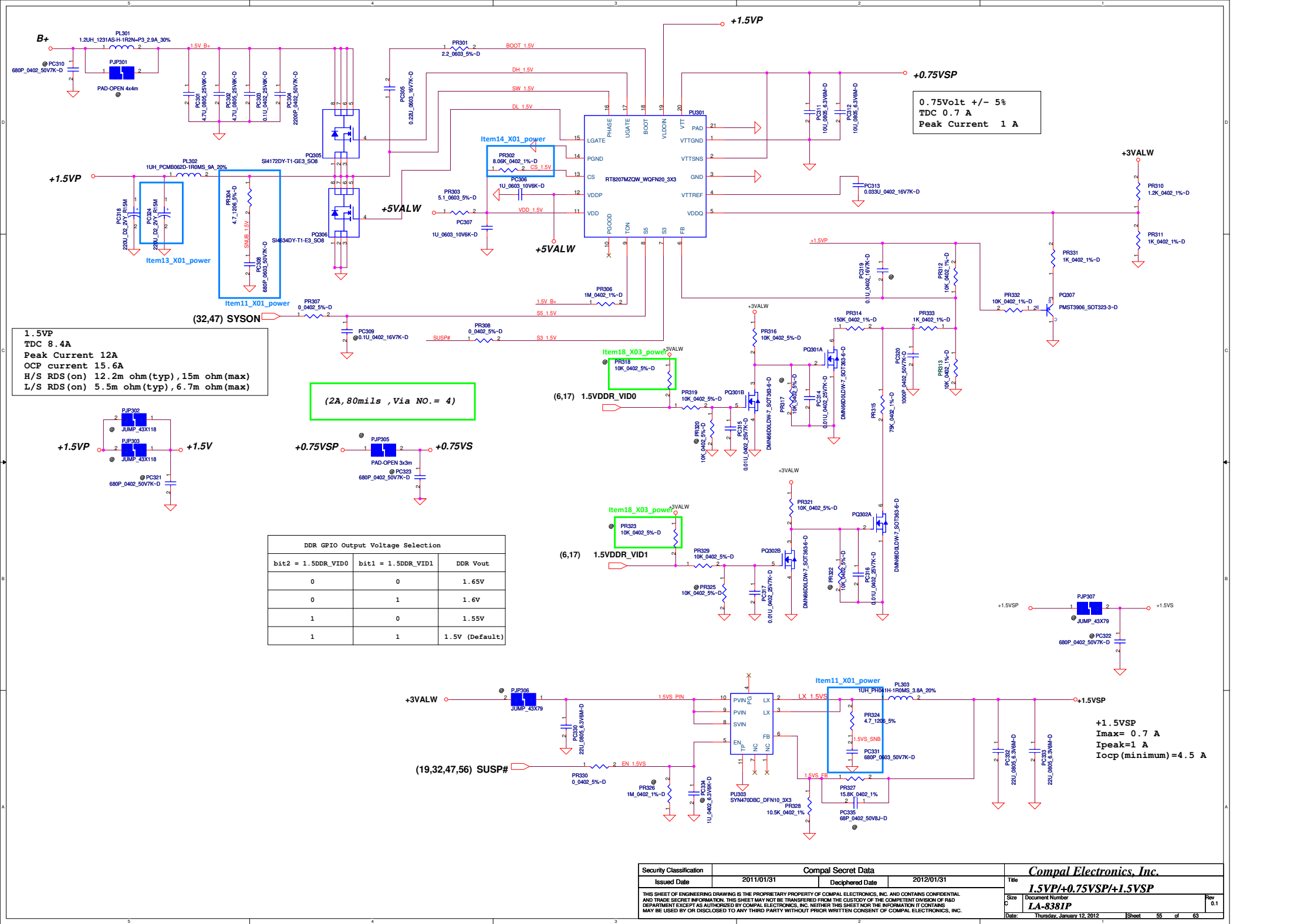
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR-CHARGER		
Issued Date	2011/01/31	Deciphered Date	2012/01/31	Title		
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				Custodian	LA-8381P	1.
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3.3VALWP
TDC 11.09A
Peak Current 15.84A
OCP current 20.3A
H/S RDS(on) 12.2m ohm(typ), 15m ohm(max)
L/S RDS(on) 3.6m ohm(typ), 4.5m ohm(max)

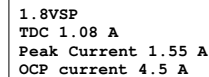
5VALWP
TDC 8.43A
Peak Current 12.05A
OCP current 15.6A
H/S RDS(on) 12.2m ohm(typ), 15m ohm(max)
L/S RDS(on) 3.6m ohm(typ), 4.5m ohm(max)



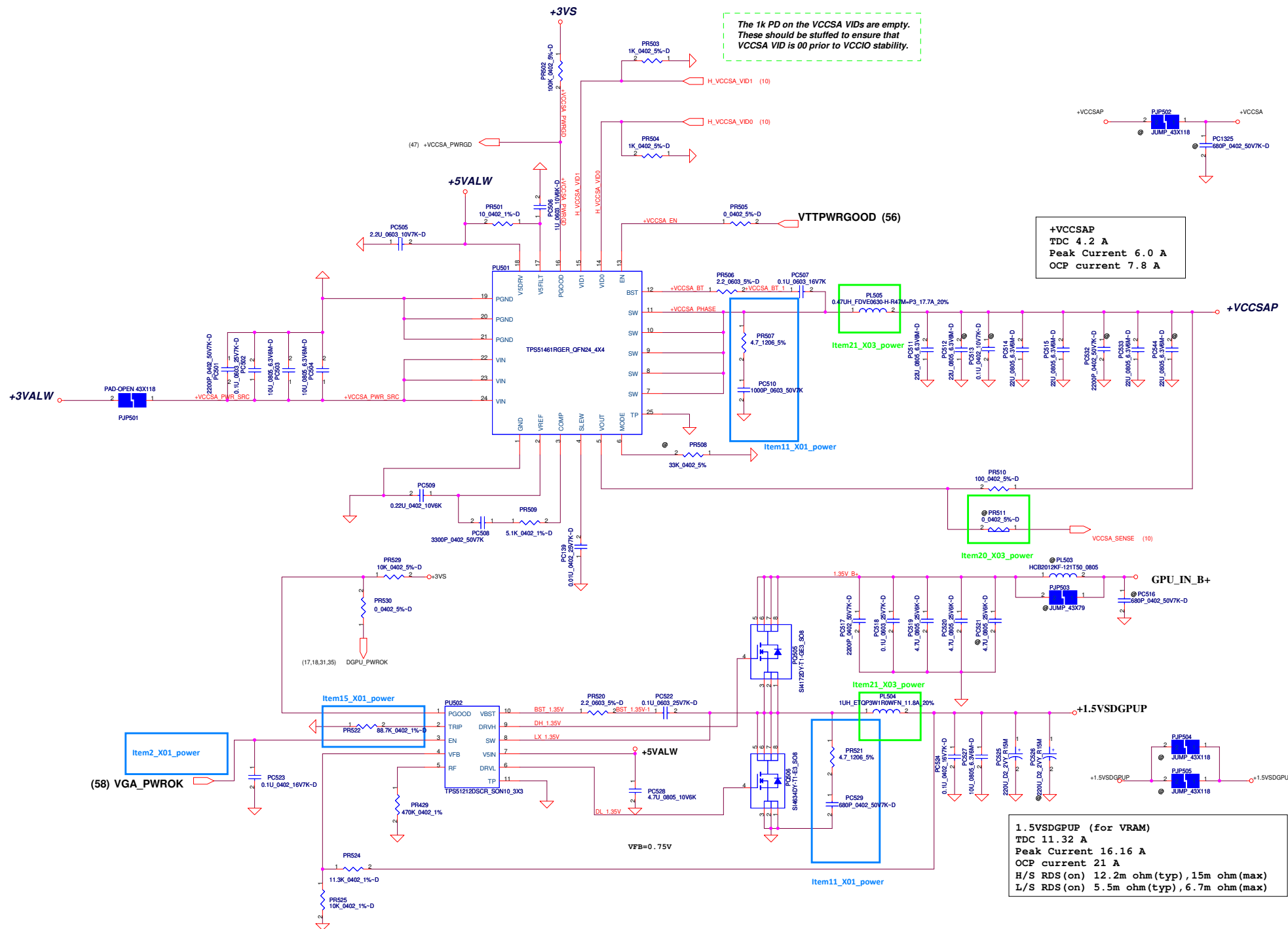
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> 3VALWP/SVALWP	
Issued Date	2011/01/31	Deciphered Date	2012/01/31	Title	
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				Document Number	0.1
				LA-8381P	
Date	Thursday, January 12, 2012	Sheet	54	of	63



Due to remove VENTURA fun,
so delete PR401.

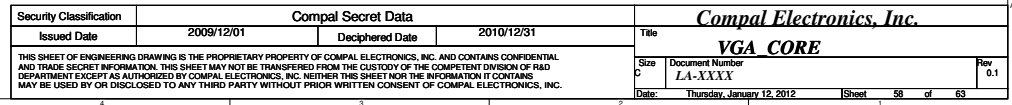


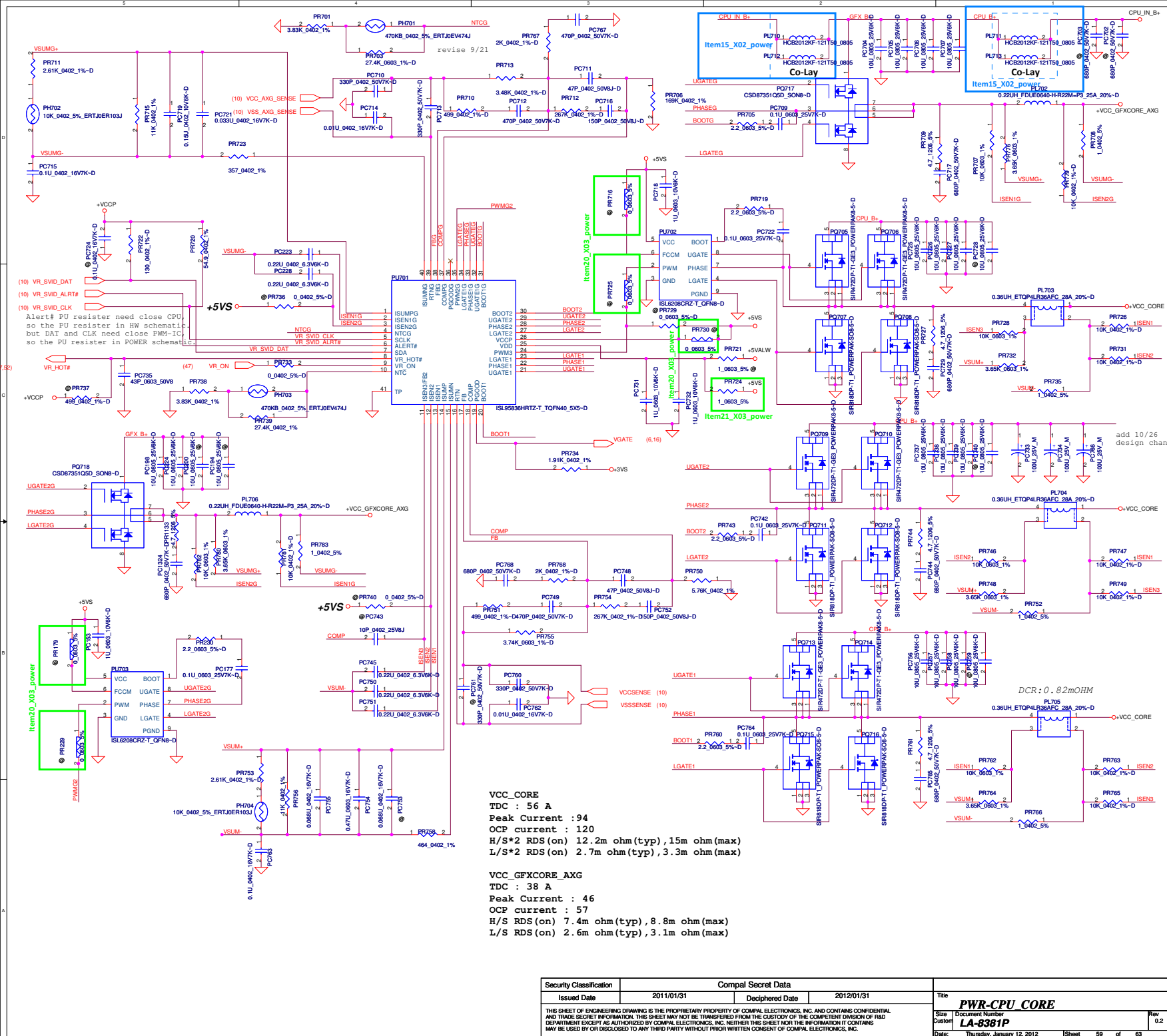
Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> PWR+VCCPP/+1.8VSP		
Issued Date	2011/01/31	Deciphered Date	2012/01/31	Title	PWR+VCCPP/+1.8VSP	
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Issued Date	2011/01/31	Deciphered Date	2012/01/31	Title
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L/S*2 RDS(on) 2.7m ohm(typ), 3.3m ohm(max)

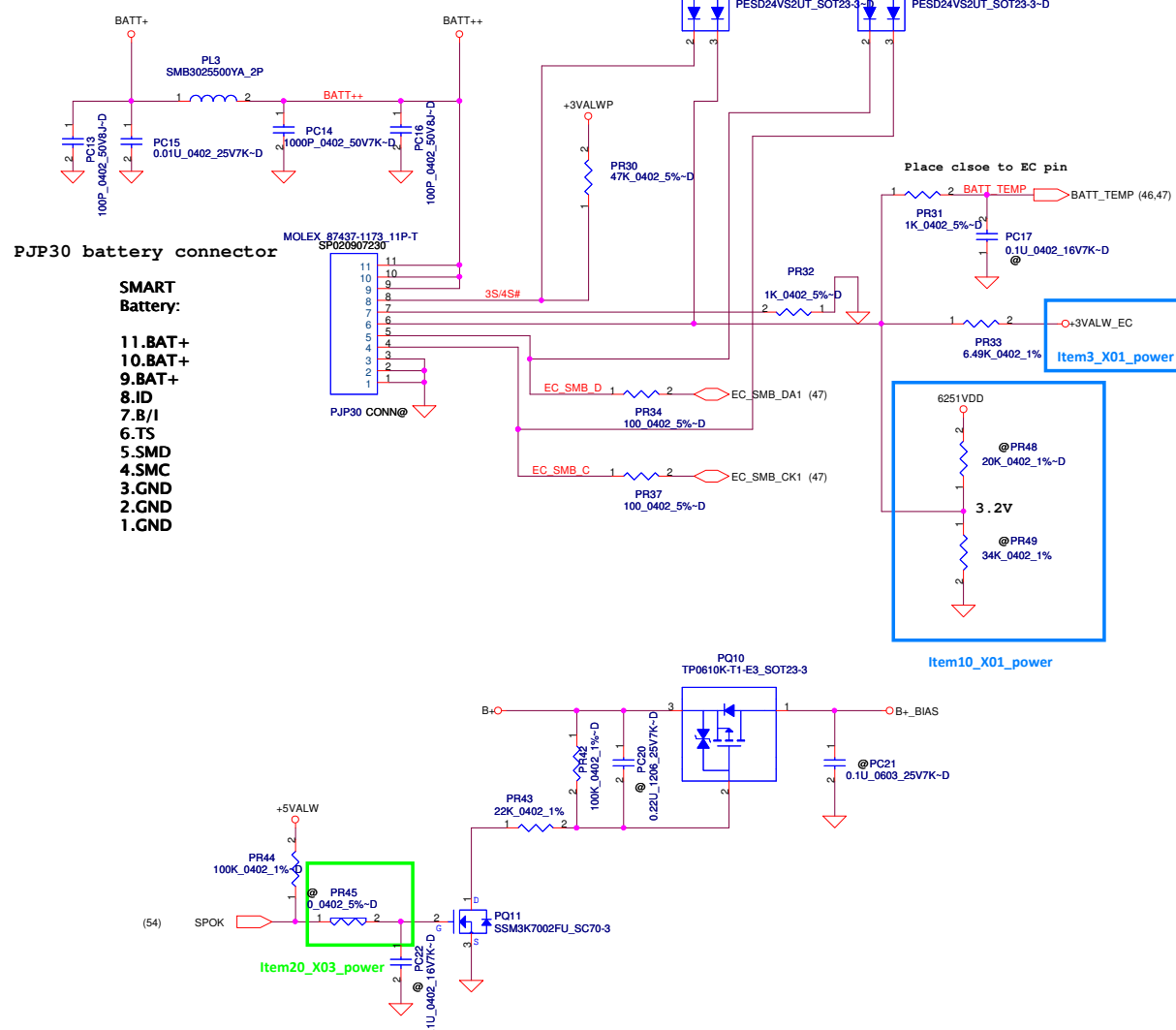




VCC_CORE
TDC : 56 A
Peak Current : 94
OCP current : 120
H/S*2 RDS(on) 12.2m ohm (typ), 15m ohm (max)
L/S*2 RDS(on) 2.7m ohm (typ), 3.3m ohm (max)

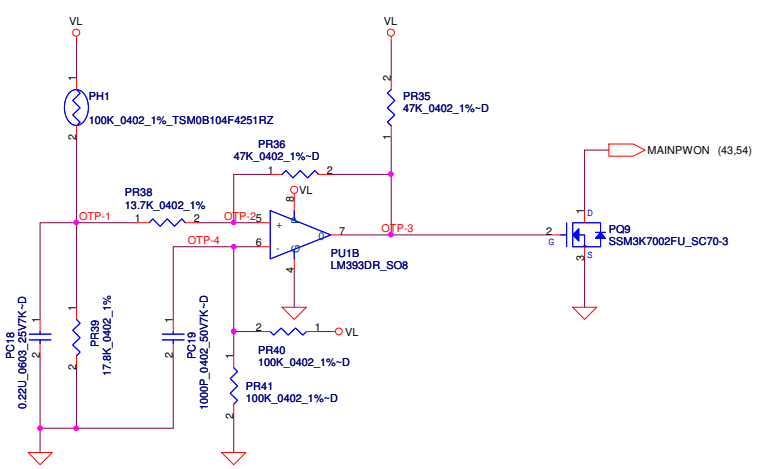
VCC_GFXCORE_AXG
TDC : 38 A
Peak Current : 46
OCP current : 57
H/S RDS(on) 7.4m ohm (typ), 8.8m ohm (max)
L/S RDS(on) 2.6m ohm (typ), 3.1m ohm (max)

Security Classification		Compal Secret Data				
Issued Date		2011/01/31	Deciphered Date		2012/01/31	Title
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Size	Document Number	Date: Thursday, January 12, 2012				Rev 0.2
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Battery Connect/OTP

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	61	PROCESSOR DECOUPLIN	11/09/9	COMPAL	Based on NVIDA check data to reduce VGA cap Q'ty	Remove PC1290-PC1293, PC1310,PC1312, PC1316.	0.1
2	55					Add PC1322, PC1323	0.1
3	58	+VGA_CORE	11/09/9	COMPAL	EE request	Add H_DPRS LPVR module port	0.1
4	51						
5	50						
6	54						
7	51						
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