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22	ICH8-M(GND) 5/5			57	DCIN				
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24	EC (P8763)			59	DDR2PWR(+1_8/+0_9V_S3_SUS)				
25	EC (KB3910S)			60	VHCORE(ISL6262A)				
26	Flash ROM XBUS/SPI			61	VGA POWER(GMCH)				
27	Mini Card			62	SYSPWR(+1_5VRUN/+1_05VRUN)				
28	FAN/HWM/HW THERMAL PROTECT			63	HDD PWR (+12VRUN)				
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35	LAN (1/2)								

BOM OPTION

COMPONENT	WINBOND	ENE
C72,RP9	NC	STUFF
COMPONENT	Samsung	Qimonda
R26	Stuff	NC
R39	NC	Stuff

PCB P/N: __-_____-__SA
__-_____-__SA
__-_____-__SA

Project Code & Schematics Subject: M630/M640 Main Board

	M630GM	M630PM	M640GM	M640PM
CR_	V		V	
NV_		V		V
NC_	V	V	V	V
Exclude "M640_"	V	V		

P. Leader	Check by	Design by

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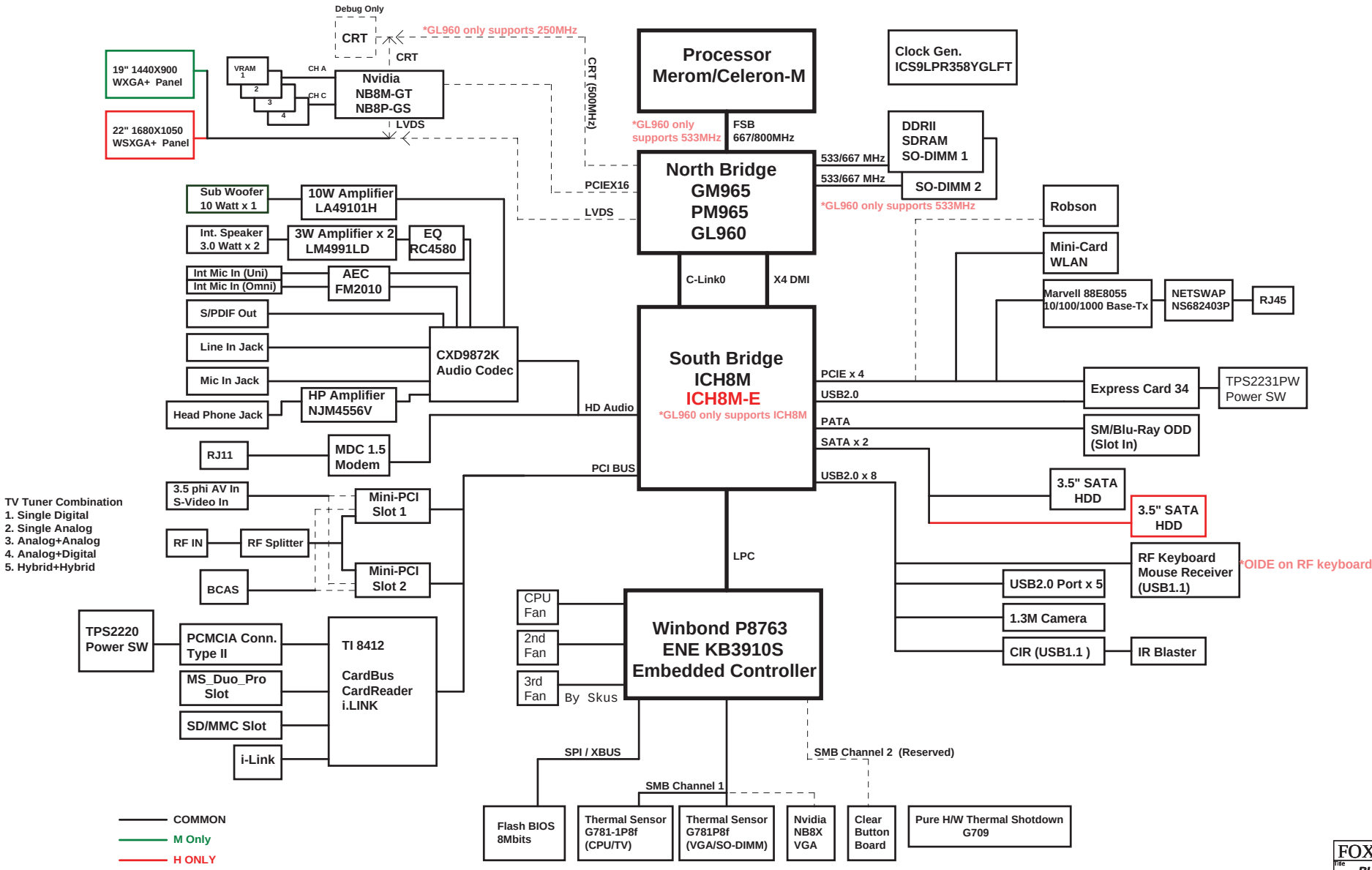
M630/640 Block Diagram (19"/22" Wide Screen)



SYSTEM DC/DC MAX8734A P.57

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC SC339 P.61

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_5VRUN

SC486 P.58

INPUTS	OUTPUTS
DCBATOUT	+1_8V_S3_SUS +0_9V_S3_SUS

CPU DC/DC ISL6262A P.59

INPUTS	OUTPUTS
DCBATOUT	VHCORE

CPU DC/DC MAX8546 P.62

INPUTS	OUTPUTS
DCBATOUT	+12VRUN

SYSTEM DC/DC GMT923/GMT966 P.63

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_25VRUN

SYSTEM DC/DC OZ811 GMT966(PEX_VDD) P.60

INPUTS	OUTPUTS
DCBATOUT DCBATOUT +1_8V_S3_SUS	+1_05VRUN NV_VDD PEX_VDD

Nvidia Gfx VDDC

INPUTS	OUTPUTS
+VGFX_CORE	+1_05VRUN (or NV_VDD)

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Title: BLOCK DIAGRAM

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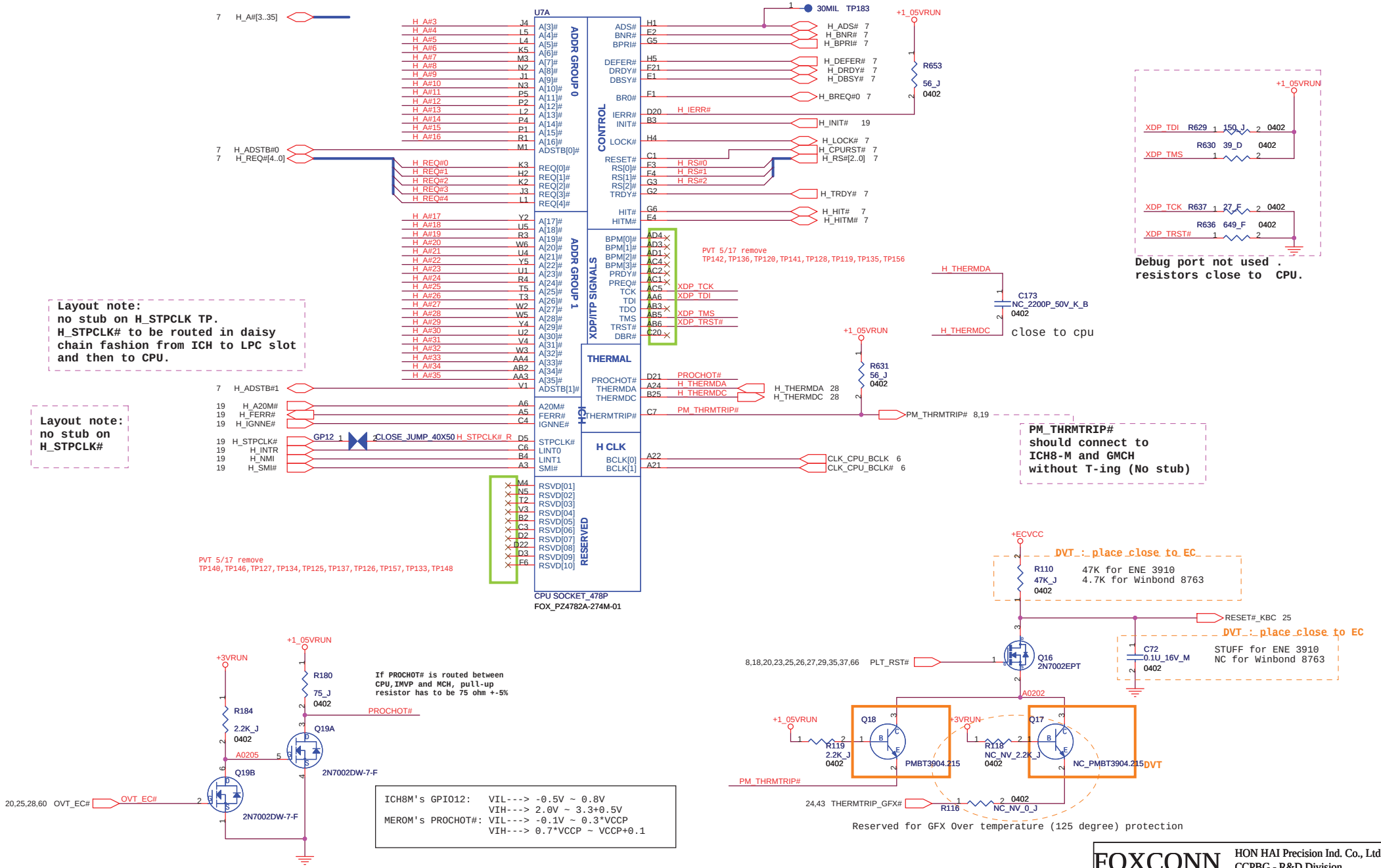

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
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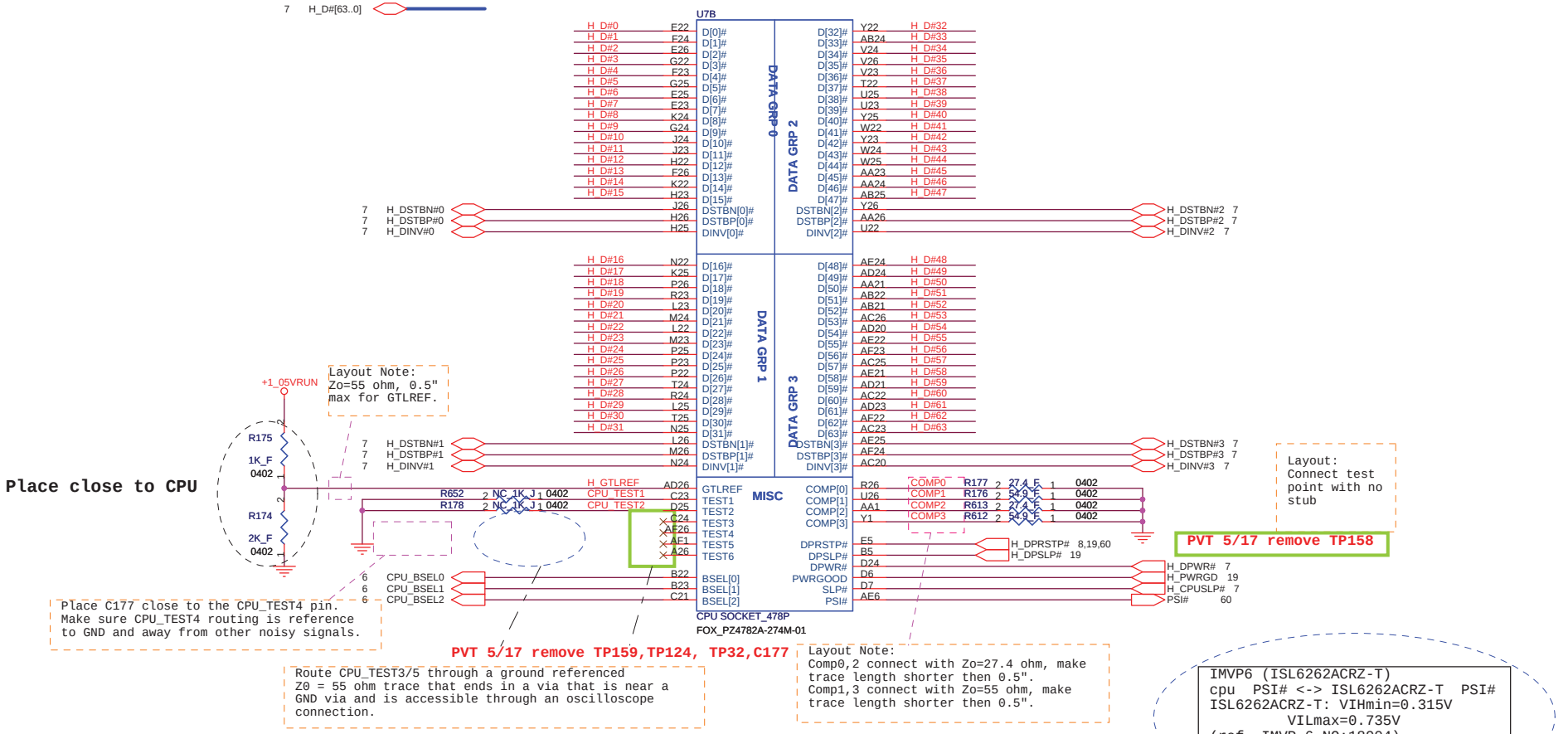

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	266MHz
L L H	133MHz
L H H	166MHz
L H L	200MHz
H H L	400MHz
H H H	Reserve
H L H	100MHz
H L L	333MHz

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Title: **Merom (HOST BUS) 2/3**

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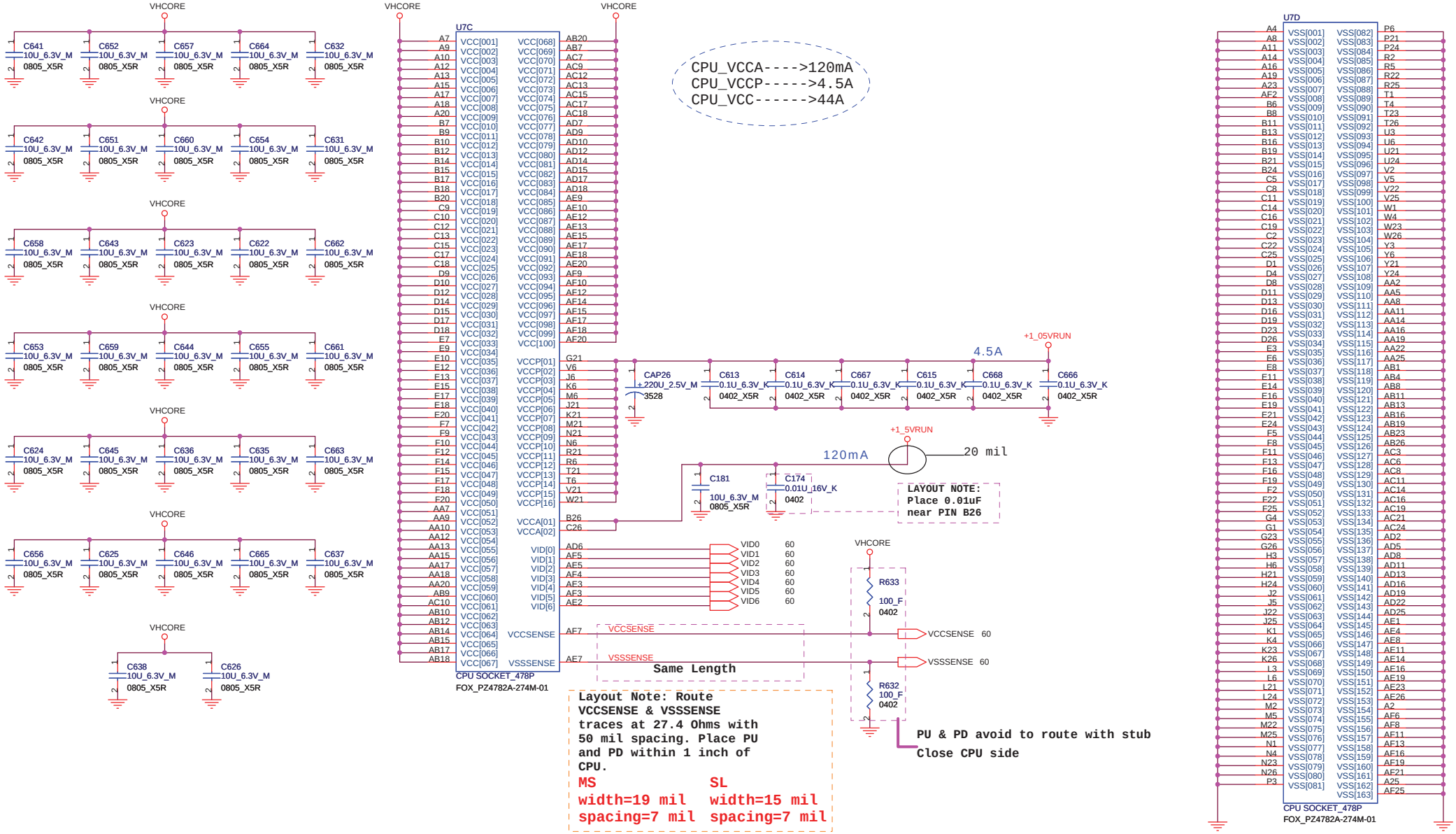

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Merom (POWER/GROUND) 3/3	
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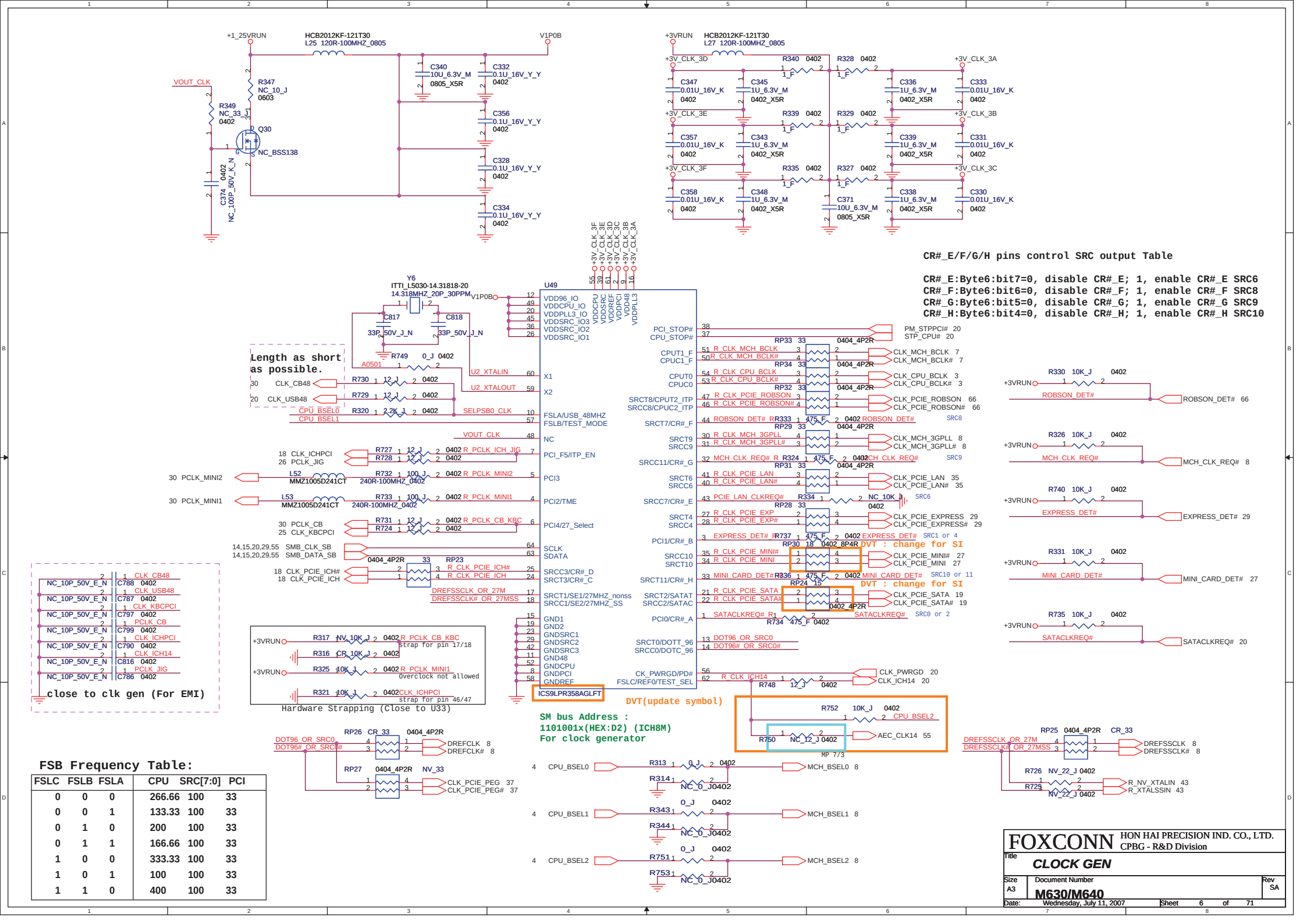

CR#_E/F/G/H pins control SRC output Table

CR#_E:Byte6:bit7=0, disable CR#_E; 1, enable CR#_E SRC6
CR#_F:Byte6:bit6=0, disable CR#_F; 1, enable CR#_F SRC8
CR#_G:Byte6:bit5=0, disable CR#_G; 1, enable CR#_G SRC9
CR#_H:Byte6:bit4=0, disable CR#_H; 1, enable CR#_H SRC10

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

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Title: **CLOCK GEN**

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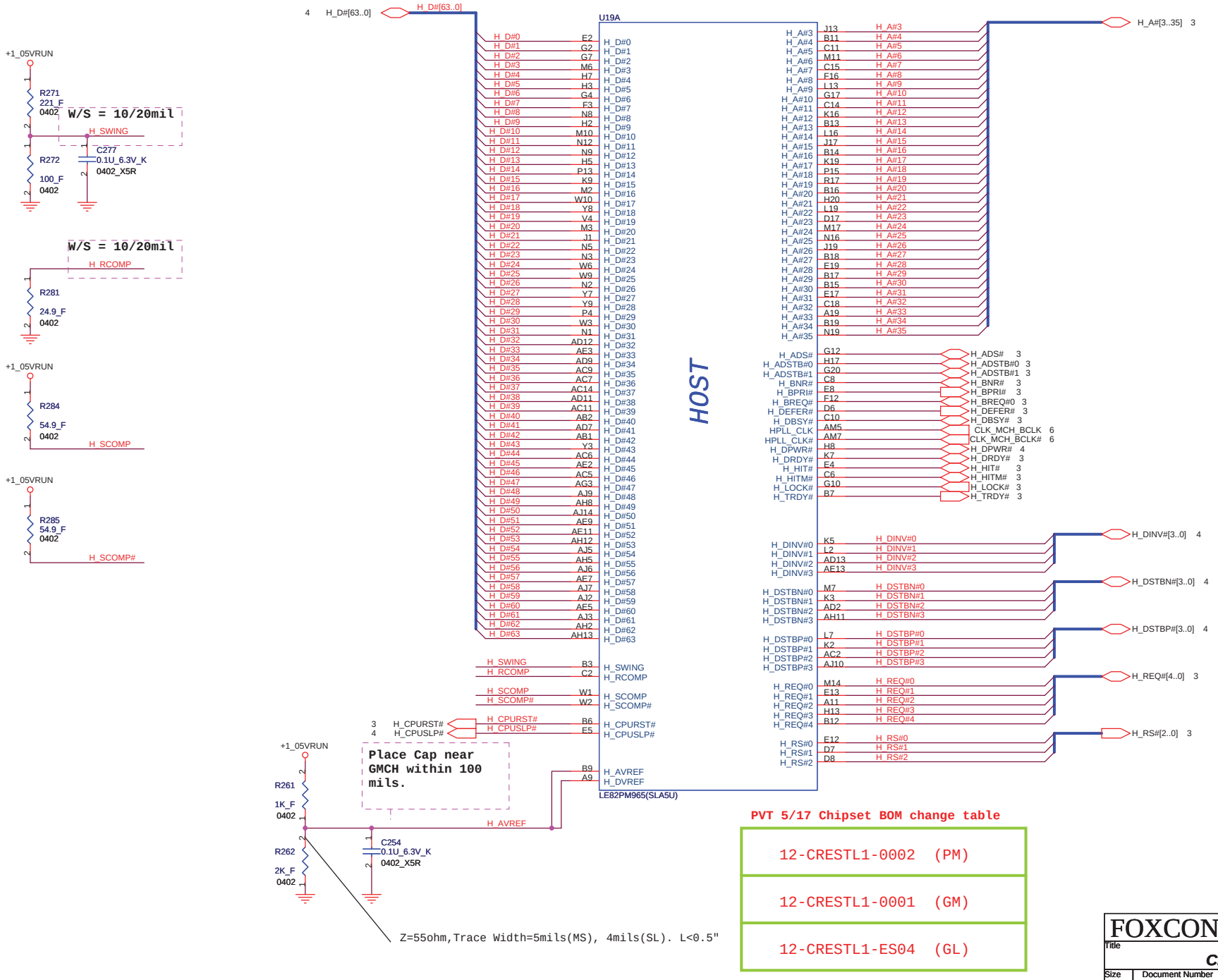

PVT 5/17 Chipset BOM change table

12-CRESTL1-0002 (PM)
12-CRESTL1-0001 (GM)
12-CRESTL1-ES04 (GL)

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Title: *Crestline (HOST) 1/of 7*

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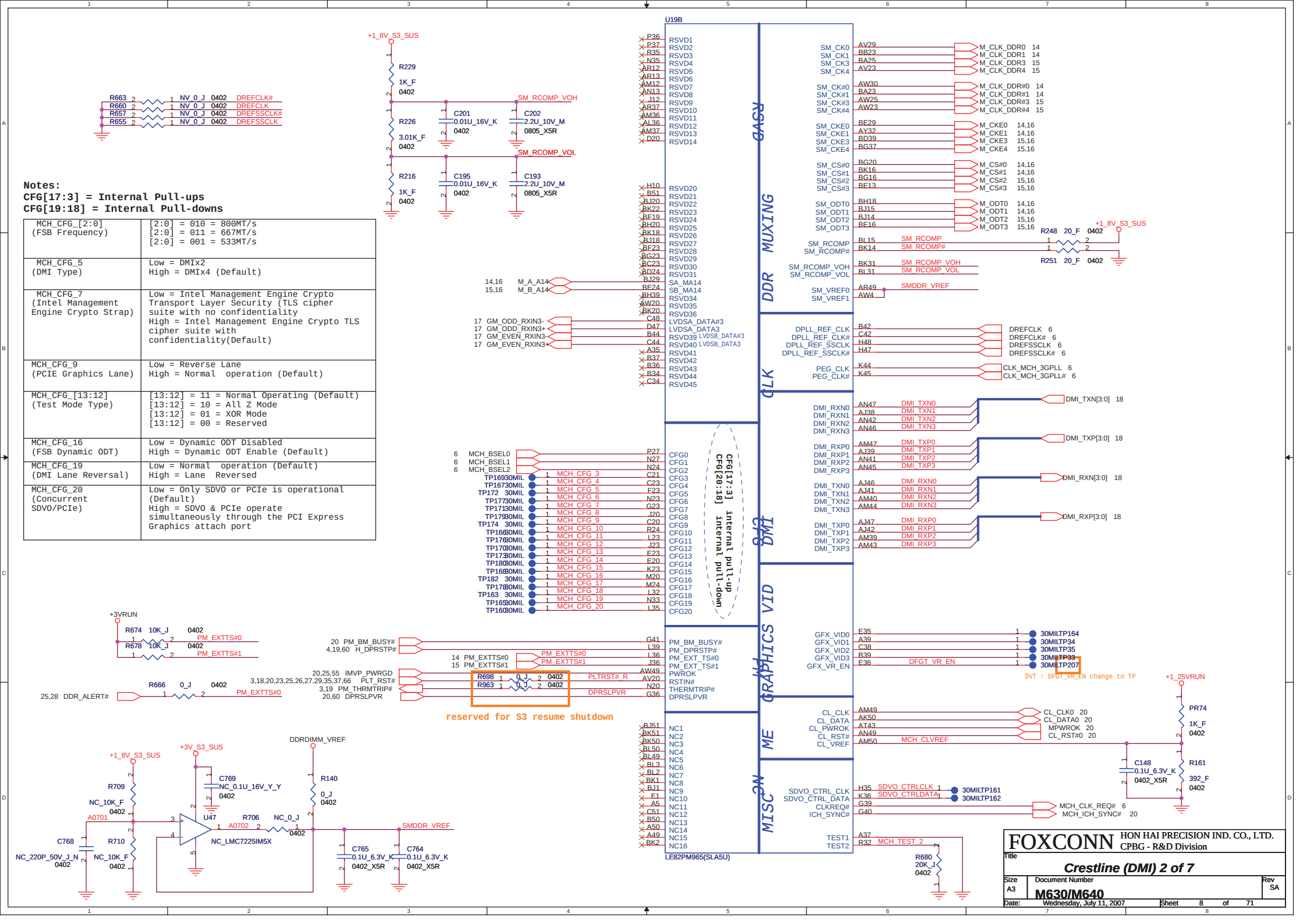
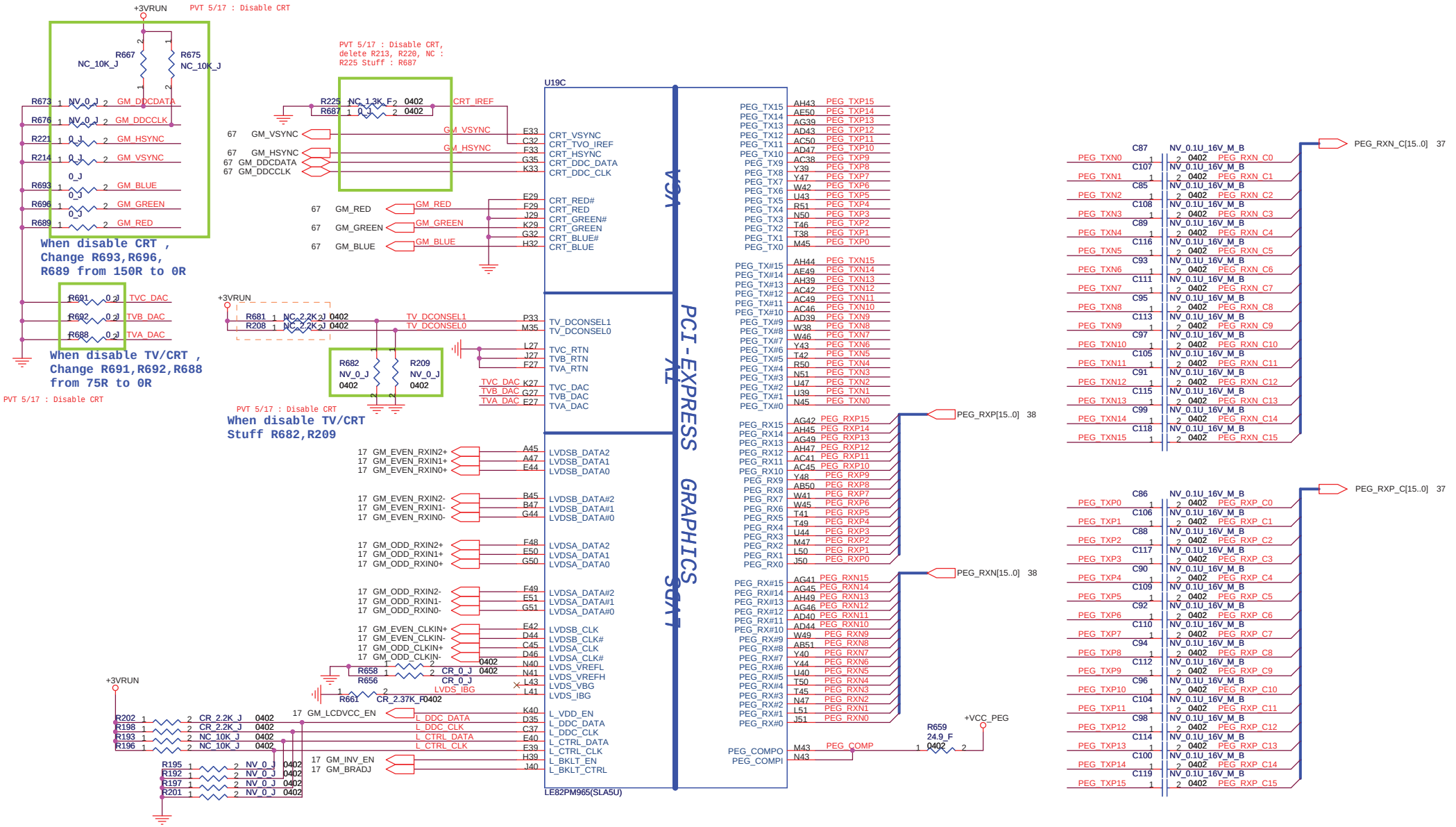
Notes:
CFG[17:3] = Internal Pull-ups
CFG[19:18] = Internal Pull-downs

MCH_CFG_[2:0] (FSB Frequency)	[2:0] = 010 = 800MT/s [2:0] = 011 = 667MT/s [2:0] = 001 = 533MT/s
MCH_CFG_5 (DMI Type)	Low = DMIx2 High = DMIx4 (Default)
MCH_CFG_7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality(Default)
MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation (Default)
MCH_CFG_[13:12] (Test Mode Type)	[13:12] = 11 = Normal Operating (Default) [13:12] = 10 = All Z Mode [13:12] = 01 = XOR Mode [13:12] = 00 = Reserved
MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable (Default)
MCH_CFG_19 (DMI Lane Reversal)	Low = Normal operation (Default) High = Lane Reversed
MCH_CFG_20 (Concurrent SDVO/PCIe)	Low = Only SDVO or PCIe is operational (Default) High = SDVO & PCIe operate simultaneously through the PCI Express Graphics attach port





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Title	Crestline (Gfx) 3 of 7	
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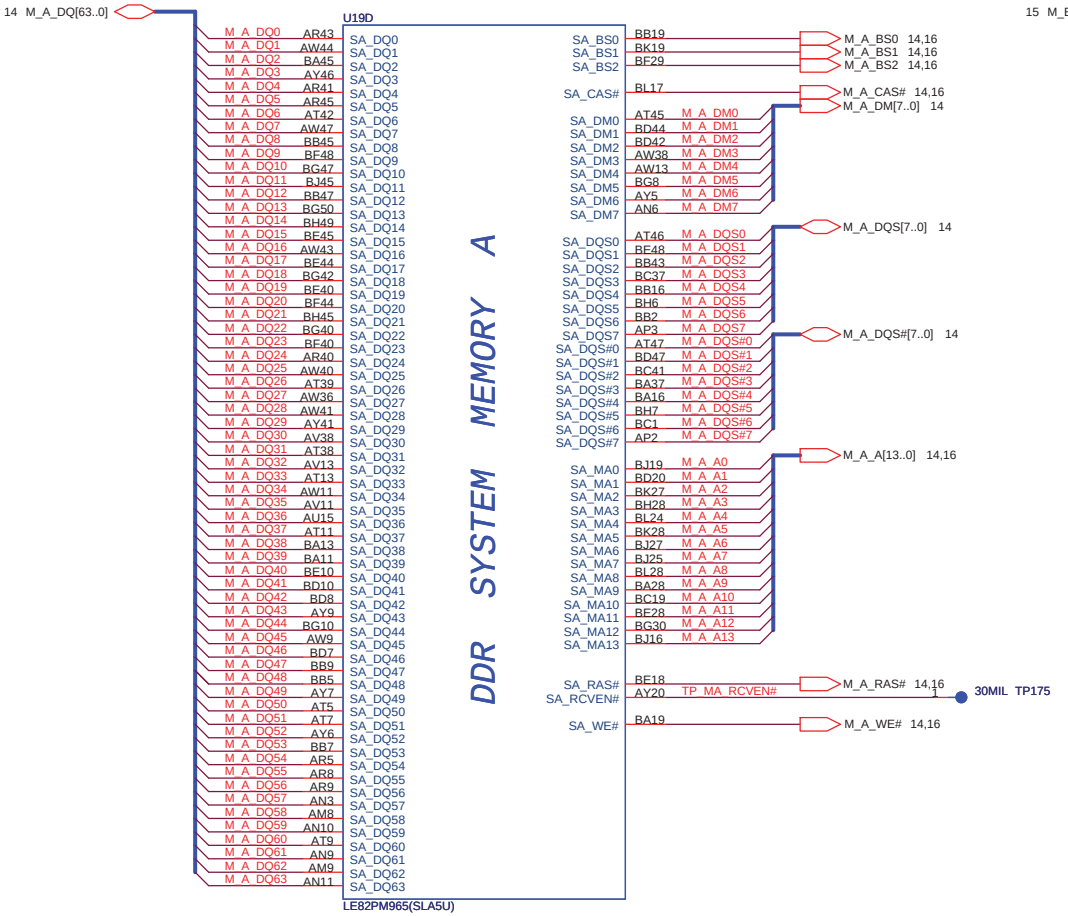

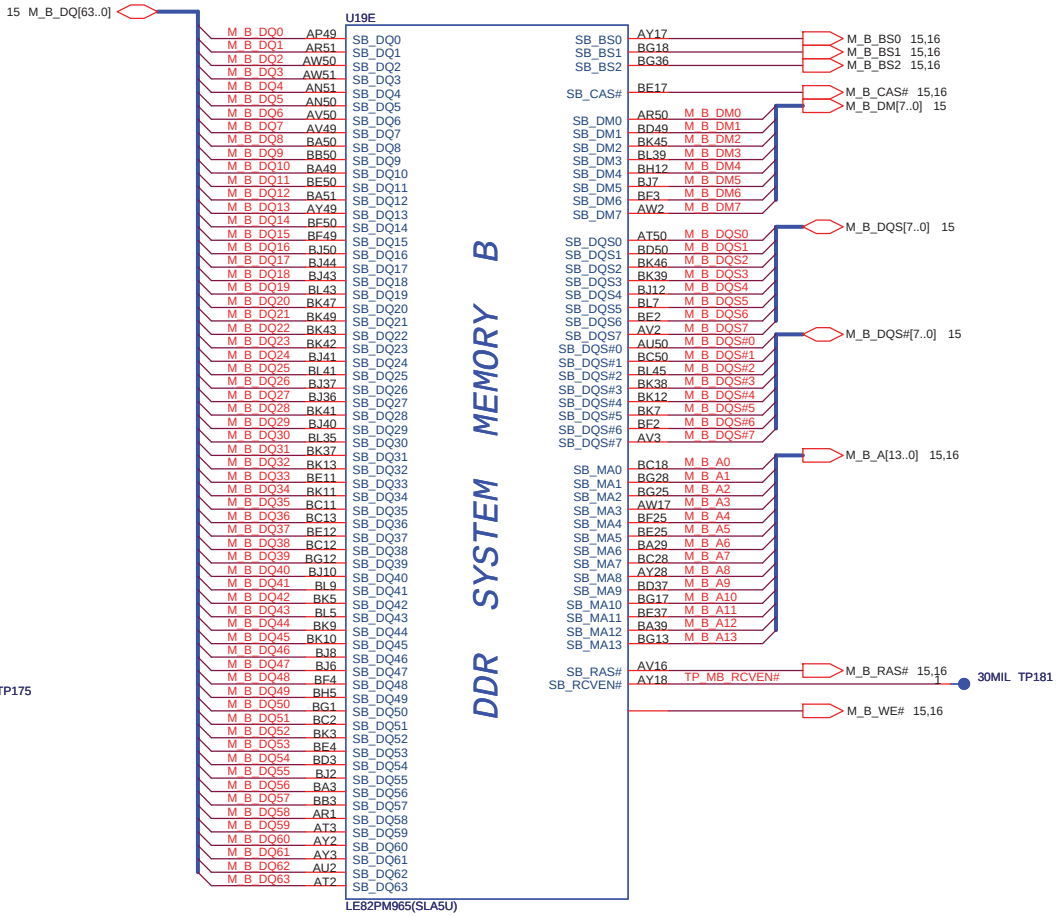

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Title: Crestline (DDRII) 4 of 7

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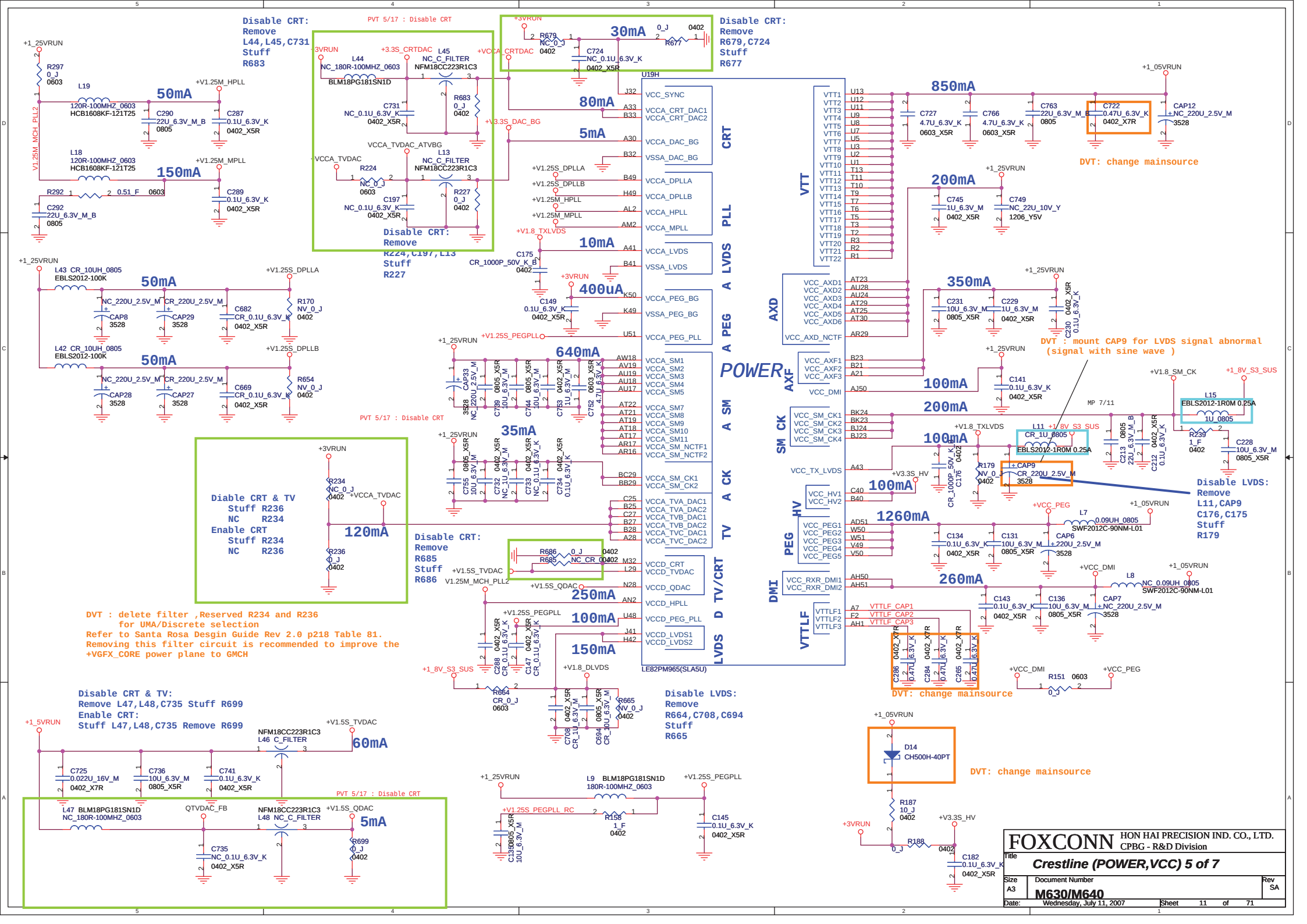
Disable CRT:
Remove
L44,L45,C731
Stuff
R683
PVT 5/17 : Disable CRT
Disable CRT:
Remove
R679,C724
Stuff
R677
Disable CRT:
Remove
R224,C197,L13
Stuff
R227
Disable CRT & TV
Stuff R236
NC R234
Enable CRT
Stuff R234
NC R236
Disable CRT:
Remove
R685
Stuff
R686
DVT : delete filter ,Reserved R234 and R236
for UMA/Discrete selection
Refer to Santa Rosa Desgin Guide Rev 2.0 p218 Table 81.
Removing this filter circuit is recommended to improve the
+VGFX_CORE power plane to GMCH
Disable CRT & TV:
Remove L47,L48,C735 Stuff R699
Enable CRT:
Stuff L47,L48,C735 Remove R699
PVT 5/17 : Disable CRT
Disable LVDS:
Remove
R664,C708,C694
Stuff
R665
DVT: change mainsource
DVT : mount CAP9 for LVDS signal abnormal
(signal with sine wave)
Disable LVDS:
Remove
L11,CAP9
C176,C175
Stuff
R179
DVT: change mainsource
DVT: change mainsource
POWER
U19H
LE82PM965(SLA5U)
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
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Crestline (POWER,VCC) 5 of 7
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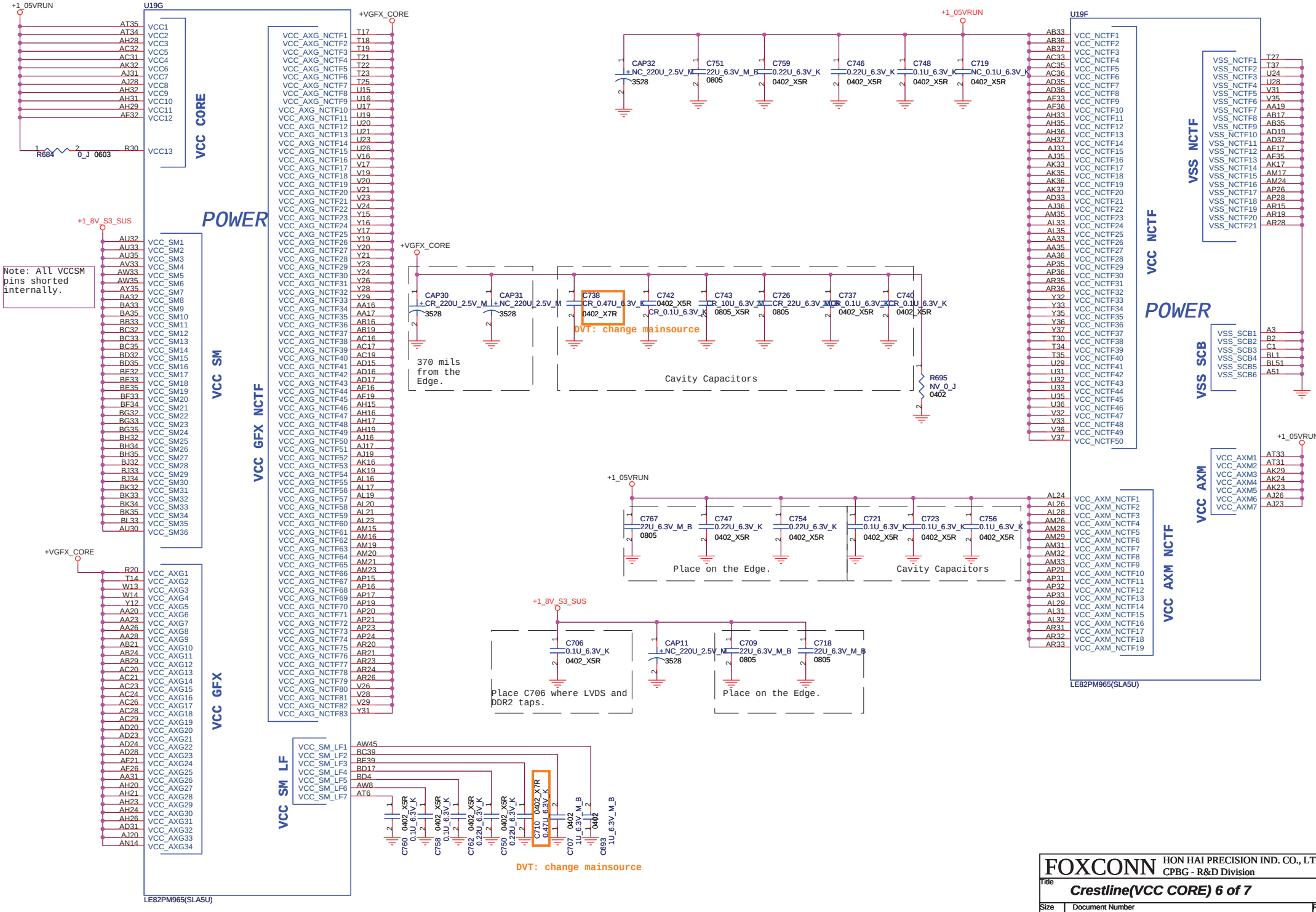

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Title: *Crestline(VCC CORE) 6 of 7*

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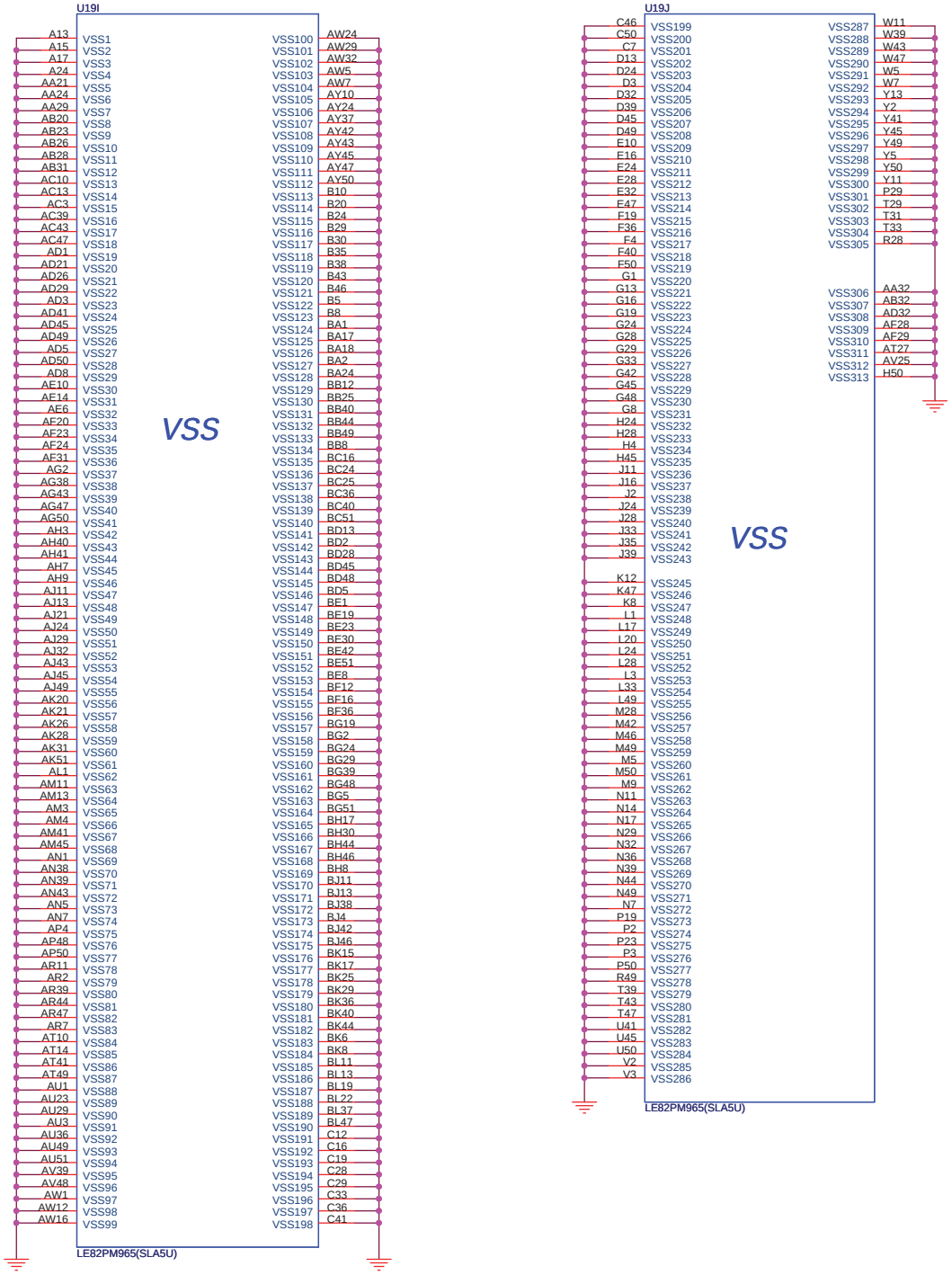

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Title: *Crestline (VSS) 7 of 7*

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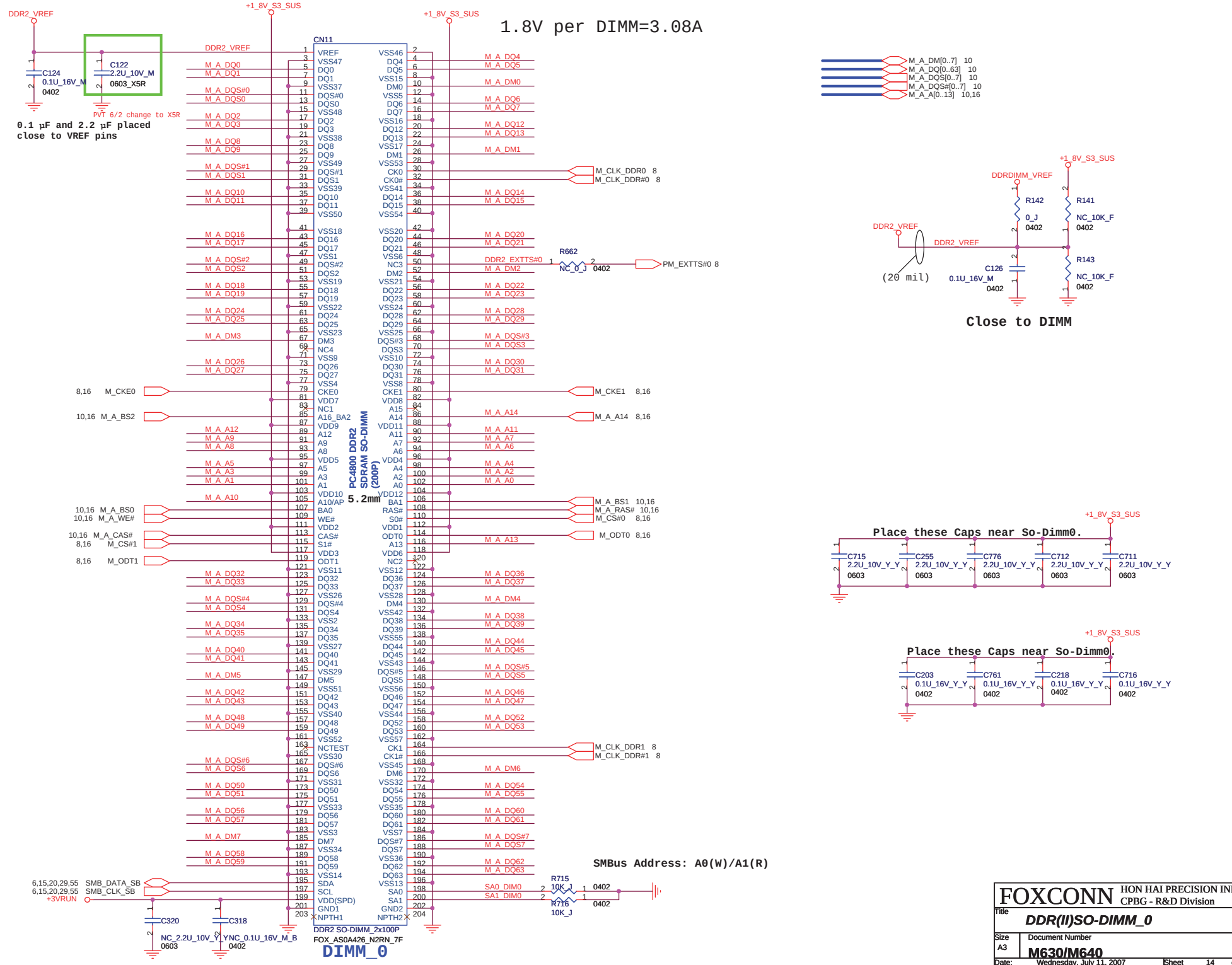

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: DDR(II)SO-DIMM_0

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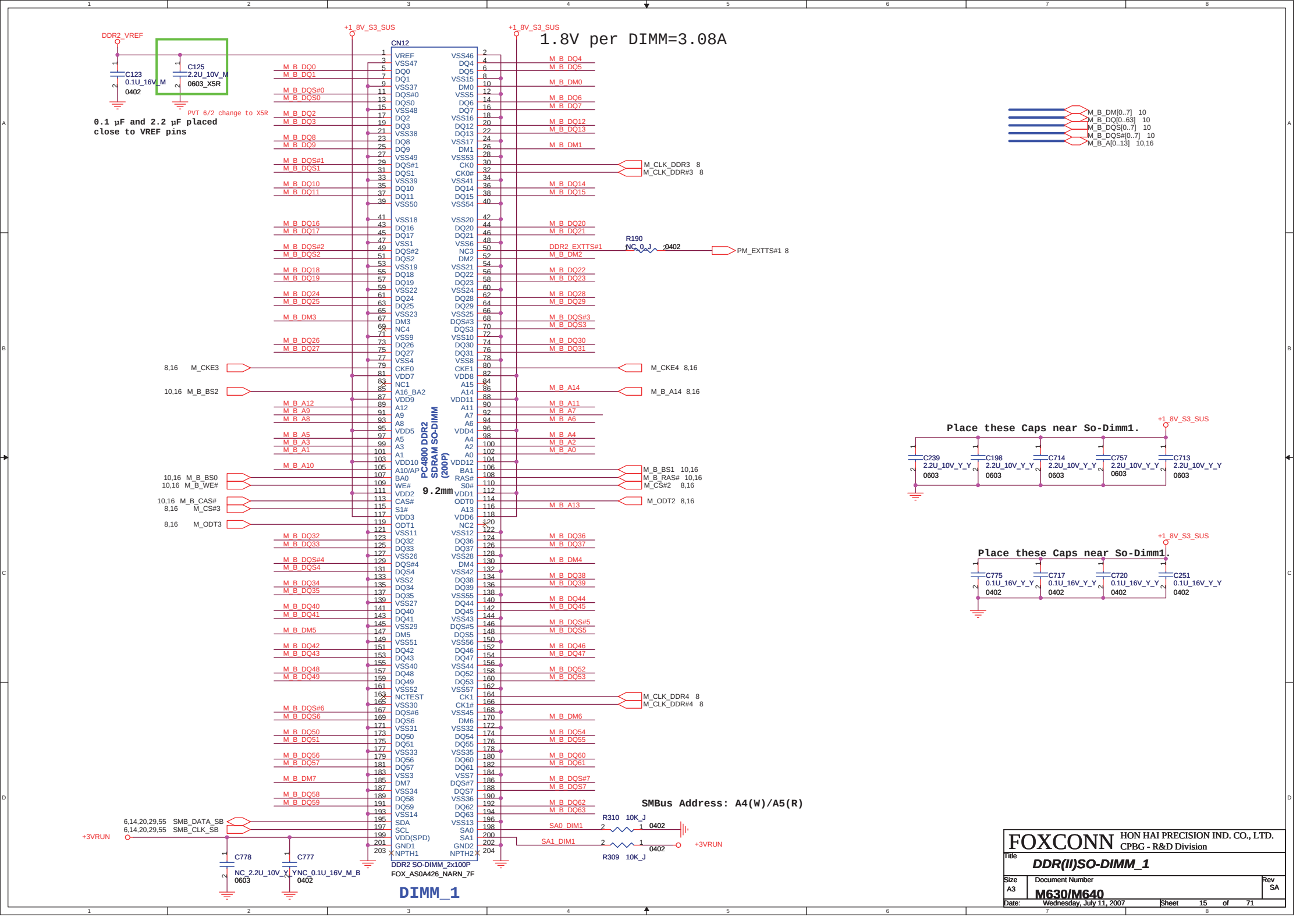
1.8V per DIMM=3.08A
DDR2_VREF
+1_8V_S3_SUS
C123 0.1U_16V_M 0402
C125 2.2U_10V_M 0603_X5R
PVT 6/2 change to X5R
0.1 µF and 2.2 µF placed close to VREF pins
CN12
PC4800 DDR2 SDRAM SO-DIMM (200P)
9.2mm
DDR2 SO-DIMM_2x100P
FOX_AS0A426_NARN_7F
DIMM_1
M_B_DM[0..7] 10
M_B_DQ[0..63] 10
M_B_DQS[0..7] 10
M_B_DQS#[0..7] 10
M_B_A[0..13] 10,16
M_CLK_DDR3 8
M_CLK_DDR#3 8
M_CLK_DDR4 8
M_CLK_DDR#4 8
R190 NC_0_J 0402
DDR2_EXTTS#1
PM_EXTTS#1 8
M_CKE3 8,16
M_CKE4 8,16
M_B_BS2 10,16
M_B_A14 8,16
M_B_BS0 10,16
M_B_WE# 10,16
M_B_BS1 10,16
M_B_RAS# 10,16
M_CS#2 8,16
M_B_CAS# 10,16
M_CS#3 8,16
M_ODT2 8,16
M_ODT3 8,16
Place these Caps near So-Dimm1.
C239 2.2U_10V_Y_Y 0603
C198 2.2U_10V_Y_Y 0603
C714 2.2U_10V_Y_Y 0603
C757 2.2U_10V_Y_Y 0603
C713 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm1.
C775 0.1U_16V_Y_Y 0402
C717 0.1U_16V_Y_Y 0402
C720 0.1U_16V_Y_Y 0402
C251 0.1U_16V_Y_Y 0402
SMBus Address: A4(W)/A5(R)
6,14,20,29,55 SMB_DATA_SB
6,14,20,29,55 SMB_CLK_SB
+3VRUN
R310 10K_J 0402
R309 10K_J 0402
SA0_DIM1
SA1_DIM1
C778 NC_2.2U_10V_Y 0603
C777 NC_0.1U_16V_M_B 0402
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Title
DDR(II)SO-DIMM_1
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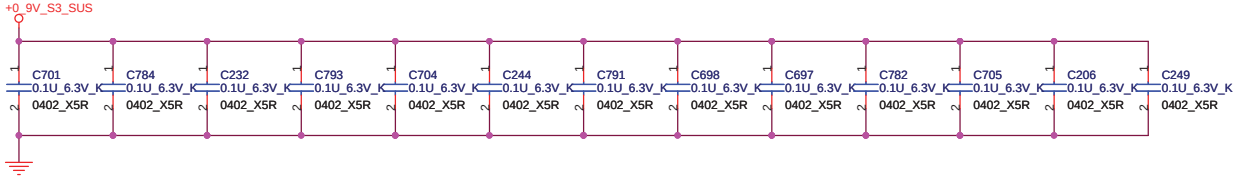
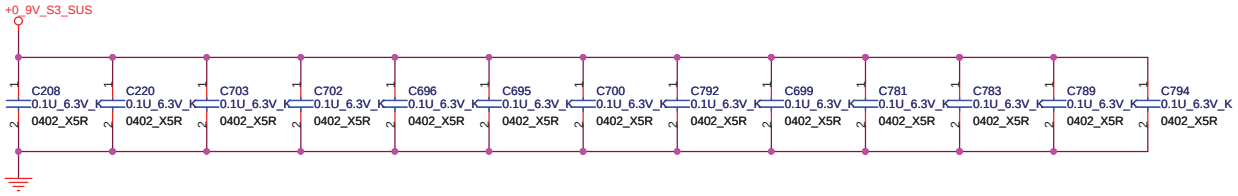


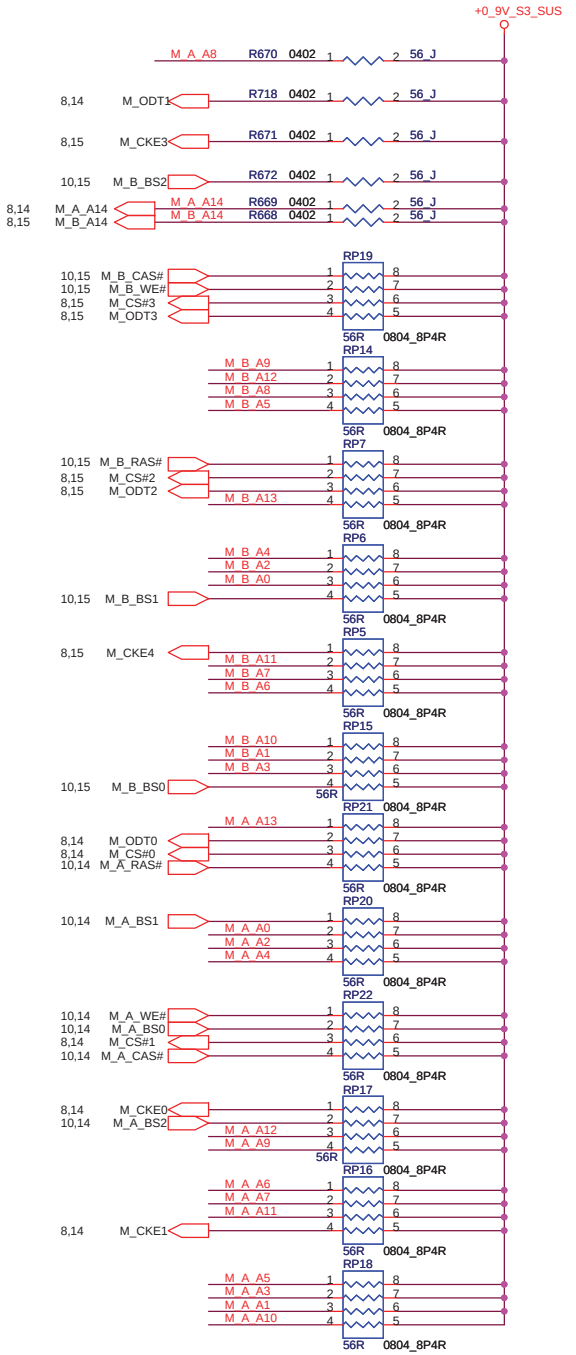
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9_S3_VSUS



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9V_S3_SUS

10,14 M_A_A[0..13]

10,15 M_B_A[0..13]



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Title: ***DDR(II)Termination***

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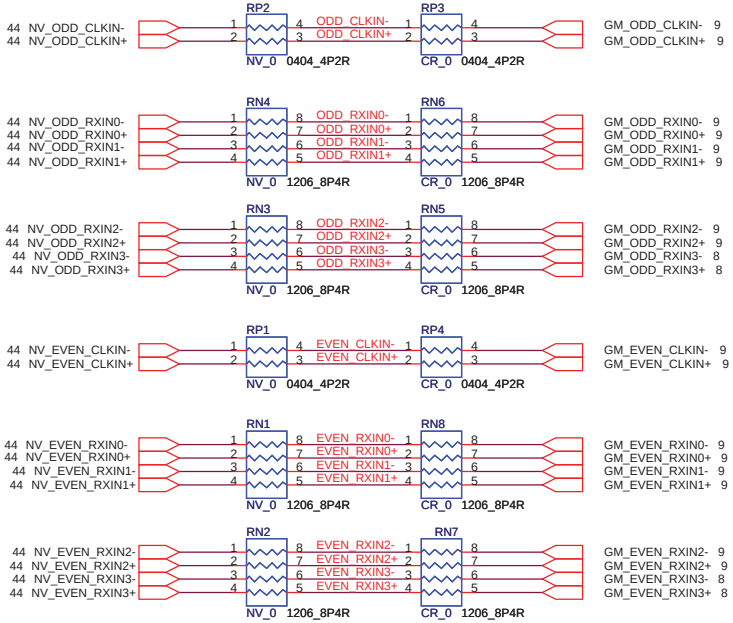
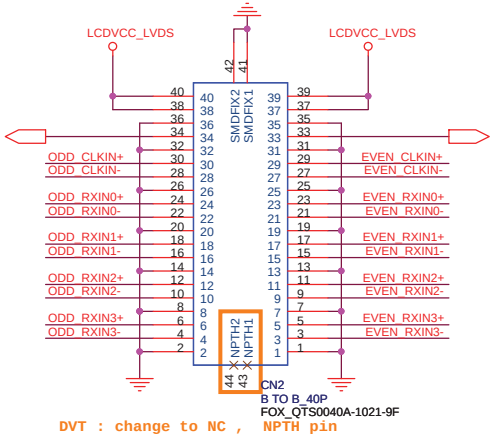
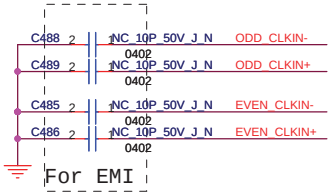
LVDS





DVT : change to NC , NPTH pin

LVDS CONNECTOR

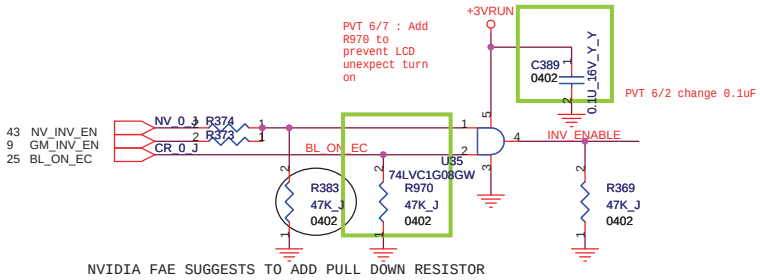


M630, 19"

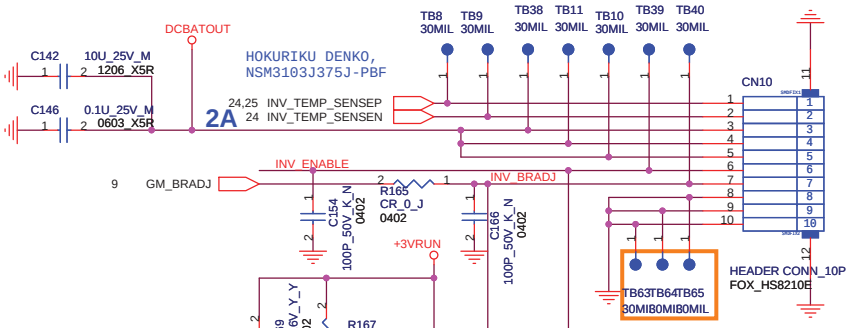
	Type 1	Type 2	Type 3	Type 4
00	AUO M190PW01 V.1			V
01			V	
10		V		
11				

M640, 22"

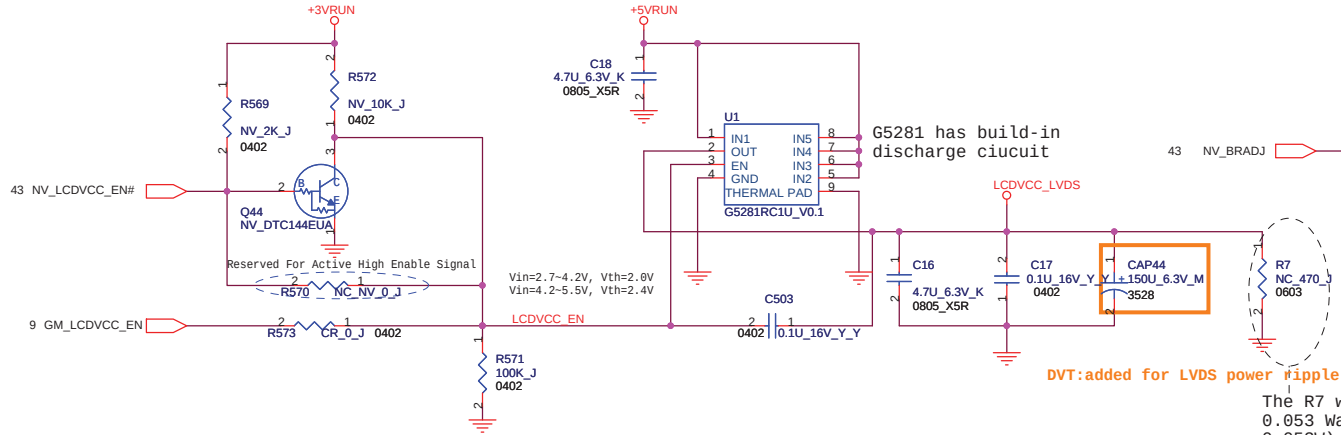
	Type 1	Type 2	Type 3	Type 4
00	AUO M220EW01 V.2			V
01			V	
10		V		
11				



NVIDIA FAE SUGGESTS TO ADD PULL DOWN RESISTOR



INVERTER CONNECTOR



DVT:added for LVDS power ripple (too large,spec is 200mv)

The R7 will consume about 0.053 Watt (5x5/470 = 0.053W). We changed resistor to 0603 size (1/10 Watt)

LCD POWER

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Size A3	Document Number M630/M640		Rev SA
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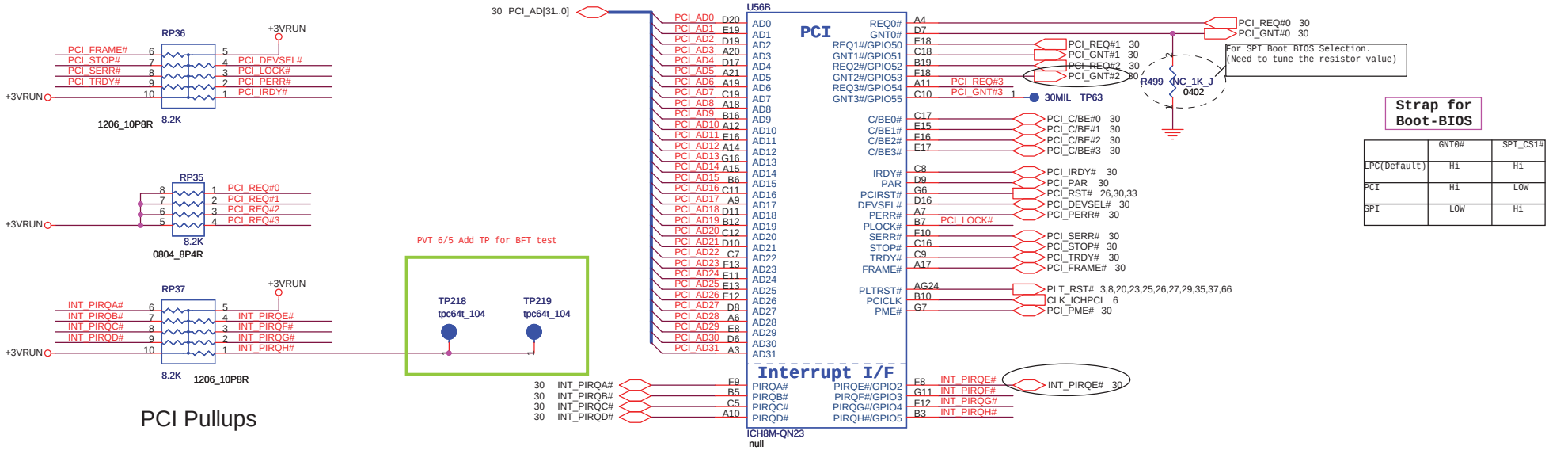


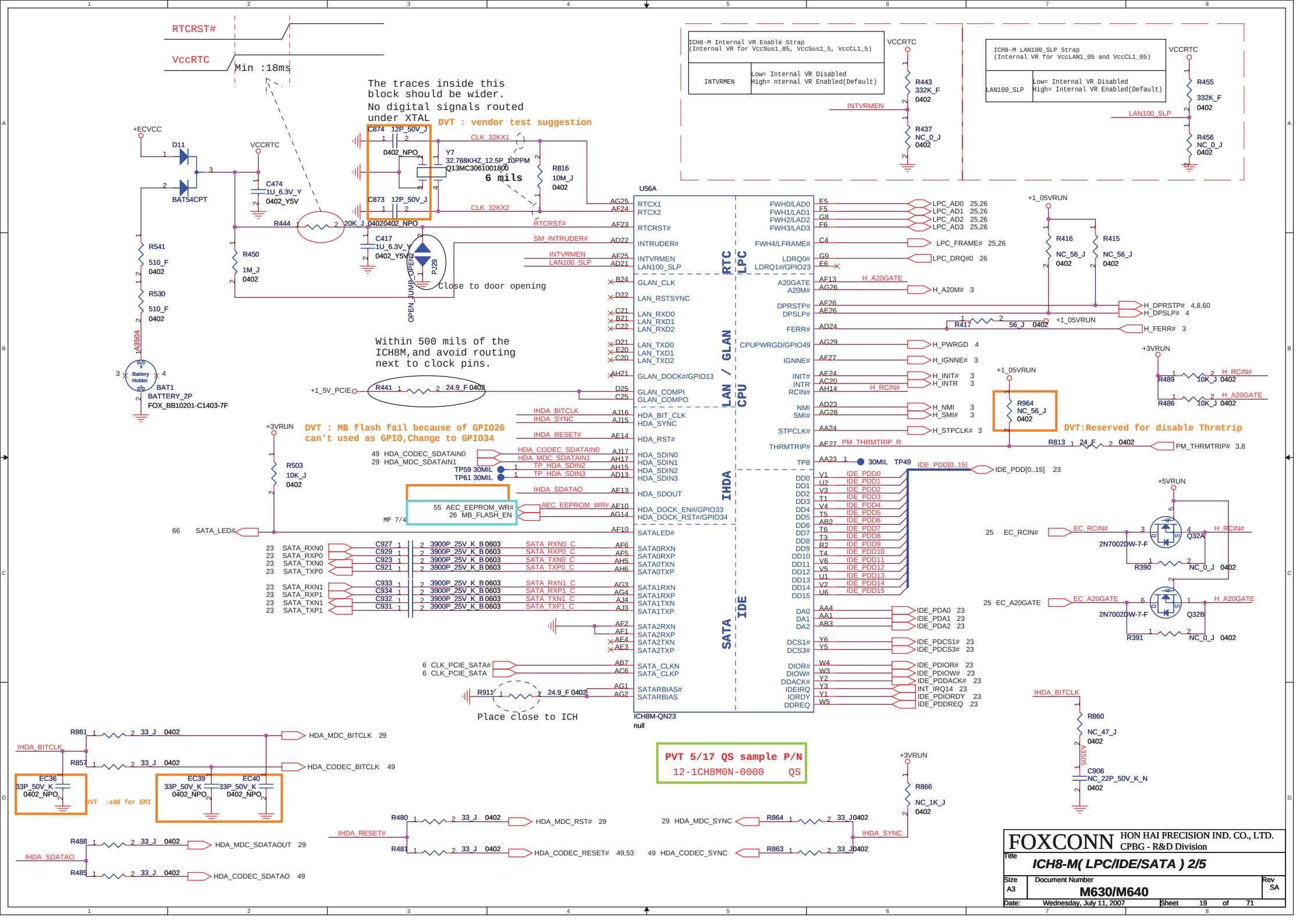
USB PORT	Function
PORT-0	REAR-1
PORT-1	REAR-2
PORT-2	REAR-3
PORT-3	SIDE-1
PORT-4	SIDE-2
PORT-5	EXPRESS CARD
PORT-6	CAMERA
PORT-7	CIR
PORT-8	RF KBD
PORT-9	NC

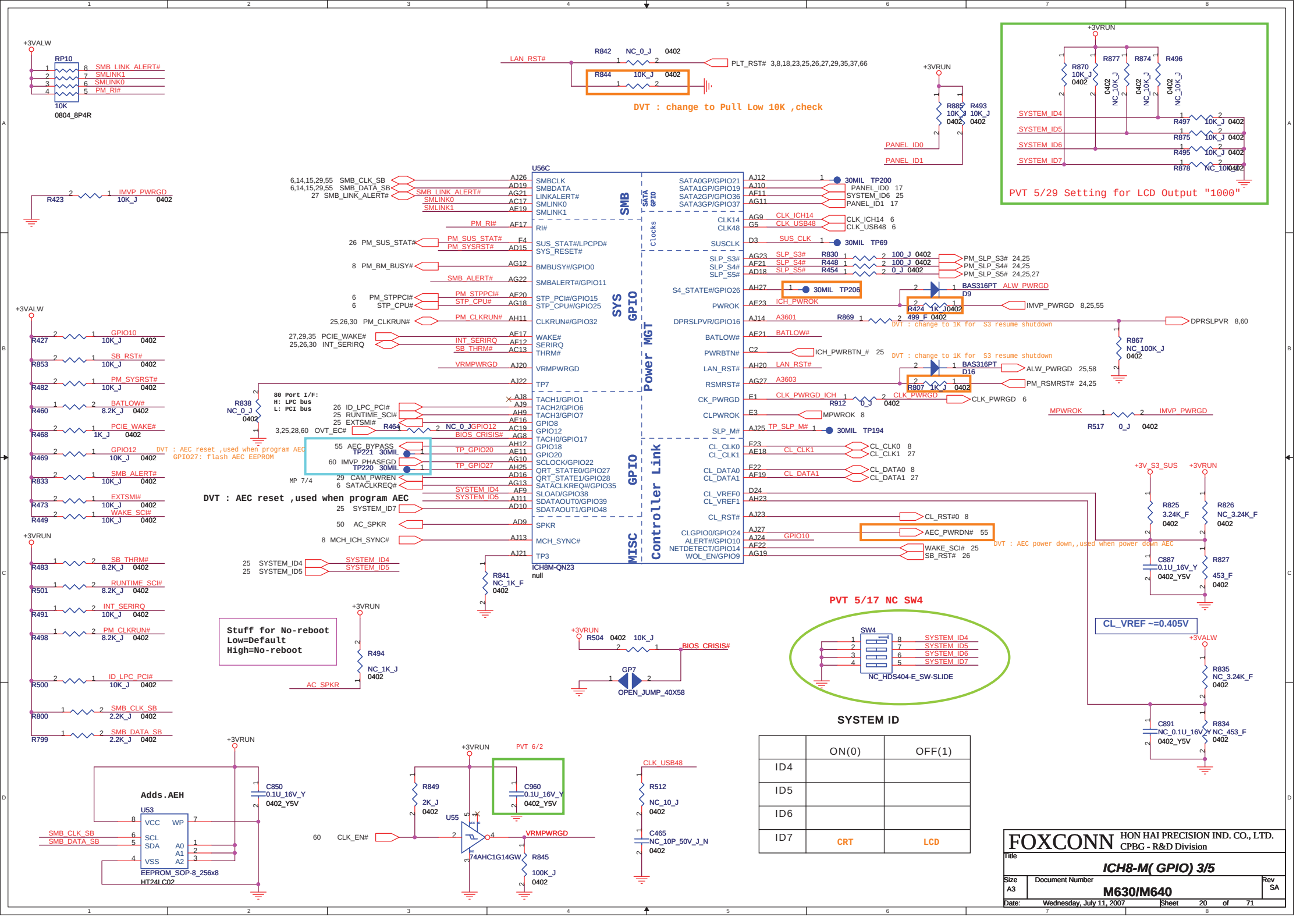
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

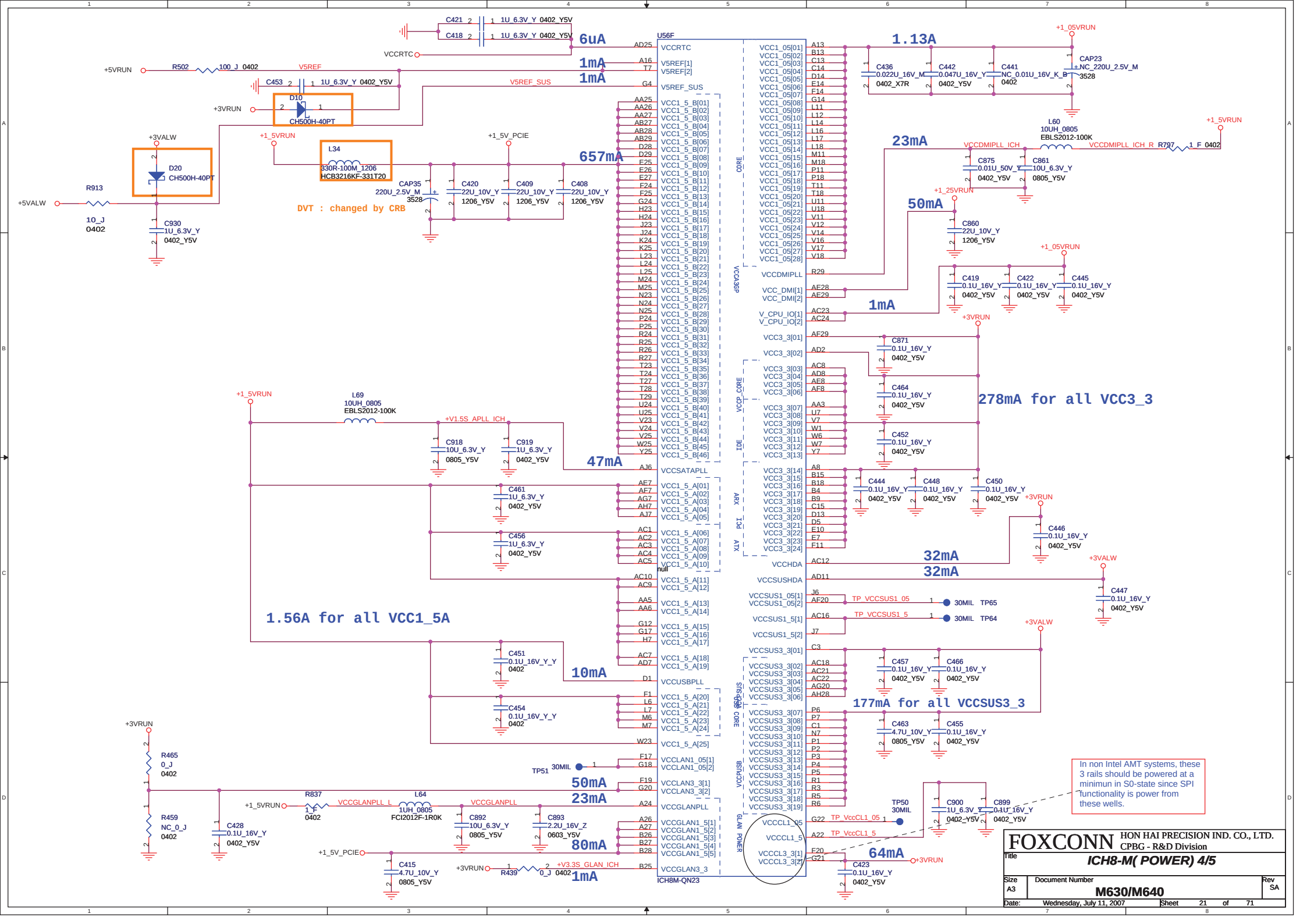
Title: ICH8-M(PCI/DMI/USB/PCIE) 1/5

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 18 of 71


RTCRST#
VccRTC
Min :18ms
The traces inside this block should be wider.
No digital signals routed under XTAL
DVT : vendor test suggestion
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5, VccCL1_5)
INTVRMEN
Low= Internal VR Disabled
High= nternal VR Enabled(Default)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
LAN100_SLP
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
U56A
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
ICH8M-QN23
null
close to door opening
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
DVT : MB flash fail because of GPIO26 can't used as GPIO,Change to GPIO34
DVT:Reserved for disable Thrmtrip
Place close to ICH
PVT 5/17 QS sample P/N
12-1CH8M0N-0000 QS
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH8-M(LPC/IDE/SATA) 2/5
M630/M640
Wednesday, July 11, 2007
Sheet 19 of 71


DVT : change to Pull Low 10K ,check
PVT 5/29 Setting for LCD Output "1000"
DVT : AEC reset ,used when program AEC
Stuff for No-reboot
Low=Default
High=No-reboot
PVT 5/17 NC SW4
CL_VREF ~=0.405V
SYSTEM ID
ON(0)
OFF(1)
ID4
ID5
ID6
ID7
CRT
LCD
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
ICH8-M(GPIO) 3/5
M630/M640
Wednesday, July 11, 2007
Sheet 20 of 71


6uA
1mA
1mA
657mA
47mA
10mA
50mA
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
278mA for all VCC3_3
32mA
32mA
177mA for all VCCSUS3_3
64mA
1.56A for all VCC1_5A
DVT : changed by CRB
U56F
ICH8M-QN23
CORE
VCCA3GP
VCCP CORE
DEI
ARX
DCI
ATX
SUS CORE
SUS PWR
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCCSATAPLL
VCCUSBPLL
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCCHDA
VCCSUSHDA
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
TP_VCCSUS1_05
TP_VCCSUS1_5
TP_VccCL1_05
TP_VccCL1_5
In non Intel AMT systems, these 3 rails should be powered at a minimun in S0-state since SPI functionality is power from these wells.
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
ICH8-M(POWER) 4/5
Size A3
Document Number
M630/M640
Rev SA
Date: Wednesday, July 11, 2007
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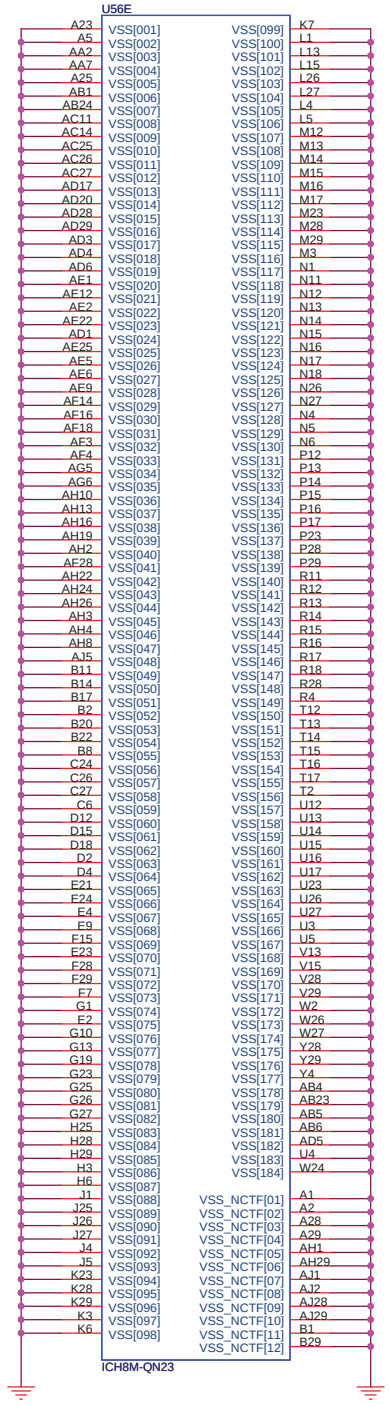

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: ICH8-M(GND) 5/5

Size: A3 | Document Number: M630/M640 | Rev: SA

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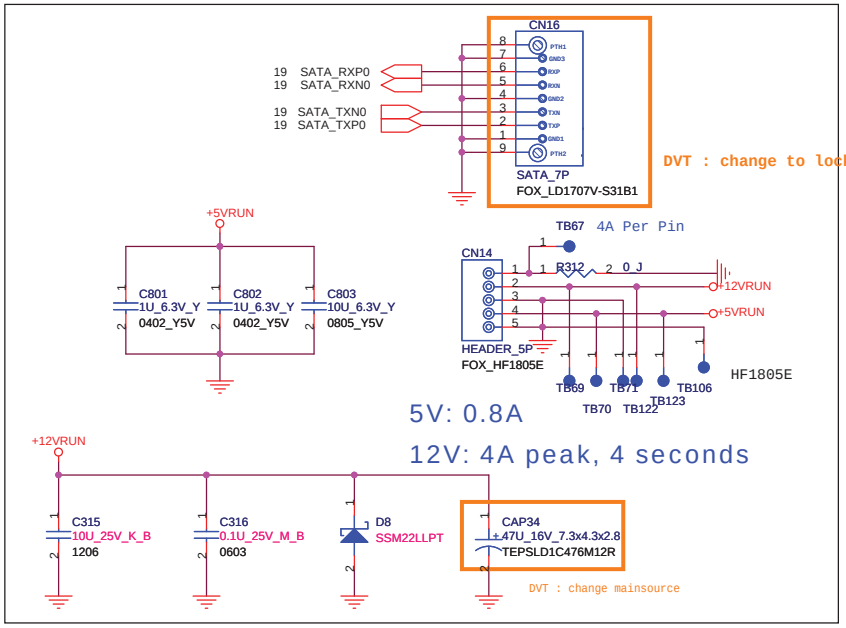
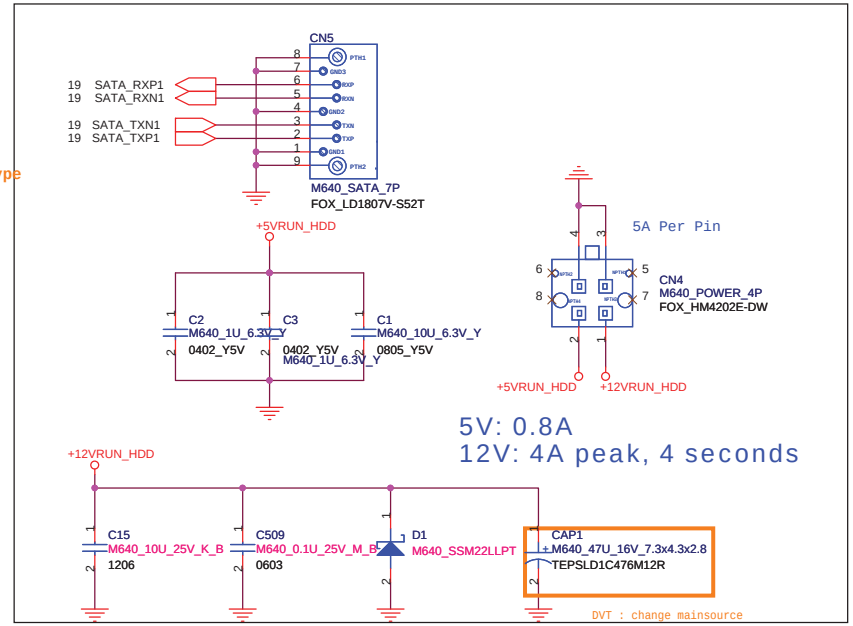
SATA HDD CONN

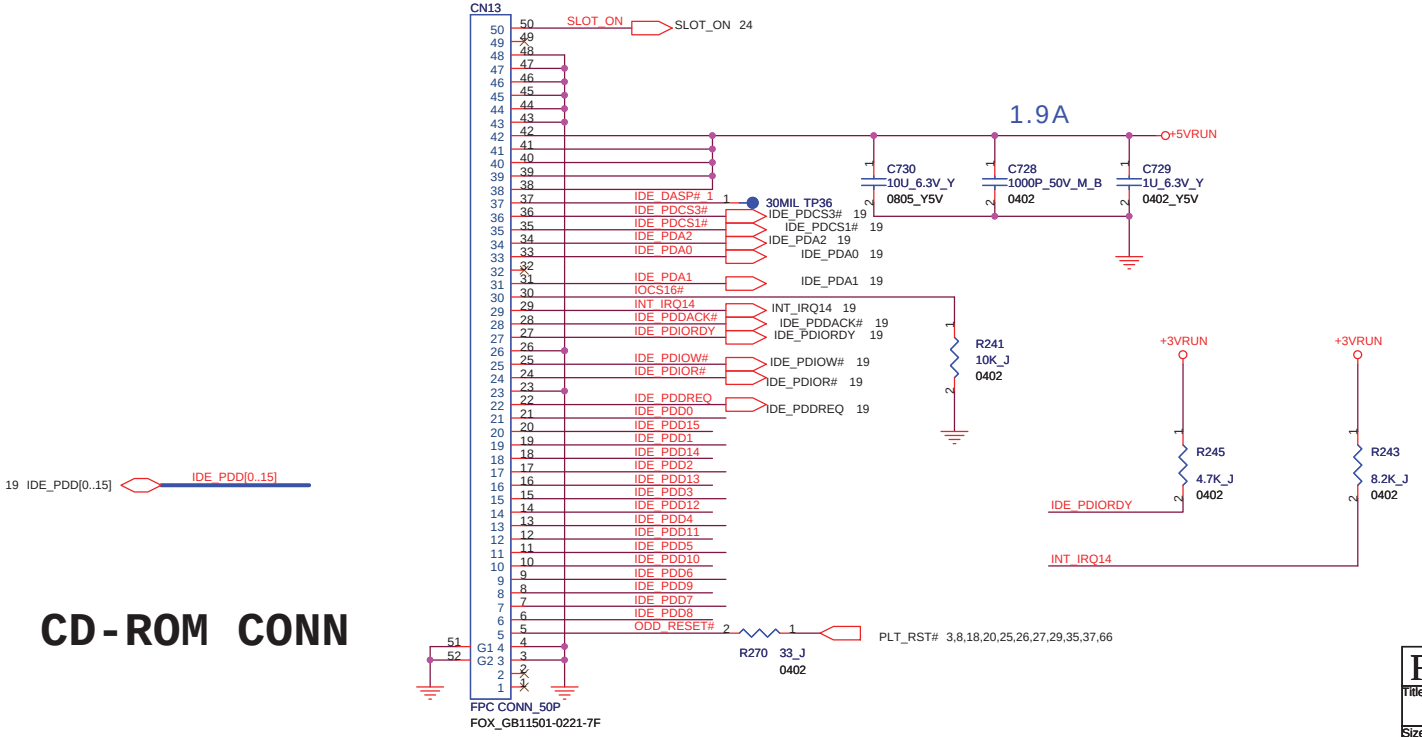


HDD1

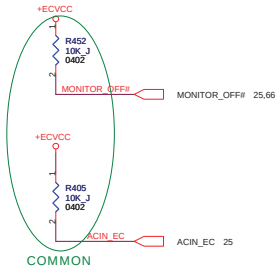


HDD2

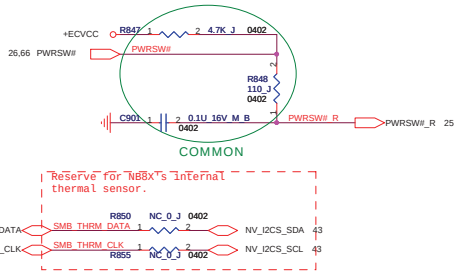
CD-ROM CONN

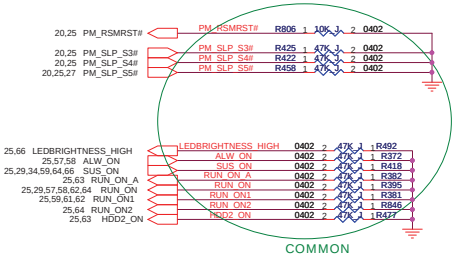


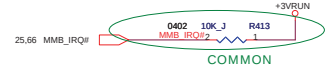
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 23 of 71	

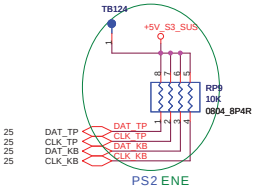


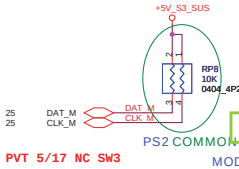
DVT : delete winbond









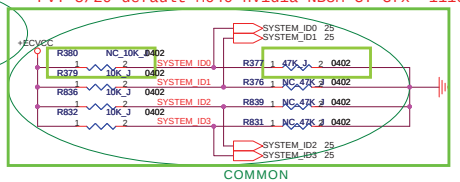


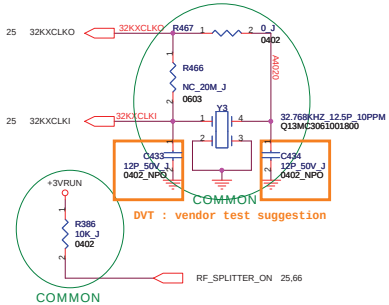
PVT 6/1 Add system ID table

	0	1
SYSTEM_ID0	R377	R380
SYSTEM_ID1	R376	R379
SYSTEM_ID2	R839	R836
SYSTEM_ID3	R831	R832

M630 PVT SKU	M630 8M 256H	M630 8M 128Q	M630 GM	M630 GL
SYSTEM_ID0	0	0	1	0
SYSTEM_ID1	1	1	0	0
SYSTEM_ID2	0	0	0	0
SYSTEM_ID3	1	1	1	1
M640 PVT SKU	M640 8M 256Q	M640 8M 128H	M640 GM	
SYSTEM_ID0	0	0	1	
SYSTEM_ID1	1	1	0	
SYSTEM_ID2	1	1	1	
SYSTEM_ID3	1	1	1	

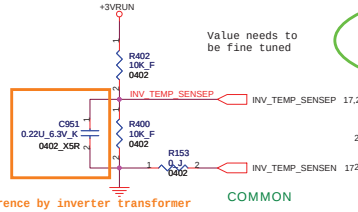
PVT 5/29 default M640 nVidia NB8M-GT Gfx "1110"





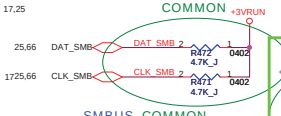
H(3.0-3.6) :RF AMP ON * default (need to pull up)
L(0) :RF AMP OFF

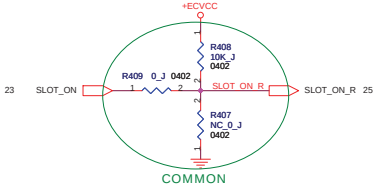
DVT :netname in 3910 don't connect

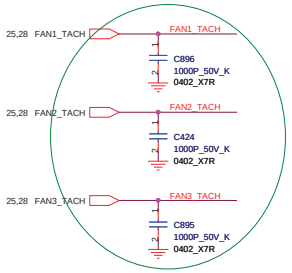


Value needs to be fine tuned

DVT : thermistor interference by inverter transformer







JTAG Select Configuration

JEN0#(Pin24)	JENK#(Pin53)	Pins 17,20,21, 23,25,27	Pins 47,48,50 51,52
No power-down resistor		GPIO port signals	Keyboard scan out
Add 10K pull down	No pull down	JTAG signals	Keyboard scan out
No pull down	Add 10K pull down	GPIO port signals	JATG signals
Add 10K pull down		IIIegal Srap Combination	

SYSTEM ID Table		
ID1	ID0	Graphics Chip
0	0	Intel GL960
0	1	Intel GM965
1	0	nVidia NB8M-GT Gfx
1	1	nVidia NB8P-GS Gfx

SYSTEM ID Table		
ID3	ID2	Model Name
0	0	Reserved
0	1	M620
1	0	M630
1	1	M640

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	EC(KB3925)		
Size: Custom	Document Number: M630/M640		Rev: 0.1
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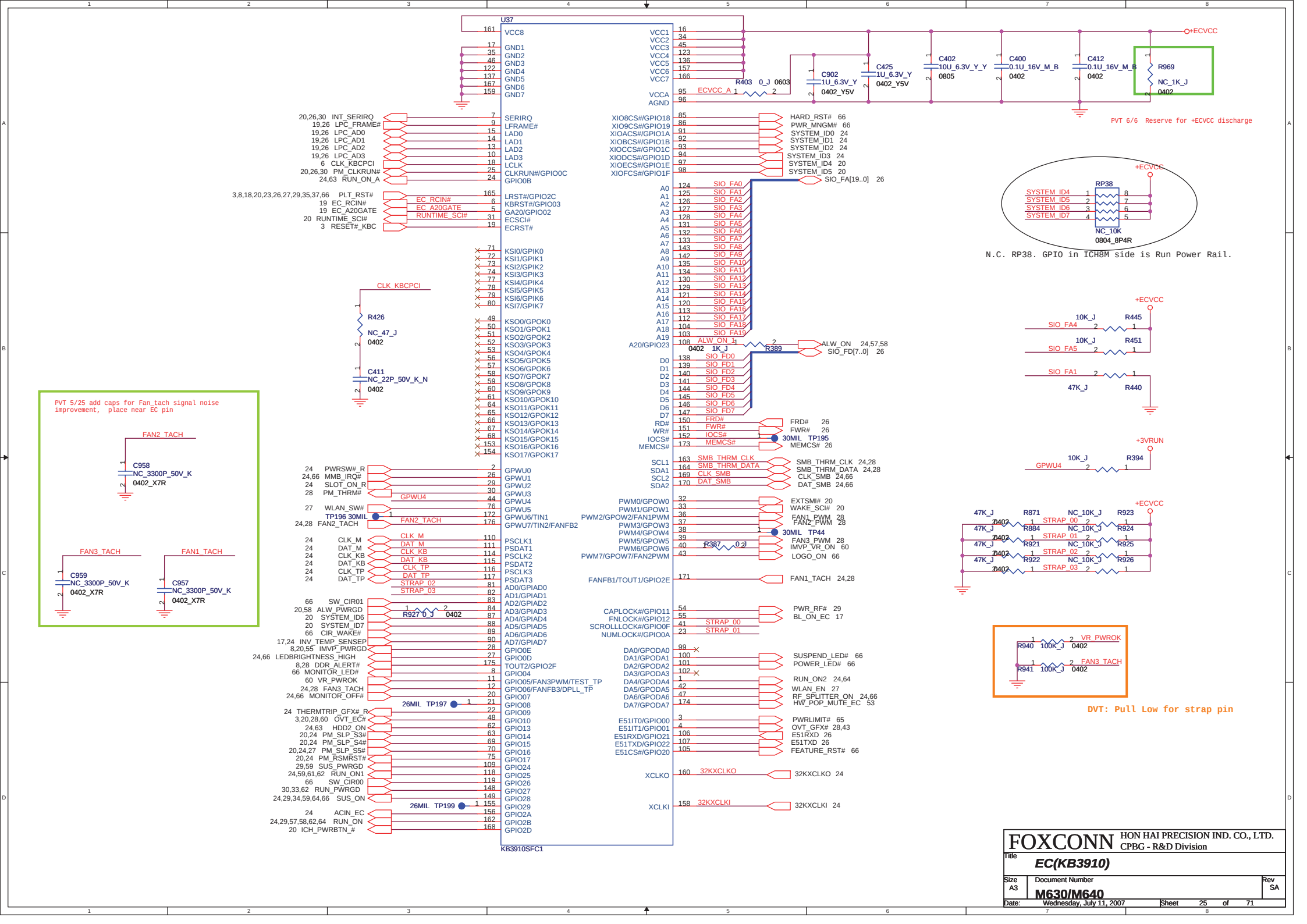
U37
KB3910SFC1
+ECVCC
R403 0_J 0603
C902 1U_6.3V_Y 0402_Y5V
C425 1U_6.3V_Y 0402_Y5V
C402 10U_6.3V_Y_Y 0805
C400 0.1U_16V_M_B 0402
C412 0.1U_16V_M_B 0402
R969 NC_1K_J 0402
PVT 6/6 Reserve for +ECVCC discharge
RP38 NC_10K 0804_8P4R
N.C. RP38. GPIO in ICH8M side is Run Power Rail.
R426 NC_47_J 0402
C411 NC_22P_50V_K_N 0402
PVT 5/25 add caps for Fan_tach signal noise improvement, place near EC pin
C958 NC_3300P_50V_K 0402_X7R
C959 NC_3300P_50V_K 0402_X7R
C957 NC_3300P_50V_K 0402_X7R
R445 10K_J
R451 10K_J
R440 47K_J
R394 10K_J
R389 0402 1K_J
R387 0_J
R927 0_J 0402
TP196 30MIL
TP195 30MIL
TP44 30MIL
TP197 26MIL
TP199 26MIL
R871 R884 R921 R922 R923 R924 R925 R926 47K_J
STRAP_00 STRAP_01 STRAP_02 STRAP_03
R940 R941 100K_J 0402
VR_PWROK
FAN3_TACH
DVT: Pull Low for strap pin
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
EC(KB3910)
Size A3
Document Number
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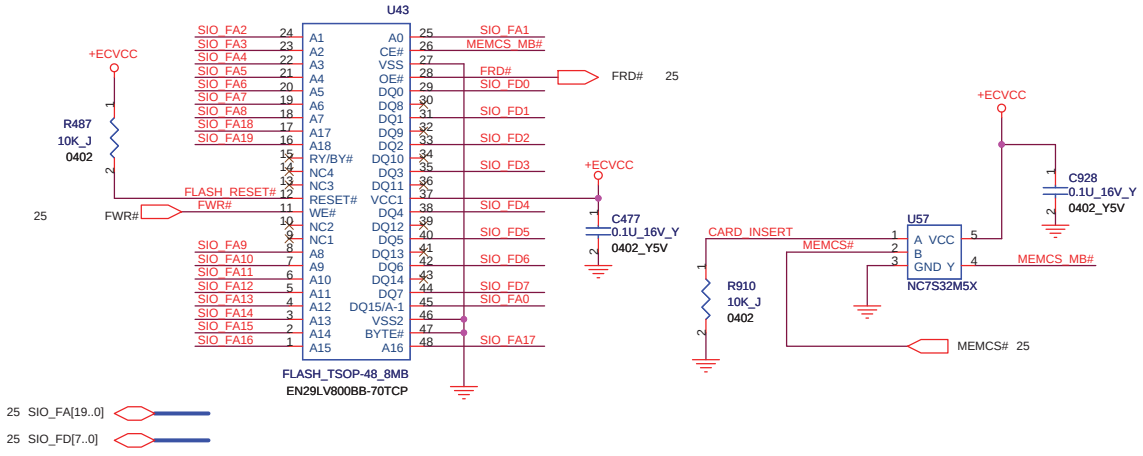
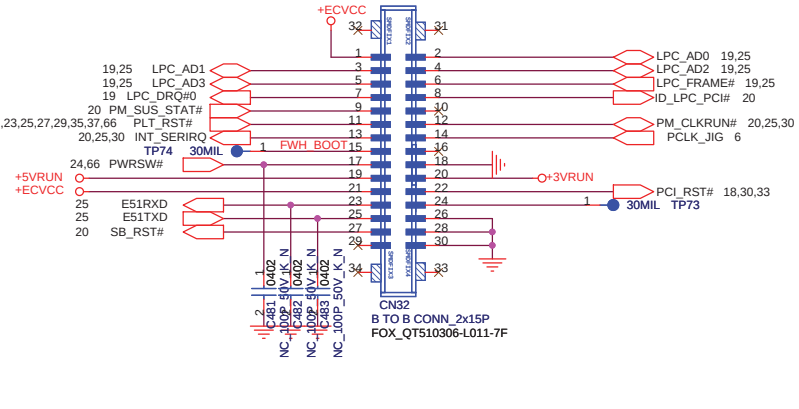


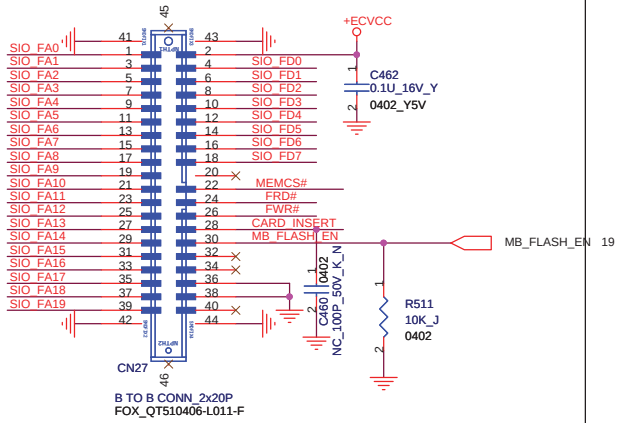
XBUS BIOS ROM

DVT : delete winbond

WINBOND



JIG-120 DEBUG PORT



EXTERNAL XBUS ROM INTERFACE

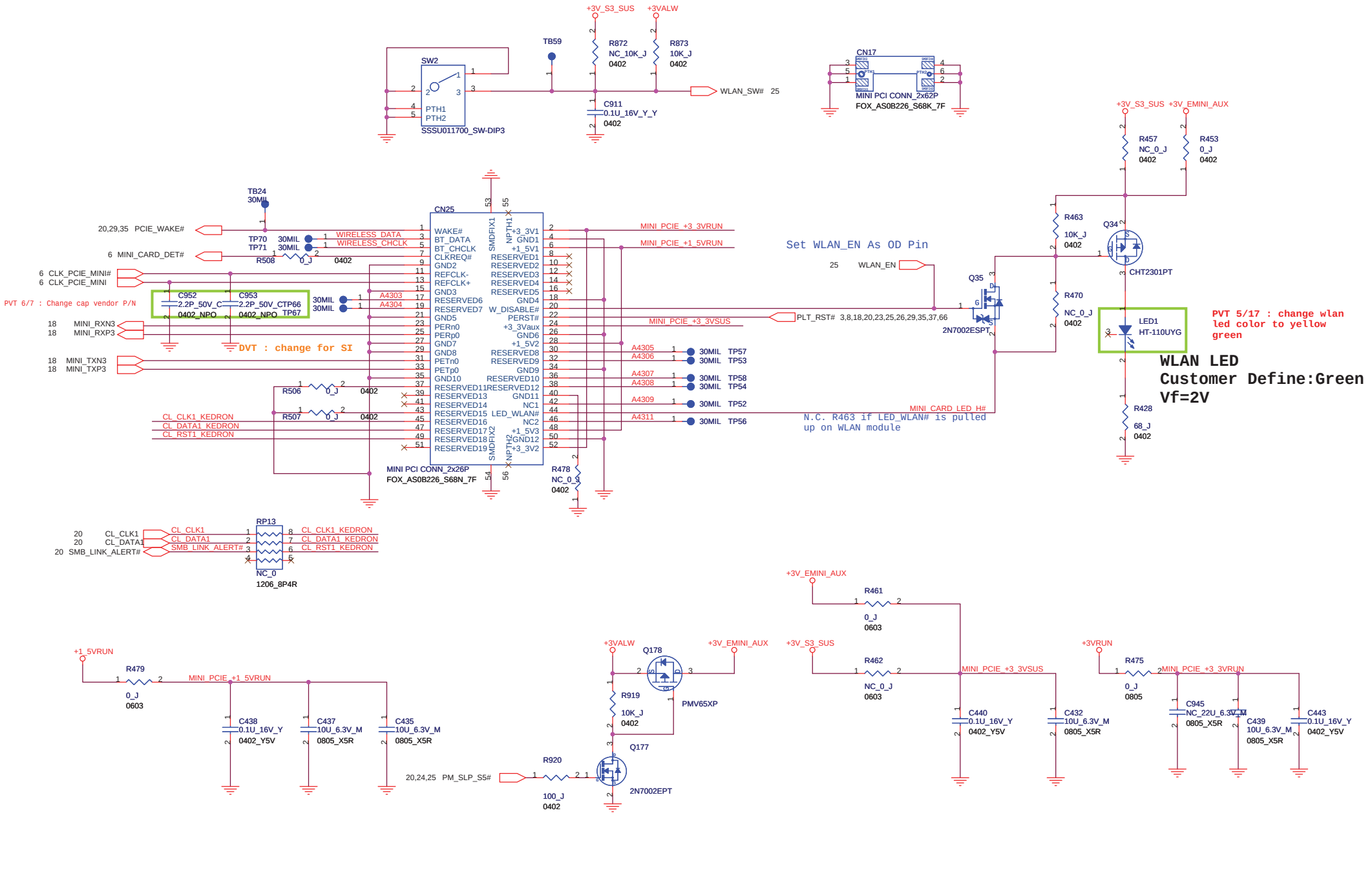
DVT : delete winbond

JTAG INTERFACE

WINBOND

EXTERNAL SPI ROM INTERFACE

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*Flash ROM/X-Bus CONN*	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 26 of 71	



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *Mini_Card*

Size: A3 | Document Number: **M630/M640** | Rev: SA

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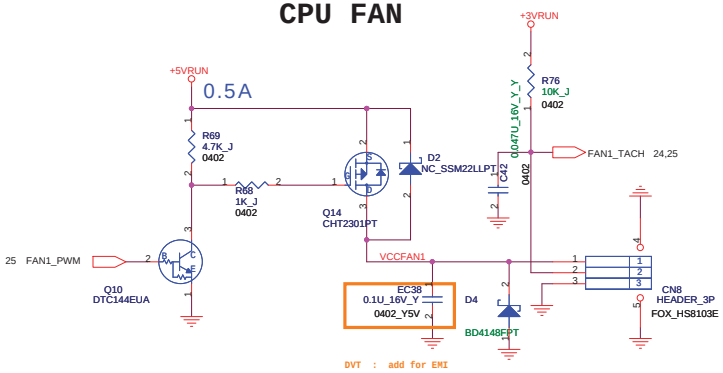
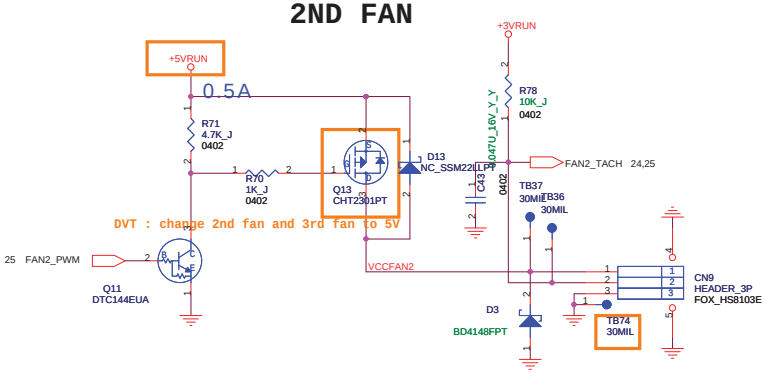
CPU FAN

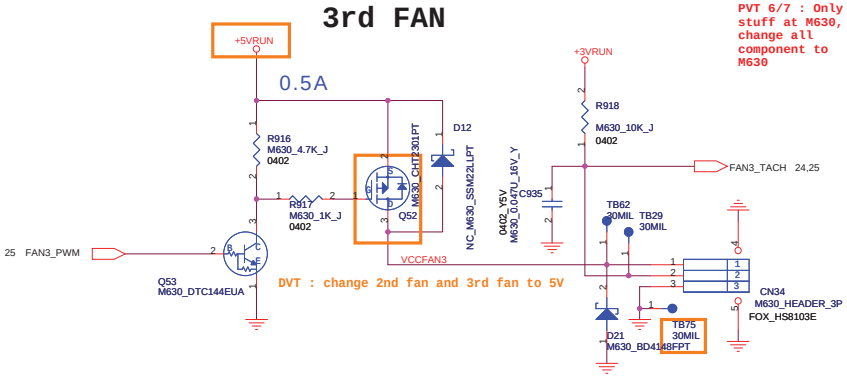


2ND FAN

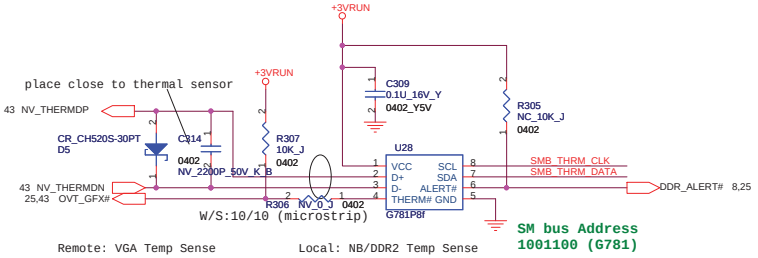


3rd FAN

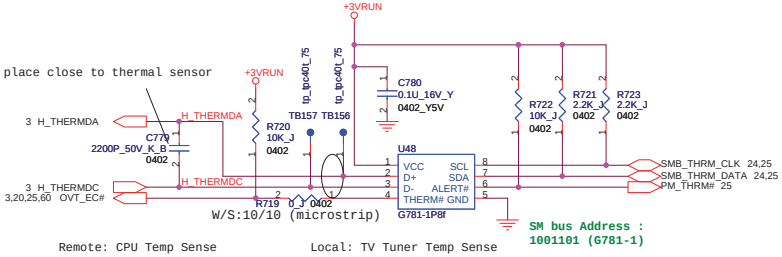
PVT 6/7 : Only stuff at M630, change all component to M630



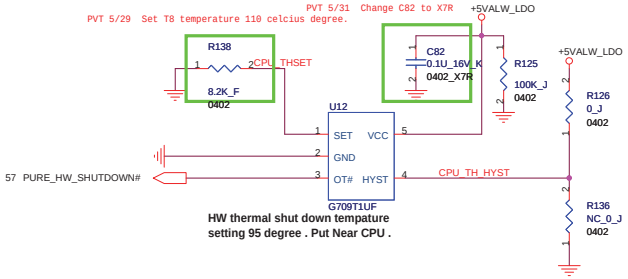
VGA SENSOR



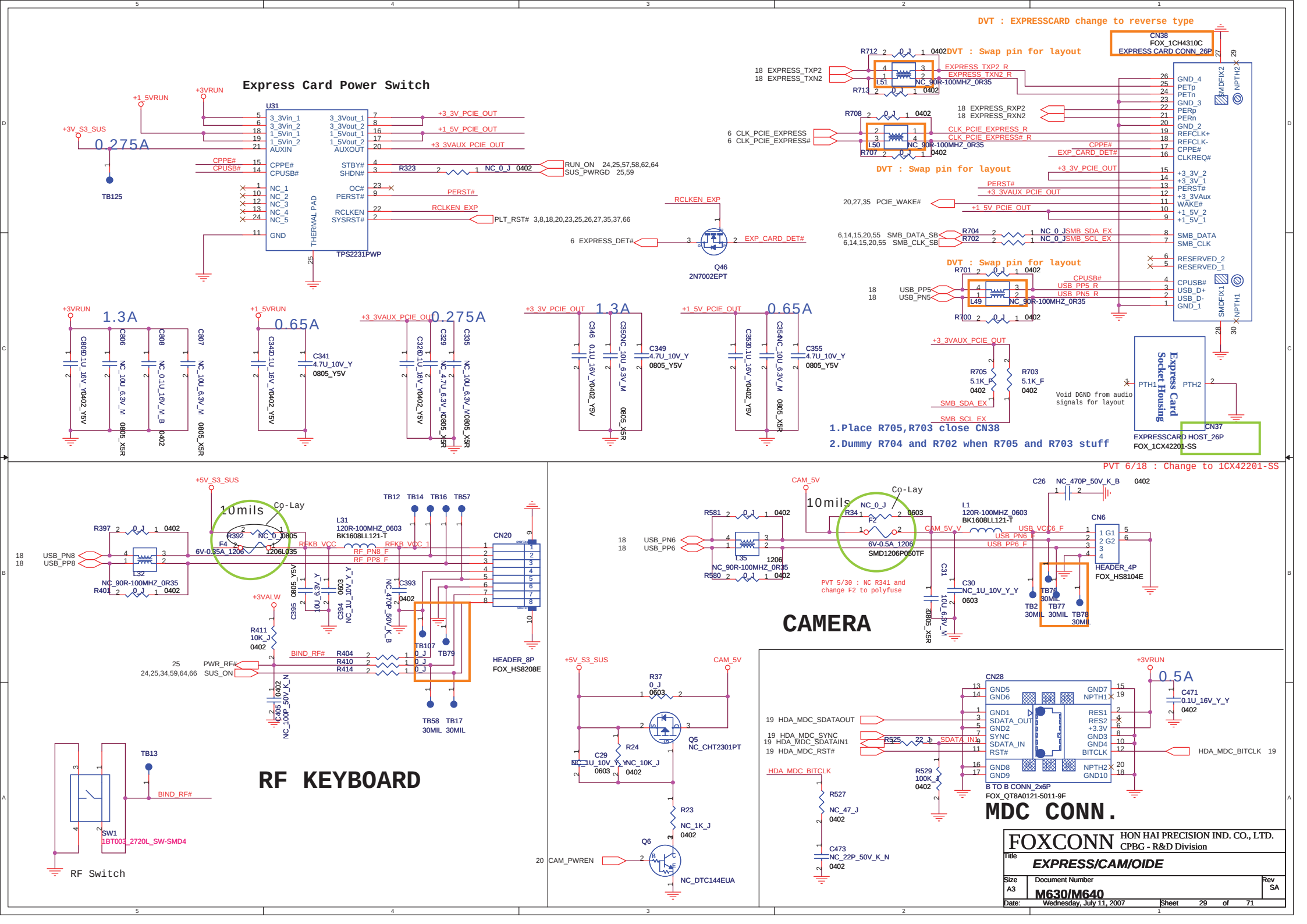
CPU SENSOR



HW THERMAL PROTECTION



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FAN/HW THERMAL PROTECT	
Size: Custom	Document Number: M630/M640	Rev: SA
Date: Friday, July 27, 2007	Sheet 28 of 71	


Express Card Power Switch
U31
TPS2231PWP
THERMAL PAD
TB125
+3V_S3_SUS
0.275A
+1_5VRUN
+3VRUN
+3_3V_PCIE_OUT
+1_5V_PCIE_OUT
+3_3VAUX_PCIE_OUT
RUN_ON 24,25,57,58,62,64
SUS_PWRGD 25,59
PERST#
RCLKEN_EXP
PLT_RST# 3,8,18,20,23,25,26,27,35,37,66
EXPRESS_DET#
EXP_CARD_DET#
Q46
2N7002EPT
1.3A
0.65A
0.275A
DVT : EXPRESSCARD change to reverse type
DVT : Swap pin for layout
CN38
FOX_1CH4310C
EXPRESS CARD CONN_26P
EXPRESS_TXP2
EXPRESS_TXN2
EXPRESS_RXP2
EXPRESS_RXN2
CLK_PCIE_EXPRESS
CLK_PCIE_EXPRESS#
PCIE_WAKE#
SMB_DATA_SB
SMB_CLK_SB
USB_PP5
USB_PN5
Express Card Socket Housing
EXPRESSCARD HOST_26P
FOX_1CX42201-SS
Void DGND from audio signals for layout
1.Place R705,R703 close CN38
2.Dummy R704 and R702 when R705 and R703 stuff
PVT 6/18 : Change to 1CX42201-SS
CAMERA
PVT 5/30 : NC R341 and change F2 to polyfuse
RF KEYBOARD
RF Switch
BIND_RF#
PWR_RF#
SUS_ON
CAM_PWREN
HEADER_8P
FOX_HS8208E
HEADER_4P
FOX_HS8104E
MDC CONN.
B TO B CONN_2x6P
FOX_QT8A0121-5011-9F
HDA_MDC_SDATAOUT
HDA_MDC_SYNC
HDA_MDC_SDATAIN1
HDA_MDC_RST#
HDA_MDC_BITCLK
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
EXPRESS/CAM/OIDE
M630/M640
Wednesday, July 11, 2007
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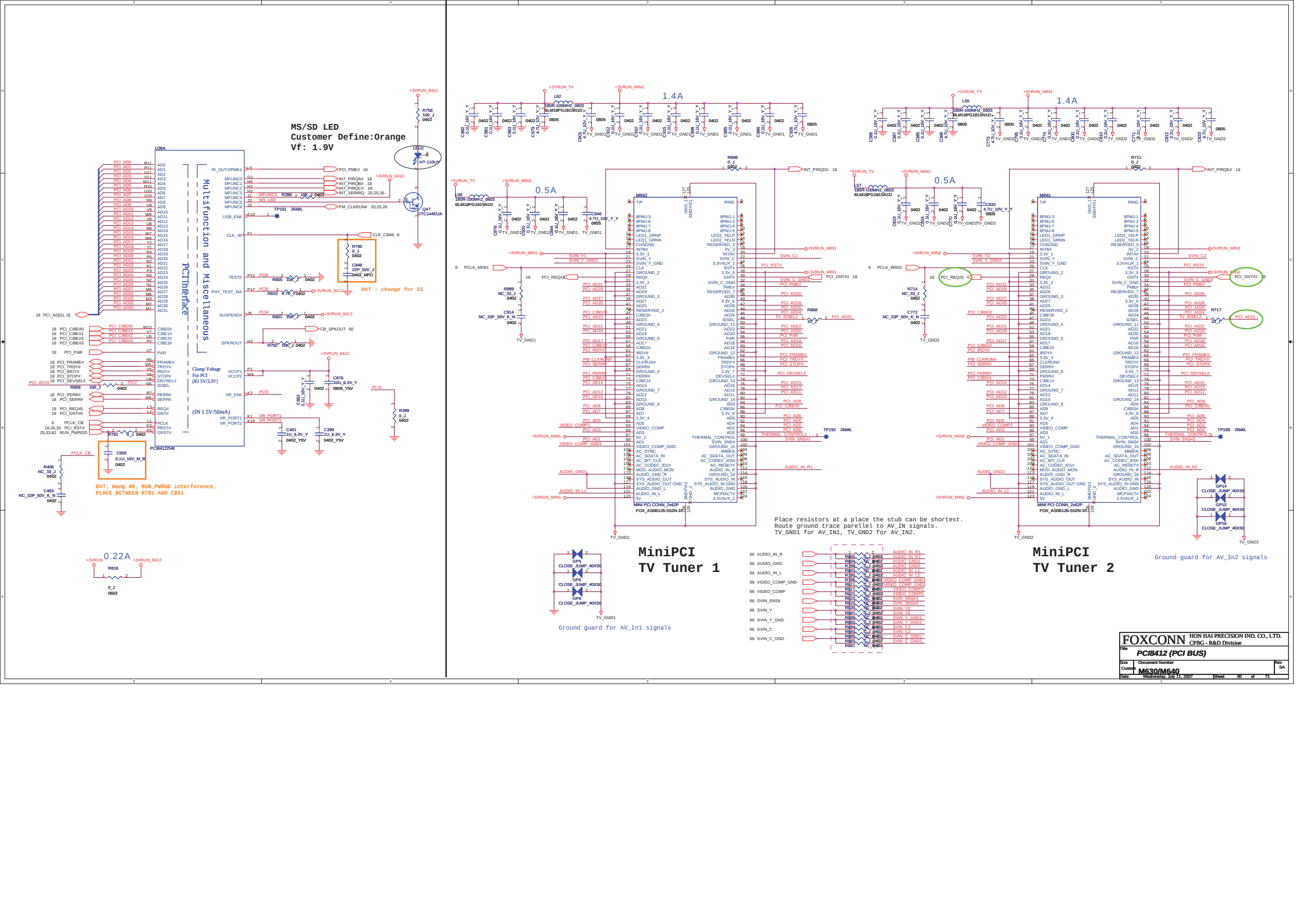
MS/SD LED
Customer Define:Orange
Vf: 1.9V
Multifunction and Miscellaneous
PCI Interface
Clamp Voltage For PCI (IO 5V/3.3V)
(IN 1.5V/50mA)
PCI8412ZHK
DVT: Hang 49, RUN_PWRGD interference, PLACE BETWEEN R791 AND C851
DVT : change for SI
0.22A
1.4A
0.5A
MiniPCI TV Tuner 1
MiniPCI TV Tuner 2
Ground guard for AV_In1 signals
Ground guard for AV_In2 signals
Place resistors at a place the stub can be shortest.
Route ground trace parellel to AV_IN signals.
TV_GND1 for AV_IN1, TV_GND2 for AV_IN2.
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
PCI8412 (PCI BUS)
M630/M640
Wednesday, July 11, 2007
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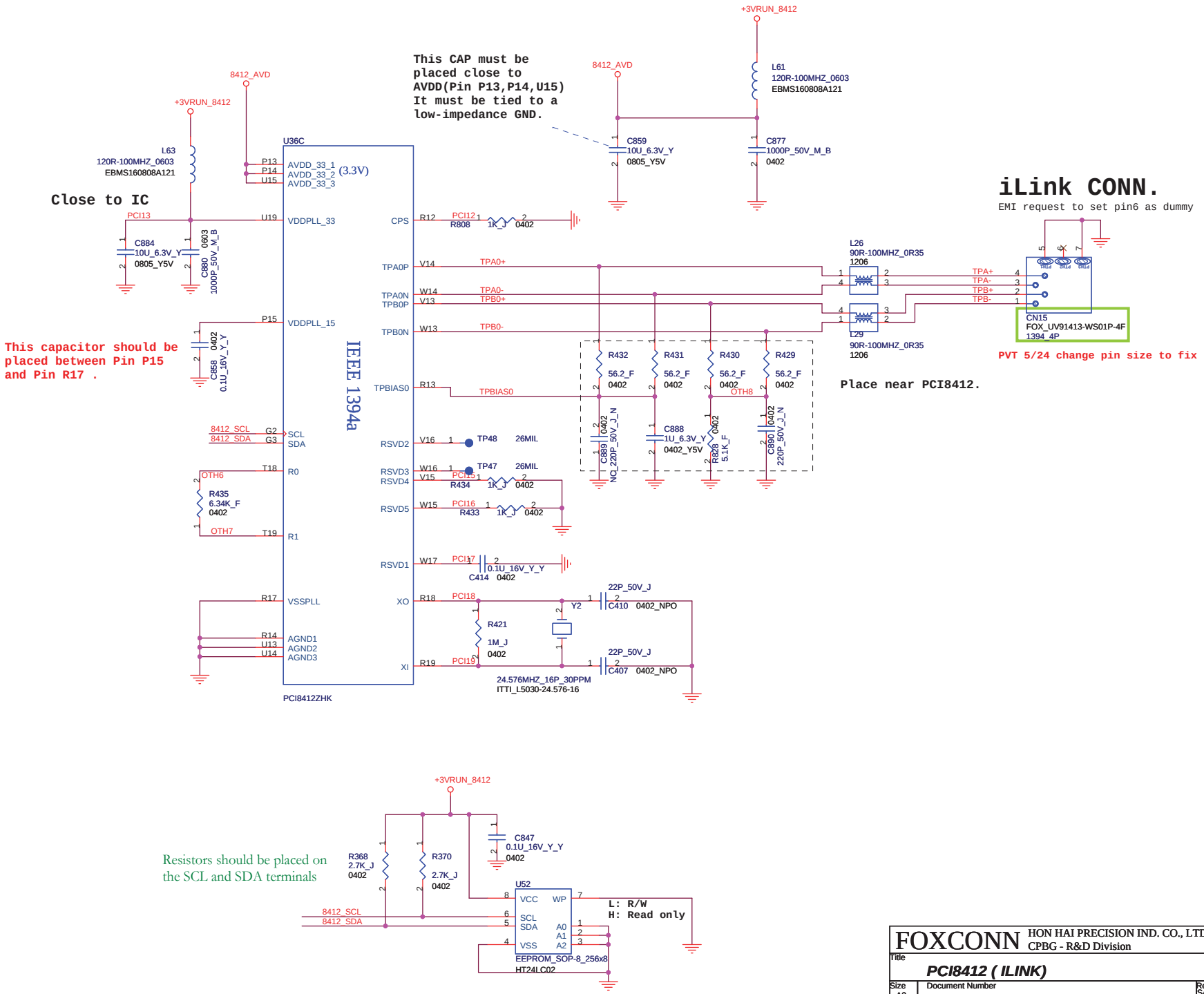
This CAP must be placed close to AVDD(Pin P13,P14,U15) It must be tied to a low-impedance GND.
Close to IC
This capacitor should be placed between Pin P15 and Pin R17 .
Place near PCI8412.
iLink CONN.
EMI request to set pin6 as dummy
PVT 5/24 change pin size to fix
U36C
PCI8412ZHK
IEEE 1394a
AVDD_33_1
AVDD_33_2 (3.3V)
AVDD_33_3
VDDPLL_33
VDDPLL_15
VSSPLL
AGND1
AGND2
AGND3
SCL
SDA
R0
R1
CPS
TPA0P
TPA0N
TPB0P
TPB0N
TPBIAS0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
XO
XI
L63 120R-100MHZ_0603 EBMS160808A121
L61 120R-100MHZ_0603 EBMS160808A121
L26 90R-100MHZ_0R35 1206
L29 90R-100MHZ_0R35 1206
CN15 FOX_UV91413-WS01P-4F 1394_4P
24.576MHZ_16P_30PPM ITTI_L5030-24.576-16
Resistors should be placed on the SCL and SDA terminals
U52
EEPROM_SOP-8_256x8
HT24LC02
L: R/W
H: Read only
FOXCONN
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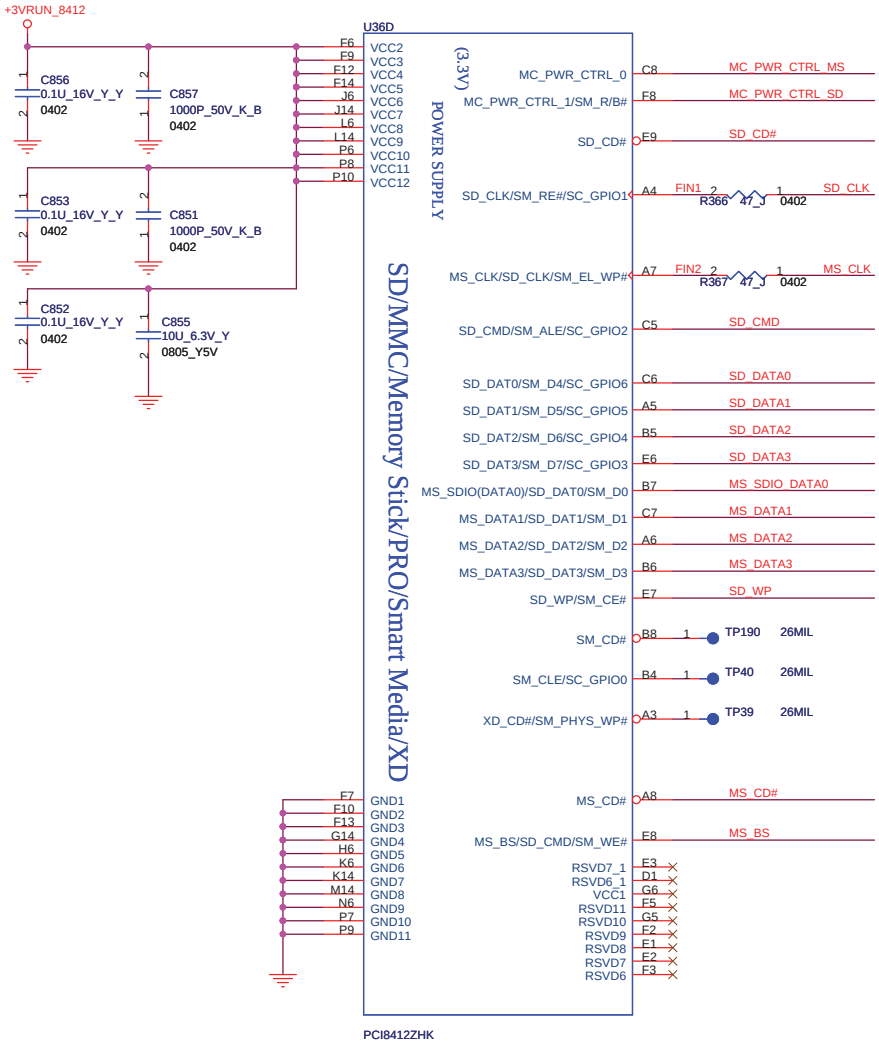
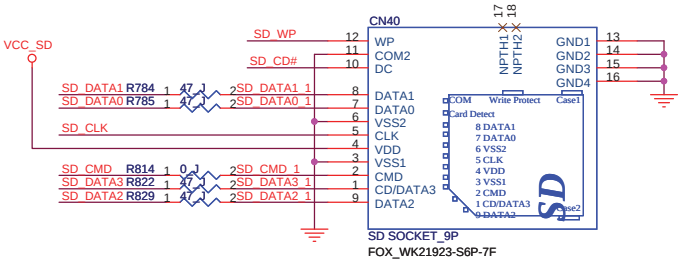
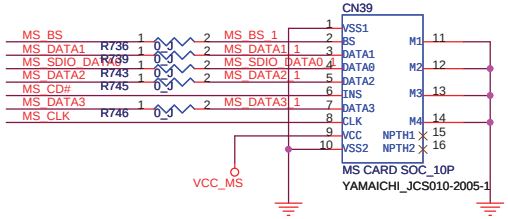
CPBG - R&D Division
PCI8412 (ILINK)
M630/M640
Wednesday, July 11, 2007

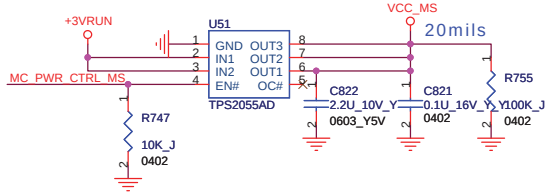


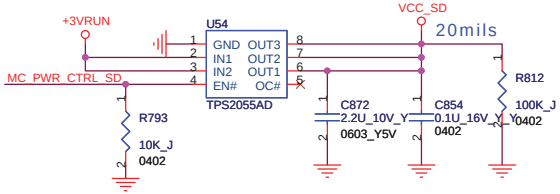
SD

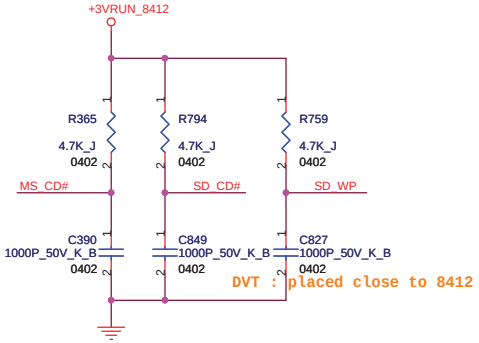


MS Pro/Duo









FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI8412 (MS/SD)/MDC	
Size A3	Document Number M630/M640	Rev SA
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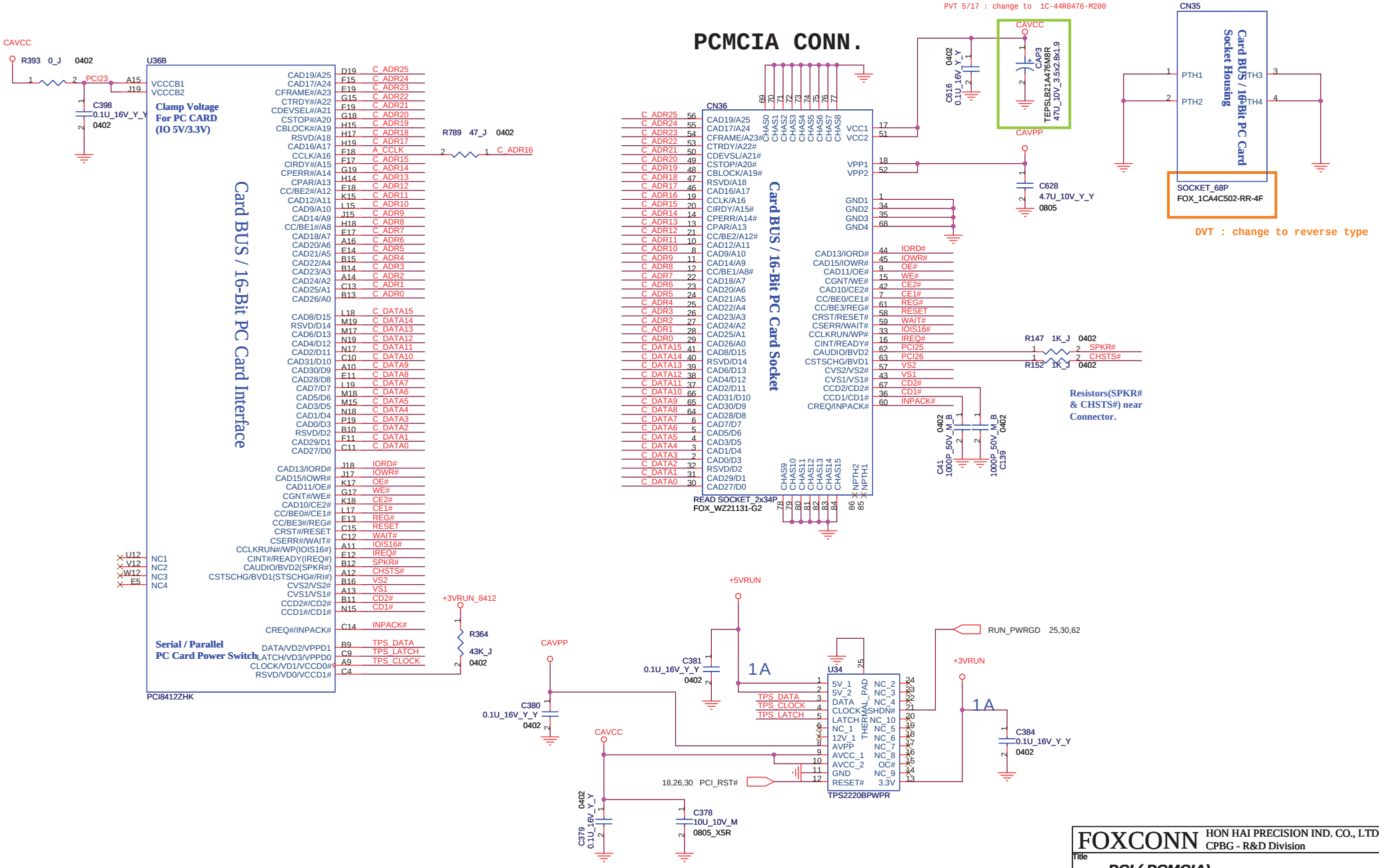
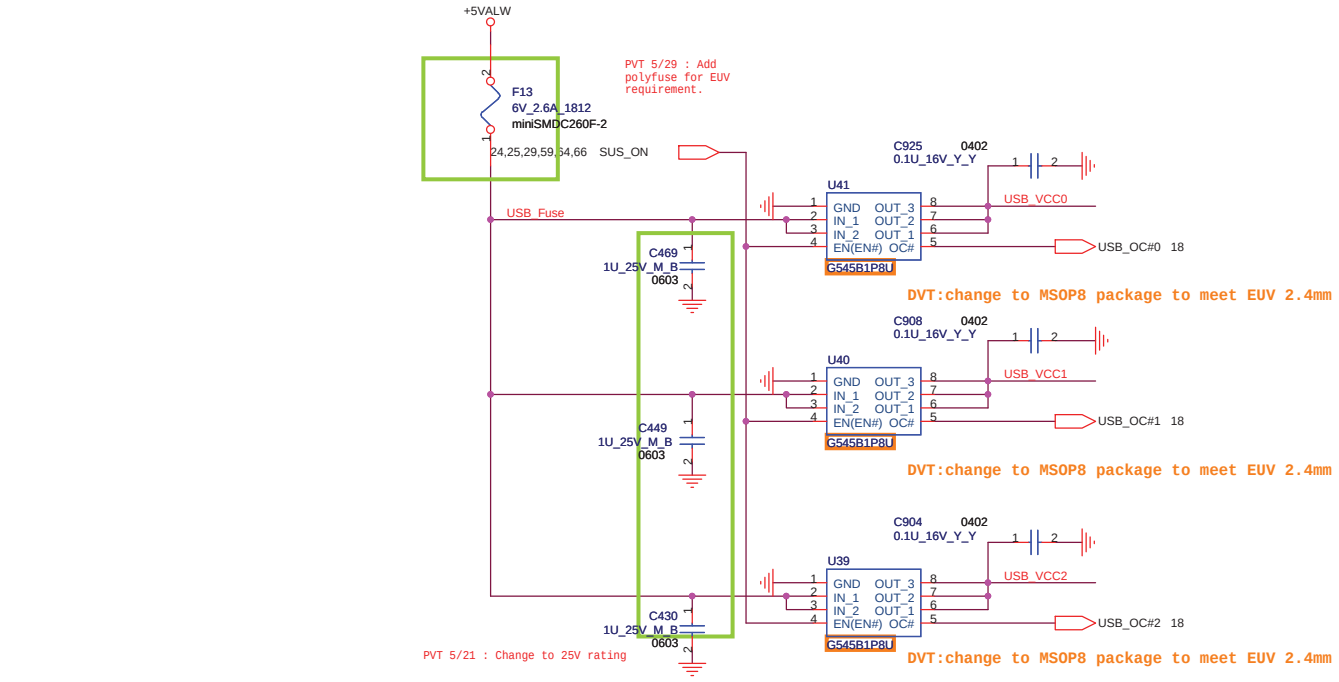
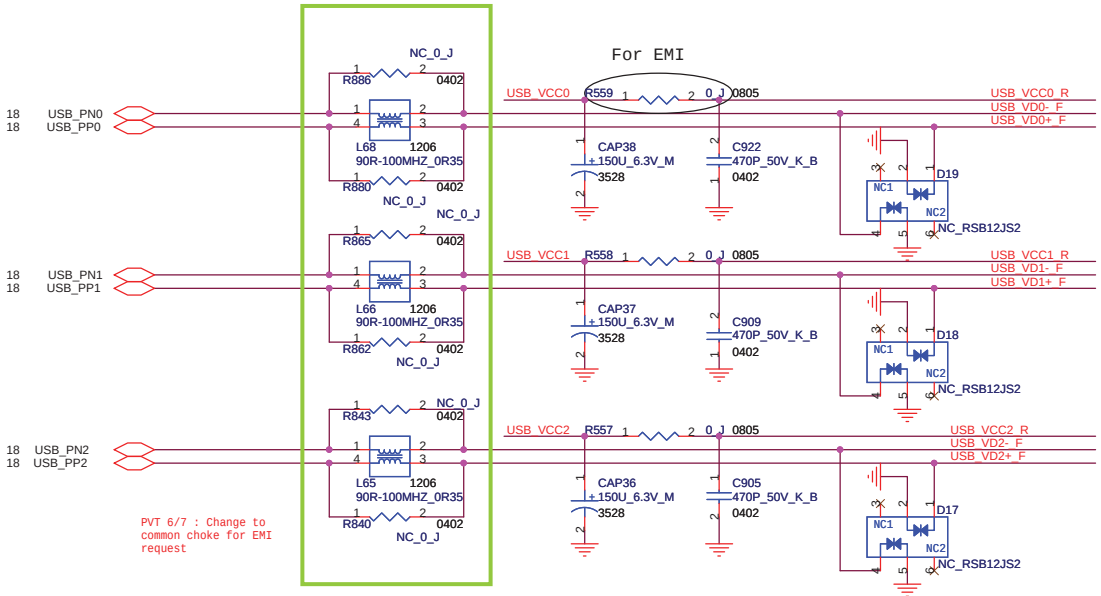
PCMCIA CONN.

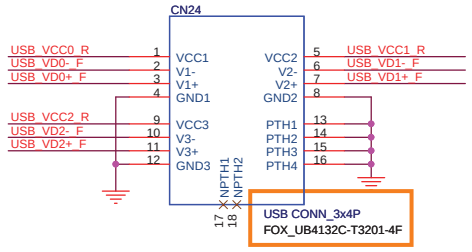


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	PCI (PCMCIA)		
Size A3	Document Number		Rev SA
Date: Wednesday, July 11, 2007	Sheet 33 of 71		





REAR USB CONN X 3



DVT change to black color

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: USB2.0 PORT		
Size: A3	Document Number: M630/M640	Rev: SA
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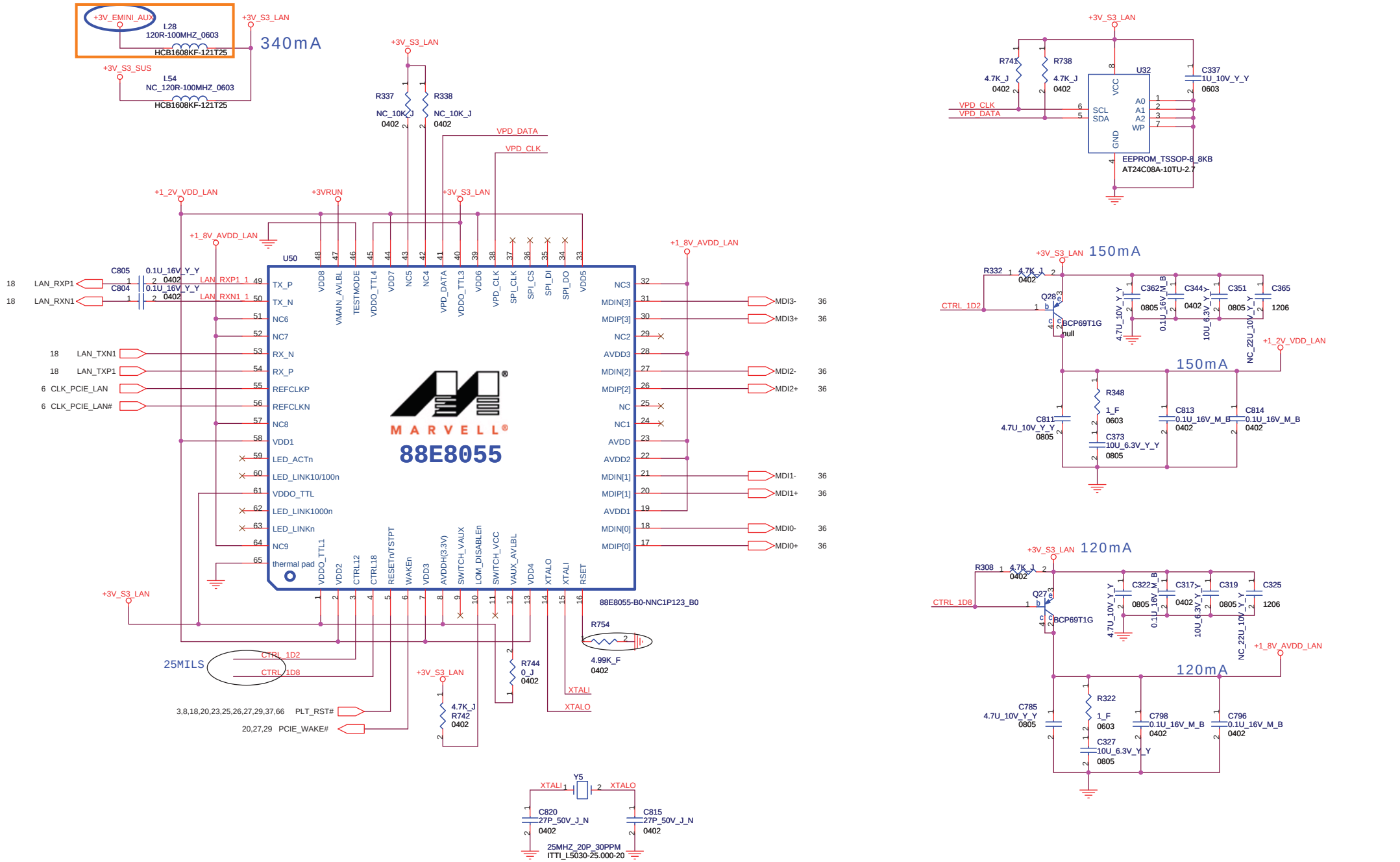
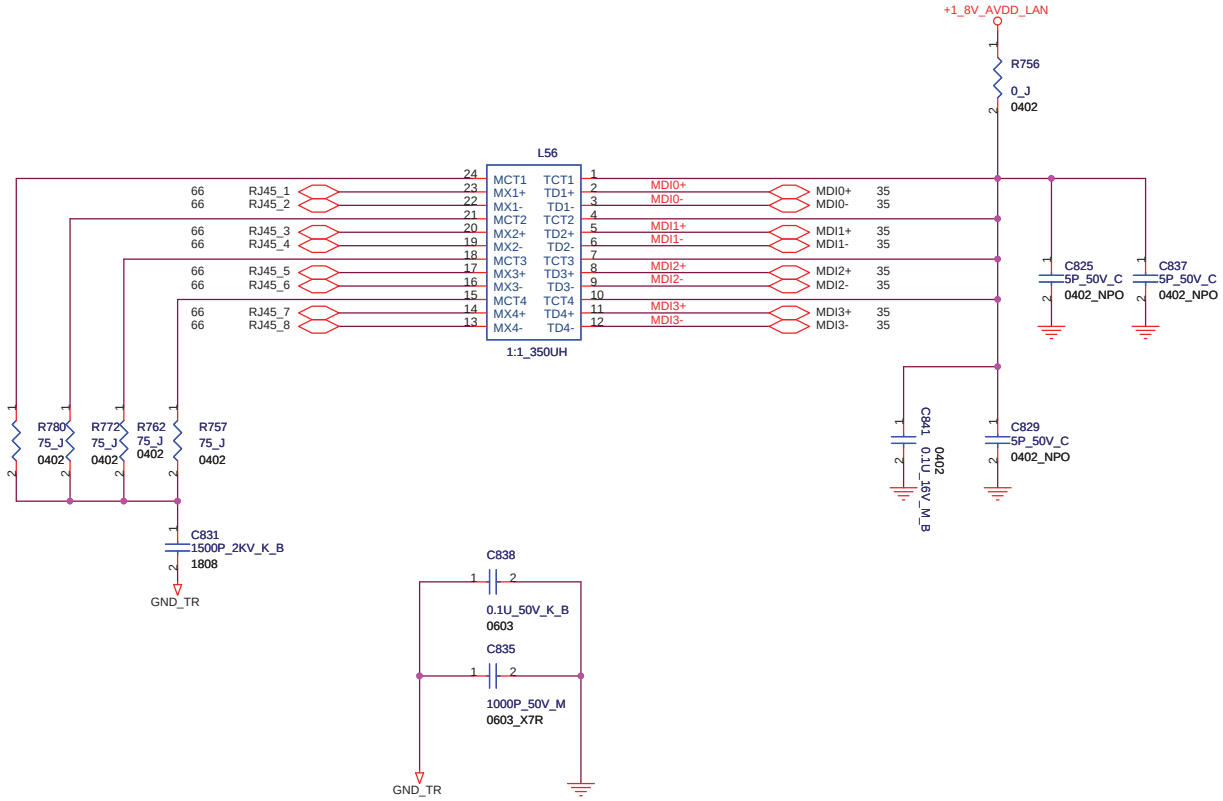
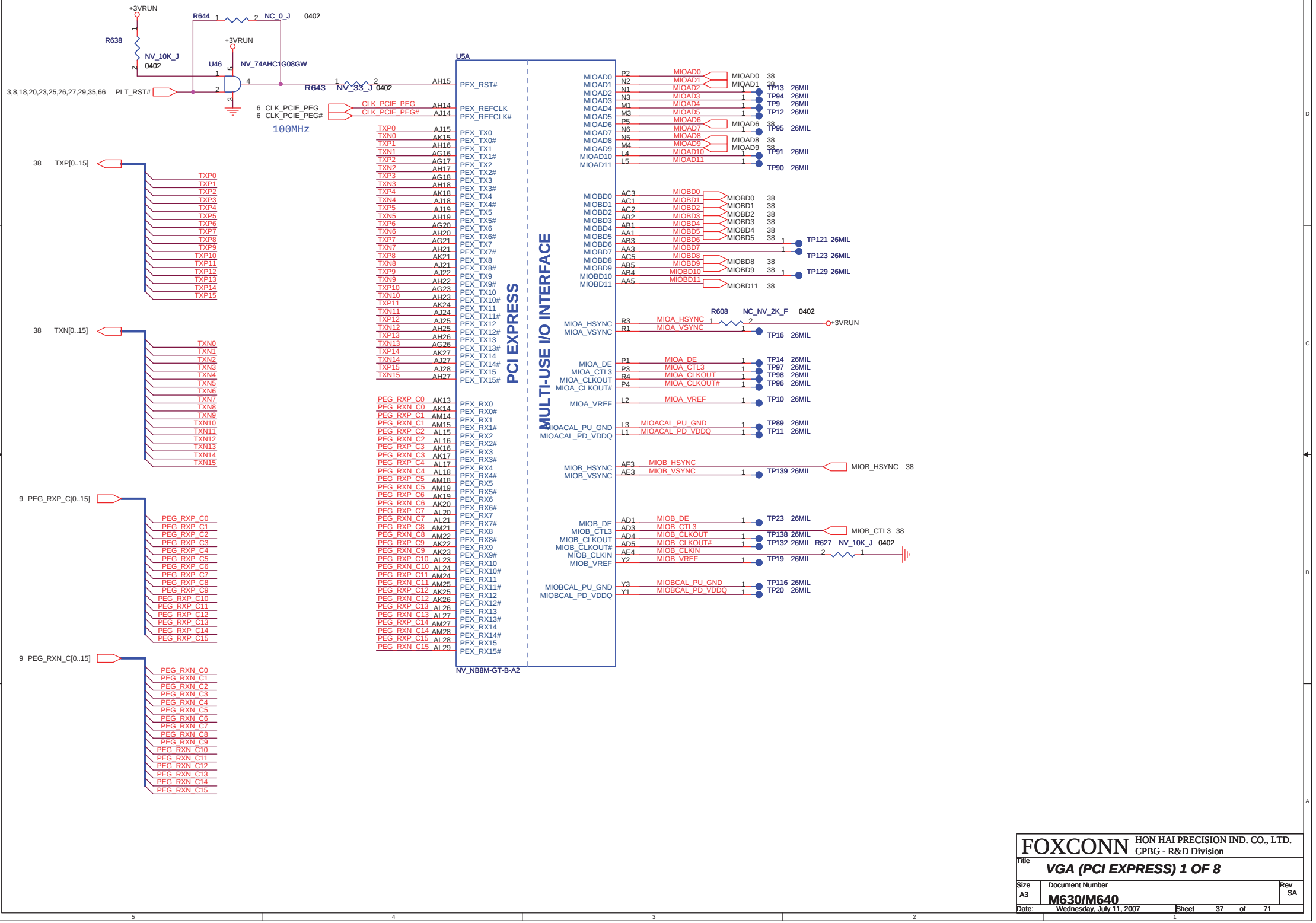
To support S4 wake up **DVT : support S4 wake up , power change to +3V_EMINI_AUX**



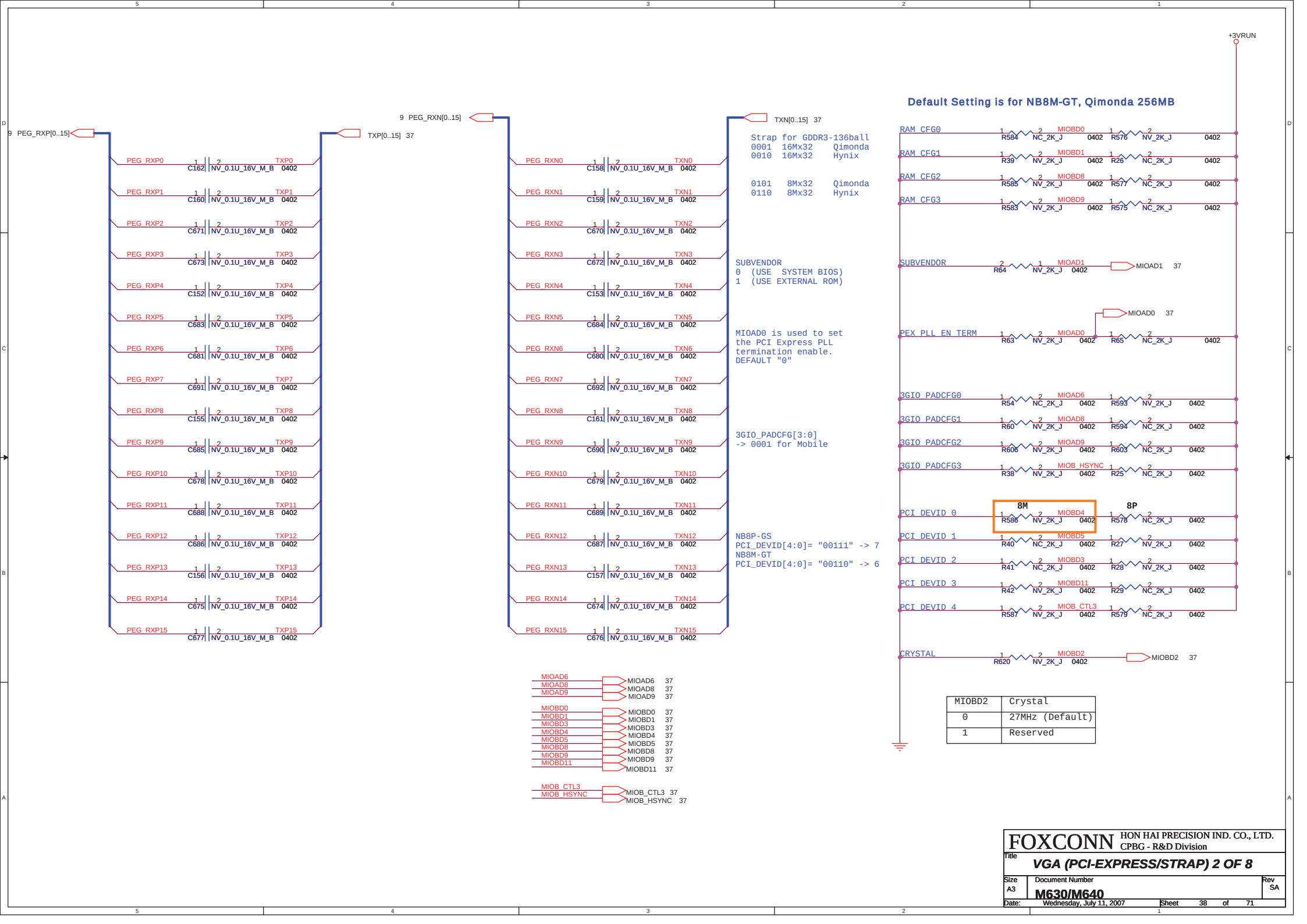
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN Controller	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 35 of 71	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN Transformer	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 36 of 71	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	VGA (PCI EXPRESS) 1 OF 8		
Size A3	Document Number M630/M640		Rev SA
Date: Wednesday, July 11, 2007	Sheet 37 of 71		



MIOBD2	Crystal
0	27MHz (Default)
1	Reserved

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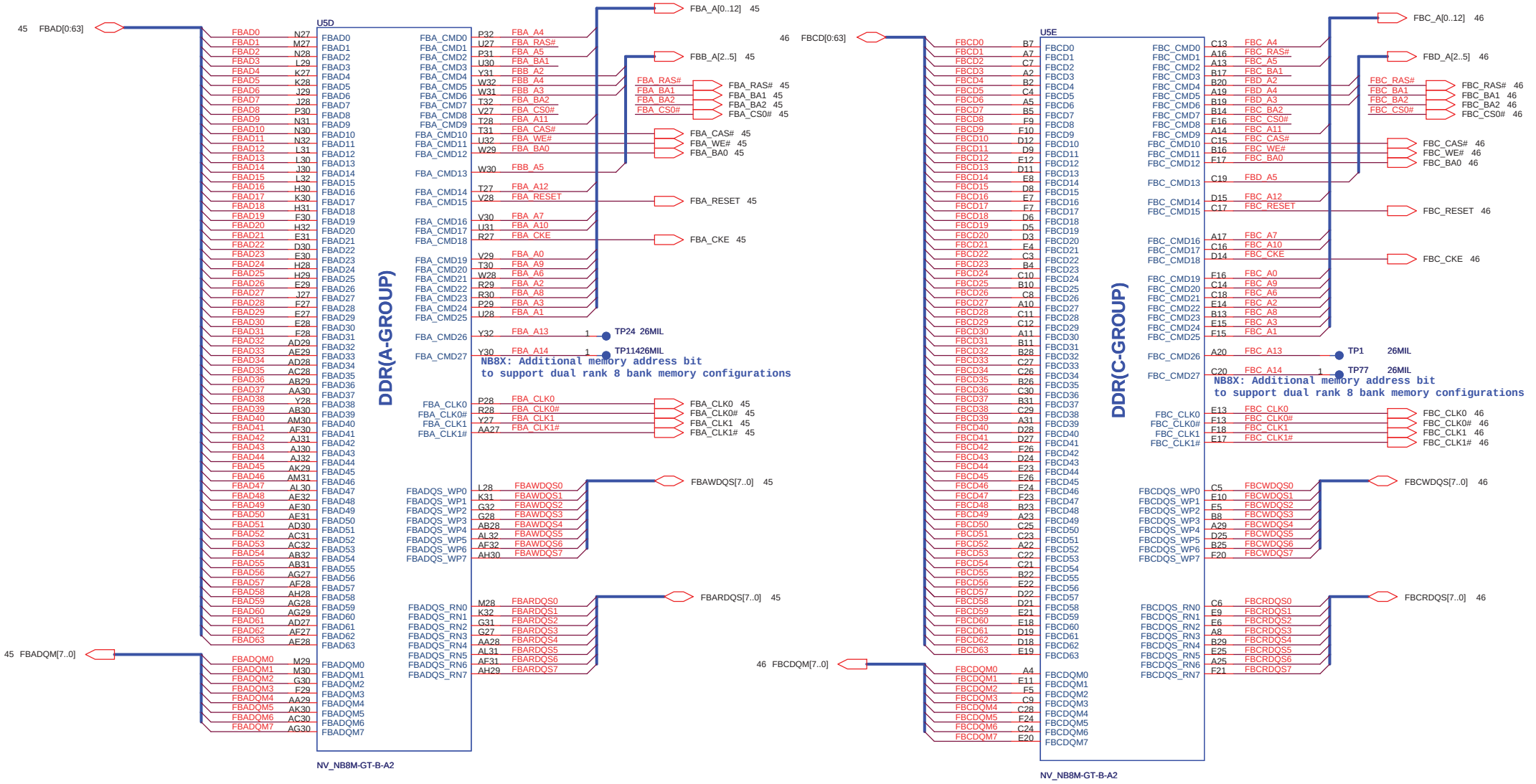
CPBG - R&D Division

Title: VGA (PCI-EXPRESS/STRAP) 2 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 38 of 71

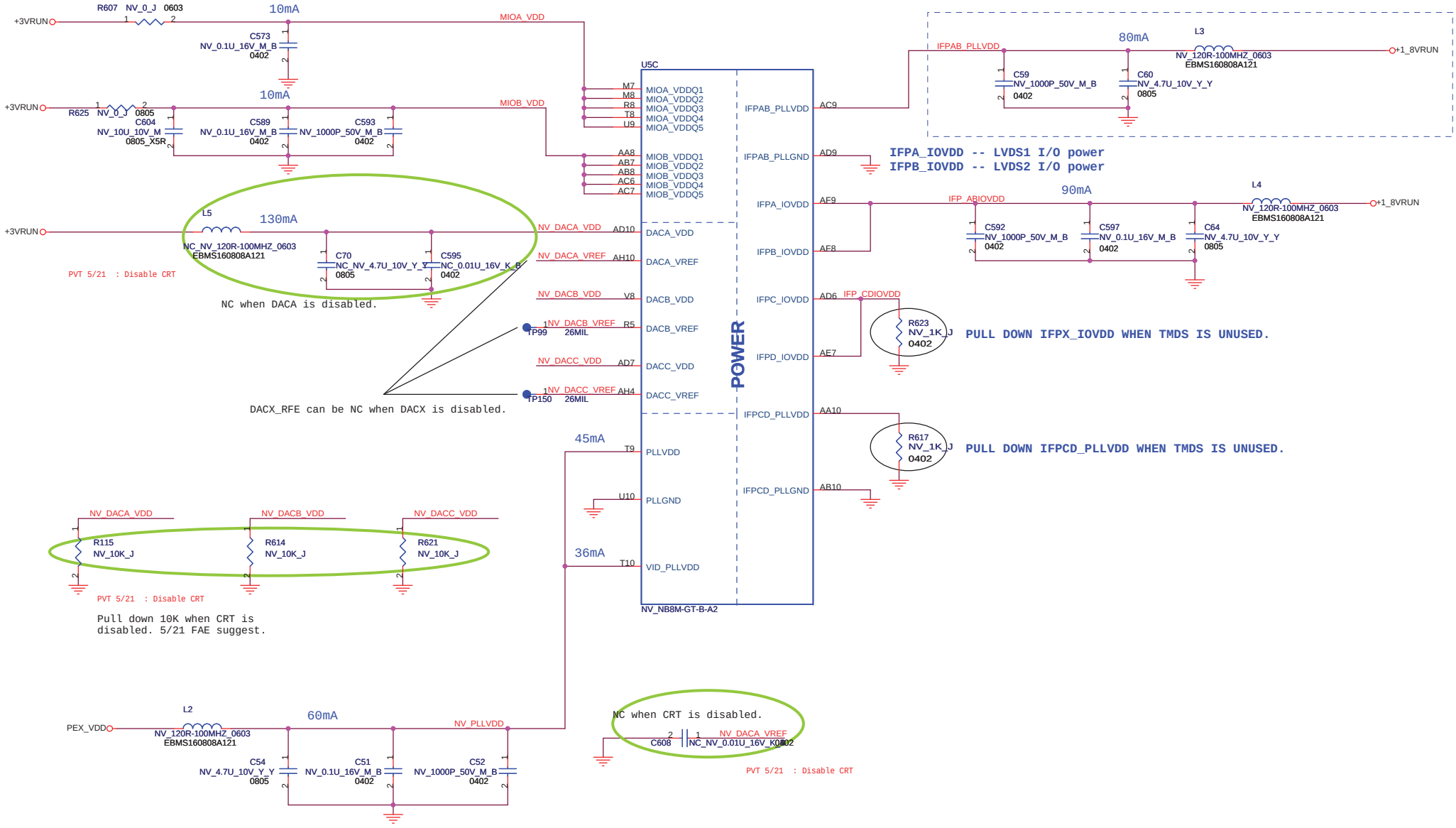


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

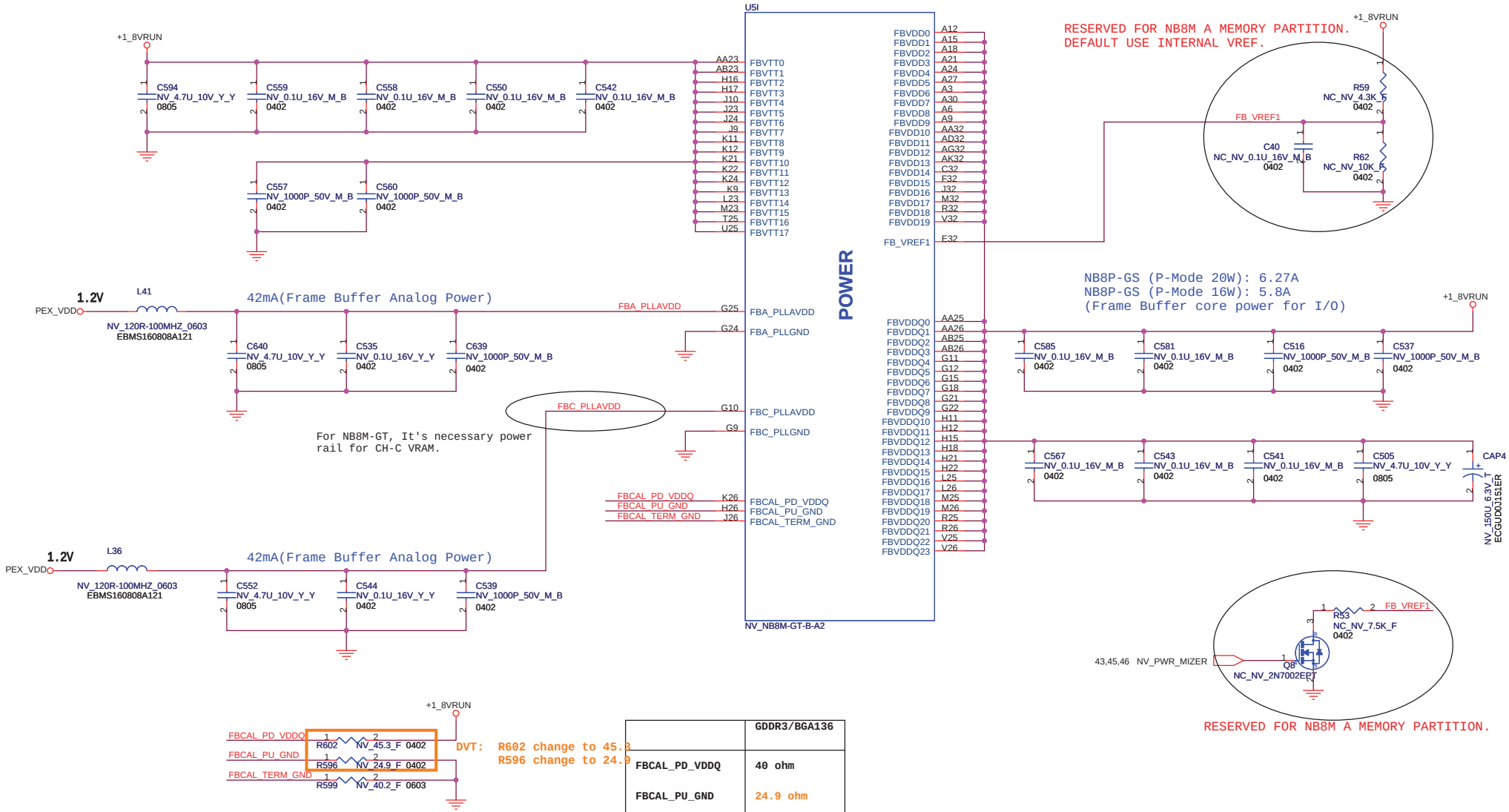
Title: VGA (GDDR) 3 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 39 of 71



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (POWER) 4 OF 8	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 40 of 71	



	GDDR3/BGA136
FBCAL_PD_VDDQ	40 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40 ohm

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Title: VGA (POWER) 5 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

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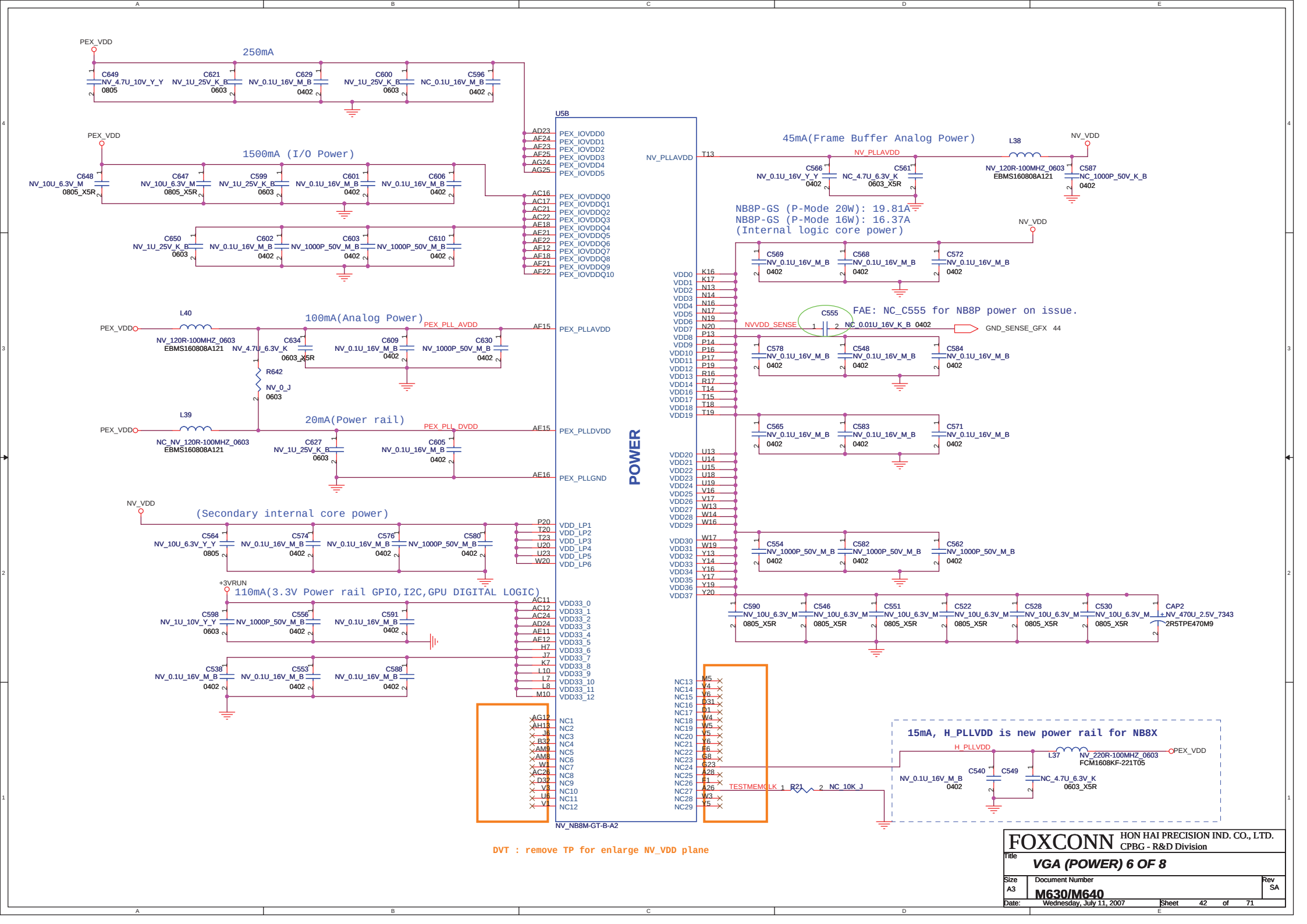
PEX_VDD
250mA
C649 NV_4.7U_10V_Y_Y 0805
C621 NV_1U_25V_K_B 0603
C629 NV_0.1U_16V_M_B 0402
C600 NV_1U_25V_K_B 0603
C596 NC_0.1U_16V_M_B 0402
1500mA (I/O Power)
C648 NV_10U_6.3V_M 0805_X5R
C647 NV_10U_6.3V_M 0805_X5R
C599 NV_1U_25V_K_B 0603
C601 NV_0.1U_16V_M_B 0402
C606 NV_0.1U_16V_M_B 0402
C650 NV_1U_25V_K_B 0603
C602 NV_0.1U_16V_M_B 0402
C603 NV_1000P_50V_M_B 0402
C610 NV_1000P_50V_M_B 0402
U5B
AD23 AF24 AF23 AF25 AG24 AG25 PEX_IOVDD0 PEX_IOVDD1 PEX_IOVDD2 PEX_IOVDD3 PEX_IOVDD4 PEX_IOVDD5
AC16 AC17 AC21 AC22 AE18 AE21 AE22 AF12 AF18 AF21 AE22 PEX_IOVDDQ0 PEX_IOVDDQ1 PEX_IOVDDQ2 PEX_IOVDDQ3 PEX_IOVDDQ4 PEX_IOVDDQ5 PEX_IOVDDQ6 PEX_IOVDDQ7 PEX_IOVDDQ8 PEX_IOVDDQ9 PEX_IOVDDQ10
100mA(Analog Power)
L40
PEX_VDD
NV_120R-100MHZ_0603 EBMS160808A121
C634 NV_4.7U_6.3V_K 0603_X5R
C609 NV_0.1U_16V_M_B 0402
C630 NV_1000P_50V_M_B 0402
PEX_PLL_AVDD
AE15 PEX_PLLAVDD
R642 NV_0_J 0603
20mA(Power rail)
L39
PEX_VDD
NC_NV_120R-100MHZ_0603 EBMS160808A121
C627 NV_1U_25V_K_B 0603
C605 NV_0.1U_16V_M_B 0402
PEX_PLL_DVDD
AE15 PEX_PLLDVDD
AE16 PEX_PLLGND
NV_VDD
(Secondary internal core power)
C564 NV_10U_6.3V_Y_Y 0805
C574 NV_0.1U_16V_M_B 0402
C576 NV_0.1U_16V_M_B 0402
C580 NV_1000P_50V_M_B 0402
P20 T20 T23 U20 U23 W20 VDD_LP1 VDD_LP2 VDD_LP3 VDD_LP4 VDD_LP5 VDD_LP6
+3VRUN
110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)
C598 NV_1U_10V_Y_Y 0603
C556 NV_1000P_50V_M_B 0402
C591 NV_0.1U_16V_M_B 0402
C538 NV_0.1U_16V_M_B 0402
C553 NV_0.1U_16V_M_B 0402
C588 NV_0.1U_16V_M_B 0402
AC11 AC12 AC24 AD24 AE11 AE12 H7 J7 K7 L10 L7 L8 M10 VDD33_0 VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5 VDD33_6 VDD33_7 VDD33_8 VDD33_9 VDD33_10 VDD33_11 VDD33_12
AG12 AH13 J6 R32 AM9 AM8 W1 AC26 D32 V3 U6 V1 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12
NV_NB8M-GT-B-A2
POWER
NV_PLLAVDD T13
45mA(Frame Buffer Analog Power)
L38
NV_VDD
NV_PLLAVDD
C566 NV_0.1U_16V_Y_Y 0402
C561 NC_4.7U_6.3V_K 0603_X5R
NV_120R-100MHZ_0603 EBMS160808A121
C587 NC_1000P_50V_K_B 0402
NB8P-GS (P-Mode 20W): 19.81A
NB8P-GS (P-Mode 16W): 16.37A
(Internal logic core power)
NV_VDD
C569 NV_0.1U_16V_M_B 0402
C568 NV_0.1U_16V_M_B 0402
C572 NV_0.1U_16V_M_B 0402
C555
FAE: NC_C555 for NB8P power on issue.
NVVDD_SENSE
NC_0.01U_16V_K_B 0402
GND_SENSE_GFX 44
C578 NV_0.1U_16V_M_B 0402
C548 NV_0.1U_16V_M_B 0402
C584 NV_0.1U_16V_M_B 0402
C565 NV_0.1U_16V_M_B 0402
C583 NV_0.1U_16V_M_B 0402
C571 NV_0.1U_16V_M_B 0402
C554 NV_1000P_50V_M_B 0402
C582 NV_1000P_50V_M_B 0402
C562 NV_1000P_50V_M_B 0402
C590 NV_10U_6.3V_M 0805_X5R
C546 NV_10U_6.3V_M 0805_X5R
C551 NV_10U_6.3V_M 0805_X5R
C522 NV_10U_6.3V_M 0805_X5R
C528 NV_10U_6.3V_M 0805_X5R
C530 NV_10U_6.3V_M 0805_X5R
CAP2 NV_470U_2.5V_7343 2R5TPE470M9
VDD0 K16 VDD1 K17 VDD2 N13 VDD3 N14 VDD4 N16 VDD5 N17 VDD6 N19 VDD7 N20 VDD8 P13 VDD9 P14 P16 VDD10 P17 VDD11 P19 VDD12 R16 VDD13 R17 VDD14 T14 VDD16 T15 VDD17 T18 VDD18 T19 VDD19
VDD20 U13 VDD21 U14 VDD22 U15 VDD23 U18 VDD24 U19 VDD25 V16 VDD26 V17 VDD27 W13 VDD28 W14 VDD29 W16
VDD30 W17 VDD31 W19 VDD32 Y13 VDD33 Y14 VDD34 Y16 VDD35 Y17 VDD36 Y19 VDD37 Y20
NC13 M5 NC14 V4 NC15 V6 NC16 D31 NC17 D1 NC18 W4 NC19 W5 NC20 Y5 NC21 Y6 NC22 E6 NC23 G8 NC24 G23 NC25 A28 NC26 F1 NC27 A26 NC28 W3 NC29 Y5
TESTMEMCLK
R21 NC_10K_J
15mA, H_PLLVDD is new power rail for NB8X
H_PLLVDD
L37 NV_220R-100MHZ_0603 FCM1608KF-221T05
PEX_VDD
C540 NV_0.1U_16V_M_B 0402
C549 NC_4.7U_6.3V_K 0603_X5R
DVT : remove TP for enlarge NV_VDD plane
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NB8X: Slave I2C/SMBUS
compatible interface. (Addr: 0x9e)

2006/8/30 Update

	I/O	Inter pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)	
GPIO1	I	Yes	DVI Hot Plug Detect 1(HPD1)	
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	**Active High**
GPIO3	O	No	Panel Power(LCD0_VDD)	**Active Low**
GPIO4	O	Yes	LCDBacklight enable(LCD0_BL_EN)	**Active High**
GPIO5	O	Yes	GPU Voltage selection (GPU_VID0)	
GPIO6	O	Yes	GPU Voltage selection (GPU_VID1)	
GPIO7	O	Yes	GPU/Memory Voltage selection(GPU_VID2/MEM_VID)	
GPIO8	I/OD	No	Over Temperature Shutdown	**Active Low**
GPIO9	I/OD	No	THERMAL ALERT I/O, FAN PWM Control	**Active Low**
GPIO10	I/O	No	Memory Vref switch(MEM_VREF)	
GPIO11	O	No	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)	
GPIO12	I	No	AC power detect input (AC_DET)	
GPIO13	O	No	Power supply control (PWR_CTRL0)	
GPIO14	O	No	Power supply control (PWR_CTRL1)	

Could be NC if HDCP is not used.

Boundary scans in conjunction with testmode pin.

DVT : remove TP for enlarge NV_VDD plane

DVT : GPIO5 connect to VGA power

DVT : value change to NV_

NB8X: XTALIN use 3.3V level

OVERTEMP LATCHING CIRCUIT

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

0 = connect to GND
M= unconnected
1 = connect directly to VDD

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

nVidia support Down -1.25%

This chip can use MK1726 or P1819B

R616 place near GPU
R79 place near spectrum chip

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Title: VGA (MULTIUSE) 7 OF 8

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CLOSE TO GPU.75 Ohm to GND when CRT is disabled. (FAE suggest to NC 5/21)

PVT 5/21 : change to NC

R647 1 2 NC_NV_75_0402 NV_DACARED
R645 1 2 NC_NV_75_0402 NV_DACAGREEN
R646 1 2 NC_NV_75_0402 NV_DACABLUE

PVT 5/17 : change to NC

R626 1 2 NC_124_F 0402 NV_DACA_RSET

N.C. when CRT is disabled

U5H

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54 GND55 GND56 GND57 GND58 GND59 GND60 GND61 GND62 GND63 GND64 GND65 GND66 GND67 GND68 GND69 GND70 GND71 GND72 GND73 GND74 GND75 GND76 GND77 GND78 GND79 GND80

GND

GND81 GND82 GND83 GND84 GND85 GND86 GND87 GND88 GND89 GND90 GND91 GND92 GND93 GND94 GND95 GND96 GND97 GND98 GND99 GND100 GND101 GND102 GND103 GND104 GND105 GND106 GND107 GND108 GND109 GND110 GND111 GND112 GND113 GND114 GND115 GND116 GND117 GND118 GND119 GND120 GND121 GND122 GND123 GND124 GND125 GND126 GND127 GND128 GND129 GND130 GND131 GND132 GND133 GND134 GND135 GND136 GND137 GND138 GND139 GND140 GND141 GND142 GND143 GND144 GND145 GND146 GND147 GND148 GND149 GND150 GND151 GND152 GND153 GND154 GND155

D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M21 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 AL10 AG13 AM10

GND_SENSE_GFX 42

NV_NB8M-GT-B-A2

U5G

DACA_RSET AH9
DACB_RSET R7 NV_DACB_RSET 1 TP15 26MIL

N.C. when DACB is unused

CRT

67 NV_DACARED NV_DACARED AH11 DACA_RED
67 NV_DACAGREEN NV_DACAGREEN AJ12 DACA_GREEN
67 NV_DACABLUE NV_DACABLUE AH12 DACA_BLUE

70mA

AG9 DACA_IDUMP
67 NV_DACAHSYNC NV_DACAHSYNC AE10 DACA_HSYNC
67 NV_DACAVSYNC NV_DACAVSYNC AK10 DACA_VSYNC
26MIL TP144 1 TP_NV_DACC_RSET AF5 DACC_RSET

N.C. when DACC is unused

TV

DACB_RED R6 NV_DACBRED
DACB_GREEN T5 NV_DACBGREEN
DACB_BLUE T6 NV_DACBBLUE

100mA

DACB_IDUMP V7
DACB_CSYNC U5 NV_DACB_CSYNC 1 TP104 26MIL

VIDEO DAC

NV_DACCRED AF6 DACC_RED
NV_DACCGREEN AG6 DACC_GREEN
NV_DACCBLUE AE5 DACC_BLUE

70mA

AG4 DACC_IDUMP
26MIL TP149 1 NV_DACCHSYNC AG7 DACC_HSYNC
26MIL TP147 1 NV_DACCVSYNC AG5 DACC_VSYNC

DVI

LVDS

17 NV_ODD_CLKIN- NV_ODD_CLKIN- AJ9 IFPA_TXC#
17 NV_ODD_CLKIN+ NV_ODD_CLKIN+ AK9 IFPA_TXC
17 NV_ODD_RXIN0- NV_ODD_RXIN0- AJ6 IFPA_TXD0#
17 NV_ODD_RXIN0+ NV_ODD_RXIN0+ AH6 IFPA_TXD0
17 NV_ODD_RXIN1- NV_ODD_RXIN1- AH7 IFPA_TXD1#
17 NV_ODD_RXIN1+ NV_ODD_RXIN1+ AH8 IFPA_TXD1
17 NV_ODD_RXIN2- NV_ODD_RXIN2- AK8 IFPA_TXD#
17 NV_ODD_RXIN2+ NV_ODD_RXIN2+ AJ8 IFPA_TXD2
17 NV_ODD_RXIN3- NV_ODD_RXIN3- AH5 IFPA_TXD3#
17 NV_ODD_RXIN3+ NV_ODD_RXIN3+ AJ5 IFPA_TXD3
17 NV_EVEN_CLKIN- NV_EVEN_CLKIN- AL4 IFPB_TXC#
17 NV_EVEN_CLKIN+ NV_EVEN_CLKIN+ AK4 IFPB_TXC
17 NV_EVEN_RXIN0- NV_EVEN_RXIN0- AM5 IFPB_TXD4#
17 NV_EVEN_RXIN0+ NV_EVEN_RXIN0+ AM6 IFPB_TXD4
17 NV_EVEN_RXIN1- NV_EVEN_RXIN1- AL7 IFPB_TXD5#
17 NV_EVEN_RXIN1+ NV_EVEN_RXIN1+ AM7 IFPB_TXD5
17 NV_EVEN_RXIN2- NV_EVEN_RXIN2- AK5 IFPB_TXD6#
17 NV_EVEN_RXIN2+ NV_EVEN_RXIN2+ AK6 IFPB_TXD6
17 NV_EVEN_RXIN3- NV_EVEN_RXIN3- AL8 IFPB_TXD7#
17 NV_EVEN_RXIN3+ NV_EVEN_RXIN3+ AK7 IFPB_TXD7
26MIL TP31 1 IFPAB_RSET AL5 IFPAB_RSET

TMDS

IFPC_TXC# AM3
IFPC_TXC AM2
IFPC_TXD0# AE1
IFPC_TXD0 AE2
IFPC_TXD1# AF2
IFPC_TXD1 AF1
IFPC_TXD2# AH1
IFPC_TXD2 AG1
IFPD_TXC# AH2
IFPD_TXC AG3
IFPD_TXD4# AJ1
IFPD_TXD4 AK1
IFPD_TXD5# AL1
IFPD_TXD5 AL2
IFPD_TXD6# AJ3
IFPD_TXD6 AJ2
IFPCD_RSET AH3

NV_NB8M-GT-B-A2

DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

CLOSE TO GPU

PVT 5/22 : change to NC

NV_DACBRED R609 1 2 NC_NV_75_0402
NV_DACBGREEN R610 1 2 NC_NV_75_0402
NV_DACBBLUE R611 1 2 NC_NV_75_0402

DACB UNUSED. TERMINATED TO GND WITH 75 OHM RESISTOR. (FAE suggest to NC 5/21)

CLOSE TO GPU

PVT 5/22 : change to NC

NV_DACCRED R634 1 2 NC_NV_75_0402
NV_DACCGREEN R635 1 2 NC_NV_75_0402
NV_DACCBLUE R624 1 2 NC_NV_75_0402

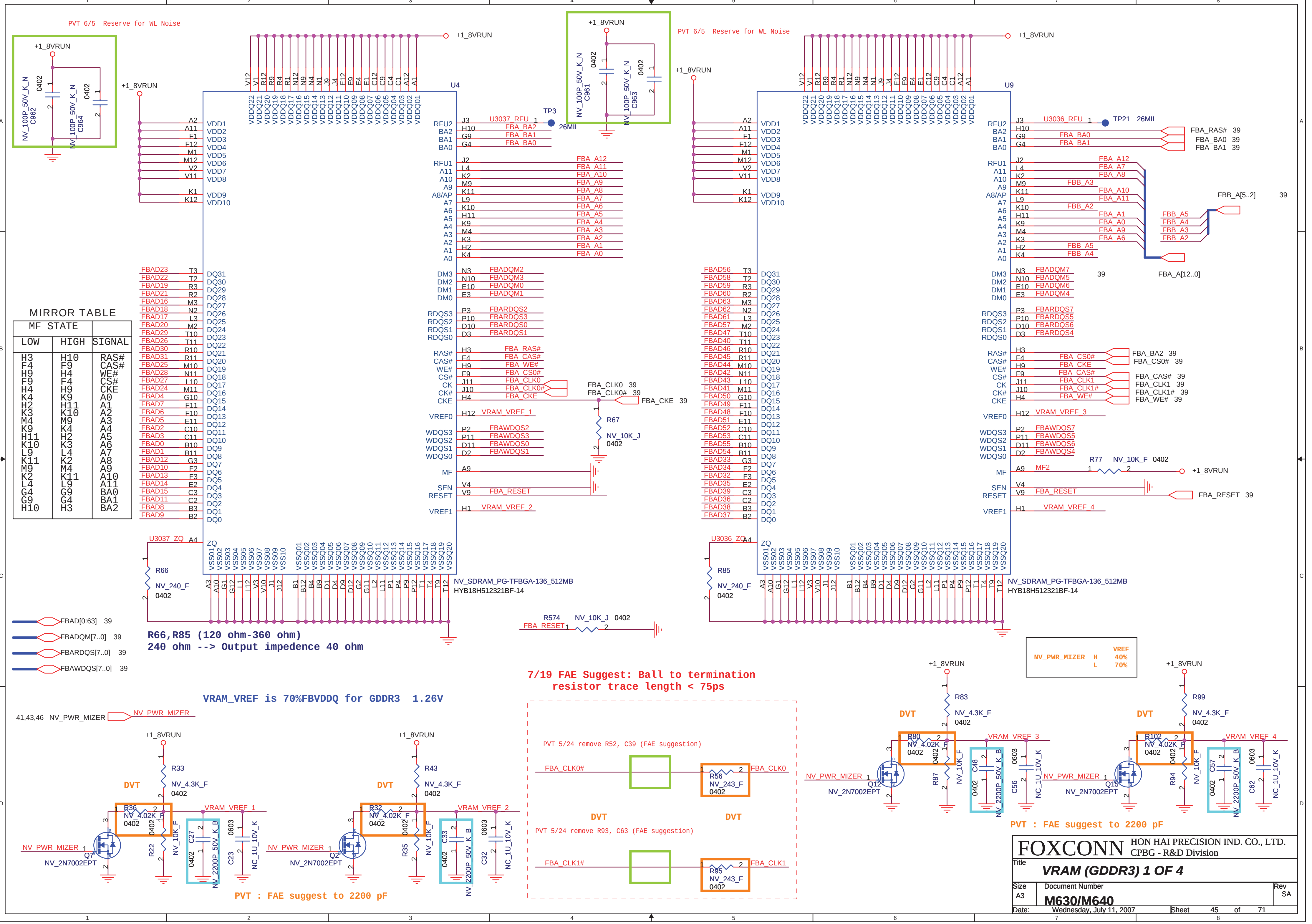
DACC UNUSED. TERMINATED TO GND WITH 75 OHM RESISTOR. (FAE suggest to NC 5/21)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (LVDS/DAC) 8 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Friday, July 27, 2007 | Sheet 44 of 71



MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

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CPBG - R&D Division

Title: **VRAM (GDDR3) 1 OF 4**

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 45 of 71

PVT 6/5 Reserve for WL Noise

PVT 6/5 Reserve for WL Noise

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

R6,R15(120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

PVT 5/24 remove R17, C24 (FAE suggestion)

PVT 5/24 remove R561, C487 (FAE suggestion)

PVT : FAE suggest to 2200 pF

PVT : FAE suggest to 2200 pF

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VRAM (GDDR3) 2 OF 4
Size A3	Document Number M630/M640
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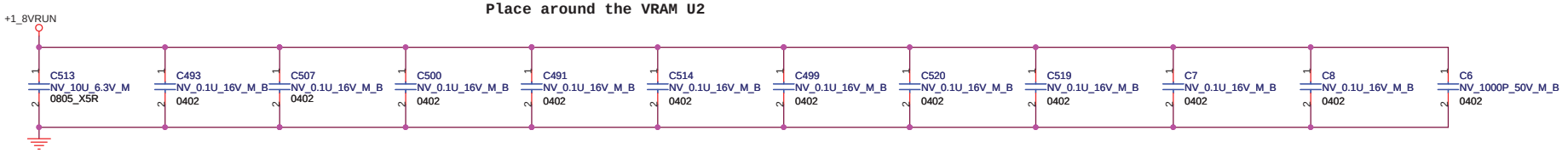
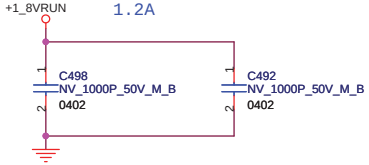
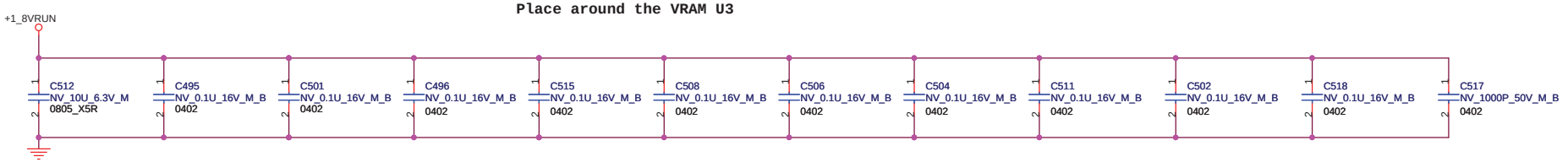
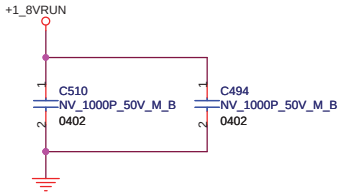
Place around the VRAM U2





Place around the VRAM U3





FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM (GDDR3) 2 OF 4

Size: A3 | Document Number: M630/M640 | Rev: SA

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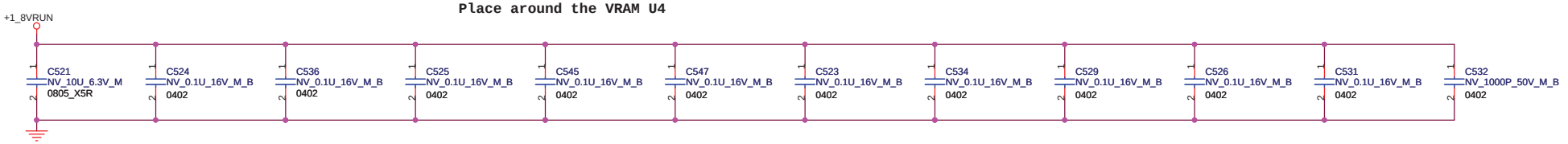
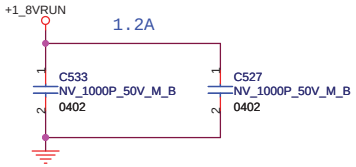
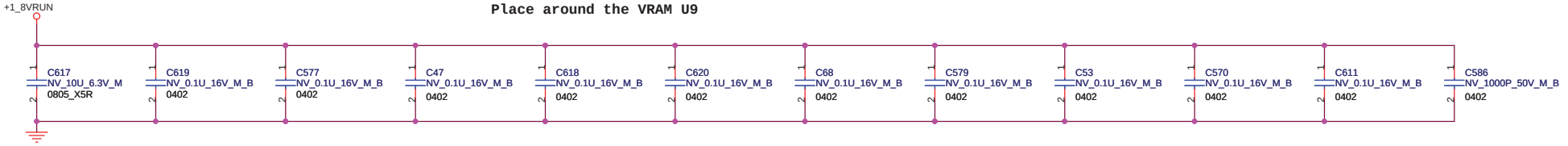
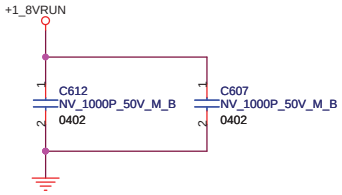
Place around the VRAM U4





Place around the VRAM U9





FOXCONN HON HAI PRECISION IND. CO., LTD.
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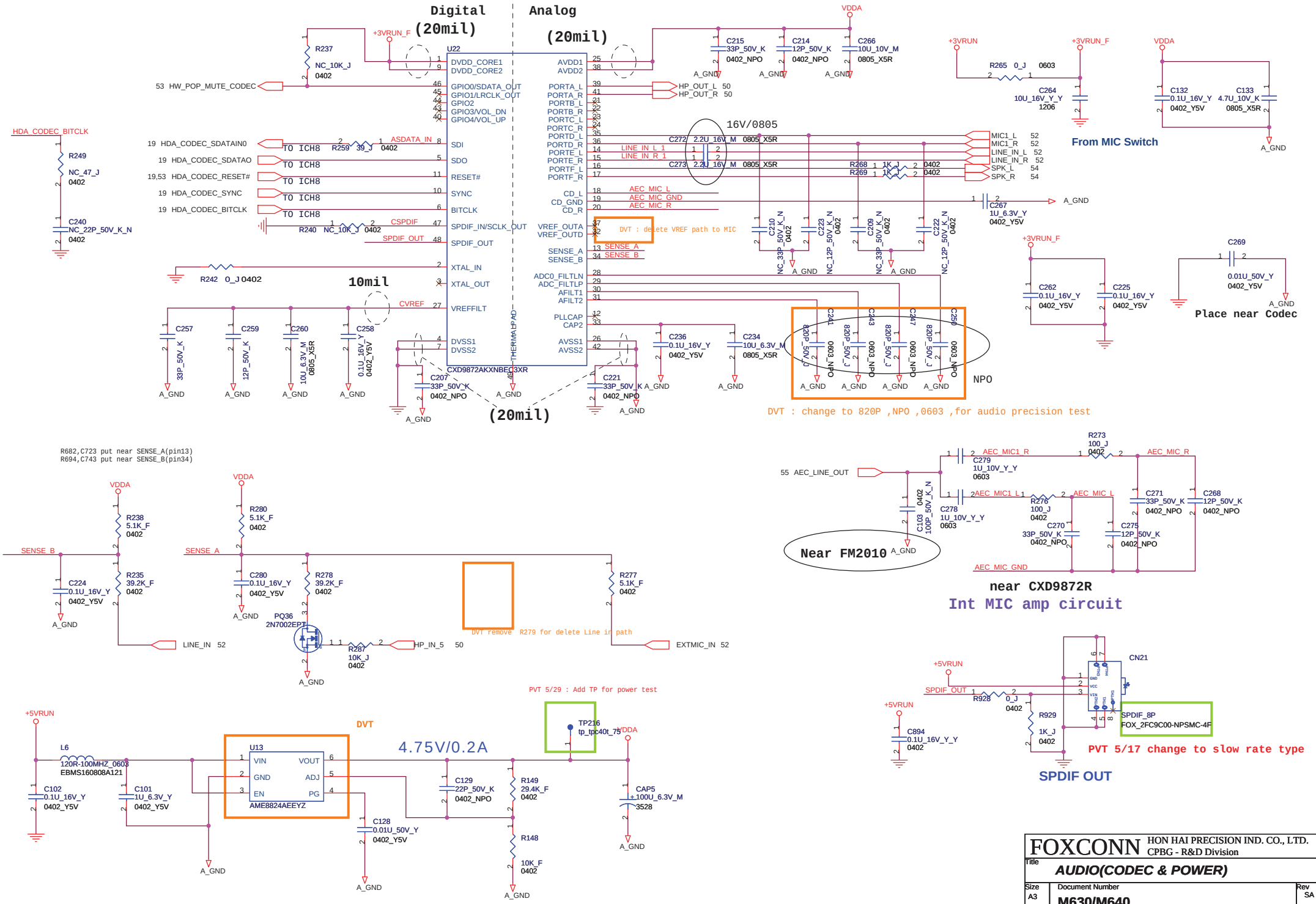
Title: *VRAM (POWERBYPASS) 4 OF 4*

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 48 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **AUDIO(CODEC & POWER)**

Size	Document Number	Rev
A3	M630/M640	SA

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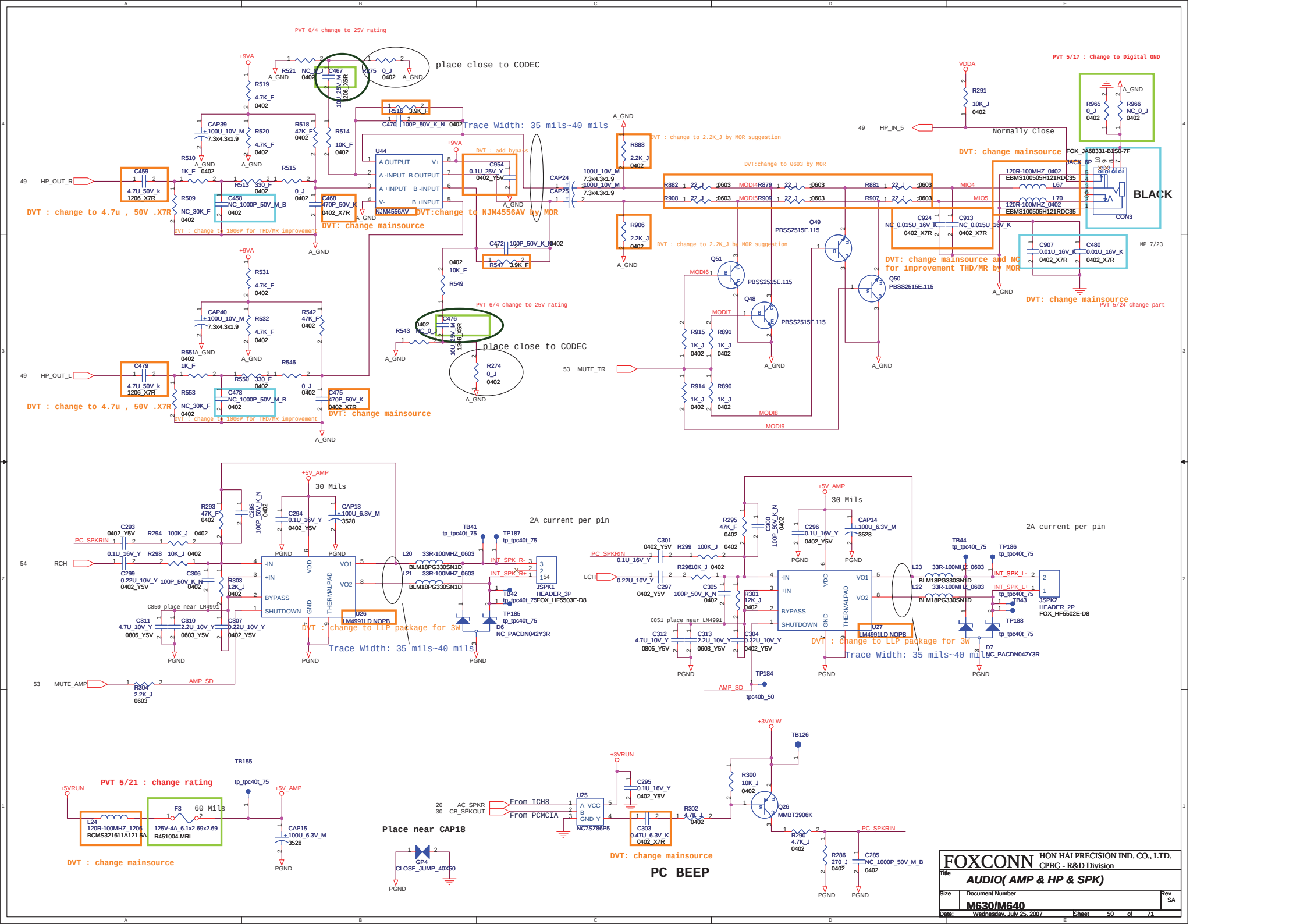
PVT 6/4 change to 25V rating
place close to CODEC
Trace Width: 35 mils~40 mils
DVT : change to 2.2K_J by MOR suggestion
DVT:change to 0603 by MOR
DVT : add bypass
DVT:change to NJM4556AV by MOR
DVT : change to 4.7u , 50V .X7R
DVT : change to 1000P for THD/MR improvement
DVT: change mainsource
PVT 6/4 change to 25V rating
place close to CODEC
DVT : change to 2.2K_J by MOR suggestion
PVT 5/17 : Change to Digital GND
Normally Close
DVT: change mainsource
FOX_JA68331-B1S0-7F
JACK_6P
BLACK
CON3
DVT: change mainsource and NC
for improvement THD/MR by MOR
MP 7/23
DVT: change mainsource
PVT 5/24 change part
DVT : change to 4.7u , 50V .X7R
DVT : change to 1000P for THD/MR improvement
DVT: change mainsource
+5V_AMP
30 Mils
2A current per pin
DVT : change to LLP package for 3W
Trace Width: 35 mils~40 mils
2A current per pin
DVT : change to LLP package for 3W
Trace Width: 35 mils~40 mils
PVT 5/21 : change rating
DVT : change mainsource
Place near CAP18
DVT: change mainsource
PC BEEP
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
AUDIO(AMP & HP & SPK)
M630/M640
Wednesday, July 25, 2007
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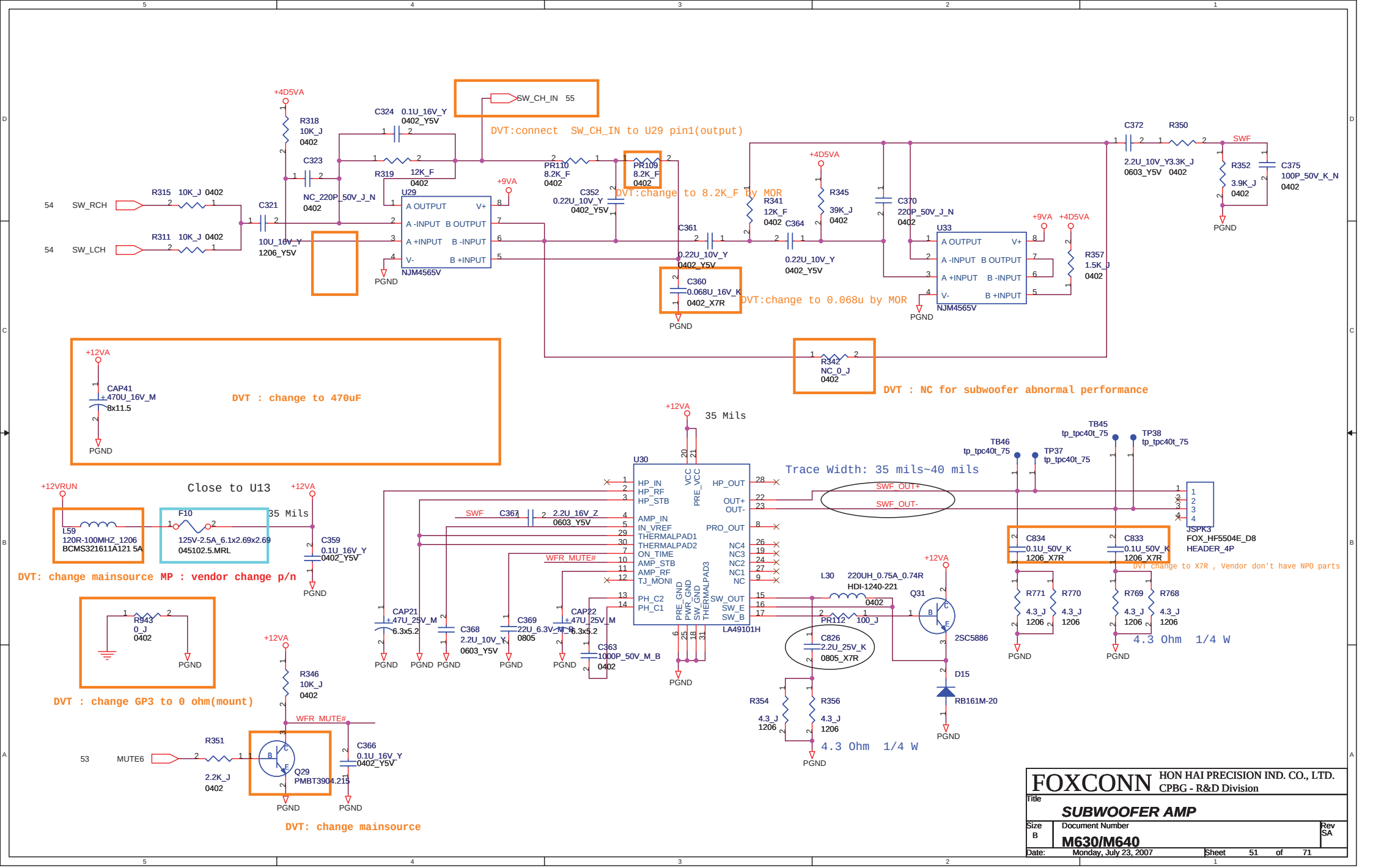
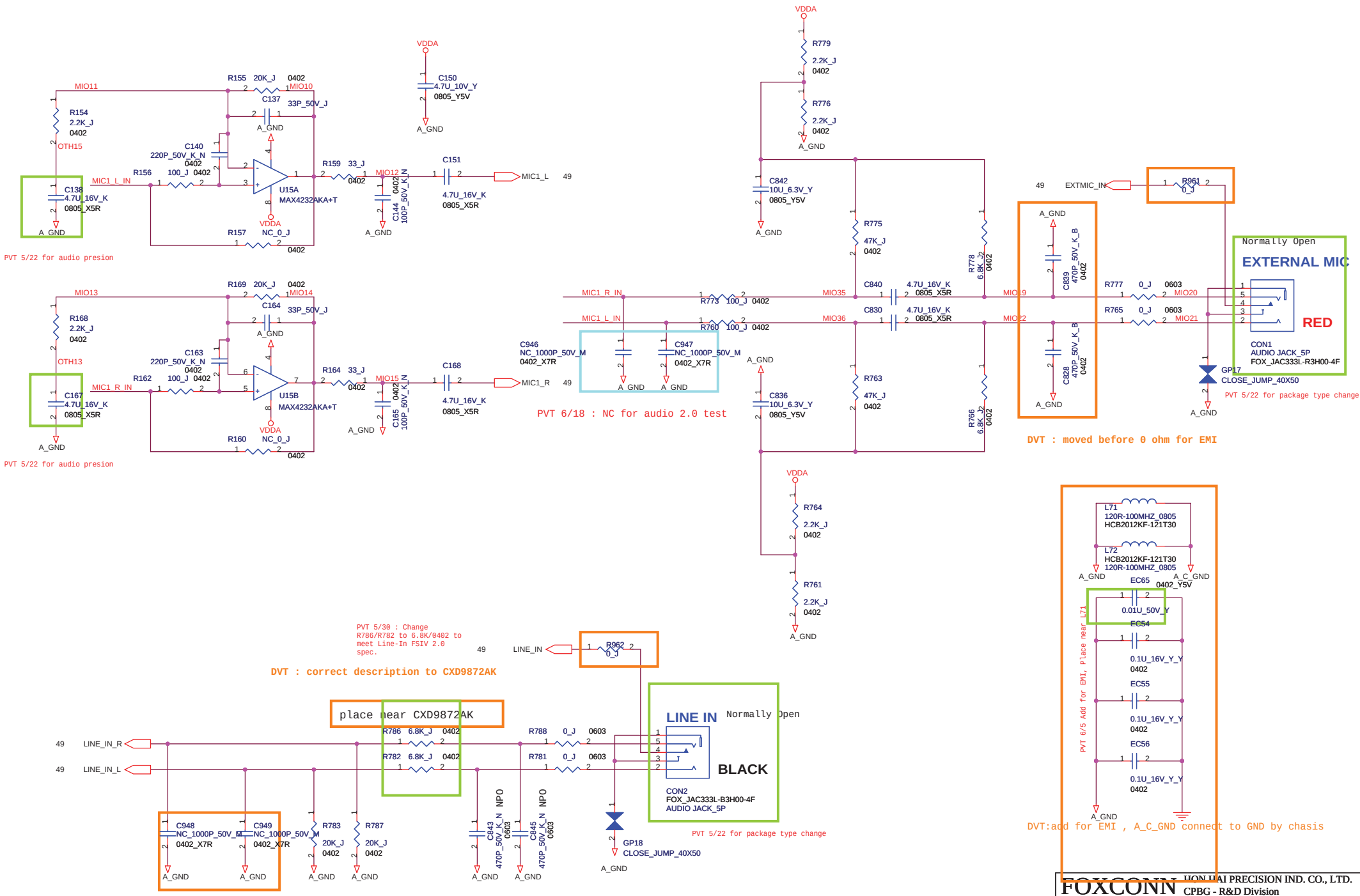


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	**SUBWOOFER AMP**
Size B	Document Number **M630/M640** Rev SA
Date: Monday, July 23, 2007	Sheet 51 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: AUDIO(EXT MIC & LINE IN & SPDIF)

Size	Document Number	Rev
A3	M630/M640	SA

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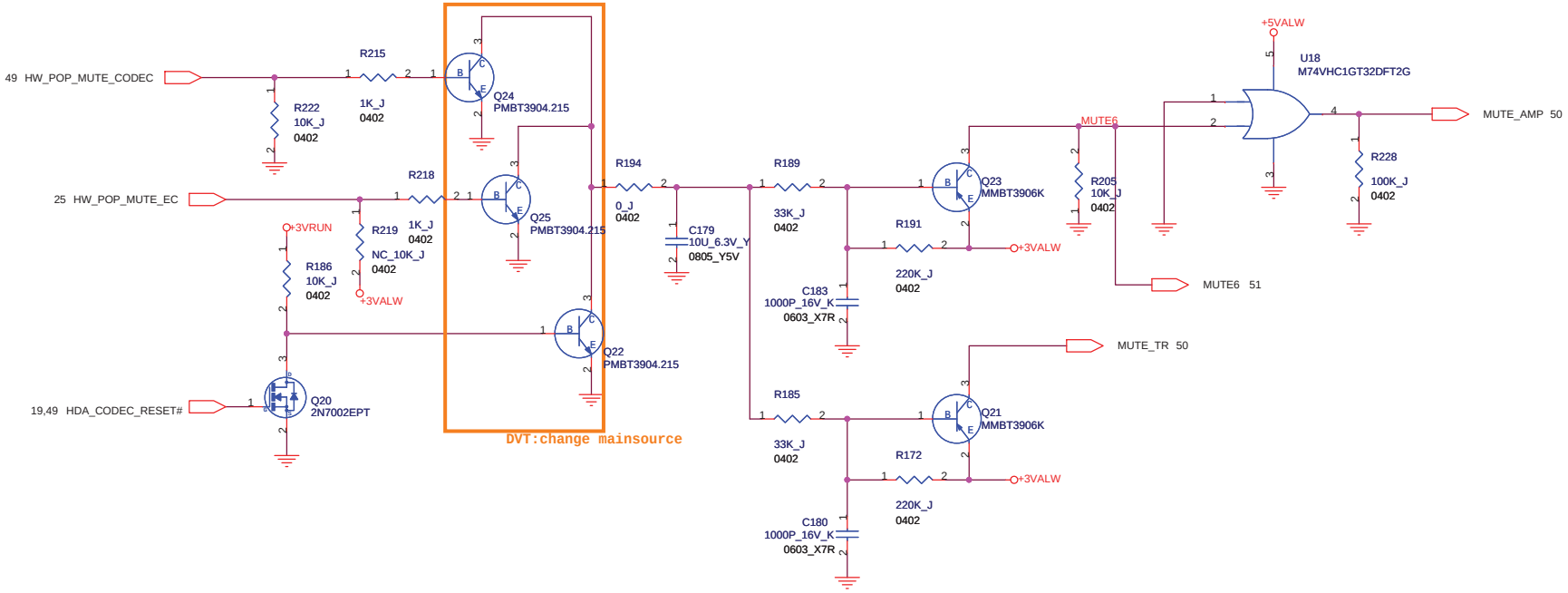

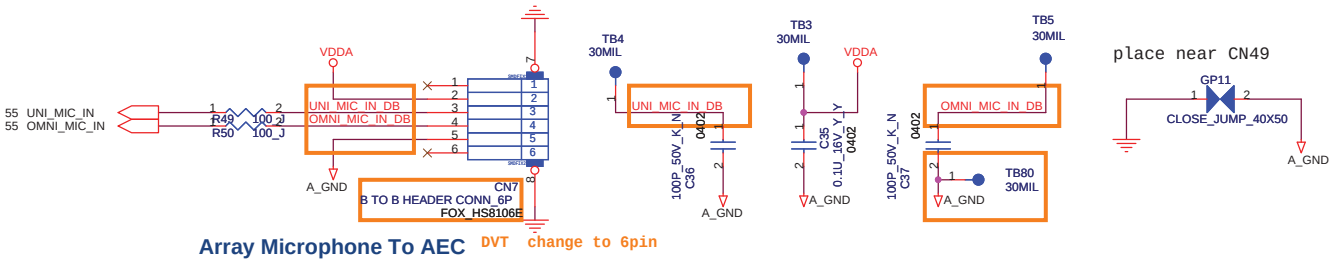

Array Microphone To AEC DVT change to 6pin

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*AUDIO (MUTE & INT MIC)*	
Size A3	Document Number **M630/M640**	Rev SA
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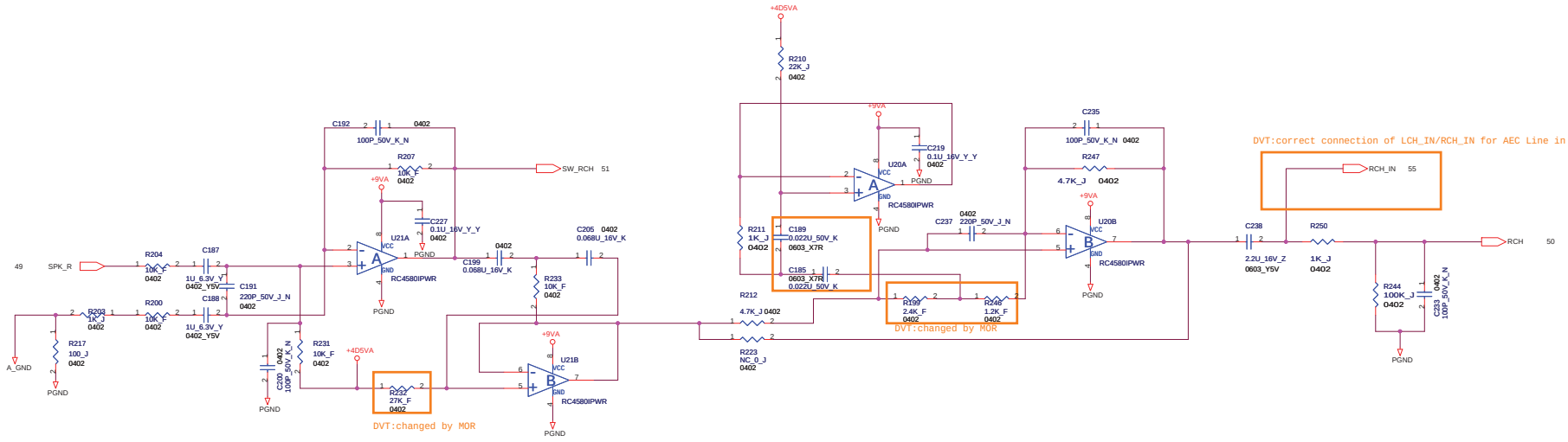
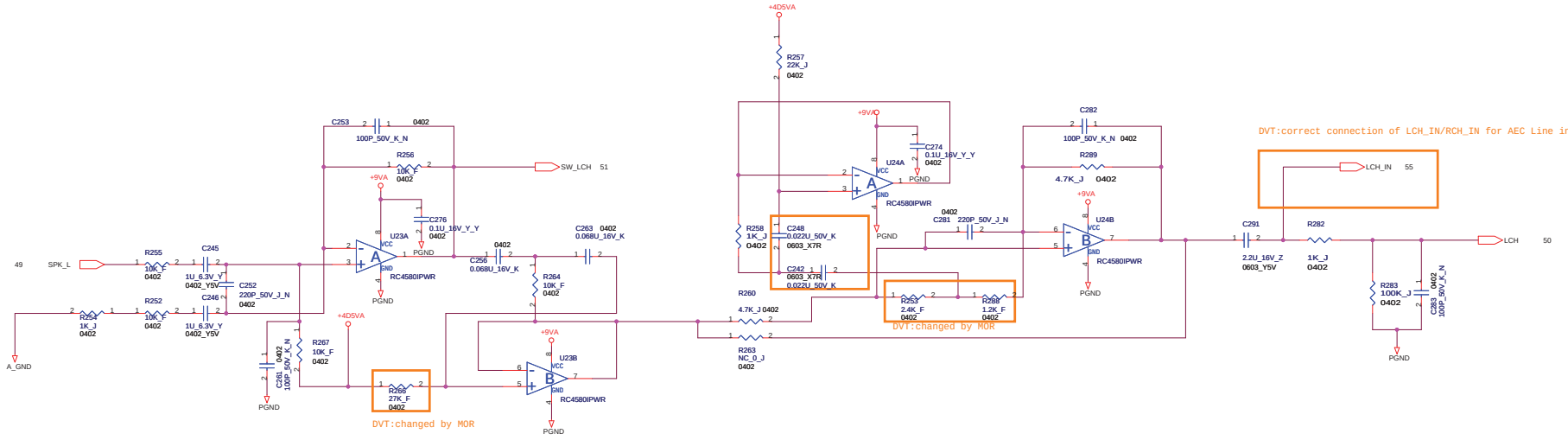
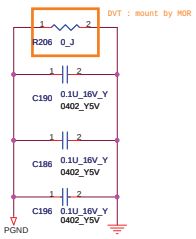


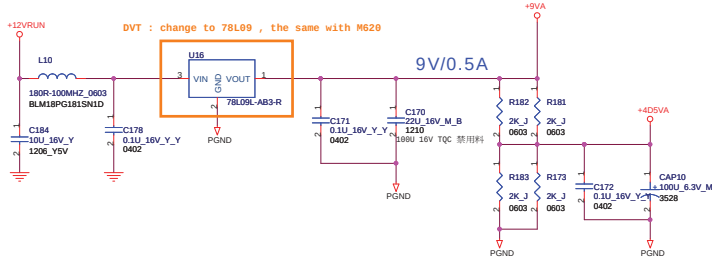


Reserved for EMI

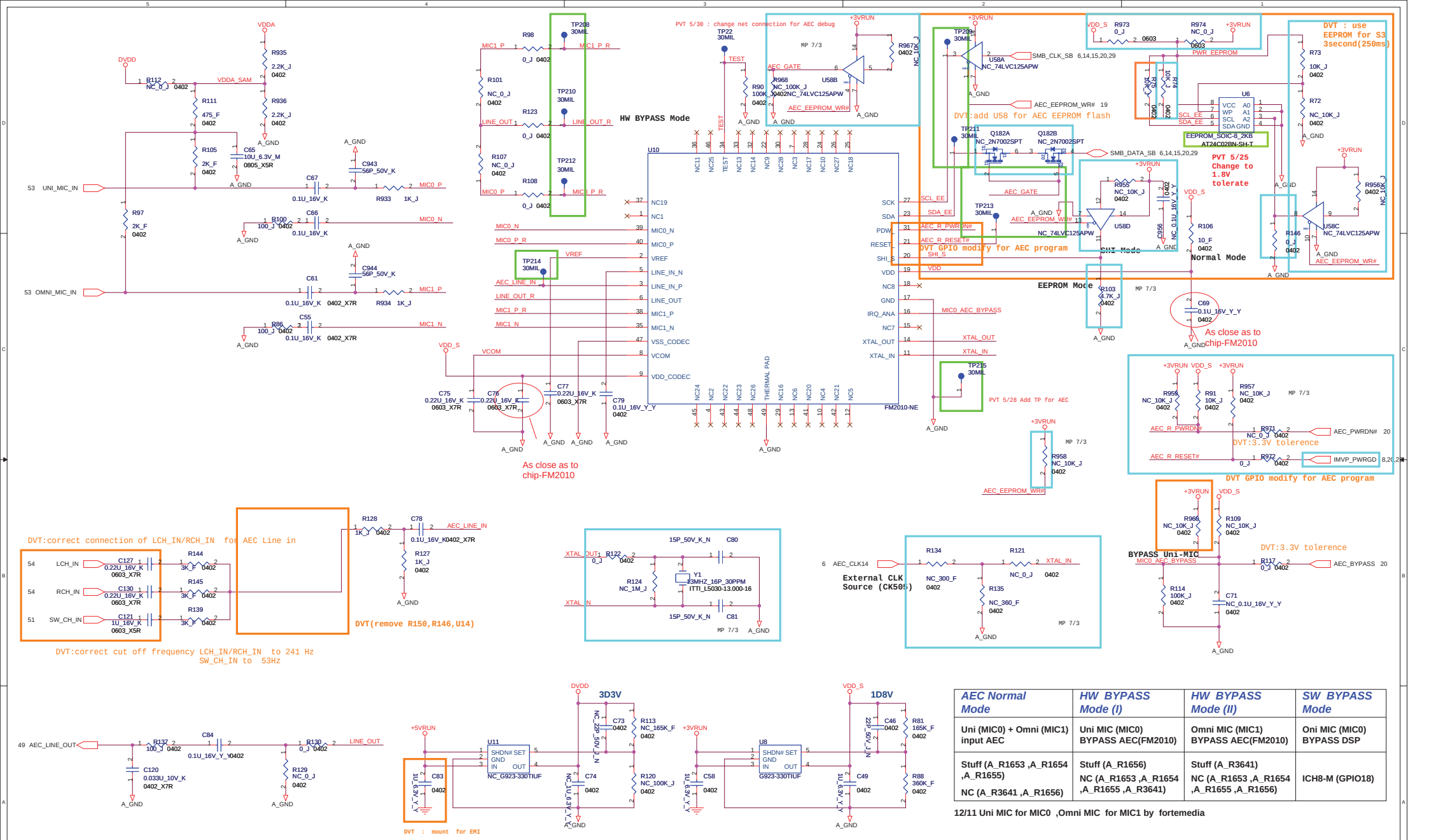


For MIC-IN quality improvement

Do not place near each other & far apart within PGND area.



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO(EQ)		
Size A2	Document Number M630/M640		Rev SA
Date: Wednesday, July 11, 2007	Sheet 54 of 71		



AEC Normal Mode	HW BYPASS Mode (I)	HW BYPASS Mode (II)	SW BYPASS Mode
Uni (MIC0) + Omni (MIC1) input AEC	Uni MIC (MIC0) BYPASS AEC(FM2010)	Omni MIC (MIC1) BYPASS AEC(FM2010)	Oni MIC (MIC0) BYPASS DSP
Stuff (A_R1653 ,A_R1654 ,A_R1655) NC (A_R3641 ,A_R1656)	Stuff (A_R1656) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R3641)	Stuff (A_R3641) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R1656)	ICH8-M (GPIO18)

12/11 Uni MIC for MIC0 ,Omni MIC for MIC1 by fortemedia

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	AUDIO (AEC)
Size / Document Number	Custom M630/M640
Rev	SA
Date:	Wednesday, July 25, 2007
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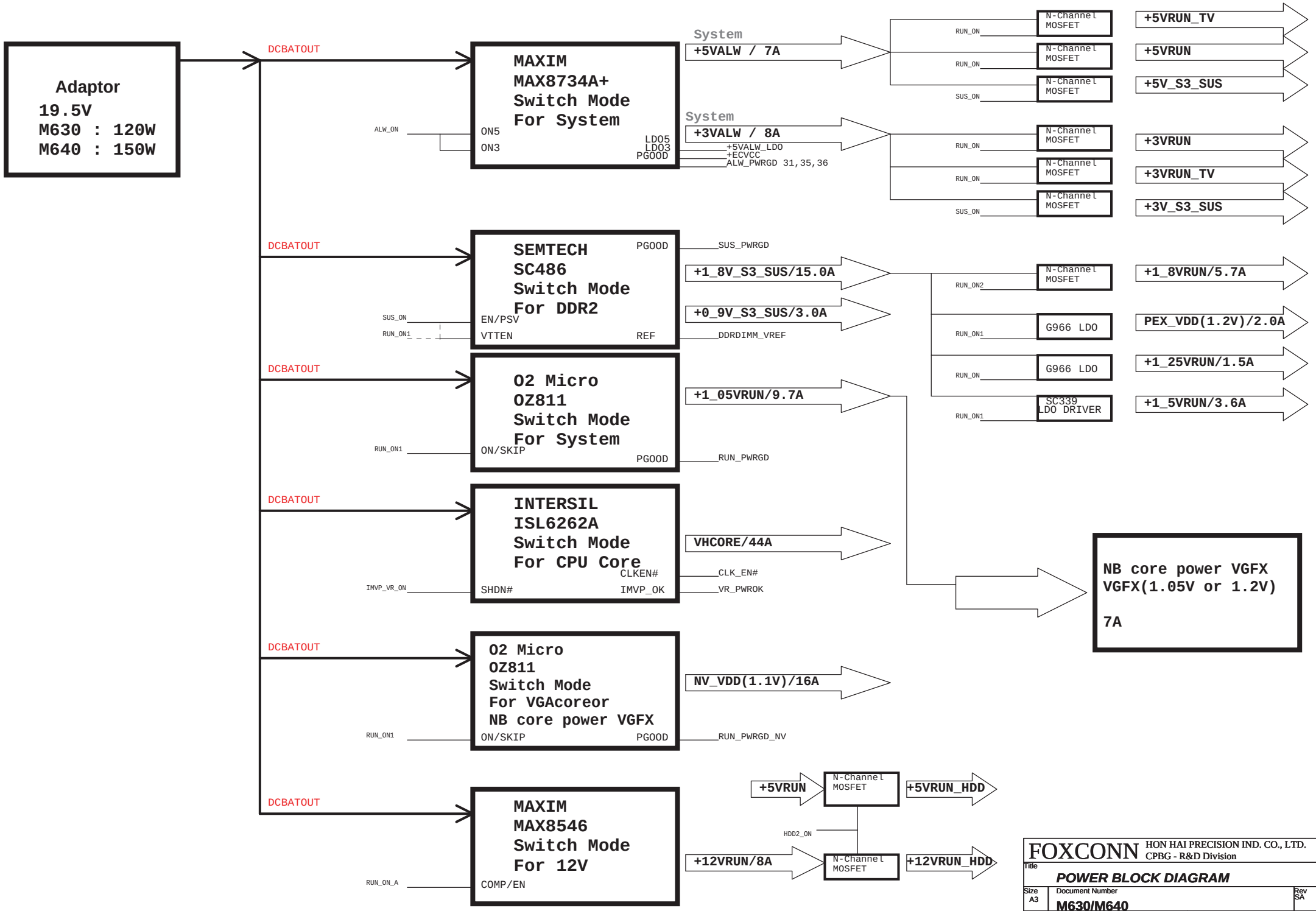
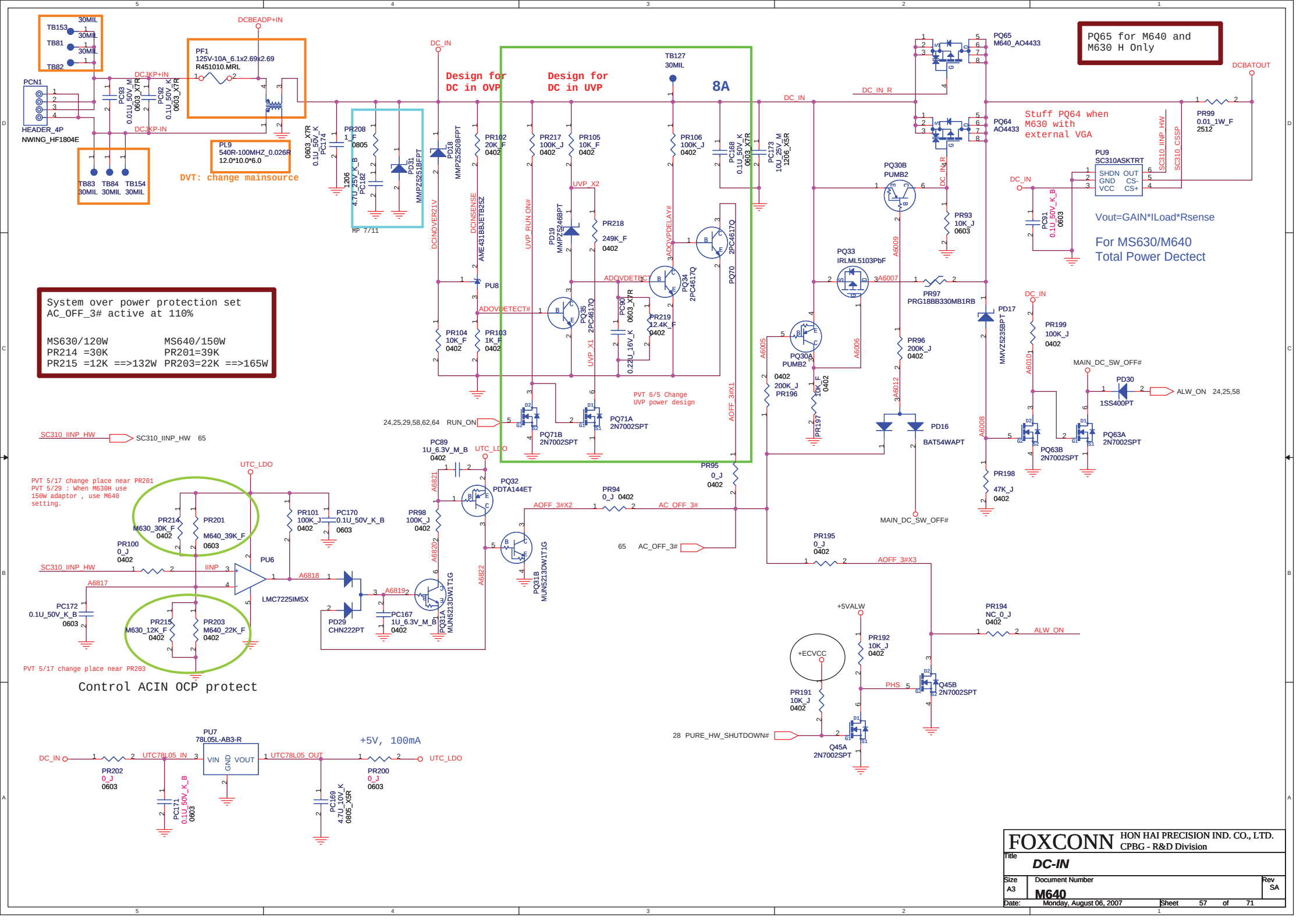


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: POWER BLOCK DIAGRAM

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 56 of 71


PQ65 for M640 and M630 H Only
Design for DC in OVP
Design for DC in UVP
8A
DC_IN
DCBEADP+IN
DCBATOUT
PF1 125V-10A_6.1x2.69x2.69 R451010.MRL
PL9 540R-100MHZ_0.026R 12.0*10.0*6.0
DVT: change mainsource
Stuff PQ64 when M630 with external VGA
Vout=GAIN*ILoad*Rsense
For MS630/M640 Total Power Dectect
System over power protection set
AC_OFF_3# active at 110%
MS630/120W MS640/150W
PR214 =30K PR201=39K
PR215 =12K ==>132W PR203=22K ==>165W
PVT 6/5 Change UVP power design
PVT 5/17 change place near PR201
PVT 5/29 : When M630H use 150W adaptor , use M640 setting.
PVT 5/17 change place near PR203
Control ACIN OCP protect
+5V, 100mA
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
DC-IN
M640
Monday, August 06, 2007
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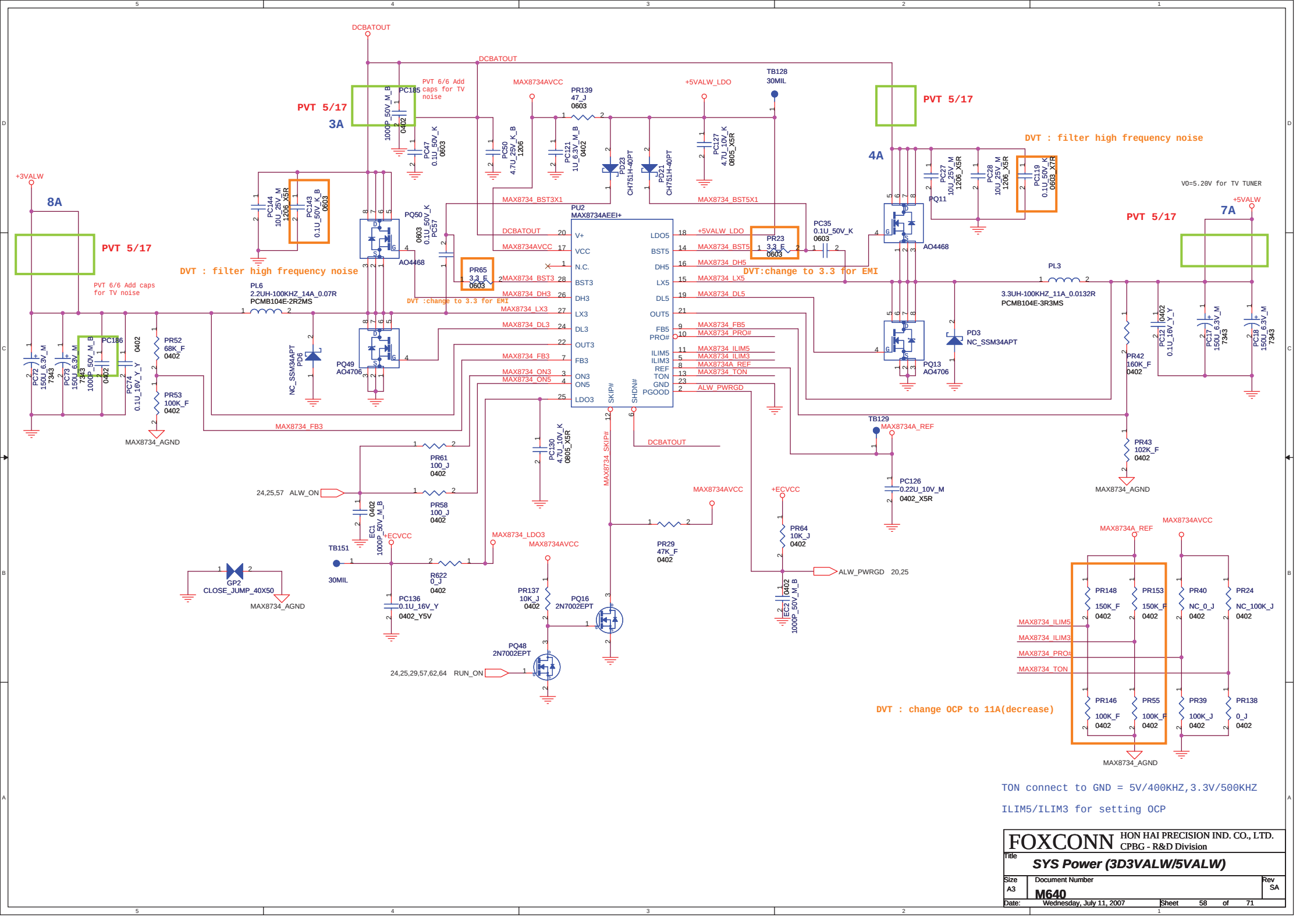
DCBATOUT
PVT 5/17
3A
PVT 6/6 Add caps for TV noise
MAX8734AVCC
+5VALW_LDO
TB128
30MIL
PR139
47_J
0603
PC185
1000P_50V_M_B
0402
PC47
0.1U_50V_K
0603
PC50
4.7U_25V_K_B
1206
PC121
1U_6.3V_M_B
0402
PD23
CH751H-40PT
PD21
CH751H-40PT
PC127
4.7U_10V_K
0805_X5R
PVT 5/17
4A
DVT : filter high frequency noise
PC27
10U_25V_M
1206_X5R
PC28
10U_25V_M
1206_X5R
PC119
0.1U_50V_K
0603_X7R
PQ11
AO4468
VO=5.20V for TV TUNER
+5VALW
PVT 5/17
7A
+3VALW
8A
PVT 5/17
PC144
10U_25V_M
1206_X5R
PC143
0.1U_50V_K_B
0603
PQ50
0603
0.1U_50V_K
PC57
AO4468
DVT : filter high frequency noise
PR65
3.3_F
0603
DVT :change to 3.3 for EMI
PU2
MAX8734AEEI+
MAX8734_BST3X1
MAX8734_BST5X1
DCBATOUT
MAX8734AVCC
V+
VCC
N.C.
BST3
DH3
LX3
DL3
OUT3
FB3
ON3
ON5
LDO3
SKIP#
SHDN#
LDO5
BST5
DH5
LX5
DL5
OUT5
FB5
PRO#
ILIM5
ILIM3
REF
TON
GND
PGOOD
+5VALW_LDO
MAX8734_BST5
MAX8734_DH5
MAX8734_LX5
MAX8734_DL5
MAX8734_FB5
MAX8734_PRO#
MAX8734_ILIM5
MAX8734_ILIM3
MAX8734A_REF
MAX8734_TON
ALW_PWRGD
PR23
3.3_F
0603
PC35
0.1U_50V_K
0603
DVT:change to 3.3 for EMI
PL3
3.3UH-100KHZ_11A_0.0132R
PCMB104E-3R3MS
PD3
NC_SSM34APT
PQ13
AO4706
PR42
160K_F
0402
PC12
0.1U_16V_Y
0402
PC17
150U_6.3V_M
7343
PC18
150U_6.3V_M
7343
PL6
2.2UH-100KHZ_14A_0.07R
PCMB104E-2R2MS
PVT 6/6 Add caps for TV noise
PC72
150U_6.3V_M
7343
PC73
150U_6.3V_M
7343
PC186
1000P_50V_M_B
0402
PC74
0.1U_16V_Y_Y
0402
PR52
68K_F
0402
PR53
100K_F
0402
MAX8734_AGND
NC_SSM34APT
PD6
PQ49
AO4706
MAX8734_FB3
MAX8734_LX3
MAX8734_DL3
MAX8734_FB3
MAX8734_ON3
MAX8734_ON5
DVT :change to 3.3 for EMI
TB129
MAX8734A_REF
PR43
102K_F
0402
PC126
0.22U_10V_M
0402_X5R
PR61
100_J
0402
24,25,57 ALW_ON
PR58
100_J
0402
EC1
1000P_50V_M_B
0402
PC130
4.7U_10V_K
0805_X5R
MAX8734_SKIP#
DCBATOUT
MAX8734AVCC
+ECVCC
PR29
47K_F
0402
PR64
10K_J
0402
ALW_PWRGD 20,25
EC2
1000P_50V_M_B
0402
TB151
30MIL
GP2
CLOSE_JUMP_40X50
MAX8734_AGND
+ECVCC
MAX8734_LDO3
MAX8734AVCC
R622
0_J
0402
PC136
0.1U_16V_Y
0402_Y5V
PR137
10K_J
0402
PQ16
2N7002EPT
PQ48
2N7002EPT
24,25,29,57,62,64 RUN_ON
MAX8734A_REF
MAX8734AVCC
PR148
150K_F
0402
PR153
150K_F
0402
PR40
NC_0_J
0402
PR24
NC_100K_J
0402
MAX8734_ILIM5
MAX8734_ILIM3
MAX8734_PRO#
MAX8734_TON
PR146
100K_F
0402
PR55
100K_F
0402
PR39
100K_J
0402
PR138
0_J
0402
MAX8734_AGND
DVT : change OCP to 11A(decrease)
TON connect to GND = 5V/400KHZ,3.3V/500KHZ
ILIM5/ILIM3 for setting OCP
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
SYS Power (3D3VALW/5VALW)
Size
A3
Document Number
M640
Rev
SA
Date:
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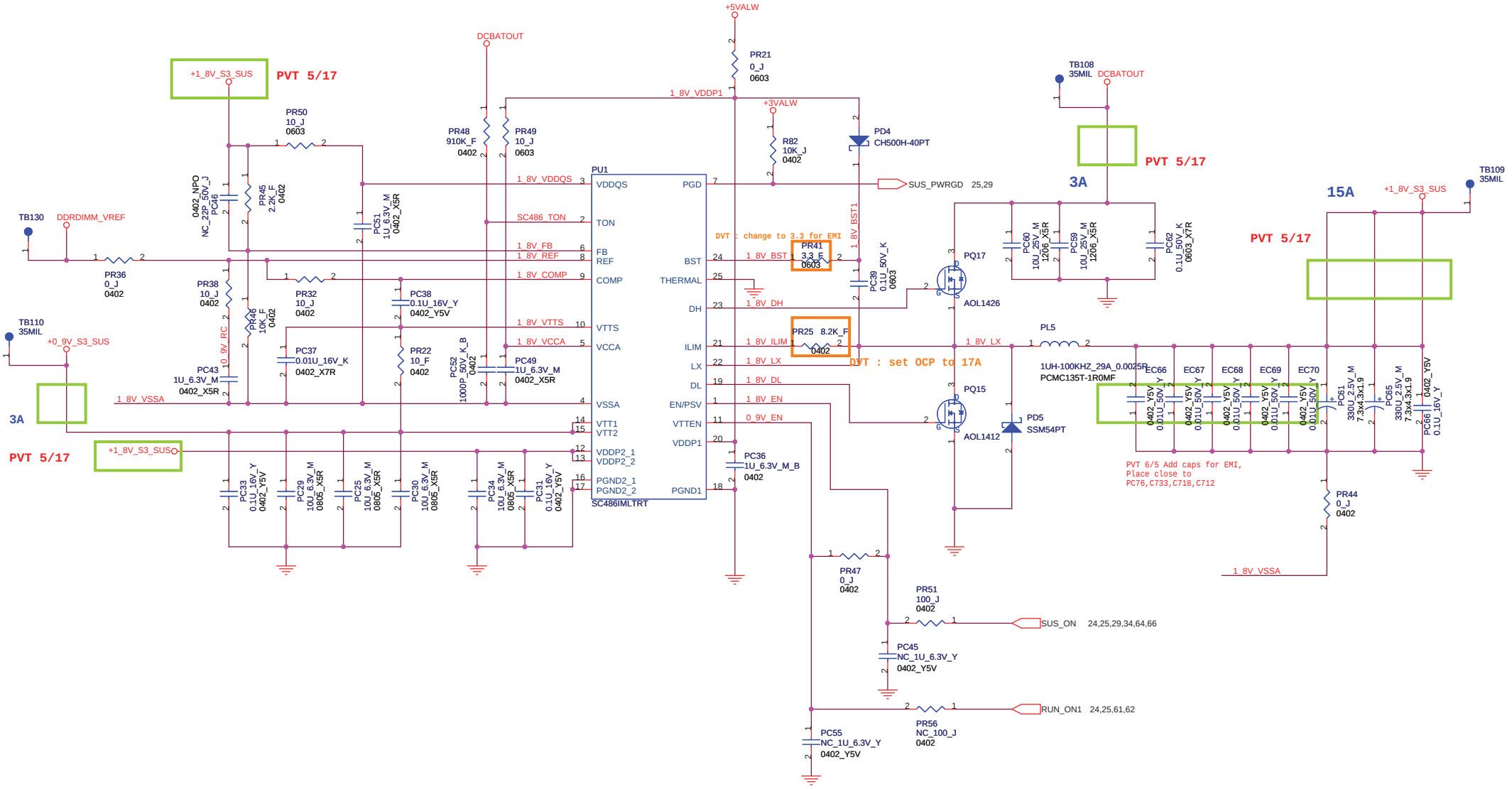
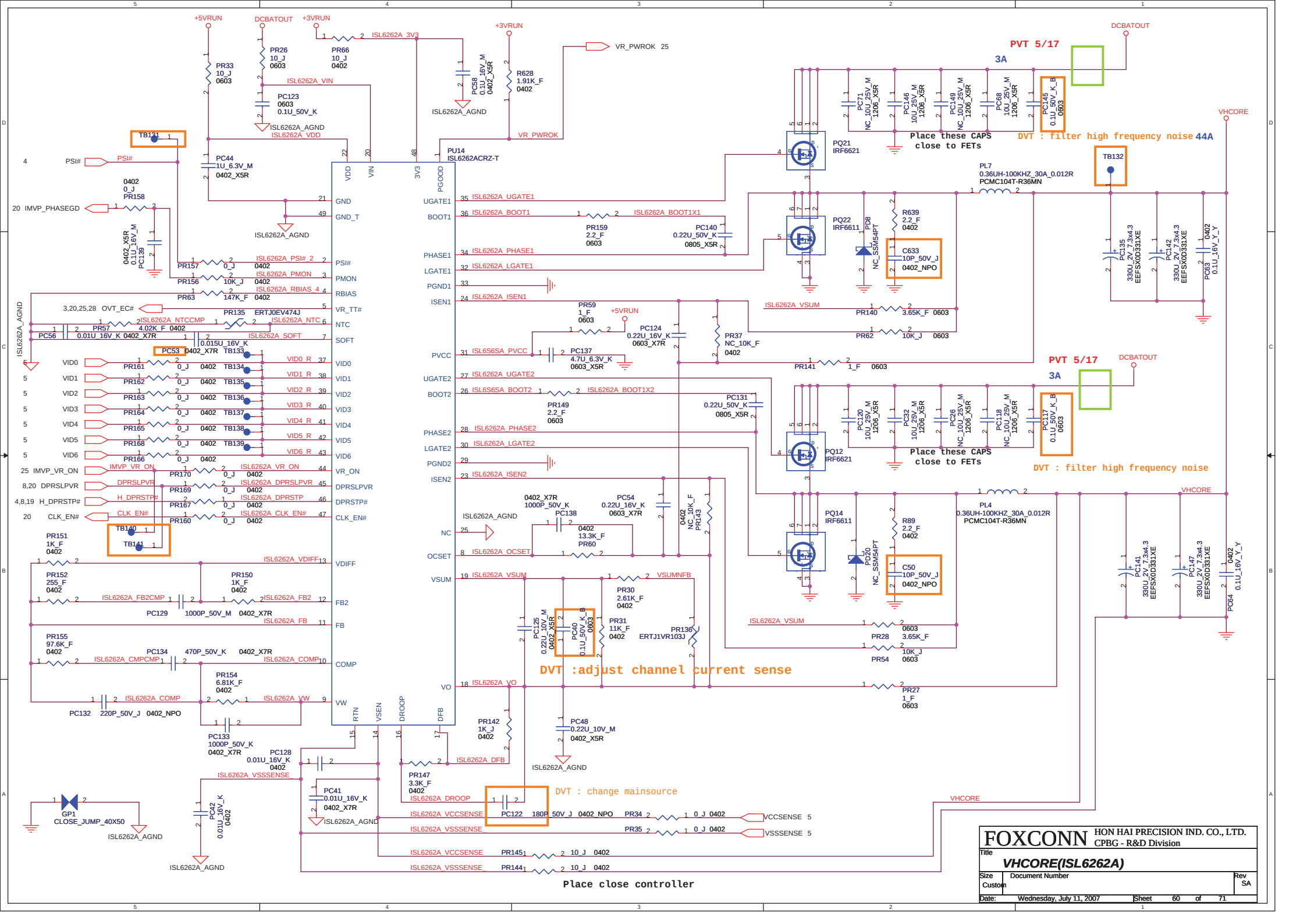
71



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 59 of 71	


PU14
ISL6262ACRZ-T
PVT 5/17
3A
PVT 5/17
3A
DVT : filter high frequency noise
DVT : filter high frequency noise
Place these CAPS close to FETs
Place these CAPS close to FETs
DVT :adjust channel current sense
DVT : change mainsource
Place close controller
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
VHCORE(ISL6262A)
Wednesday, July 11, 2007
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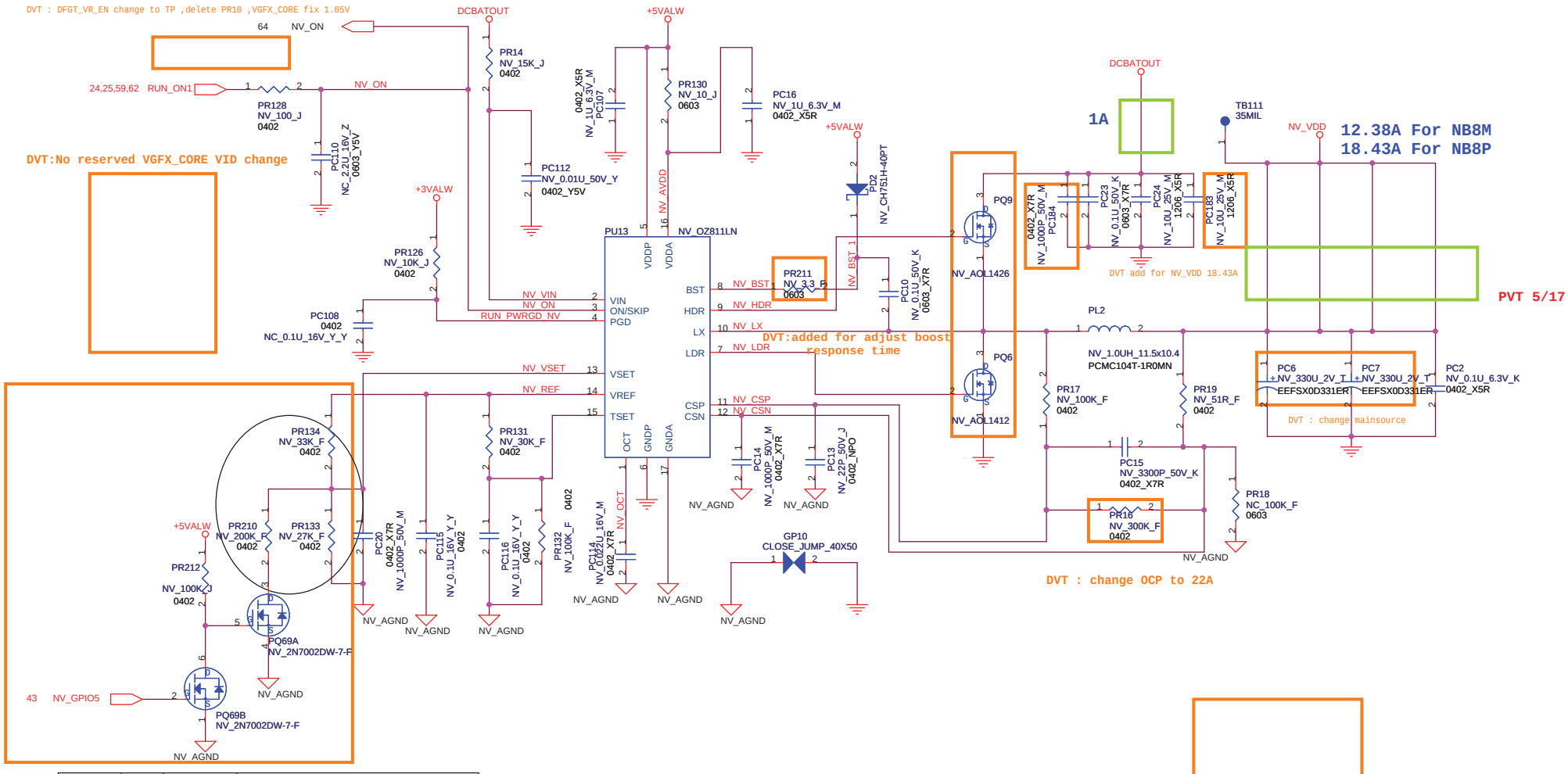
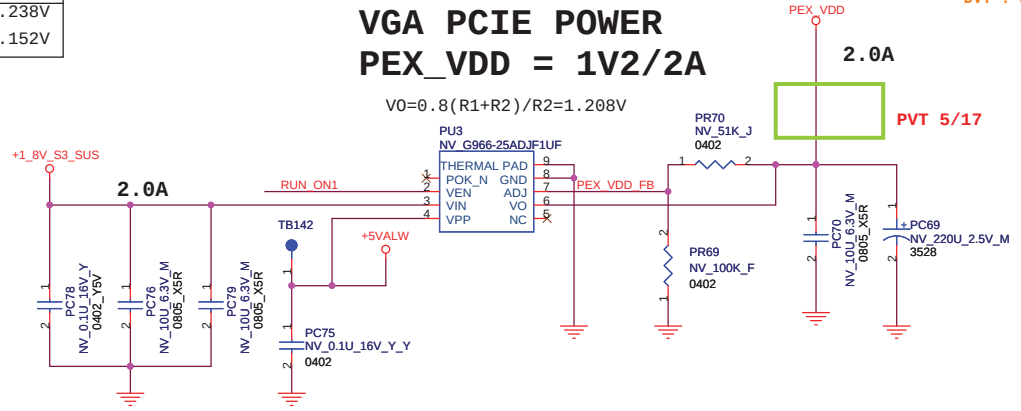


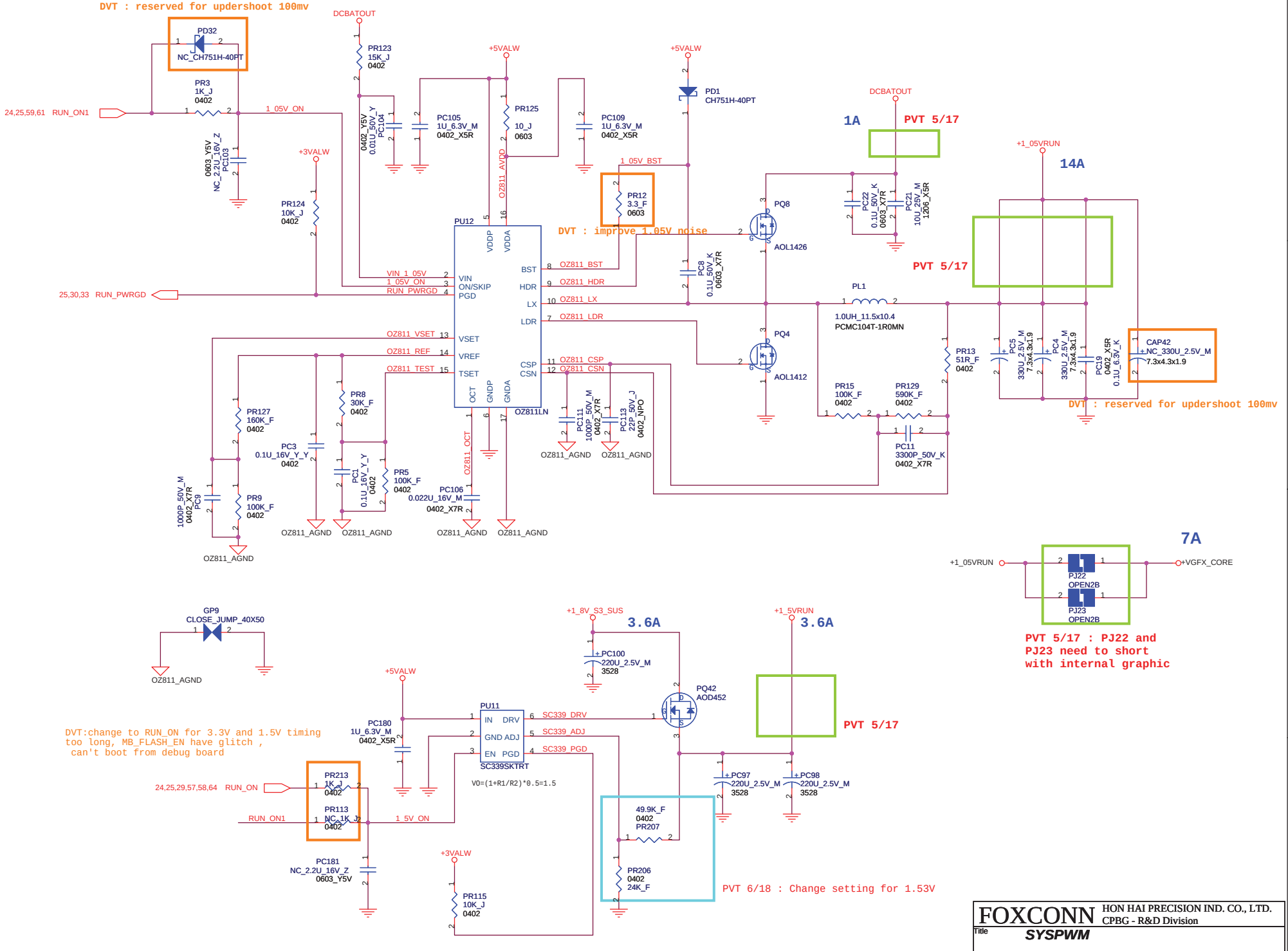
	I/O	Inter pull low	GPIO TABLE
GPIO5	O	Yes	GPU Voltage H: NVDD=1.238V GPU Voltage L: NVDD=1.152V

VGA PCIE POWER
PEX_VDD = 1V2/2A

VO=0.8(R1+R2)/R2=1.208V



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA POWER(GMCH)	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 61 of 71	


DVT : reserved for updershoot 100mv
PD32
NC_CH751H-40PT
DCBATOUT
PR123
15K_J
0402
PR3
1K_J
0402
24,25,59,61 RUN_ON1
1_05V_ON
PC103
0603_Y5V
NC_2.2U_16V_Z
+3VALW
PR124
10K_J
0402
PC104
0402_Y5V
0.01U_50V_Y
PC105
1U_6.3V_M
0402_X5R
+5VALW
PR125
10_J
0603
OZ811_AVDD
PC109
1U_6.3V_M
0402_X5R
PD1
CH751H-40PT
1_05V_BST
PR12
3.3_F
0603
PU12
VDDP
VDDA
BST
HDR
LX
LDR
VIN
ON/SKIP
PGD
VSET
VREF
TSET
OCT
GNDP
GNDA
CSP
CSN
OZ811LN
VIN_1_05V
1_05V_ON
RUN_PWRGD
25,30,33 RUN_PWRGD
OZ811_BST
OZ811_HDR
OZ811_LX
OZ811_LDR
OZ811_VSET
OZ811_REF
OZ811_TEST
OZ811_CSP
OZ811_CSN
OZ811_OCT
DVT : improve 1.05V noise
PQ8
AOL1426
PC8
0.1U_50V_K
0603_X7R
PQ4
AOL1412
PL1
1.0UH_11.5x10.4
PCMC104T-1R0MN
1A
PVT 5/17
DCBATOUT
PC22
0.1U_50V_K
0603_X7R
PC21
10U_25V_M
1206_X5R
+1_05VRUN
14A
PVT 5/17
PC5
330U_2.5V_M
7.3x4.3x1.9
PC4
330U_2.5V_M
7.3x4.3x1.9
PC19
0402_X5R
0.1U_6.3V_K
CAP42
NC_330U_2.5V_M
7.3x4.3x1.9
DVT : reserved for updershoot 100mv
PR13
51R_F
0402
PR15
100K_F
0402
PR129
590K_F
0402
PC11
3300P_50V_K
0402_X7R
PR127
160K_F
0402
PR8
30K_F
0402
PC3
0.1U_16V_Y_Y
0402
PC1
0.1U_16V_Y_Y
0402
PR5
100K_F
0402
PC106
0.022U_16V_M
0402_X7R
PR9
100K_F
0402
PC9
1000P_50V_M
0402_X7R
PC111
1000P_50V_M
0402_X7R
PC113
22P_50V_J
0402_NPO
OZ811_AGND
7A
+1_05VRUN
PJ22
OPEN2B
PJ23
OPEN2B
+VGFX_CORE
PVT 5/17 : PJ22 and
PJ23 need to short
with internal graphic
GP9
CLOSE_JUMP_40X50
+1_8V_S3_SUS
3.6A
PC100
220U_2.5V_M
3528
+1_5VRUN
3.6A
PQ42
AOD452
PVT 5/17
PC180
1U_6.3V_M
0402_X5R
PU11
IN
DRV
GND
ADJ
EN
PGD
SC339SKTRT
SC339_DRV
SC339_ADJ
SC339_PGD
V0=(1+R1/R2)*0.5=1.5
DVT:change to RUN_ON for 3.3V and 1.5V timing
too long, MB_FLASH_EN have glitch ,
can't boot from debug board
24,25,29,57,58,64 RUN_ON
RUN_ON1
PR213
1K_J
0402
PR113
NC_1K_J2
0402
1_5V_ON
PC181
NC_2.2U_16V_Z
0603_Y5V
PR115
10K_J
0402
PC97
220U_2.5V_M
3528
PC98
220U_2.5V_M
3528
49.9K_F
0402
PR207
PR206
0402
24K_F
PVT 6/18 : Change setting for 1.53V
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
SYSPWM
Size
A3
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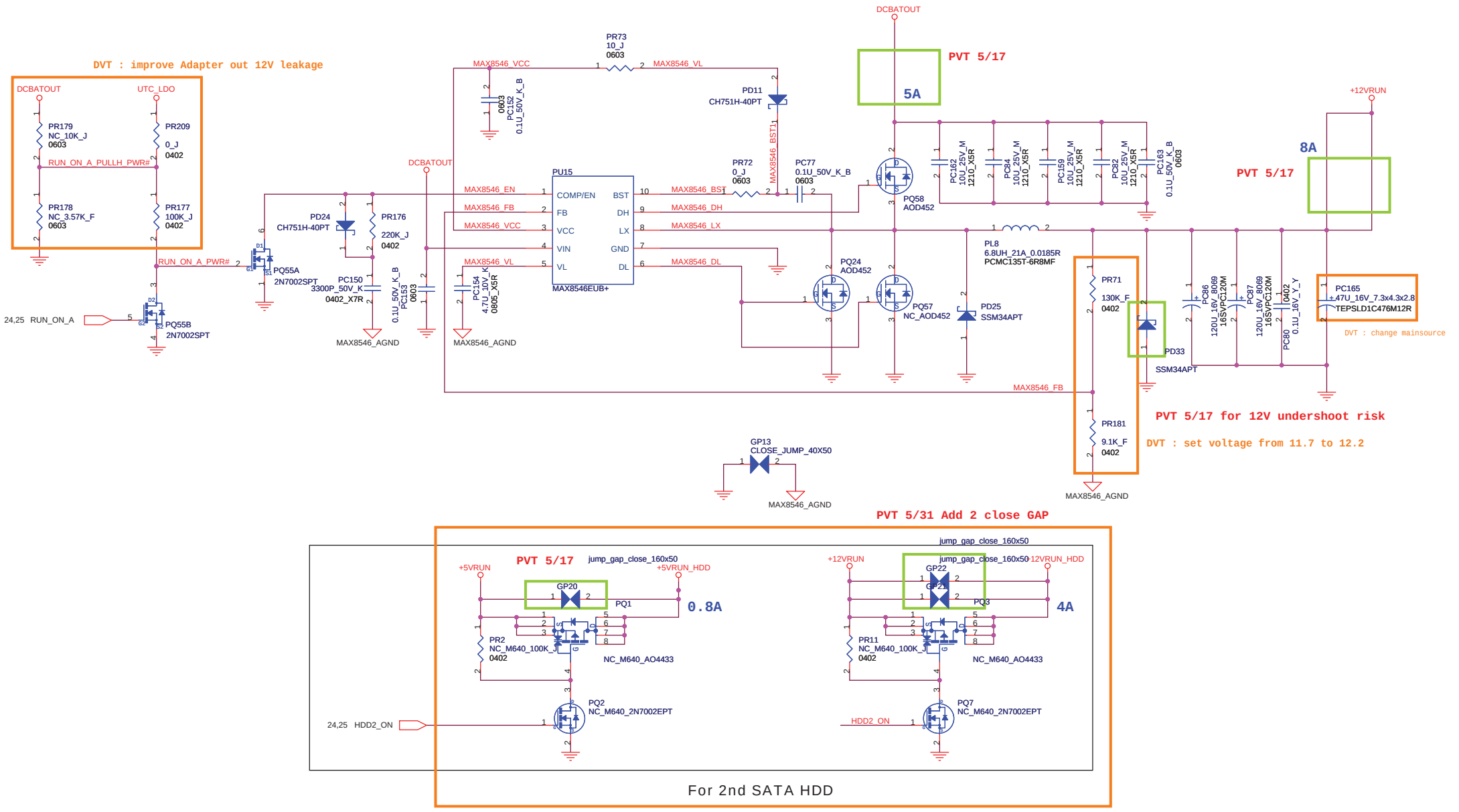

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	+12VRUN POWER(MAX8546)
Size A3	Document Number M630/M640 Rev SB
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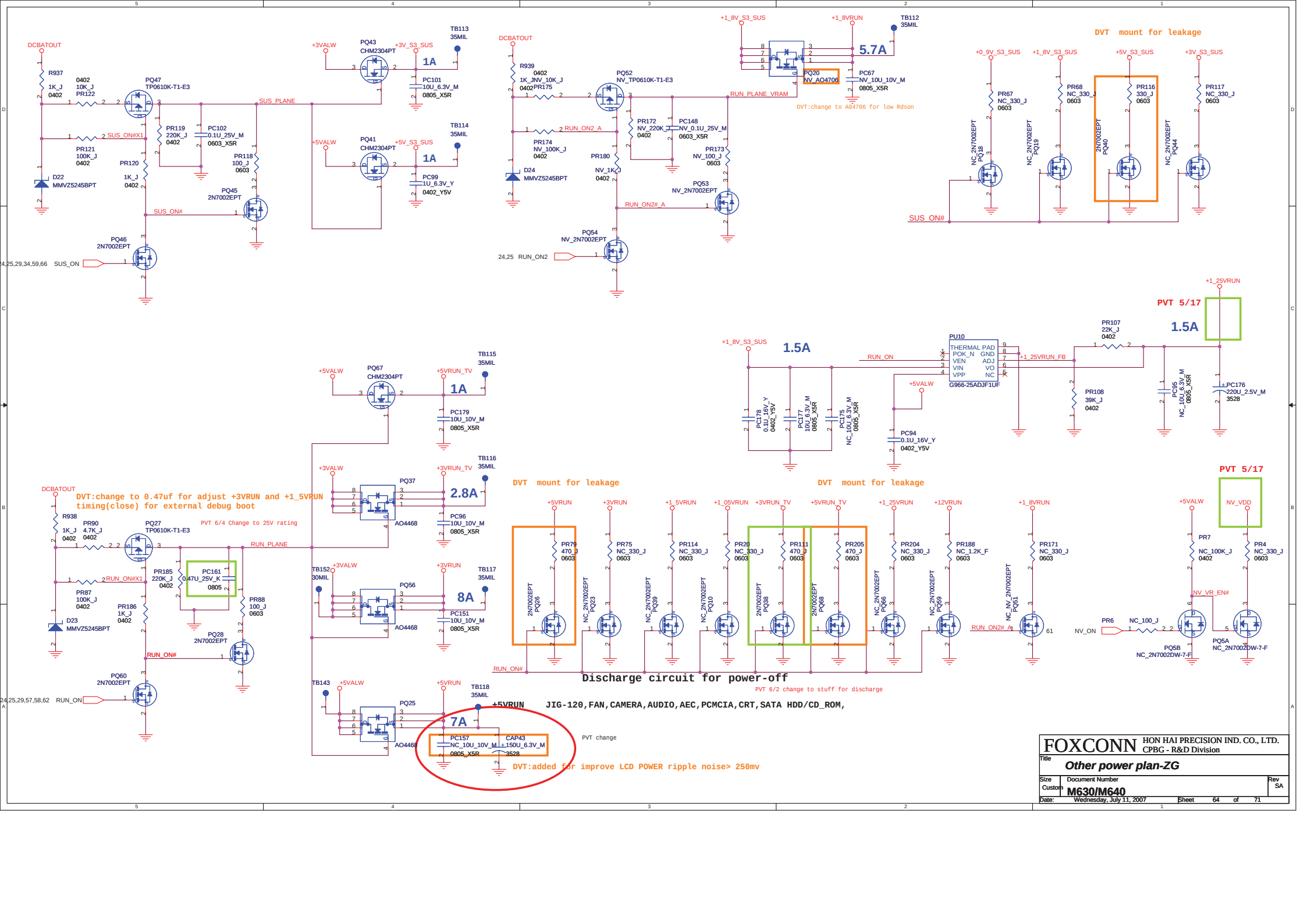
DCBATOUT
R937
1K_J
0402
PR122
0402
10K_J
PQ47
TP0610K-T1-E3
SUS_PLANE
SUS_ON#X1
PR121
100K_J
0402
PR119
220K_J
0402
PC102
0.1U_25V_M
0603_X5R
PR120
1K_J
0402
PR118
100_J
0603
D22
MMVZ5245BPT
PQ45
2N7002EPT
SUS_ON#
PQ46
2N7002EPT
4,25,29,34,59,66 SUS_ON
+3VALW
PQ43
CHM2304PT
+3V_S3_SUS
TB113
35MIL
1A
PC101
10U_6.3V_M
0805_X5R
+5VALW
PQ41
CHM2304PT
+5V_S3_SUS
TB114
35MIL
1A
PC99
1U_6.3V_Y
0402_Y5V
DCBATOUT
R939
0402
1K_JNV_10K_J
0402PR175
PQ52
NV_TP0610K-T1-E3
RUN_PLANE_VRAM
RUN_ON2_A
PR174
NV_100K_J
0402
PR180
NV_1K_J
0402
PR172
NV_220K_J
0402
PC148
NV_0.1U_25V_M
0603_X5R
PR173
NV_100_J
0603
D24
MMVZ5245BPT
PQ53
NV_2N7002EPT
RUN_ON2# A
PQ54
NV_2N7002EPT
24,25 RUN_ON2
+1_8V_S3_SUS
+1_8VRUN
TB112
35MIL
5.7A
PQ20
NV_AO4706
PC67
NV_10U_10V_M
0805_X5R
DVT:change to A04706 for low Rdson
DVT mount for leakage
+0_9V_S3_SUS
+1_8V_S3_SUS
+5V_S3_SUS
+3V_S3_SUS
PR67
NC_330_J
0603
PR68
NC_330_J
0603
PR116
330_J
0603
PR117
NC_330_J
0603
NC_2N7002EPT
PQ18
NC_2N7002EPT
PQ19
2N7002EPT
PQ40
NC_2N7002EPT
PQ44
SUS_ON#
PVT 5/17
+1_25VRUN
1.5A
+1_8V_S3_SUS
1.5A
RUN_ON
PU10
THERMAL PAD
POK_N GND
VEN ADJ
VIN VO
VPP NC
G966-25ADJF1UF
+1_25VRUN_FB
PR107
22K_J
0402
PR108
39K_J
0402
PC178
0.1U_16V_Y
0402_Y5V
PC177
100_6.3V_M
0805_X5R
PC175
NC_100_6.3V_M
0805_X5R
+5VALW
PC94
0.1U_16V_Y
0402_Y5V
PC95
NC_100_6.3V_M
0805_X5R
±PC176
220U_2.5V_M
3528
DCBATOUT
DVT:change to 0.47uf for adjust +3VRUN and +1_5VRUN
timing(close) for external debug boot
R938
1K_J
0402
PR90
4.7K_J
0402
PQ27
TP0610K-T1-E3
PVT 6/4 Change to 25V rating
RUN_PLANE
RUN_ON#X1
PR185
220K_J
0402
PC161
0.47U_25V_K
0805
PR87
100K_J
0402
PR186
1K_J
0402
PR88
100_J
0603
D23
MMVZ5245BPT
PQ28
2N7002EPT
RUN_ON#
PQ60
2N7002EPT
24,25,29,57,58,62 RUN_ON
+5VALW
PQ67
CHM2304PT
+5VRUN_TV
TB115
35MIL
1A
PC179
10U_10V_M
0805_X5R
+3VALW
PQ37
+3VRUN_TV
TB116
35MIL
2.8A
AO4468
PC96
10U_10V_M
0805_X5R
TB152
30MIL
+3VALW
PQ56
+3VRUN
TB117
35MIL
8A
AO4468
PC151
10U_10V_M
0805_X5R
TB143
+5VALW
PQ25
+5VRUN
TB118
35MIL
7A
AO4468
PC157
NC_10U_10V_M
0805_X5R
CAP43
±150U_6.3V_M
3528
PVT change
DVT:added for improve LCD POWER ripple noise> 250mv
DVT mount for leakage
DVT mount for leakage
+5VRUN
+3VRUN
+1_5VRUN
+1_05VRUN
+3VRUN_TV
+5VRUN_TV
+1_25VRUN
+12VRUN
+1_8VRUN
PR79
470_J
0603
2N7002EPT
PQ26
PR75
NC_330_J
0603
NC_2N7002EPT
PQ23
PR114
NC_330_J
0603
NC_2N7002EPT
PQ39
PR20
NC_330_J
0603
NC_2N7002EPT
PQ10
PR111
470_J
0603
2N7002EPT
PQ38
PR205
470_J
0603
2N7002EPT
PQ68
PR204
NC_330_J
0603
NC_2N7002EPT
PQ66
PR188
NC_1.2K_F
0603
NC_2N7002EPT
PQ69
PR171
NC_330_J
0603
NC_2N7002EPT
PQ61
RUN_ON2# A
61
RUN_ON#
Discharge circuit for power-off
PVT 6/2 change to stuff for discharge
PVT 5/17
+5VALW
NV_VDD
PR7
NC_100K_J
0402
PR4
NC_330_J
0603
NV_VR_EN#
PR6
NC_100_J
NV_ON
PQ5B
NC_2N7002DW-7-F
PQ5A
NC_2N7002DW-7-F
+5VRUN JIG-120,FAN,CAMERA,AUDIO,AEC,PCMCIA,CRT,SATA HDD/CD_ROM,
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
Other power plan-ZG
Size
Custom
Document Number
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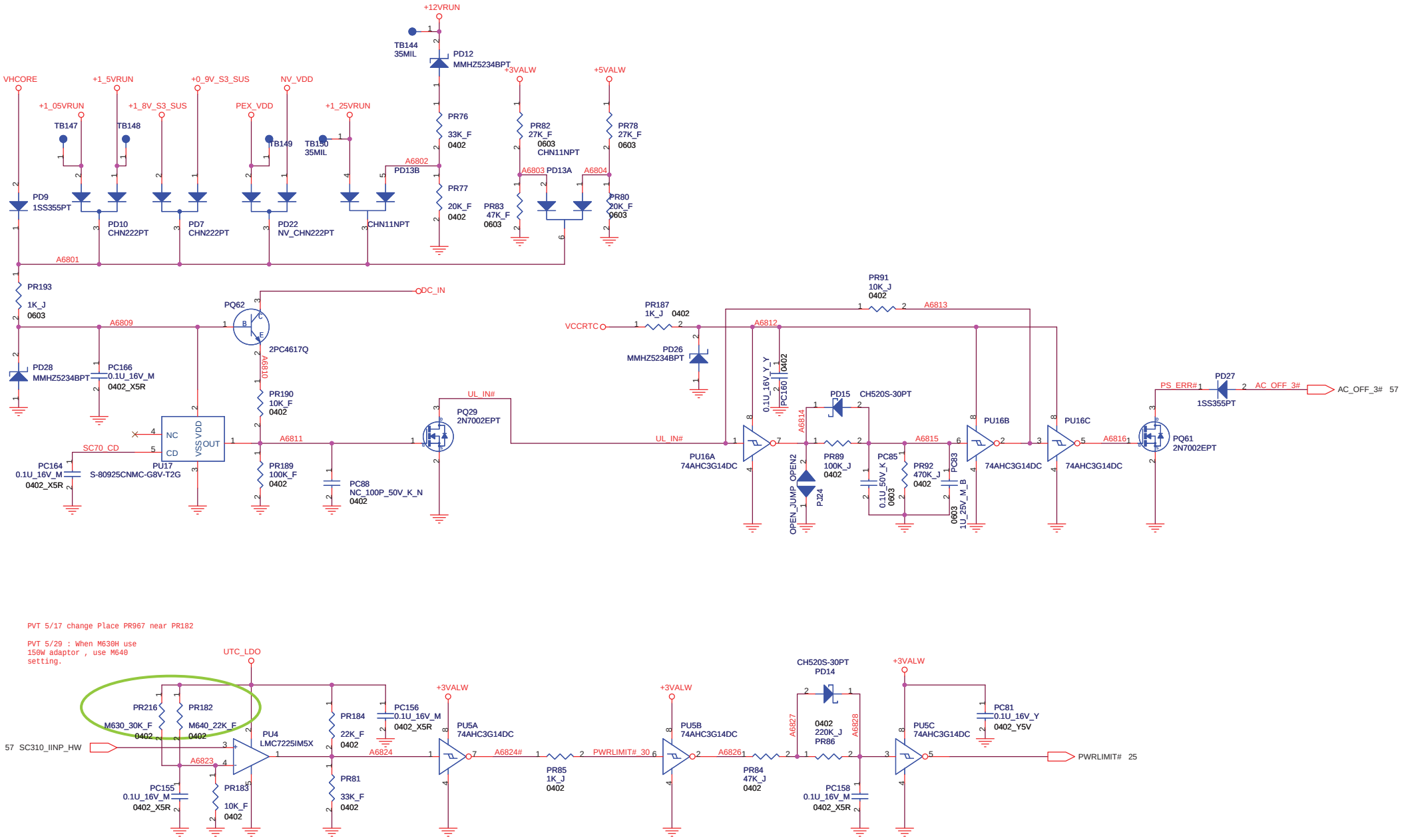

PWLIMIT
System power saving mode set
PWLIMIT active at 95%

MS630 120W	MS640
PR216 =30K	PR182=22K
PR183 =10K ==>114W	PR183=10K ==>140W

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *OVP protection-ZG*

Size: A3 | Document Number: M630/M640 | Rev: SA

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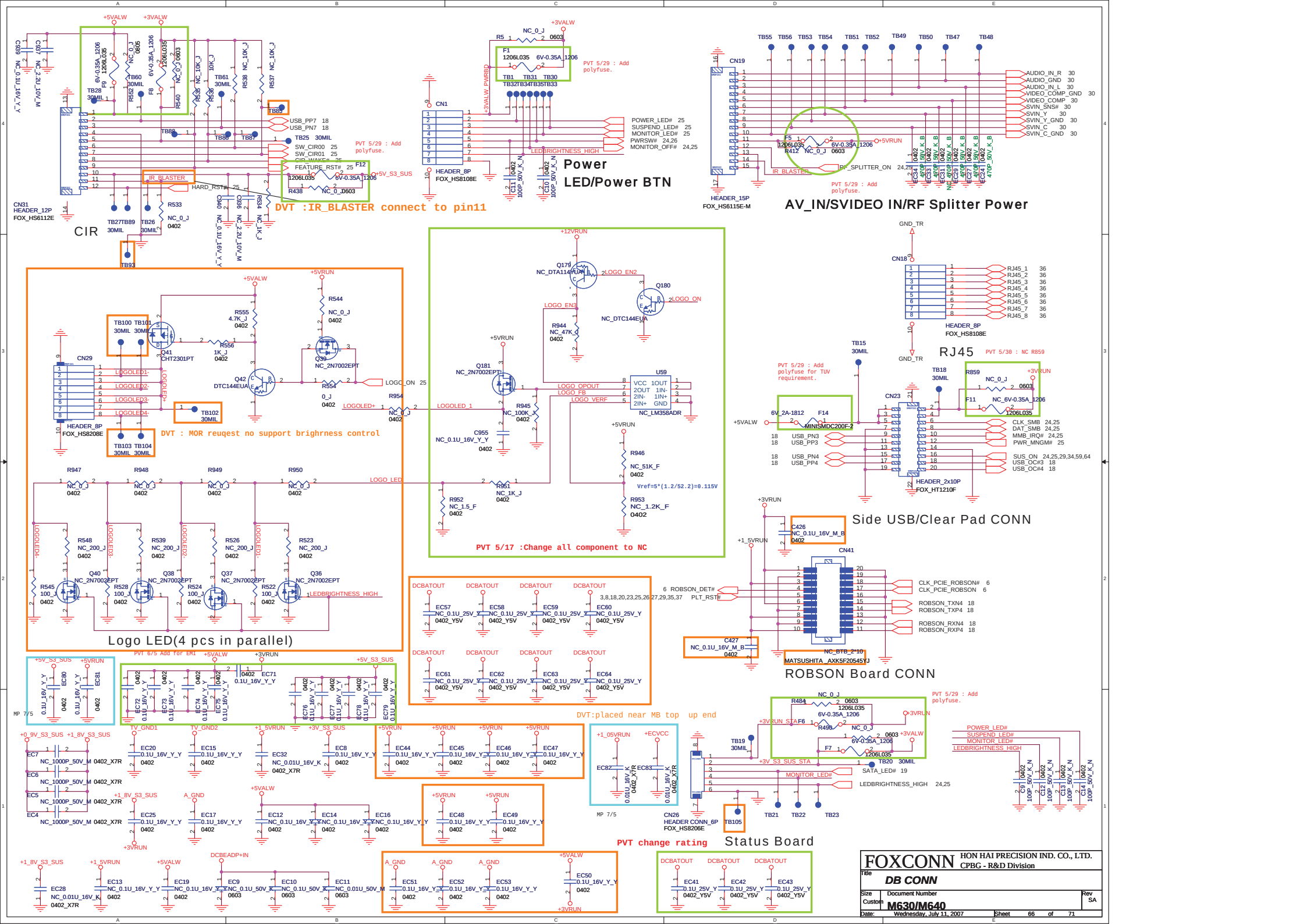
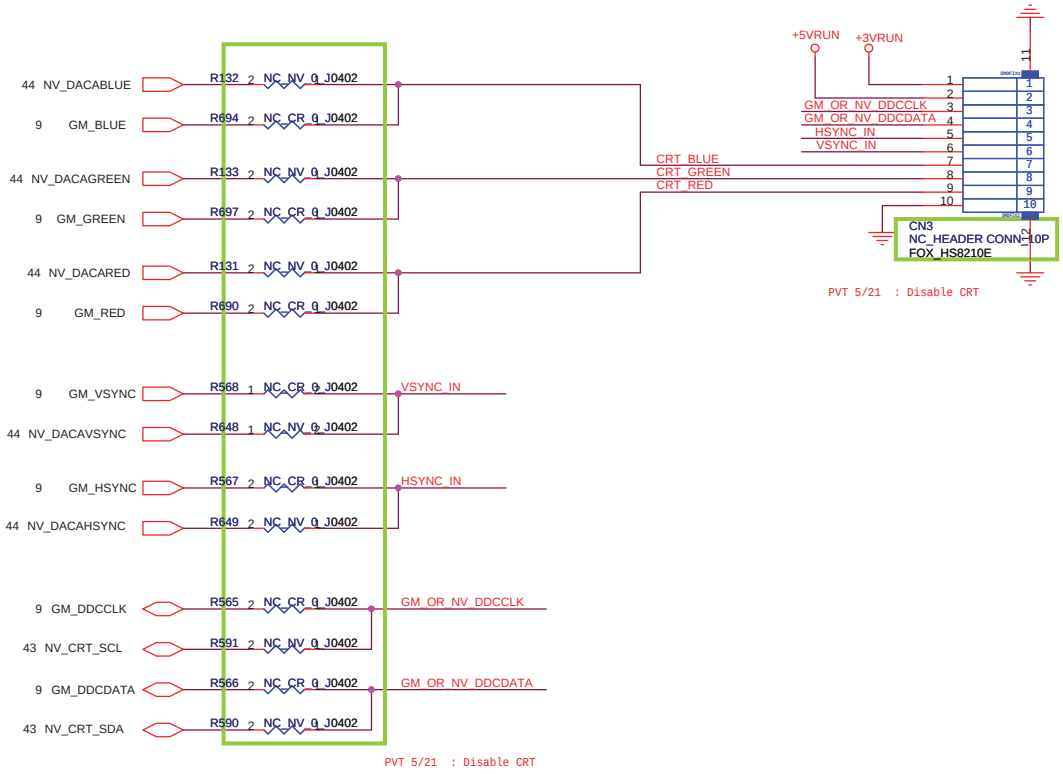
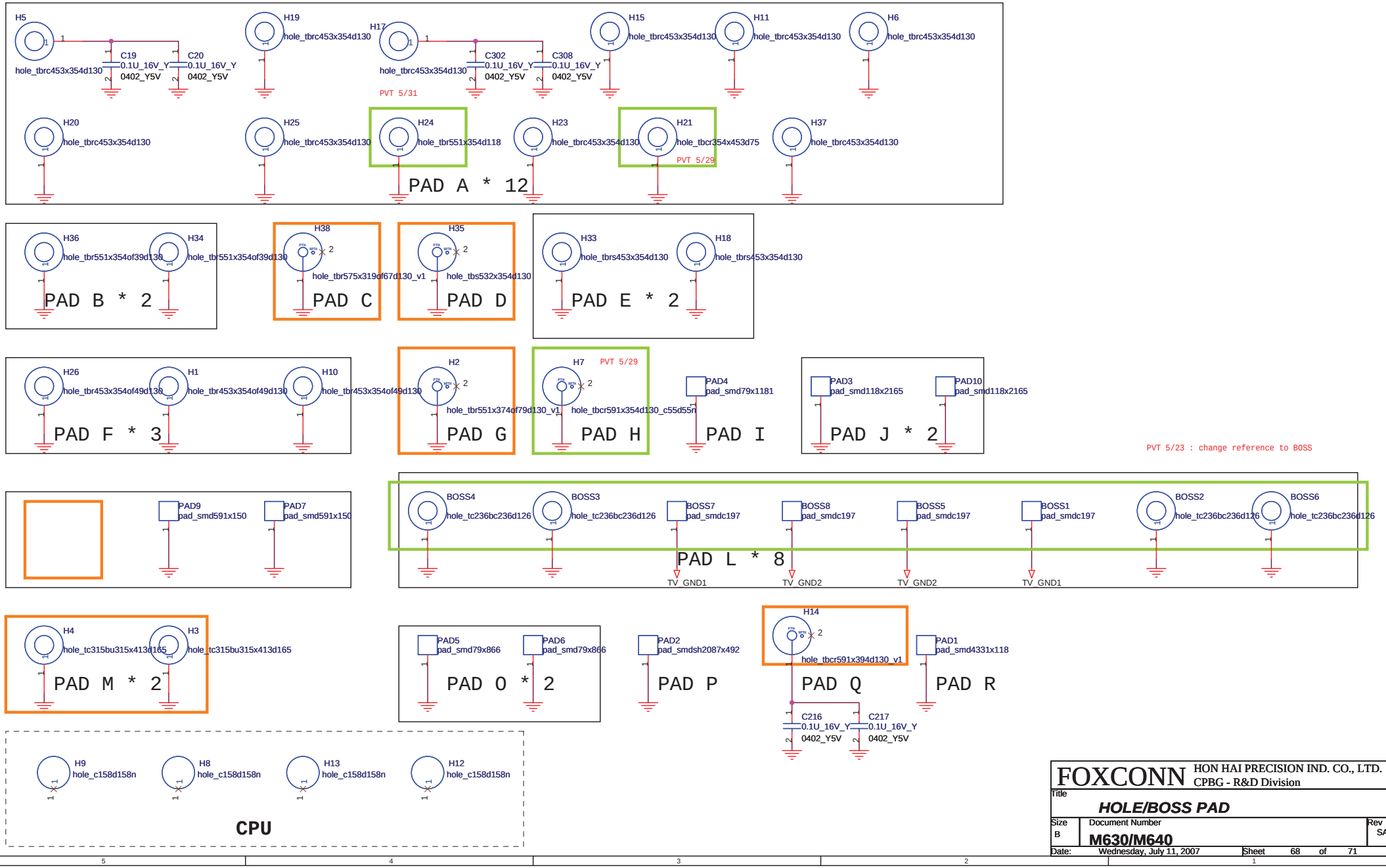

CIR
DVT :IR_BLASTER connect to pin11
Power
LED/Power BTN
AV_IN/SVIDEO IN/RF Splitter Power
DVT : MOR reuqest no support brighrness control
Logo LED(4 pcs in parallel)
PVT 5/17 :Change all component to NC
RJ45
Side USB/Clear Pad CONN
ROBSON Board CONN
DVT:placed near MB top up end
Status Board
PVT change rating
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
DB CONN
M630/M640
Wednesday, July 11, 2007



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M630/M640	Rev: SA
Date: Friday, July 27, 2007	Sheet 67 of 71	



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **HOLE/BOSS PAD**

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B	M630/M640	SA

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070206
P06 update U49 symbol data to ICS9LPR358AGLFT
P55 remove R150,R146,U14 short R128 pin1 and R145 pin2 for AEC function fail

0301
NV design change
change R596 from 30 to 24.9ohm
change R502 from 40.2 to 45.3 ohm
change R52,R93,R17,R561 from 240 to 0 ohm
       R56,R95,R19,R560 from 240 to 243 ohm
change R1,R10,R18,R32,R36,R80,R102,R563 from 7.5k to 4.02k ohm

0302
 P53 modify netname for netname consistance for UNI_MIC_IN and OMNI_MIC_IN
 P25 add R940,R941 for KBC strap pin pull low
 P30 add C950 for RUN_PWRGD interferenced ,hang 49
 P24 mount R398 for THERMTRIP_GFX#_R disconnection
Crystal vendor suggestion
 (1)P19 change C874,C873 to 12P
 (2)P24 change C433,C434 to 12P
AEC EEPROM mounted for S3
 P55 mount R72,U6,R75,
     NC R92,R96,R104
AEC programming GPI change
 P20 GPIO24 connect to AEC_PWRDN# for power down AEC
     GPIO20 connect to AEC_RESEt# for programming AEC
Brightness control not support for Logo LED
 P66 (1)NC Q36,R523,Q37,R526,Q38,R539,Q40,R548
     (2)change R545,R58,R524,R522 from 200 to 100 ohm
Mount parts for leakage
 P64 mount PR116,PQ40,PR205,PQ68,PR79,PQ26
MB_FLASH function fail :change MB_FLASH_EN from SB GPIO 26 to GPIO34,GPIO26 can't used as GPIO
 P20 connect GPIo6 to TP206 , connect GPIo34 to MB_FLASH_EN ,add R942
change 2nd and 3rd fan from 12V to 5V , change Q52,Q13 to CHT2301 for 5V source

P51 NC R342 for subwoofer abnormal performance
P24 add C951 for thermistor interference by inverter transformer
P50 change F3 to 1M-F1252A5-F000 for the same with M620
P51 change F10 to 1M-F1252A5-F000 for the same with M620

0305
P20 change R844 to 10K, LAN_RST# change to pull low 10K

0306
POWER
P58 change PR148,PR153 to 150K_F,PR146,PR55 to 100K_F
    to change ocp setting to 11A
P61 (1)change PR16 to 1M_F to change OCP to 15A
    (2)delete PJ10,PJ9 ,VGFX_CORE from NV_OUT
P63 change PR71 to 130K_F,PR181 to 9.1K_F , change 12V from 11.7 to 12.2v
P59 change PR25 to 8.2K_F to set OCP to 17A
P60 mount PC145,PC117 to filter high frequency noise
P58 mount PC119,PC143 to filter high frequency noise
P62 change PR12 to 3.3_F to improve 1.05V noise
P63 change PR177 to 100K_J,add PR209,NC PR179,PR178 for improve
    adapter out 12V leakage

P33 modify CN36 symbol for PCMCIA reverse type,
P35 change ln power to +3V_EMINI_AUX to support S4 wake up

0307
P50 change U26,U27 to LLP package for support 3W
P61 change PQ9 to AOL1426 ,PQ6 to AOL1412 for support 15A NV_VDD
P34 change U41,U40,U39 to MSOP8 to meet EUV 2.4mm

0309
correct EVT BOM mian source to Substitute List
(1)P50,P60 change PC53,C913,C924 to 1C-2B20153-K000
(2)change C468,C475,C480,C907 to 1C-2B20471-K000
(3)P11,P12,P50 change C265,C284,C286,C722,C710,C738,C303 to 1C-2B20474-K000
(4)P50,P51 change L24 ,L59 to 1L-BBCMS32-1600
(5)P57 ,change PL9 to 1L-FBHWP12-1000
(6)P49 ,change C241,C243,C247,C250 to 820P NPO 0603
(7)P60 ,change PC122 to 1C-2N20181-J600
P25 delete Winbond solution

0313
P60 change PC40 to 0.1u to adjust channel current sense by vendor suggestion
P54 change U16 to 78L09L , the same with M620
P61 add PR210,PQ69,change PR133 to 28K_F for VGA power mizer(1.2V and 1.15V switch)
P43 connect NV_GPIO5 to VGA power for power mizer(1.2V and 1.15V switch)
P43 change R930,R931,C938 value to NV_*
P06 connect R752 pin 1 to R750 pin1 to follow CPU_BSEL0
P27 change LED1 to HT-110NG for changing wlan led to side
P51 change CAP16~20 to 47UF for 68UF shortage(evt used 47uf)
P50 change L67,L70 to EBMS100505H121RDC35 for changing mainsource(EVT use this part)

0314
P53 change CN7 to HS8106,防呆
P67 NC CN3(CRT CONN) for ME interfere with thermal module
P34 change CN24 to FOX_UB4132C-T3201-4F,black color
P31 change CN15 to FOX_UV91413-WS01P-4F,black color
P11 delete L12,C194,C211,L17,L16,C204,L14,C226,R230
    Reserved R234 to +3VRUN and R236 to GND for UMA/Discrete selection,
    Refer to Santa Rosa design Guide Rev 2.0 Table 81.

0319
Modify for Clock SI
P30 mount R790,0 ohm and C848,22P for PCI_CB48 SI fail]
P06,P27 change RP30 to 18 ohm ,add C 2.2p for CLK_PCIE_MINI# SI fail
P06 change RP24 to 15ohm for CLK_PCIE_SATA# SI fail

P29 swap L51,L50,L49 for layout

0322
MOR
P49 remove R279 for delete Line in path
P50 change C458,C478 to 1000P ,X7R for THD/MR improvement
P50 add C for U44 bypass
P50 change C924 and C913 to NC for THD/MR improvement
P50 change the connection of CON3 pin7 and pin8 to DGND
P50 change GP3 to 0ohm resistor (mounted)
P52 delete R774 and R767 completely for delete MIC VREF path from CODEC
P49 U22 pin32 change to NC for delete MIC VREF path from CODEC

P45 change C27,C33,C48,C57 to 0.01uf by nvidia FAE suggestion
P46 change C28,C947,C5,C21 to 0.01uf by nvidia FAE suggestion

EMI
P59 change PR41 to 3.3ohm for EMI
P58 change PR23,PR65 to 3.3 ohm for EMI
P19 add EC36,EC39,EC40 33P bypass for BITCLK

P55 mount C83 for EMI

0326
(1)add AEC_EEPROM_WR# for programming AEC EEPROM
(2)connect DFGT_VR_EN to TP and delete PR10 , VGFX_CORE 1.05V fix

0327
(3)reserved Linear voltage control circuit for logo led suddenly off (U59,Q180,Q179,Q18

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Title: ***History***

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Custom	M630/M640	SA

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