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P. Leader	Check by	Design by

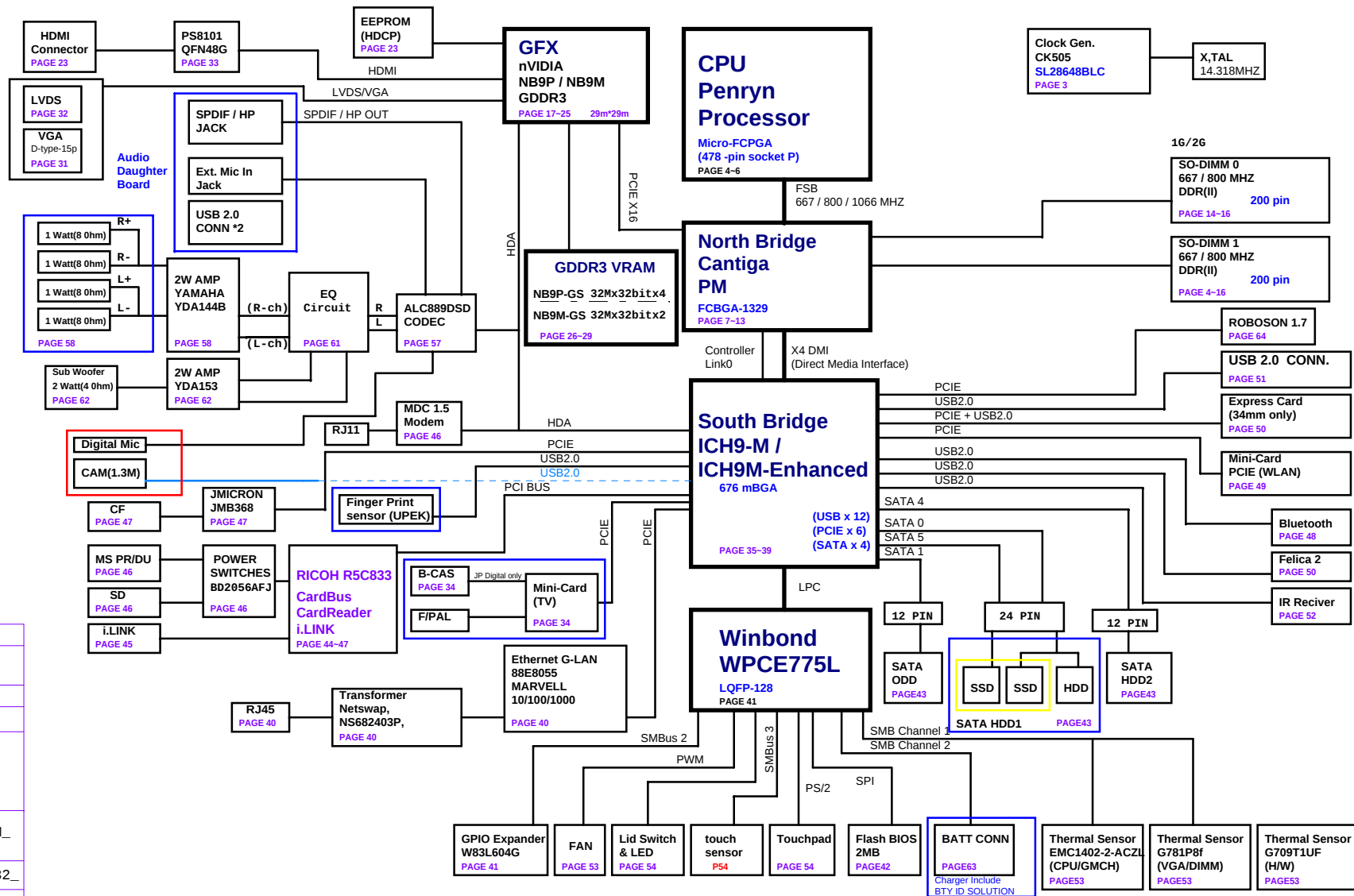
DVT to PVT

Project Code & Schematics Subject: M780 EVT Main Board

PCB P/N: FUBAI 1P-0086102-8010

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Index
Size A3	Document Number M780(MBX-194)
Date: Monday, June 16, 2008	Rev 0.1
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M780 Montevina Block Diagram



TI CHARGER	
BQ24751	P.63
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC	
ISL6236IRZA-T	P.64
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW

SYSTEM DC/DC	
SC411	P.65
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM

SYSTEM DC/DC	
ISL6269A	P.66
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS

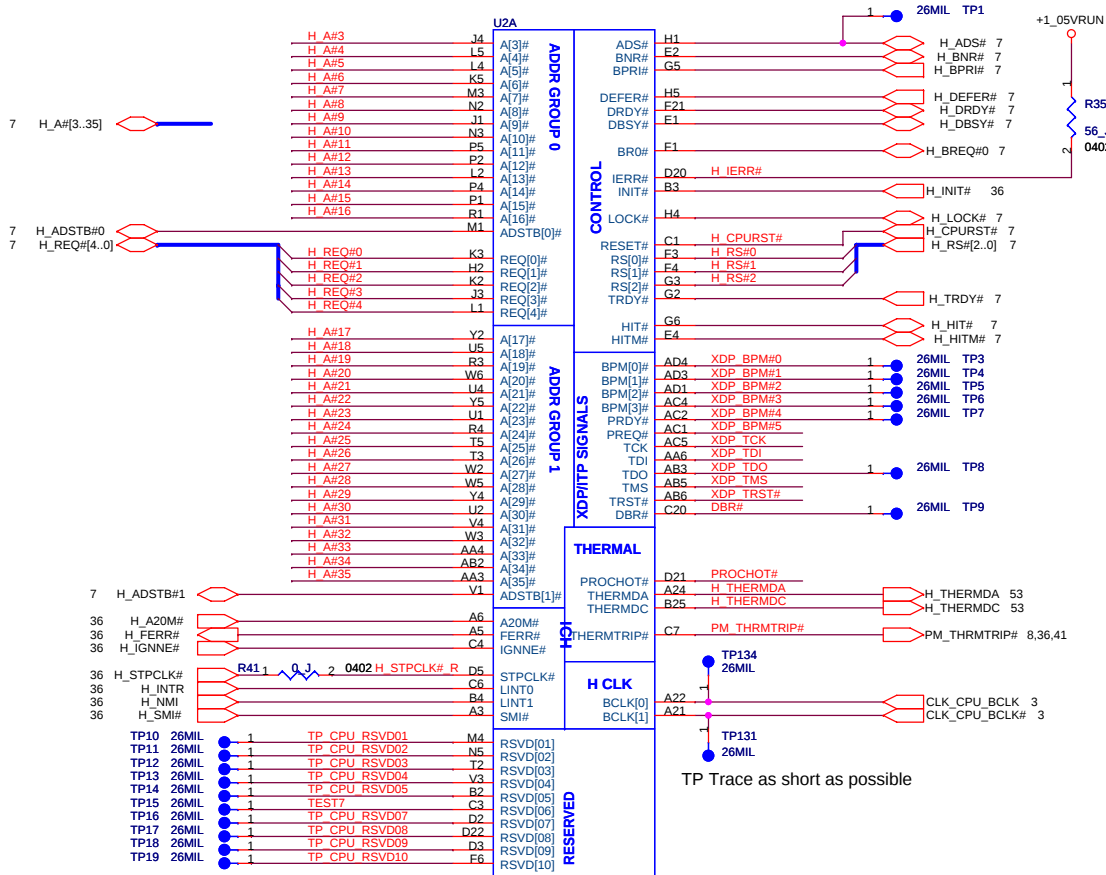
SYSTEM DC/DC	
G2998	P.66
INPUTS	OUTPUTS
DCBATOUT	+0_9VRUN

CPU DC/DC	
ISL6266A	P.67
INPUTS	OUTPUTS
DCBATOUT	VHORE

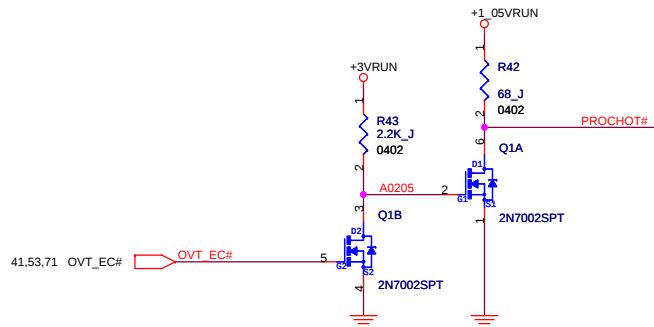
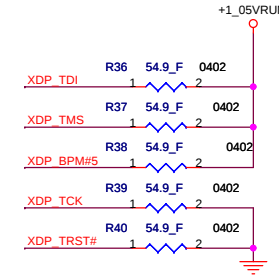
SYSTEM DC/DC	
APL5913	P.70
INPUTS	OUTPUTS
+1_5VRUN	APL5913

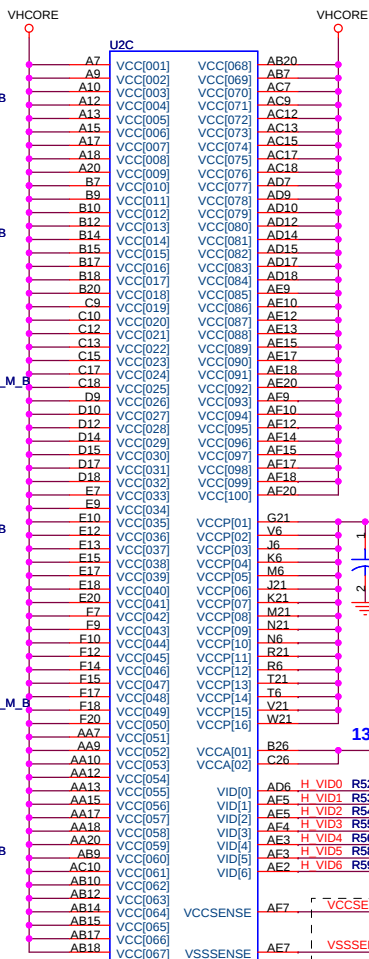
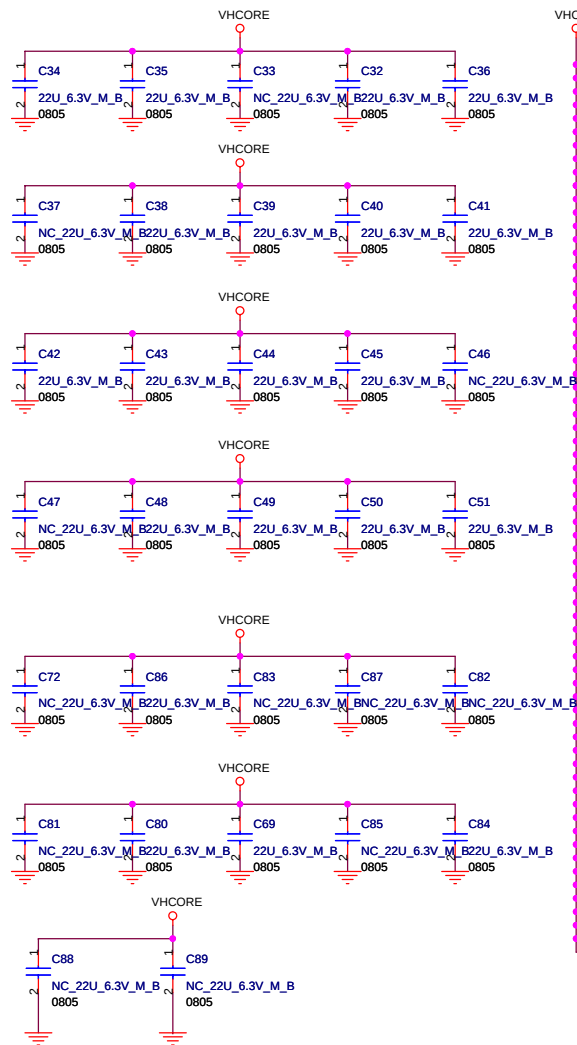
SYSTEM DC/DC	
SC411	P.70
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

M780 BOM configuration	
unstuff	NC_
NB9P-GS + NB9M-GS	NV_
for L model	NV9L_
for M model	NV9M_
B-CAS Card, Felica module for J SKU stuff	LNC_
Roboson, TV Tuner, IR, Receiver, CF Card Slot unstuff for L Model	
for H M model	NV9HM_
for L model 32Mx32 SDDR3	NV9L32_
for H model	NV9H_
for Qimonda VRAM	NV9QI_
for Samsung VRAM	NV9SAM_

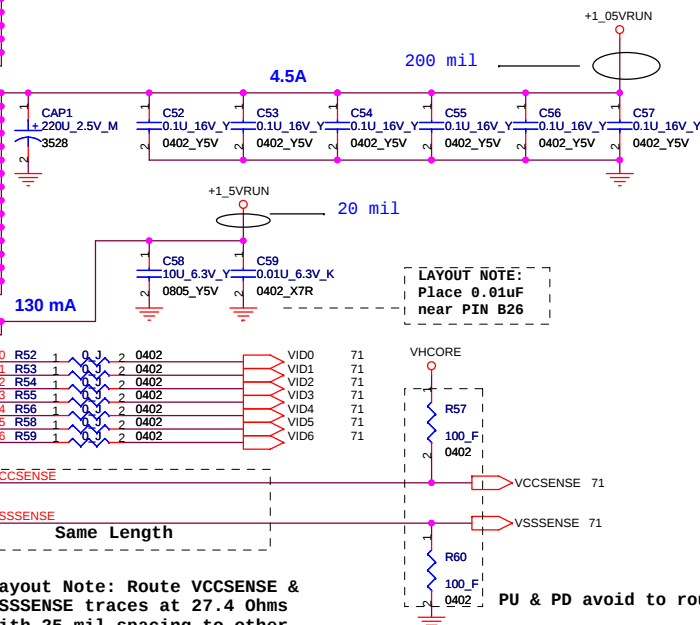


H_CPURST# 1 26MIL TP2
as Close as possible to Pin out trace



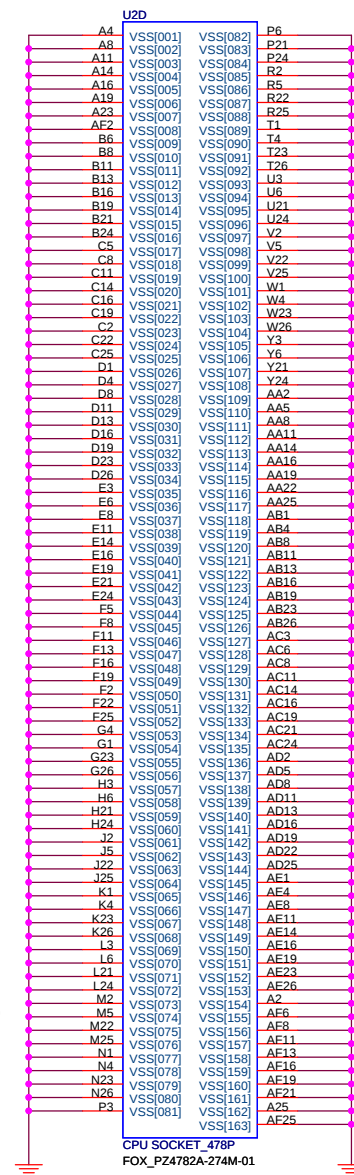


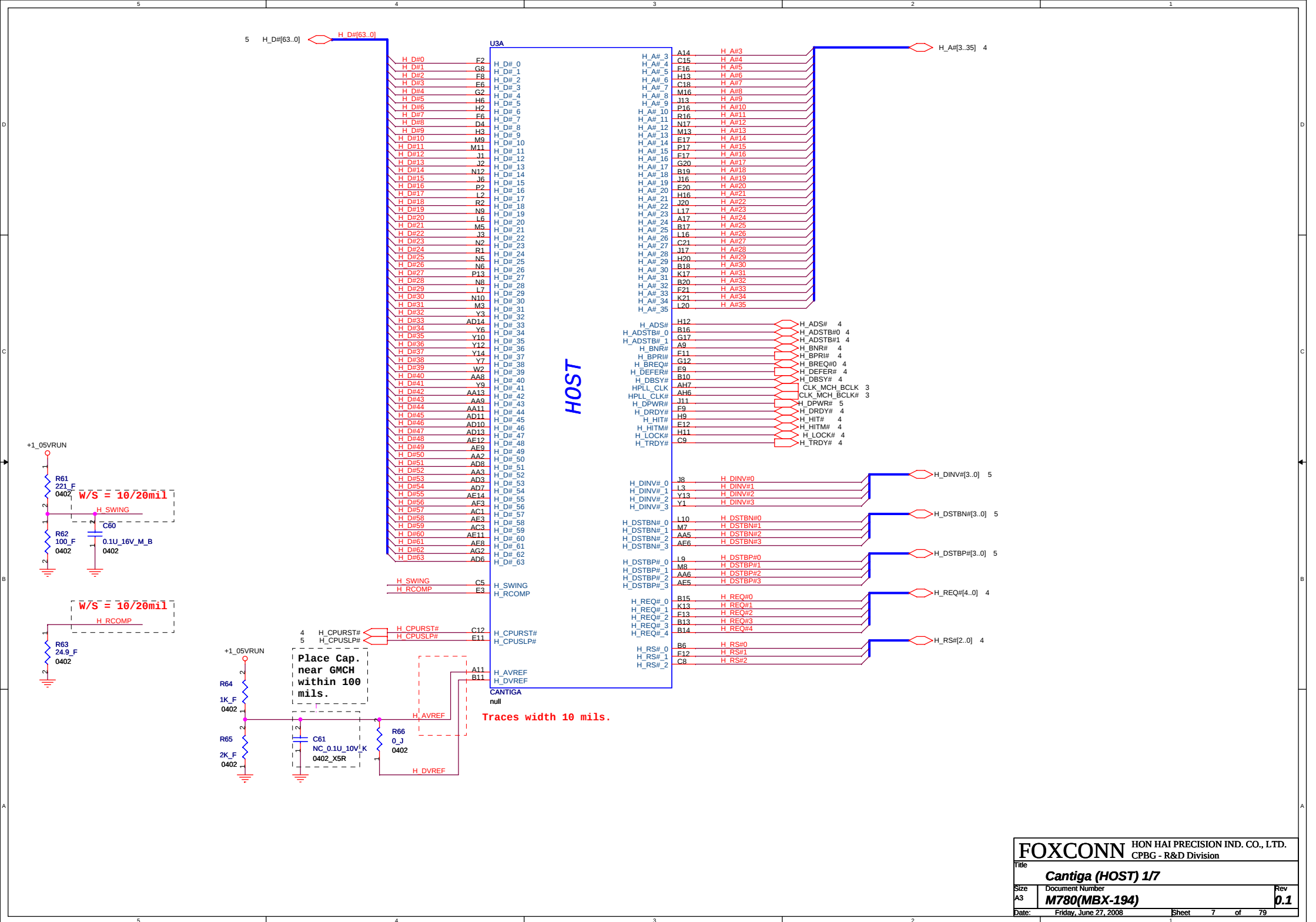
CPU_VCCA----->0.13A
CPU_VCCP----->4.5A
CPU_VCC----->47A

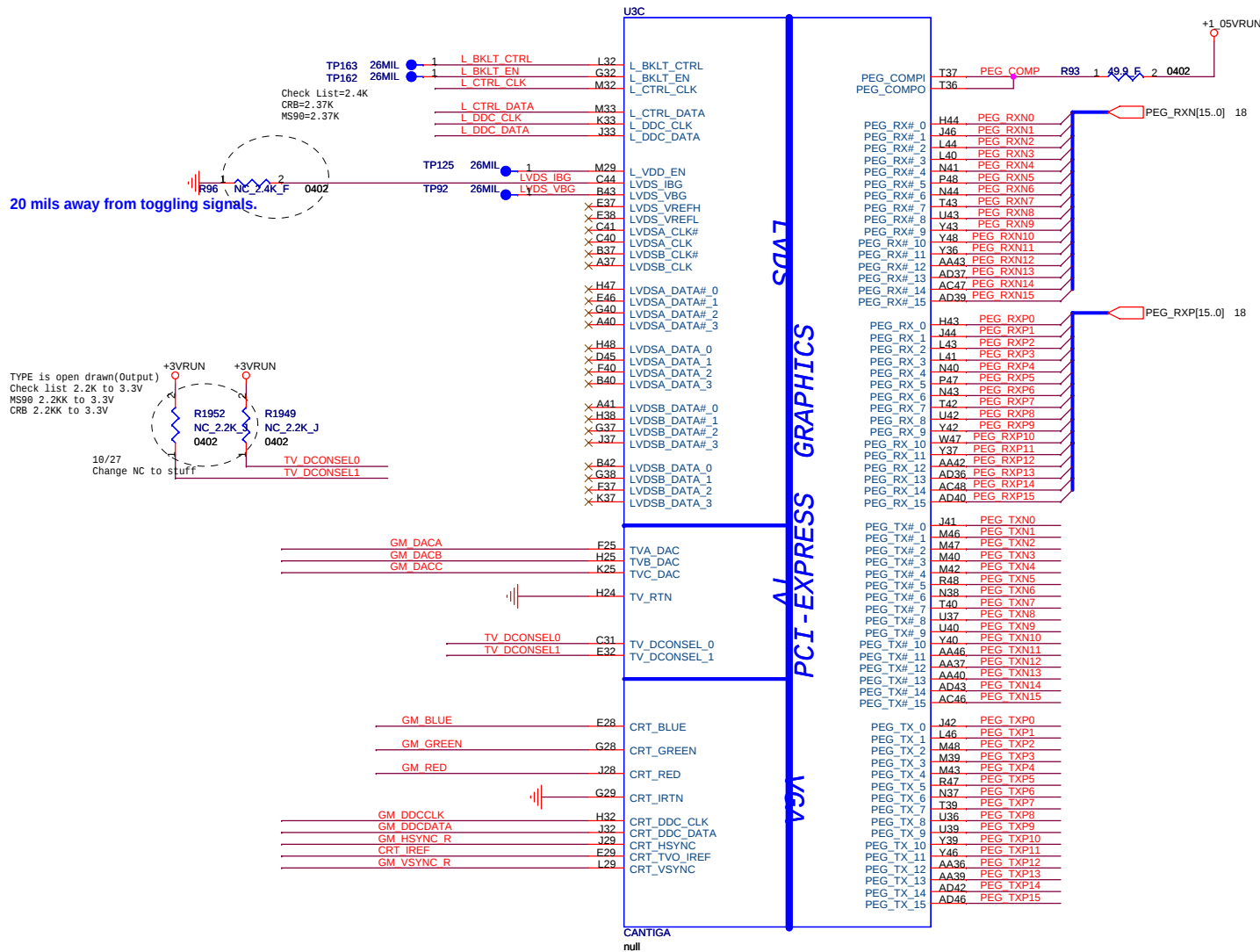


Layout Note: Route VCCS and VSSS traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

Outer width=19 mil spacing=7 mil
Inner width=14 mil spacing=7 mil
Length match < 25 mil



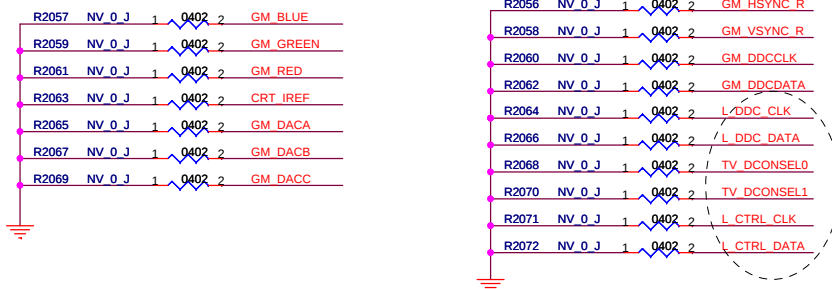


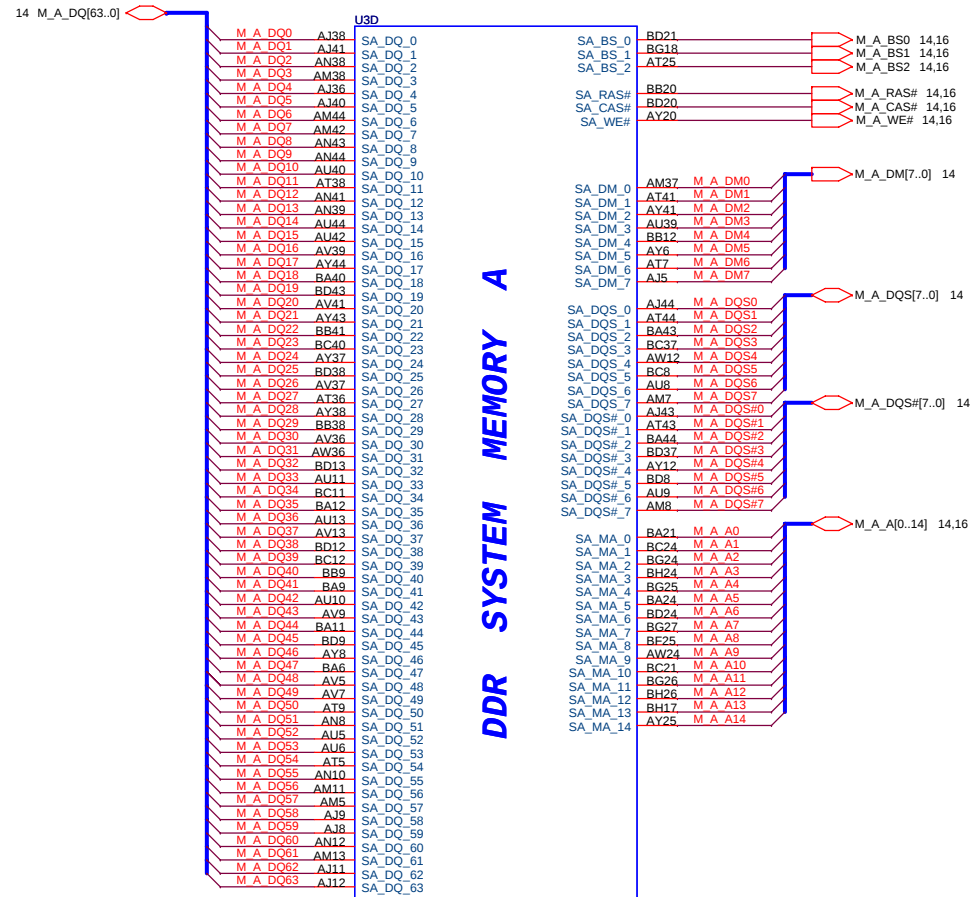


214.(Page 9) 07/11/28 Change PCIE Capcitor size from 0402 to 0201

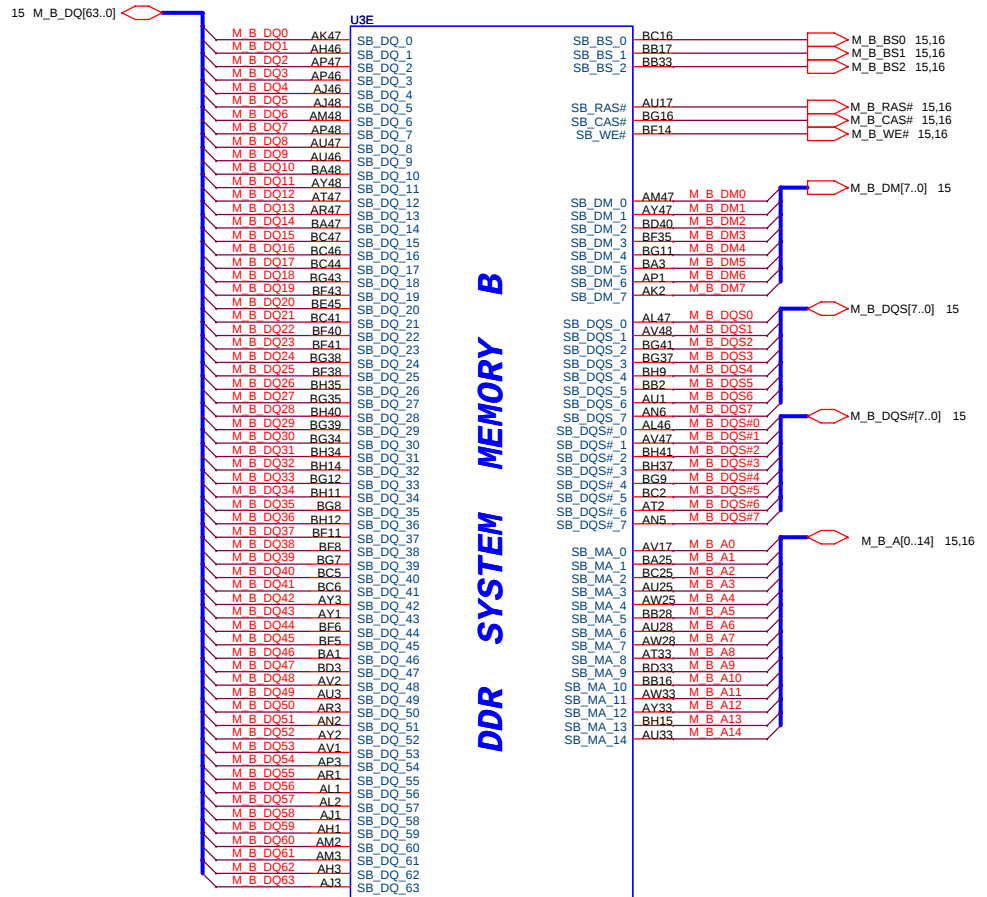


External Graphics (GMCH CRT/TVOUT Disable)

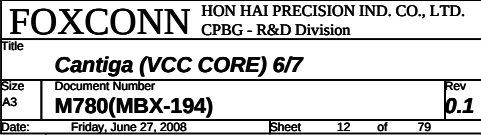


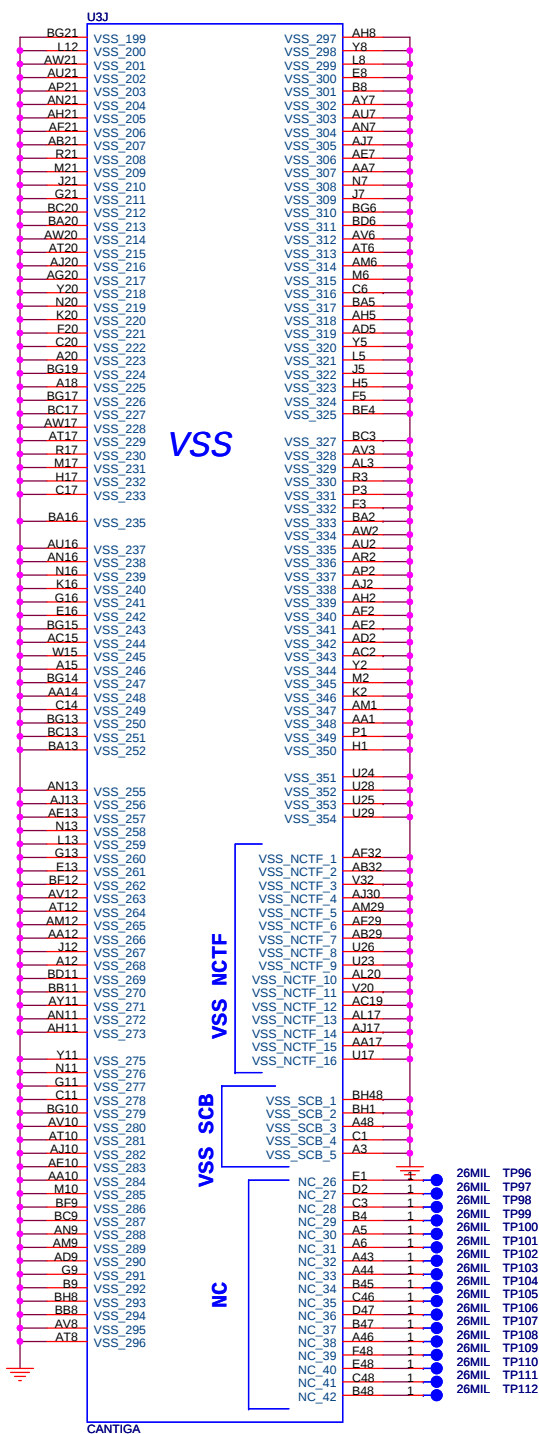
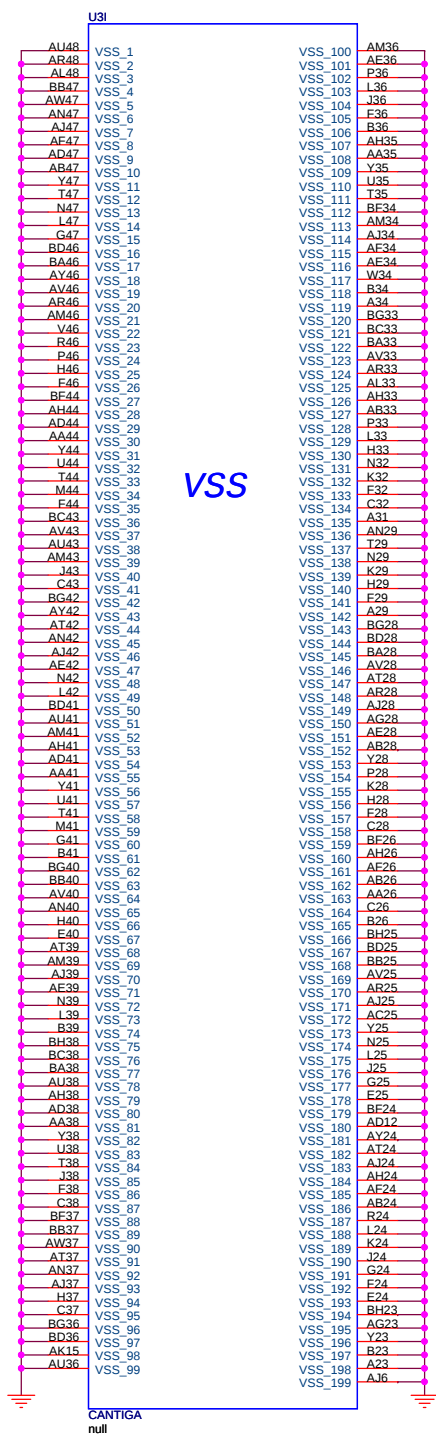


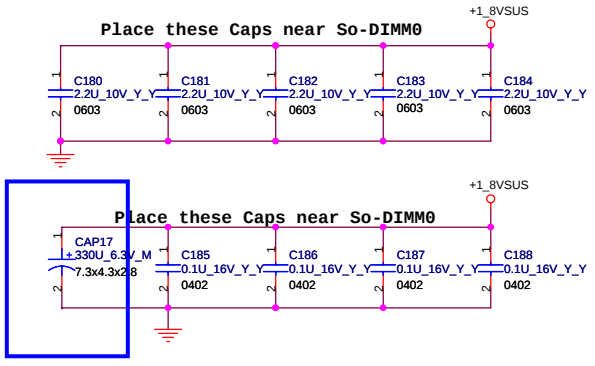
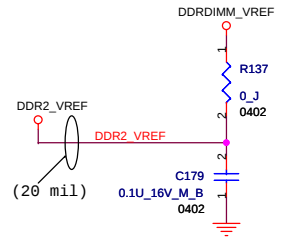
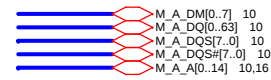
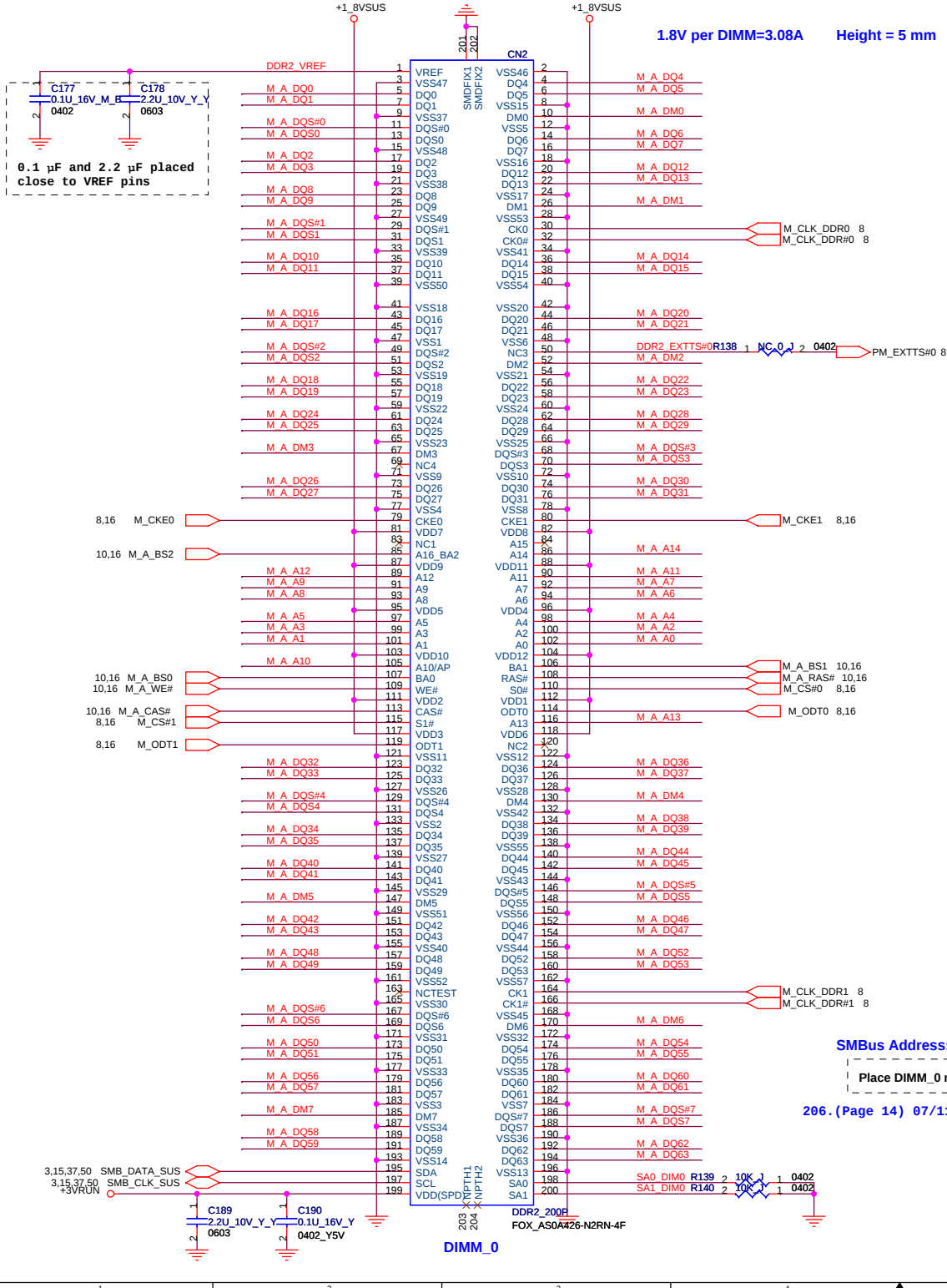
CANTIGA
null



CANTIGA
null





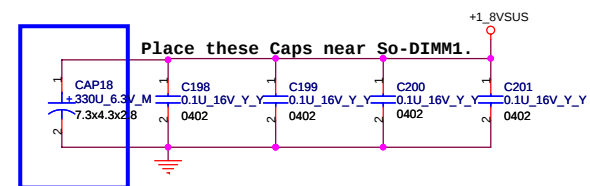
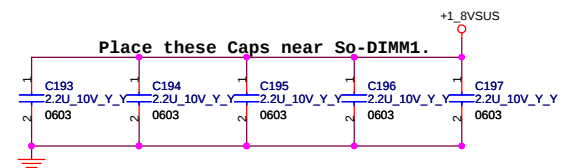
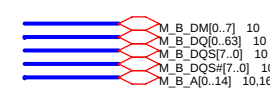


SMBus Address: A0H(W)/A1H(R)

Place DIMM_0 near GMCH

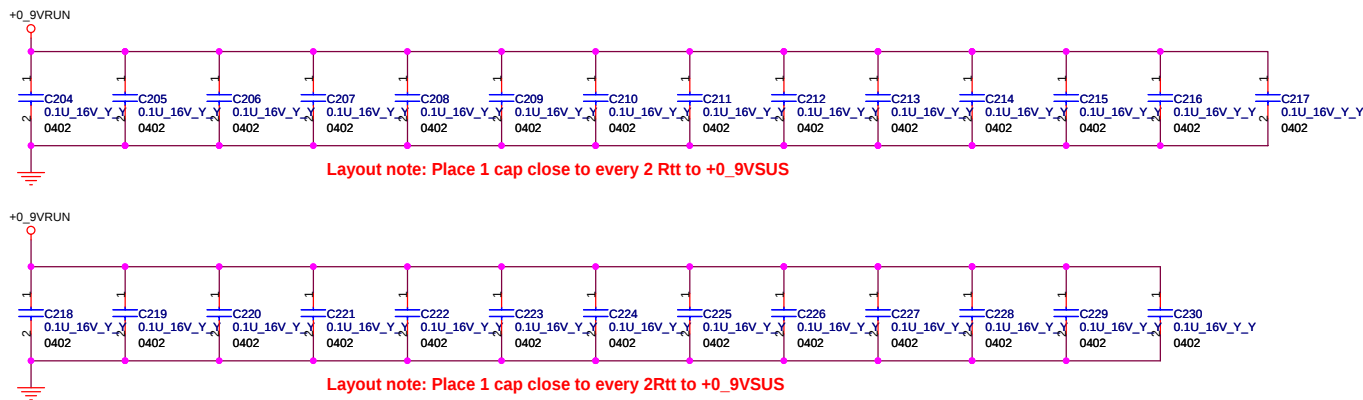
206. (Page 14) 07/11/27 change DDR2 CONN(CN1) from FOX_AS0A426-N5SN-7F to FOX_AS0A426_MN2RN_7F

FOXCONN		HON HAI PRECISION IND. CO., L.TD.	
CPBG - R&D Division			
Title: DDR(II)SO-DIMM_0			
Size: A3	Document Number: M780(MBX-194)	Rev: 0.1	
Date: Friday, June 13, 2008	Sheet: 14	of: 79	



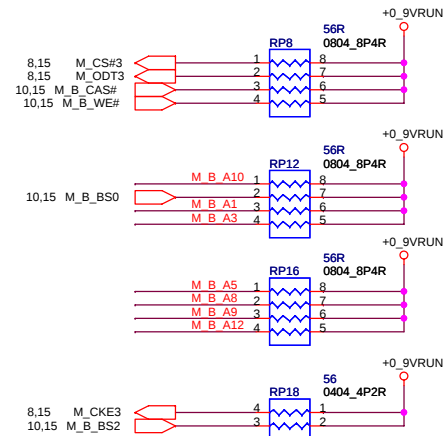
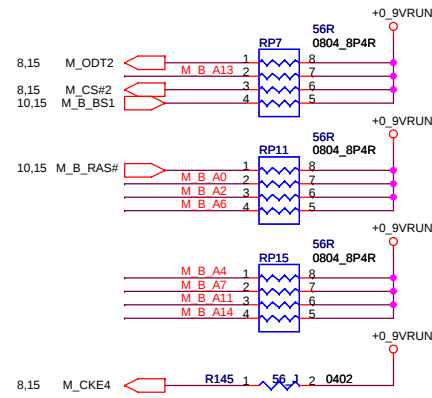
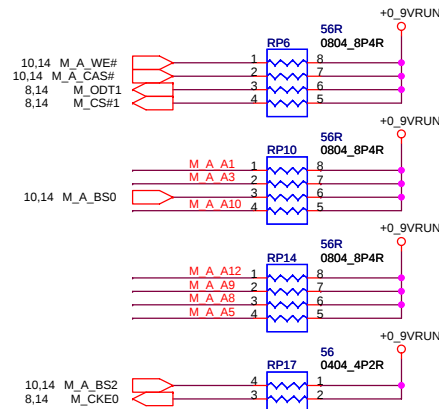
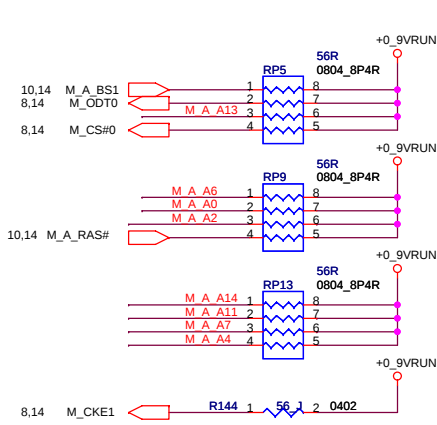
DIMM_1 is placed farther from the GMCH than DIMM_0

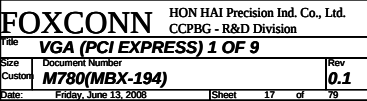
207. (Page 14) 07/11/27 change DDR2 CONN(CN2) from FOX_AS0A426_N4RC_4F to FOX_AS0A426_MARN_7F



10,14 M_A_A[0..14]

10,15 M_B_A[0..14]







XCLK_277 0 (Reserved) 1 (27M Hz)	
NB9X TVMODE[2:0] 000	
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present)	ROM_SI (XXXX)
SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk)	ROM_SO (1000)
PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK (0010)
USER[3:0] 1000	STRAP0 (1111)
NB9X 3GIO_PADCFG[3:0] 0001	STRAP1 (0001)
NB9X PCI_DEVID[4:0] NB9P-GS X1001 NB9M-GS X1001	STRAP2 (1001)

0100 64-bit Reserved
0101 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111 32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung

0000 64-bit Reserved
0001 16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010 16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011 16Mx32 GDDR3 - 136 ball 64-bit Samsung

<< ROM_SI Setting condition >>

H Model

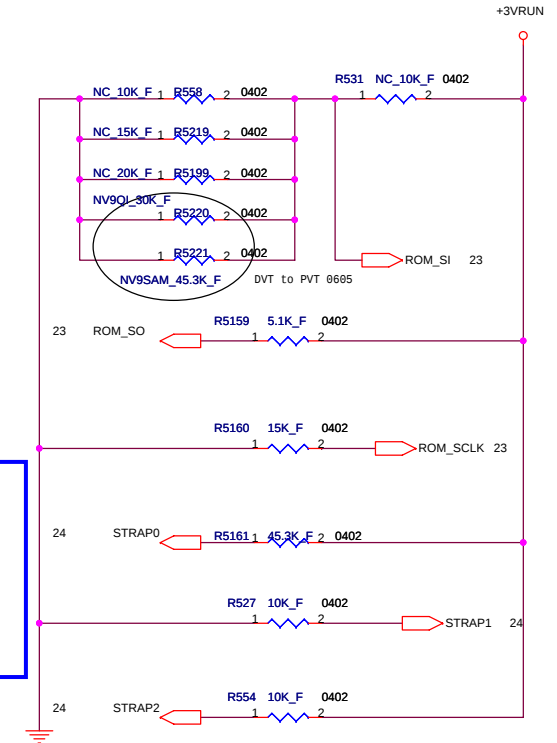
=> 32Mx32bx4 - 0101 Qimonda - 30K pull Low

M Model

=> 32Mx32bx4 - 0101(Qimonda) - 30K pul Low

L Model

=> 32Mx32bx2 - 0101 Qimonda - 30K pull Low



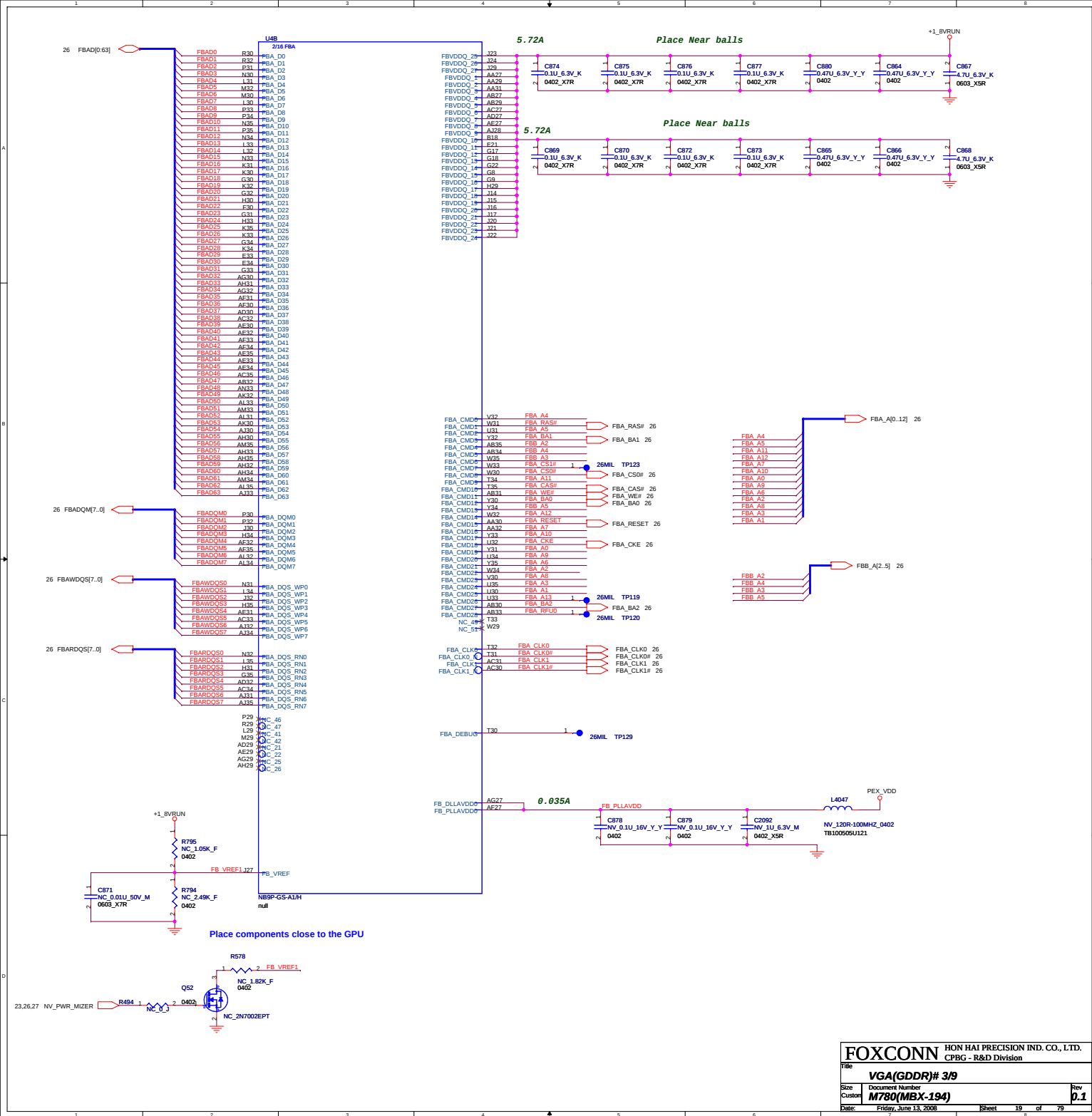
Logical Strap bit Mapping

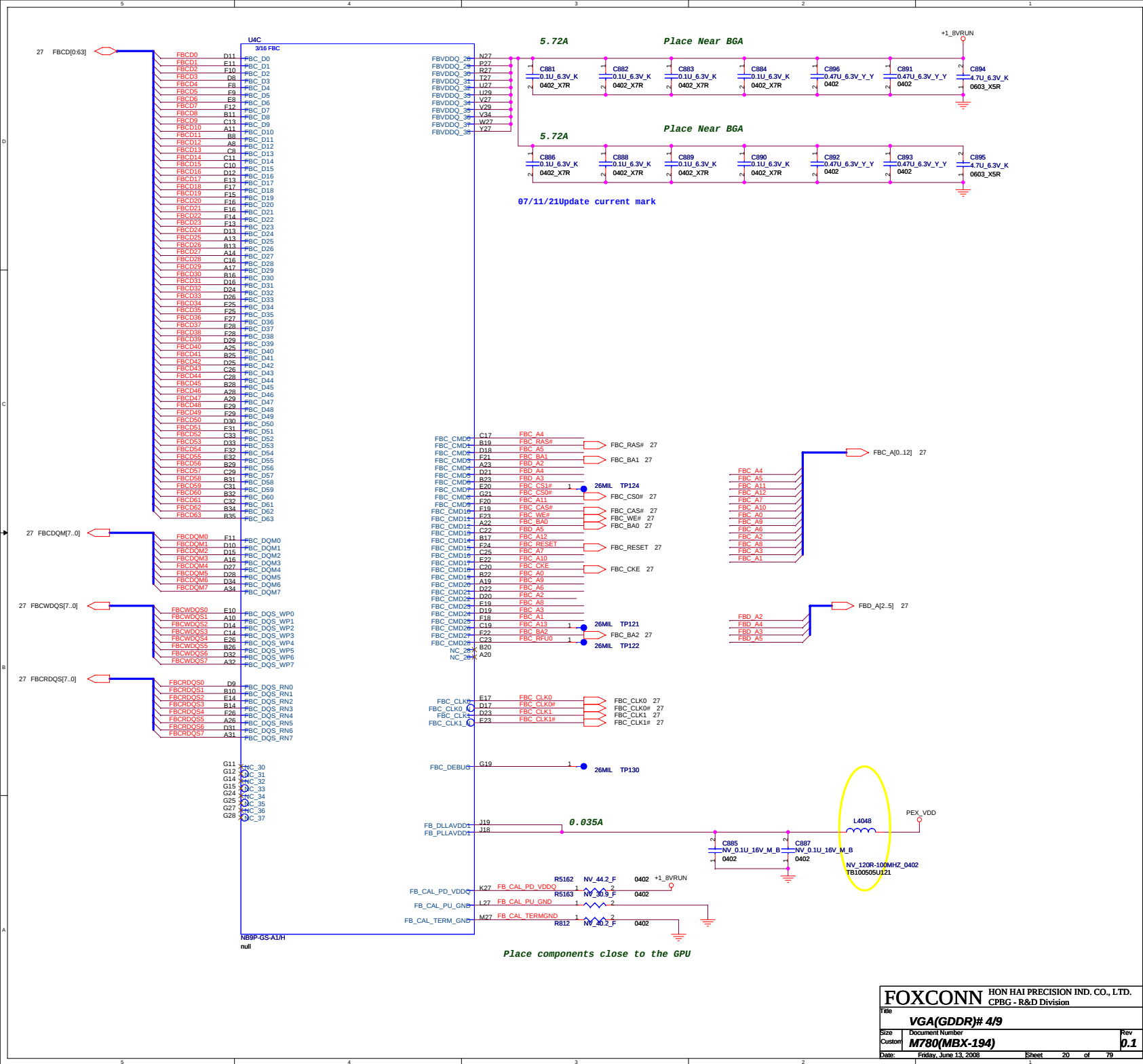
Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

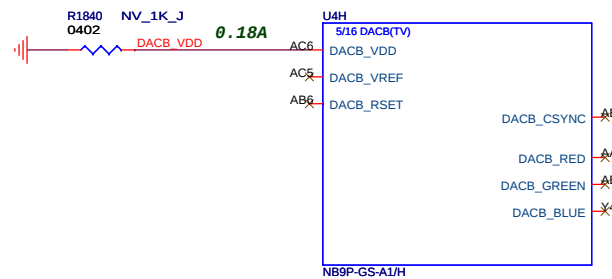
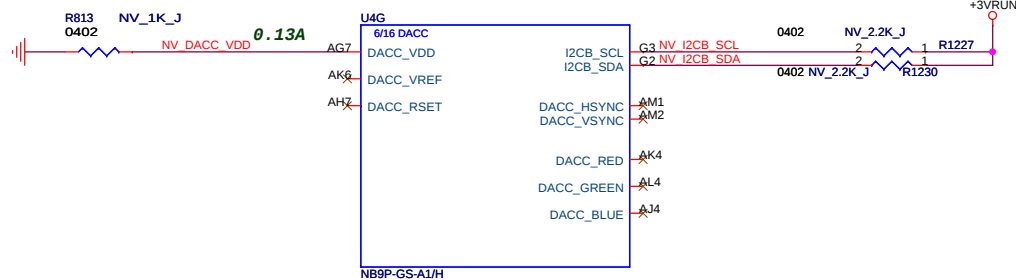
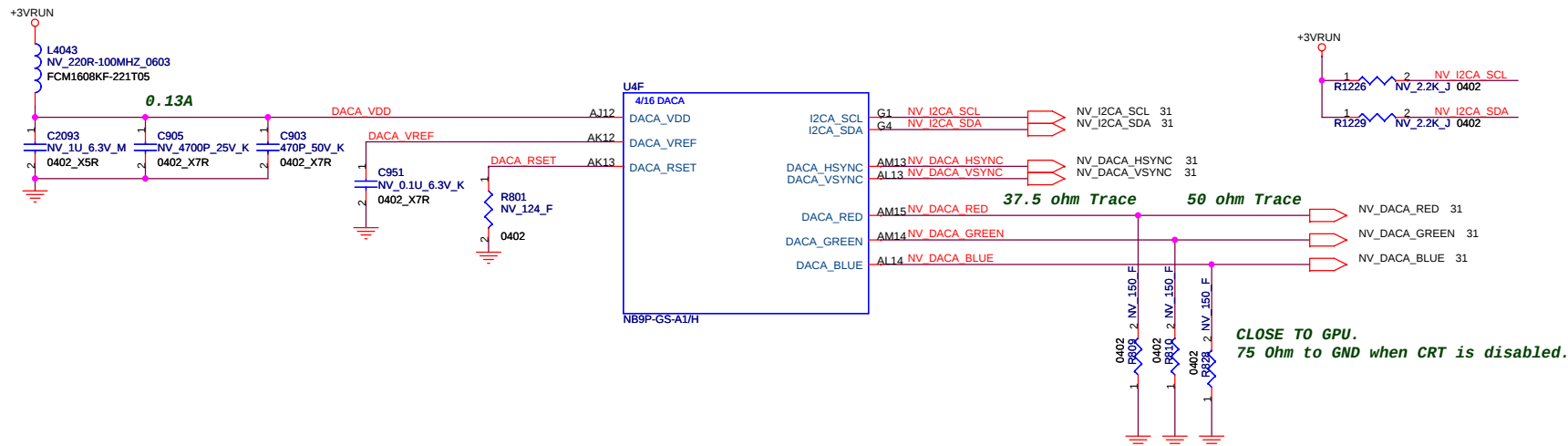
Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

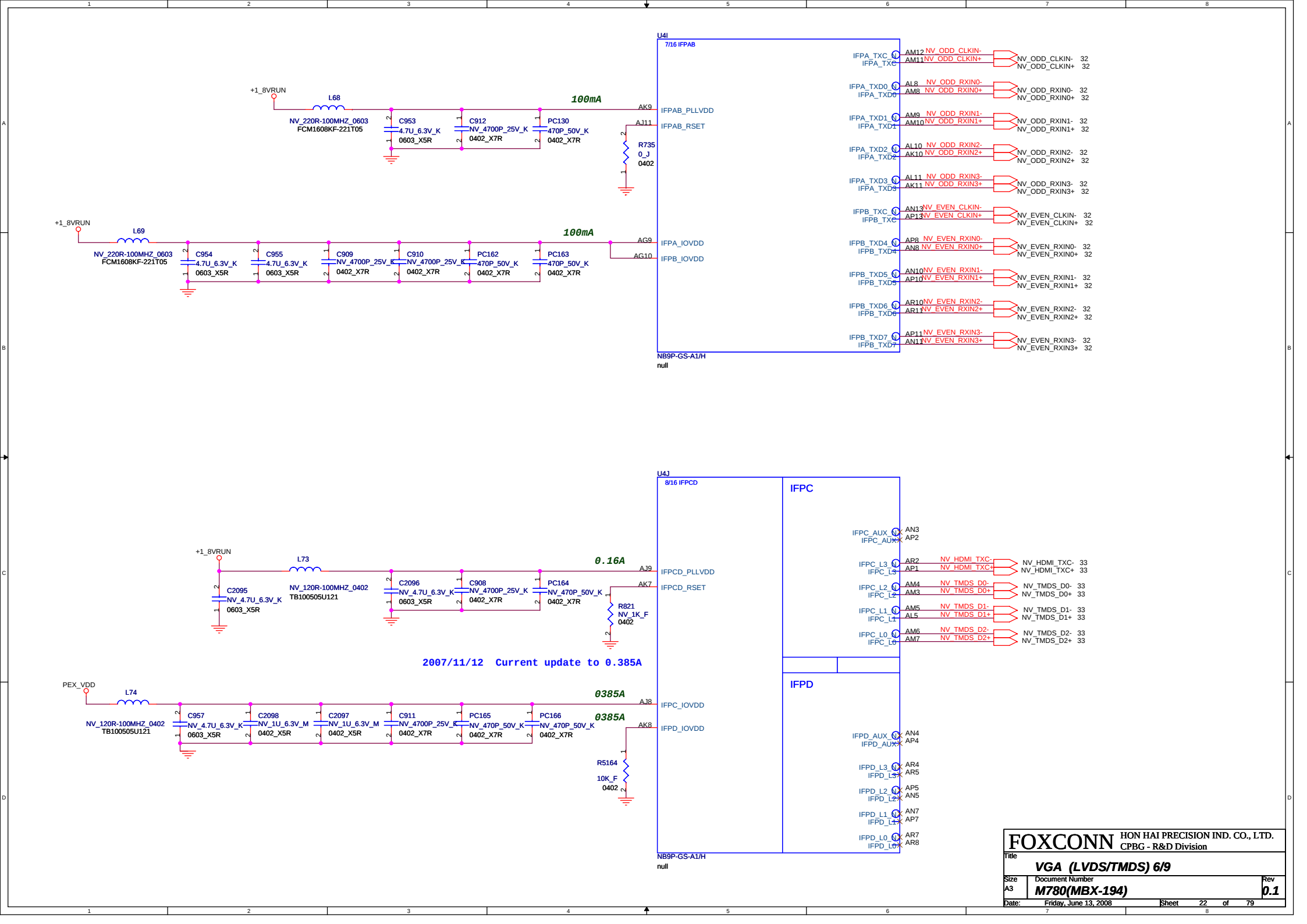
Refer to <GB1 Family Design Guide DG-03276-001 v01_secured>

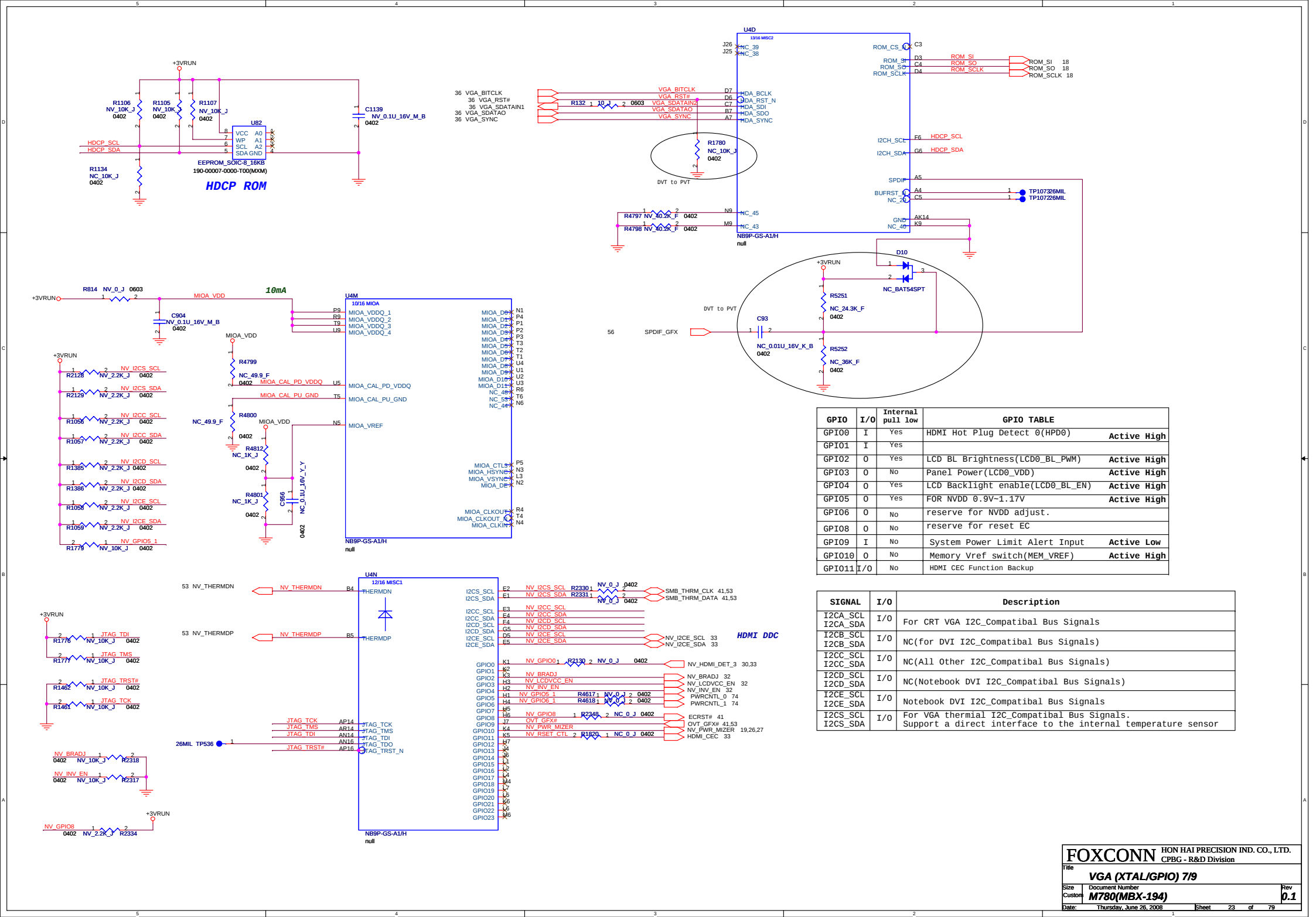






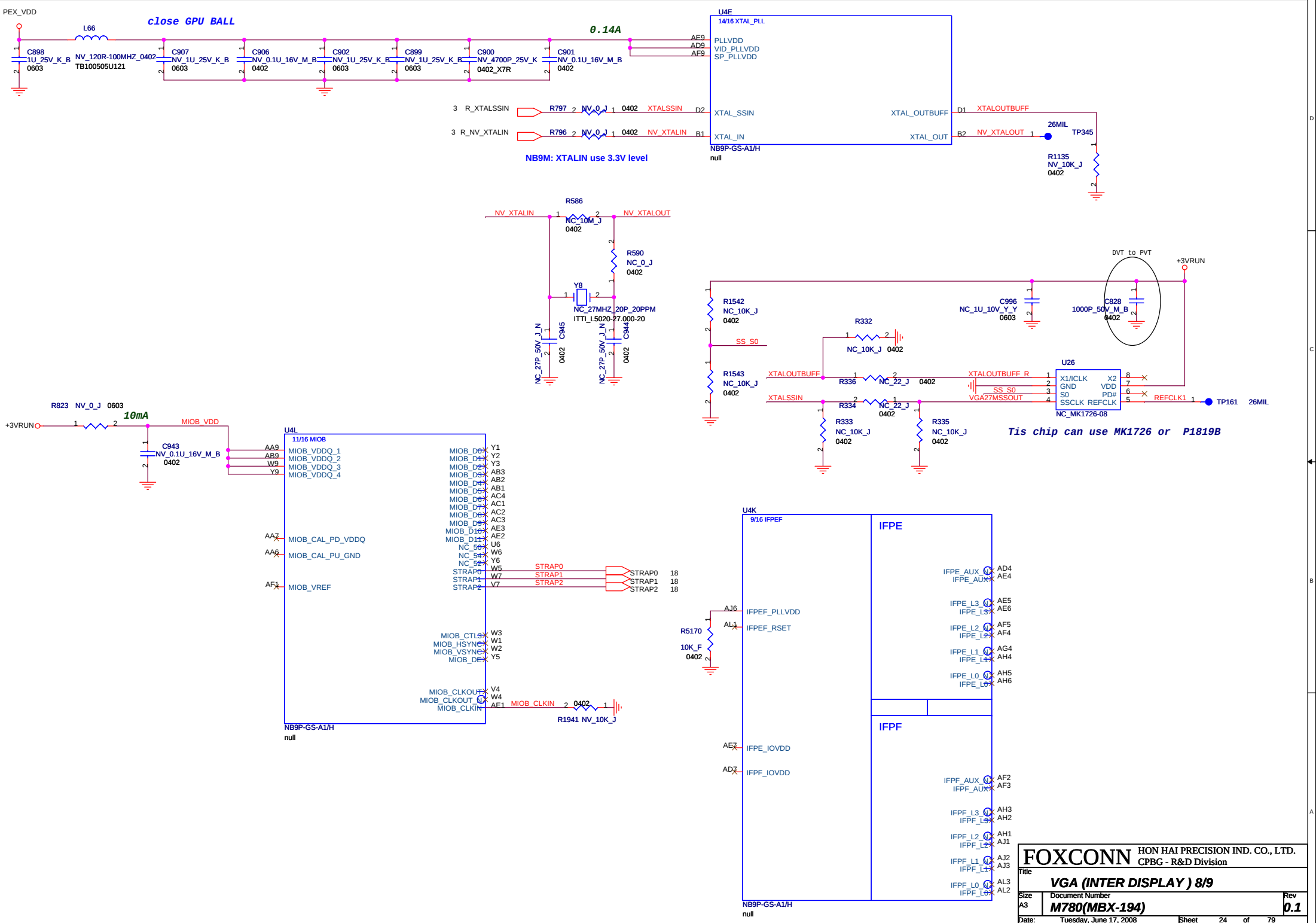
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DCLK	SCC
	VGA-DDBDATA	SbA

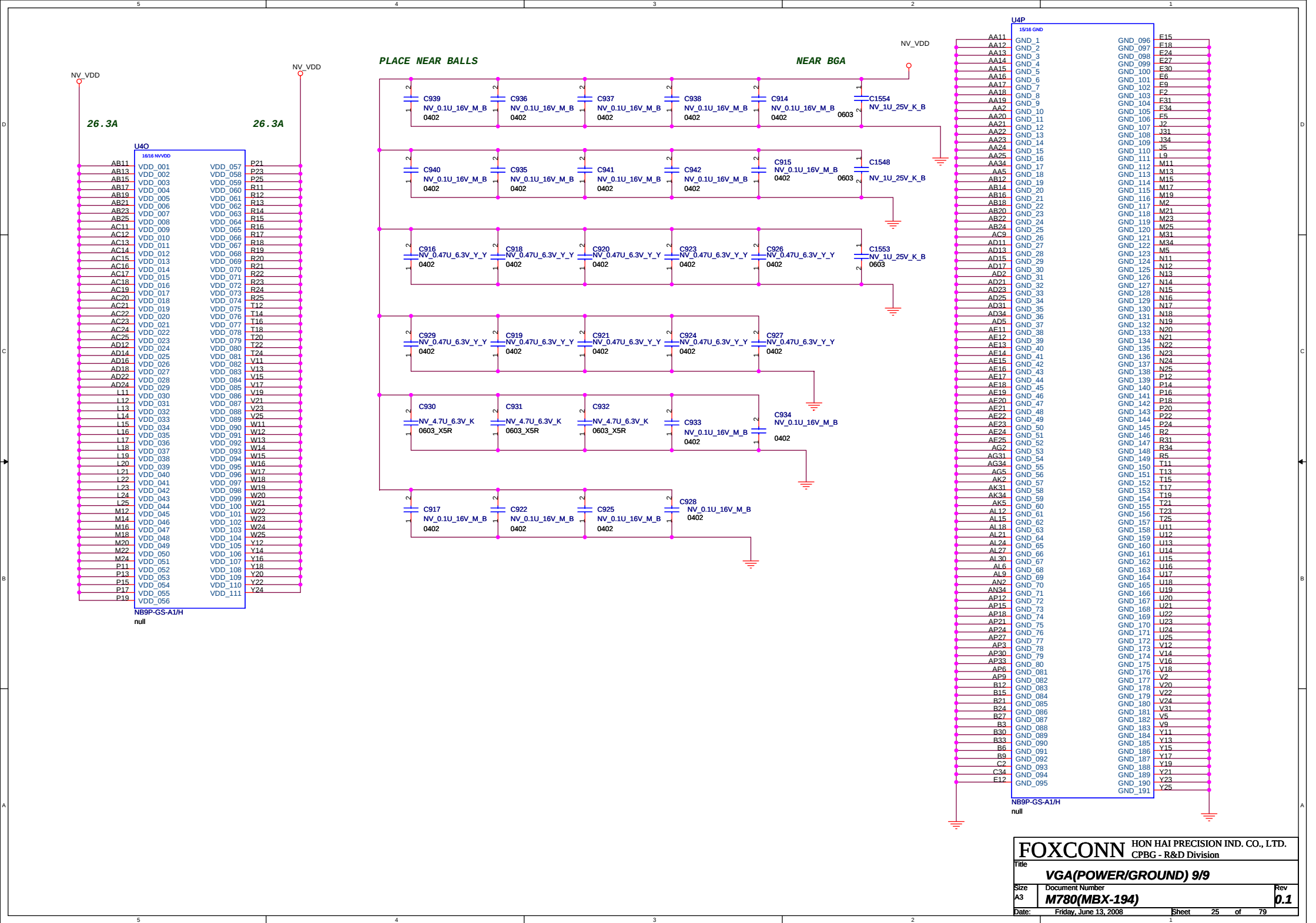


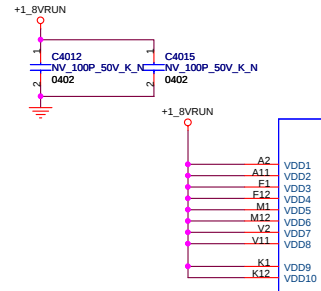


GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)	Active High
GPIO1	I	Yes		
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	FOR NVDD 0.9V-1.17V	Active High
GPIO6	O	No	reserve for NVDD adjust.	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low
GPIO10	O	No	Memory Vref switch(MEM_VREF)	Active High
GPIO11	I/O	No	HDMI CEC Function Backup	

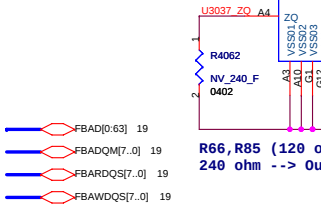
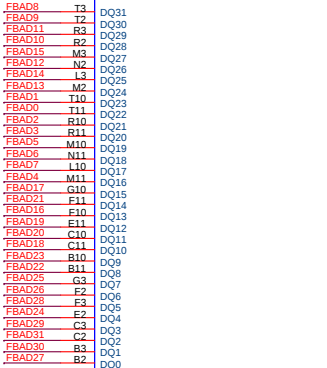
SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(All Other I2C_Compatibal Bus Signals)
I2CD_SCL I2CD_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CE_SCL I2CE_SDA	I/O	Notebook DVI I2C_Compatibal Bus Signals
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor





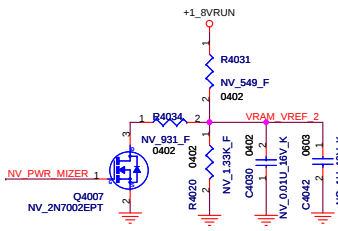
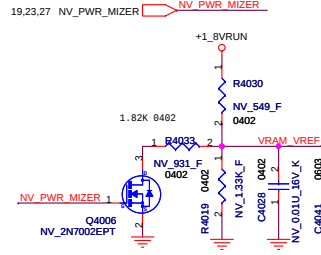


MIRROR TABLE		
MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H1	H10	A1
K3	K8	A2
M4	M9	A3
K9	K4	A4
H11	H1	A5
K10	K3	A6
L9	L4	A7
K11	K6	A8
M9	M4	A9
K2	K11	A10
CL4	L9	A11
G9	G4	BA0
G9	G4	BA1
H10	H3	BA2

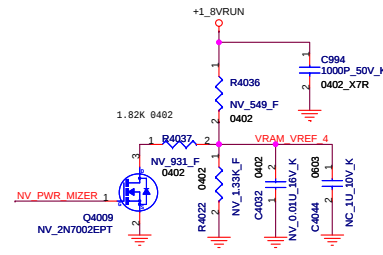
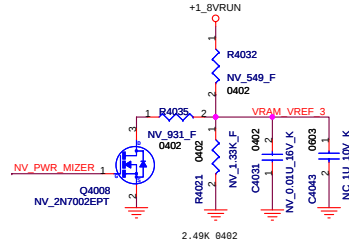
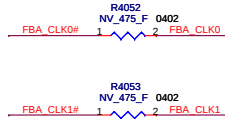


R66,R85 (120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

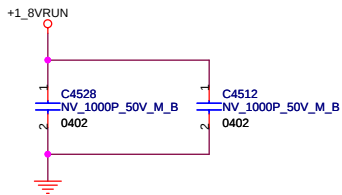
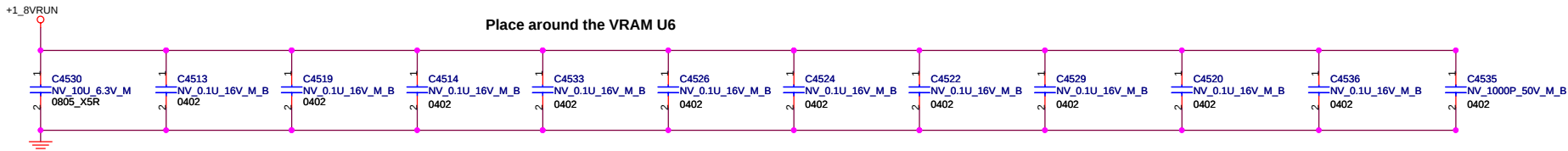
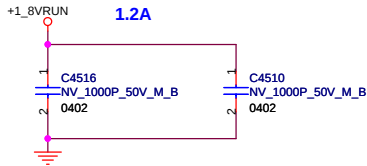
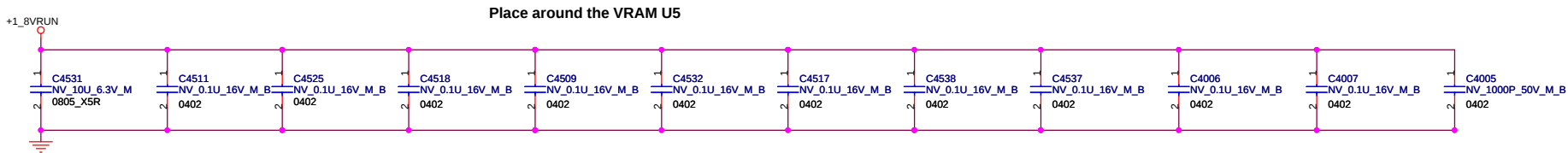


7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

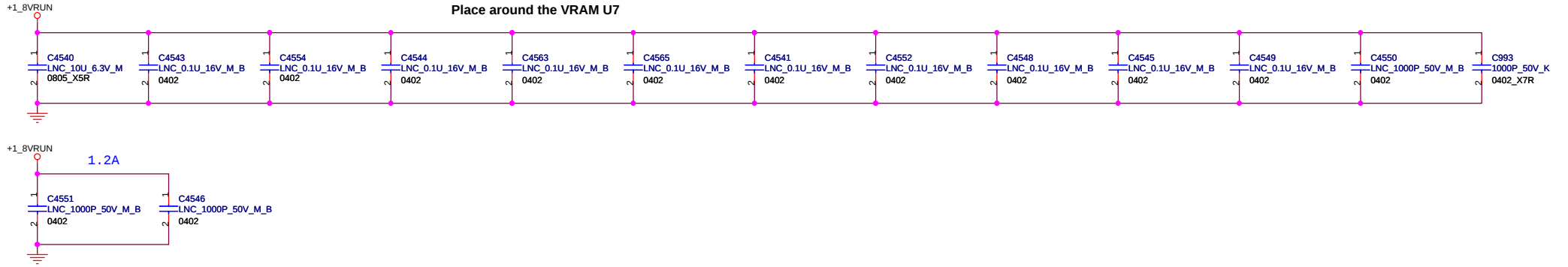


	0..30	32..63
CM00	A4	RAS#
CM01	RAS#	RAS#
CM02	A5	BA1
CM03	BA1	A2
CM04	A2	A4
CM05	A4	A3
CM06	A3	CS1#
CM07	CS1#	CS0#
CM08	CS0#	CS0#
CM09	A11	A11
CM10	CAS#	CAS#
CM11	WE#	WE#
CM12	BA0	BA0
CM13	A5	A5
CM14	A12	A12
CM15	RST7/00T	RST7/00T
CM16	A7	A7
CM17	A10	A10
CM18	CKE	CKE
CM19	A0	A0
CM20	A9	A9
CM21	A6	A6
CM22	A2	A2
CM23	A8	A8
CM24	A3	A3
CM25	A1	A1
CM26	A13	A13
CM27	BA2	BA2
CM28	RFU8	RFU8
CM29	RFU1	RFU1
CM30	RFU2	RFU2

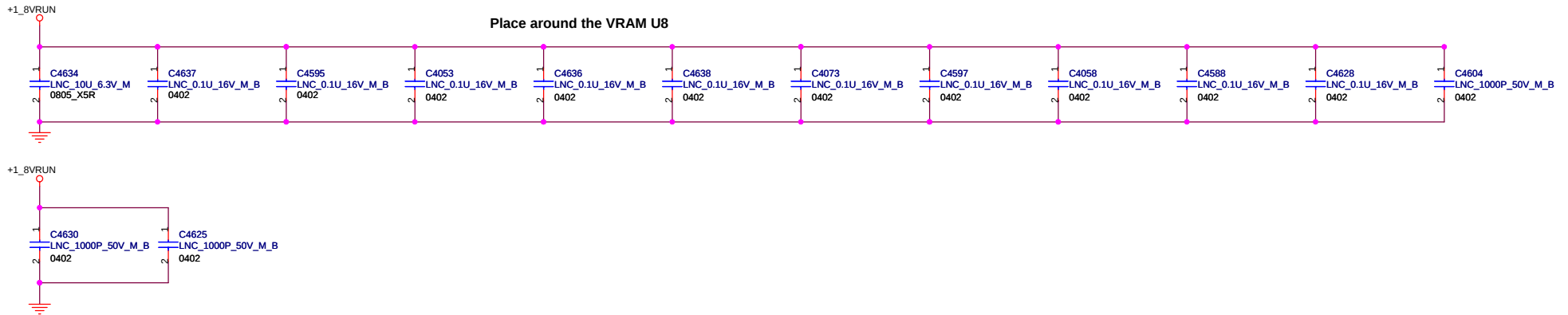
VREF	
H	50%
L	70%



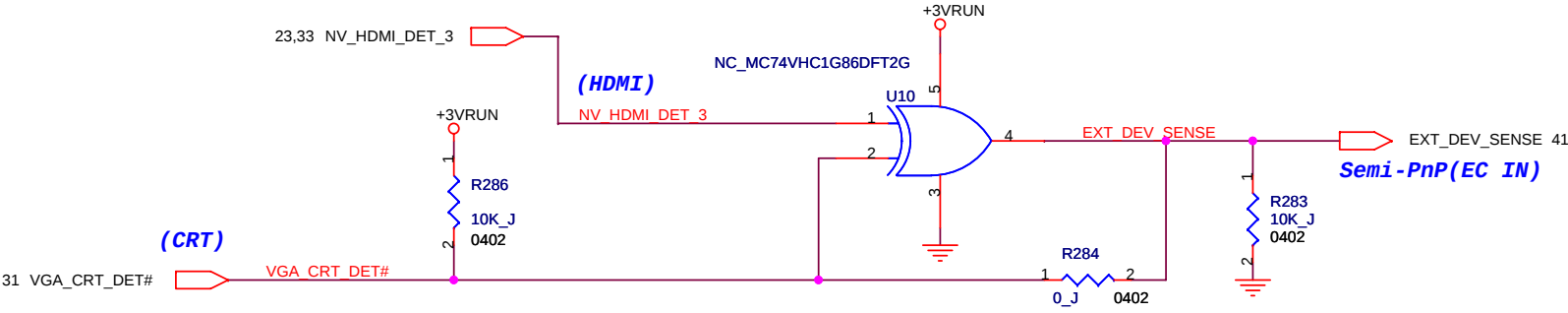
Place around the VRAM U7



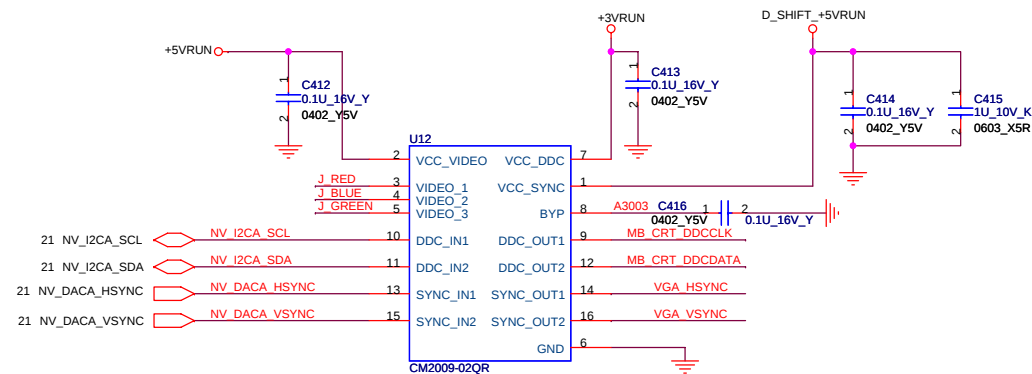
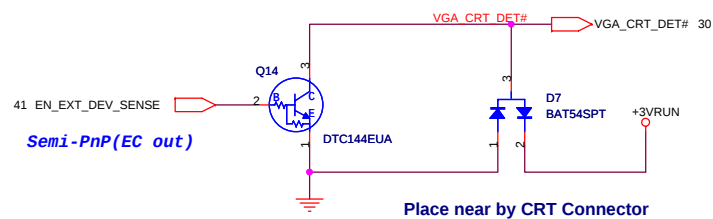
Place around the VRAM U8



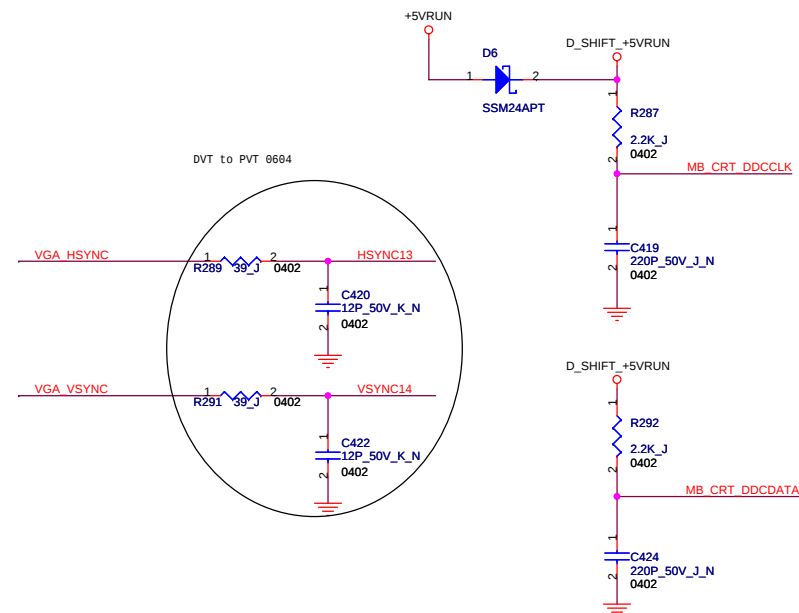
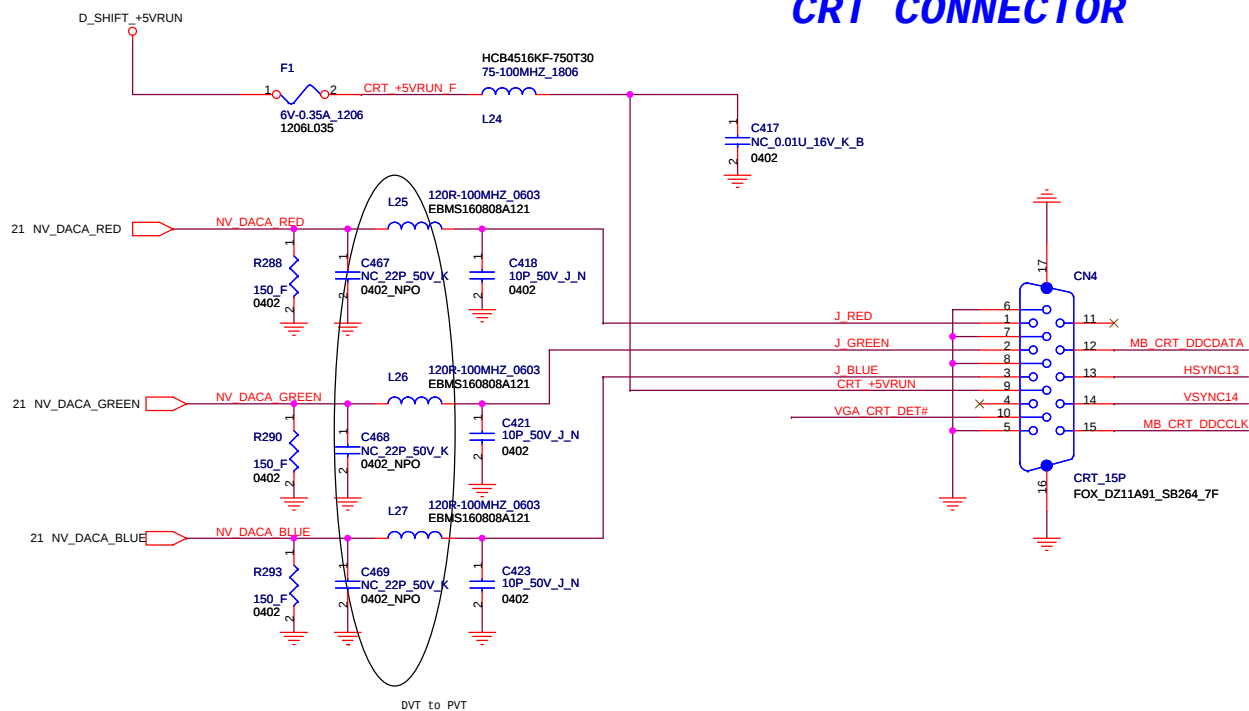
Semi-PnP Circuit



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		CPBG - R&D Division	
Title			
Semi-PnP			
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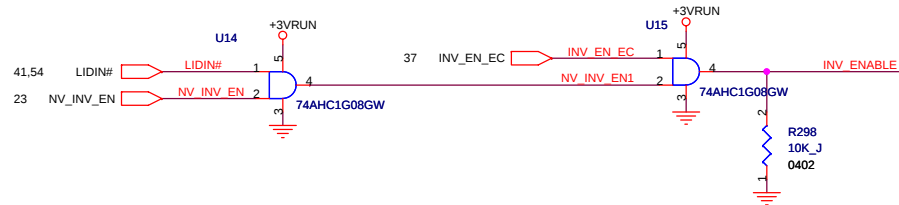
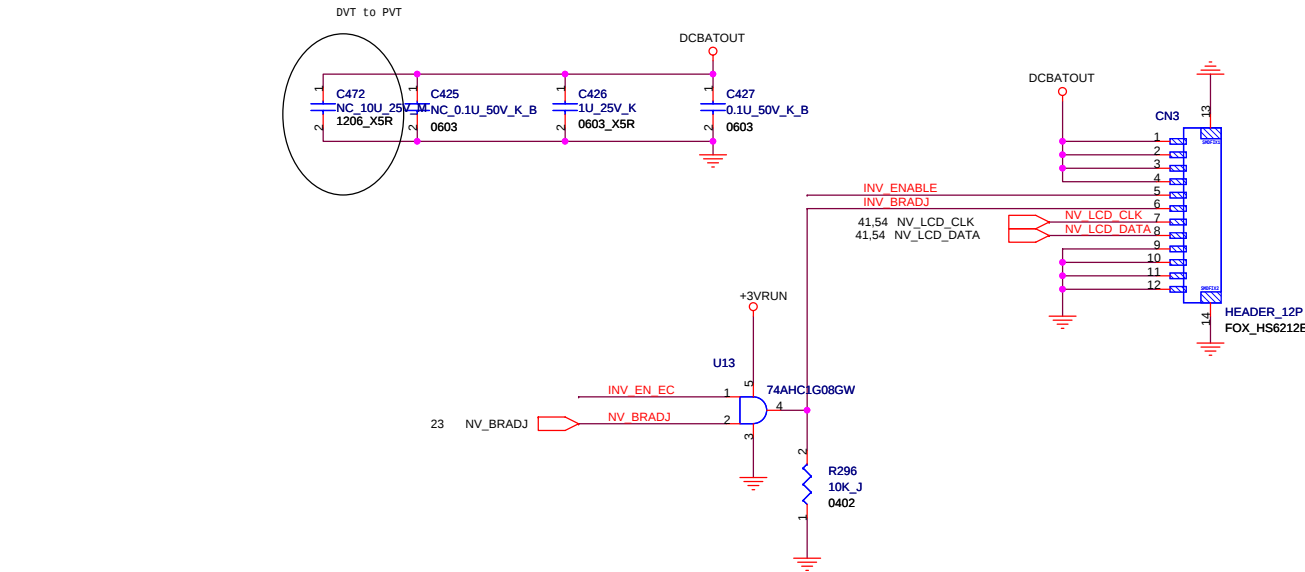


CRT CONNECTOR

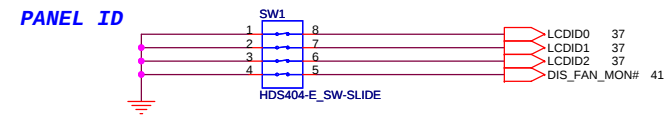
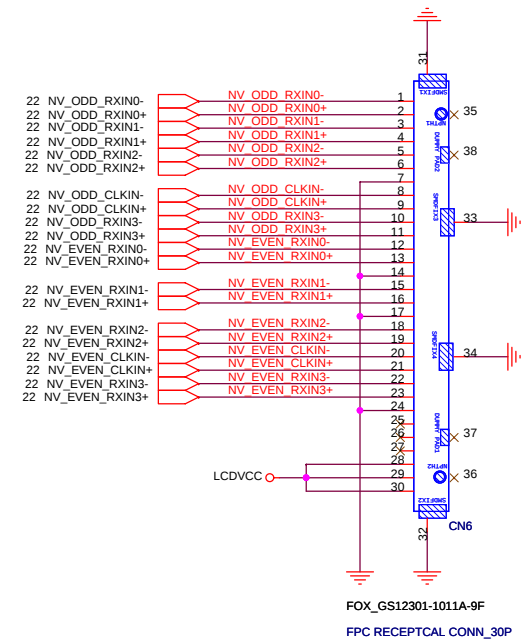
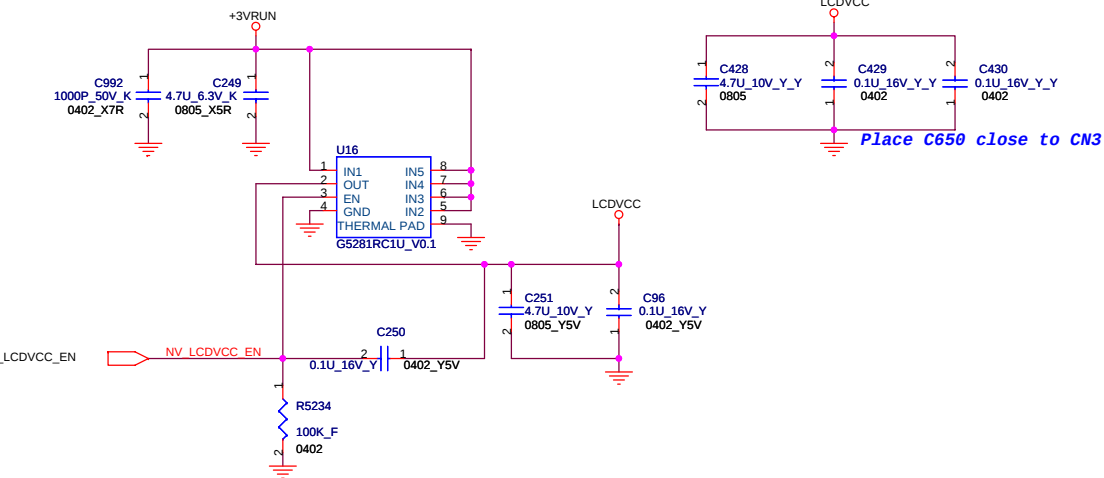


BLU CONNECTOR

LVDS CONNECTOR

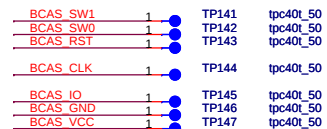
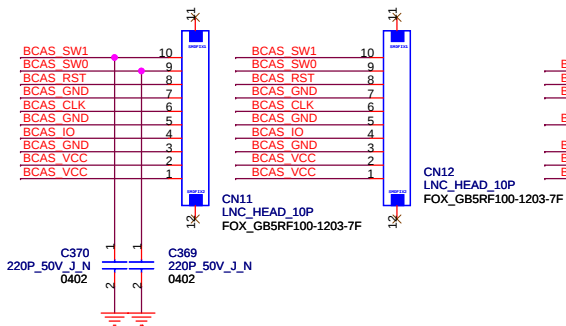
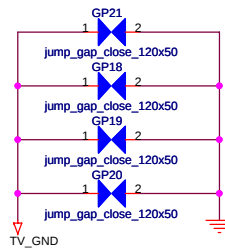
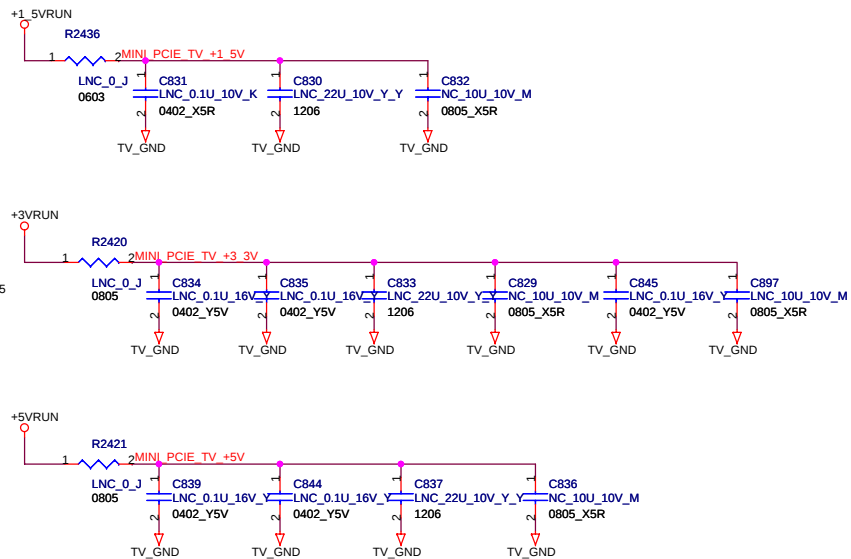
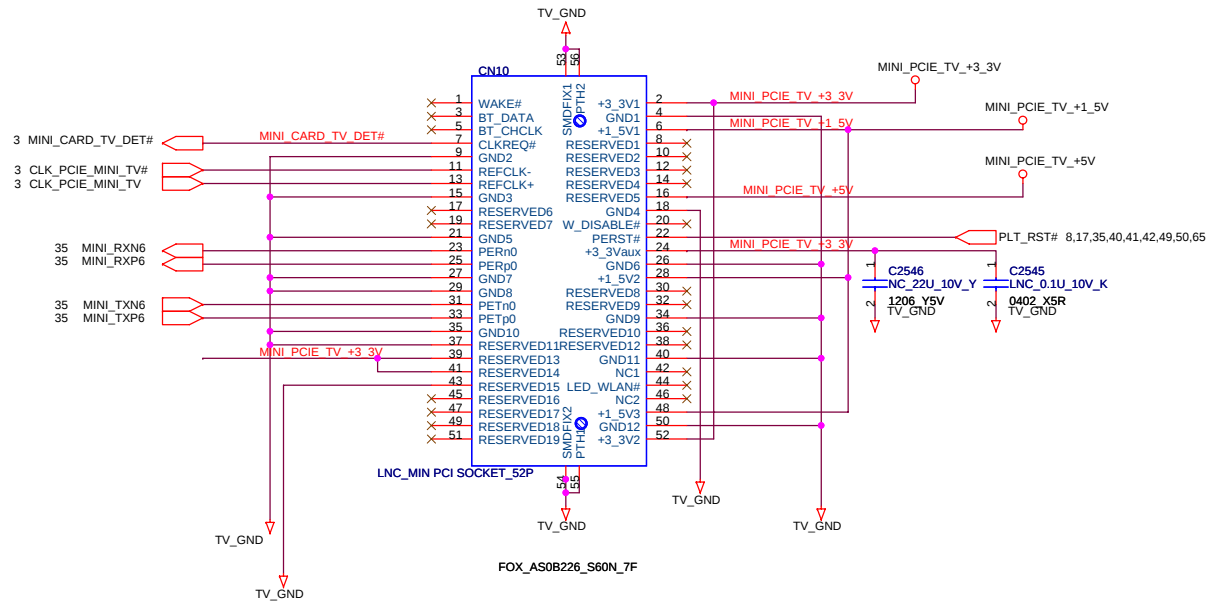


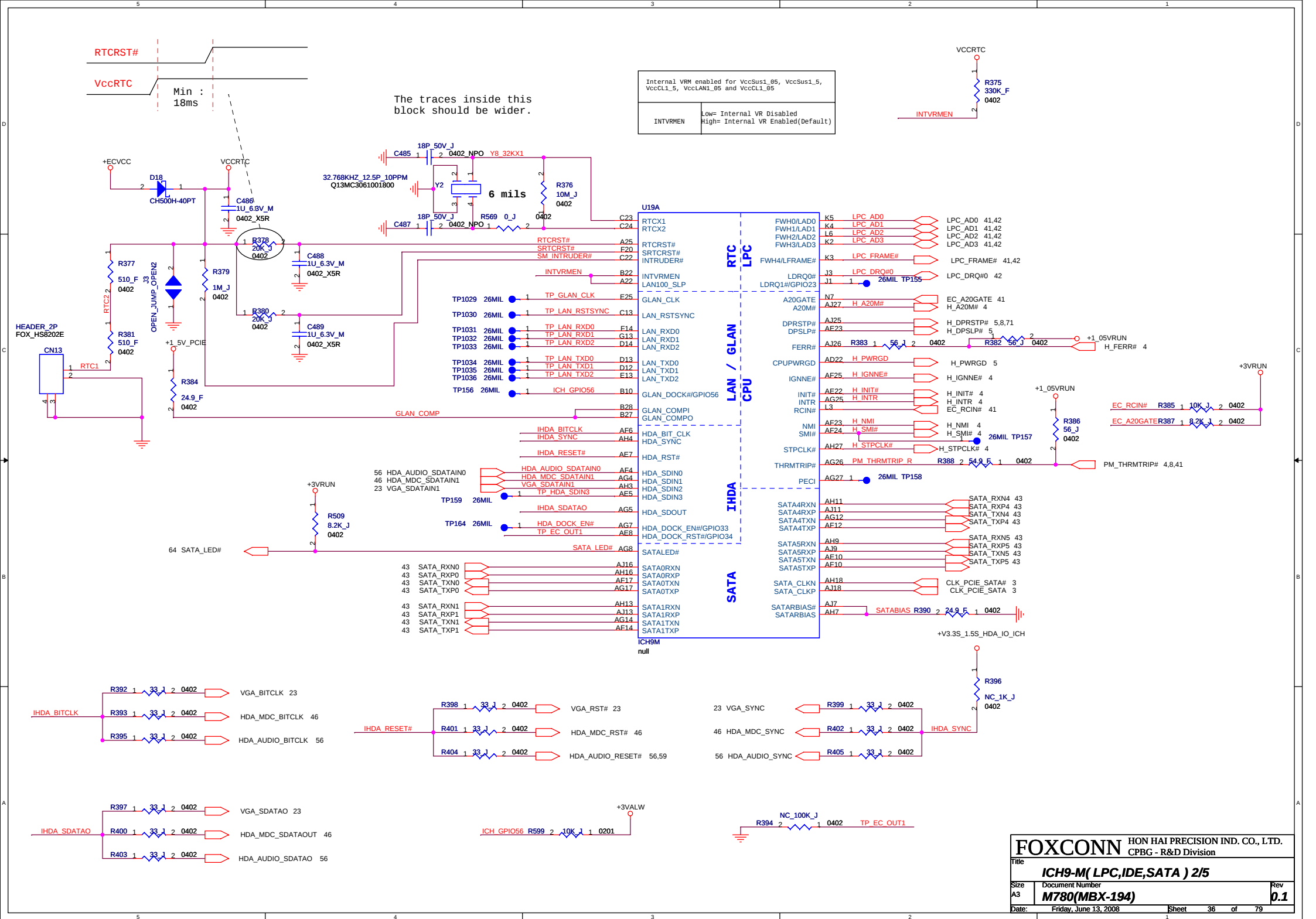
Current limit is from 1.1A to 2.1A.

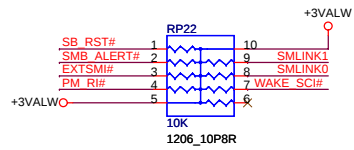


	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
Eagle1	1	0	0	1
Eagle2	1	0	1	0
Eagle3	1	0	1	1
DISABLE FAN LOCK FUNCTION	1	X	X	X

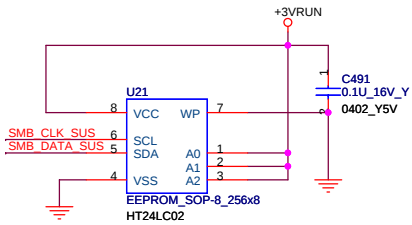
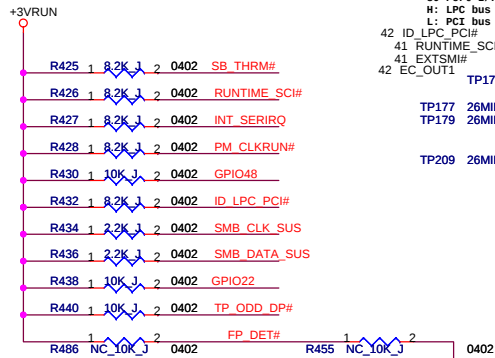
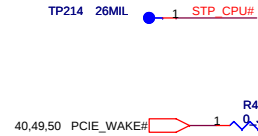
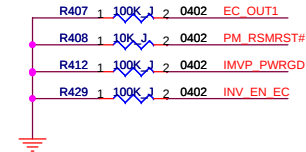
ON:0 , OFF:1



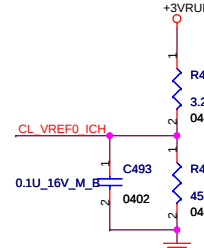
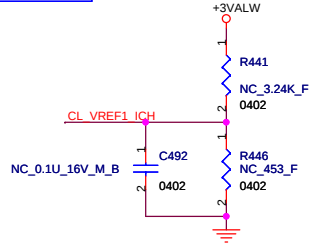
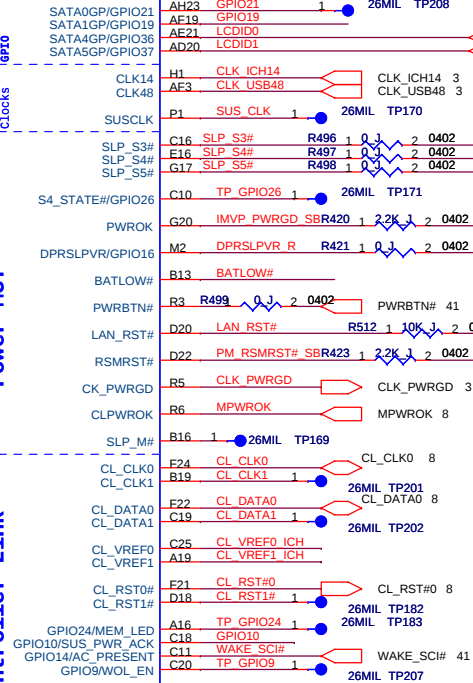
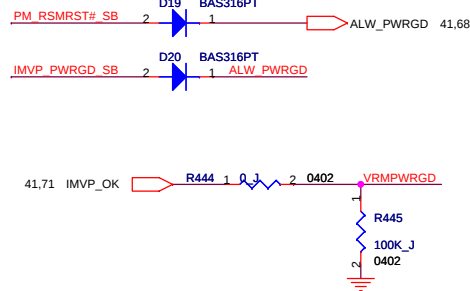
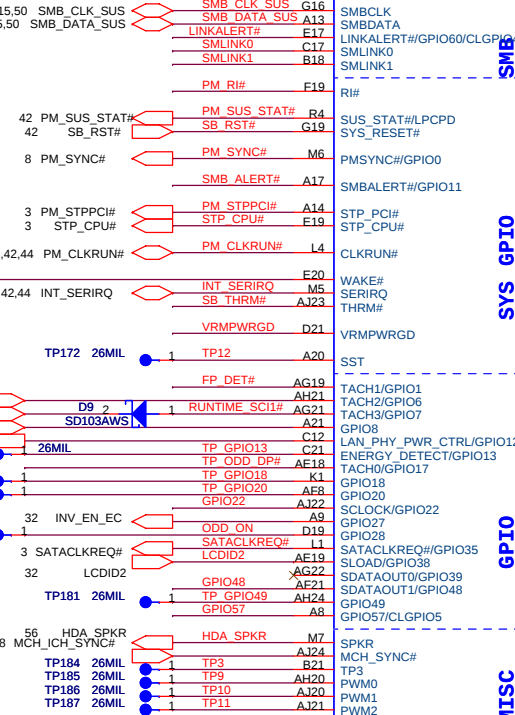




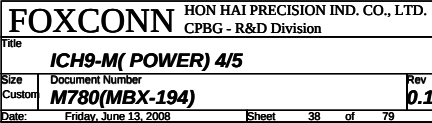
Stuff for No-reboot
Low=Default
High=No-reboot

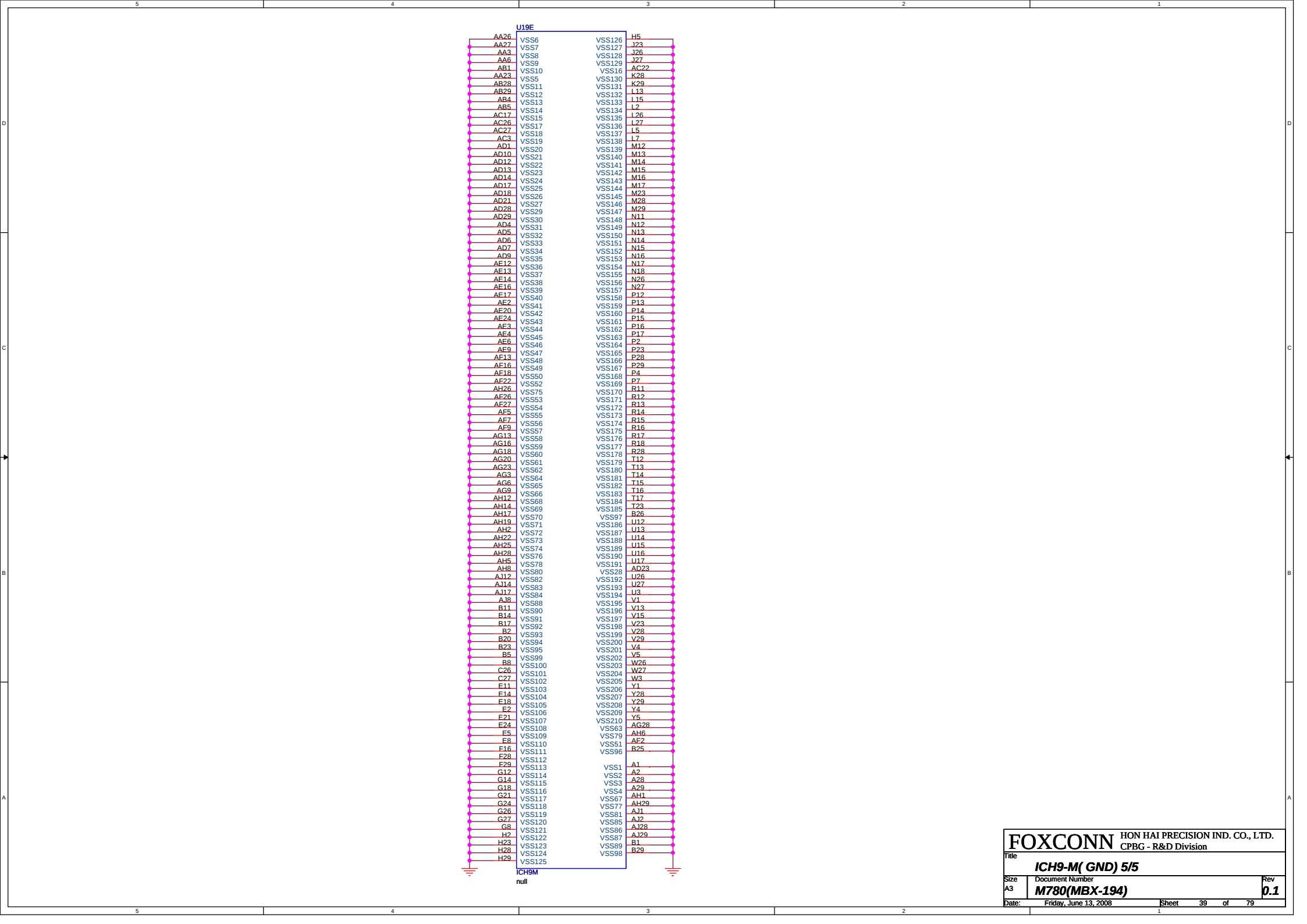


SMBus Address: AEH



Change to 0402





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ICH9-M(GND) 5/5

Size

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0.1

Date:

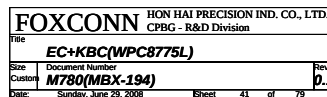
Friday, June 13, 2008

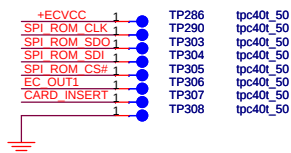
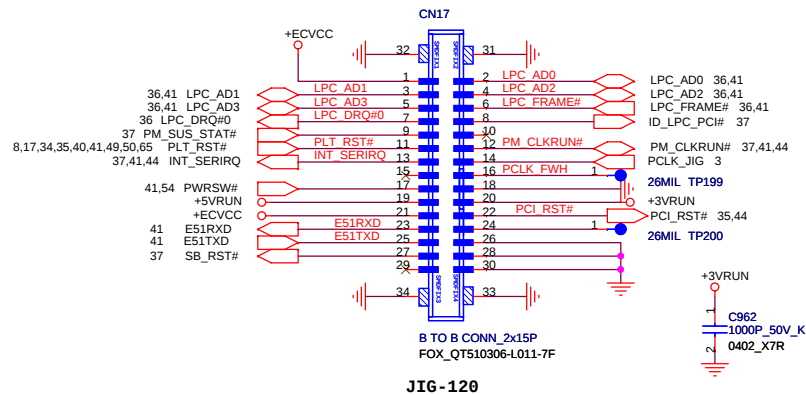
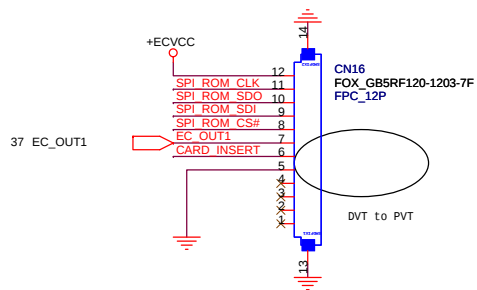
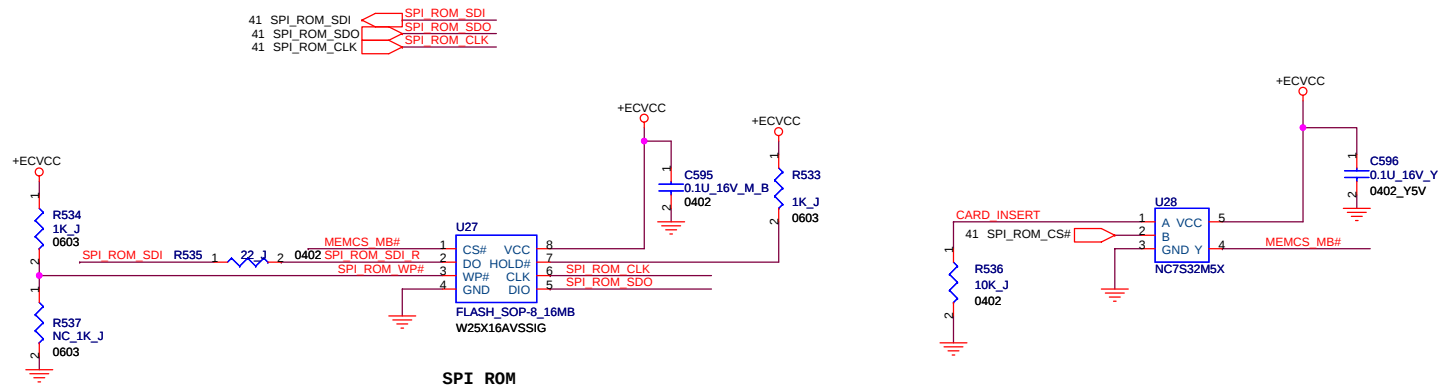
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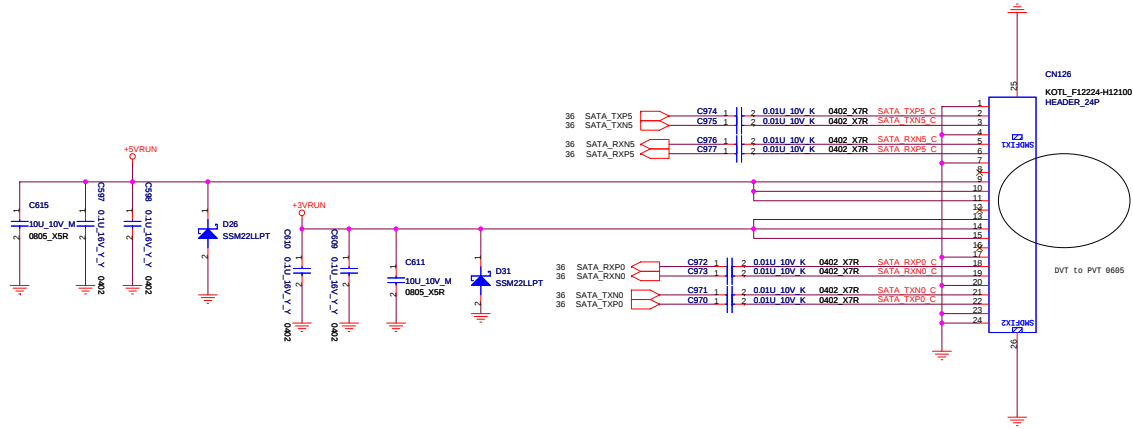
of

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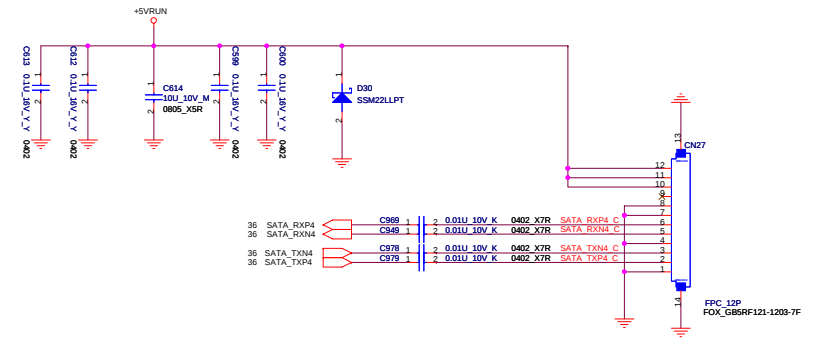


SATA HDD CONN(FPC)

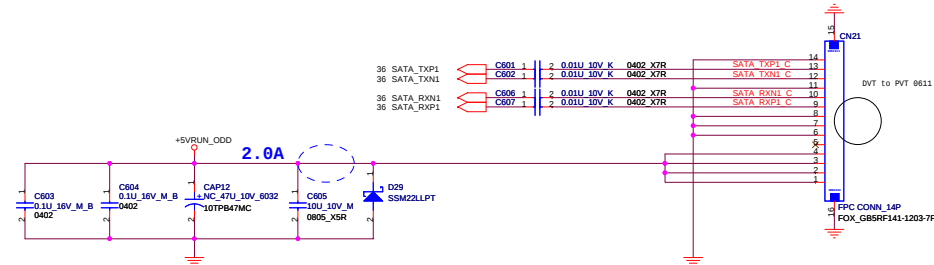


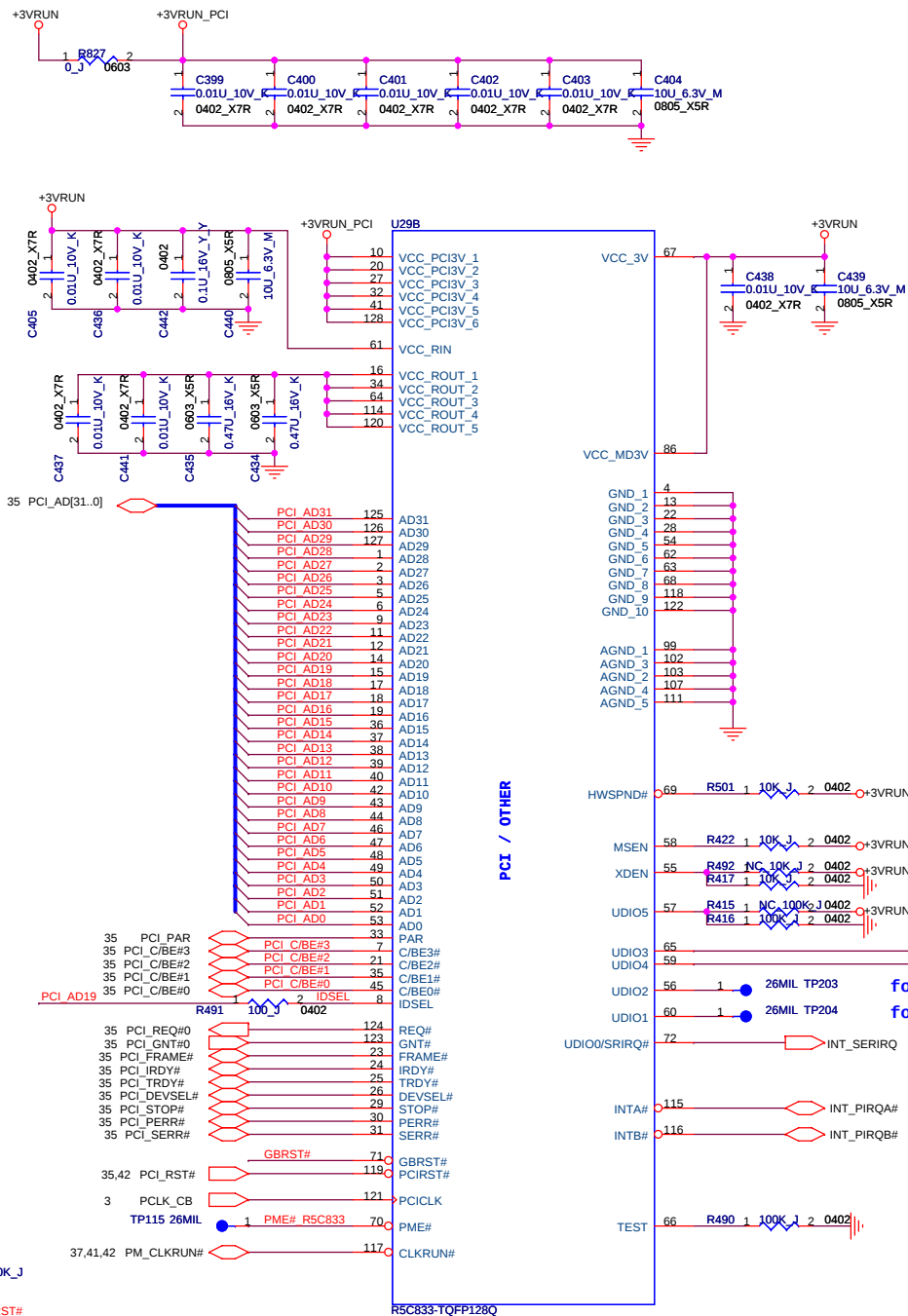
SATA0 : HDD or SSD (just connect to 24 Pin connector)
 SATA1 : ODD (fixed)
 SATA4 : HDD.(fixed for Single HDD connector)
 SATA5 : SSD.(just connect to 24 Pin connector)

SATA HDD CONN1(FPC)

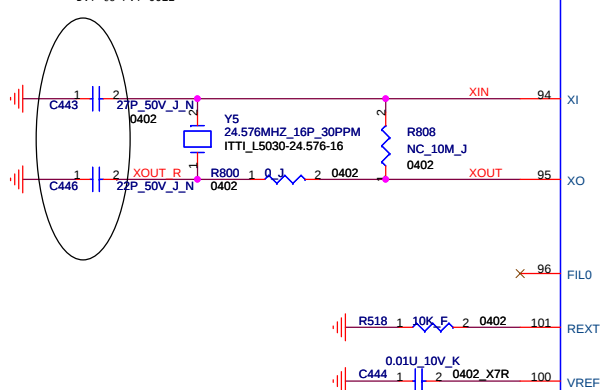


SATA ODD CONN(FPC)

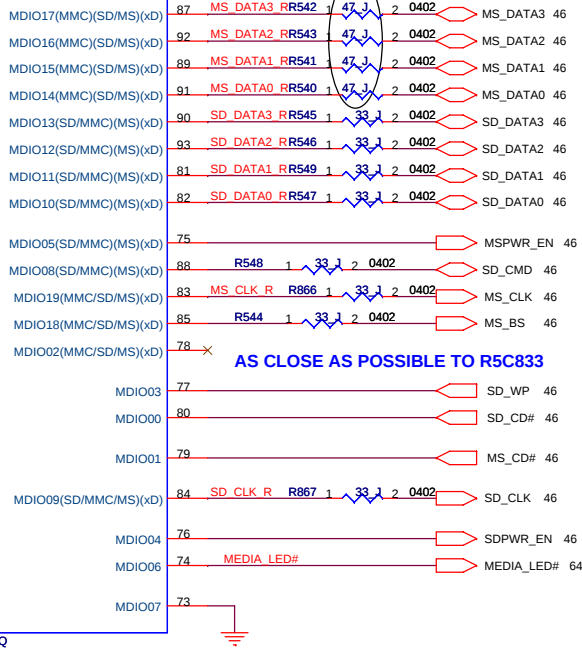




DVT to PVT 0612

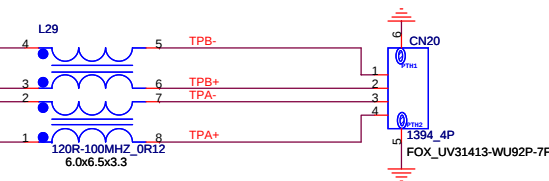


IEEE1394/SD



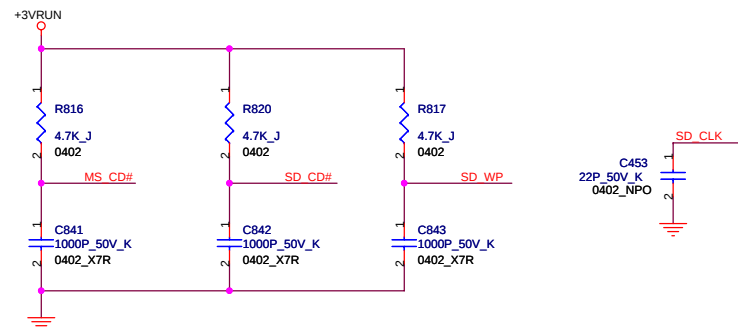
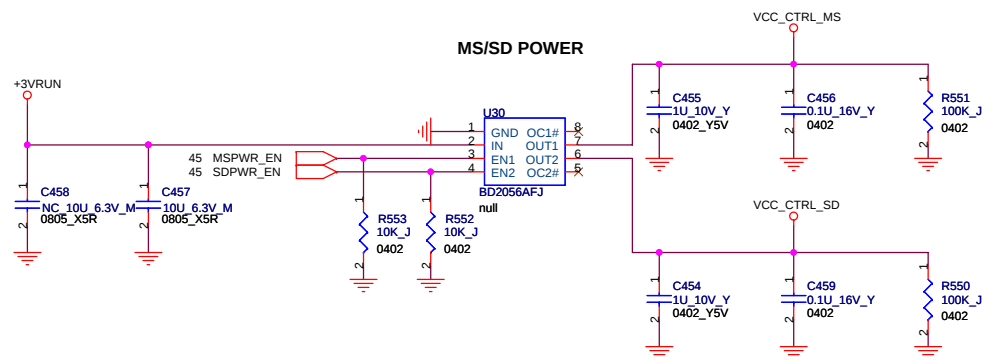
iLink CONN.

118. (Page 30) 07/11/12 Change L29 from 1L-FTR1DB6-5600 to 1L-F0D6560-TE00.

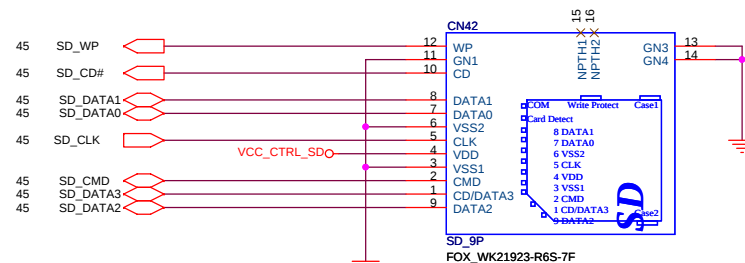


iLink CONN.

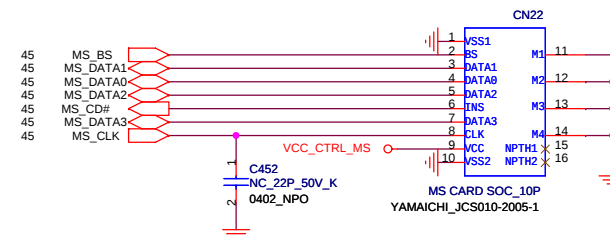
204. (Page 45) 07/11/27 change iLink CONN from FOX_UV31413-WR56P-7F to FOX_UV31413-WZ03P-7F.



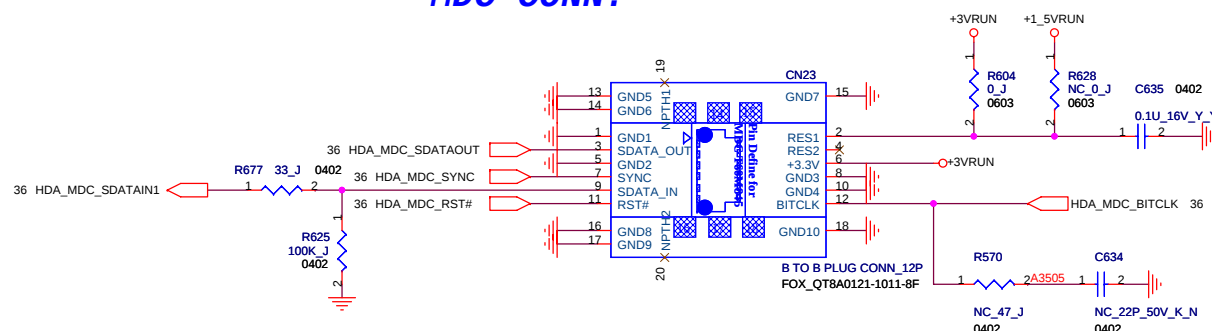
SD CONN.



MS STD/DUO CONN.



MDC CONN.



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Title
PCI (MS-DUO/MDC)

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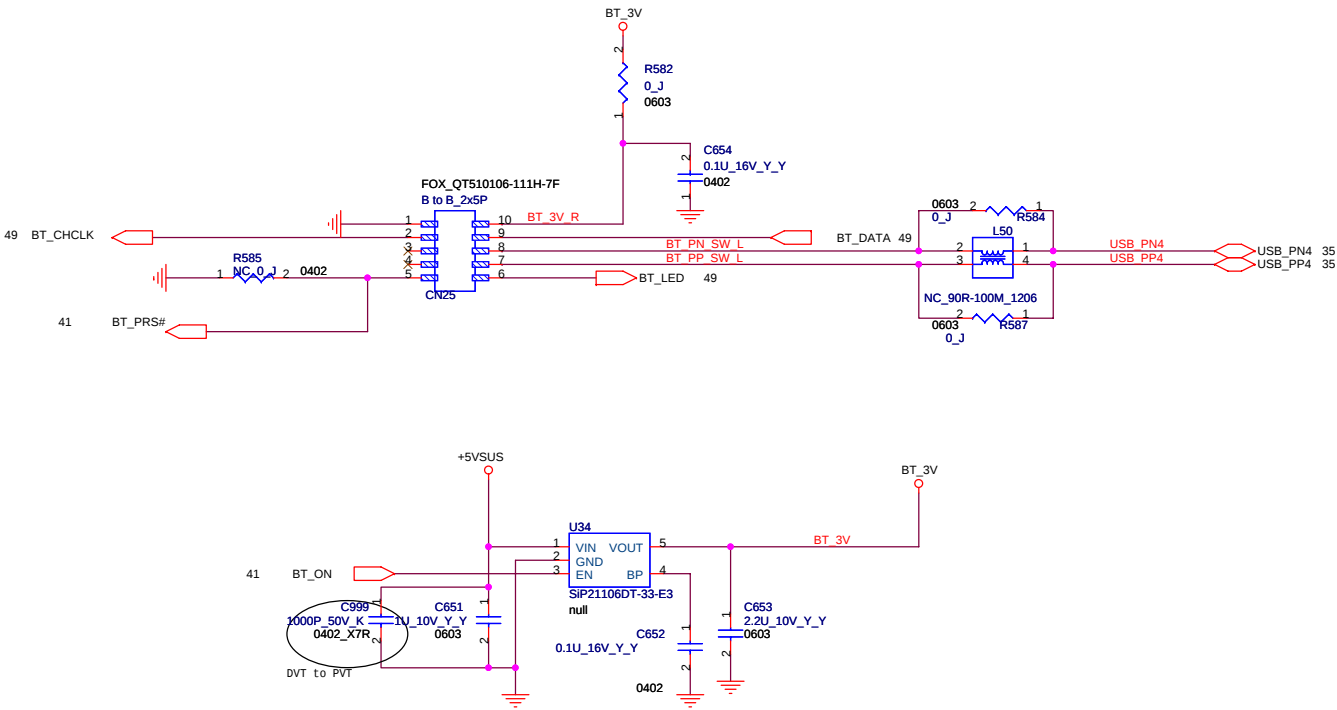
A3 **M780(MBX-194)**

Date: Friday, June 27, 2008

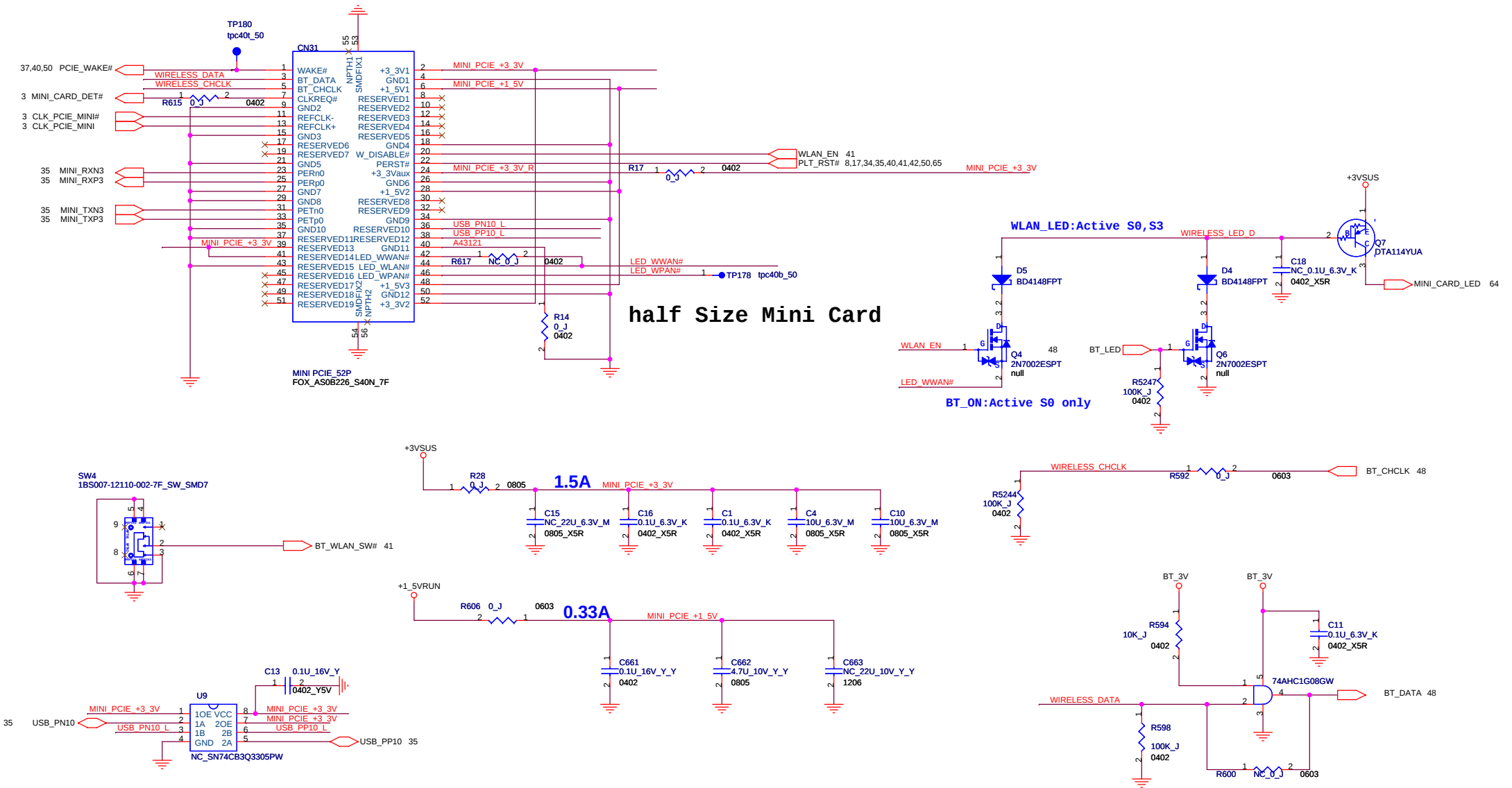
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Bluetooth connector



Mini-PCIE Card connector(WLA)

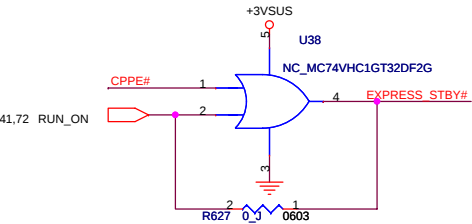
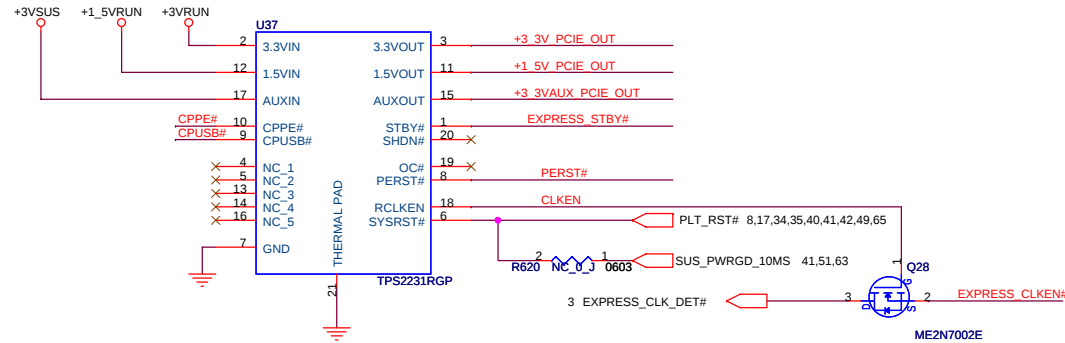


VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SRDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

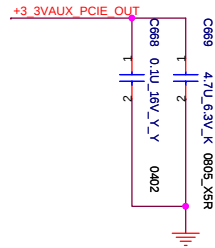
+1_5V=>0.65A

+3_3VAux=>0.275A

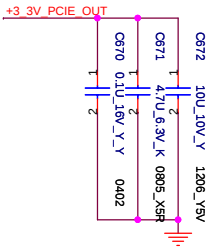
+3_3V=>1.3A



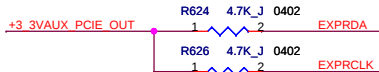
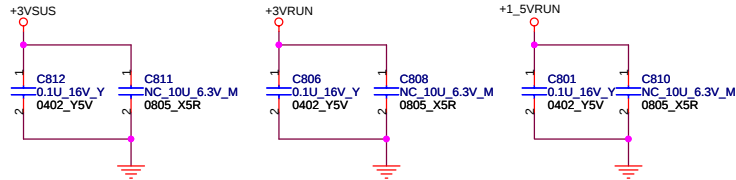
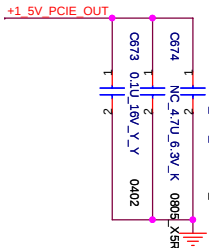
Supply Max 275mA



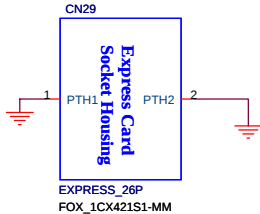
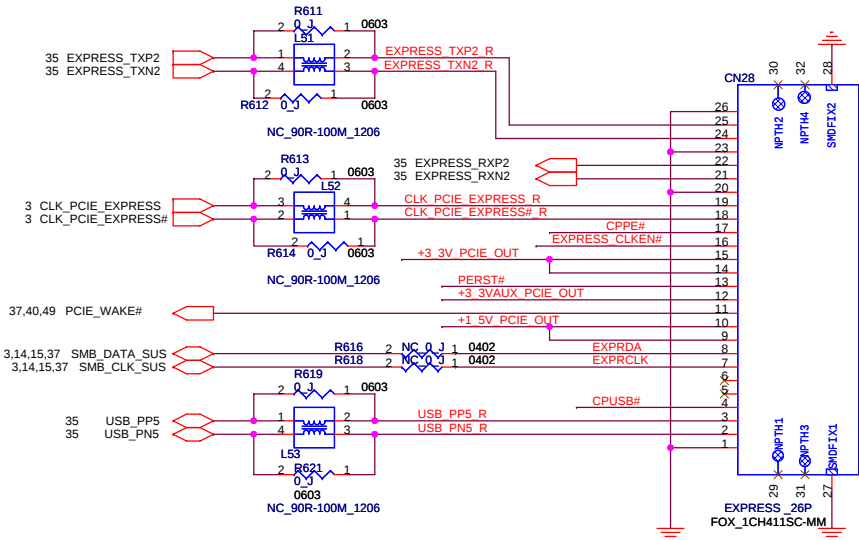
Supply Max 1300mA



Supply Max 650mA

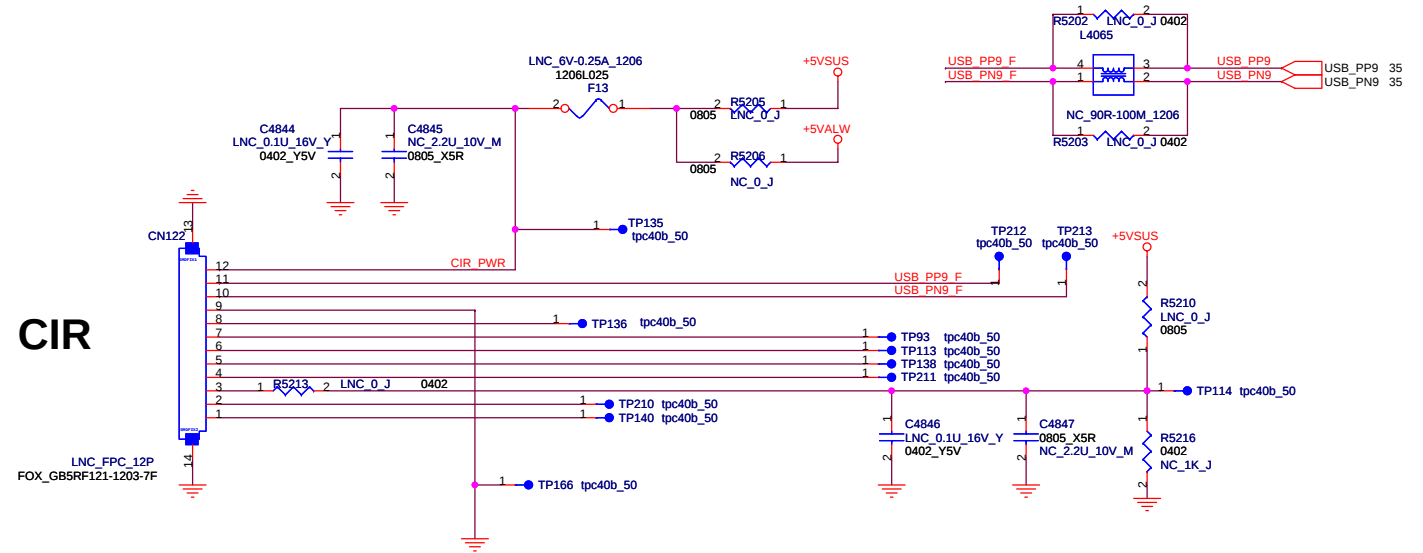


EXPRESS Card Slot

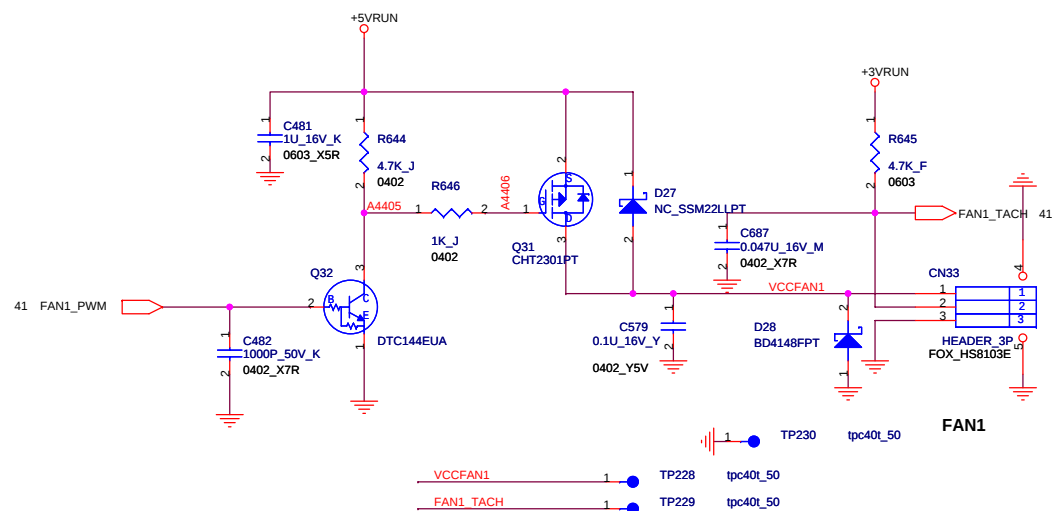


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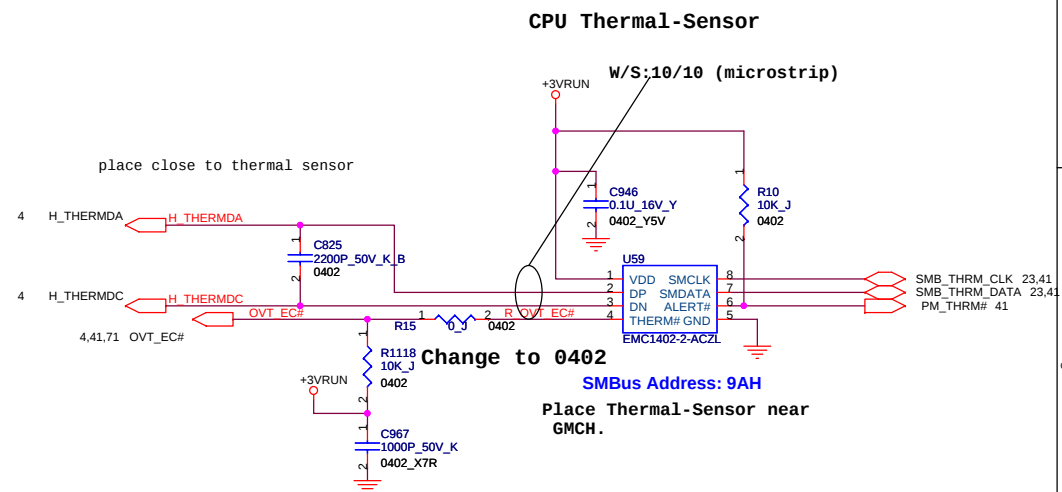
IR Rreceiver connector



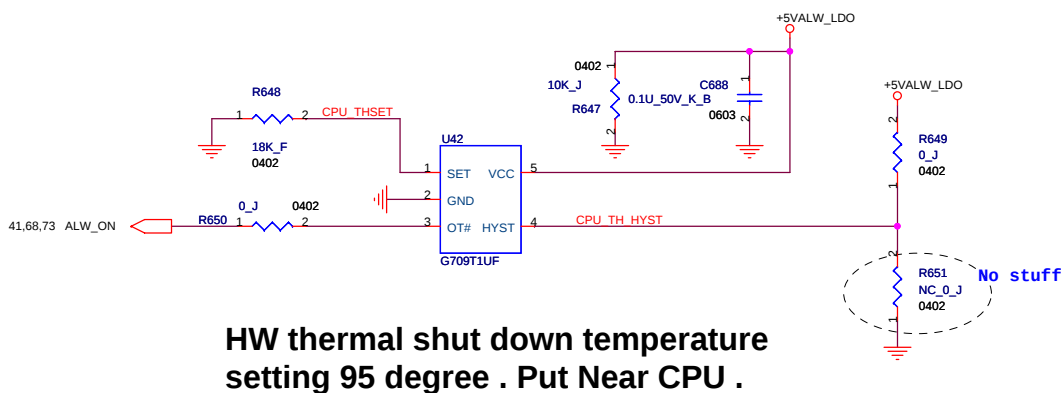
FAN circuit



CPU Thermal-Sensor

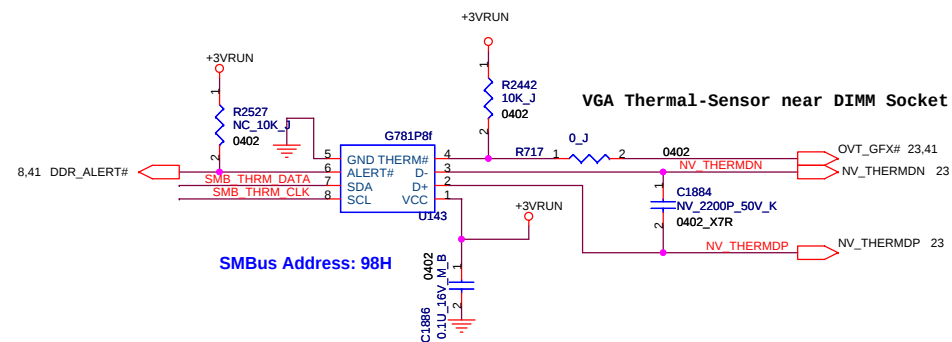


HW THERMAL PROTECTION

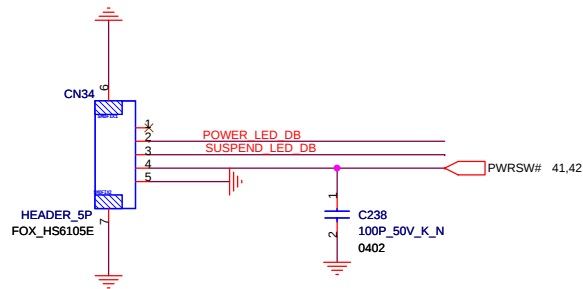


HW thermal shut down temperature setting 95 degree . Put Near CPU .

VGA Thermal-Sensor



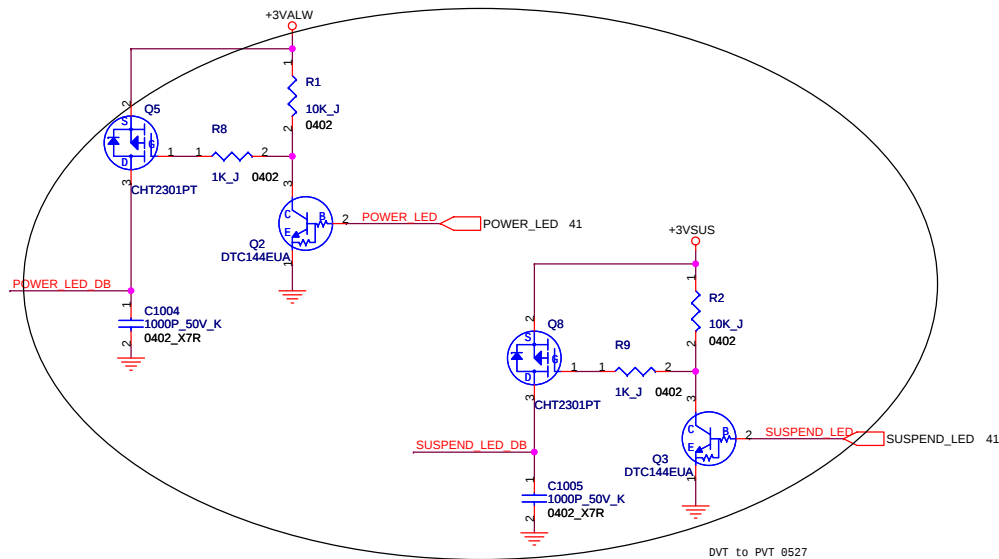
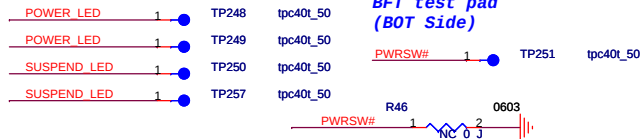
To Power Button Board Connector



BFT test pad (TOP Side)

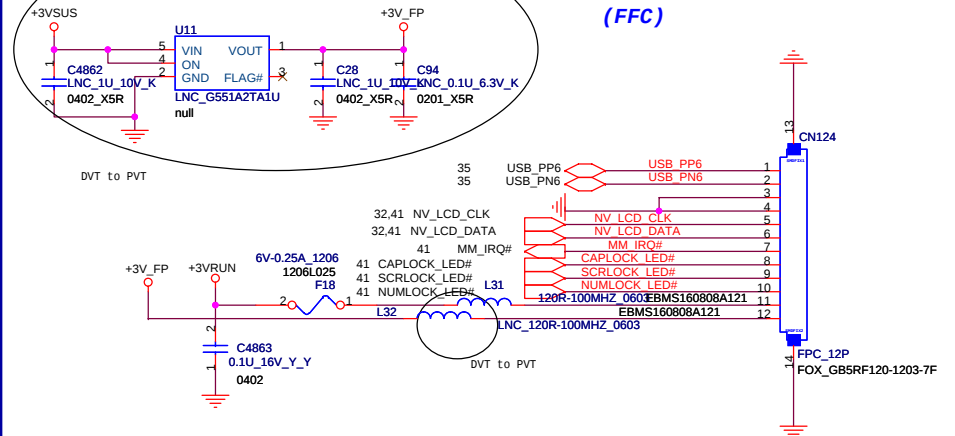


BFT test pad (BOT Side)

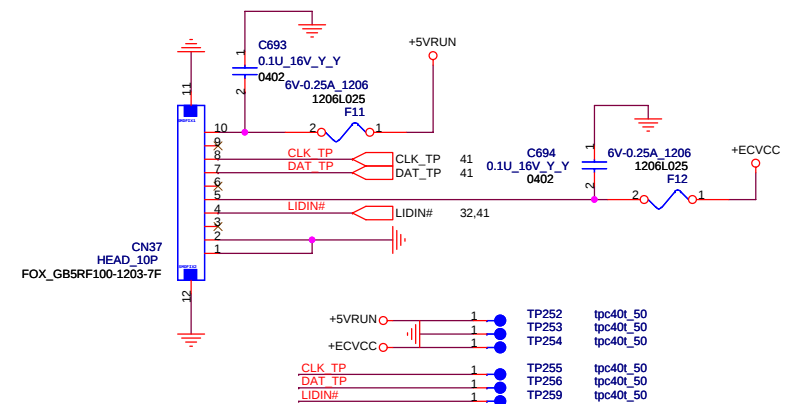


To TV Function Board Connector

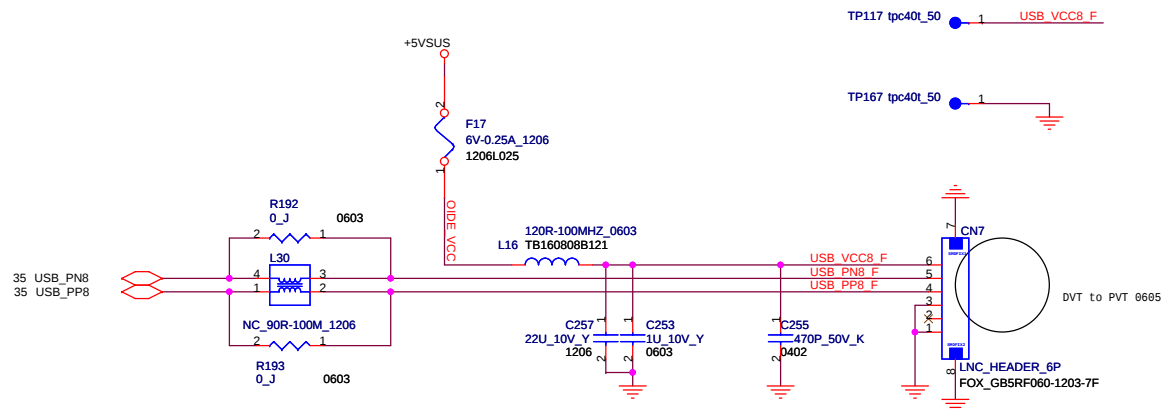
(FFC)



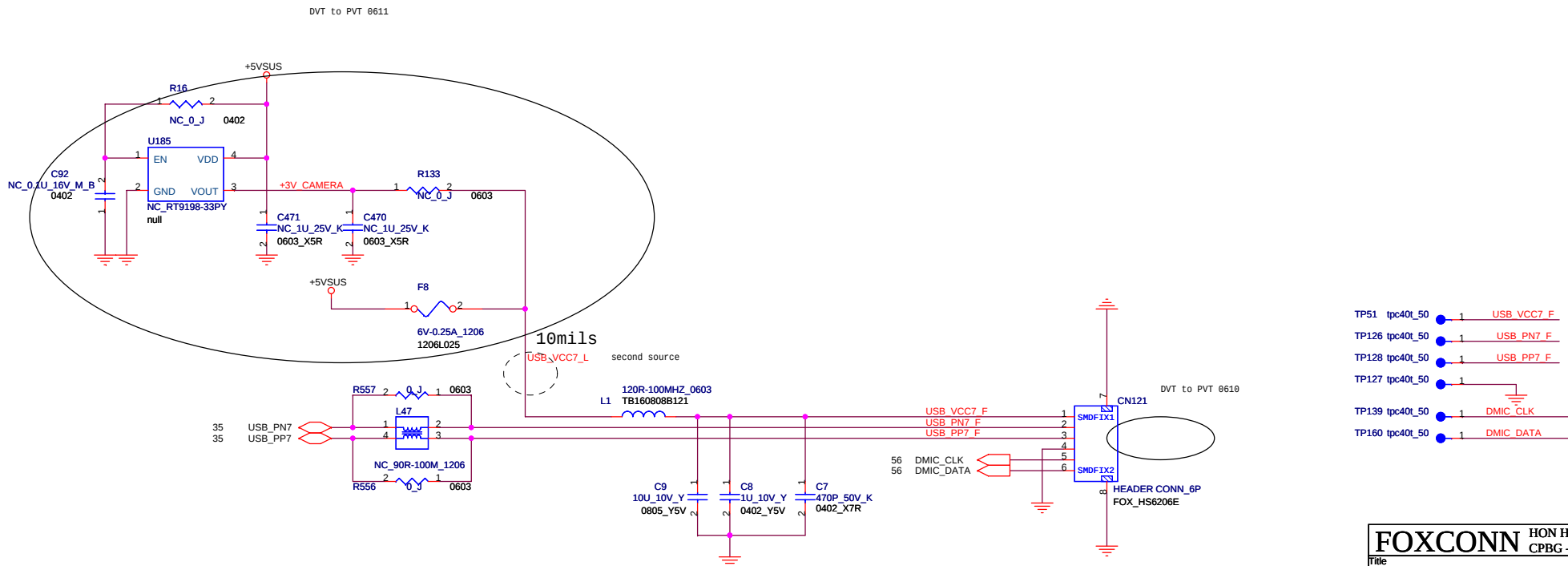
To Touch Pad Board Connector (FFC)



OIDE Connector

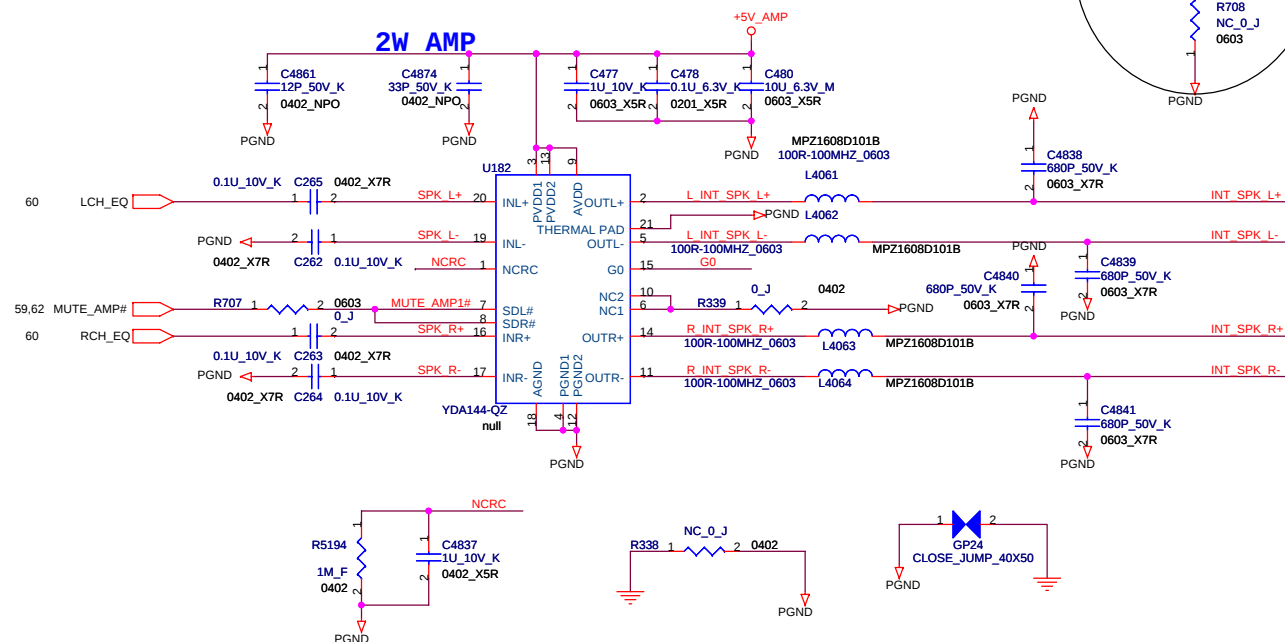


CAMERA +MIC CONN.



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OIDE/CAM			
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SPEAKER AMP

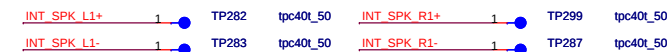


INTERNAL SPEAKER Connector

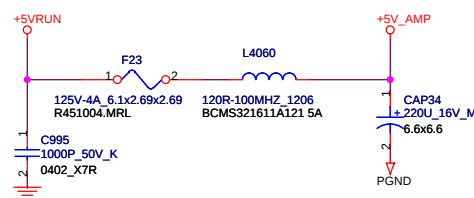


(20mil)

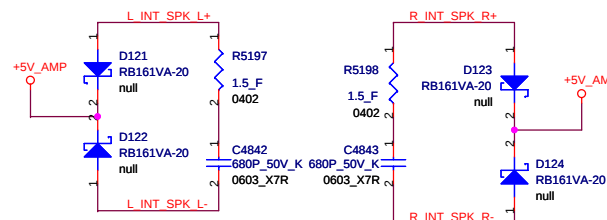
BFT Test Pad



SPEAKER POWER

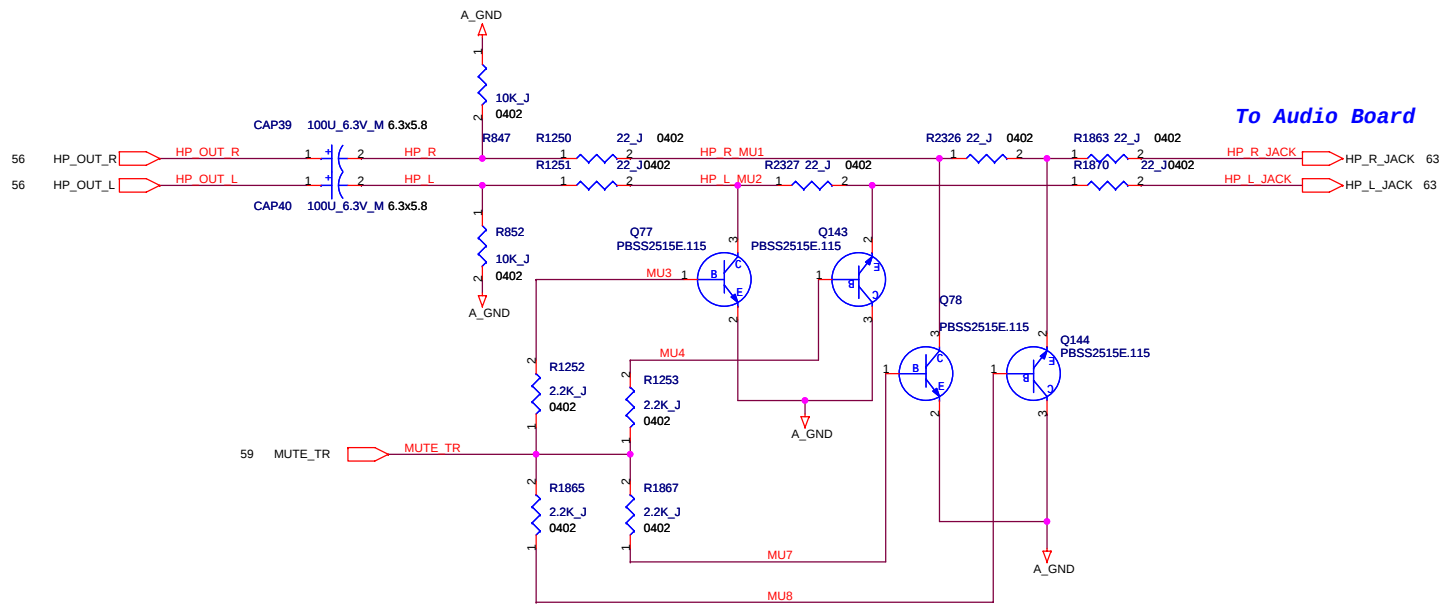


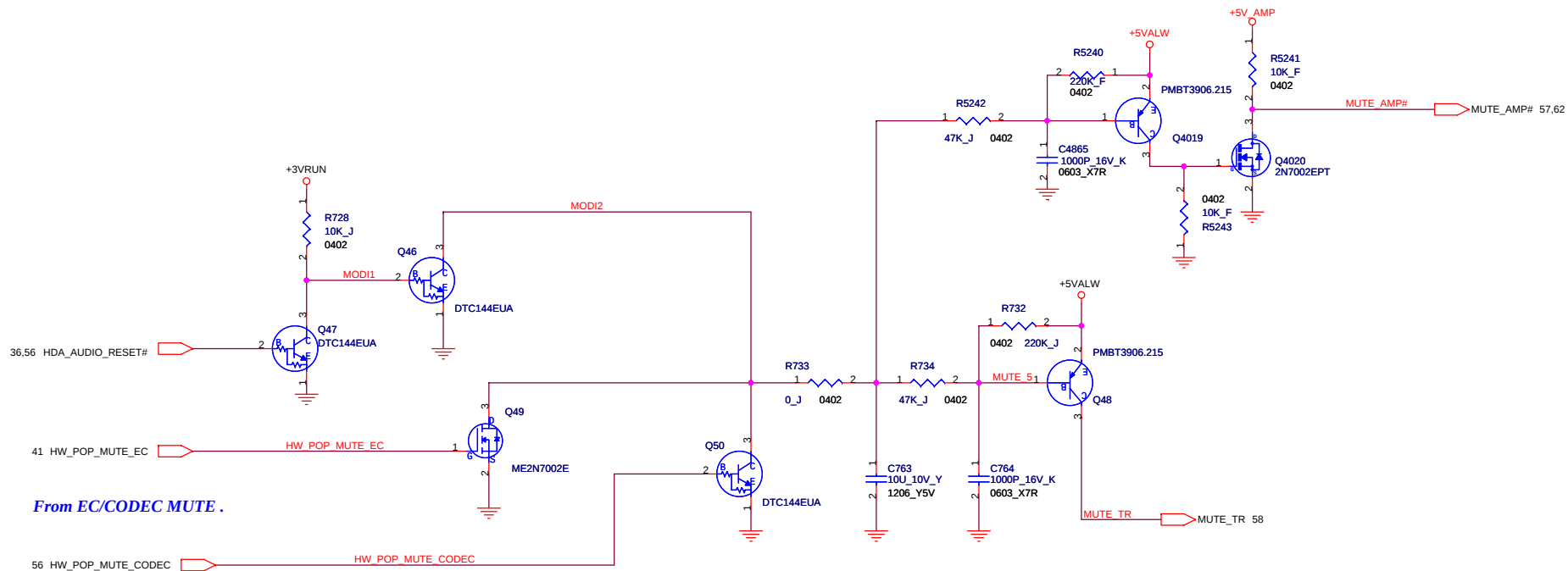
Close to Amp

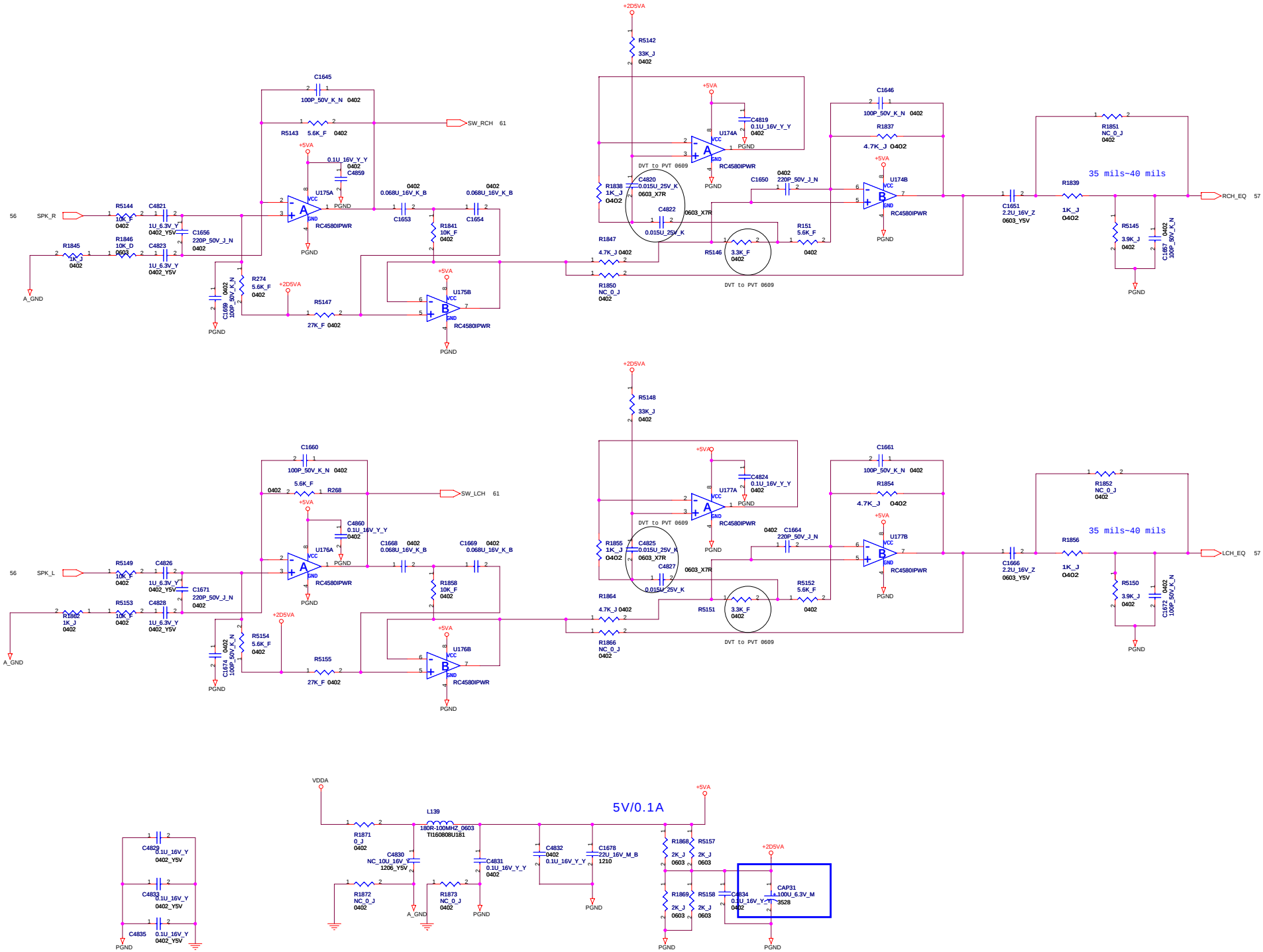


GAIN

External adjustable	Adjustable range from 12db to 18db
Fixed	Pull high=18db Pull low=12db







Filter Circuit

Vendor recommendation not use for

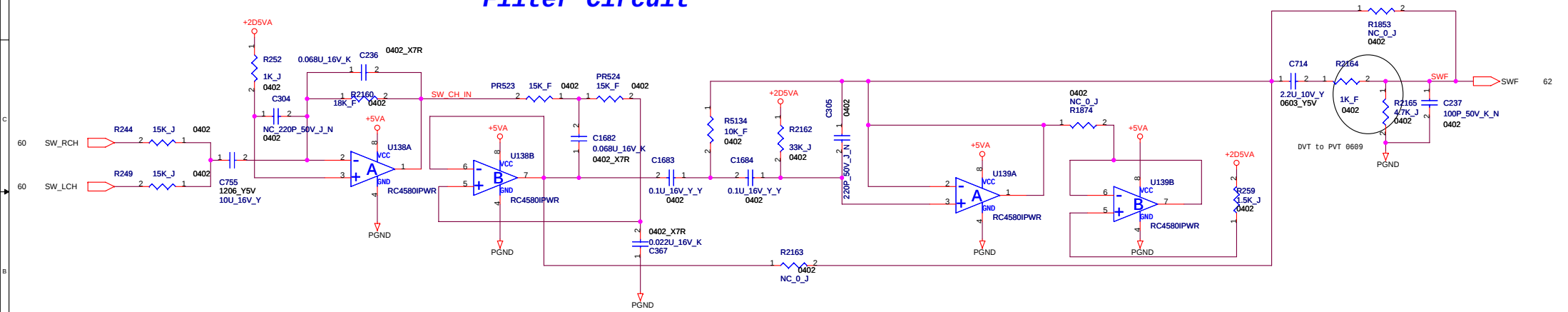
1) Input impedance

As described in the datasheet (P5), match input impedance at IN+ and IN-.

We are afraid of pop noise on this board.

Current SWF impedance is too big, so we recommend to reduce SWF output impedance.

Does R2164, R2165 and C237 Circuit need?

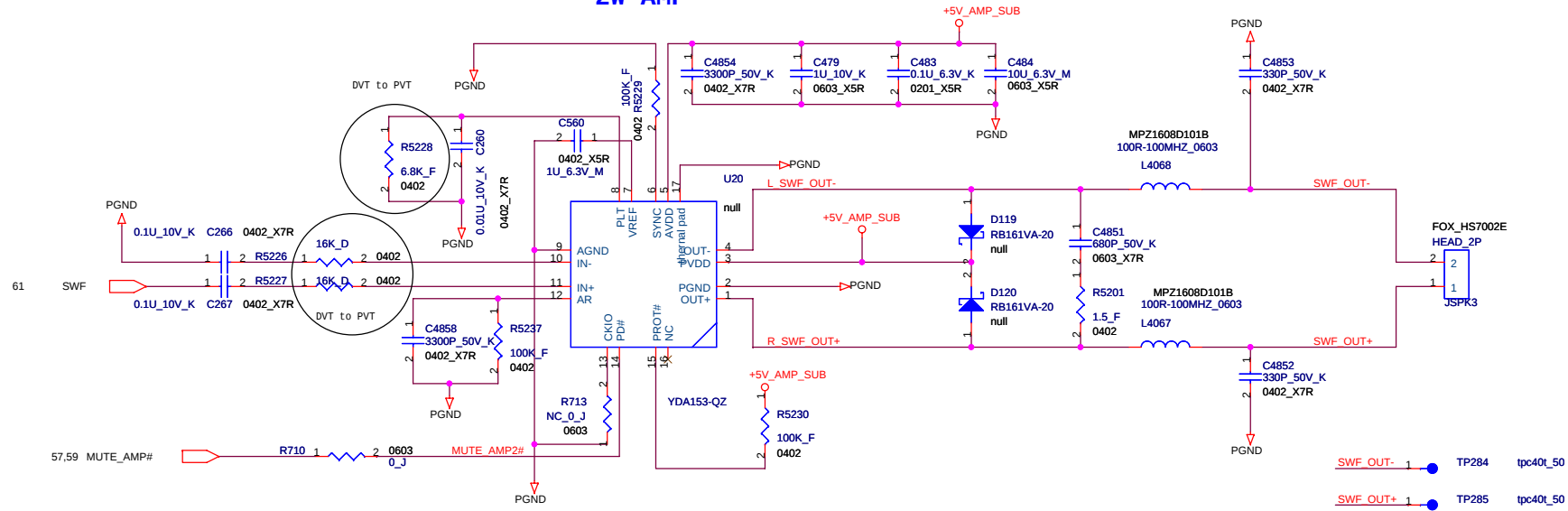


FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title		
Filter Circuit		
Size	Document Number	Rev
Custom	M780(MBX-194)	0.1
Date:	Friday, June 13, 2008	Sheet 61 of 79

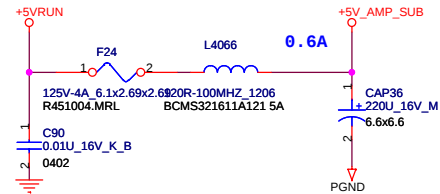
SUB_WOOFER AMP

C479, C484
Locate them close to PVDD pin

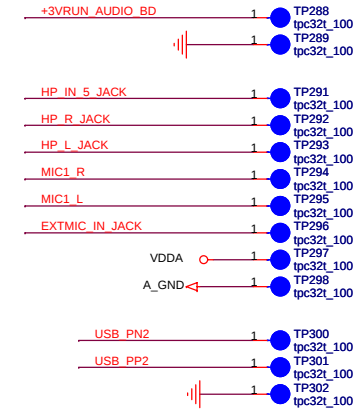
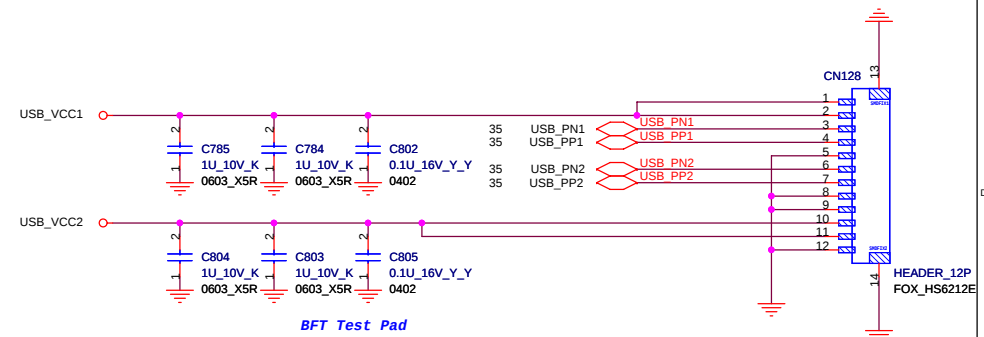
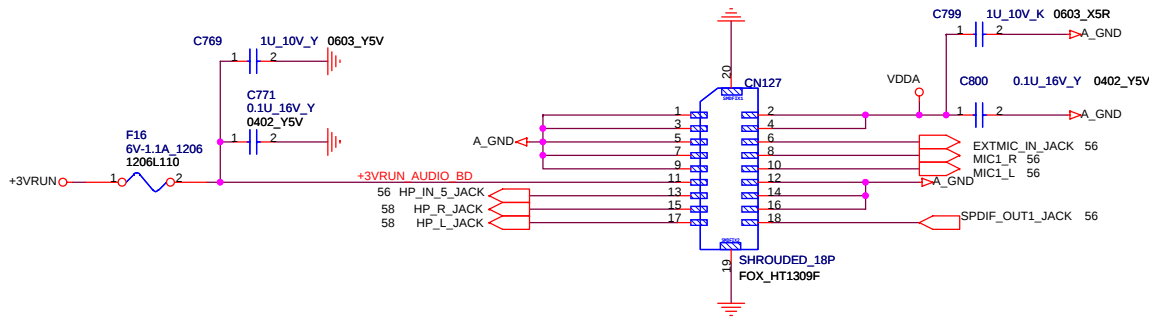
2W AMP



SUB_WOOFER POWER

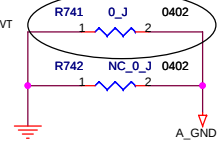


Audio Board connector

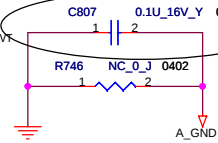


Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

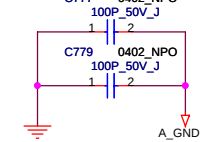


Close screw hole H5

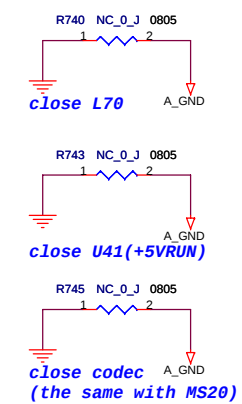


Isolate screw hole H4, and add EMI/ESD solution

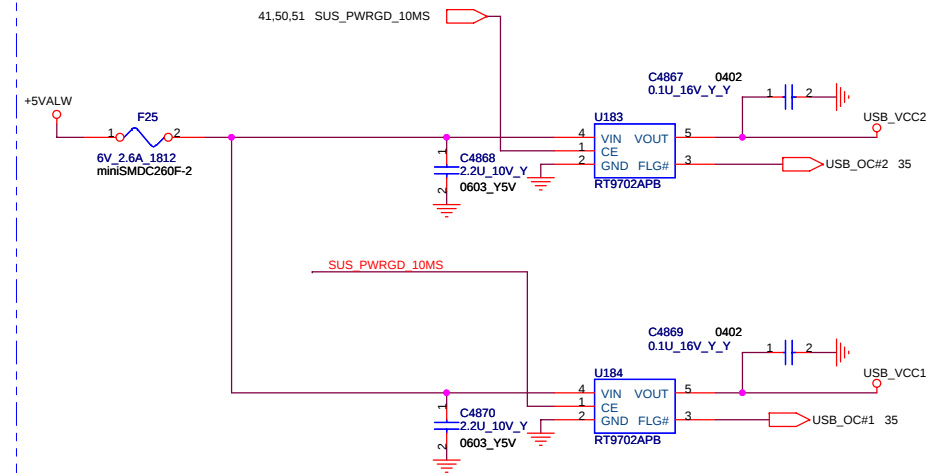
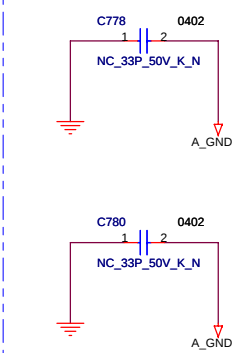
EMI



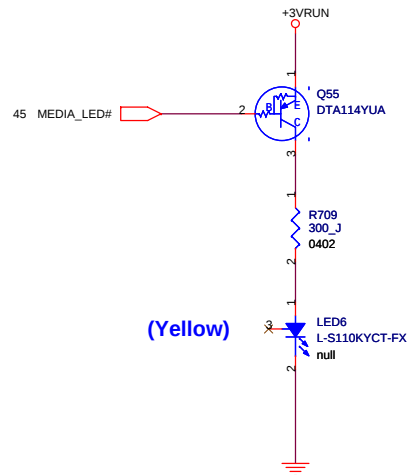
Add jumper resistor for Return patch



Original EMI back up solution to continue with MS20(bridge between GND and A_GND)



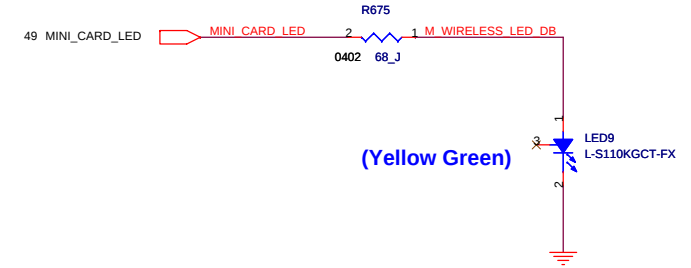
MS/SD LED



(Yellow)

230.(Page 64) 07/12/05 Change MS/SD LED control signal share one LED

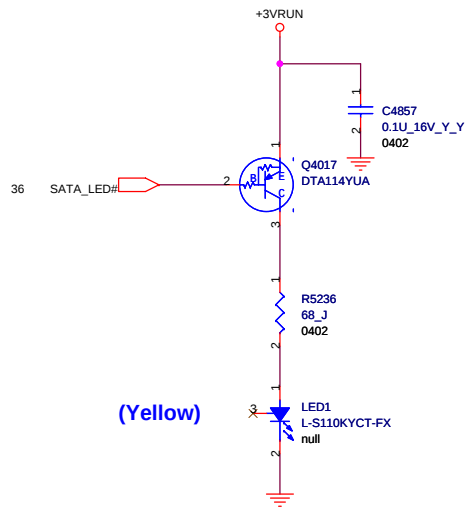
WLAN/BLUETOOTH LED



(Yellow Green)

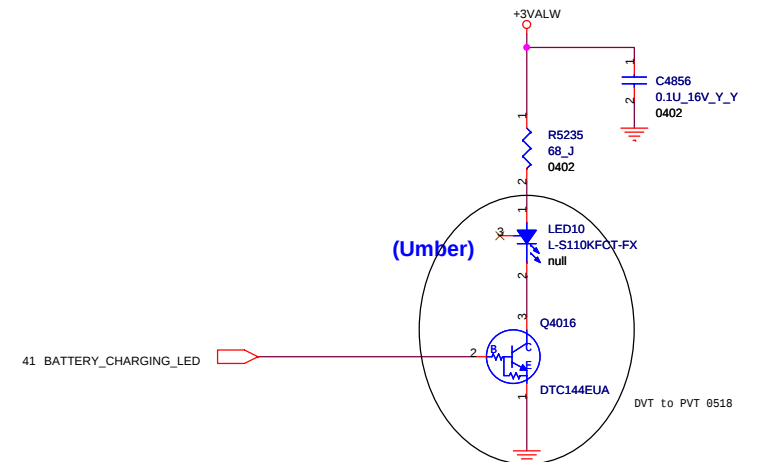
232.(Page 64) 07/12/05 Change Wireless/Bluetooth LED control signal share one LED

HDD/ODD LED

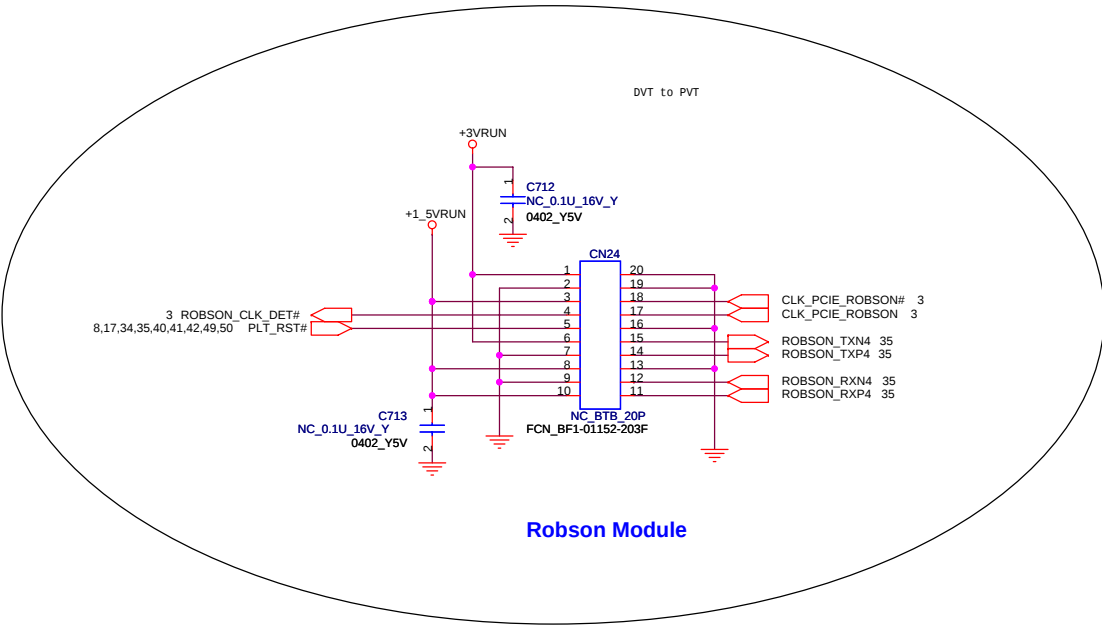


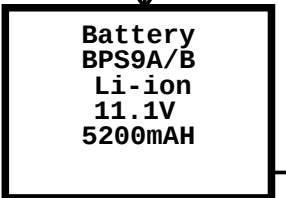
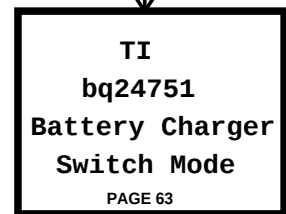
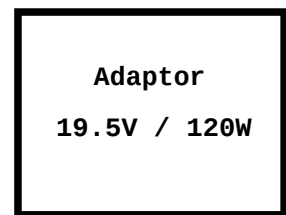
(Yellow)

Charge LED



(Umber)





DCBATOUT

ALW_ON

DCBATOUT

SUS_ON

DCBATOUT

RUN_ON1

DCBATOUT

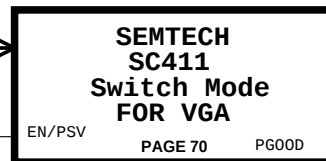
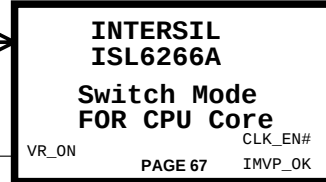
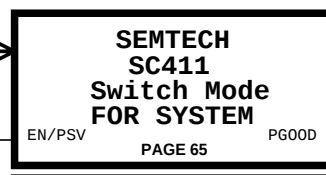
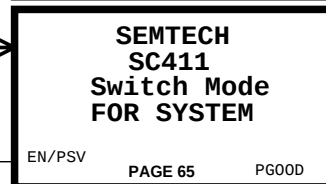
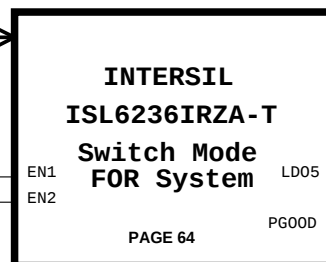
RUN_ON1

DCBATOUT

IMVP_VR_ON

DCBATOUT

RUN_ON1



System

+5VALW/6A

System

+3VALW/5A

+5VALW_LDO

ALW_PWRGD

+12V For Load switch

+1_8VSUS/12A

+1_05VRUN/5A

+1_5VRUN/4.5A

VHCORE/50A

NV_VDD(0.9V/1.2V)/21A

SUS_ON

RUN_ON

SUS_ON

RUN_ON

RUN_ON2

DDR2_PWRGD

RUN_PWRGD

RUN_ON1

EC_CLK_EN#

IMVP_OK

N-Channel transistor

N-Channel transistor

N-Channel transistor

N-Channel transistor

N-Channel transistor

62998 LDO

APL5913 LDO

+5VSUS/1A

+5VRUN/4.5A

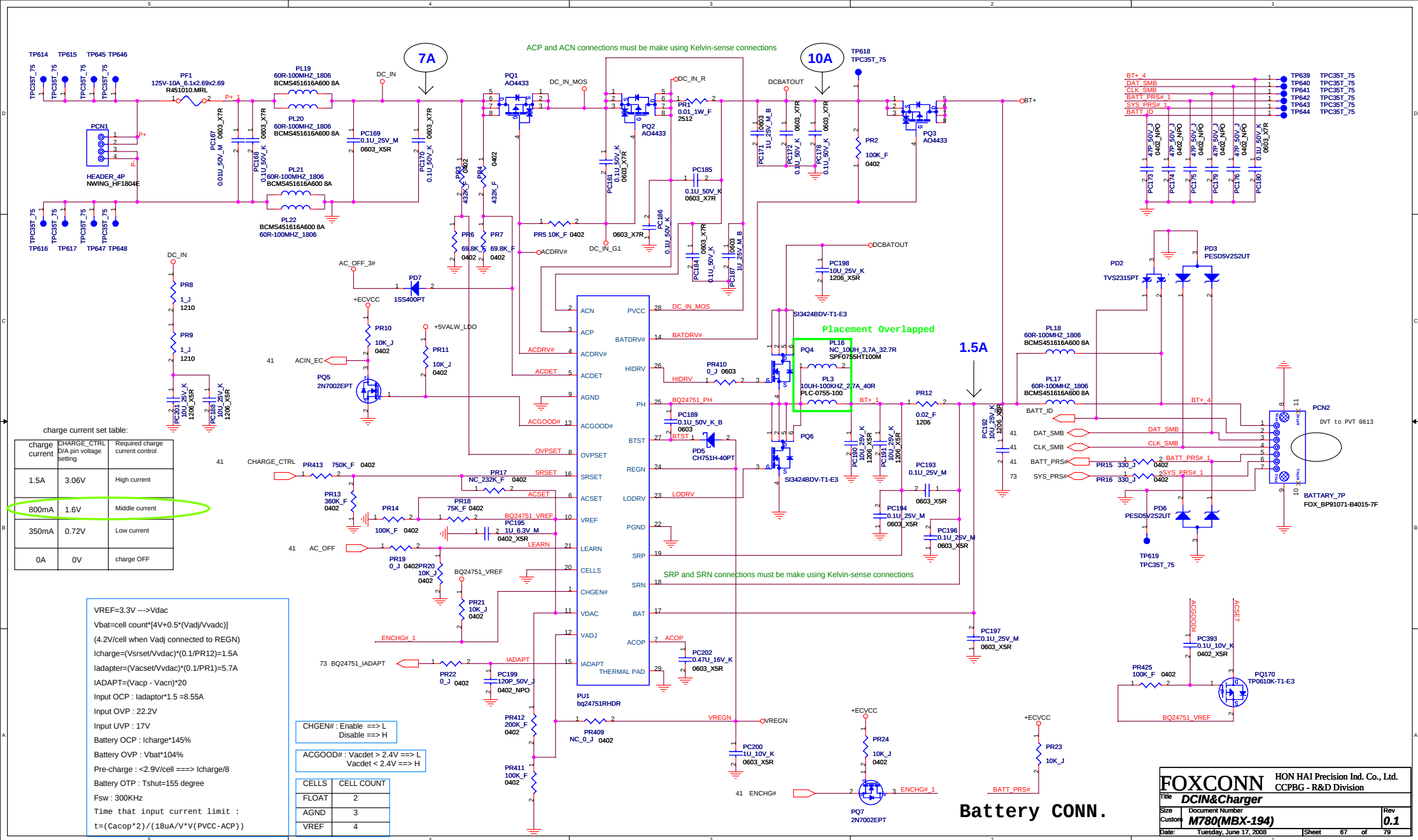
+3VSUS/1A

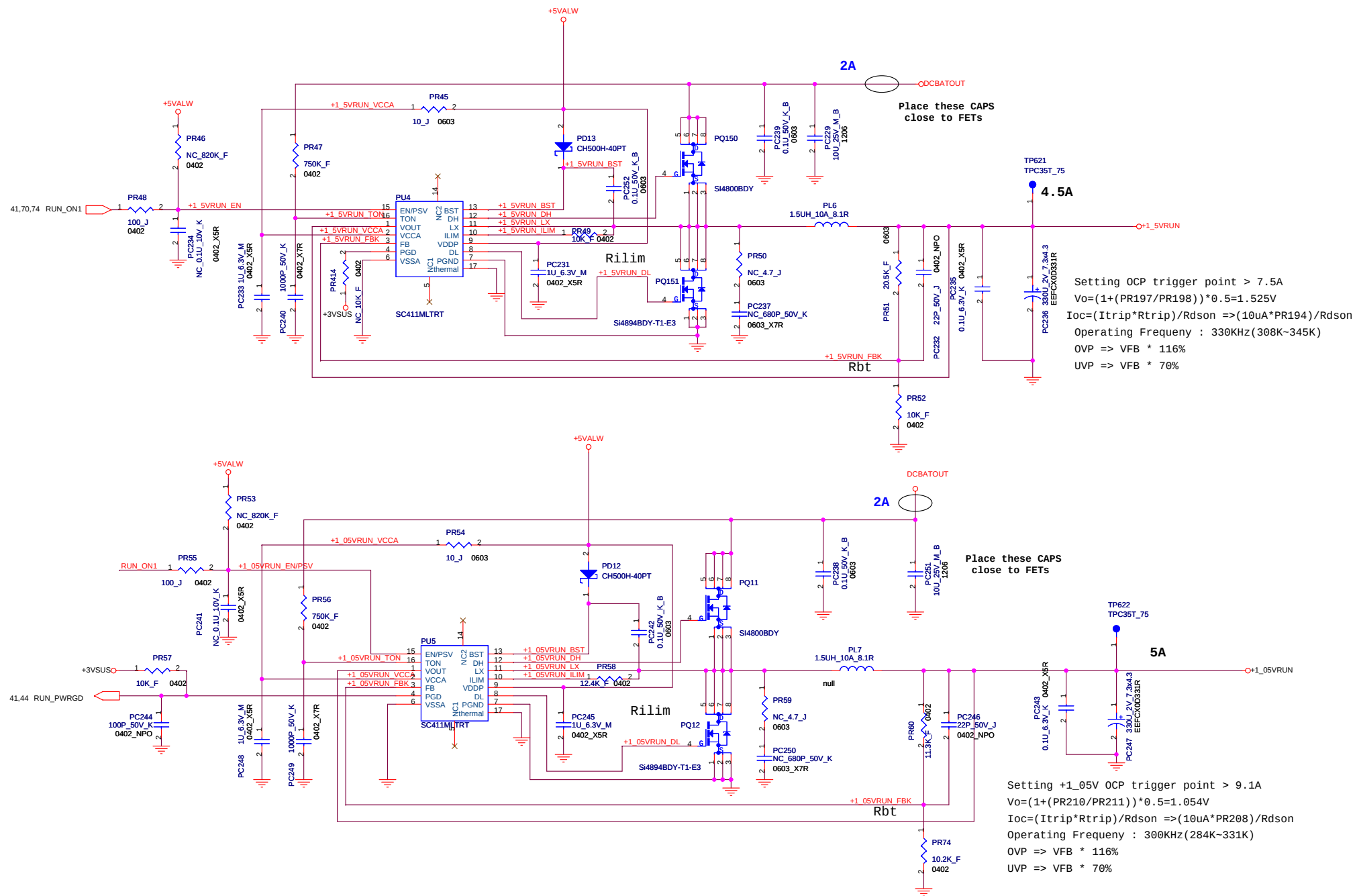
+3VRUN/3.5A

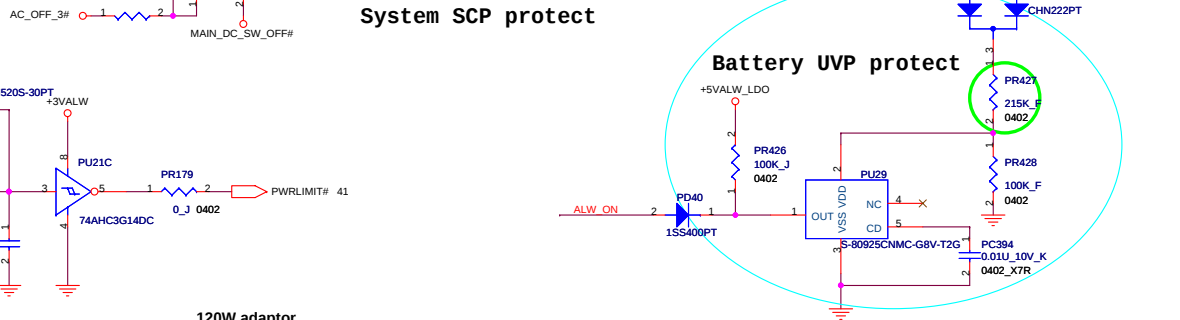
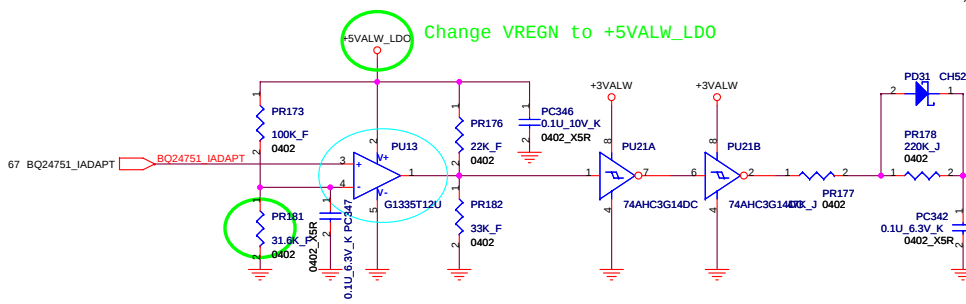
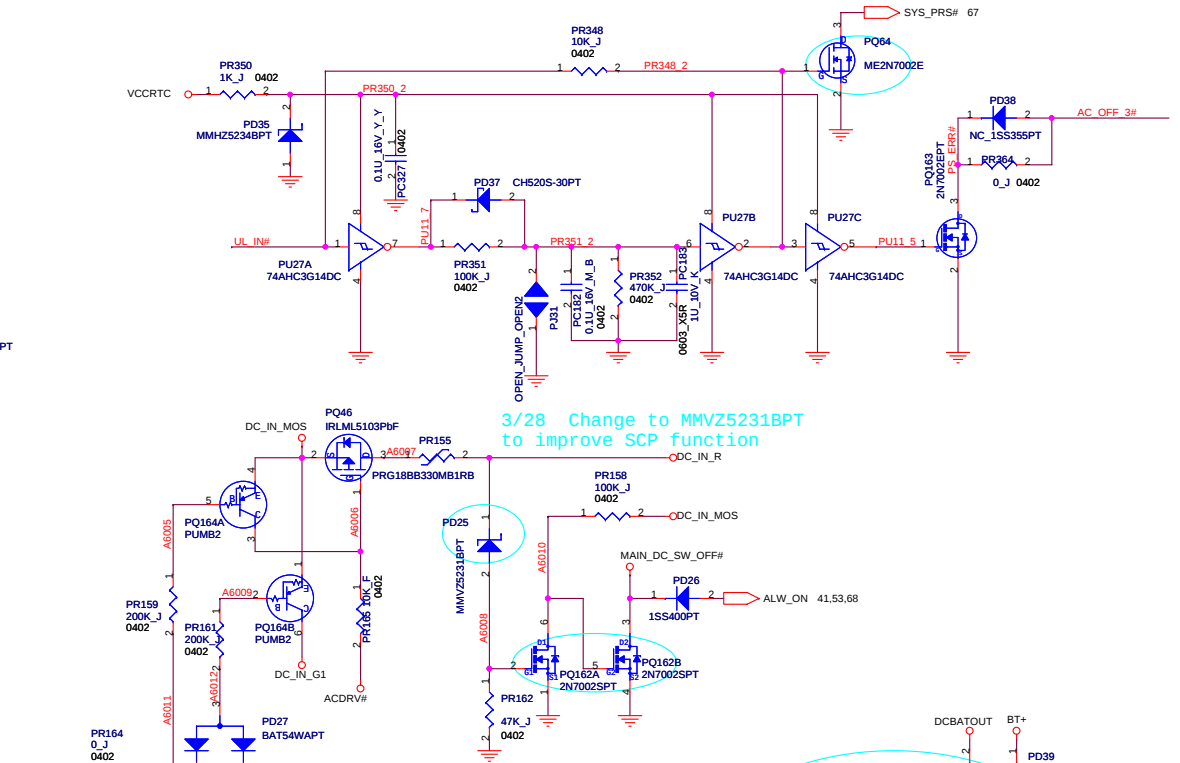
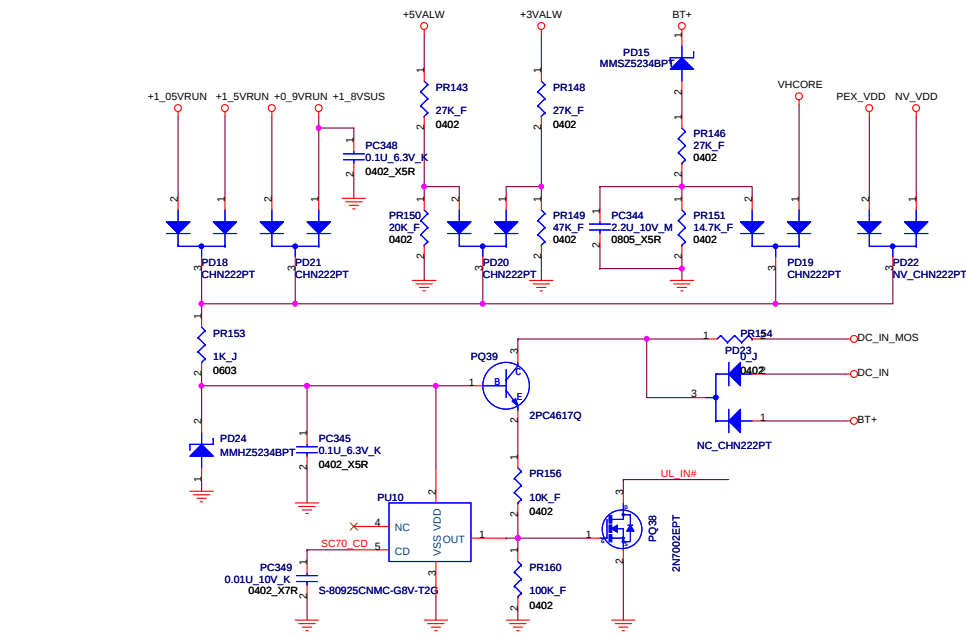
+1_8VRUN/5A

PEX_VDD(0.9V)/2A

PEX_VDD(1.113V)/1.6A







120W adaptor

PWRLIMIT	1.2V/114W
----------	-----------

Adaptor max load: 7.7A under 3 sec
Adaptor OCP: 9.7A typ
11A max

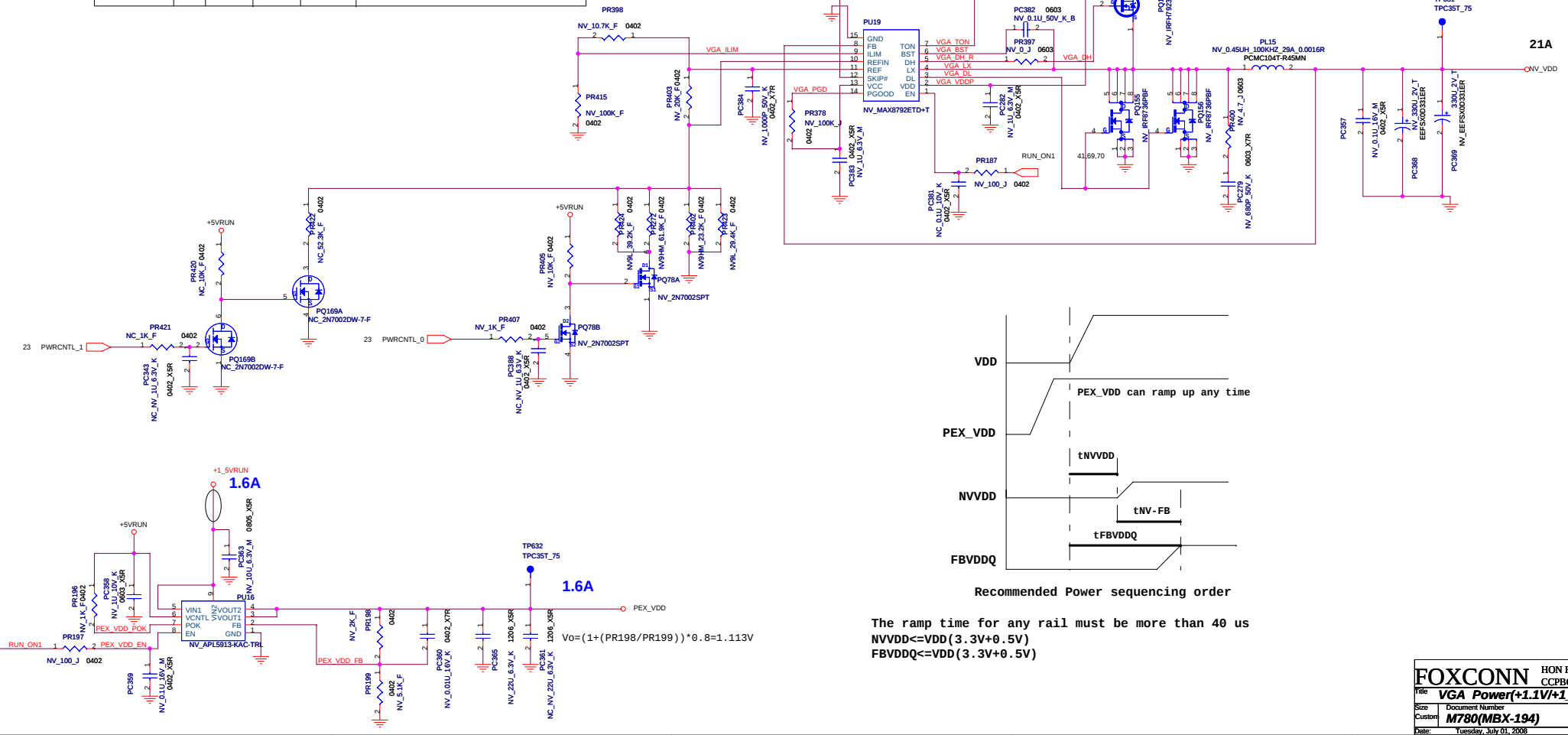
3/28 Add battery UVP protect circuit to separate SCP and OCP function.

TABLE(01/08)

NB9P	I/O	Inter pull low			PR402: 23.2K_1%_0402, 1R-0002322-F200 PR272: 61.9K_1%_0402, 1R-0006192-F200
GPU Voltage			1.05V	0.9V	
PWRCNTL_0	0	Yes	H	L	

NB9M	I/O	Inter pull low			PR423: 29.4K_1%_0402, 1R-0002942-F200 PR424: 39.2K_1%_0402, 1R-0003922-F200
GPU Voltage			1.17V	0.9V	
PWRCNTL_0	0	Yes	H	L	

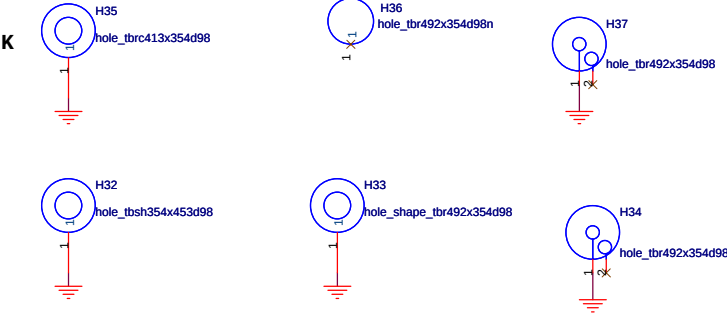
Setting current limit trigger point >25A
 $V_o = V_f$; $V_f = ((PR272 + PR402) / (PR403 + PR272 + PR402)) * 2$
 $V_{lim} = 20[I_o - I_r / 2] * R_{low-dsn} * 1.2$
 Operating Frequency : 300KHz
 $OVP \Rightarrow V_o + 0.25V$
 $UVP \Rightarrow V_{FB} - 0.16V$



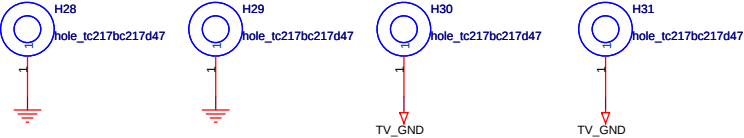
HOLE(TOP SIDE)

HOLE(BOTTOM SIDE)

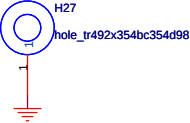
Type 1



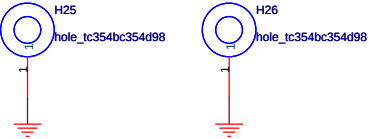
Type 2



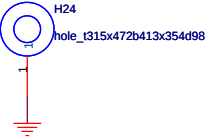
Type 3



Type 4



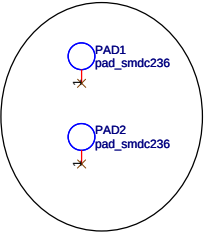
Type 5



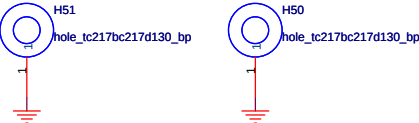
Type 6



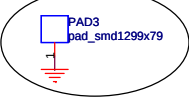
DVT to PVT 0617



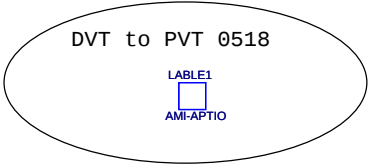
Robason Hole



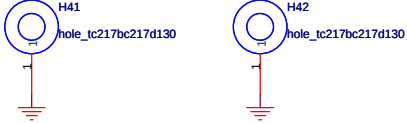
DVT to PVT



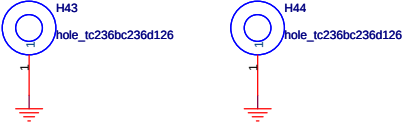
DVT to PVT 0518



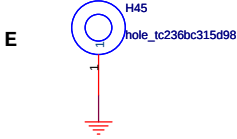
Type 2



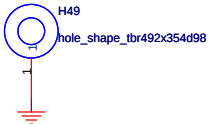
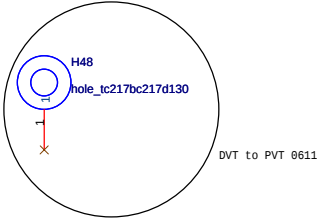
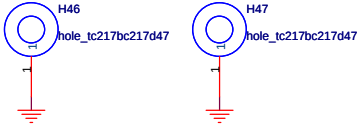
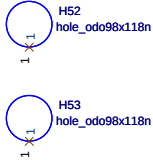
Type 3



Type 4



Type CPU



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CPBG - R&D Division		
Title	HOLE & BOSS	
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Date:	Wednesday, June 25, 2008	Sheet 75 of 79

EVT TO DVT

Page 20 .Add power source for FB_DLLAVDD1 & FB_PLLAVDD1

Page 61. change R2164 from 1K to 2.7K for MOR request

Page 57. change SPK AMP Gain setting to 18dB for MOR request

Page 48,49. change BT LED control signal source from BT module directly

Page 32,41. Use SW1 one pin to disable Fan monitor function

Page 54. F11,F12,F18,F19 change from 350mA to 250mA

Page 59. Change Q4019 pin 2 from +3VALW to +5VALW

Page 37. Change EC_OUT1 pin to GPIO12

Page 41. Add R572,R573,R574 pull low

Page 61. R259 NC

Page 41. Add C465,C466 47pF pull low

Page 24. Add R586,R590 for MOR request.

Page 3. Add R5248 in series for MCH_CLK_REQ#.

Page 47. Add F27 Poly switch for CF card protection.

Page 37. Add D9 diode for RUNTIME_SCI# leakage.

Page 41. Add D17,D24 for EC_RCIN#,EC_A20GATE leakage.

Page 23. Add R1779 for PWRCNTL_0 pull high.

Page 37. Add R455 for Finger print Detect.

Page 60,63. Remove C4830,R740,R743,R745 for MOR request.

Page 33. Add R340,Q122,R2373,Q123 for HDMI drop issue.

Page 3. Add C820 ,C821 for Robson CLK to match rising and falling time spec.

Page 52. Add F13 for CIR FFC protection.

Page 40. Add R75 ,R5249,C138 for 8057 used

Page 49. Remove C18,add R617 for MOR request.

Page 41. Add C913 for EMI.

Page 42. Add C962 for EMI.

Page 53. Add C967 for EMI.

Page 71. Add C968 for EMI.

Page 68. Add C990 for EMI.

Page 74. Add C991 for EMI.

Page 32. Add C992 for EMI.

Page 56. Add C368 for TV .

Page 60. change C4820,C4822,C4825,C4827 to 0.047U
R5146,R5151 to 1.8k R151,R5152 t o5.6k

Page 61. change R244,R249 to15k R2160 to 18k, PR523,PR524 to 15k, C367 to 0.022U, R2164 to 1.8k.

Page 31. Add C467,C468,C469 for EMI.

Page 46. Mount C453 for EMI.

Page 41. Add R575 for CF always power on.

Page 37. Remove R455,R486 for FP_DET#,change by BIOS detect.

Page 6. add C88,C89 for MOR request.

Page 72. add R5250 for MOR request.

Page 34. add C370,C369 for EMI

Page 41. add C371 for EMI

Page 29. add C993 for EMI

Page 26. add C994 for EMI

Page 41. change charge LED to high active.

Page 57. add C995 for EMI.

Page 33. add C997 for EMI.

Page 62. add C90 for EMI.

Page 41. add C91 for EMI.

Page 54. add C238 for EMI.

Page 47. add U17 ,R91,R92 for CF solution.

Page 73. change PR181 from 34k to 31.6k for changing power limit from 118W to 114W

DVT to PVT

Page 64(LED Status) .charging LED logic change

Page 75(HOLE & BOSS) .Add AMI label on M/BD

Page 31(CRT) .change VSYNC and HSYNC resistor and capacitor for SI test fail.

Page 54(Daughter Board Conn) .change PWR and Suspend LED logic same as M760 for more brightness.

Page 47(PCI CF) .separate CF controller power and card power for hot-plug issue.

Page .change NV9P,9M ,HDCP KEY HH P/N

Page 17(VGA (PCI-E) 1/9) .L4049 change vendor

Page 41(EC+KBC (WPCE775L) .change RP24,RP25 to +3VALW

Page 67(DCIN&Charger) .Delete P31 and P32

Page 68(SYS Power(+3.3V/+5V) .Delete P33 and P34

Page 69(SYS Power(+1.5V/+1.05V) .Delete P37 and P38

Page 70(DDR2 Power(+1.8V/+0.9V) .Delete P310 and P313

Page 71(CPU_Vcore---ISL6266A) .Delete P312

Page 74(VGA Power(0.9V/+1.05V) .Delete P315,P316,P317

Page 43(SATA HDD/CD-ROM) .change CN126 to KOTL

Page 3(CLOCK GEN (SL28648BLC) .U123 change HH P/N

Page 18(VGA (PCI-E BUS)Strap 2/9) .add samsung VRAM strap pin

Page 55(OIDE/CAM) .change OIDE connector to LNC _____ PVT 0605.pdf

Page 60(AUDIO(EQ) .C4820,C4822,C4825,C4827; Change from 0.047u/50V to 0.015u/25V,R5146,R5151; Change from 1.8k to 3.3k

Page 61(AVD20 (Filter Circuit) .R2164 change to 1k,R2165 change to 4.7k

Page 72(Other's power plan) .R5250 mount,PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC

Page 51(USB 2.0) .add USB connector TID No.

Page 55(OIDE/CAM) .change camera connector for easy to unplug.

Page 43(SATA HDD/CD-ROM) .change ODD connector to 14 pin

Page 75(HOLE & BOSS) .change H48 to PTH type

Page 55(OIDE/CAM) .reserve 3.3V for camera module.

Page 47(PCI CF) .change discharge circuit for CF card power,add 4.7U for CF card power ,change CF card LED power source.

Page 45(PCI (ILINK) .change Y5 capacitor for accuracy.

Page 71(CPU_Vcore---ISL6266A) .PR429 NC

Page 67(DCIN&Charger) .PCN2 add two pillars to fix position for our production line smoothly. _____PVT 0613.pdf

Page 1(index) .change HH P/N

Page 75(HOLE & BOSS) .add two PAD for ME request

Page 68(SYS Power (+3.3V/+5V) .PU2 Pin9 ,pin10 connect from +5VALW_PWM to +5VALW _____ PVT 0617.pdf

Page 41(EC+KBC (WPCE775L) .mount R516,C592 for EMI

Page 24(VGA (INTER DISPLAY) 8/9) .mount C828 for EMI

Page 41(EC+KBC (WPCE775L) .add C998 for EMI

Page 48(bluetooth) .add C999 for EMI

Page 40(Marvell GLAN(88E8055) .add C1000 for EMI

Page 72(Other's power plan) .add C1001 for EMI

Page 41(EC+KBC (WPCE775L) .add C1002 for EMI

Page 56(AUDIO(CODEC & POWER) .add C1003 for EMI

Page 54(Daughter Board Conn) .add C1004,C1005 for EMI

Page 54(Daughter Board Conn) .add L31,L32 for EMI

Page 23(VGA (XTAL/GPIO) 7/9) . reserve D10,R5251,R5252,C93,R1780 for HDMI Audio issue.

Page 56(AUDIO(CODEC & POWER) . reserve R749,C12 for HDMI Audio issue.

Page 63(Audio BOARD conn) . mount R741,change R744 to C807 0.1u for EMI

Page 56(AUDIO(CODEC & POWER) .change R5222 to C809 0.1uf for EMI.

Page 42(AUDIO(Flash ROM/SPI) .CN16 change from 1200 to 1203 for EOL issue.

Page 65(Robson 1.7 Connector) .remove CN24,C712,C713 for Robson no used.

Page 65(AUDIO (SUBWOOFER AMP).change R5228 from 68k to 6.8k for MOR request.

Page 75(HOLE & BOSS) .Add PAD 3 for ME request.

Page 75(LVDS) .reserve C472 for invertor power _____ PVT 0625.pdf

Page 31(CRT) .change L25,L26,L27 to 120R bead,C467,C468,C469 to NC.

Page 62(AUDIO (SUBWOOFER AMP) .change R5226,R5227 to 0.5% resistors

Page 54(Daughter Board Conn) .add U11 for finger print protection. _____ PVT 0627.pdf

Page 71(CPU_Vcore---ISL6266A) .PC389 NC,PC299,PC289 mount for solid cap issue.

Page 68(SYS Power (+3.3V/+5V) .PC387 NC for solid cap issue

Page 74(VGA Power(0.9V/+1.05V) .PC391 NC,PC353 mount for solid cap issue.

Page 32(LVDS) .Add C472 for solid cap issue.

Page 45(PCI (ILINK) .change R540-R543 to 47 ohm for MS overshoot and undershoot issue.

Page 41(EC+KBC (WPCE775L) .R516,C592 NC for signal quality.

Page 3(CLOCK GEN (SL28648BLC) .change R767 to 47 ohm for EMI issue. _____ PVT 0629.pdf