

Schematics Page Index (Title / Revision / Change Date)

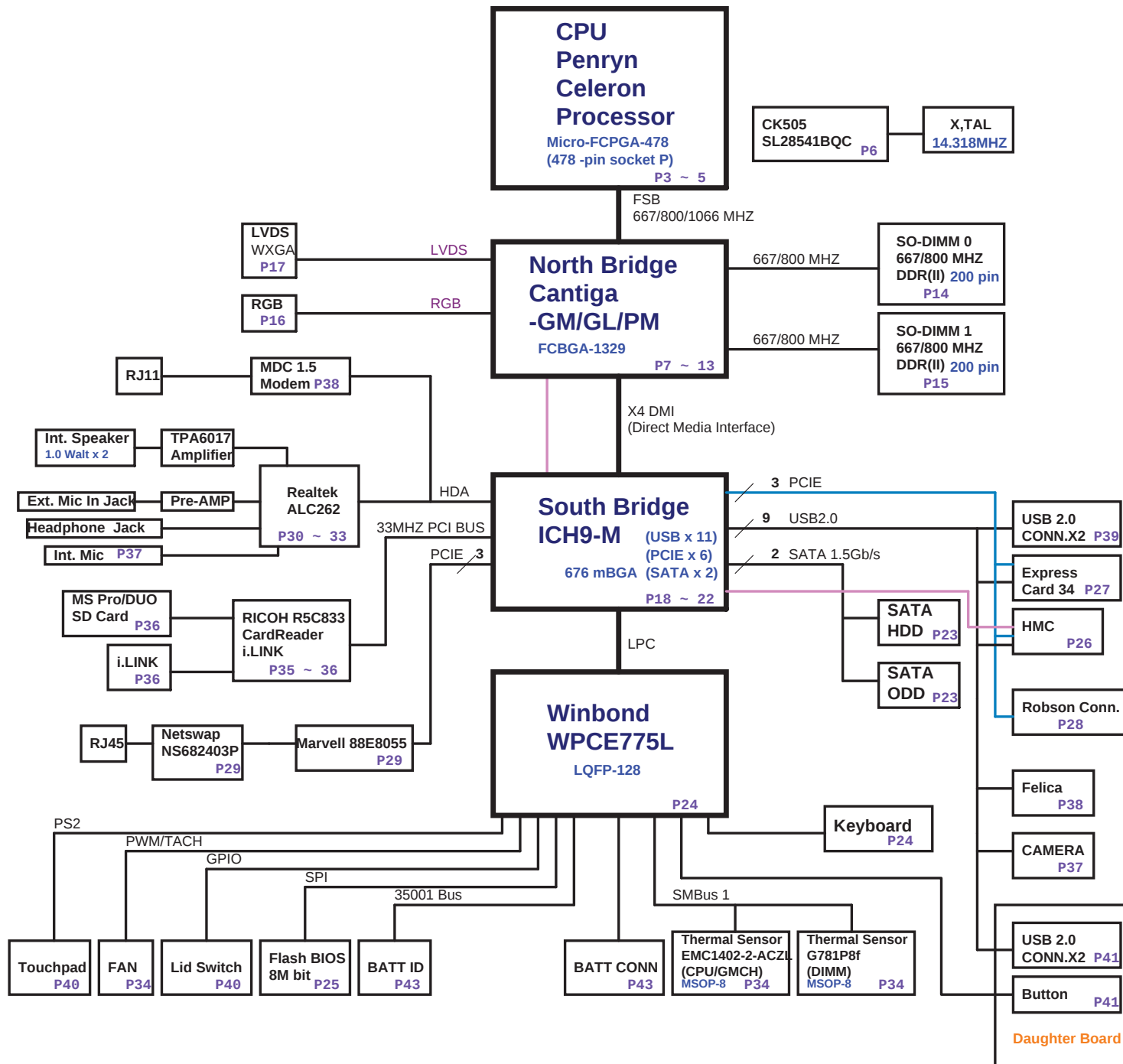
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15	DDRII(S0-DIMM_1) 2/2	1.0	08'07'03	50	HOLE	1.0	08'07'03
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Project Code & Schematics Subject: M790 Main Board_6L

PCB P/N:	1P-0086J01-6010(IRIS)
U/B P/N:	1P-1086J02-6010(IRIS)
P/B P/N:	1P-1086J03-6010(IRIS)
R/B P/N:	1P-1086J01-6010(IRIS)

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FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
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M790(Montevina)



TI CHARGER BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC TPS51125RGER P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW

SYSTEM DC/DC SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM

SYSTEM DC/DC TPS51116RGER P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS +0_9VSUS

CPU DC/DC ISL6262A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHOCORE

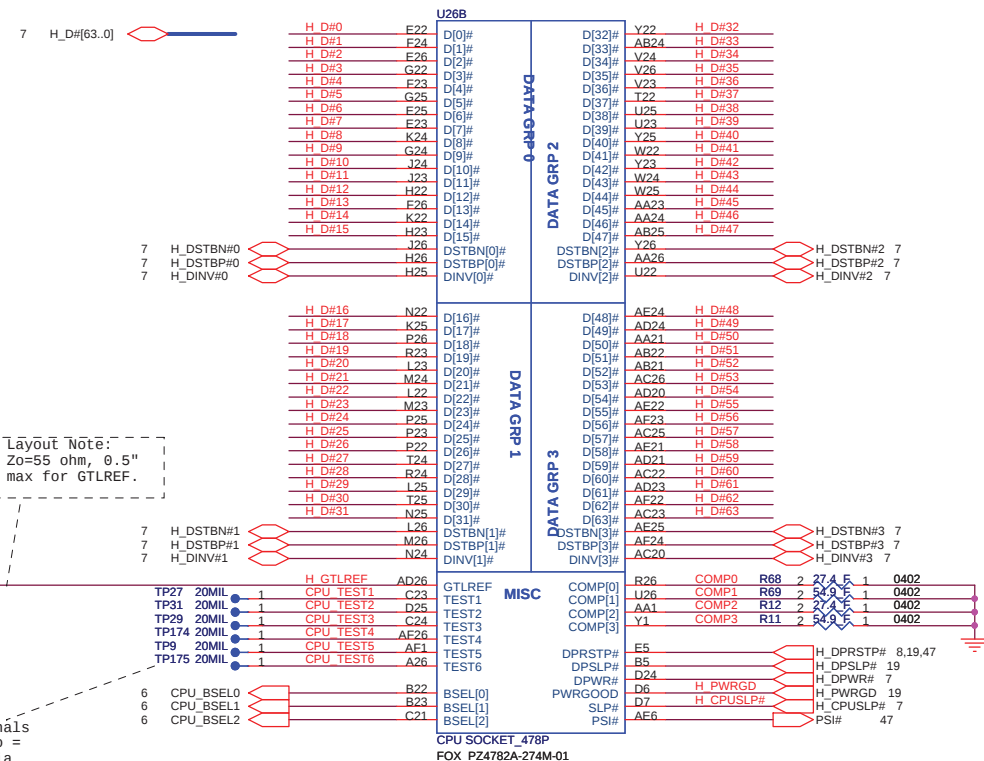
SYSTEM DC/DC APL5912 P.70	
INPUTS	OUTPUTS
+1_5VRUN	PEX_VDD

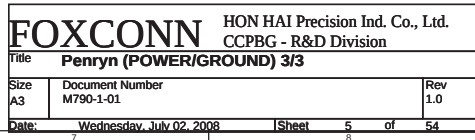
SYSTEM DC/DC TPS51117 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

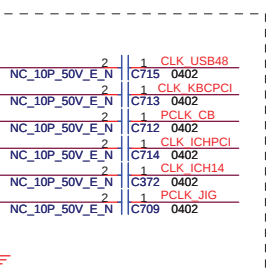
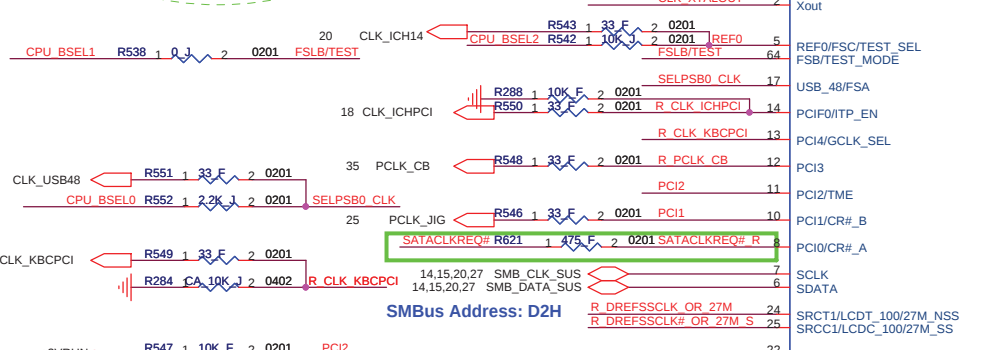
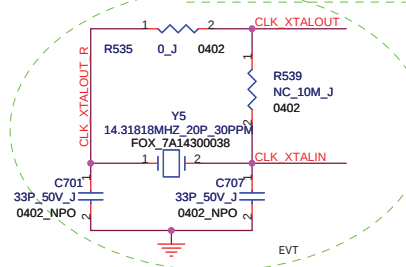
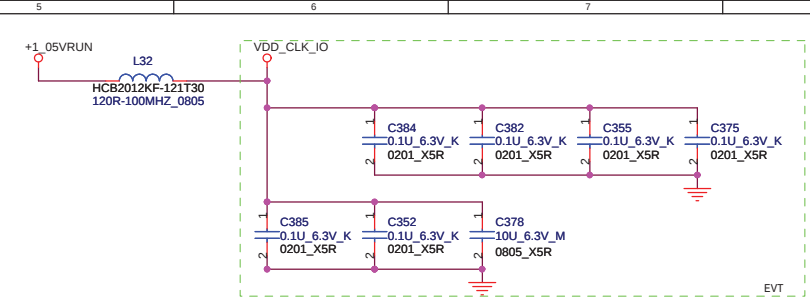
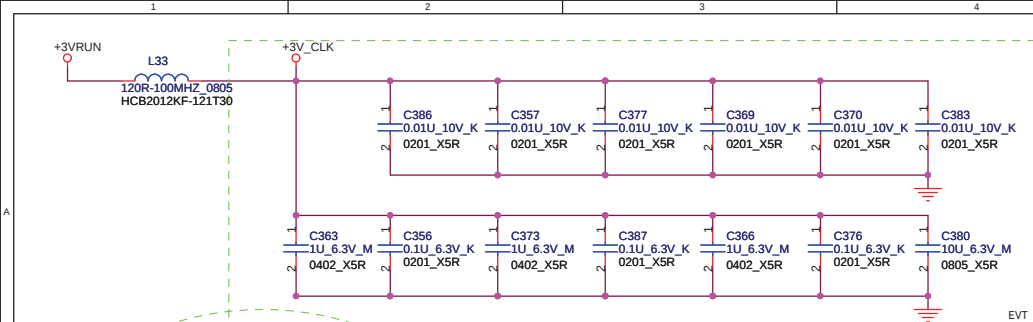
SYSTEM DC/DC MAX8776 P.71	
INPUTS	OUTPUTS
DCBATOUT	+VGF_X_CORE

Place close to CPU

Route the TEST3 and TEST5 signals through a ground referenced $Z_o = 55\text{-ohm}$ trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.





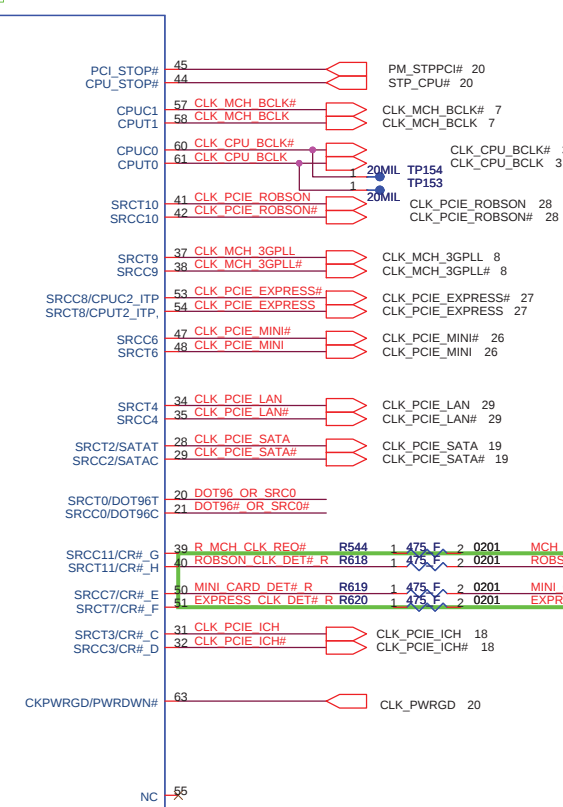
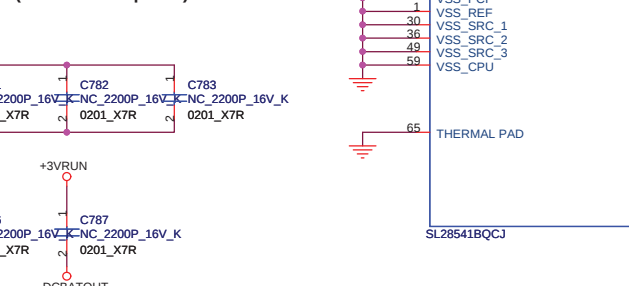


close to clk gen (For EMI)

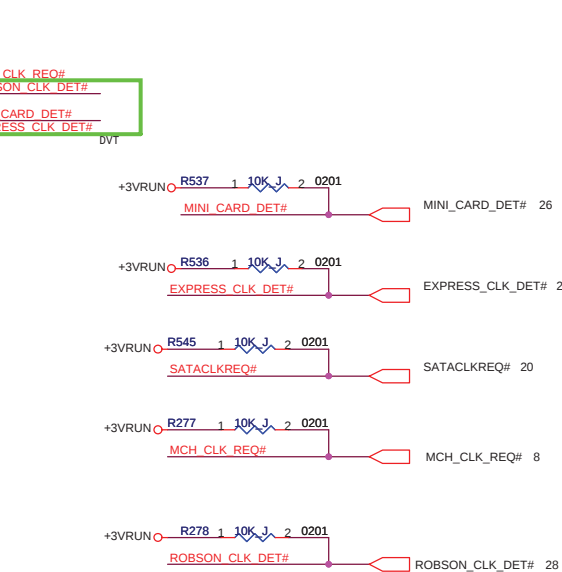
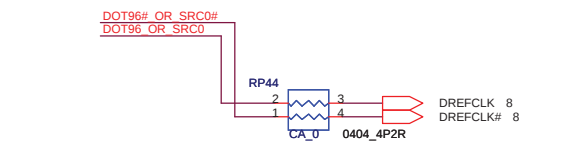
FSB Frequency Table:

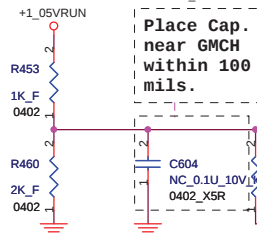
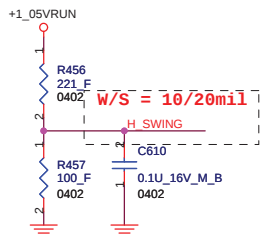
FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

(For EMI request)



Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	ROBSON_CLK_DET#





H D#0 F2 H D# 0
 H D#1 G8 H D# 1
 H D#2 F8 H D# 2
 H D#3 E5 H D# 3
 H D#4 G2 H D# 4
 H D#5 H6 H D# 5
 H D#6 H2 H D# 6
 H D#7 F6 H D# 7
 H D#8 D4 H D# 8
 H D#9 H3 H D# 9
 H D#10 M9 H D# 10
 H D#11 M11 H D# 11
 H D#12 J1 H D# 12
 H D#13 J2 H D# 13
 H D#14 N12 H D# 14
 H D#15 J6 H D# 15
 H D#16 P2 H D# 16
 H D#17 L2 H D# 17
 H D#18 R2 H D# 18
 H D#19 N9 H D# 19
 H D#20 L6 H D# 20
 H D#21 M5 H D# 21
 H D#22 J3 H D# 22
 H D#23 N2 H D# 23
 H D#24 R1 H D# 24
 H D#25 N5 H D# 25
 H D#26 N6 H D# 26
 H D#27 P13 H D# 27
 H D#28 N8 H D# 28
 H D#29 L7 H D# 29
 H D#30 N10 H D# 30
 H D#31 M3 H D# 31
 H D#32 Y3 H D# 32
 H D#33 AD14 H D# 33
 H D#34 Y6 H D# 34
 H D#35 Y10 H D# 35
 H D#36 Y12 H D# 36
 H D#37 Y14 H D# 37
 H D#38 Y7 H D# 38
 H D#39 W2 H D# 39
 H D#40 AA8 H D# 40
 H D#41 Y9 H D# 41
 H D#42 AA13 H D# 42
 H D#43 AA9 H D# 43
 H D#44 AA11 H D# 44
 H D#45 AD11 H D# 45
 H D#46 AD10 H D# 46
 H D#47 AD13 H D# 47
 H D#48 AE12 H D# 48
 H D#49 AE9 H D# 49
 H D#50 AA2 H D# 50
 H D#51 AD8 H D# 51
 H D#52 AA3 H D# 52
 H D#53 AD3 H D# 53
 H D#54 AD7 H D# 54
 H D#55 AE14 H D# 55
 H D#56 AE3 H D# 56
 H D#57 AC1 H D# 57
 H D#58 AE3 H D# 58
 H D#59 AC3 H D# 59
 H D#60 AE11 H D# 60
 H D#61 AE8 H D# 61
 H D#62 AG2 H D# 62
 H D#63 AD6 H D# 63

H SWING C5
 H RCOMP E3

Traces width 10 mils.

CANTIGA GM

H AVREF
H DVREF

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

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H_CPUSLP#

H_CPURST#
H_CPUSLP#

H_CPURST#
H_CPUSLP#

HOST

H_A#_3 A14 H_A#3
 H_A#_4 C15 H_A#4
 H_A#_5 F16 H_A#5
 H_A#_6 H13 H_A#6
 H_A#_7 C18 H_A#7
 H_A#_8 M16 H_A#8
 H_A#_9 J13 H_A#9
 H_A#_10 P16 H_A#10
 H_A#_11 R16 H_A#11
 H_A#_12 N17 H_A#12
 H_A#_13 M13 H_A#13
 H_A#_14 E17 H_A#14
 H_A#_15 E17 H_A#15
 H_A#_16 G20 H_A#16
 H_A#_17 G20 H_A#17
 H_A#_18 B19 H_A#18
 H_A#_19 J16 H_A#19
 H_A#_20 E20 H_A#20
 H_A#_21 H16 H_A#21
 H_A#_22 J20 H_A#22
 H_A#_23 L17 H_A#23
 H_A#_24 A17 H_A#24
 H_A#_25 B17 H_A#25
 H_A#_26 L16 H_A#26
 H_A#_27 C21 H_A#27
 H_A#_28 J17 H_A#28
 H_A#_29 H20 H_A#29
 H_A#_30 B18 H_A#30
 H_A#_31 K17 H_A#31
 H_A#_32 B20 H_A#32
 H_A#_33 E21 H_A#33
 H_A#_34 K21 H_A#34
 H_A#_35 L20 H_A#35

H_ADS# H12 H_ADS# 3
 H_ADSTB#_0 B16 H_ADSTB#0 3
 H_ADSTB#_1 G17 H_ADSTB#1 3
 H_BNR# A9 H_BNR# 3
 H_BPRI# E11 H_BPRI# 3
 H_BREQ# G12 H_BREQ# 3
 H_DEFER# E9 H_DEFER# 3
 H_DBSY# B10 H_DBSY# 3
 HPLL_CLK AH7 CLK_MCH_BCLK 6
 HPLL_CLK AH6 CLK_MCH_BCLK# 6
 H_DPWR# J11 H_DPWR# 4
 H_DRDY# E9 H_DRDY# 3
 H_HIT# H9 H_HIT# 3
 H_HITM# E12 H_HITM# 3
 H_LOCK# H11 H_LOCK# 3
 H_TRDY# C9 H_TRDY# 3

H_DINV#_0 J8 H_DINV#0 4
 H_DINV#_1 L3 H_DINV#1 4
 H_DINV#_2 Y13 H_DINV#2 4
 H_DINV#_3 Y1 H_DINV#3 4

H_DSTBN#_0 L10 H_DSTBN#0 4
 H_DSTBN#_1 M7 H_DSTBN#1 4
 H_DSTBN#_2 AA5 H_DSTBN#2 4
 H_DSTBN#_3 AE6 H_DSTBN#3 4

H_DSTBP#_0 L9 H_DSTBP#0 4
 H_DSTBP#_1 M8 H_DSTBP#1 4
 H_DSTBP#_2 AA6 H_DSTBP#2 4
 H_DSTBP#_3 AE5 H_DSTBP#3 4

H_REQ#_0 B15 H_REQ#0 3
 H_REQ#_1 K13 H_REQ#1 3
 H_REQ#_2 E13 H_REQ#2 3
 H_REQ#_3 B13 H_REQ#3 3
 H_REQ#_4 B14 H_REQ#4 3

H_RS#_0 B6 H_RS#0 3
 H_RS#_1 E12 H_RS#1 3
 H_RS#_2 C8 H_RS#2 3

MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2-> 1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/ DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

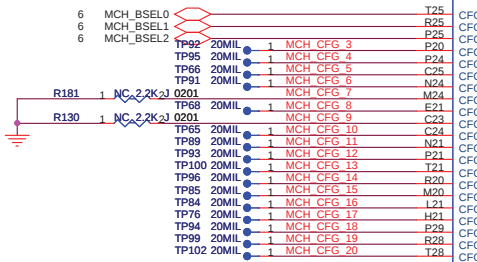
U32B

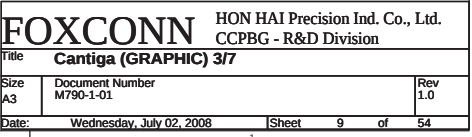
M36 M36 RESERVED_7
N36 N36 RESERVED_10
R33 R33 RESERVED_12
T33 T33 RESERVED_17
AH9 AH9 RESERVED_11
AH10 AH10 RESERVED_9
AH12 AH12 RESERVED_8
AH13 AH13 RESERVED_2
K12 K12 RESERVED_14
AL34 AL34 RESERVED_18
AK34 AK34 RESERVED_14
AN35 AN35 RESERVED_21
AM35 AM35 RESERVED_19
T24 T24 RESERVED_13

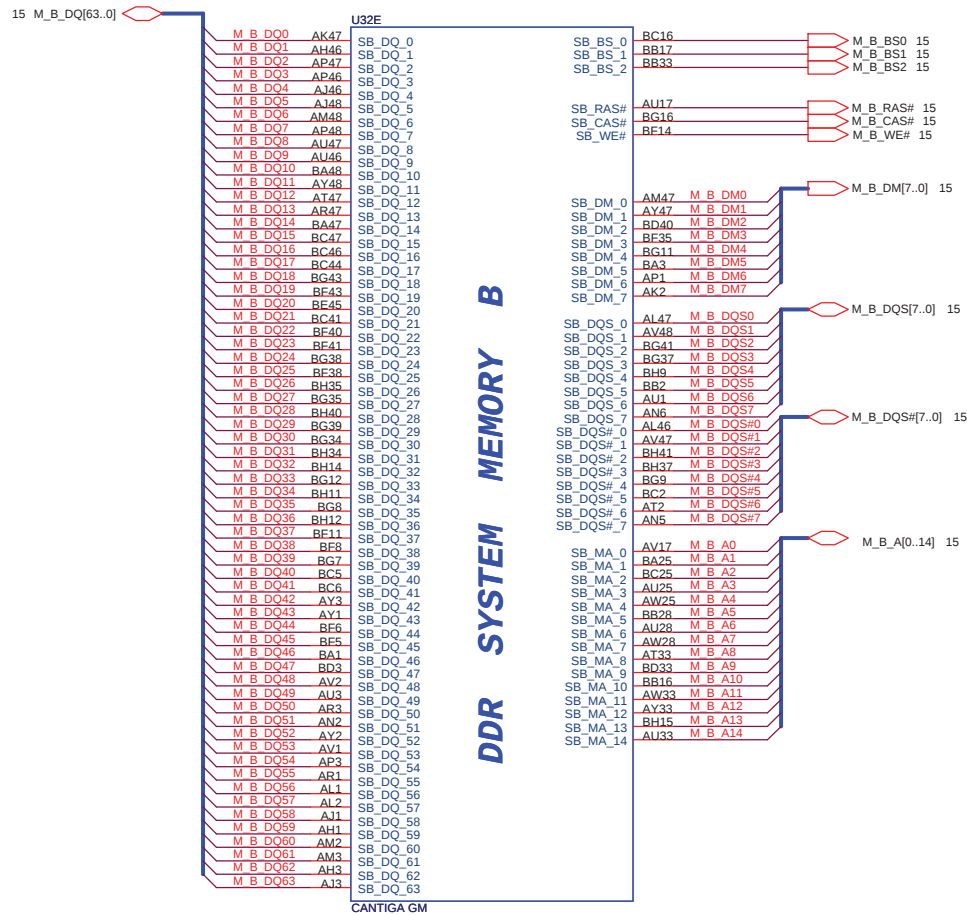
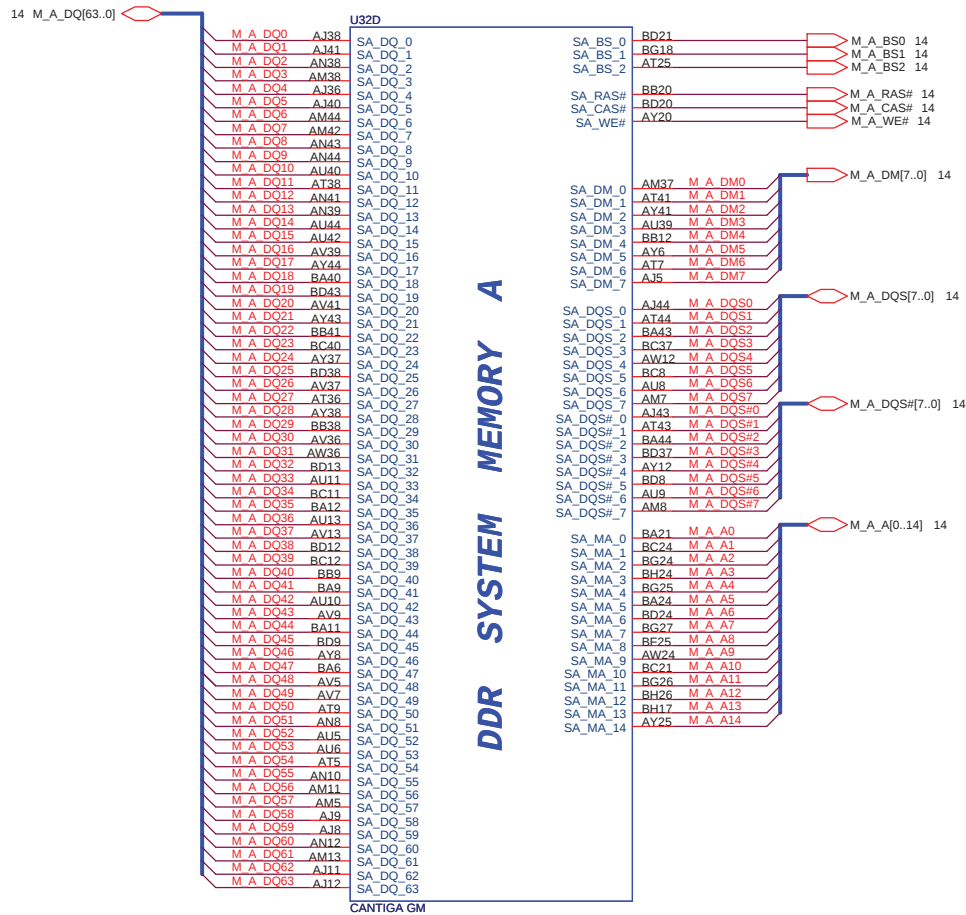
B31 B31 RESERVED_4
B2 B2 RESERVED_3
M1 M1 RESERVED_6

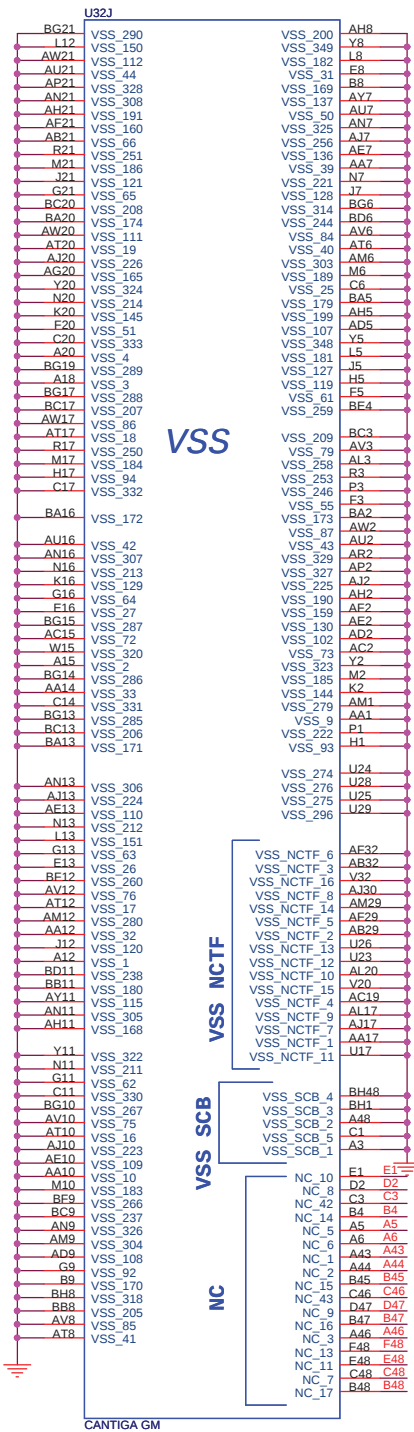
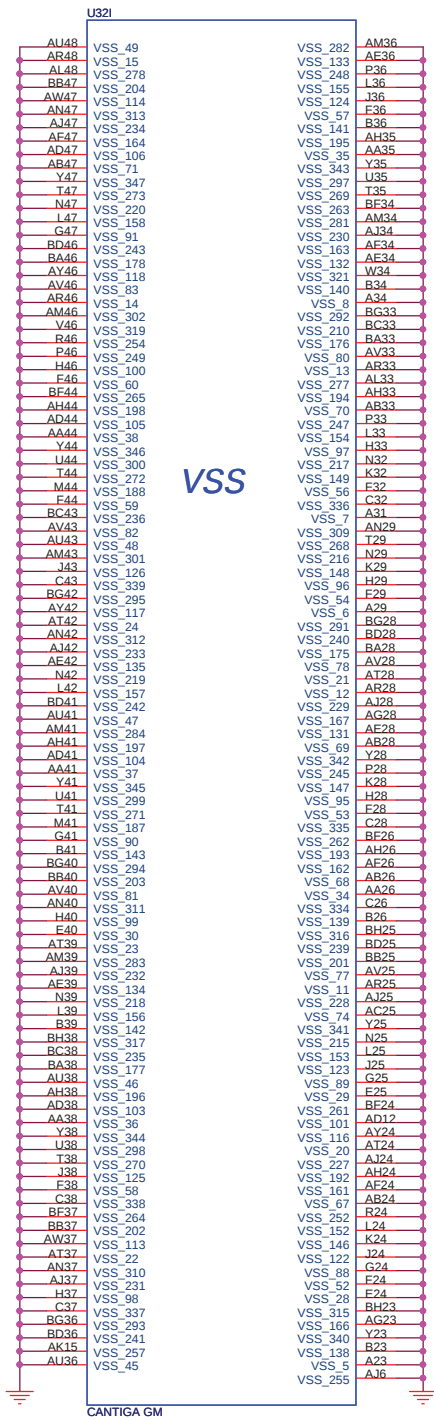
AY21 AY21 RESERVED_1

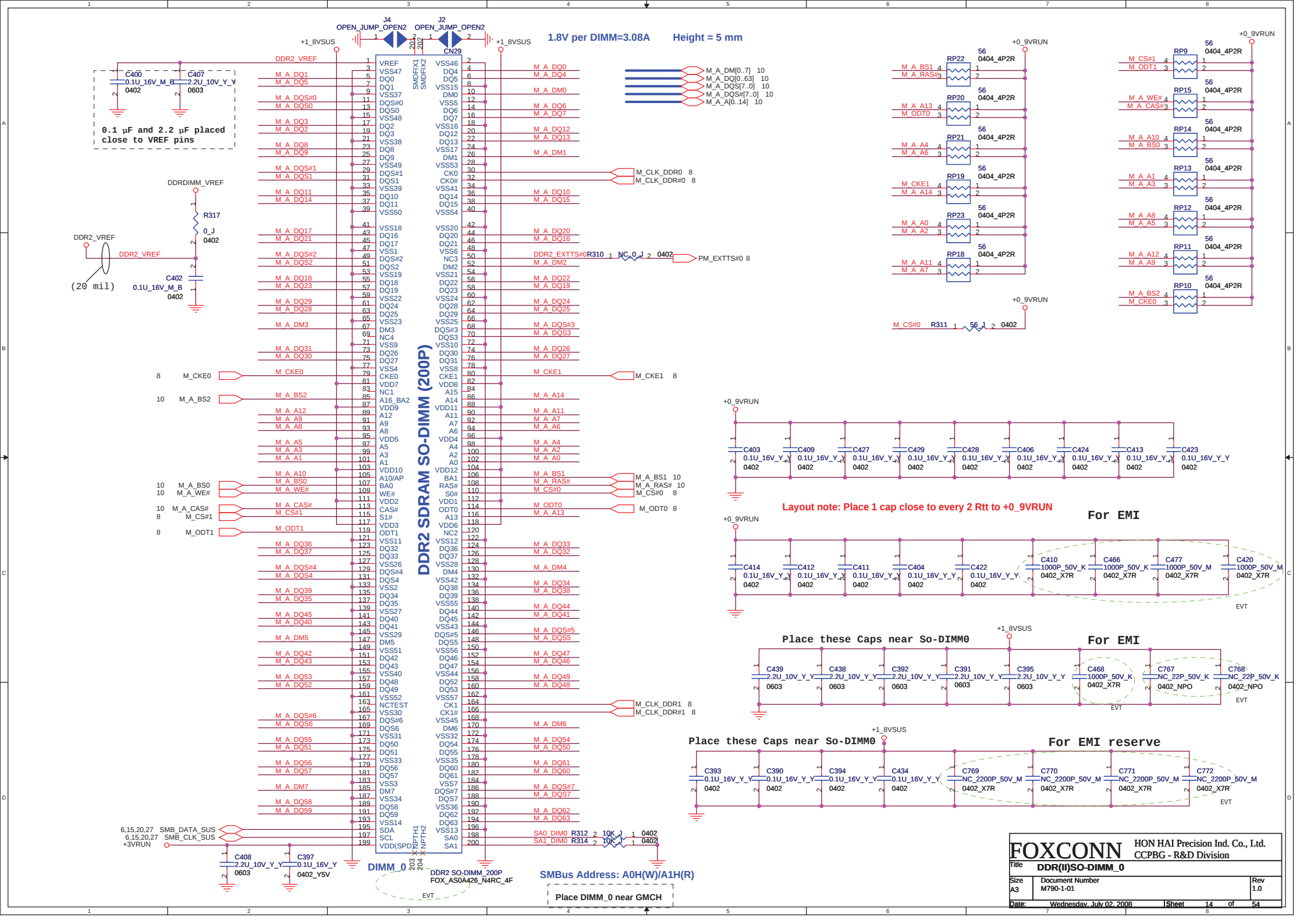
BG23 BG23 RESERVED_20
BF23 BF23 RESERVED_16
BH18 BH18 RESERVED_22
BF18 BF18 RESERVED_15

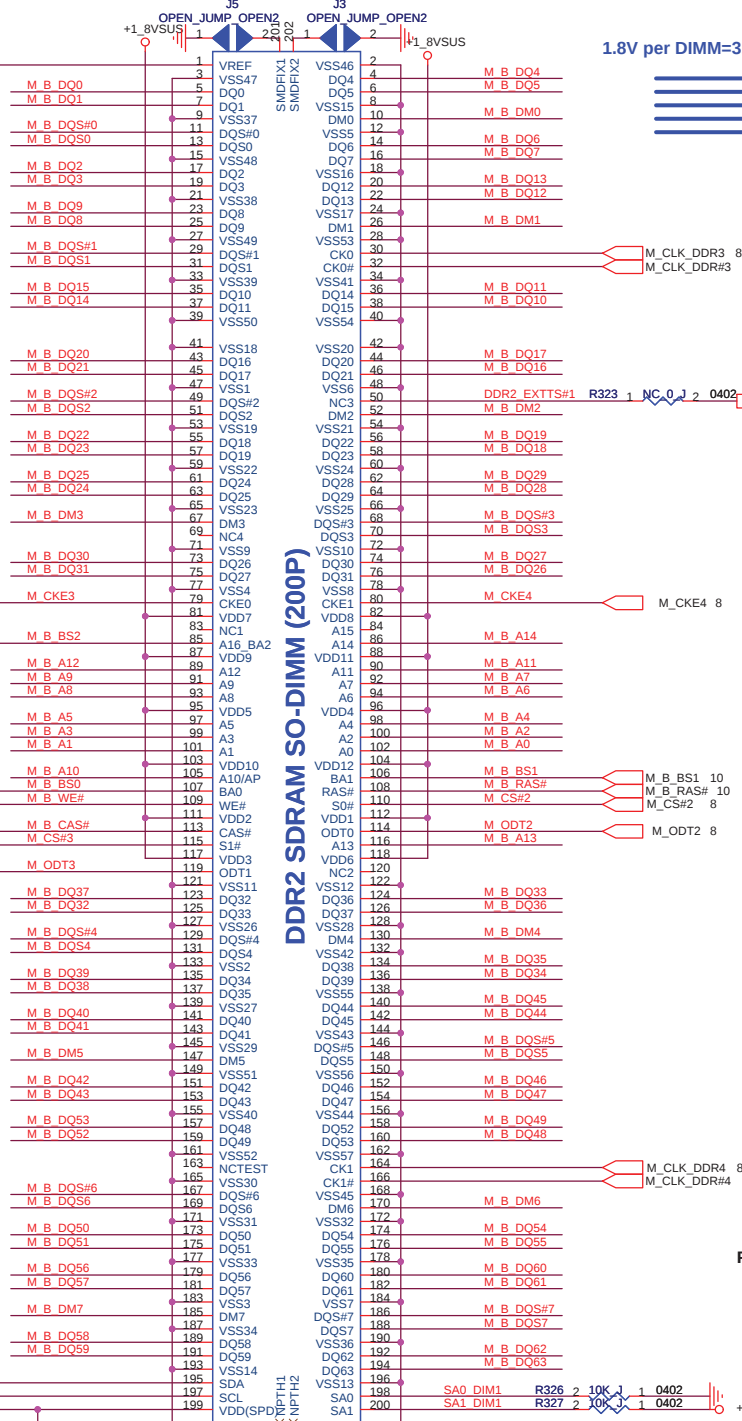
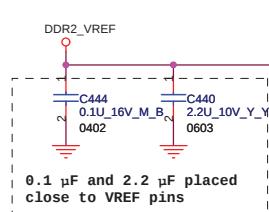




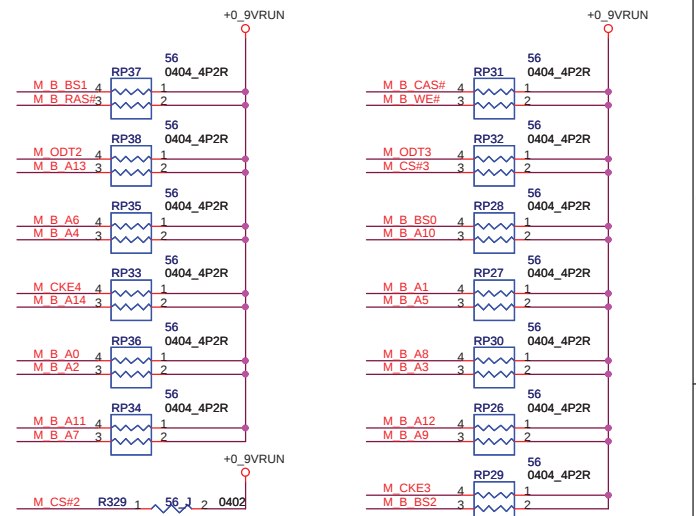
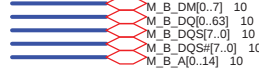






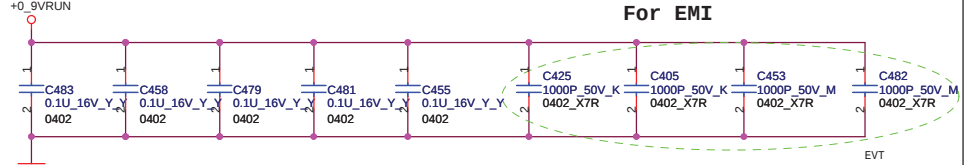


1.8V per DIMM=3.08A Height = 4 mm



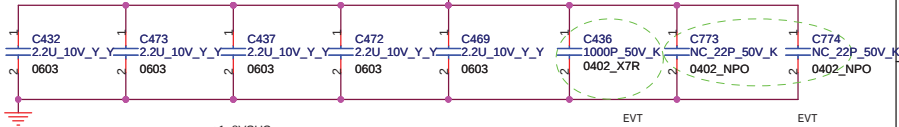
Layout note: Place 1 cap close to every 2R_{tt} to +0.9VVRUN

For EMI



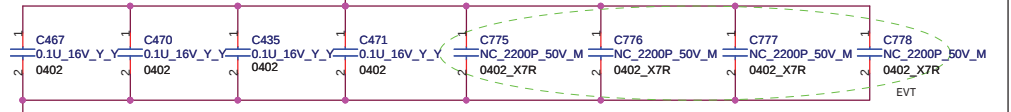
Place these Caps near So-DIMM1.

For EMI



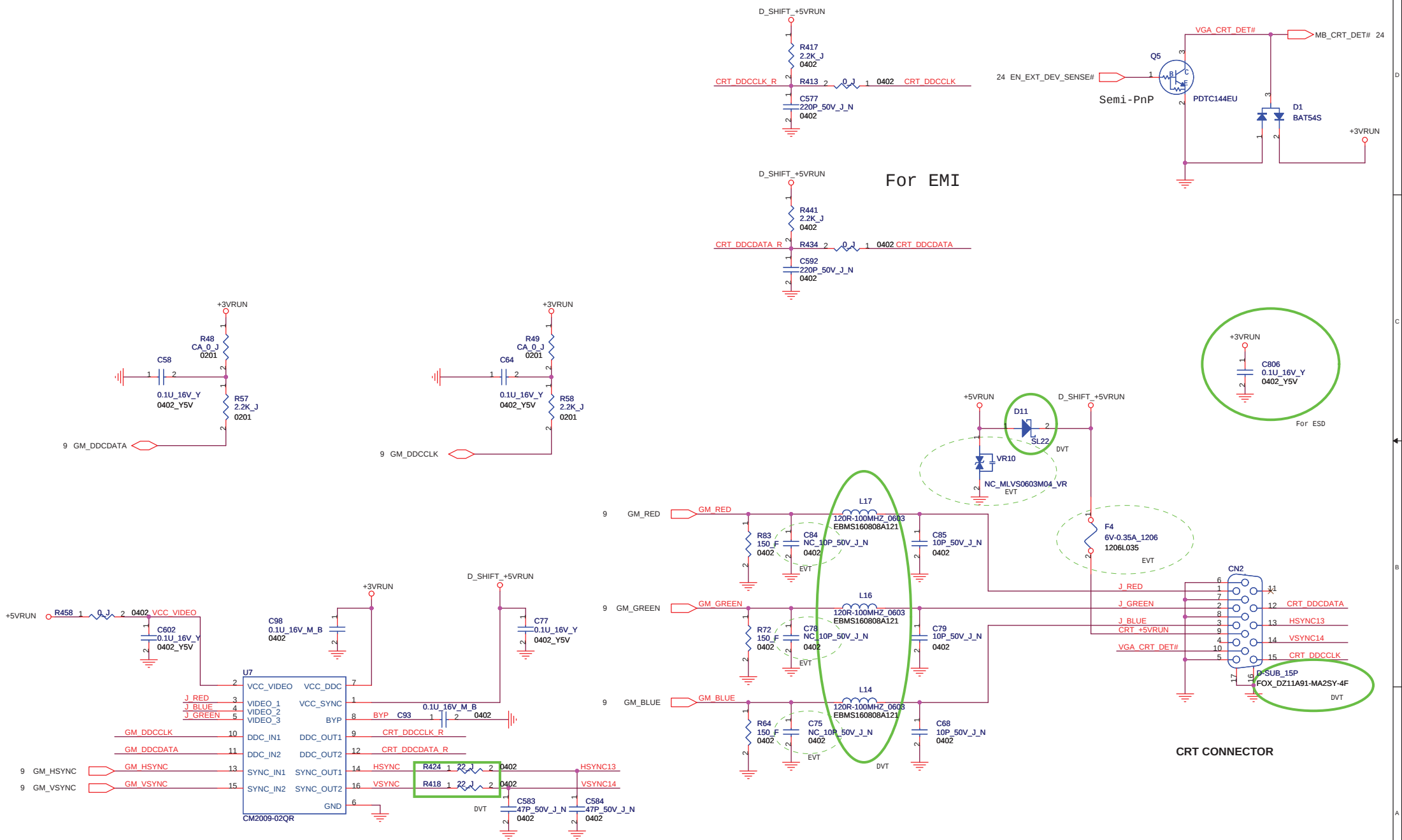
Place these Caps near So-DIMM1.

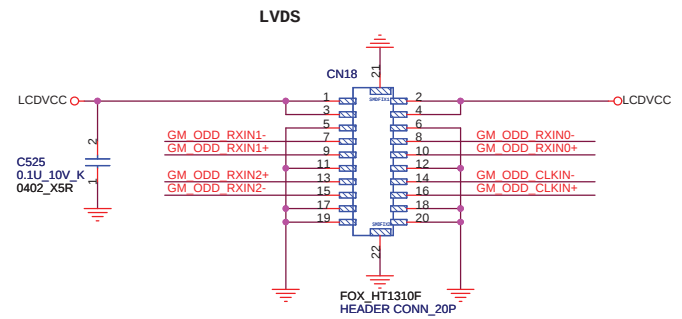
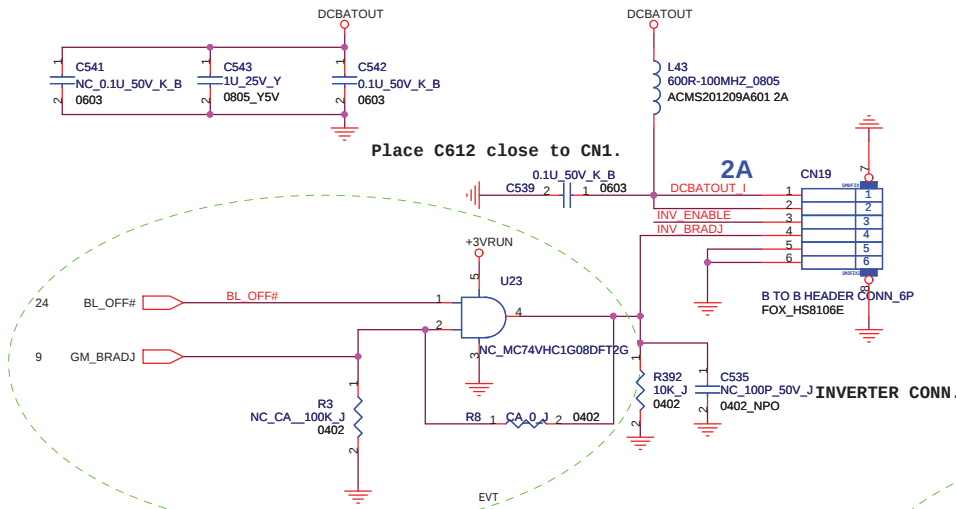
For EMI reserve



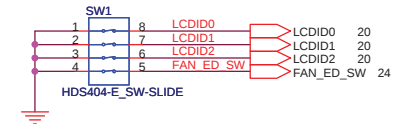
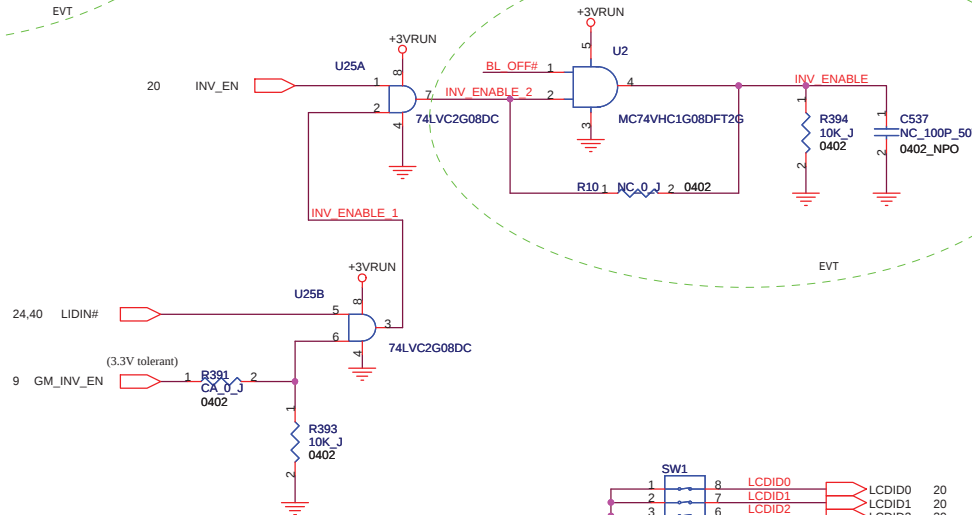
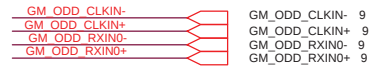
SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0



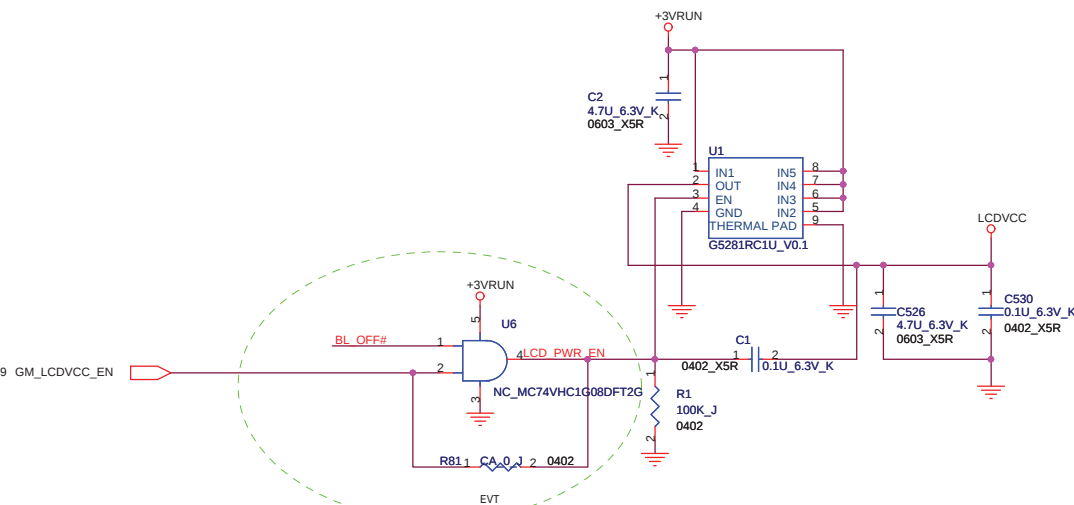


LVDS

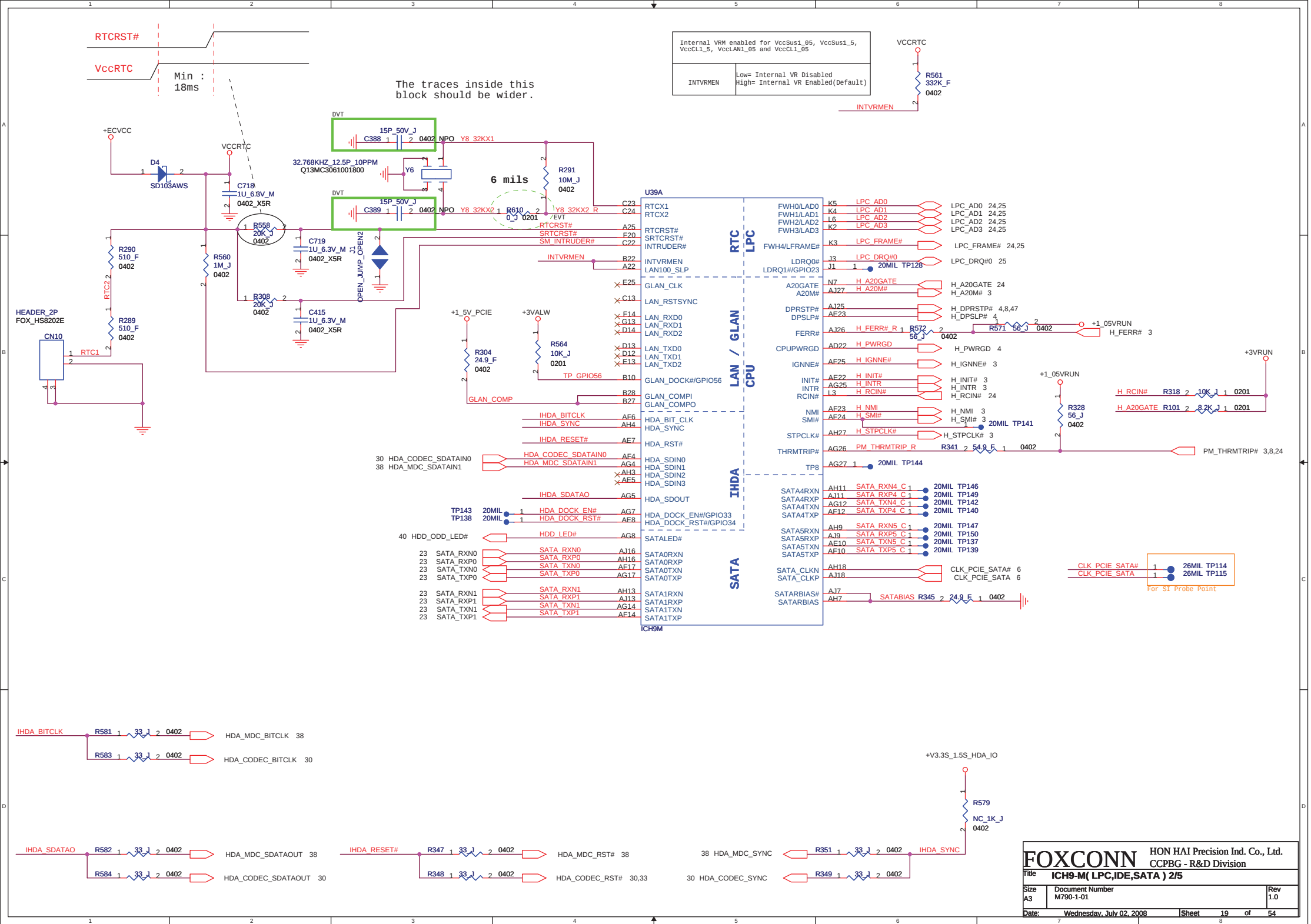


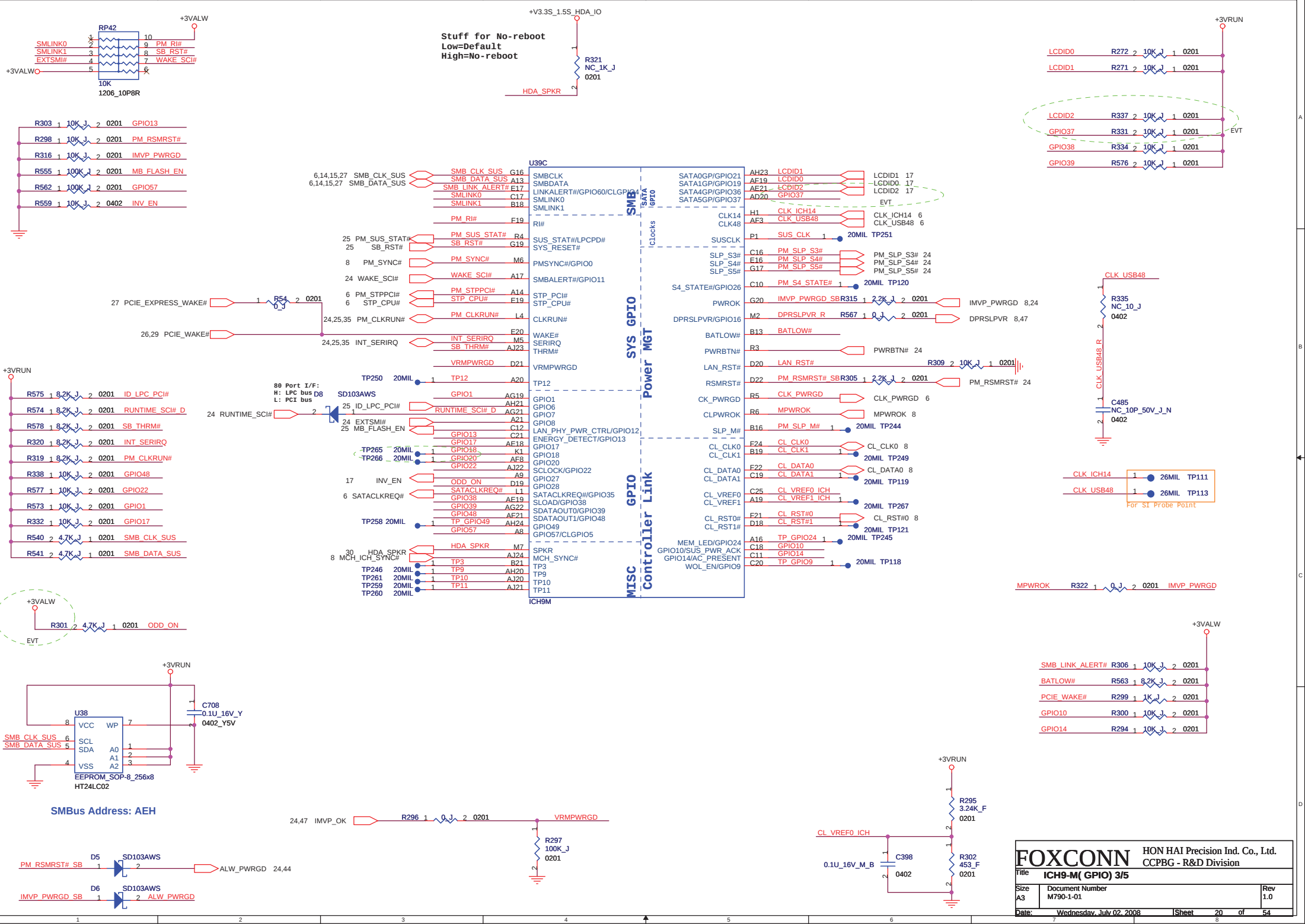
PANEL ID

Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vendor	At0	CPT	LPL	LPL
Device Name	B154EW02V7	CLAA154WB03	LP154WX4-TLC5	LP154WX5-TLA1
Panel ID [3..0]	001	010	011	100

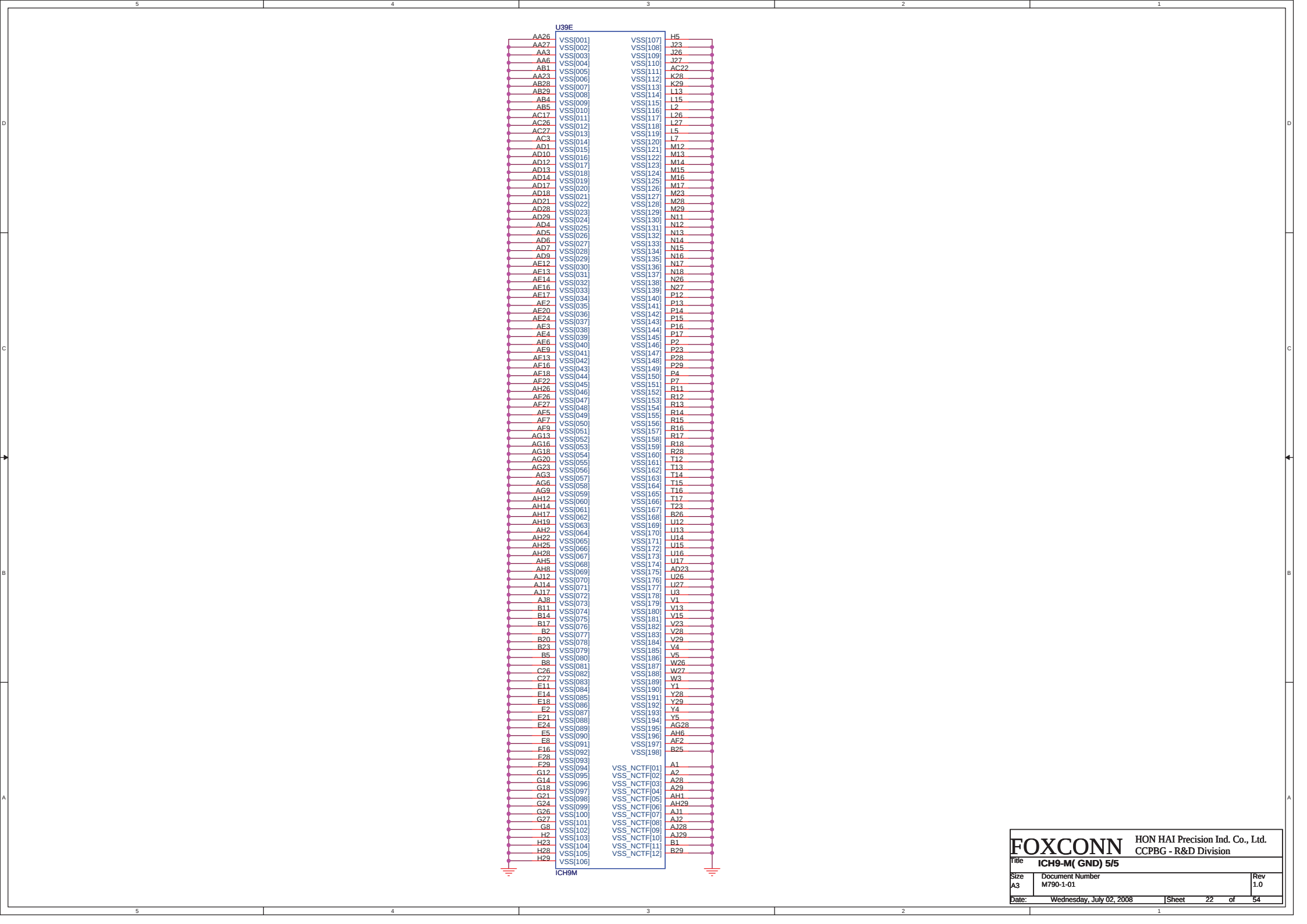




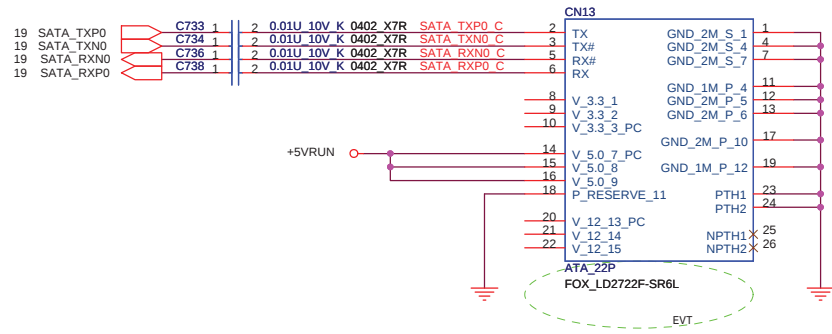
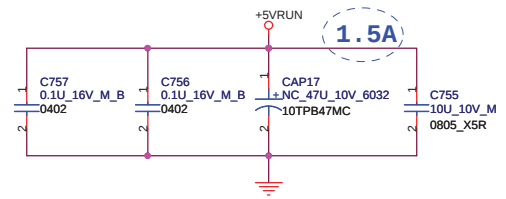




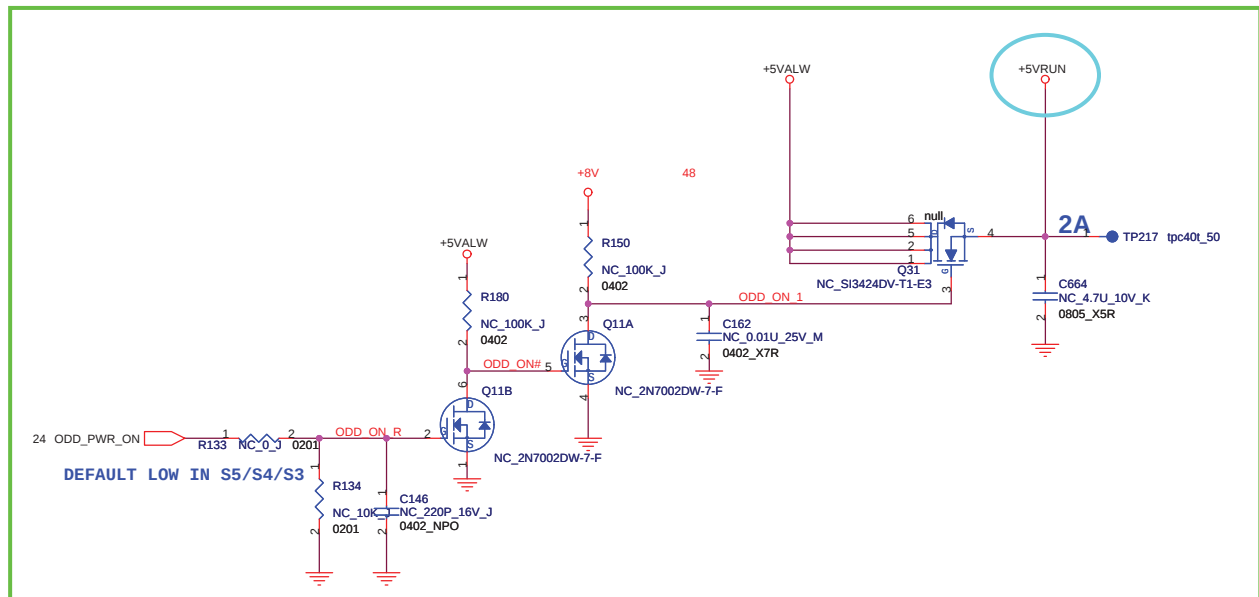
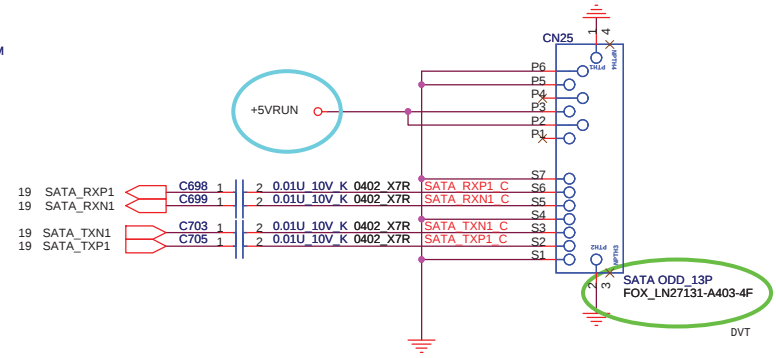
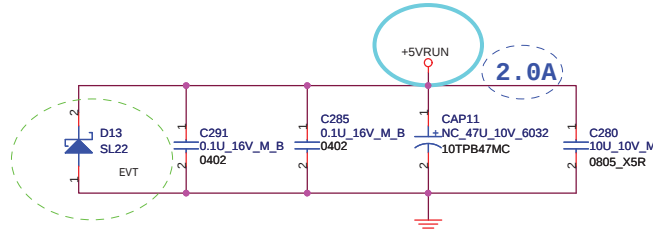


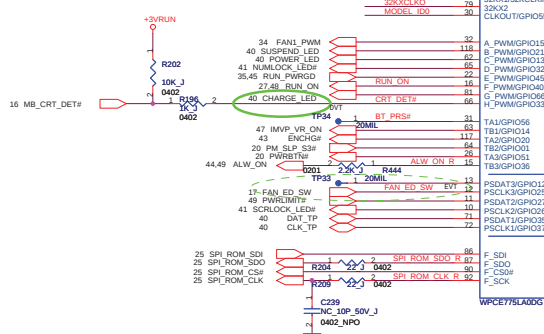
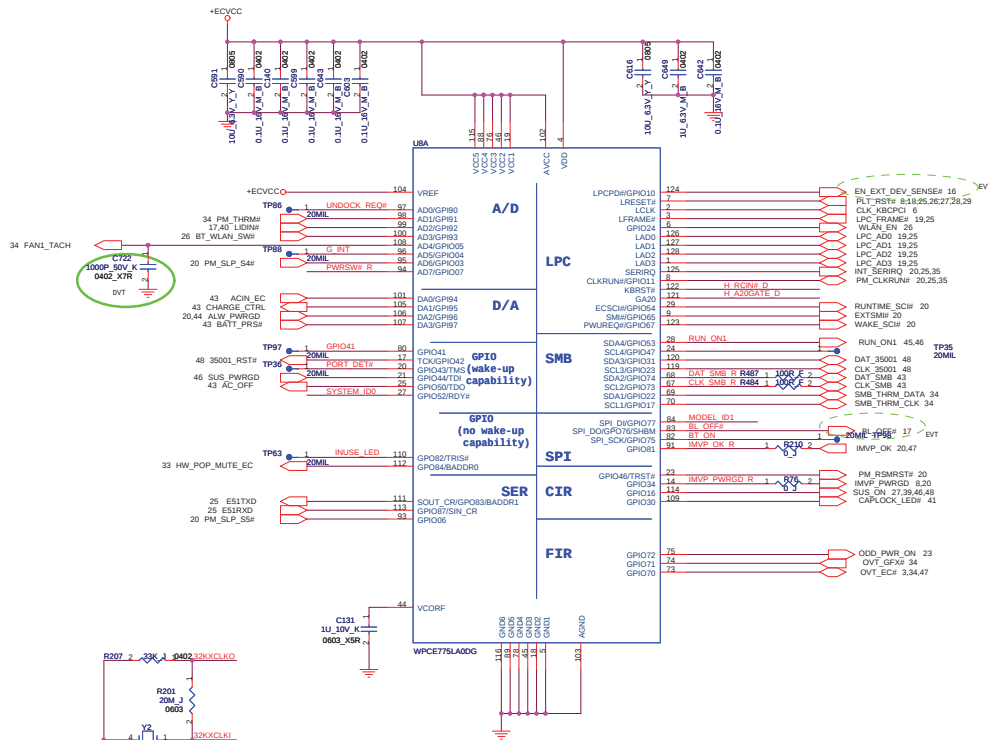
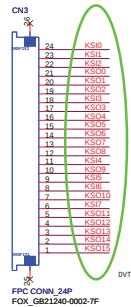


SATA HDD CONN

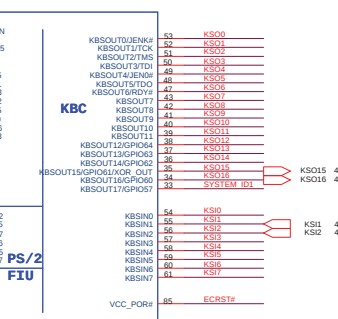
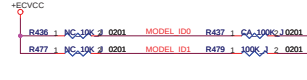


SATA ODD CONN

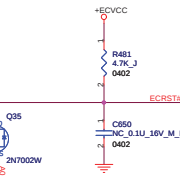
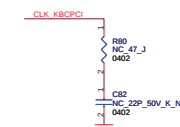
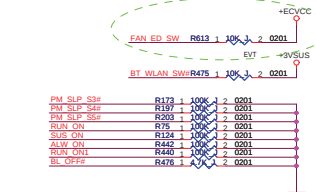
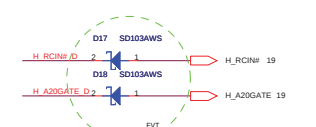
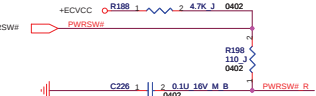
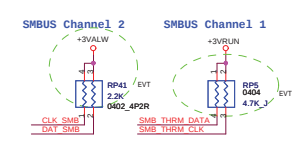
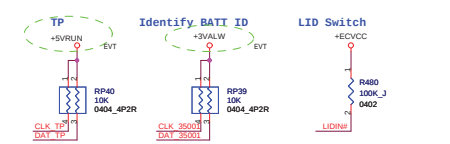
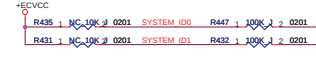


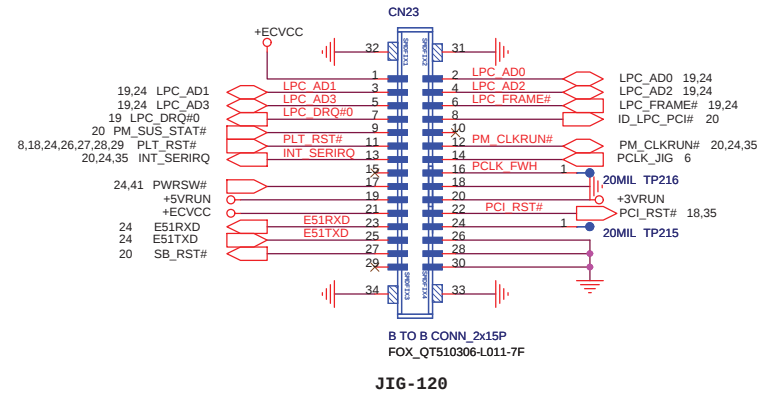
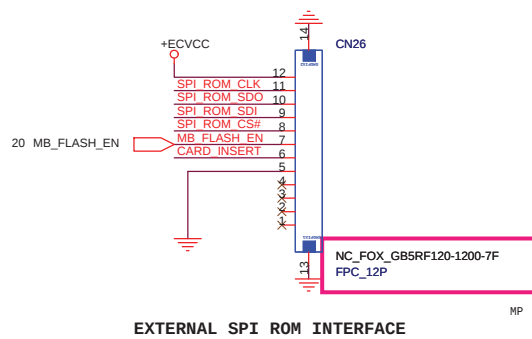
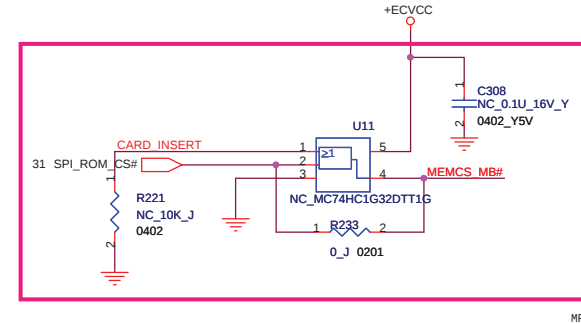
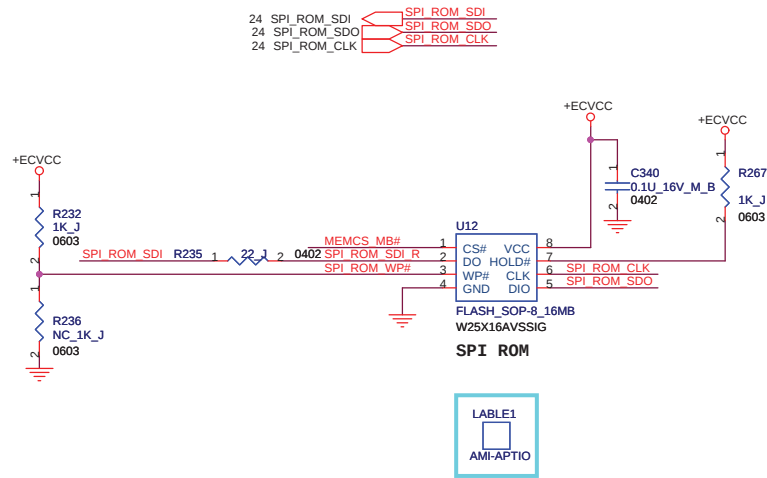


ID1	ID0	Sku
0	0	C09N-H
0	1	C09N-H



ID1	ID0	Sku
0	0	M790



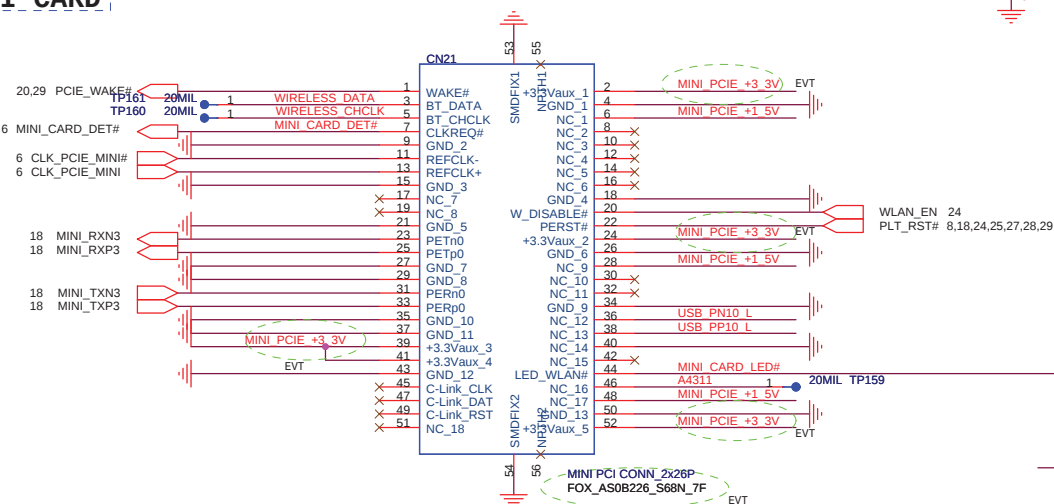
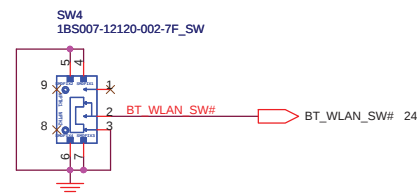




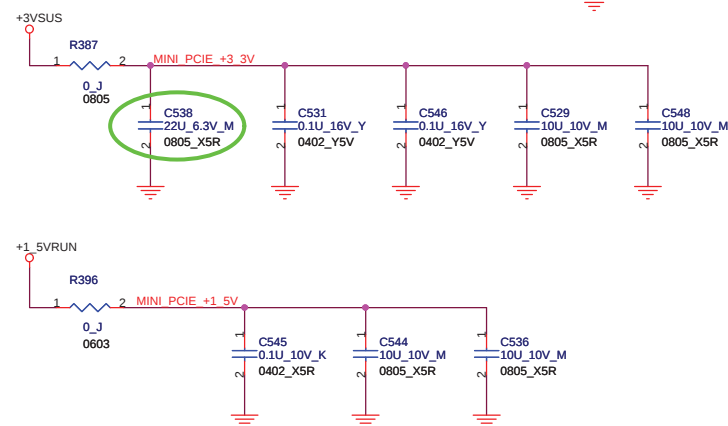
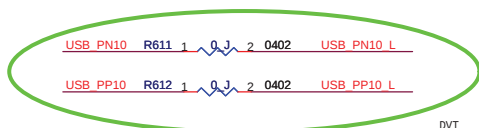
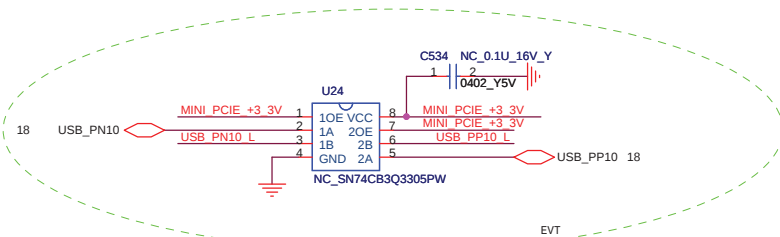
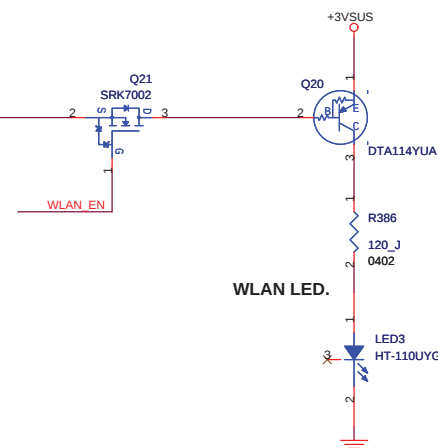
MINI CARD

+1.5V=>0.5A Peak/0.375A Normal
+3.3VAux=>2.75A Peak/1.1A Normal

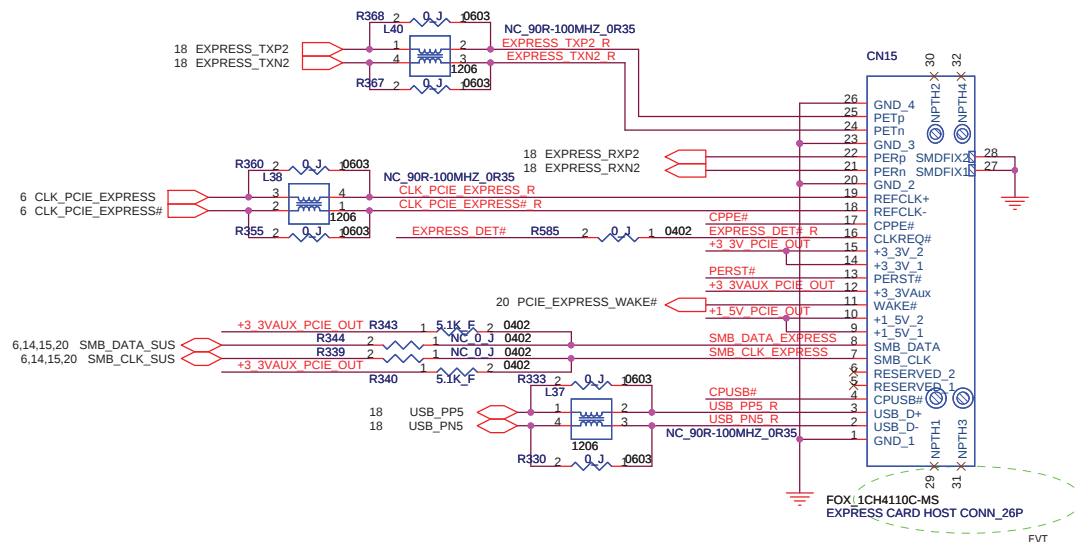
WLAN ON/OFF Switch



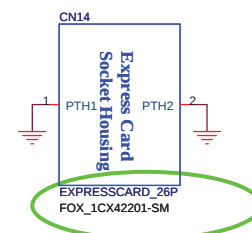
Mini Card. WLAN

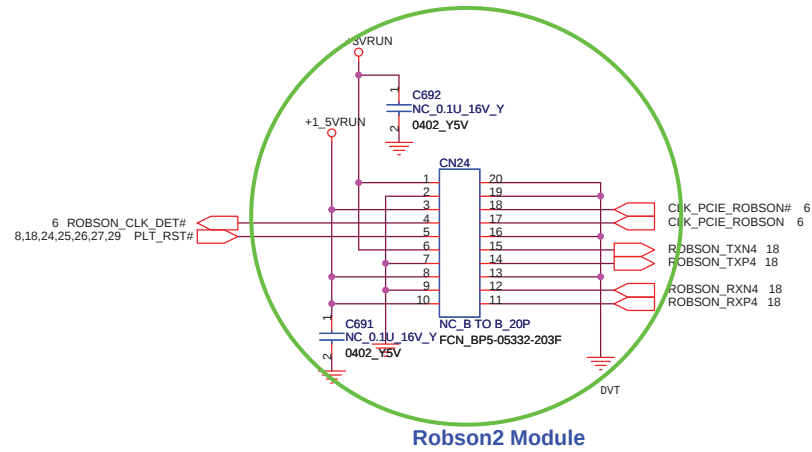


Express Card Power Switch

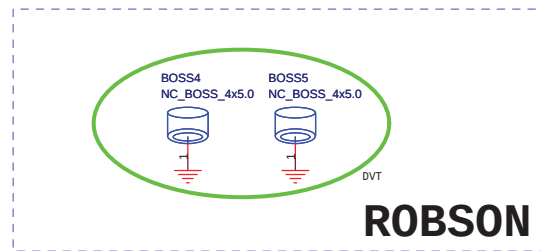


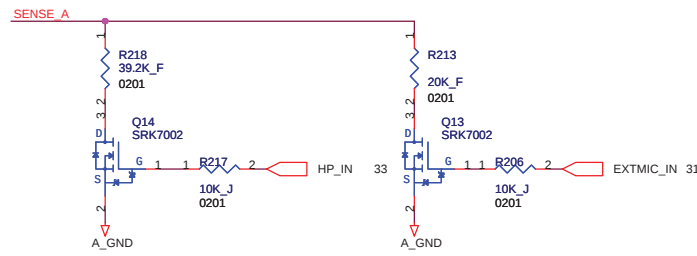
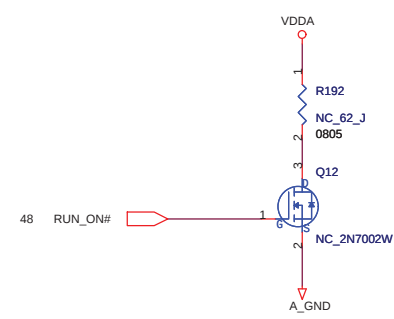
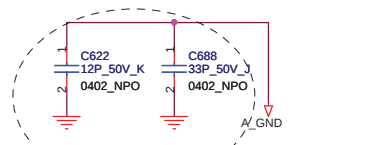
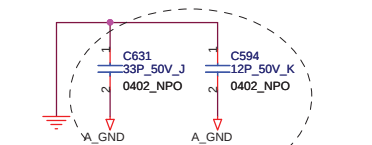
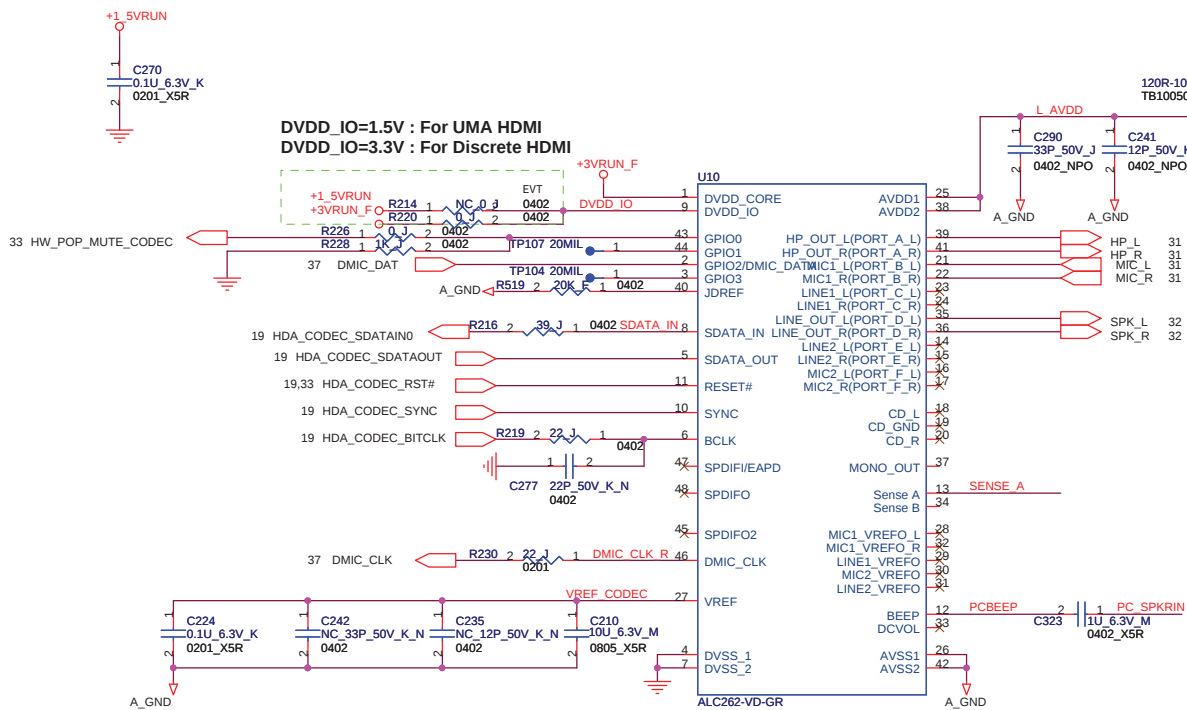
Express Card Slot.



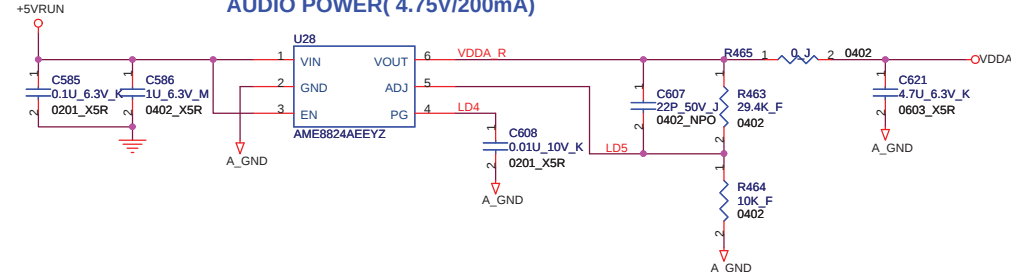


EVT2 11/6 Need to update new connector.

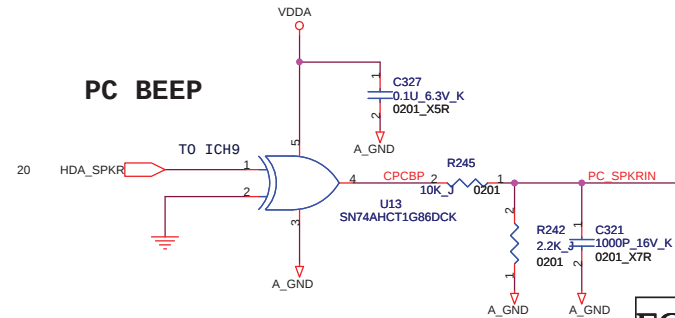


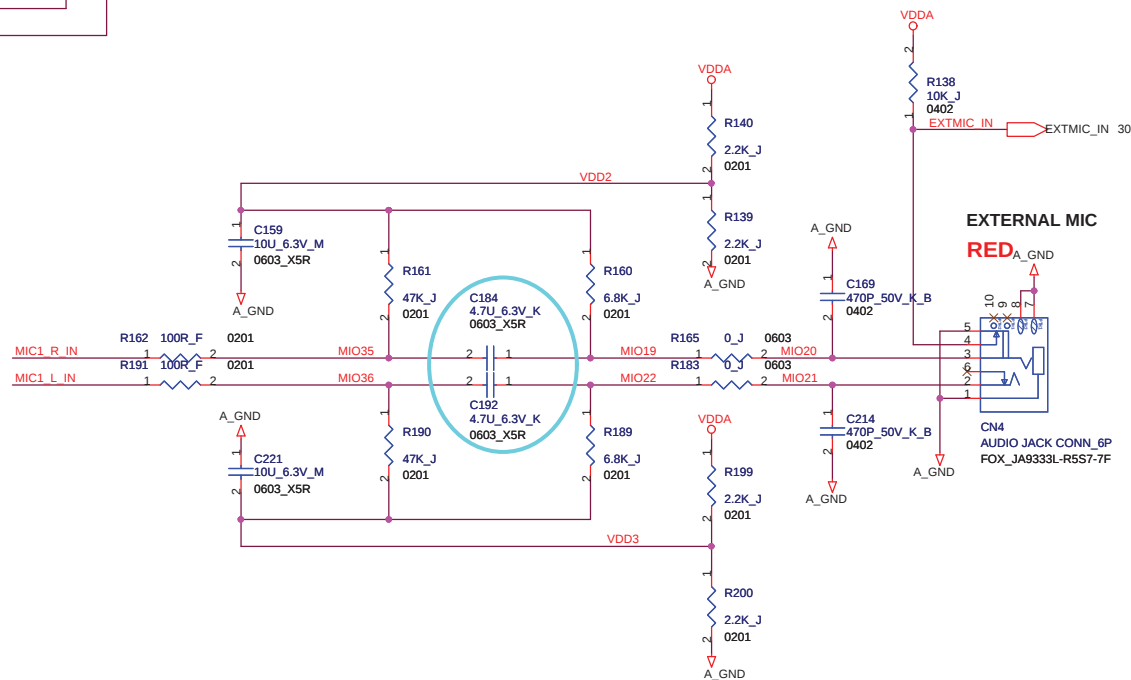
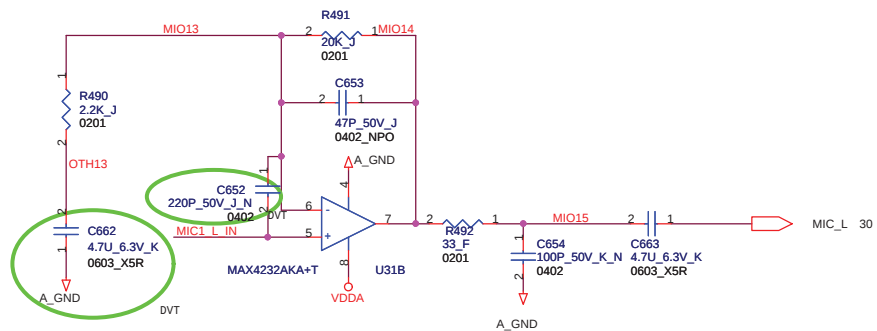
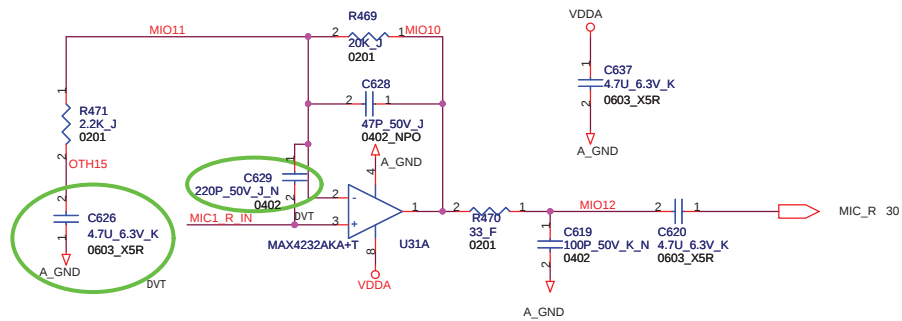
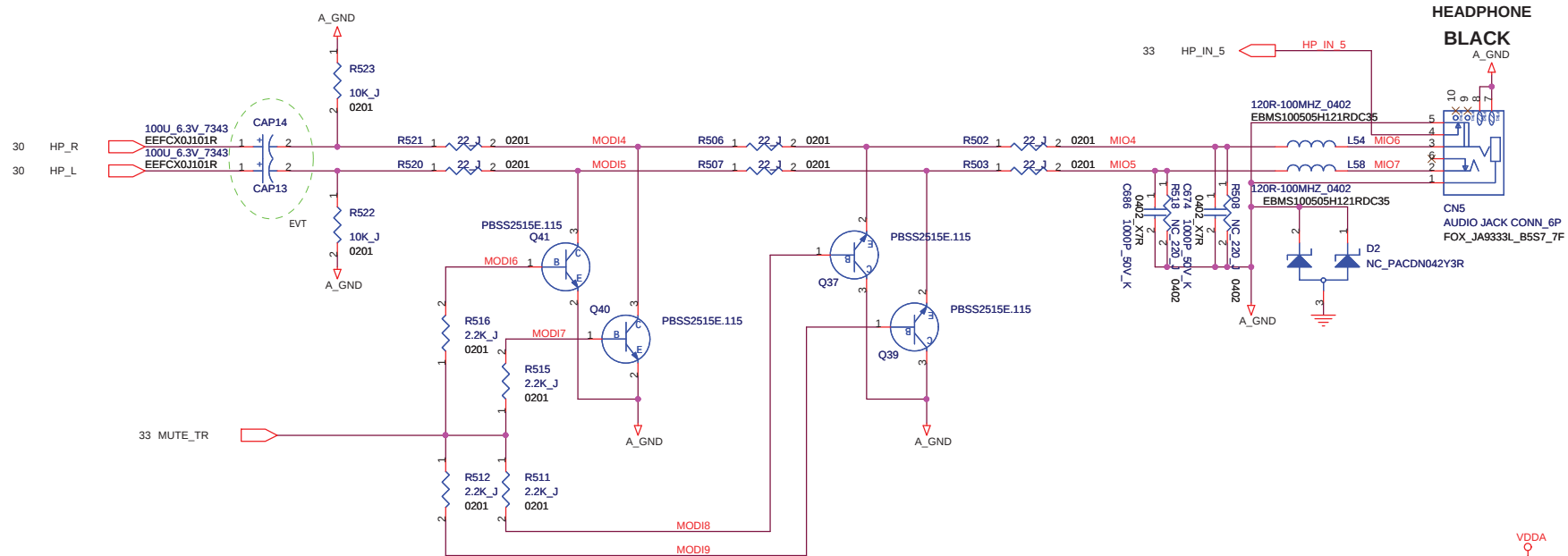


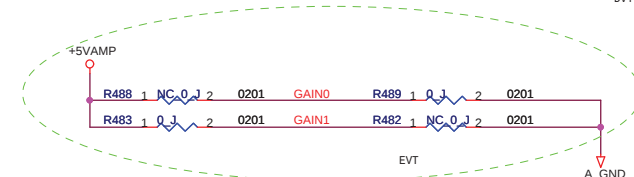
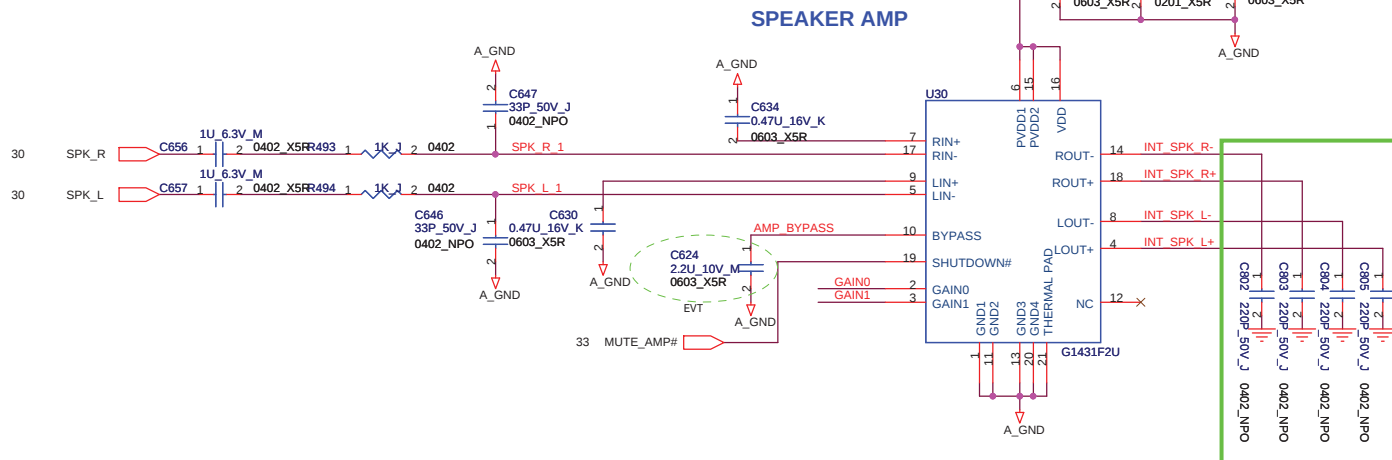
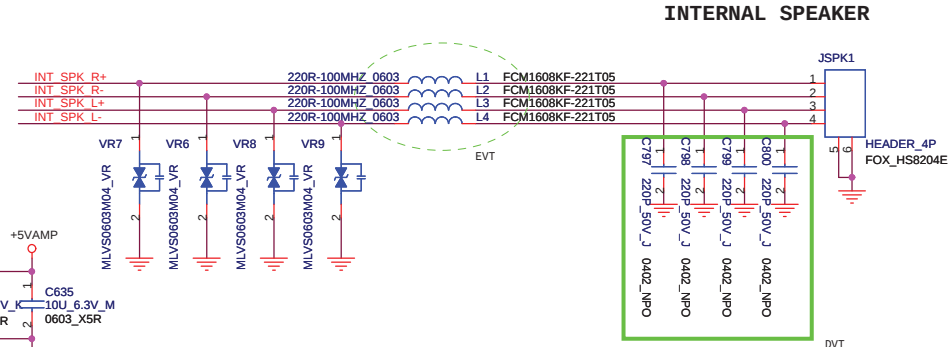
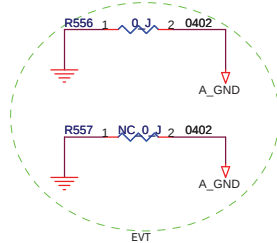
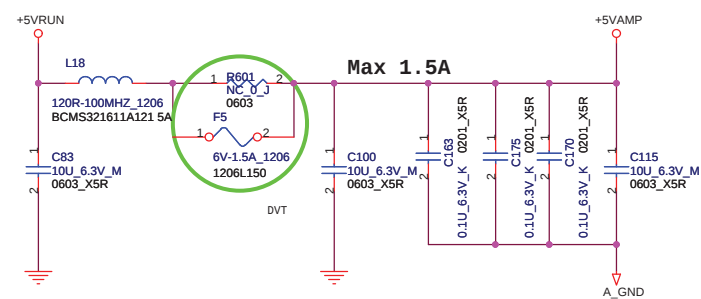
AUDIO POWER(4.75V/200mA)



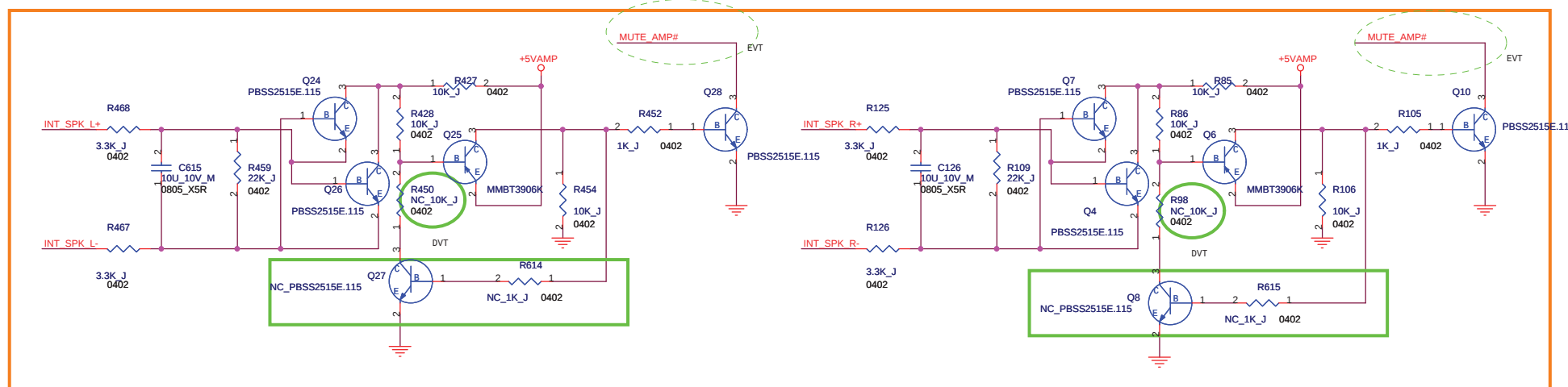
PC BEEP



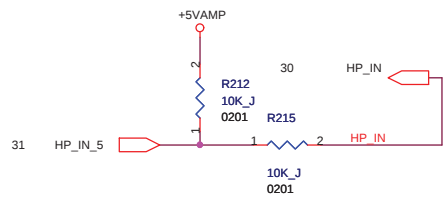




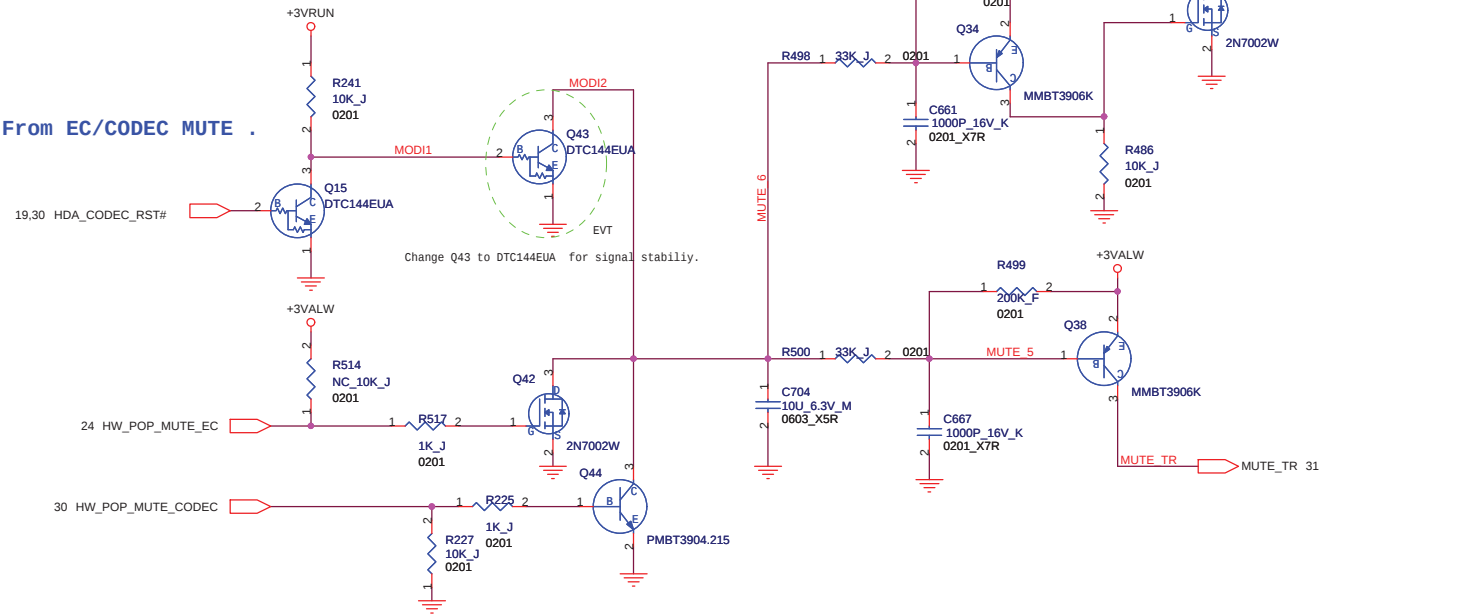
	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

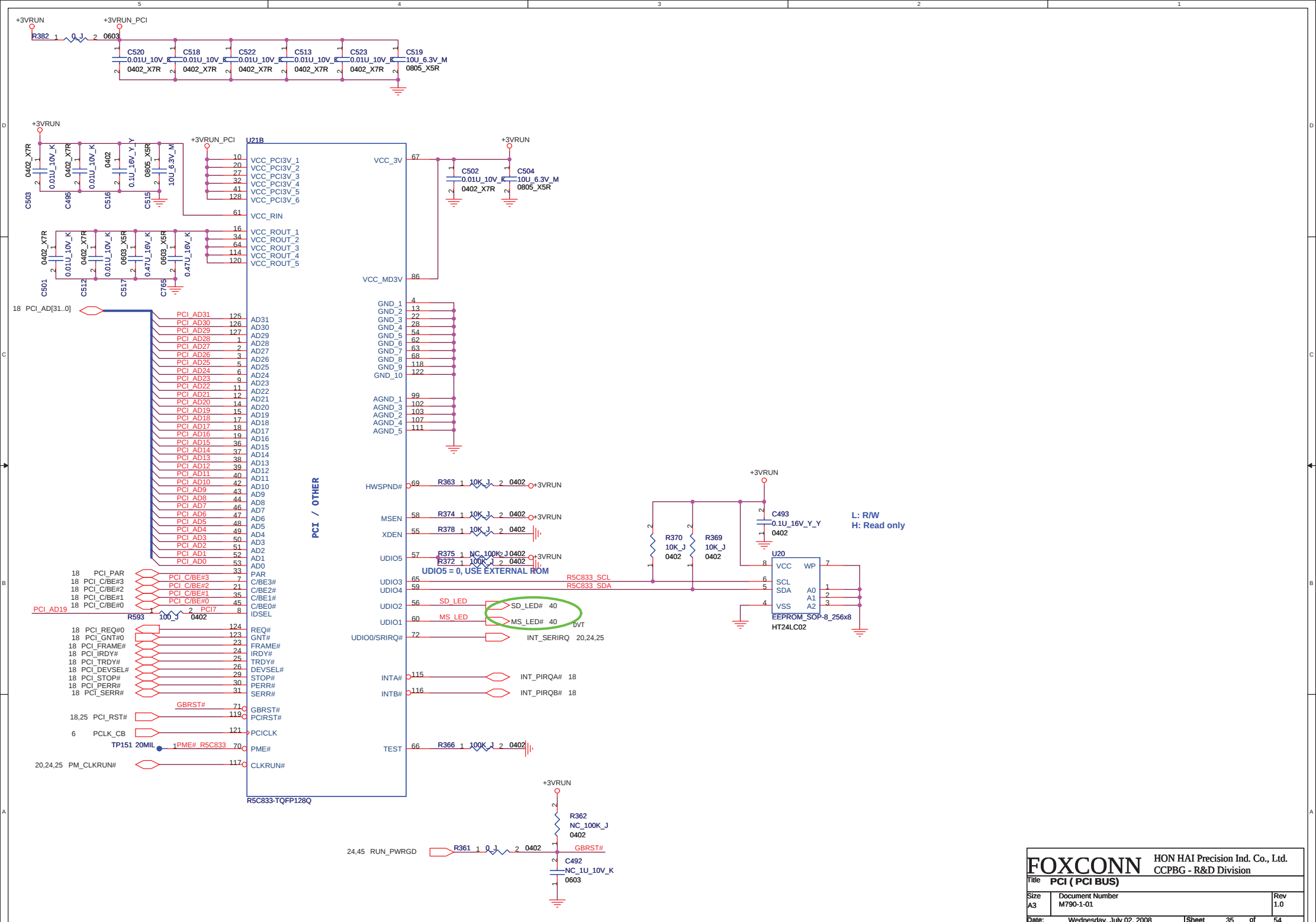


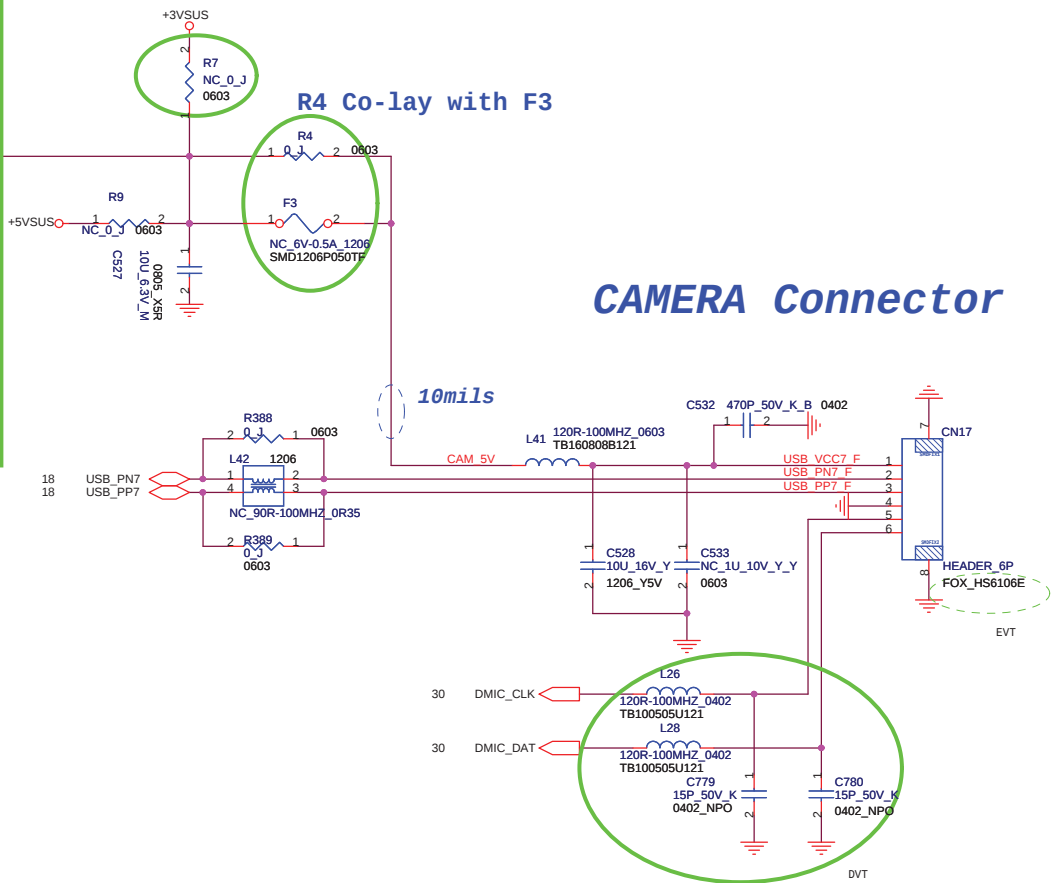
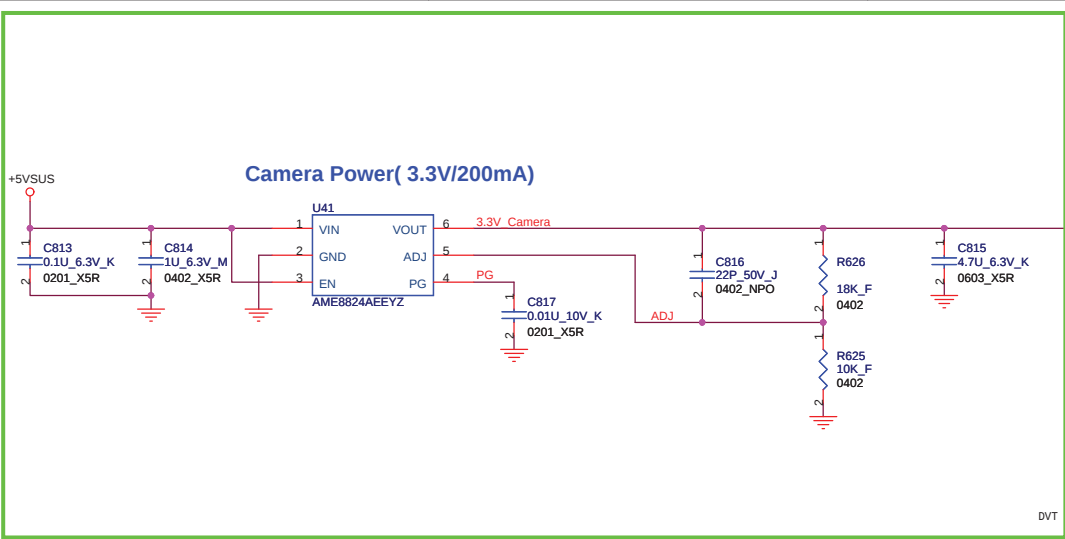
For Mor request,add the speaker cable short protection circuit

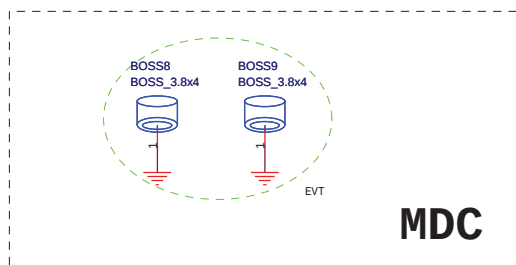
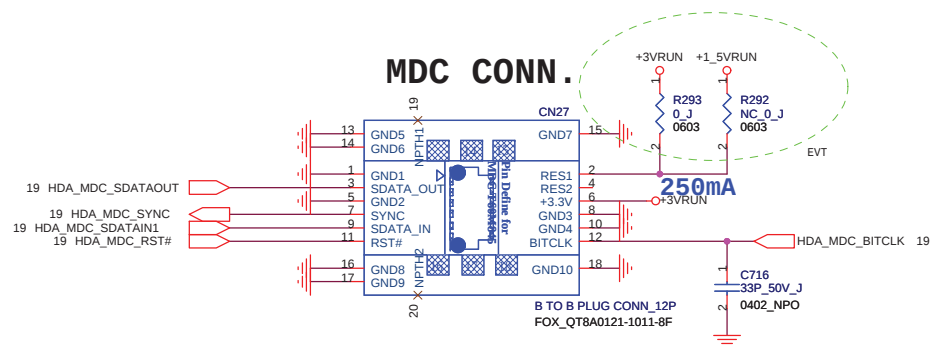
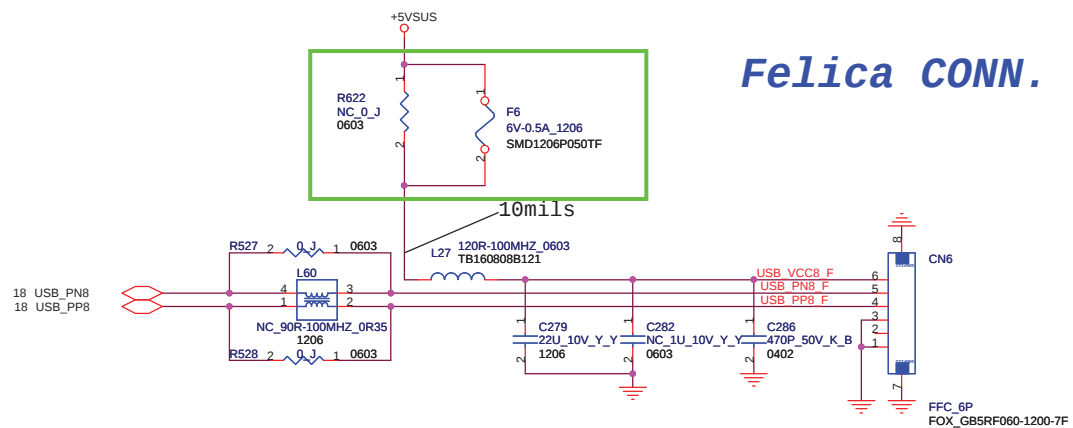


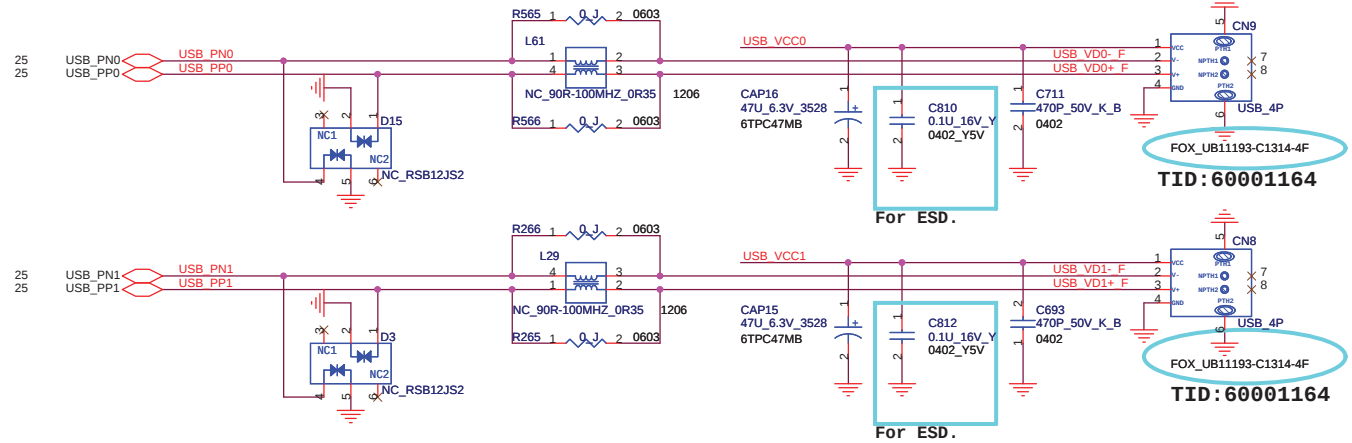
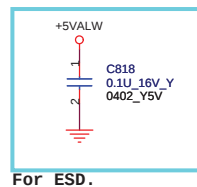
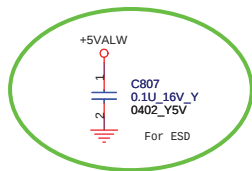
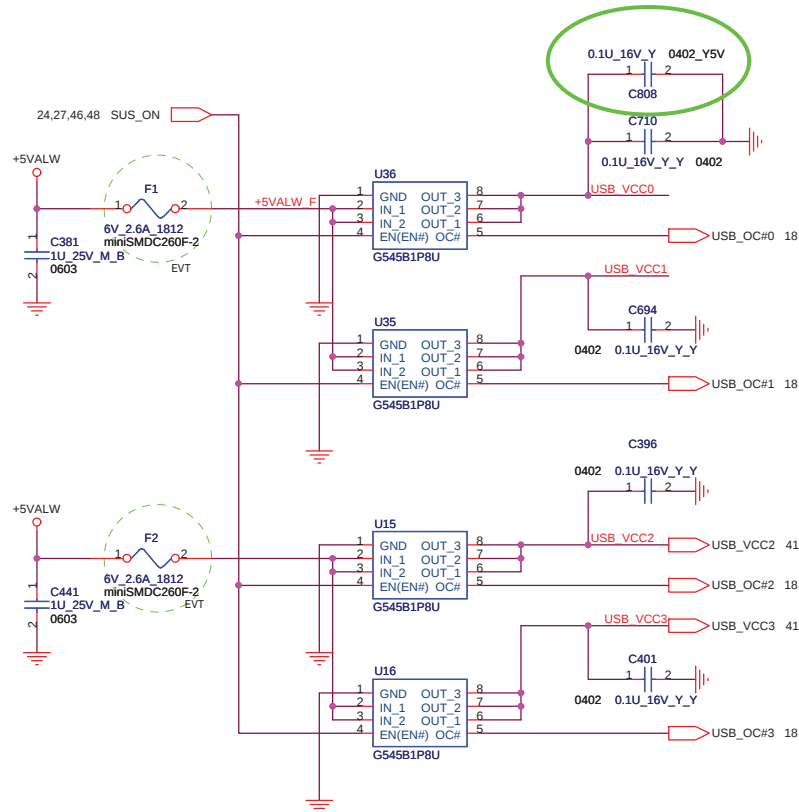
From EC/CODEC MUTE .

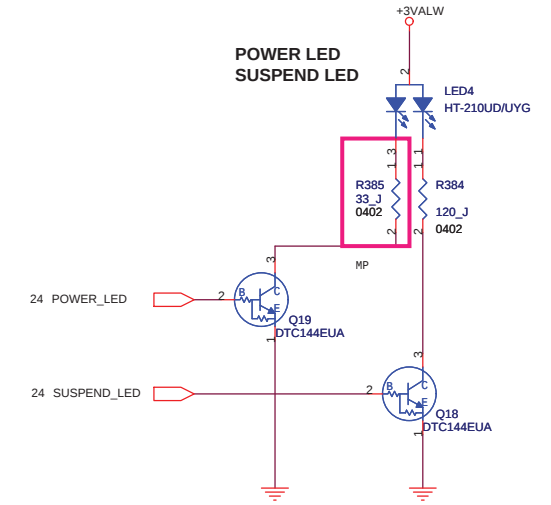
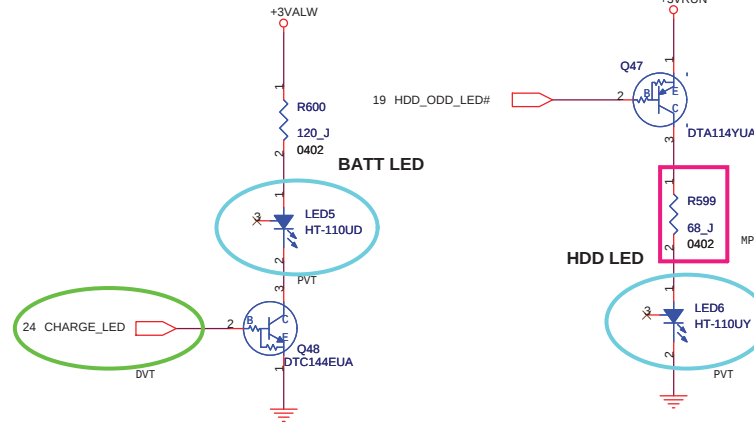
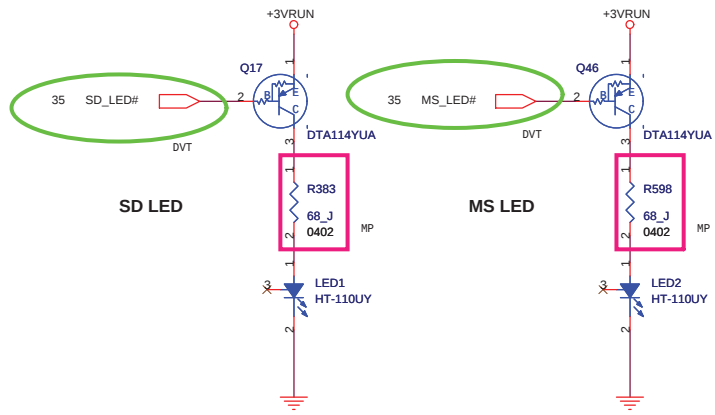




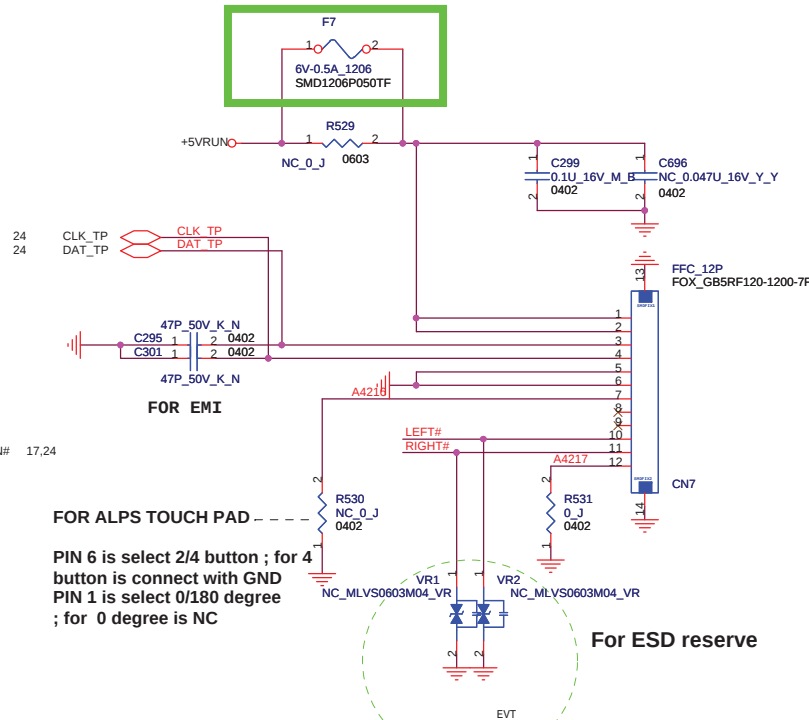
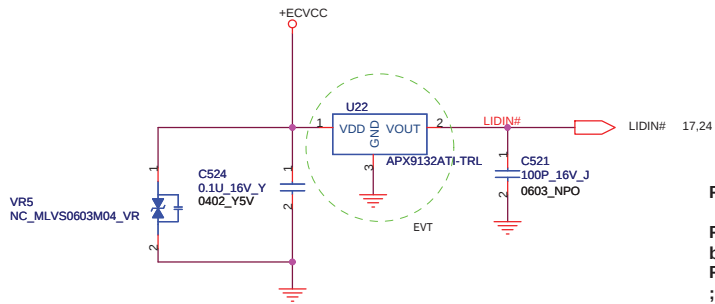




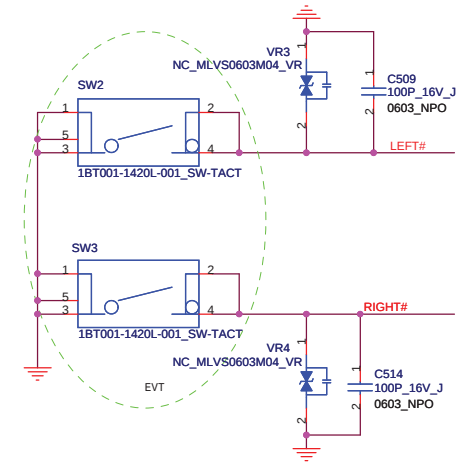




LID Switch

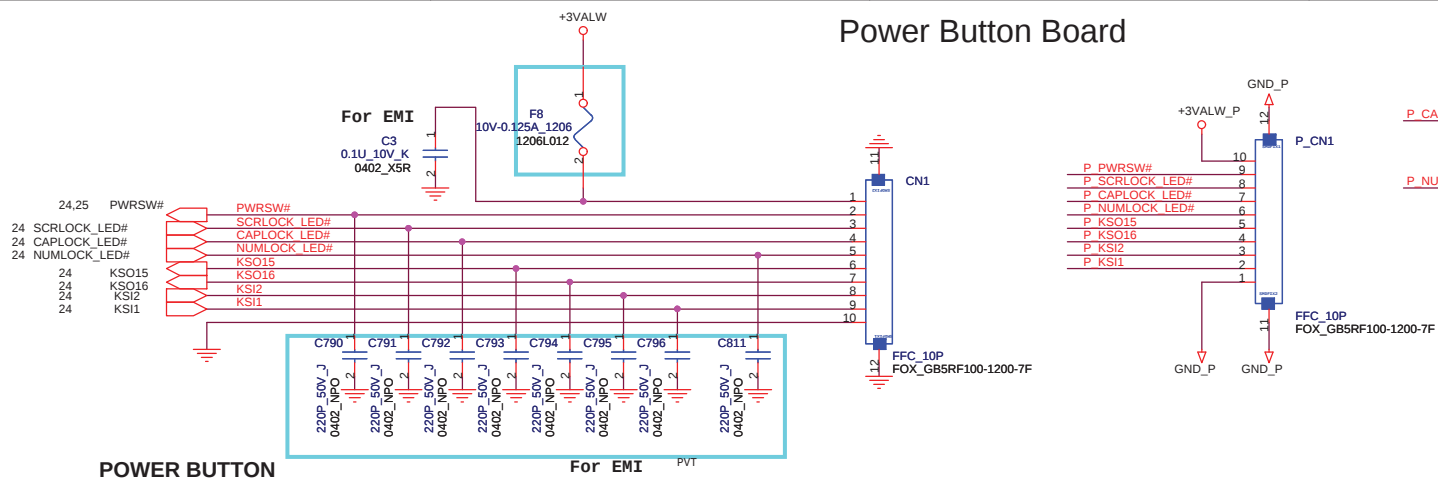


TP_LEFT Button



TP_Right Button

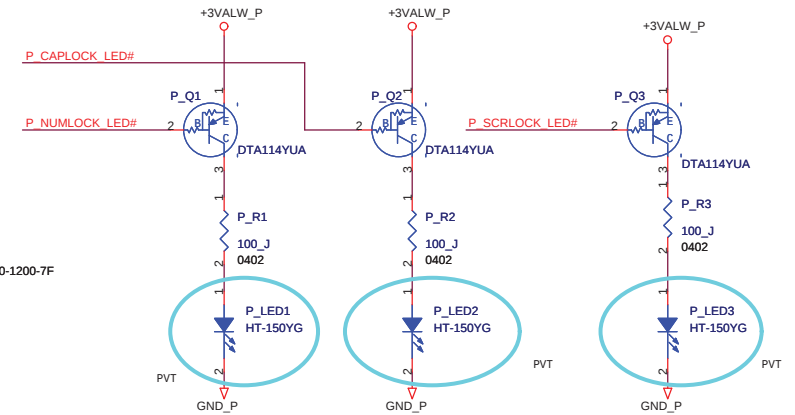
Power Button Board



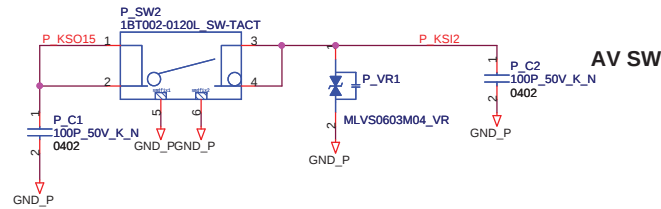
NUM LOCK LED

CAP LED

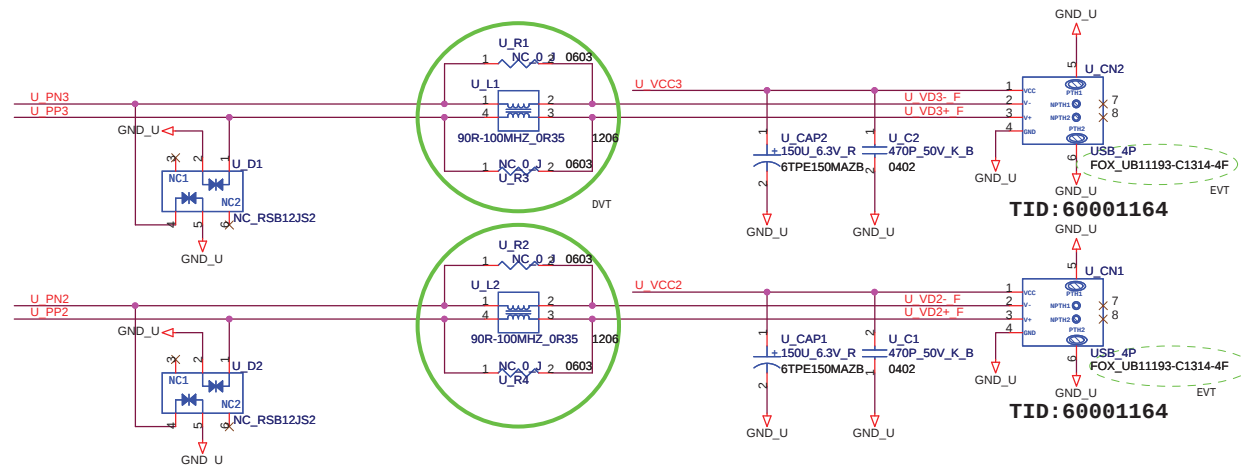
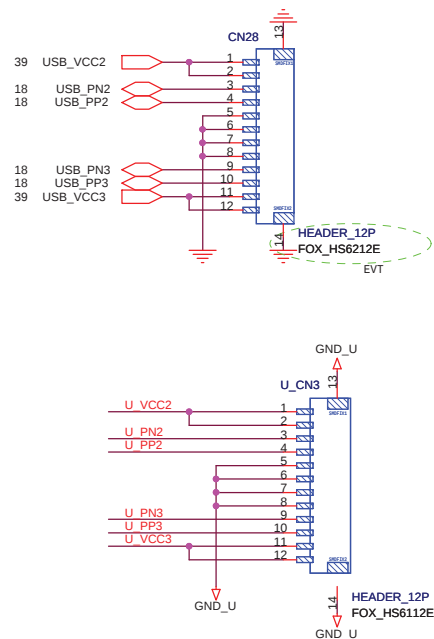
SCROLL LOCK LED



S1 SW

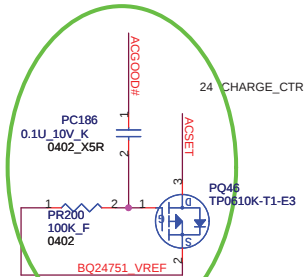


USB Board



charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF



VREF=3.3V --->Vdac
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR11) = 1.5A$
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR1) = 4.1A$
 $I_{ADAPT} = (V_{acp} - V_{vacn}) * 20$
 Input OCP: $(V_{acp} - V_{vacn})_{max} / PR2 = 100mV / 15m\Omega = 6.6A$
 Input OVP : 22.2V
 Input UVP : 17V
 Battery OCP : $I_{charge} * 145\%$
 Battery OVP : $V_{bat} * 104\%$
 Pre-charge : $< 2.9V / \text{cell} ==> I_{charge} / 8$
 Battery OTP : $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$
 Time that input current limit :
 $t = (C_{acop} * 2) / (18uA * V * (PVCC - ACN)) = 0.48s$

ENCHG# : Enable ==> L Disable ==> H	
ACGOOD# : Vacdet > 2.4V ==> L Vacdet < 2.4V ==> H	
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

ACP and ACN connections must be make using Kelvin-sense connections

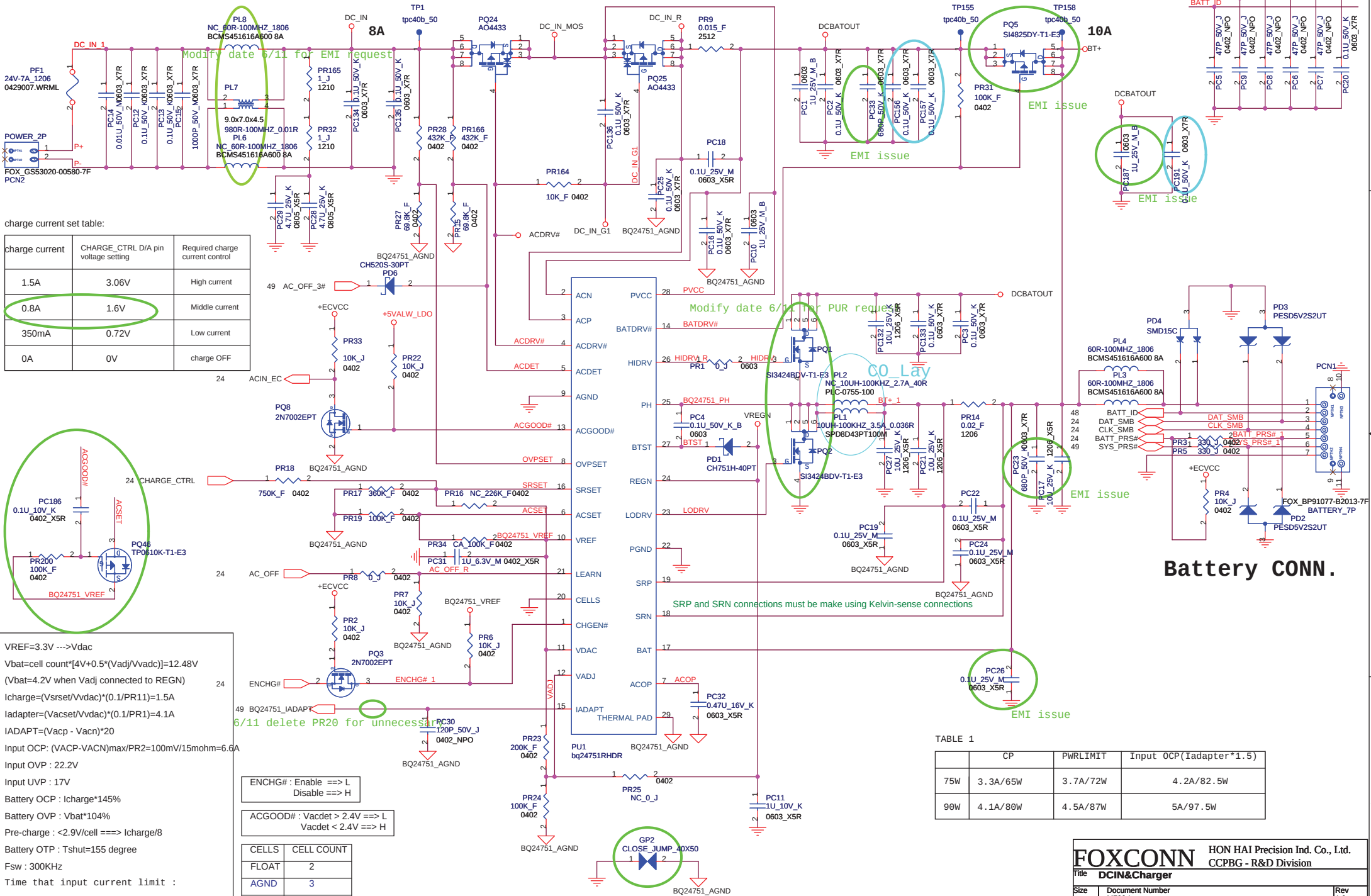
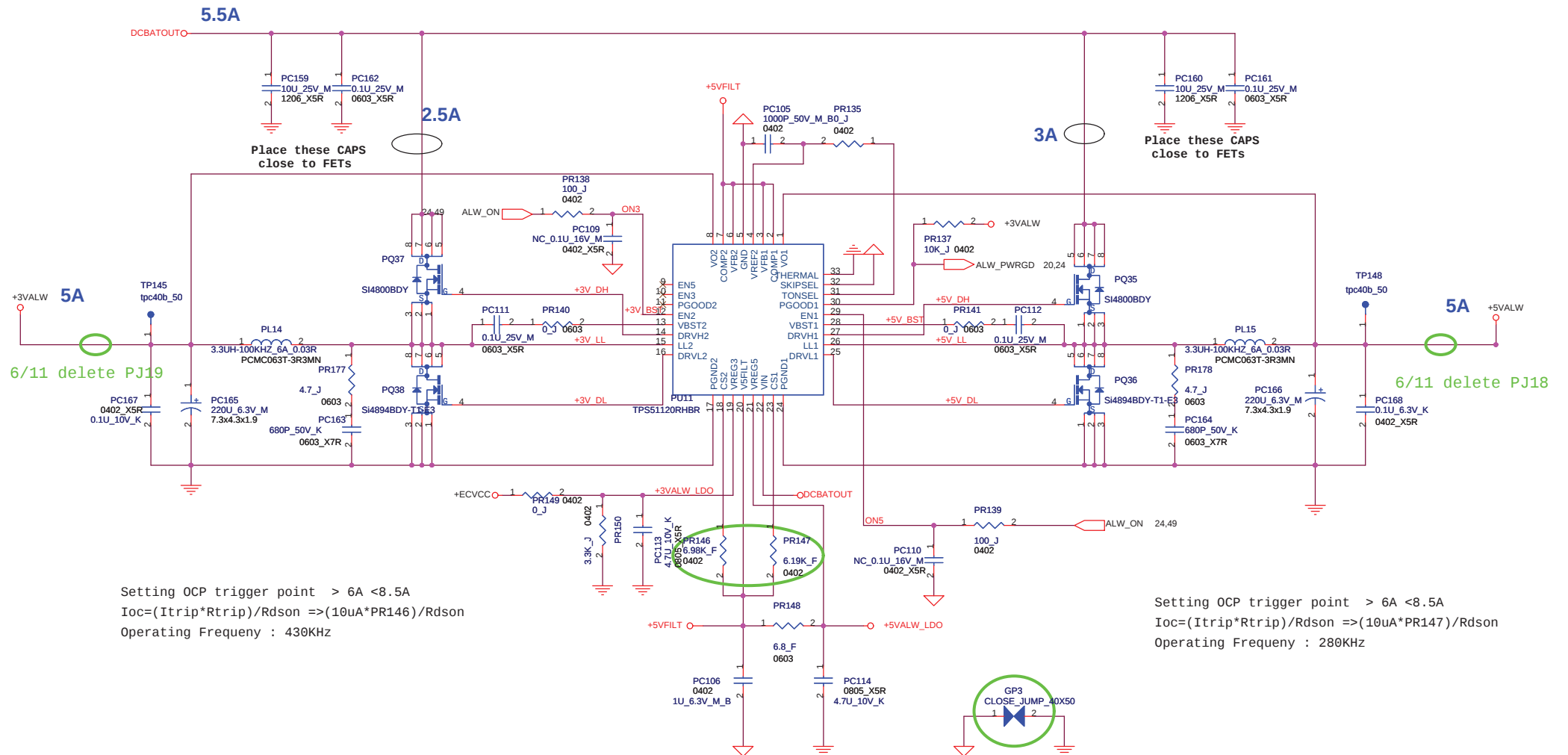
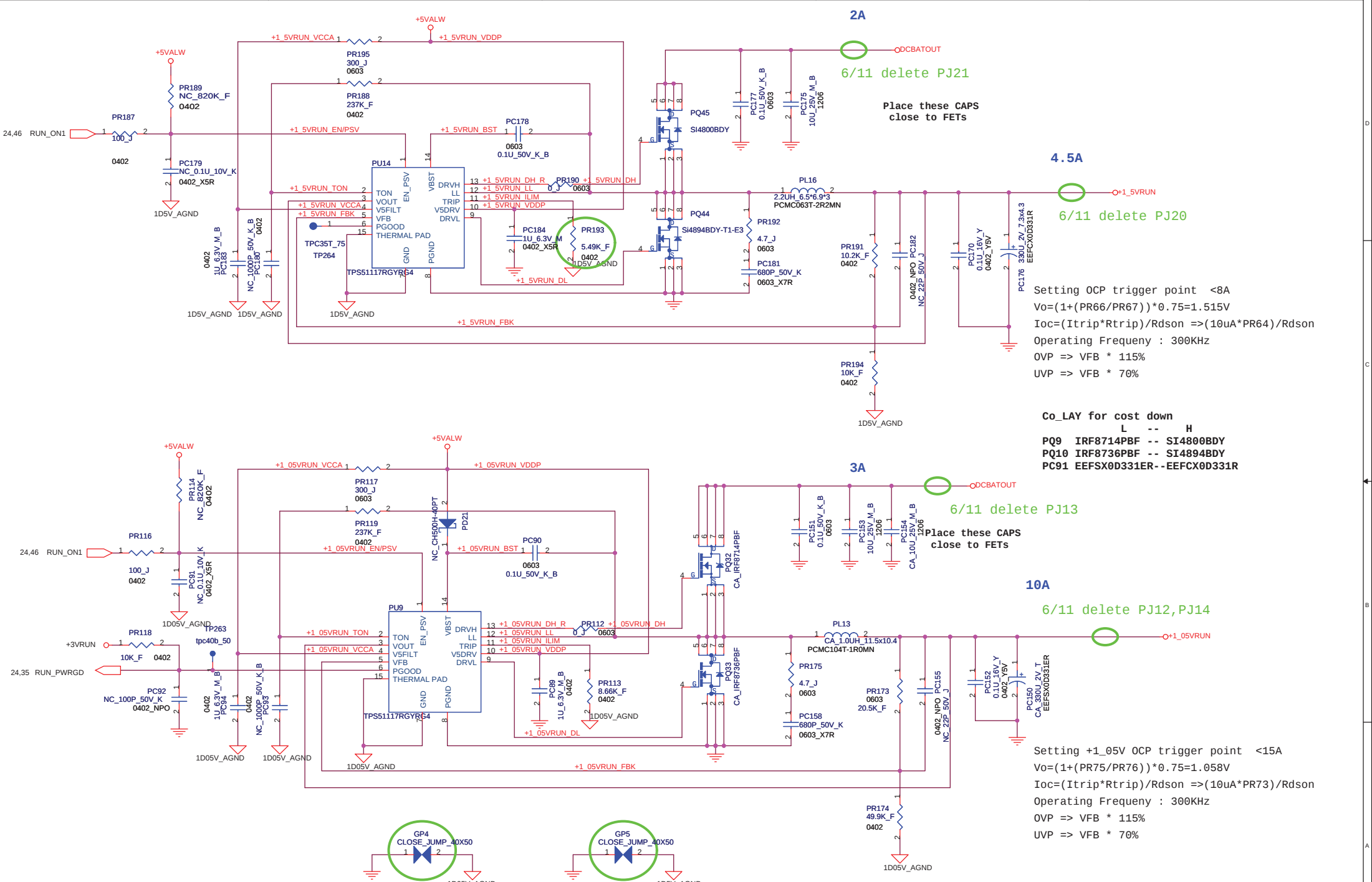


TABLE 1

	CP	PWRLIMIT	Input OCP(Iadapter*1.5)
75W	3.3A/65W	3.7A/72W	4.2A/82.5W
90W	4.1A/80W	4.5A/87W	5A/97.5W





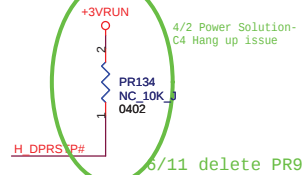
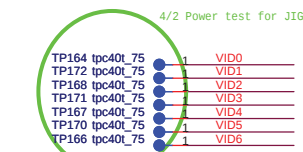
4.5A

10A

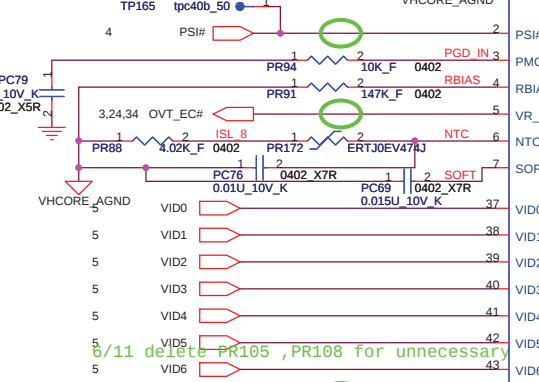
Setting OCP trigger point <8A
 $V_o = (1 + (PR66/PR67)) * 0.75 = 1.515V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR64) / R_{dson}$
Operating Frequency : 300KHz
OVP $\Rightarrow V_{FB} * 115\%$
UVP $\Rightarrow V_{FB} * 70\%$

Setting +1.05V OCP trigger point <15A
 $V_o = (1 + (PR75/PR76)) * 0.75 = 1.058V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR73) / R_{dson}$
Operating Frequency : 300KHz
OVP $\Rightarrow V_{FB} * 115\%$
UVP $\Rightarrow V_{FB} * 70\%$

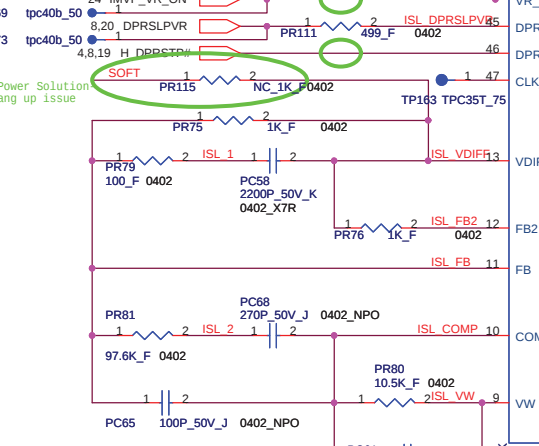
Co_LAY for cost down
L -- H
PQ9 IRF8714PBF -- SI4800BDY
PQ10 IRF8736PBF -- SI4894BDY
PC91 EEFSX0D331ER -- EEFCX0D331R



6/11 delete PR97 ,PR89 for unnecessary



6/11 delete PR105 ,PR108 for unnecessary



OCP Setting

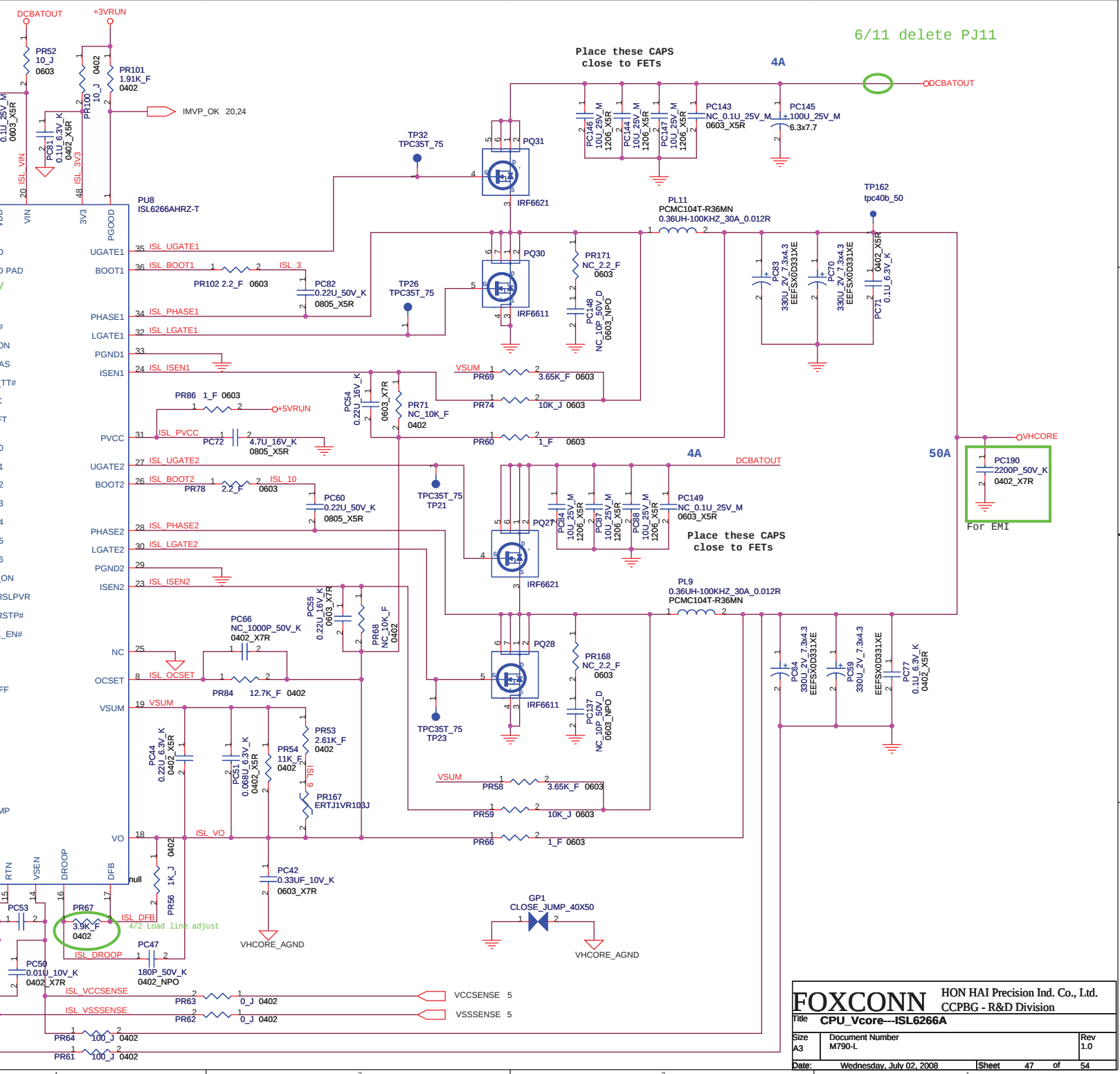
Switching Frequency = 300KHz

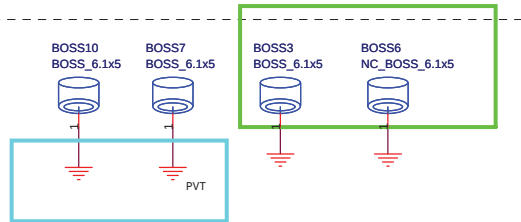
$R_{fset}[k\Omega] = (P[us] - 0.29) * 2.33, F=1/P$

OCP point = 63.3A

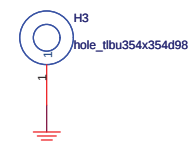
OCP point => $I_{oc} = (R_{oc} * 10uA) / R_{droop}, R_{droop} = 2.1mV$

Load line adjust => PR210(greaten => load line deepen)

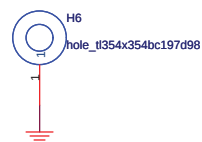




Thermal Module



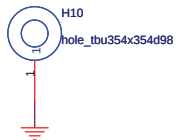
Near CRT



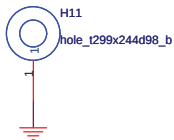
Near AUDIO



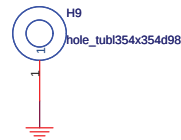
Near USB



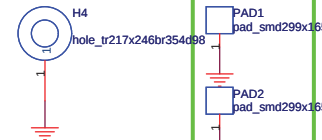
Near Express card



Near SD card



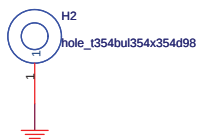
Near MS card



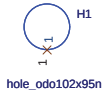
Near ODD



Near DC-IN



Near Robson

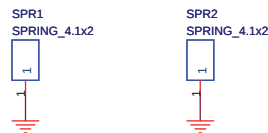


Near HDD

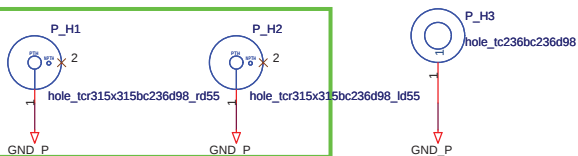


CPU

Finger

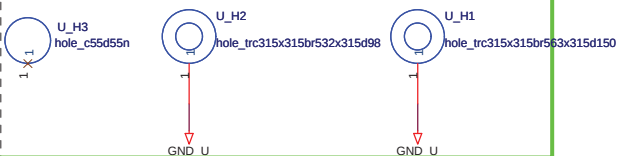


DVT



Power board

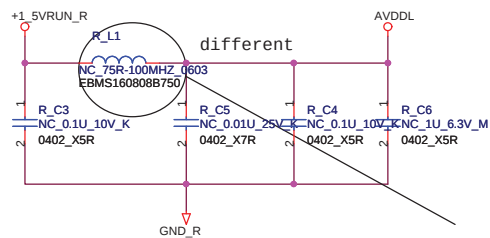
DVT



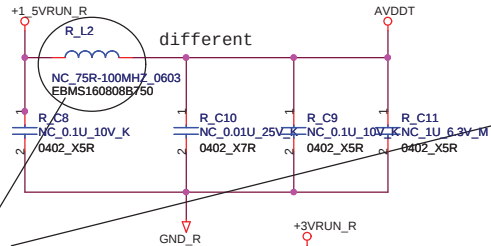
USB board

DVT

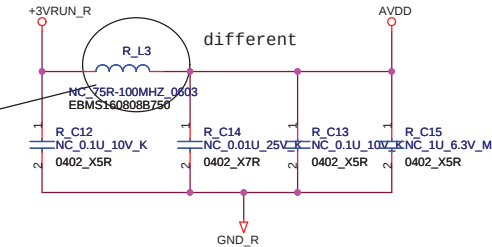
LAYOUT NOTE:
Place as close as possible
to AVDDL pins of Diamond Lake



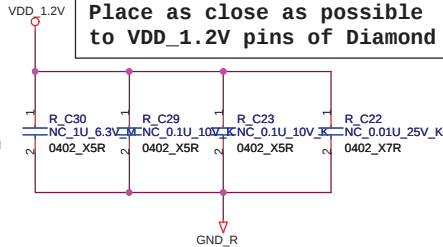
LAYOUT NOTE:
Place as close as possible
to AVDDT pins of Diamond Lake



LAYOUT NOTE:
Place as close as possible
to AVDD pins of Diamond Lake



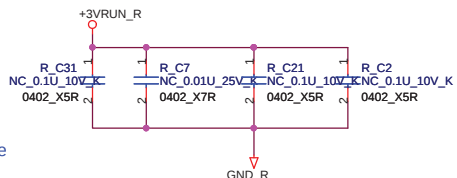
LAYOUT NOTE:
Place as close as possible
to VDD_1.2V pins of Diamond Lake



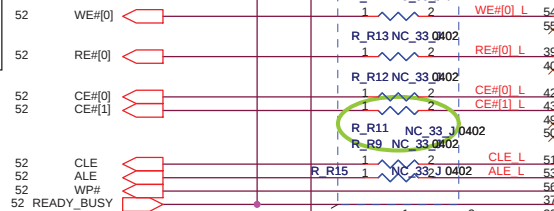
Intel sch use 70ohm /100MHZ

change

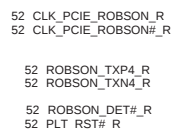
LAYOUT NOTE:
Place as close as possible
to +3VRUN pins of Diamond Lake



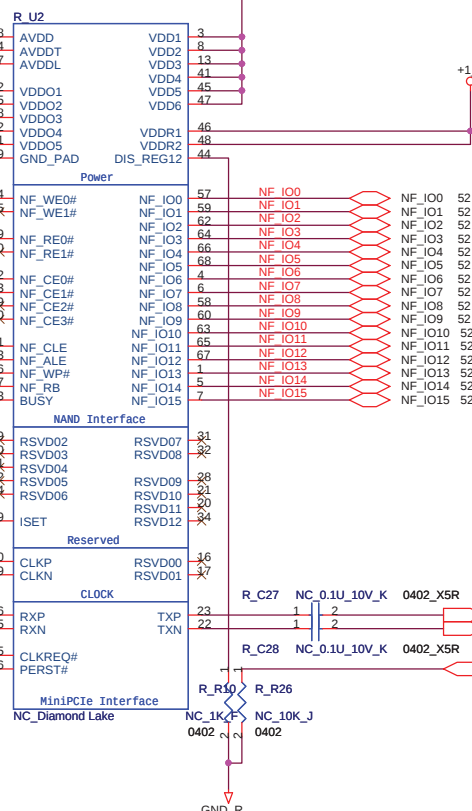
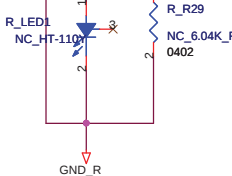
LAYOUT NOTE:
Close to NAND Flash



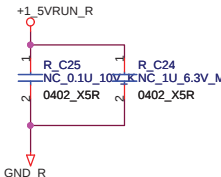
LAYOUT NOTE:
Close to Diamond Lake



Ultra Bright
Yellow Green



LAYOUT NOTE:
Place as close as possible
to VDDR1 and VDDR2 pins
of Diamond Lake



M790 EVT

(2008/01/23)
Update 8Layer H/L versio to 6Layer L version.

(2008/01/24)
Page 6. Change Clock to B version.
Page 25. Change SPI rom to new version.
Page 36. Change L62,delete L63 same as M760.

(2008/01/28)
Page 14/15. Add C767~C778 for EMI reserve.
Page 19. Add R610 damping resistor for adjustment for MOR request.
Page 20. Change GPIO18,20 to GPIO36,37 and delete R269,R270.
Page 23. Change D13 to mount.
Page 24. Change RP39,RP41 to +3VALW.Add D17,D18 for EC leakage current issue.
Page 29. Add R602,R603 damping resistor for adjustment for MOR request.
Page 32. Add R601 for MOR request.
Page 36. Add R604,R605 damping resistor for adjustment for MOR request.
Page 37. Add R611,R612,C779,C780 for EMI reserve.
Page 48. Change PQ40 from SI2304BDS-T1-E3 to SI2316DS-T1-E3 and Change PQ19 from IRF8714PBF to FDS8880_NL for MOR request.

(2008/01/29)
Page 50. Add H13~H16,P_H3.

(2008/01/30)
Page 50. Update H4,U_H1,U_H2.

(2008/01/31)
Page 20. Not AMT support,so delete R556, R557 and C722.
Page 32. Change GP2,GP3 to R556,R557.
Page 33. Change R486 connect to D_GND.
Page 50. Add Boss10.

(2008/02/01)
Page 49. Change PJ17 from PD13 pin1 to pin2.

(2008/02/02)
Page 17/24. Add FAN error detect function in panel switch pin4.
Page 32. Change C624 to 2.2uF for pop noise issue.

(2008/02/14)
Update some error discription for MOR request.

(2008/02/18)
Page 32. Mount Audio cable short components for EVT test.

(2008/02/20)
Page 32. Change U30 from TI(TPA6017) to GMT(G1431F2U) for pop noise issue.

(2008/02/21)
Page 17. Update Panel ID table.
Page 24. Update R447 CA to Mount,R437 Mount to CA.
Page 46. Add PJ10.
Page 14/15.Add J2/J3 for EMI request.
Page 6. Add reserverve C781,C782,C783 for EMI request.
Page 29. Add reserverve C784,C785 for EMI request.

(2008/02/22)
Page 14/15.Add J4/J5 for EMI request.
Page 6. Add reserverve C786,C787 for EMI request.

(2008/02/26)
Page 5. Change C76 from 6.3V to 10V for PUR request.
Page 11. Change C201,C225,C679,C681,C143,C168,C596,C601,C605 from 10V to 16V for PUR request.
Page 18/29. Change C32,C35,C449,C450,C725,C726,C727,C728,C729,C730 to 0.1uF,6.3V,10% for PUR request.
Page 31. Change R202 for PUR request.
Page 31. Change Q37,Q39,Q40,Q41 to PBSS2515E.115 for PUR request.
Page 32/33. Change Q6,Q25,Q34,Q38 to MMBT3906K for PUR request.
Page 33. Change Q33/Q44 to MMBT3904 for PUR request.

M790 DVT

(2008/02/28)
Page 33. Change Q33/Q44 to PMBT3904.215 for PUR request.

(2008/03/03)
Page 52. Change R_U1,R_U3 to 8Gbit size and change R_R11,R_R18,R_R25 to mount.

(2008/03/05)
Page 24. Mirror CN3 for Int. keyboard issue.

(2008/03/06)
Page 38. Mirror CN6 for easy A'ssy.
Page 44. Change PR146 to 6.8K,PR147 to 5.49K for OCP current adjust.
Page 45. Change PR193 to 5.49K for OCP current adjust.

(2008/03/24)
For PUR request change C624 2.2uF(1.25mm) to (0.8mm),C510/PC42 0.33uF(X5R) to (X7R).
Page 38. SWAP L60 for CN6 mirror issue.
Page 24/40. Change CHARGE_LED# low enable to H enabe same as M750/M760.

(2008/03/28)
Page 24. Add C722(1000pF) for FAN speed stable.

(2008/04/02)
Page 28/51/52. Change Robson function to no mount.

(2008/04/07)
Page 23. Del PJ4 Change PJ3 type for JIG.
Page 43. Add for charger ocp improve.
Page 43~46,48. A_GND and P_GND change to GP2~6.
Page 47. Add PR134,PR115 for Power Solution- C4 Hang up issue.
Page 47. tpc40b_50 Change to tpc40t_75 power point part for JIG.
Page 49. Add Battery UVP protect for power issue.

(2008/04/08)
Page 29. Add C733,R269,R270/R616(no mount),Change R44 to 4.99Kohm and NC CTRL_1D8 circuit for 88E8057.
Page 32. Change R98,R450,Q8,Q27 to NC and Add R614,R615 no mount for speaker cable short protection circuit.
Page 35/40. Change MS/SD LED to Low active.

(2008/04/11)
Page 31. Change C182,C194 to 0.1uF for MIC THD+N issue
Page 49.Change PR199 to 215Kohm for Battery UVP adjust.

(2008/04/14)
Page 31. Change C626,C662 to 4.7uF for MIC FSIV issue.
Page 29. Design for 88E8055.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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(2008/04/14)

Page 16. Change L14,L16,L17 to 120ohm/100Mhz bead for CRT EMI issue.
Page 32. Add C797~C800(220pF)for Speaker EMI issue.
Page 37. Change R611,R612 to L26,L28 120ohm/100Mhz bead and C779,C780 to 15pF for Camera EMI issue.
Page 41. Add C790~C79(220pF)for power board EMI issue.

(2008/04/15)

Page 50. Change Boss7 pin2 connect to RC for EMI reserve and Add Finger SPR1,SPR2 for EMI issue.
Page 32. Add C802~C805(220pF)for Speaker EMI issue.

(2008/04/18)

Page 23. Update ODD connector for MOR request.
Page 26. Add R611,R612 and Change U24,C534 to no mount for MOR request.

(2008/04/21)

Page 19. Change C388,C389 to 15pF for Y6 test fail.
Page 24. Change C245,C246 to 18pF for Y2 test fail.
Page 31. Change C629,C652 to 220pF same as M760.
Page 36. Change C496,C497 to 27pF for Y3 test fail.Change R352,R353,R356,R357 to 100ohm,R590 to 33ohm for MS/SD fail items.

(2008/04/23)

Page 16. Update CN2 VGA connector type.

(2008/04/24)

Page 41. Change U_R1~R4 to NC,U_L1,L2 to mount.
Page 43. Add PC187,and Change PC23,PC33 to 680P for EMI request.

(2008/04/25)

Page 16. Update D11 to SL22 for CRT ripple noise.

(2008/04/28)

Add C806~C808,PC188,PC189(0.1uF) for ESD solution.
Page 27. Change CN14 to FOX_1CX42201-SM for ME reuset.
Page 36. Change CN11 to Gray color,C459,C488 to X5R and R568,R359,R377 to mount for MOR request.

(2008/04/29)

Page 21. Change C717,C723 to X5R.

(2008/04/30)

Page 26. Change C538 to mount for ripple noise.
Page 37. Change R7/F3 to mount,R9/R4 to NC for 3.3V Camera.
Page 50. Change BOSS3,6,7,10 to 1M-1F50M20-5000 and NC BOSS6.

(2008/05/02)

For MOR request,add F5,F6,F7.
Page 6. Add R618~R621 475ohm for CR# issue.
Page 21. Change C721 to 1uF for Intel design change.

(2008/05/06)

Page 16. Change R418,R424 to 30 ohm for Graphic test fail item.
Page 50. Update PAD1,2 size.

(2008/05/07)

Page 36. Change R590 to 22ohm for SD card clock issue.
Page 37. Add resver regulater IC for Camera power.
Page 41. Add C811 for ESD issue.
Page 50. Add resver C812,R623 for EMI issue.
Page 43. Change PQ5 from A04433 to SI4825DY-T1-E3 for EMI issue.
Page 47. Add PC190 for EMI issue.

(2008/05/08)

Page 6. Add TP153,TP154 for FSB easy measure.

BOM Change

Change CN25 to LN27131-A403-4F.
Change R352,R353,R356,R357 to 68ohm.
Change R601 to mount,F5 to NC.
Change U41,C813~C817,R626,R625,R4 to mount,R7,F3 to NC.

(2008/05/14)

Page 16. Change R418,R424 to 22ohm for CRT issue.
Page 43. Change PL6,PL8 to no mount,Change PL7 to 1000R-100MHZ_0.015R for EMI issue.
Page 47. Change PR115 to no mount.

M790 PVT

(2008/06/03)

Page 25. Add lable1 for BIOS.
Page 39. Change CN8,CN9 to grey color.

(2008/06/11)

Page 23. Delete PJ3 for unnecessary
Page 43. Change PL7 to 1L-FPWC090-7H01 for EMI request.
Page 43. Change PQ1,PQ2 from17-S134240-VT00 to 17-S13424B-DV00 for PUR request.
Page 43. Delete PR20 for unnecessary
Page 44. Delete PJ18,PJ19 for unnecessary
Page 45. Delete PJ12,PJ13,PJ14,PJ20 ,PJ21for unnecessary
Page 46. Delete PJ6,PJ7,PJ8,PJ9 ,PJ10 for unnecessary
Page 47. Delete PJ11,PR97,PR89,PR105,PR108 for unnecessary
Page 48. Delete PR77,PR72,PR65 for unnecessary
Page 49. Delete PR12,PR38,PR46 for unnecessary

(2008/06/16)

Page 32. Change F5 to 1.5A and to mount for MOR request.

(2008/06/23)

Page 41. Change C790~C796,C811 to 220pF for EMI and Hotkey issue.
Page 41. Add Fuse(F8) in power source on power board for short test.
Page 43. Mount PC156,PC157 and Add PC191 for EMI issue.
Page 50. Change BOSS7,10 connect to GND.

(2008/06/24)

Page 40. Change LED1,LED2,LED6 to HT-110UY,LED5 to HT-110UD.R383,R598 to 120ohm for MOR request.
Page 41. Change P_LED1~P_LED3 to HT-150YG.P_R1~P_R3 to 100 ohm for MOR request.

(2008/07/02)

Page 31. Change C184,C192 to 4.7uf 0603 for MIC THD+N issue this change same as M761.
Add ESD solution C810,C812,C818,PC192(0.1uF).

M790 MP

(2008/07/24)

Page 25. Change CN26,U11,C308,R221 to no mount,R233 to mount.
Page 40. Change R385 to 33ohm,R383,R598,R599 to 68ohm for LED bright issue.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
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