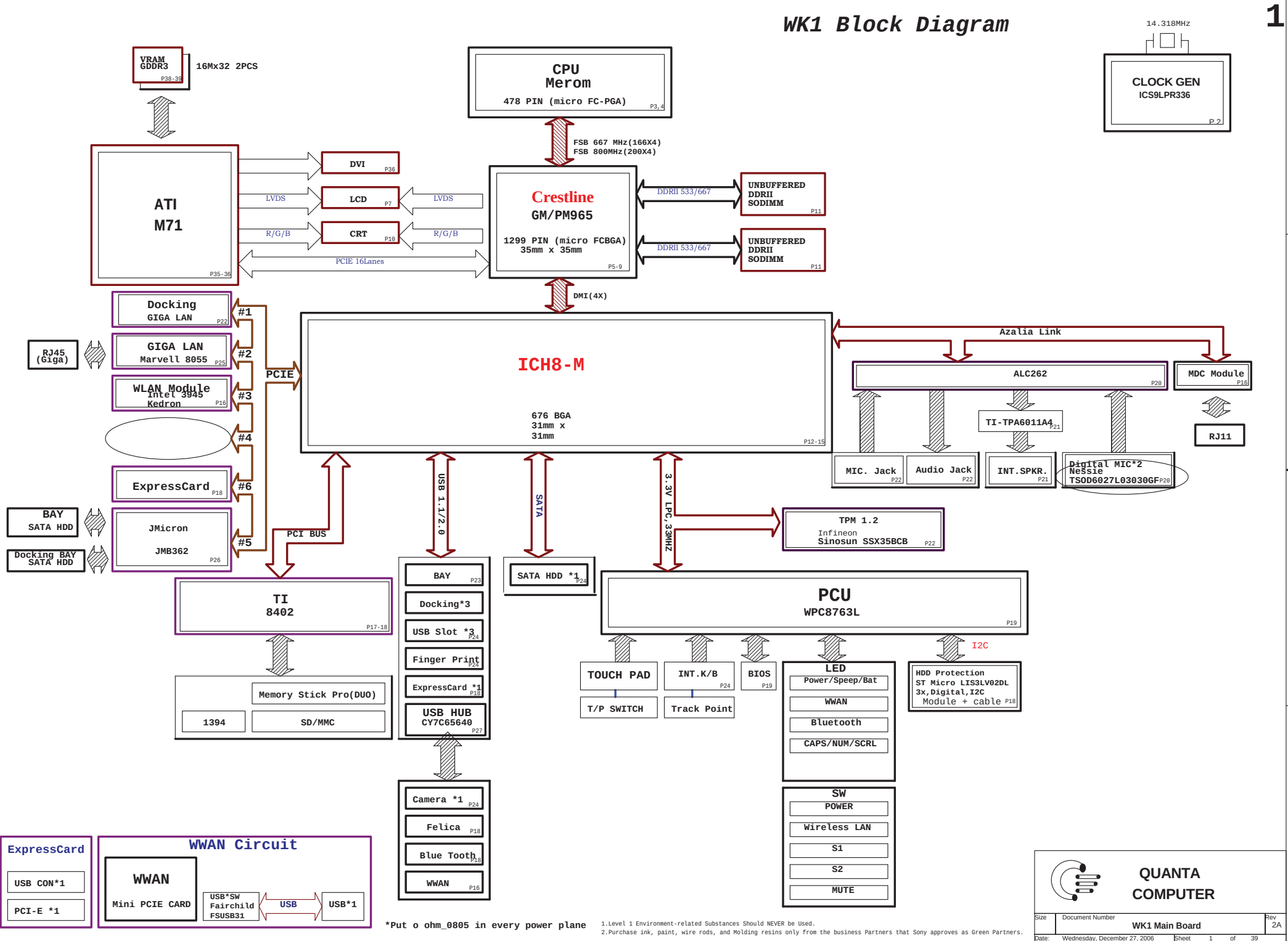
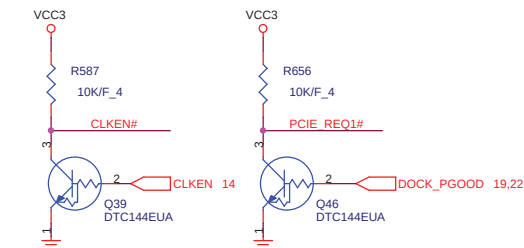


WK1 Block Diagram

1





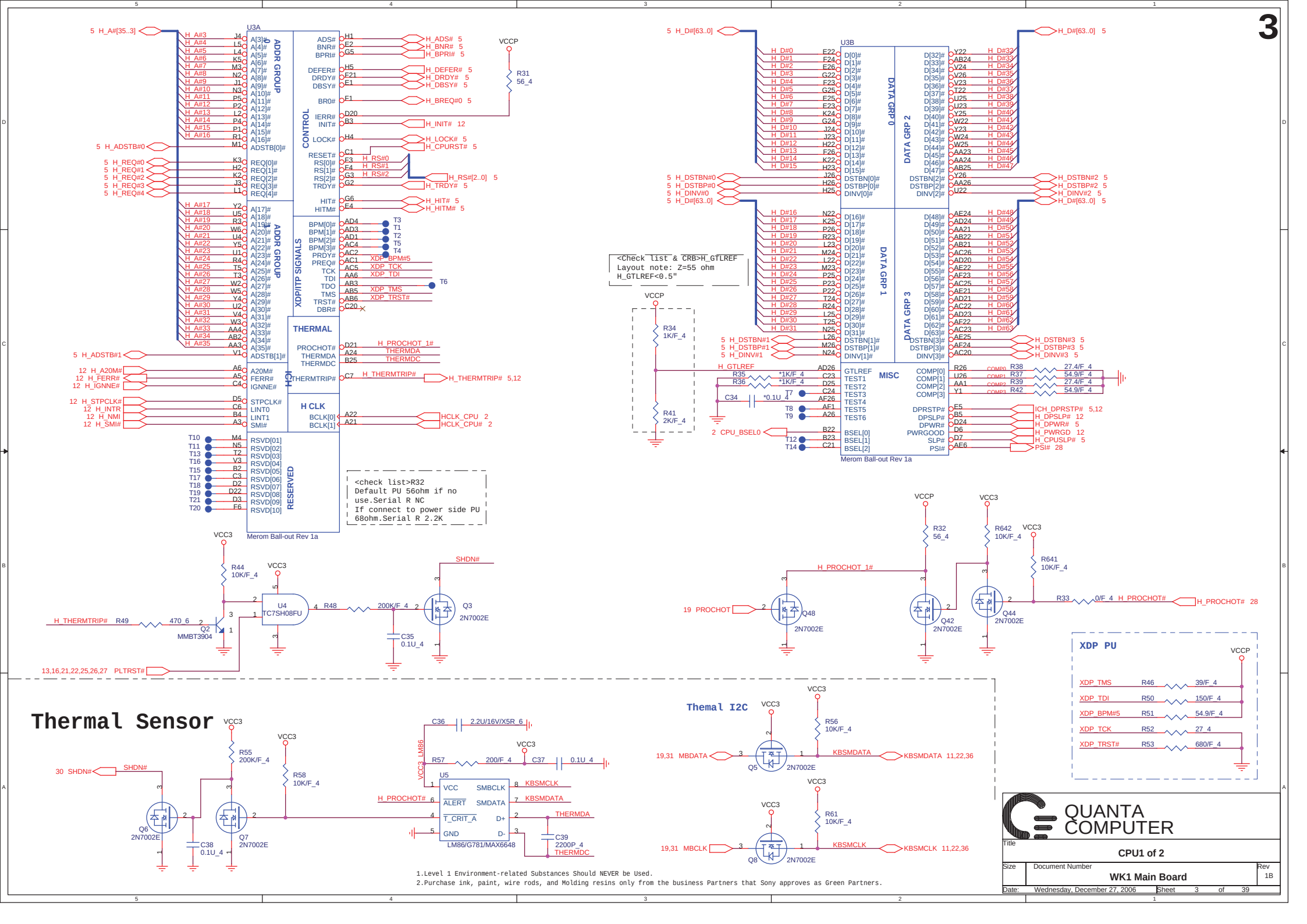
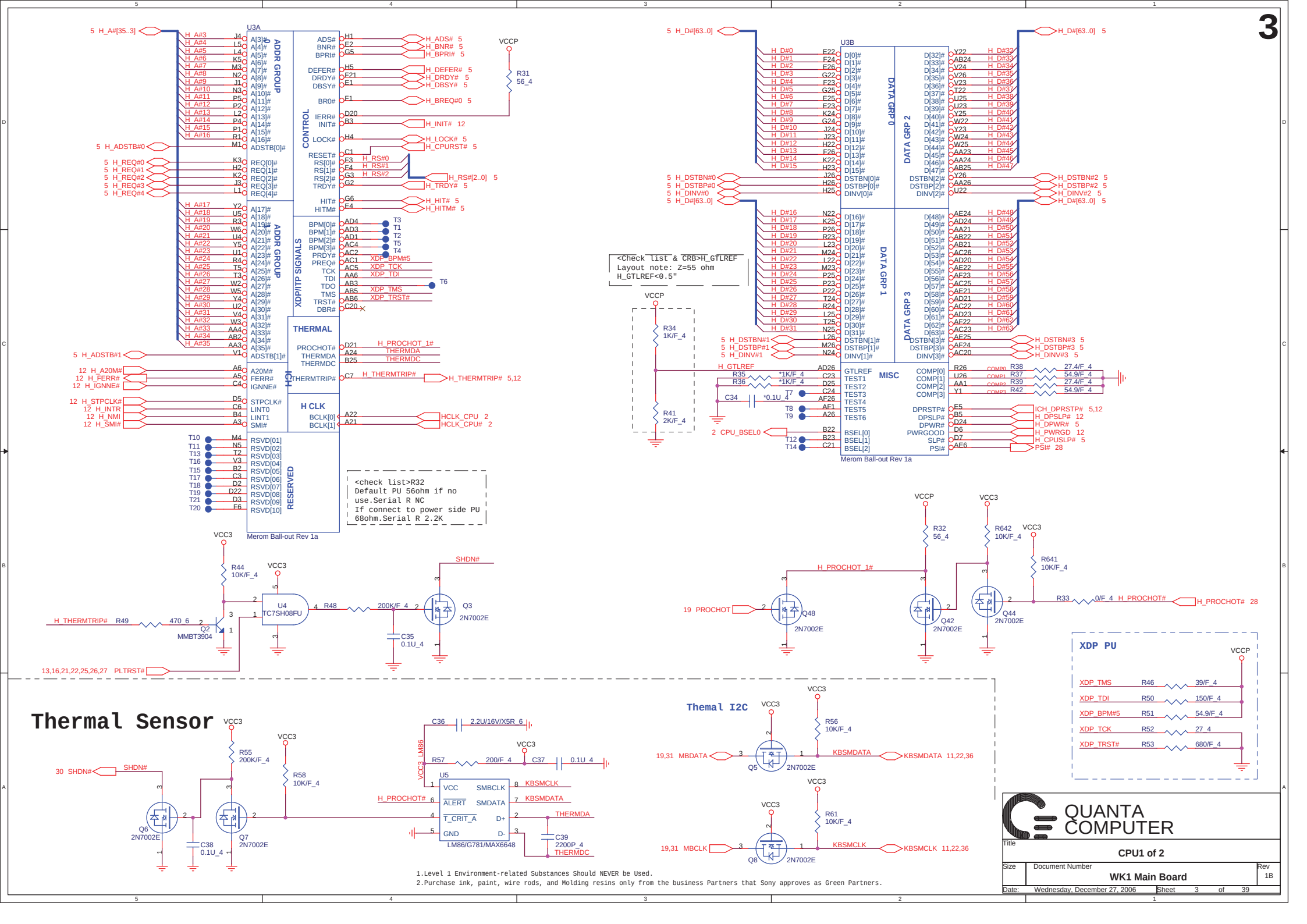
PCIE REQ EXPRESSCARD#	R717	10K/F 4
PCIE REQ LAN#	R715	10K/F 4
PCIE REQ SATA#	R712	10K/F 4
PCIE REQ MCH#	R612	10K/F 4
PCIE REQ MINI#	R613	10K/F 4

* 0	: PIN6/7 SRC
1	: PIN 6,7 CPI

PIN 34	PIN 43	PIN 44	PIN 47	PIN 48
L0 R26 10K	D0T96T	D0T96C	LCD 100/96T	LCD 100/96C
HI R498 10K	27MHz non-Spread	27MHz Spread	SRC0T	SRC0C

Thermal PAD 73

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Title	
CLOCK GENERATOR	
Size	Document Number
	WK1 Main Board
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COMPUTER

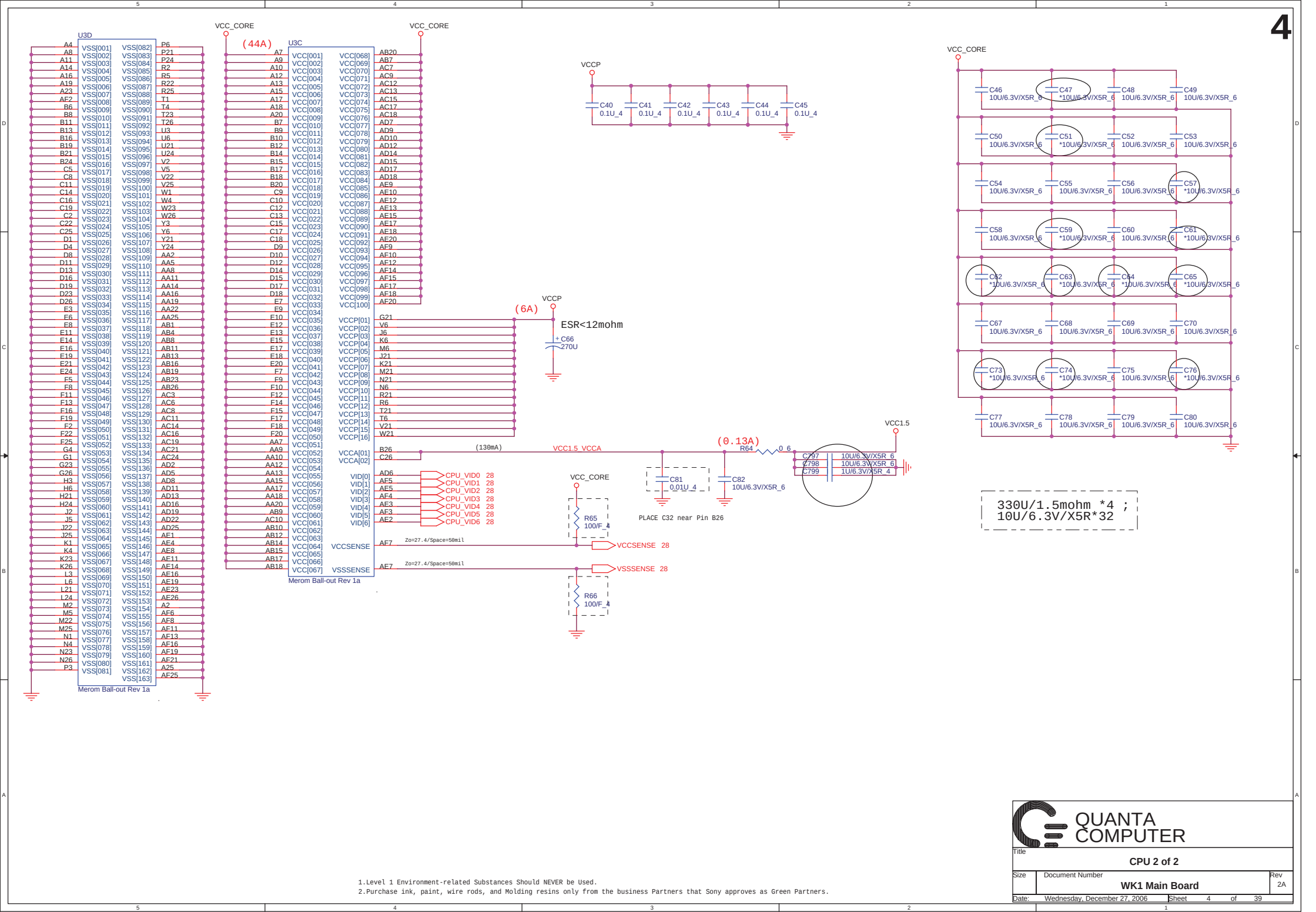
CPU 2 of 2

Size	Document Number	Rev
------	-----------------	-----

WK1 Main Board

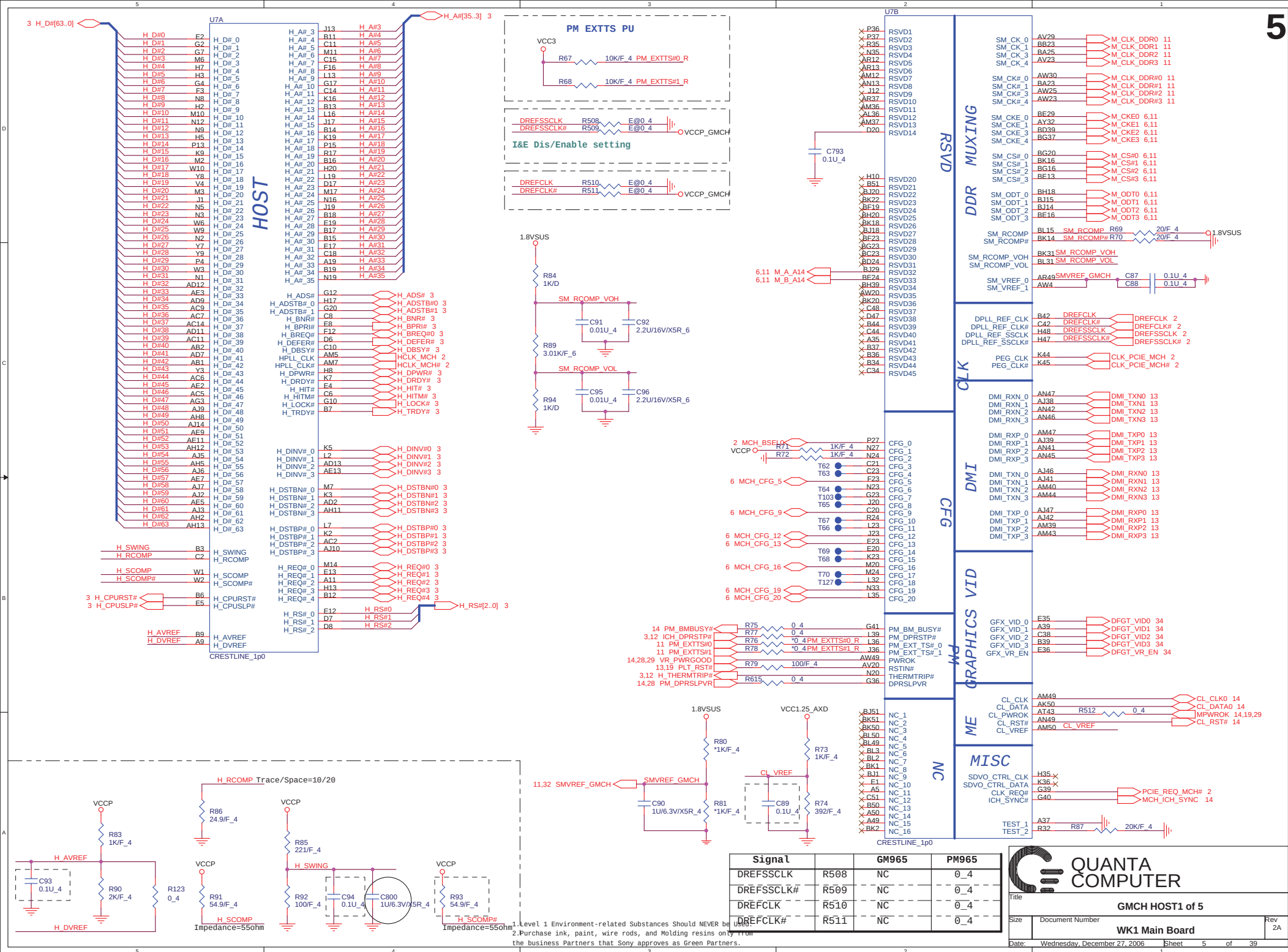
2A

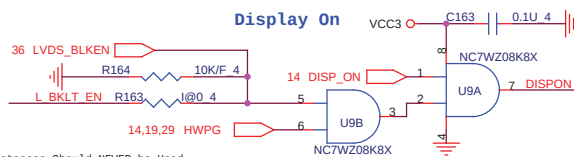
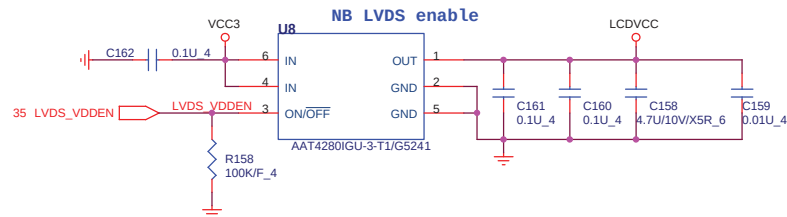
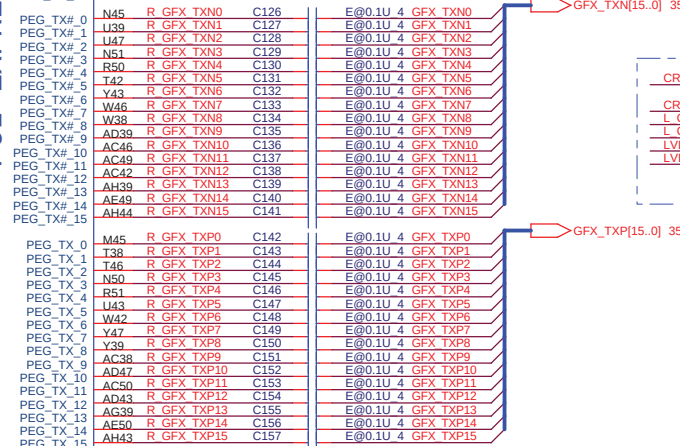
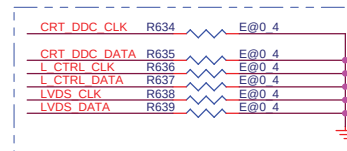
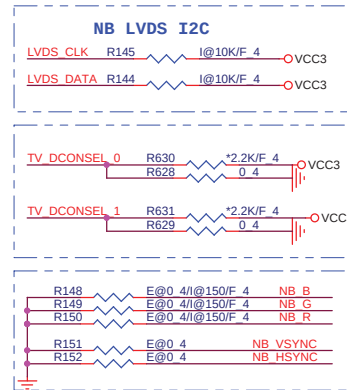
Date: Wednesday, December 27, 2006 Sheet 4 of 39



1.Level 1 Environment-related Substances Should NEVER be Used.

1. Level 1 Environment-Related Substances should NEVER be used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





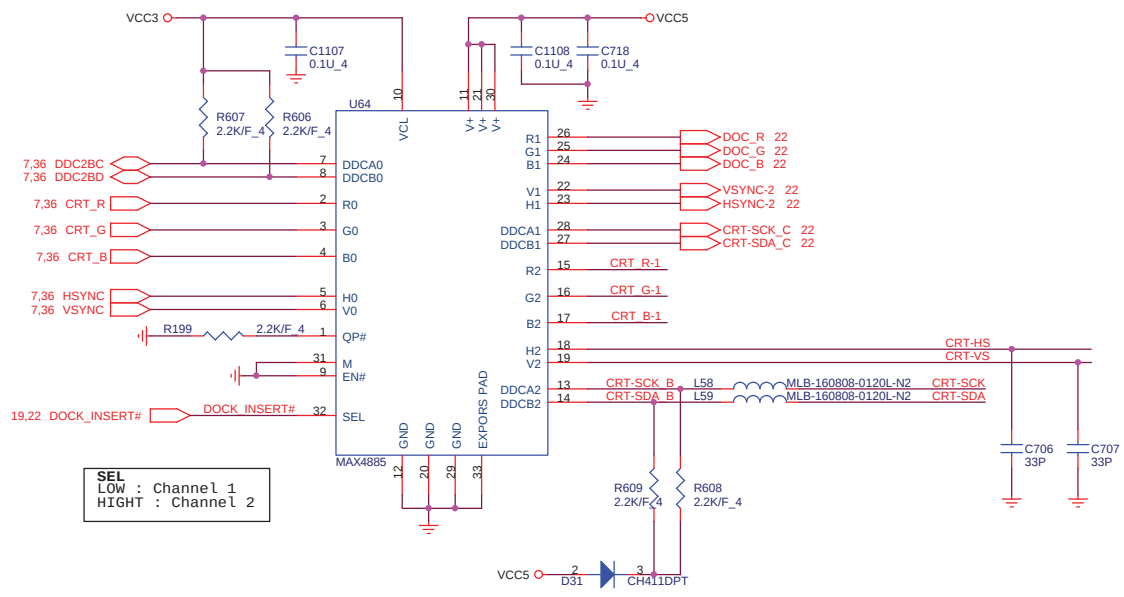
E@: 965PM(EXT) should mount		I@: 965GM(INT) should mount		7
Signal		965GM	965PM	
NB_B	R153	0_4	NI	
	R148	150_4	0_4	
NB_G	R154	0_4	NI	
	R149	150_4	0_4	
NB_R	R155	0_4	NI	
	R150	150_4	0_4	
NB_VSYNC	R151	NI	0_4	
	R162	30.1/F_4	NI	
NB_HSYNC	R152	NI	0_4	
	R159	30.1/F_4	NI	
LVDS_IBG	R124	2.4K/F_4	NI	
LVDS	RP63	0X2	NI	
	RP70			
	RP71	NI	0X2	
	RP78			
L_BKLT_EN	R163	0_4	NI	
L_CTRL_CLK	R146	10K	NI	
	R636	NI	0_4	
L_CTRL_DATA	R143	10K	NI	
	R637	NI	0_4	
LVDS_VDDEN	R141	0_4	NI	
DDC2BC	R156	0_4	NI	
	R634	NI	0_4	
DDC2BD	R157	0_4	NI	
	R635	NI	0_4	
CRT_REST	R161	1.3K/F	0_4	
L_DDC_CLK	R491	0_4	NI	
	R638	NI	0_4	
L_DDC_DATA	R492	0_4	NI	
	R639	NI	0_4	
GFX	C126	NI	0.1UF_4	
	C157			
BRIGHT	R170	0_4	NI	
	R171	NI	0_4	



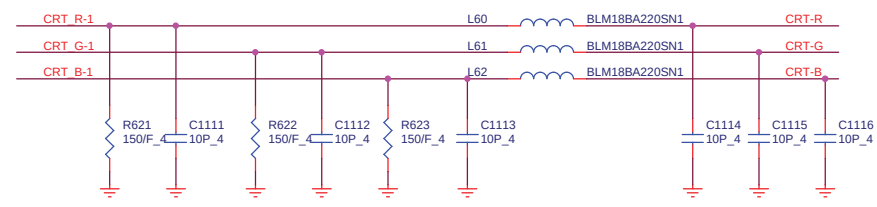
Title			
GMCH DMI VEDIO 3 of 5			
Size	Document Number	Rev	
	WK1 Main Board	2A	
Date:	Wednesday, December 27, 2006	Sheet	7 of 39



2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



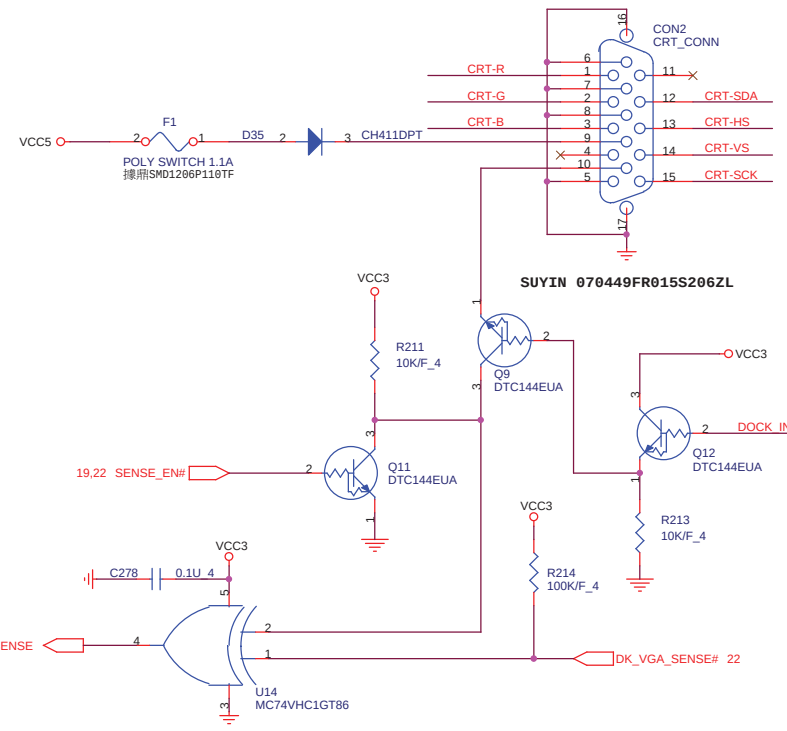
SEL
LOW : Channel 1
HIGHT : Channel 2



MAX4885

EN#	M	SEL	
L	L	L	1:2 Mode buffers Enabled H0 to H1 , V0 to V1
L	L	H	1:2 Mode buffers Enabled H0 to H2 , V0 to V2
L	H	L	2:1Mode buffers Disabled H0 to H1 , V0 to V1
L	H	H	2:1Mode buffers Disabled H0 to H1 , V0 to V1

	SENSE_EN#	MB CRT	DOCK CRT	DOCK DVI	CRT_SENSE
All no Plug	L	H	H	L	L
MB CRT Plug	L	L	H	L	H
DOCK CRT Plug	L	H	L	L	H
DOCK DVI Plug	L	H	H	H	H
SENSE EN	H	X	X	X	L
DOCK CRT/DVI Plug	L	H	L	H	L
DOCK CRT/MB CRT Plug	L	L	L	L	L



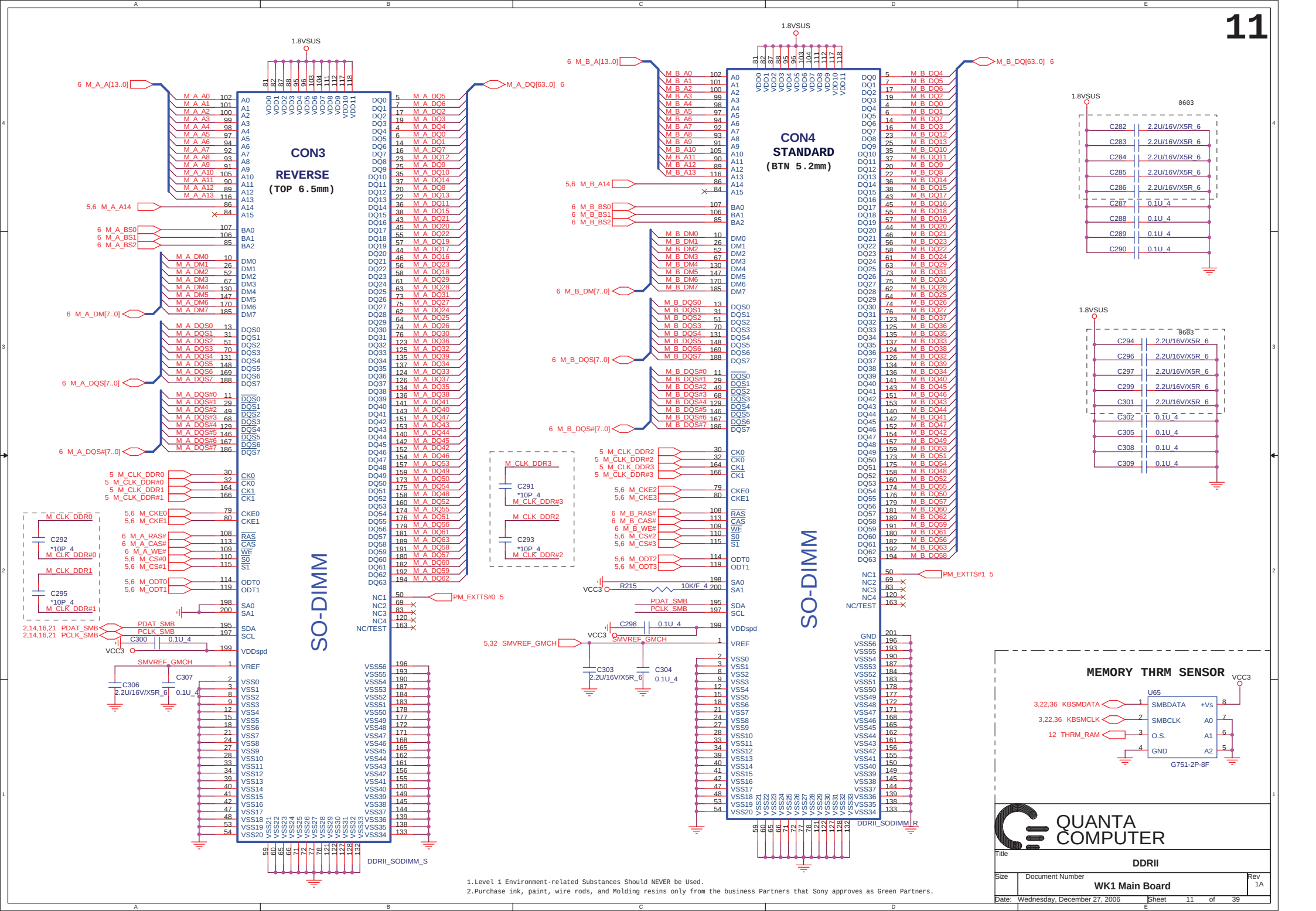
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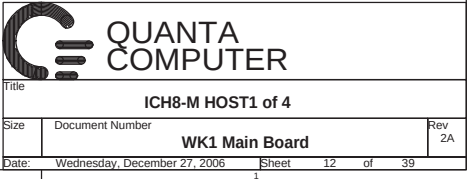
QUANTA
COMPUTER

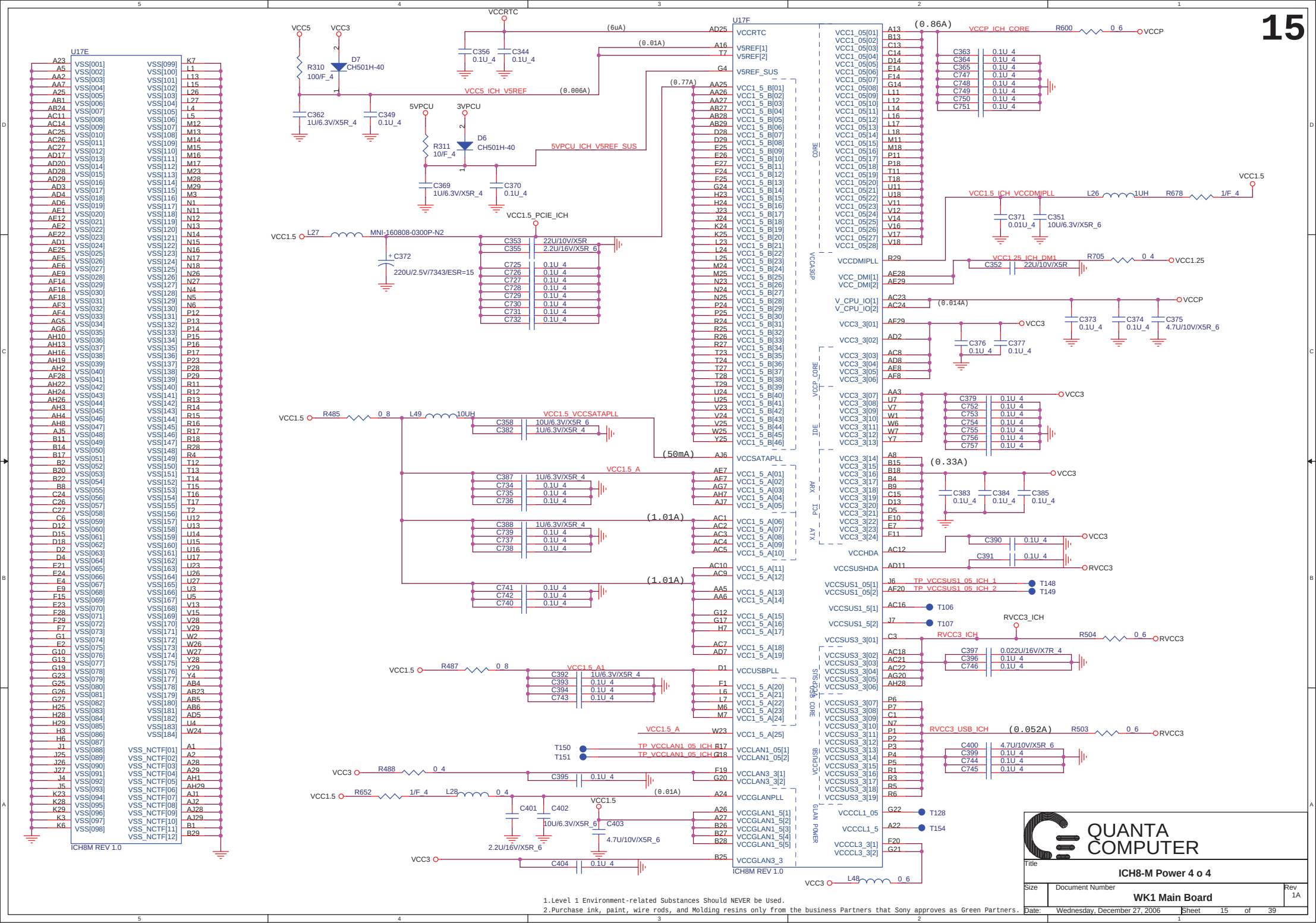
Title: CRT

Size: Document Number: WK1 Main Board Rev: 2A

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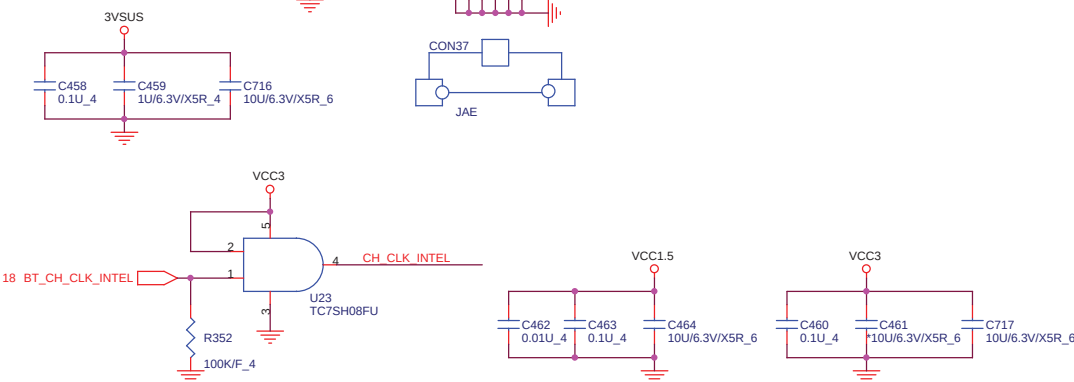
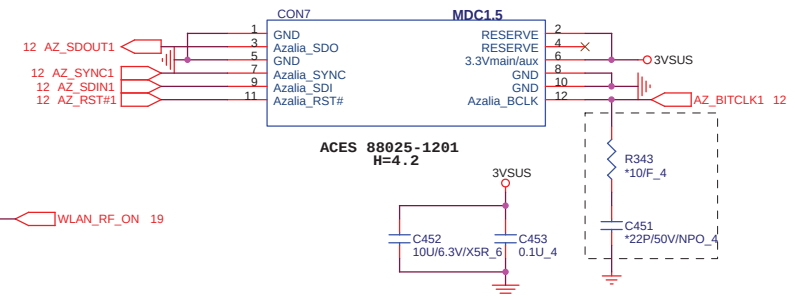
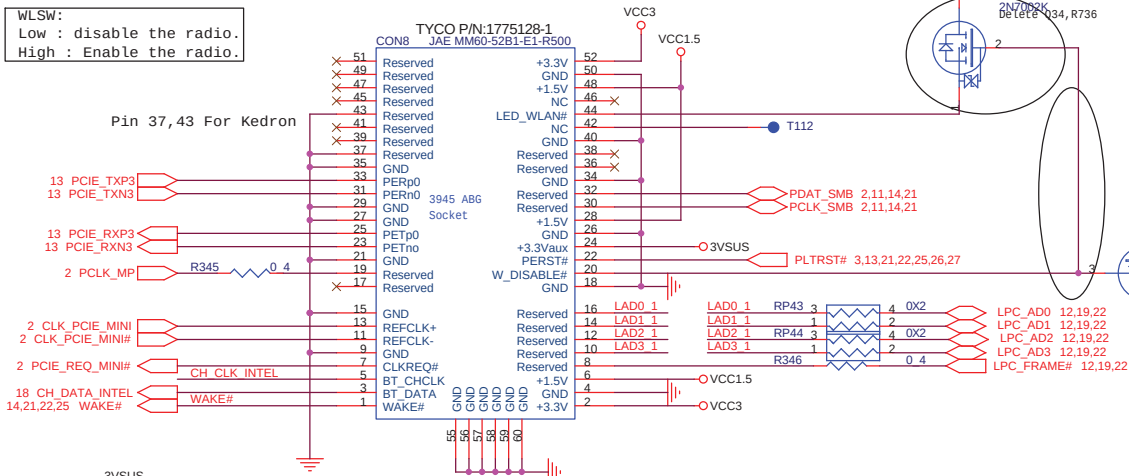


```
LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.
```

```
WLSW:
Low : disable the radio.
High : Enable the radio.
```

Mini PCI-E Card FOR WL

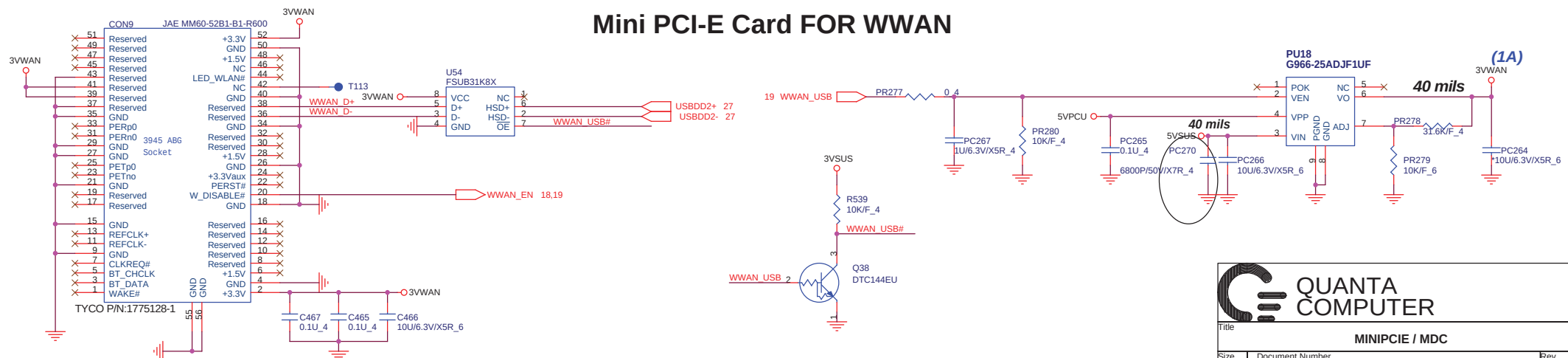
MDC V1.5



ROBSON 512MB/1GB NAND

Delete CON

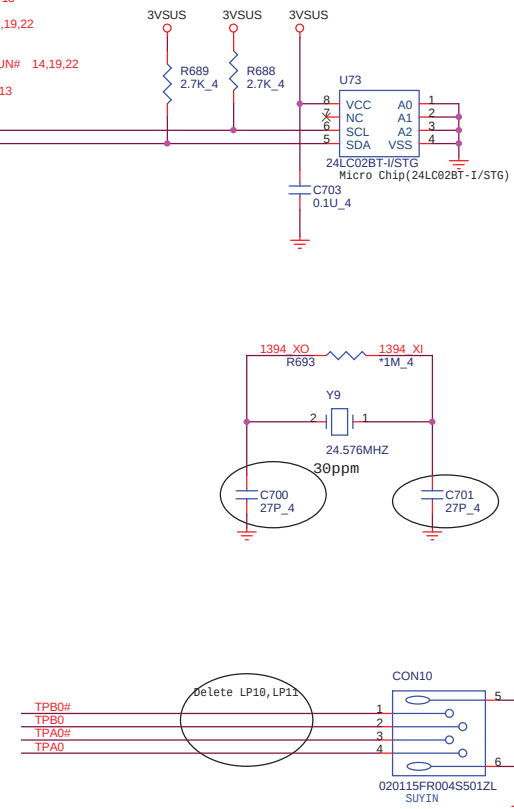
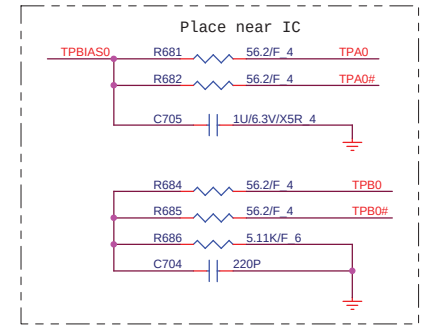
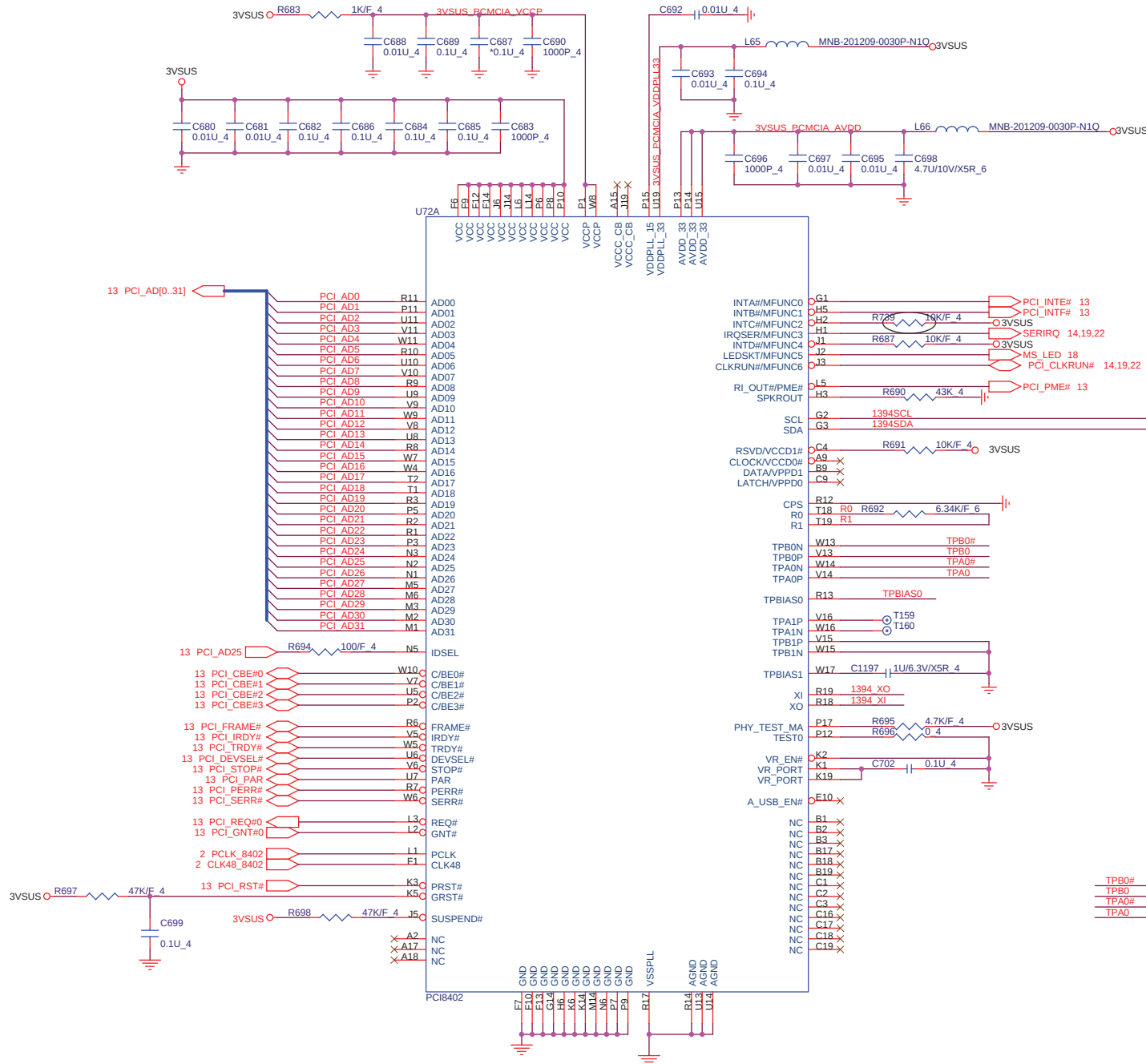
Mini PCI-E Card FOR WWAN

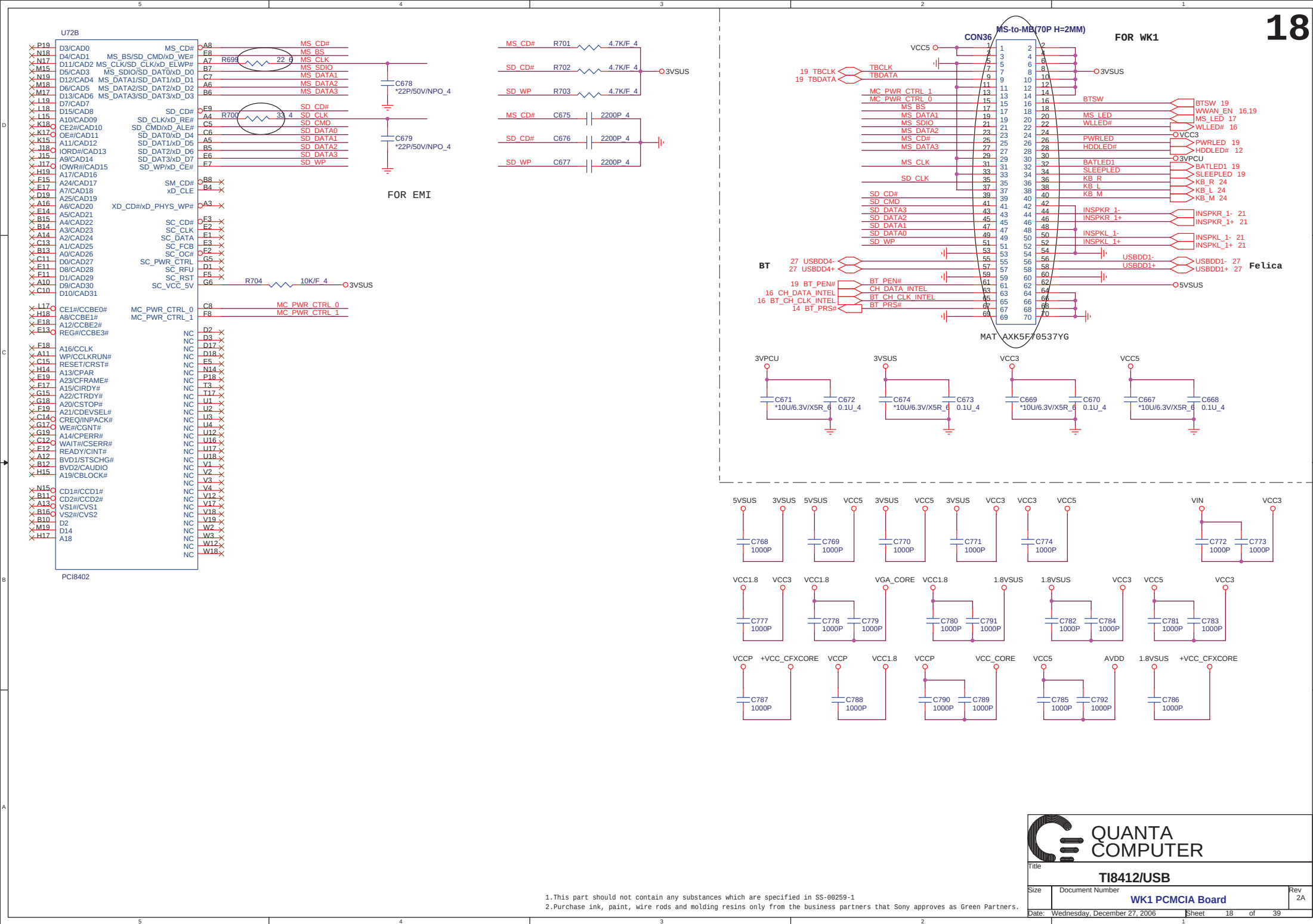


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Title			
MINIPCIE / MDC			
Size	Document Number		Rev
	WK1 Main Board		2A
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1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





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Title: **T8412/USB**

Size: Document Number **WK1 PCMCIA Board**

Date: Wednesday, December 27, 2006 Sheet 18 of 39

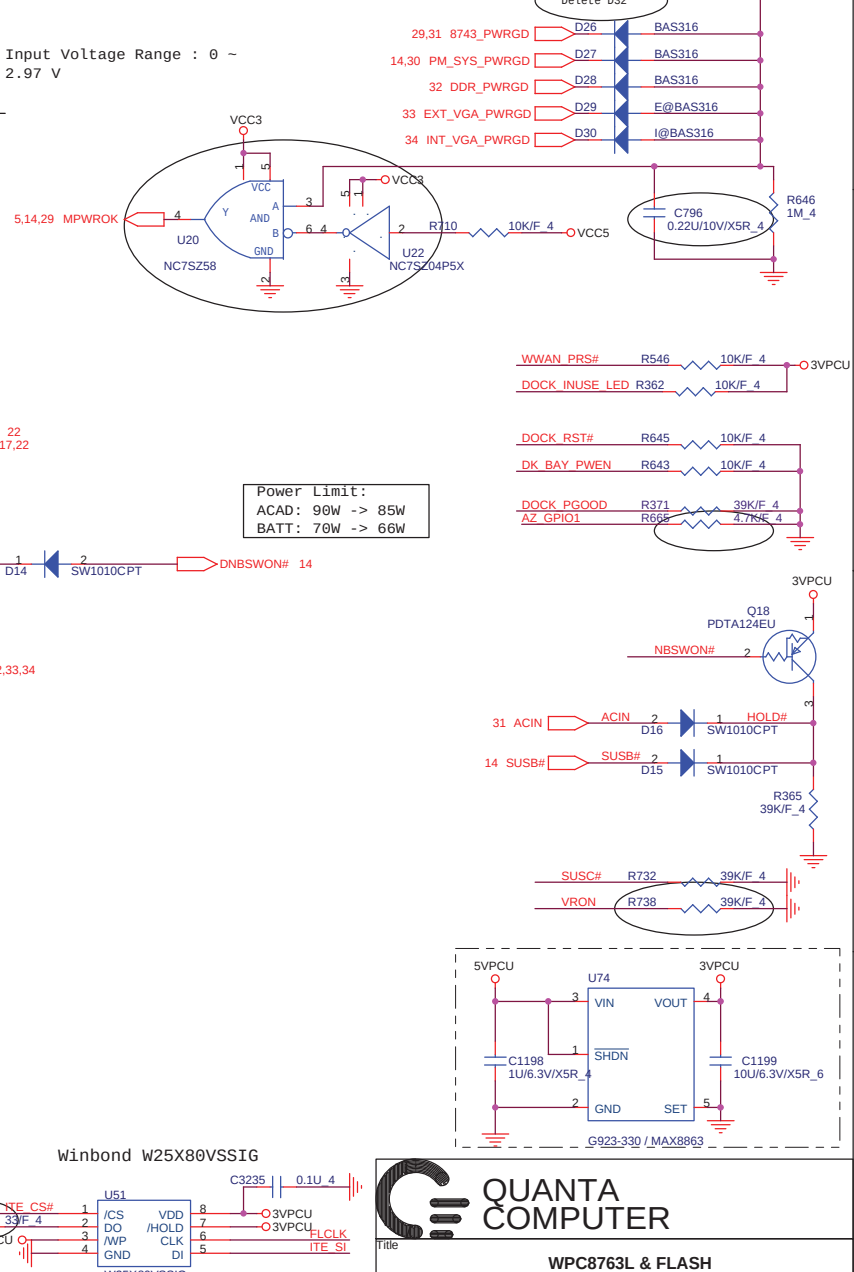
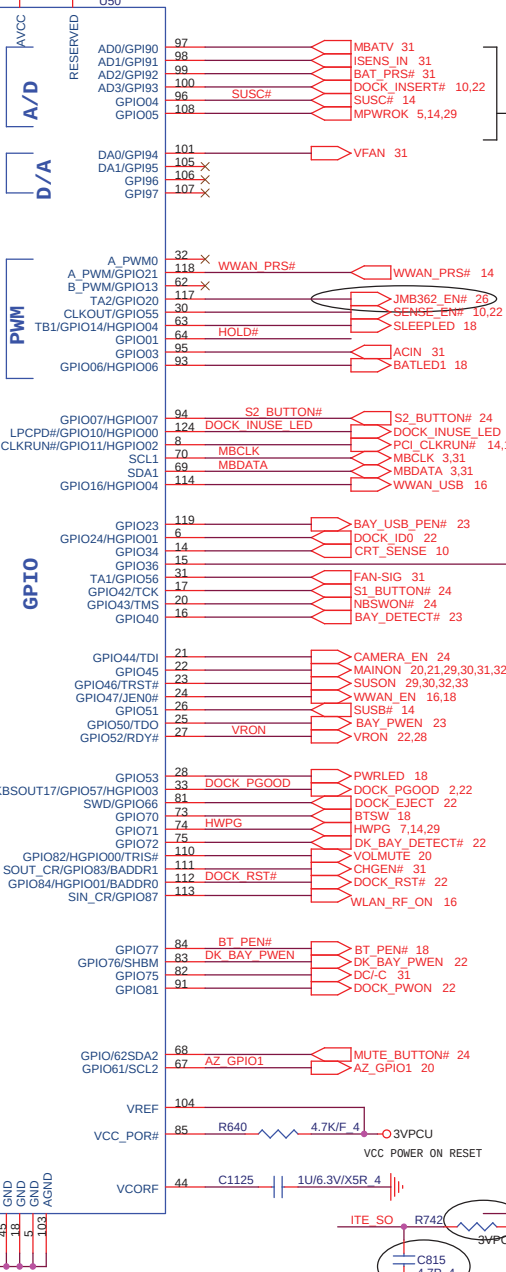
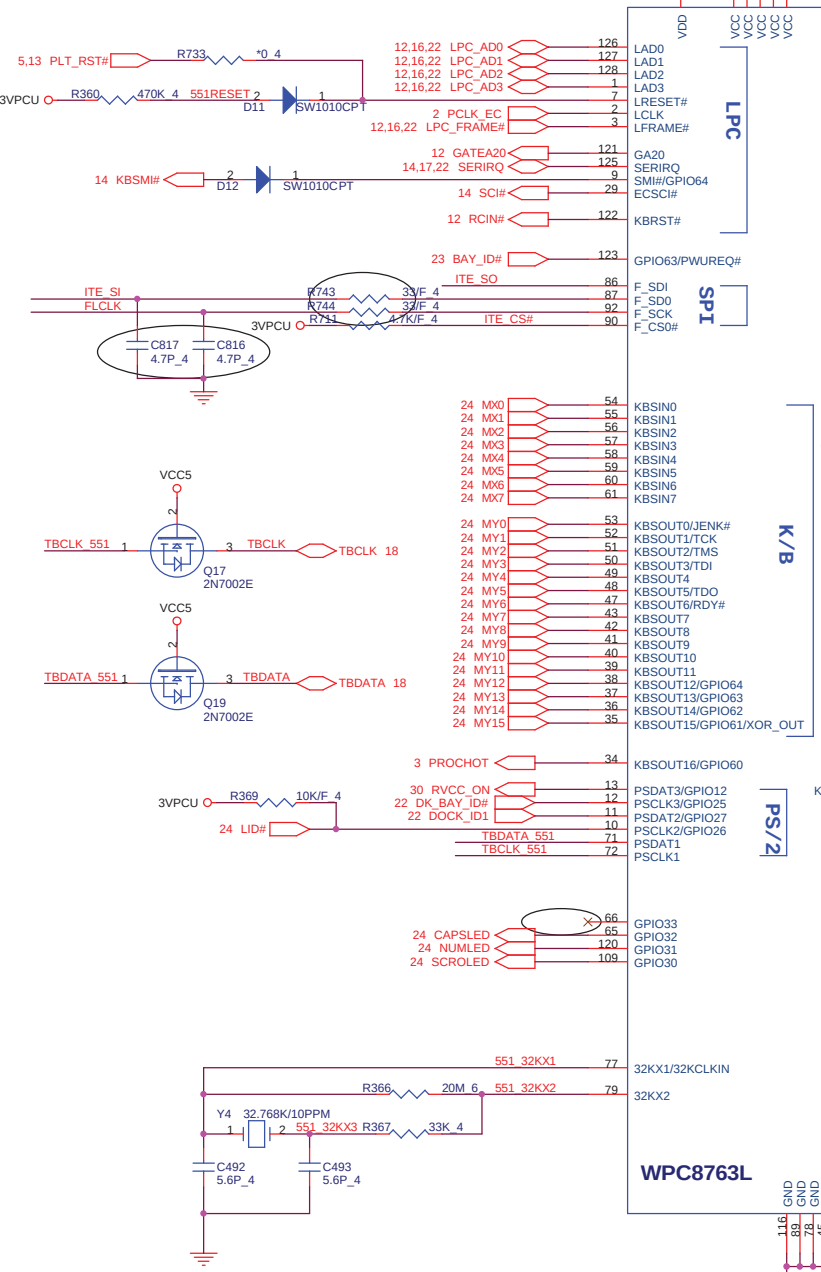
Rev 2A

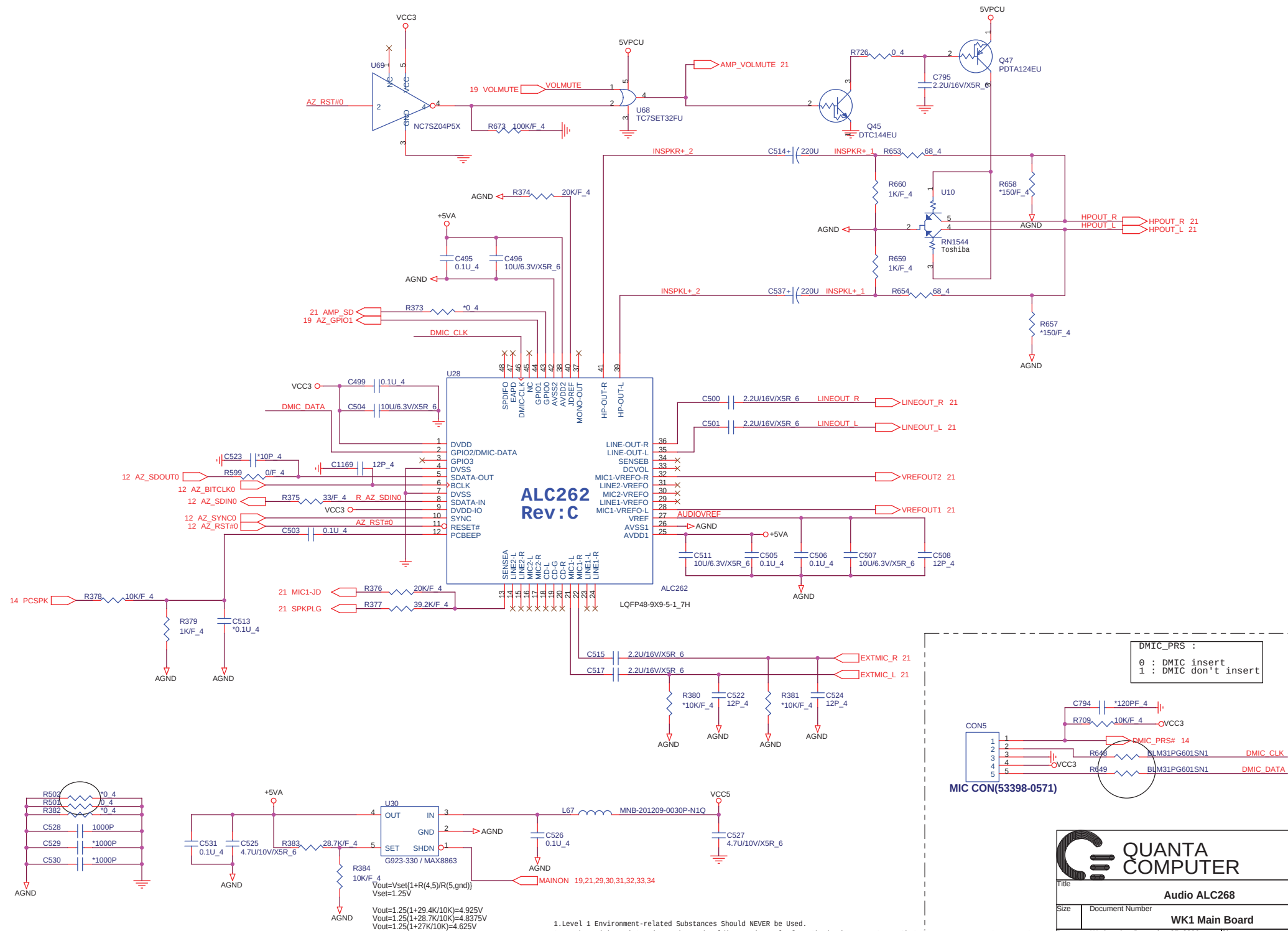
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0 (HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1	
0 1	XOR-TRF TEST	

SHMB: SHMB(If = 0 Enable share host BIOS memory)

DOCK_RST# : BADDR0
T?: BADDR1

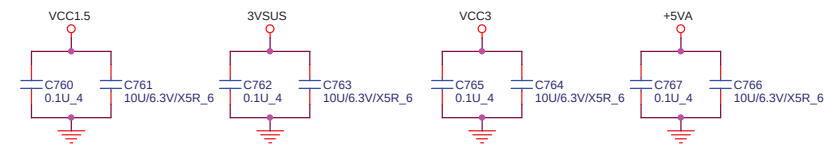
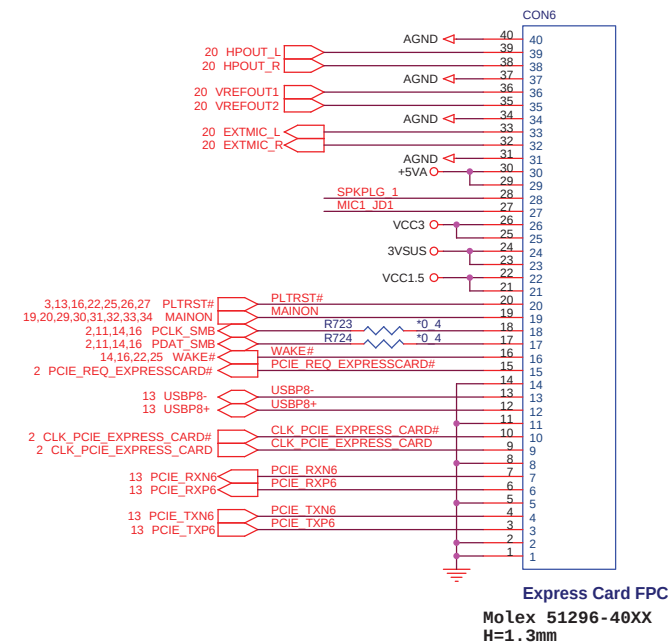
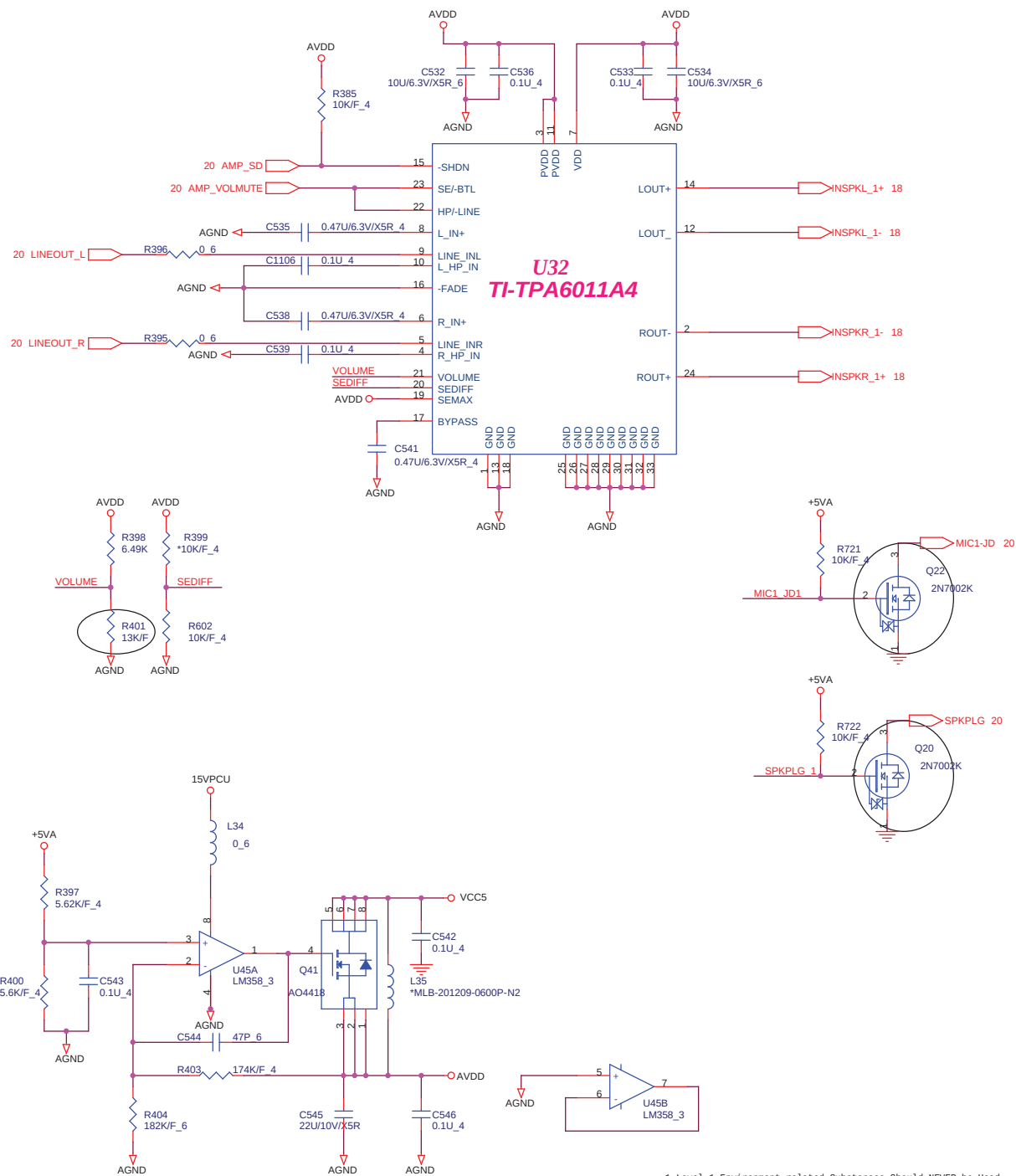




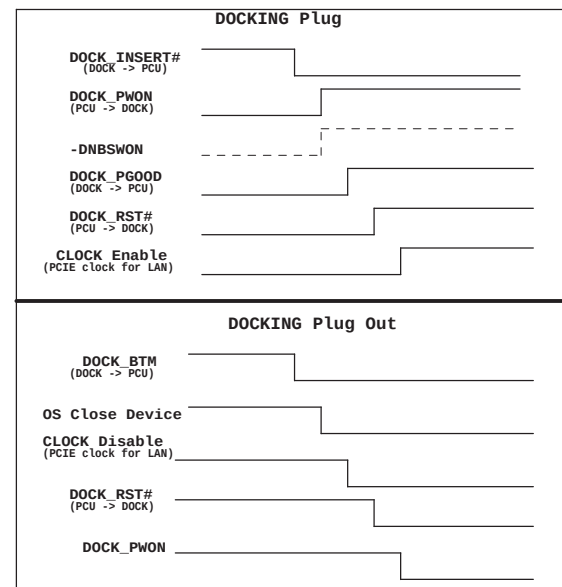
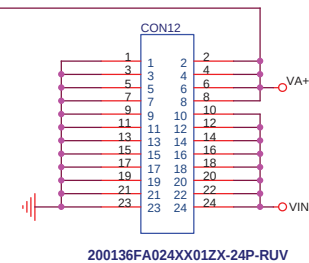
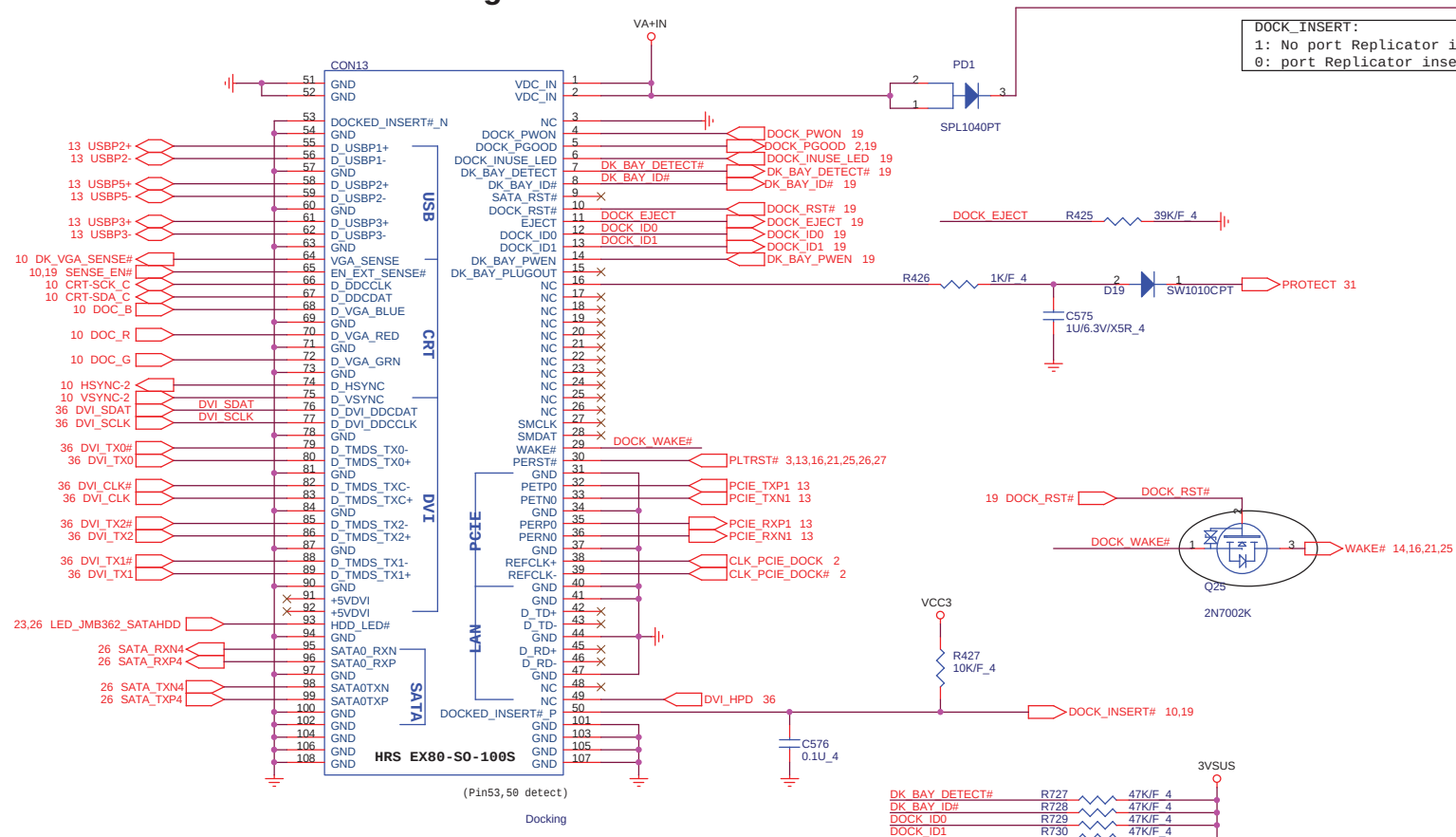
Title			Audio ALC268		
Size			Document Number		
			WK1 Main Board		
			Rev 2A		

Date: Wednesday, December 27, 2006 Sheet 20 of 39

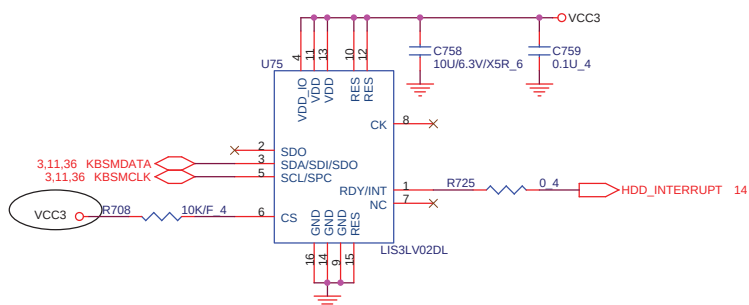
Audio amplifier



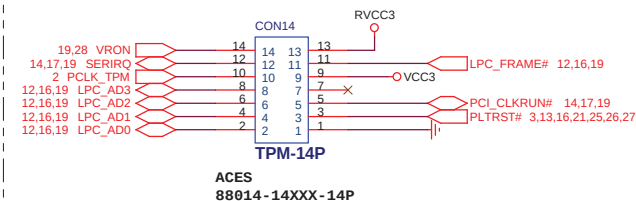
Docking



HDD PROTECT



TPM



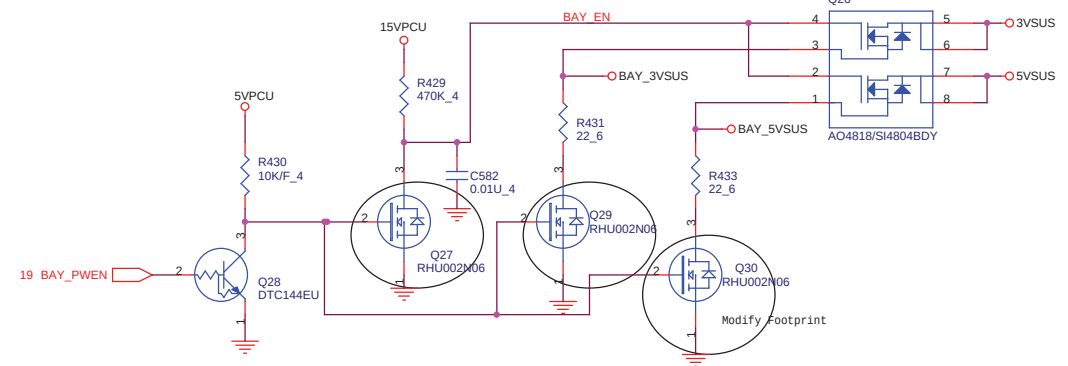
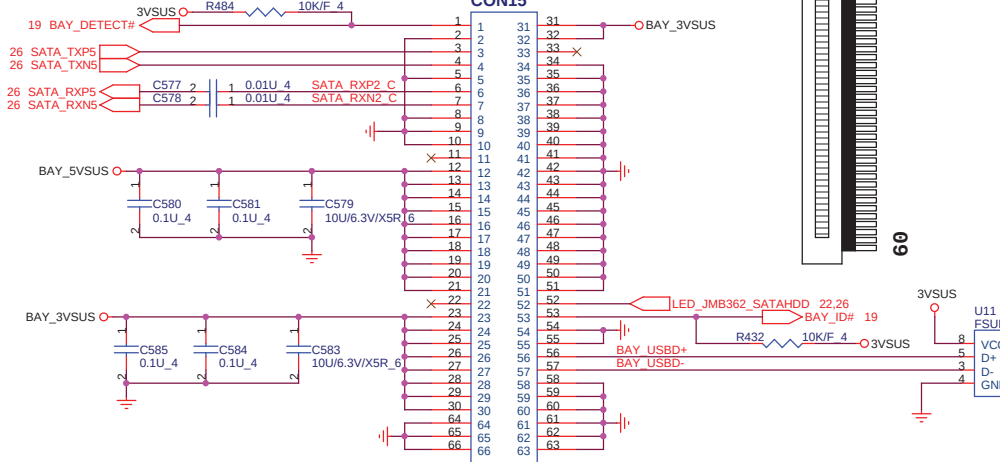
1. Level 1 Environment-related Substances Should NEVER be Used.
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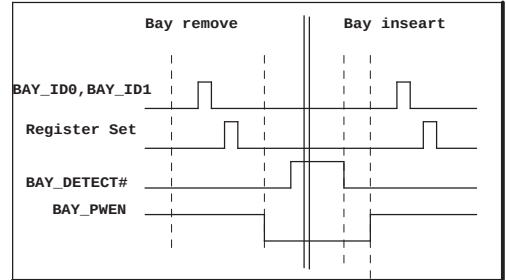
Title			
Docking/TPM			
Size	Document Number		Rev
	WK1 Main Board		2A
Date:	Wednesday, December 27, 2006	Sheet	22 of 39

BAY to ODD/HDD

BAY_CONNECTOR(500152FB060SX002X)
CON15

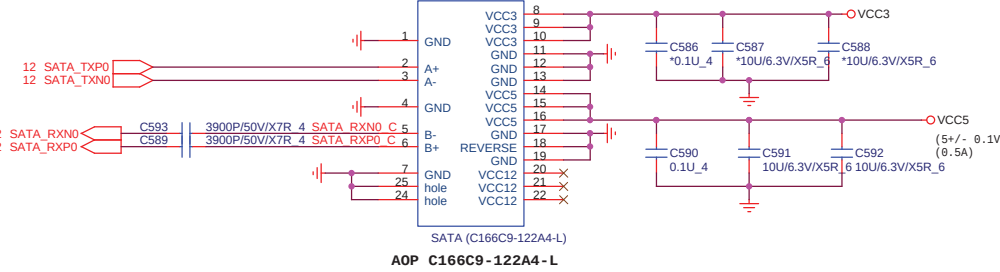


BAY_ID#	SATA Device	BAY_USB_PEN#
0	1	HI
1	2	LO

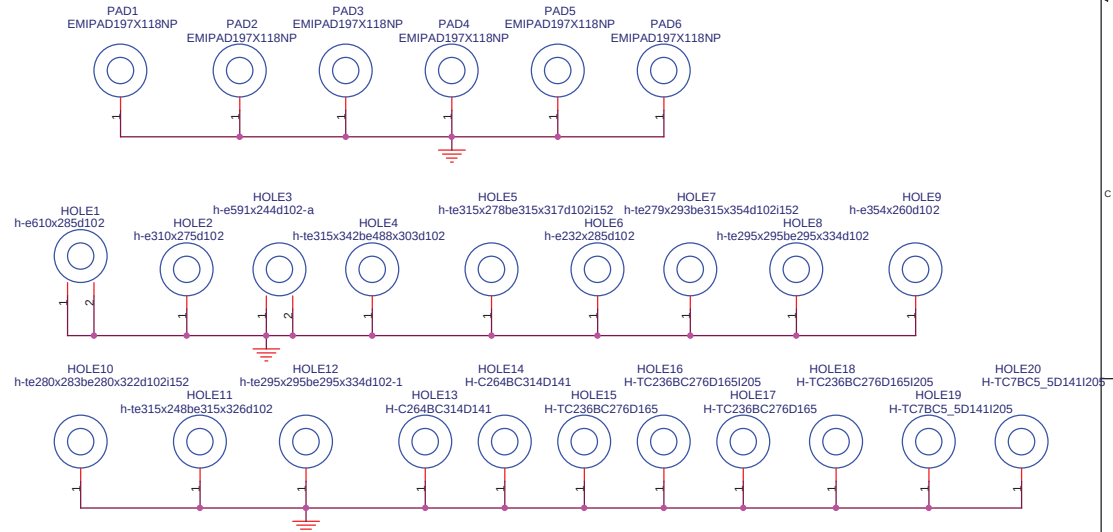


HDD CONNECTOR-1

CON16



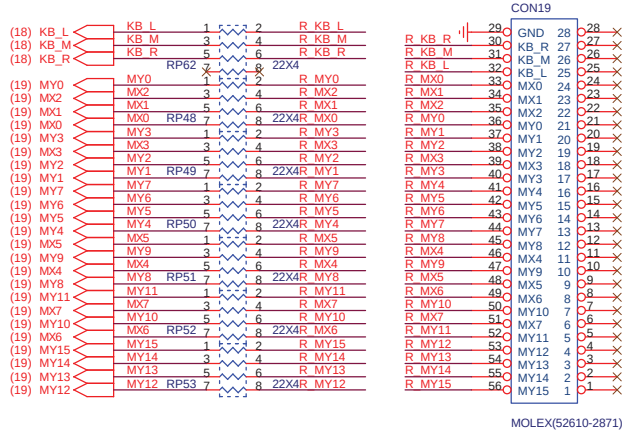
AOP C166C9-122A4-L



Title		
HDD/BAY		
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1.Level 1 Environment-related Substances Should NEVER be Used.
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KEYBOARD

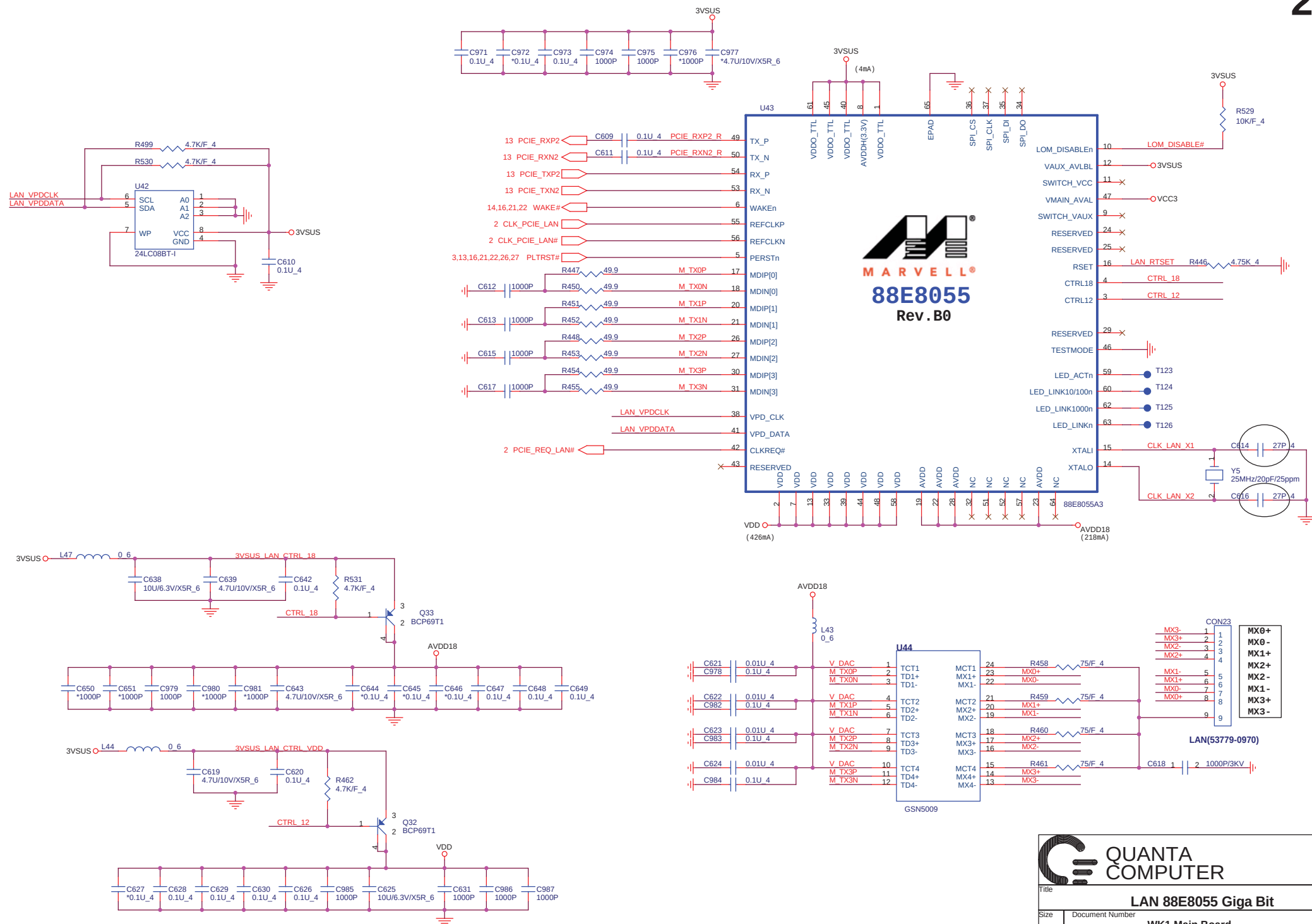




QUANTA
COMPUTER

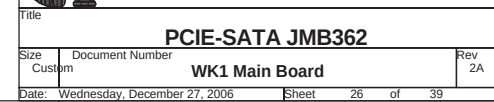
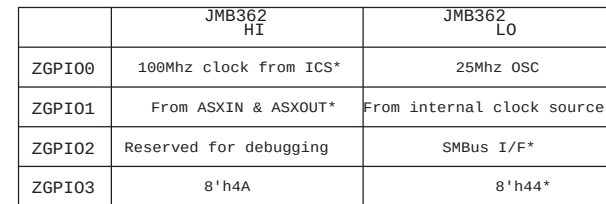
LAN 88E8055 Giga Bit

WK1 Main Board

Rev
2A

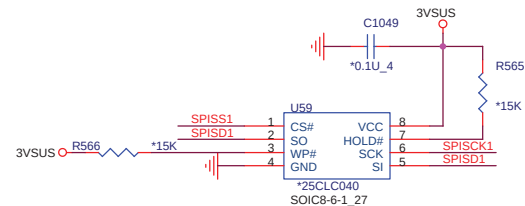
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2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



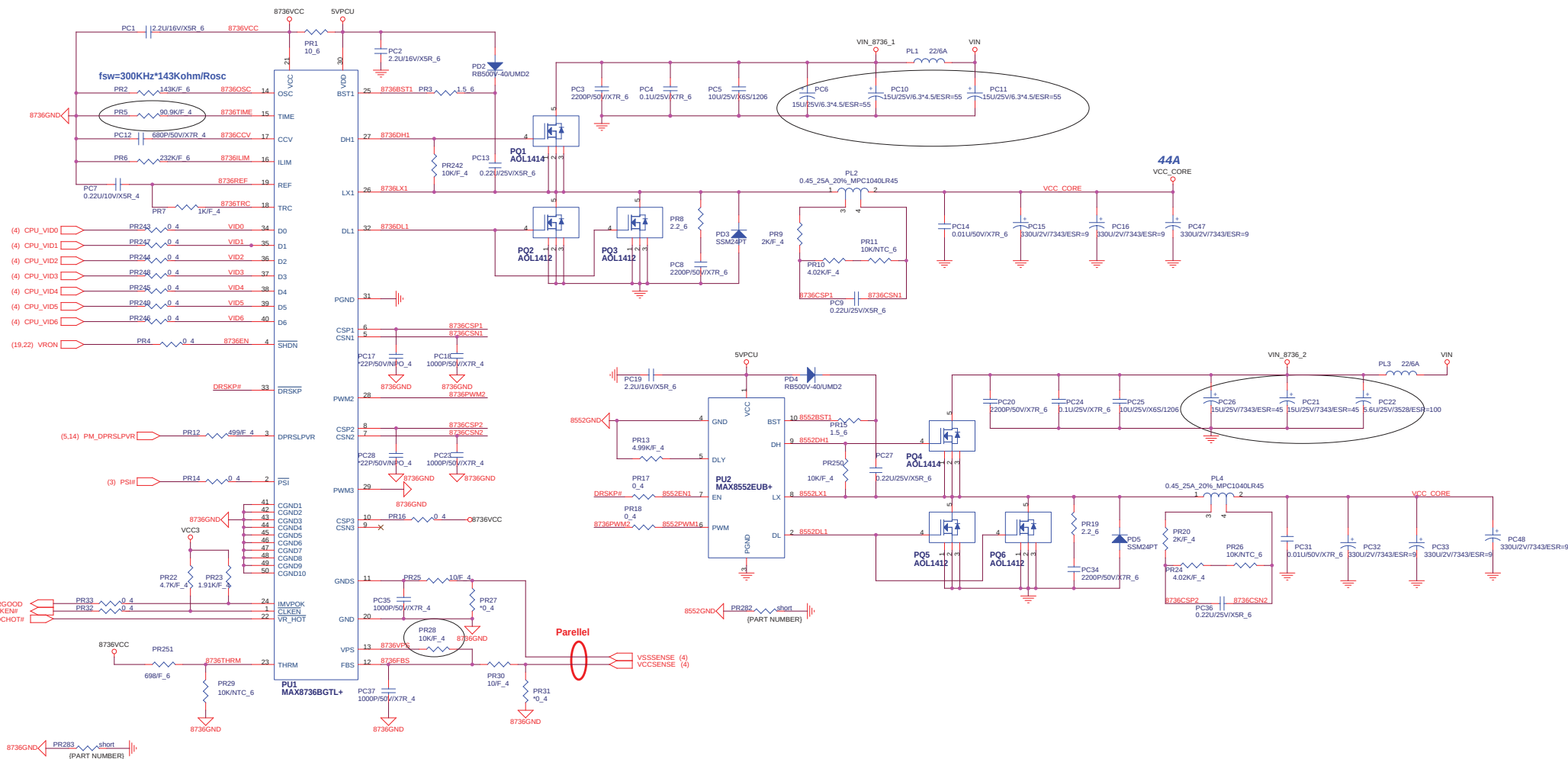
1. Level 1 Environment-related Substances should NEVER be Used.

2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



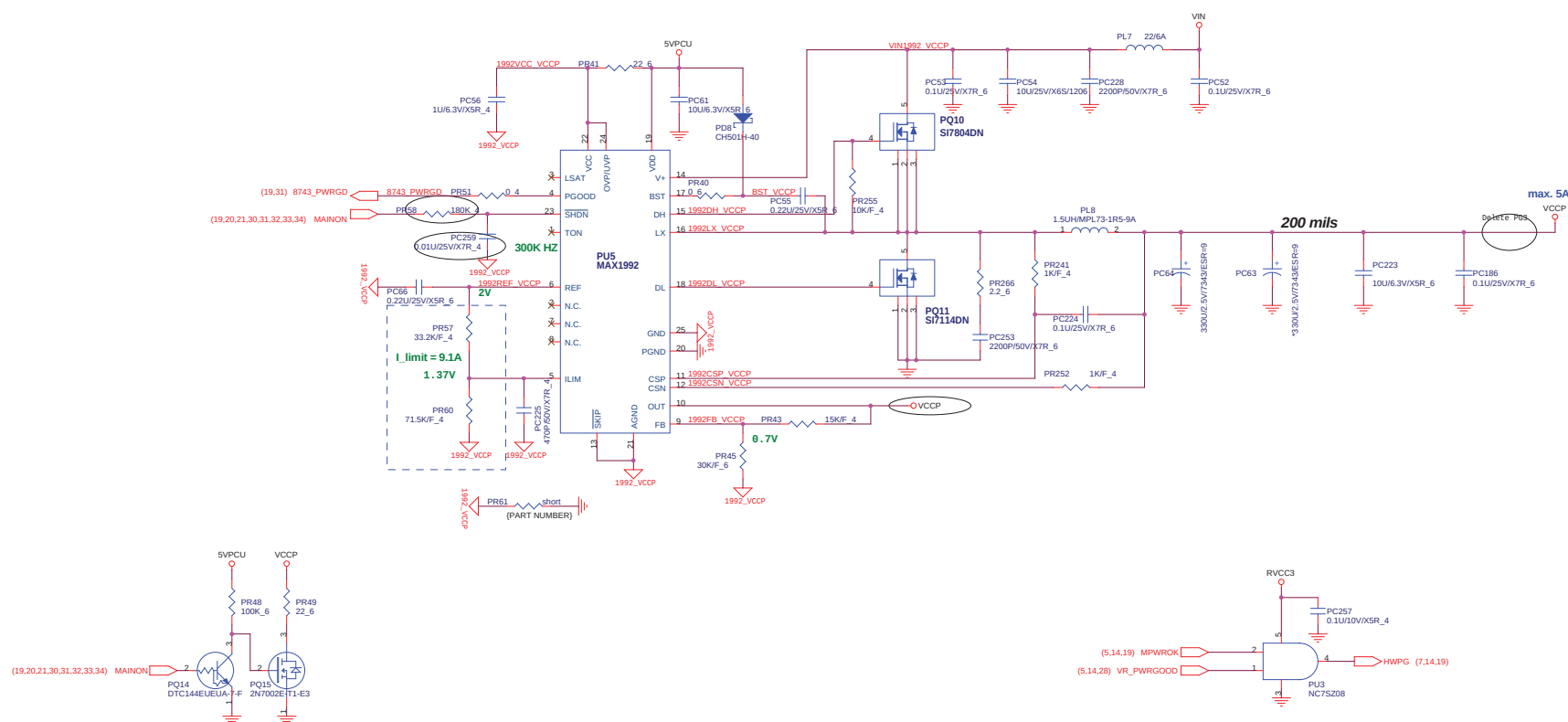
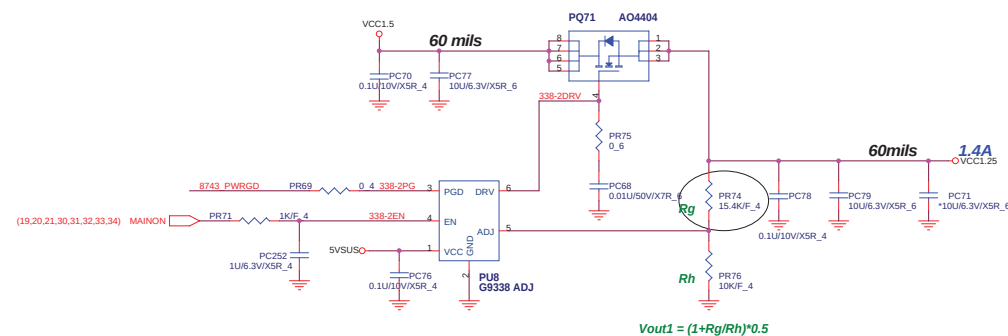
CPU CORE

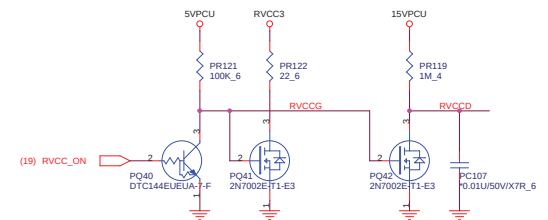
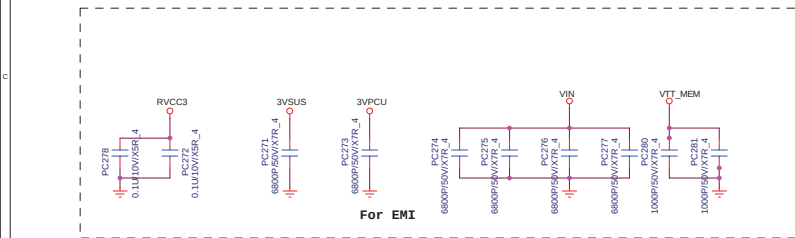
dV Target/dt=12.5mV/us*71.5kohm/R TIME

$$R_{ILIM(PK)} = 8V \cdot R_{TRC} / I(PK)_{LIMIT} \cdot R_{sense}$$


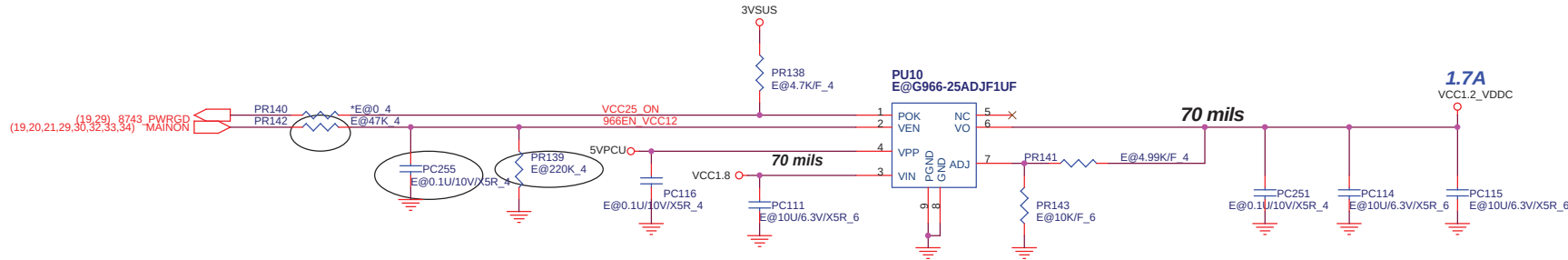
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

VCC1.5

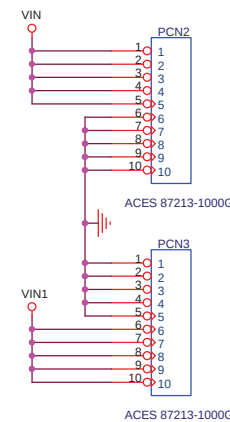
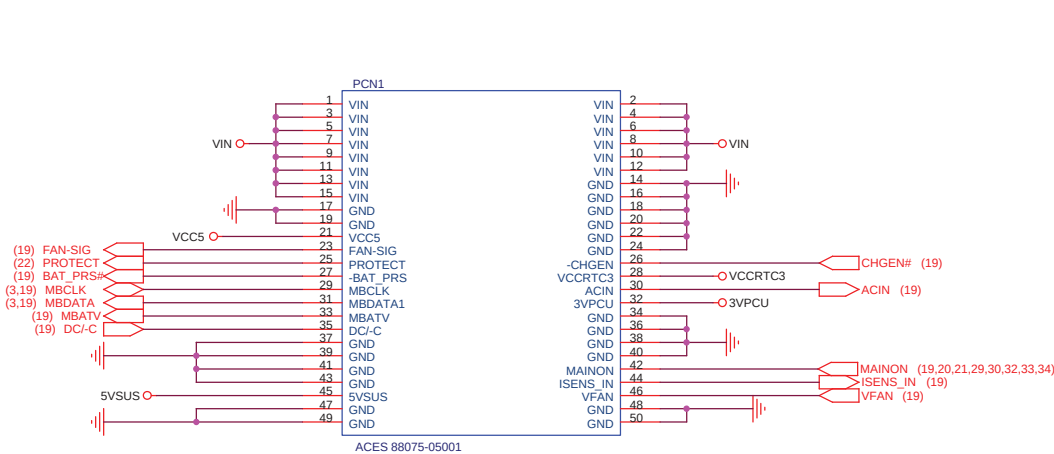
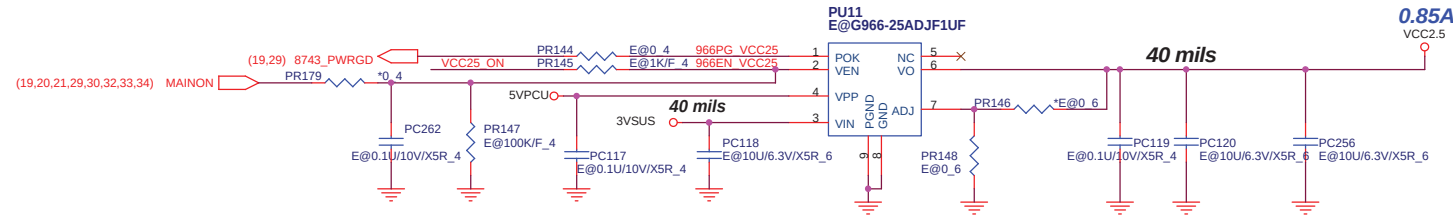




VCC1.2_VDDC



VCC2.5



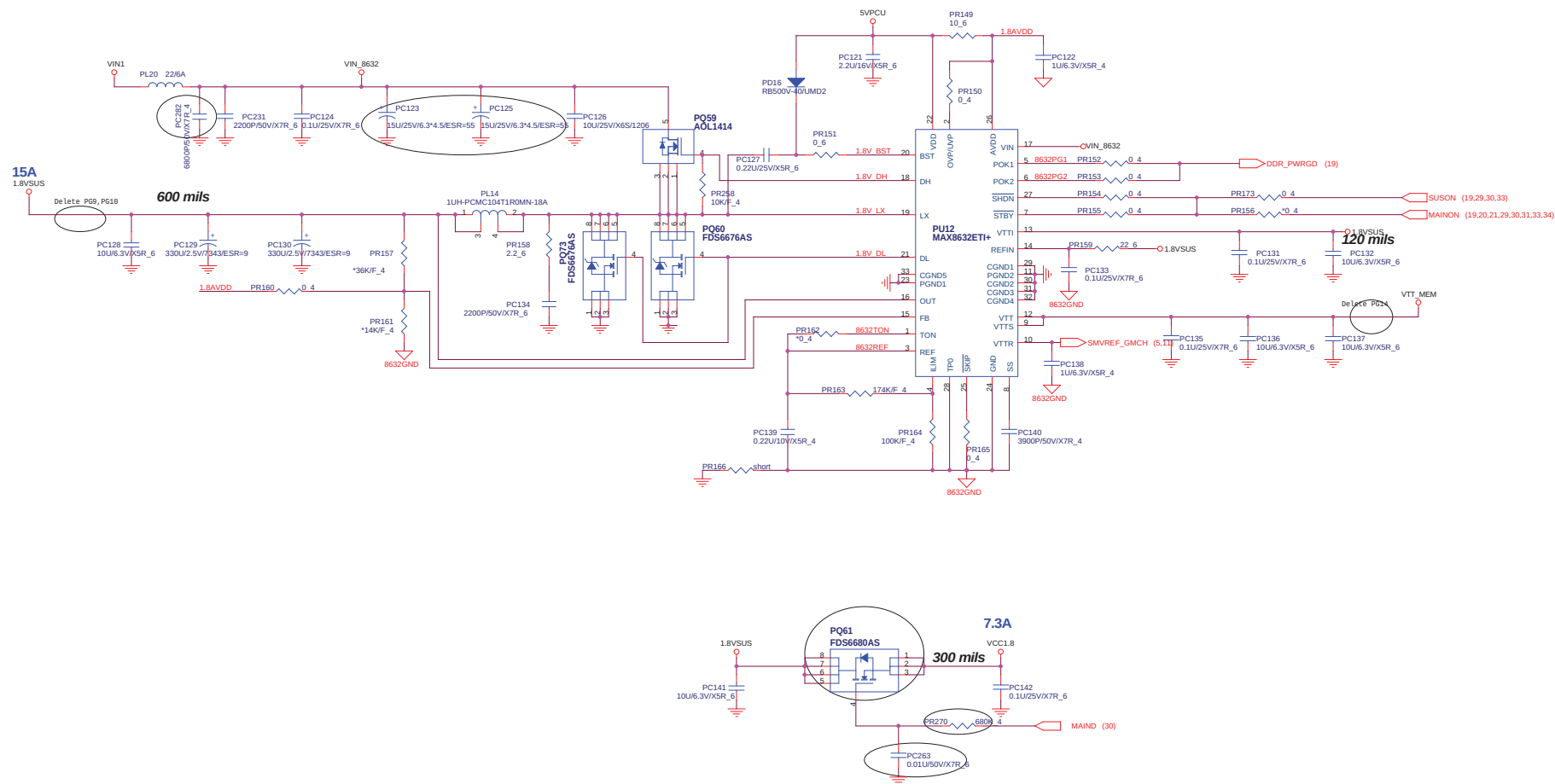


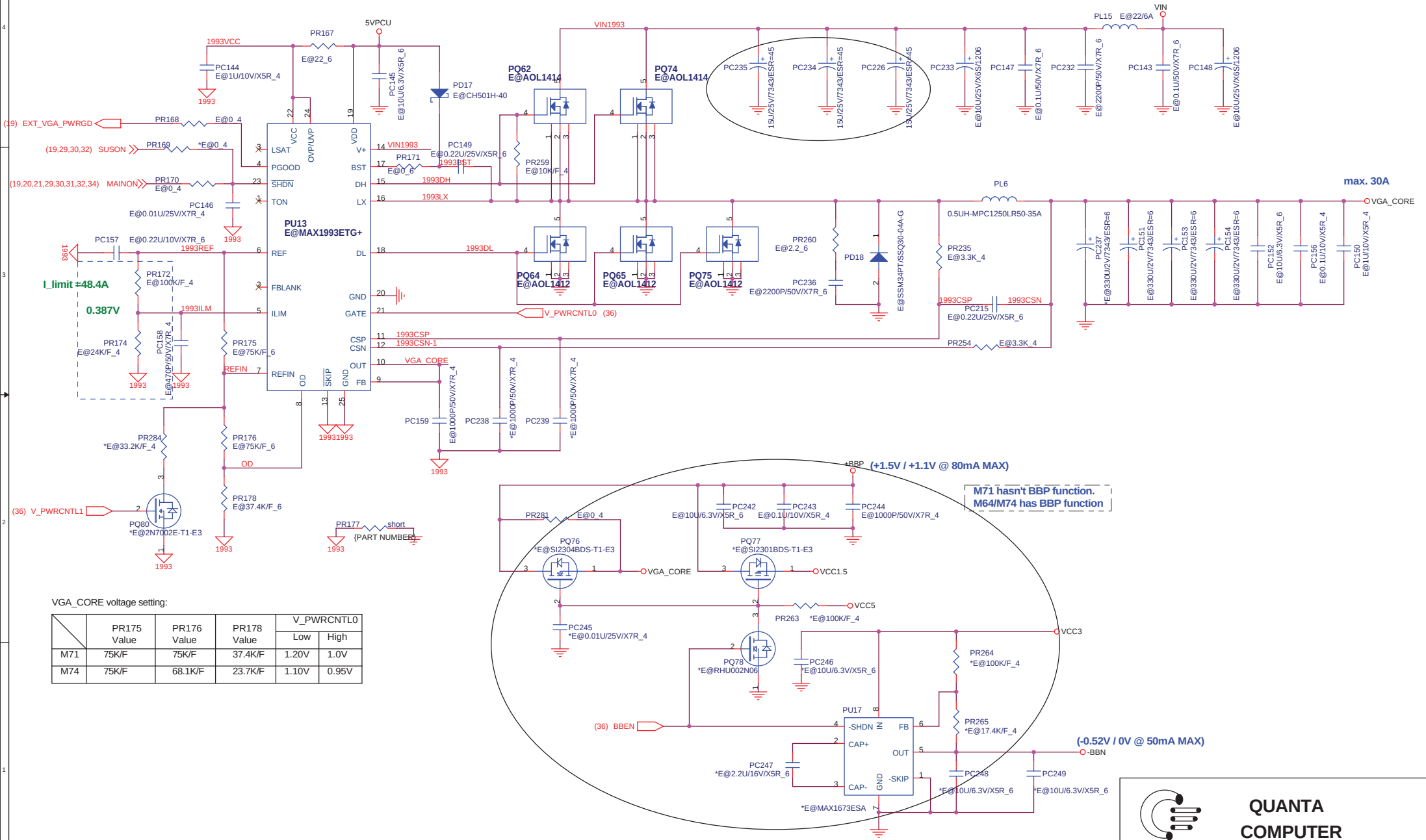
**QUANTA
COMPUTER**

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	WK1 Main Board	2A
Date:	Wednesday, December 27, 2006	Sheet 31 of 39

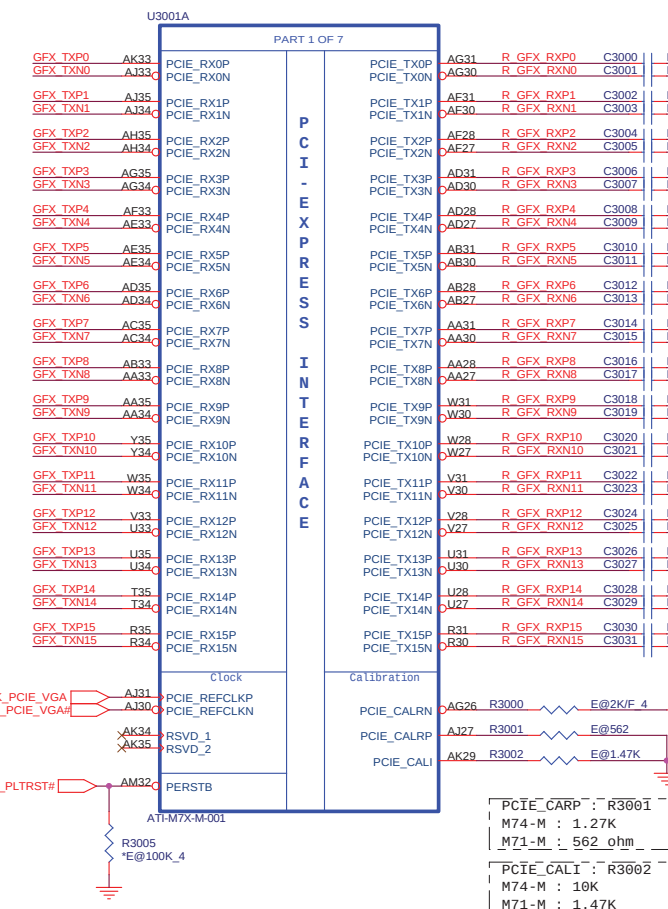
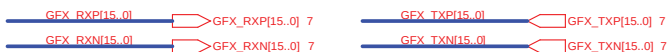
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1.8VSUS & VTT_MEM

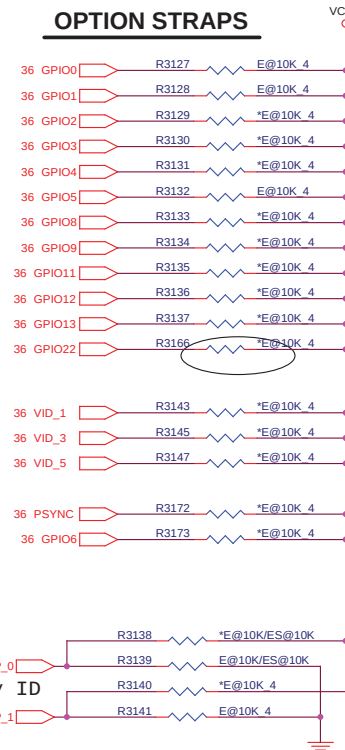




**QUANTA
COMPUTER**



OPTION STRAPS



M71/74-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing (recommended)	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB(Default) 001x - No ROM,MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	GPIO(9,13,12,11) 0000 (internal pull-down)
HDCP ROM Chip Select	GPIO22	A 10K external pull-up (3.3V) is required if a ROM is used.	0 (internal pull-down)
VIP_DEVICE	PSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	(DVPDATA_3 - 2)	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - Infineon 16M*32 – 2pcs(channelA) 11 - Samsung 16M*32- 2pcs(channelA)	(Default = 10)

MEMTYPE1	MEMTYPE0	R3124	R3125	R3122	R3123	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 8M x 32(AB - CD channel)
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3 : 8M x 32(AB - CD channel)
1	0	10K	NC	NC	10K	10 - Infineon 16M*32 - 2pcs(AB channel)
1	1	10K	NC	10K	NC	11 - Samsung 16M*32- 2pcs(AB channel)

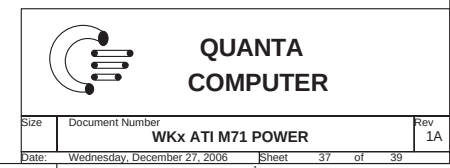


**QUANTA
COMPUTER**

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	WK1 ATI PCIE			
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1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



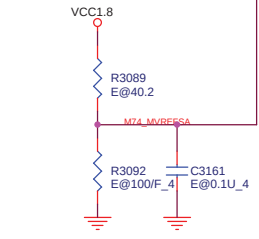
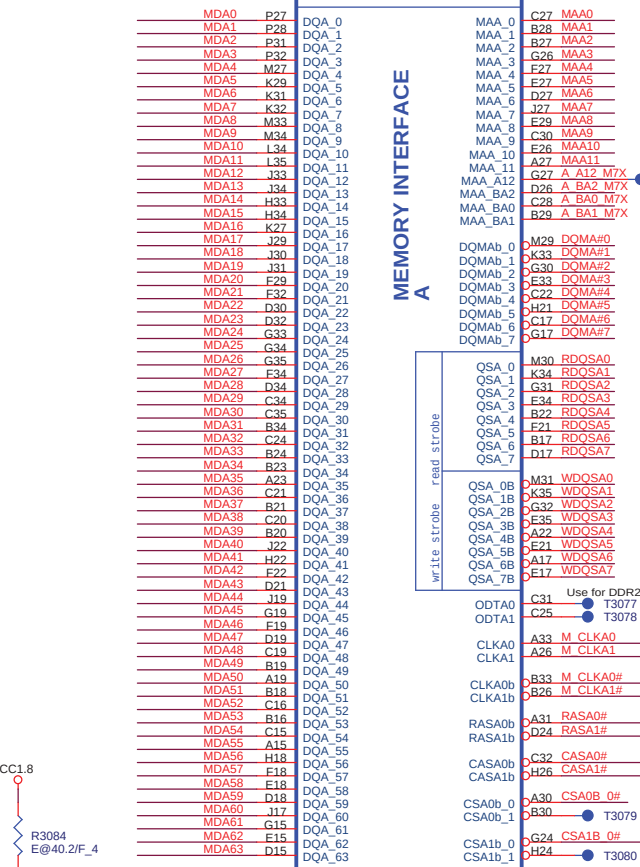


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Channel A

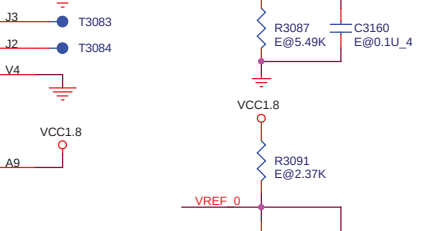
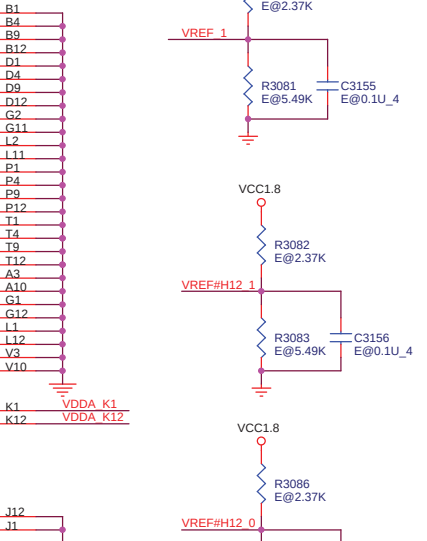
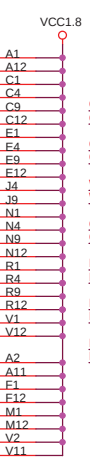
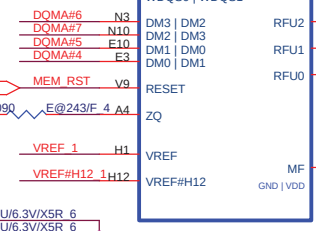
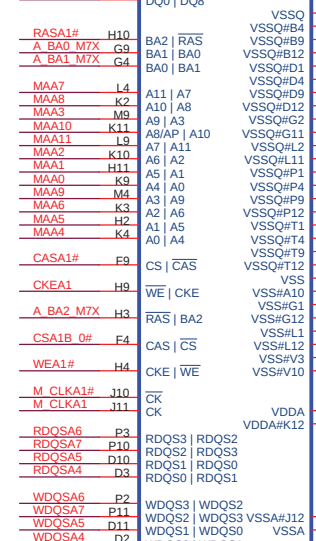
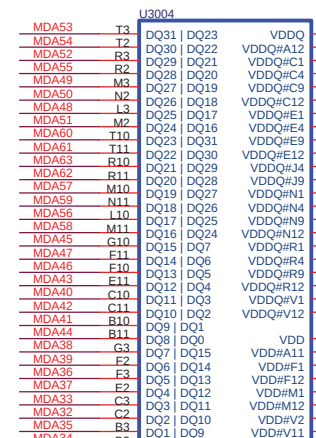
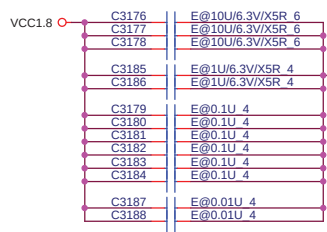
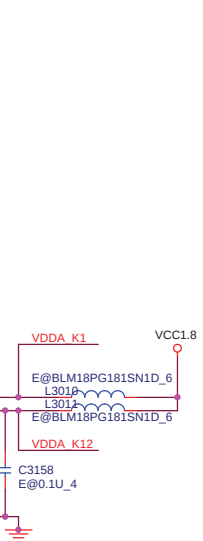
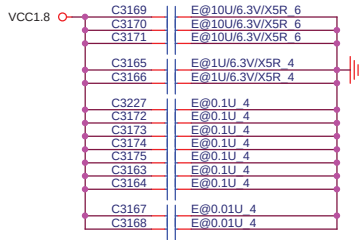
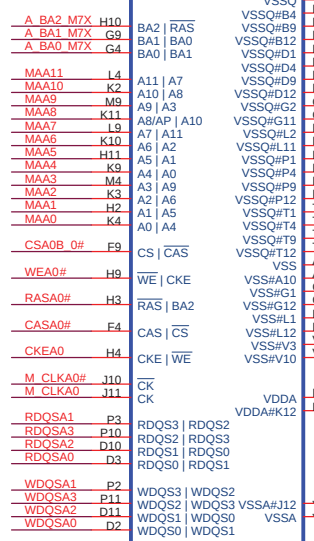
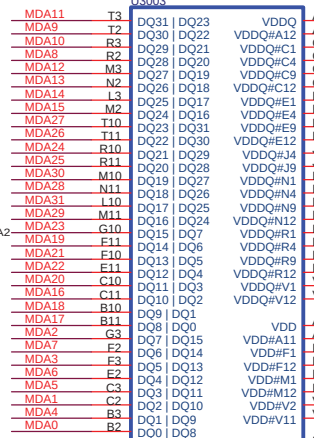
Part 3 of 7

MEMORY INTERFACE
A



Signal	DDR1,2	DDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R

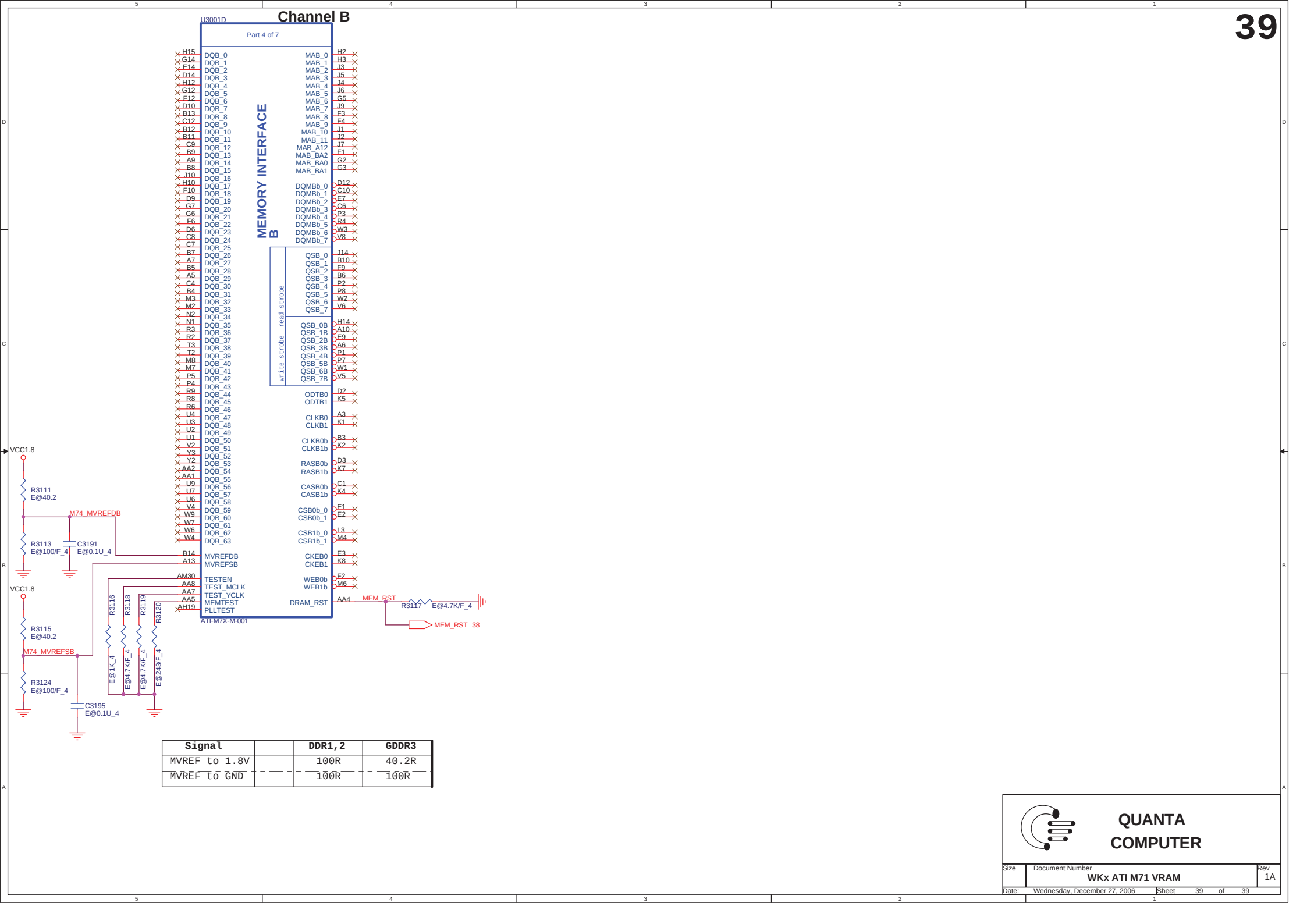
T3094
For 8 Banks MAA_13=BA2



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1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Signal		DDR1,2	GDDR3
MVREF to 1.8V	---	100R	40.2R
MVREF to GND	---	100R	100R