

Schematics Page Index (Title / Revision / Change Date)							
Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	0.20	06/5/22	36	DC_IN/Charger (MAX1909)	0.20	06/5/22
02	Block Diagram	0.20	06/5/22	37	SYSPWR(+3VALW/+5VALW)	0.20	06/5/22
03	Yonah(HOST BUS) 1/2	0.20	06/5/22	38	SYSPWR(+1_5VRUN/+1_05VRUN)	0.20	06/5/22
04	Yonah(HOST BUS) 2/3	0.20	06/5/22	39	VHCORE(ISL6262)	0.20	06/5/22
05	Yonah(Power/Gnd) 3/3	0.20	06/5/22	40	Others power plan	0.20	06/5/22
06	CALISTOGA (HOST) 1/7	0.20	06/5/22	41	OVP protection	0.20	06/5/22
07	CALISTOG (DMI) 2/7	0.20	06/5/22	42	DDR2PWR(+1_8V_SUS/+0_9VRUN)	0.20	06/5/22
08	CALIST (GRAPHIC) 3/7	0.20	06/5/22	43	CLOCK GEN	0.20	06/5/22
09	CALISTOGA (DDRII) 4/7	0.20	06/5/22	44	HOLE	0.20	06/5/22
10	CALIST (POWER,VCC) 5/7	0.20	06/5/22	45	POWER SEQUENCE	0.20	06/5/22
11	CALIST (VCC CORE) 6/7	0.20	06/5/22	46	History	0.20	06/5/22
12	CALIST (VSS) 7/7	0.20	06/5/22	47	History	0.20	06/5/22
13	DDRII(S0-DIMM_0) 1/3	0.20	06/5/22				
14	DDRII(S0-DIMM_1) 2/3	0.20	06/5/22				
15	DDRII(Termination) 3/3	0.20	06/5/22				
16	LVDS / S_VIDEO	0.20	06/5/22				
17	ICH7-M(PCI/USB) 1/5	0.20	06/5/22				
18	ICH7-M(LPC,IDE,SATA)2/5	0.20	06/5/22				
19	ICH7-M(GPIO) 3/5	0.20	06/5/22				
20	ICH7-M(POWER) 4/5	0.20	06/5/22				
21	ICH7-M(GND) 5/5	0.20	06/5/22				
22	SATA HDD/CD-ROM	0.20	06/5/22				
23	EC+KBC	0.20	06/5/22				
24	Flash ROM/XBUS	0.20	06/5/22				
25	Mini_Card/BT	0.20	06/5/22				
26	FAN/HW THERMAL PROTECT	0.20	06/5/22				
27	EXPRESS/OIDE/TP	0.20	06/5/22				
28	PCI (PCI BUS)	0.20	06/5/22				
29	PCI (ILINK)	0.20	06/5/22				
30	PCI (MS)	0.20	06/5/22				
31	PCI (PCMCIA)	0.20	06/5/22				
32	USB2.0	0.20	06/5/22				
33	CRT	0.20	06/5/22				
34	DB CONNS & LED	0.20	06/5/22				
35	Power Design Diagram	0.20	06/5/22				

PCB P/N:

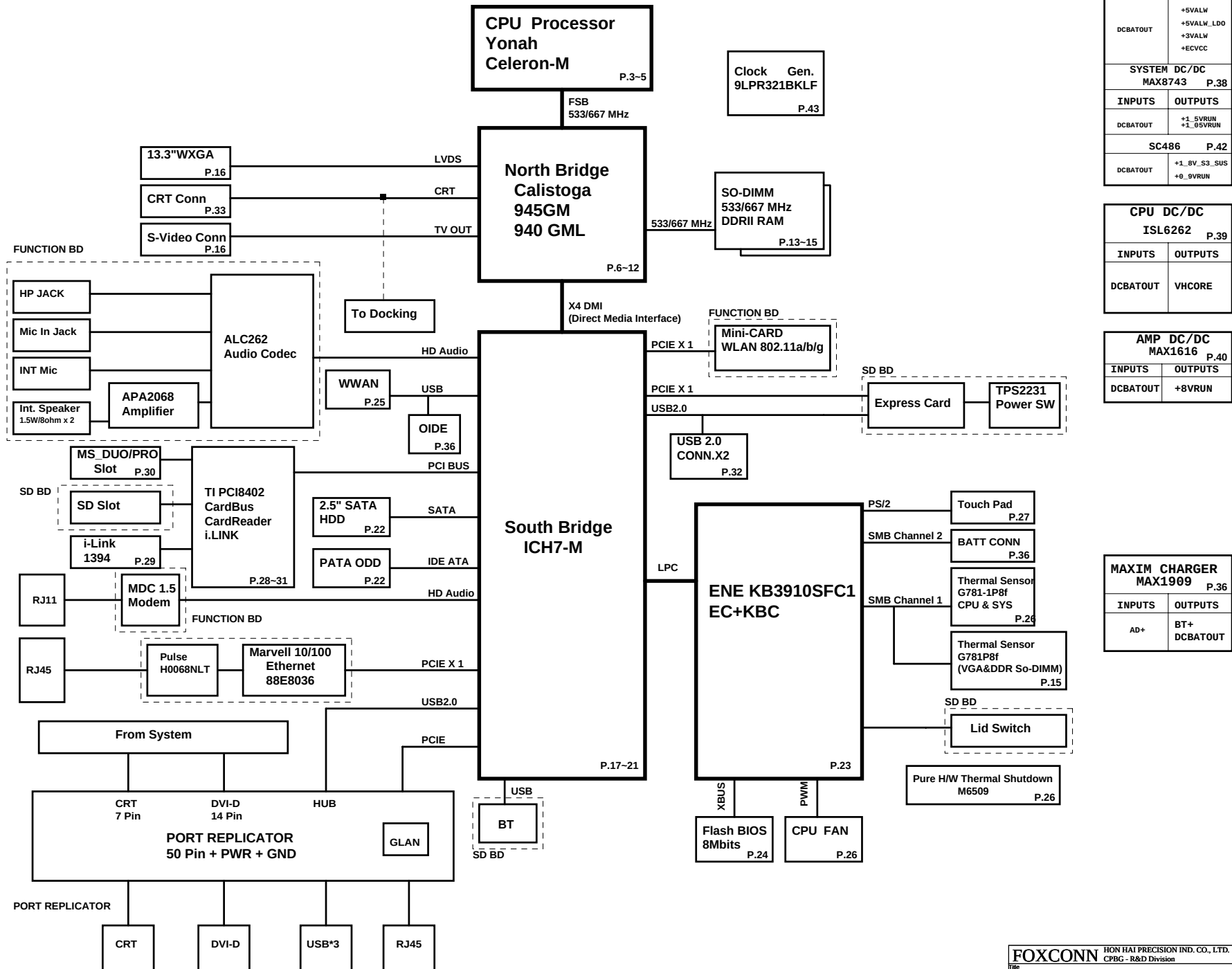
1P-0065102-80SA - FUBAI
1P-0065201-80SA - NANYA
1P-0065503-80SA - HANNSTAR

Project Code & Schematics Subject: MS60-L Main Board

P. Leader	Check by	Design by

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title Index Page		
Size	Document Number	Rev
Custom	MS60-1-05 (MBX-163)	0.20
Date:	Monday, June 19, 2006	Sheet 1 of 47

MS60 (CALISTOGA GM Block Diagram)



SYSTEM DC/DC MAX8734 P.3	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LD +3VALW +ECVCC
SYSTEM DC/DC MAX8743 P.3	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486 P.4	
DCBATOUT	+1_8V_S3_SU +0_9VRUN

CPU DC/DC ISL6262 P.3	
INPUTS	OUTPUTS
DCBATOUT	VH CORE

AMP DC/DC MAX1616 P.4	
INPUTS	OUTPUTS
DCBATOUT	+8V _{RUN}

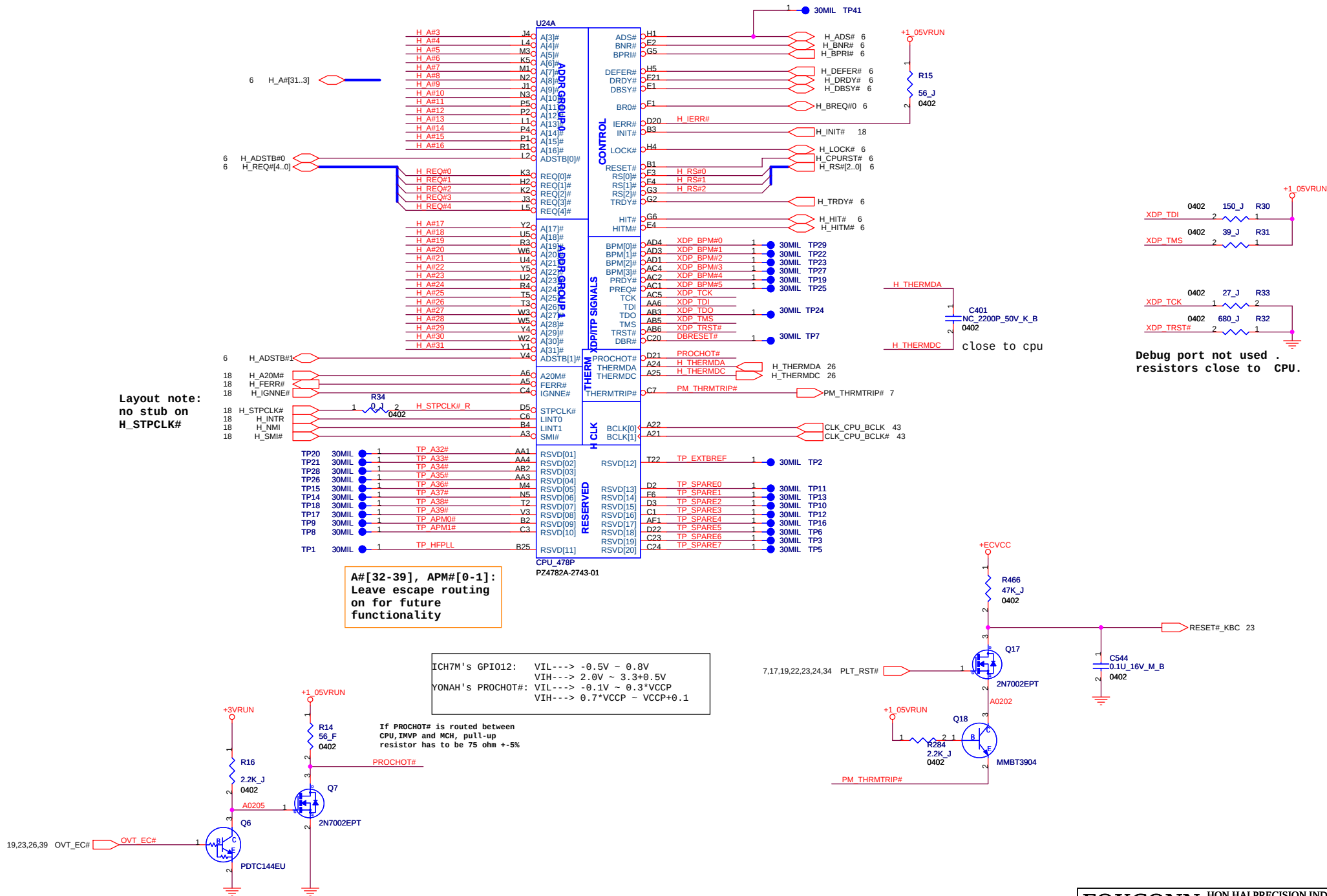
MAXIM CHARGER MAX1909 P.3	
INPUTS	OUTPUTS
AD+	BT+ DCBATOU

Layout note:
no stub on
H_STPCLK#

A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPI012: VIL --- -0.5V ~ 0.8V
VIH --- 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL --- -0.1V ~ 0.3*VCCP
VIH --- 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU, IMVP and MCH, pull-up
resistor has to be 75 ohm +-5%



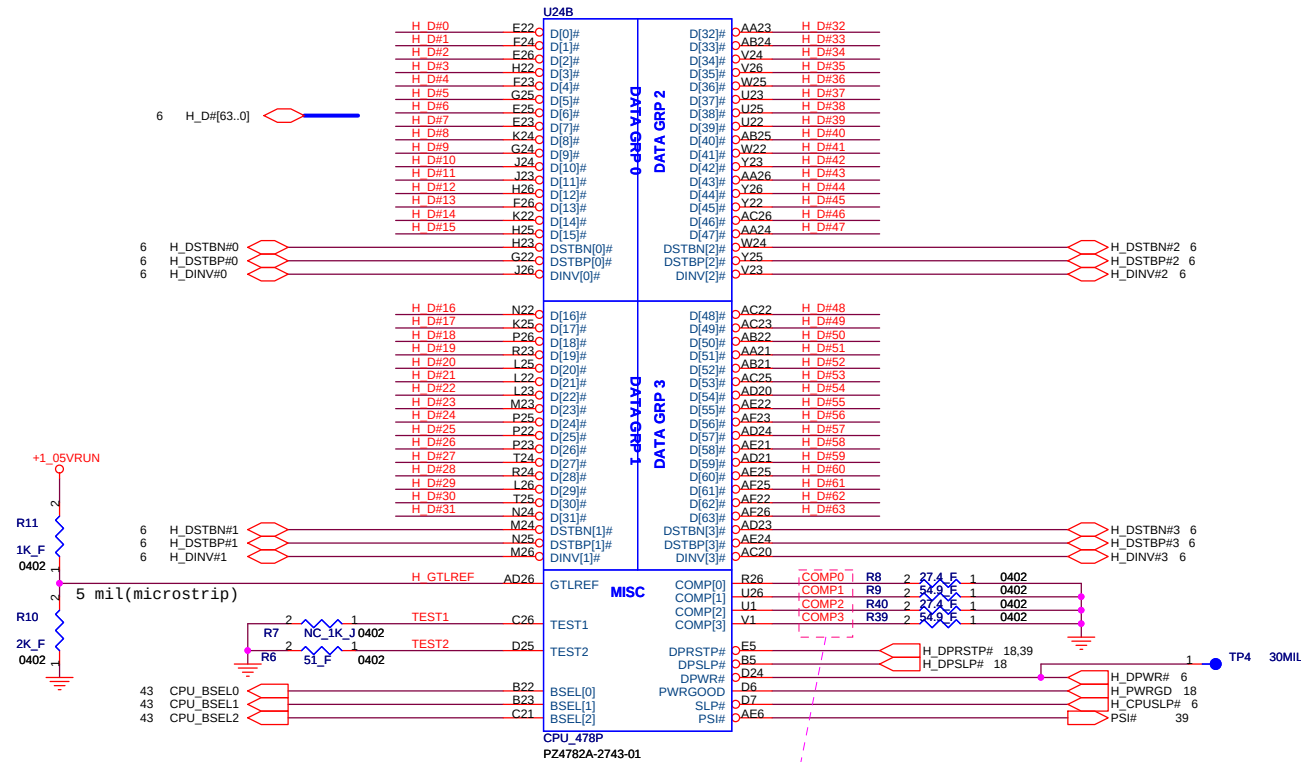
Place close to CPU

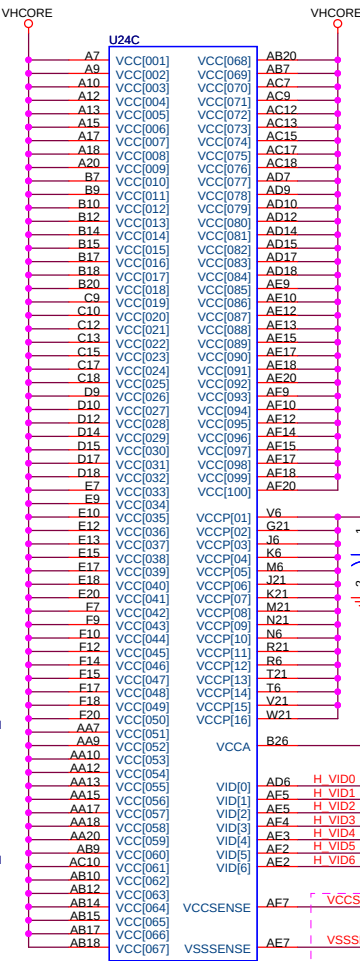
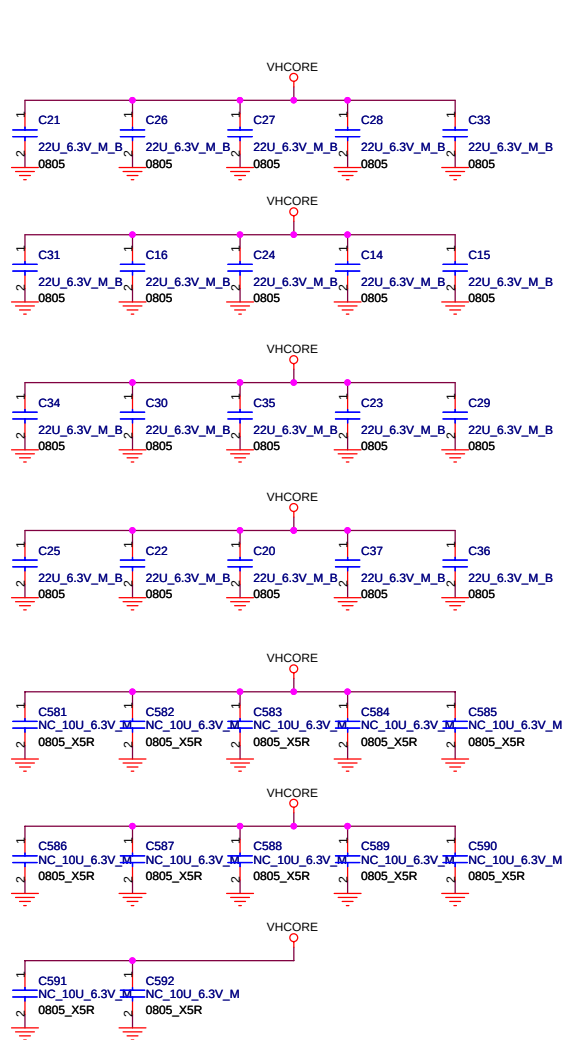
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

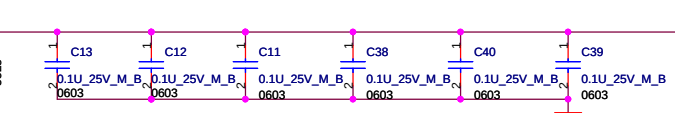
BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".



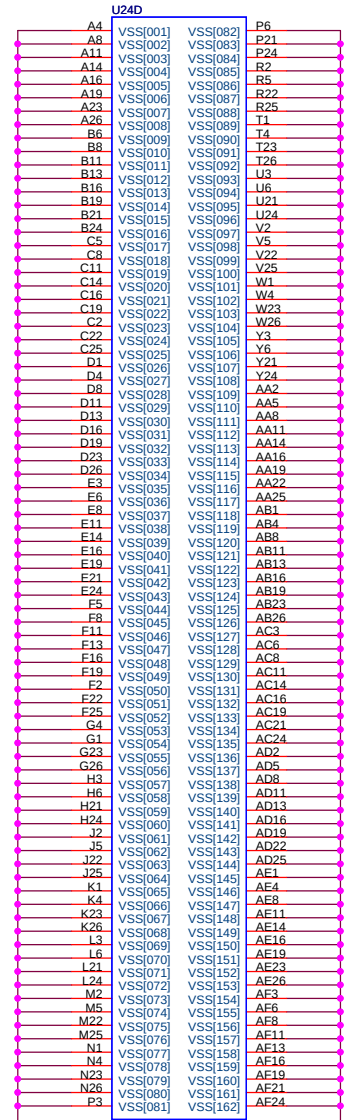


CPU_VCCA---->130mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A for Yona
 44A for Merom

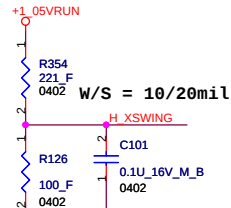
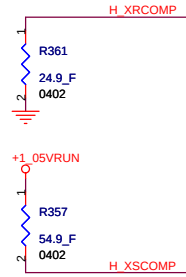


maximum current is 130mA for CPU_VCCA in Merom
 and 600A/us slew rate for CPU_VCCA

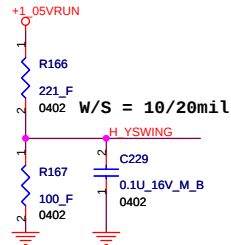
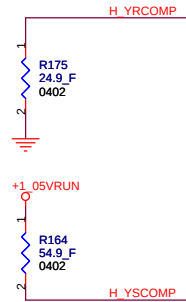
Layout Note: Route
 VCCSENSE traces at 27.4
 Ohms with 50 mil spacing.
 Place PU and PD within 1
 inch of cpu.
 width=18 mil
 spacing=7 mil



W/S = 10/20mil



W/S = 10/20mil



4 H_D#[63..0]

H_D#[63..0]

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA2	H_D#_43
H_D#44	AA6	H_D#_44
H_D#45	AA10	H_D#_45
H_D#46	Y8	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING

43 CLK_MCH_BCLK#

43 CLK_MCH_BCLK#

H_CLKIN	AG2	H_CLKIN
H_CLKIN#	AG1	H_CLKIN#

GM Q688CGM 12-0688CGM-0000
PM Q688CPM 12-0688CPM-0000
GML 9406GML-QK60-A3 12-9406GML0-A300

HOST

H_A#_3	H_A#3	H_A#_3
H_A#_4	H_A#4	H_A#_4
H_A#_5	H_A#5	H_A#_5
H_A#_6	H_A#6	H_A#_6
H_A#_7	H_A#7	H_A#_7
H_A#_8	H_A#8	H_A#_8
H_A#_9	H_A#9	H_A#_9
H_A#_10	H_A#10	H_A#_10
H_A#_11	H_A#11	H_A#_11
H_A#_12	H_A#12	H_A#_12
H_A#_13	H_A#13	H_A#_13
H_A#_14	H_A#14	H_A#_14
H_A#_15	H_A#15	H_A#_15
H_A#_16	H_A#16	H_A#_16
H_A#_17	H_A#17	H_A#_17
H_A#_18	H_A#18	H_A#_18
H_A#_19	H_A#19	H_A#_19
H_A#_20	H_A#20	H_A#_20
H_A#_21	H_A#21	H_A#_21
H_A#_22	H_A#22	H_A#_22
H_A#_23	H_A#23	H_A#_23
H_A#_24	H_A#24	H_A#_24
H_A#_25	H_A#25	H_A#_25
H_A#_26	H_A#26	H_A#_26
H_A#_27	H_A#27	H_A#_27
H_A#_28	H_A#28	H_A#_28
H_A#_29	H_A#29	H_A#_29
H_A#_30	H_A#30	H_A#_30
H_A#_31	H_A#31	H_A#_31

H_ADS#	3	H_ADS#
H_ADSTB#_0	3	H_ADSTB#_0
H_ADSTB#_1	3	H_ADSTB#_1
H_BNR#	3	H_BNR#
H_BPR#	3	H_BPR#
H_BREQ#0	3	H_BREQ#0
H_CPURST#	3	H_CPURST#
H_DBSTY#	3	H_DBSTY#
H_DEFER#	3	H_DEFER#
H_DPWR#	4	H_DPWR#
H_DRDY#	3	H_DRDY#
H_VREF_1	3	H_VREF_1

H_DINV#_0	4	H_DINV#_0
H_DINV#_1	4	H_DINV#_1
H_DINV#_2	4	H_DINV#_2
H_DINV#_3	4	H_DINV#_3

H_DSTBN#_0	4	H_DSTBN#_0
H_DSTBN#_1	4	H_DSTBN#_1
H_DSTBN#_2	4	H_DSTBN#_2
H_DSTBN#_3	4	H_DSTBN#_3

H_DSTBP#_0	4	H_DSTBP#_0
H_DSTBP#_1	4	H_DSTBP#_1
H_DSTBP#_2	4	H_DSTBP#_2
H_DSTBP#_3	4	H_DSTBP#_3

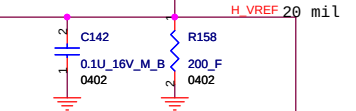
H_HIT#	3	H_HIT#
H_HITM#	3	H_HITM#
H_LOCK#	3	H_LOCK#

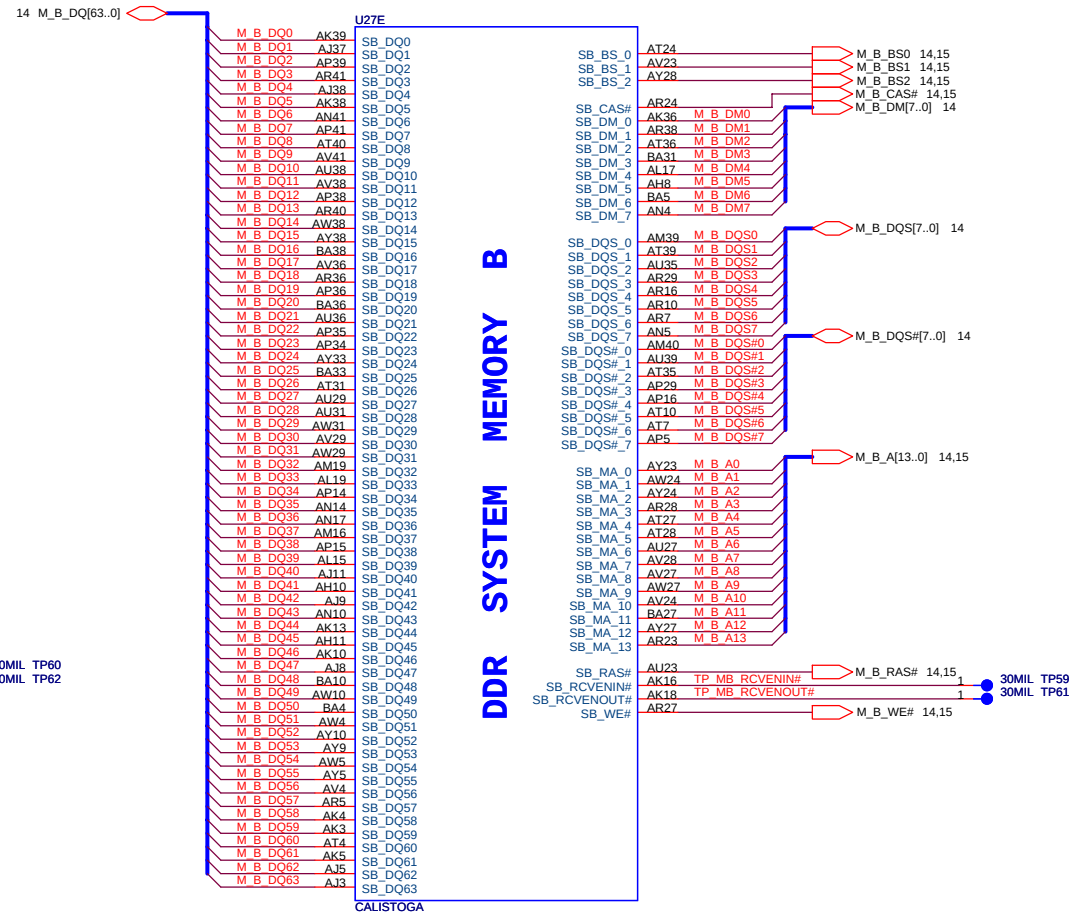
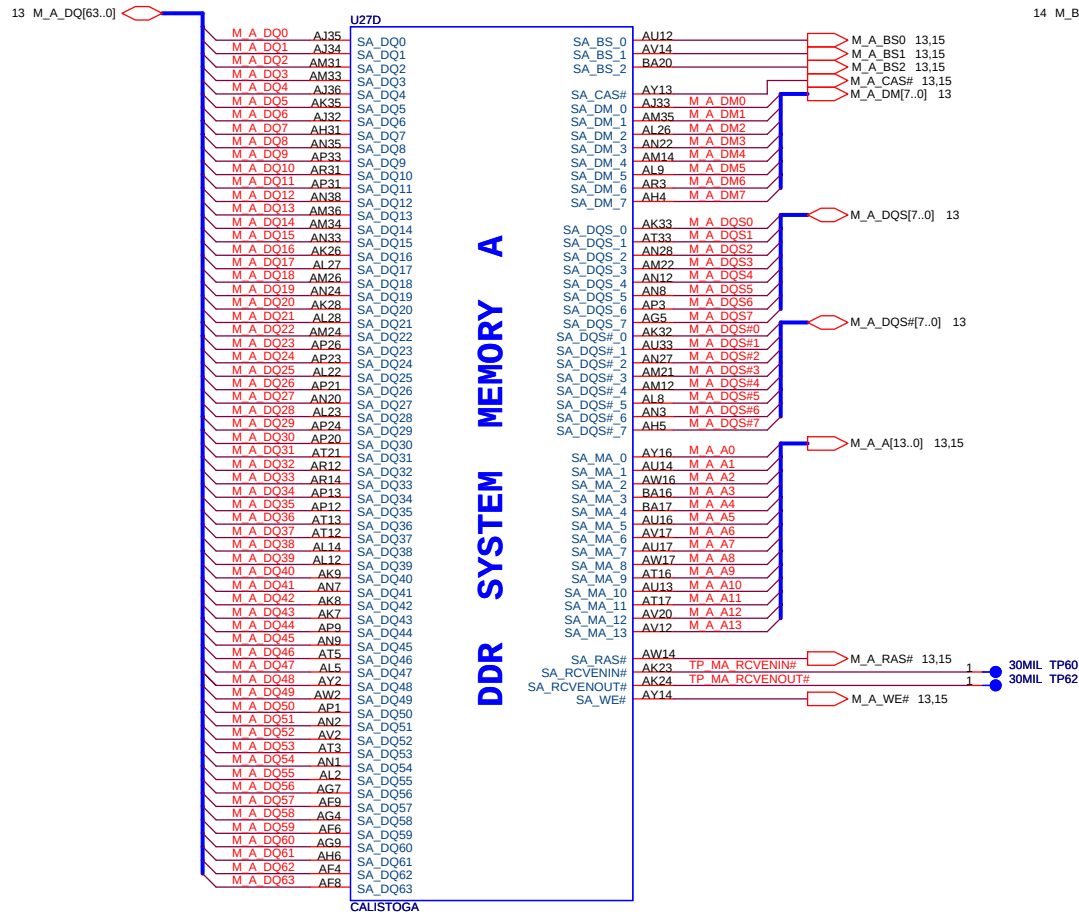
H_REQ#_0	3	H_REQ#_0
H_REQ#_1	3	H_REQ#_1
H_REQ#_2	3	H_REQ#_2
H_REQ#_3	3	H_REQ#_3
H_REQ#_4	3	H_REQ#_4

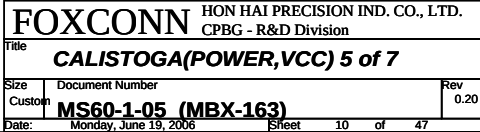
H_RS#_0	3	H_RS#_0
H_RS#_1	3	H_RS#_1
H_RS#_2	3	H_RS#_2

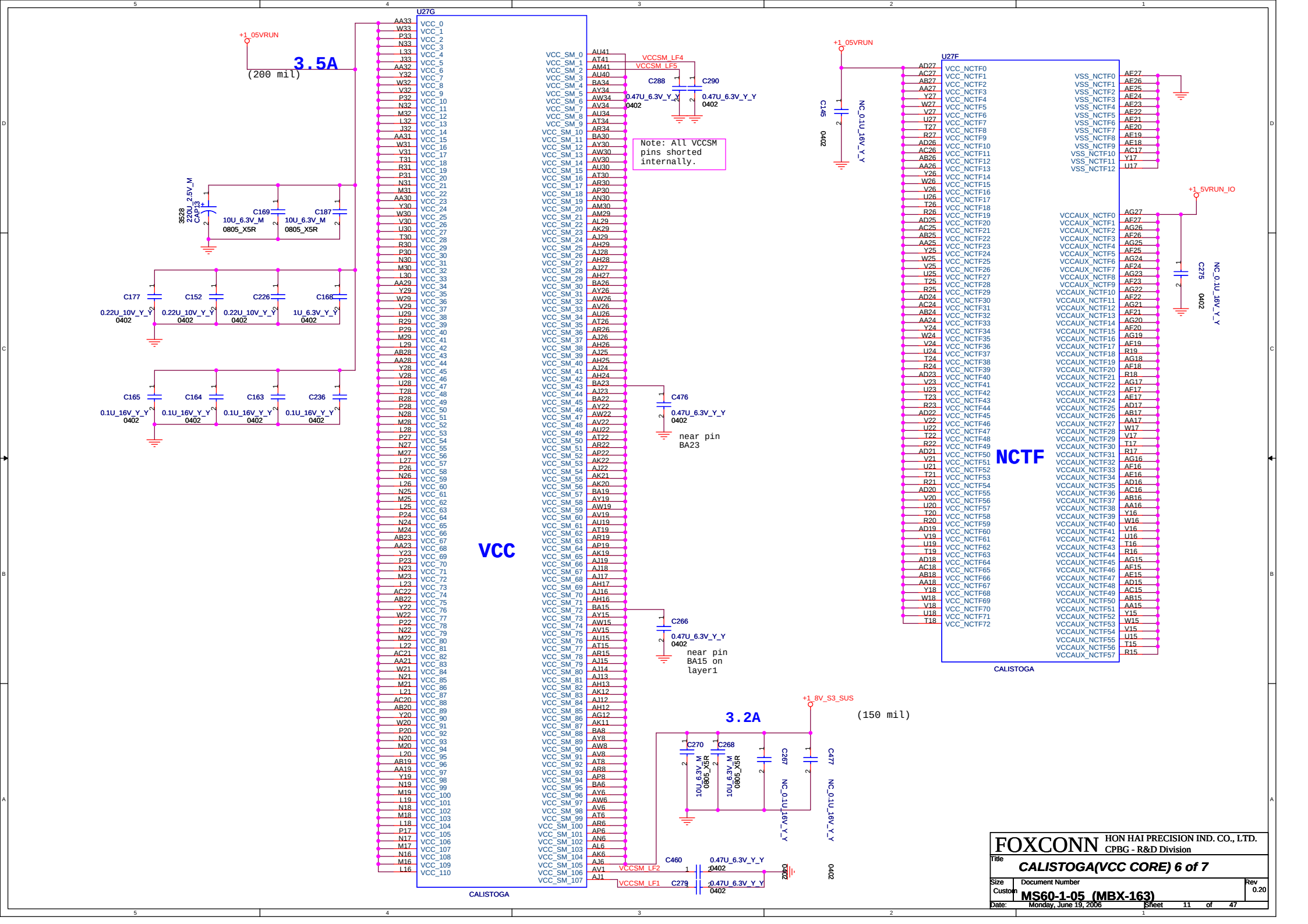
H_SLP#	4	H_SLP#
H_TRDY#	3	H_TRDY#

Place Cap.
near GMCH
within 100
mils.









7 MCH_CFG_5 ◀ 1 ● 30MIL TP45

MCH_CFG_5
Low = DMIX2
High = DMIX4

MCH_CFG_18
(VCC_CORE Select)
Low = 1.05V(default)
High = 1.5V

7 MCH_CFG_18 ◀

7 MCH_CFG_6 ◀ 1 ● 30MIL TP40

MCH_CFG_6
Low = Moby Dick
High = Calistoga
DDR2 select (default high)

MCH_CFG_19
(DMI LANE REVERSAL)
Low = Normal(default)
High = LANES REVERSED

7 MCH_CFG_19 ◀

7 MCH_CFG_7 ◀ 1 ● 30MIL TP36

MCH_CFG_7
(CPU Strap)
Low = RSVD
High = Mobile Yonah processor

7 MCH_CFG_9 ◀ 1 ● 30MIL TP36

MCH_CFG_9
(PCIE Graphics Lane)
Low = Reverse Lane
High = Normal operation

For layout convenience

MCH_CFG_20
(PCIE Backward Interoperability mode)
Low = Only SDVO or PCIE x1 is operational (defaults)
High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 ◀ 1 ● 30MIL TP52

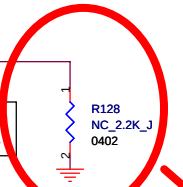
7 MCH_CFG_10 ◀ 1 ● 30MIL TP35

MCH_CFG_10
(HOST PLL VCC SELECT)
Low = RESERVED
High = MOBILITY

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

7 MCH_CFG_11 ◀ 1 ● 30MIL TP35

MCH_CFG_11
(PSB 4x CLK ENABLE)
Low = Reserved
High = Calistoga



7 MCH_CFG_12 ◀ 1 ● 30MIL TP47

7 MCH_CFG_13 ◀ 1 ● 30MIL TP55

MCH_CFG [13:12]
(XOR/ALLZ)
00=Partial Clock Gating Disable
01=XOR Mode Enable
10=All-Z Mode Enable
11=Normal Operation(Default)

7 MCH_CFG_16 ◀ 1 ● 30MIL TP44

MCH_CFG_16
(FSB Dynamic ODT)
Low = Dynamic ODT Disabled
High = Dynamic ODT Enable



AC41	VSS_0	AK34	VSS_97
AA41	VSS_1	AG34	VSS_98
WA1	VSS_2	AF34	VSS_99
TA1	VSS_3	AE34	VSS_100
PA1	VSS_4	AC34	VSS_101
MA1	VSS_5	C34	VSS_102
JA1	VSS_6	AW33	VSS_103
FA1	VSS_7	AV33	VSS_104
AV40	VSS_8	AR33	VSS_105
AP40	VSS_9	C23	VSS_106
AK40	VSS_10	AE33	VSS_107
AL40	VSS_11	K22	VSS_108
AG40	VSS_12	V33	VSS_109
AE40	VSS_13	T33	VSS_110
R40	VSS_14	E22	VSS_111
AY39	VSS_15	M33	VSS_112
AW39	VSS_16	H33	VSS_113
AV39	VSS_17	G33	VSS_114
AW39	VSS_18	F33	VSS_115
AV39	VSS_19	D33	VSS_116
AW39	VSS_20	B33	VSS_117
AN39	VSS_21	AH32	VSS_118
AJ39	VSS_22	AG32	VSS_119
AC39	VSS_23	AF32	VSS_120
AB39	VSS_24	Y21	VSS_121
AA39	VSS_25	AC32	VSS_122
Y39	VSS_26	AB32	VSS_123
W39	VSS_27	G32	VSS_124
V39	VSS_28	B32	VSS_125
T39	VSS_29	AY31	VSS_126
R39	VSS_30	AV31	VSS_127
P39	VSS_31	AN31	VSS_128
N39	VSS_32	AL31	VSS_129
M39	VSS_33	AG31	VSS_130
L39	VSS_34	AB31	VSS_131
J39	VSS_35	Y31	VSS_132
H39	VSS_36	AB30	VSS_133
G39	VSS_37	E30	VSS_134
F39	VSS_38	AT29	VSS_135
D39	VSS_39	AN29	VSS_136
AT38	VSS_40	AB29	VSS_137
AM38	VSS_41	T29	VSS_138
AH38	VSS_42	N29	VSS_139
AG38	VSS_43	K29	VSS_140
AE38	VSS_44	G29	VSS_141
AE38	VSS_45	E29	VSS_142
C38	VSS_46	C29	VSS_143
AK37	VSS_47	B29	VSS_144
AH37	VSS_48	A29	VSS_145
AB37	VSS_49	BA28	VSS_146
AA37	VSS_50	AM28	VSS_147
Y37	VSS_51	AP28	VSS_148
W37	VSS_52	AL28	VSS_149
V37	VSS_53	AM28	VSS_150
T37	VSS_54	AD28	VSS_151
R37	VSS_55	AC28	VSS_152
P37	VSS_56	W28	VSS_153
N37	VSS_57	C16	VSS_154
M37	VSS_58	E28	VSS_155
L37	VSS_59	AP27	VSS_156
J37	VSS_60	AM27	VSS_157
H37	VSS_61	AK27	VSS_158
G37	VSS_62	J27	VSS_159
F37	VSS_63	L15	VSS_160
D37	VSS_64	E27	VSS_161
AW36	VSS_65	C27	VSS_162
AN36	VSS_66	B27	VSS_163
AG36	VSS_67	AN26	VSS_164
AE36	VSS_68	M26	VSS_165
AE36	VSS_69	K26	VSS_166
AC36	VSS_70	AA14	VSS_167
AC36	VSS_71	D26	VSS_168
C36	VSS_72	AK25	VSS_169
B36	VSS_73	P25	VSS_170
BA35	VSS_74	K25	VSS_171
AV35	VSS_75	H25	VSS_172
AR35	VSS_76	AR13	VSS_173
AG35	VSS_77	D25	VSS_174
AE35	VSS_78	A25	VSS_175
AB35	VSS_79	BA24	VSS_176
AA35	VSS_80	AU24	VSS_177
Y35	VSS_81	AL24	VSS_178
W35	VSS_82	AW23	VSS_179
V35	VSS_83		
T35	VSS_84		
R35	VSS_85		
P35	VSS_86		
N35	VSS_87		
M35	VSS_88		
L35	VSS_89		
J35	VSS_90		
H35	VSS_91		
G35	VSS_92		
F35	VSS_93		
D35	VSS_94		
C35	VSS_95		
AN34	VSS_96		

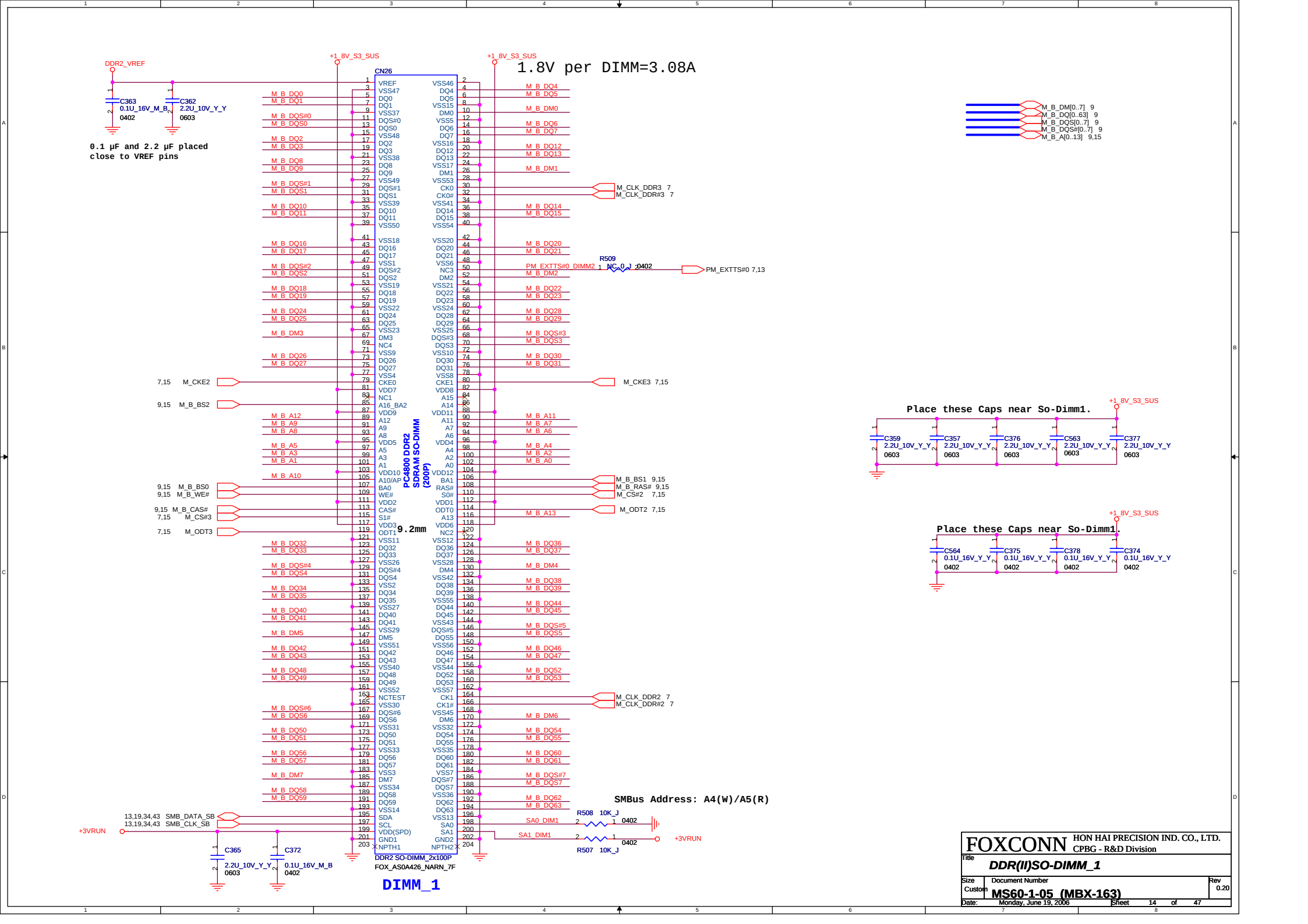
VSS

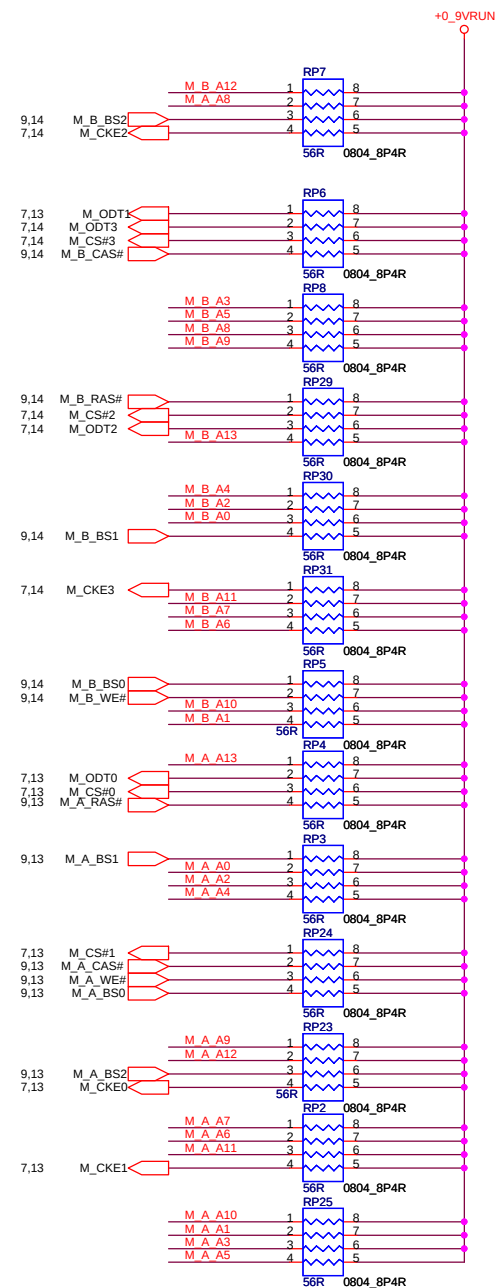
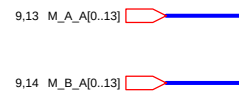
AT23	VSS_180	J11	VSS_273
AN23	VSS_181	D11	VSS_274
AM23	VSS_182	B11	VSS_275
AH23	VSS_183	AV10	VSS_276
AC23	VSS_184	AP10	VSS_277
W23	VSS_185	AL10	VSS_278
K23	VSS_186	AJ10	VSS_279
J23	VSS_187	AG10	VSS_280
F23	VSS_188	AC10	VSS_281
C23	VSS_189	W10	VSS_282
AE23	VSS_190	U10	VSS_283
K22	VSS_191	BA9	VSS_284
G22	VSS_192	AW9	VSS_285
E22	VSS_193	AR9	VSS_286
D22	VSS_194	AH9	VSS_287
A22	VSS_195	AB9	VSS_288
BA21	VSS_196	Y9	VSS_289
AV21	VSS_197	G9	VSS_290
AR21	VSS_198	E9	VSS_291
AN21	VSS_199	A9	VSS_292
AL21	VSS_200	AG8	VSS_293
AB21	VSS_201	AD8	VSS_294
Y21	VSS_202	AA8	VSS_295
P21	VSS_203	U8	VSS_296
K21	VSS_204	K8	VSS_297
J21	VSS_205	C8	VSS_298
H21	VSS_206	BA7	VSS_299
C21	VSS_207	AV7	VSS_300
AW20	VSS_208	AP7	VSS_301
AR20	VSS_209	AL7	VSS_302
AN20	VSS_210	AJ7	VSS_303
AA20	VSS_211	AH7	VSS_304
K20	VSS_212	AG7	VSS_305
B20	VSS_213	AD7	VSS_306
A20	VSS_214	AC7	VSS_307
AN19	VSS_215	R7	VSS_308
AC19	VSS_216	G7	VSS_309
E30	VSS_217	D7	VSS_310
W19	VSS_218	AG6	VSS_311
K19	VSS_219	AD6	VSS_312
G19	VSS_220	AB6	VSS_313
C19	VSS_221	Y6	VSS_314
AH18	VSS_222	U6	VSS_315
K18	VSS_223	N6	VSS_316
H18	VSS_224	K6	VSS_317
D18	VSS_225	H6	VSS_318
A18	VSS_226	B6	VSS_319
AY17	VSS_227	AV5	VSS_320
AR17	VSS_228	AP5	VSS_321
AP17	VSS_229	AD5	VSS_322
AM17	VSS_230	AA5	VSS_323
AK17	VSS_231	AR4	VSS_324
AV16	VSS_232	AL4	VSS_325
AN16	VSS_233	AJ4	VSS_326
AL16	VSS_234	Y4	VSS_327
J16	VSS_235	U4	VSS_328
W16	VSS_236	AG4	VSS_329
C16	VSS_237	AD4	VSS_330
E16	VSS_238	AC4	VSS_331
AP15	VSS_239	R4	VSS_332
AM15	VSS_240	J4	VSS_333
AK15	VSS_241	F4	VSS_334
N15	VSS_242	C4	VSS_335
M15	VSS_243	AY3	VSS_336
L15	VSS_244	AW3	VSS_337
E15	VSS_245	AP3	VSS_338
B15	VSS_246	AA3	VSS_339
C15	VSS_247	AR3	VSS_340
AW14	VSS_248	AL3	VSS_341
AD14	VSS_249	AJ3	VSS_342
AA14	VSS_250	Y3	VSS_343
K14	VSS_251	U3	VSS_344
VSS_252	VSS_252	AG3	VSS_345
H14	VSS_253	AD3	VSS_346
E14	VSS_254	AC3	VSS_347
AV13	VSS_255	G3	VSS_348
AR13	VSS_256	U2	VSS_349
AN13	VSS_257	H2	VSS_350
A25	VSS_258	F2	VSS_351
BA24	VSS_259	C2	VSS_352
AU24	VSS_260	N2	VSS_353
AL24	VSS_261	J2	VSS_354
AW23	VSS_262	H2	VSS_355
	VSS_263	F2	VSS_356
	VSS_264	C2	VSS_357
	VSS_265	N2	VSS_358
	VSS_266	J2	VSS_359
	VSS_267	H2	VSS_360
	VSS_268	F2	VSS_361
	VSS_269	C2	VSS_362
	VSS_270	N2	VSS_363
	VSS_271	J2	VSS_364
	VSS_272	H2	VSS_365
	VSS_273	F2	VSS_366
	VSS_274	C2	VSS_367
	VSS_275	N2	VSS_368
	VSS_276	J2	VSS_369
	VSS_277	H2	VSS_370
	VSS_278	F2	VSS_371
	VSS_279	C2	VSS_372
	VSS_280	N2	VSS_373
	VSS_281	J2	VSS_374
	VSS_282	H2	VSS_375
	VSS_283	F2	VSS_376
	VSS_284	C2	VSS_377
	VSS_285	N2	VSS_378
	VSS_286	J2	VSS_379
	VSS_287	H2	VSS_380
	VSS_288	F2	VSS_381
	VSS_289	C2	VSS_382
	VSS_290	N2	VSS_383
	VSS_291	J2	VSS_384
	VSS_292	H2	VSS_385
	VSS_293	F2	VSS_386
	VSS_294	C2	VSS_387
	VSS_295	N2	VSS_388
	VSS_296	J2	VSS_389
	VSS_297	H2	VSS_390
	VSS_298	F2	VSS_391
	VSS_299	C2	VSS_392
	VSS_300	N2	VSS_393
	VSS_301	J2	VSS_394
	VSS_302	H2	VSS_395
	VSS_303	F2	VSS_396
	VSS_304	C2	VSS_397
	VSS_305	N2	VSS_398
	VSS_306	J2	VSS_399
	VSS_307	H2	VSS_400
	VSS_308	F2	VSS_401
	VSS_309	C2	VSS_402
	VSS_310	N2	VSS_403
	VSS_311	J2	VSS_404
	VSS_312	H2	VSS_405
	VSS_313	F2	VSS_406
	VSS_314	C2	VSS_407
	VSS_315	N2	VSS_408
	VSS_316	J2	VSS_409
	VSS_317	H2	VSS_410
	VSS_318	F2	VSS_411
	VSS_319	C2	VSS_412
	VSS_320	N2	VSS_413
	VSS_321	J2	VSS_414
	VSS_322	H2	VSS_415
	VSS_323	F2	VSS_416
	VSS_324	C2	VSS_417
	VSS_325	N2	VSS_418
	VSS_326	J2	VSS_419
	VSS_327	H2	VSS_420
	VSS_328	F2	VSS_421
	VSS_329	C2	VSS_422
	VSS_330	N2	VSS_423
	VSS_331	J2	VSS_424
	VSS_332	H2	VSS_425
	VSS_333	F2	VSS_426
	VSS_334	C2	VSS_427
	VSS_335	N2	VSS_428
	VSS_336	J2	VSS_429
	VSS_337	H2	VSS_430
	VSS_338	F2	VSS_431
	VSS_339	C2	VSS_432
	VSS_340	N2	VSS_433
	VSS_341	J2	VSS_434
	VSS_342	H2	VSS_435
	VSS_343	F2	VSS_436
	VSS_344	C2	VSS_437
	VSS_345	N2	VSS_438
	VSS_346	J2	VSS_439
	VSS_347	H2	VSS_440
	VSS_348	F2	VSS_441
	VSS_349	C2	VSS_442
	VSS_350	N2	VSS_443
	VSS_351	J2	VSS_444
	VSS_352	H2	VSS_445
	VSS_353	F2	VSS_446
	VSS_354	C2	VSS_447
	VSS_355	N2	VSS_448
	VSS_356	J2	VSS_449
	VSS_357	H2	VSS_450
	VSS_358	F2	VSS_451
	VSS_359	C2	VSS_452
	VSS_360	N2	VSS_453

VSS

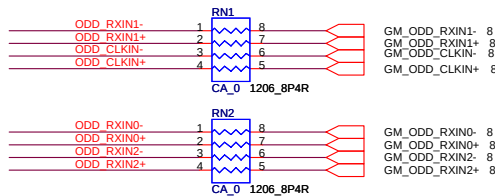
CALISTOGA

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

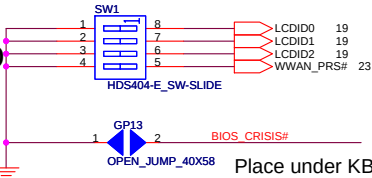




LVDS

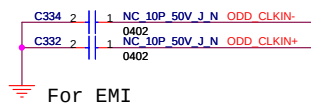


PANEL ID

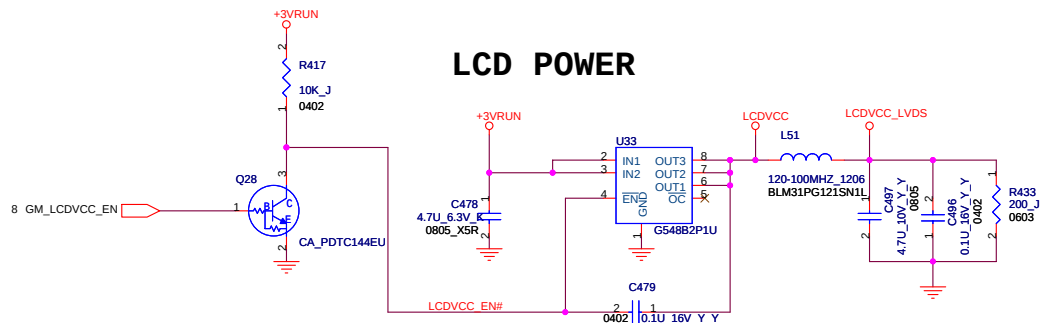


Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	

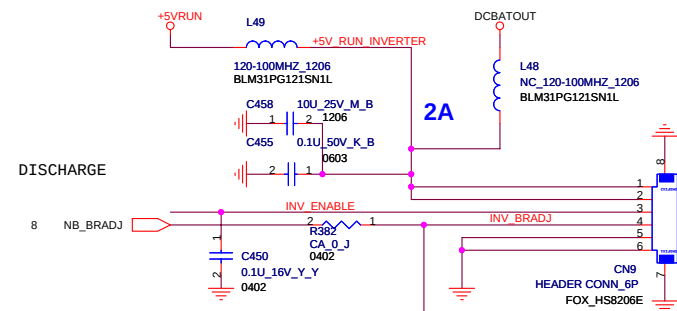
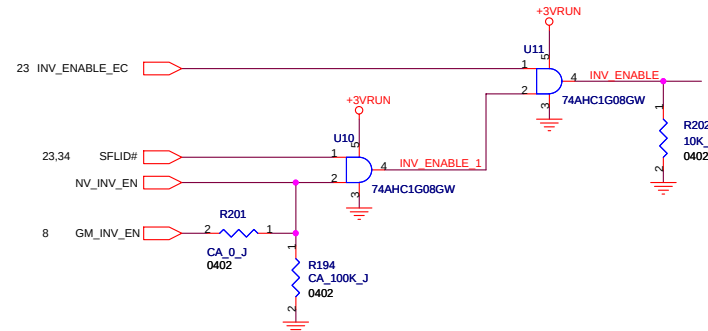
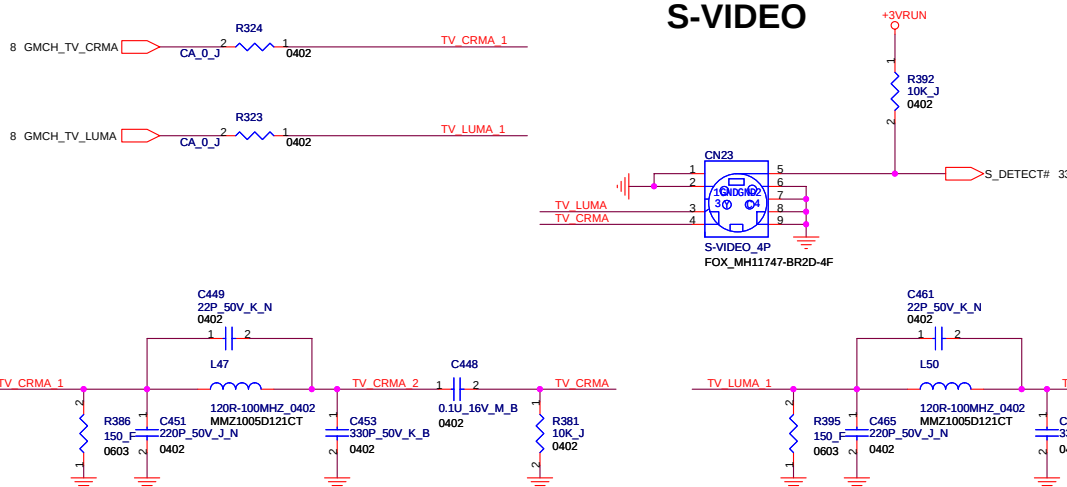
LVDS CONNECTOR

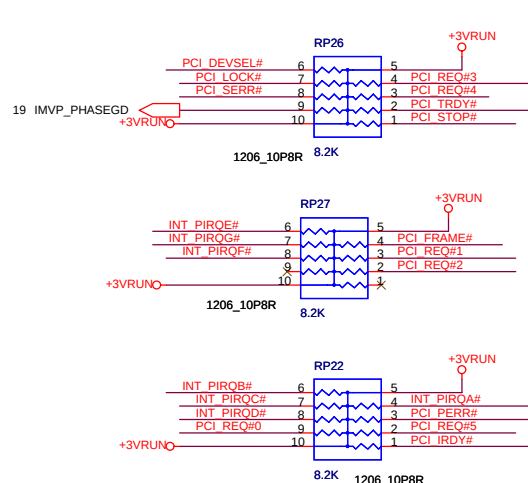


LCD POWER

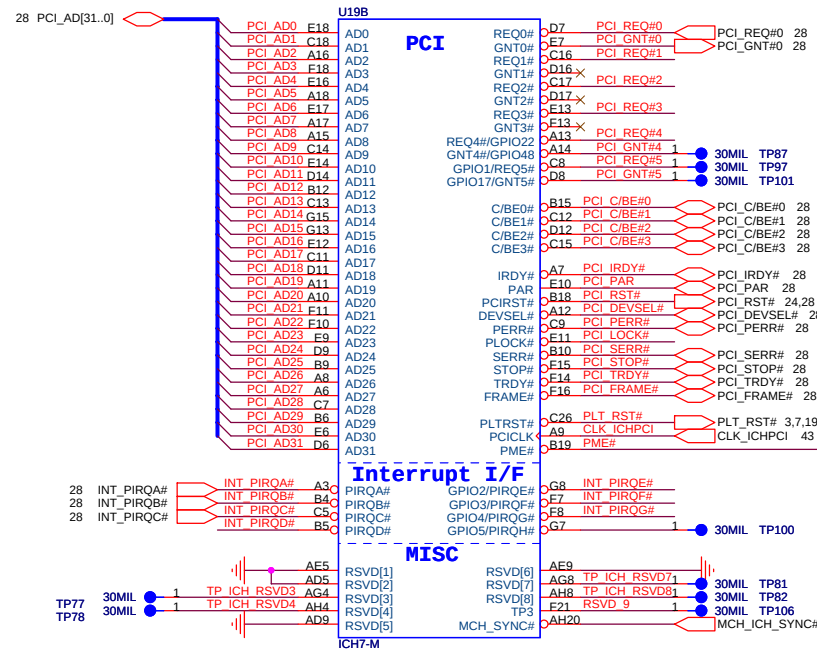


S-VIDEO

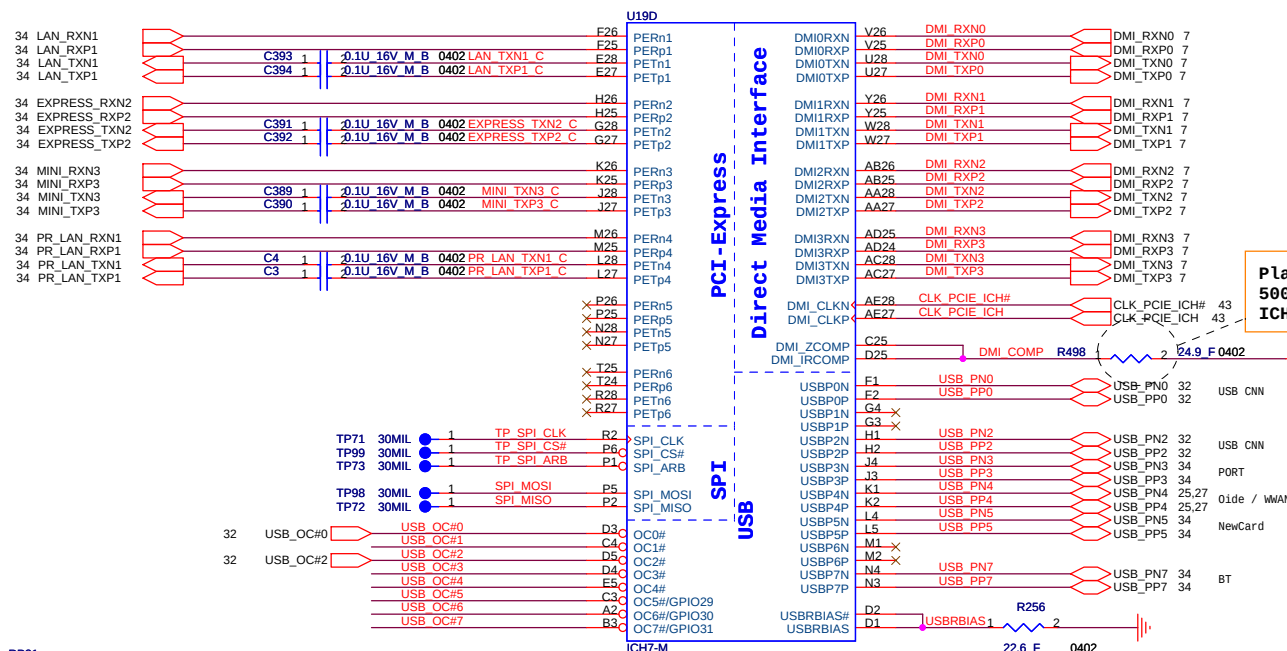




PCI Pullups

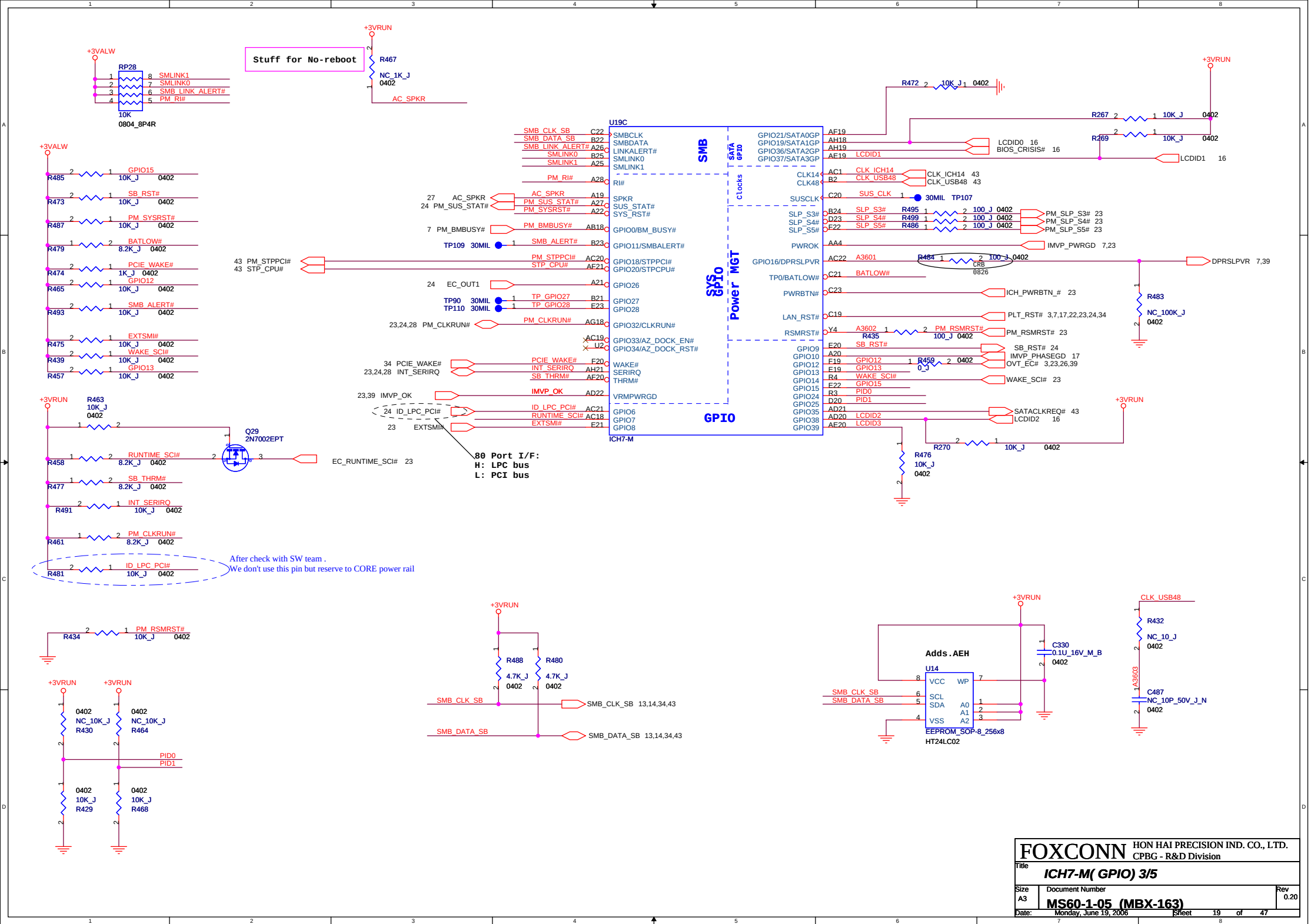


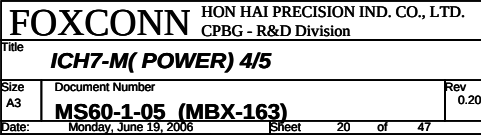
Test leakage voltage in BB



Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals

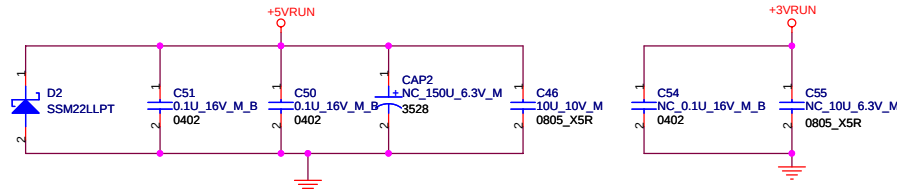
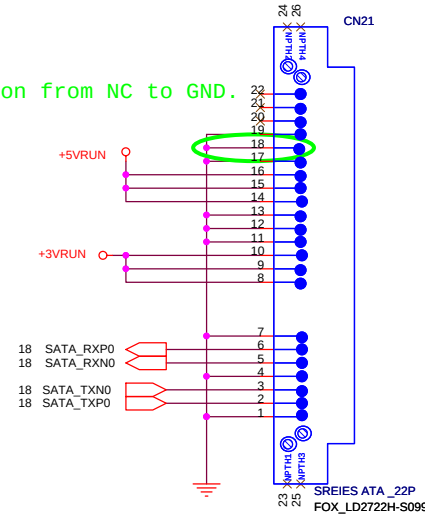






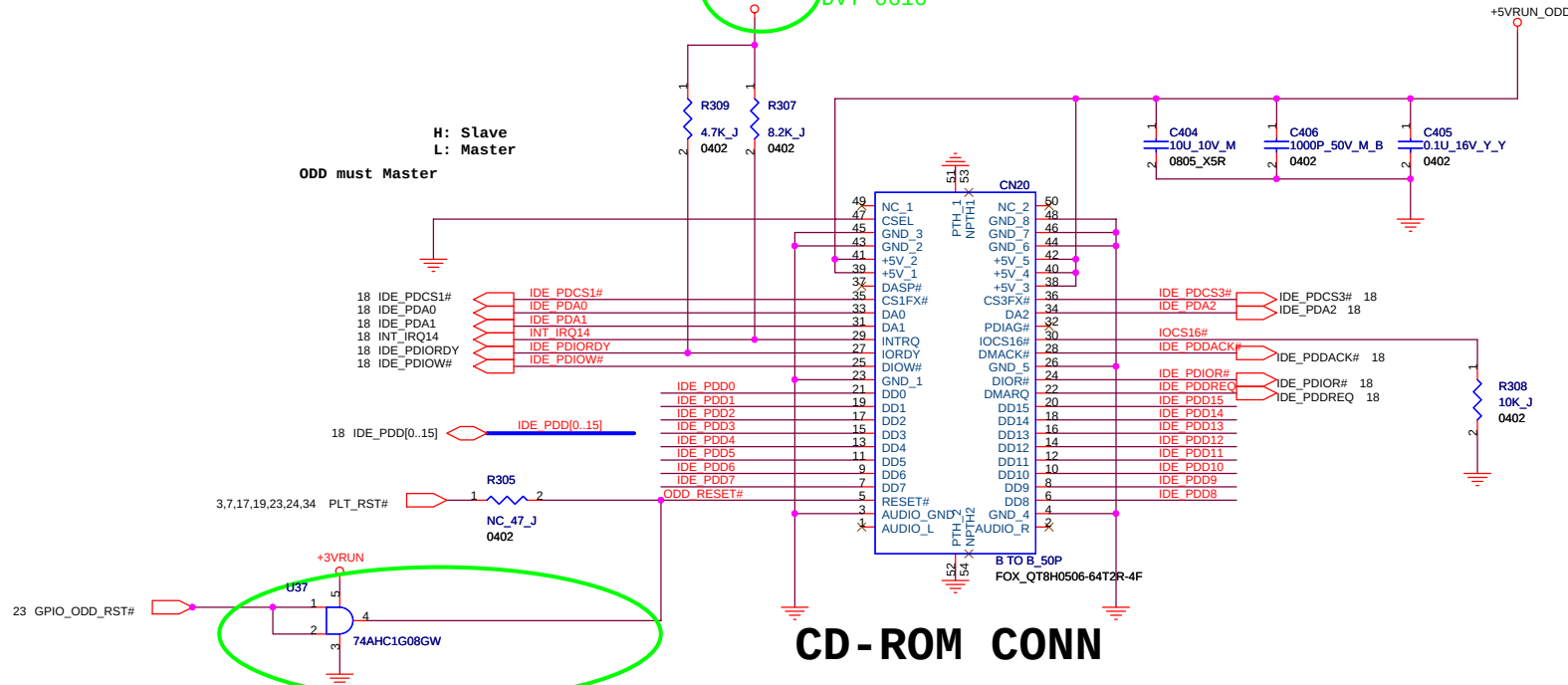
SATA HDD CONN

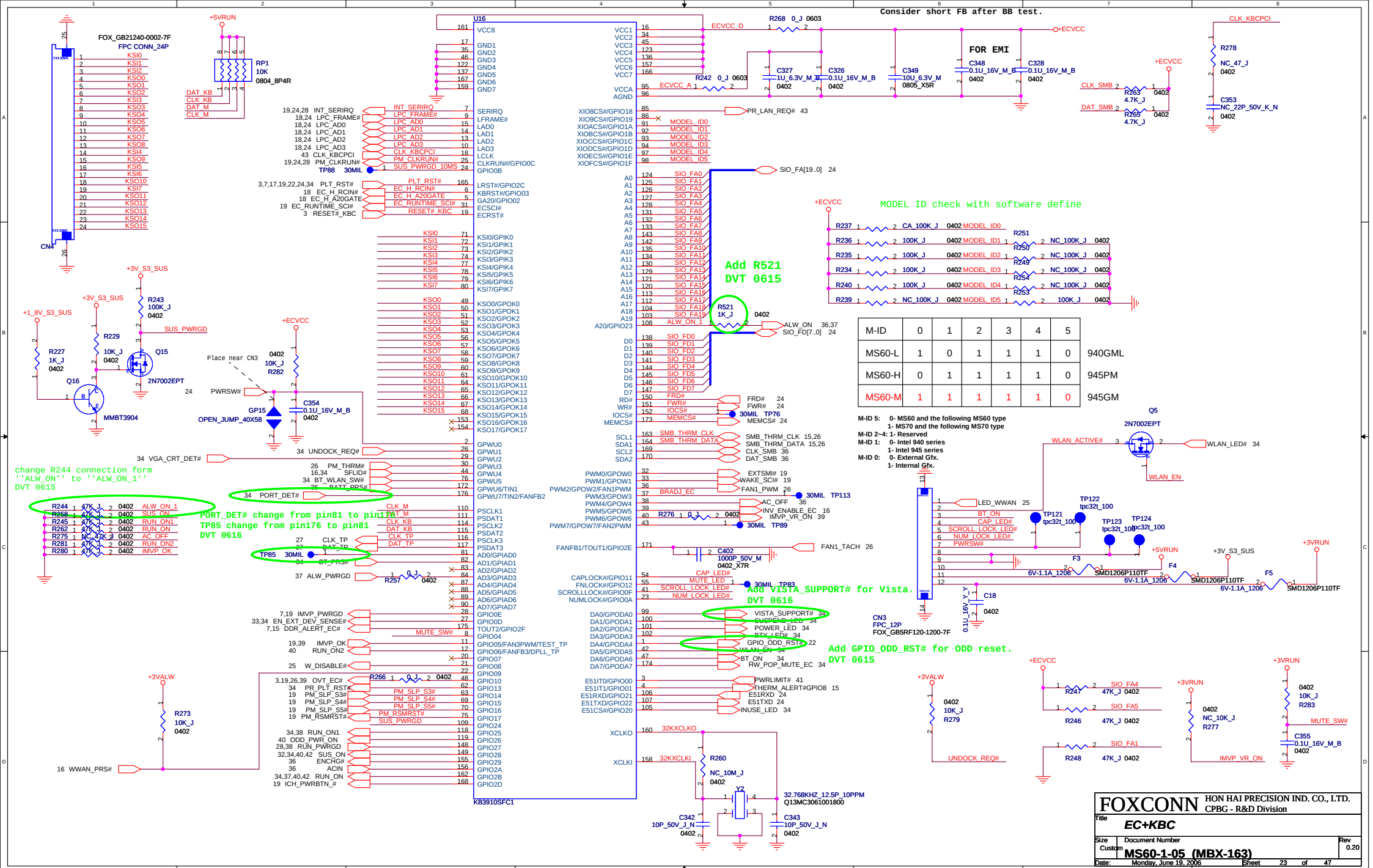
CN21's pin18 change connection from NC to GND.
DVT 0616



Change from +3VRUN to +3VRUN_ODD
DVT 0616

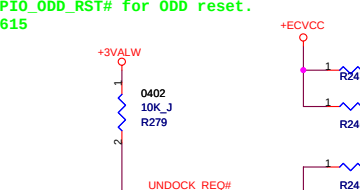
H: Slave
L: Master
ODD must Master

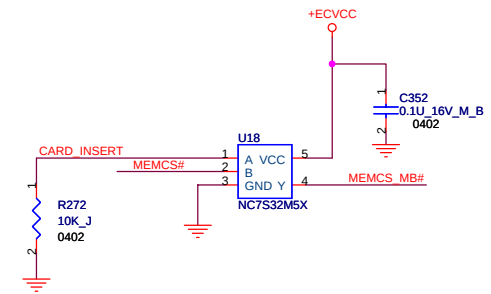




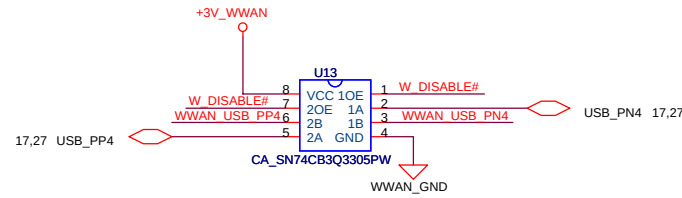
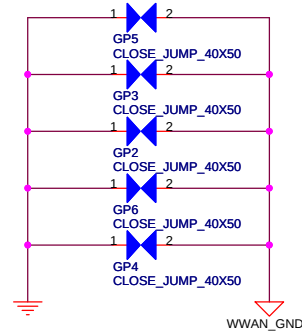
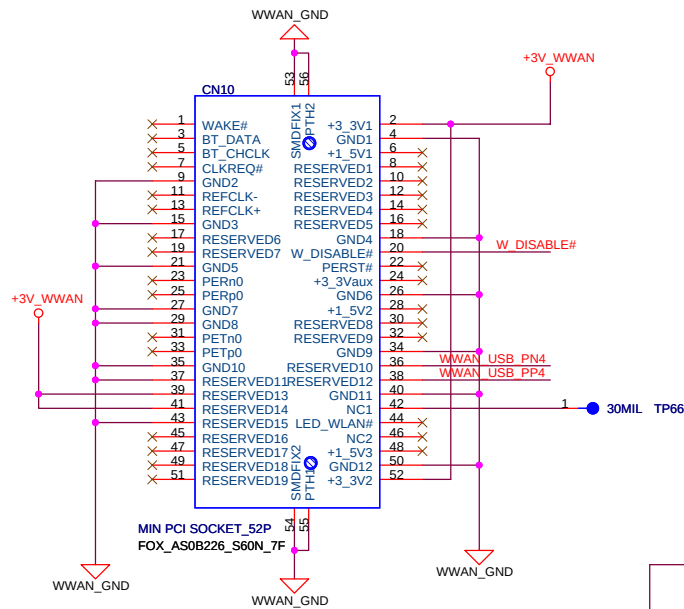
M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM

M-ID 5: 0- MS60 and the following MS60 type
1- MS70 and the following MS70 type
M-ID 2-4: 1- Reserved
M-ID 1: 0- Intel 940 series
1- Intel 945 series
M-ID 0: 0- External Gtx.
1- Internal Gtx.



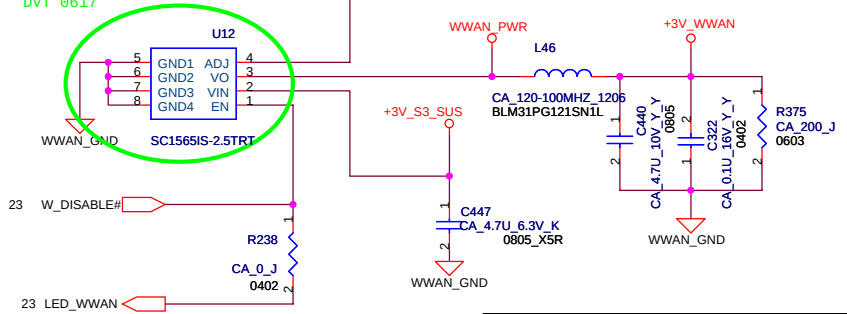


FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title Flash ROM/X-Bus CONN			
Size A3	Document Number MS60-1-05 (MBX-163)		Rev 0.20
Date	Monday, June 19, 2006		Sheet 24 of 47



WWAN POWER

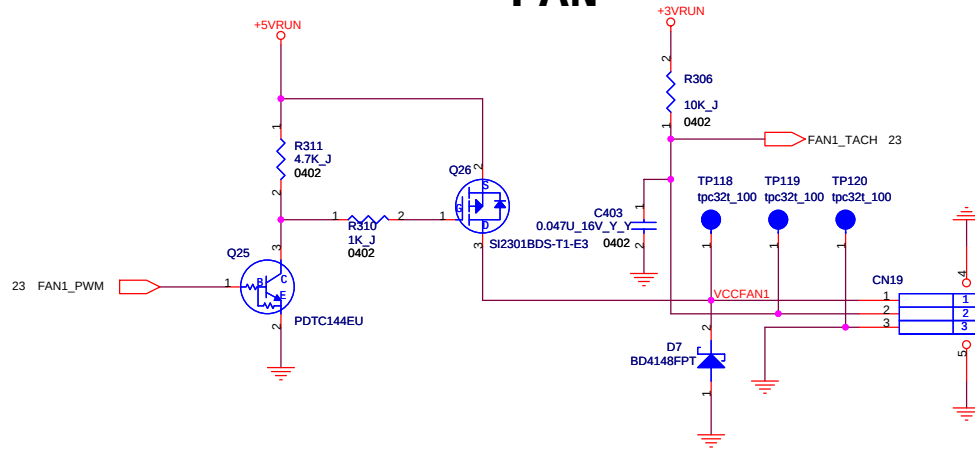
U12 change to SC1565IS-2.5TRT
DVT 0617



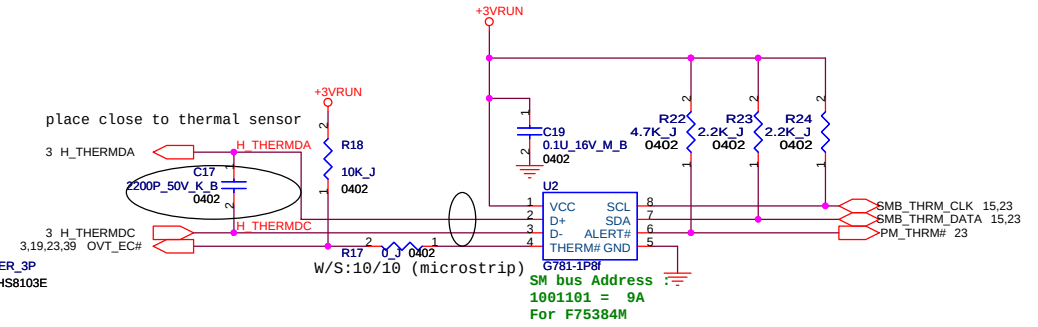
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
Size		Document Number	
Custom		MS60-1-05 (MBX-163)	
Date:		Monday, June 19, 2006	Sheet 25 of 47

Rev 0.20

FAN

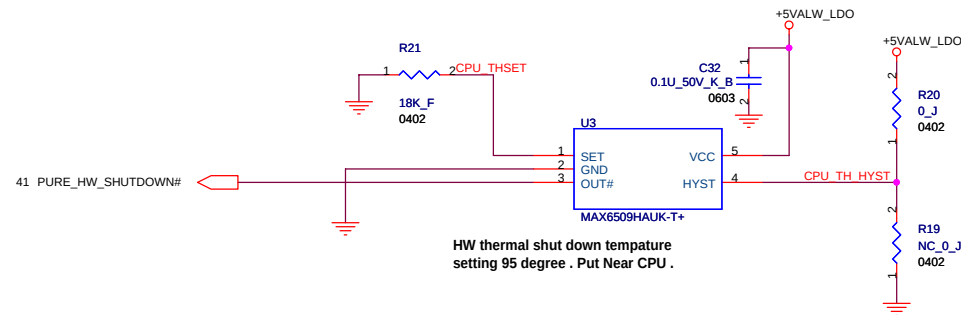


CPU SENSOR

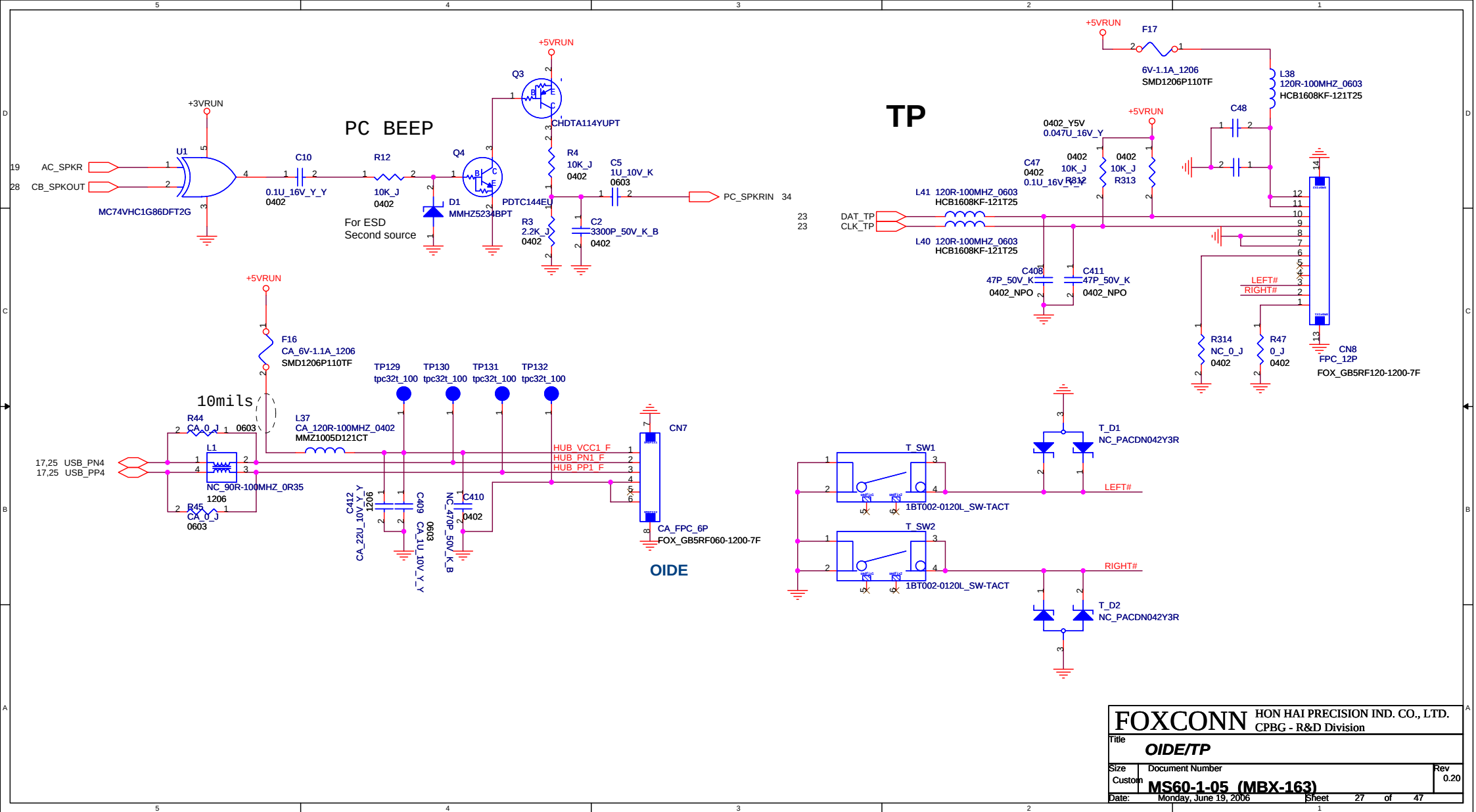


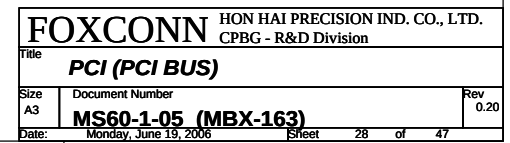
Place Thermal-Sensor near
CPU & GMCH.

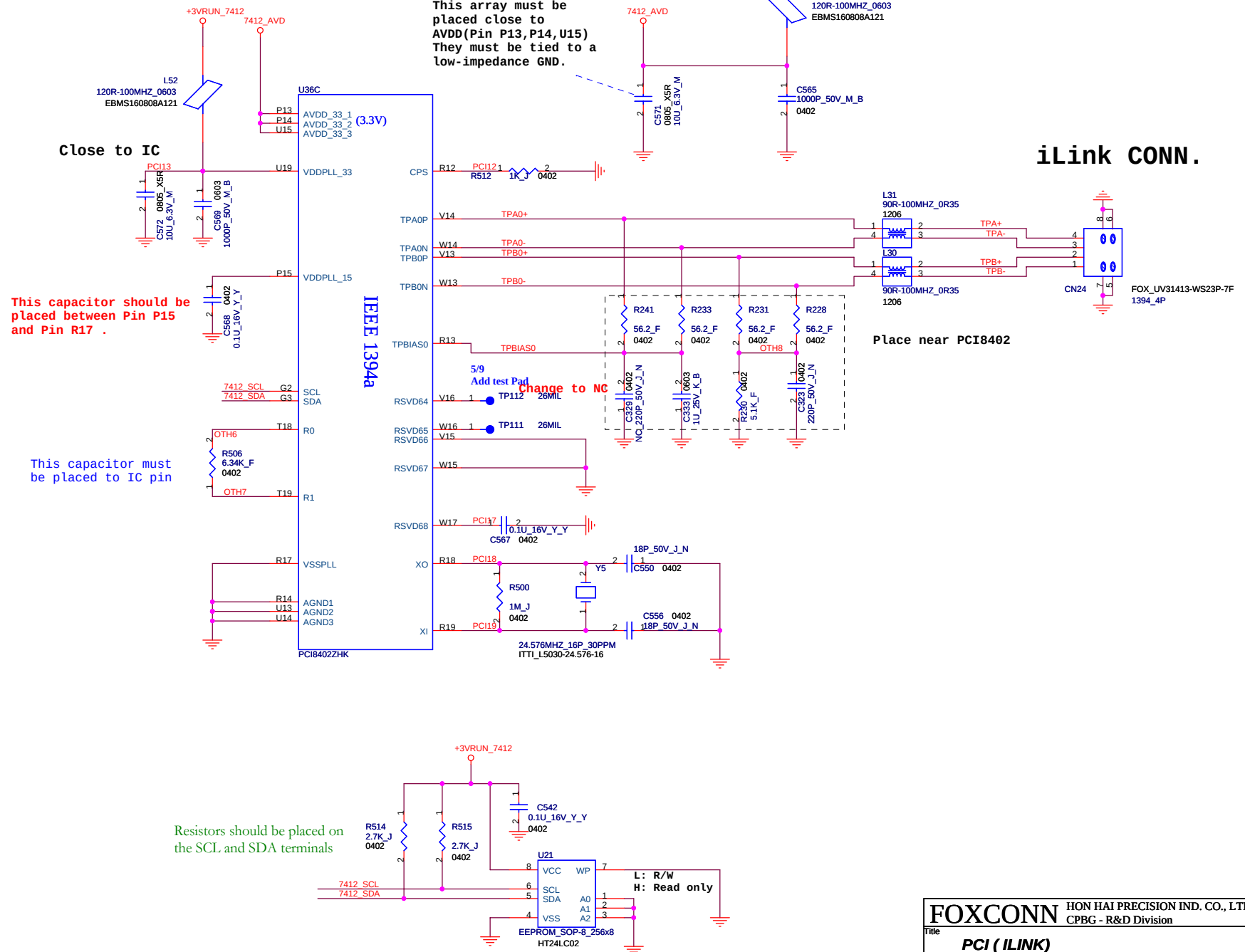
HW THERMAL PROTECTION

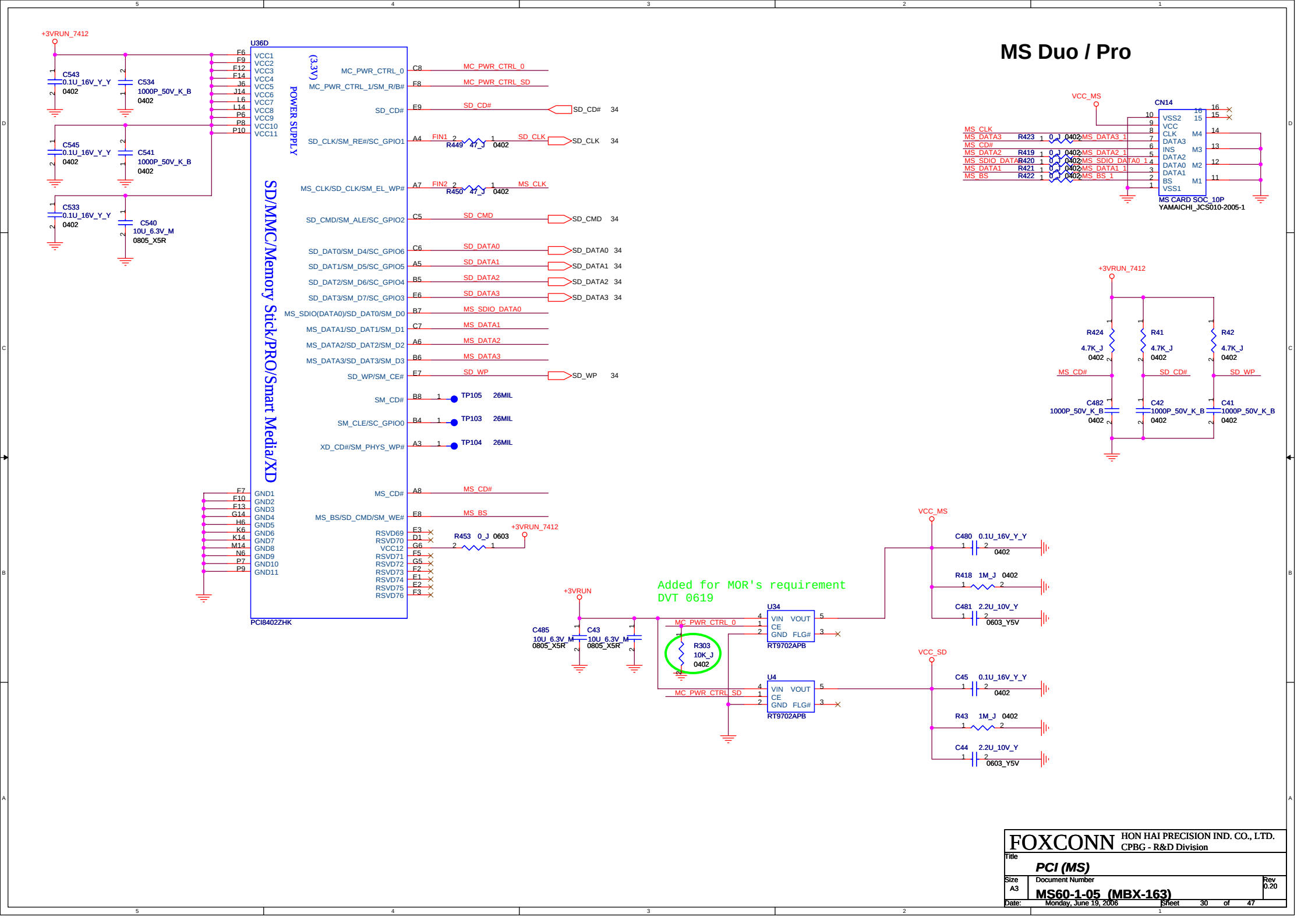


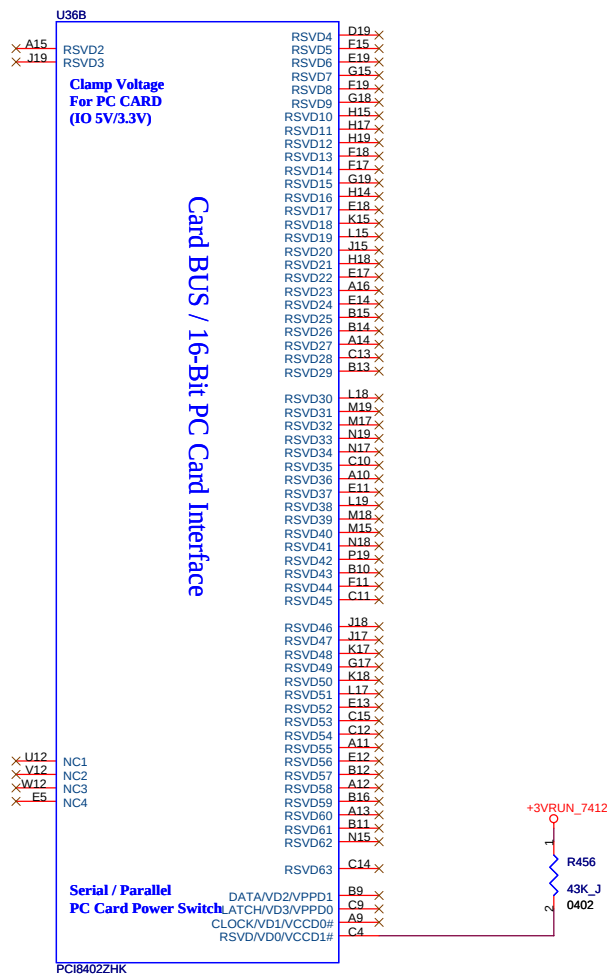
HW thermal shut down temperature
setting 95 degree . Put Near CPU .

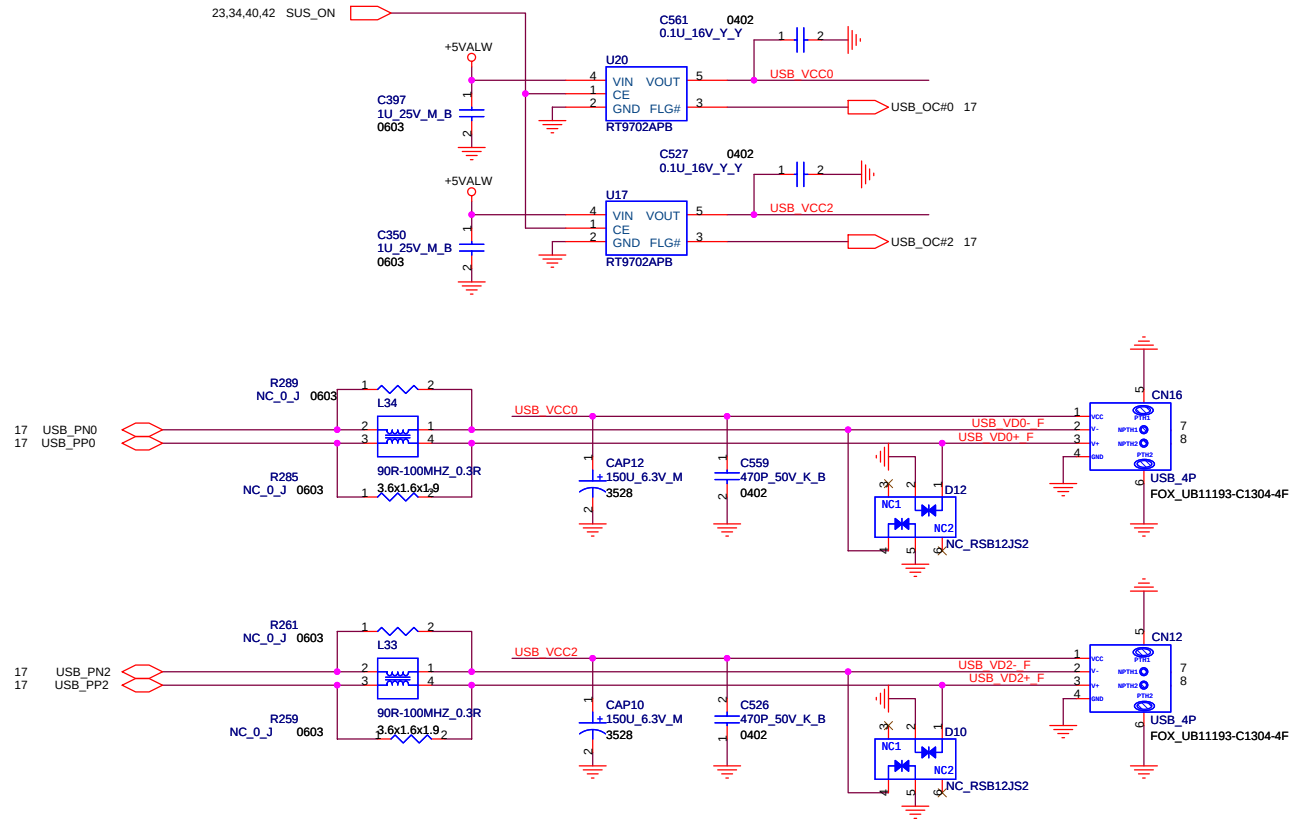


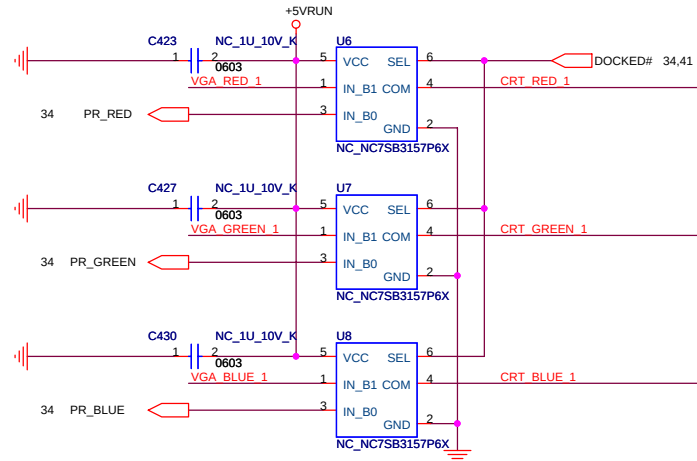
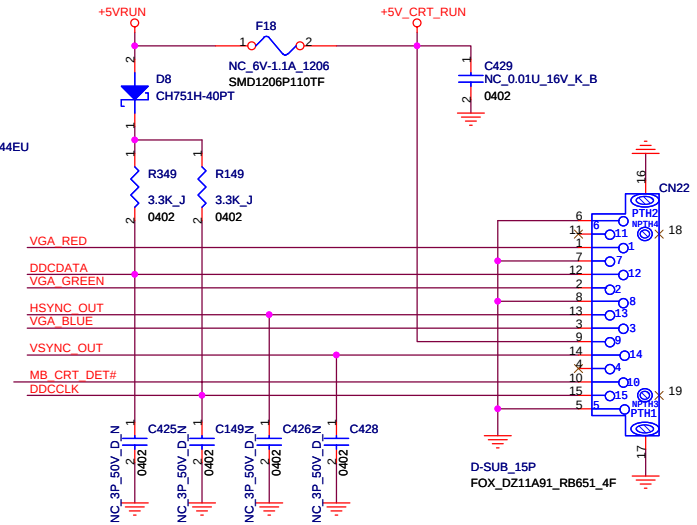
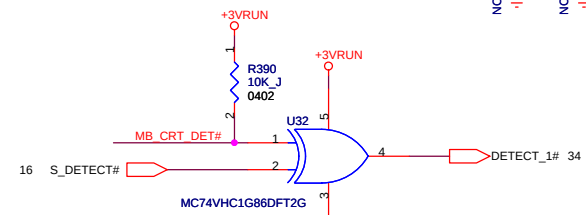
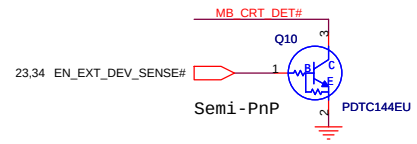
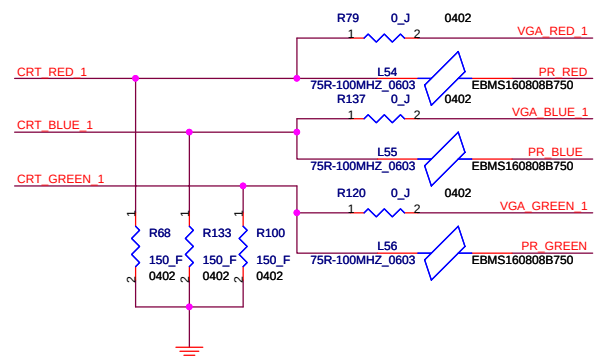
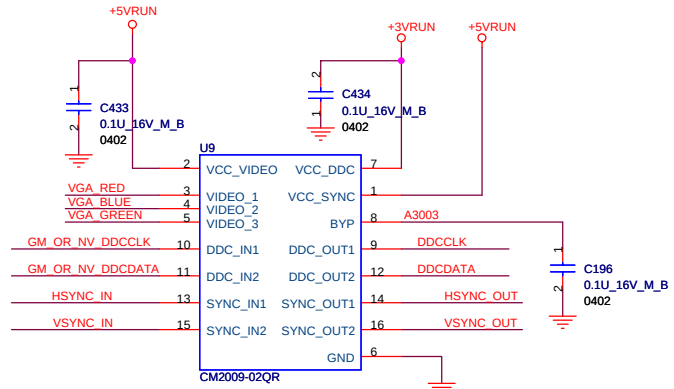
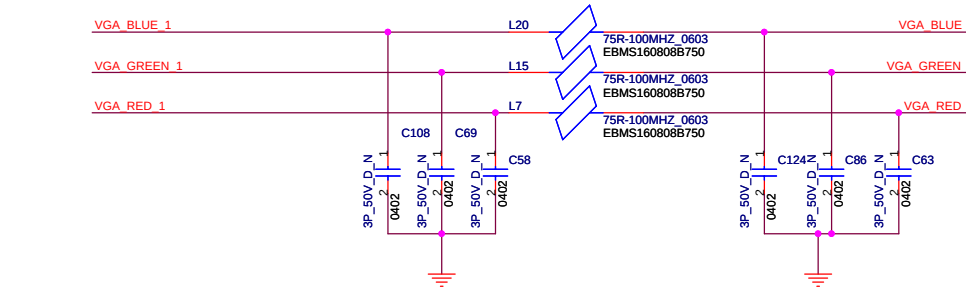
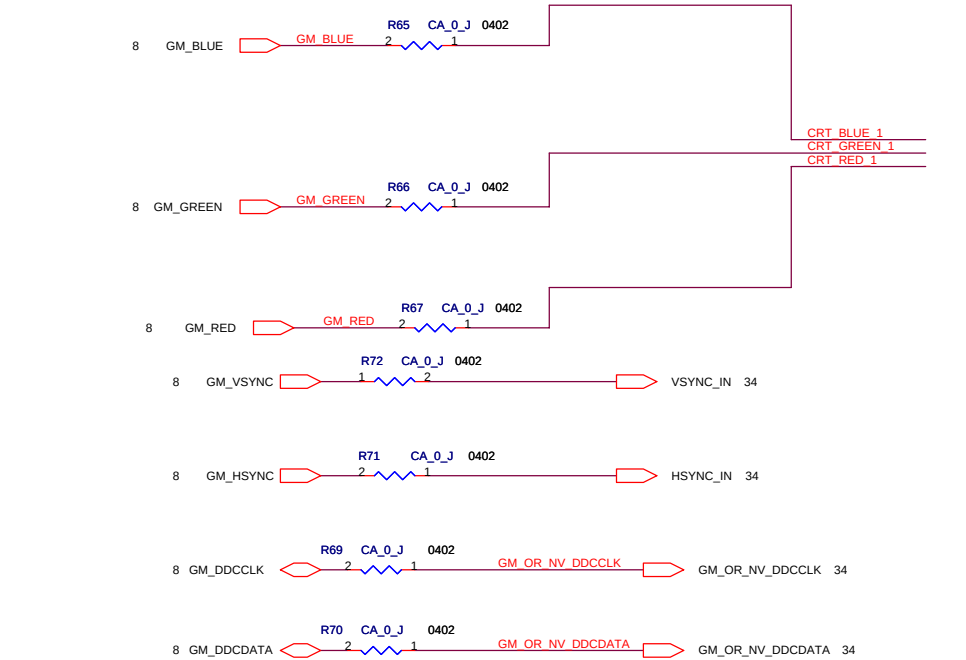


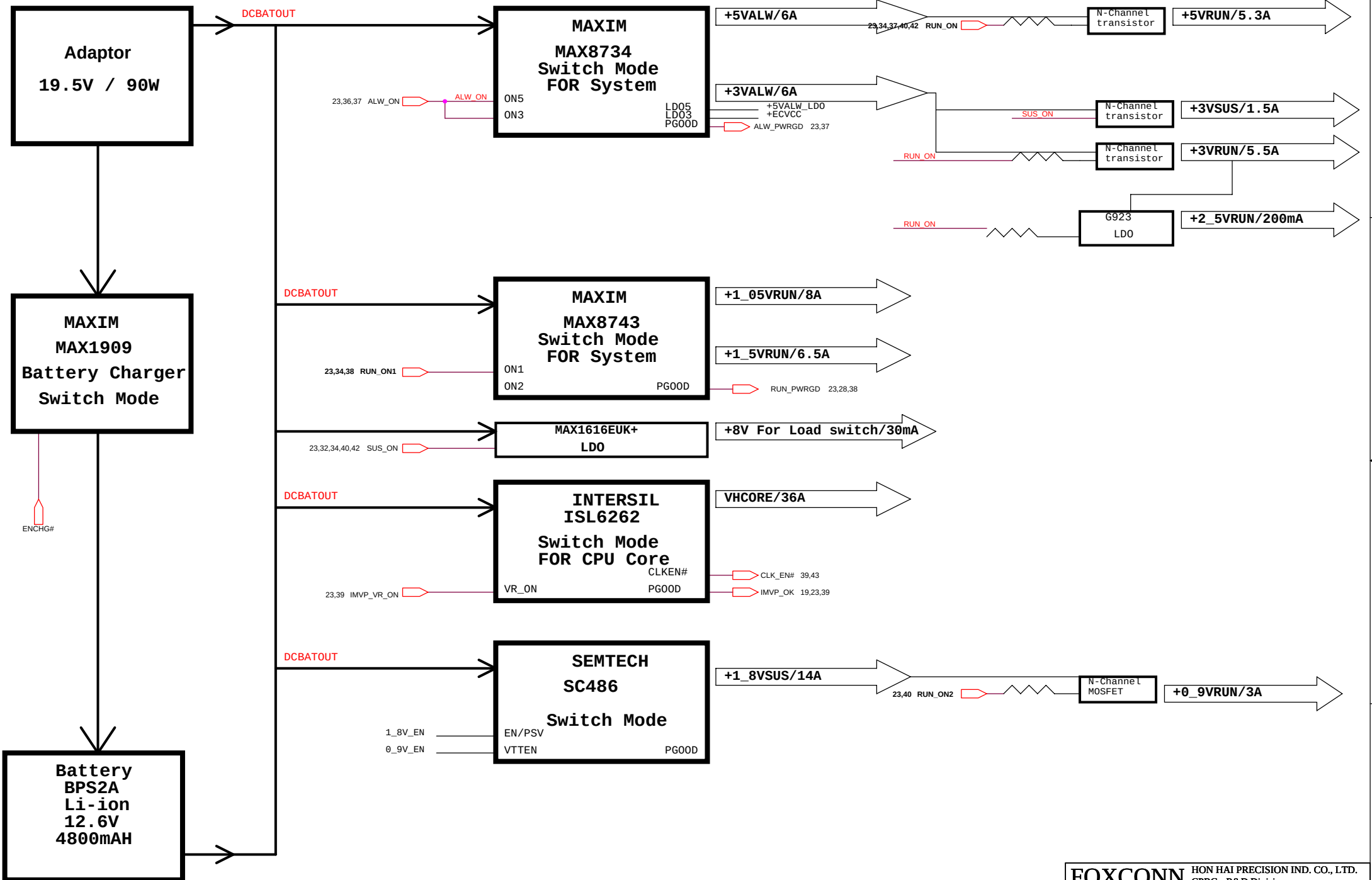


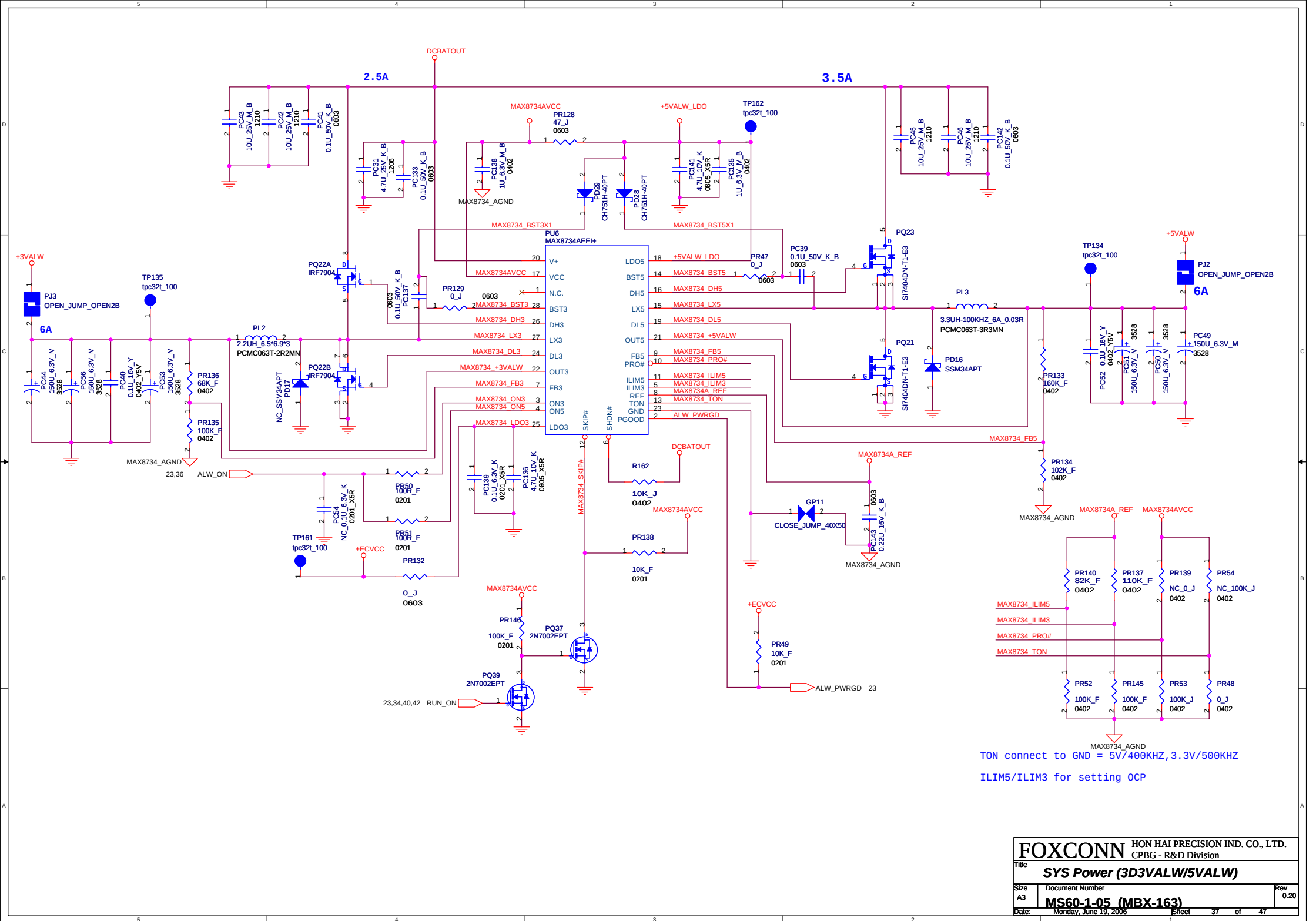




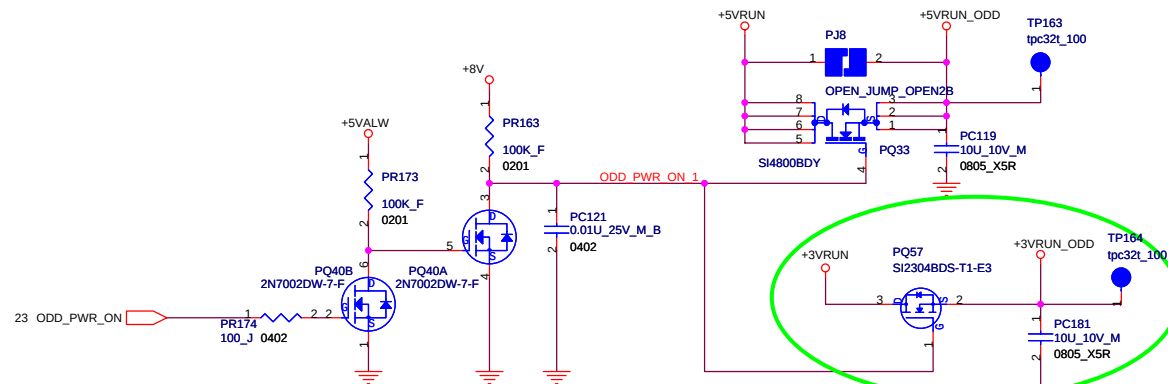
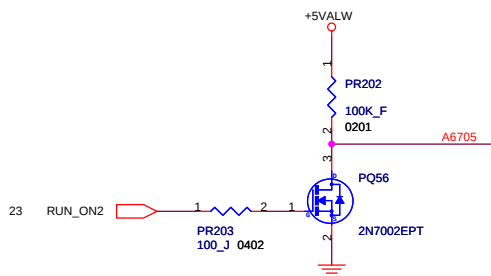
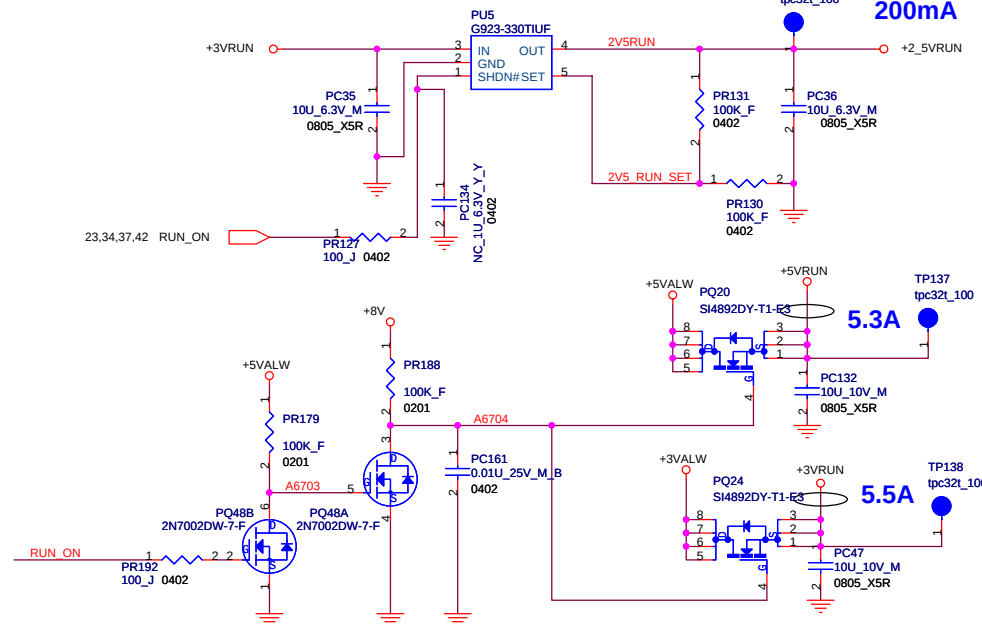
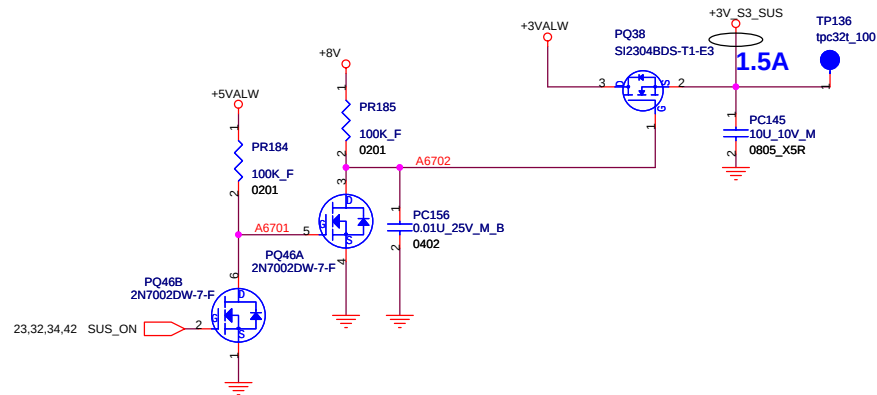




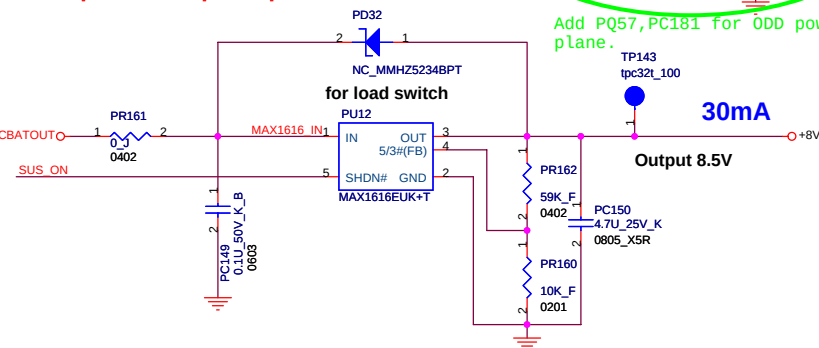
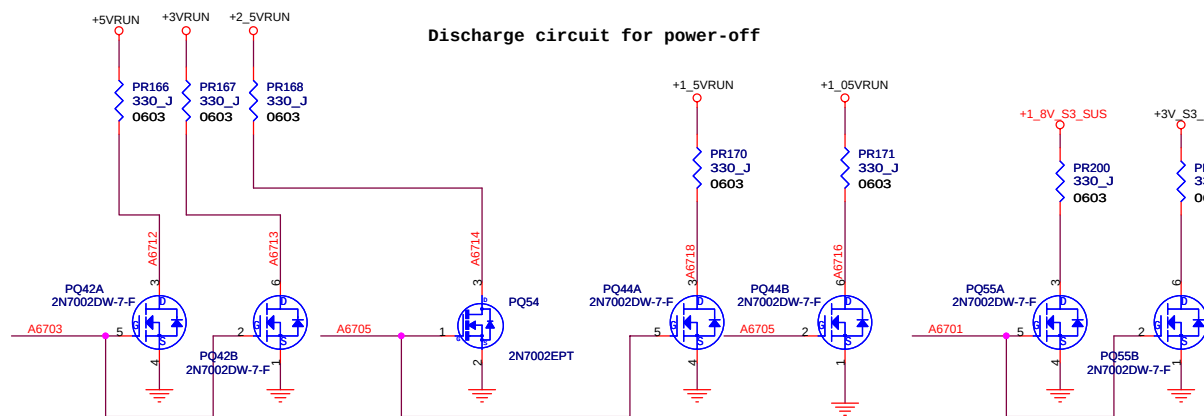


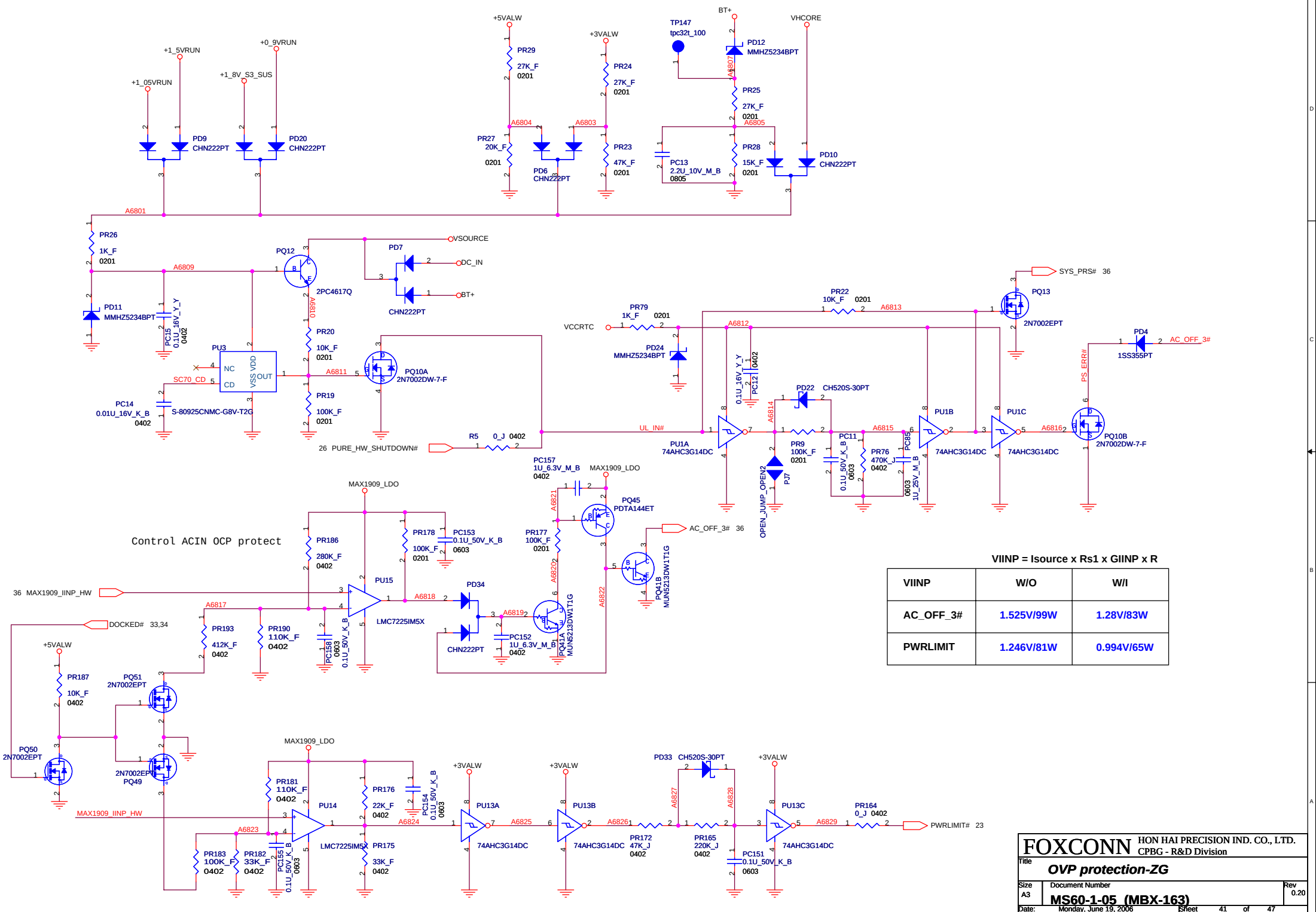


TON connect to GND = 5V/400KHZ, 3.3V/500KHZ
 ILIM5/ILIM3 for setting OCP



Discharge circuit for power-off

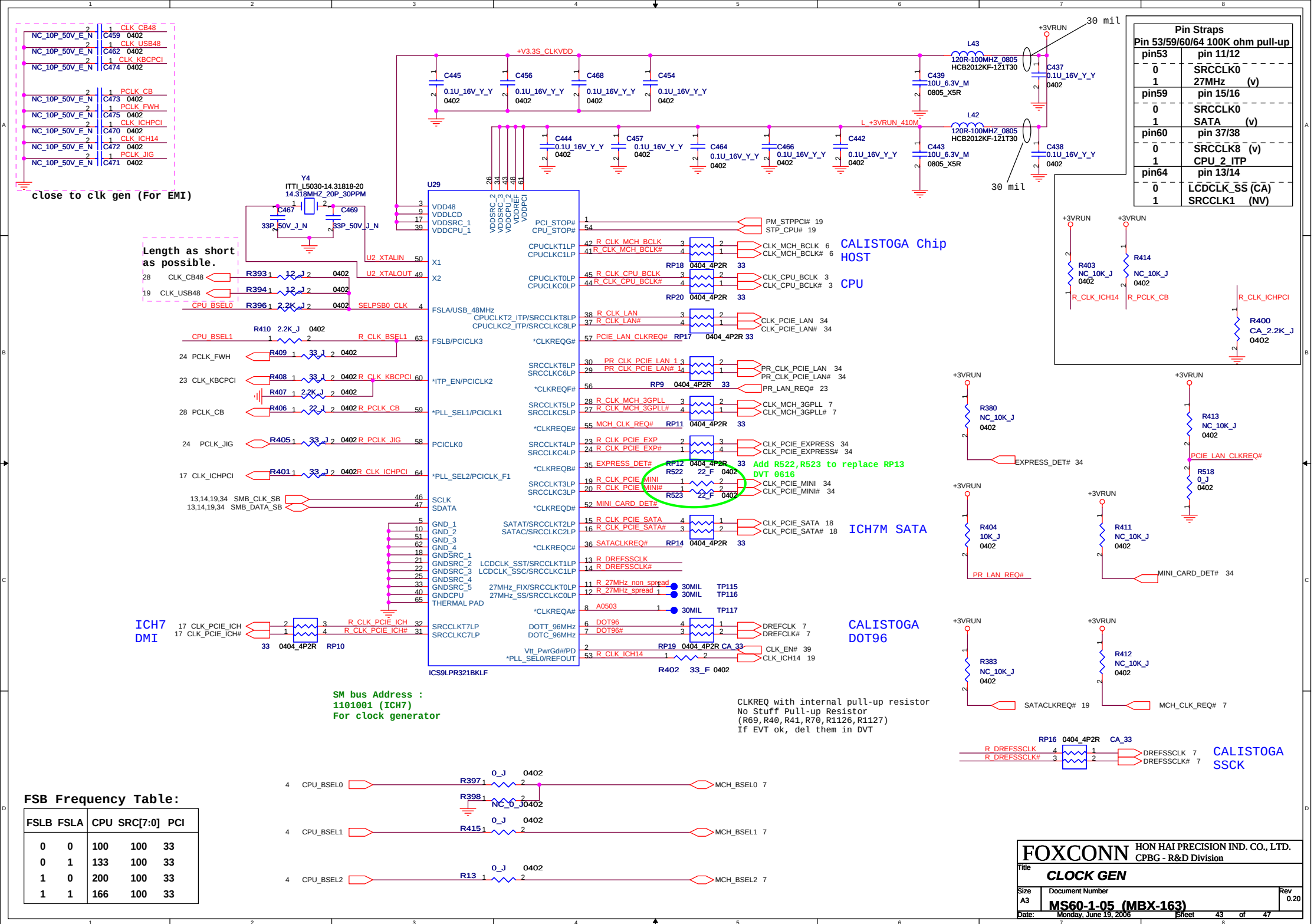


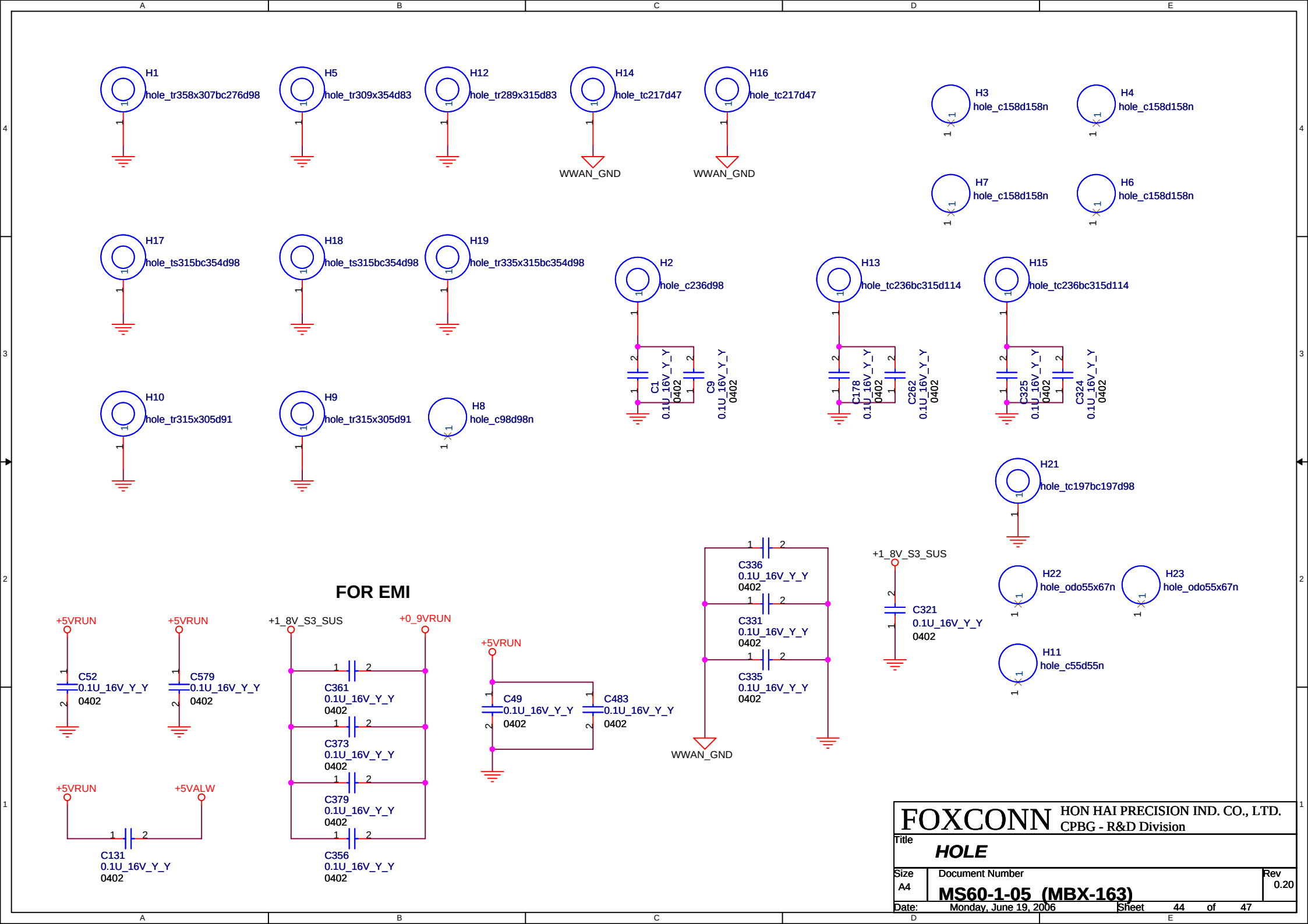


Control ACIN OCP protect

$$VIINP = I_{source} \times R_{s1} \times G_{IINP} \times R$$

VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W





MS60 Power On Sequence Timing

Version : 0.0
Modified date : 2/14/2006

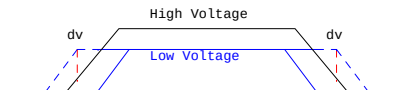
NOTE : (EC KB3910 Min. response time is 1ms)

1. T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
2. T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
3. T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
4. T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
5. T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
6. T06(Please reference Intel 16971 Page 301 of t234 timing)
7. T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
8. T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
9. T09 : For MS01 current SPEC
10. T10 :Please refer to Intel 16971 Page 300 of t214 timing
11. T11 :Please refer to Intel 16971 Page 303 of t216 timing
12. T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms;Please reference Intel 16971 Page 301of t232 timing)
13. T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
14. T14 : For MS01 current SPEC Min. is 5 ms
15. DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
16. IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
17. In 67X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
18. T15 : Please refer to MAX8771 datasheet
20. T16: Please refer to MAX8771 datasheet
21. T17 : Please refer to Intel CK410(14690) page 53
22. T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
23. CPU_PWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
24. T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark : (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

1. V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
2. V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
3. +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
4. +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
5. +3.3VRUN -> +2_5VRUN, dt:0.3mV
6. +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
7. +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV

R/C delay
(47K/
0.1uF)



T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns-2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
Power Sequence			
Size	Document Number	Rev	
C	MS60-1-05 (MBX-163)	0.20	
Date:	Monday, June 19, 2006	Sheet	45 of 47

<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage.
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout conveniently

<70>2006/05/12 PR198 change to 5.6k/0402_1% to modify 1.8V OCP seting value.
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to ''FOX_MH11747-BR2D-4F'' for ME requirement.
P/N:2N-000400N-FK00

<72>2006/05/12 CN3,CN8 change to ''FOX_GB5RF120-1200-7F'' for ME requirement.
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to ''FFOXCONN_GB5RF060_1200_7F'' for ME requirement.
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to ''FOXCONN_UB11193_C1304_4F'' for ME requirement.
P/N:1N-0004000-FE00

<75>2006/05/12 CN9 change to ''FOXCONN_HS8206E'' for ME requirement.
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to ''Panasonic,EEFSX0D331ER'' .Del PC75 for power requirement.
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.
P/N:17-2N7002D-W000
P/N:1R-0000331-J300
P/N:1R-0000104-F100
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to ''FOXCONN_PZ4782A_2743_01'' for ME requirement.
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.
P/N:1C-2N20100-J000

<80>2006/05/18 CN12,CN16 change footprint to ''FOXCONN_UB11193_C1304_4F_HM'' for DFM.

<81>2006/05/18 Add R519,R520,C593,C594 on ''IAC_BITCLK'' signal for EMI requirement.
P/N:1R-0000000-J200
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to '' hole_tc236bc315d114'' for ME requirement.
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC_IN trace for EMI requirement.
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.
P/N:1R-0000000-J200

DVT change list

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and connect GPIO_ODD_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form ''ALW_ON'' to ''ALW_ON_1'' for customer's requirement.
P/N : 1R-0000102-J200

<90>2006/06/16 PORT_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal ''VISTA_SUPPORT#'' that is connected form EC's pin99 to CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PC181 for ODD power plane.
P/N:17-S12304B-DS00
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.
P/N:17-1RF7807-2000
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT_IN power trace for EMI requirement.
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.
P/N:1C-2B30105-M000
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC_ condition for power requirement.

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title History			
Size	Document Number		Rev
Custom	MS60-1-05 (MBX-163)		0.20
Date:	Monday, June 19, 2006	Sheet	47 of 47