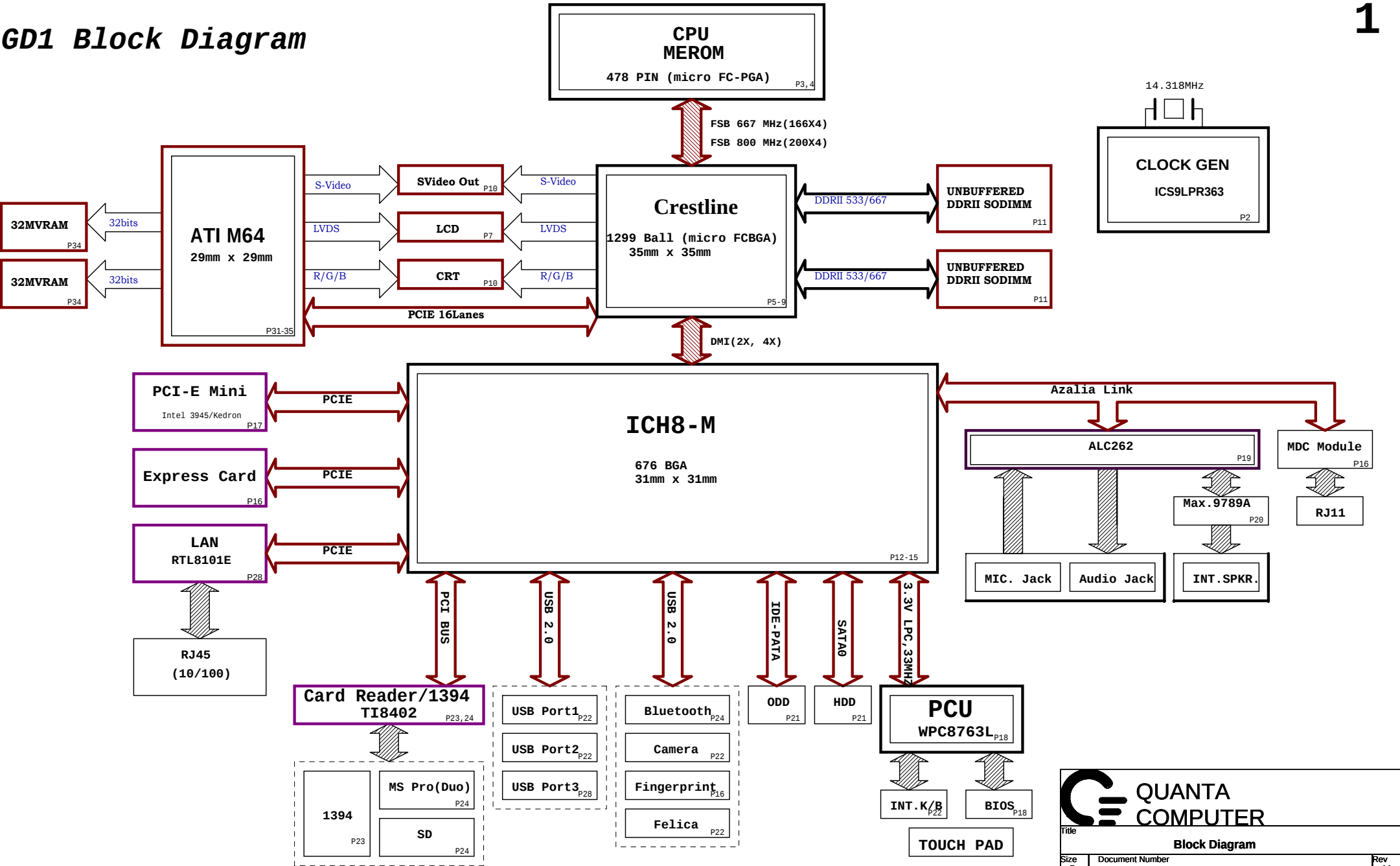
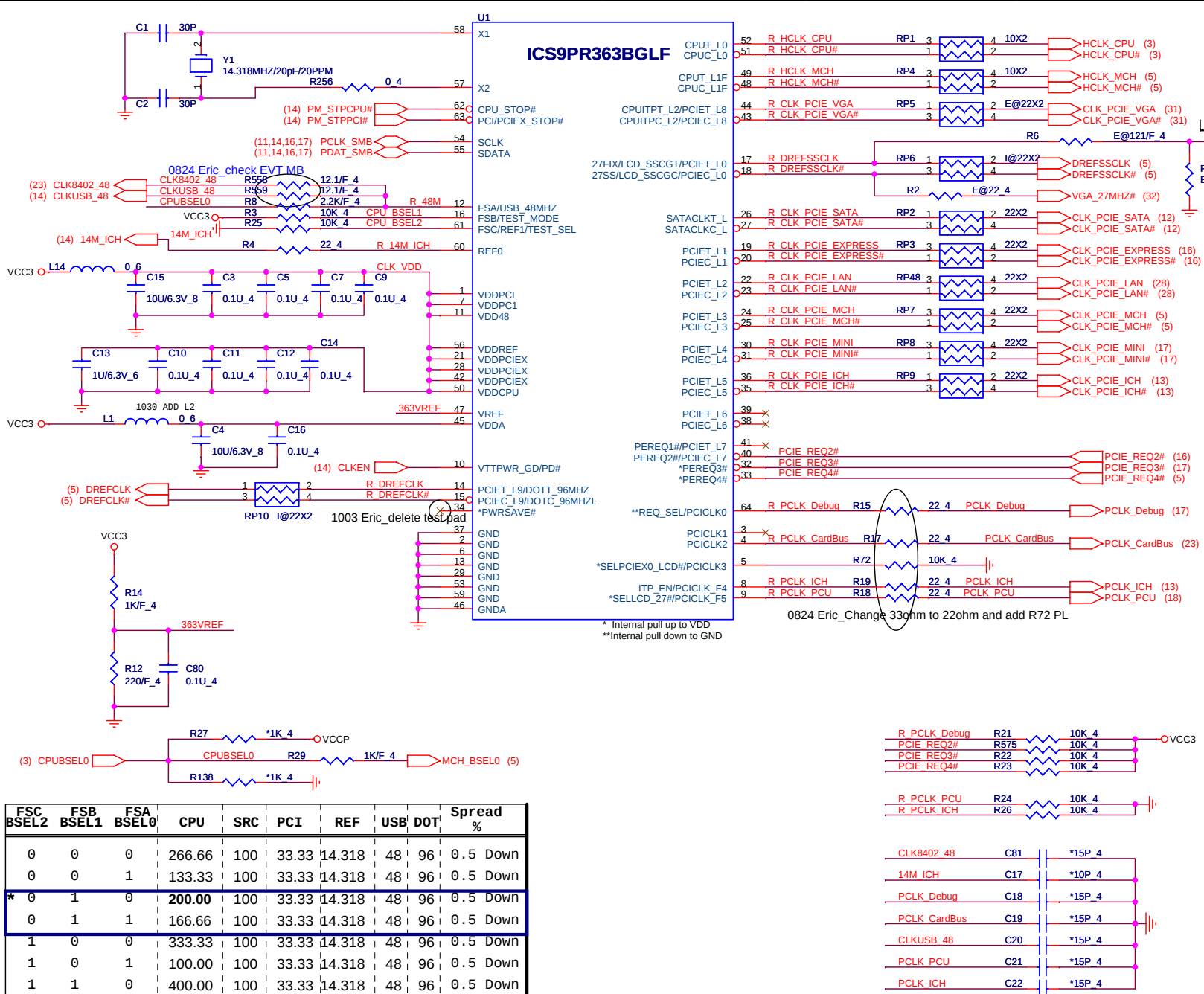


GD1 Block Diagram



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Check level M64=1.2V; M72/74=1.8V

Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
VGA_27MHZ#	R7	NI	71.5
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R494	PIN 9 R26	PIN 14/15	PIN 17/18
LO (10K)	LO (10K)	PCIEX9	27MHZ
HI (NC)	HI (NC)	DOT96	LCD
HI (NC)	HI (NC)	PCIEX9	PCIEX0
		DOT96	PCIEX0

ITP_EN(PIN8)

LOW : PIN43/44 SRC

HIGH : PIN43, 44 CPUTP

PCIE_REQ1#	PCIE_L0	PCIE_L6
PCIE_REQ2#	PCIE_L1	PCIE_L8
PCIE_REQ3#	PCIE_L2	PCIE_L4
PCIE_REQ4#	PCIE_L3	PCIE_L5

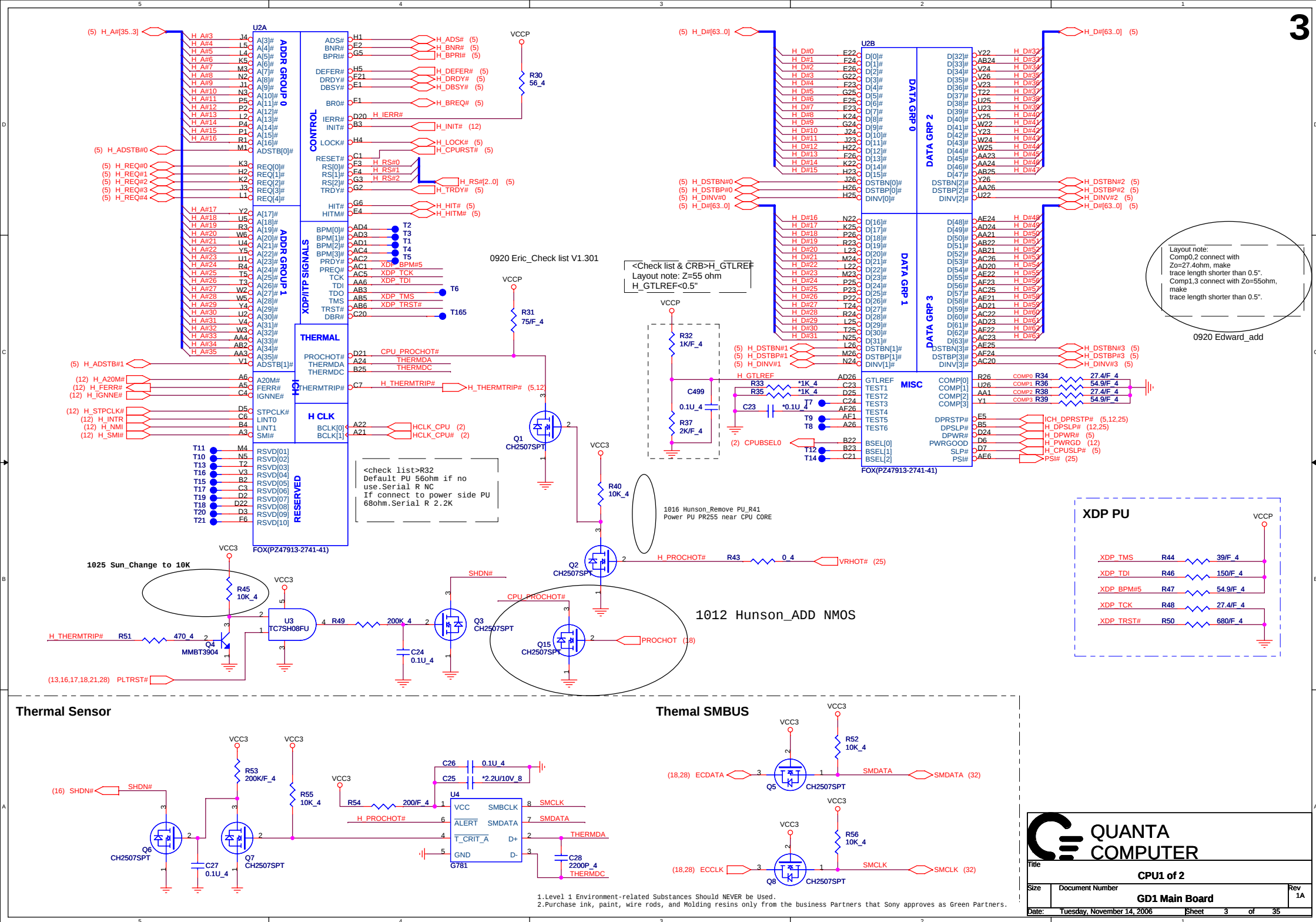
QUANTA
COMPUTER

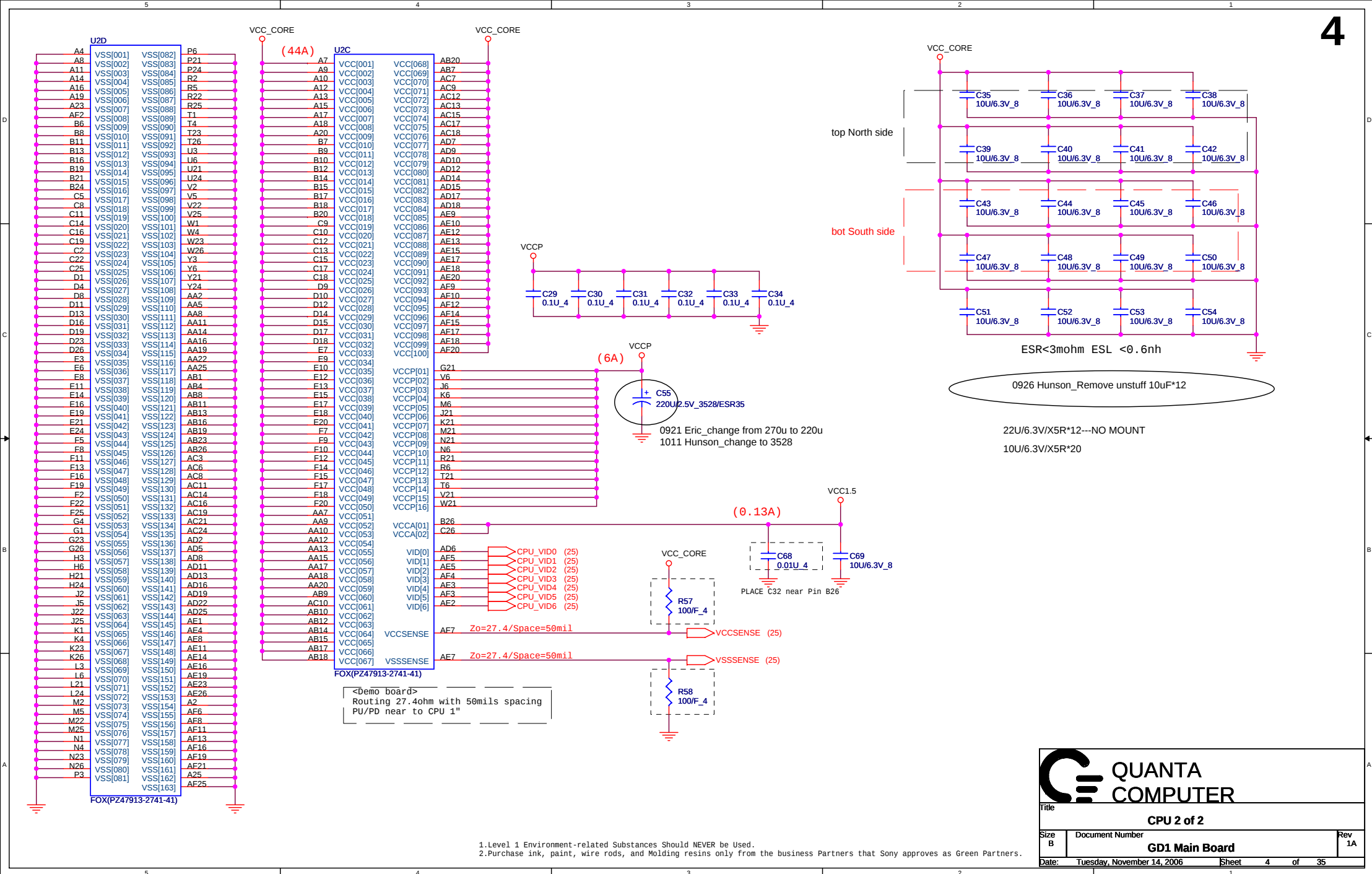
Title: **CLOCK GENERATOR**

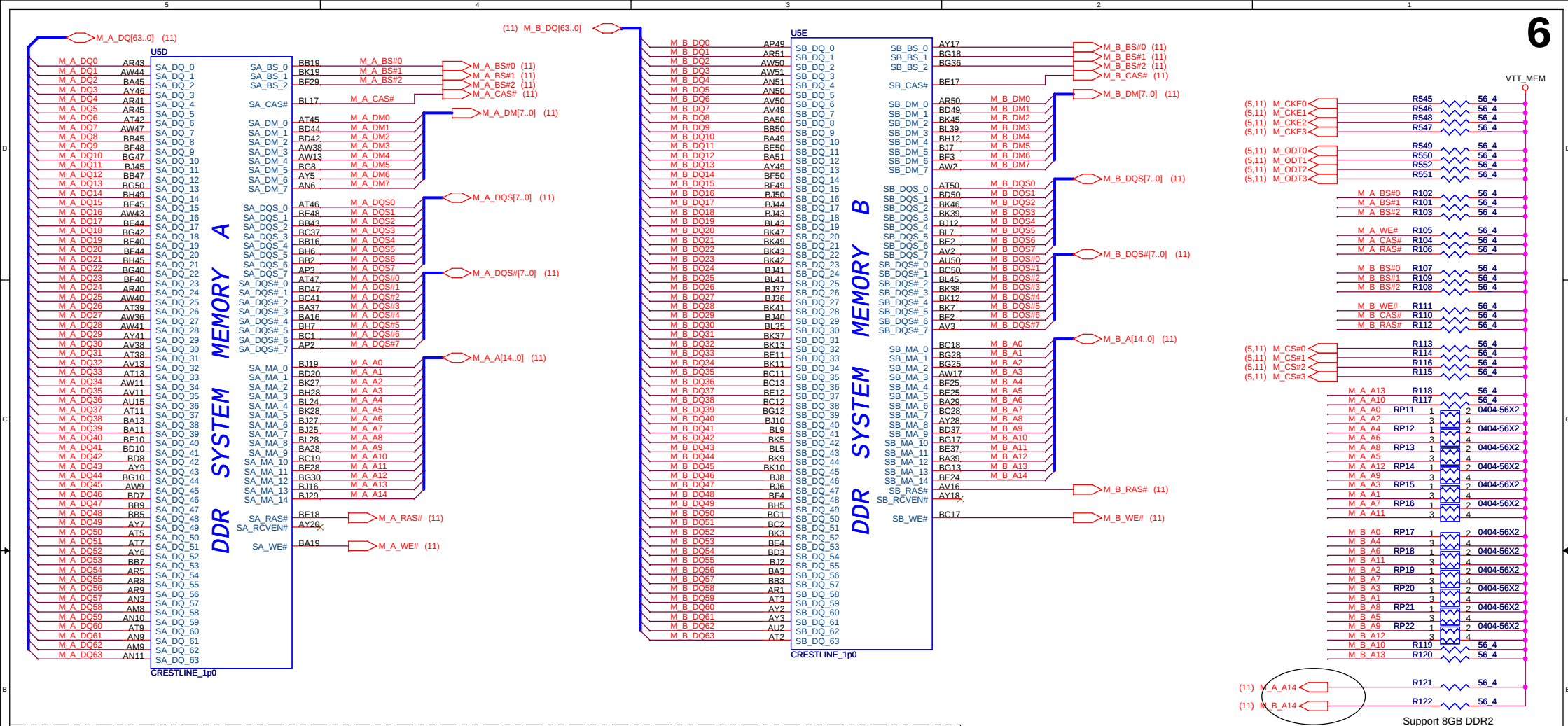
Size B Document Number: **GD1 Main Board** Rev 1A

Date: Wednesday, November 15, 2006 Sheet 2 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

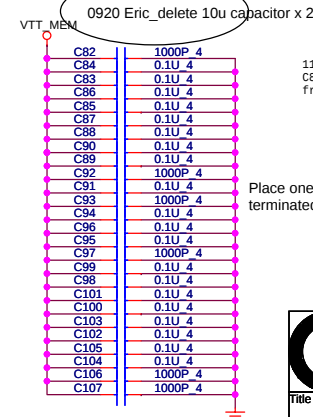
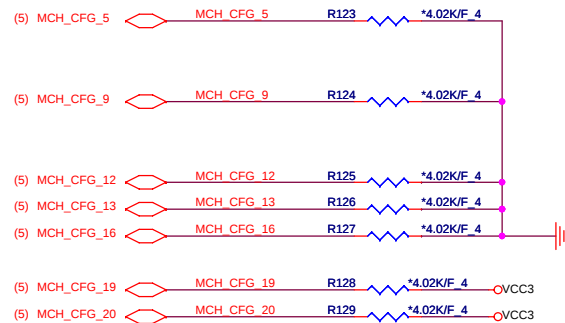






GMCH Strap pin description

	Low	High
C6F5	DMiX2	* DMiX4
C6F6		RSVD for 945GMS
C6F7	RSVD	* CPU type: Mobile CPU
C6F9	PCIE Graphics lan : Reverse Lane	* PCIE Graphics lan : Normal operation
C6F10		reserved
C6F11		reserved
C6F16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
C6F18 *	GMCH core: 1.05V	GMCH core: 1.5V
C6F19 *	DMI LANE Normal	DMI LANE Reversed
C6F20 *	only SDVO or PCIE x1 is operational	SDVO and PCIE x1 are operation simultaneously via the PEG port
C6F[13:12]	00 = Partial clock gating disable 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)	
Int.Pull-down : C6F 18,19,20 Int.Pull-high : C6F C6 3-17		

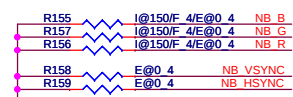
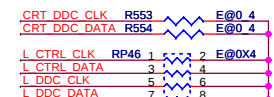
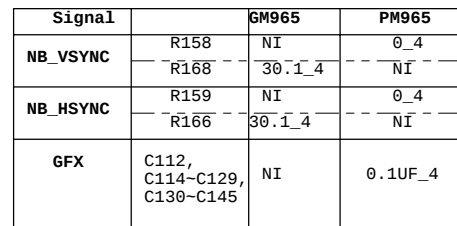


1192 Hunson change
C82, C92, C93, C97, C106, C107 to 1000P
from RF interference

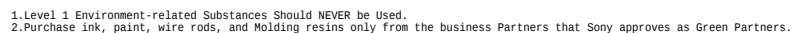
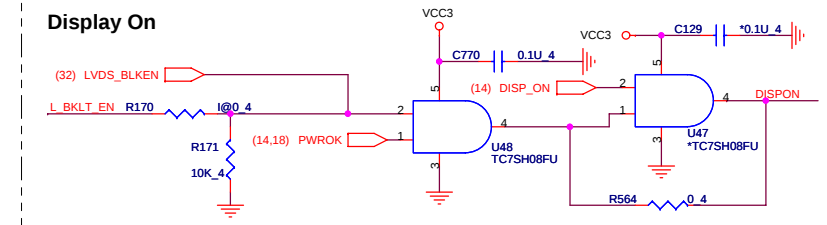
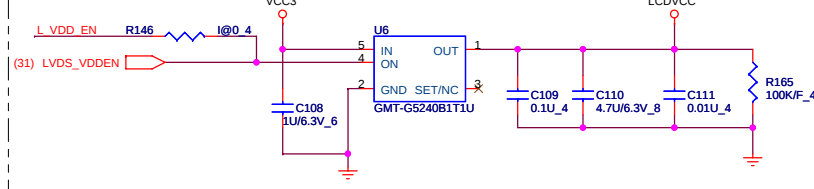
Place one cap close to every 2 pull-up resistors
terminated to VccSus0_9(Total 0.1u x 26)

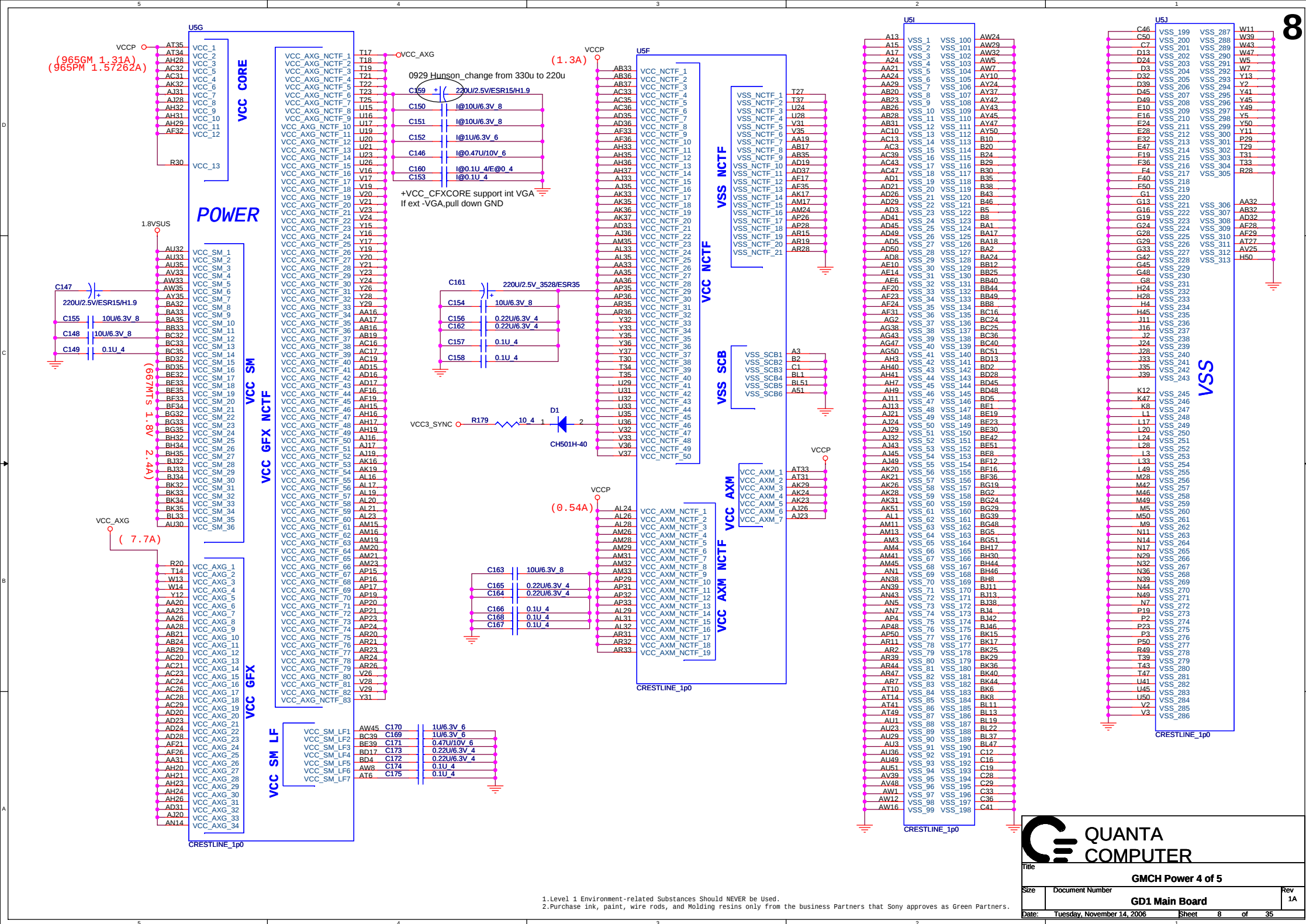
QUANTA
COMPUTER

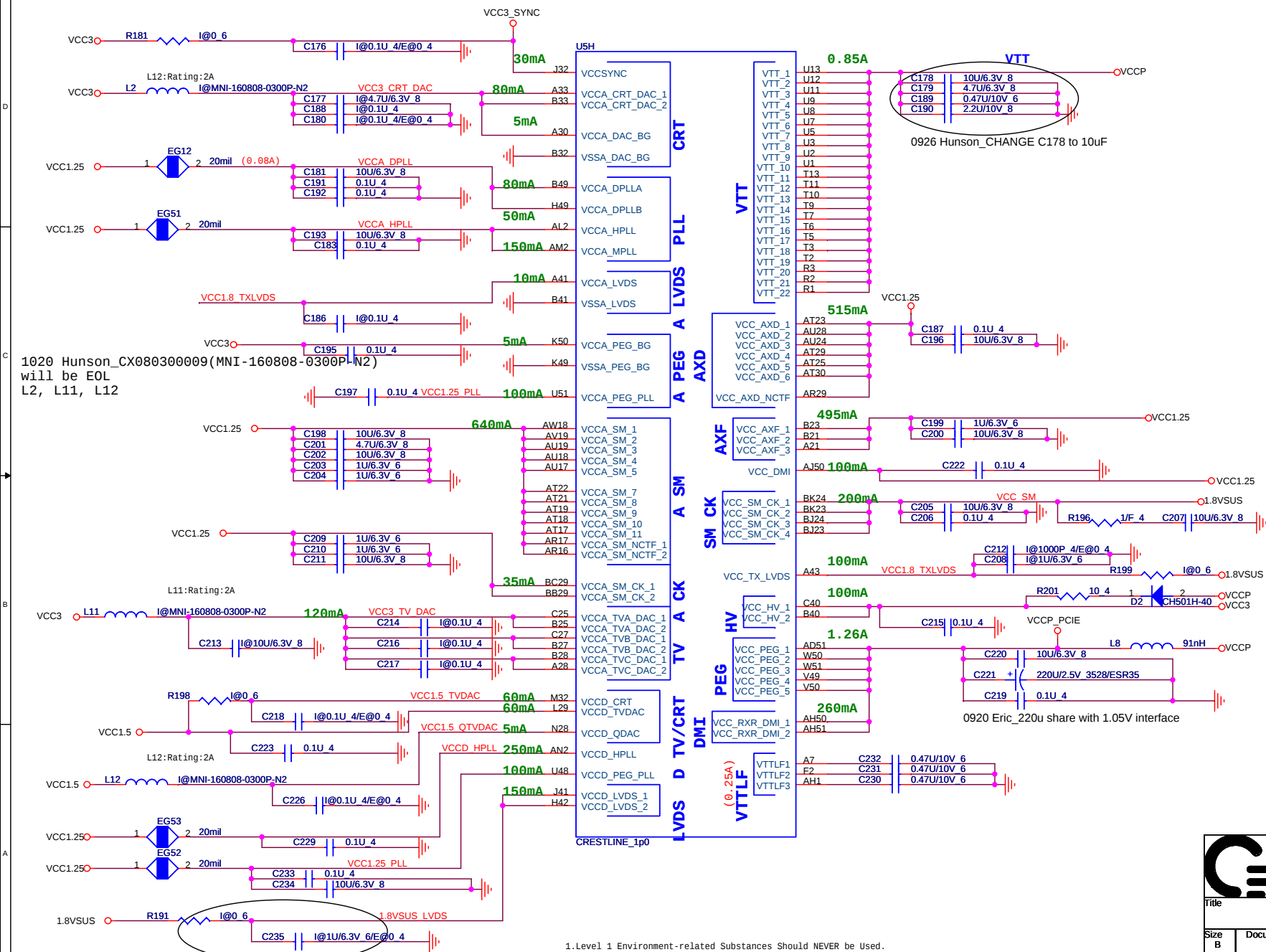
Title				GMCH DDR II 2 of 5				Rev 1A
Size		Document Number						
		GD1 Main Board						
Date:		Tuesday, November 14, 2006		Sheet		6 of 35		



Signal		9656M	965PM
NB_B	R160	0_4	NI
	R155	150_4	0_4
NB_G	R161	0_4	NI
	R157	150_4	0_4
NB_R	R162	0_4	NI
	R156	150_4	0_4
L_IBG	R147	2.4K_4	NI
LVDS	RP38 RP41~RP43	0X2	NI
L_BKLT_EN	R170	0_4	NI
L_CTRL_CLK	R130	10K	NI
	RP46	NI	0X4
L_CTRL_DATA	R145	10K	NI
	RP46	NI	0X4
LVDS_VDDEN	R146	0_4	NI
DDC2BC	R163	0_4	NI
	R553	NI	0_4
DDC2BD	R164	0_4	NI
	R554	NI	0_4
CRT_TV0_IREF	R167	1.3K_4	0
L_DDC_CLK	RP46	NI	0X4
L_DDC_DATA	RP46	NI	0X4
BRIGHT	R173	0_4	NI
	R175	NI	0_4







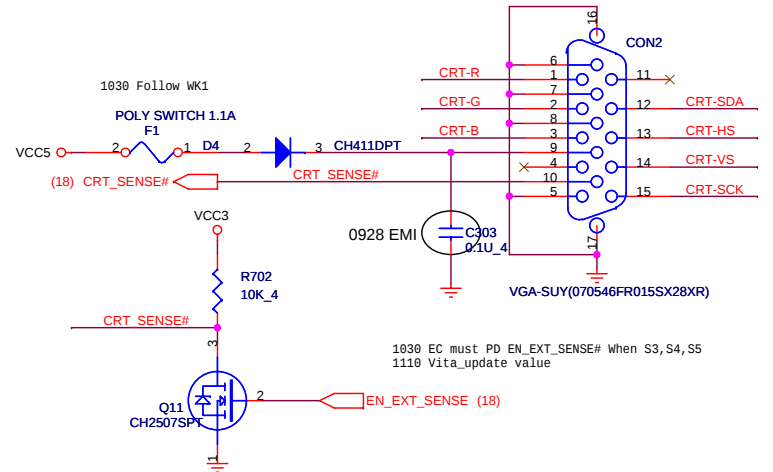
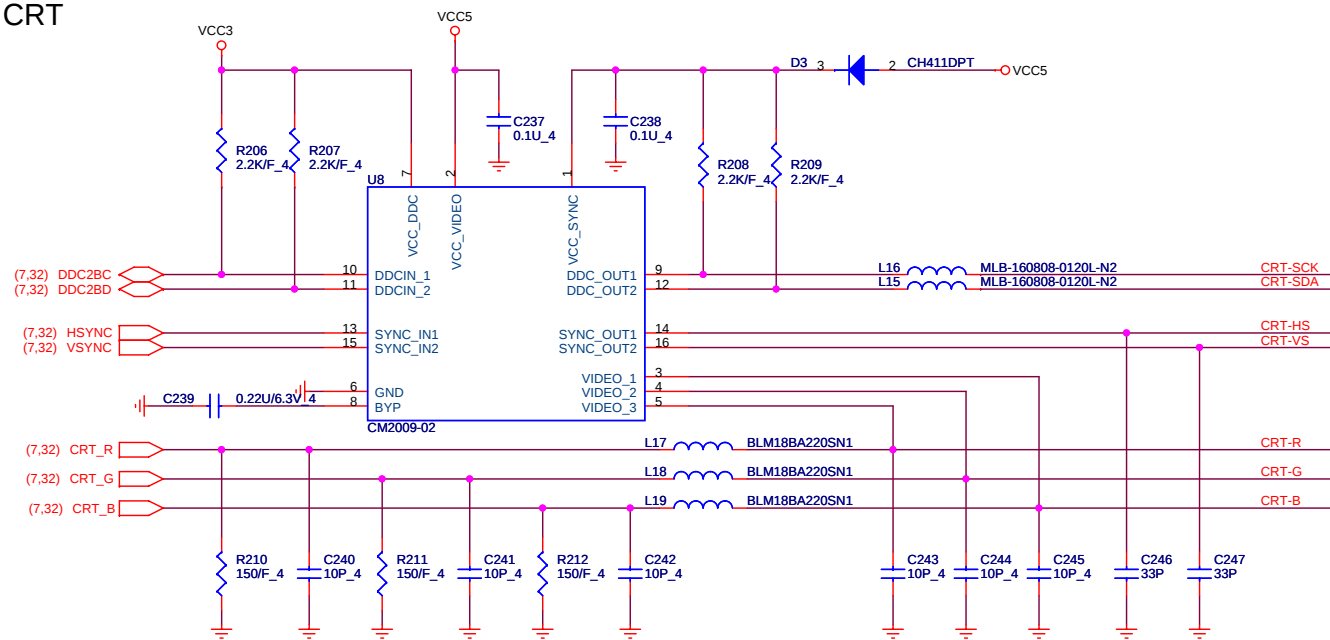
Signal		965GM	965PM
VCCA_TV_DAC	L12	V	X
	C244	V	X
	C245	V	X
	C246	V	X
	C248	V	X
VCC1.5_TVDAC	L14	V	X
	C250	V	X
	C247	V	X
	R195	X	V
VCC1.5_QTVDAC	L17	V	X
	C257	V	X
	C258	V	X
	R197	X	V

Signal		965GM	965PM
VCCA_DAC_BG	L8	V	X
	C214	V	X
	R181	X	V
VCCSYNC	R177	V	X
	C201	V	X
	C202	V	X
	R178	X	V
VCC3_CRT_DAC	L7	V	X
	C203	V	X
	C211	V	X
	R179	X	V
VCCD_LVDS	R198	V	X
	C265	V	X
	C264	V	X
	R199	X	V
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
VCC_TX_LVDS	R192	V	X
	C240	V	X
	C238	V	X
	R191	X	V

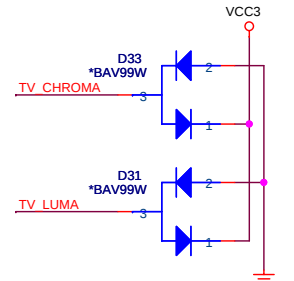
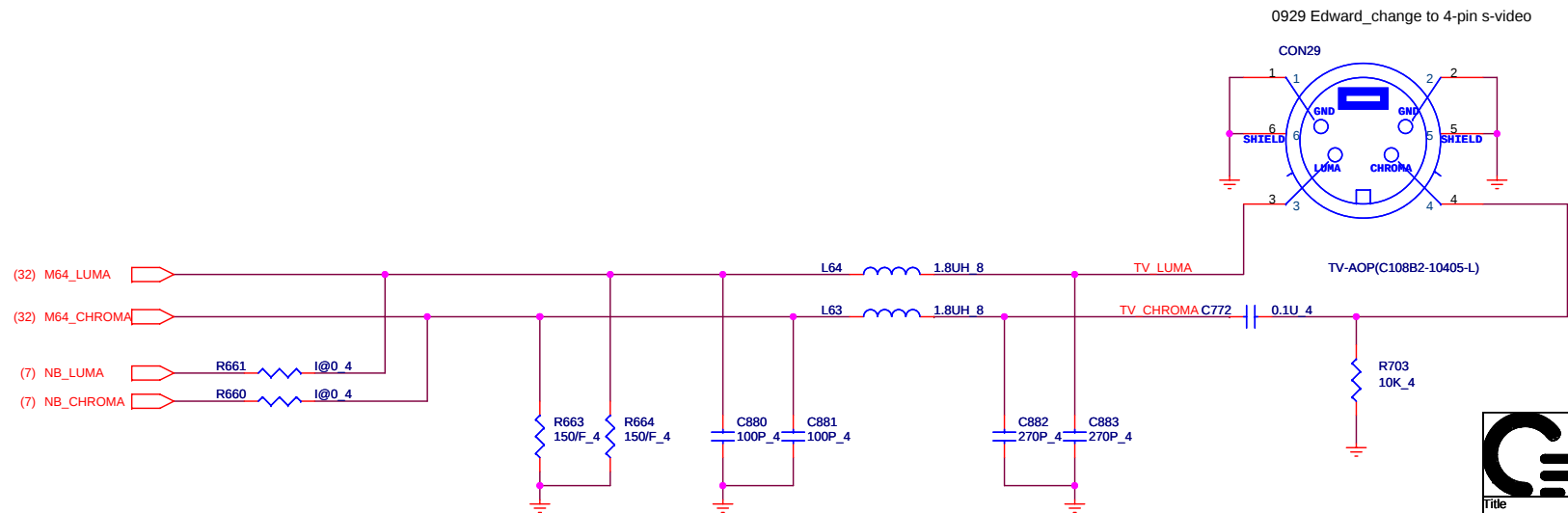


Title				
GMCH Power 2 5 of 5				
Size	Document Number			Rev
B	GD1 Main Board			1A
Date:	Tuesday, November 14, 2006	Sheet	9	of 35

CRT

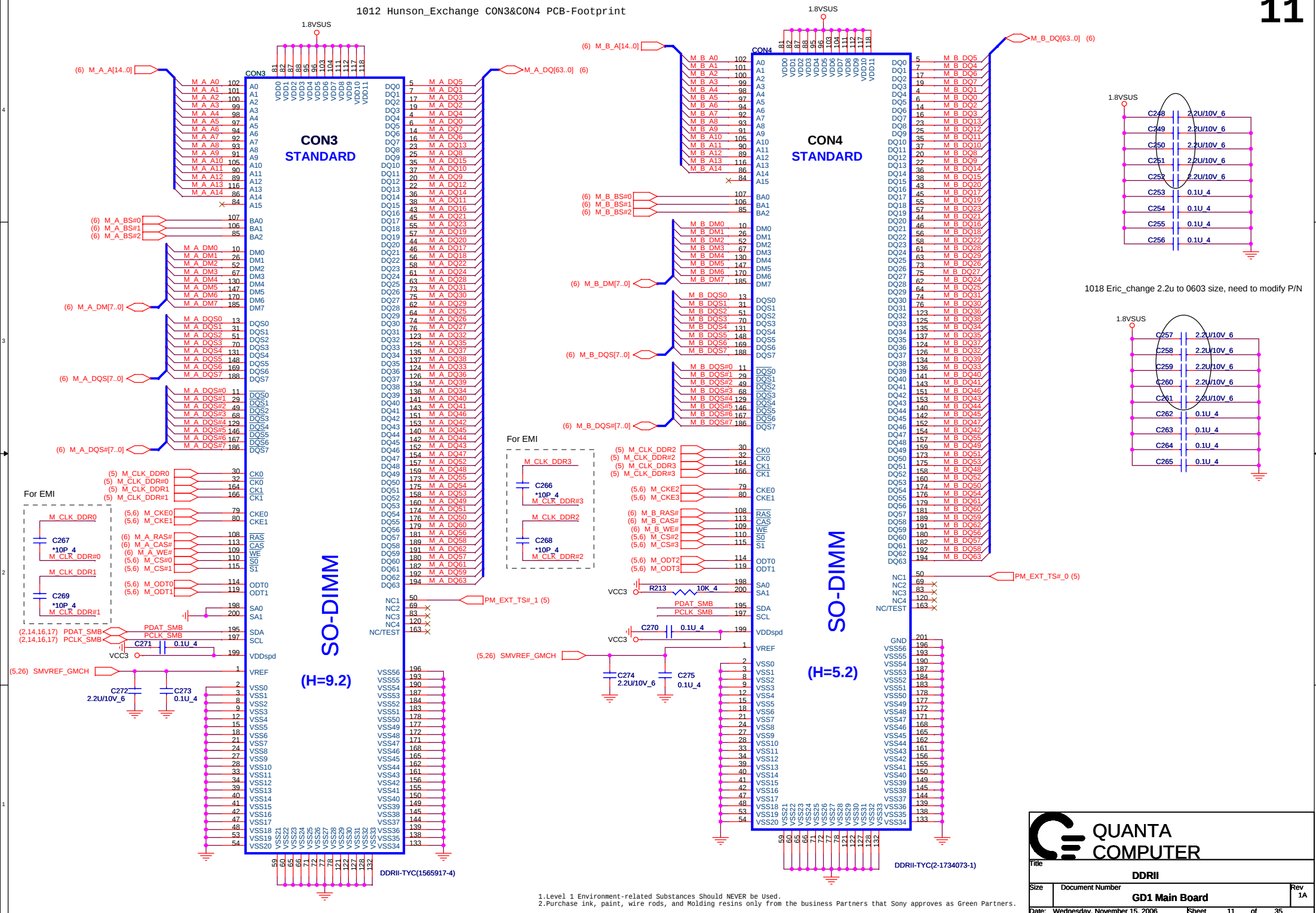


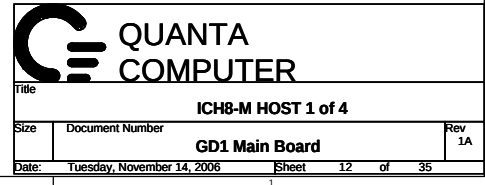
S-VIDEO_OUT



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER	
Title	
CRT & S-VIDEO	
Size	Document Number
B	
GD1 Main Board	
Date:	Wednesday, November 15, 2006
Sheet	10 of 35
Rev	1A



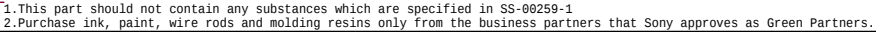


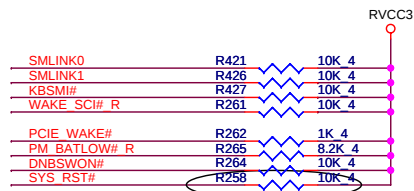
PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

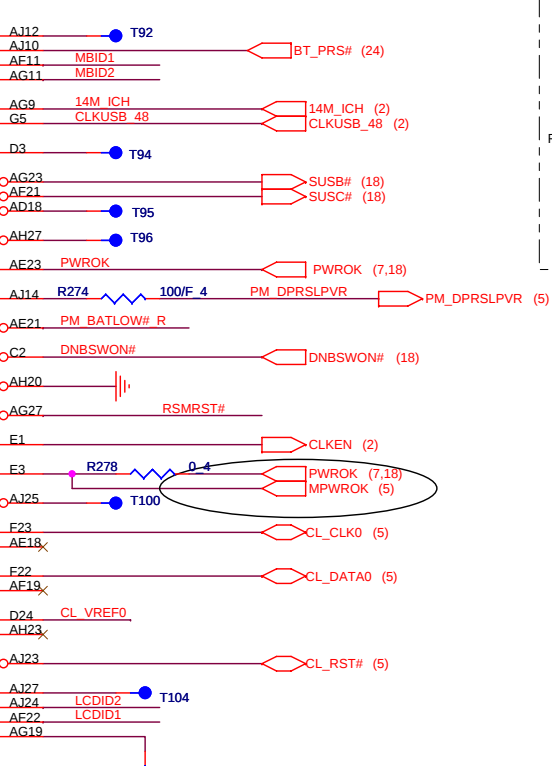
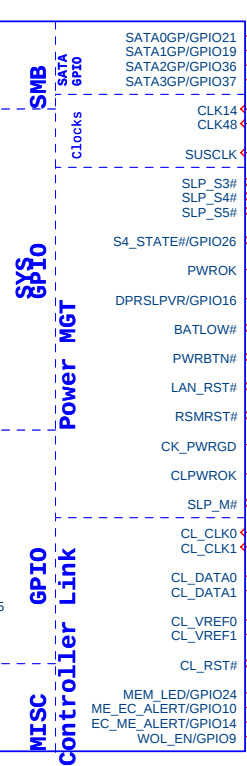
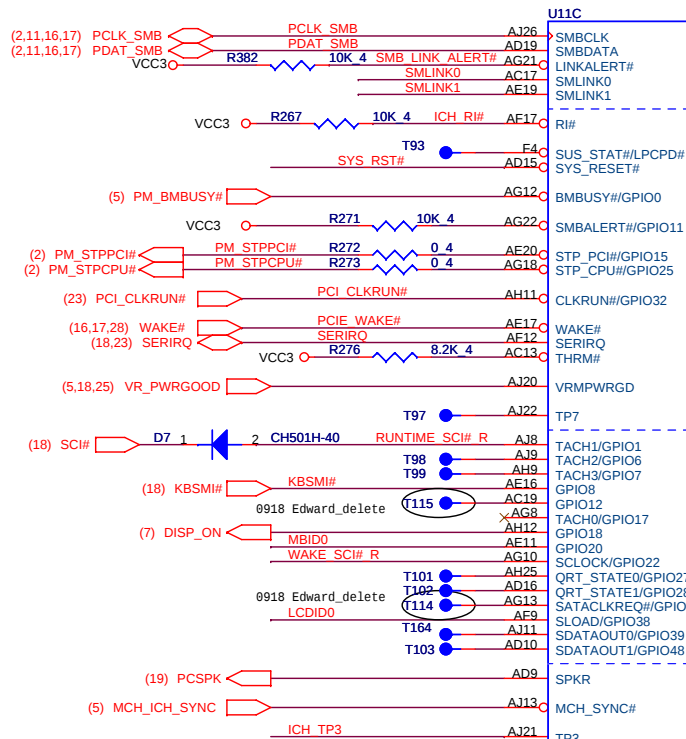
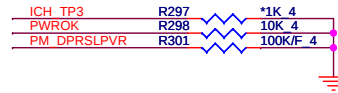
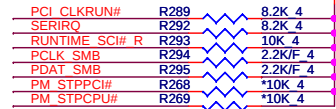


Title	ICH8-M PCIE 2 of 4		
Size B	Document Number GD1 Main Board	Rev 1A	
Date:	Tuesday, November 14, 2006	Sheet	13 of 35



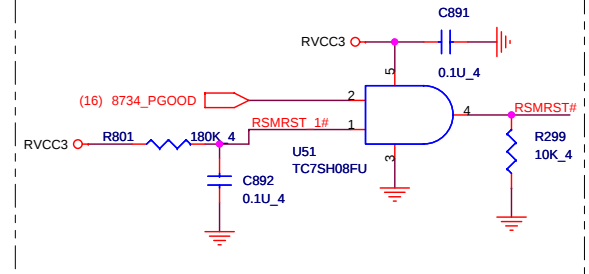


0915 Edward.Tsai follow intel check list



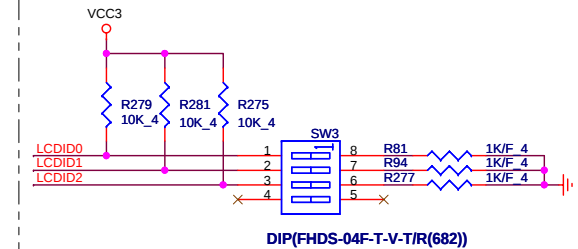
RSMRST# must be after RVCC3 10 ms

RSMRST#

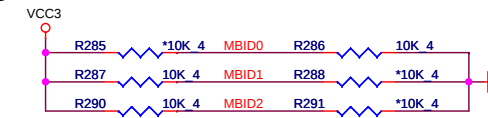


LCD ID

1012 Edward_Change SW3 PN#



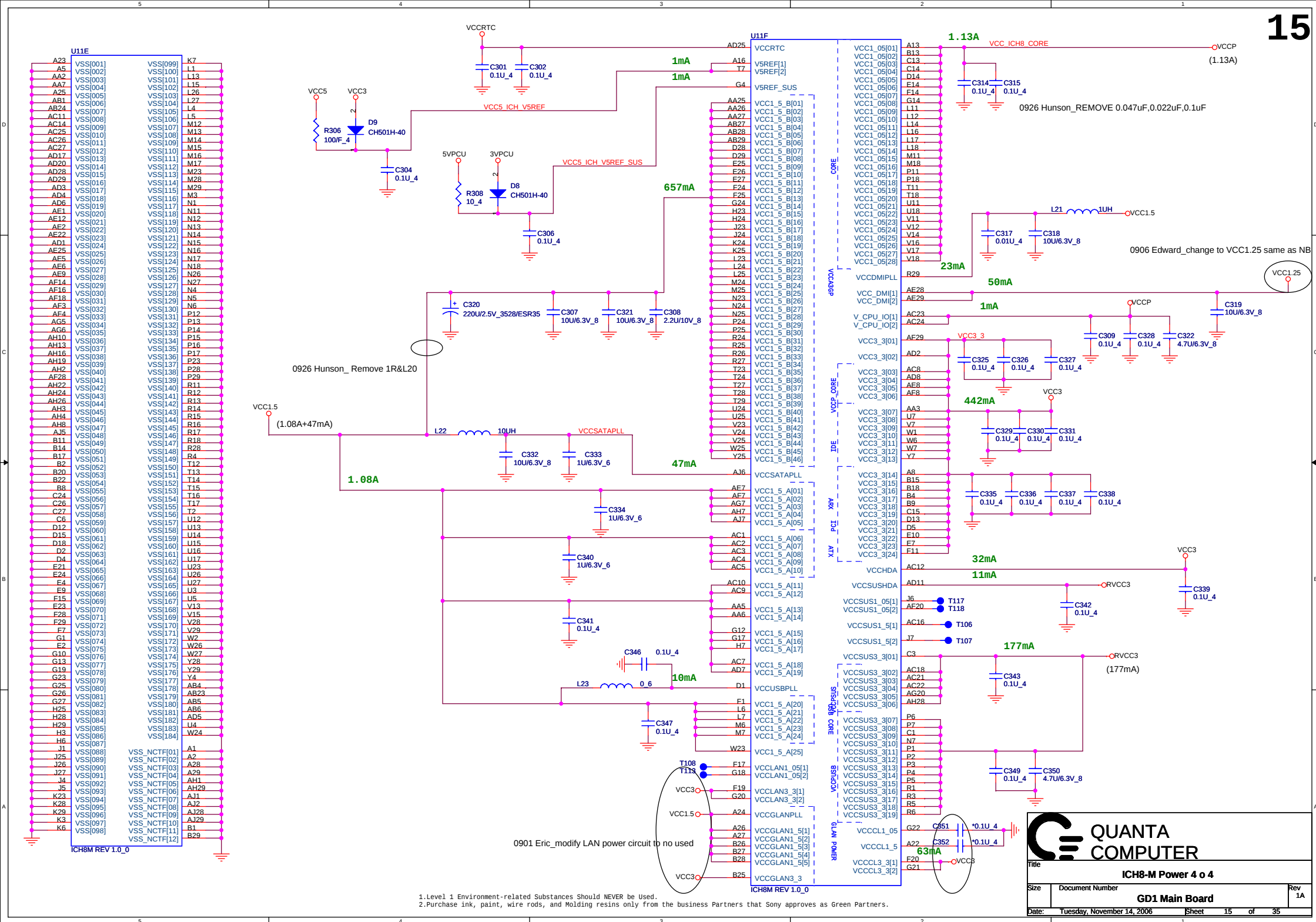
MB ID



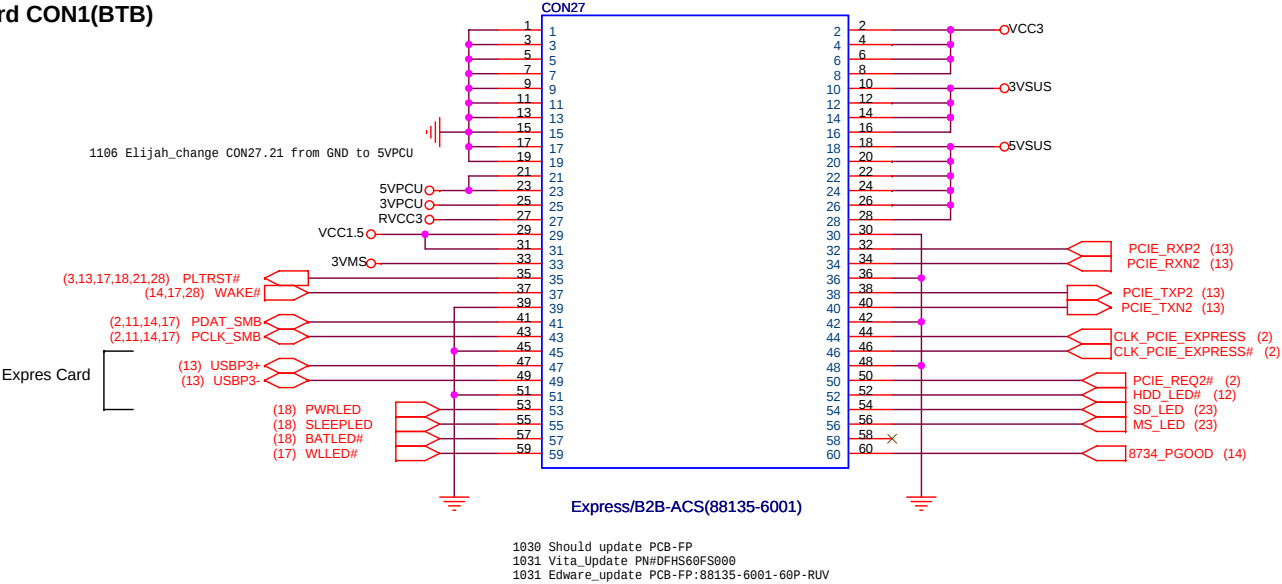
QUANTA
COMPUTER

Title		
ICH8-M GPIO 3 of 4		
Size	Document Number	Rev
B	GD1 Main Board	1A
Date:	Wednesday, November 15, 2006	Sheet 14 of 35

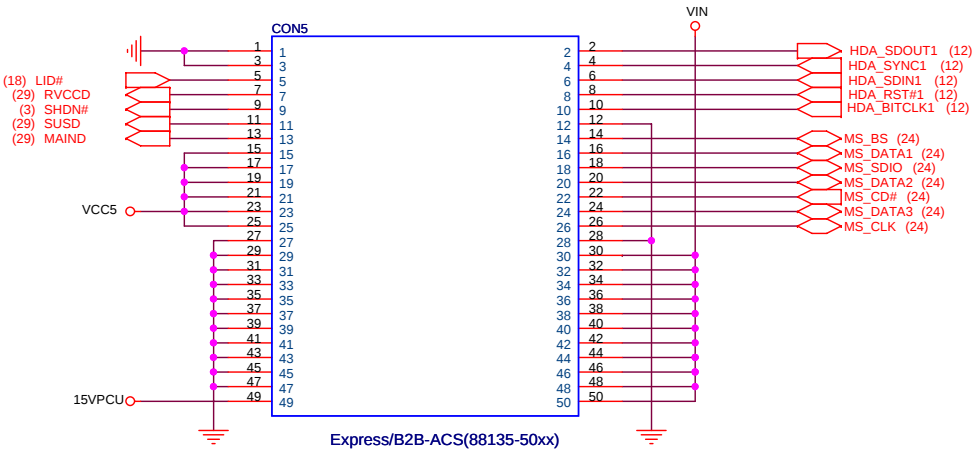
- Level 1 Environment-related Substances Should NEVER be Used.
- Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



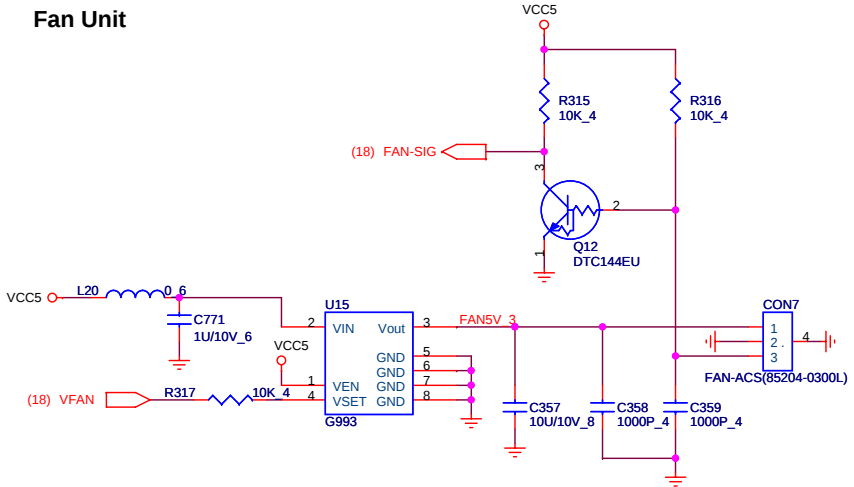
Express Board CON1(BTB)



Express Board CON2(BTB)



Fan Unit



Title		
Express Card		
Size	Document Number	Rev
B		1A
GD1 Main Board		
Date:	Tuesday, November 14, 2006	Sheet 16 of 35

1. This part should not contain any substances which are specified in SS-00259-1.
2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

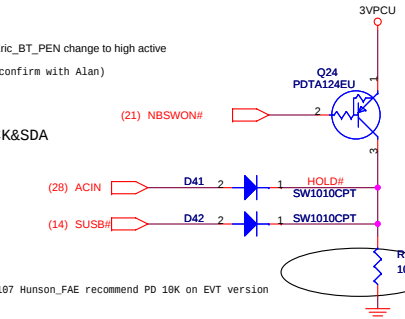
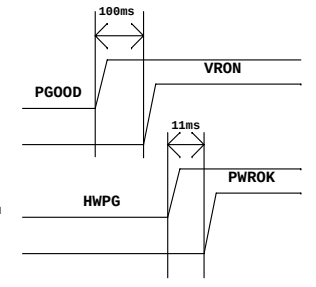
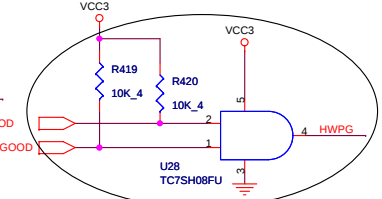
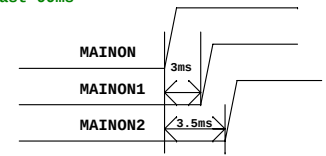
I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	[HCFGBAH, HCFGBAL] [HCFGBAH, HCFGBAL]+1	
0 1	XOR-TREE TEST	

DOCK_RST# *BADDR0
DK_BAY_PWEN: BADDR1

BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
VRON must be after PGOOD at least 99ms

MAINON <-- 3ms --> MAION1
MAINON <-- 3.5ms --> MAION2

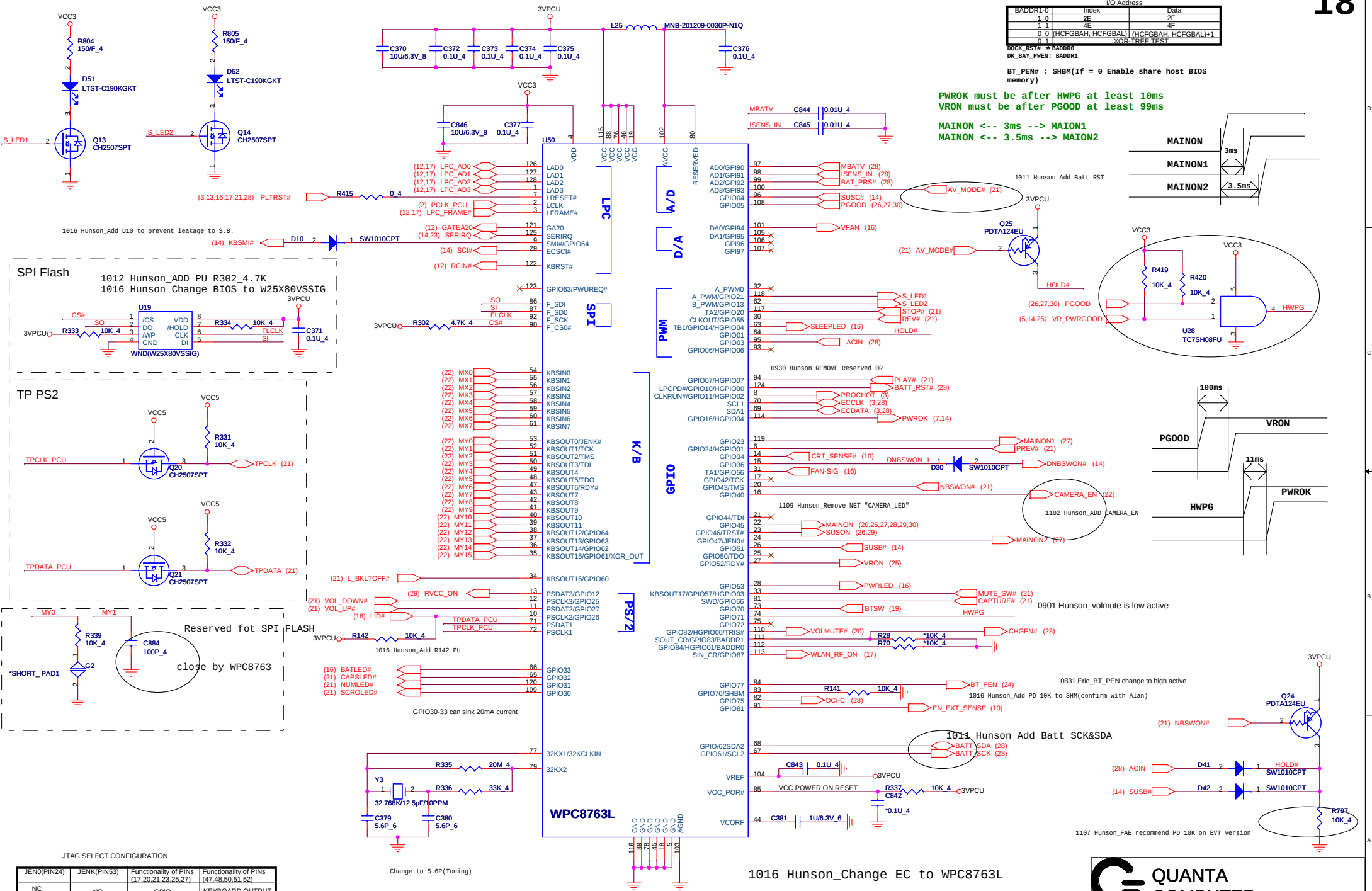


1107 Hunson_FAE recommend PD 10K on EVT version

1016 Hunson_Change EC to WPC8763L

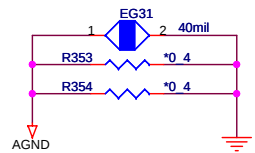
QUANTA COMPUTER		
Title: WPC8763L & SPI FLASH		
Size	Document Number	Rev 1A
G01 Main Board		
Date:	Tuesday, November 14, 2006	Sheet 18 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



JTAG SELECT CONFIGURATION			
JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD	Illegal Strap combination	

Audio decoupling



1101 FAE comment

(20) EAPD

VCC3

Low enable speaker

High enable HP

0928 EMI

1101 FAE comment

Analog MIC Connector

1013 Hunson Add Pre_AMP(MAX9812H) in MIC/B
1020 Hunson_Change 87213-0400G

Audio/B CON(B2B)

- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

ALC262

ALC262-VC2-GR

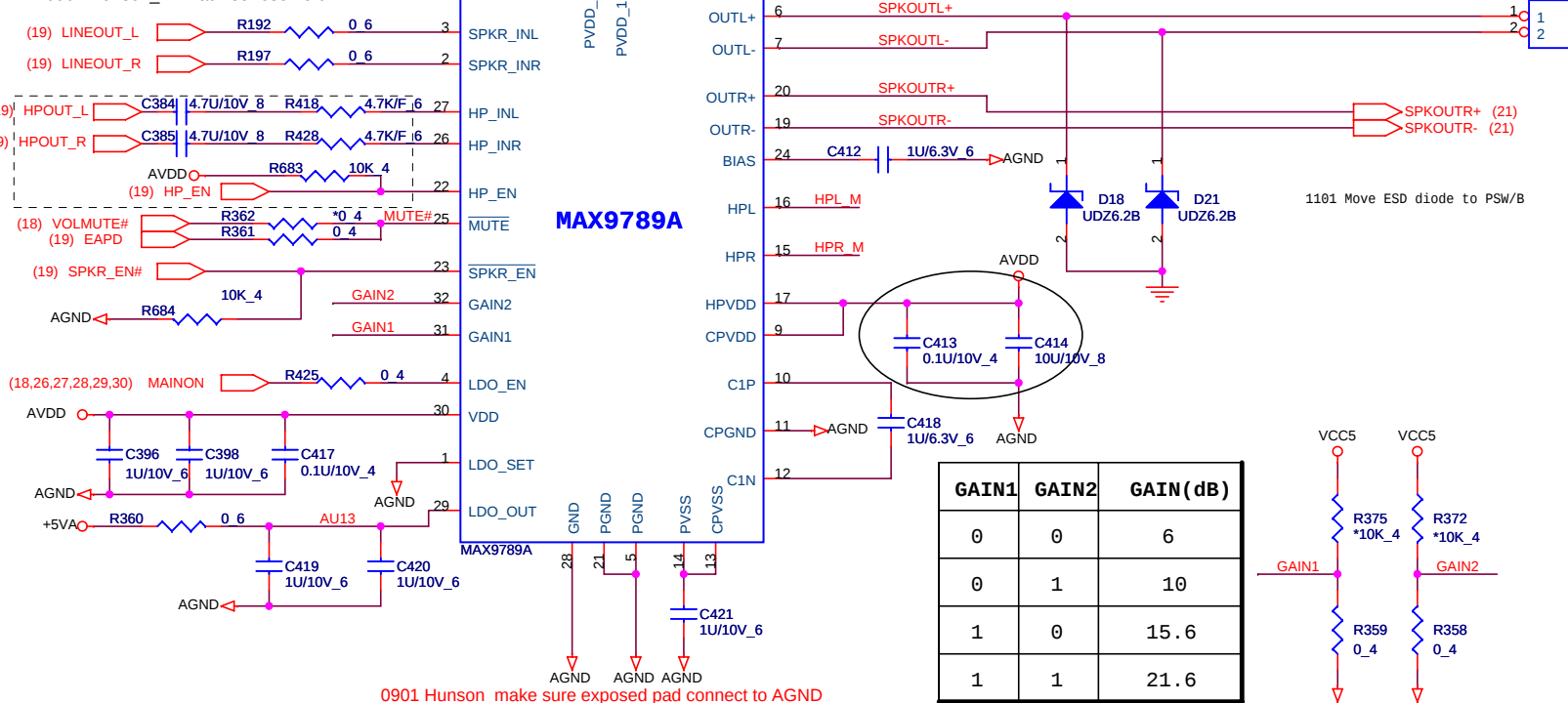
AUDIO/B ACS(88135-1601)



Title			Audio ALC268	
Size	Document Number	Rev		1A
Custom	GD1 Main Board			
Date:	Tuesday, November 14, 2006	Sheet	19	of 35

0904 Hunson_best Frequency response
with 9789A from FAE comment

0904 Hunson_FAE advise reserve 0R

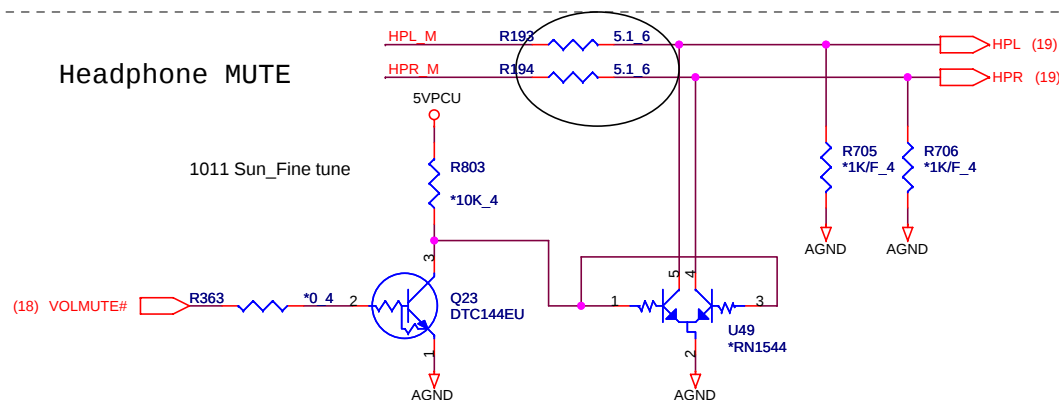


0901 Hunson_make sure exposed pad connect to AGND

1101 Move ESD diode to PSW/B

Headphone MUTE

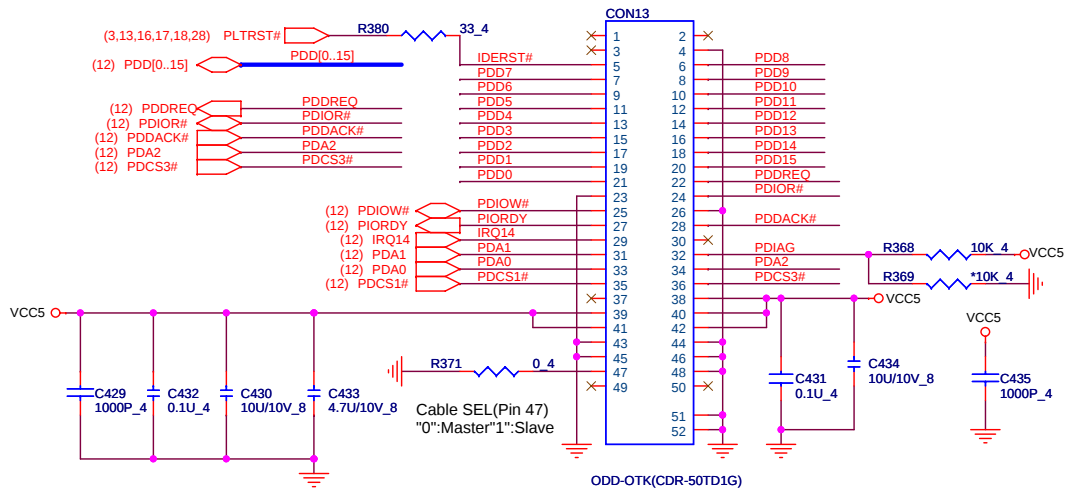
1011 Sun_Fine tune



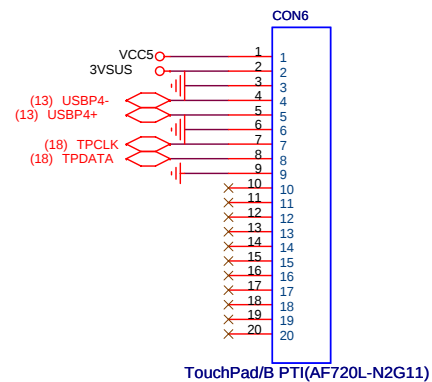
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Title		
Audio AMP. & Speaker		
Size	Document Number	Rev
Custom	GD1 Main Board	1A
Date:	Tuesday, November 14, 2006	Sheet 20 of 35

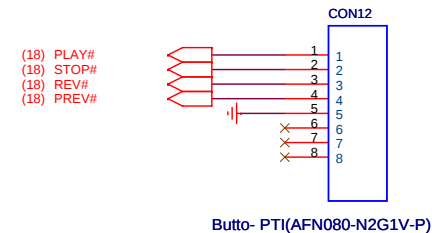
ODD CONNECTOR



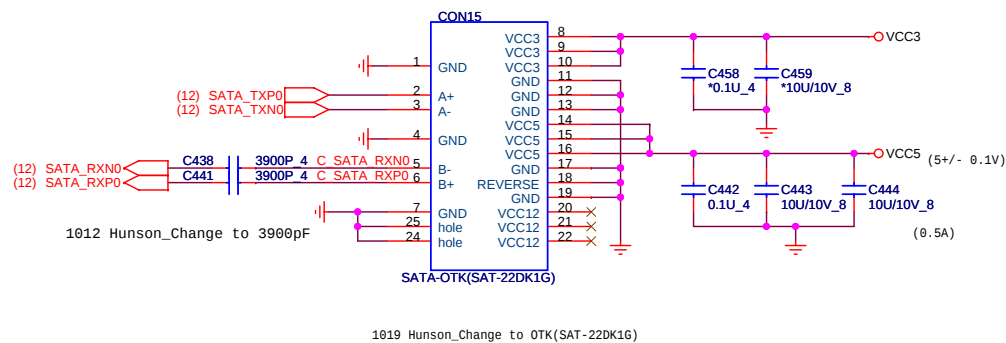
TouchPAD Board CON(FFC)



Button CON(FFC)

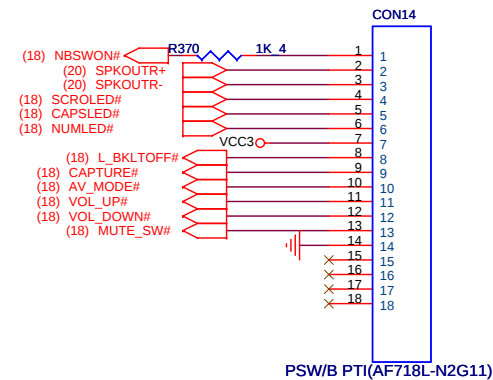


HDD CONNECTOR



PSW Board CON(FFC)

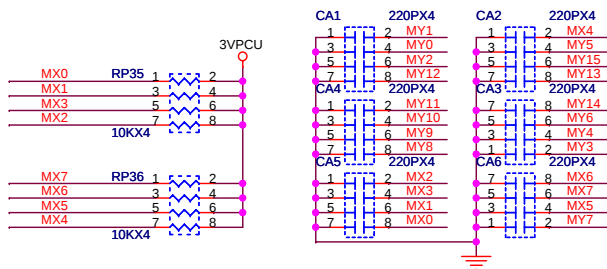
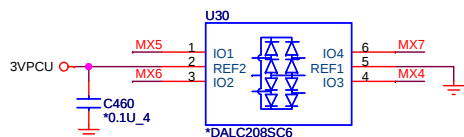
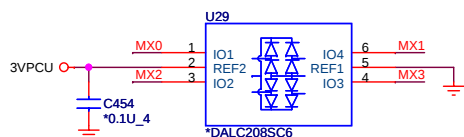
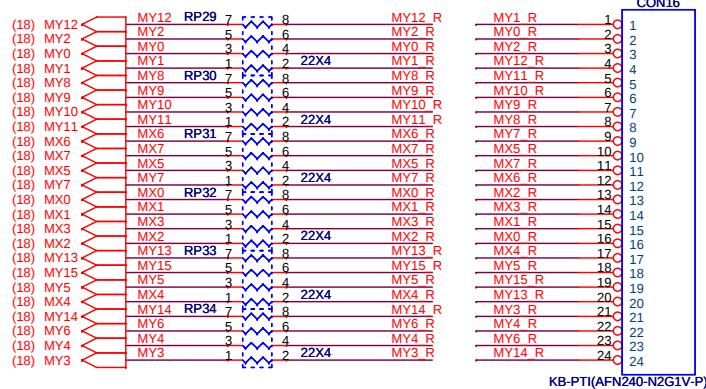
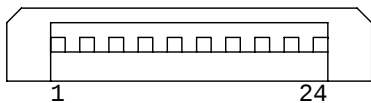
1031 Hunson_update PCB-FP



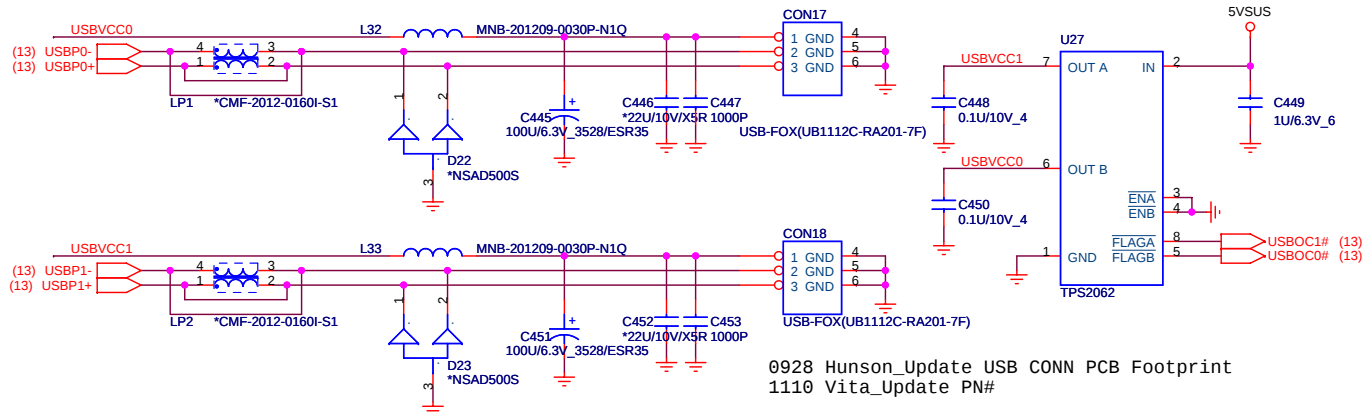
- Level 1 Environment-related Substances Should NEVER be Used.
- Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER	
Title: HDD/ODD/PW CON	
Size: B	Document Number: GD1 Main Board
Date: Wednesday, November 15, 2006	Rev: 1A
Sheet: 21	of 35

Keyboard

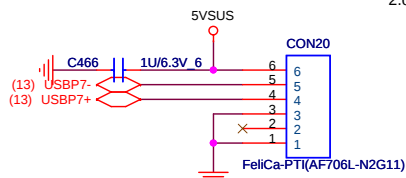


USB Port x 2



0928 Hunson_Update USB CONN PCB Footprint
1110 Vita_Update PN#

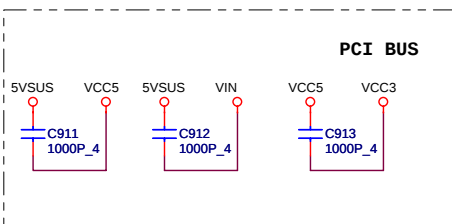
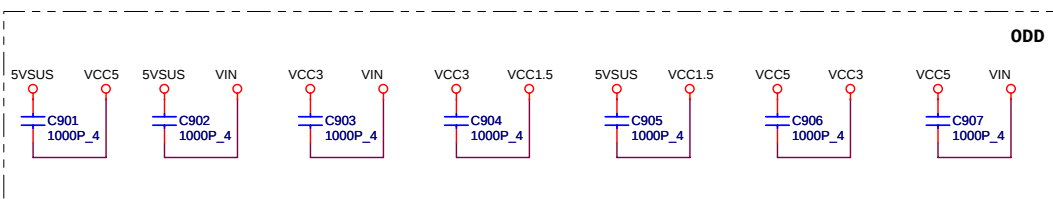
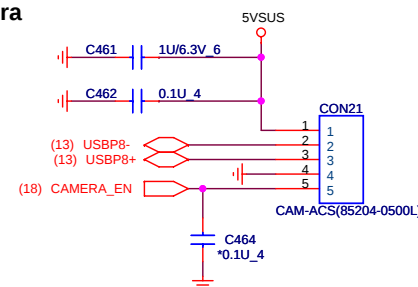
Felica



1012 Edward_Change CON20 PN#(gold-pating)

0929 Eric_
1.change material to gold plating
2.change Foot Print to PTI

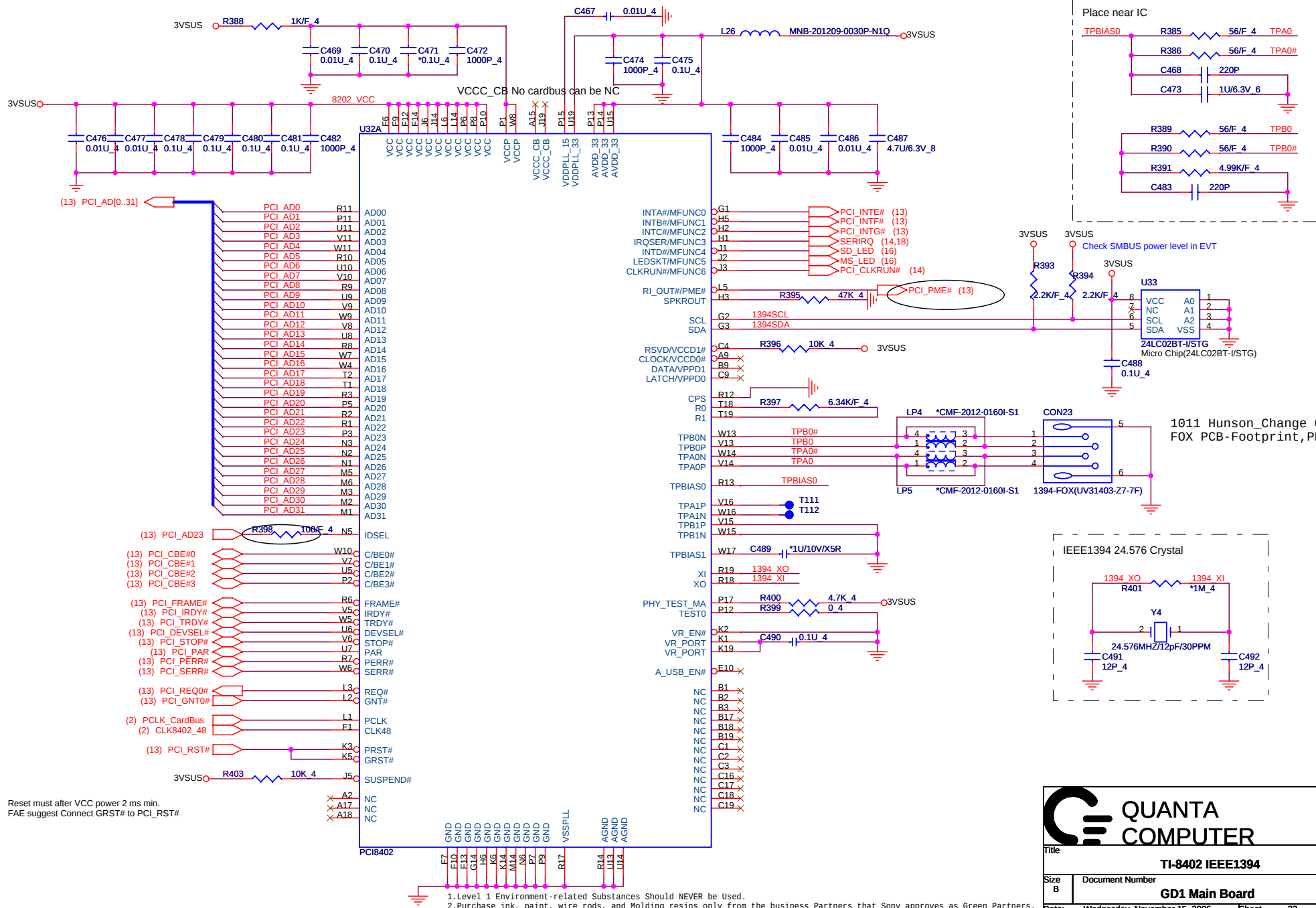
USB Camera

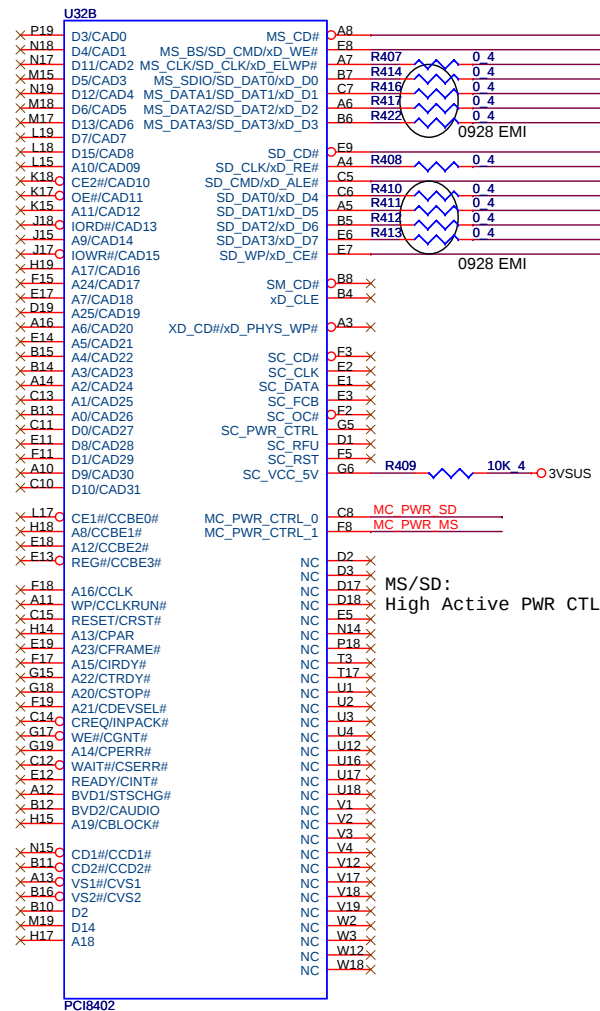


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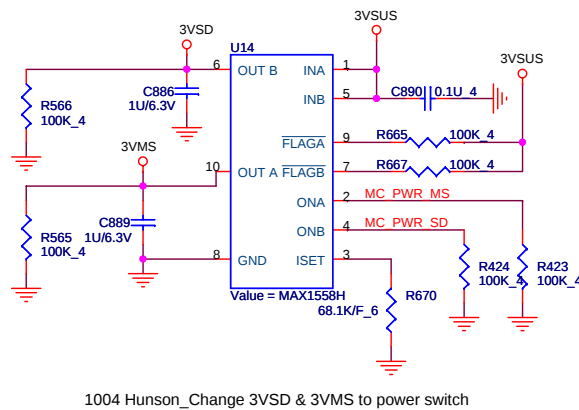


Title		K/B ,USB Device	
Size	Document Number	GD1 Main Board	
B		Date: Wednesday, November 15, 2006	Sheet 22 of 35
			Rev 1A

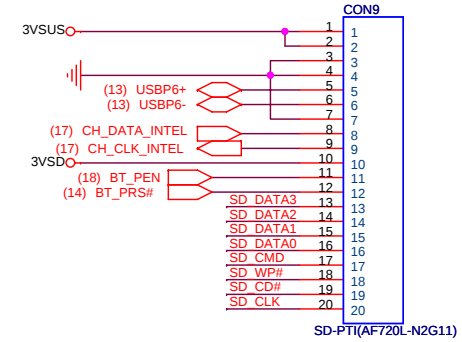




SD & MS Power Switch



SD CON(FPC)

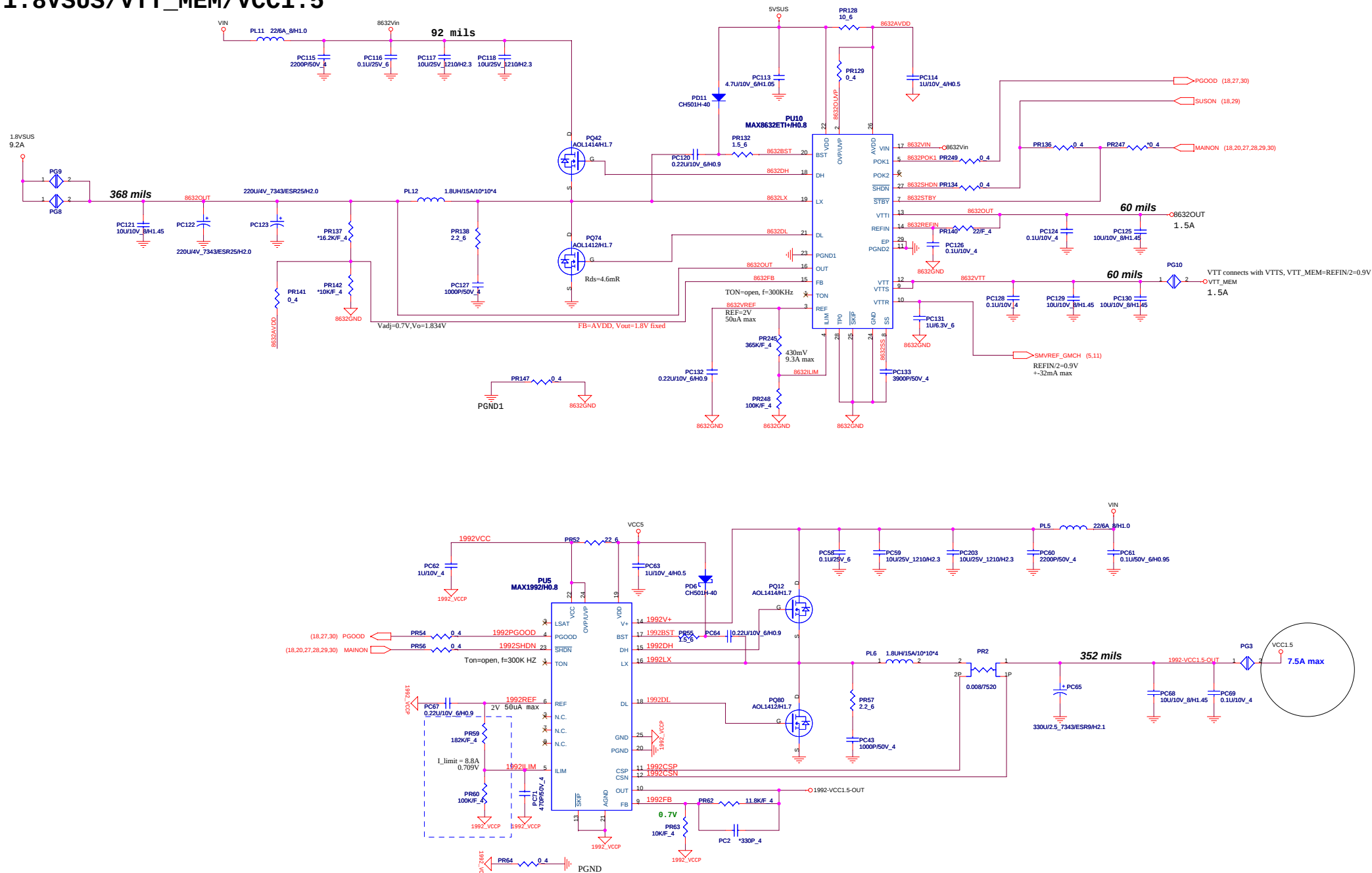


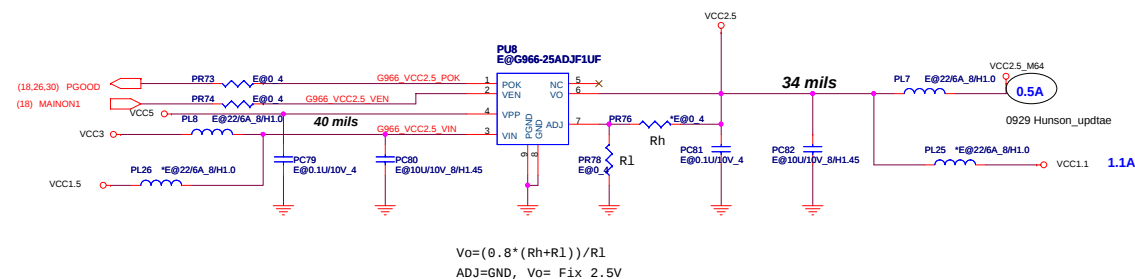
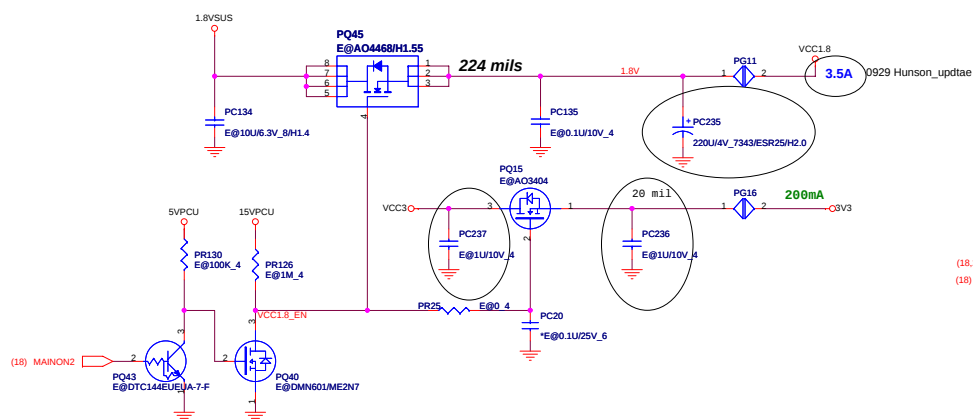
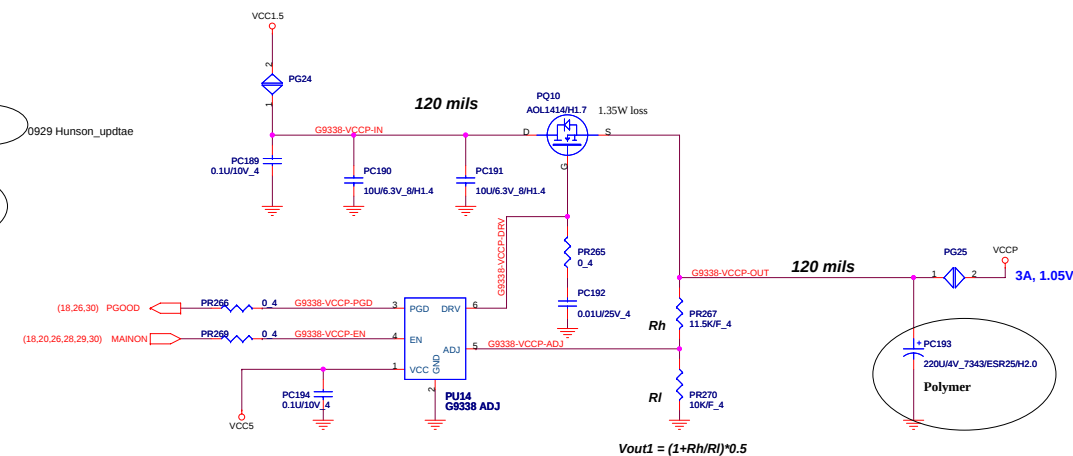
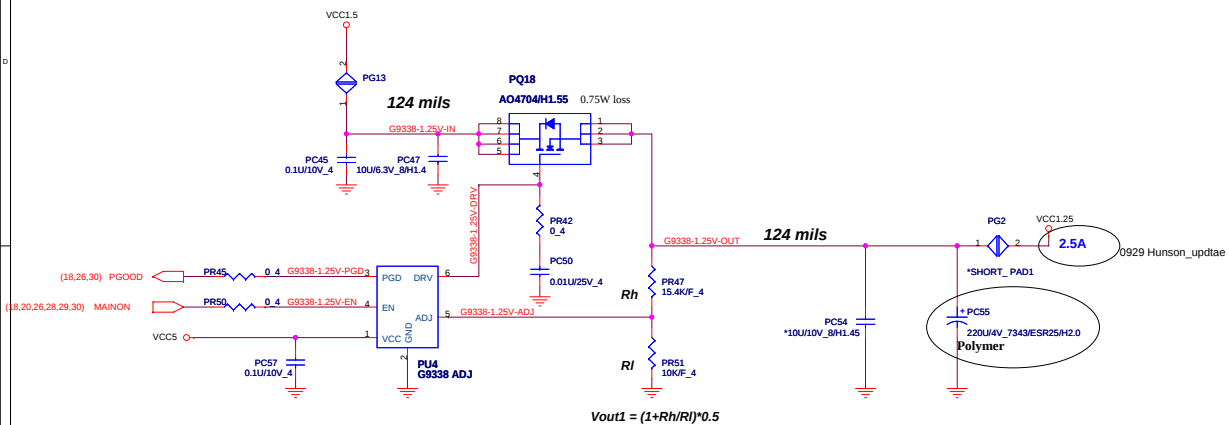
1031 Hunson_Change pin assignment
FAE comment:MS/SD_clock must have 3W space away DATA[0:3]



Title			TI-8402 MS & SD
Size	Document Number		Rev
B	GD1 Main Board		1A
Date:	Wednesday, November 15, 2006	Sheet	24 of 35

- 1.Level 1 Environment-related Substances Should NEVER be Used.
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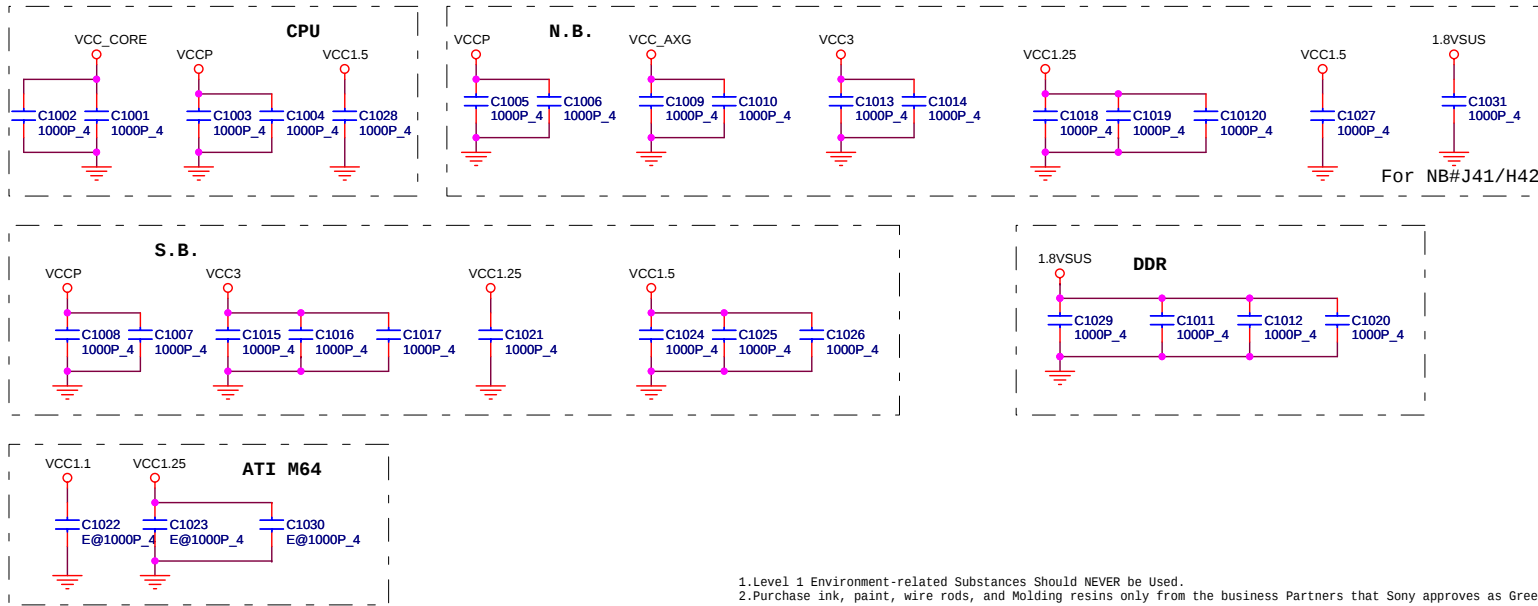
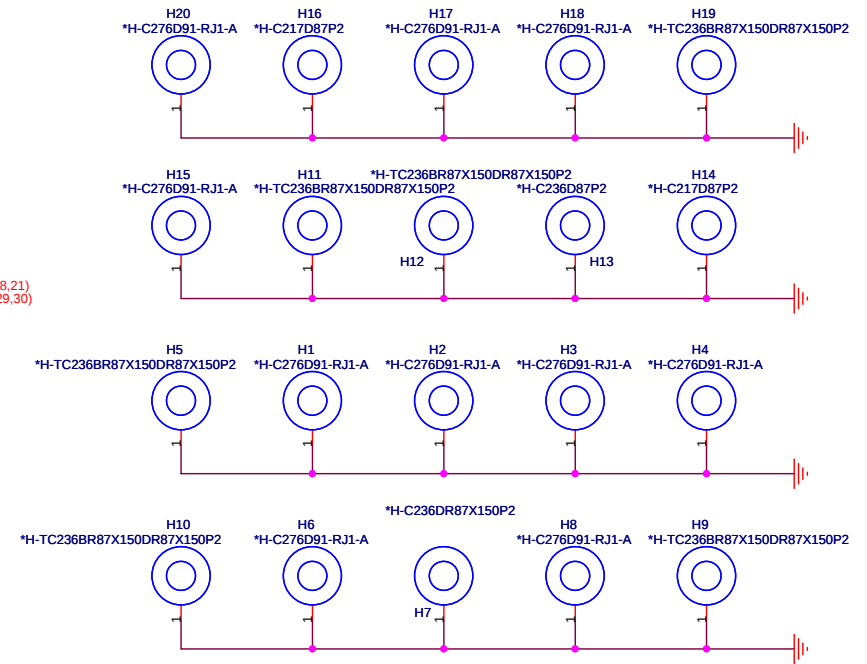
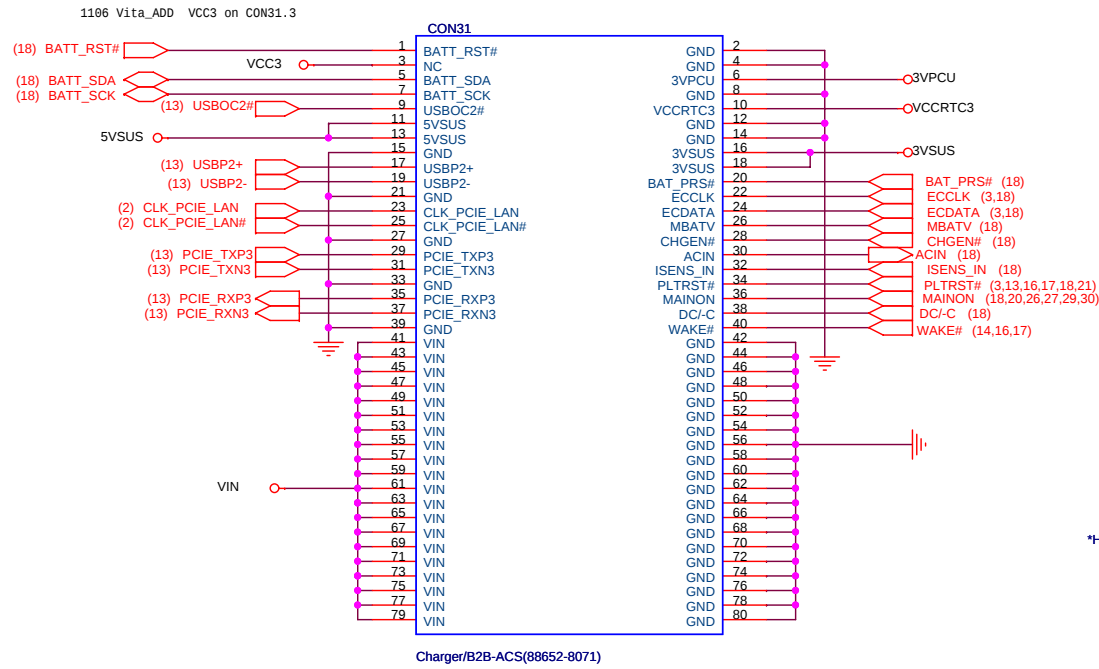




In progress

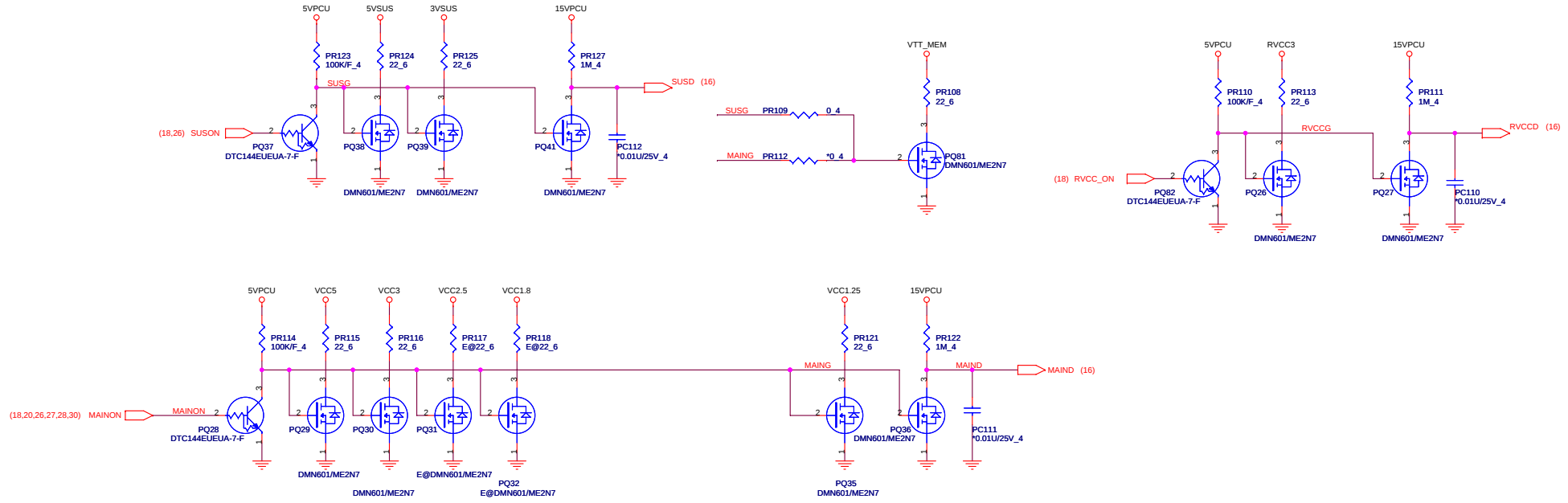
QUANTA COMPUTER			
VCCP & VCC1.5 & VCC1.25			
Size	Document Number	Rev	
	RD3 Main Board	1A	
Date:	Tuesday, November 14, 2006	Sheet	27 of 35

1027 Vita modify pin definition



- Level 1 Environment-related Substances Should NEVER be Used.
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Title			
Power Charger & LAN CON			
Size B	Document Number		Rev 1A
GD1 Main Board			
Date: Wednesday, November 15, 2006	Sheet	28	of 35



In progress

 QUANTA COMPUTER		
Title 3VPCU & 5VPCU		
Size Custom	Document Number RD3 Main Board	Rev 1A
Date: Wednesday, November 15, 2006 Sheet 29 of 35		

1. Level 1 Environment-related Substances Should NEVER be Used.
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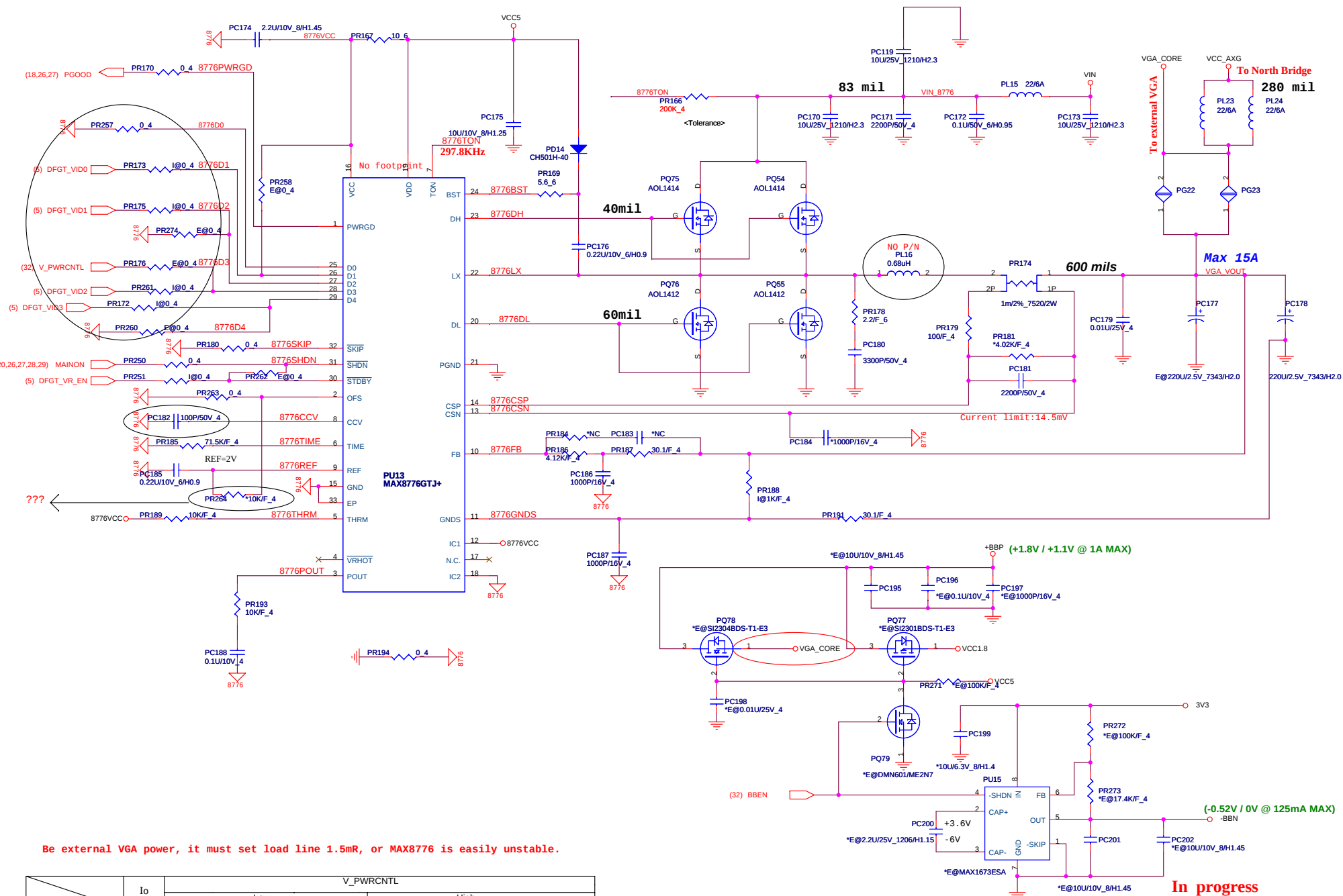


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COMPUTER

VGA CORE

RD3 Main Board

Date: Tuesday, November 14, 2006 Sheet 30 of 35

Rev
1/

	Io	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A	VID	

U3001A

PART 1 OF 7

GFX_TXP0 AK33
GFX_TXN0 AJ33
GFX_TXP1 AJ35
GFX_TXN1 AJ34
GFX_TXP2 AH35
GFX_TXN2 AH34
GFX_TXP3 AG35
GFX_TXN3 AG34
GFX_TXP4 AE33
GFX_TXN4 AE33
GFX_TXP5 AE35
GFX_TXN5 AE34
GFX_TXP6 AD35
GFX_TXN6 AD34
GFX_TXP7 AC35
GFX_TXN7 AC34
GFX_TXP8 AB33
GFX_TXN8 AB33
GFX_TXP9 AA35
GFX_TXN9 AA34
GFX_TXP10 Y35
GFX_TXN10 Y34
GFX_TXP11 W35
GFX_TXN11 W34
GFX_TXP12 V33
GFX_TXN12 U33
GFX_TXP13 U35
GFX_TXN13 U34
GFX_TXP14 T35
GFX_TXN14 T34
GFX_TXP15 R35
GFX_TXN15 R34

PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N

PCI EXPRESS INTERFACE

PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N

Calibration

PCIE_CALRN
PCIE_CALRP
PCIE_CALI

Clock

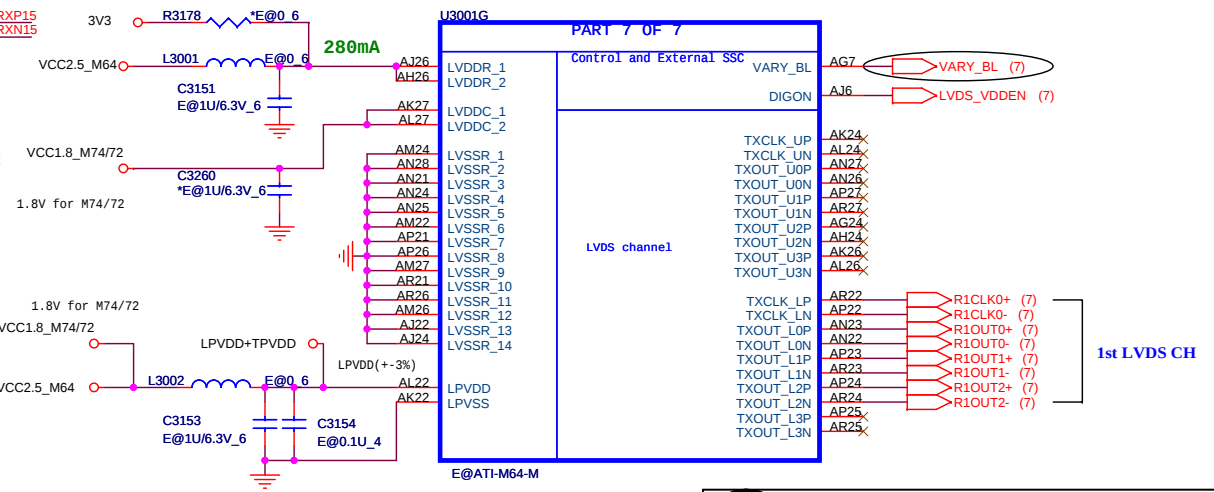
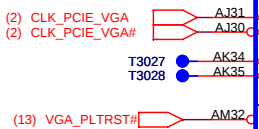
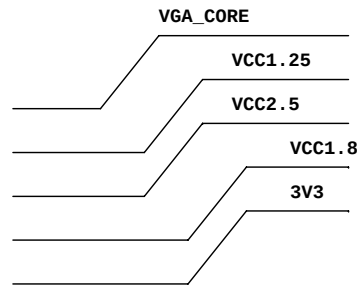
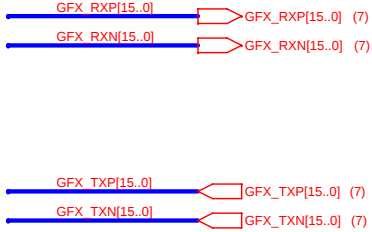
PCIE_REFCLKP
PCIE_REFCLKN
RSVD_1
RSVD_2

PERSTB

E@ATI-M64-M

AG31 C GFX_RXP0 C3000
AG30 C GFX_RXN0 C3001
AF31 C GFX_RXP1 C3002
AF30 C GFX_RXN1 C3003
AE28 C GFX_RXP2 C3004
AE27 C GFX_RXN2 C3005
AD31 C GFX_RXP3 C3006
AD30 C GFX_RXN3 C3007
AD28 C GFX_RXP4 C3008
AD27 C GFX_RXN4 C3009
AB31 C GFX_RXP5 C3010
AB30 C GFX_RXN5 C3011
AB28 C GFX_RXP6 C3012
AB27 C GFX_RXN6 C3013
AA31 C GFX_RXP7 C3014
AA30 C GFX_RXN7 C3015
AA28 C GFX_RXP8 C3016
AA27 C GFX_RXN8 C3017
W31 C GFX_RXP9 C3018
W30 C GFX_RXN9 C3019
W28 C GFX_RXP10 C3020
W27 C GFX_RXN10 C3021
V31 C GFX_RXP11 C3022
V30 C GFX_RXN11 C3023
V28 C GFX_RXP12 C3024
V27 C GFX_RXN12 C3025
U31 C GFX_RXP13 C3026
U30 C GFX_RXN13 C3027
U28 C GFX_RXP14 C3028
U27 C GFX_RXN14 C3029
R31 C GFX_RXP15 C3030
R30 C GFX_RXN15 C3031

E@0.1U 4 GFX_RXP0
E@0.1U 4 GFX_RXN0
E@0.1U 4 GFX_RXP1
E@0.1U 4 GFX_RXN1
E@0.1U 4 GFX_RXP2
E@0.1U 4 GFX_RXN2
E@0.1U 4 GFX_RXP3
E@0.1U 4 GFX_RXN3
E@0.1U 4 GFX_RXP4
E@0.1U 4 GFX_RXN4
E@0.1U 4 GFX_RXP5
E@0.1U 4 GFX_RXN5
E@0.1U 4 GFX_RXP6
E@0.1U 4 GFX_RXN6
E@0.1U 4 GFX_RXP7
E@0.1U 4 GFX_RXN7
E@0.1U 4 GFX_RXP8
E@0.1U 4 GFX_RXN8
E@0.1U 4 GFX_RXP9
E@0.1U 4 GFX_RXN9
E@0.1U 4 GFX_RXP10
E@0.1U 4 GFX_RXN10
E@0.1U 4 GFX_RXP11
E@0.1U 4 GFX_RXN11
E@0.1U 4 GFX_RXP12
E@0.1U 4 GFX_RXN12
E@0.1U 4 GFX_RXP13
E@0.1U 4 GFX_RXN13
E@0.1U 4 GFX_RXP14
E@0.1U 4 GFX_RXN14
E@0.1U 4 GFX_RXP15
E@0.1U 4 GFX_RXN15



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Title

ATI M64M PCIE

Size B

Document Number

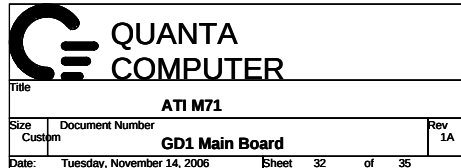
Rev 1A

GD1 Main Board

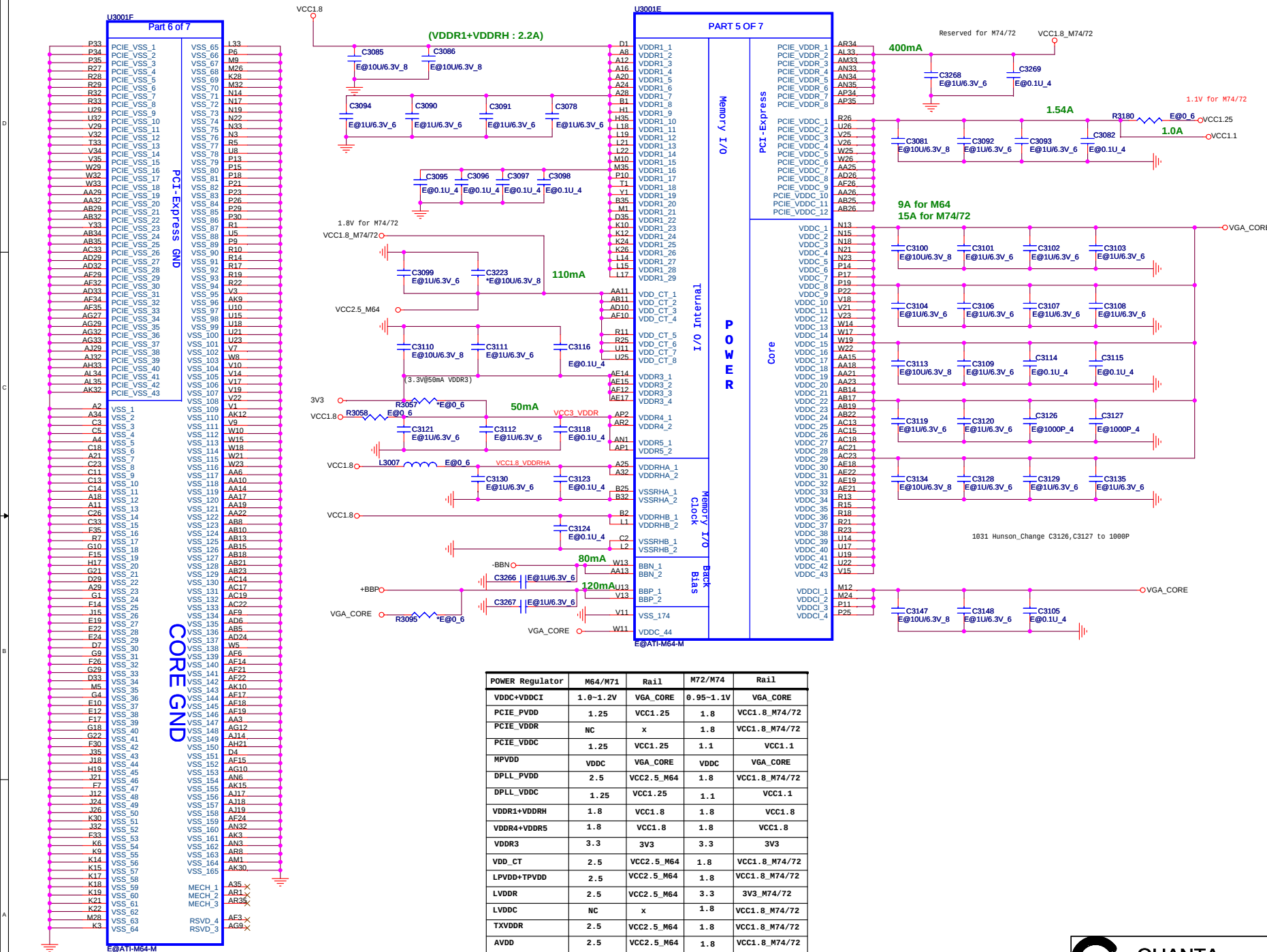
Date: Tuesday, November 14, 2006

Sheet 31 of 35

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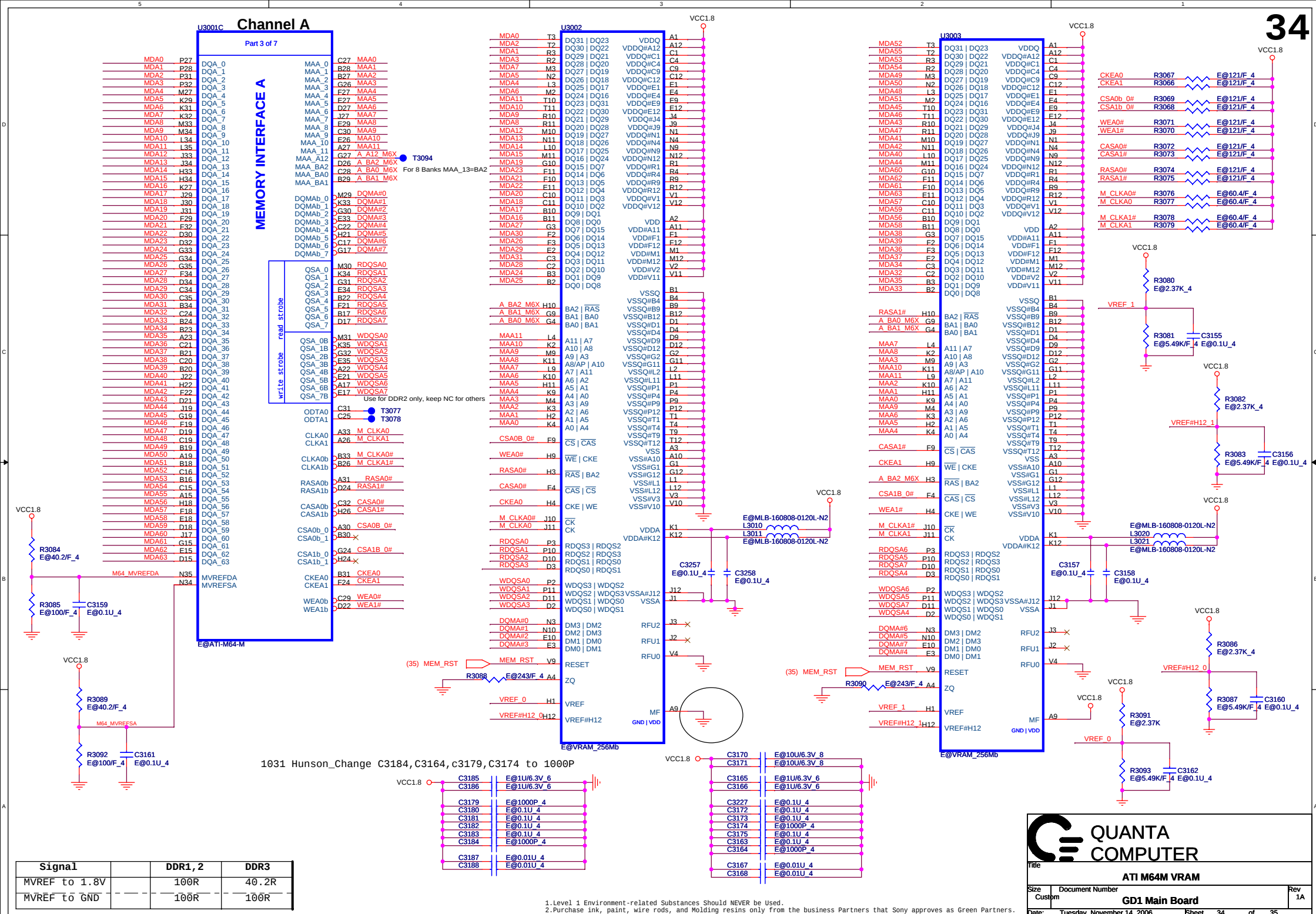


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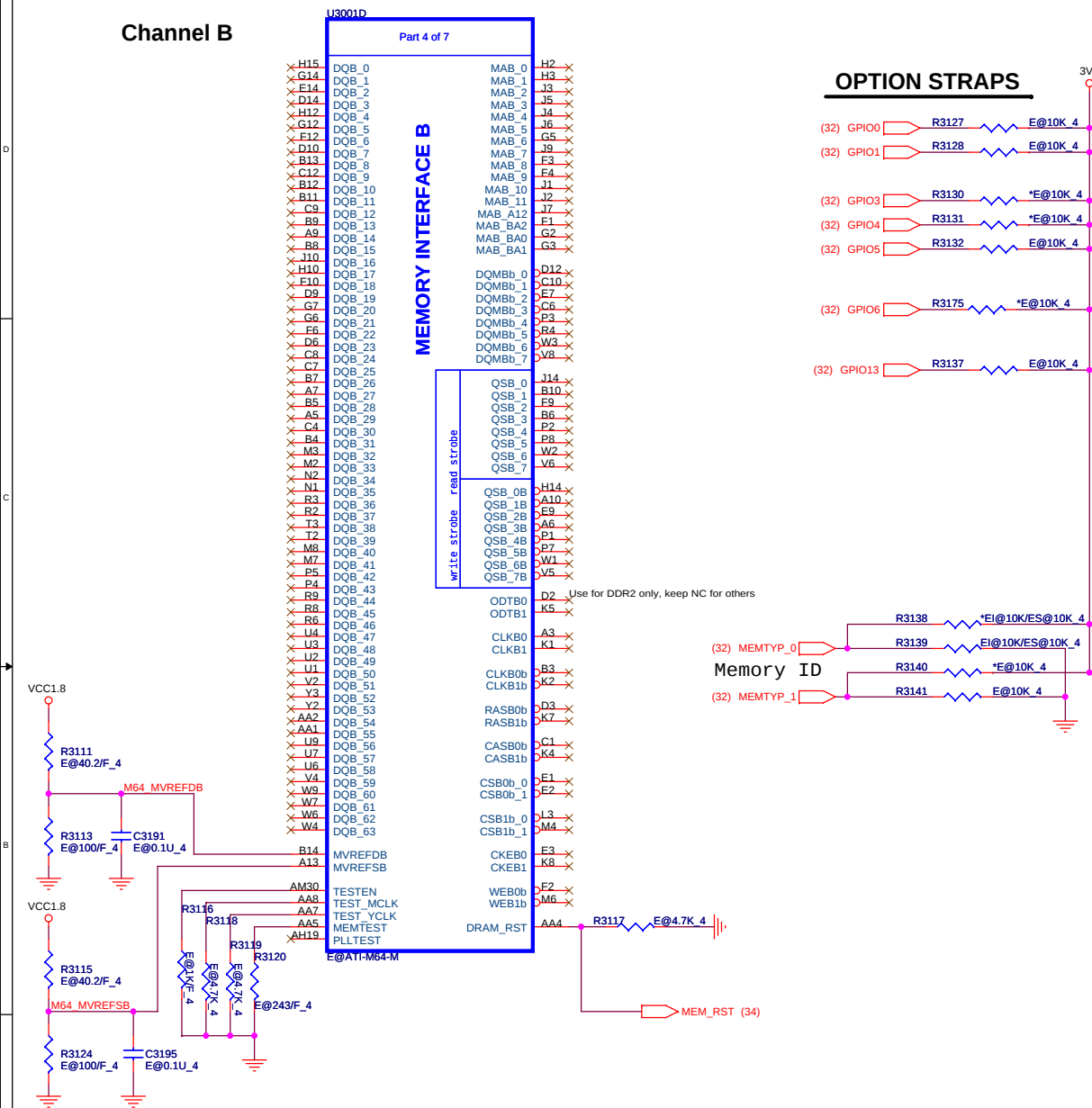


POWER Regulator	M64/M71	Rail	M72/M74	Rail
VDDC+VDDCI	1.0-1.2V	VGA_CORE	0.95-1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
LVDDC	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

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Channel B



M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM 0 Output from ROM)	

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3124	R3125	R3122	R3123	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - RESERVED
1	1	10K	NC	10K	NC	11 - RESERVED



QUANTA
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Title			ATI M64-M STRAP		
Size	Document Number				Rev
Custom	GD1 Main Board				1A
Date:	Tuesday, November 14, 2006	Sheet	35	of	35