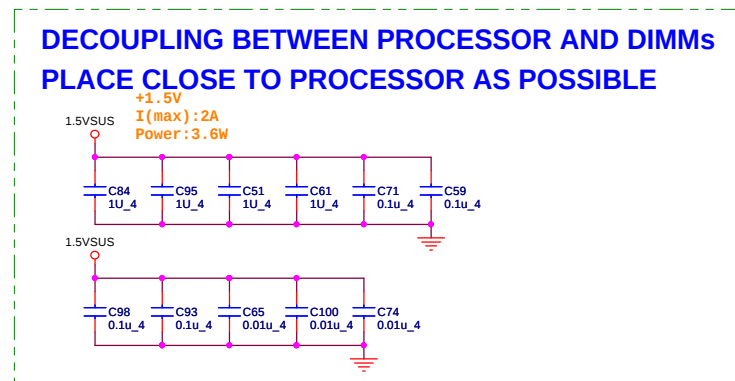
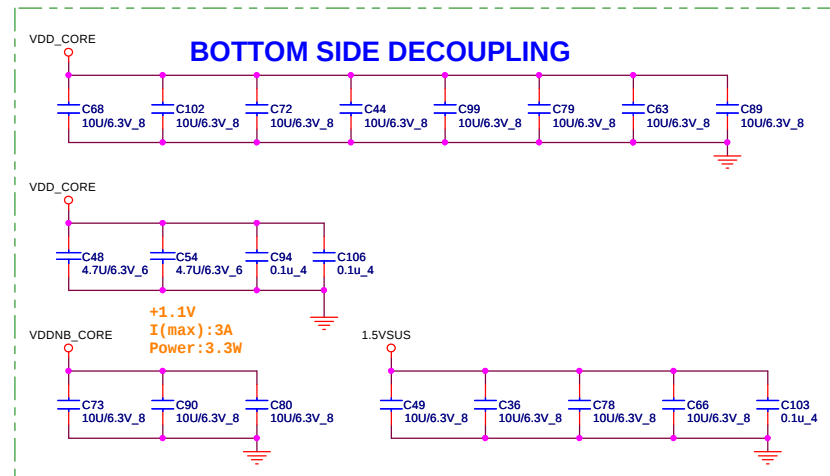
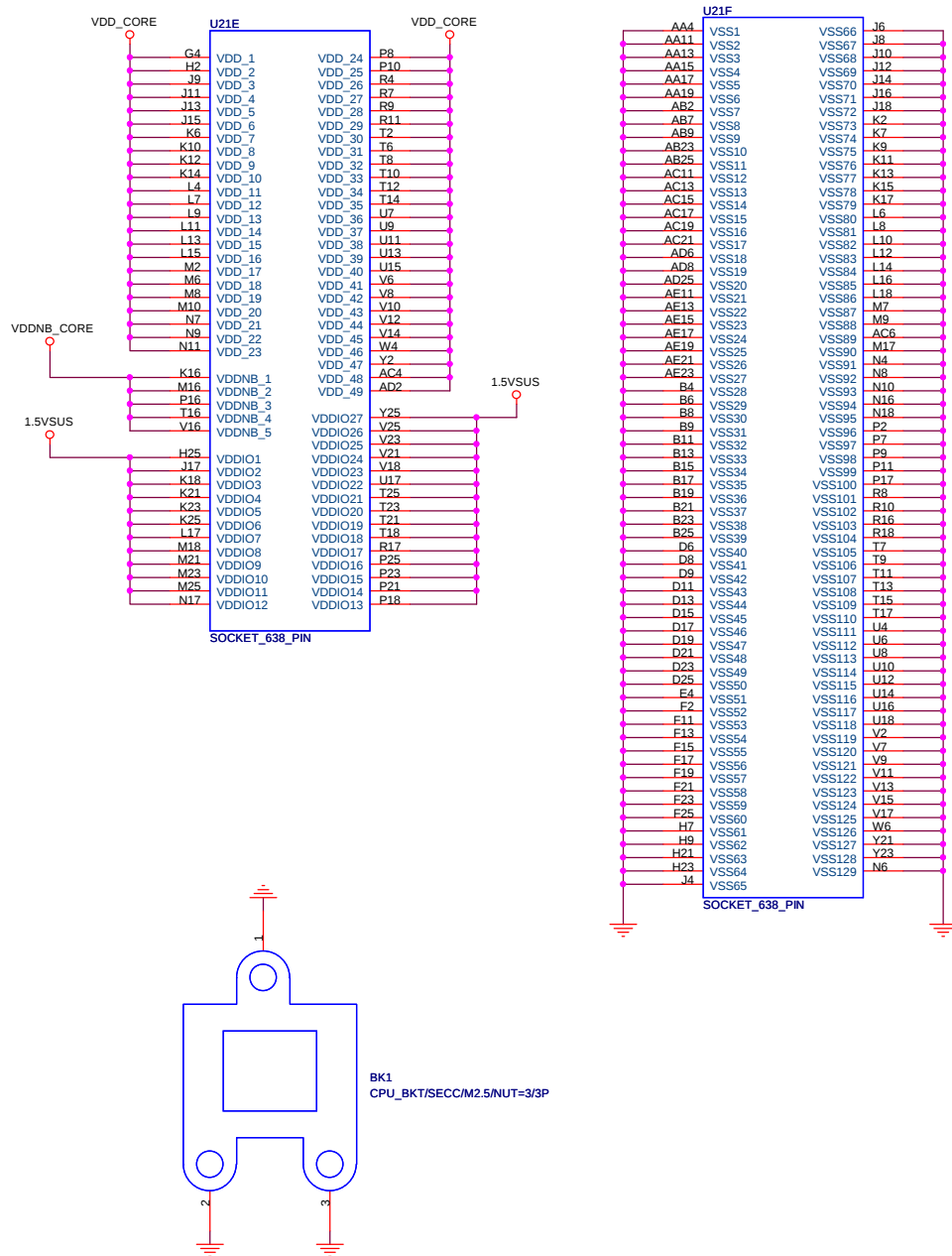




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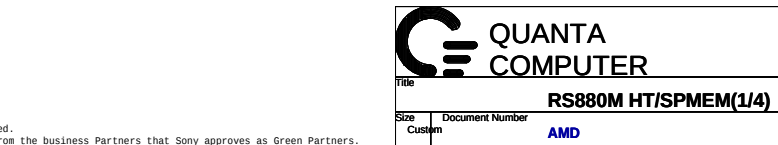
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners

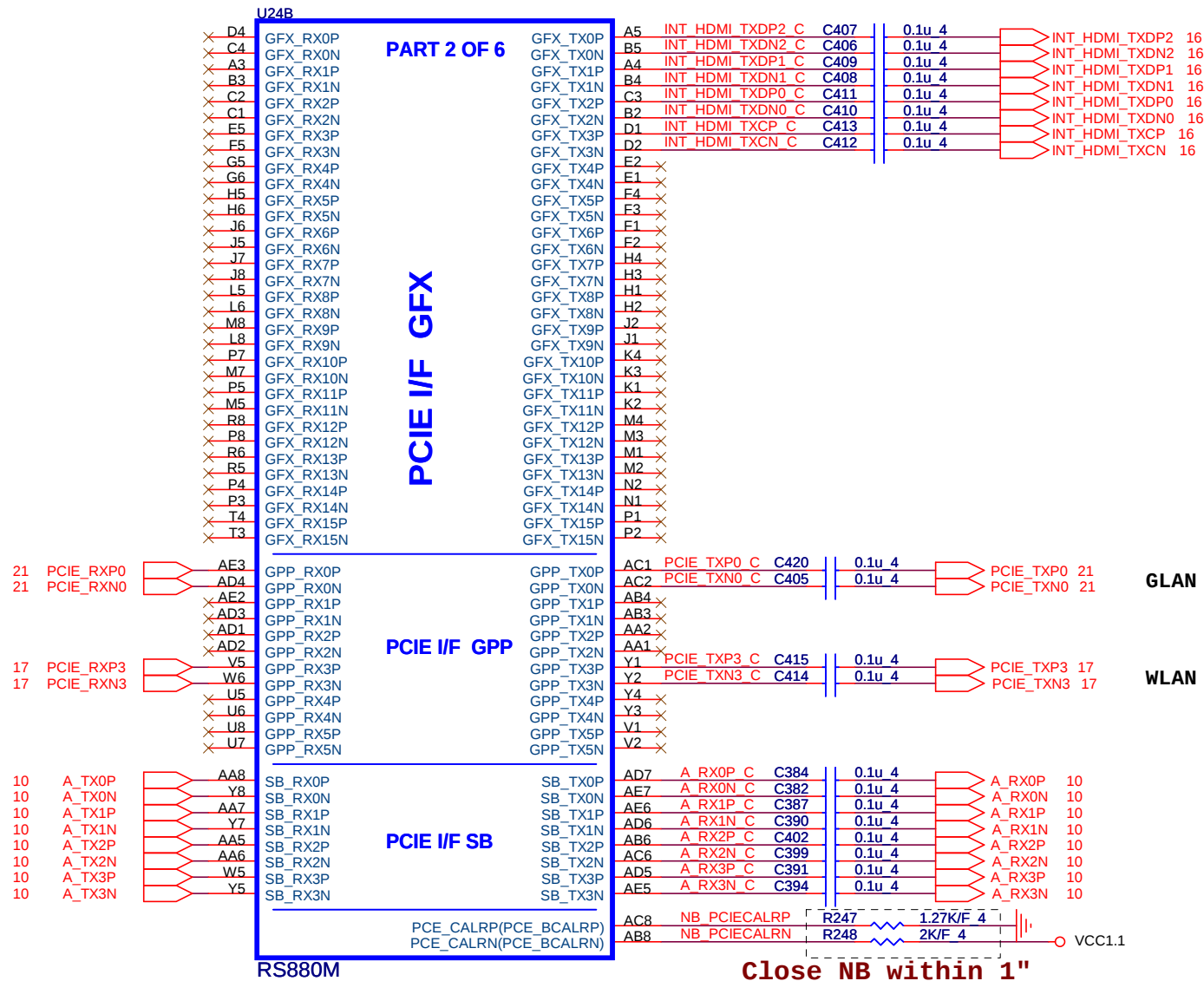
Socket Type	QCI P/N
Normal	DG0^8000018
90 degree	DG0^8000023

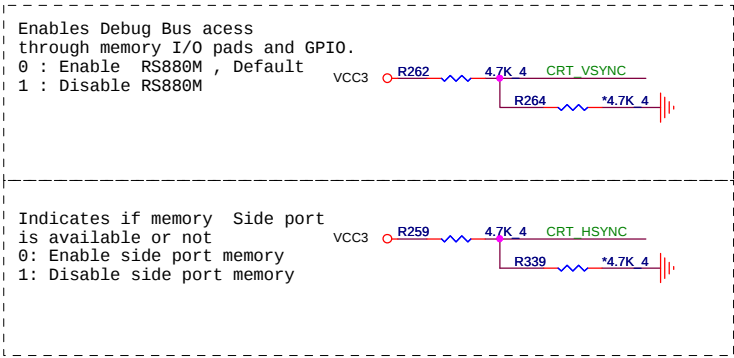




Resins Should NEVER be Used. Molding resins only from the business Partners that Sony approves as Green Partners.

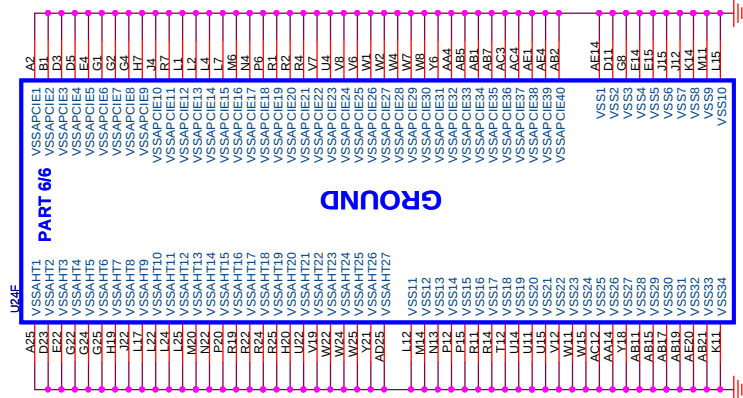




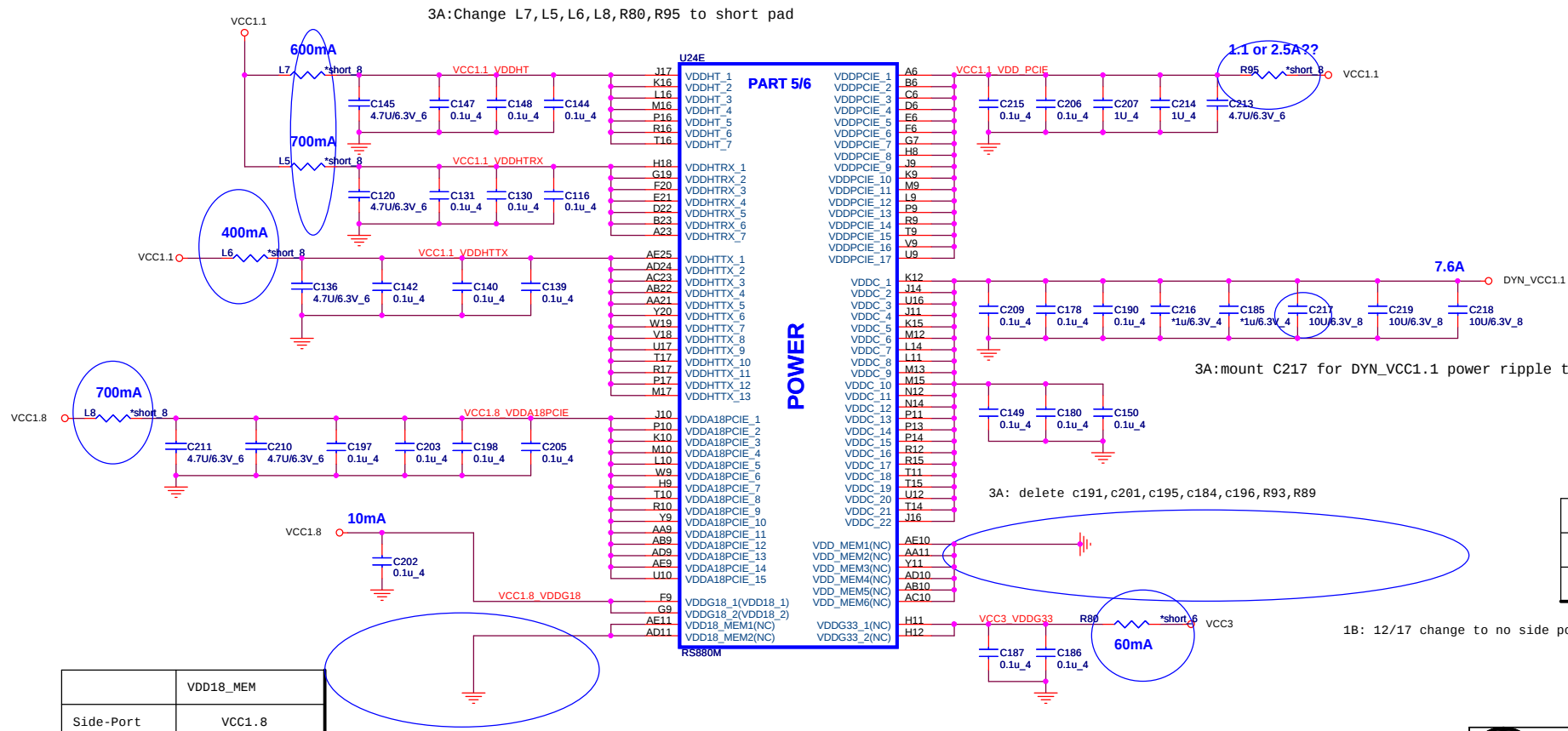


1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 QUANTA COMPUTER			
Title			
RS880M SYSTEM(3/4)			
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GROUND



PART 5/6

POWER

	VDD18_MEM
Side-Port	VCC1.8
No Side-Port	GND

	VDD_MEM
Side-Port	VCC1.5
No Side-Port	GND



QUANTA
COMPUTER

Title

RS880M POWER(4/4)

Size

Custom

Document Number

AMD

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Rev

3A

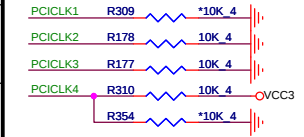
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Strap Table

1221,AMD suggest R309 unimpunt

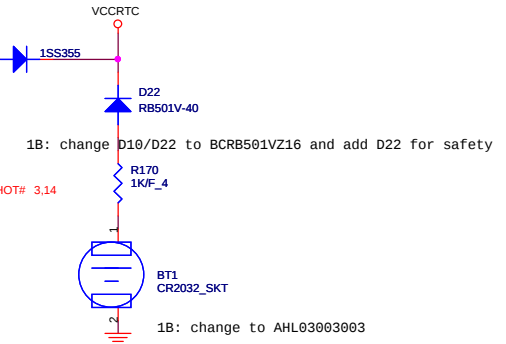
PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4
ALLOW PCIe Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE
FORCE PCIe Gen1	Watchdog Timer Disable	IGNORE DEBUG STRAPS	Fusion CLOCK MODE

PCI Strap

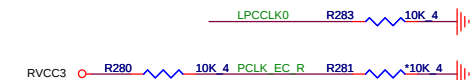


1B: delete no need PU R128/R161/R272/R155, add R354 for optional

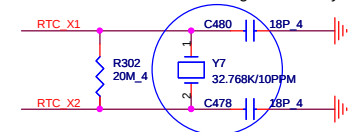
RTC



LPCLK0	LPCLK1
H=Enable embedded EC	H=Enable Internal CLK Gen.
L=Disable embedded EC	L=Disable Internal CLK Gen.



3A:1/22 change Y7 P/N(BG332768909) and C478=18PF for timing accuracy



QUANTA COMPUTER		
Title SB8X0 PCI/CLK/LPC(1/4)		
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SB820 Part 1 of 5

PCICLK0
PCICLK1/GPO36
PCICLK2/GPO37
PCICLK3/GPO38
PCICLK4/14M_OSC/GPO39

PCIRST# R

AD0/GPIO0
AD1/GPIO1
AD2/GPIO2
AD3/GPIO3
AD4/GPIO4
AD5/GPIO5
AD6/GPIO6
AD7/GPIO7
AD8/GPIO8
AD9/GPIO9
AD10/GPIO10
AD11/GPIO11
AD12/GPIO12
AD13/GPIO13
AD14/GPIO14
AD15/GPIO15
AD16/GPIO16
AD17/GPIO17
AD18/GPIO18
AD19/GPIO19
AD20/GPIO20
AD21/GPIO21
AD22/GPIO22
AD23/GPIO23
AD24/GPIO24
AD25/GPIO25
AD26/GPIO26
AD27/GPIO27
AD28/GPIO28
AD29/GPIO29
AD30/GPIO30
AD31/GPIO31

CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#/GPIO40
REQ2#/CLK_REQ8#/GPIO41
REQ3#/CLK_REQ5#/GPIO42
GNT0#
GNT1#/GPIO44
GNT2#/GPIO45
GNT3#/CLK_REQ7#/GPIO46
CLKRUN#
LOCK#

INTE#/GPIO32
INTF#/GPIO33
INTG#/GPIO34
INTH#/GPIO35

LPCLK0
LPCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/CLK_REQ6#/GPIO49
SERIRQ 22

ALLOW_LDTSTP/DMA_ACTIVE#
PCLK0#
LDT_PG
LDT_STP#
LDT_RST#

32K_X1
32K_X2
RTC_X1
RTC_X2
D2
B2
B1
VDDBT_RTC_G

G2
SHORT_PAD1
C333 1U_4
C311 0.1u_4

VCC_RTC 2.5V-3.6V

INTRUDER_ALERT#
VDDBT_RTC_G

INTRUDER_ALERT#

INTRUDER_ALERT#

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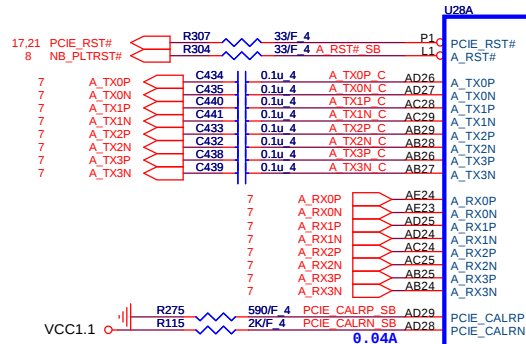
INTRUDER_ALERT#

INTRUDER_ALERT#

INTRUDER_ALERT#

INTRUDER_ALERT#

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



SB8xx only supports 2 GPP port 2 & 3 is not supported.

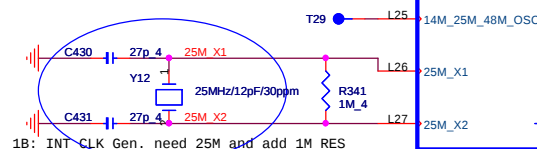
1B: modify INT clock for display

3A: delete RP5,RP29,RP32,RP15,RP35,RP30

CLK_PCIE_EXP ;CLK_PCIE_EXN remove 12/29

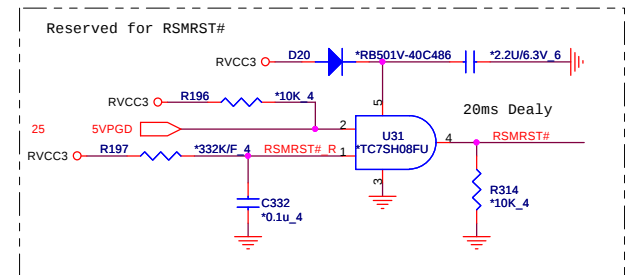
GPP4 - 5 used for NB PCIE

1B:change to test point



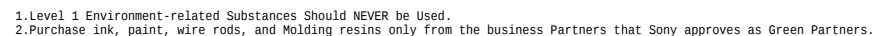
1B: INT-CLK Gen. need 25M and add 1M RES

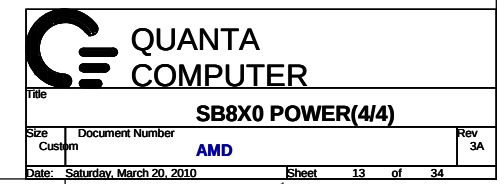
3A:1/22 change Y12 P/N: BG625000486 and C430=C431 27PF for timing accuracy



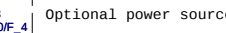
	GPI0200, GPI0199
PULL HIGH	H, H=Reserved H, L=SPI ROM
PULL LOW	L, H=LPC ROM(Default) L, L=FWH ROM

```
3A Remove Panel ID      3A :delete RP27,SW1,RP25
```



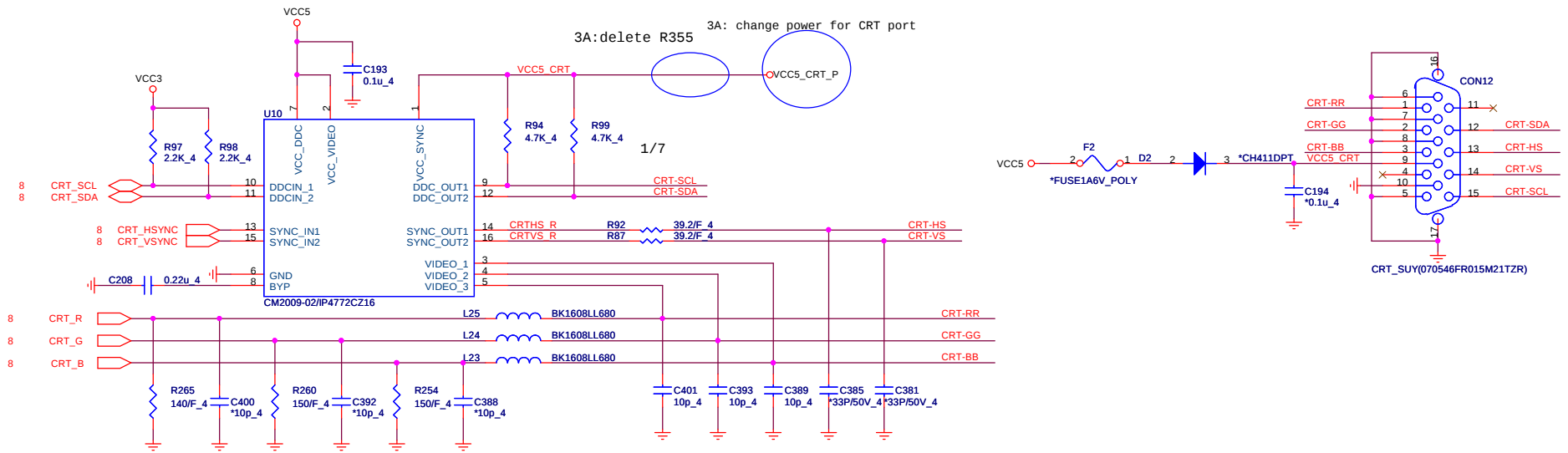


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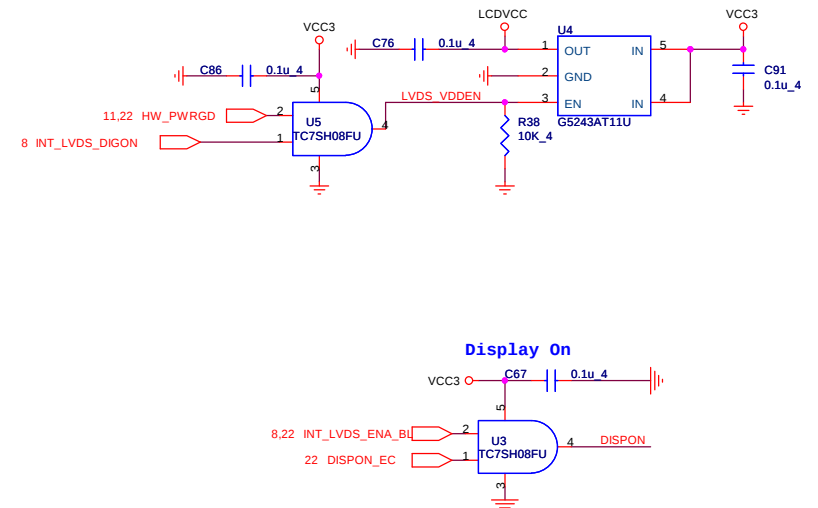
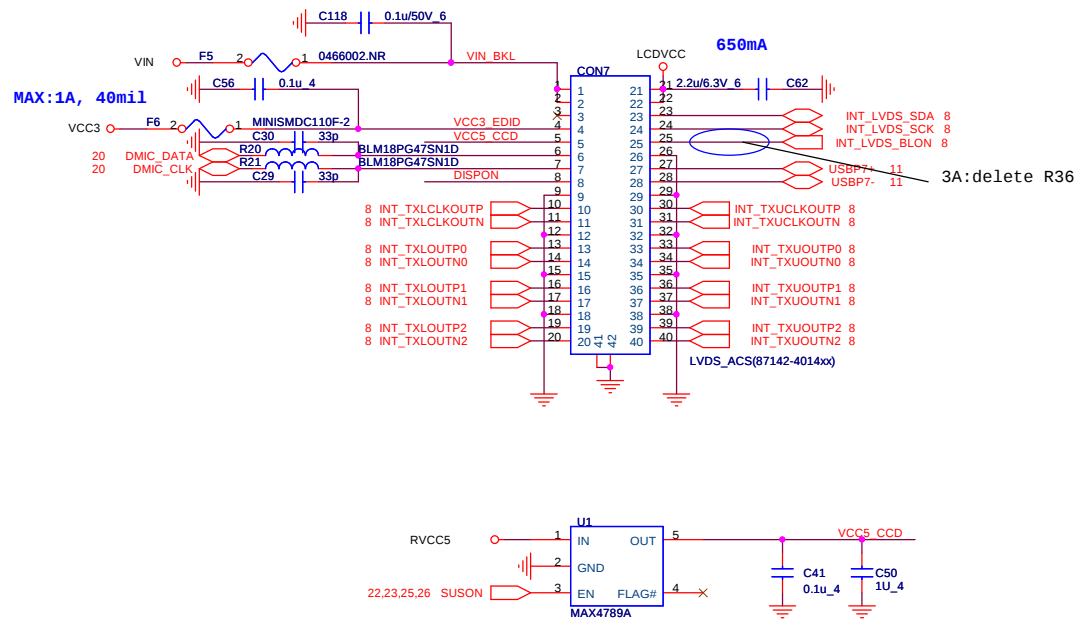


CRT

15

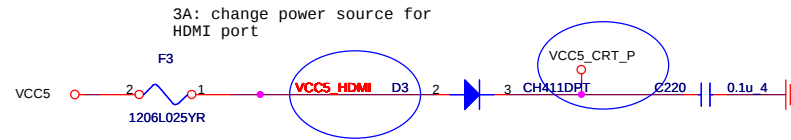


LVDS



Title			
CRT/LVDS			
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3A: change power source for CRT port



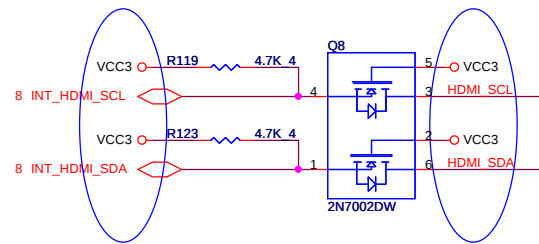
For EMI

INT_HDMI_TXDP0 R271 *100/F 4 INT_HDMI_TXDN0
 INT_HDMI_TXDP1 R269 *100/F 4 INT_HDMI_TXDN1
 INT_HDMI_TXDP2 R270 *100/F 4 INT_HDMI_TXDN2
 HDMI_TXCP R268 *100/F 4 HDMI_TXCN

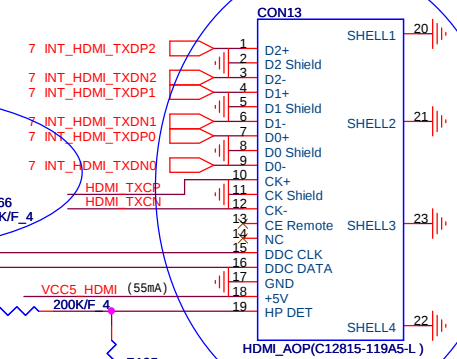
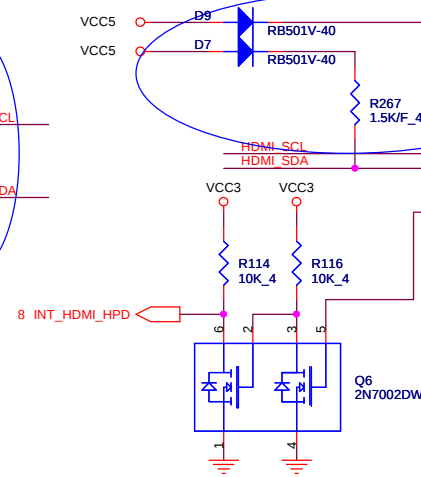
3A:delete RP38

7 INT_HDMI_TXCP
 7 INT_HDMI_TXCN

3A : VCC5 -> VCC3

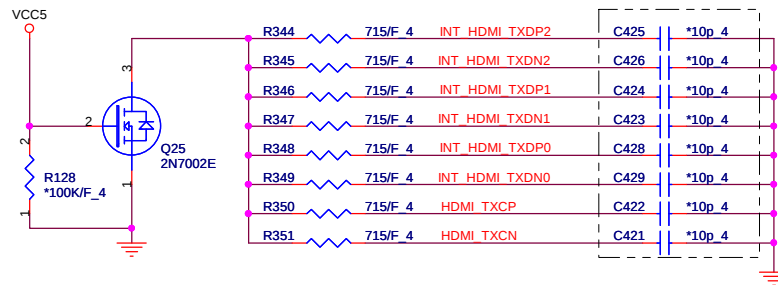


3A:Prevent incorrect voltage level



3A: Change CON13 footprint:
 from hdmi-c12806-11908-1-19p-v to Hdmi-c12825-11908-1-19p-v

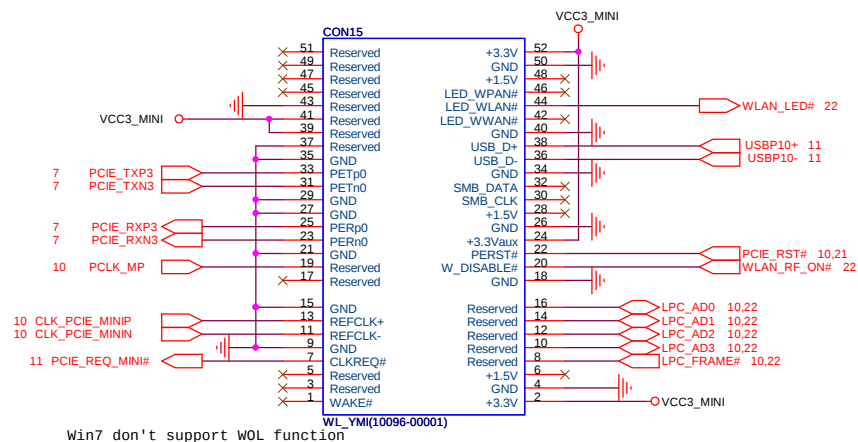
For ESD



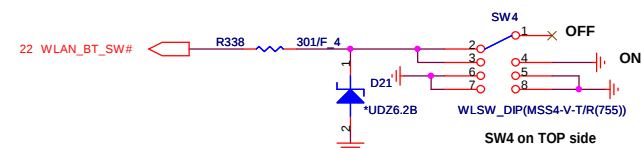
1.Level 1 Environment-related Substances Should NEVER be Used.
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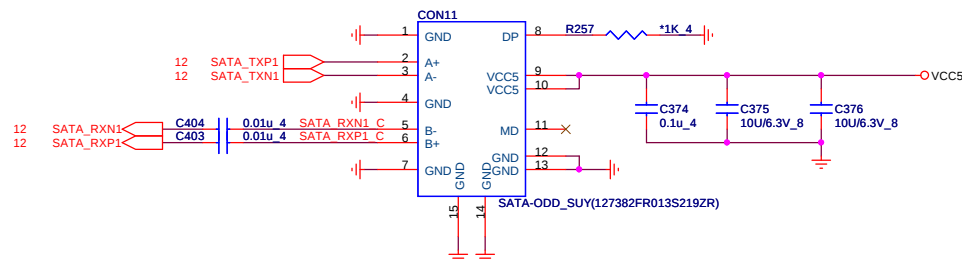
Title			HDMI
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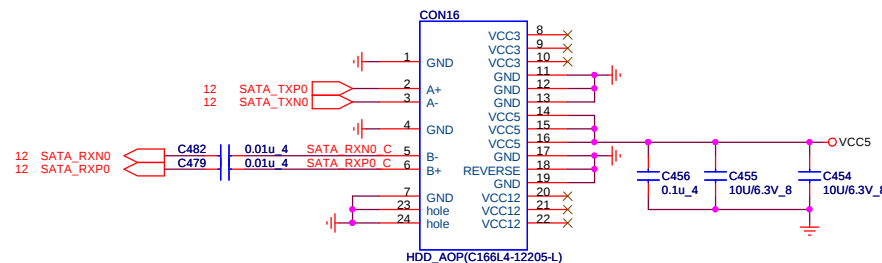
WLAN_BT_S/W



SATA ODD



SATA HDD



QUANTA

COMPUTER

Title			WLAN/HDD/ODD		
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D



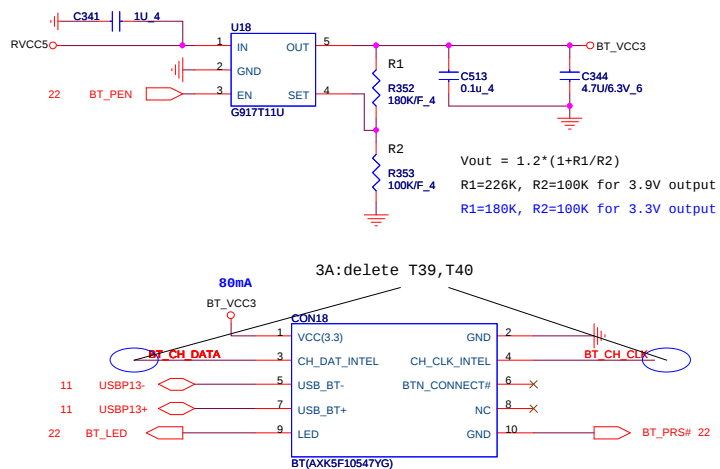
MR1

[illegible]

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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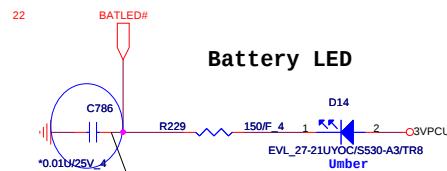
1

Bluetooth

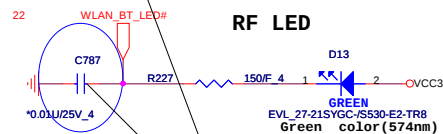


Two Color :
 everylight : 19-22UYOSYGC (BEAG0028ZA0_
 liteon : LTST-C195KGKFKT (BEAG0032ZA0_
 Amber:
 everylight : 19-21UYOC/S530-A6/TR8 (BEAB0015Z06)
 liteon : LTST-C190KFKT (BEAB0006Z07)
 Green :
 everylight : 19-21SYGC/S530-E2/TR8 (BEYG0053ZA2)
 liteon : LTST-C190KGKT (BEGR0000Z07)
 Yellow:
 everylight : 19-21UYC/S530-A2/TR8 (BEYL0016Z08)
 liteon : LTST-C190KSKT (BEYL0024Z01)

Battery LED

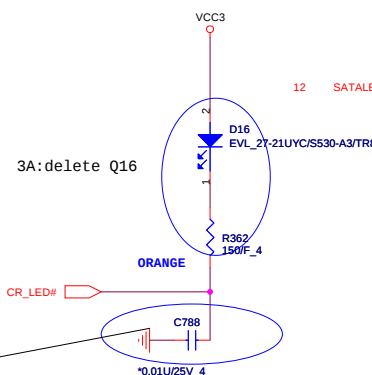


RF LED

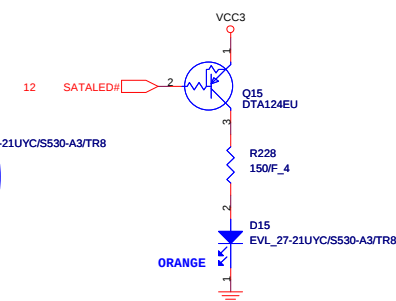


3A : Reverse C786, C787, C788 FP for ESD

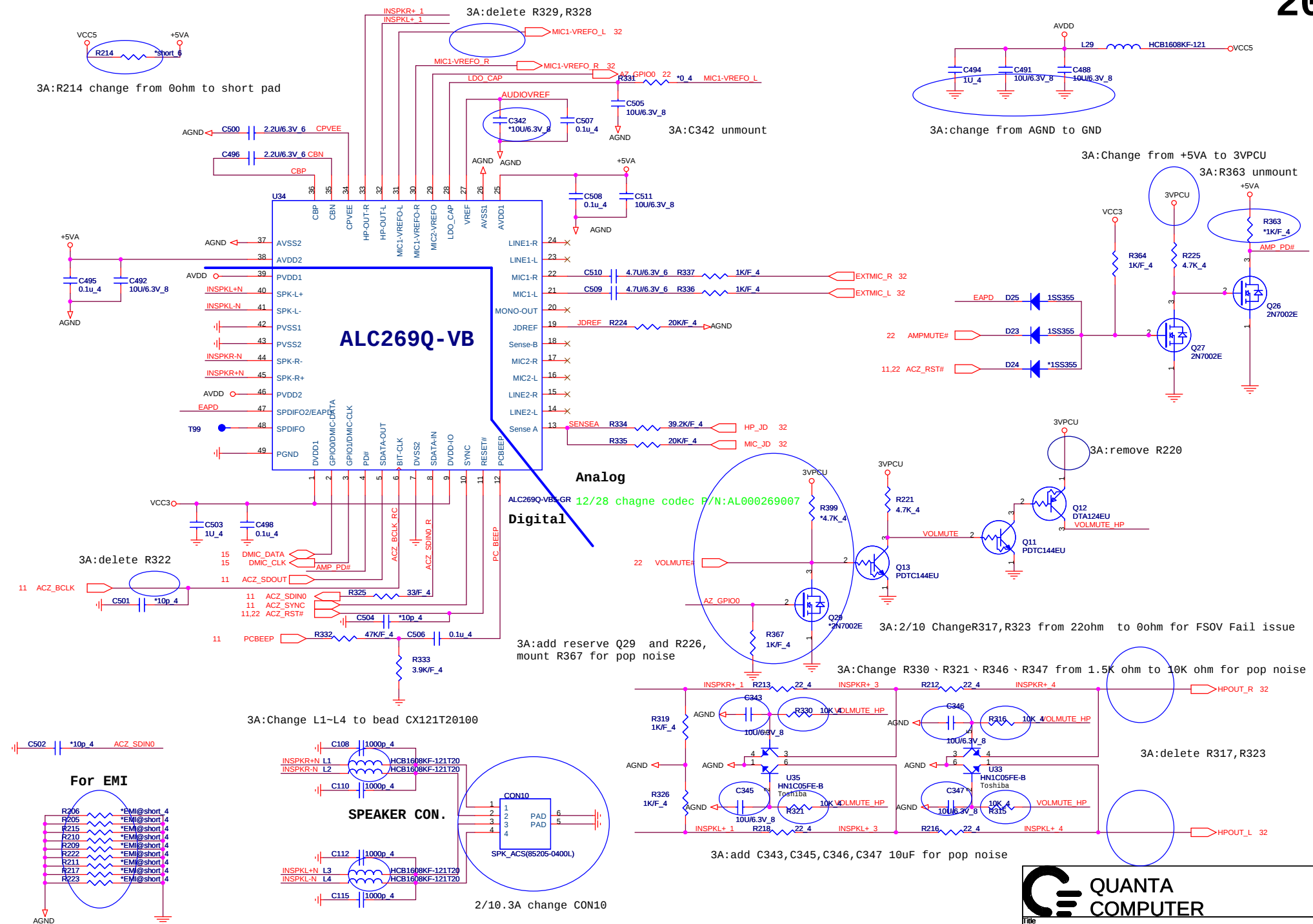
CR LED

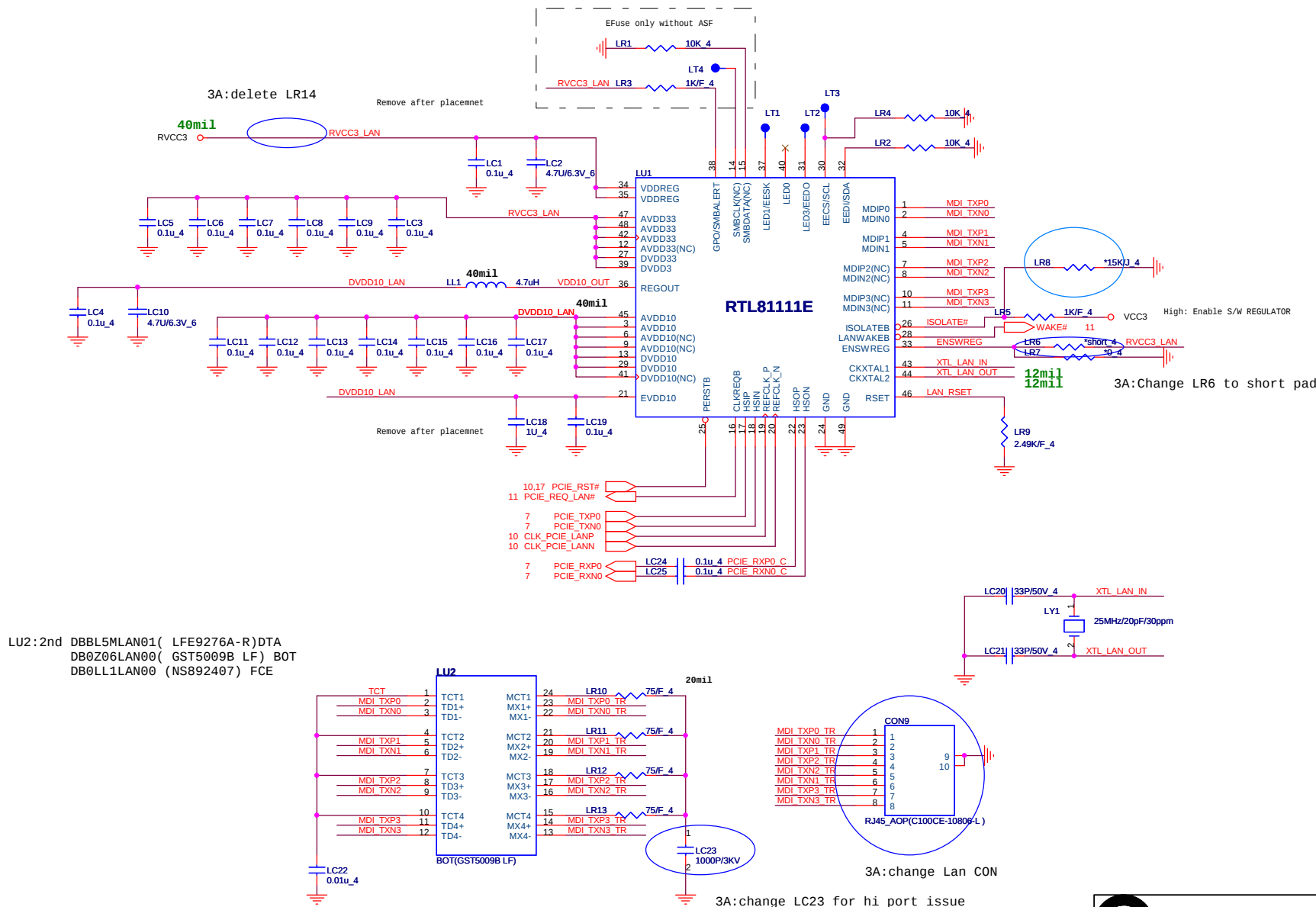


HDD LED



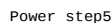
Title			
Express Card/LED/BT			
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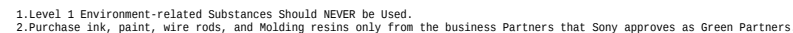
Title			LAN RTL8111E
Size	Document Number	Rev	
Custom	AMD	3A	
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DOCK_RST# : BADDR6
T?: BADDR1

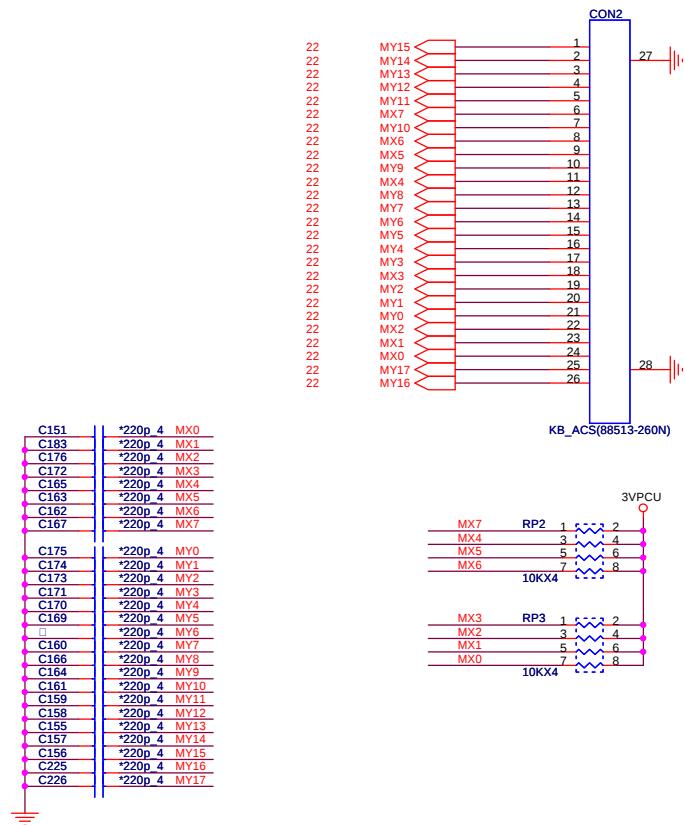


Title **WPC8775L & FLASH**

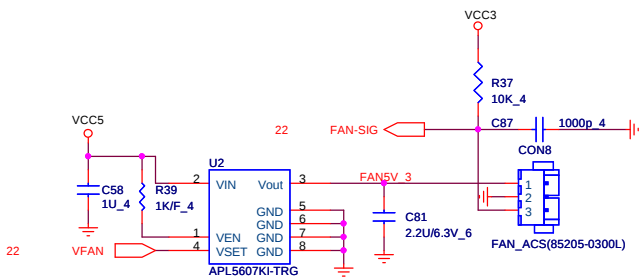
Size Custom	Document Number AMD	Rev 3A
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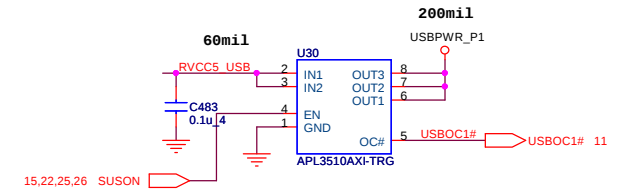
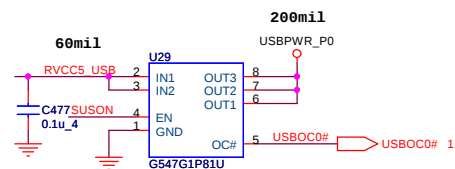
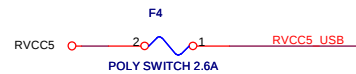
KEYBOARD



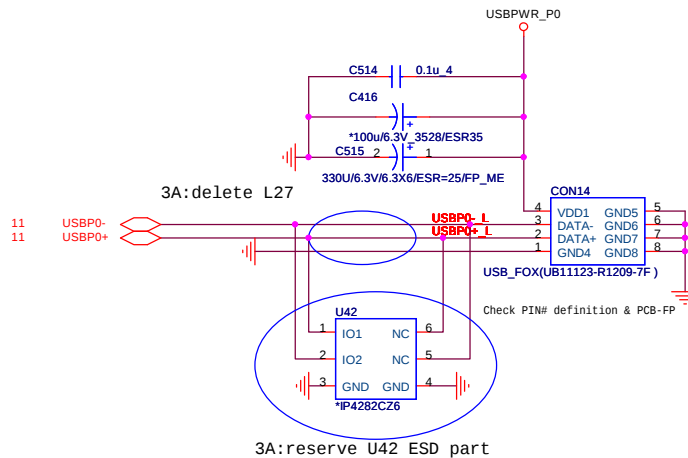
FAN



USB Port

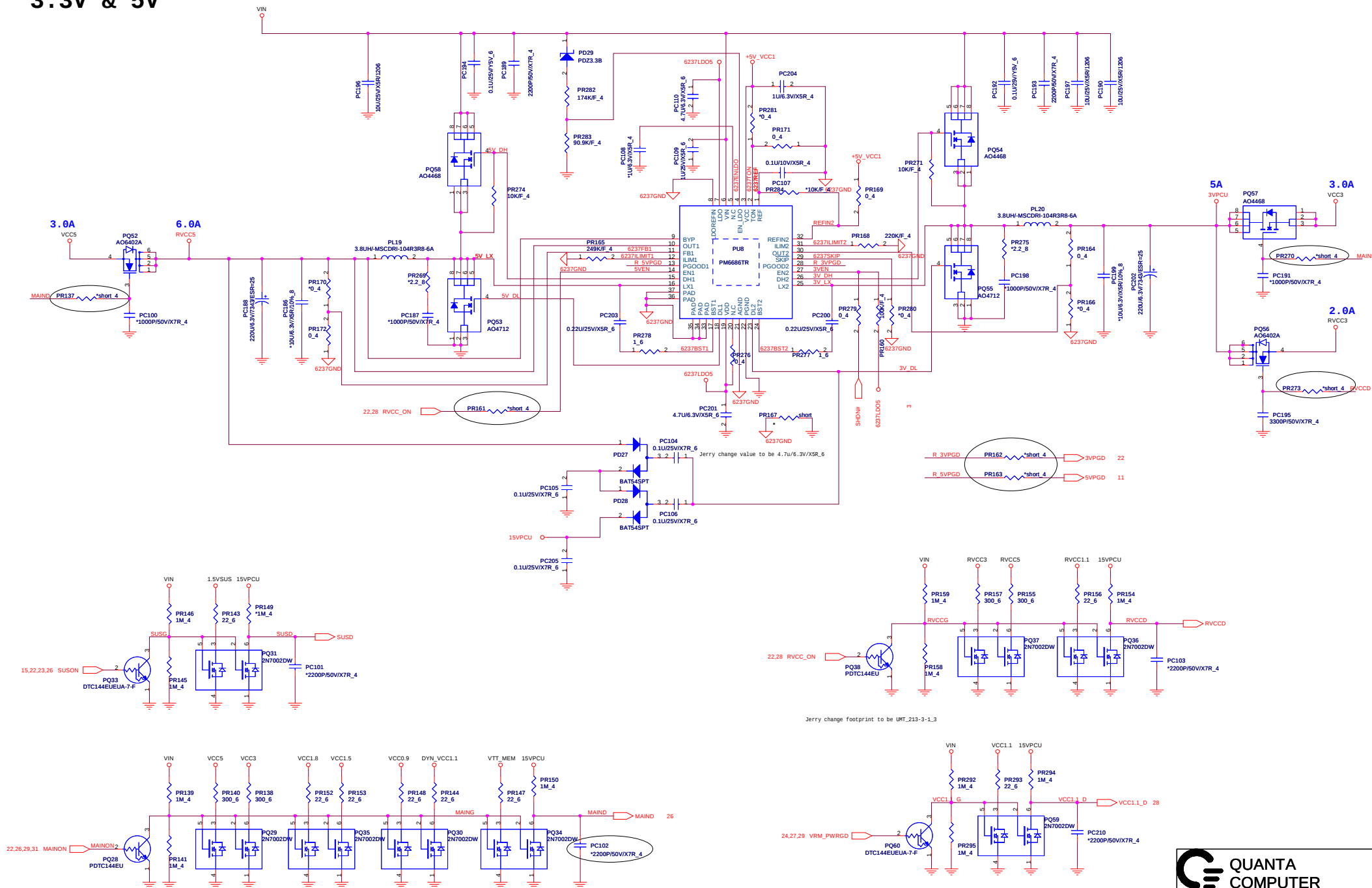


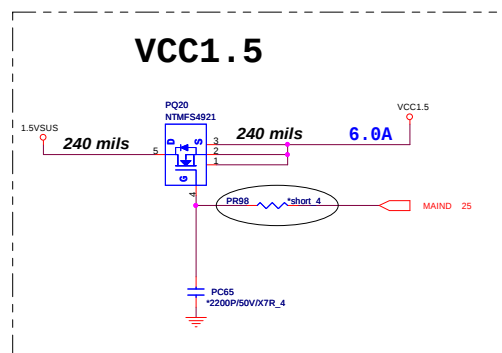
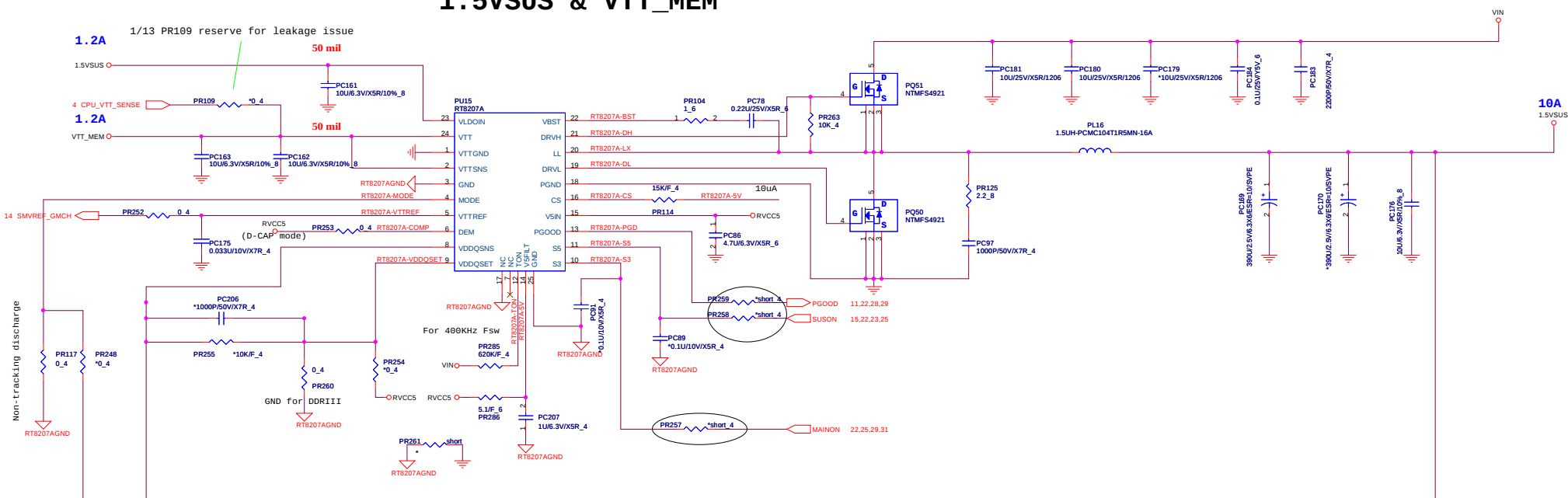
USB Port on MB



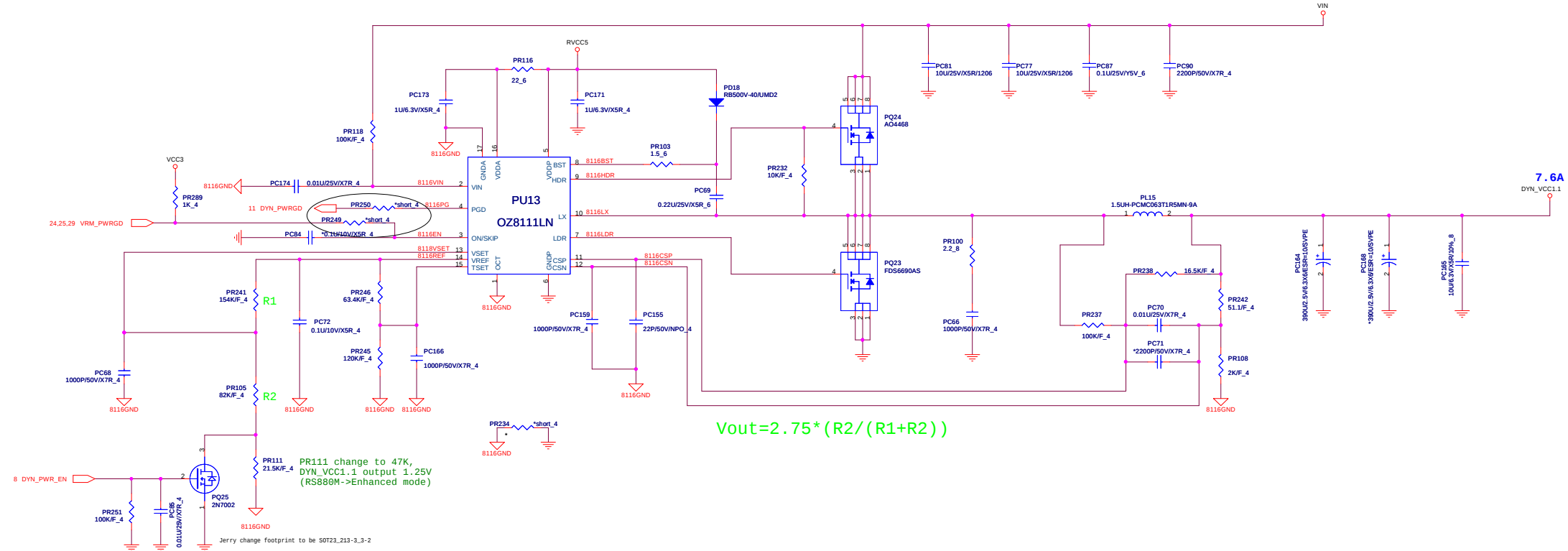
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





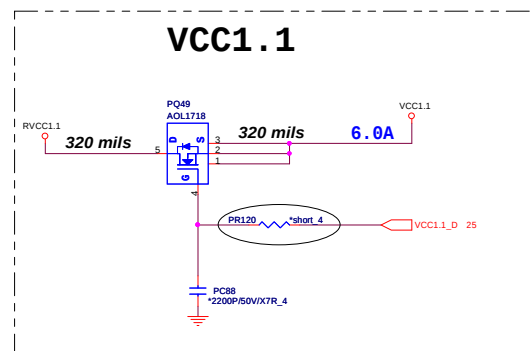
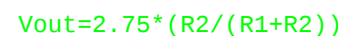


STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

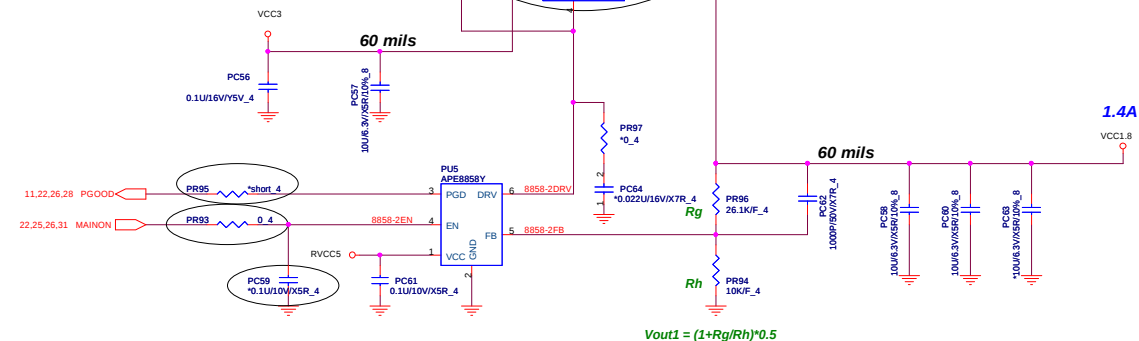
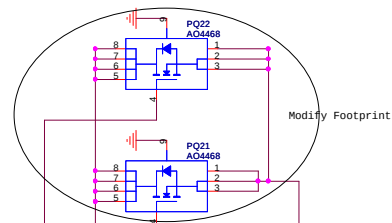


DYN_PWR_EN	High	Low
DYN_VCC1.1	0.95V	1.1V

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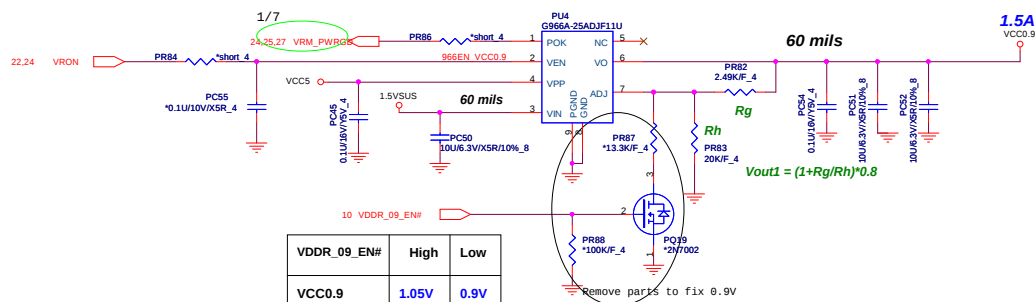


VCC1.8



$$V_{out1} = (1 + R_g/R_h) \cdot 0.5$$

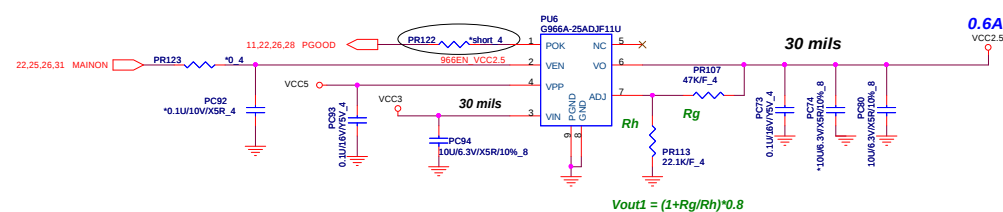
VCC0.9



VDDR_09_EN#	High	Low
VCC0.9	1.05V	0.9V

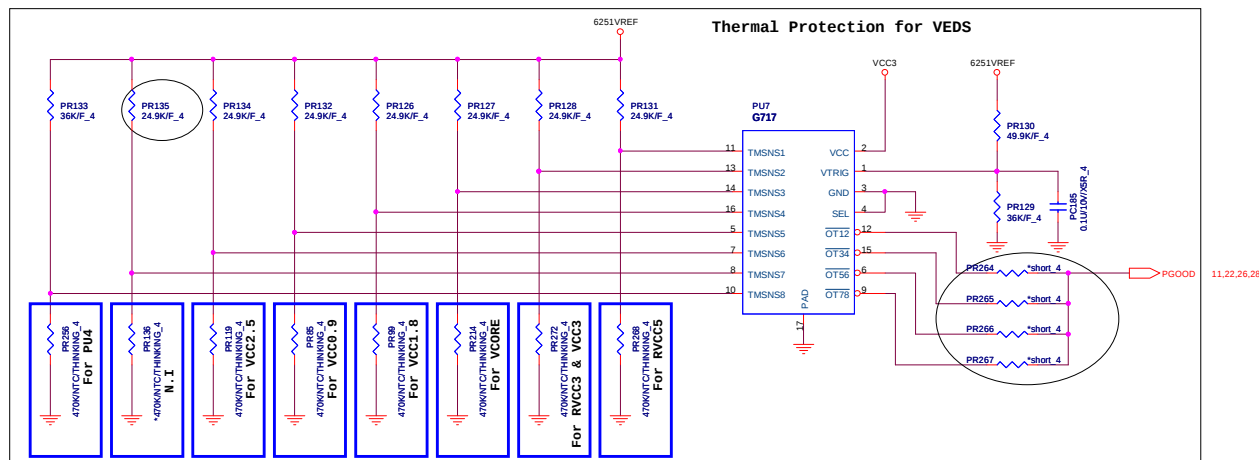
 Remove parts to fix 0.9V

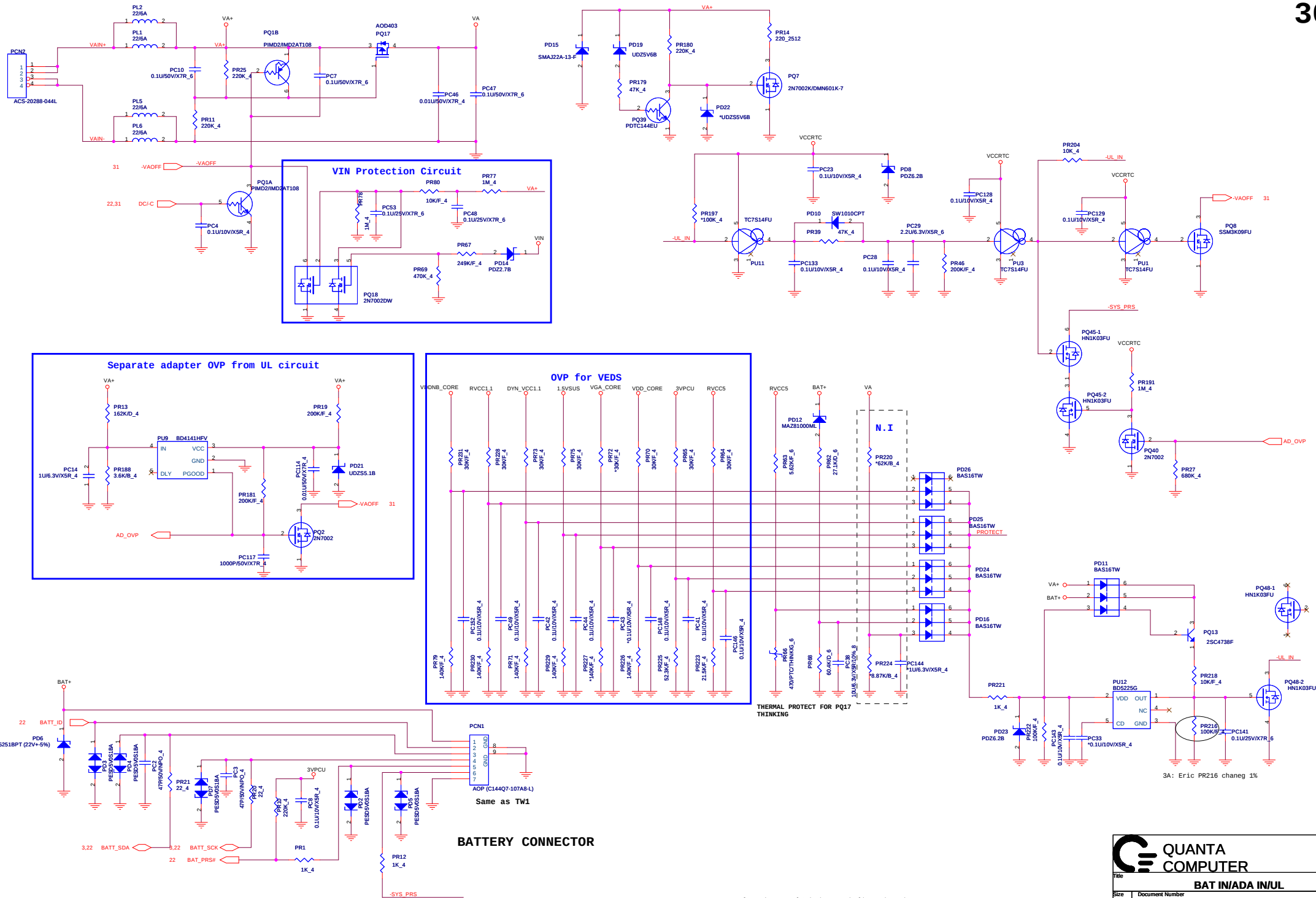
VCC2.5

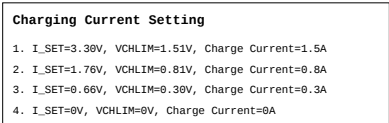


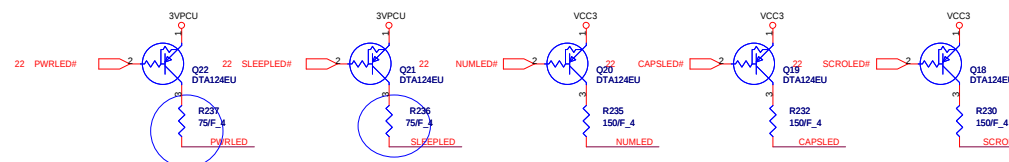
$$V_{out1} = (1 + R_g/R_h) \cdot 0.8$$

Thermal Protection for VEDS

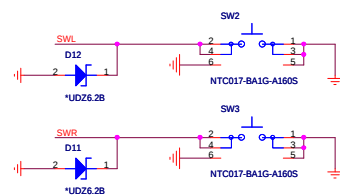




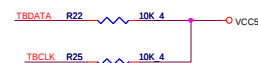
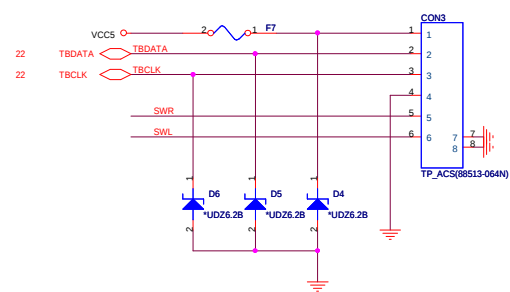




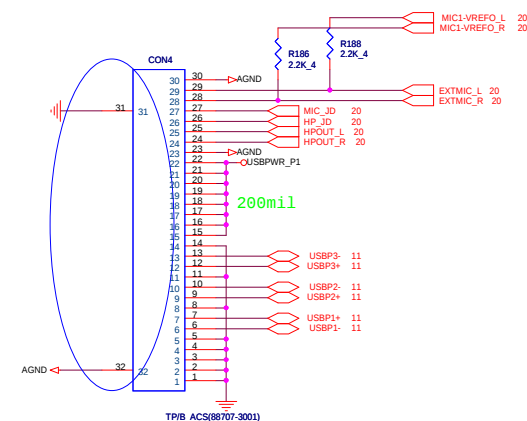
3A: change R236, R237 from 150 ohm to 75ohm for two color LED



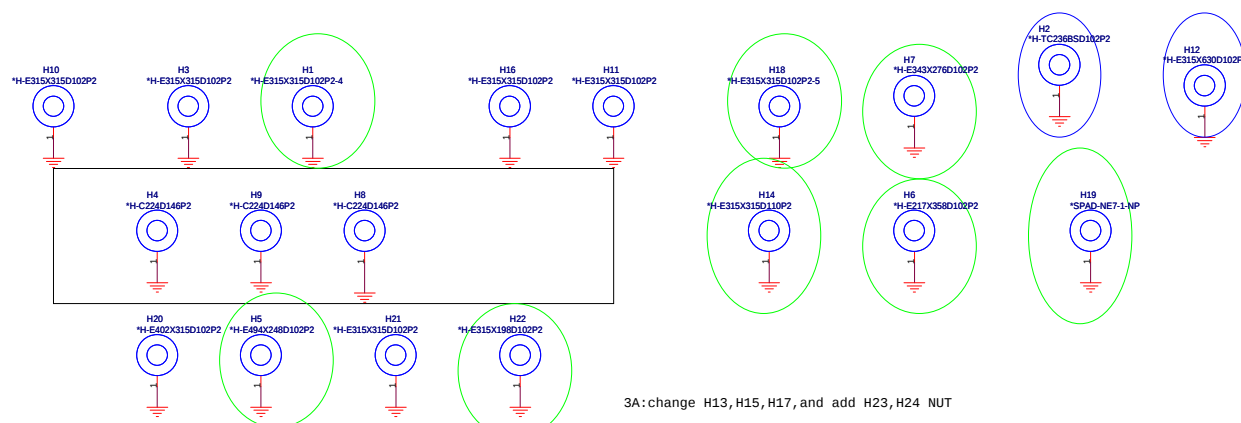
MB to TP connector



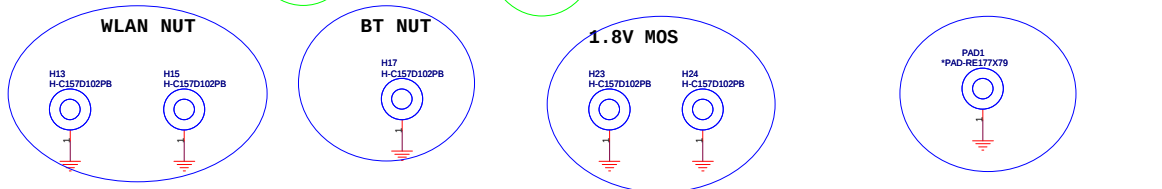
MB to USB board



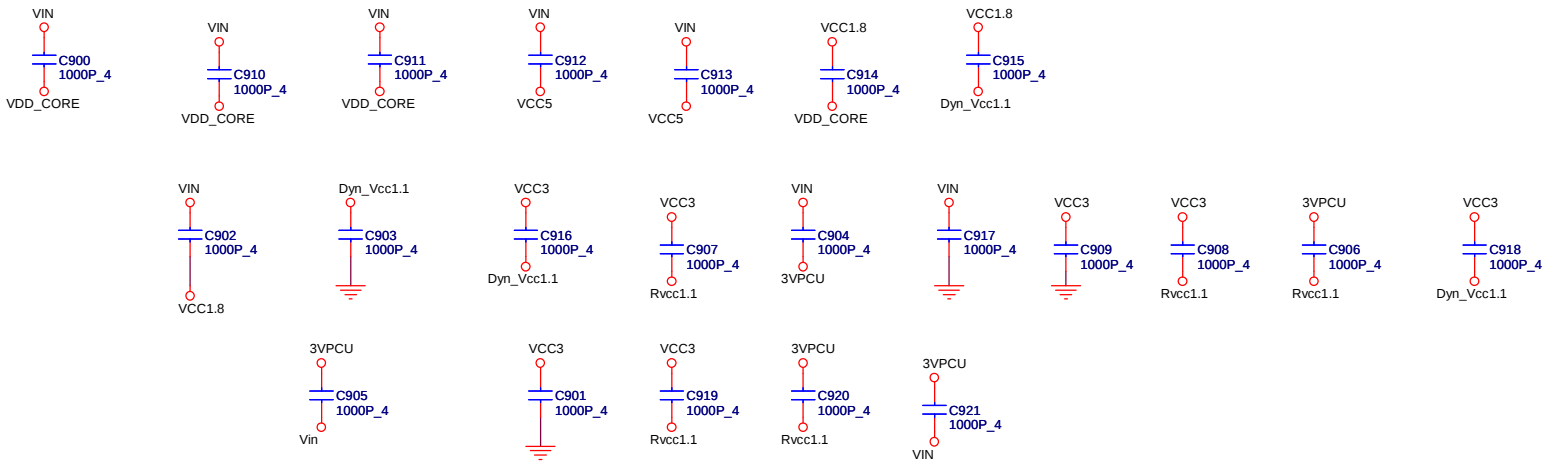
3A change from 88511-3091 to 88707-3091



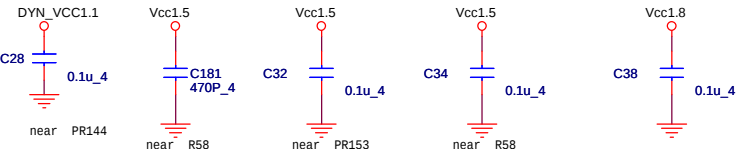
3A: change H13, H15, H17, and add H23, H24 NUT



Decoupling Cap



Power ripple



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QUANTA
COMPUTER

Title			Decoupling Cap		
Size	Document Number				Rev
B	AMD				3A
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			E		

Power on Sequence required:

- SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

- RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3, +1.1V ramp before VCC_NB

CPU_LDT_RST#
(SB TO CPU)
CPU_LDT_PWRGD
(SB TO CPU)
CPU_CLKP/N

SB OUTPUT - -NB_PWRGD
NB_PWRGD_IN
SB INPUT - -SB_PWRGD

GROUP B

GROUP A

PGOOD(DYN)
DYN_VCC1.1
VLD1(VCC1.1)
VCC1.1
VRM_PWRGD
VCC0.9
VDD_CORE
(VRON)
VDDNB_CORE

PGOOD(2.5)
VCC2.5
(CPU_VDDA_2.5_RUN)
VCC1.5
PGOOD(1.8)
VCC1.8
VCC3, VCC5
MAINON
SUSON
PM_SLP_S3#

CPU MEM CTL &
DDR3 SODIMM PWRs

PGOOD(1.5)
MEM_VTT
1.5VSUS

CPU_THM/SB/SB_SCL1/2
SB_KB/SPI/LPC ROM PWRs

PM_SLP_S5#
EC_DNBSWON#
RSMRST#
PGOOD(1.1)
RVCC5, RVCC3, RVCC1.1

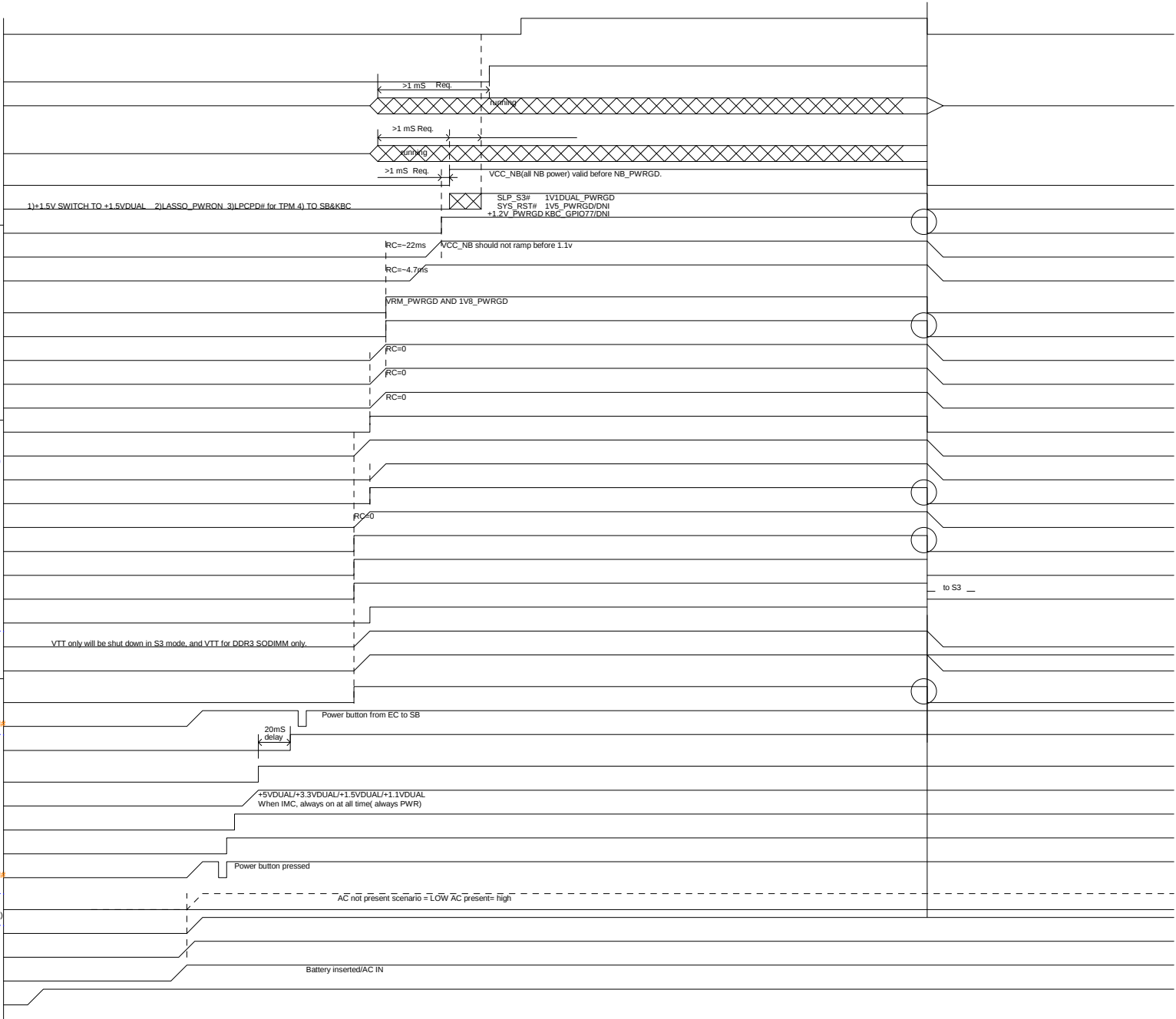
VDD_DUAL_EN
RVCC_ON

KBC is ready

EC_DNBSWON#
DNBSWON#

KBC is powered by
A_VBAT & +3.3VALW

AC_OK
(ACIN detect)
3VPCU
LDO 5.4V
(from DCIN)
+VIN/+12V_HD
A_VBAT





QUANTA
COMPUTER

File

Size C

Document Number

AMD

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Rev 3A

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Change History

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

S		4		3		2		1	
12/21								35	
Page 10--R309 unmount									
Page 8--R252 mount(CS00002JB38)RESISTOR CHIP 0 1/16W +-5%(0402)									
Page 8--R101 & R106 unmount									
Page 12--mount R184,R179,R289(CS31002FB26) RC0402,RC0402-C,0402-CNXT									
Page 11--change R174,R175,R278,R146 to 10Kohm(CS31002JB28; RES CHIP 10K 1/16W +-5% (0402))									
Page 21--LU1 change AL008111001 to AL008111002									
Page 20--C29,C30 Mount 33PF CH03306JB04									
Page 10--R20,R21 change CS00003J951 to bead CX8PG471000									
12/22									
Page 16--RP38 pin2 & pin 4 change net name :HDMI_TCXP & HDMI_TXCN									
Page 16--C422 & C421 change net name :HDMI_TCXP & HDMI_TXCN									
Page 32--H12 need change footprint									
Page 32--H22 need change footprint									
Page 32--remove H19									
Page 32--Add H23 & H24									
Page 10-- modify net name as NB_DISP_CLKN									
12/23									
Page 32--PU VCC5 TBDATA & TBCLK		Page 32--change footprint							
				H1 : H-E315X315D102P2-4					
				H2 : H-E315X630D102P2					
Page 20--add 3 pcs 0ohm for EMI				H5 : H-E494X248D102P2					
				H6 : H-E217X358D102P2					
				H7 : H-E343X276D102P2					
Page 32--Add H23 footprint H-E315X315D102P2				H12 : H-C236D102P2					
& H24 footprint H-E315X315D102P2				H18 : H-E315X315D102P2-5					
				H22 : H-E315X198D102P2					
12/24									
Page 21 -- change 25MHz XTAL P/N:BG625000737									
LC20 & LC21 change to CH03306JB04									
12/25									
Page 15 --camera power source 從USB power 改成RVCC5									
12/28									
Page 22 --U11(35001) ID pin 漏電問題,									
請參考GD3加上diode, R108,R110,100 ohm									
PU改成2.2K;R272 10k ohm PU改成4.7k ohm									
Page 22 --slp_s5#從EC pin 26改成106, 相當於Intel的slp_s4#, pin 26到106中間留一顆0 ohm接起來先不上									
Page 11,15,22 --SB_PWRGD接到EC pin 16, 並改名爲HW_PWRGD, 以方便辨識									
Page 20 --change codec U34 P/N:AL000269007									
12/29									
Page 19 --remove Express card		1/15							
1/13				Page 3:con20 CPU_LDT_RST# add C31(reserve)					
Page18: MC8 unmount for MS card				Page 21: LU1 pin 30 add LR4 10Kohm					
recognize issue				Page 29: mount PR86					
Page4 : Reverse CPU_VTT_SENSE PU				AJ069700T08-->IC CTRL(605P)SB820M					
VCC0.9				AJ075200T16--> IC CTRL(528P)RS880M					
Page26: PR109 reserve for leakage				Page 16: Change CON13 footprint					
issue				-->hdmi-c12806-11908-1-19p-v					
1/19		1/18							
Page 32: H19 add Spad-NE7-1-NP				Page 3: T10 & T11 change footprint TP3050					
Page 32 :H14 change footprint									
H-E315X315D110P2									
Page 21: LU2 Change P/N DBBL5MLAN01									
						</			

1/21--->改版PVT
Page 21:LU1 pin26 ISOLATE# add 15kohm PD
1/22
Page 10: Y7 change P/N:BG332768909
C478 change to 18PF

Page 10: change Y12 P/N: BG625000486
and C430=C431 27PF for timing accuracy
Page 21:LY1 Change 25MHz XTAL P/N:BG625000486(2nd:BG625000737)

2/10
Page11: HW_PWR6D PD 10Kohm ---decrease impact on switch issue
Page 20: ChangeR317,R323 from 22ohm to 0ohm for FSOV Fail issue
Page 20: AMP_PD# power change from +5VA to 3VPCU
Page 22: add INT_LVDS_ENA_BL pin for EC control backlight
Page11: R174,R175 change from 10kohm to 2.2kohm
Page14: C10 chagne from 10UF to 4.7UF
Page15: chagne CON7 LVDS con
Page19: chagne CON18 BT con
Page17: chagne WLAN switch SW4
Page20: chagne spk con CON10
Page3: CPU_LDT_RST# add R69 short pad for debug

3/5
Page16: change power source for CRT port
Page16: change D9,D7 P/N and mount R266,R267
Page21: LR8 umount
Page22: R68 mount

3/8
Page 24: Change PC 142 footprint ECAP10X6S-Z01
Page 16: Change CON13 footprint & P/N:
from hdmi-c12806-11908-1-19p-v to Hdmi-c12825-11908-1-19p-v
3/9
Page 23: delete L27
Page6 & Page11: remove all side port component

3/10
Page 3:add C291 & C137(mount) change from 0.1u(CH4102M9B13) to 180pf (CH11806JB09)
for power noise
Page 3:C31(mount) change from 33pf to 180pf (CH11806JB09)
for power noise

3/11
Page6 :R47 and R49 change from 0ohm to short pad
Page8 :R245 change from 0ohm to short pad
Page20 :remove R220
Page20 :change C488,C491,C494 from AGND to GND
Page 3 & 22 & 10: Change CPU Prochot schematic controlled by EC
Page 3 mount R267
Page 6:delete R56 & R63
Page 8: change R83,R77,R65,R253,R71,R57,R91,R245 & R250 to short pad
Page 8: delete R255,R252

3/12
Page 9: delete R251,R249,C377,c191,c201,c195,c184,c196,R93,R89 for no side port
Page 10: delete RP5,RP29,RP32,RP15,RP35,RP30
Page 10: delete R300
Page 11:delete RP27,SW1,RP25 (remove Panel ID set)
Page 18:Change MR19,MR3,MR2,MR9,MR10,MR11,MR12,MR13,MR14,MR15,MR16,MR17,MR18,MR8 to short pad
Page 24:Change PC142 footprint Ecap10x6s-SMT
Page20 :delete R322,R329,R328
Page21 :delete LR14
Page21 :change LR6 to short pad
Page 9: Change L7,L5,L6,L8,R80,R95 to short pad
Page 13: Change R187,L10,L9,L15,L13,L28,L18,R169,L12,L11,L19,L14,L17,R127,R284,L26,R145 to short pad

3/15
Page 20: reserve Q29 and R399,
mount R367 for pop noise
Page 20:Change R330、R321、R346、R347 from 1.5K ohm to 10K ohm for pop noise
Page 20:add C343,C345,C346,C347 10uF for pop noise
Page 8:R86 change from 301ohm to 1Kohm
Page 11:R207& R208 from 100k ohm to 10k ohm
Page 20:R363 unmount
Page 18:ML1 & MR4 change to short pad
Page 19:delete Q16
Page21:change con9 from DFTJ08FR085 to DFTJ08FR167
Page22:U13 GPIO66 PL 10kohm(R159)
Page 12:delete R176
Page 15:delete R36
Page 19:con18 delete T39,T40
Page 20:delete R317,R323
Page 20:R214 change from 0ohm to short pad
Page 22:delete R68
Page 3:delete con20 & C31 & C267
Page 3:reserve C182 0.1uF
Page 3:R69 change to short pad

3/16
Page 23:reserve U42 ESD part
Page 32:change con4 抽屨式
Page 32:change H13,H15,H17,and add H23,H24 NUT
Page 19:Reverse C786, C787, C788 FP for ESD
Page 20:C342 unmount
Page 20:CPU_PROCHOT# add C312
Page 9:mount C217 for DYN_VCC1.1 power ripple too large

3/17
Page20:R206,R205,R215,R210,R209,R222,R211,R217,R223 change to short pad
Page 3:reserve C184 0.1uF
Page21:change LC23 from 1000P/2KV to 1000P/3KV
Page 3:delete R51,R50
Page 4:delete R11
Page20:L1~L4 change P/N to CX121T20100
Page 16:delete RP38
Page 18:delete MRP1
Page 22:delete R155
Page 3:delete R238
Page 15:delete R355
Page 15: R273 change from CS41002JB20 to CS41002FB28

3/20
Page 32: change R236,R237 from 150 ohm to 75ohm for two color LED

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