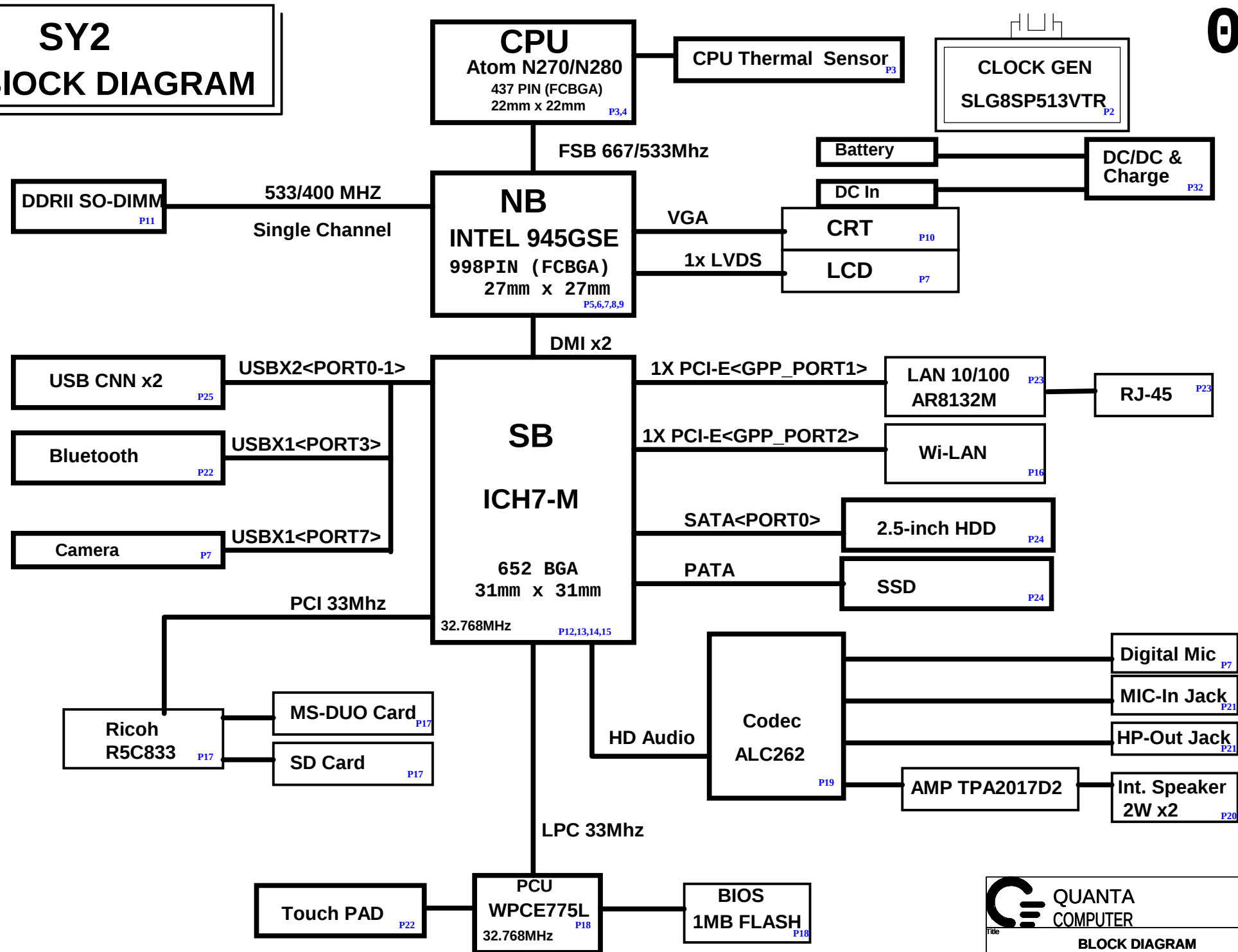
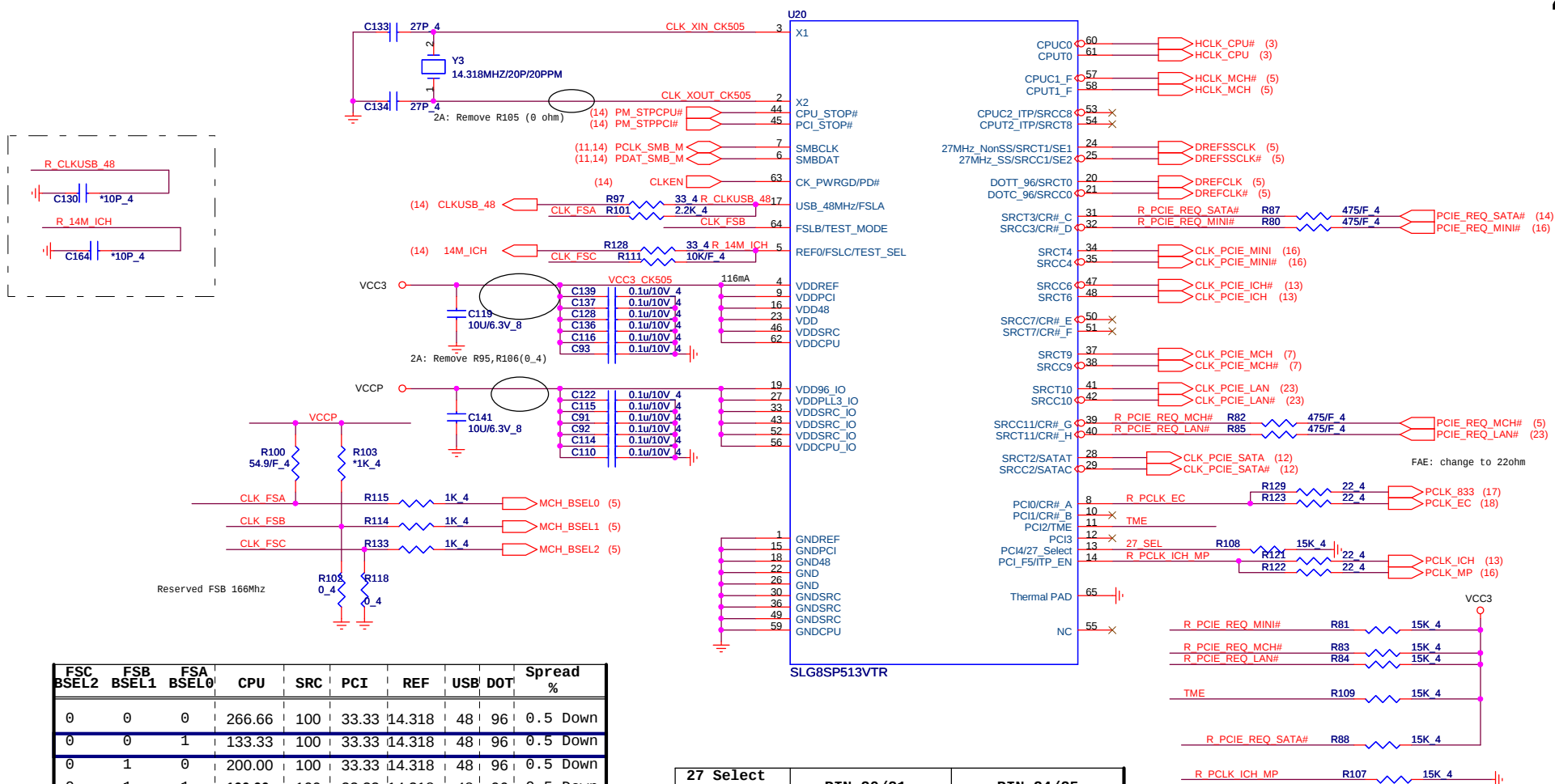


SY2 BLOCK DIAGRAM

01



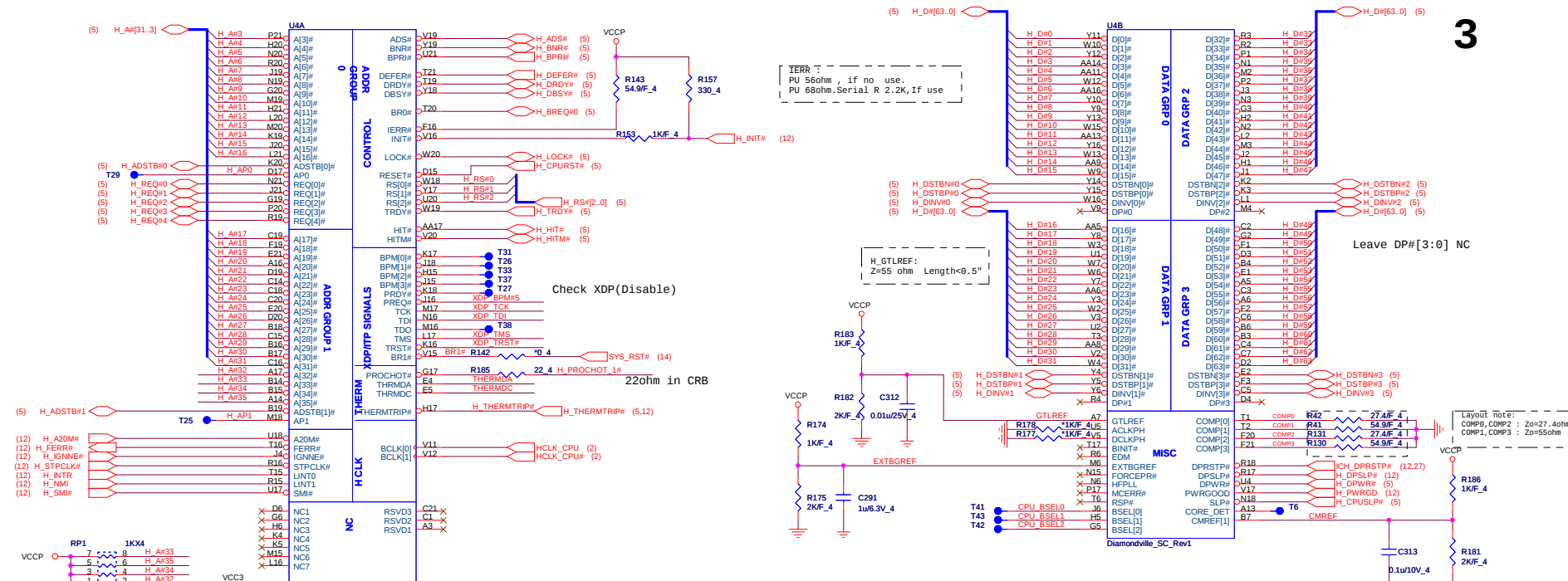
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



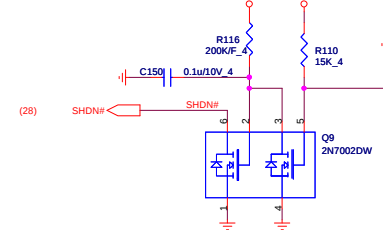
1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



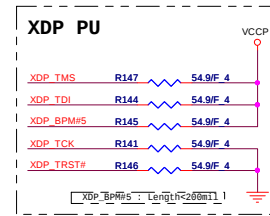
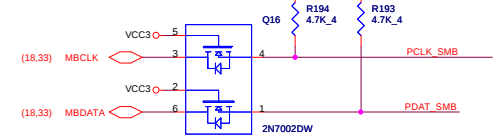
Title					
CLKGEN					
Size	Document Number				Rev
Custom	SY2 MB				2C
Date	Friday, April 10, 2009		Sheet	2 of 36	



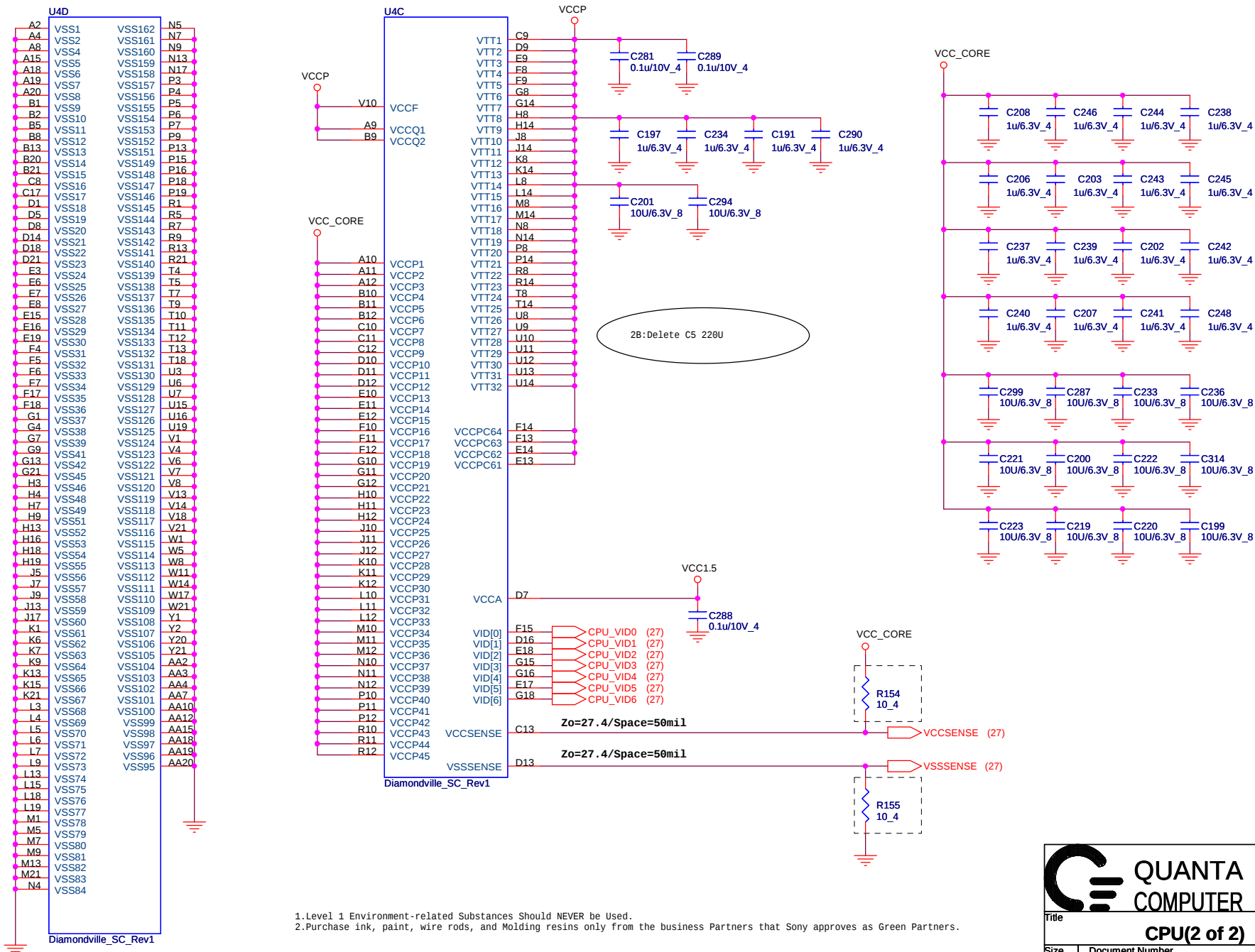
Thermal Sensor



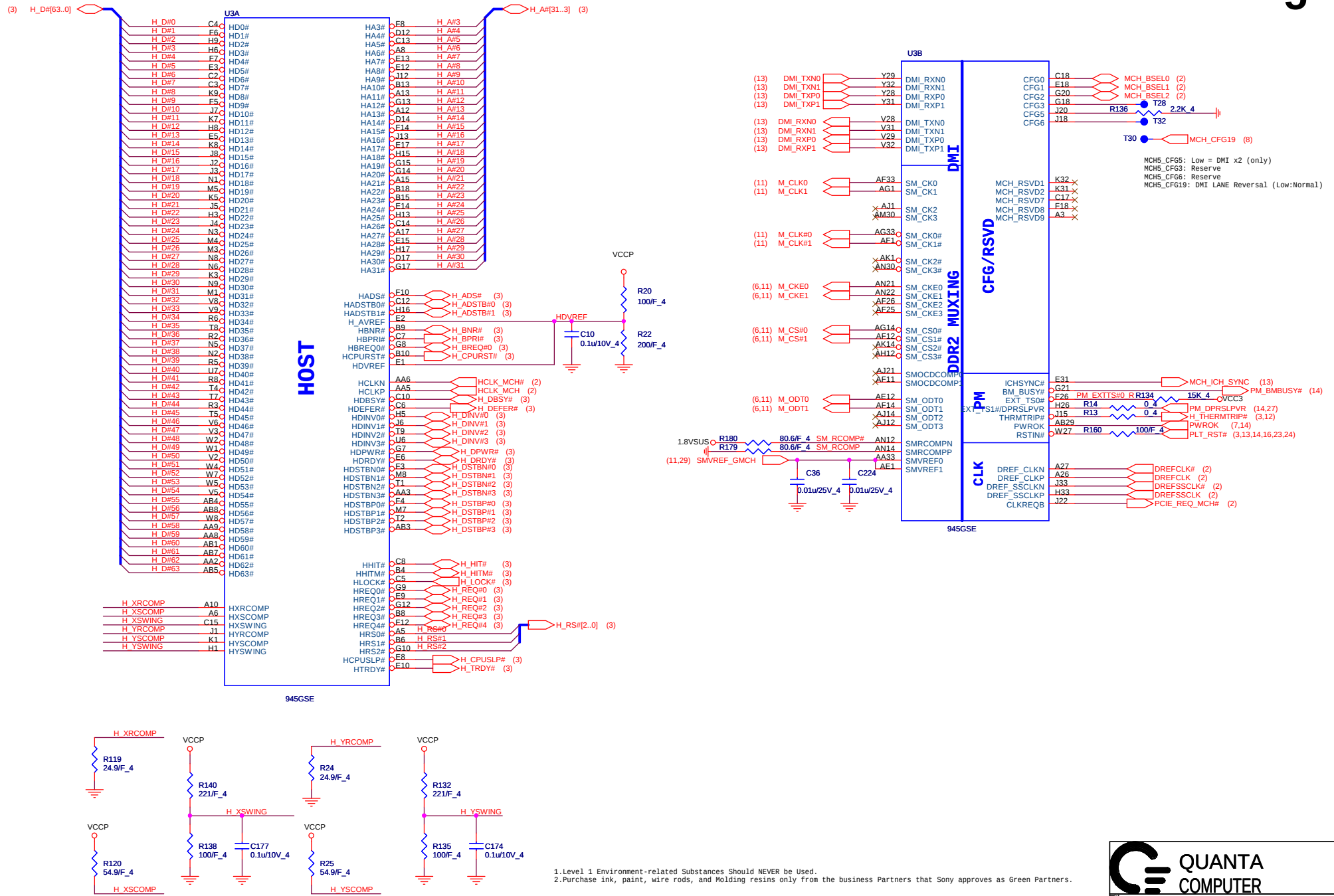
Thermal I2C



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



 QUANTA COMPUTER		
Title		
CPU(2 of 2)		
Size	Document Number	Rev
Custom	SY2 MB	2C
Date:	Friday, April 10, 2009	Sheet 4 of 36



(11) M_A_DQ[63..0]

U3C

DDR2 SYSTEM MEMORY

945GSE

SA_BS_0
SA_BS_1
SA_BS_2
SA_DM0
SA_DM1
SA_DM2
SA_DM3
SA_DM4
SA_DM5
SA_DM6
SA_DM7
SA_DQS0
SA_DQS1
SA_DQS2
SA_DQS3
SA_DQS4
SA_DQS5
SA_DQS6
SA_DQS7
SA_DQS0#
SA_DQS1#
SA_DQS2#
SA_DQS3#
SA_DQS4#
SA_DQS5#
SA_DQS6#
SA_DQS7#
SA_MA0
SA_MA1
SA_MA2
SA_MA3
SA_MA4
SA_MA5
SA_MA6
SA_MA7
SA_MA8
SA_MA9
SA_MA10
SA_MA11
SA_MA12
SA_MA13
SA_CAS#
SA_RAS#
SA_RCVENINB
SA_RCVENOUTB
SA_WEB
SB_BS_0
SB_BS_1
SB_BS_2
SB_MA0
SB_MA1
SB_MA2
SB_MA3
SB_MA4
SB_MA5
SB_MA6
SB_MA7
SB_MA8
SB_MA9
SB_MA10
SB_MA11
SB_MA12
SB_MA13

AK12
AH11
AG17
AB30
AL31
AF30
AK26
AL9
AG7
AK5
AH3
AC28
AJ30
AK33
AL25
AN9
AH8
AM2
AE3
AC29
AK30
AJ33
AM25
AN8
AJ8
AM3
AE2
AJ15
AM17
AM15
AH15
AK15
AN15
AJ18
AF19
AN17
AL17
AG16
AL18
AG18
AL14
AJ17
AK18
AN28
AM28
AH17
AH21
AJ20
AE27
AN20
AL21
AK21
AK22
AL22
AH22
AG22
AE21
AM21
AE21
AL20
AE22
AE26
AE20

M_A_BS0
M_A_BS1
M_A_BS2
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7
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M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_CAS#
M_A_BS#
M_A_RAS#
M_A_WE#

M_A_BS0 (11)
M_A_BS1 (11)
M_A_BS2 (11)
M_A_DM[7..0] (11)
M_A_DQS[7..0] (11)
M_A_DQS# [7..0] (11)
M_A_A[13..0] (11)
M_A_CAS# (11)
M_A_RAS# (11)
M_A_WE# (11)

M_CS#0
M_ODT0
M_CKE1
M_CKE0
M_ODT1
M_CS#1

M_CS#0 RN2
M_RAS#
M_ODT0
M_A_A13
M_CKE1 RN7
M_A_A7
M_A_A6
M_CKE0
M_ODT1
M_CS#1

M_A_A3 RN4
M_A_A1
M_A_A10
M_A_A2
M_A_A11 RN6
M_A_A0
M_A_BS2
M_A_A12
M_A_A4 RN5
M_A_A9
M_A_A8
M_A_A5

M_A_BS1 RN3
M_A_BS0
M_A_CAS#
M_A_WE#

VTT_MEM
VTT_MEM

C334
C328
C335
C333
C339
C336
C331
C341
C332
C330
C340
C338
C337
C329

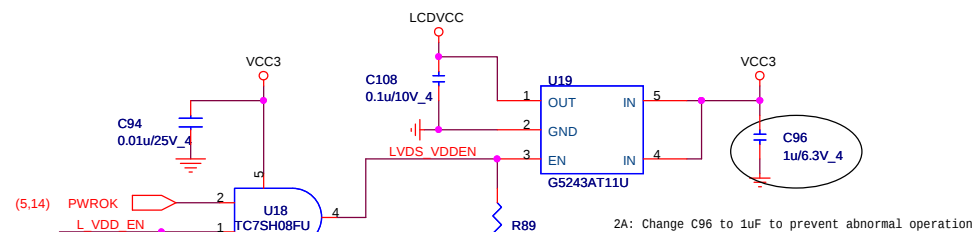
0.1u/10V 4
0.1u/10V 4
0.1u/10V 4
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0.1u/10V 4
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0.1u/10V 4
0.1u/10V 4

6

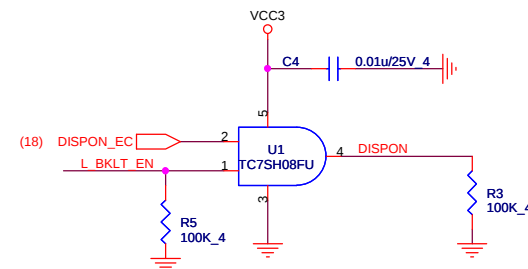


QUANTA
COMPUTER

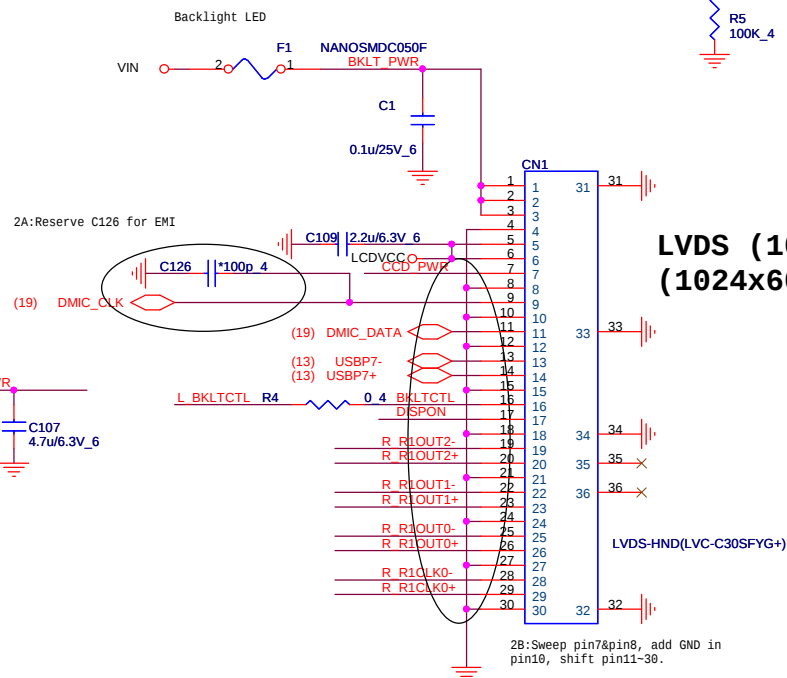
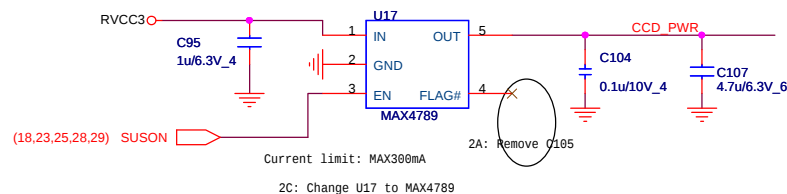
Title		
GMCH DDR (2 of 5)		
Size	Document Number	Rev
Custom	SY2 MB	2C
Date:	Friday, April 10, 2009	Sheet 6 of 36



Display On



LVDS (10.1")
(1024x600, 1366x768)



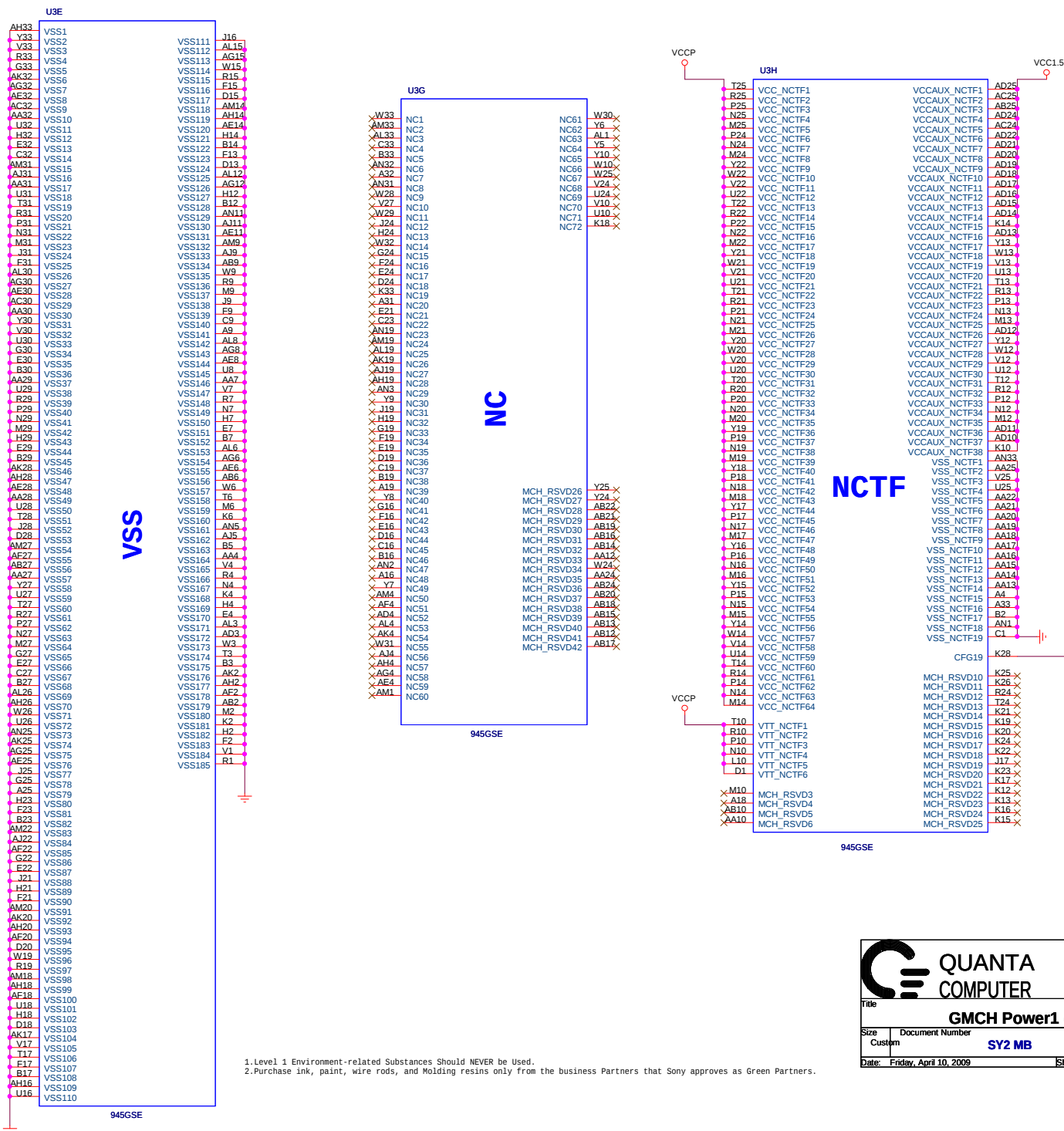
QUANTA
COMPUTER

Title	GMCH DMI VIDEO (3of 5)
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SY2 MB

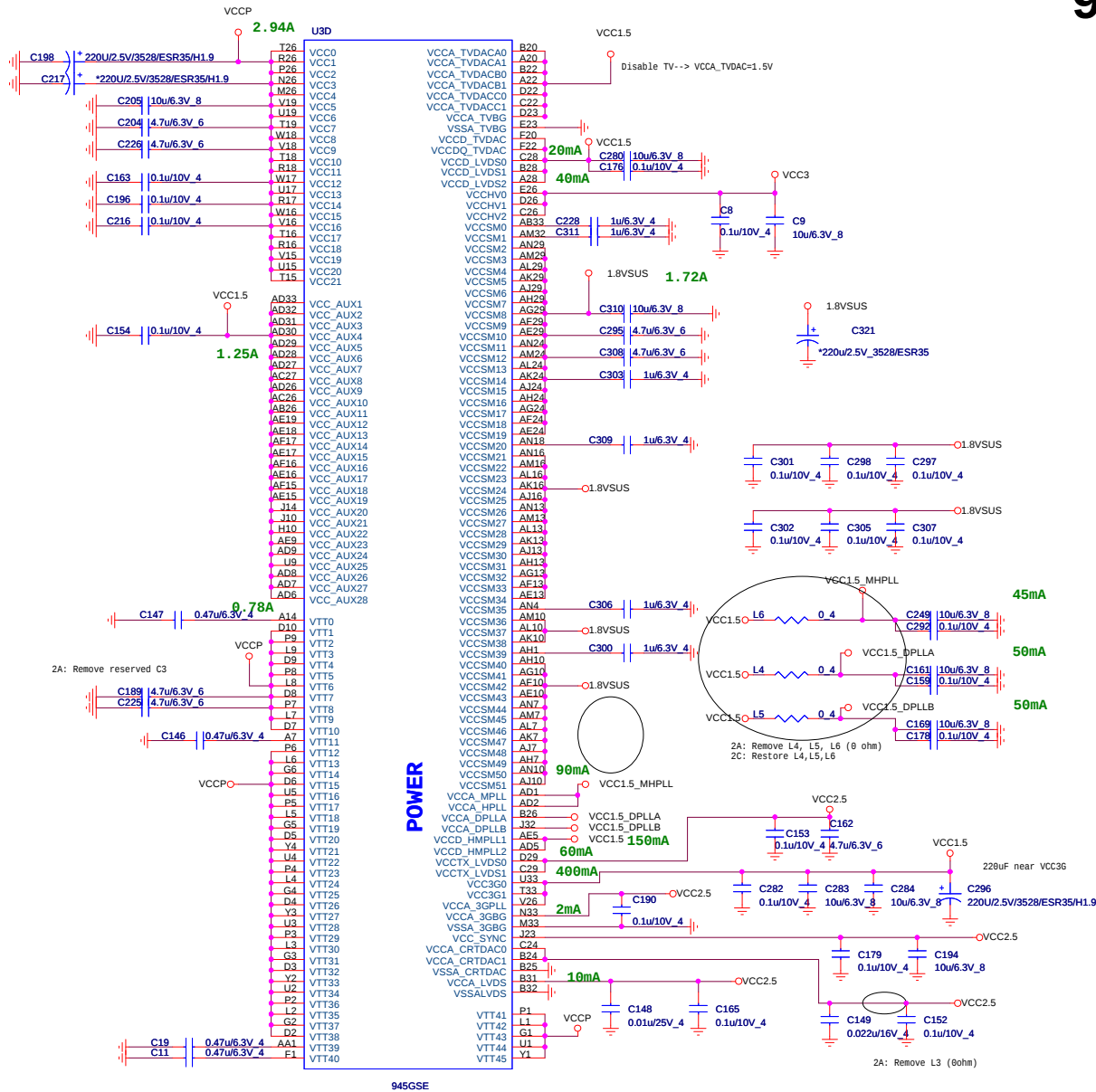
Rev	2C
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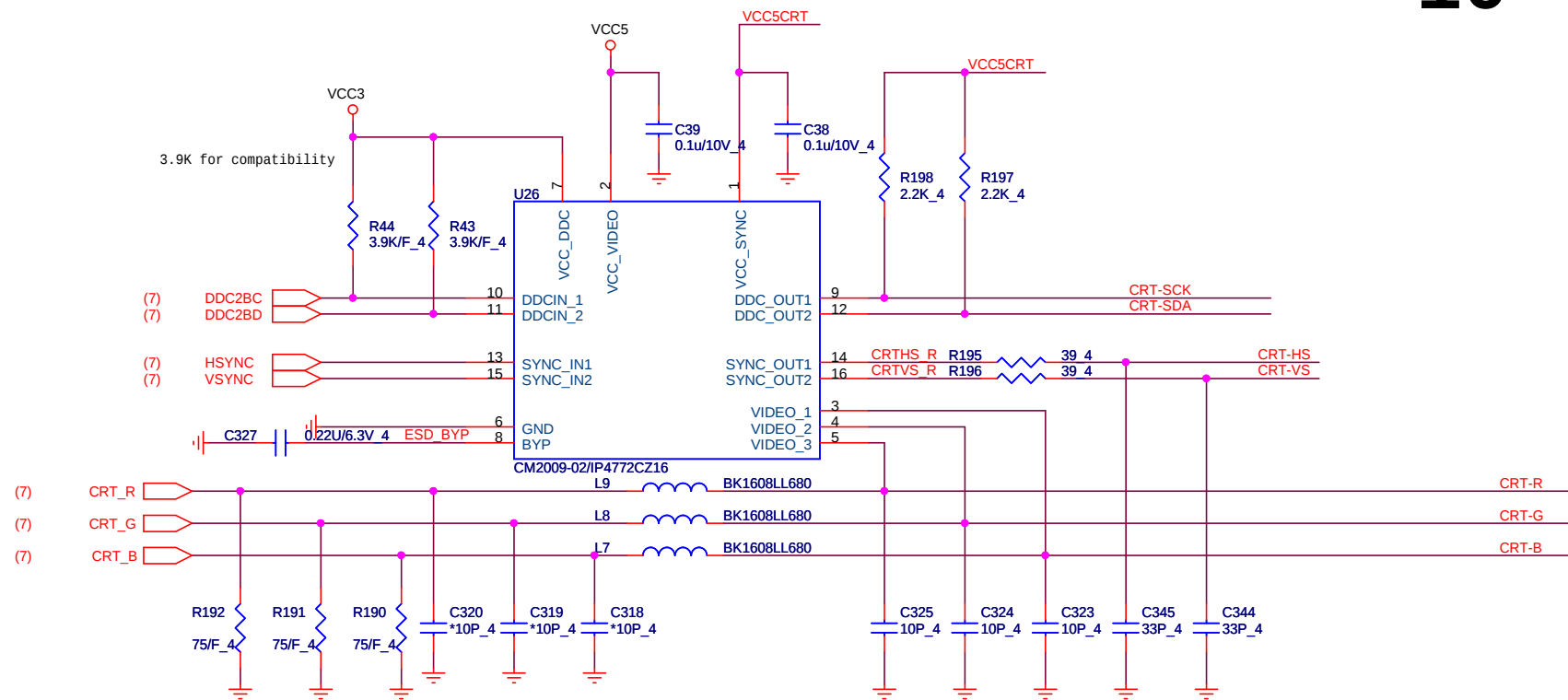
Sheet 7 of 36



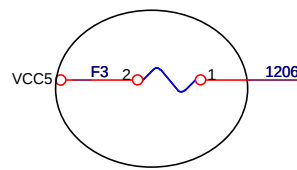
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

		
Title		
GMCH Power1 (4of 5)		
Size	Document Number	Rev
Custom	SY2 MB	2C
Date: Friday, April 10, 2009	Sheet	8 of 36



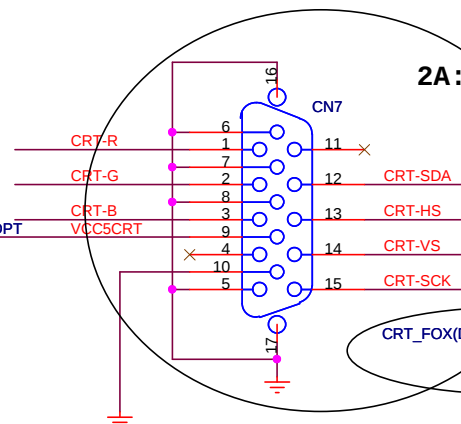


VCC5CRT(5V+-10%)
Current limit <1A



2A: Change F3 to 0.25A ((hold))

2A: Correct PCB-FP symbol



2A: Change CRT CN in gray color(new p/n)



Title

CRT

Size
Custom

Document Number

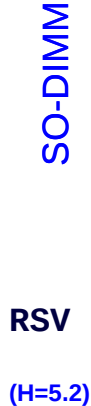
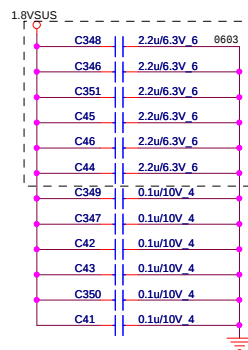
SY2 MB

Rev
2C

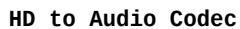
Date: Friday, April 10, 2009

Sheet 10 of 36

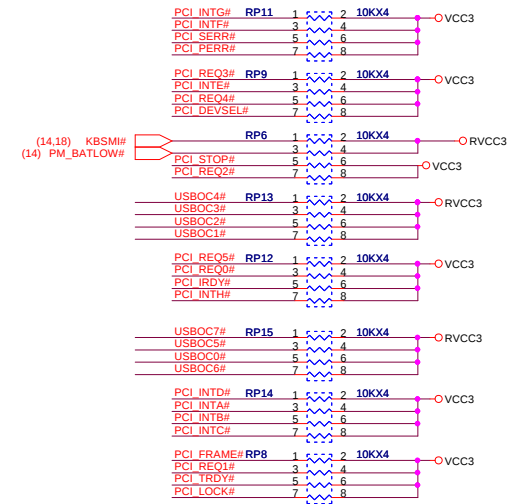
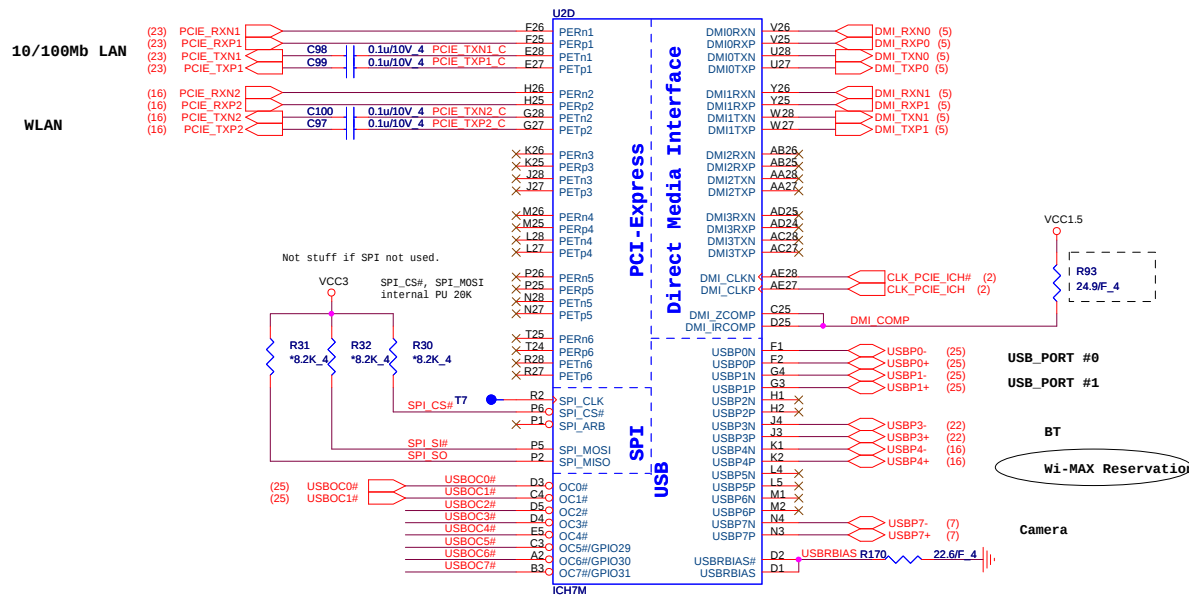
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



 QUANTA COMPUTER		DDRII SODIMMx1	
Title		Rev	
Size Custom	Document Number SY2 MB	Sheet 11	of 36
Date: Friday, April 10, 2009		Rev 20	



1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



SPI_CS#	Internal PD ;Should not be PU
SPI_MISO	Internal PU ;Should not be PD

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---

ICH Boot BIOS select

PCI_GNT#5 (INT PU)	PCI_GNT#4 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	IPC (Default)

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2



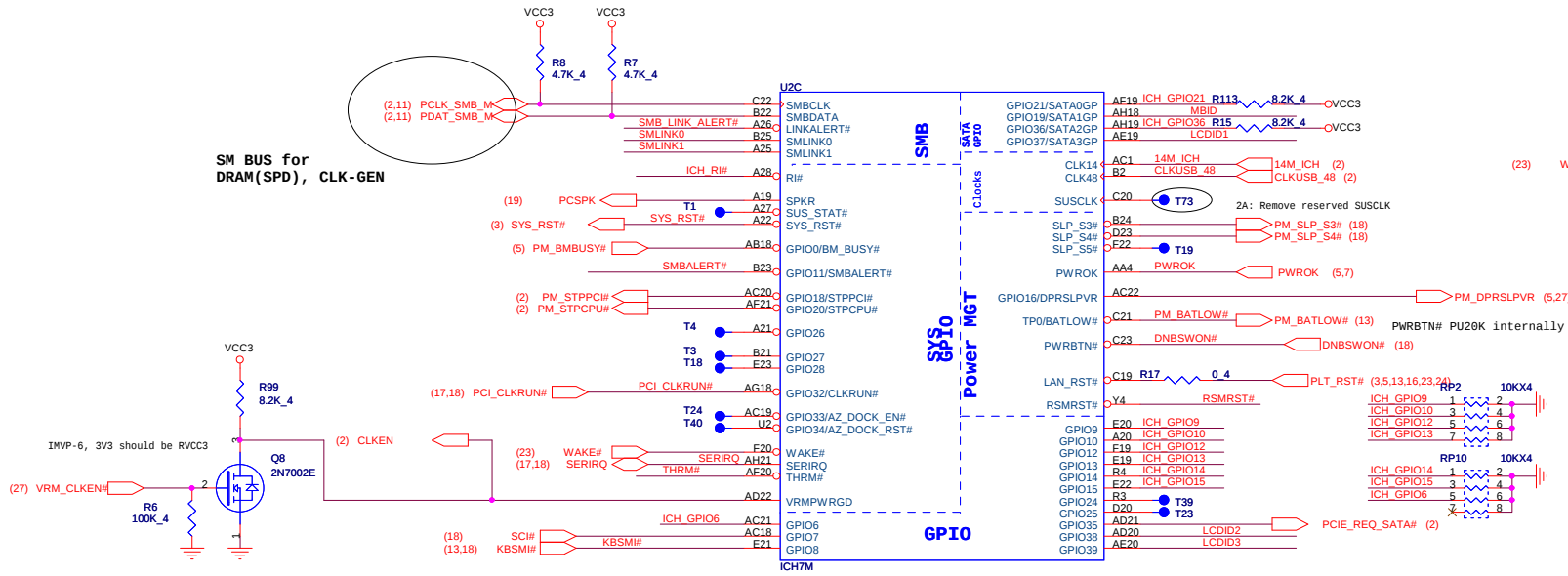
Title
ICH9-M PCI-E, USB, PCI (2 of 4)

Size Custom Document Number **SY2 MB** Rev 2C

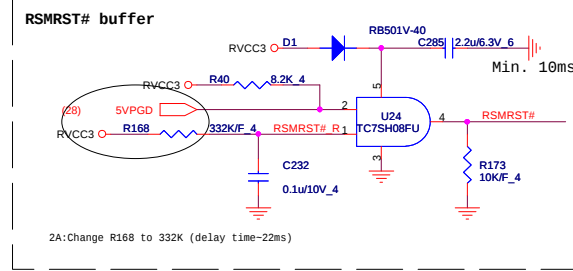
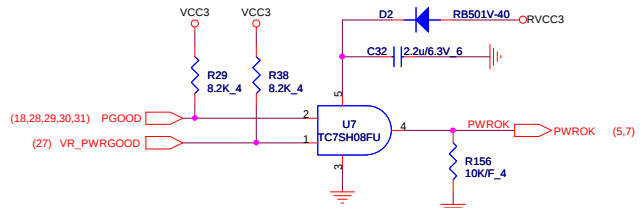
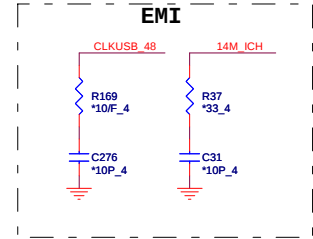
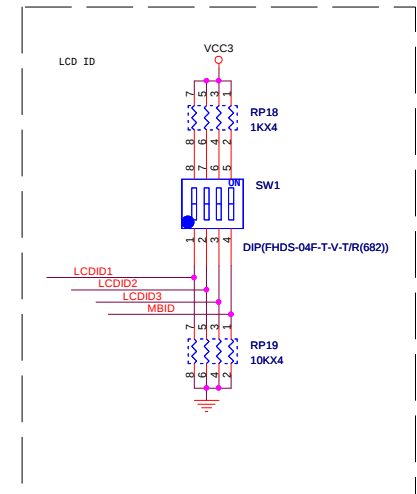
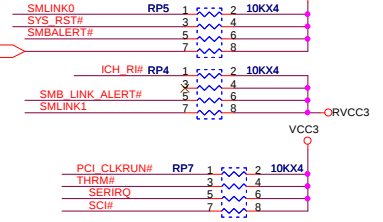
Date: Friday, April 10, 2009 Sheet 13 of 36

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

SM BUS for
DRAM (SPD), CLK-GEN

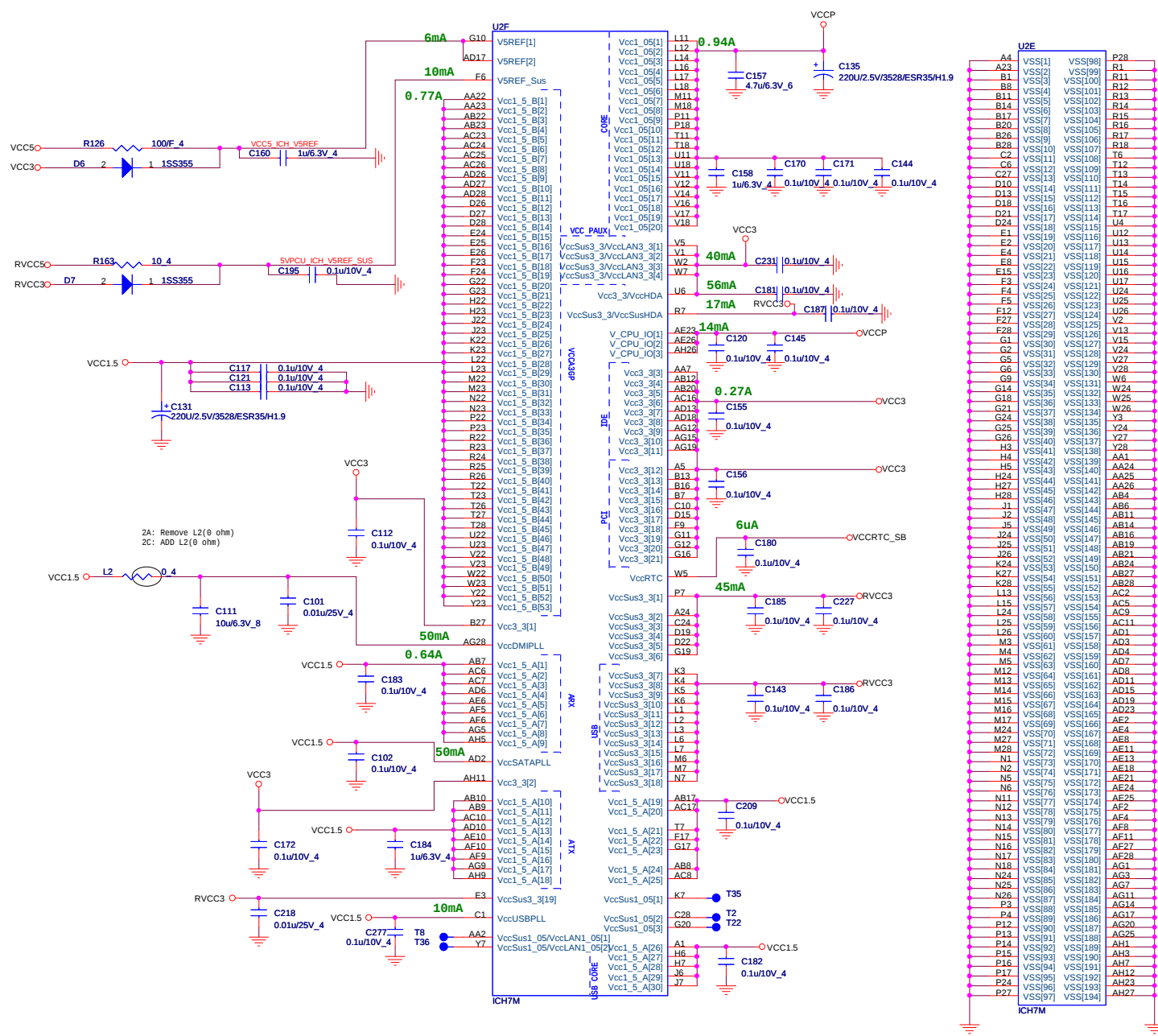


(23) WAKE#



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

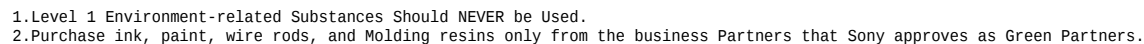
Title		
ICH9-M GPIO(30f 4)		
Size	Document Number	Rev
Custom	SY2 MB	2C
Date:	Friday, April 10, 2009	Sheet 14 of 36

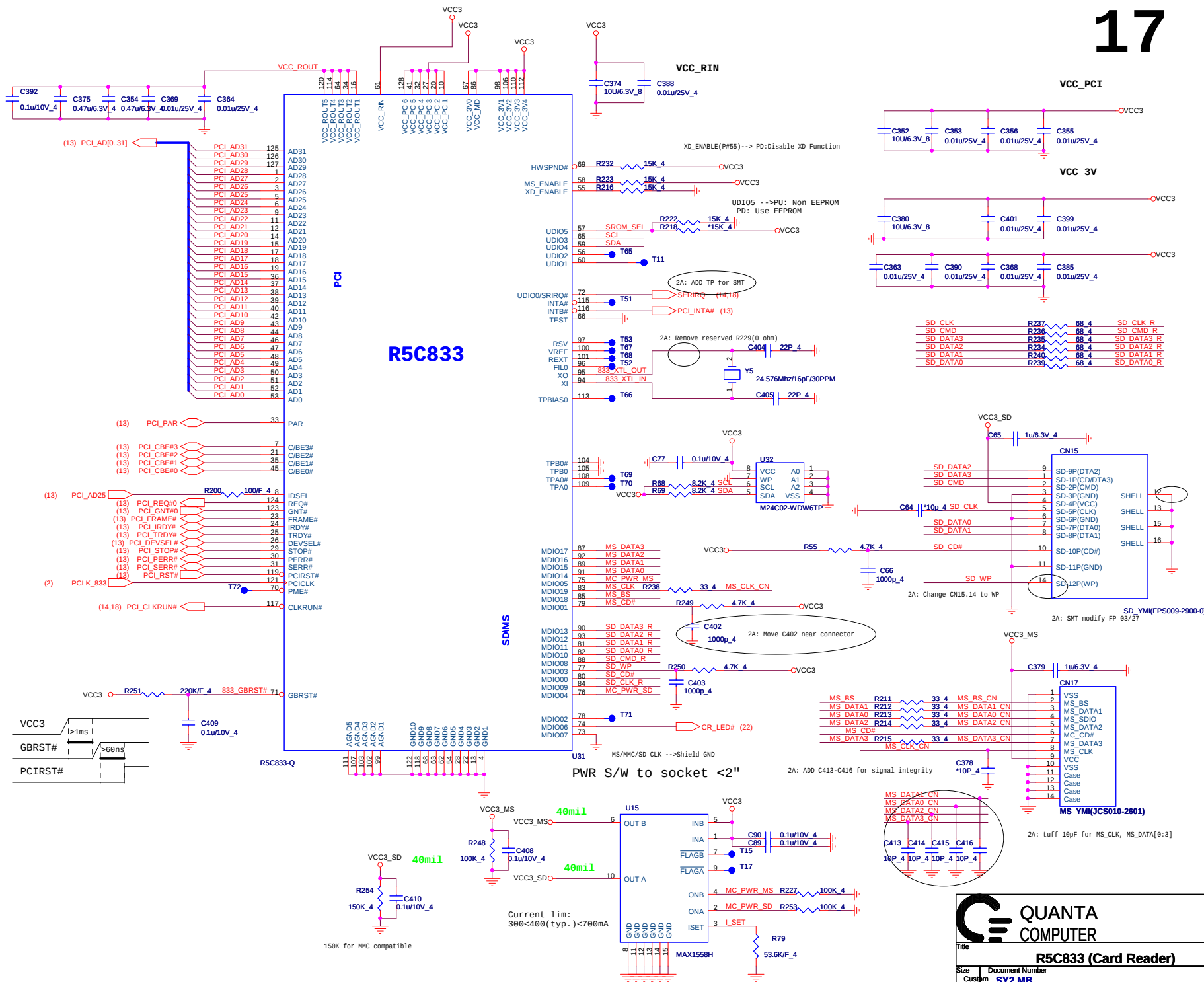


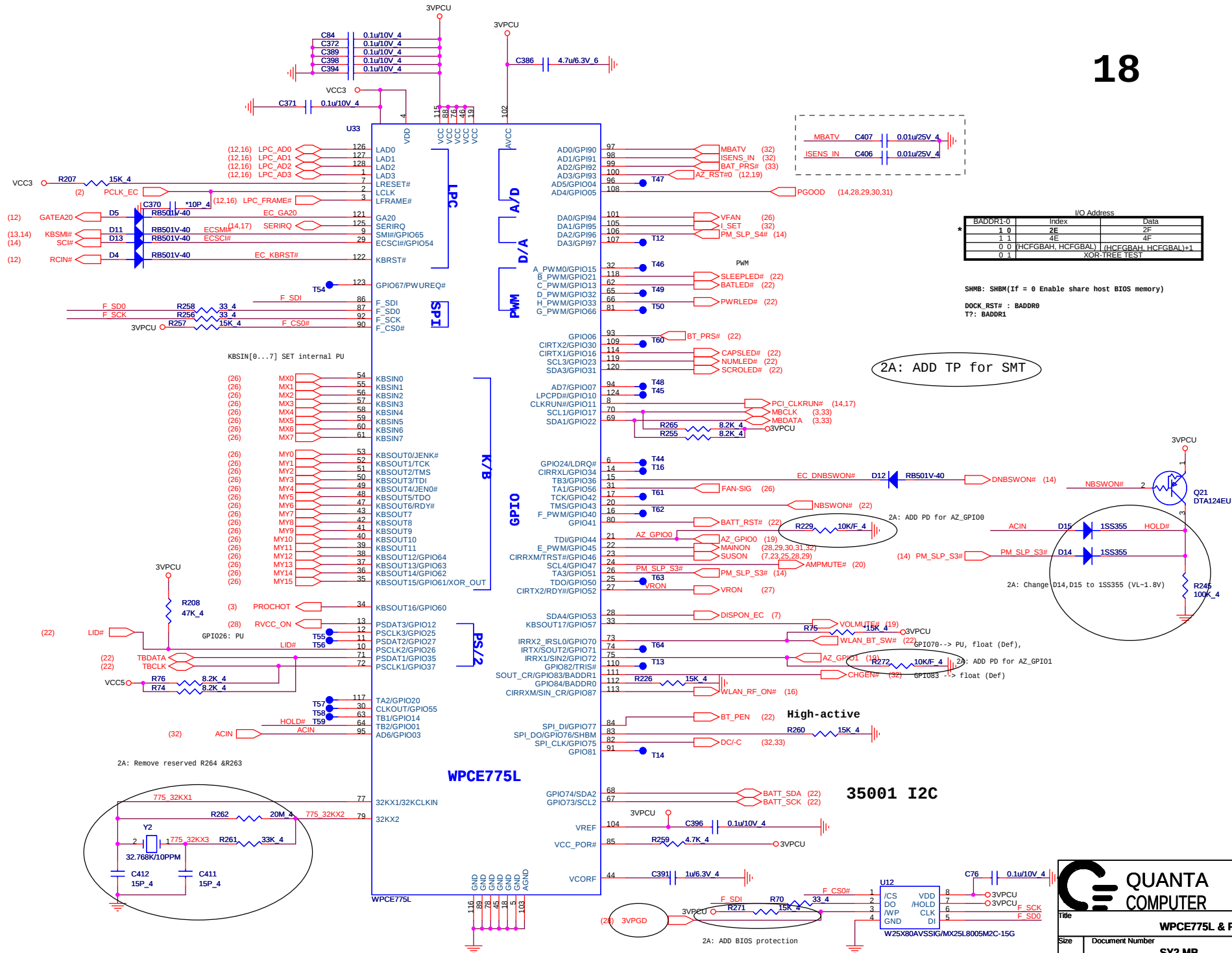
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

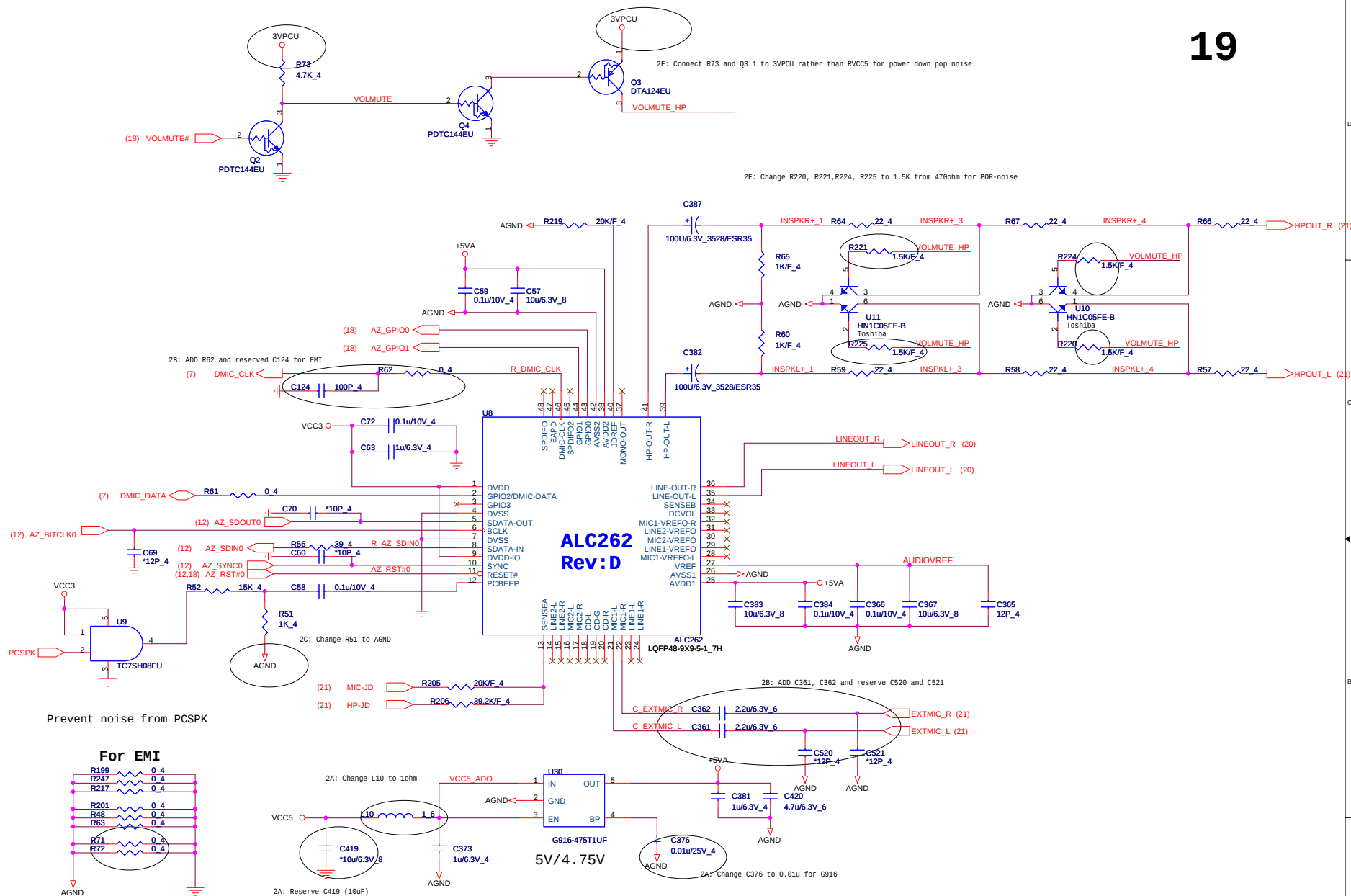
Wi-LAN ripple(3.3V, 1.5V) <100mV

Wi-LAN ripple(3.3V, 1.5V) <100mV

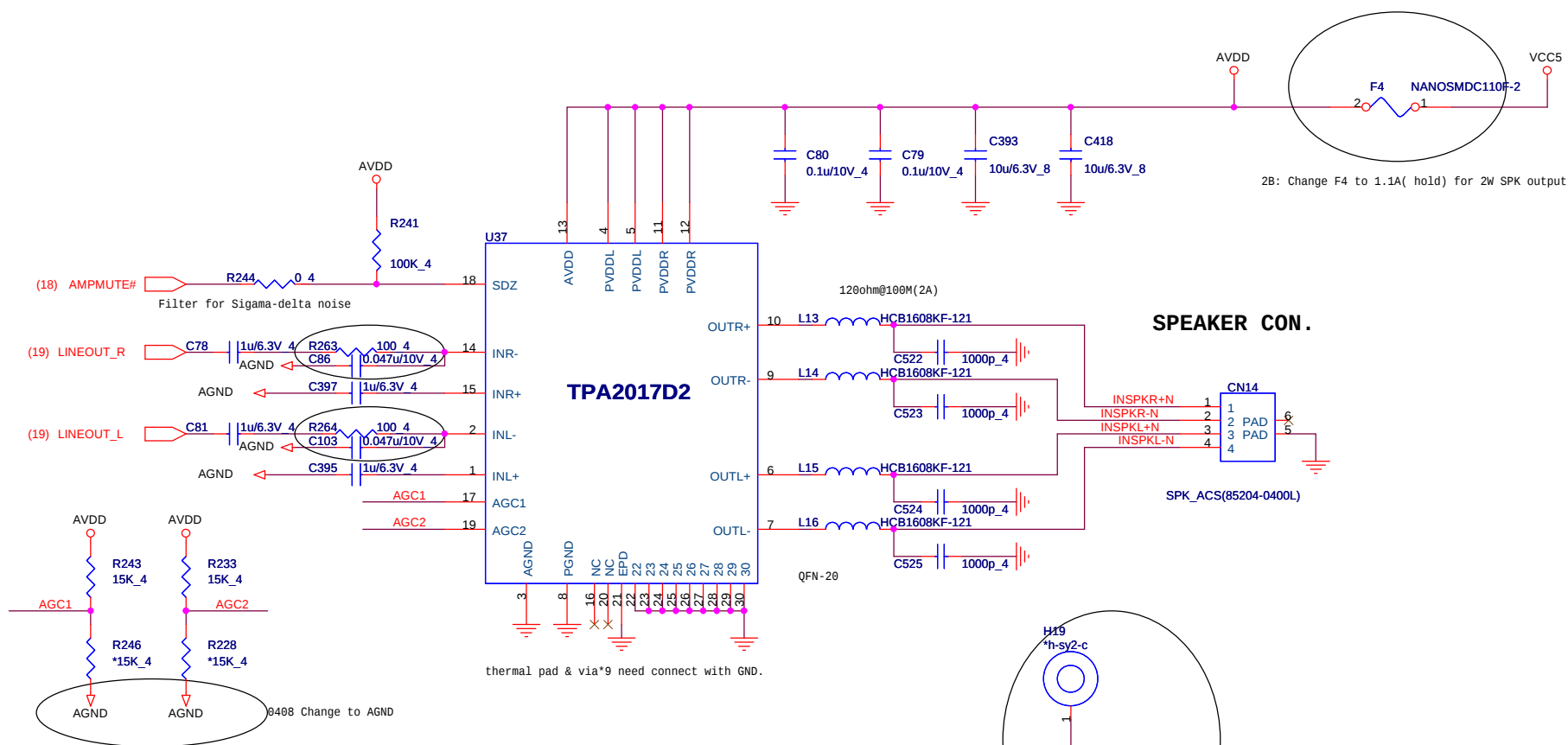








2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

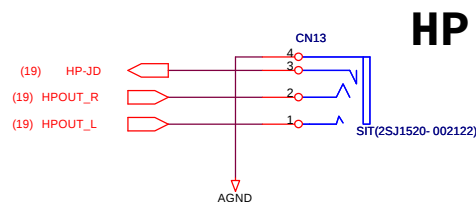
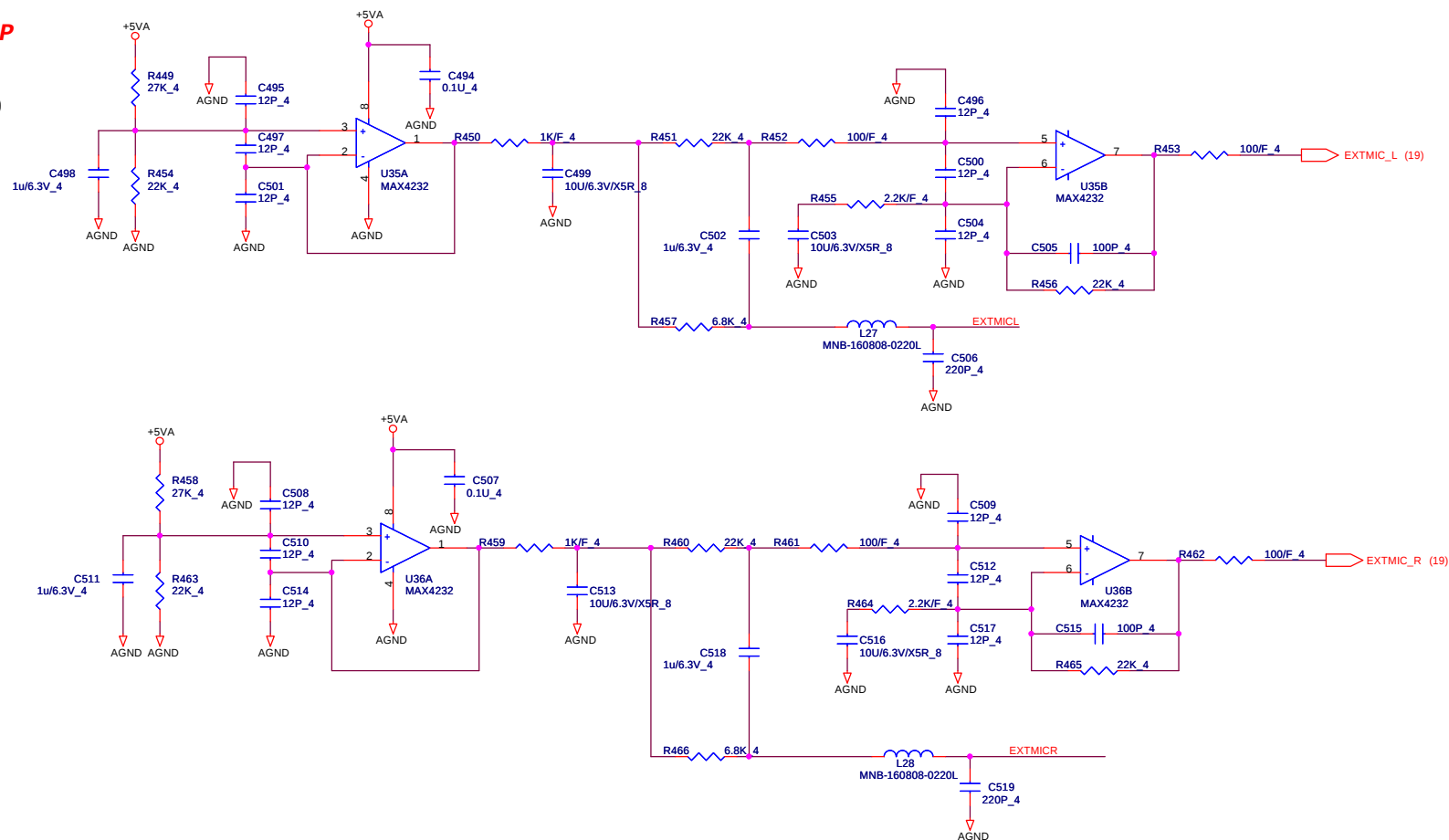


AGC1	AGC2	Function
0	0	AGC Function Disable
0	1	AGC, LIMITER Function Enable
1	0	AGC, LIMITER, Compression Function Enable
1	1	AGC, LIMITER, Compression and Noise Gate Function Enable

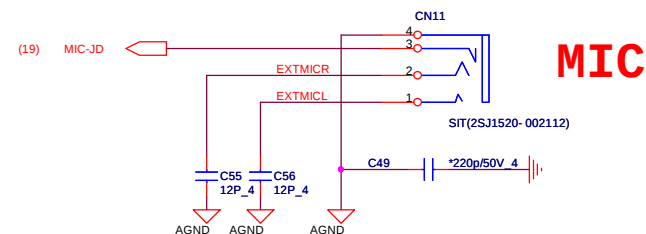
1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

MIC Pre-AMP

2A: Change MIC- AMP circuit

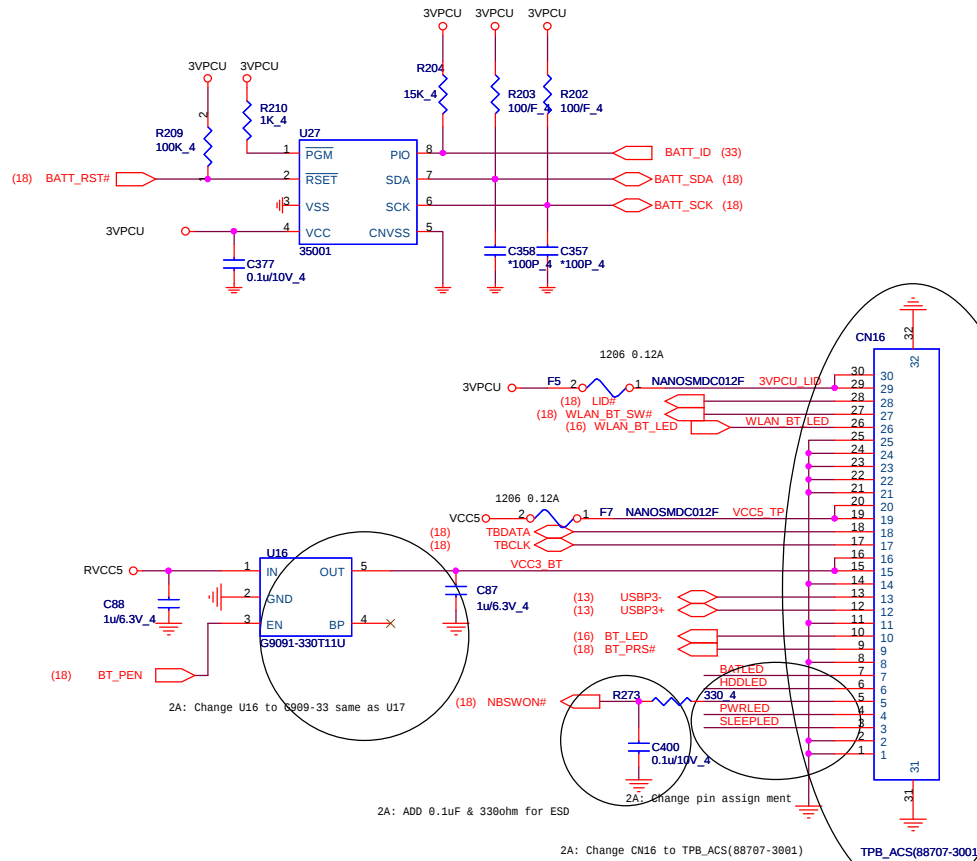


HP



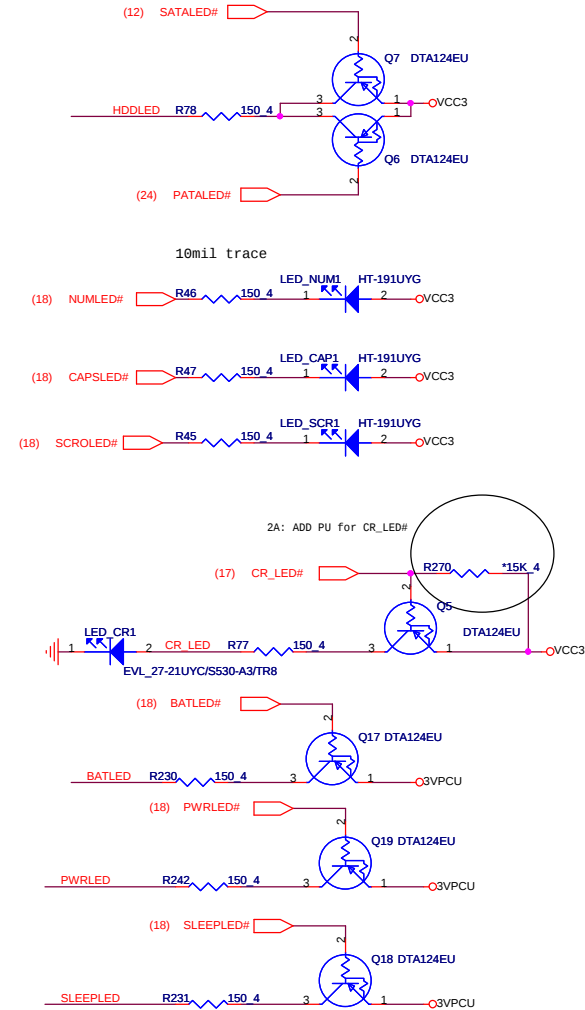
MIC

QUANTA COMPUTER			
File			
AUDIO JACK & MIC PRE-AMP			
Size Custom	Document Number SY2 MB	Rev 2C	
Date: Friday, April 10, 2009		Sheet 21	of 36



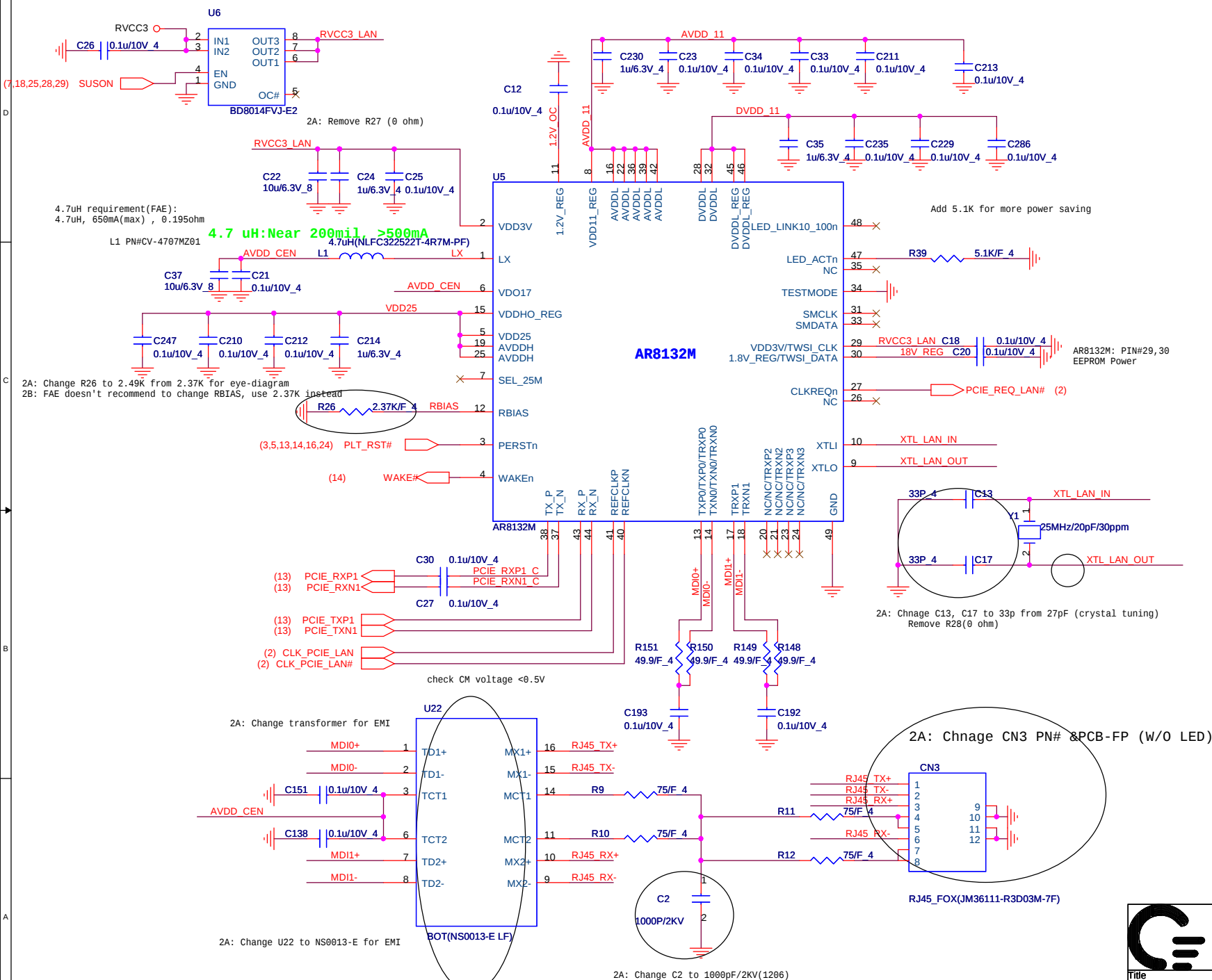
"Power, S0 (green), S3 (Umber flash), S4 (off), S5 (off)
 "Charger status in Umber color, Charge (on), Error (flash quickly)
 "HDD status, LED in yellow color
 "Caps Lock/Num Lock/Scroll Lock in green color
 "Wireless status in green color
 "Memory Stick Duo/SD Card status in yellow color
 "Camera status in green color (on Camera module)

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



QUANTA
COMPUTER

Title		
35001/LED/Button/TP/BT		
Size	Document Number	Rev
Custom	SY2 MB	2C
Date:	Friday, April 10, 2009	Sheet 22 of 36



1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 QUANTA COMPUTER			
Title LAN AR8132M			
Size Custom	Document Number SY2 MB	Rev 2C	
Date: Friday, April 10, 2009	Sheet	23	of 36

24



Size	Document Number
Custom	SY2 MB

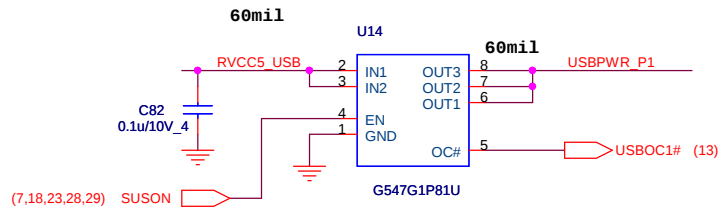
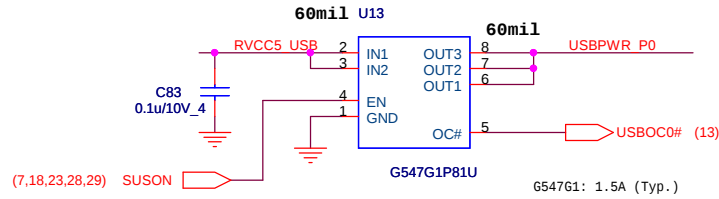
Date: Friday, April 10, 2009

Sheet 24 of 36

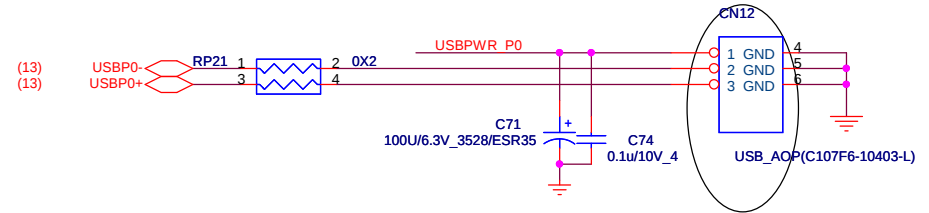
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

USB Power and Over current

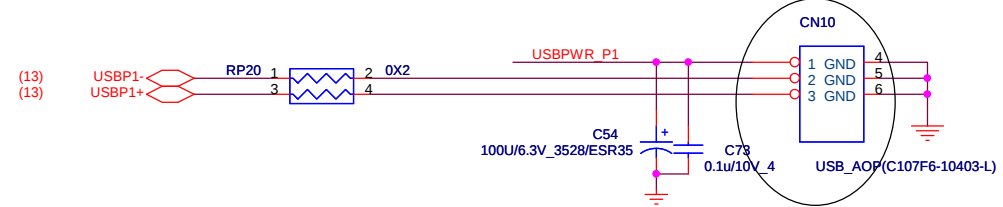
Current limit =1.5~2A



USB Connector



2A: Change CN10, CN12 PN# (gray color)

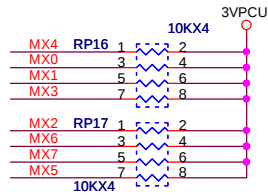


- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

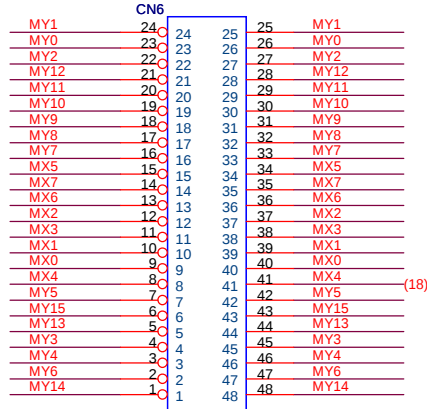
		QUANTA COMPUTER	
Title USB			
Size Custom	Document Number SY2 MB		Rev 2C
Date: Friday, April 10, 2009		Sheet 25 of 36	

INT. KEYBOARD

26

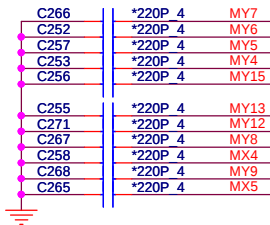
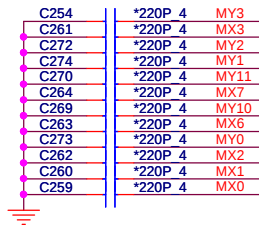


MX[0..7] >> MX[0..7] (18)
MY[0..15] >> MY[0..15] (18)

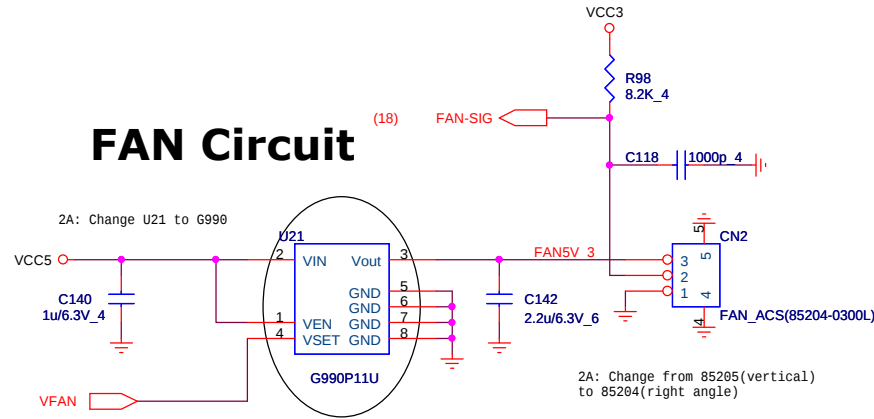


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check internal PU

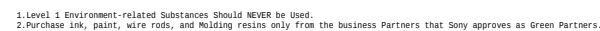


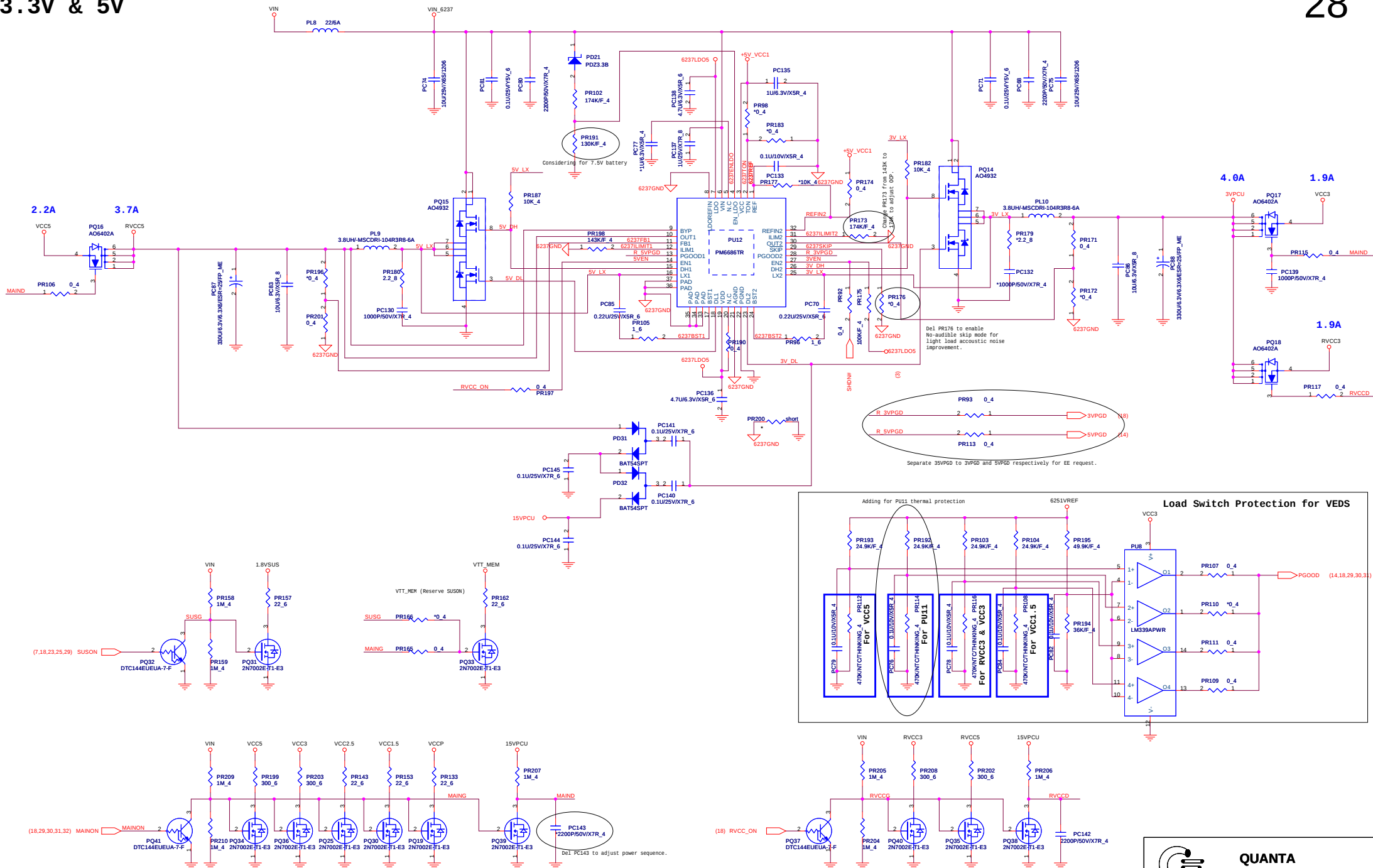
FAN Circuit



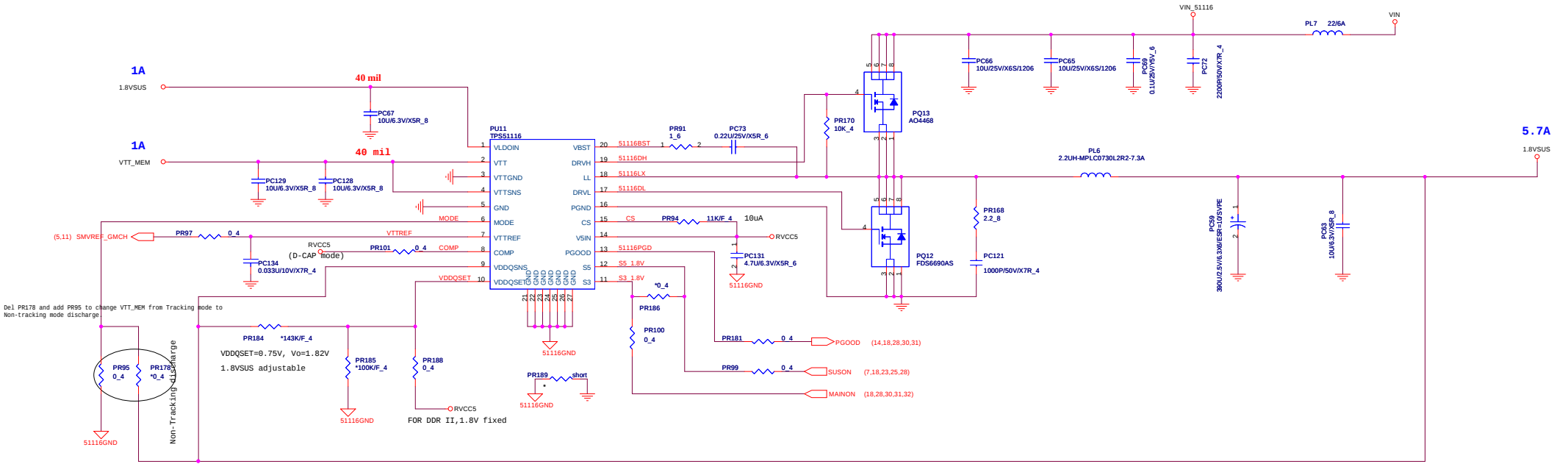
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K/B, FAN, T/P			
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1.Level 1 Environment-related Substances Should NEVER be Used.
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1.8VSUS & VTT_MEM

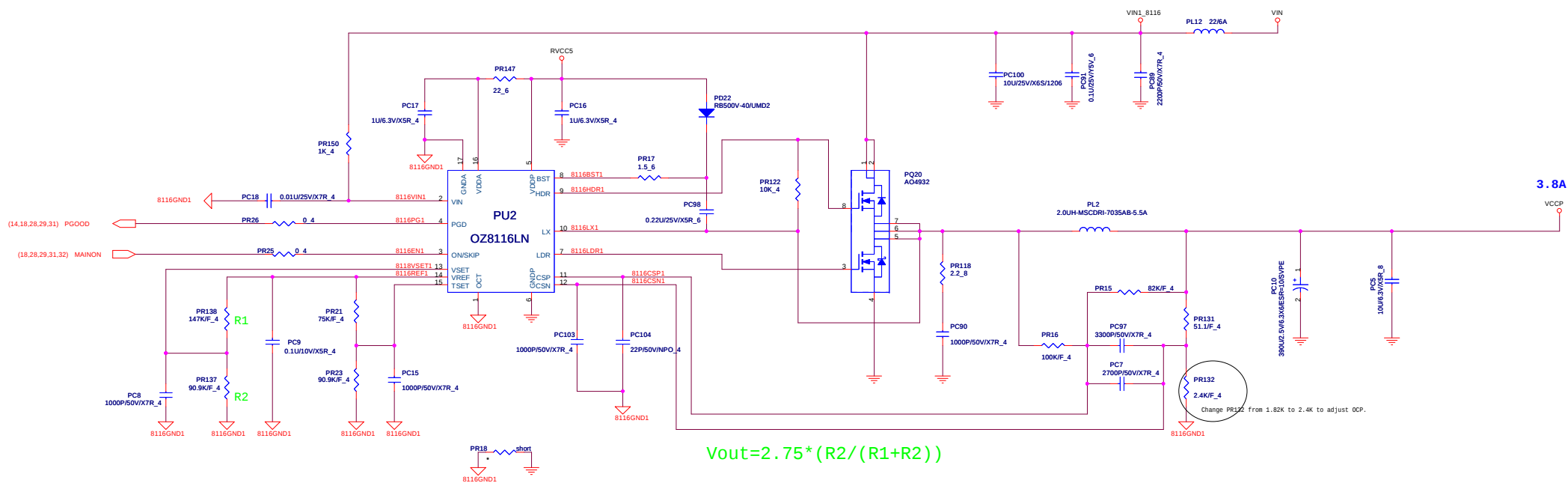


MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.6V<VDDQ<3V

VTT = VTTREF = VDDQSNS/2 = 0.9V

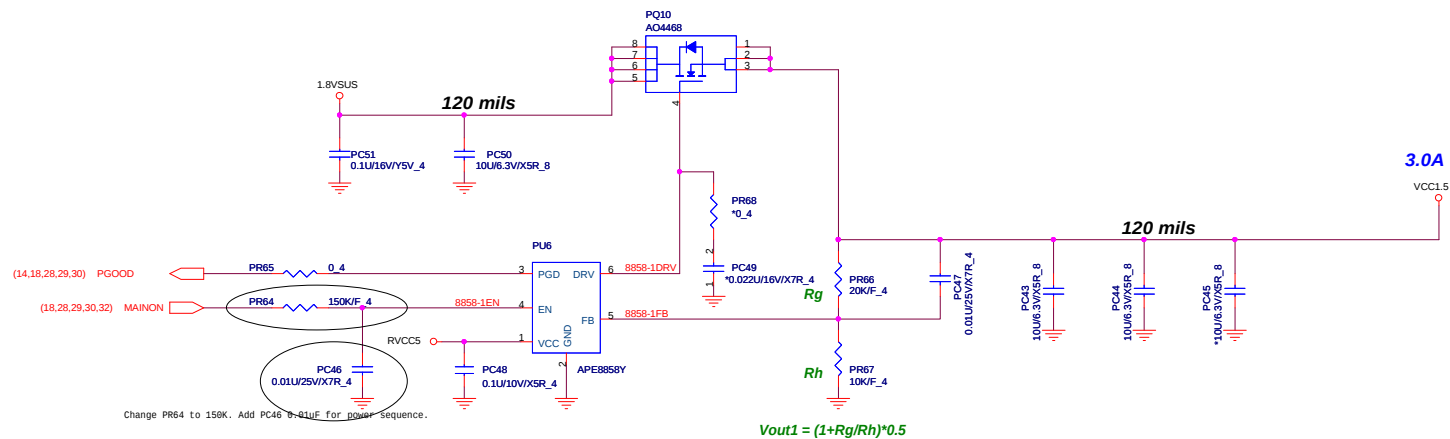
STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off



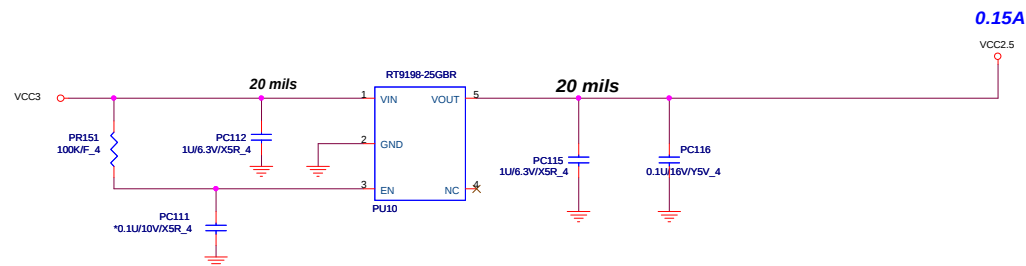
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VCC1.5

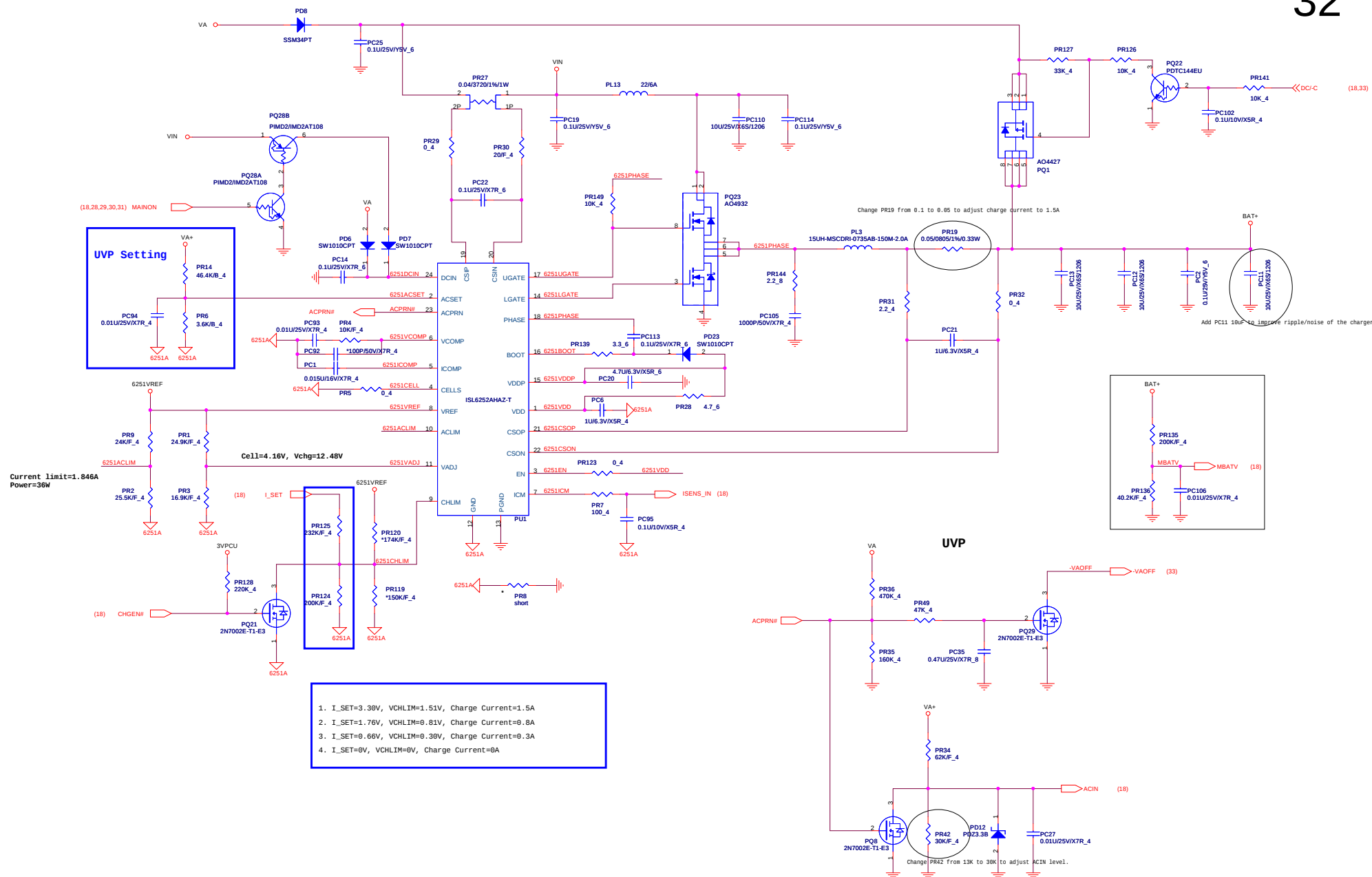
31



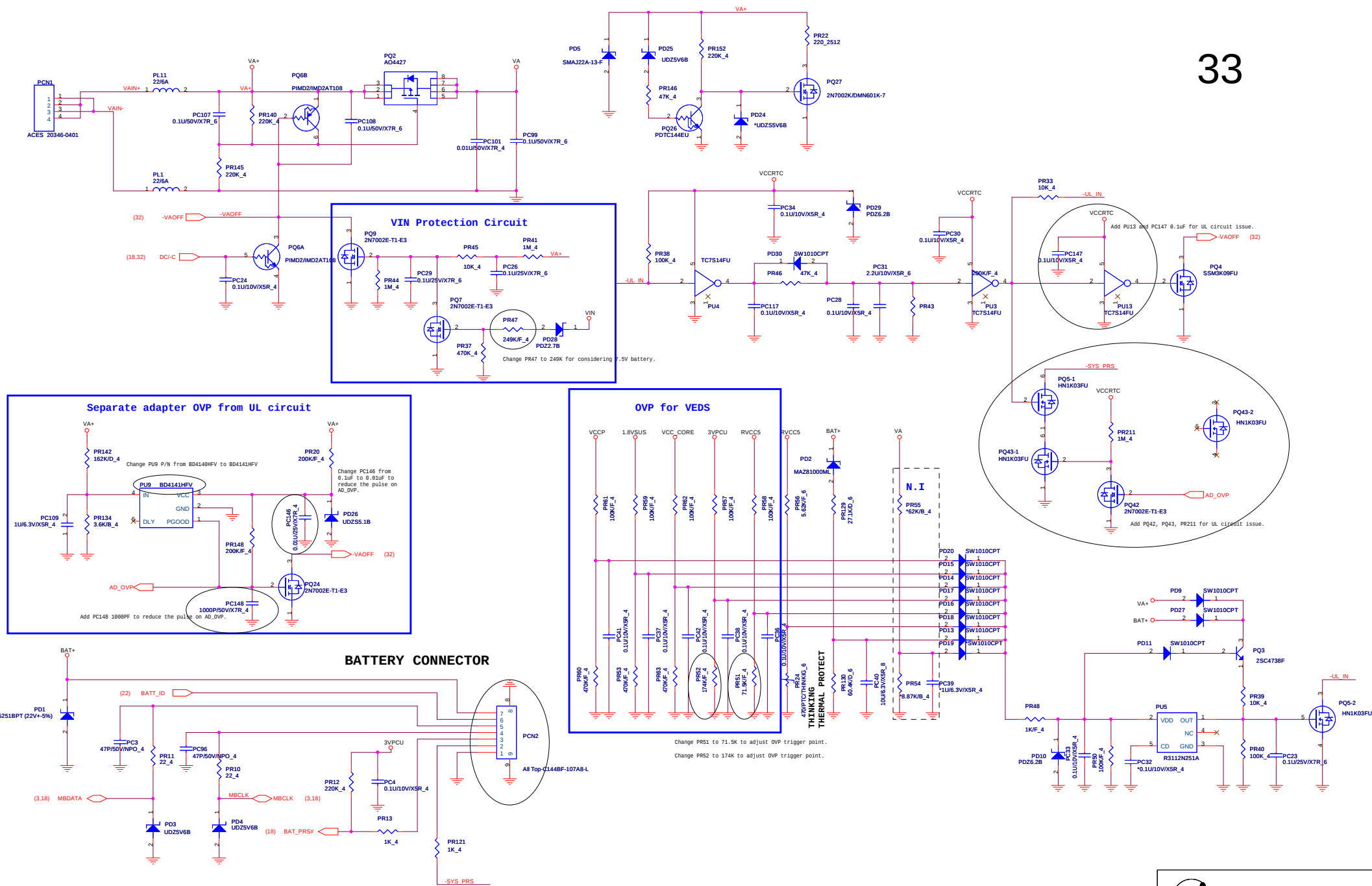
VCC2.5



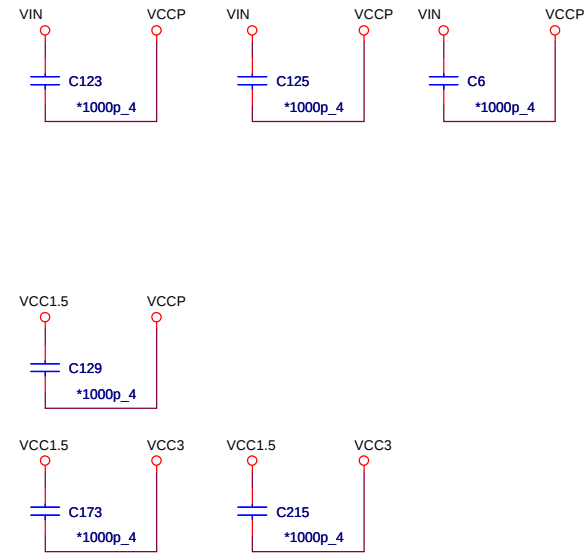
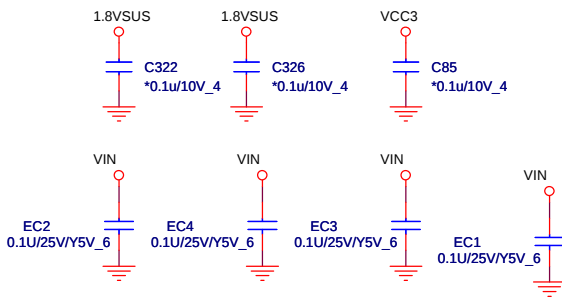
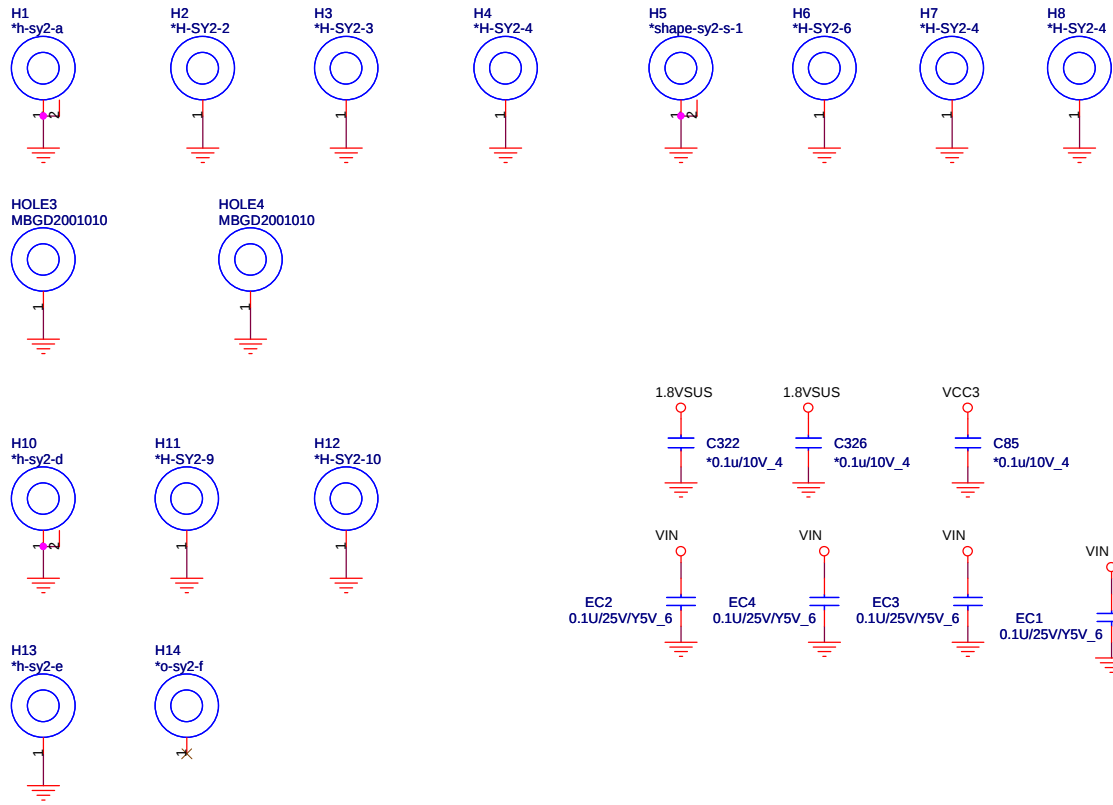
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2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



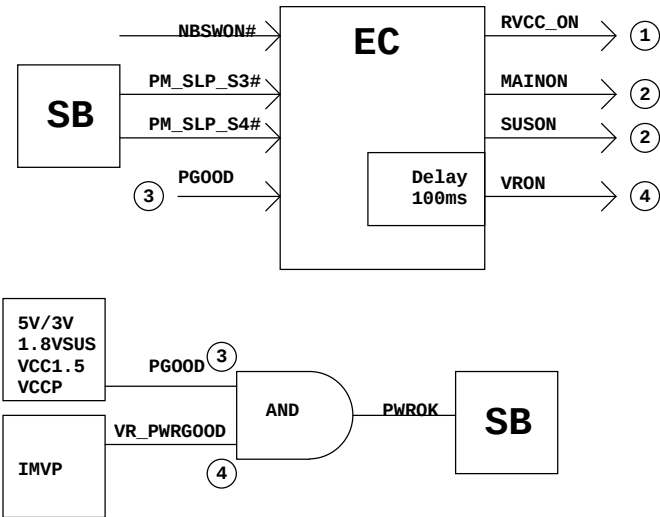
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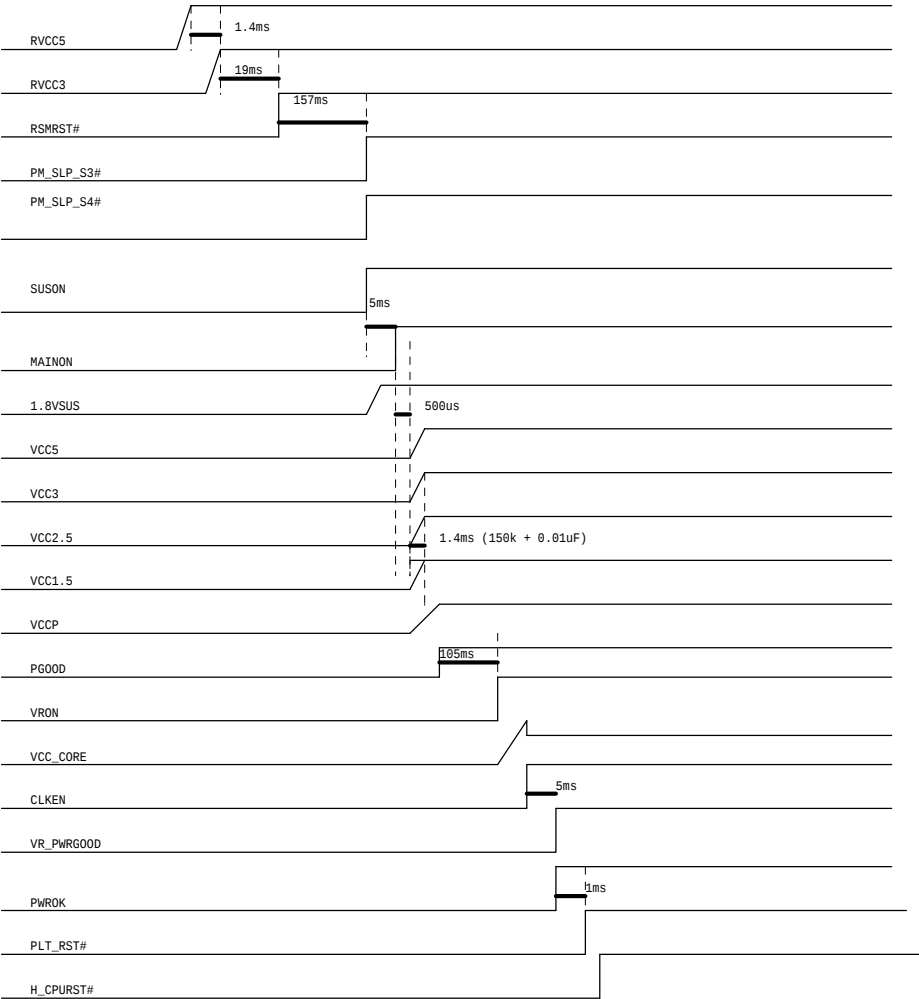
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SY2 Power-up Block



Power State Table											
AC Mode	S0	S3	S4	S5	BATT	S0	S3	S4	S5		
6237LD05	ON	ON	ON	ON	6237LD05	ON	ON	ON	ON		
3VPCU	ON	ON	ON	ON	3VPCU	ON	ON	ON	ON		
RVCC5	ON	ON	ON	OFF	RVCC5	ON	ON	OFF	OFF		
RVCC3	ON	ON	ON	OFF	RVCC3	ON	ON	OFF	OFF		
1.8VSUS	ON	ON	OFF	OFF	1.8VSUS	ON	ON	OFF	OFF		
VCC5	ON	OFF	OFF	OFF	VCC5	ON	OFF	OFF	OFF		
VCC3	ON	OFF	OFF	OFF	VCC3	ON	OFF	OFF	OFF		
VCC2.5	ON	OFF	OFF	OFF	VCC2.5	ON	OFF	OFF	OFF		
VCCP	ON	OFF	OFF	OFF	VCCP	ON	OFF	OFF	OFF		
VCC_CORE	ON	OFF	OFF	OFF	VCC_CORE	ON	OFF	OFF	OFF		

SY2 Power-up Sequencing



1219:(1A)
First release

1231:(1B)
-P.2
Modify CLK_FSC, CLK_FSB strapping circuit to CLK-GEN
Change PCI CLK damping to 22ohm (impedance matching)
-P.9
Reserve one 220uF for 1.8VSUS to 945GSE
-P.10
Change CRT-SCK, CRT-SDA PU to 2.2K for compatibility
Change DDC2BC, DDC2BD PU to 3.9K for compatibility
Change VCC5CRT circuit using fuse and Schottky
-P.14
Modify RSMRST# buffer circuit
-P.17
Change R5C833 GBRST# circuit
-P.20
Reserve 0 ohm to AMP R/L_in
Change AMP to APA2031
-P.21
Change fuse to 0.12A for Hall sensor
Change fuse to 0.12A for TP/B

0114(1C):
-P.7
Change CAMERA LDO to APL5151
-P.10
Change power of VCC_SYNC to VCC5CRT
Tie VGA CN#10 to GND
-P.14
ADD PU/PD for GPIO (default input)
-P.16
NC WL-LAN WAKE# PIN#
Change WLAN_BT_LED circuit
-P.17
STUFF 1000p_4 for MS:CD#, SD: CD#, WP
Change MS/SD Power S/W to MAX1558H
-P.19
Connect Codec GPIO1 to EC for AMP standby
Change +5VA LDO to APL5151 for better PSRR

0119(1D)
-P.2
Reserve damping resistor for crystal
-P.10
Remove CRT PnP
-P.18
Remove CRTSENSE# to disable CRT PnP
Change AMPMUT# to PIN#24(OD type)
-P.21
Change BT PWR S/W to LDO
-P.32
Separate adapter OVP from UL circuit

0202(1E)
-P.7
Change CAMERA LDO to G909-330T1U(current limit>150mA)
Change LVDS PWR S/W to G5243A
-P.14
PU "ICH_RI#" to RVCC3
-P.17
Change R5C833 INTERRUPT to INTB#
-P.21
Move CR LED to MB from TP/B

0325(2A)
-P.2
Remove reserved 0ohm (R95,R106,R105)
-P7
Change C96 to 1uF for abnormal operation
Reserve L11 and C126 for EMI
-P9
Remove reserved L3-6, C3
Remove unnecessary C105
-P10
Change F3 to 0.25A ((hold)
Change CN7 PCB-FP
-P14
Change R168 to 332K (delay time-22ms)
Remove reserved SUSCLK
-P15
Remove reserved L2
-P16
Change D10 to R8501V-40
Remove reserved R125(0 ohm)
-P17
ADD C413-C416 for signal integrity
Change CN15.14 to WP (mistake)
Remove reserved R229 (0 ohm)
Move C402 near CN17
-P18
ADD BIOS protection circuit to
ADD PD for AZ_GPIO0 and AZ_GPIO1
Change D14,D15 to 1S355 (VL-1.8V)
Remove reserved R263, R264
-P19
ADD L12 and reserved C124 for EMI
Change C376 to 0.01uF for G916
Change L10 to 1ohm
Add reserved C419 (10uF) for VCC5
-P20
Change C78,C81, C395, C397 to 0.47uF
for better Low freq response.
-P21
Change MIC- PREAMP circuit
-P22
Change U16 to G909-33 same as U17
ADD R237 and C400 for ESD
-P23
Change R26 to 2.49K for better PCIE eye
Change U6 to BD8014
Remove reserved R27 (0ohm)
Change C13 and C17 to 33pF (crystal tuning)
Change C2 to 1000p/2KV (1206 size)
Change U22 to NS013-E for EMI
-P24
Change F2 to 0.5A(Hold)
-P26
Change U21 to GMT G990
-P28
Remove PC143 for power up sequence
-P29
Mount PR96 and un-stuff PR178 for discharge mode
-P31
Cange PR64/PC46 to 150K/ 0.1u for power up sequence

0403 (2B)
-P4
Remove reserved C5
-P7
Change CN1 pin definition
-P12
Reserve R27 (0 ohm)
-P19
ADD C124 with 100pF for DMIC_CLK
ADD C361, C362 and reserve C520 and C521
-P20
Change F4 to 1.1A(hold) for 2W SPK
Change U34(AMP) to TPA2016D2
-P24
Change SSD FFC CNN to easy on type.
-P.27
Remove jumper PG3.
Remove PC55 due to PC55 is reserved only.
-P.28
Remove jumper PG5, PG6
Change PR173 from 143K to 174K to adjust OCP.
Del PR176 to enable No-audible skip mode for light load accoustic
noise improvement.
Del PC143 to adjust power sequence.
Separate 35VPGD to 3VPGD and 5VPGD respectively for EE request.
-P.29
Remove jumper PG4, PG8.
Del PR178 and add PR95 to change VTT_MEM from Tracking mode to
Non-tracking mode discharge.
-P.30
Remove jumper PG1.
Change PR132 from 1.82K to 2.4K to adjust OCP.
-P.31
Remove jumper PG2, PG7.
Change PR64 to 150K. Add PC46 0.01uF for power sequence.
-P.32
Change PR19 from 0.1 to 0.05 to adjust charge current to 1.5A
Add PC11 10uF to improve ripple/noise of the charger.
Change PR42 from 13K to 30K to adjust ACIN level.
-P.33
Add PU13 and PC147 0.1uF for UL circuit issue.
Add PC149 1000PF to reduce the pulse on AD_OVP.
Change PC146 from 0.1uF to 0.01uF to reduce the pulse on AD_OVP.
Add PQ42, PQ43, PR211 for UL circuit issue.
Change PU9 P/N from BD4140HFV to BD4141HFV due to supplier change its
P/N.

0406A(2C)
-P.7
Change U17 to MAX4789
-P.9
Reserve L4,L5,L6
-P.15
Reserve L2
-P.19
Change R51 to connect AGND
-P.20
Change AMP(U37) to TPA2017D2
-P35
Update Power up sequence

0409 (2E)
-P.19
Connect R73 and Q3.1 to 3VPCU rather than RVCC5 for power down pop noise.
Change R220, R221,R224, R225 to 1.5K from 470ohm for POP-noise

0409 (2F)
-P.28
Add PR192, PR114, PC76 for PU11 thermal protection.
Change PR191 to 130K for considering 7.5V battery.

0408 (2D)
-P.27
Add PC149, PC150 to improve accoustic noise.
-P.33
Change PR47 to 249K for considering 7.5V battery.
Change PR51 to 71.5K to adjust OVP trigger point.
Change PR52 to 174K to adjust OVP trigger point.

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