MODEL NAME : *QBR00*
PCB NO : *LA-8341P*
BOM P/N : *TBD*

Compal Confidential

Voyager MLK

Schematic Document

Rev: A00

2012-02-16

@ : Nopop Component

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Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: LA-8341P	Rev: 1.0
Date: Friday, March 02, 2012	Sheet 1 of 71	

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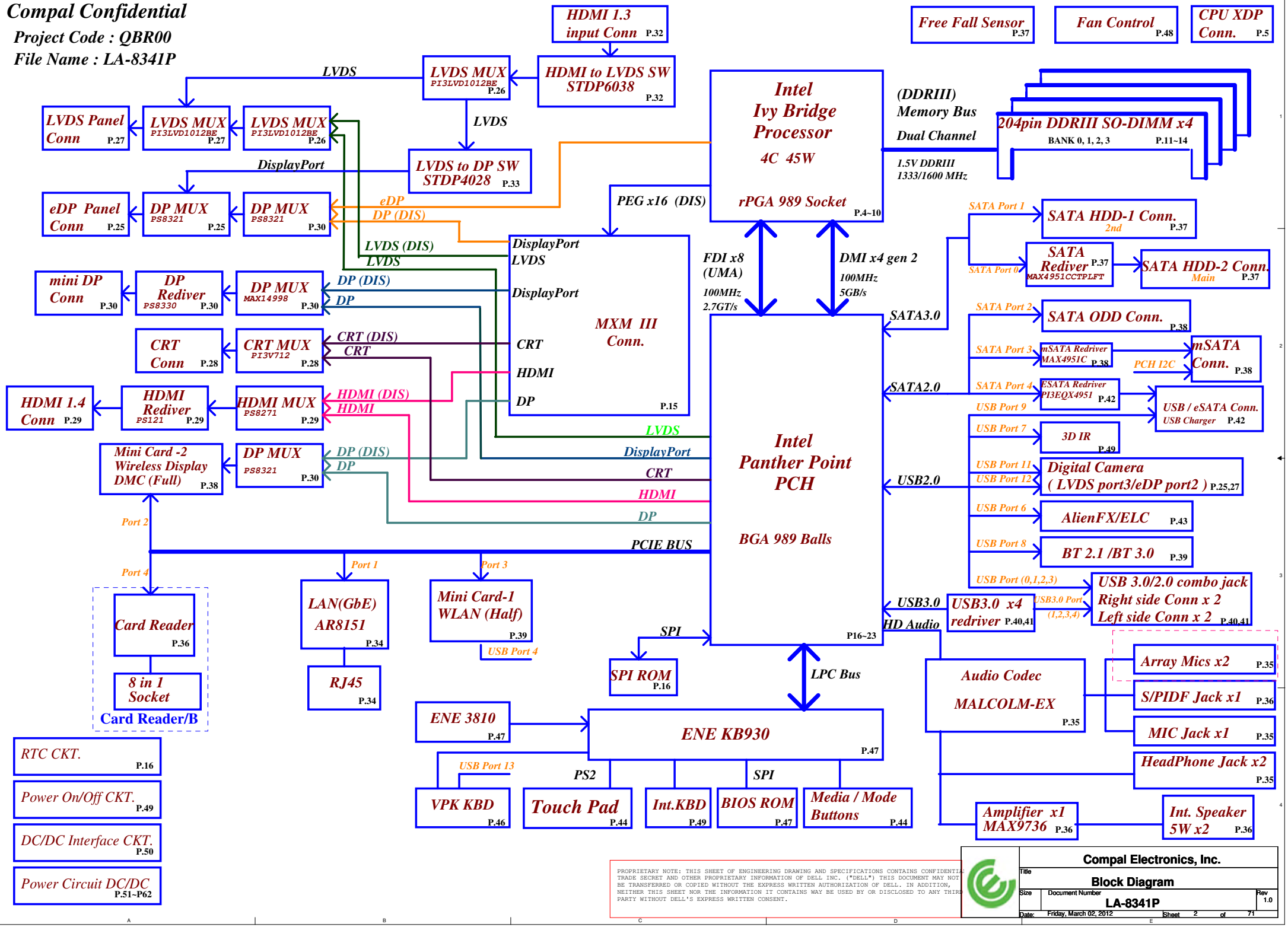
Project Code : QBR00

File Name : LA-8341P



Compal Electronics, Inc.

Title: Block Diagram

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 2 of 71

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (Pre-ST)
3	0.4 (ST)
4	1.0 (QT)
5	
6	
7	

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Symbol Note :

: means Digital Ground

: means Analog Ground

PM TABLE

power plane / State	+5VALW +3VALW +3VLP +3V_PCH	+1.5V	+5VS +3VS +1.8VS +1.5VS +0.75VS +3VMXM +5VMXM +VCCP +VCCSA +VCC_CORE +1.5V_CPU_VDDQ
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

USB 2.0

USB PORT#	DESTINATION
0	JUSB1(USB3.0 P1)
1	JUSB2(USB3.0 P2)
2	JUSB3(USB3.0 P3)
3	JUSB4(USB3.0 P4)
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	JESATA
7	IR SENSOR
8	Bluetooth
9	AlienFX/ELC
10	None
11	eDP CAMERA
12	LVDS CAMERA
13	VPK K/B

CLK

DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLKOUT_PCIE0	None	CLKOUTFLEX0	None
CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
CLKOUT_PCIE2	MINI CARD-2 DMC	CLKOUTFLEX2	None
CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
CLKOUT_PCIE4	CARD READER		
CLKOUT_PCIE5	None		
CLKOUT_PCIE6	None		
CLKOUT_PCIE7	None		
CLKOUT_PEG_A	MXM		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

Power plane	Voltage
+3VALW +3V_PCH +3VS +3VMXM	3.3V

SATA	DESTINATION
SATA0	HDD2
SATA1	HDD1
SATA2	ODD
SATA3	mSATA
SATA4	ESATA
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

10,

Connector Location	Source	Strap pin setting								
JUSB1	1st PERICOM	U628 PI3EQX7502 X76_Pericom@ SA000056E0L	R12 4.7K_0402_5%~D @	R53 4.7K_0402_5%~D X76_Pericom@	R25 4.7K_0402_5%~D @	R49 4.7K_0402_5%~D X76_Pericom@	R337 4.7K_0402_5%~D @	R413 4.7K_0402_5%~D @	R412 4.7K_0402_5%~D @	R1828 3.3K_0402_5% X76_Pericom@
	2nd PARADE	U628 PS8710B X76_Parade@ SA00004VQ00	R12 4.7K_0402_5%~D X76_Parade@	R53 4.7K_0402_5%~D @	R25 4.7K_0402_5%~D X76_Parade@	R49 4.7K_0402_5%~D @	R337 4.7K_0402_5%~D @	R413 4.7K_0402_5%~D @	R412 4.7K_0402_5%~D @	R1828 3.3K_0402_5% X76_Parade@
	3rd ASMedia	U628 ASM1464 X76_Asmedia@ SA000054400	R12 4.7K_0402_5%~D @	R53 4.7K_0402_5%~D @	R25 4.7K_0402_5%~D @	R49 4.7K_0402_5%~D @	R337 2K_0402_5%~D X76_Asmedia@	R413 0_0402_5%~D X76_Asmedia@	R412 0_0402_5%~D X76_Asmedia@	R1828 4.7K_0402_5%~D @

Connector Location	Source	Strap pin setting								
JUSB2	1st PERICOM	U629 PI3EQX7502 X76_Pericom@ SA000056E0L	R47 4.7K_0402_5%~D @	R81 4.7K_0402_5%~D X76_Pericom@	R46 4.7K_0402_5%~D @	R67 4.7K_0402_5%~D X76_Pericom@	R314 4.7K_0402_5%~D @	R415 4.7K_0402_5%~D @	R414 4.7K_0402_5%~D @	R1833 3.3K_0402_5% X76_Pericom@
	2nd PARADE	U629 PS8710B X76_Parade@ SA00004VQ00	R47 4.7K_0402_5%~D X76_Parade@	R81 4.7K_0402_5%~D @	R46 4.7K_0402_5%~D X76_Parade@	R67 4.7K_0402_5%~D @	R314 4.7K_0402_5%~D @	R415 4.7K_0402_5%~D @	R414 4.7K_0402_5%~D @	R1833 3.3K_0402_5% X76_Parade@
	3rd ASMedia	U629 ASM1464 X76_Asmedia@ SA000054400	R47 4.7K_0402_5%~D @	R81 4.7K_0402_5%~D @	R46 4.7K_0402_5%~D @	R67 4.7K_0402_5%~D @	R314 2K_0402_5%~D X76_Asmedia@	R415 0_0402_5%~D X76_Asmedia@	R414 0_0402_5%~D X76_Asmedia@	R1833 4.7K_0402_5%~D @

Connector Location	Source	Strap pin setting								
JUSB3	1st PERICOM	U630 PI3EQX7502 X76_Pericom@ SA000056E0L	R192 4.7K_0402_5%~D @	R120 4.7K_0402_5%~D X76_Pericom@	R187 4.7K_0402_5%~D @	R105 4.7K_0402_5%~D X76_Pericom@	R343 4.7K_0402_5%~D @	R420 4.7K_0402_5%~D @	R419 4.7K_0402_5%~D @	R1834 3.3K_0402_5% X76_Pericom@
	2nd PARADE	U630 PS8710B X76_Parade@ SA00004VQ00	R192 4.7K_0402_5%~D X76_Parade@	R120 4.7K_0402_5%~D @	R187 4.7K_0402_5%~D X76_Parade@	R105 4.7K_0402_5%~D @	R343 4.7K_0402_5%~D @	R420 4.7K_0402_5%~D @	R419 4.7K_0402_5%~D @	R1834 3.3K_0402_5% X76_Parade@
	3rd ASMedia	U630 ASM1464 X76_Asmedia@ SA000054400	R192 4.7K_0402_5%~D @	R120 4.7K_0402_5%~D @	R187 4.7K_0402_5%~D @	R105 4.7K_0402_5%~D @	R343 2K_0402_5%~D X76_Asmedia@	R420 0_0402_5%~D X76_Asmedia@	R419 0_0402_5%~D X76_Asmedia@	R1834 4.7K_0402_5%~D @

Connector Location	Source	Strap pin setting								
JUSB4	1st PERICOM	U631 PI3EQX7502 X76_Pericom@ SA000056E0L	R197 4.7K_0402_5%~D @	R183 4.7K_0402_5%~D X76_Pericom@	R196 4.7K_0402_5%~D @	R182 4.7K_0402_5%~D X76_Pericom@	R344 4.7K_0402_5%~D @	R424 4.7K_0402_5%~D @	R421 4.7K_0402_5%~D @	R1835 3.3K_0402_5% X76_Pericom@
	2nd PARADE	U631 PS8710B X76_Parade@ SA00004VQ00	R197 4.7K_0402_5%~D X76_Parade@	R183 4.7K_0402_5%~D @	R196 4.7K_0402_5%~D X76_Parade@	R182 4.7K_0402_5%~D @	R344 4.7K_0402_5%~D @	R424 4.7K_0402_5%~D @	R421 4.7K_0402_5%~D @	R1835 3.3K_0402_5% X76_Parade@
	3rd ASMedia	U631 ASM1464 X76_Asmedia@ SA000054400	R197 4.7K_0402_5%~D @	R183 4.7K_0402_5%~D @	R196 4.7K_0402_5%~D @	R182 4.7K_0402_5%~D @	R344 2K_0402_5%~D X76_Asmedia@	R424 0_0402_5%~D X76_Asmedia@	R421 0_0402_5%~D X76_Asmedia@	R1835 4.7K_0402_5%~D @

BOM Control	POP	NC
1st PERICOM	X76_Pericom@	@
2nd PARADE	X76_Parade@	@
3rd ASMedia	X76_Asmedia@	@

0224 note-
1, QT build only use Pericom.
2, Parade need to wait for the new revision.
3, Need to got DM permission, then can use Asmedia.

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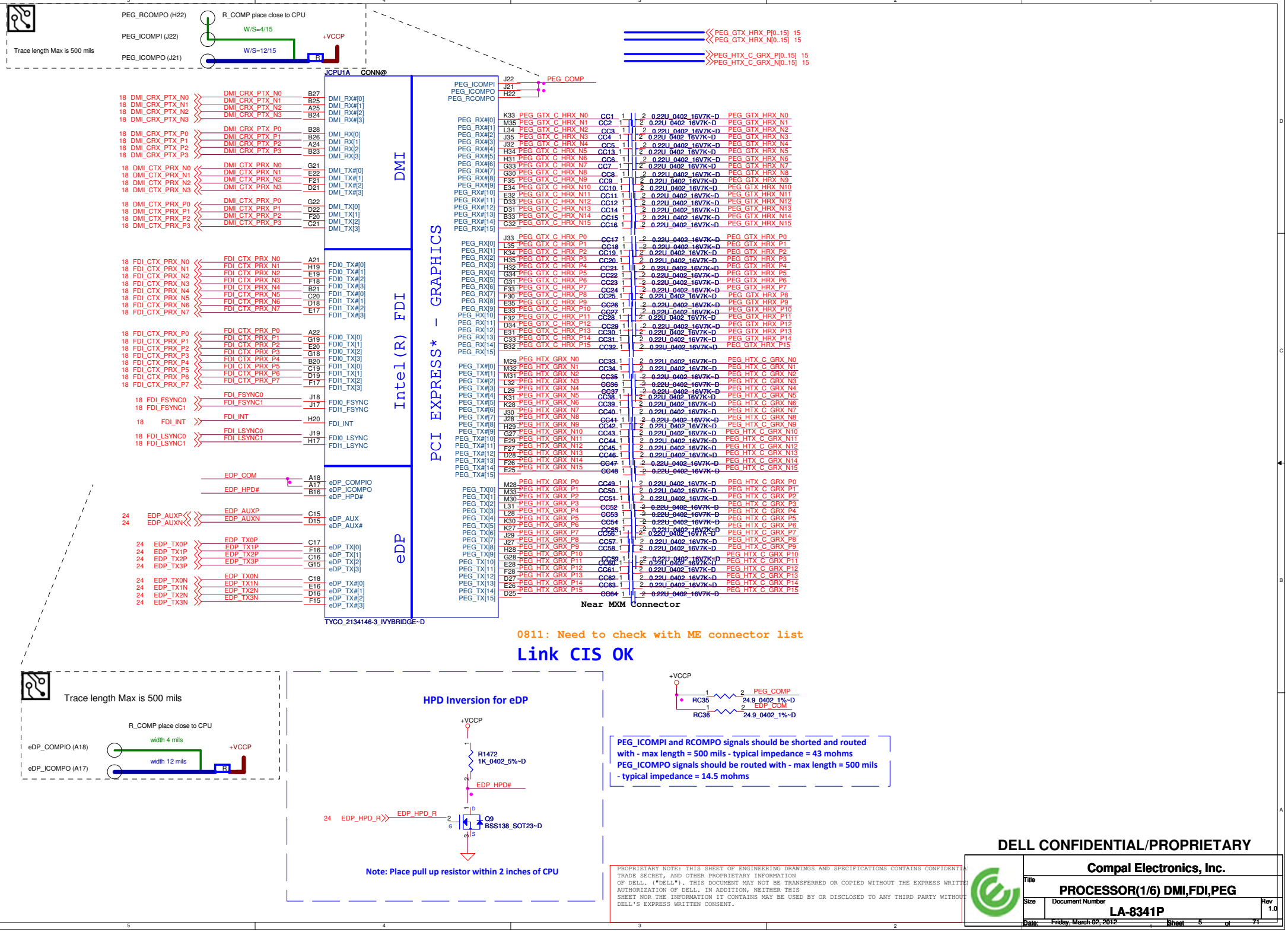
Title: USB3.0 Config setting

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 4 of 71



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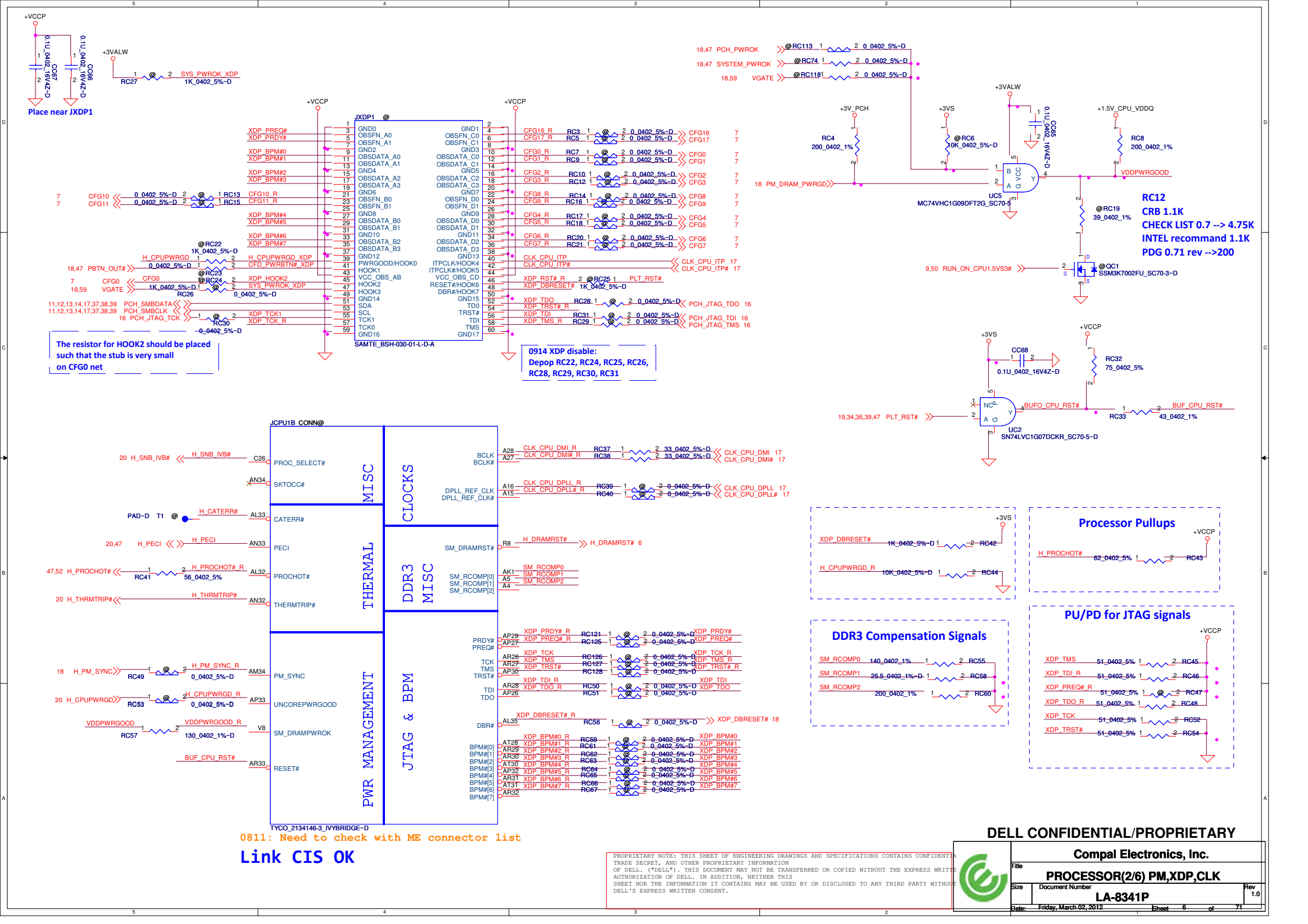
Title: PROCESSOR(1/6) DMI,FDI,PEG

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 5 of 71


Place near JXDP1
JXDP1 @
SAMTE_BSH-030-01-L-D-A
The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net
0914 XDP disable:
Depop RC22, RC24, RC25, RC26, RC28, RC29, RC30, RC31
RC12
CRB 1.1K
CHECK LIST 0.7 --> 4.75K
INTEL recommand 1.1K
PDG 0.71 rev -->200
UC5
MC74VHC1G09DFT2G_SC70-5
@QC1
SSM3K7002FU_SC70-3~D
UC2
SN74LVC1G07DCKR_SC70-5~D
JCPU1B_CONN@
TYCO_2134146-3_IVYBRIDGE~D
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
Processor Pullups
DDR3 Compensation Signals
PU/PD for JTAG signals
0811: Need to check with ME connector list
Link CIS OK
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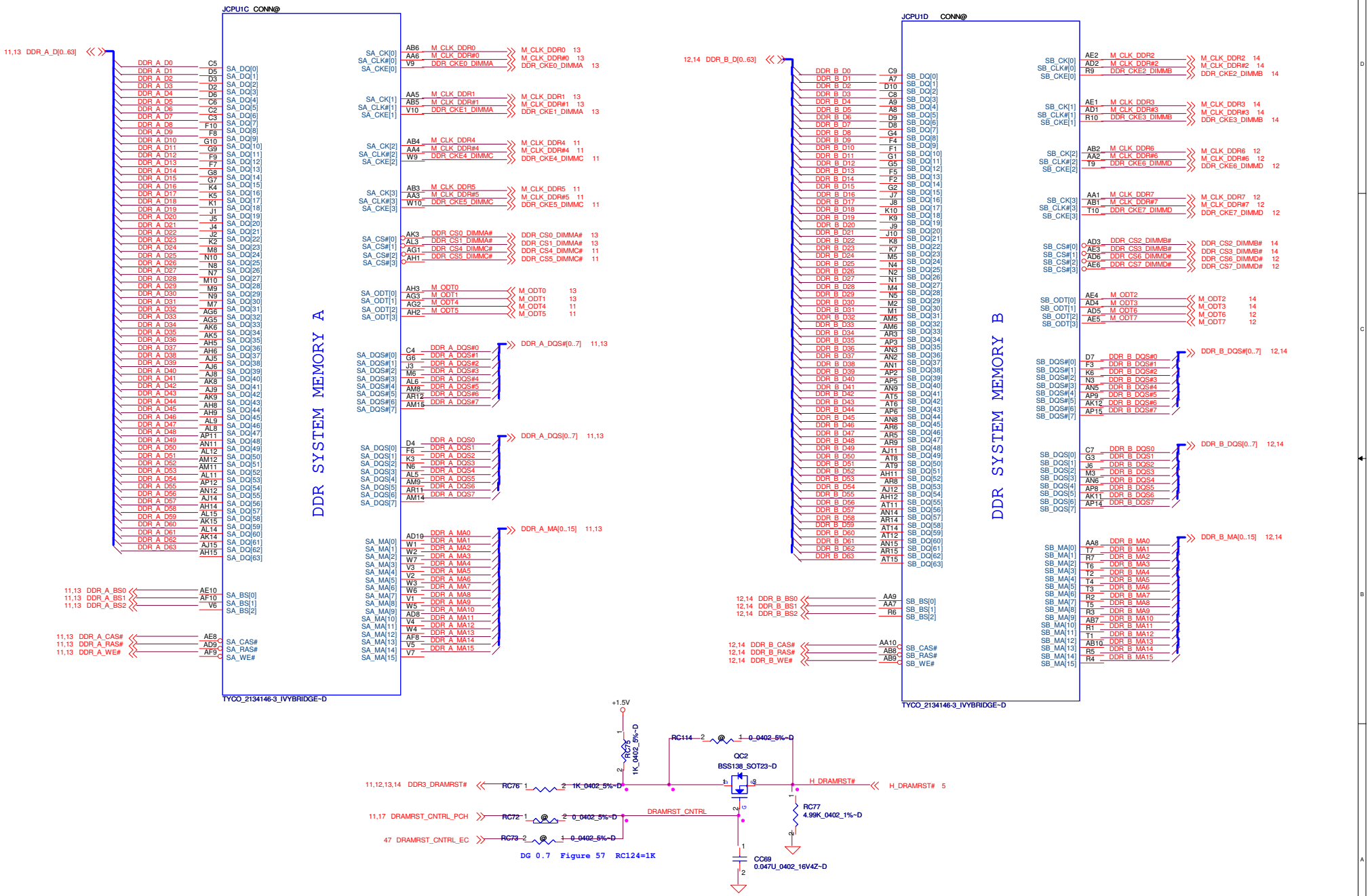
Compal Electronics, Inc.
PROCESSOR(2/6) PM,XDP,CLK
LA-8341P
Friday, March 02, 2012

Need to confired
when Intel spec release.



DG 0.7 Figure 57 RC124=1K

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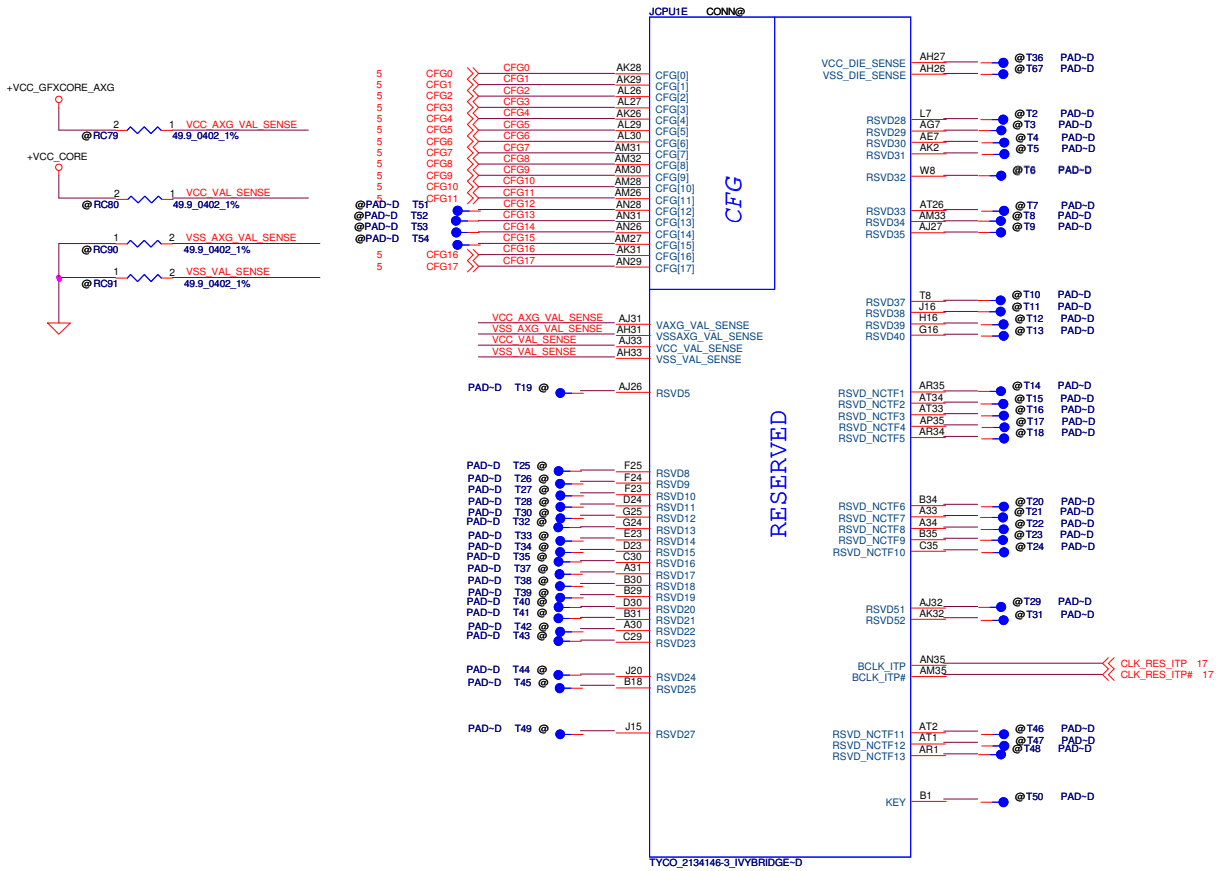
Compal Electronics, Inc.

Title: PROCESSOR(3/6) DDRIII

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 7 of 71



CFG Straps for Processor

CFG2 — @RC79 1K_0402_1%~D

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4 — RC81 1K_0402_1%~D

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6 / CFG5 — @RC87 1K_0402_1%~D, @RC88 1K_0402_1%~D

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7 — @RC89 1K_0402_1%~D

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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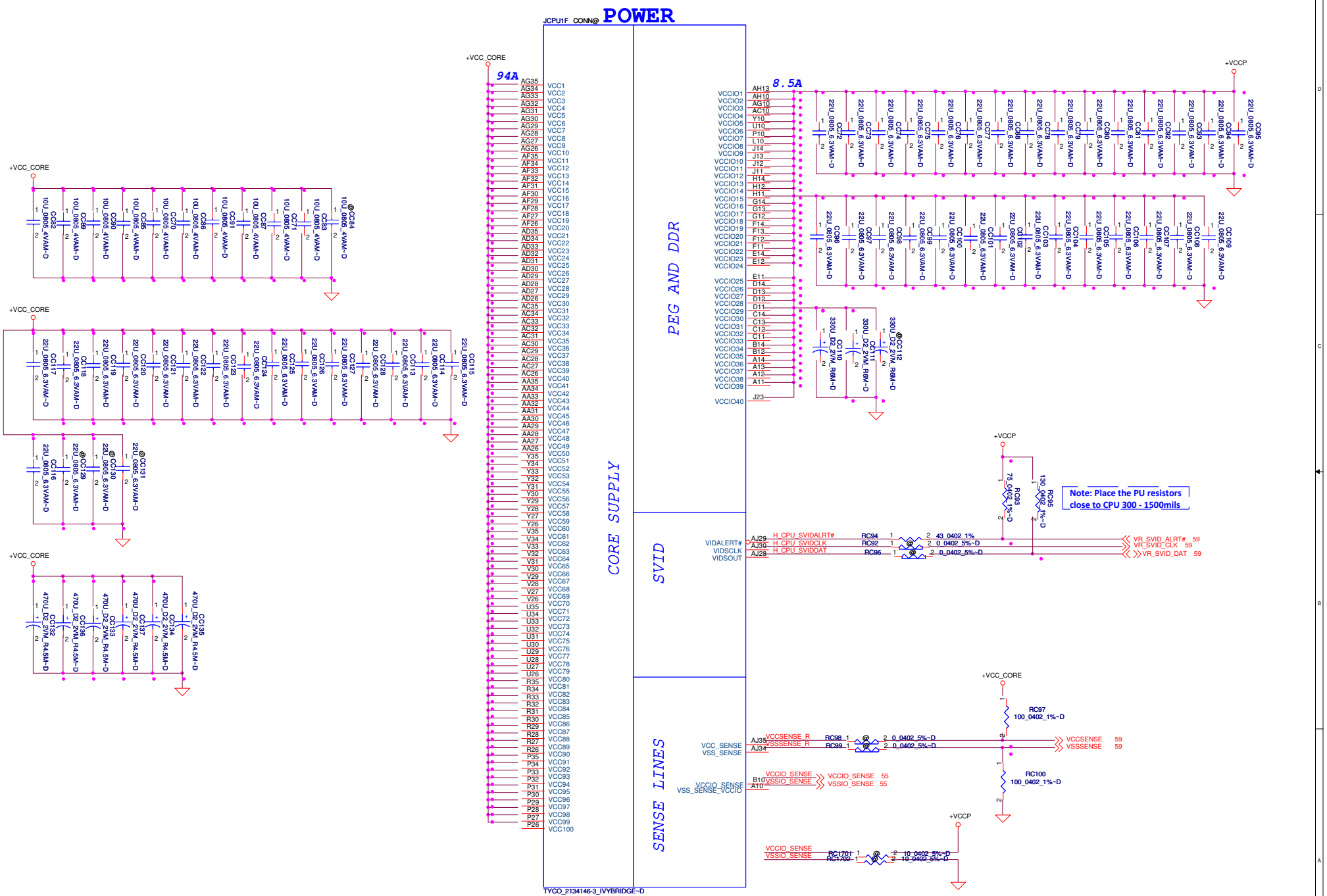
Title: PROCESSOR(4/6) RSVD,CFG

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 8 of 71

POWER



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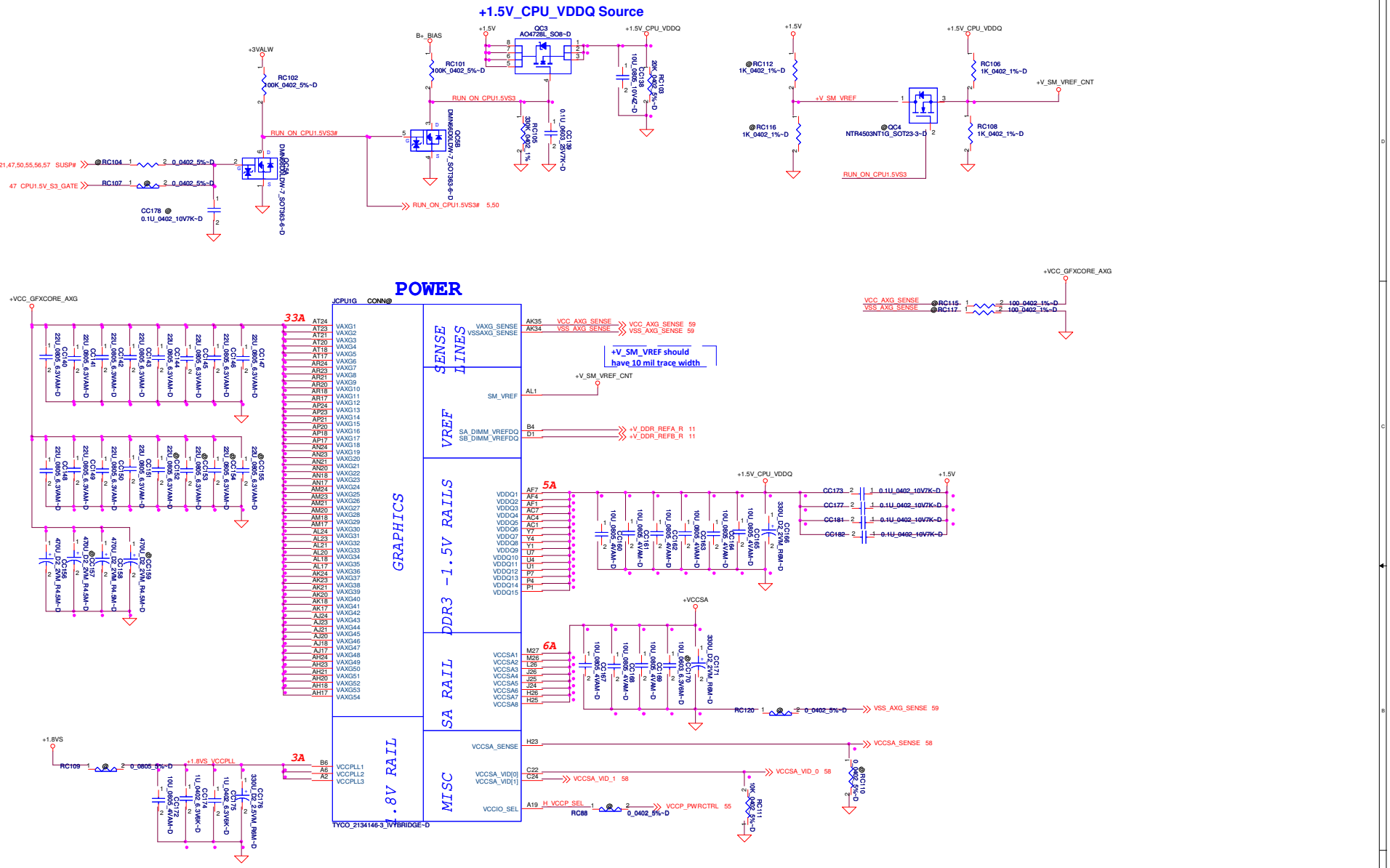
Title: PROCESSOR(5/6) PWR,BYPASS

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 9 of 71



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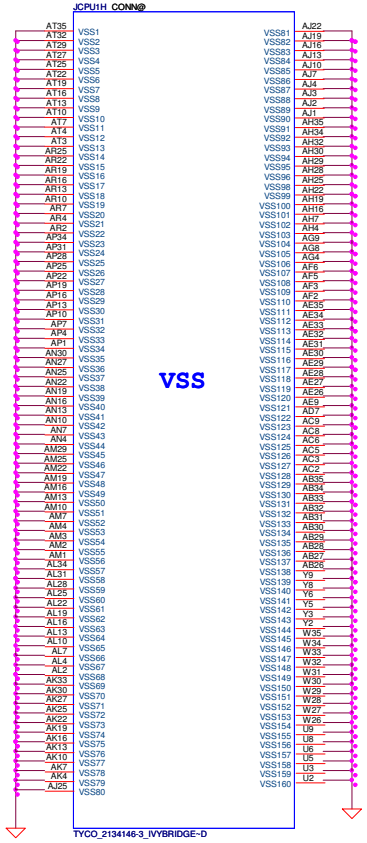
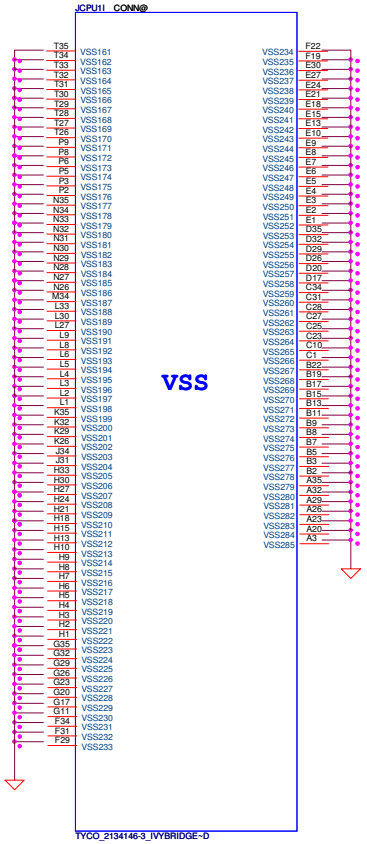
Compal Electronics, Inc.		
Title: PROCESSOR(6/6) PWR,VSS		
Size	Document Number: LA-8341P	Rev: 1.0
Date: Friday, March 02, 2012	Sheet 10 of 71	





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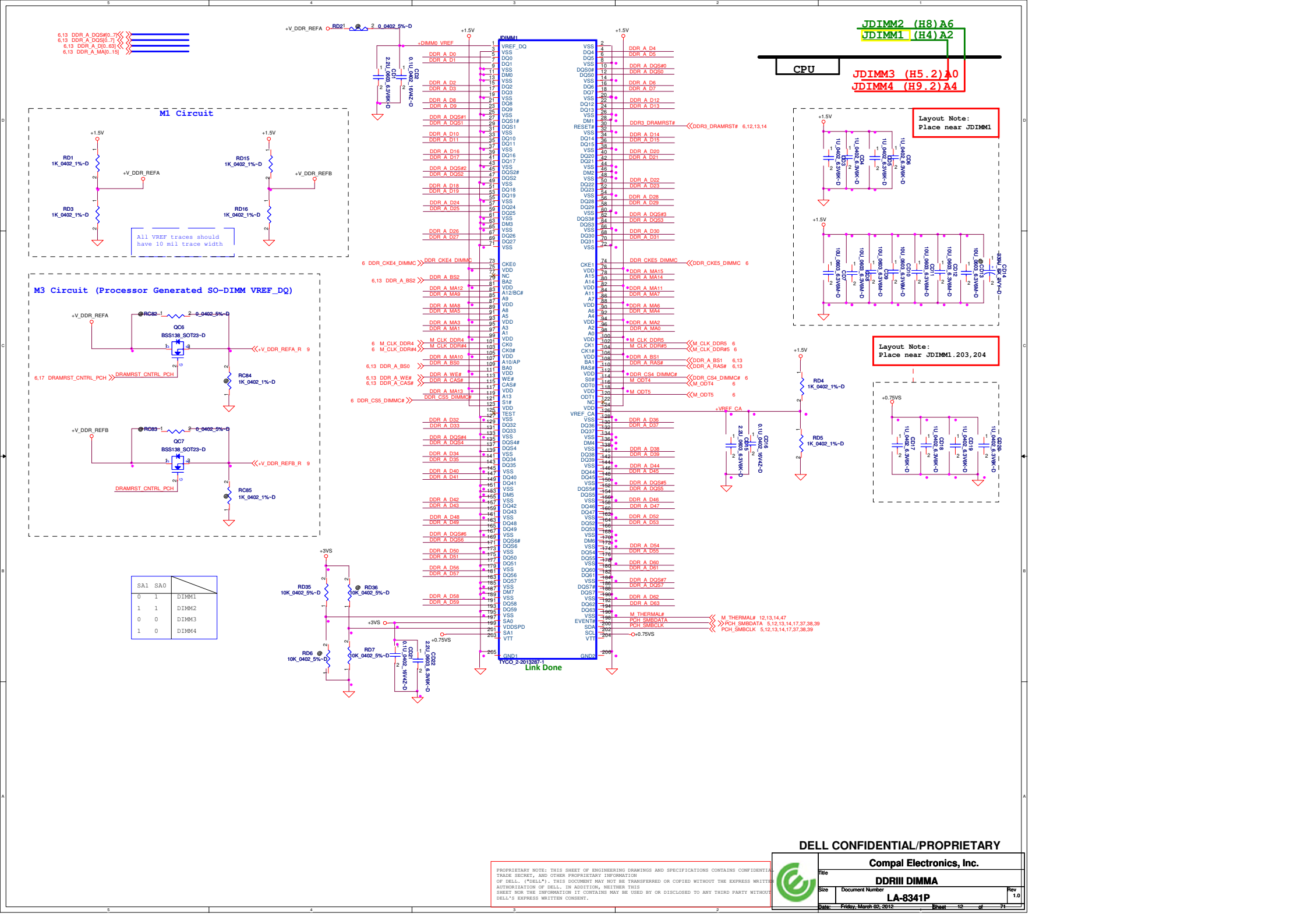
Compal Electronics, Inc.

Title: PROCESSOR(6/6) PWR,VSS

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 11 of 71


JDIMM2 (H8)A6
JDIMM1 (H4)A2
CPU
JDIMM3 (H5.2)A0
JDIMM4 (H9.2)A4
M1 Circuit
All VREF traces should have 10 mil trace width
M3 Circuit (Processor Generated SO-DIMM VREF_DQ)
Layout Note: Place near JDIMM1
Layout Note: Place near JDIMM1,203,204
Link Done
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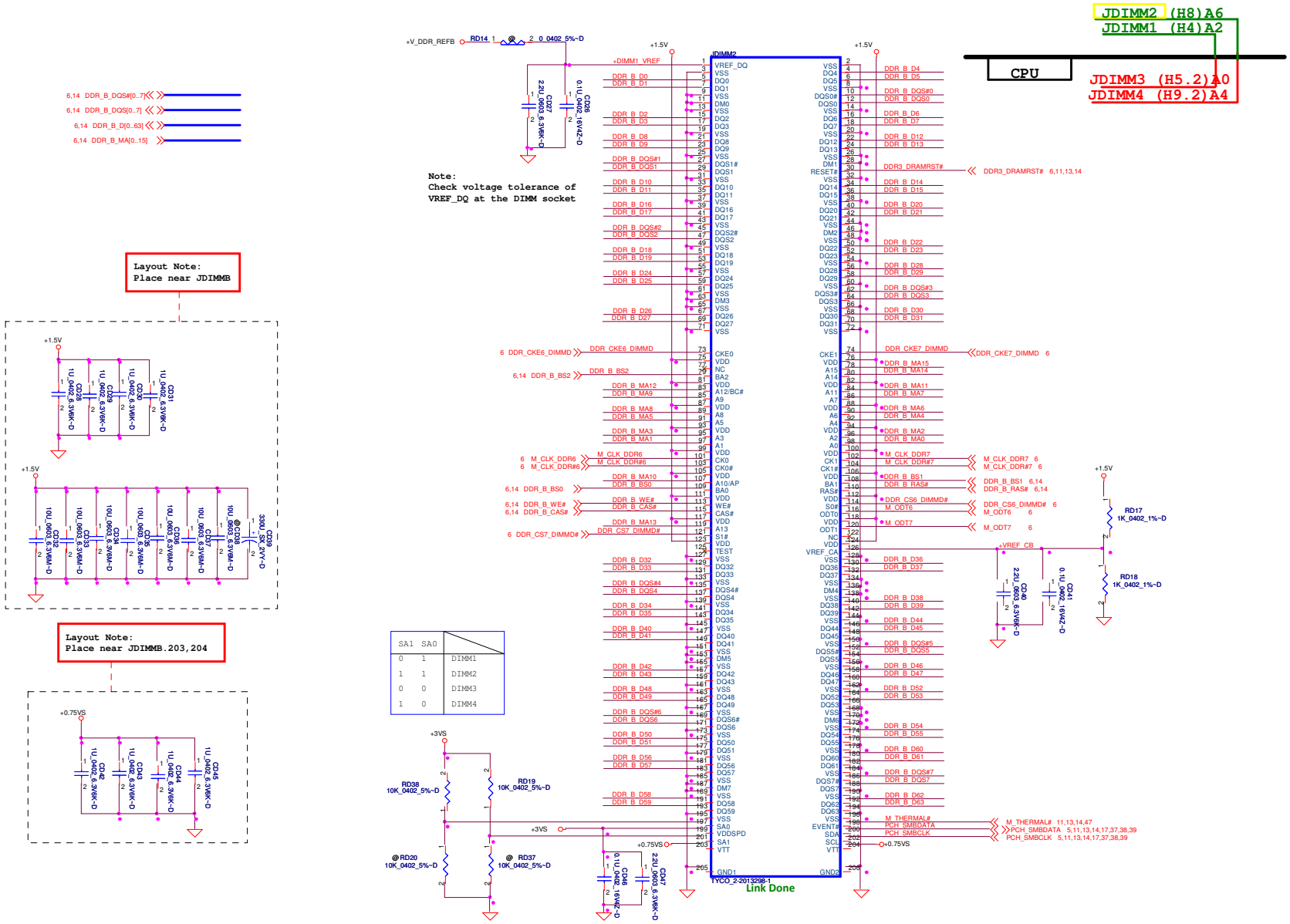
DDRIII DIMMA
LA-8341P
Friday, March 02, 2012



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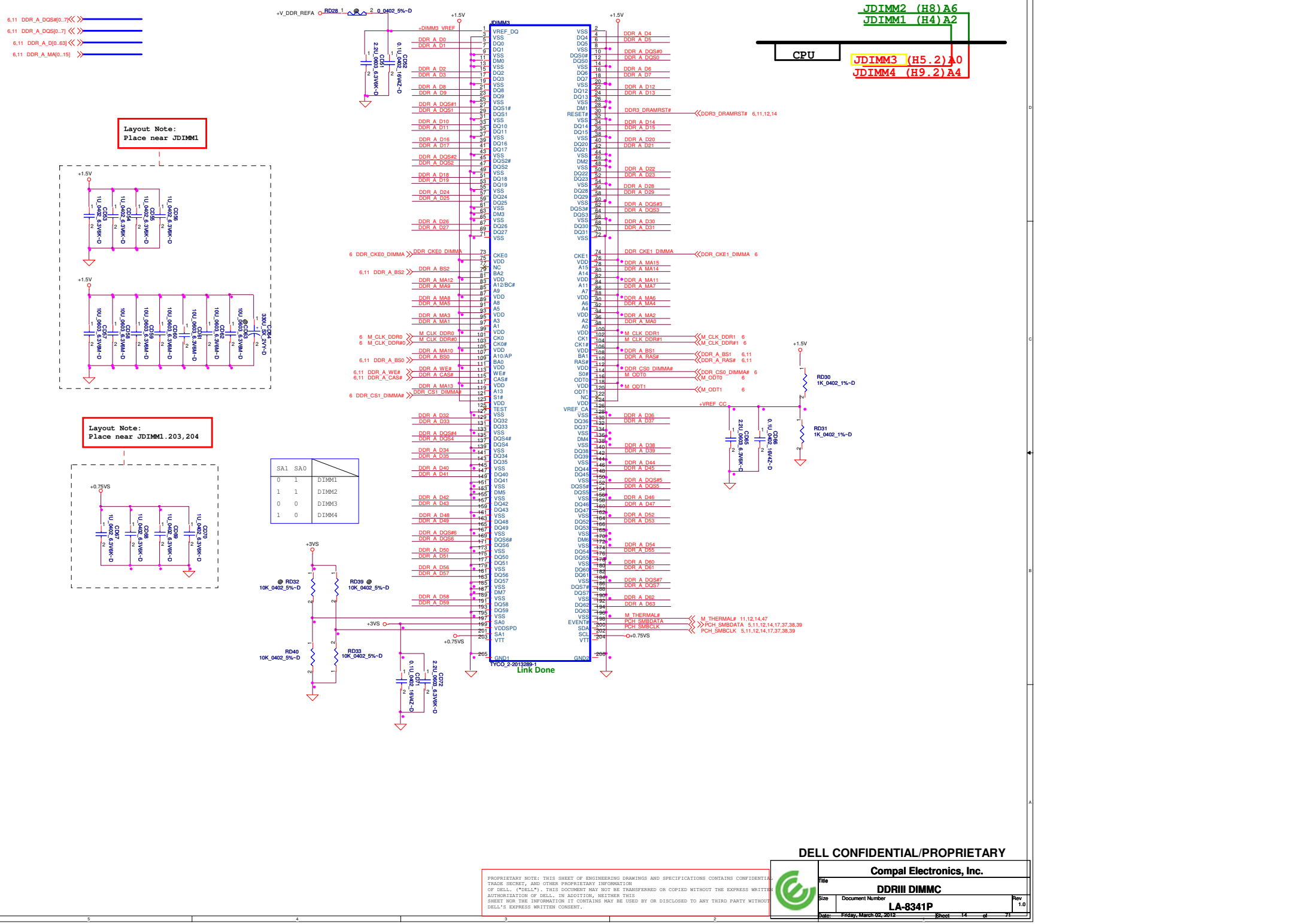
Title: DDRIII DIMMB		
Size	Document Number: LA-8341P	Rev: 1.0
Date: Friday, March 02, 2012	Sheet 19 of 71	



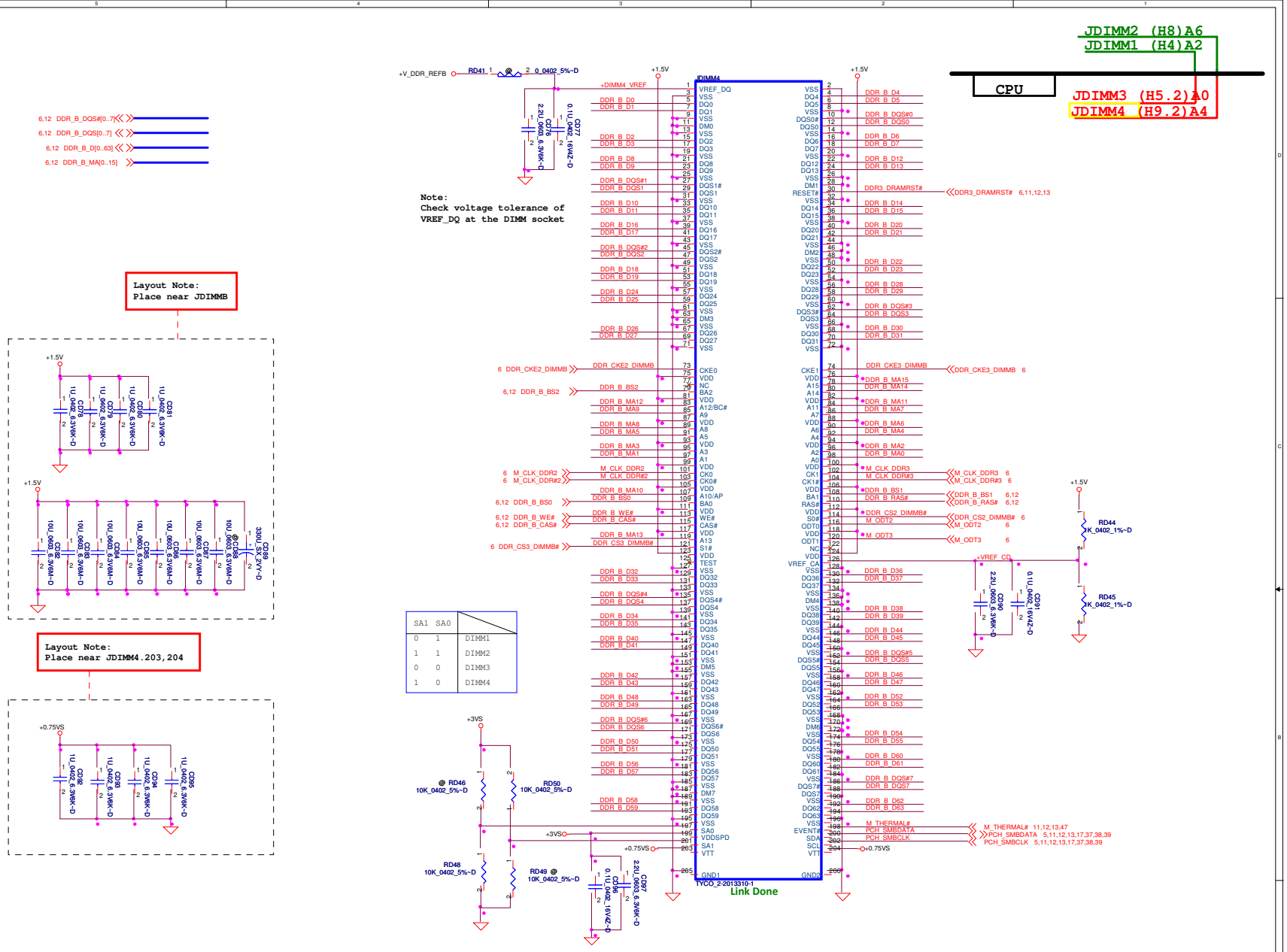
Compal Electronics, Inc.

Title: DDRIII DIMMC

Size: Document Number: LA-8341P

Rev: 1.0

Date: Friday, March 02, 2012 Sheet 14 of 71



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Title: DDRIII DIMMD		
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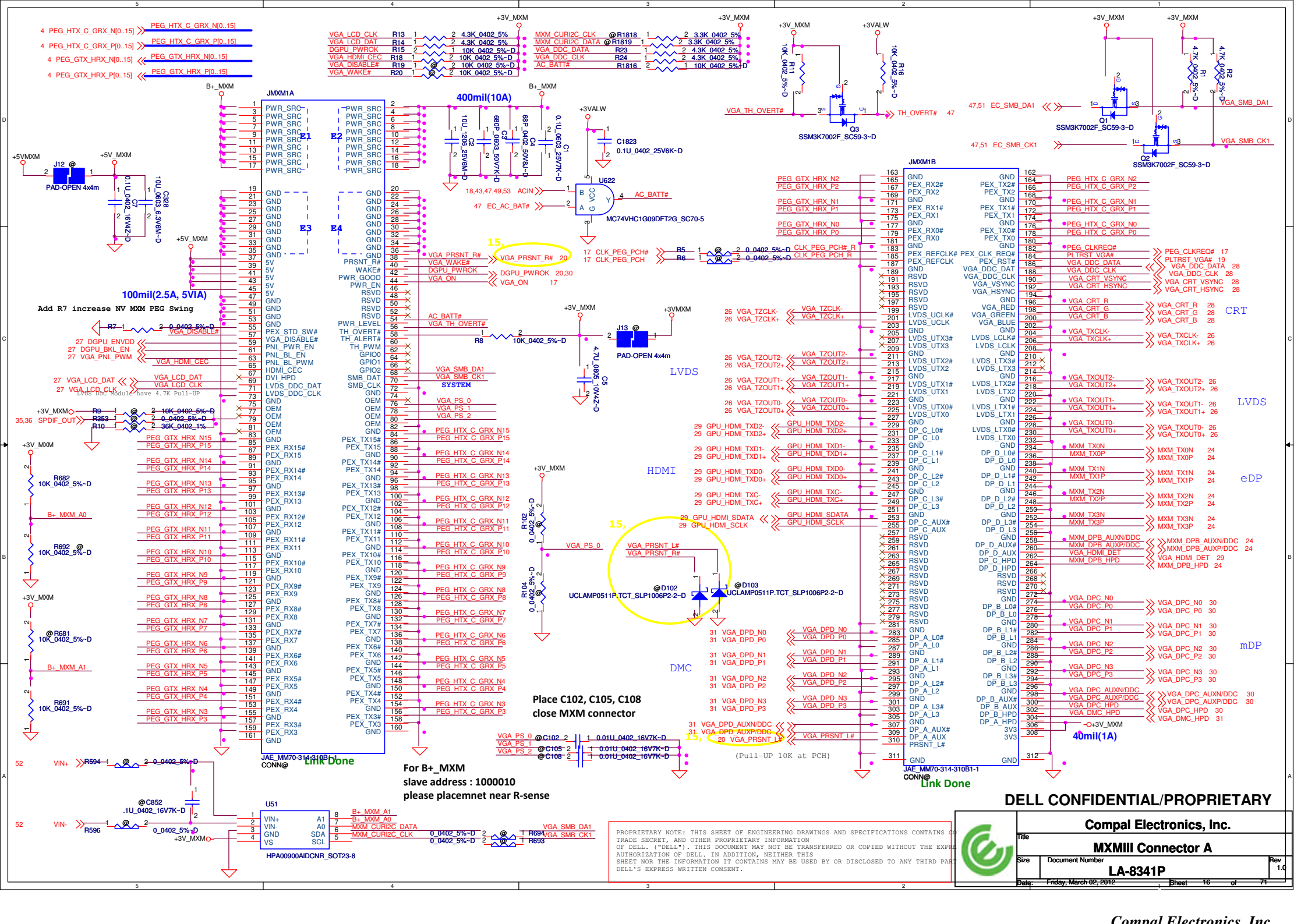
Date: Friday, March 02, 2012	Sheet 15 of 71	



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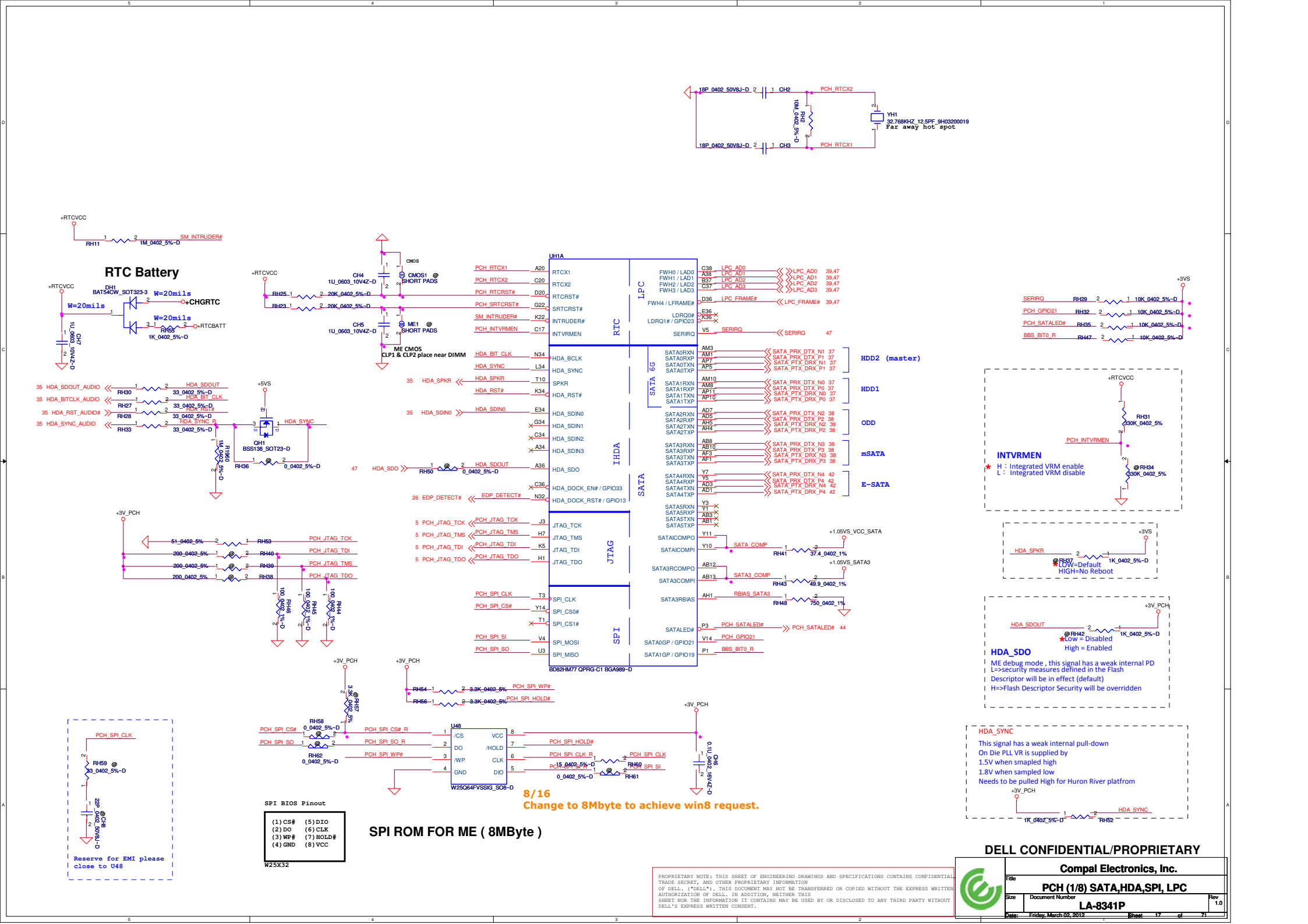
Compal Electronics, Inc.	
Title	MXMIII Connector A
Size	Document Number: LA-8341P
Rev	1.0
Date:	Friday, March 02, 2012
Sheet	16 of 71


RTC Battery
ME CMOS
CLP1 & CLP2 place near DIMM
UH1A
BD82HM77 QPRG-C1 BGA989-D
LPC
RTC
SATA
IHDA
JTAG
SPI
HDD2 (master)
HDD1
ODD
mSATA
E-SATA
INTVRMEN
HDA_SDO
HDA_SYNC
SPI BIOS Pinout
W25X32
SPI ROM FOR ME (8MByte)
8/16
Change to 8Mbyte to achieve win8 request.
Reserve for EMI please close to U48
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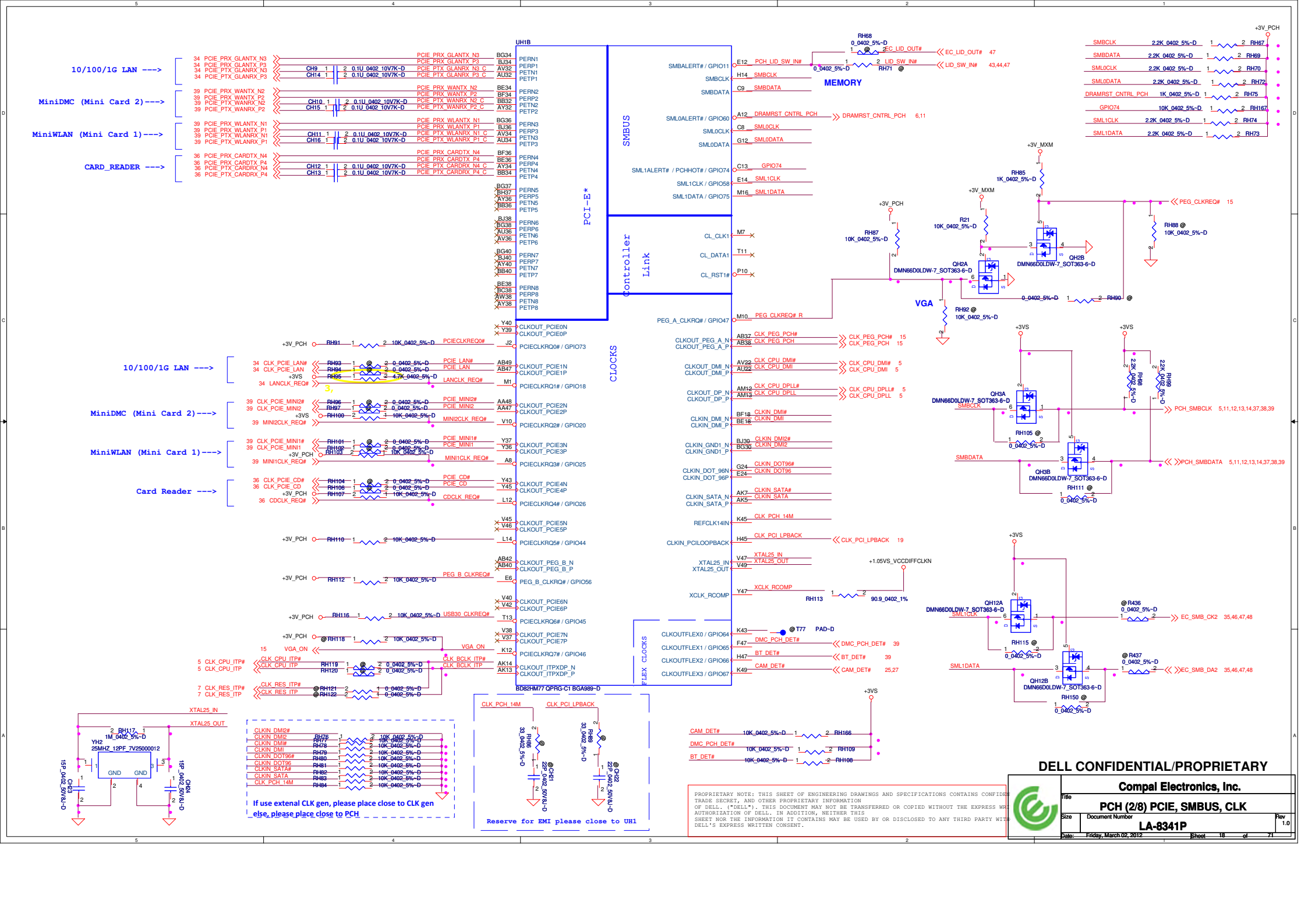
PCH (1/8) SATA,HDA,SPI, LPC
LA-8341P


10/100/1G LAN ---->
MiniDMC (Mini Card 2)---->
MiniWLAN (Mini Card 1)---->
CARD_READER ---->
UH1B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
MEMORY
VGA
BD82HM77 QPRG-C1 BGA989-D
If use extenal CLK gen, please place close to CLK gen else, please place close to PCH
Reserve for EMI please close to UH1
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PCH (2/8) PCIE, SMBUS, CLK
LA-8341P
Friday, March 02, 2012

0811: Intel request DDPB can not support eDP

UH1C

DMI_CTX_PRX_N0 BC24
DMI_CTX_PRX_N1 BE20
DMI_CTX_PRX_N2 BG18
DMI_CTX_PRX_N3 BG20
DMI_CTX_PRX_P0 BE24
DMI_CTX_PRX_P1 BC20
DMI_CTX_PRX_P2 BJ18
DMI_CTX_PRX_P3 BJ20
DMI_CRX_PTX_N0 AW24
DMI_CRX_PTX_N1 AW20
DMI_CRX_PTX_N2 BB18
DMI_CRX_PTX_N3 AV18
DMI_CRX_PTX_P0 AY24
DMI_CRX_PTX_P1 AY20
DMI_CRX_PTX_P2 AY18
DMI_CRX_PTX_P3 AU18

DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI0TXP DMI1TXP DMI2TXP DMI3TXP

DMI

+1.05VS
DMI_IRCOMP BJ24
RH124 49.9_0402_1% DMI_IRCOMP BG25
RH125 750_0402_1%~D RBIAS_CPY BH21
DMI2RBIAS
4mil width and place within 500mil of the PCH

FDI

FDI_RXN0 BJ14 FDI_CTX_PRX_N0 — FDI_CTX_PRX_N0 4
FDI_RXN1 AY14 FDI_CTX_PRX_N1 — FDI_CTX_PRX_N1 4
FDI_RXN2 BE14 FDI_CTX_PRX_N2 — FDI_CTX_PRX_N2 4
FDI_RXN3 BH13 FDI_CTX_PRX_N3 — FDI_CTX_PRX_N3 4
FDI_RXN4 BC12 FDI_CTX_PRX_N4 — FDI_CTX_PRX_N4 4
FDI_RXN5 BJ12 FDI_CTX_PRX_N5 — FDI_CTX_PRX_N5 4
FDI_RXN6 BG10 FDI_CTX_PRX_N6 — FDI_CTX_PRX_N6 4
FDI_RXN7 BG9 FDI_CTX_PRX_N7 — FDI_CTX_PRX_N7 4
FDI_RXP0 BG14 FDI_CTX_PRX_P0 — FDI_CTX_PRX_P0 4
FDI_RXP1 BB14 FDI_CTX_PRX_P1 — FDI_CTX_PRX_P1 4
FDI_RXP2 BF14 FDI_CTX_PRX_P2 — FDI_CTX_PRX_P2 4
FDI_RXP3 BG13 FDI_CTX_PRX_P3 — FDI_CTX_PRX_P3 4
FDI_RXP4 BE12 FDI_CTX_PRX_P4 — FDI_CTX_PRX_P4 4
FDI_RXP5 BG12 FDI_CTX_PRX_P5 — FDI_CTX_PRX_P5 4
FDI_RXP6 BJ10 FDI_CTX_PRX_P6 — FDI_CTX_PRX_P6 4
FDI_RXP7 BH9 FDI_CTX_PRX_P7 — FDI_CTX_PRX_P7 4

FDI_INT AW16 FDI_INT — FDI_INT 4
FDI_FSYNC0 AV12 FDI_FSYNC0 — FDI_FSYNC0 4
FDI_FSYNC1 BC10 FDI_FSYNC1 — FDI_FSYNC1 4
FDI_LSYNC0 AV14 FDI_LSYNC0 — FDI_LSYNC0 4
FDI_LSYNC1 BB10 FDI_LSYNC1 — FDI_LSYNC1 4

System Power Management

DSWVRMEN A18 DSWODVREN
DPWROK E22 PCH_DPWROK_R — RH126 1 @ 2 0_0402_5%~D PCH_RSMRST#_R
RH159 1 @ 2 0_0402_5%~D PCH_DPWROK 47
WAKE# B9 — RH128 1 @ 2 0_0402_5%~D PCIE_WAKE# 34,39,47
CLKRUN# / GPIO32 N3 PM_CLKRUN#
SUS_STAT# / GPIO61 G8 SUS_STAT# — @T76 PAD~D
SUSCLK / GPIO62 N14 SUSCLK — RH132 1 @ 2 0_0402_5%~D SUSCLK_R 47
SLP_S5# / GPIO63 D10 PM_SLP_S5# — PM_SLP_S5# 43,47
SLP_S4# H4 PM_SLP_S4# — PM_SLP_S4# 47
SLP_S3# F4 PM_SLP_S3# — PM_SLP_S3# 43,47
SLP_A# G10
SLP_SUS# G16 PM_SLP_SUS# — PM_SLP_SUS# 47
PMSYNCH AP14 H_PM_SYNC — H_PM_SYNC 5
SLP_LAN# / GPIO29 K14 — If not using integrated LAN,signal may be left as NC.

27,47 SG_AMD_BKL — @RH127 1 2 0_0402_5%~D — SUSACK# C12
XDP_DBRESET# — 5 XDP_DBRESET# — SYS_RESET# K3
5,59 VGATE — RC119 1 @ 2 0_0402_5%~D — 5,47 SYSTEM_PWROK — RH129 @ 1 2 0_0402_5%~D — SYS_PWROK P12
5,47 PCH_PWROK — RH130 1 @ 2 0_0402_5%~D PM_PWROK_R — PWROK L22
47 PCH_APWROK — RH131 1 @ 2 0_0402_5%~D — APWROK L10
5 PM_DRAM_PWRGD — PM_DRAM_PWRGD — DRAMPWROK B13
47 PCH_RSMRST# — RH133 1 @ 2 0_0402_5%~D PCH_RSMRST#_R — RSMRST# C21
47 SUSPWRDNACK — RH134 1 @ 2 0_0402_5%~D SUSPWRDNACK_R — SUSWARN#/SUSPWRDNACK/GPIO30 K16
5,47 PBTN_OUT# — RH135 1 @ 2 0_0402_5%~D PBTN_OUT#_R — PWRBTN# E20
ACIN_PCH — ACPRESENT / GPIO31 H20
BATLOW# — BATLOW# / GPIO72 E10
RI# — RI# A10

BD82HM77 QPRG-C1 BGA989~D

UH1D

LVDS

27 IGPU_BKLT_EN — IGPU_BKLT_EN — L_BKLTEN J47
27,47 PCH_ENVDD — PCH_ENVDD — L_VDD_EN M45
27 PCH_INV_PWM — P45 L_BKLTCTL
27 PCH_LCD_CLK — PCH_LCD_CLK — L_DDC_CLK T40
27 PCH_LCD_DATA — PCH_LCD_DATA — L_DDC_DATA K47
CTRL_CLK T45 L_CTRL_CLK
CTRL_DATA P39 L_CTRL_DATA
RH144 2 1 2.37K_0402_1%~D LVDS_IBG — LVD_IBG AF37
LVD_VBG AF36
Minimum speacing of 20mils for LVD_IBG
LVD_VREFH AE48
LVD_VREFL AE47

26 PCH_TXCLK- — PCH_TXCLK- — LVDSA_CLK# AK39
26 PCH_TXCLK+ — PCH_TXCLK+ — LVDSA_CLK AK40
26 PCH_TXOUT0- — PCH_TXOUT0- — LVDSA_DATA#0 AN48
26 PCH_TXOUT1- — PCH_TXOUT1- — LVDSA_DATA#1 AM47
26 PCH_TXOUT2- — PCH_TXOUT2- — LVDSA_DATA#2 AK47
LVDSA_DATA#3 AJ48
26 PCH_TXOUT0+ — PCH_TXOUT0+ — LVDSA_DATA0 AN47
26 PCH_TXOUT1+ — PCH_TXOUT1+ — LVDSA_DATA1 AM49
26 PCH_TXOUT2+ — PCH_TXOUT2+ — LVDSA_DATA2 AK49
LVDSA_DATA3 AJ47

26 PCH_TZCLK- — PCH_TZCLK- — LVDSB_CLK# AF40
26 PCH_TZCLK+ — PCH_TZCLK+ — LVDSB_CLK AF39
26 PCH_TZOUT0- — PCH_TZOUT0- — LVDSB_DATA#0 AH45
26 PCH_TZOUT1- — PCH_TZOUT1- — LVDSB_DATA#1 AH47
26 PCH_TZOUT2- — PCH_TZOUT2- — LVDSB_DATA#2 AF49
LVDSB_DATA#3 AF45
26 PCH_TZOUT0+ — PCH_TZOUT0+ — LVDSB_DATA0 AH43
26 PCH_TZOUT1+ — PCH_TZOUT1+ — LVDSB_DATA1 AH49
26 PCH_TZOUT2+ — PCH_TZOUT2+ — LVDSB_DATA2 AF47
LVDSB_DATA3 AF43

CRT

28 PCH_CRT_BLU — PCH_CRT_BLU — CRT_BLUE N48
28 PCH_CRT_GRN — PCH_CRT_GRN — CRT_GREEN P49
28 PCH_CRT_RED — PCH_CRT_RED — CRT_RED T49
28 PCH_CRT_DDC_CLK — PCH_CRT_DDC_CLK — CRT_DDC_CLK T39
28 PCH_CRT_DDC_DAT — PCH_CRT_DDC_DAT — CRT_DDC_DATA M40
28 PCH_CRT_HSYNC — RH136 1 2 33_0402_5%~D HSYNC — CRT_HSYNC M47
28 PCH_CRT_VSYNC — RH138 1 2 33_0402_5%~D VSYNC — CRT_VSYNC M49
CRT_IREF T43
DAC_IREF T42
RH140 1K_0402_0.5%~D

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 HDMICLK_NB — HDMICLK_NB 29
SDVO_CTRLDATA M39 HDMIDAT_NB — HDMIDAT_NB 29

HDMI

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 TMDS_B_HPD — TMDS_B_HPD 29
DDPB_0N AV42 TMDS_B_DATA2# — TMDS_B_DATA2# 29
DDPB_0P AV40 TMDS_B_DATA2 — TMDS_B_DATA2 29
DDPB_1N AV45 TMDS_B_DATA1# — TMDS_B_DATA1# 29
DDPB_1P AV46 TMDS_B_DATA1 — TMDS_B_DATA1 29
DDPB_2N AU48 TMDS_B_DATA0# — TMDS_B_DATA0# 29
DDPB_2P AU47 TMDS_B_DATA0 — TMDS_B_DATA0 29
DDPB_3N AV47 TMDS_B_CLK# — TMDS_B_CLK# 29
DDPB_3P AV49 TMDS_B_CLK — TMDS_B_CLK 29

mDP

DDPC_CTRLCLK P46 PCH_DPC_CLK — PCH_DPC_CLK 30
DDPC_CTRLDATA P42 PCH_DPC_DAT — PCH_DPC_DAT 30
DDPC_AUXN AP47 PCH_DPC_AUXN — PCH_DPC_AUXN 30
DDPC_AUXP AP49 PCH_DPC_AUXP — PCH_DPC_AUXP 30
DDPC_HPD AT38 DP_HPD — DP_HPD 30
DDPC_0N AY47 PCH_DPC_N0 — PCH_DPC_N0 30
DDPC_0P AY49 PCH_DPC_P0 — PCH_DPC_P0 30
DDPC_1N AY43 PCH_DPC_N1 — PCH_DPC_N1 30
DDPC_1P AY45 PCH_DPC_P1 — PCH_DPC_P1 30
DDPC_2N BA47 PCH_DPC_N2 — PCH_DPC_N2 30
DDPC_2P BA48 PCH_DPC_P2 — PCH_DPC_P2 30
DDPC_3N BB47 PCH_DPC_N3 — PCH_DPC_N3 30
DDPC_3P BB49 PCH_DPC_P3 — PCH_DPC_P3 30

DMC HDMI

DDPD_CTRLCLK M43 PCH_DPD_CLK — PCH_DPD_CLK 31
DDPD_CTRLDATA M36 PCH_DPD_DAT — PCH_DPD_DAT 31
DDPD_AUXN AT45 PCH_DPD_AUXN/DDC — PCH_DPD_AUXN/DDC 31
DDPD_AUXP AT43 PCH_DPD_AUXP/DDC — PCH_DPD_AUXP/DDC 31
DDPD_HPD BH41 PCH_DMC_HPD — PCH_DMC_HPD 31
DDPD_0N BB43 PCH_DPD_N0 — PCH_DPD_N0 31
DDPD_0P BB45 PCH_DPD_P0 — PCH_DPD_P0 31
DDPD_1N BF44 PCH_DPD_N1 — PCH_DPD_N1 31
DDPD_1P BE44 PCH_DPD_P1 — PCH_DPD_P1 31
DDPD_2N BF42 PCH_DPD_N2 — PCH_DPD_N2 31
DDPD_2P BE42 PCH_DPD_P2 — PCH_DPD_P2 31
DDPD_3N BJ42 PCH_DPD_N3 — PCH_DPD_N3 31
DDPD_3P BG42 PCH_DPD_P3 — PCH_DPD_P3 31

BD82HM77 QPRG-C1 BGA989~D

+3V_PCH
R1899 10K_0402_5%
R1900 10K_0402_5%
ACIN_PCH
15,43,47,49,53 ACIN
QH11B DMN66D0LDW-7_SOT363-6~D
QH11A DMN66D0LDW-7_SOT363-6~D

+RTCVCC
RH147 330K_0402_5%
DSWODVREN
@ RH151 330K_0402_5%
DSWODVREN - On Die DSW VR Enable
H : Enable
L : Disable

+3VS
RH148 2.2K_0402_5%~D PCH_CRT_DDC_CLK
RH152 2.2K_0402_5%~D PCH_CRT_DDC_DAT
RH155 2.2K_0402_5%~D CTRL_CLK
RH157 2.2K_0402_5%~D CTRL_DATA
@R78 8.2K_0402_5% PM_CLKRUN#
RV1 2.2K_0402_5%~D PCH_LCD_CLK
RV2 2.2K_0402_5%~D PCH_LCD_DATA

R1696 10K_0402_5%~D PM_CLKRUN#
RH142 10K_0402_1%~D PCH_DPWROK
RH149 150_0402_1% PCH_RSMRST#
RH153 150_0402_1% PCH_SUSWARN#
RH156 150_0402_1% PCH_ENVDD
RH158 100K_0402_5%~D IGPU_BKLT_EN
RH123 100K_0402_5%~D PCH_RSMRST#
R1697 10K_0402_5%~D

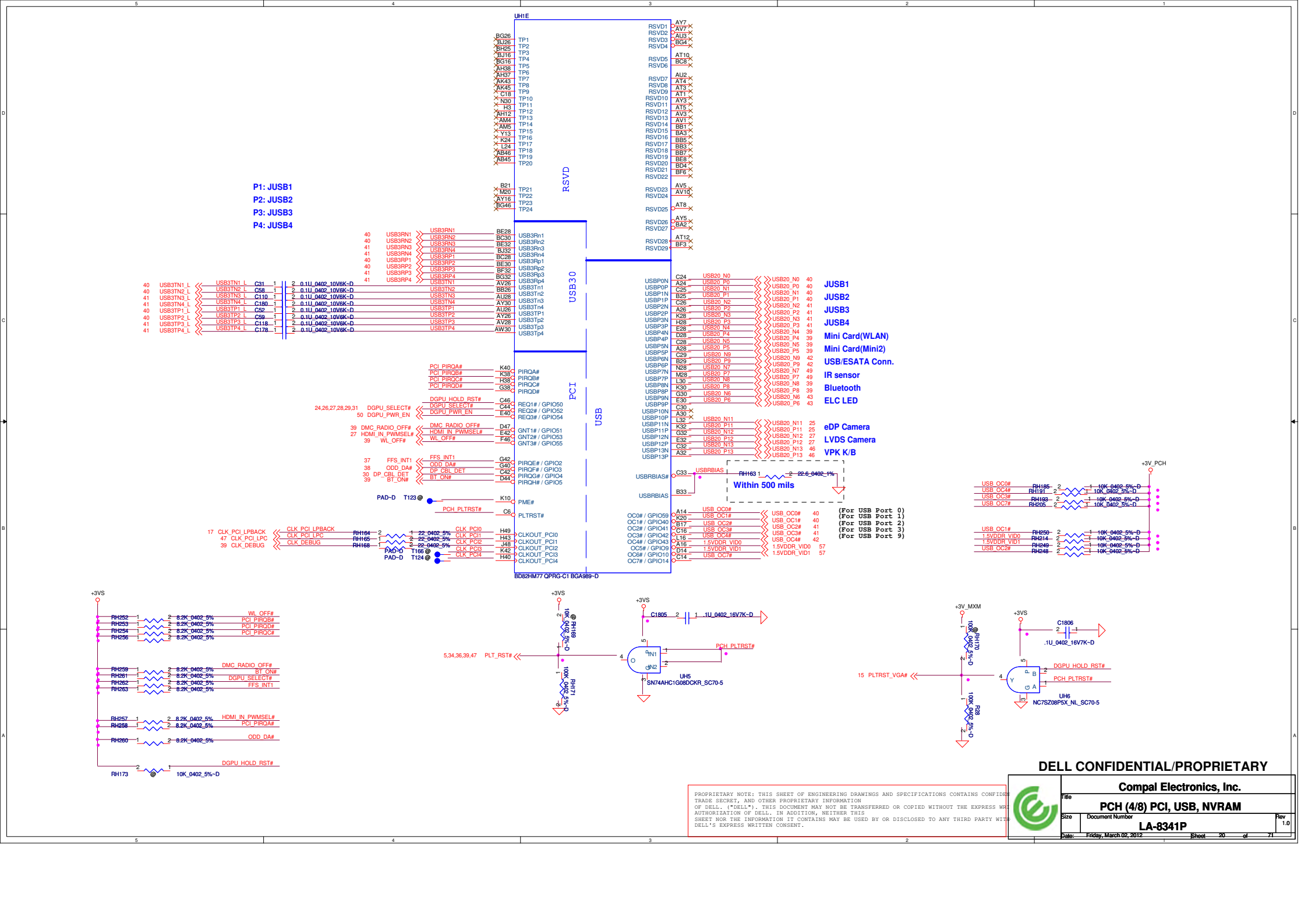
+3V_PCH
BATLOW# — RH143 10K_0402_5%~D
RI# — RH145 10K_0402_5%~D
WAKE# — RH146 1K_0402_5%~D
SUSPWRDNACK_R — RH154 10K_0402_5%~D
SUSPWRDNACK_R — RH172 0_0402_5%~D — SUSACK# R

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size: Document Number: LA-8341P Rev: 1.0

Date: Friday, March 02, 2012 Sheet 19 of 71


UH1E
RSVD
USB30
PCI
USB
BD82HM77 QPRG-C1 BGA989~D
P1: JUSB1
P2: JUSB2
P3: JUSB3
P4: JUSB4
JUSB1
JUSB2
JUSB3
JUSB4
Mini Card(WLAN)
Mini Card(Mini2)
USB/ESATA Conn.
IR sensor
Bluetooth
ELC LED
eDP Camera
LVDS Camera
VPK K/B
Within 500 mils
(For USB Port 0)
(For USB Port 1)
(For USB Port 2)
(For USB Port 3)
(For USB Port 9)
UH5
SN74AHC1G08DCKR_SC70-5
UH6
NC7SZ08P5X_NL_SC70-5
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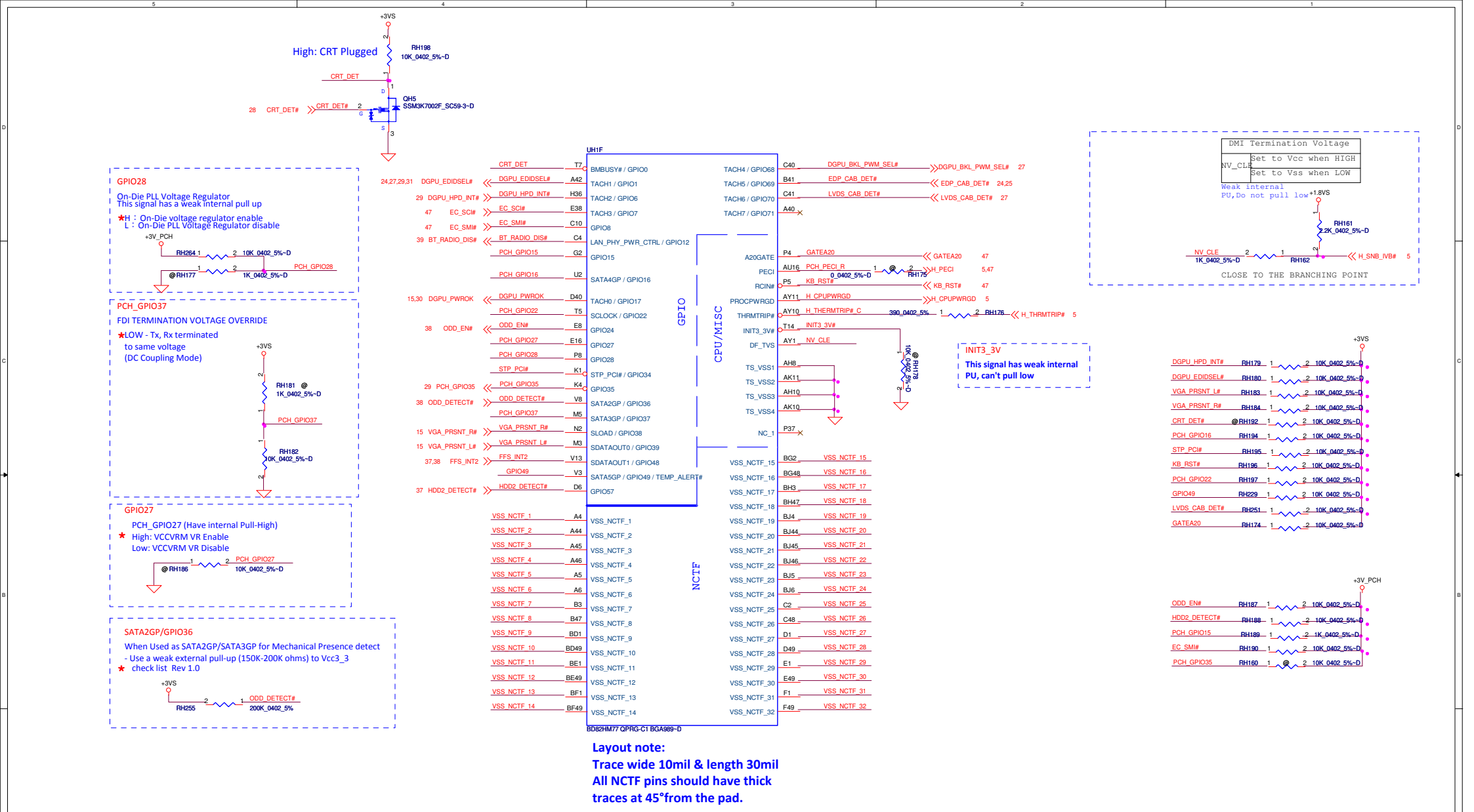
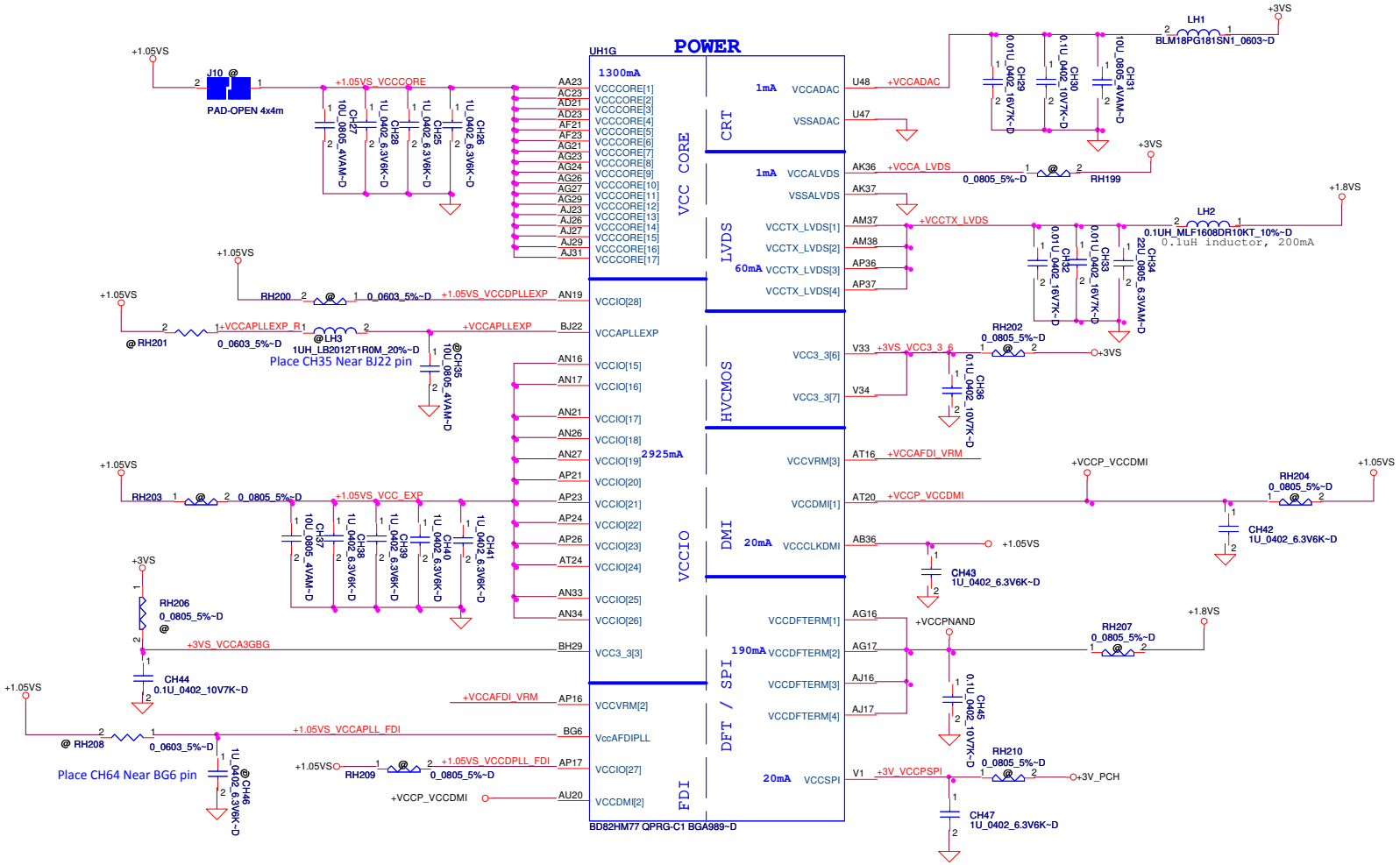
Compal Electronics, Inc.
Title
PCH (4/8) PCI, USB, NVRAM
Size
Document Number
LA-8341P
Rev
1.0
Date: Friday, March 02, 2012
Sheet 20 of 71



Compal Electronics, Inc.	
Title	PCH (5/8) GPIO, CPU, MISC
Size	Document Number: LA-8341P
Rev	1.0
Date: Friday, March 02, 2012	Sheet 21 of 71



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Title: PCH (6/8) PWR

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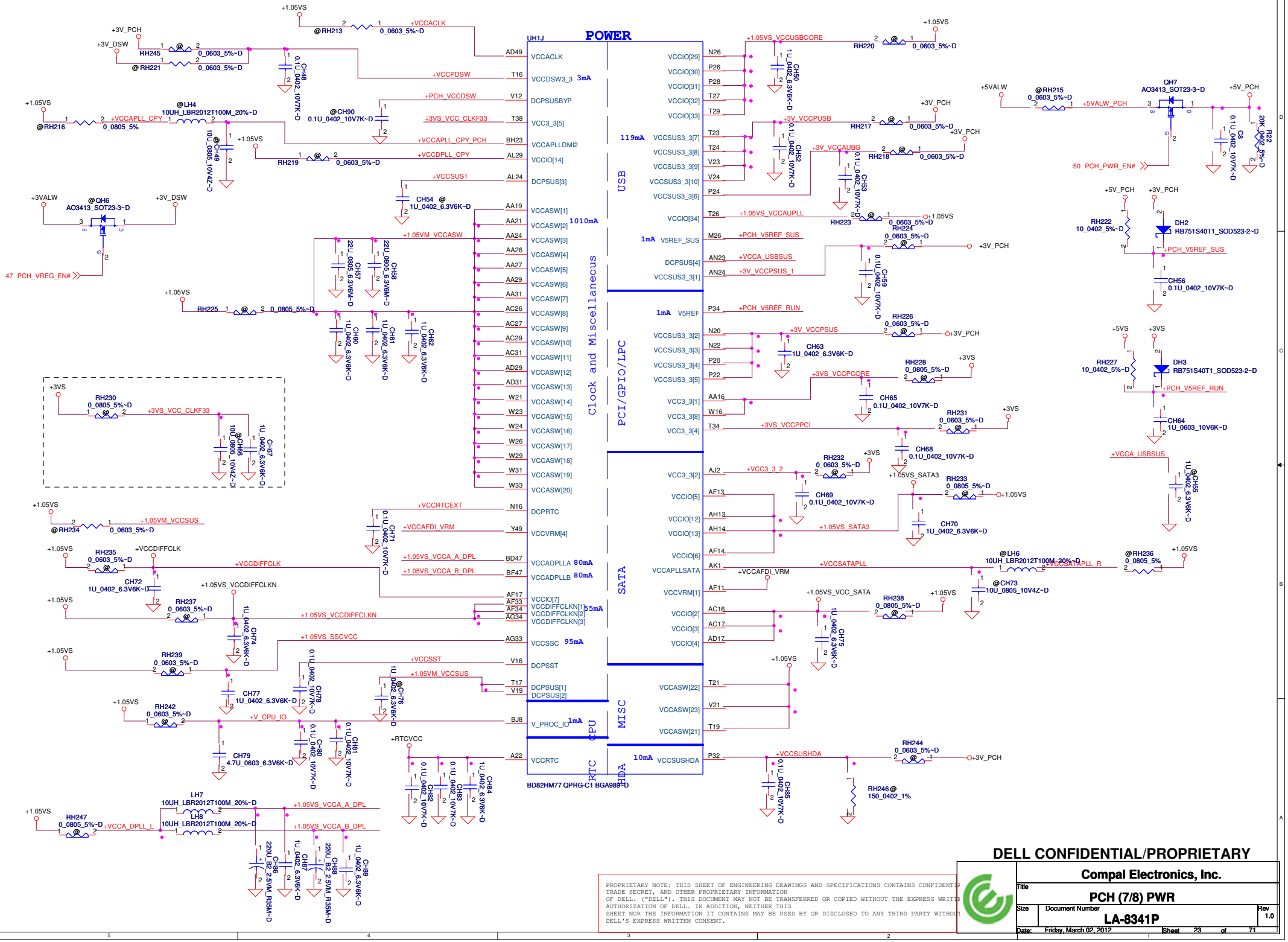
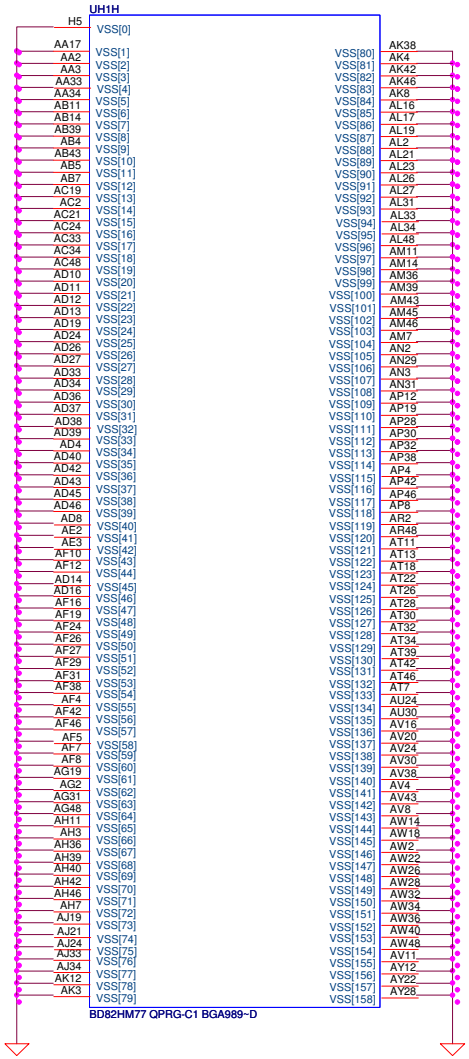
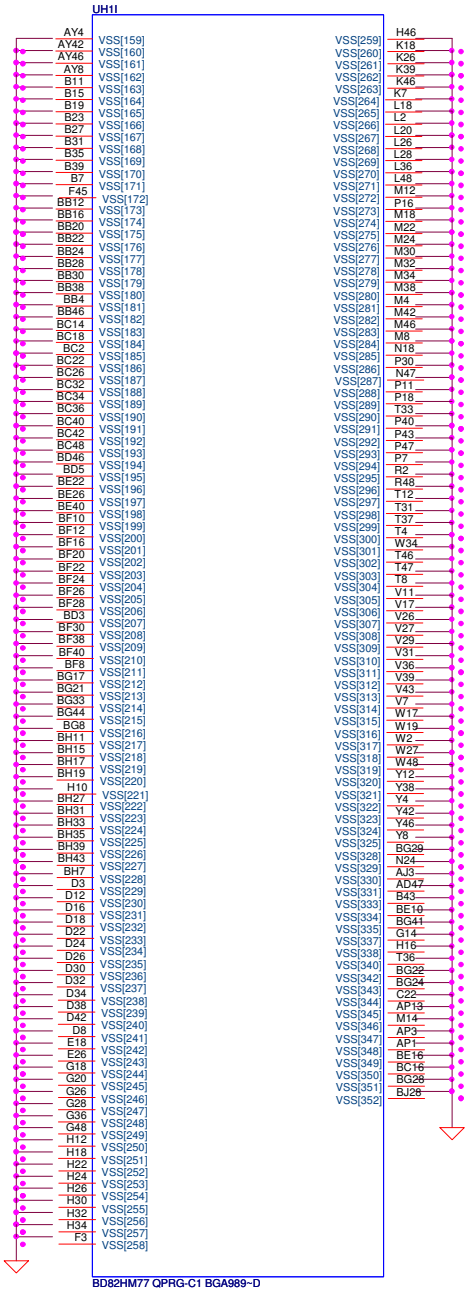
Date: Friday, March 02, 2012 | Sheet 22 of 71







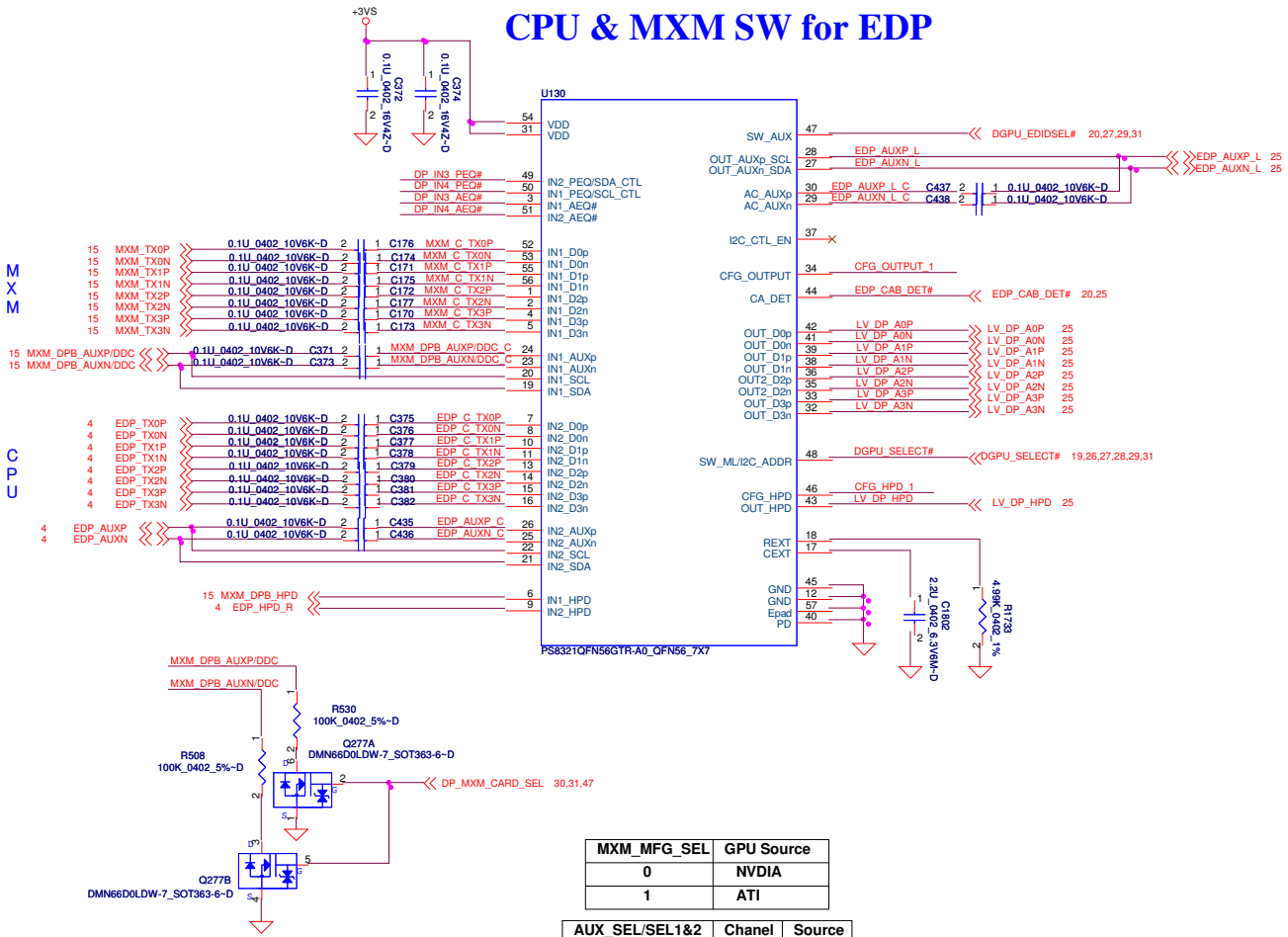
Compal Electronics, Inc.

Title: PCH (8/8) VSS

Size: | Document Number: LA-8341P | Rev: 1.0

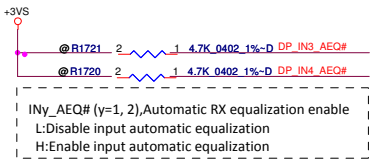
Date: Friday, March 02, 2012 | Sheet 24 of 71

CPU & MXM SW for EDP

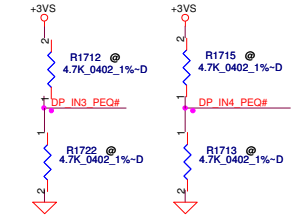


MXM_MFG_SEL	GPU Source
0	NVDIA
1	ATI

AUX_SEL/SEL1&2	Chanel	Source
0	A	CPU
1	B	MXM

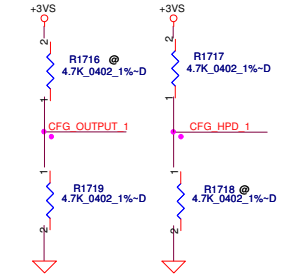


INy_AEQ# (y=1, 2),Automatic RX equalization enable
L:Disable input automatic equalization
H:Enable input automatic equalization



INy_PEQ(y = 1, 2),Programmable input equalization level setting
L:Low EQ setting (LEQ), default
H:High EQ setting (HEQ)
M:No EQ

CFG_OUTPUT: output configuration
L:Output is tracking DPCD register setting (auto interception)
H:Output swing level fixed at 600mV and no pre-emphasis
M:Output swing level is fixed at 400mV and no pre-emphasis



CFG_HPD,HPD switching configuration
L:HPD is switched by SW_ML
H:HPD is switched by SW_AUX
M:HPD is switched with overlap

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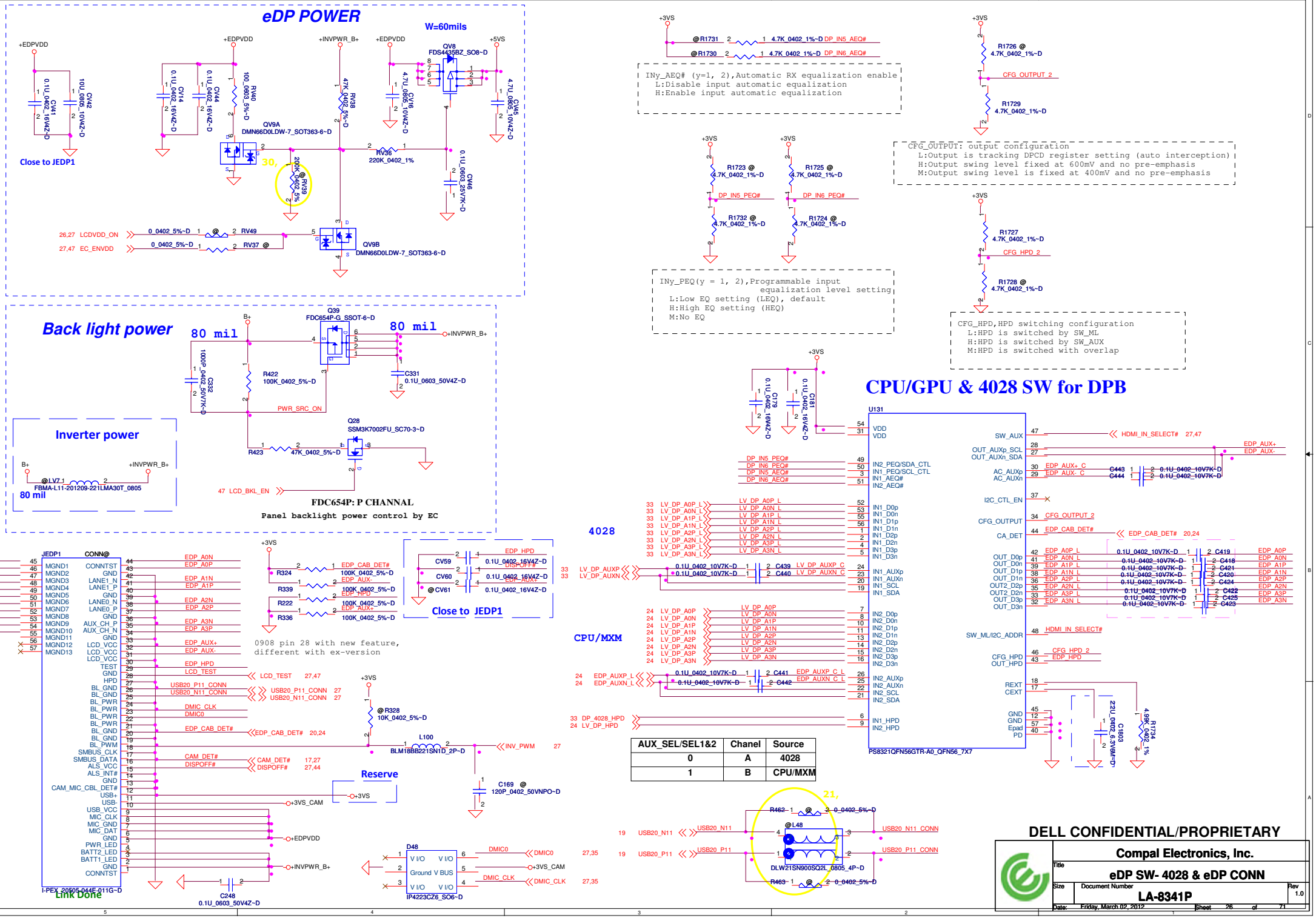
Title: eDP SW- GPU & CPU

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 25 of 71


eDP POWER
W=60mils
Close to JEDP1
QV9A DMN66D0LDW-7_SOT363-6~D
QV9B DMN66D0LDW-7_SOT363-6~D
QV6 FDS4435BZ_SO8~D
RV36 220K_0402_1%
RV39 200K_0402_5%
RV49
RV37 @
26,27 LCDVDD_ON
27,47 EC_ENVDD
Back light power
80 mil
80 mil
Q39 FDC654P-G_SSOT-6~D
Q28 SSM3K7002FU_SC70-3~D
R422 100K_0402_5%~D
R423 47K_0402_5%~D
PWR_SRC_ON
47 LCD_BKL_EN
Inverter power
80 mil
FBMA-L11-201209-221LMA30T_0805
FDC654P: P CHANNAL
Panel backlight power control by EC
INy_AEQ# (y=1, 2),Automatic RX equalization enable
L:Disable input automatic equalization
H:Enable input automatic equalization
INy_PEQ(y = 1, 2),Programmable input equalization level setting
L:Low EQ setting (LEQ), default
H:High EQ setting (HEQ)
M:No EQ
CFG_OUTPUT: output configuration
L:Output is tracking DPCD register setting (auto interception)
H:Output swing level fixed at 600mV and no pre-emphasis
M:Output swing level is fixed at 400mV and no pre-emphasis
CFG_HPD,HPD switching configuration
L:HPD is switched by SW_ML
H:HPD is switched by SW_AUX
M:HPD is switched with overlap
CPU/GPU & 4028 SW for DPB
U131
PS8321QFN56GTR-A0_QFN56_7X7
4028
CPU/MXM
AUX_SEL/SEL1&2
Chanel
Source
0
A
4028
1
B
CPU/MXM
JEDP1
CONN@
I-PEX_20505-044E-011G~D
Link Done
0908 pin 28 with new feature, different with ex-version
Reserve
L100 BLM18BB221SN1D_2P~D
IP4223CZ6_SO6~D
DLW21SN900SQ2L_0805_4P~D
21,
Close to JEDP1
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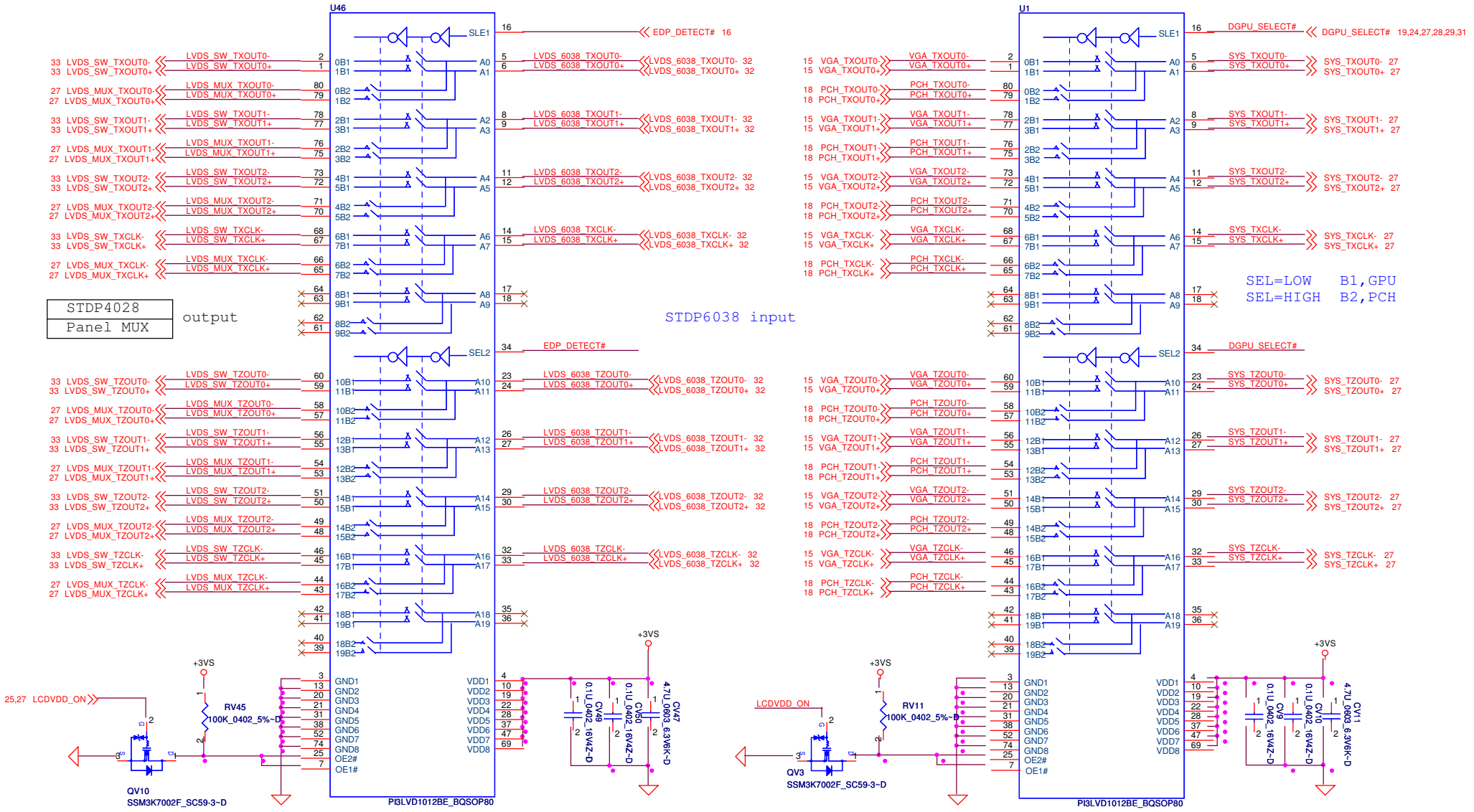
eDP SW- 4028 & eDP CONN
LA-8341P
Rev 1.0
Friday, March 02, 2012
Sheet 26 of 71

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS

SEL	Y
L	GPU
H	PCH



SEL	Y
L	STDP4028
H	Panel MUX

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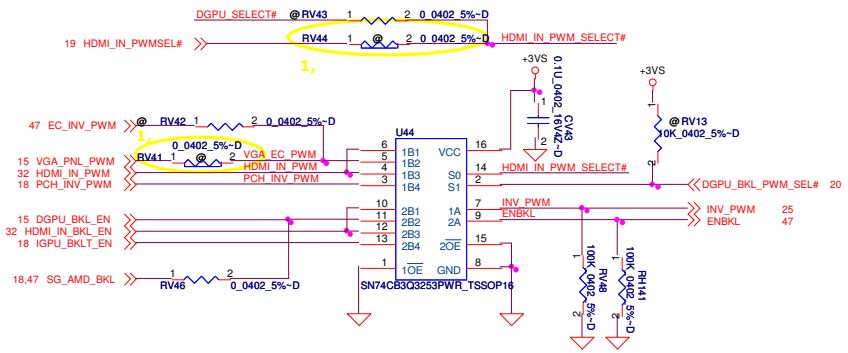
Title: LVDS SW- 1 to 2 & GPU/PCH

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 27 of 71

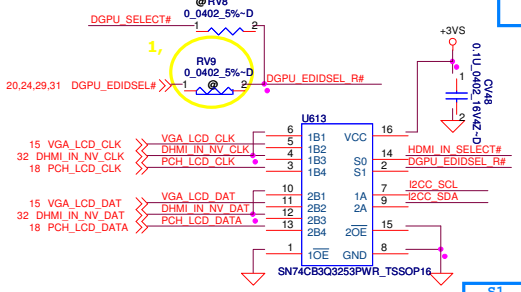
LCD Backlight Selector

PCH/GPU MUX & 6038 MUX SW for LVDS

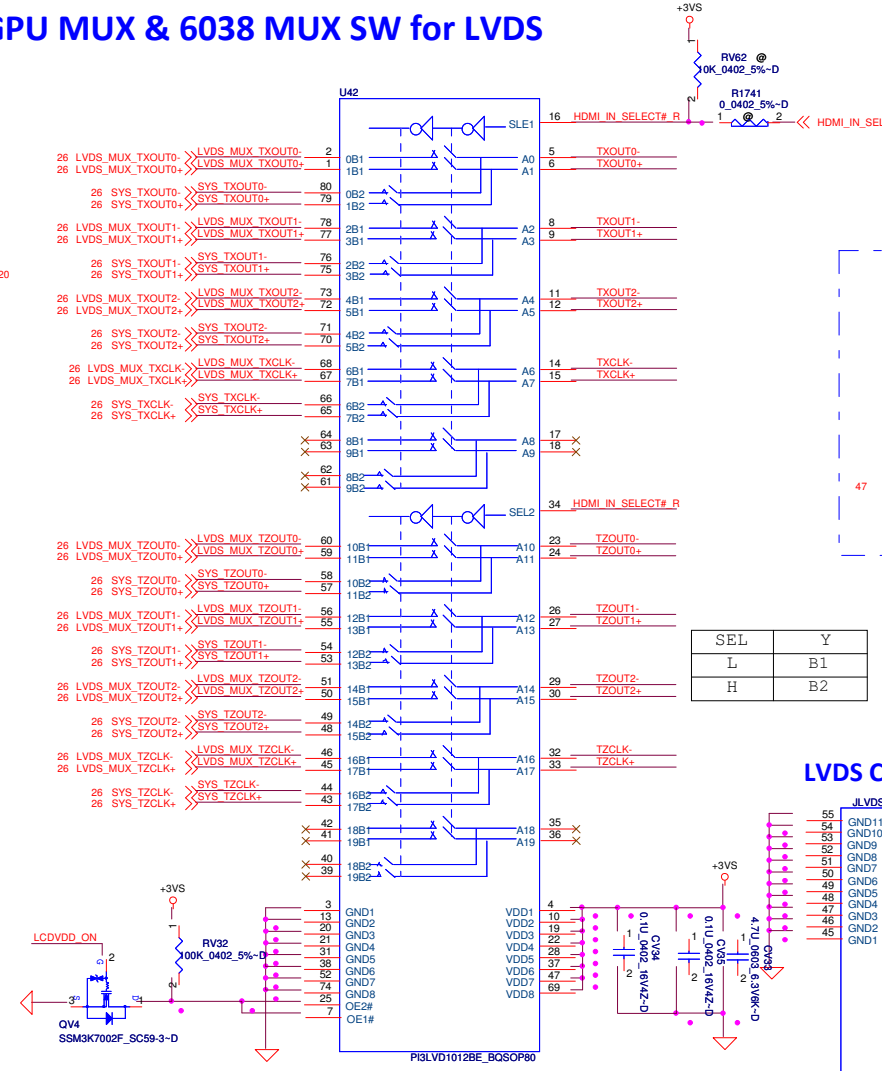


S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA

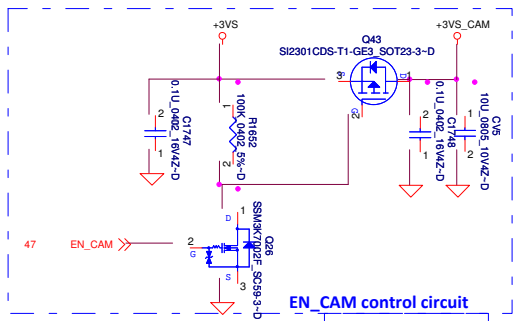
LCD DDC Selector

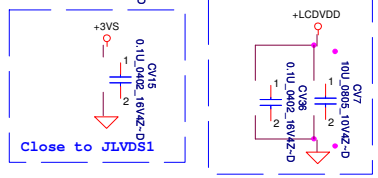


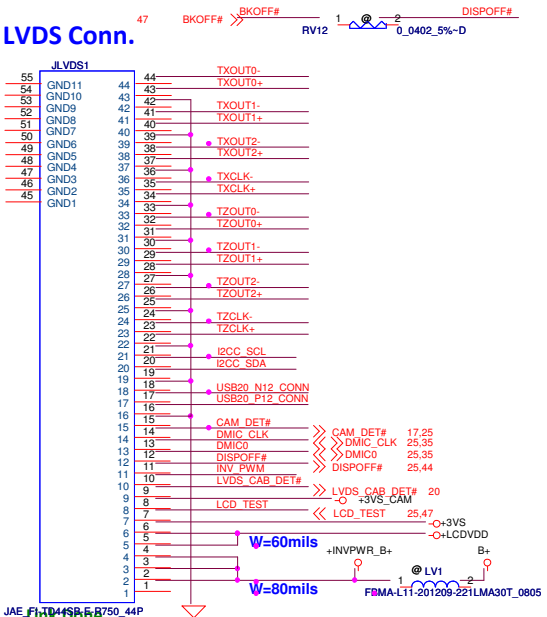
S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA



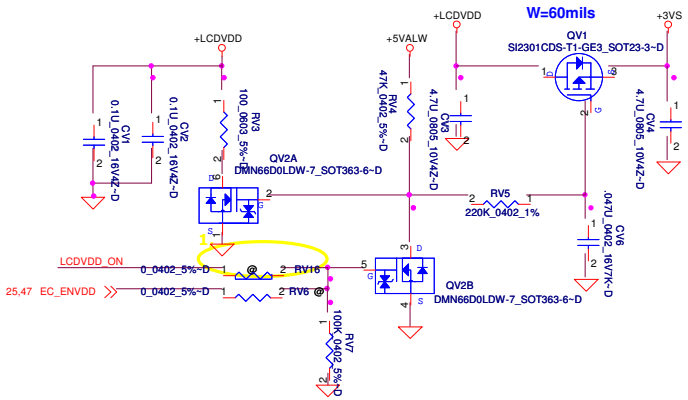
SEL	Y
L	B1
H	B2

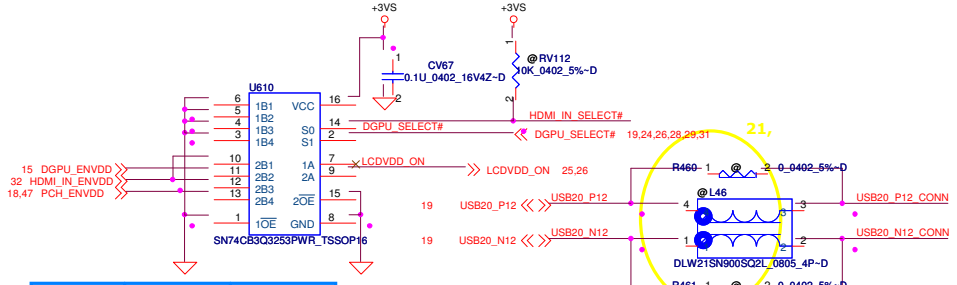






LCD POWER





S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN
1	1	1B4 2B4	UMA

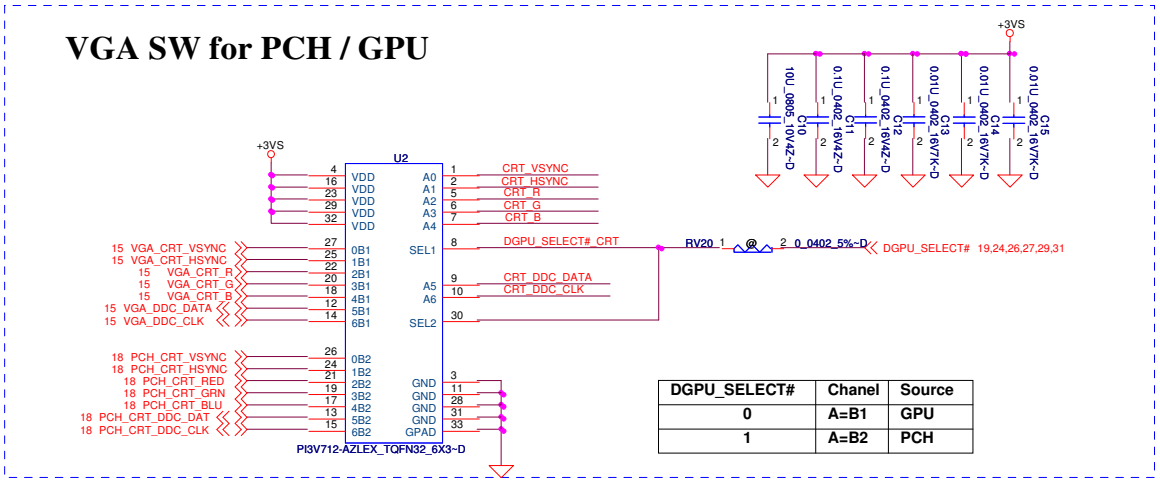
Compal Electronics, Inc.

Title: LVDS SW- 6038/SYSTEM & CONN

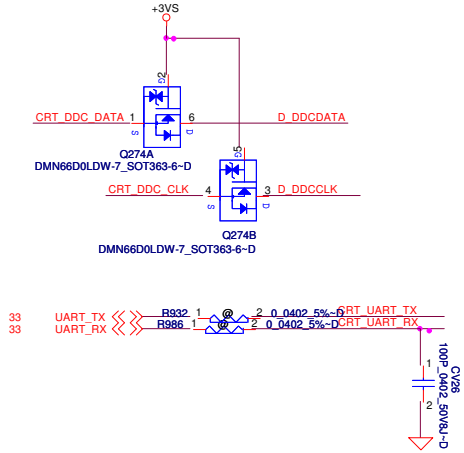
Size: | Document Number: LA-8341P | Rev: 1.0

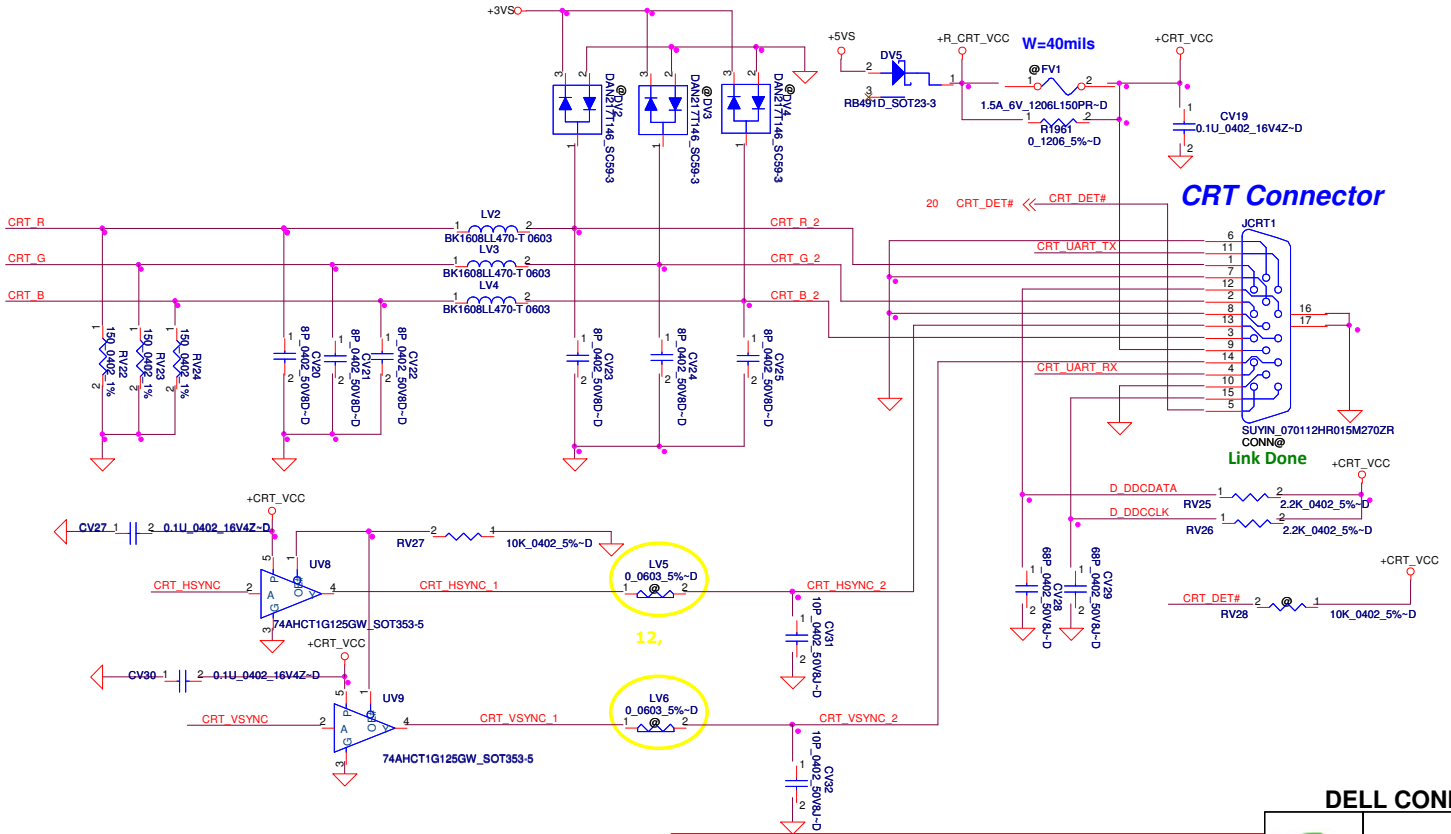
Date: Friday, March 02, 2012 | Sheet 28 of 71

VGA SW for PCH / GPU



DGPU_SELECT#	Chanel	Source
0	A=B1	GPU
1	A=B2	PCH





Compal Electronics, Inc.

Title: CRT SW

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 29 of 71

PS8271
PEQ=L, Middle level receiving equalization selection
PEQ=H, High level receiving equalization selection
PEQ=M, Low level receiving equalization selection

PS121
When DDCBUF_EN# is HIGH, the DDC channel is disabled, SCL/SDA and SCLZ/SDAZ are disconnected

PS121 CFG0/ CFG1
SCLZ/SDAZ output voltage select;
CFG1:0=00 LOW-level input voltage: <0.40V LOW-level output voltage: 0.60V
PS121 PC0/PC1/PC2
Inputs equalization control, default inputs equalization setting at 12 dB
000: 12 dB, 001: 16 dB, 010: 10 dB, 011: 7 dB
100: 1.5 dB, 101: 4 dB, 110: 9 dB, 111: 7 dB

HDMI_SW_DET	0	1
Y	IN1	IN2
	MXM	PCH

8/25 change RV53 from 430 to 499ohm

W=40mils

Place LC Filte closed to JHDMI

HDMI Connector output

Reserve for EMI please close to JHDMI2

CIS link OK

Compal Electronics, Inc.

Title: HDMI SW

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 30 of 71

DP Redriver

PCH/GPU AUX&LANE SW for DPB

17, Change P/N, mfr. P/N, value, part description

DGPU_EDIDSEL#_R	Chanel	Source
0	B1	GPU
1	B2	PCH

SW_AUX	Chanel	Source
0	IN1	GPU
1	IN2	PCH

DGPU_SEL#	Chanel	Source
0	NC	GPU
1	NO	PCH

MXM_MFG_SEL	GPU Source
0	NVDIA
1	ATI

Near to NV

Place close JDP1

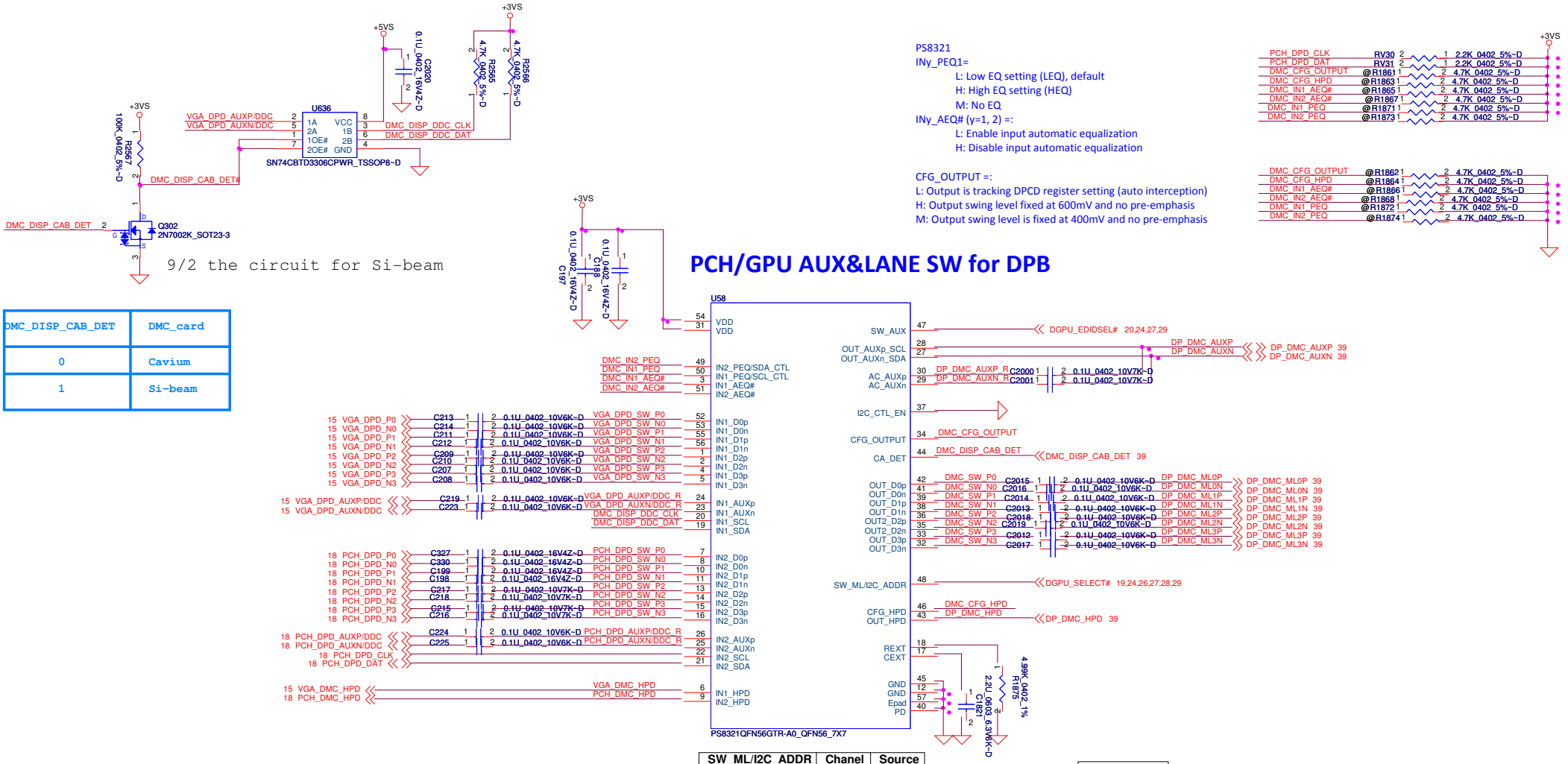
Link Done

Compal Electronics, Inc.

Title: DP SW for mDP CONN

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 31 of 71



DMC_DISP_CAB_DET	DMC_card
0	Cavium
1	Si-beam

SW_ML/I2C_ADDR	Chanel	Source
0	IN1	GPU
1	IN2	PCH

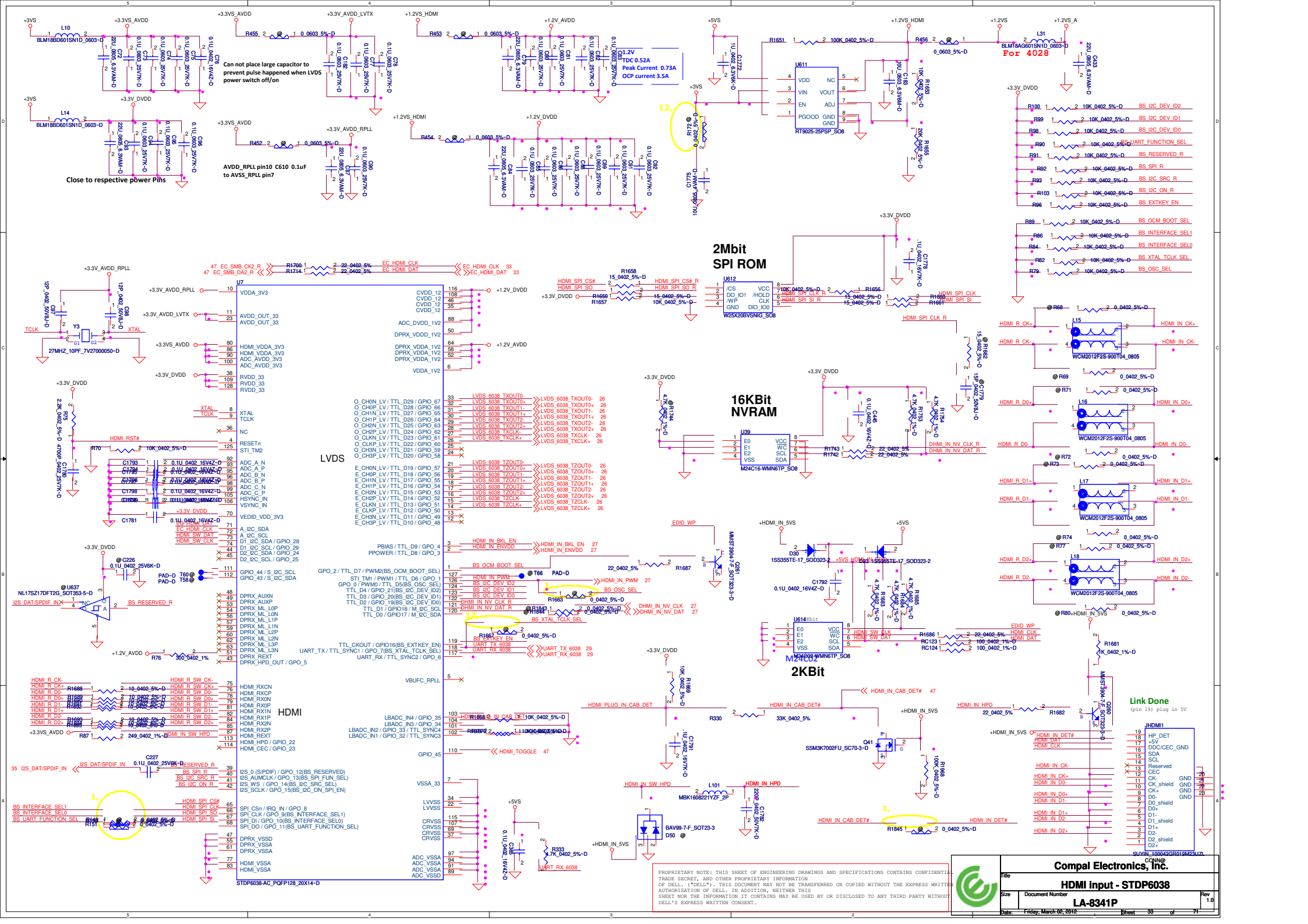
MXM_MFG_SEL	GPU Source
0	NVDIA
1	ATI

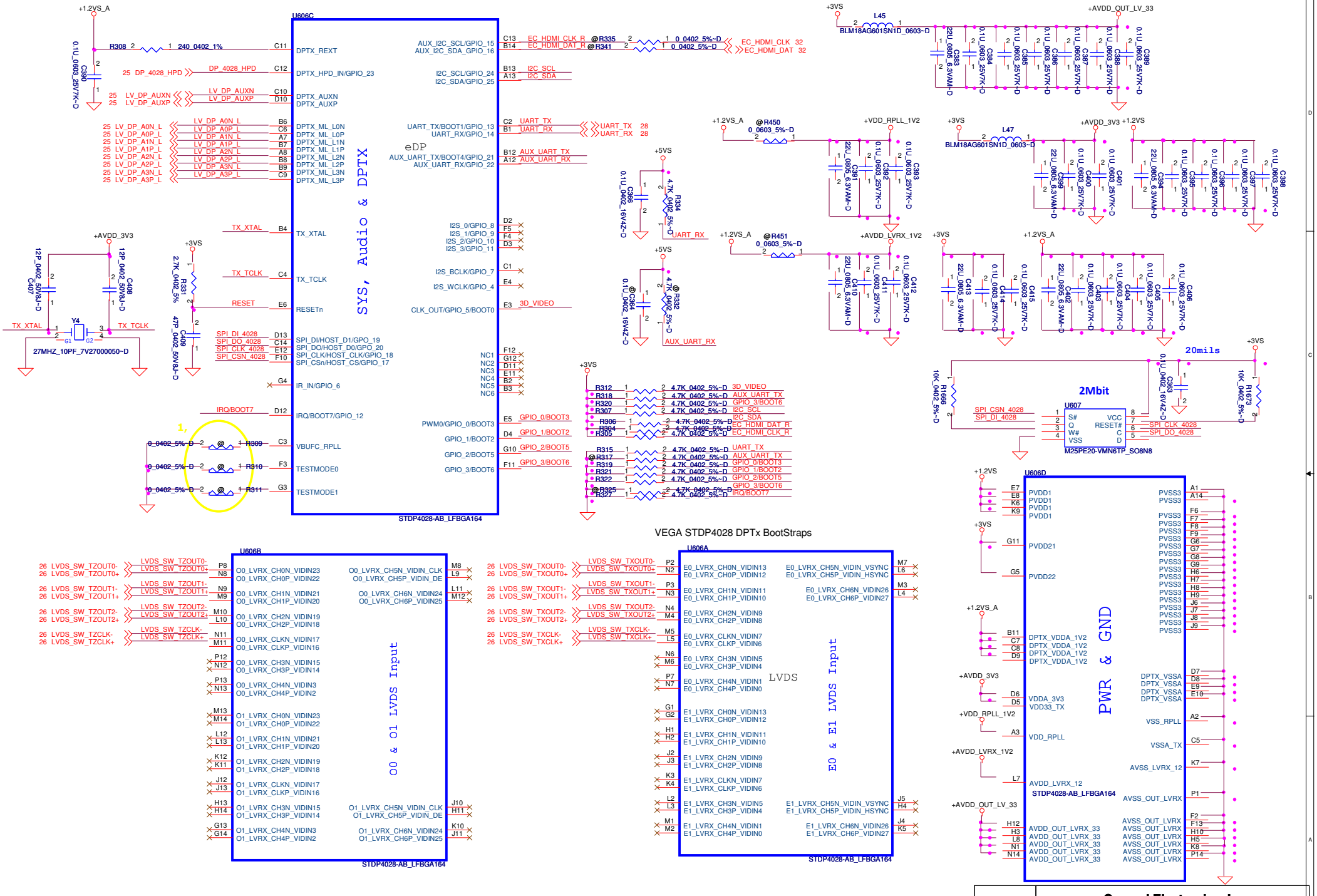
Compal Electronics, Inc.

Title: HDMI SW for DMC

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 32 of 71


Can not place large capacitor to prevent pulse happened when LVDS power switch off/on
Close to respective power Pins
AVDD_RPLL pin10 C610 0.1uF to AVSS_RPLL pin7
1.2V TDC 0.52A Peak Current 0.73A OCP current 3.5A
For 4028
2Mbit SPI ROM
16KBit NVRAM
2KBit
HDMI
LVDS
Link Done
Compal Electronics, Inc.
HDMI input - STDP6038
LA-8341P
Friday, March 02, 2012



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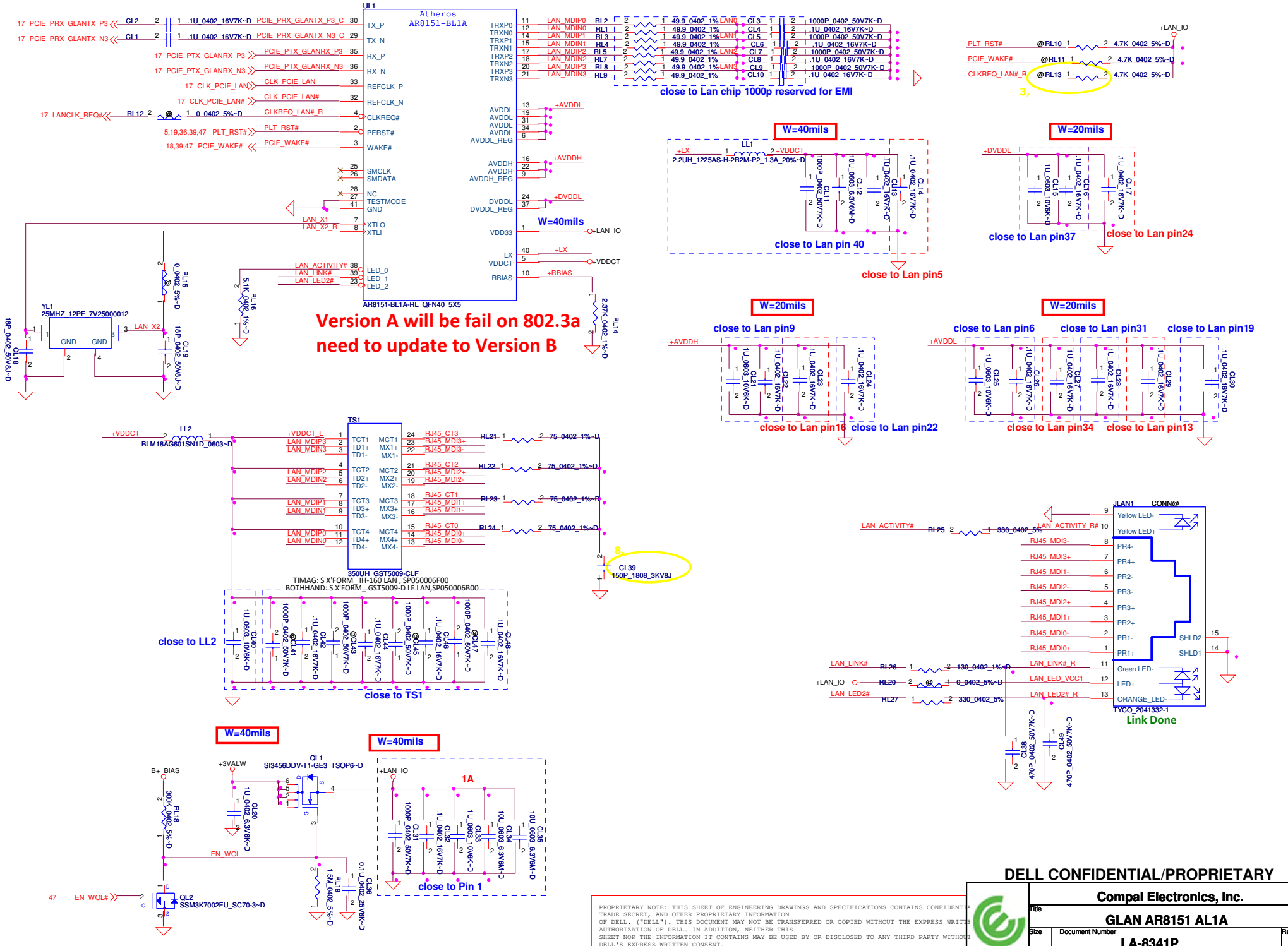
Compal Electronics, Inc.	
Title	LVDS transfer eDP-STDP4028
Size	Document Number: LA-8341P
Rev	1.0
Date:	Friday, March 02, 2012
Sheet	34 of 71


UL1
Atheros
AR8151-BL1A
AR8151-BL1A-RL_QFN40_5X5
close to Lan chip 1000p reserved for EMI
W=40mils
W=20mils
close to Lan pin 40
close to Lan pin5
close to Lan pin37
close to Lan pin24
close to Lan pin9
close to Lan pin16
close to Lan pin22
close to Lan pin6
close to Lan pin31
close to Lan pin19
close to Lan pin34
close to Lan pin13
Version A will be fail on 802.3a
need to update to Version B
TS1
350UH_GST5009-CLF
close to LL2
close to TS1
JLAN1
CONN@
TYCO_2041332-1
Link Done
QL1
SI3456DDV-T1-GE3_TSOP6~D
QL2
SSM3K7002FU_SC70-3~D
1A
close to Pin 1
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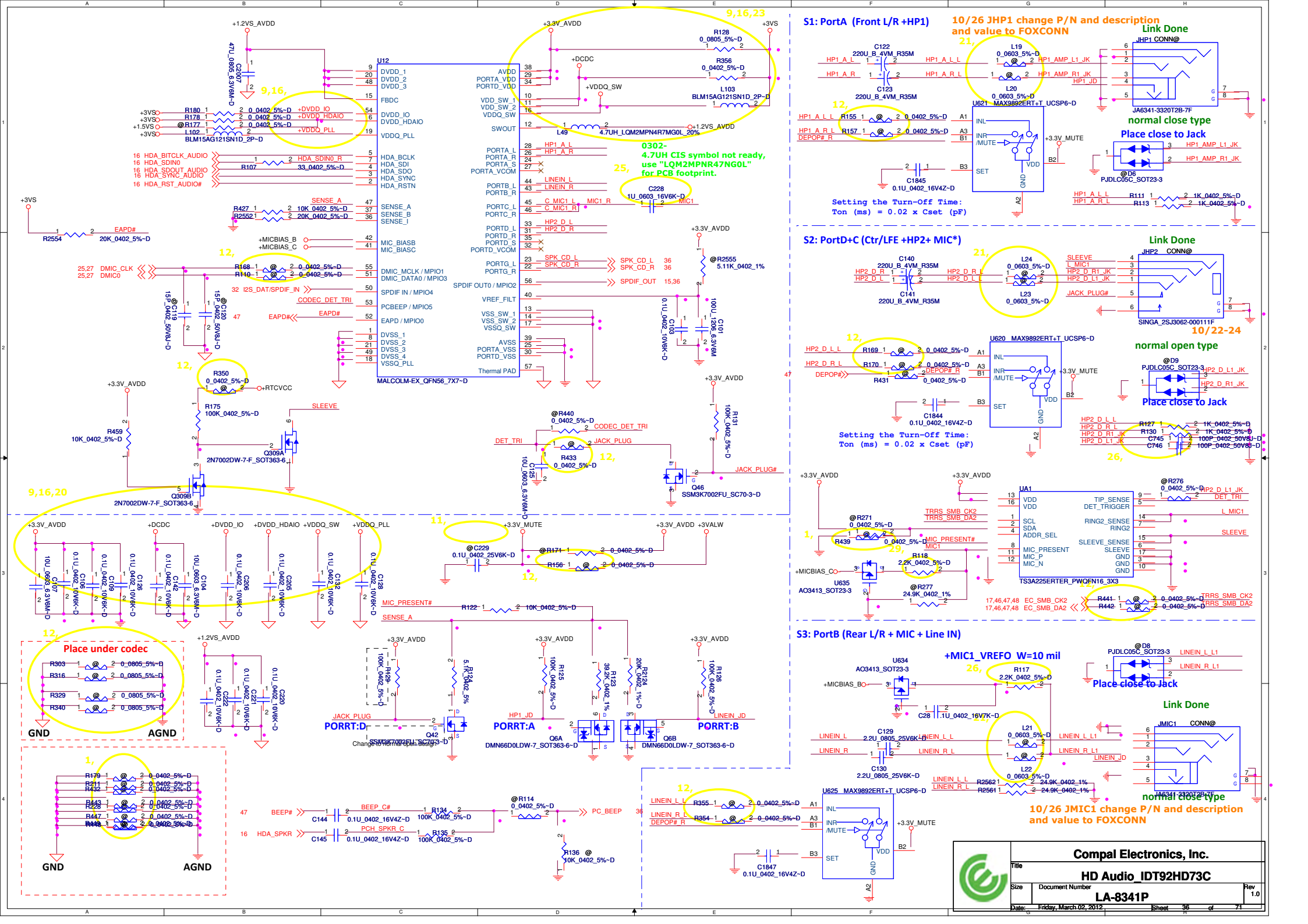
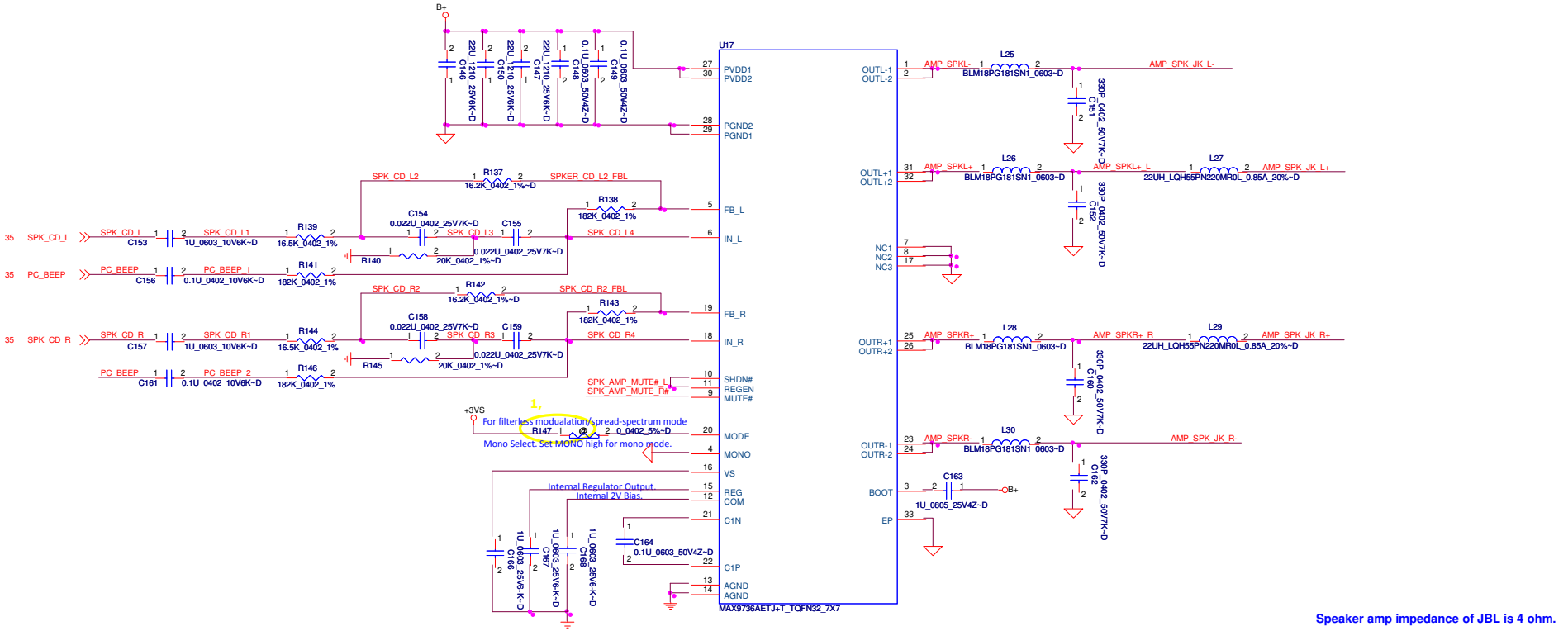
Compal Electronics, Inc.
GLAN AR8151 AL1A
LA-8341P
Friday, March 02, 2012
35 of 71

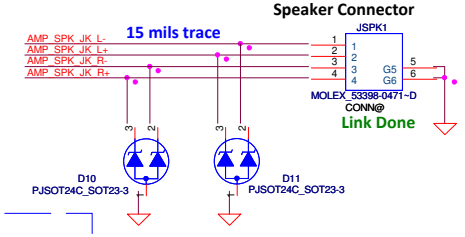

S1: PortA (Front L/R +HP1)
10/26 JHP1 change P/N and description and value to FOXCONN
Link Done
normal close type
Place close to Jack
Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)
S2: PortD+C (Ctr/LFE +HP2+ MIC*)
Link Done
10/22-24
normal open type
Place close to Jack
Setting the Turn-Off Time:
Ton (ms) = 0.02 x Cset (pF)
S3: PortB (Rear L/R + MIC + Line IN)
+MIC1_VREFO W=10 mil
Place close to Jack
Link Done
normal close type
10/26 JMIC1 change P/N and description and value to FOXCONN
0302-
4.7UH CIS symbol not ready,
use "LQM2MPNR47NG0L"
for PCB footprint.
Place under codec
GND
AGND
PORRT:D
PORRT:A
PORRT:B
Change to normal open design
MALCOLM-EX_QFN56_7X7~D
Compal Electronics, Inc.
HD Audio_IDT92HD73C
LA-8341P
Rev 1.0
Friday, March 02, 2012
Sheet 36 of 71



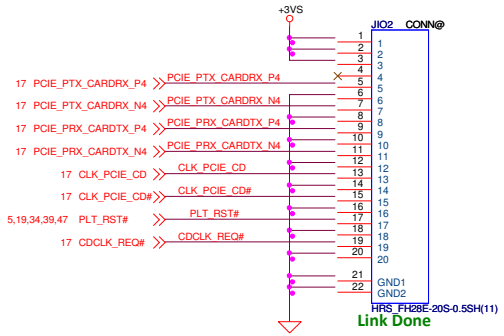
Layout note:
Please place below componets on moat between A GND and D GND.
(R119, R147, R155, R157, R158, R164)

Speaker amp impedance of JBL is 4 ohm.

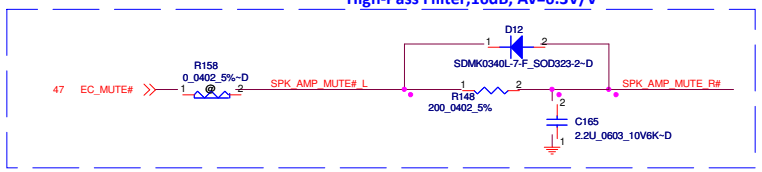
Speaker Connector



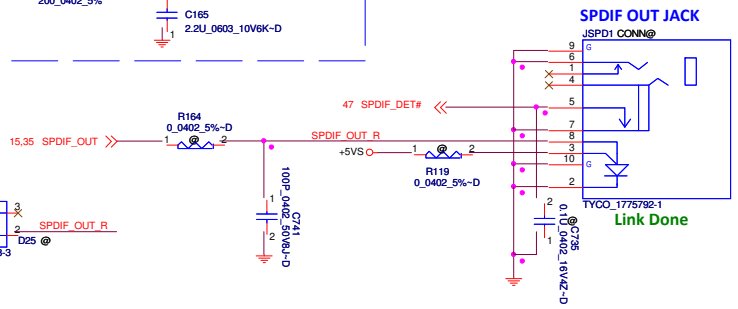
Card Reader/B CONN



High-Pass Filiter,16dB, Av=6.3V/V



SPDIF OUT JACK

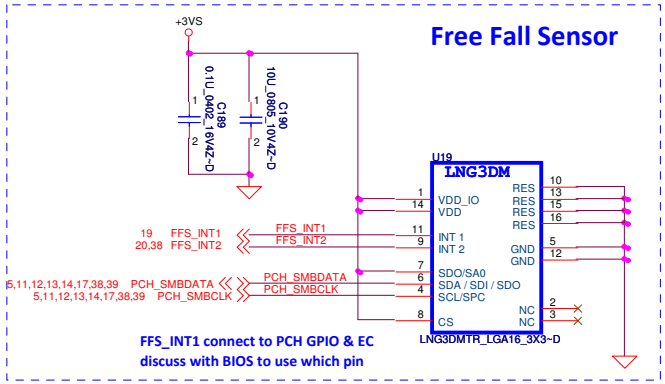


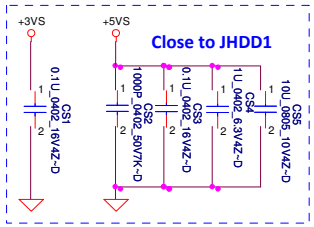
Compal Electronics, Inc.

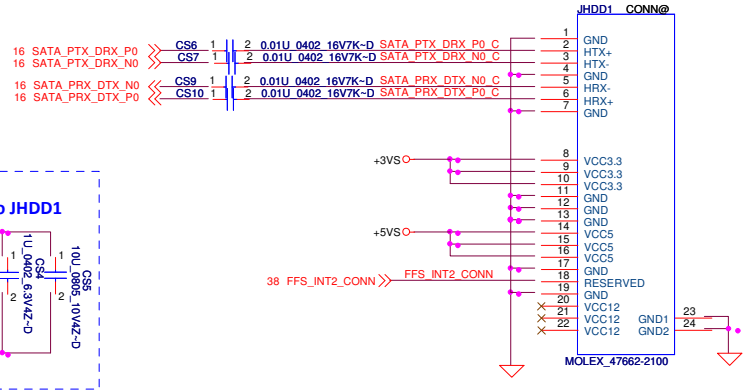
Title: Speaker AMP / CardReader_B conn

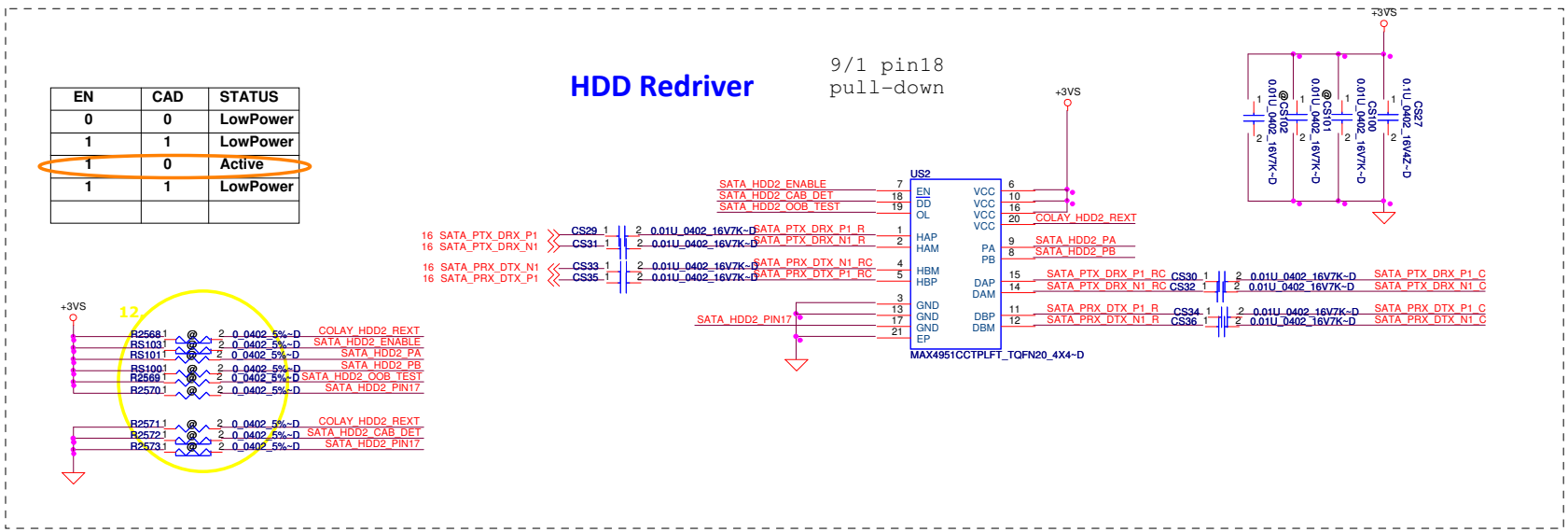
Size | Document Number: LA-8341P | Rev: 1.0

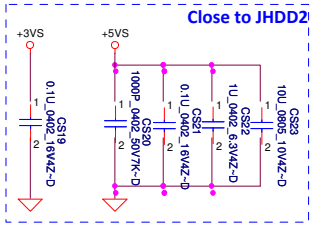
Date: Friday, March 02, 2012 | Sheet 37 of 71

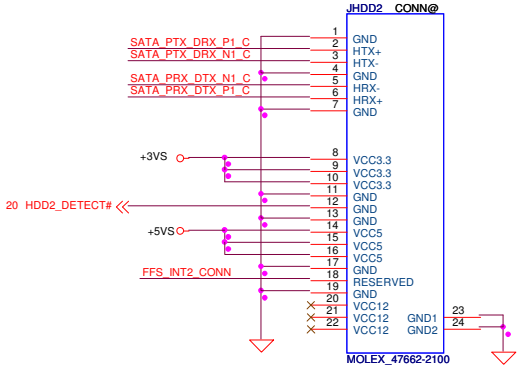












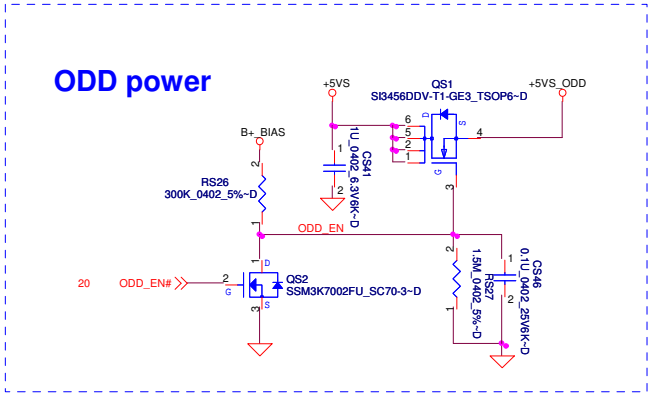
Compal Electronics, Inc.

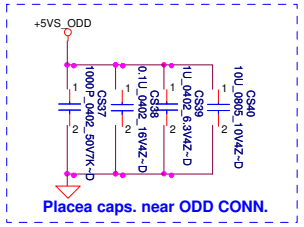
Title: SATA HDD1 & HDD2

Size: Document Number: LA-8341P Rev: 1.0

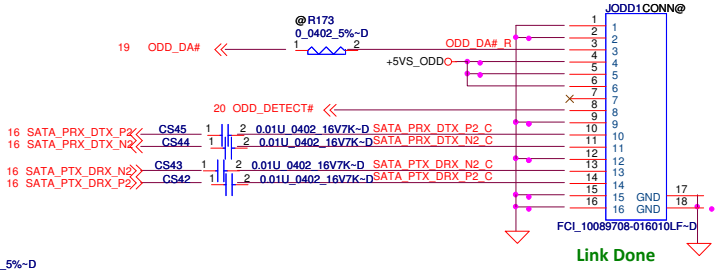
Date: Friday, March 02, 2012 Sheet 38 of 71

ODD power

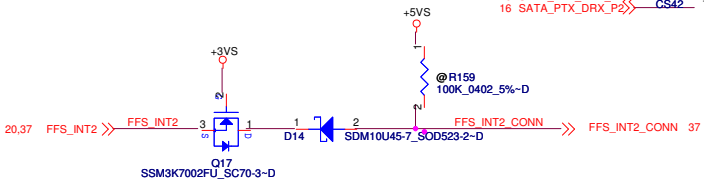


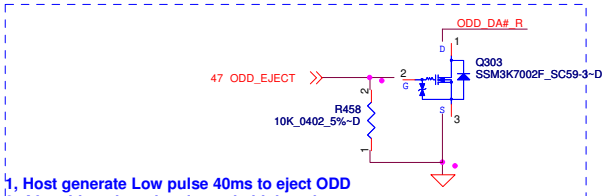


SATA ODD Conn.

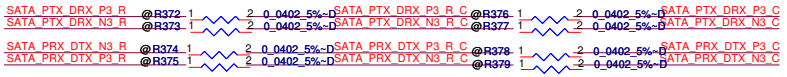


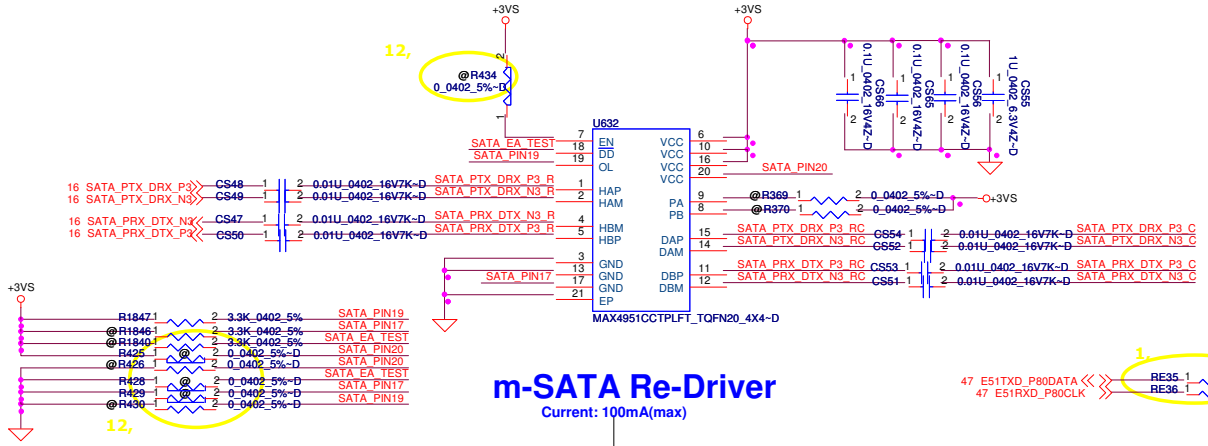
Link Done





9/5
follow JMINI1 connector usage

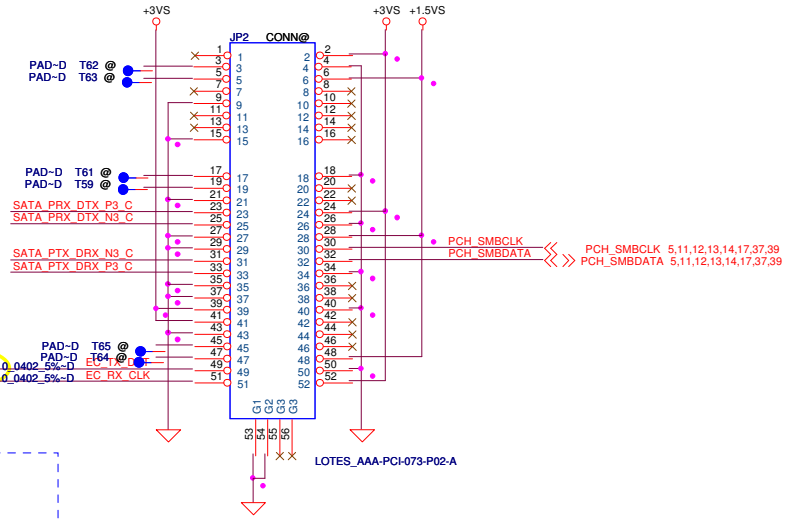


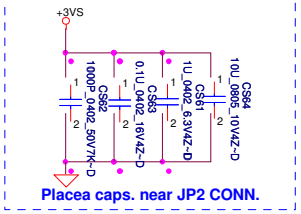


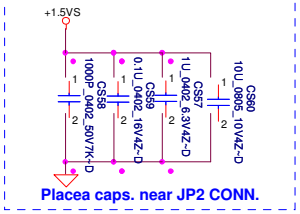
m-SATA Re-Driver

Current: 100mA(max)

Operating Supply Current
PA = PB = VCC, D10.2 pattern, f = 3GHz,
70mA(Typ)~100mA
PA = PB = GND, D10.2 pattern, f = 3GHz,
60mA(Typ)~85mA







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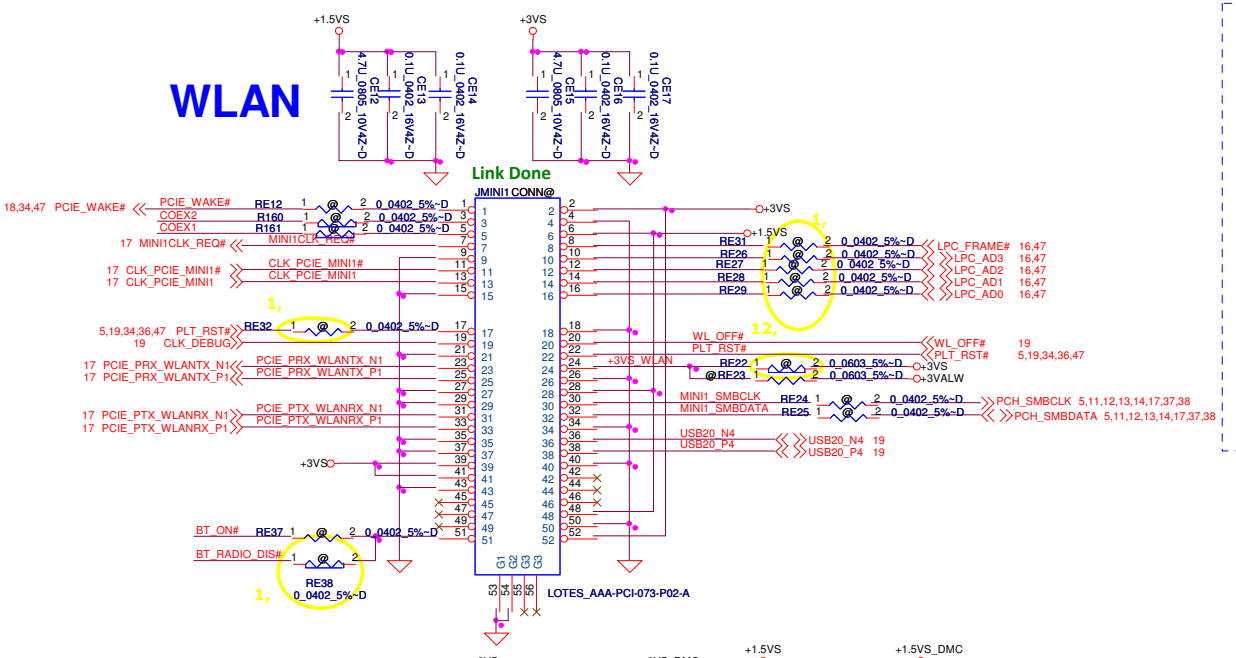
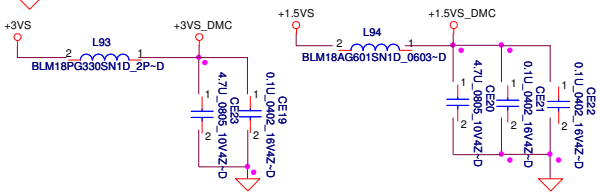
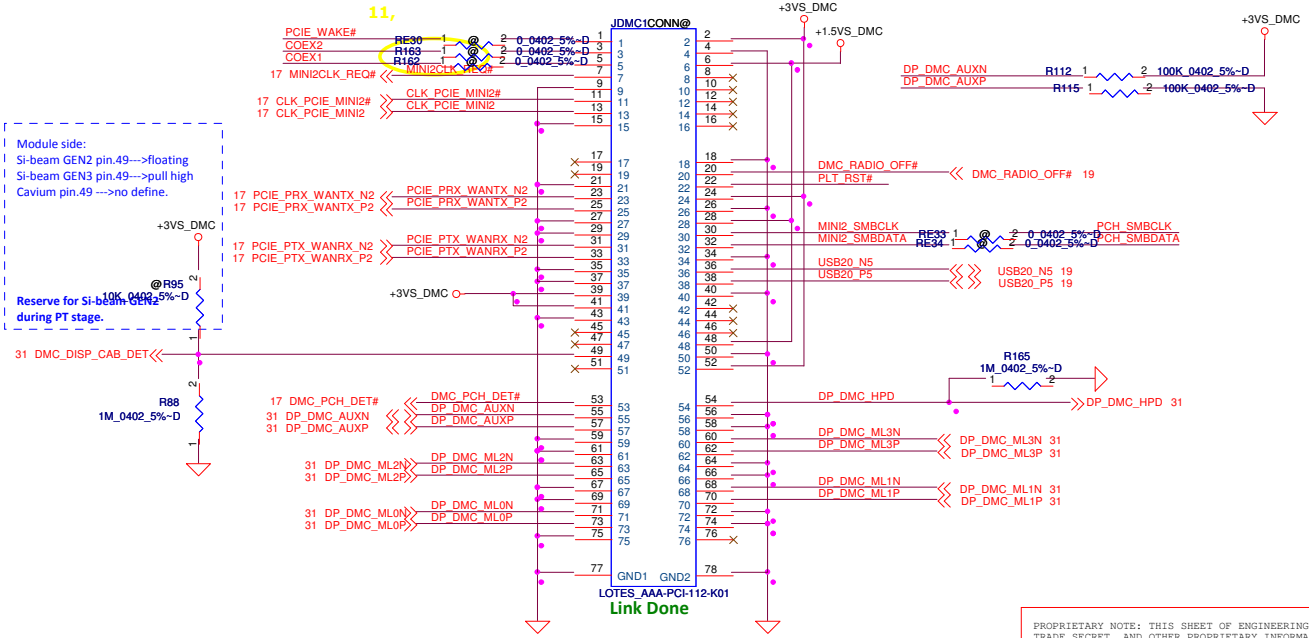
Compal Electronics, Inc.	
Title	SATA HDD3 & ODD & FFS
Size	Document Number: LA-8341P
Rev	1.0
Date: Friday, March 02, 2012	Sheet 39 of 71

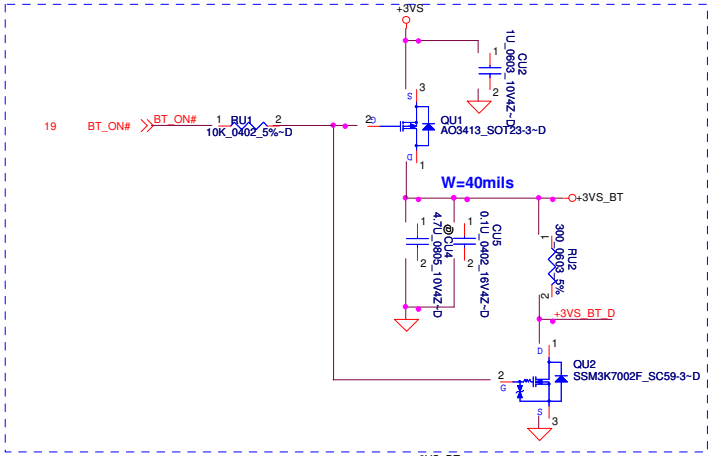
WLAN



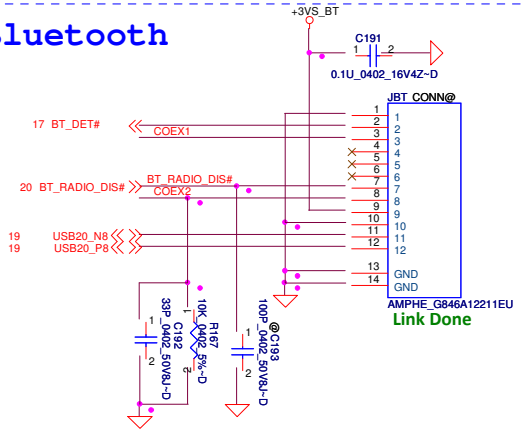


Display Mini Card (DMC)





Bluetooth

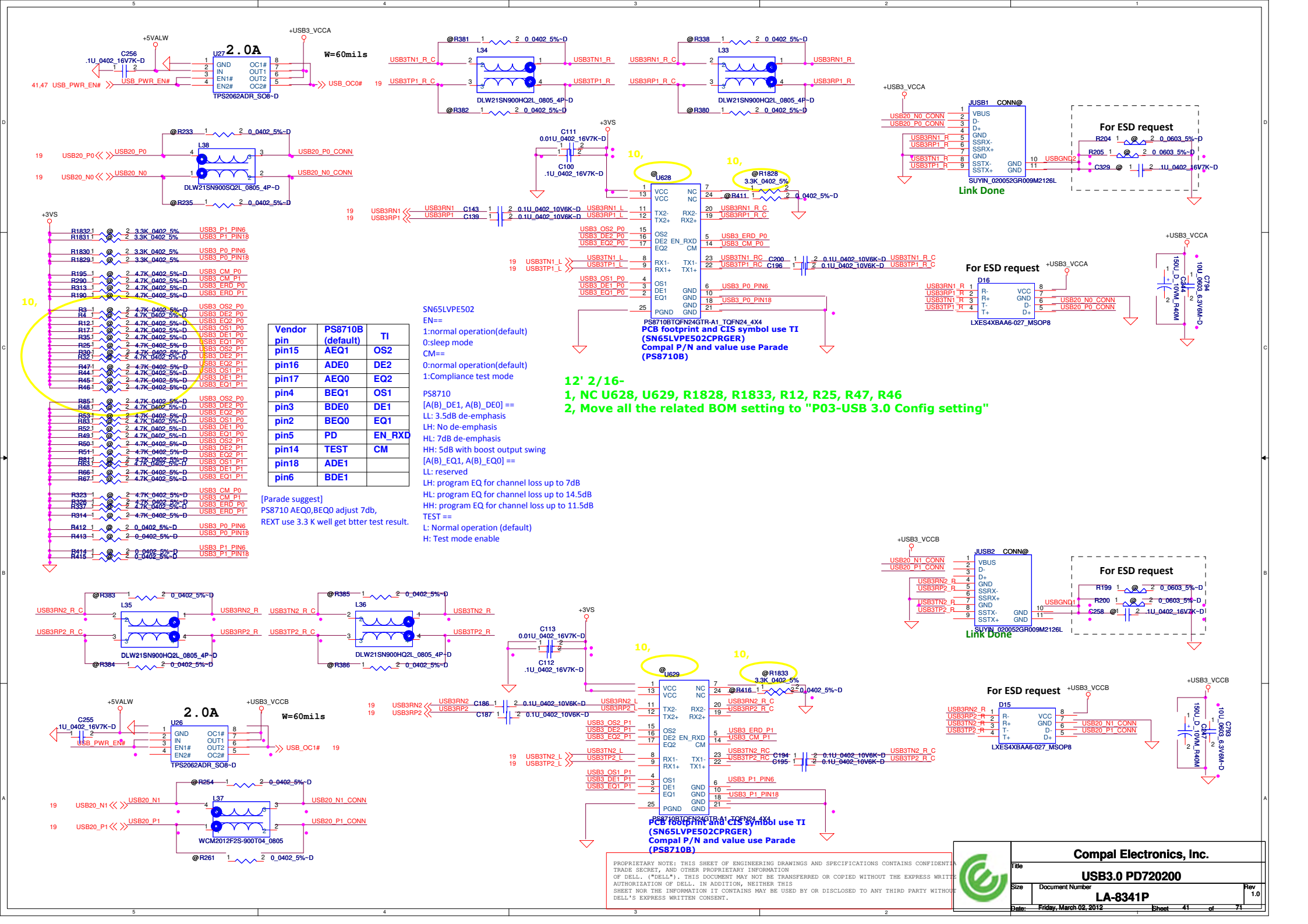


Compal Electronics, Inc.

Title: Mini Card WLAN / DMC / BT

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 40 of 71

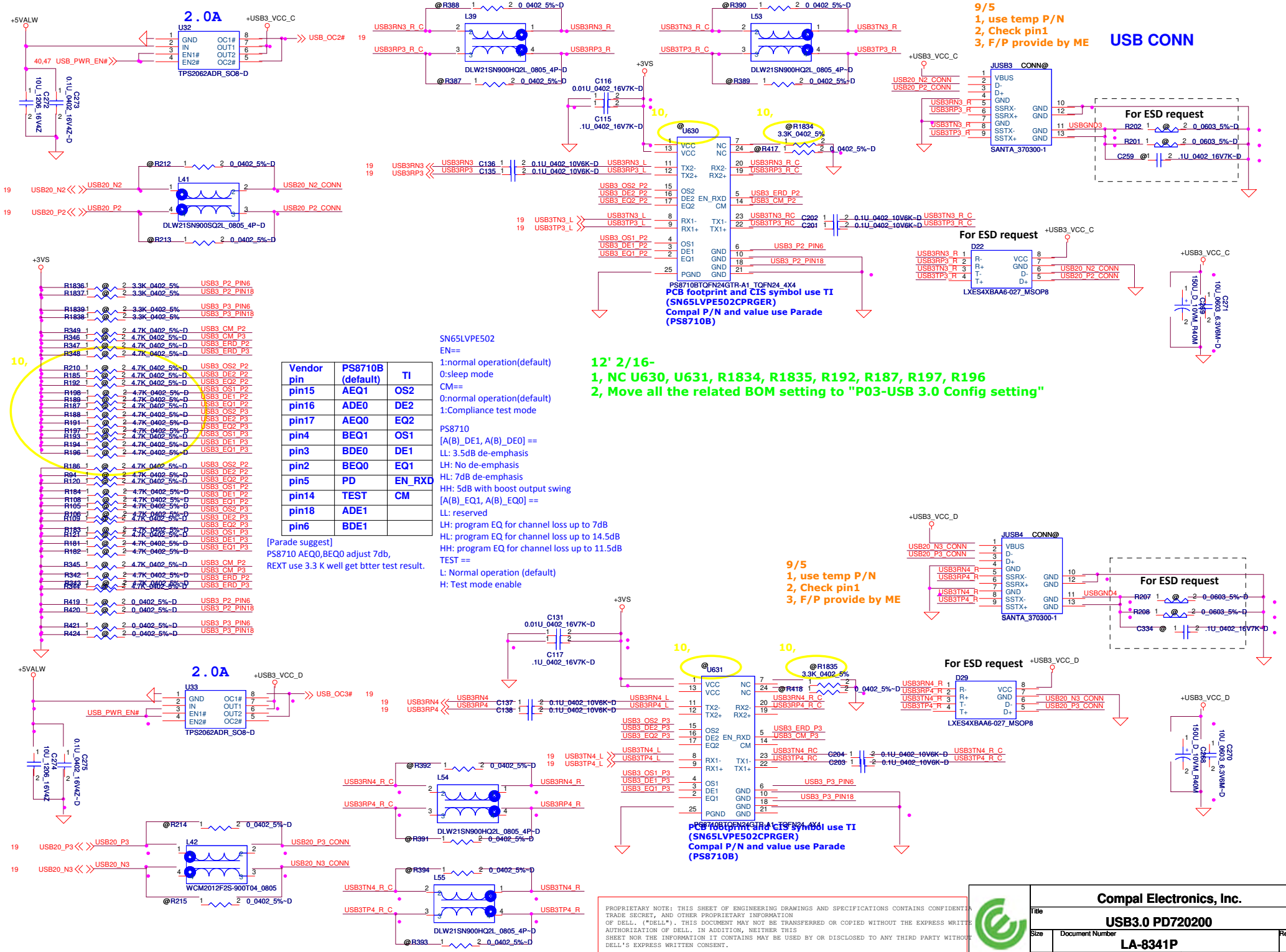


Compal Electronics, Inc.

Title: USB3.0 PD720200

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 41 of 71



Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

[Parade suggest]
PS8710 AEQ0,BEQ0 adjust 7db,
REXT use 3.3 K well get btter test result.

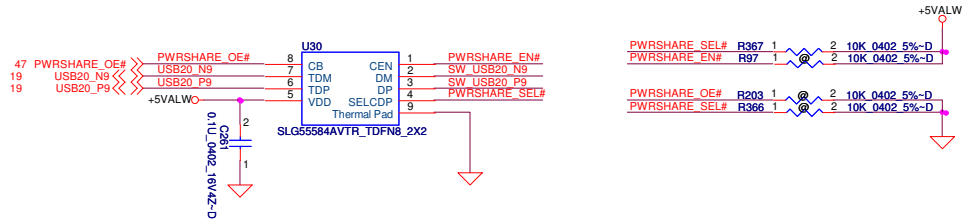
Compal Electronics, Inc.

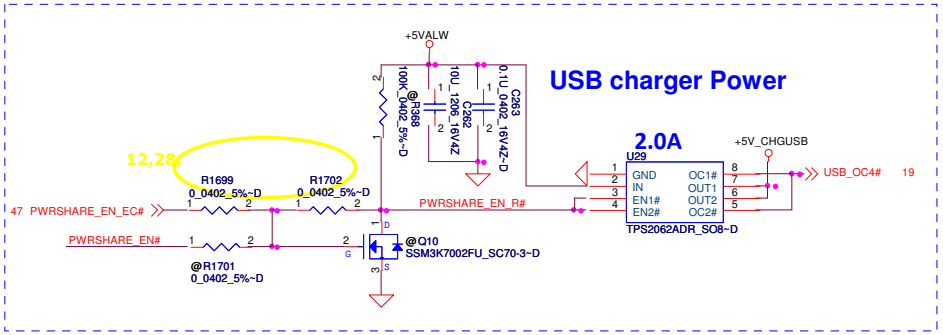
Title: USB3.0 PD720200

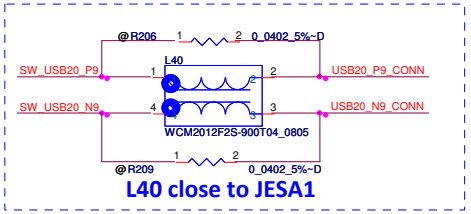
Size: | Document Number: LA-8341P | Rev: 1.0

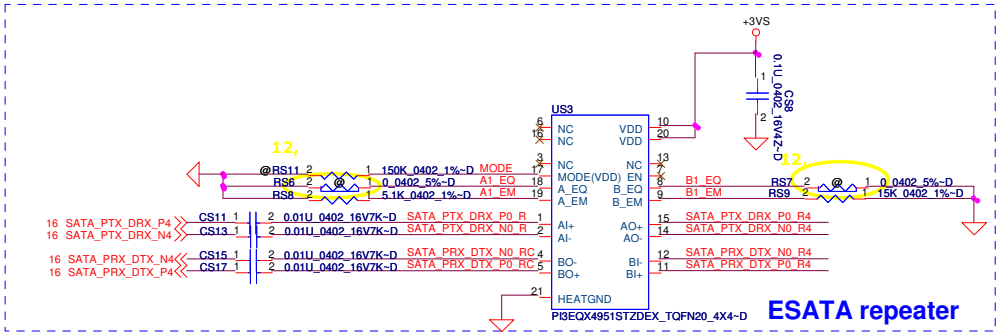
Date: Friday, March 02, 2012 | Sheet 42 of 71

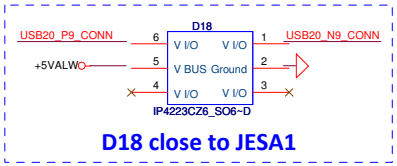
Power share









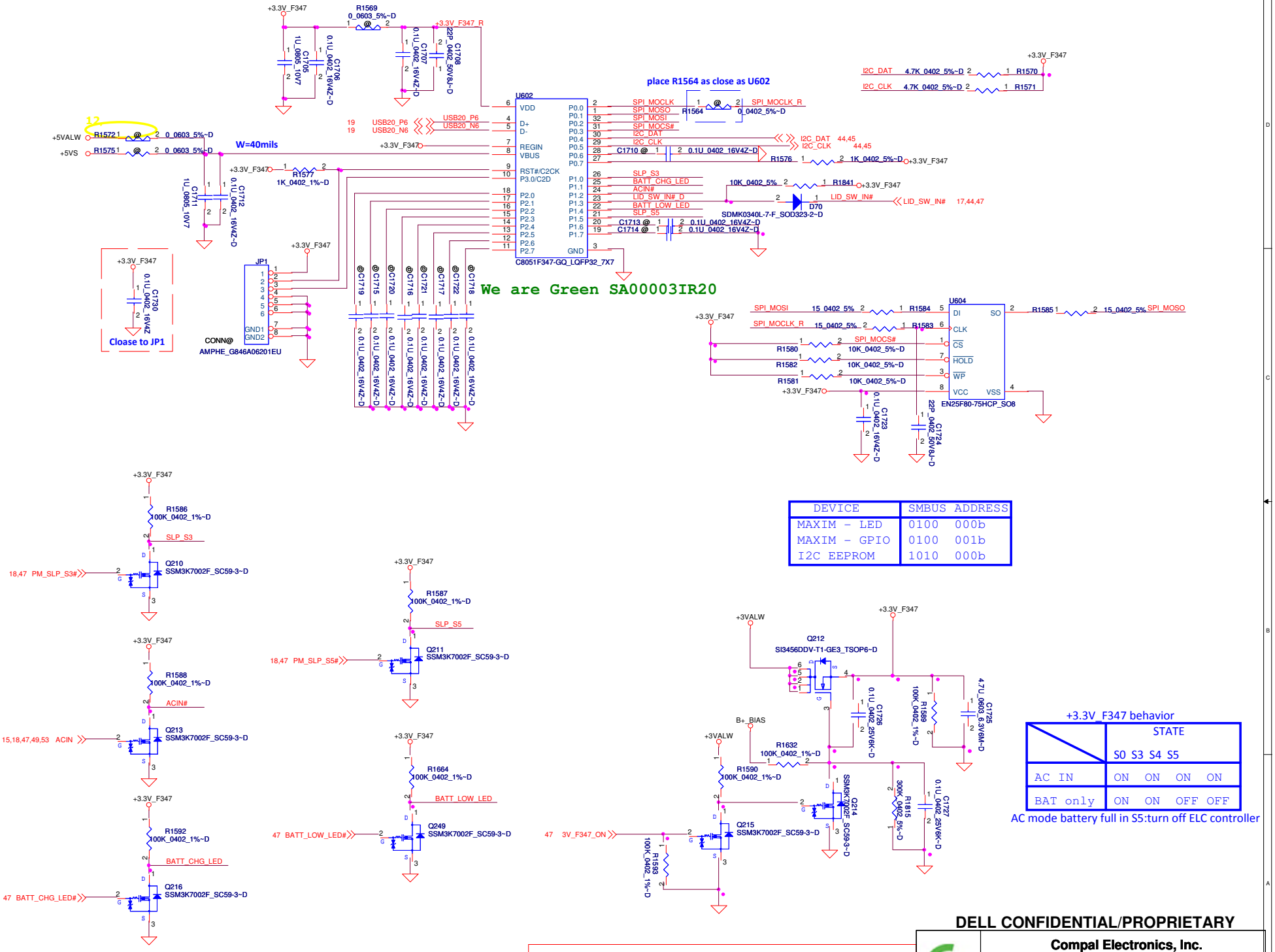


Compal Electronics, Inc.

Title: USB/ESATA TS3USB221RSER

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 43 of 71



DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

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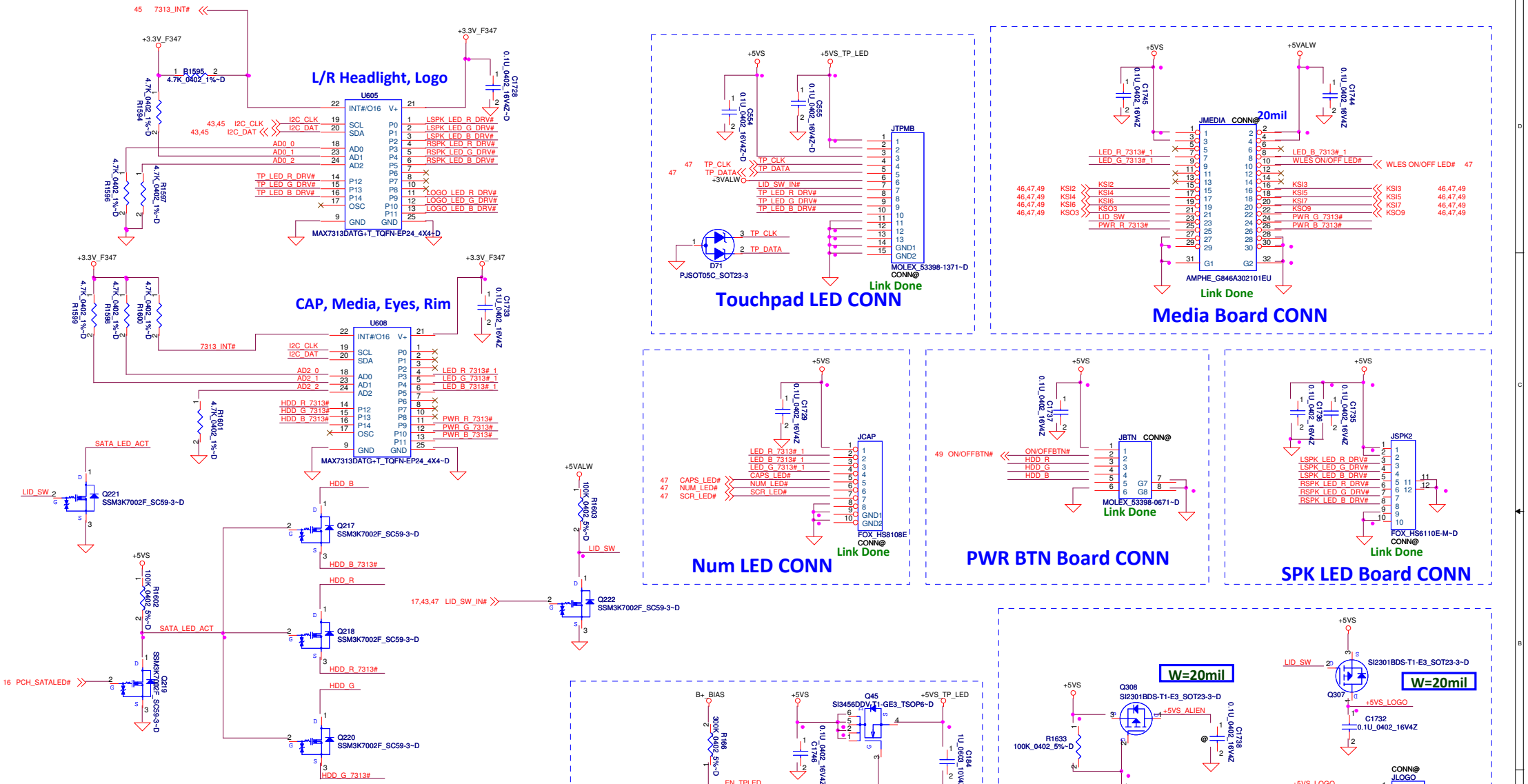
Compal Electronics, Inc.	
Title	ELC (1)
Size	Document Number: LA-8341P
Rev	1.0
Date:	Friday, March 02, 2012
Sheet	44 of 71



Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	L/R Headlight , Logo, TP
U608	0	1	1	Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim

Compal Electronics, Inc.

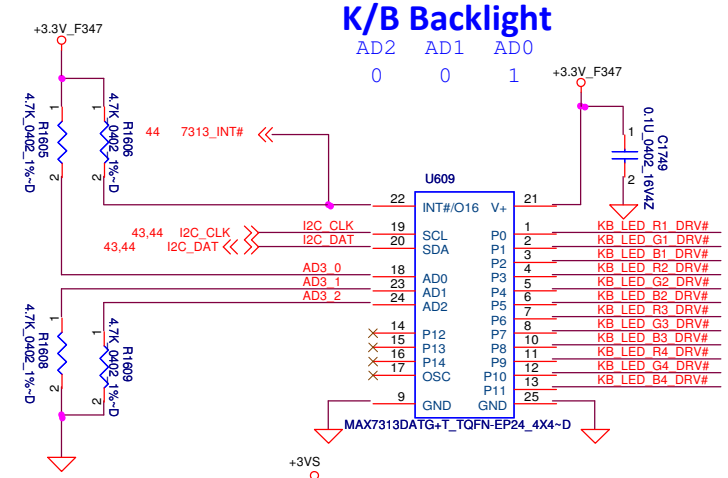
Title: ELC (2)

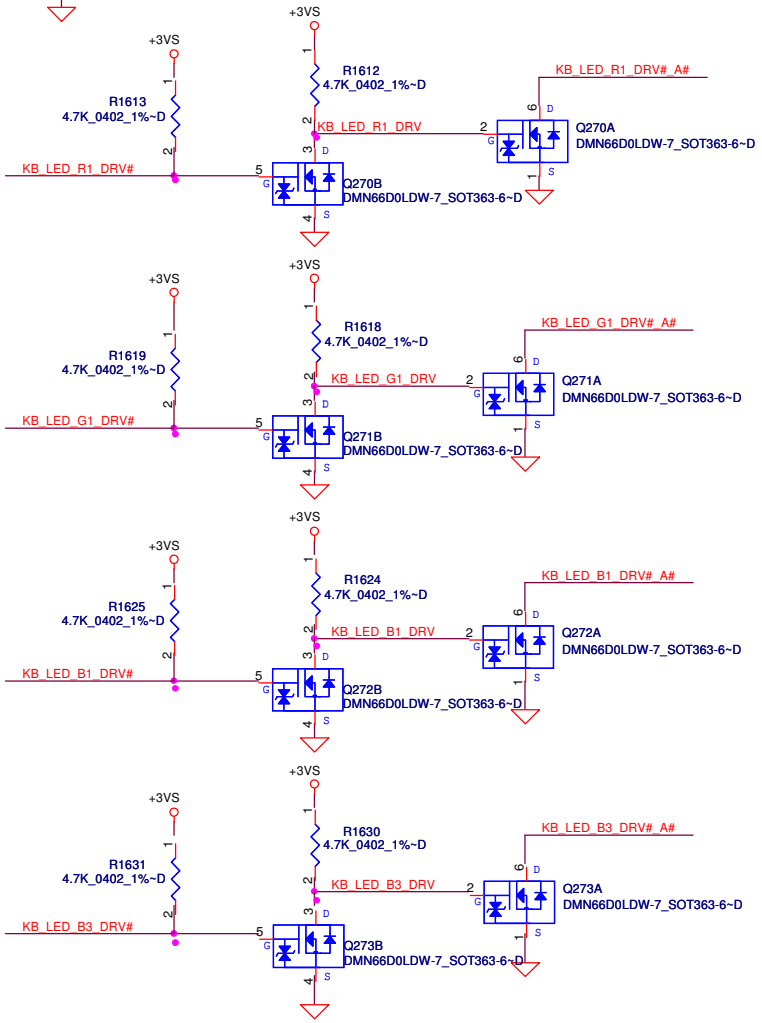
Size | Document Number: LA-8341P | Rev: 1.0

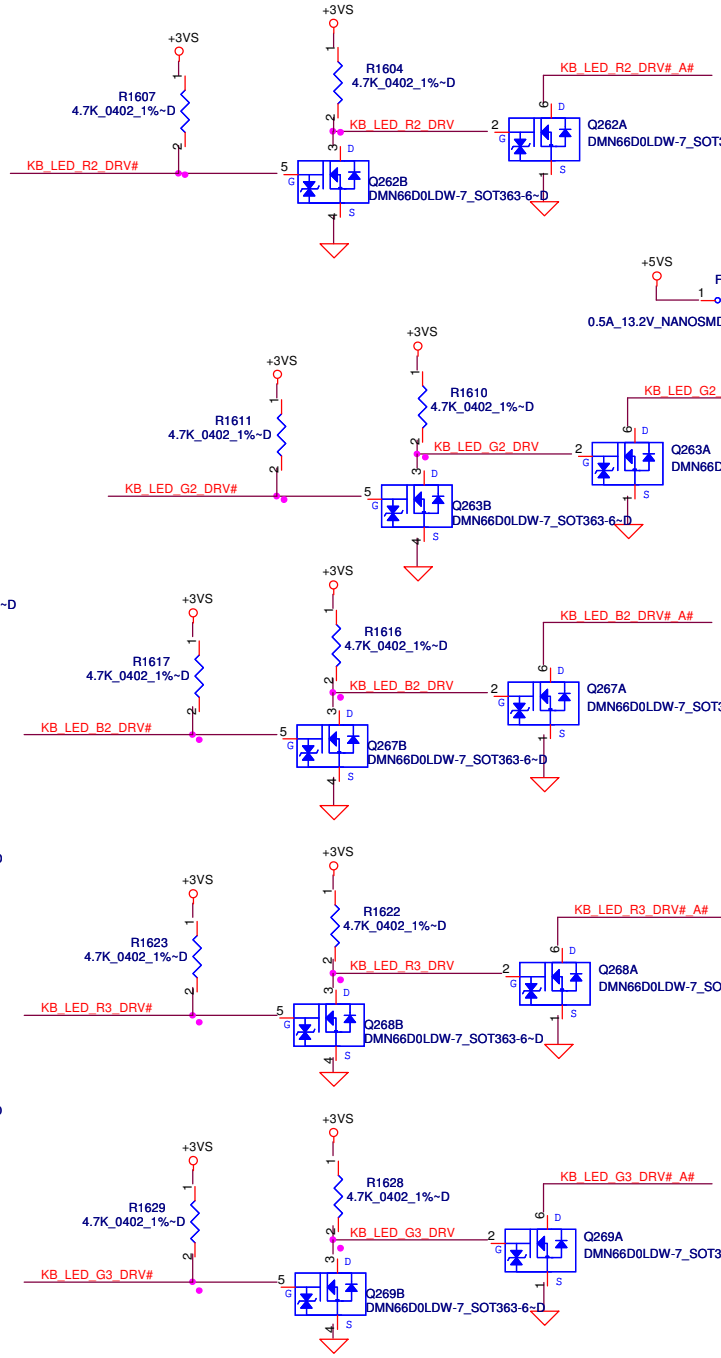
Date: Friday, March 02, 2012 | Sheet 45 of 71

K/B Backlight

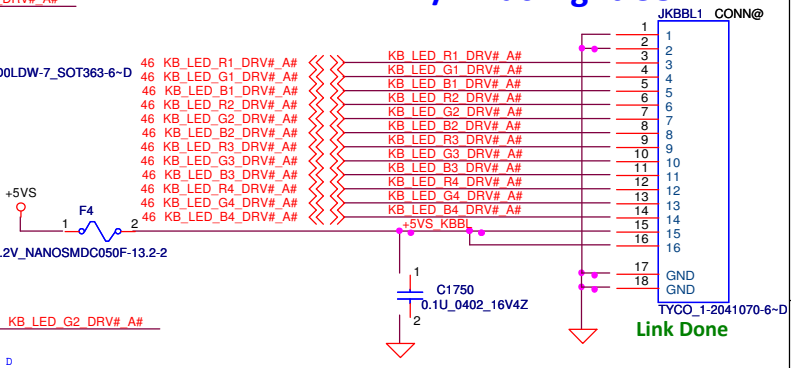
AD2 AD1 AD0
0 0 1







K/B Backlight CONN



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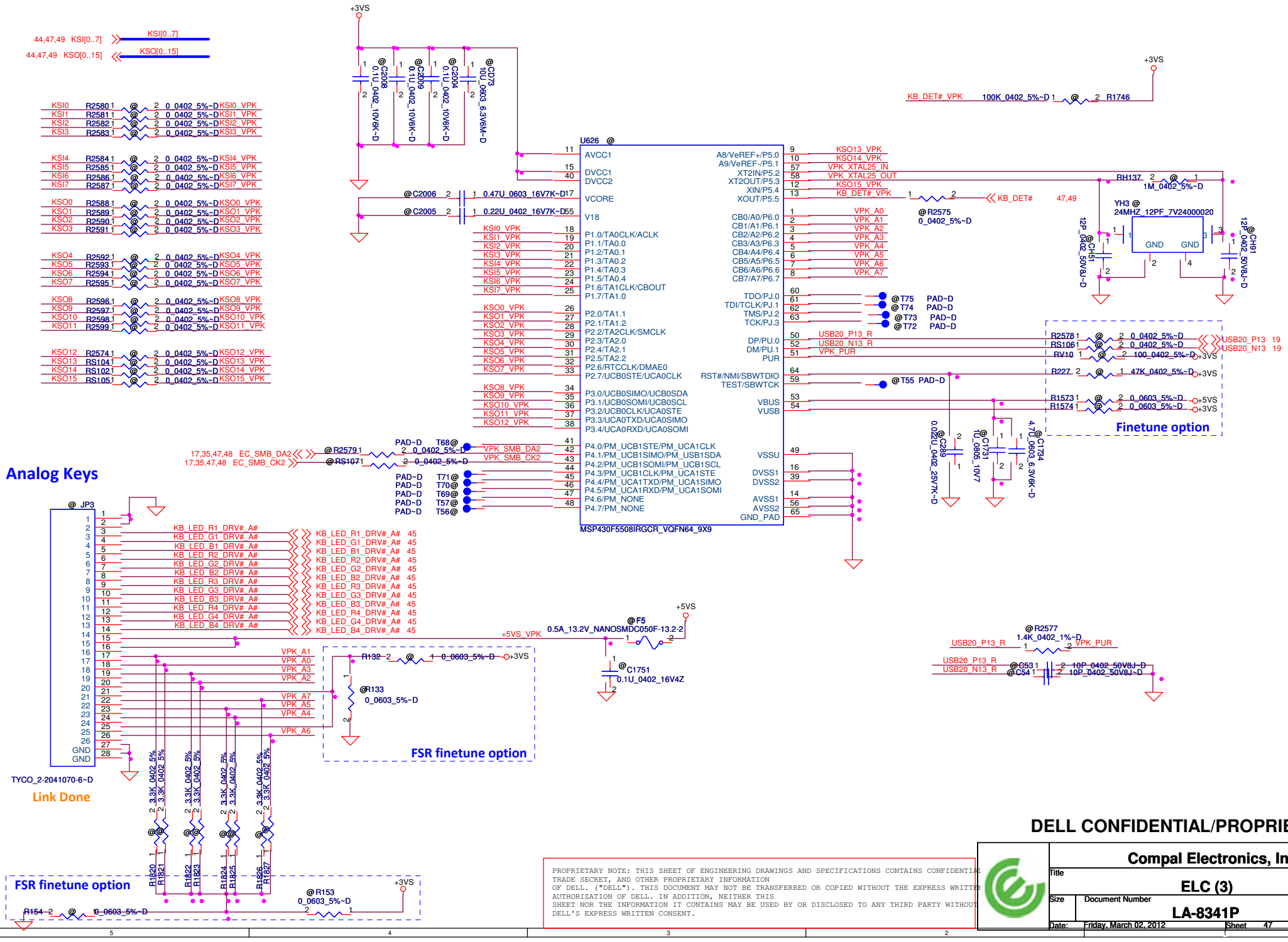
Compal Electronics, Inc.		
Title: ELC (3)		
Size	Document Number: LA-8341P	Rev: 1.0
Date: Friday, March 02, 2012	Sheet 46 of 71	


Analog Keys
U626
MSP430F5508IRGCR_VQFN64_9X9
TYCO_2-2041070-6~D
Link Done
FSR finetune option
FSR finetune option
Finetune option
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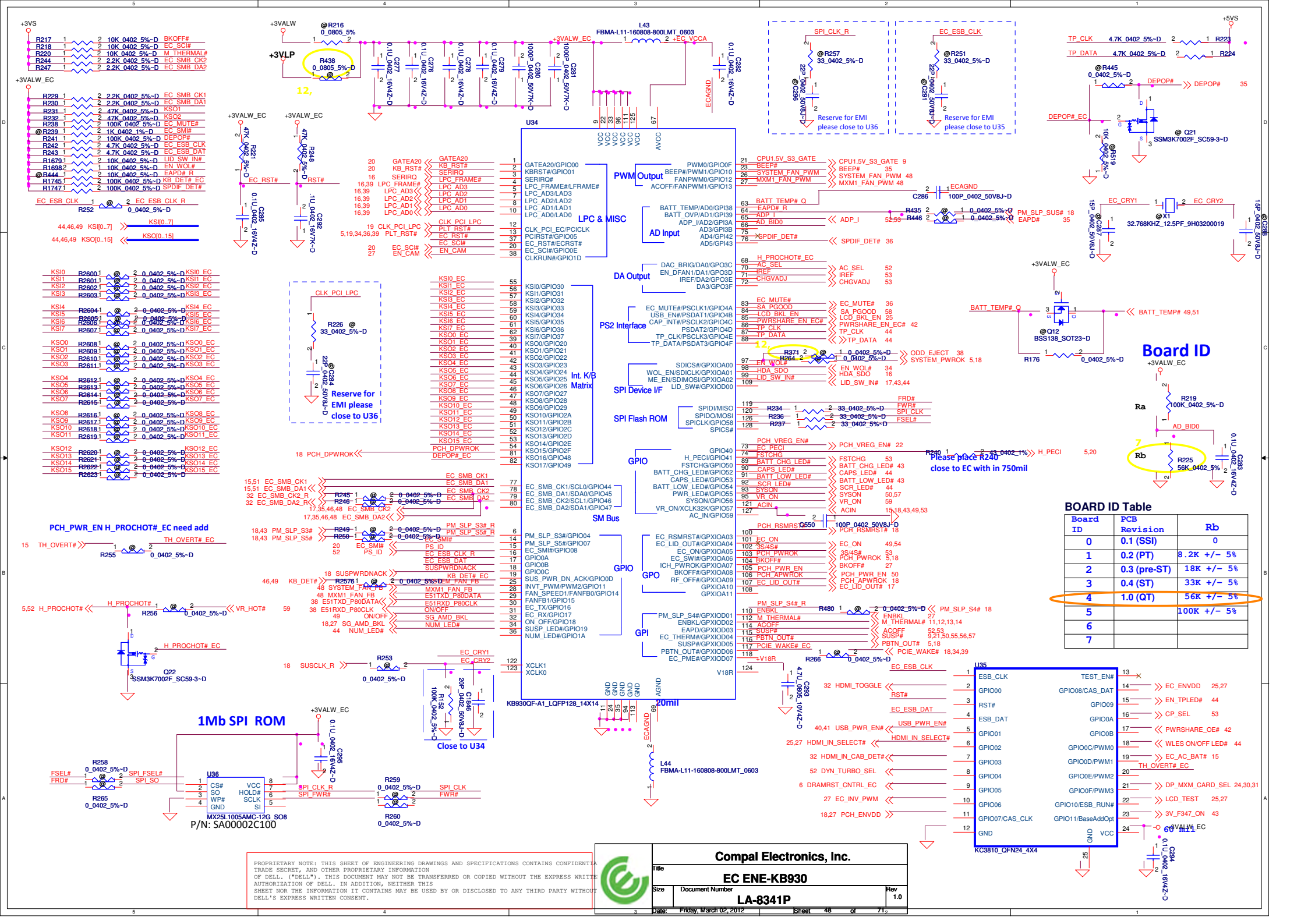
Compal Electronics, Inc.
Title
ELC (3)
Size
Document Number
LA-8341P
Rev
1.0
Date: Friday, March 02, 2012
Sheet 47 of 71


U34
KB930QF-A1_LQFP128_14X14
Int. K/B Matrix
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
SPI Device I/F
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Reserve for EMI please close to U36
Reserve for EMI please close to U35
Reserve for EMI please close to U36
Close to U34
20mil
60 mil
Please place R240 close to EC with in 750mil
Board ID
BOARD ID Table
Board ID | PCB Revision | Rb
0 | 0.1 (SSI) | 0
1 | 0.2 (PT) | 8.2K +/- 5%
2 | 0.3 (pre-ST) | 18K +/- 5%
3 | 0.4 (ST) | 33K +/- 5%
4 | 1.0 (QT) | 56K +/- 5%
5 | | 100K +/- 5%
6 | |
7 | |
PCH_PWR_EN H_PROCHOT#_EC need add
1Mb SPI ROM
P/N: SA00002C100
MX25L1005AMC-12G_SO8
KC3810_QFN24_4X4
Q22 SSM3K7002F_SC59-3~D
Q21 SSM3K7002F_SC59-3~D
Q12 BSS138_SOT23~D
L43 FBMA-L11-160808-800LMT_0603
L44 FBMA-L11-160808-800LMT_0603
X1 32.768KHZ_12.5PF_9H032000019
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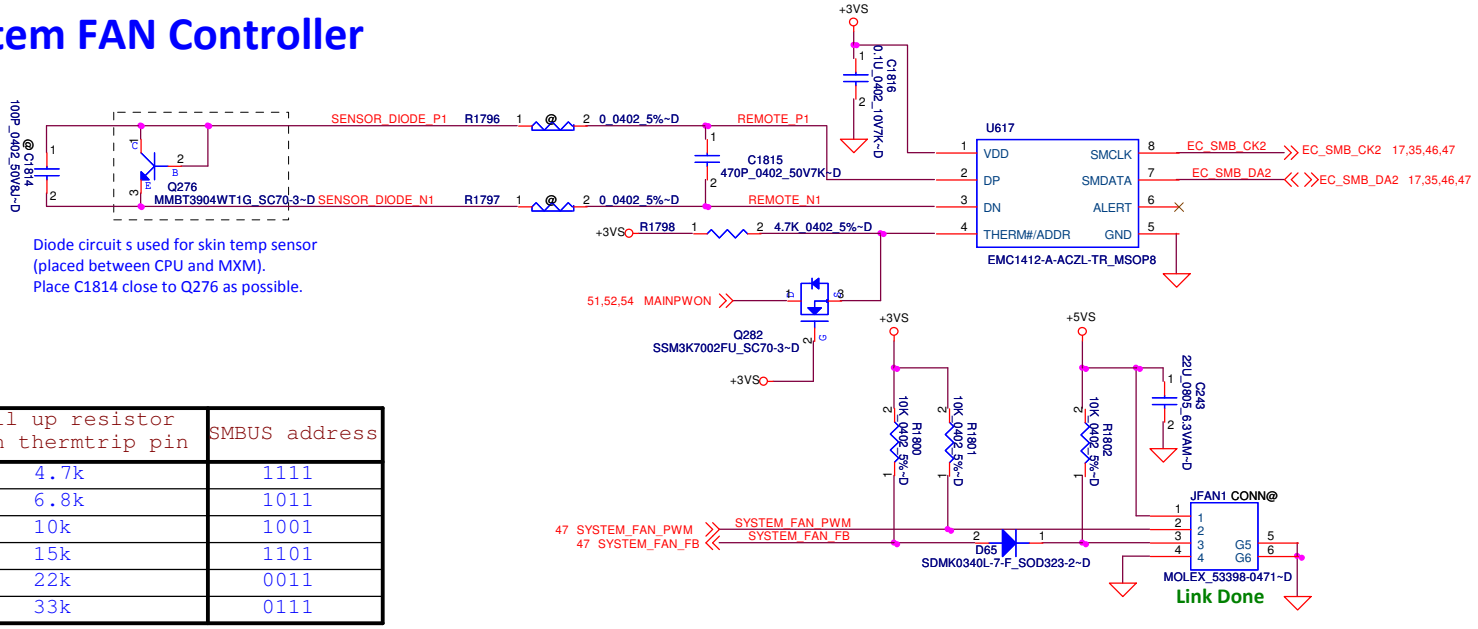
EC ENE-KB930
LA-8341P
Rev 1.0
Date: Friday, March 02, 2012
Sheet 48 of 71

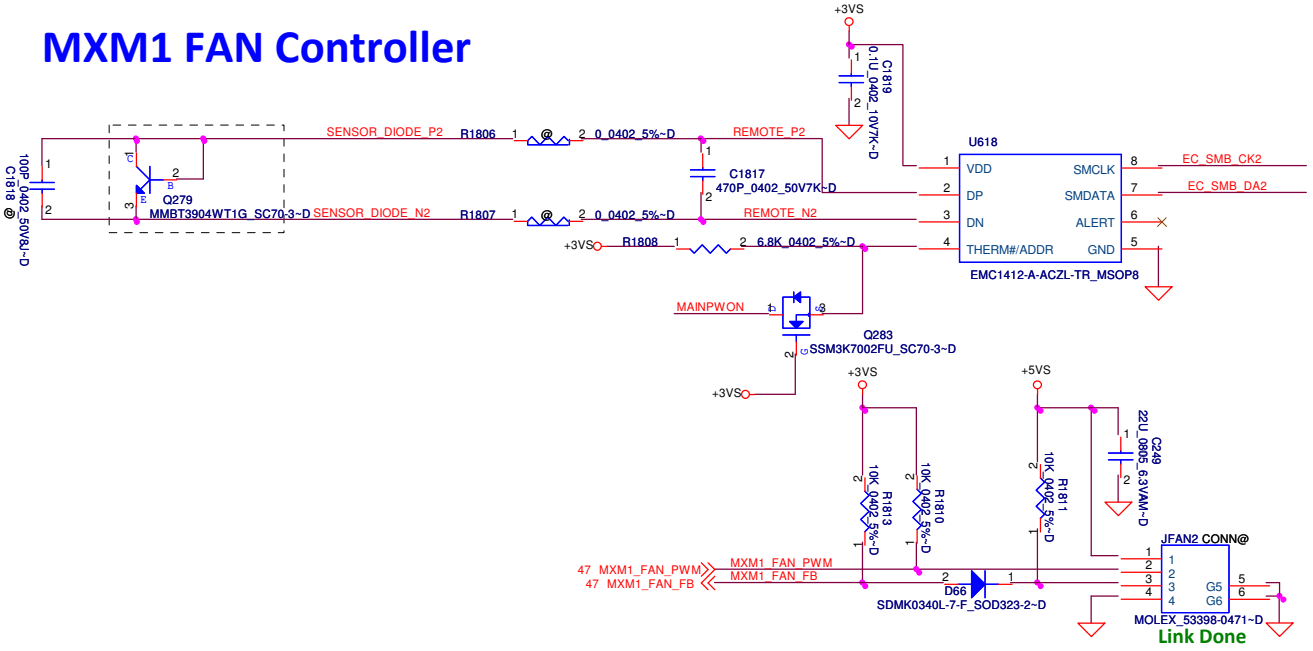
System FAN Controller



Diode circuit s used for skin temp sensor
(placed between CPU and MXM).
Place C1814 close to Q276 as possible.

Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111

MXM1 FAN Controller

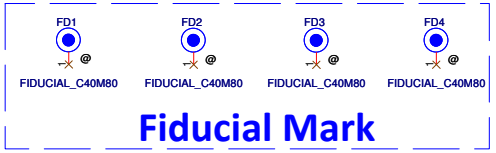


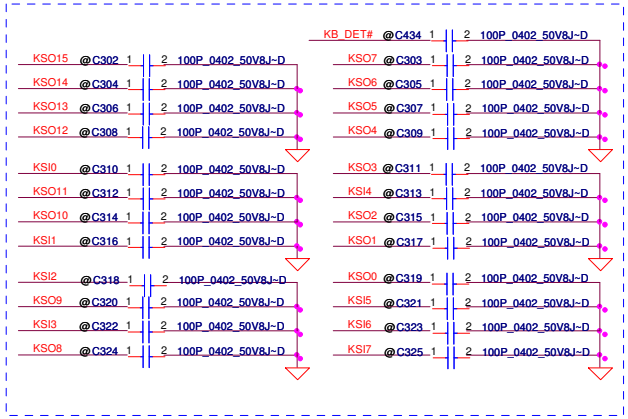
Compal Electronics, Inc.

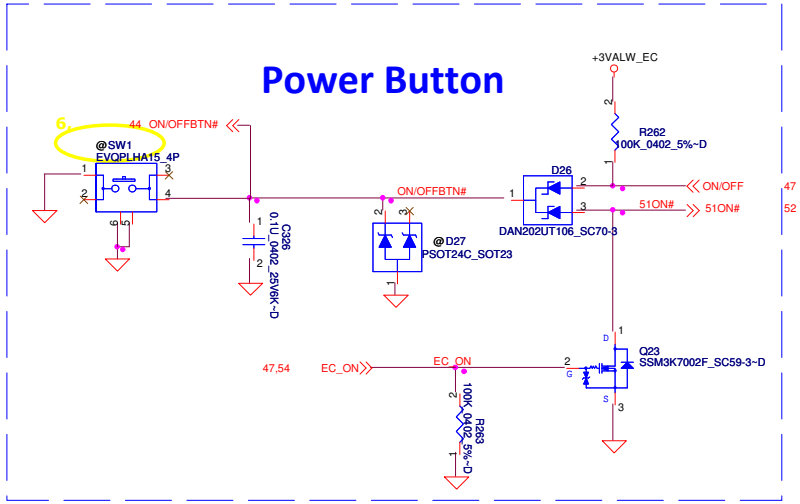
Title: Thermal Sensor & FAN

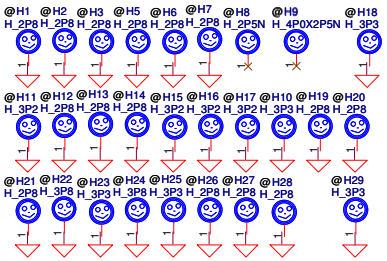
Size | Document Number: LA-8341P | Rev: 1.0

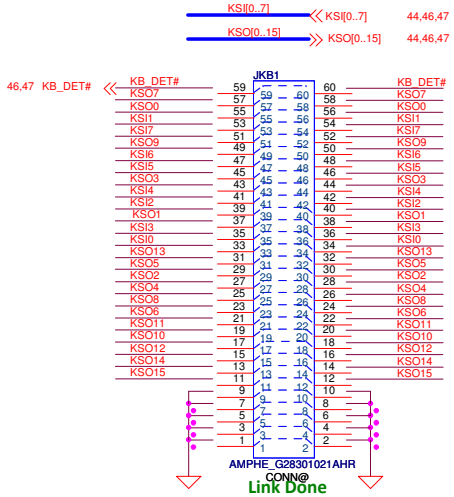
Date: Friday, March 02, 2012 | Sheet 49 of 71

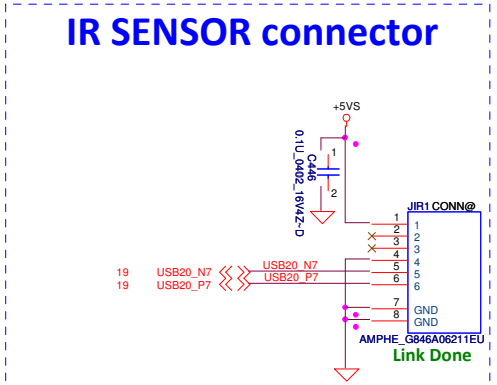












Compal Electronics, Inc.

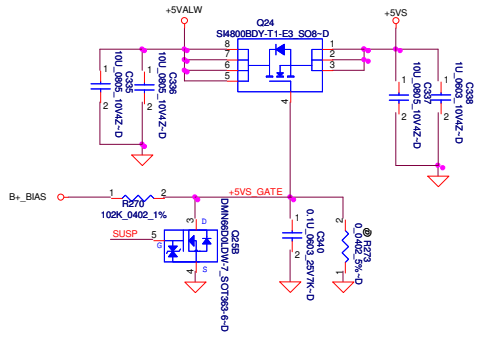
Title: KB & Power Button & IR

Size: | Document Number: LA-8341P | Rev: 1.0

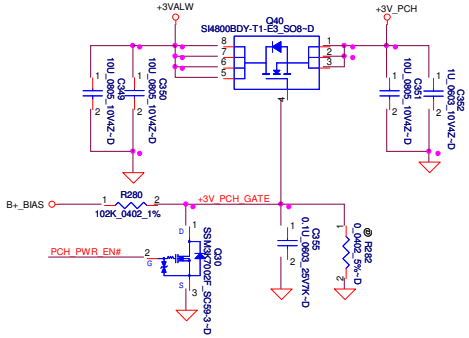
Date: Friday, March 02, 2012 | Sheet 50 of 71

DC to DC

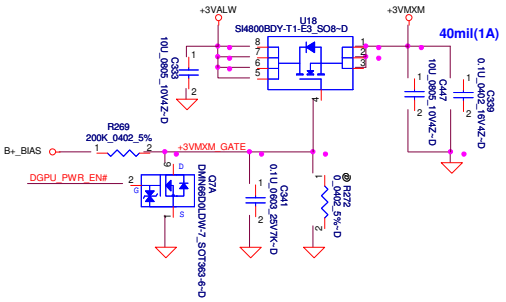
+5VALW to +5VS



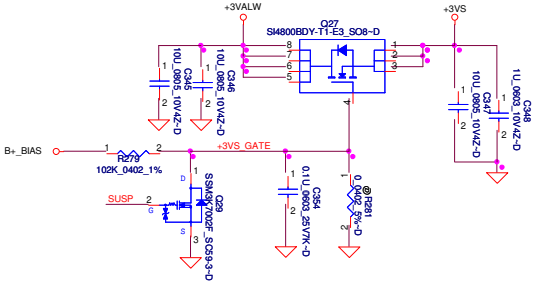
+3VALW to +3V_PCH



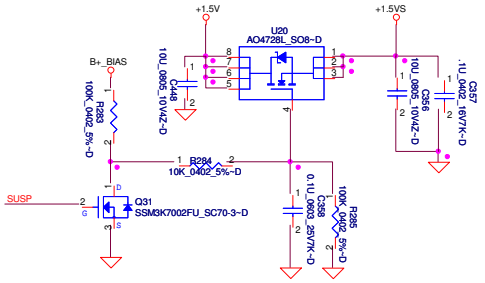
+3VALW to +3VMXM Transfer



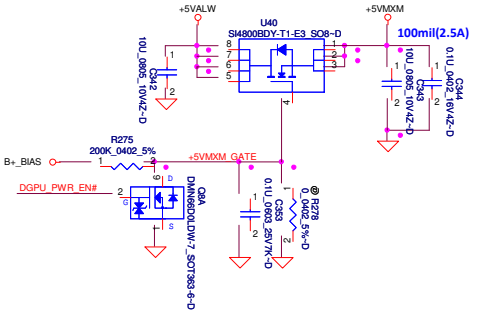
+3VALW to +3VS



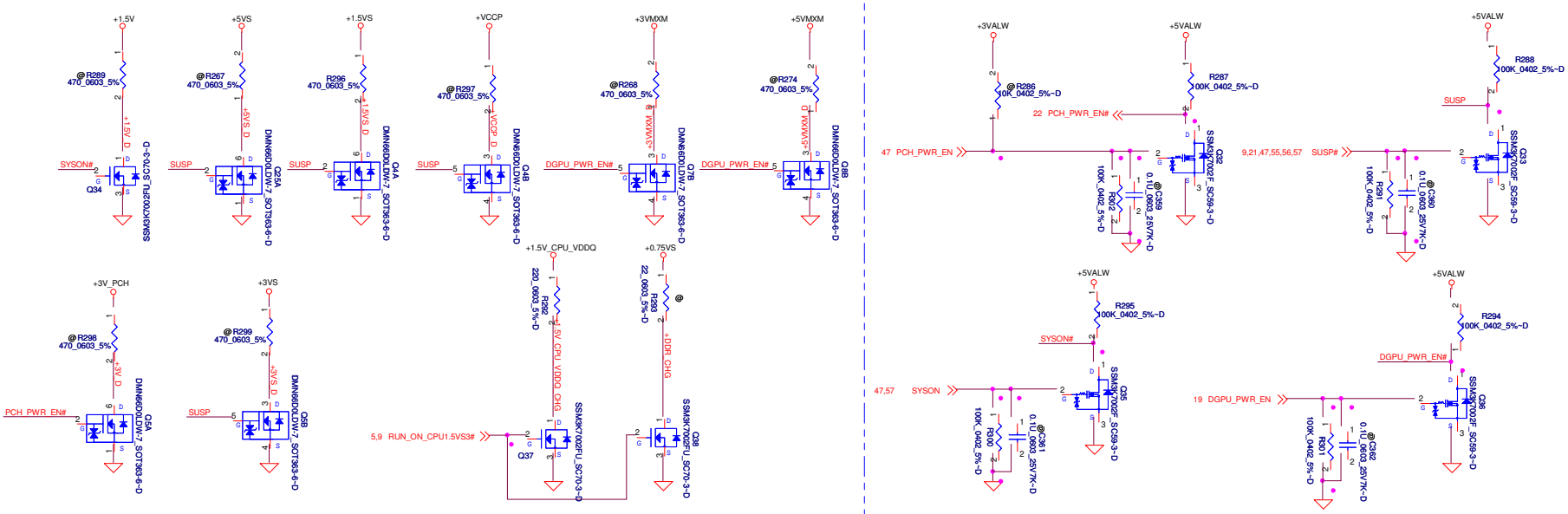
+1.5V To +1.5VS



+5VALW to +5VMXM



Discharge Circuit

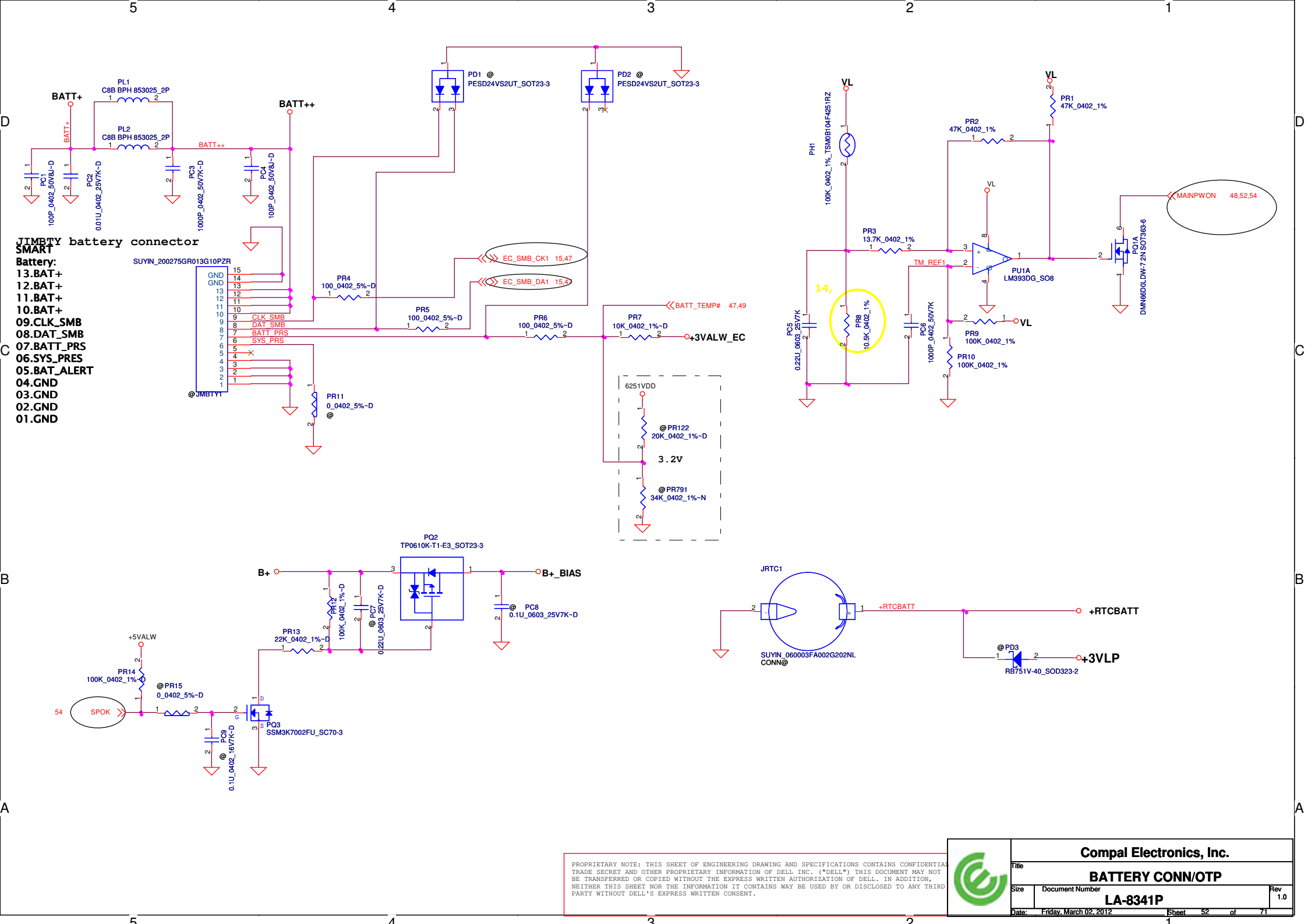


Compal Electronics, Inc.

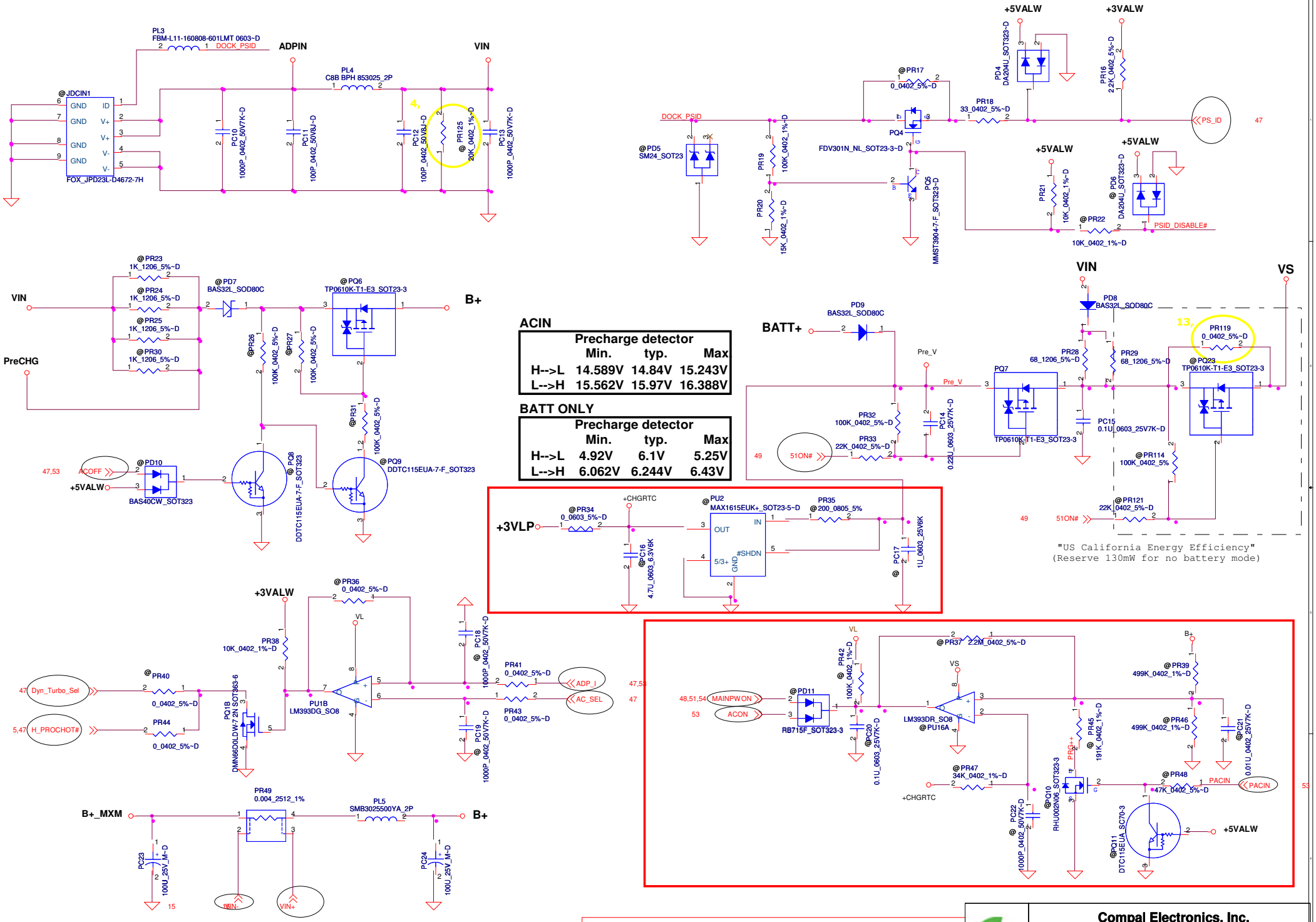
Title: DC/DC Interface

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 51 of 71



Compal Electronics, Inc.	
Title	BATTERY CONN/OTP
Size	Document Number: LA-8341P
Rev	1.0
Date:	Friday, March 02, 2012
Sheet	52 of 71

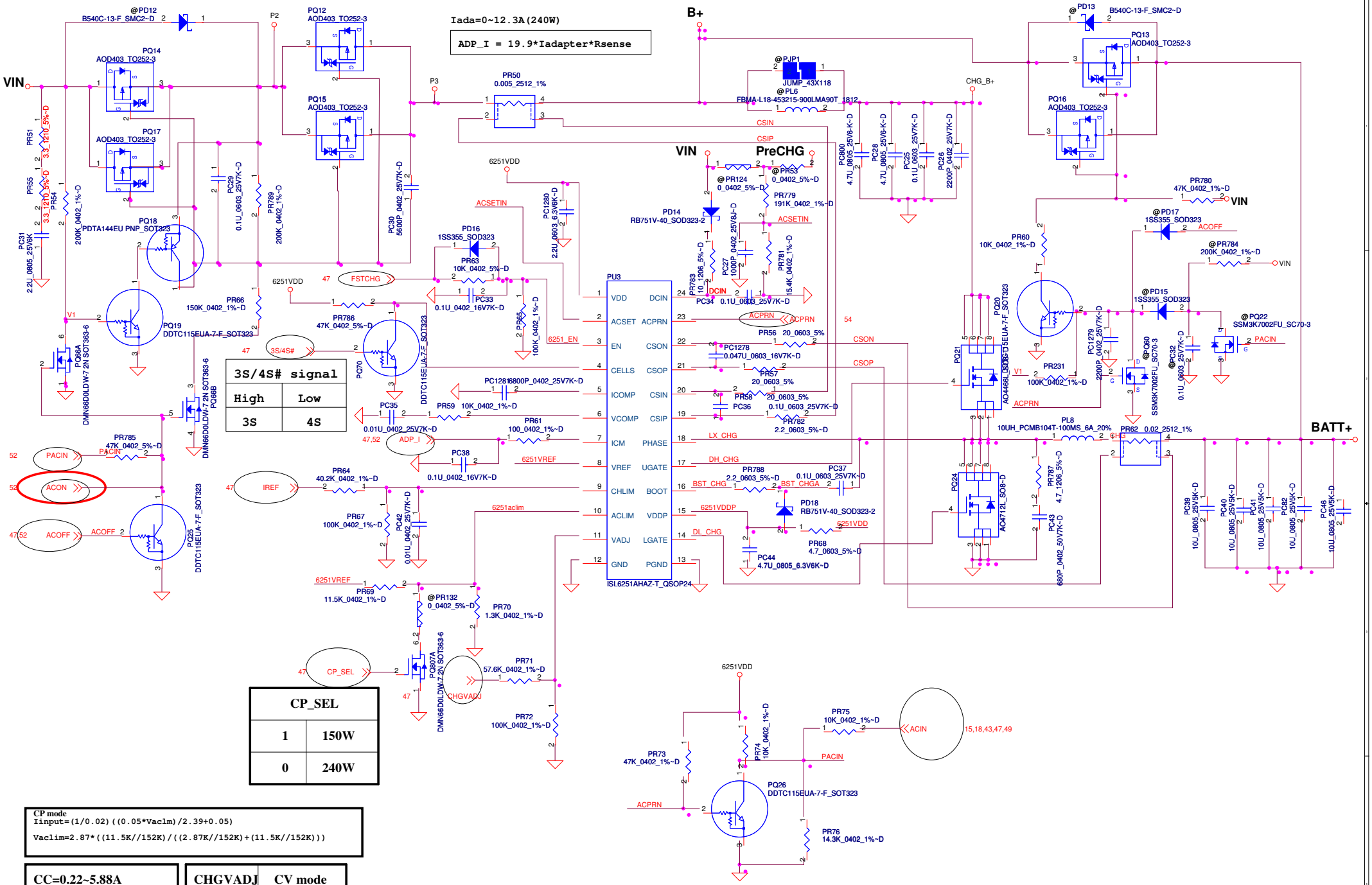


Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 53 of 71


Iada=0~12.3A(240W)
ADP_I = 19.9*Iadapter*Rsense
B+
VIN
PreCHG
BATT+
CHG_B+
ISL6251AHAZ-T_QSOP24
3S/4S# signal
High
Low
3S
4S
CP_SEL
1
150W
0
240W
CP mode
Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)
Vaclim=2.87*((11.5K//152K)/((2.87K//152K)+(11.5K//152K)))
CC=0.22~5.88A
IREF=1*Icharge
IREF=0.22V~3.294V
CHGVADJ
CV mode
0V
4V per cell
1.882V
4.2V per cell
3.3V
4.35V per cell
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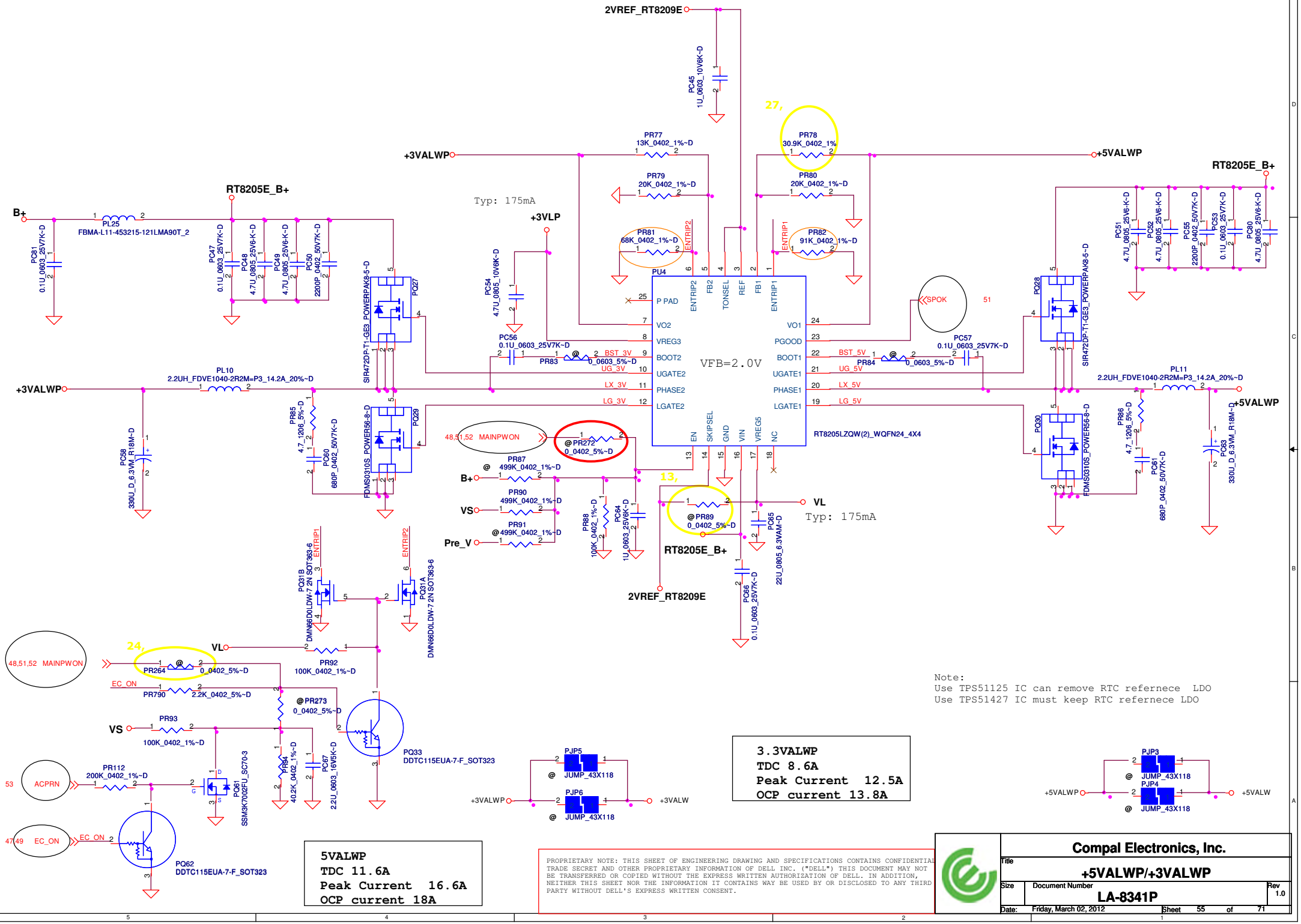
Compal Electronics, Inc.
Title
CHARGER
Size
Document Number
LA-8341P
Rev
1.0
Date: Friday, March 02, 2012
Sheet 54 of 71


2VREF_RT8209E
PC45 1U_0603_10V6K~D
27,
PR78 30.9K_0402_1%
PR77 13K_0402_1%~D
PR79 20K_0402_1%~D
PR80 20K_0402_1%~D
+3VALWP
+5VALWP
RT8205E_B+
Typ: 175mA
+3VLP
PR81 68K_0402_1%~D
PR82 91K_0402_1%~D
ENTRIP2
ENTRIP1
PU4
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
RT8205LZQW(2)_WQFN24_4X4
VFB=2.0V
SPOK
51
PC54 4.7U_0805_10V6K~D
PC56 0.1U_0603_25V7K~D
PR83 0_0603_5%~D
BST_3V
UG_3V
LX_3V
LG_3V
PC57 0.1U_0603_25V7K~D
PR84 0_0603_5%~D
BST_5V
UG_5V
LX_5V
LG_5V
PL25 FBMA-L11-453215-121LMA90T_2
PL10 2.2UH_FDVE1040-2R2M=P3_14.2A_20%~D
PL11 2.2UH_FDVE1040-2R2M=P3_14.2A_20%~D
PC81 0.1U_0603_25V7K~D
PC47 0.1U_0603_25V7K~D
PC48 4.7U_0805_25V6-K~D
PC49 4.7U_0805_25V6-K~D
PC50 2200P_0402_50V7K~D
PC51 4.7U_0805_25V6-K~D
PC52 4.7U_0805_25V6-K~D
PC55 2200P_0402_50V7K~D
PC53 0.1U_0603_25V7K~D
PC80 4.7U_0805_25V6-K~D
PQ27 SIR472DP-T1-GE3_POWERPAK8-5-D
PQ28 SIR472DP-T1-GE3_POWERPAK8-5-D
PQ29 FDMS0310S_POWER56-8-D
PQ30 FDMS0310S_POWER56-8-D
PR85 4.7_1206_5%~D
PR86 4.7_1206_5%~D
PC58 330U_D_6.3VM_R18M~D
PC60 680P_0402_50V7K~D
PC61 680P_0402_50V7K~D
PC63 330U_D_6.3VM_R18M~D
48,51,52 MAINPWON
PR272 0_0402_5%~D
PR87 499K_0402_1%~D
PR90 499K_0402_1%~D
PR91 499K_0402_1%~D
PR88 100K_0402_1%~D
PC64 1U_0603_25V6K~D
PR89 0_0402_5%~D
PC65 22U_0805_6.3VAM~D
PC66 0.1U_0603_25V7K~D
B+
VS
Pre_V
VL
Typ: 175mA
13,
RT8205E_B+
2VREF_RT8209E
PQ31B DMN66D0LDW-7 2N SOT363-6
PQ31A DMN66D0LDW-7 2N SOT363-6
ENTRIP1
ENTRIP2
24,
48,51,52 MAINPWON
PR264 0_0402_5%~D
PR92 100K_0402_1%~D
EC_ON
PR790 2.2K_0402_5%~D
@PR273 0_0402_5%~D
PR93 100K_0402_1%~D
PR112 200K_0402_1%~D
PR94 40.2K_0402_1%~D
PC67 2.2U_0603_16V6K~D
PQ61 SSM3K7002FU_SC70-3
PQ33 DDTC115EUA-7-F_SOT323
PQ62 DDTC115EUA-7-F_SOT323
53 ACPRN
47,49 EC_ON
PJP5 JUMP_43X118
PJP6 JUMP_43X118
PJP3 JUMP_43X118
PJP4 JUMP_43X118
+3VALW
+5VALW
3.3VALWP
TDC 8.6A
Peak Current 12.5A
OCP current 13.8A
5VALWP
TDC 11.6A
Peak Current 16.6A
OCP current 18A
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO
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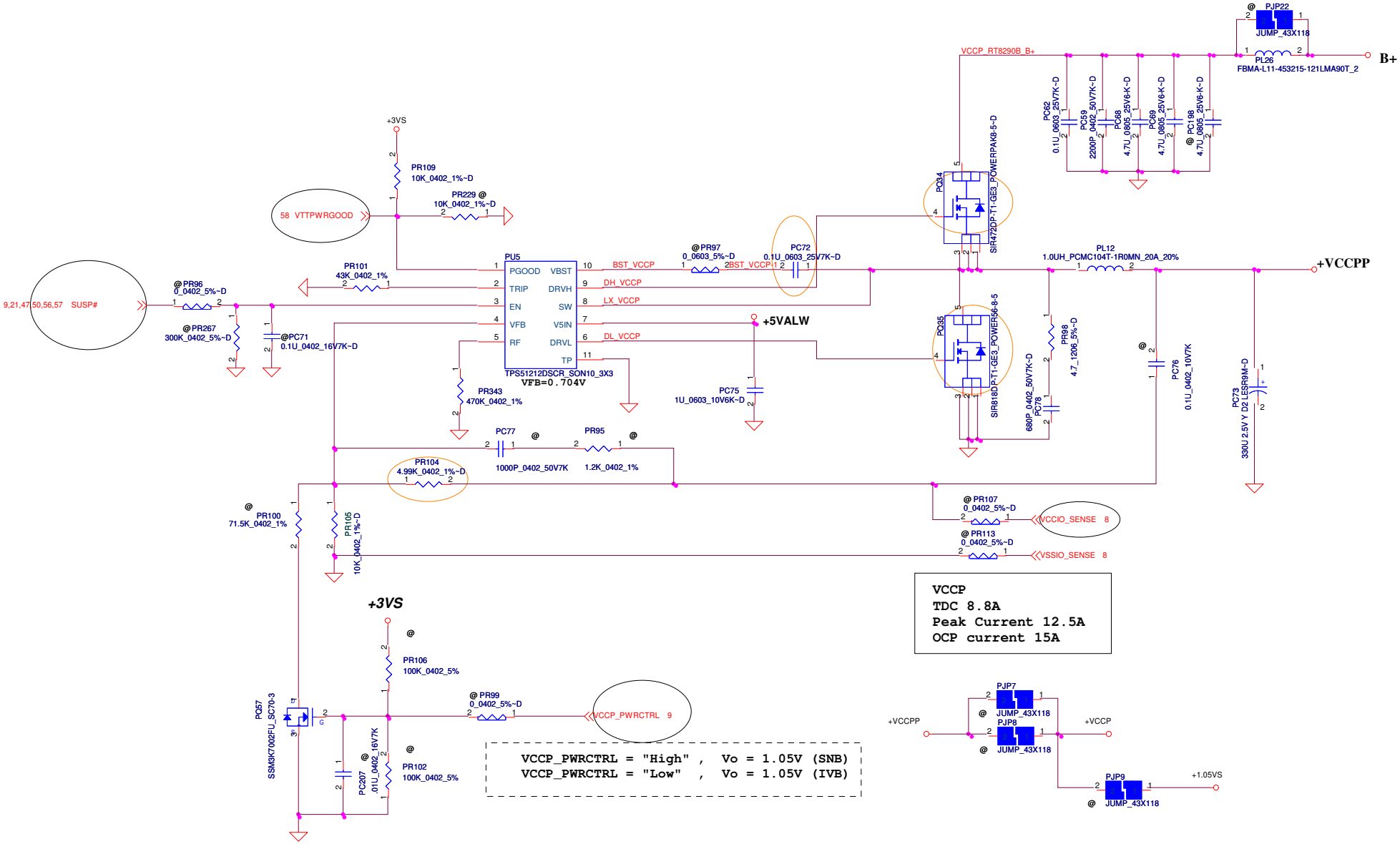
Compal Electronics, Inc.
Title
+5VALWP/+3VALWP
Size
Document Number
LA-8341P
Rev
1.0
Date: Friday, March 02, 2012
Sheet 55 of 71

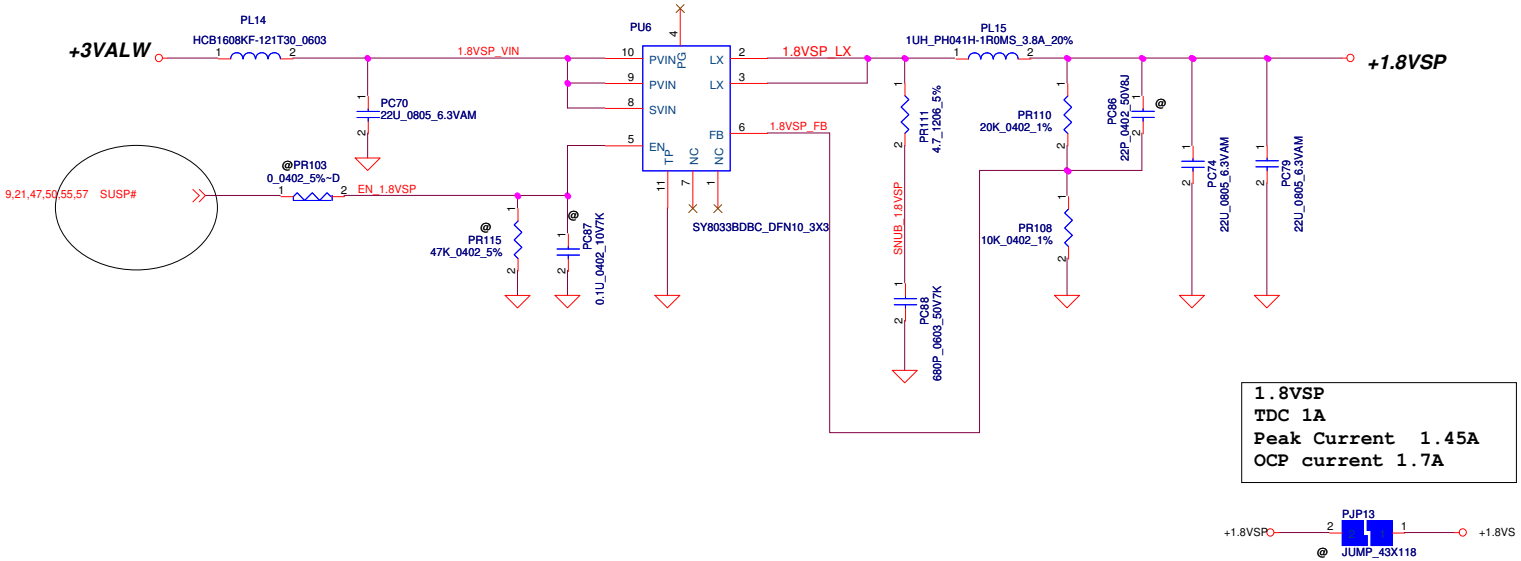


Compal Electronics, Inc.

Title: +VCCPP

Size: Document Number: LA-8341P Rev: 1.0

Date: Friday, March 02, 2012 Sheet 56 of 71



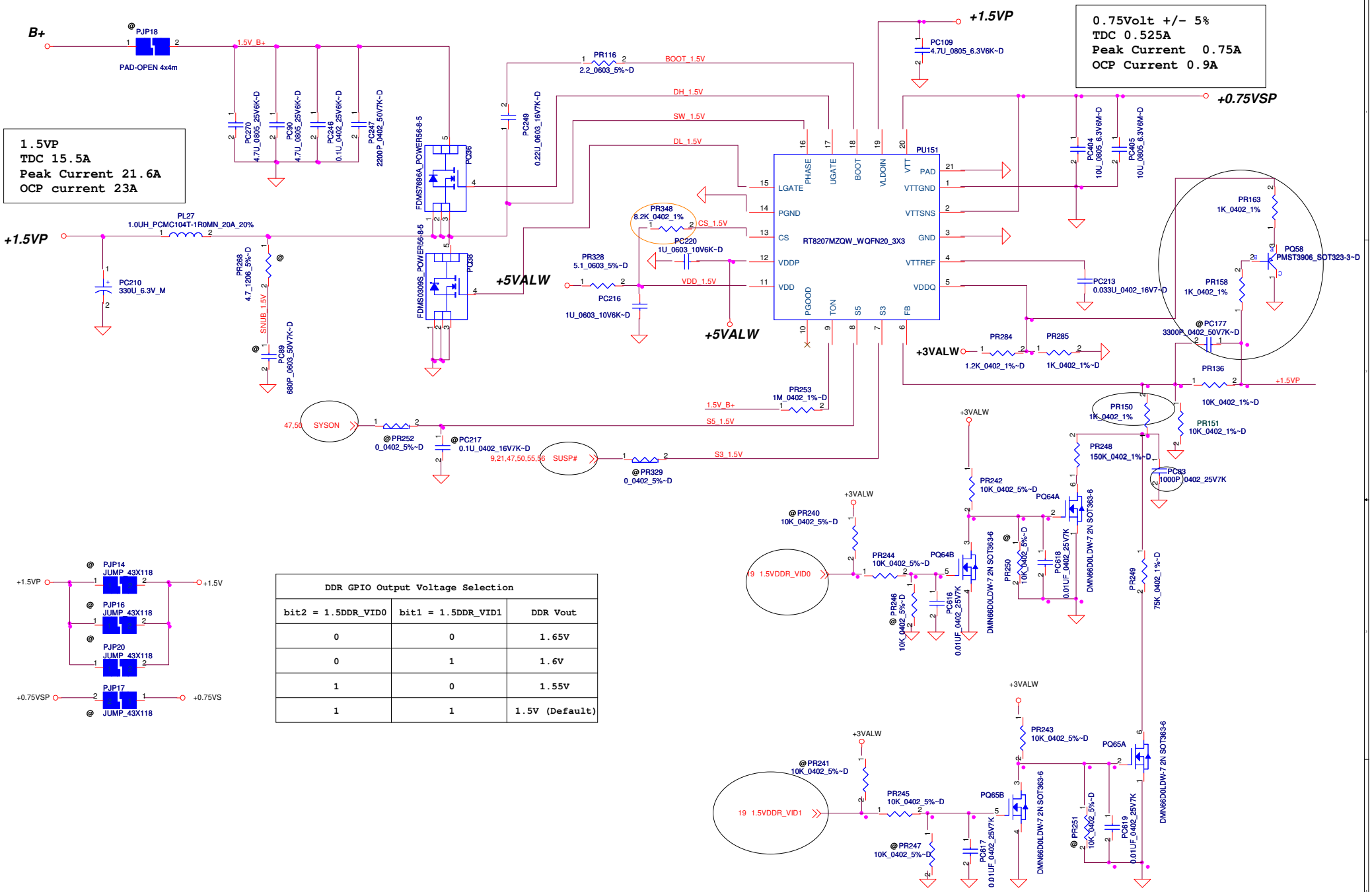
1.8VSP
TDC 1A
Peak Current 1.45A
OCP current 1.7A

Compal Electronics, Inc.

Title: +1.8VSP

Size: Document Number: LA-8341P Rev: 1.0

Date: Friday, March 02, 2012 Sheet 57 of 71



DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

Compal Electronics, Inc.

Title: +1.5VSP/0.75VSP

Size: | Document Number: LA-8341P | Rev: 1.0

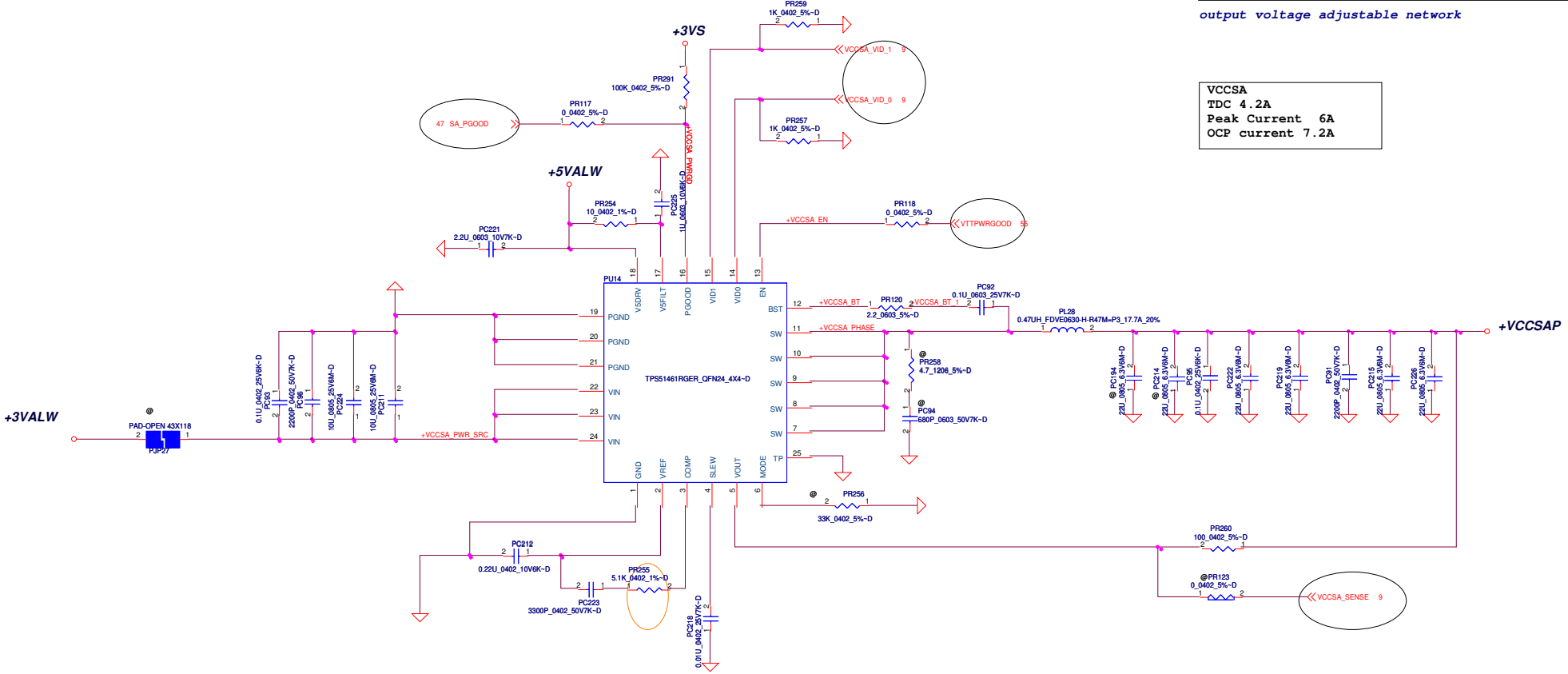
Date: Friday, March 02, 2012 | Sheet 58 of 71

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

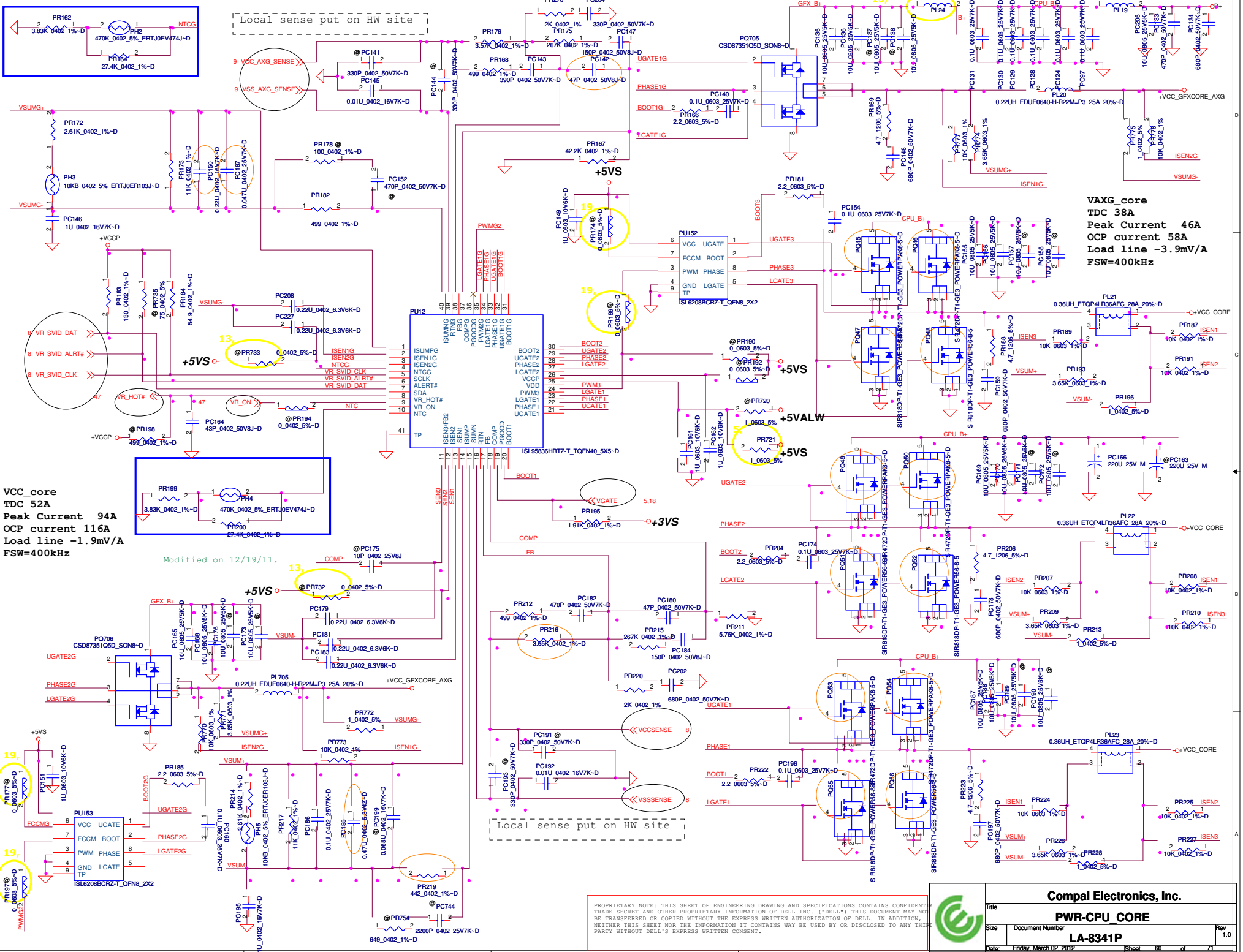


Compal Electronics, Inc.

Title: PWR-VCCSA_COREP

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 59 of 71



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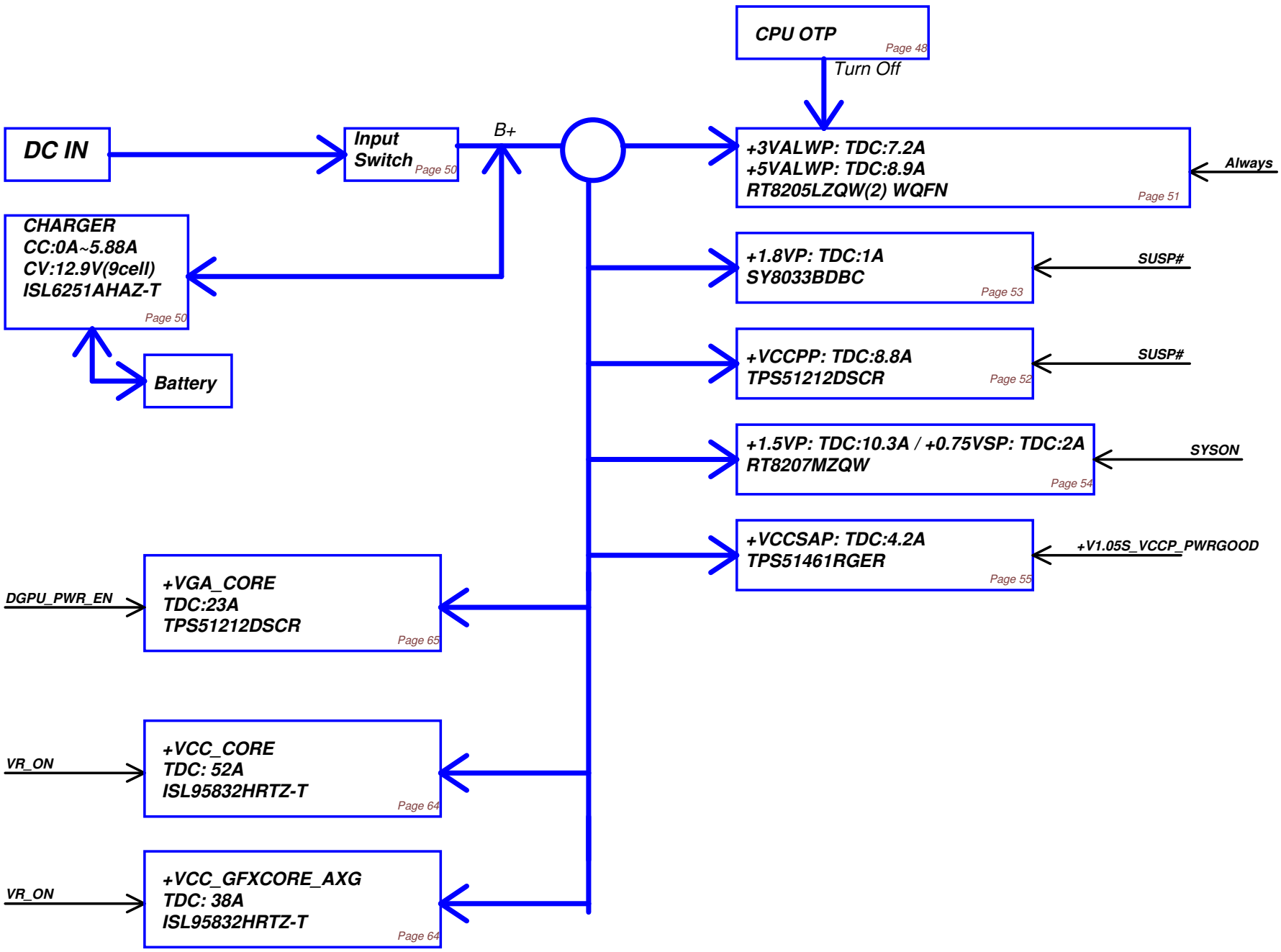
Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size | Document Number: **LA-8341P** | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 61 of 71

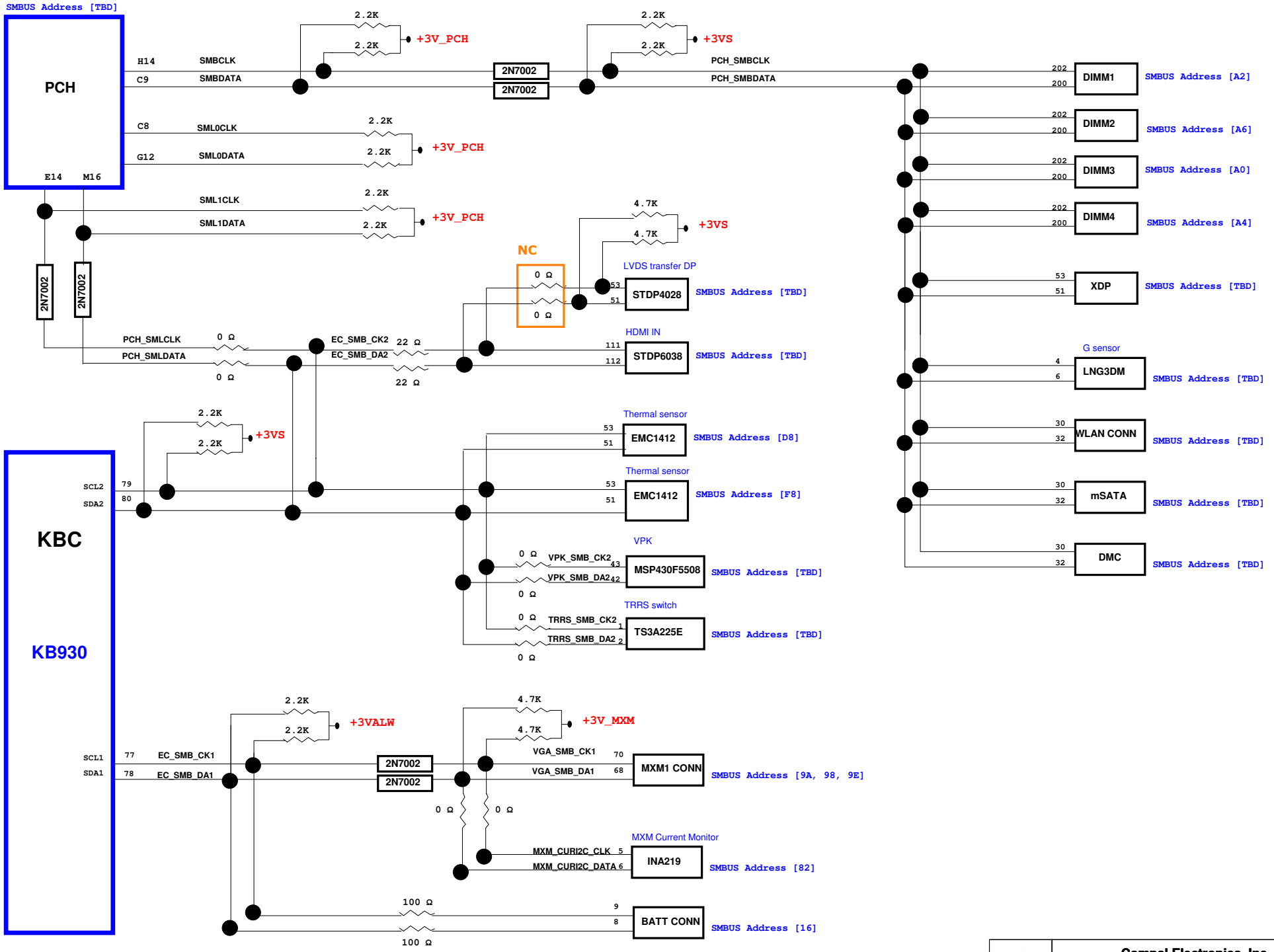
Power block



Compal Electronics, Inc.		
Title: POWER BLOCK DIAGRAM		
Size	Document Number: LA-8341P	Rev: 1.0
Date: Friday, March 02, 2012	Sheet 62 of 71	

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

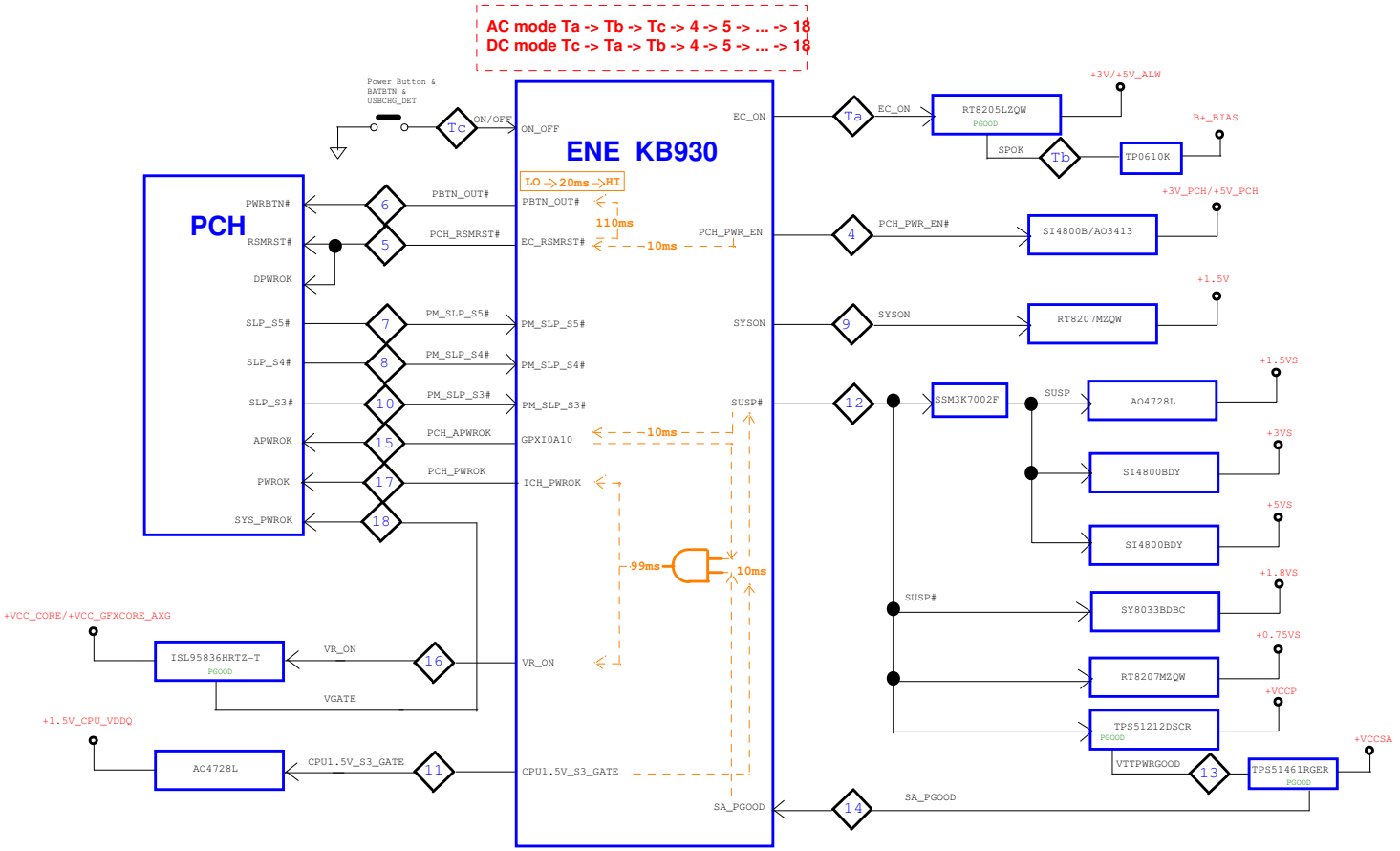


Compal Electronics, Inc.

Title: SMbus

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 64 of 71



Compal Electronics, Inc.

Title: Power Sequence Diagram

Size | Document Number: LA-8341P | Rev: 1.0

Date: Friday, March 02, 2012 | Sheet 65 of 71

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30		11'10/11		Only need to reserve one AC coupling cap for the DP signals from PCH (MXM) to DP redriver.	1,Remove C68, C69, C65, C67, C63, C64, C57, C66, C297, C298, C426, C427 C416, C417, C369, C370, C121, C367, C299, C300 related circuits. 2, Add C368, C301related circuits.	X01
2	29		11'10/11		Reserve pull HI circuit for TMDS output driver pre-emphasis and EMI setting.	Reserve RV57 pull HI to +3VS and NC.	X01
3	4,24		11'10/11			Change EDP_HPD# to EDP_HPD_R	X01
4	25		11'10/12		Solve QV9A derating issue.	Add RV39 to devide voltage.	X01
5	50		11'10/18		To solve two step issue for PCH_PWR_EN#	NC R286 and pop R302.	X01
6	30		11'10/18		For DP function from PCH port.	Pop R2263 and R2264	X01
7	50		11'10/18		Modify discharge circuits for back drive improve.	1, NC R289, R267, R297, R268, R274, R298, R299, R292, R293. 2, Change Q7B, Q8B enable signals to DGPU_PWR_EN#.	X01
8	32, 35		11'10/18		Remove HDMI_IN_AUDIO_CODEC signals.	Remove "HDMI_IN_AUDIO_CODEC" related signals and remove R1842.	X01
9	19, 46, 47		11'10/18		For material shortage issue, change all array resister to single resister	RP1-> R2580~ R2583, RP2-> R2584~ R2587, RP3-> R2588~ R2591 RP4-> R2592~ R2595, RP5-> R2596~ R2599, RP7-> R2600~ R2603 RP8-> R2604~ R2607, RP9-> R2608~ R2611, RP10-> R2612~ R2615 RP11-> R2616~ R2619, RP11-> R2620~ R2623, RPH1->RH185, RH191, RH193, RH205 RPH2-> RH250, RH214, RH249, RH248, RPH3-> RH252, RH253, RH254, RH256 RPH4-> RH257, RH258, RH260, RPH5-> RH259, RH261, RH262, RH263	X01
10	47, 51, 54		11'10/19		ERP lot6 implementation	1, NC R216 and pop R438. 2, NC PR273 and pop PR790. 3, change PR7 pull Hi to +3VALW_EC.	X01
11	38		11'10/19		Update zero power ODD circuit for leakage prevent.	Pop R173	X01
12	16,17,32, 33,34,46, 47		11'10/19		Update crystal usage.	1, change crystal components for YH3, YH2, YL1, Y3, Y4, X1, YH1 2, change C97, C98, CH23, CH24=15pF, Change CL18, CL19=18pF	X01
13	47		11'10/20		Update Board ID to PT stage.	Change R225 to 8.2K.	X01
14	20		11'10/20		Follow INTEL review list: All unused GPIOs, which are GPI by default needs to be pulled up to their respective power wells through 8.2 kohm to 10 kohm resistor	1, Add RH264 and pull HI to +3V_PCH 2, Pop RH194	X01
15	22		11'10/20		Follow INTEL review list: VCCASW[22-23] do not require series resistors.	NC RH240, RH241 and RH243 and use short pad.	X01
16	21		11'10/20		Follow INTEL review list: VCCCLKDMI filter is no longer required. Keep the Cdecap, but remove the Cfitler/Lfilter.	Change LH11 to RH265 and use short pad.	X01
17	9		11'10/20		Follow INTEL review list: +1.5V voltage divider for SM_VREF uses 1K Ohm	RC112,RC116 change to 1K and NC.	X01
18	20, 57		11'10/20		Solve Back drive issue for +3VS and +3V_PCH	NC PR240, PR241, RH192	X01
19	5, 50		11'10/20		Follow INTEL review list suggestion.	NC RC19 and QC1 and pop R292	X01
20	32, 33		11'10/20		Follow vendor suggestion change L to 0 ohm.	Change L11, L12, L13, L32, L46, L48, L52 to R452, R453, R454, R455, R450, R451, R456 and pop them.	X01
21	32		11'10/21		Delete HDMI_IN_AUDIO_CODEC pull HI resitors.	Remove R1665.	
22	9		11'10/21			Remove J8.	
23	21, 22		11'10/22		Remove short jump usage.	Remove RH240, RH241, RH243, RH265 and short directly between +1.05VS and PCH.	
24	35		11'10/22		1, Update combo jack to normal open type. 2, EAPD# pull high to prevent floating status to EC.	1, Update JHP2 to CIS symbol, and add R457 between Q42 pin1 and pin2. NC R129 and Q42 2, add R2554 pull HI to +3VS.	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	49		11'10/22		Add one power switch for debug purpose.	Add SW1.	X01
26	39		11'10/22		Follow INTEL review list: PDG recommends 100K PD on AUXP and 100K PU o AUXN	1, Add R112 pull HI to +3VS_DMC. 2, Add R115 pull Low to GND.	X01
27	28		11'10/22		Modify CRT_DET# circuits.	Reserve RV28 pull HI to +CRT_VCC for CRT_DET# and NC.	X01
28	35		11'10/25		Update combo jack to normal open type.	1, Remove R457, add Q46, R116, R131, only NC R116 2, Change R2553 to C228. 3, Reserve R171, R156, R174, C229 related circuits and only pop R171. and modify U620, U621.pinB2 connect to +3.3V_MUTE.	X01
29	30		11'10/25		Prevent DP leakage.	Add D72 related circuits and pop it.	X01
30	30		11'10/25		1, After Maxim FAE review, change to DP mux to SSI design. 2, Change decoupling cap to 220nF. 3, For DP to HDMI dongle function.	1, Add C68, C69, C65, C67, C63, C64, C57, C66, C297, C298, C426, C427,C416, C417, C369, C370, C121, C367, C299, C300 related circuits back and change the value to 220nF and pop all the componets . 2, Change C35, C36, C37, C38, C40, C45, C48, C49 to 220nF. 3, Reserve U638,Q304, R2626, C2021 and pop componets.	X01
31	49		11'10/25		Modify SW1 circuits to avoid SMT error.	NC SW1 pin2 and pin 3	X01
32	32		11'10/25		After ST FAE feedback: 1, STDP6038 doesn't need to read / write the panel EDID 2, Keep I2S_DAT/SPDIF_IN has better performance 3, Avoid I2S_DAT/SPDIF_IN signal has attenuation problem duo to long trance	1, NC R1843 and R1844 2, change R156 to C227 3, reserve U637 and C226 related circuits and NC.	X01
33	35		11'10/25		1, Fix fast hot plug and Headset no sound issue. Also improve external speaker Power down pop noise. 2, Improve Power on pop noise at external speaker.	1, Change R111, R113 from "No stuff" to "stuff 1k ohm". 2, Change R155, R157 from 100 ohm to 0 ohm.	X01
34	15		11'10/25		Follow sourcer suggestion.	Change U51 from INA219AIDCNRG4 to HPA00900AIDCNR .	X01
35	18		11'10/25		For BIOS verify SUSACK# function.	Add RH172 between SUSACK#_R and SUSPWRDNACK_R	X01
36	36		11'10/26		For PC_BEEP no warning sound during boot up process.	Change R148 to 200 ohm.	X01
37	42		11'10/26		Follow CIS suggestion, change ESATA footprint to "TAIWI_EU093-117CRL-TW_11P-T"		X01
38	59		11'10/26		Layout space concern.	change PL19, PL24 to HCB4532KF-800T90.	X01
39	49,51, 52		11'10/26		Fulfill "US California Energy Efficiency" standard that reserve 130mW for no battery mode.	1, PWR: Reserve PR122, PR791, PQ23, PR114, PR121 related circuits and NC. Only Add PR119 2, EE: Reserve Q305, Q306, R457 related circuits and NC.	X01
40	42		11'10/26		Change ESATA footprint back to TYCO.		X01
41	51		11'10/26		change PR791 to from "R_0402-N" to "R_0402 footprint"		X01
42	35		11'10/26		change net name from "JACK_PLUG#_R" to "JACK_PLUG"		X01
43	47,49,51		11'10/26		change net name from "BATT_TEMP" to "BATT_TEMP#"		X01
44	35		11'10/26		Follow JHP1 solution to JHP2.	1, Change R127, R130 from "No stuff" to "stuff 1k ohm". 2, Change R169, R170 from 100 ohm to 0 ohm.	X01
45	31,39		11'10/26		1, Reserve for SI-BEAM GEN2 card usage for PT build. 2, Change the MOS to protect ESD.	1, Reserve R95 pull HI to +3V_DMC and NC. 2, Change Q302 to 2N7002K.	X01
46	35		11'10/27		Follow vendor suggest.	Change C129, C130 to 0805 size.	X01
47	59		11'10/27		For Layout interference concern.	Change PL24 to original footprint same as SSI stage. But still use HCB4532KF-800T90.	X01
48	28		11'10/27		Due to CRT EA fail.	Change bead LV2,LV3,LV4 from BLM18BB600SN1D to TAIYO BK1608LL470-T	X01
49	59		11'10/27			Connect PU12.pin41 to GND	X01
50	55, 59		11'11/07		Correct both IGPU and VCCP OCP setting.	Change PR182 from 357 ohm to 499 ohm, and PR101 from 33k ohm to 43k ohm.	X01

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47		11'12/07		Change Board ID setting for ST stage.	Change R225 to 18K/5%	X02
2	25		11'12/07		For EDP power sequence EA.	Change RV40 to 100 ohm (0603) size.	X02
3	21		11'12/07		Adding a 1uF at U47 for +VCCAFDI_VRM		X02
4	32,33		11'12/07		For PASS crystal EA test, finetune cap setting.	1, Change C97 and C98 from 15pF to 12pF. 2, Change C407 and C408 from 10pF to 12pF.	X02
5	28		11'12/07		Per CRT EA, HSYNC and VSYNC undershoot and overshoot over spec.	Change LV5 and LV6 from bead to 0 ohm.	X02
6	25,27		11'12/07		ESD Vbus setting different between USB and DMIC/DCLK.	Move USB20_P(N)11 to D49, Change D48 power rail to +3VS_CAM.	X02
7	44		11'12/07		Modify Logo board related circuits.		X02
8	30		11'12/07		For Optimus, mDP output from dGPU.		X02
9	17,47		11'12/07			Chang KB_DET# from PCH to EC(pin 25)	X02
10	28		11'12/07			Change FV1 footprint to F_1206L150PR(F2's footprint)	X02
11	46		11'12/07		VPK function no implement, NC related components.		X02
12	42		11'12/07		Per sourcer suggestion, change USB charger IC to PI5USB1457A.		X02
13	32		11'12/07		Per reference spec and 2nd source consideration.	Change C183 from 0.1uF to 10uF.	X02
14	35		11'12/07		Avoid noise during S5 & G3 mode, add a circuit at sleeve pin.		X02
15	30		11'12/13		To prevent floating by other source.	Add a 100K PD at U8 pin 4 net "VGA_DPC_HPD".	X02
16			11'12/13		Change some option setting 0 ohm to short pad.		X02
17	42		11'12/13		Update USB power share circuits.	Move R1701 and keep NC, add R1702, NC R368.	X02
18	47		11'12/13		Change Board ID setting back to PT stage.	Change R225 back to 8.2K/5%	X02
19	19		11'12/13		For Intel chipset Hub1 EMI issue, swap USB port9 and port6		X02
20	25,27		11'12/13		Per EMI request.	Adding 0 ohm and 90ohm CM-mode choke colayout on USB port 11 and port12.	X02
21	16		11'12/13		Vendor improve their production.	U48 change to W25Q64FVSSIG(58nm)from W25Q64CVSSIG(90nm)	X02
22	28		11'12/13			Change FV1 part same as F2.	X02
23	27		11'12/13		For LVDS power sequence EA.	Change RV3 to 100 ohm (0603) size.	X02
24	47		11'12/13		Reduce power consumption on S5 mode.	Change R238 and R241 from 10K to 100K.	X02
25	47		11'12/13		Update "US California Energy Efficiency" circuits.	1, Add Q12 and NC. 2, Add R176 and POP.	X02
26	59		11'12/13			POWER PC164 change 0402 type	X02
27	25,27		11'12/20			NC L46,L48, Pop R462,R463,R460 and R461.	X02
28	16~23		11'12/20		Update PCH PN to QS sample	Change MFR.P/N, Compal P/N, Part description and value of PCH.	X02
29	59		11'12/20		Update power 2nd source usage for ISL6208BCRZ-T	Add PU152, PU153 and pop, NC PU11, PU15	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
30	47		11'12/20		Change Board ID setting for ST stage.	Change R225 to 18K/5%	X02
31	35		11'12/20			change Q309 to 2N7002DW-7	X02
32	35		11'12/20		Reserve for pop noise	change HP mute IC's power rail to +3VALW, pop R156, depop R171.	X02
33	35		11'12/20		Update combo jack circuits.	Add C745, C746 to GND.	X02
34	40,41		11'12/20		For signal jitter noise tolerance consideration, remove USB3.0 redriver 0 ohm co-layout resistor.	Remove R362~R365, R358~R361, R399~R402, R395~R398, R350~R357, R403~R410	X02
35	35		11'12/20		Solve iPHONE Can't record issue	NC R277.	X02
36	59		11'12/21		Update power 2nd source usage for ISL6208BCRZ-T	Delete PU11, PU15	X02
37	35		11'12/21		Per EMI suggest, avoid noise effect.	Add R350 and pop.	X02
38	39		11'12/21		Solve combo card (WIFI+BT) BT function cannot be recognized.	Add RE37 and NC.	X02
39	30		11'12/22		Correct SN74CBT3257CPWR supply voltage.	Add R351 and R352, NC R351 and POP R352.	X02
40	15		11'12/22		Update MXM relate circuits.	Add R353 and NC.	X02
41			12'01/02		Change some option setting 0 ohm to short pad.		X02
42	43		12'01/02			Remove PJP J11.	X02
43	39		12'01/02		Update combo card (WIFI+BT) BT function enable circuits.	Add RE38 and pop.	X02
44	28		12'01/05		Due to material shortage issue.	Change DV5 to 2nd source "RB491D_SOT23-3".	X02
45	36, 47		12'01/05		ADD SPDIF detect pin	1, Connect JSPD1 pin 5 to EC pin 76. 2, Adding 100K PU(+3VALW_EC) at pin76. NC C735.	X02
46	35		12'01/05		AP measurement fine tune.	Change C129 and C130 to "S CER CAP 2.2U 25V K X5R 0805 H1.25"	X02
47	40, 41		12'01/05		Due to material shortage issue.	1, Change C122,C123,C140,C141 to 2nd source material "220U_B_4VM_R35M". 2, Change C244,C247,C268,C269 source to "150U_D_10VM_R40M".	X02
48	38		12'01/05		Due to common parts issue.	Change Q303 to "SSM3K7002F_SC59-3~D"	X02
49	47		12'01/05		Update Board ID setting to formal ST stage.	Change R225 to 33K ohm.	X02
50	20, 29		12'01/05		Correct NET- name	Change GPIO30 net name to PCH_GPIO35.	X02
51	5		12'01/05		NC unnecessary parts.	RC27 and RC23 NC.	X02
52	39		12'01/05		Change some short pad back to 0 ohm.	Change RE26,RE27,RE28,RE29,RE31,RE32 and R162, R163 back to 0 ohm.	X02
53	35		12'01/05		Delete unnecessary parts.	Remove R116.	X02
54			12'01/05		Change some option setting 0 ohm to short pad for power parts.		X02
55	22,32,33, 35,38,47		12'01/06		Change some option setting 0 ohm to short pad.		X02
56	35		12'01/06		Reserve for de-pop circuits.	Add U625, R354, R355, C1847 related circuits.	X02
57	35		12'01/09		Follow vendor suggest, improve THD+N measurement test.	Add C28 between U634 pin1 and pin2.	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	18,32,33,35,36,38,39		12'02/15		1, NC Unnecessary parts. 2, Short 0 ohm for MP	1, NC RE26, RE27,RE28,RE29,RE31,RE32,RE35,RE36 2, Change RH132,RV41,RV44,RV9,RV16,R58,R352,R1663,R1845,R179,R211,R432,R443,R228,R447~R449,R439,R147,R309~R311,R149~R151,RE38 to short pad.	A00
2	29		12'02/15		Remove HDMI BITS debug option 0 ohm near connector.	R931 and R985 change to 0 ohm and NC.	A00
3	17,34		12'02/15		For WOL support and prevent leakage.	Populate RH95 and change from 10K to 4.7K. RL13 change to NC.	A00
4	52		12'02/15		For Erp lot 6 adapter issue	Adding a 20K at ADPIN (default NC)	A00
5	59		12'02/15		According PWR team suggestion to modify circuits.	PR720 power rail change from +5VALW to +5VS.	A00
6	49		12'02/15		NC Unnecessary parts.	NC SW1 for MP	A00
7	47		12'02/15		Change Board ID setting for QT stage.	Change R225 to 56K ohm.	A00
8	34		12'02/16		For PASS LAN ISN and EMI test in Chinese new regulation.	Change CL39 to 150pF.	A00
9	35		12'02/16		Follow vendor suggestion to reserve 0 ohm location for ripple noise reduce.	1, R180 change to 0402 0ohm. 2, R178 change to 0402 0ohm. 3, Add 0603 0ohm for (U12 Pin 10,11) 4, Add 0402 0ohm for (U12 Pin 16) 5, Add 0402 0ohm for (U12 Pin 19) 6, R128 change to 0603 0ohm.	A00
10	40,41,63		12'02/16		1, For BITS issue solve, USB3 Re-driver change to Pericom 2, Create strap pin table for USB3.0 redriver IC control.	1, NC U628, U629, R1828, R1833, R12, R25, R47, R46 2, NC U630, U631, R1834, R1835, R192, R187, R197, R196 3, Move all the related BOM setting to "P63-USB 3.0 Config setting"	A00
11	39		12'02/17		1, Remove Unnecessary audio circuits. 2, NC Unnecessary DMC circuits.	1, Delete R174 2, NC R162,R163	A00
12	28,29,30,32,35,37,38,39,42,43,47		12'02/17		Short 0 ohm for MP	1, Change R303, R316, R329, R340 to 0805 short pad 2, Change RS7, RS6, RE22, R441, R442, R438, R434, R433, R425, R428, R429, R371, R354, R355, R350, R2573, R2572, RS103, R2568, R2558, R2559, R172, R1702, R1699, R169, R170, R1667, R1572, R156, R155, R157, R110, R168, R101, LV5,LV6 to short pad.	A00
13	51		12'02/17		According PWR team suggestion, fine tune material usage	1, Change PL24 component same as PL19, but footprint keep the same. 2, Change PR89, PR119, PR732, PR733 component same as PR36.	A00
14	52,54,59		12'02/17		According Thermal and PWR team suggestion, fine tune OTP resistor setting.	Change PR8 to 10.5Kohm /1%.	A00
15	15		12'02/21		Prevent PCH GPIO38 ESD damage.	Reserve ESD protector for VGA_PRSNT_R# and VGA_PRSNT_L#. Pop D102 and NC D103.	A00
16	35		12'02/21		Follow vendor suggestion to modify.	1, Change R128 to 0805 size and R356 to 0402 size. 2, Separate U12.pin54,pin6,pin19 to different power rail. 3, Change R358 to L102 "BLM15AG121SN1D_2P"	A00
17	30		12'02/21		Per EIA and factory requirement.	Update U5 chip version to "PS8330BQFN48GTR2-A0"	A00
18	30		12'02/21		For BITS HDCP warning message issue.	NC R2261,R2262,C2021,U638,R2626 and Q304.	A00
19	59		12'02/21		According PWR team suggestion, fine tune material usage	Change PR174,PR177,PR186,PR197 to short pad.	A00
20	35		12'02/21		Follow Audio reference circuits to add one more cap for AVDD power.	Add C126 and pop it.	A00
21	25,27,35		12'02/22		According EMI team suggestion, fine tune material usage	Change L19,L20,L21,L22,L23,L24 and R460,R461,R462,R463 to 0 ohm short pad.	A00
22	30		12'02/23		For BITS HDCP warning message issue.	1, Pop R2261,R2262,C2021,U638,R2626 and Q304. 2, Change R2261 and R2261 to 2.2K. 3, Delete C297, C298, C299 and C300 and add R358~R361. 4, C368 and C301 change to 0.1uF(X7R).	A00
23	35		12'02/23		Follow vendor suggestion to modify.	1, Delete R357 and add L103, and pop it 2, change L49 to "4.7UH_LQM2MPN4R7MG0L_20%"	A00
24	54		12'02/23		According PWR team suggestion, fine tune material usage	Change PR264 to short pad.	A00

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	35		12'02/26		According AP test result that leverage with AW_14"	Update C228 to 1UF	A00
26	35		12'02/29		Improve AP test result.	1, Update C745 and C746 to populate. 2, R117 change from 3.3K(0402) to 2.2K(0402)	A00
27	54		12'02/29		According PWR team suggestion, fine tune material usage	Change PR78 to "30.9K_0402_1%".	A00
28	42		12'02/29		Reserve 0 ohm option for USB charger circuits.	Change R1699 and R1702 to 0 ohm.	A00
29	35		12'03/01		Improve AP test result.	R118 change from 3.3K(0402) to 2.2K(0402)	A00
30	25		12'03/02		Solve eDP related issue.	RV39 NC	