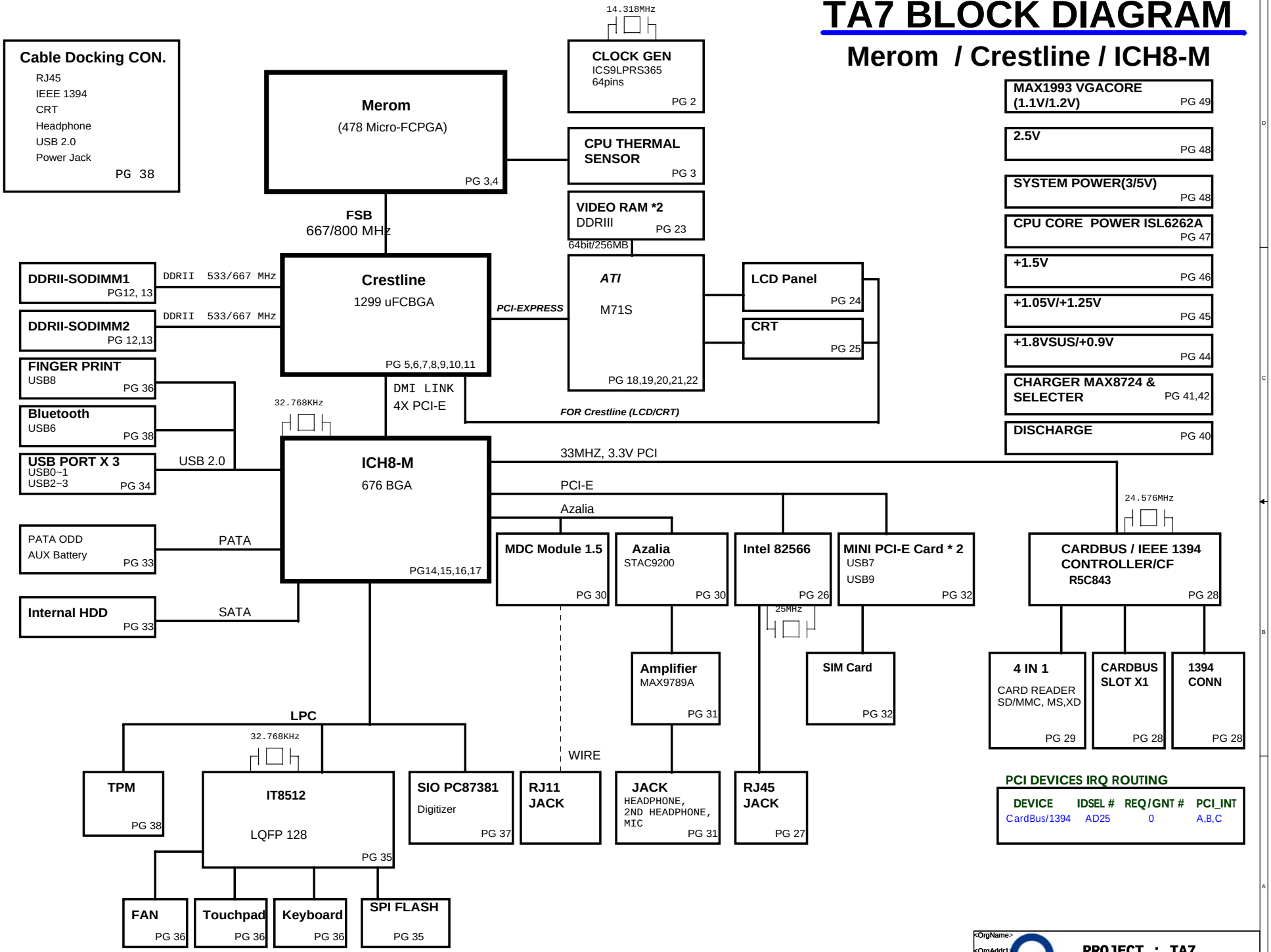
TA7 BLOCK DIAGRAM

Merom / Crestline / ICH8-M



PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394	AD25	0	A,B,C

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A

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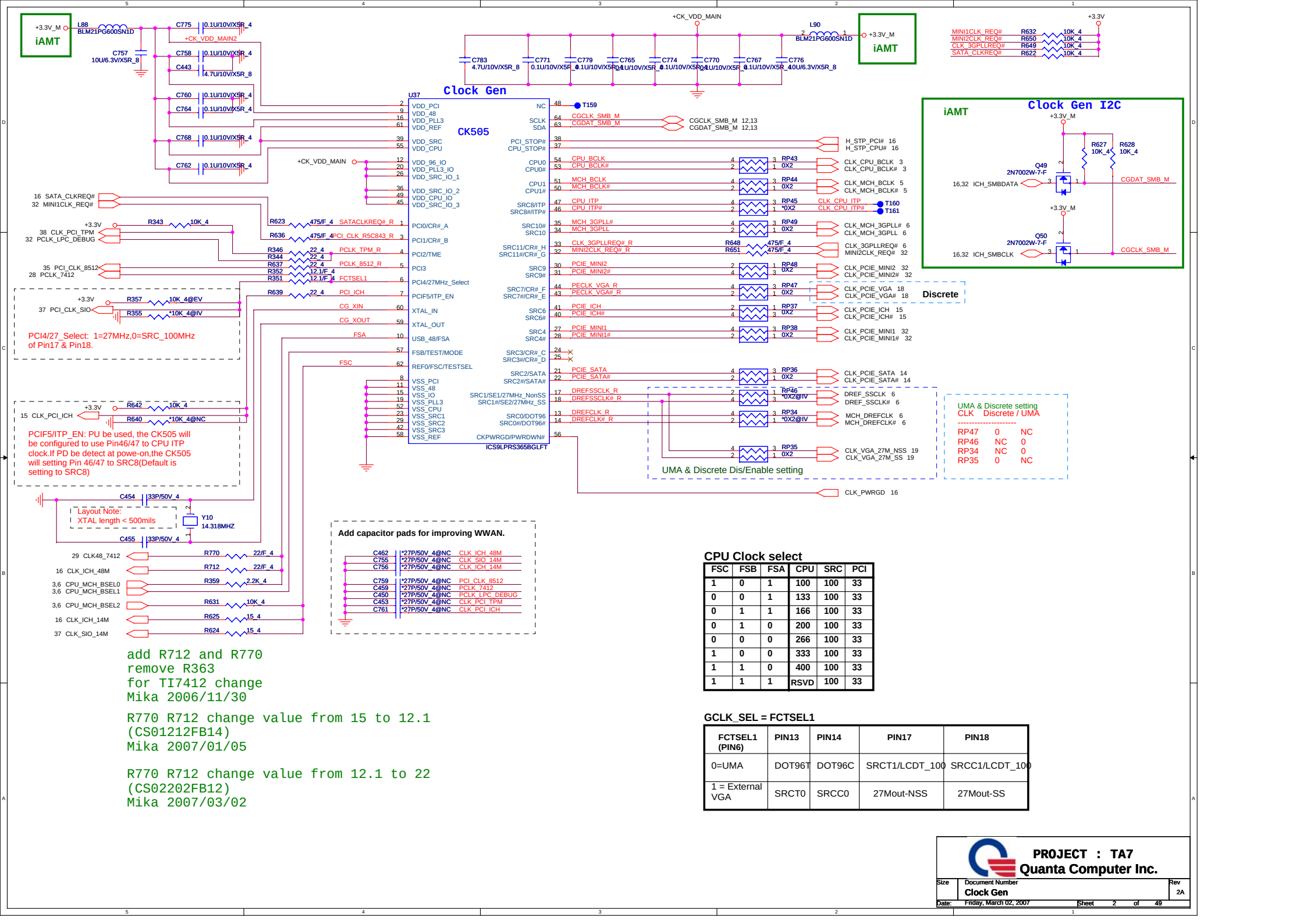

CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCC1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

add R712 and R770
remove R363
for TI7412 change
Mika 2006/11/30

R770 R712 change value from 15 to 12.1
(CS01212FB14)
Mika 2007/01/05

R770 R712 change value from 12.1 to 22
(CS02202FB12)
Mika 2007/03/02

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	Clock Gen	2A
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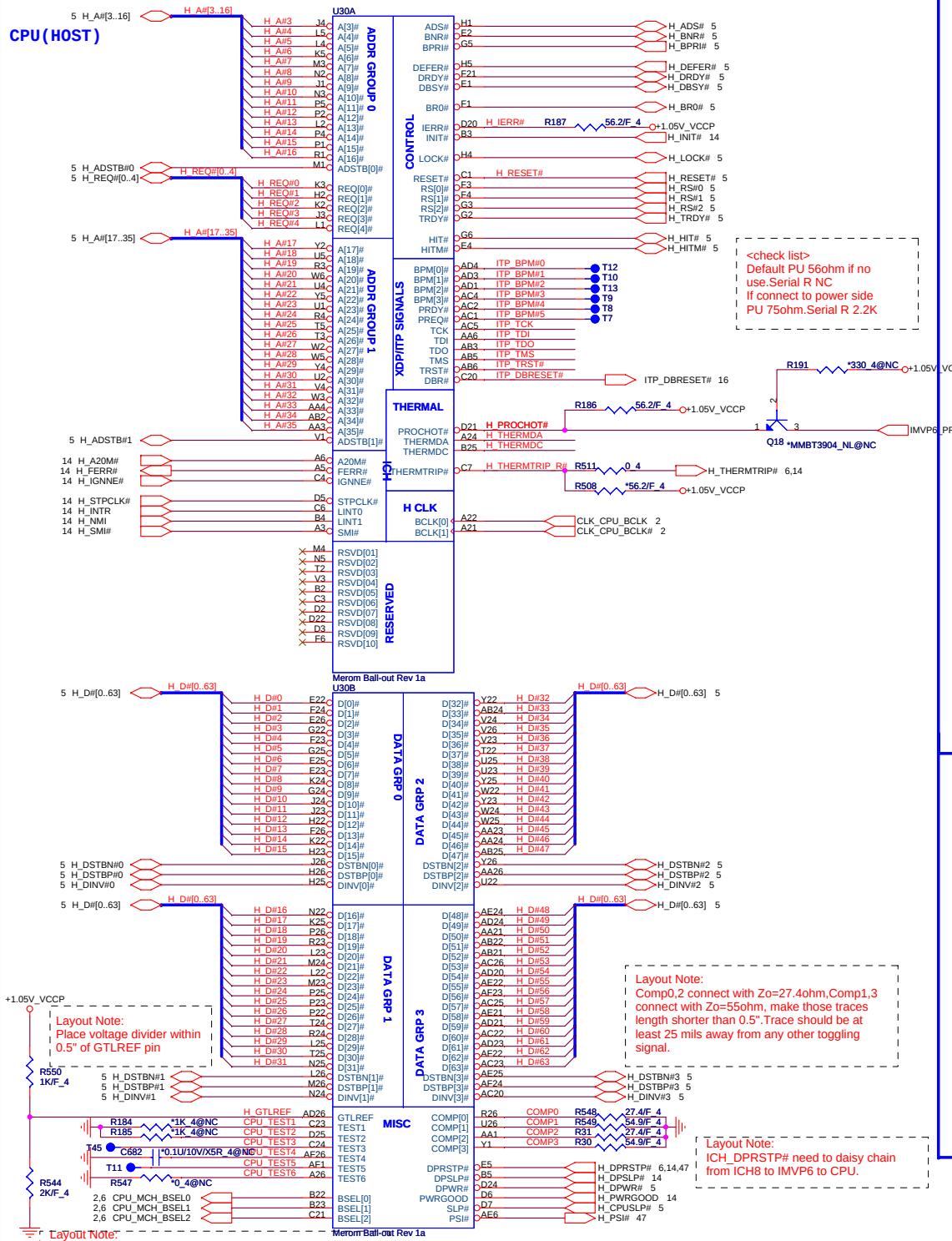
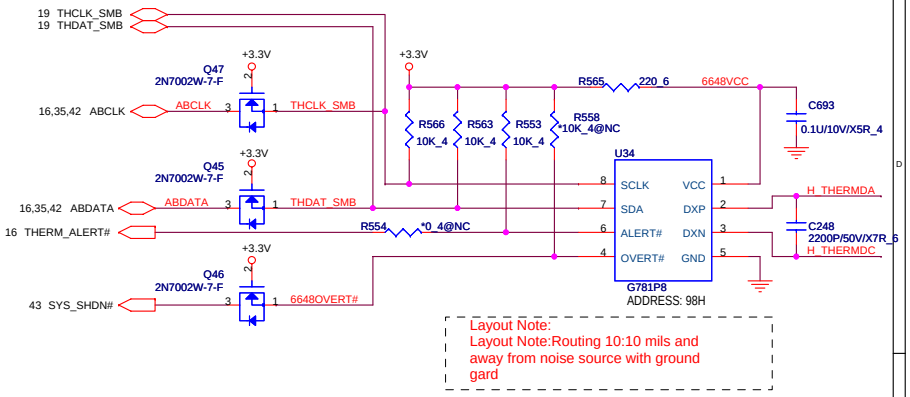
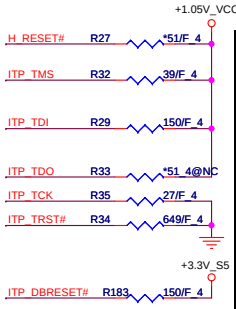
CPU(HOST)



CPU Thermal monitor



Populate ITP700Flex for bringup



ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

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Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	1A

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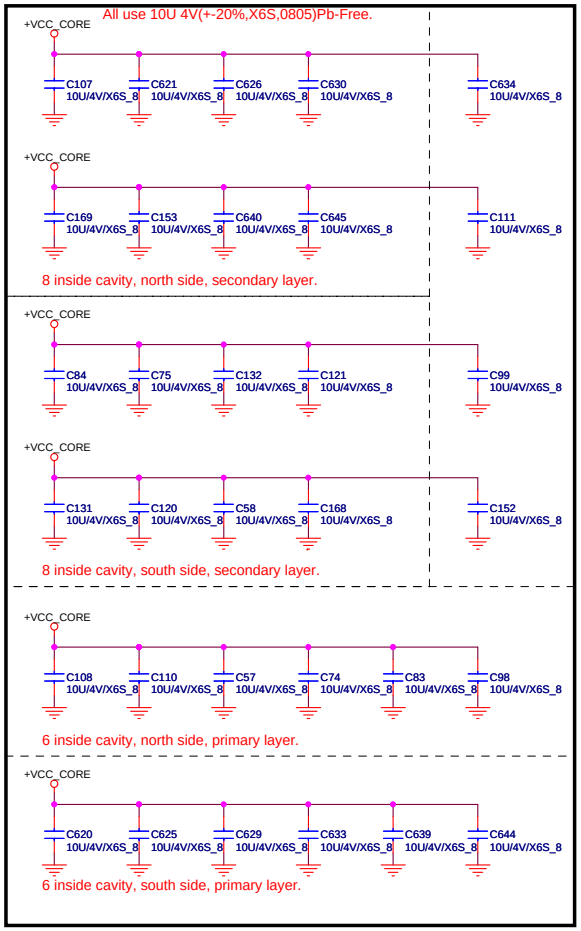
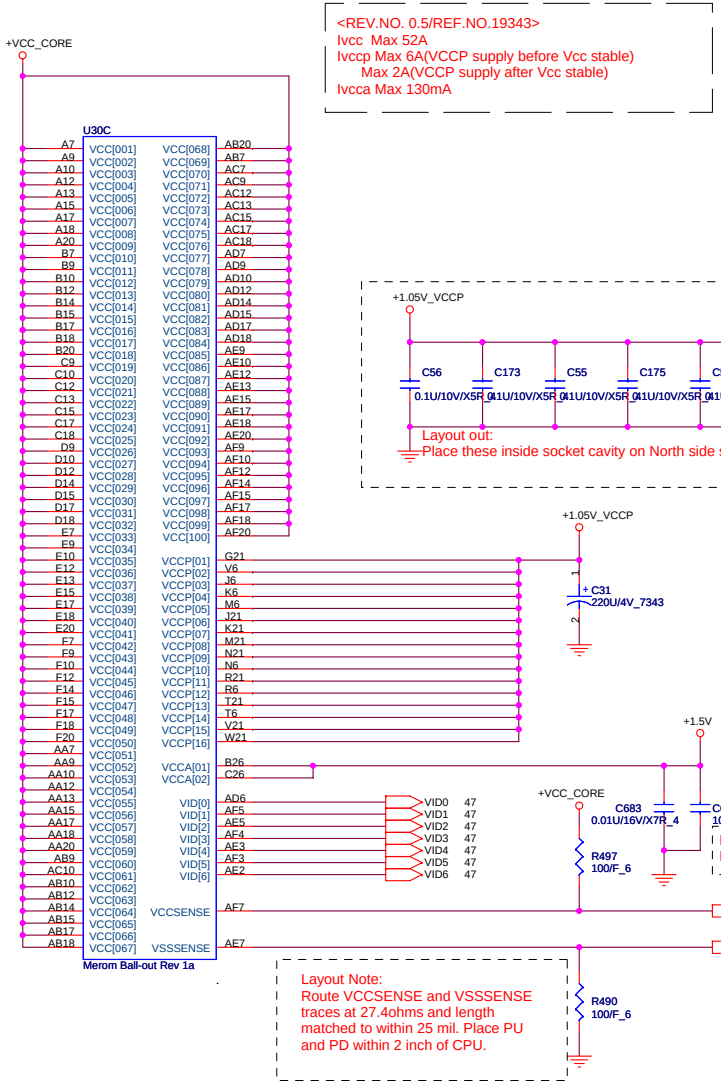
CPU(Power)





PROJECT : TA7			
Quanta Computer Inc.			
Size	Document Number		Rev
	CPU(2 of 2)		1A
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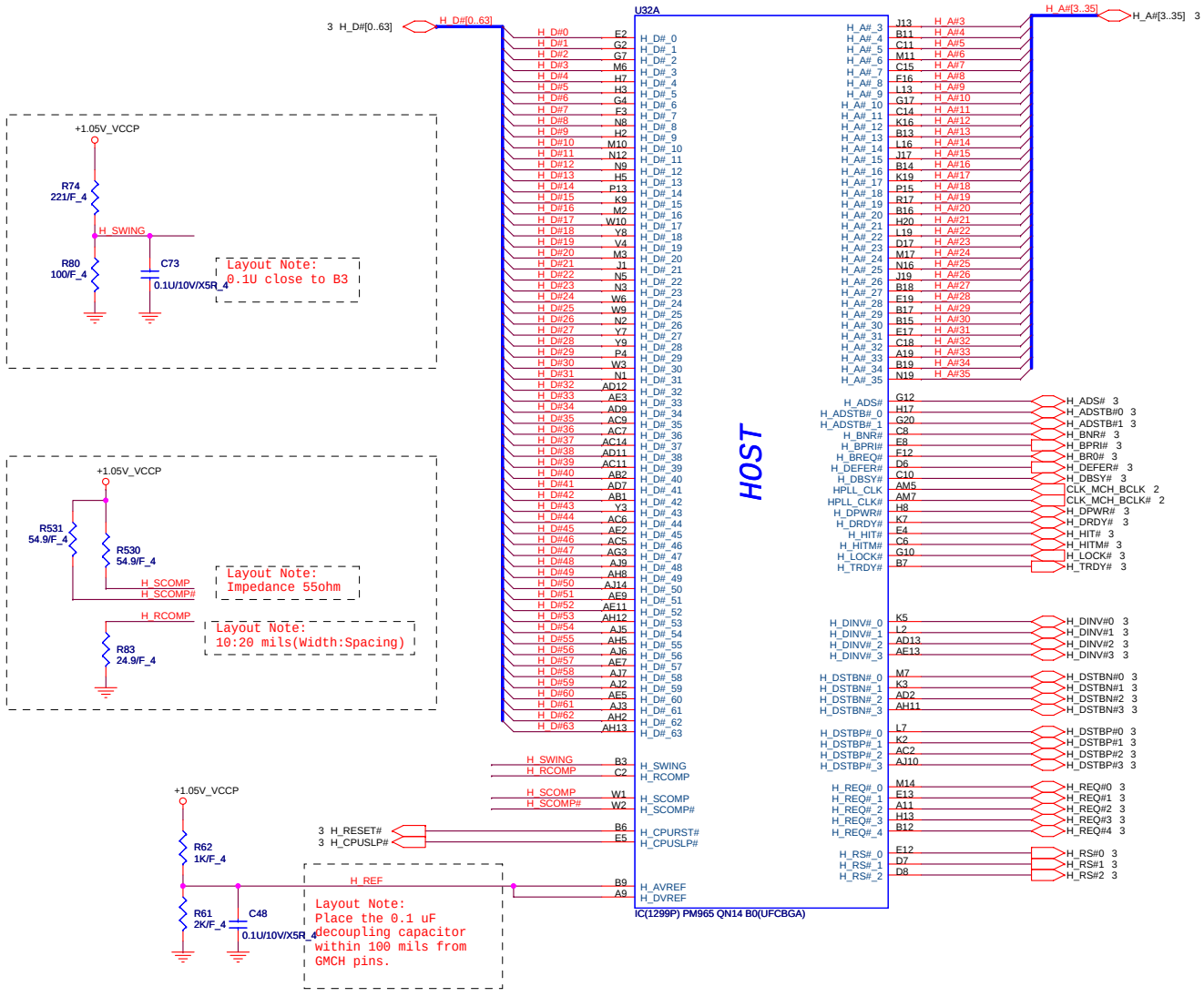
NB(HOST)



PROJECT : TA7
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Size	Document Number	Rev
	GMCH HOST(1 of 6)	1A
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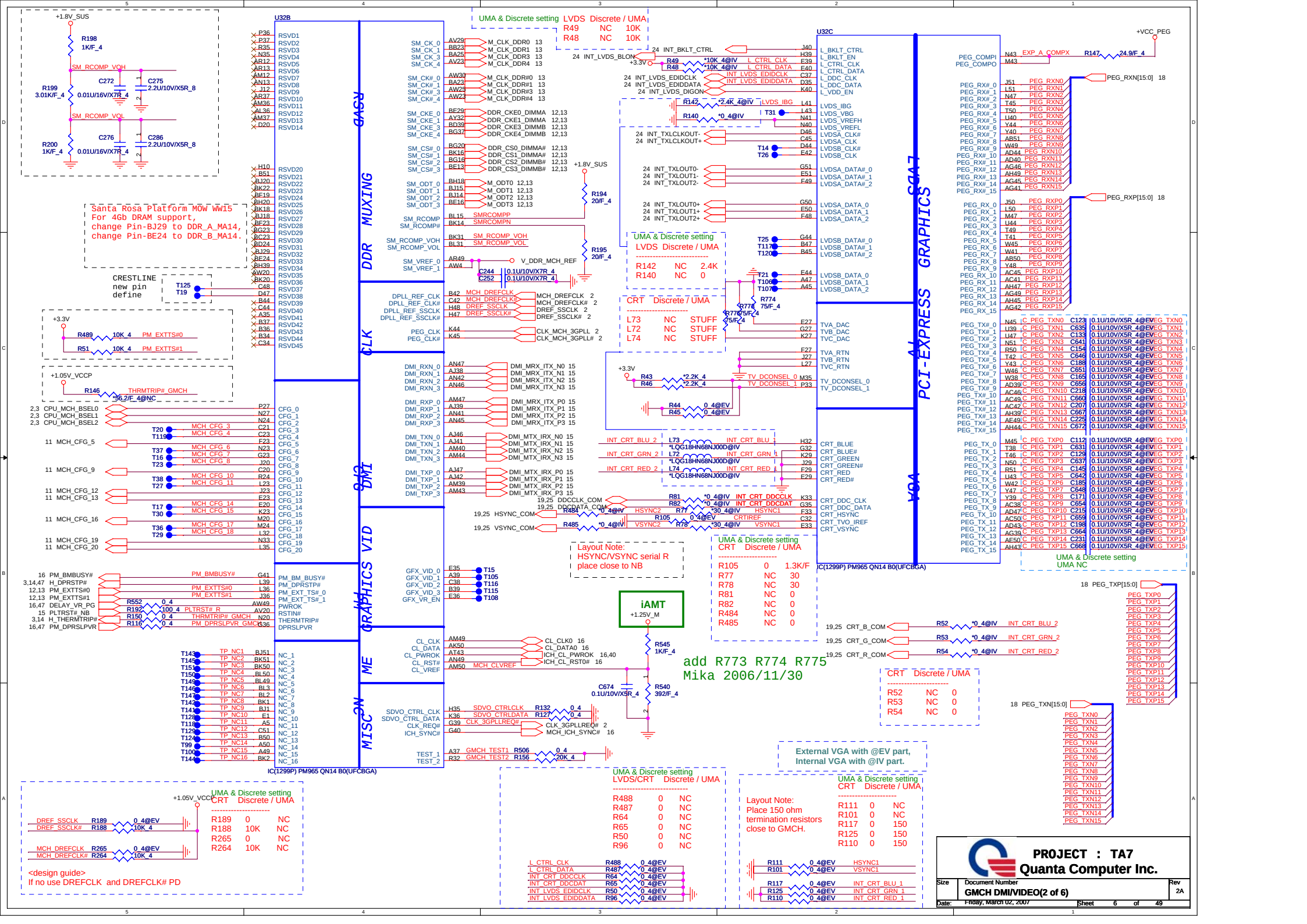
U32B
U32C
DMI
CLK
DDR MUXING
GRAPHICS VID
MISC
GMCH
PCI-EXPRESS GRAPHICS
SDVO
CRT
IC(1299P) PM965 QN14 B0(UFCBGA)
Santa Rosa Platform MOW WW15
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.
CRESTLINE
new pin
define
UMA & Discrete setting
LVDS Discrete / UMA
R49 NC 10K
R48 NC 10K
CRT Discrete / UMA
R142 NC 2.4K
R140 NC 0
L73 NC STUFF
L72 NC STUFF
L74 NC STUFF
R105 0 1.3K/F
R77 NC 30
R78 NC 30
R81 NC 0
R82 NC 0
R484 NC 0
R485 NC 0
R52 NC 0
R53 NC 0
R54 NC 0
LVDS/CRT Discrete / UMA
R488 0 NC
R487 0 NC
R64 0 NC
R65 0 NC
R50 0 NC
R96 0 NC
R189 0 NC
R188 10K NC
R265 0 NC
R264 10K NC
R111 0 NC
R101 0 NC
R117 0 150
R125 0 150
R110 0 150
UMA NC
iAMT
+1.25V_M
add R773 R774 R775
Mika 2006/11/30
Layout Note:
HSYNC/VSYNC serial R
place close to NB
Layout Note:
Place 150 ohm
termination resistors
close to GMCH.
External VGA with @EV part,
Internal VGA with @IV part.
<design guide>
If no use DREFCLK and DREFCLK# PD
PROJECT : TA7
Quanta Computer Inc.
GMCH DMI/VIDEO(2 of 6)
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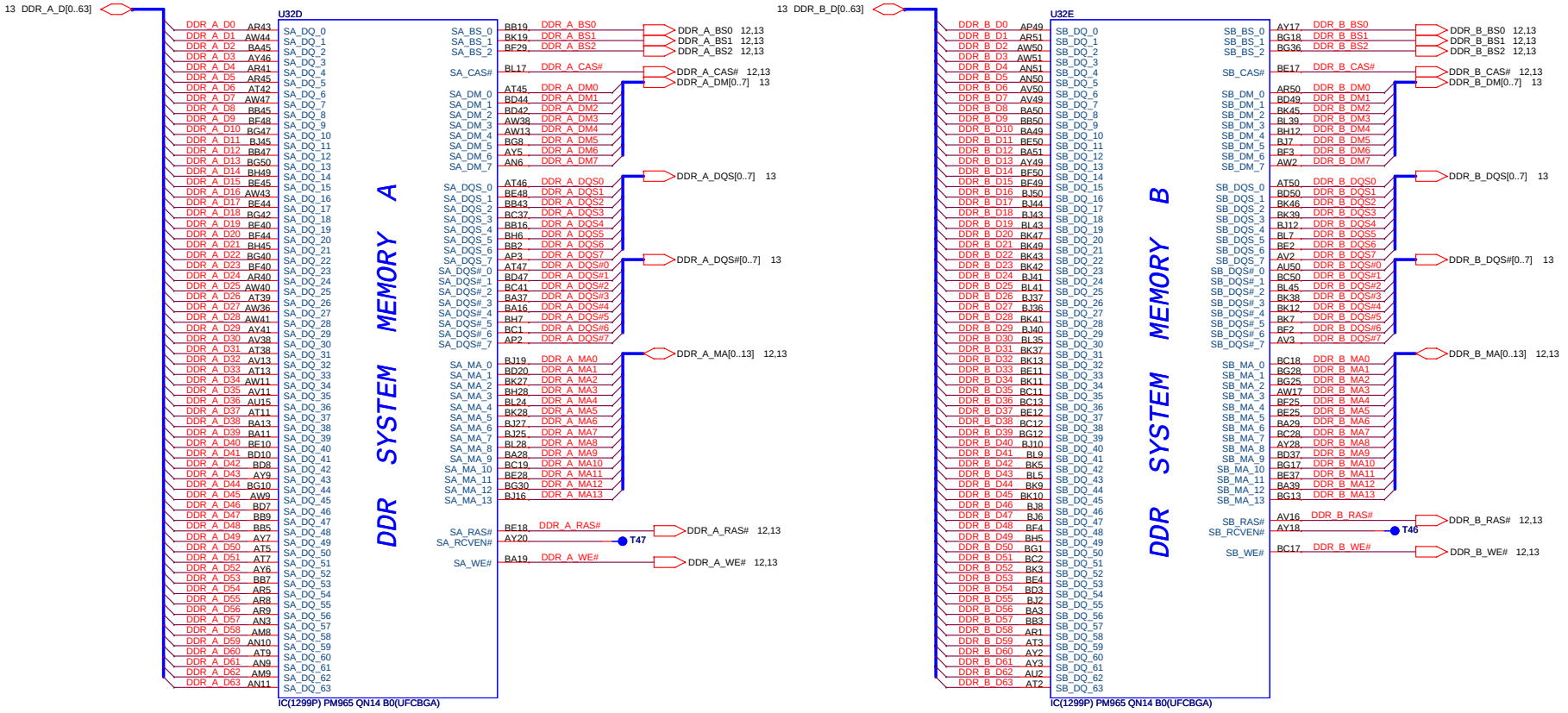
NB(Memory controller)



<OrgName>
<OrgAddr1>
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<OrgAddr4>

PROJECT : TA7

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR/Strap(3 of 6)	1A

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GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

POWER

+1.05V_VCCP

U32G

VCC CORE: AT35 AT34 AH28 AC32 AC31 AK32 AJ31 AJ28 AH32 AH31 AH29 AF32 R30 → VCC_1 VCC_2 VCC_3 VCC_5 VCC_4 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13

+1.8V_SUS

IVCCSM supply current 1 channel 1.615A 2 channel 3.138A

C246 0.1U/10V/X5R_4 | C309 + 220U/4V_7343 | C266 22U/4V/X6S_8 | C258 22U/4V/X6S_8

Layout Note: Place C125 where LVDS and DDR2 taps.

VCC SM: AU32 AU33 AU35 AV33 AW33 AW35 AY35 BA32 BA33 BA35 BB33 BC32 BC33 BC35 BD32 BD35 BE32 BE33 BE35 BF33 BE34 BG32 BG33 BG35 BH32 BH34 BH35 BJ32 BJ33 BJ34 BK32 BK33 BK34 BK35 BL33 AU30 → VCC_SM_1 … VCC_SM_36

change C309 value from 330U/2V to 220U/4V
Mika 2006/12/26

+VCC_AXG

VCC GFX: R20 T14 W13 W14 Y12 AA20 AA23 AA26 AA28 AB21 AB24 AB29 AC20 AC21 AC23 AC24 AC26 AC28 AC29 AD20 AD23 AD24 AD28 AF21 AF26 AA31 AH20 AH21 AH23 AH24 AH26 AD31 AJ20 AN14 → VCC_AXG_1 … VCC_AXG_34

IC(1299P) PM965 QN14 B0(UFCBGA)

VCC GFX NCTF: VCC_AXG_NCTF_1 … VCC_AXG_NCTF_83 → T17 T18 T19 T21 T22 T23 T25 U15 U16 U17 U19 U20 U21 U23 U26 V16 V17 V19 V20 V21 V23 V24 Y15 Y16 Y17 Y19 Y20 Y21 Y23 Y24 Y26 Y28 Y29 AA16 AA17 AB16 AB19 AC16 AC17 AC19 AD15 AD16 AD17 AE16 AF19 AH15 AH16 AH17 AH19 AJ16 AJ17 AK16 AK19 AL16 AL17 AL19 AL20 AL21 AL23 AM15 AM16 AM19 AM20 AM21 AM23 AP15 AP16 AP17 AP19 AP20 AP21 AP23 AP24 AR20 AR21 AR23 AR24 AR26 V26 V28 V29 Y31

VCC SM LF: VCC_SM_LF1 … VCC_SM_LF7 → AW45 BC39 BE39 BD17 BD4 AW8 AT6 (VCCSM_LF1 … VCCSM_LF7)

C241 0.1U/10V/X5R_4 | C254 1U/10V/X5R_4 | C261 22U/10V/X7R_6 | C262 0.22U/6.3V/X5R_4 | C269 0.47U/10V/X7R_6 | C251 1U/6.3V/X5R_6 | C256 1U/6.3V/X5R_6

+3.3V — R496 10_4 — +VCC_GMCH_L — D26 CH751H-40PT

Ivcc (External GFX 1.310 A, integrate 1.572 A)

+1.05V_VCCP

Layout Note: 370 mils from edge.

C604 220U/2.5V_7343 | C650 | C653 | C172 | C164 0.1U/10V/X5R_4 | 22U/4V/X6S_8 | 0.22U/6.3V/X5R_4 | 0.22U/6.3V/X5R_4

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

+VCC_AXG

Layout Note: 370 mils from edge.

R84 *HI0805R800R-5A | R85 *HI0805R800R-5A | +1.05V_VCCP

C139 *330U/2V_7343@NC | C181 *330U/2V_7343@NC | C249 *330U/2V_7343@NC | C104 *330U/2V_7343@NC

UMA & Discrete setting

C196 *0.1U/10V/X5R_4@IV | C187 0.1U/10V/X5R_4@IV | C228 *0.47U/10V/X7R_6@IV | C163 *1U/6.3V/X5R_6@IV | C156 *22U/4V/X6S_8@IV | C223 0_8@EV

UMA & Discrete setting

Layout Note: Inside GMCH cavity for VCC_AXG.

UMA & Discrete setting
VCC_AXG Discrete / UMA

R84	NC	STUFF
R85	NC	STUFF
C104	NC	NC
C249	NC	NC
C181	NC	330U
C139	NC	330U
C196	NC	0.1U
C187	NC	0.1U
C228	NC	0.47U
C163	NC	1U
C156	NC	22U
C223	0	10U

External VGA with @EV part, Internal VGA with @IV part.

Ivcc_AXM Controller supply current 540mA

iAMT +1.05V_M

Layout Note: Inside GMCH cavity for VCC_AXG.

C222 0.1U/10V/X5R_4 | C234 0.1U/10V/X5R_4 | C210 0.1U/10V/X5R_4

C235 22U/4V/X6S_8 | C240 0.22U/10V/X7R_6 | C220 0.22U/10V/X7R_6

Layout Note: Place close to GMCH edge.

U32F

VCC NCTF: VCC_NCTF_1 … VCC_NCTF_50 → AB33 AB36 AB37 AC33 AC35 AC36 AD35 AD36 AF33 AF36 AH33 AH35 AH36 AH37 AJ33 AJ35 AK33 AK35 AK36 AK37 AD33 AJ36 AM35 AL33 AL35 AA33 AA35 AA36 AP35 AP36 AR35 AR36 Y32 Y33 Y35 Y36 Y37 T30 T34 T35 U29 U31 U32 U33 U35 U36 V32 V33 V36 V37

VSS NCTF: VSS_NCTF_1 … VSS_NCTF_21 → T27 T37 U24 U28 V31 V35 AA19 AB17 AB35 AD19 AD37 AF17 AF35 AK17 AM17 AM24 AP26 AP28 AR15 AR19 AR28

VSS SCB: VSS_SCB1 … VSS_SCB6 → A3 B2 C1 BL1 BL51 A51

iAMT +1.05V_M

VCC AXM NCTF: VCC_AXM_NCTF_1 … VCC_AXM_NCTF_19 → AL24 AL26 AL28 AM26 AM28 AM29 AM31 AM32 AM33 AP29 AP31 AP32 AP33 AL29 AL31 AL32 AR31 AR32 AR33

VCC AXM: VCC_AXM_1 … VCC_AXM_7 → AT33 AT31 AK29 AK24 AK23 AJ26 AJ23

IC(1299P) PM965 QN14 B0(UFCBGA)

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	GMCH Power-1(4 of 6)	1A
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UMA & Discrete setting
PLL Discrete / UMA
L13 NC 10uH
C38 NC 470U
C72 0 0.1U
L77 NC 10uH
C600 NC 470U
C102 0 0.1U

UMA & Discrete setting
CRT Discrete / UMA
R55 NC 0
C42 NC 0.1U
R59 NC 0
R124 0 22nF
C610 NC 10U
L66 NC STUFF
C609 NC 0.1U
R504 NC 0
R87 0 22nF

External VGA with @EV part,
Internal VGA with @IV part.

IVCC_SYNC current 0.01A

IVCCA_DPLLA~B current 0.08A

IVCCA_HPLL current 0.05A

IVCCA_MPLL current 0.15A

IVCCA_LVDS current 0.01A

UMA & Discrete setting LVDS Discrete / UMA
R95 0 1000P

IVCCA_PEG_BG current 0.04A

change C306 value
from 100U/10V to 220U/4V
Mika 2006/12/26

IVCCD_CRT current 0.06A

IVCCD_TVDAC current 0.06A

IVCC_QDAC current 0.005A

UMA & Discrete setting
CRT Discrete / UMA
L18 NC 100ohm
C60 NC 0.1U
R72 NC 0
R148 0 1UF
R133 0 NC
R141 NC 0

IVCCD_HPLL current 0.25A

IVCCA/D_PEG_PLL current 0.1A

IVCCD_LVDS current 0.15A

UMA & Discrete setting
LVDS Discrete / UMA
R58 NC 0
C71 0 1U
C50 NC NC
C80 NC 1000P

If:SDVO Disabled,VCCD_LVDS to GND.
If:SDVO Enabled,VCCD_LVDS to +1.8V.

IC(1299P) PM965 QN14 B0(UFCBGA)

Ivtt_FSB core supply current 0.85A

Ivcc_AXD current 0.25A

Ivcc_AXF current 0.35A

Ivcc_DMI current 0.1A

Ivcc_SM_CK current 0.2A

IVCC_TX_LVDS current 0.1A

IVCC_HV current 0.1A

UMA & Discrete setting
LVDS Discrete / UMA
L65 NC 1UH
C34 NC 220U
R97 0 1000P

Ivcc_PEG PCI-E current 1.2A

Ivcc_RX_DMI current 0.25A

+3V_VCC_HV

40 mil wide

D8 *CH751H-40PT

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	GMCH Power-2(5 of 6)	1A
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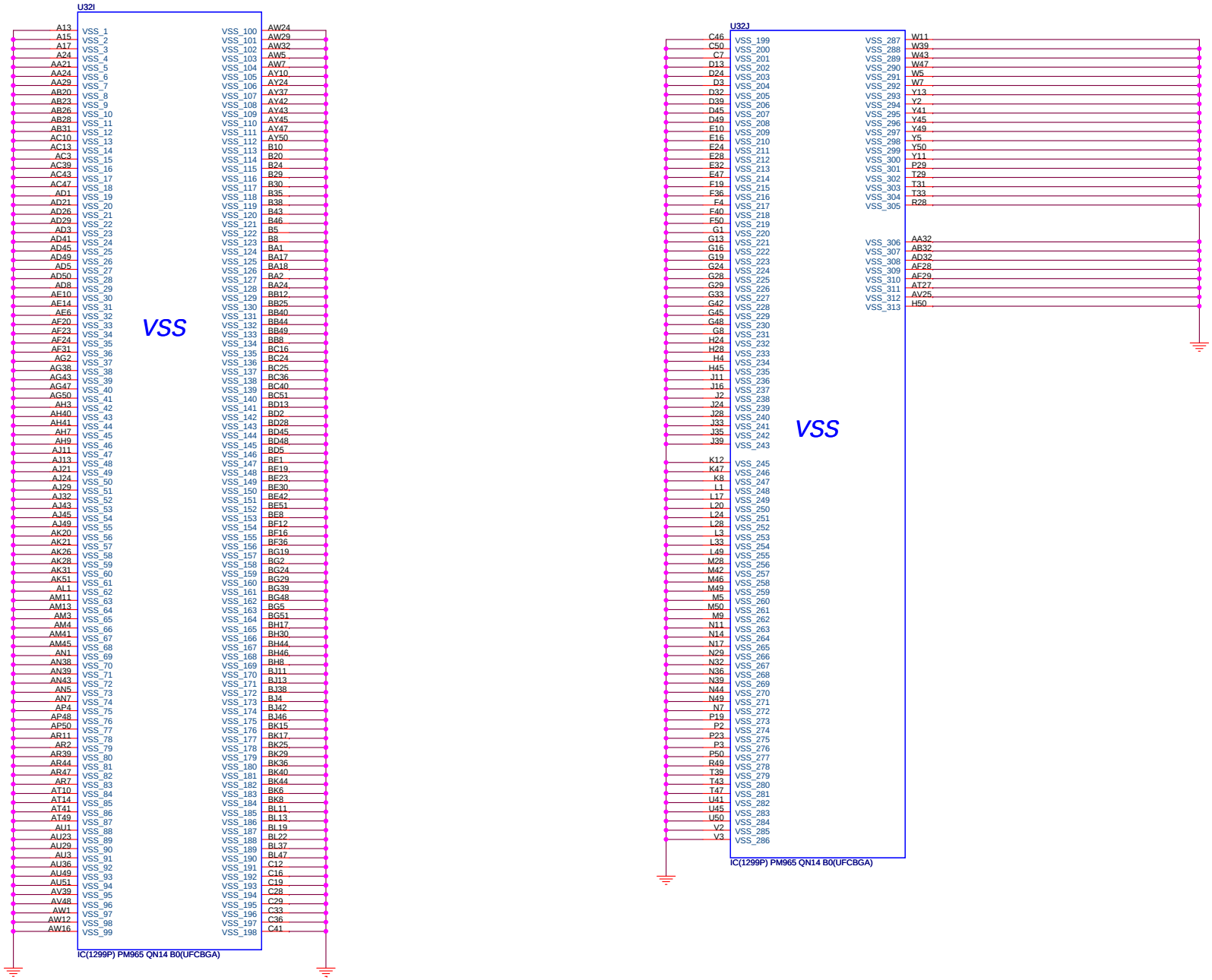
NB(Power-3)



PROJECT : TA7

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Size	Document Number	Rev
	GMCH Power-3(6 of 6)	1A
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Strap table

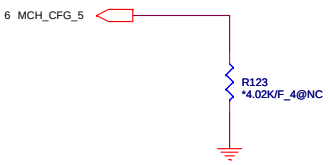
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

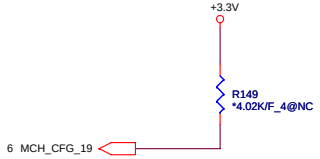
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



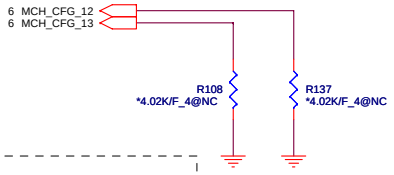
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



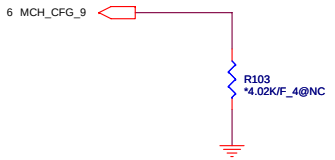
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

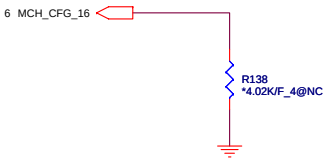


SDVO Present

Strap define at External DVI control page

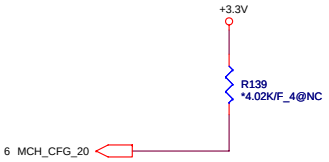
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

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Size	Document Number	Rev
	GMCH Strap Table	1A
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DDR2 Dual channel A/B PU

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C353 C406 C408 C389 C363 C409 C362 C405 C404 C426 C388 C350 C386
0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C390 C428 C427 C403 C351 C352 C354 C349 C425 C387 C407 C402 C429
0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4 0.1U/10V/X5R_4

Please these resistor closely DIMMA,all trace length<750 mil.

+0.9V_DDR_VTT

7,13 DDR_A_MA[0..13]								DDR_B_MA[0..13] 7,13
6,13 M_ODT0	M_ODT0	RP32	56X2	RP17	56X2	DDR_B_BS1		DDR_B_BS1 7,13
	DDR_A_MA13					DDR_B_MA0		
	DDR_A_MA8	RP22	56X2	RP10	56X2	DDR_B_MA5		
	DDR_A_MA5					DDR_B_MA3		
	DDR_A_MA3	RP23	56X2	RP9	56X2	DDR_B_MA1		
	DDR_A_MA1					DDR_B_MA8		
6,13 DDR_CKE1_DIMMA		RP27	56X2	RP16	56X2	DDR_B_MA4		
	DDR_A_MA11					DDR_B_MA2		
	DDR_A_MA10	RP24	56X2	RP8	56X2	DDR_B_MA12		
7,13 DDR_A_BS0	DDR_A_BS0					DDR_B_MA9		
	DDR_A_MA7	RP28	56X2	RP15	56X2	DDR_B_MA7		
	DDR_A_MA6					DDR_B_MA6		
	DDR_A_MA2	RP29	56X2	RP7	56X2			DDR_B_BS2 7,13
	DDR_A_MA4							DDR_CKE3_DIMMB 6,13
7,13 DDR_A_RAS#	DDR_A_RAS#	RP31	56X2	RP18	56X2	DDR_B_RAS#		DDR_B_RAS# 7,13
7,13 DDR_A_BS1	DDR_A_BS1					DDR_B_MA13		
	DDR_A_MA9	RP21	56X2	RP12	56X2	DDR_B_WE#		DDR_B_WE# 7,13
	DDR_A_MA12					DDR_B_CAS#		DDR_B_CAS# 7,13
7,13 DDR_A_WE#	DDR_A_WE#	RP25	56X2	RP11	56X2	DDR_B_MA10		
7,13 DDR_A_CAS#	DDR_A_CAS#					DDR_B_BS0		DDR_B_BS0 7,13
6,13 DDR_CS0_DIMMA#		RP30	56X2	RP19	56X2	M_ODT2		M_ODT2 6,13
	DDR_A_MA0							DDR_CS2_DIMMB# 6,13
6,13 DDR_CS1_DIMMA#		RP26	56X2	RP13	56X2			M_ODT3 6,13
6,13 M_ODT1								DDR_CS3_DIMMB# 6,13
6,13 DDR_CKE0_DIMMA		RP20	56X2	RP14	56X2			DDR_CKE4_DIMMB 6,13
7,13 DDR_A_BS2						DDR_B_MA11		

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V_M

R293 *220_6@NC

C431 *0.1U/10V/X5R_4@NC

U19

2,13 CGCLK_SMB_M	8	SCLK	VCC	1	LM86_3V
2,13 CGDAT_SMB_M	7	SDA	DXP	2	DDR_THERMDA
6,13 PM_EXTTS#0	6	ALERT#	DXN	3	C417 *1000P/16V/X7R_4
6,13 PM_EXTTS#1	4	OVERT#	GND	5	DDR_THERMDC

R279 *0_4@NC

*LM86CIMM@NC

*MMBT3904_NL@NC Q24

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Quanta Computer Inc.

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	DDR RES. ARRAY	1A
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A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

CN33

DDR2_SODIMM
H 9.2

PC4800 DDR2 SDRAM SO-DIMM (200P)

CKE 0,1
CLOCK 0,1

SMbus address A0

CN31

2-1734073-2
H 5.2

PC4800 DDR2 SDRAM SO-DIMM (200P)

CKE 3,4
CLOCK 3,4

SMbus address A4

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

iAMT

PROJECT : TA7
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	DDR SO-DIMM(200P)	1A
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RTC

SB Strap

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically,keep the same distance from T for all series termination resistors.

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

Layout Note: L<500mils

Layout Note: Placement close SB L<2"

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH8M REV 1.0

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Quanta Computer Inc.

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	ICH8M HOST(1 of 4)	1A
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Place TX DC blocking caps close ICH8.

32 PCIE_TX1-
32 PCIE_TX1+
C778 0.1U/10V/X5R_4 PCIE_TXN1_C
C782 0.1U/10V/X5R_4 PCIE_TXP1_C

32 PCIE_TX2-
32 PCIE_TX2+
C786 0.1U/10V/X5R_4 PCIE_TXN2_C
C788 0.1U/10V/X5R_4 PCIE_TXP2_C

26 PCIE_TX6-/GLAN_TX-
26 PCIE_TX6+/GLAN_TX+
C811 0.1U/10V/X5R_4 GLAN_TXN_C
C807 0.1U/10V/X5R_4 GLAN_TXP_C

U39D

32 PCIE_RX1-
32 PCIE_RX1+
MiniWLAN
PCIE_TXN1_C
PCIE_TXP1_C

32 PCIE_RX2-
32 PCIE_RX2+
MiniWWAN
PCIE_TXN2_C
PCIE_TXP2_C

PCI-Express Direct Media Interface

P27 PERN1
P26 PERP1
N29 PETN1
N28 PETP1
M27 PERN2
M26 PERP2
L29 PETN2
L28 PETP2
K27 PERN3
K26 PERP3
J29 PETN3
J28 PETP3
H27 PERN4
H26 PERP4
G29 PETN4
G28 PETP4
F27 PERN5
F26 PERP5
E29 PETN5
E28 PETP5
D27 PERN6/GLAN_RXN
D26 PERP6/GLAN_RXP
C29 PETN6/GLAN_TXN
C28 PETP6/GLAN_TXP

26 PCIE_RX6-/GLAN_RX-
26 PCIE_RX6+/GLAN_RX+
GLAN_TXN_C
GLAN_TXP_C

DMI0RXN V27
DMI0RXP V26
DMI0TXN U29
DMI0TXP U28
DMI1RXN Y27
DMI1RXP Y26
DMI1TXN W29
DMI1TXP W28
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA29
DMI2TXP AA28
DMI3RXN AD27
DMI3RXP AD26
DMI3TXN AC29
DMI3TXP AC28
DMI_CLKN T26
DMI_CLKP T25
DMI_ZCOMP Y23
DMI_IRCOMP Y24

DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6
DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6
DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6
DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6
CLK_PCIE_ICH# 2
CLK_PCIE_ICH 2

+1.5V_PCIE_ICH
R376 24.9/F_4
DMI_IRCOMP_R
Layout Note: DMI_IRCOMP_R<500mils

SPI

27 ICH_SPI_CLK
27 ICH_SPI_CS0#
27 ICH_SPI_CS1#
R395 15_4
R399 15_4
R391 15_4
SPI_CS1#_R
C23 SPI_CLK
B23 SPI_CS0#
E22 SPI_CS1#

27 ICH_SPI_DIN
27 ICH_SPI_DO
R396 0_4
D23 SPI_MOSI
F21 SPI_MISO

USB

34 USB_OC0#
34 USB_OC1#
34 USB_OC2#
USB_OC0#
USB_OC1#
USB_OC2#
USB_OC3#
USB_OC4#
USB_OC5#
AJ19 OC0#
AG16 OC1#/GPIO40
AG15 OC2#/GPIO41
AE15 OC3#/GPIO42
AE15 OC4#/GPIO43
AG17 OC5#/GPIO29
AD12 OC6#/GPIO30
AJ18 OC7#/GPIO31
AD14 OC8#
AH18 OC9#

32 WLAN_RF_OFF#
33,35 BAYINS#
WLAN_RF_OFF#
USB_OC8#
USB_OC9#

USBP0N G3
USBP0P G2
USBP1N H5
USBP1P H4
USBP2N H2
USBP2P H1
USBP3N J3
USBP3P J2
USBP4N K5
USBP4P K4
USBP5N K2
USBP5P K1
USBP6N L3
USBP6P L2
USBP7N M5
USBP7P M4
USBP8N M2
USBP8P M1
USBP9N N3
USBP9P N2

USBP0- 34
USBP0+ 34
USBP1- 34
USBP1+ 34
USBP2- 34
USBP2+ 34
T73
T74
USBP4- 38
USBP4+ 38
T164
T163
USBP6- 38
USBP6+ 38
USBP7- 32
USBP7+ 32
USBP8- 36
USBP8+ 36
USBP9- 32
USBP9+ 32

System
System
System
Docking 1
BLUETOOTH
MiniCard 2 WWAN
FINGER PRINT
MiniCard 1 WWAN

USBRBIAS# F2
USBRBIAS F3
USB_RBIAS_PN
R660 22.6/F_6
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8M REV 1.0

iAMT

+3.3V_S5
RP33
USB_OC2# 6
WLAN_RF_OFF# 7
USB_OC4# 8
USB_OC3# 9
10
5 USB_OC1#
4 BAYINS#
3 USB_OC0#
2 USB_OC5#
1
10K-10P8R

R332 10K_4 USB_OC8#
R617 10K_4 USB_OC9#

ICH8 Boot BIOS select

Boot BIOS Strap		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

SPI_CS1#_R R392 *1K_4@NC
PCI_GNT0# R386 *1K_4@NC

A16 SWAP Override strap

SB_NB_PCIE_RST#	Low = A16 swap override enabled High = Default

SB_NB_PCIE_RST# R394 *1K_4@NC

SB-PCI

U39B

28 PCI_AD[0..31]

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 F12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 F8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

REQ0# A4 PCI_REQ0#
GNT0# D7 PCI_GNT0#
REQ1#/GPIO50 E18 BOARD_ID1
GNT1#/GPIO51 C18 BOARD_ID2
REQ2#/GPIO52 B19 PCI_REQ2#
GNT2#/GPIO53 F18 PCI_GNT2#
REQ3#/GPIO54 A11 PCI_REQ3#
GNT3#/GPIO55 C10 SB_NB_PCIE_RST#

PCI_REQ0# 28
PCI_GNT0# 28
BOARD_ID1 16
BOARD_ID2 16
T81

C/BE0# C17
C/BE1# E15
C/BE2# F16
C/BE3# E17
PCI_C_BE0# 28
PCI_C_BE1# 28
PCI_C_BE2# 28
PCI_C_BE3# 28

IRDY# C8 PCI_IRDY#
PAR D9
PCIRST# G6
DEVSEL# D16 PCI_DEVSEL#
PERR# A7 PCI_PERR#
PLOCK# B7 PCI_PLOCK#
SERR# F10 PCI_SERR#
STOP# C16 PCI_STOP#
TRDY# C9 PCI_TRDY#
FRAME# A17 PCI_FRAME#

PCI_IRDY# 28
PCI_PAR 28
PCIRST# 28,37
PCI_DEVSEL# 28
PCI_PERR# 28
PCI_SERR# 28
PCI_STOP# 28
PCI_TRDY# 28
PCI_FRAME# 28

PLTRST# AG24 PLTRST#_NB
PCICLK B10 CLK_PCI_ICH
PME# G7
PLTRST#_NB 6
CLK_PCI_ICH 2
ICH_PME# 28

+3.3V
C436 0.1U/10V/X5R_4
U21 TC7SH08FU(F)
PLTRST# 16,18,32,37,38
R308 100K_4

Interrupt I/F

28 PCI_PIRQB#
28 PCI_PIRQC#
28 PCI_PIRQD#
R393 *0_4
PCI_PIRQA# F9 PIRQA#
PCI_PIRQB# B5 PIRQB#
PCI_PIRQC# C5 PIRQC#
PCI_PIRQD#_R A10 PIRQD#
PIRQE#/GPIO2 F8 BAYID0
PIRQF#/GPIO3 G11 BAYID1
PIRQG#/GPIO4 E12 ICH_GPIO4_PIRQG#
PIRQH#/GPIO5 B3 ICH_GPIO5_PIRQH#
BAYID0 33
BAYID1 33

ICH8M REV 1.0

Cardbus/ CardReader/1394	REQ0	GNT0	PIRQA PIRQB PIRQC

Reserved for EMI. Place resister and cap close to ICH.
CLK_PCI_ICH
R685 *10_4@NC
C834 *10P/50V_4@NC

PCI Pullups

RP51
PCI_STOP# 6
PCI_REQ2# 7
PCI_FRAME# 8
9
10
+3.3V
5 PCI_REQ3#
4 PCI_PIRQD#
3 PCI_TRDY#
2 PCI_DEVSEL#
1
8.2K-10P8R

RP39
PCI_SERR# 6
PCI_IRDY# 7
PCI_PERR# 8
PCI_PLOCK# 9
10
+3.3V
5
4
3 PCI_REQ0#
2 ICH_GPIO4_PIRQG#
1 BAYID1
8.2K-10P8R

RP50
6
7
8
PCI_PIRQA# 9
10
+3.3V
5 BAYID0
4 PCI_PIRQC#
3 PCI_PIRQB#
2 ICH_GPIO5_PIRQH#
1
8.2K-10P8R

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

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Quanta Computer Inc.

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	ICH8M PCIE(2 of 4)	1A

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remove R241 for S3 leakage current
Mika 2007/02/26

iAMT

+3.3V_S5
R336 10K_4 ICH_CL_RST1#
R334 10K_4 ICH_RI#
R322 10K_4 SCI#
R333 1K_4 ICH_PCIE_WAKE#

R336 NON-IAMT 10K
IAMT NC

iAMT

+3.3V_S5
R629 2.2K_4 ICH_SMBCLK
R335 2.2K_4 ICH_SMBDATA
R366 10K_4 AMT_SMBCLK
R368 10K_4 AMT_SMBDATA

iAMT

+3.3V_S5
Q28 *2N7002W-7-F
AMT_SMBCLK
ABCLK
ABCLK 3,35,42
Q29 *2N7002W-7-F
AMT_SMBDATA
ABDATA
ABDATA 3,35,42

+3.3V_M
R711 *10K_4@AMT H_STP_PCI#
R710 *10K_4@AMT H_STP_CPU#

+3.3V
R595 8.2K_4
CLKRUN#
R620 *10K_4@NC
Option to " Disable " clkrun. Pulling it down will keep the clks running.

U39C

2,32 ICH_SMBCLK
2,32 ICH_SMBDATA
32 ICH_CL_RST1#
ICH_SMBCLK AJ26 SMBCLK
ICH_SMBDATA AD19 SMBDATA
ICH_CL_RST1# AG21 LINKALERT#
AMT_SMBCLK AC17 SMLINK0
AMT_SMBDATA AE19 SMLINK1
SMB
ICH_RI# AF17 RI#
32,37,38 LPC_PD#
3 ITP_DBRESET#
LPC_PD# F4 SUS_STAT#/LPCPD#
AD15 SYS_RESET#
6 PM_BMBUSY# AG12 BMBUSY#/GPIO0
35 SCI# SCI# AG22 SMBALERT#/GPIO11
2 H_STP_PCI#
2 H_STP_CPU#
H_STP_PCI# AE20 STP_PCI#/GPIO15
H_STP_CPU# AG18 STP_CPU#/GPIO25
28,32,37,38 CLKRUN#
CLKRUN# AH11 CLKRUN#/GPIO32
32 ICH_PCIE_WAKE#
28,32,35,37,38 IRQ_SERIRQ
3 THERM_ALERT#
ICH_PCIE_WAKE# AE17 WAKE#
IRQ_SERIRQ AE12 SERIRQ
THERM_ALERT# AC13 THRM#
SYS GPIO
VR_PWRGD_CLKEN AJ20 VRMPWRGD
T158 AJ22 TP7
Power MGT
T154 RSVD_GPIO1 AJ8 TACH1/GPIO1
24 FPBACK# FPBACK# AJ9 TACH2/GPIO6
PEN_SW AH9 TACH3/GPIO7
35 KBSMI# KBSMI# AE16 GPIO8
46 LAN_POWER_SB AC19 GPIO12
BOARD_ID0 AG8 TACH0/GPIO17
T66 BOARD_ID3 AH12 GPIO18
AE11 GPIO20
T155 RSVD_GPIO22 AG10 SCLOCK/GPIO22
38 BT_ON# BT_ON# AH25 QRT_STATE0/GPIO27
2 SATA_CLKREQ# RST_BAY_R# AD16 QRT_STATE1/GPIO28
SATA_CLKREQ# AG13 SATACLKREQ#/GPIO35
T69 RSVD_GPIO38 AF9 SLOAD/GPIO38
T156 RSVD_GPIO39 AJ11 SDATAOUT0/GPIO39
38 TPM_SENSE# AD10 SDATAOUT1/GPIO48
30 ACZ_SPKR ACZ_SPKR AD9 SPKR
6 MCH_ICH_SYNC# R315 0_4 MCH_ICH_SYNC#_R AJ13 MCH_SYNC#
14 ICH_RSVD AJ21 TP3
GPIO Controller Link
MISC
ICH8M REV 1.0

SATA GPIO
SATA0GP/GPIO21 AJ12 R605 8.2K_4
SATA1GP/GPIO19 AJ10 R602 8.2K_4
SATA2GP/GPIO36 AE11 R328 8.2K_4
SATA3GP/GPIO37 AG11 R327 8.2K_4
+3.3V
Clocks
CLK14 AG9 CLK_ICH_14M
CLK48 G5 CLK_ICH_48M
SUSCLK D3 ICH_SUSCLK T82
SLP_S3# AG23 SLP_S3# R616 100/F_4 SUSB# 35
SLP_S4# AE21 SLP_S4# R313 100/F_4 SUSC# 35
SLP_S5# AD18 SLP_S5# T70
S4_STATE#/GPIO26 AH27 S4_STAT# 35
PWROK AE23 ICH_PWROK
DPRSLPVR/GPIO16 AJ14 PM_DPRSLPVR_R R608 100/F_4 PM_DPRSLPVR
BATLOW# AE21 PM_BATLOW#_R
PWRBTN# C2 DNBSWON#
LAN_RST# AH20 PM_LAN_ENABLE_R R619 0_4 R618 *0_4@NC R594 *0_4@NC R340 100/F_4 RSMRST#
RSMRST# AG27 PM_RSMRST#_R
CK_PWRGD E1
CLPWROK E3 ICH_CL_PWROK
SLP_M# AJ25
CL_CLK0 F23
CL_CLK1 AE18
CL_DATA0 F22
CL_DATA1 AF19
CL_VREF0 D24 CL_VREF0_SB
CL_VREF1 AH23 CL_VREF1_SB
CL_RST# AJ23
MEM_LED/GPIO24 AJ27 BAYON#
ME_EC_ALERT/GPIO10 AJ24
EC_ME_ALERT/GPIO14 AE22 EC_ME_ALERT
WOL_EN/GPIO9 AG19 LAN_WOL_EN

CLK_CLK0 6
ICH_CL_CLK1 32
CL_DATA0 6
ICH_CL_DATA1 32
ICH_CL_RST0# 6
BAYON# 33
ME_EC_ALERT 35
EC_ME_ALERT 35
LAN_WOL_EN 35
CLK_ICH_14M 2
CLK_ICH_48M 2
SUSB# 35
SUSC# 35
S4_STAT# 35
PM_DPRSLPVR 6,47
DNBSWON# 35
PM_LAN_RST# 35
PLTRST# 15,18,32,37,38
RSMRST# 35
CLK_PWRGD 2
ICH_CL_PWROK 6,40
SUSM# 35

+3.3V_S5
R241 *10K_4
PM_LAN_RST#

Place these close to ICH8.
CLK_ICH_48M R380 *10_4@NC C480 *10P/50V_4@NC
CLK_ICH_14M R342 *33_4@NC C445 *10P/50V_4@NC

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

+3.3V
0.1U/10V/X5R_4 C435
33 RST_BAY#
R304 100K_4
U20 TC7SH08FU(F)
R305 *0_4@NC
2 SATA_CLKREQ#

iAMT
+3.3V_S5
+3.3V_M
R593 3.24K/F_4
R398 3.24K/F_4
R591 453/F_4
C449 0.1U/10V/X5R_4
R397 453/F_4
C510 0.1U/10V/X5R_4
Controller Link 1 VREF for IAMT support only

+3.3V_S5
R337 10K_4 PM_BATLOW#_R
R371 10K_4 KBSMI#
R306 10K_4 RST_BAY_R#
R626 10K_4 BT_ON#
R667 10K_4 DNBSWON#
R633 10K_4 BAYON#
R320 *10K_4@NC EC_ME_ALERT
R367 10K_4 LAN_POWER_SB

+3.3V
R369 8.2K_4 THERM_ALERT#
R606 *10K_4@NC MCH_ICH_SYNC#_R
R329 10K_4 IRQ_SERIRQ
R613 *2.2K_4@NC VR_PWRGD_CLKEN
R600 10K_4 PEN_SW
R599 10K_4 RSVD_GPIO1
R603 10K_4 RSVD_GPIO22
R323 10K_4 RSVD_GPIO38
R604 10K_4 RSVD_GPIO39
R326 1M_4 TPM_SENSE#
R601 10K_4 FPBACK#

No Reboot strap
HDA_SPKR | Low = Default High = No Reboot
+3.3V
*10K_4@NC R360 ACZ_SPKR

PM_DPRSLPVR R314 *100K_4@NC
RSMRST# R596 10K_4
PM_LAN_ENABLE_R R592 *1M_4@NC
ICH_CL_PWROK R385 1M_4
LAN_WOL_EN R354 100K_4

U36
+3.3V
47 VR_PWRGD_CLKEN#
C753 0.1U/10V/X5R_4
VR_PWRGD_CLKEN
NL17SZ14DFT2G
R590 100K_4

+3.3V
+3.3V_SUS
R378 2K_4
C478 0.1U/10V/X5R_4
6,47 DELAY_VR_PG
35,40 PWROK
ICH_PWROK
U23 TC7SH08FU(F)
R375 100K_4
R374 10K_4

SW12
R301 1K_4
SWAP_SWITCH
PEN_SW
C433 1000P/16V/X7R_4
PEN DETECT SWITCH

GPIO[20]--(PCIE_MCARD2_DET#)
Integrated Pull-Down 20K.

Board ID	ID3	ID2	ID1	ID0
Default	1	1	1	1
RSV	0	0	0	1
RSV	0	0	1	0
RSV	0	0	1	1
RSV	0	1	0	0

+3.3V
R361 1K_4
R362 *10K_4@NC
R390 10K_4
R389 *10K_4@NC
R387 10K_4
R388 *10K_4@NC
R598 10K_4
R597 *10K_4@NC
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID1 15
BOARD_ID2 15

PROJECT : TA7
Quanta Computer Inc.
Size
Document Number ICH8M GPIO(3 of 4)
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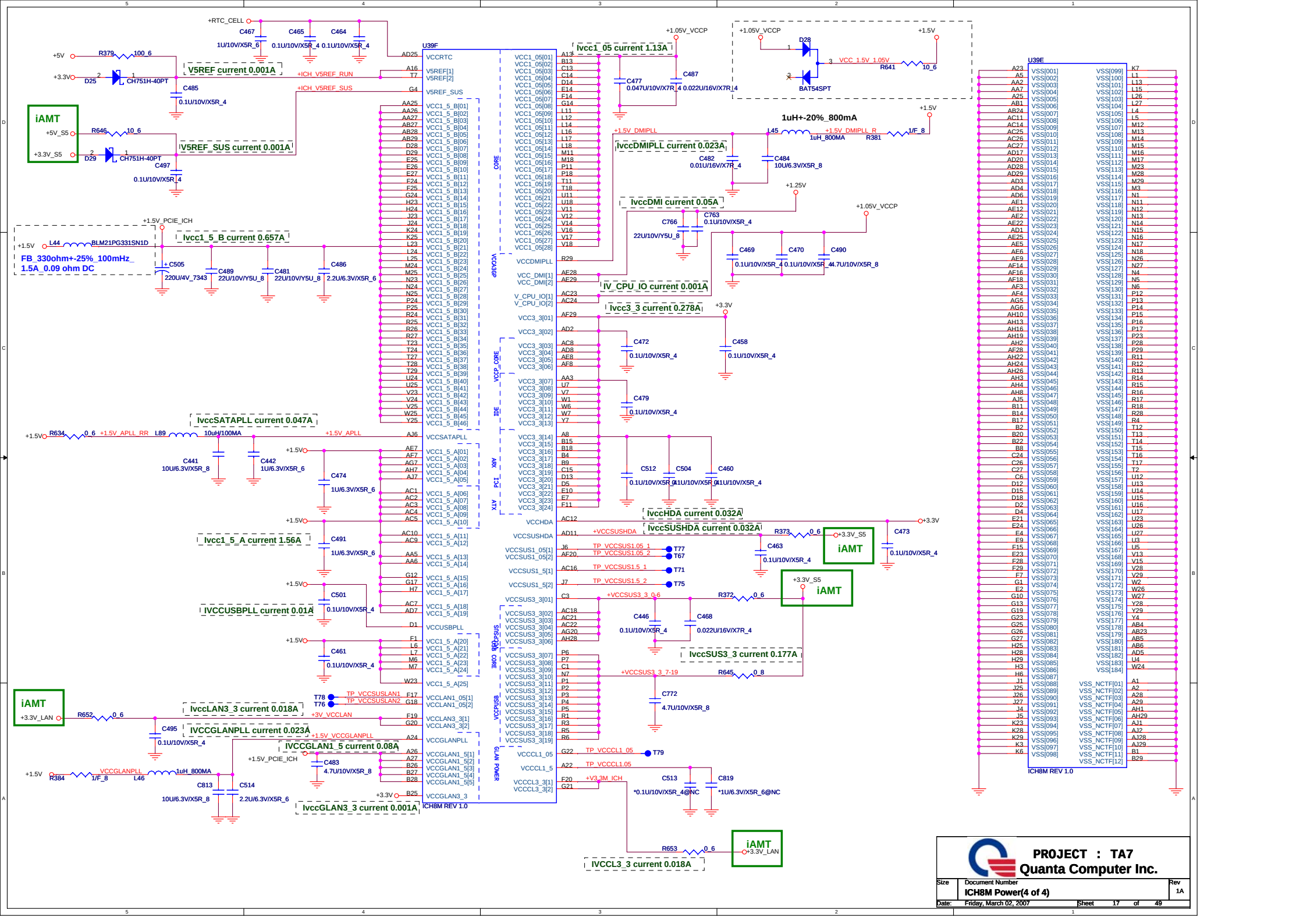
U39F
U39E
+RTC_CELL
C467
C465
C464
1U/10V/X5R_6
0.1U/10V/X5R_4
0.1U/10V/X5R_4
+5V
+3.3V
R379
100_6
D25
CH751H-40PT
V5REF current 0.001A
+ICH_V5REF_RUN
C485
0.1U/10V/X5R_4
+ICH_V5REF_SUS
iAMT
+5V_S5
+3.3V_S5
R646
10_6
D29
CH751H-40PT
V5REF_SUS current 0.001A
C497
0.1U/10V/X5R_4
+1.5V_PCIE_ICH
Ivcc1_5_B current 0.657A
+1.5V
L44
BLM21PG331SN1D
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
C505
220U/4V_7343
C489
22U/10V/Y5U_8
C481
22U/10V/Y5U_8
C486
2.2U/6.3V/X5R_6
IvccSATAPLL current 0.047A
R634
0_6
+1.5V_APLL_RR
L89
10uH/100MA
+1.5V_APLL
C441
10U/6.3V/X5R_8
C442
1U/6.3V/X5R_6
C474
1U/6.3V/X5R_6
Ivcc1_5_A current 1.56A
C491
1U/6.3V/X5R_6
IVCCUSBPLL current 0.01A
C501
0.1U/10V/X5R_4
C461
0.1U/10V/X5R_4
iAMT
+3.3V_LAN
R652
0_6
IvccLAN3_3 current 0.018A
+3V_VCCLAN
C495
0.1U/10V/X5R_4
IVCCGLANPLL current 0.023A
+1.5V_VCCGLANPLL
IVCCGLAN1_5 current 0.08A
+1.5V_PCIE_ICH
C483
4.7U/10V/X5R_8
+1.5V
R384
1/F_8
VCCGLANPLL
L46
1uH_800MA
C813
10U/6.3V/X5R_8
C514
2.2U/6.3V/X5R_6
IvccGLAN3_3 current 0.001A
T78
T76
TP_VCCSUSLAN1
TP_VCCSUSLAN2
+3.3V
ICH8M REV 1.0
Ivcc1_05 current 1.13A
+1.05V_VCCP
C477
0.047U/10V/X7R_4
C487
0.022U/16V/X7R_4
D28
BAT54SPT
+1.5V
VCC_1.5V_1.05V
R641
10_6
1uH+-20%_800mA
+1.5V_DMIPLL
IvccDMIPLL current 0.023A
L45
1uH_800MA
+1.5V_DMIPLL_R
R381
1/F_8
C482
0.01U/16V/X7R_4
C484
10U/6.3V/X5R_8
+1.25V
IvccDMI current 0.05A
C763
0.1U/10V/X5R_4
C766
22U/10V/Y5U_8
C469
0.1U/10V/X5R_4
C470
0.1U/10V/X5R_4
C490
4.7U/10V/X5R_8
IV_CPU_IO current 0.001A
Ivcc3_3 current 0.278A
C472
0.1U/10V/X5R_4
C458
0.1U/10V/X5R_4
C479
0.1U/10V/X5R_4
C512
0.1U/10V/X5R_4
C504
0.1U/10V/X5R_4
C460
0.1U/10V/X5R_4
IvccHDA current 0.032A
IvccSUSHDA current 0.032A
+VCCSUSHDA
R373
0_6
C463
0.1U/10V/X5R_4
C473
0.1U/10V/X5R_4
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
+VCCSUS3_3_0-6
R372
0_6
C446
0.1U/10V/X5R_4
C468
0.022U/16V/X7R_4
IvccSUS3_3 current 0.177A
+VCCSUS3_3_7-19
R645
0_8
C772
4.7U/10V/X5R_8
TP_VCCCL1_05
TP_VCCCL1.05
+V3.3M_ICH
C513
*0.1U/10V/X5R_4@NC
C819
*1U/6.3V/X5R_6@NC
R653
0_6
IVCCL3_3 current 0.018A
PROJECT : TA7
Quanta Computer Inc.
Size
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ICH8M Power(4 of 4)
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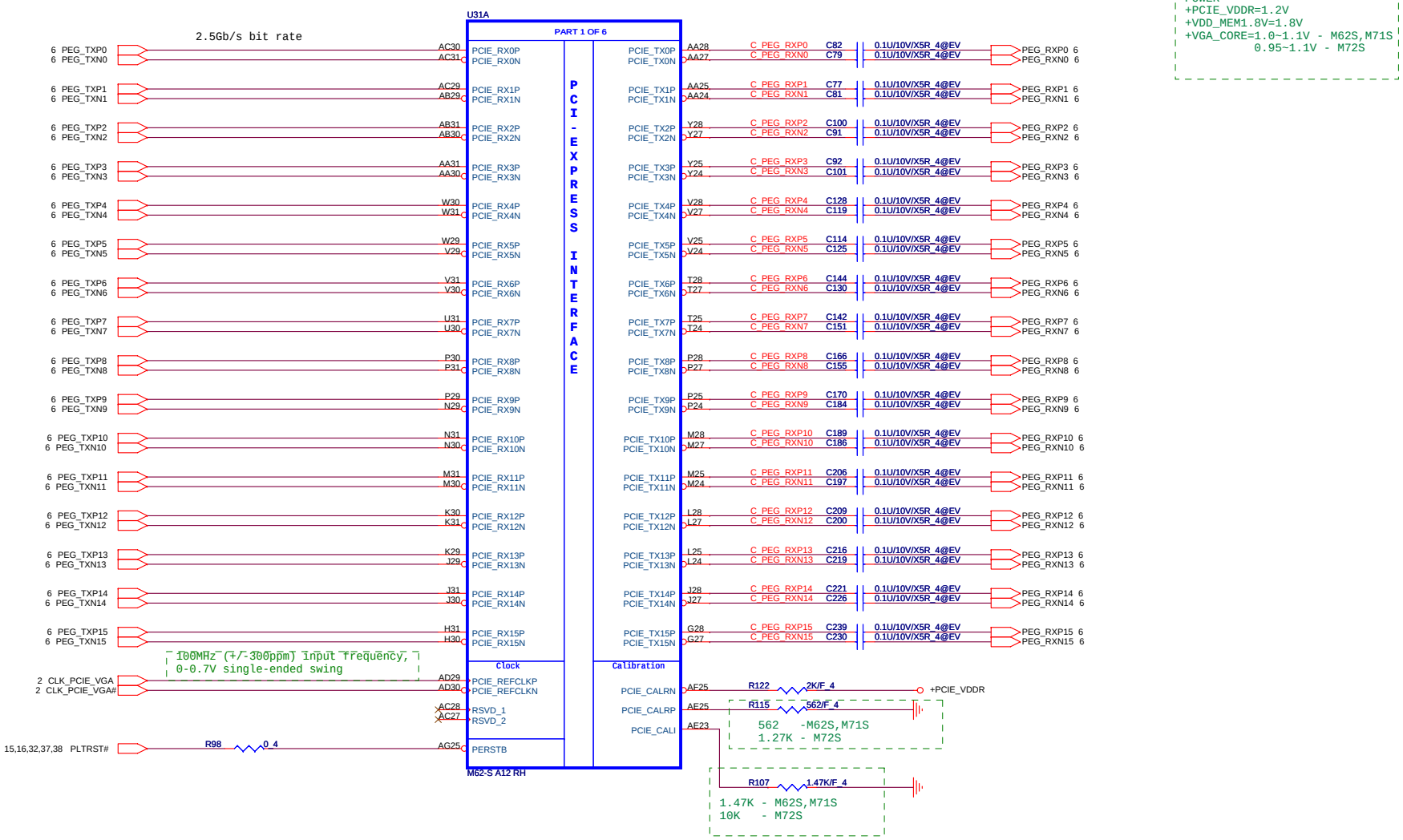

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=1.0~1.1V - M62S,M71S
0.95~1.1V - M72S

PROJECT : TA7		
Quanta Computer Inc.		
Size	Document Number: M7X/66-M_PCIE_Interface	Rev: 1A
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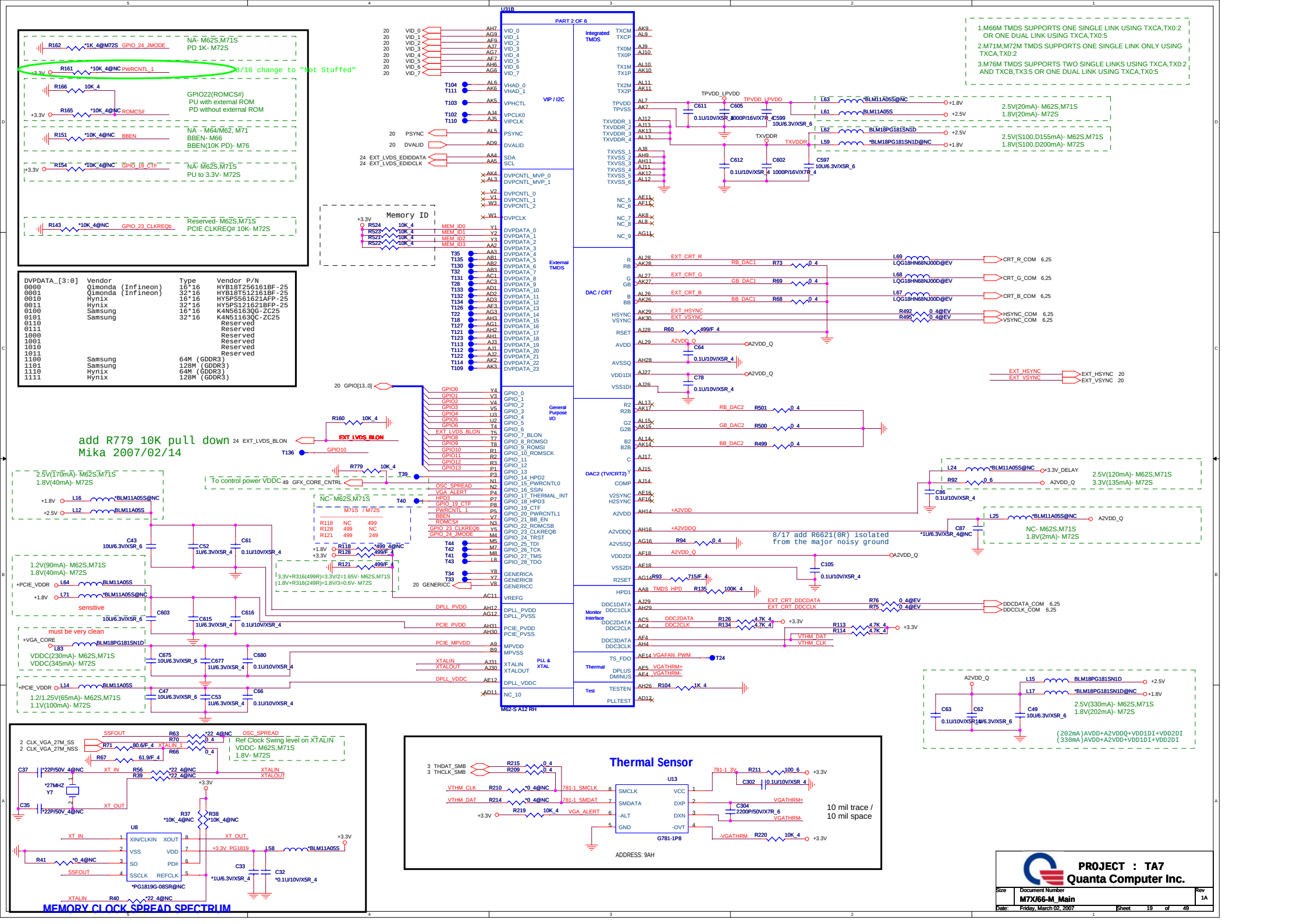
U31B
PART 2 OF 6
M62-S A12 RH
R162 *1K_4@M72S GPIO_24_JMODE
NA- M62S,M71S
PD 1K- M72S
R161 *10K_4@NC PWRCNTL_1
8/16 change to "Not Stuffed"
R166 10K_4
R165 *10K_4@NC ROMCS#
GPIO22(ROMCS#)
PU with external ROM
PD without external ROM
R151 *10K_4@NC BBEN
NA - M64/M62, M71
BBEN- M66
BBEN(10K PD)- M76
R154 *10K_4@NC GPIO_19_CTF
NA- M62S,M71S
PU to 3.3V- M72S
R143 *10K_4@NC GPIO_23_CLKREQb
Reserved- M62S,M71S
PCIE CLKREQ# 10K- M72S
Memory ID
R524 10K_4
R523 10K_4
R521 10K_4
R522 10K_4
MEM_ID0
MEM_ID1
MEM_ID2
MEM_ID3
1.M66M TMDS SUPPORTS ONE SINGLE LINK USING TXCA,TX0:2 OR ONE DUAL LINK USING TXCA,TX0:5
2.M71M,M72M TMDS SUPPORTS ONE SINGLE LINK ONLY USING TXCA,TX0:2
3.M76M TMDS SUPPORTS TWO SINGLE LINKS USING TXCA,TX0:2 AND TXCB,TX3:5 OR ONE DUAL LINK USING TXCA,TX0:5
Integrated TMDS
VIP / I2C
External TMDS
DAC / CRT
DAC2 (TV/CRT2)
General Purpose I/O
Monitor Interface
Thermal
Test
PLL & XTAL
TPVDD_LPVDD
TXVDDR
L63 *BLM11A05S@NC
L61 BLM11A05S
L62 BLM18PG181SN1D
L59 *BLM18PG181SN1D@NC
2.5V(20mA)- M62S,M71S
1.8V(20mA)- M72S
2.5V(S100,D155mA)- M62S,M71S
1.8V(S100,D200mA)- M72S
EXT_CRT_R
EXT_CRT_G
EXT_CRT_B
EXT_HSYNC
EXT_VSYNC
CRT_R_COM 6,25
CRT_G_COM 6,25
CRT_B_COM 6,25
HSYNC_COM 6,25
VSYNC_COM 6,25
A2VDD_Q
+A2VDD
+A2VDDQ
DDCDATA_COM 6,25
DDCCLK_COM 6,25
DDC2DATA
DDC2CLK
VTHM_DAT
VTHM_CLK
VGAFAN_PWM
T24
TMDS_HPD
EXT_CRT_DDCDATA
EXT_CRT_DDCCLK
DVPDATA_[3:0] Vendor Type Vendor P/N
0000 Qimonda (Infineon) 16*16 HYB18T256161BF-25
0001 Qimonda (Infineon) 32*16 HYB18T512161BF-25
0010 Hynix 16*16 HY5PS561621AFP-25
0011 Hynix 32*16 HY5PS121621BFP-25
0100 Samsung 16*16 K4N561630G-ZC25
0101 Samsung 32*16 K4N51163QC-ZC25
0110 Reserved
0111 Reserved
1000 Reserved
1001 Reserved
1010 Reserved
1011 Reserved
1100 Samsung 64M (GDDR3)
1101 Samsung 128M (GDDR3)
1110 Hynix 64M (GDDR3)
1111 Hynix 128M (GDDR3)
add R779 10K pull down
Mika 2007/02/14
R160 10K_4
EXT_LVDS_BLON
T136 GPIO10
R779 10K_4
T39
To control power VDDC
49 GFX_CORE_CNTRL
NC- M62S,M71S
M71S /M72S
R118 NC 499
R128 499 NC
R121 499 249
R119 *499_4@NC
R128 499/F_4
R121 499/F_4
3.3V+R316(499R)=3.3V/2=1.65V- M62S,M71S
1.8V+R316(249R)=1.8V/3=0.6V- M72S
8/17 add R6621(0R) isolated from the major noisy ground
2.5V(170mA)- M62S,M71S
1.8V(40mA)- M72S
L16 *BLM11A05S@NC
L12 BLM11A05S
1.2V(90mA)- M62S,M71S
1.8V(40mA)- M72S
L64 BLM11A05S
L71 *BLM11A05S@NC
sensitive
must be very clean
L83 BLM18PG181SN1D
VDDC(230mA)- M62S,M71S
VDDC(345mA)- M72S
L14 BLM11A05S
1.2/1.25V(65mA)- M62S,M71S
1.1V(100mA)- M72S
L24 *BLM11A05S@NC
R92 0_6
2.5V(120mA)- M62S,M71S
3.3V(135mA)- M72S
L25 *BLM11A05S@NC
NC- M62S,M71S
1.8V(2mA)- M72S
L15 BLM18PG181SN1D
L17 *BLM18PG181SN1D@NC
2.5V(330mA)- M62S,M71S
1.8V(202mA)- M72S
(202mA)AVDD+A2VDDQ+VDD1DI+VDD2DI
(330mA)AVDD+A2VDD+VDD1DI+VDD2DI
Ref Clock Swing level on XTALIN
VDDC- M62S,M71S
1.8V- M72S
*27MHZ
Y7
U8
XIN/CLKIN XOUT
VSS VDD
SO PD#
SSCLK REFCLK
*PG1819G-08SR@NC
+3.3V_PG1819
MEMORY CLOCK SPREAD SPECTRUM
Thermal Sensor
U13
SMCLK VCC
SMDATA DXP
-ALT DXN
GND -OVT
G781-1P8
781-1_SMCLK
781-1_SMDAT
VGA_ALERT
VGATHRM+
VGATHRM-
ADDRESS: 9AH
10 mil trace /
10 mil space
PROJECT : TA7
Quanta Computer Inc.
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M7X/66-M_Main
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1A
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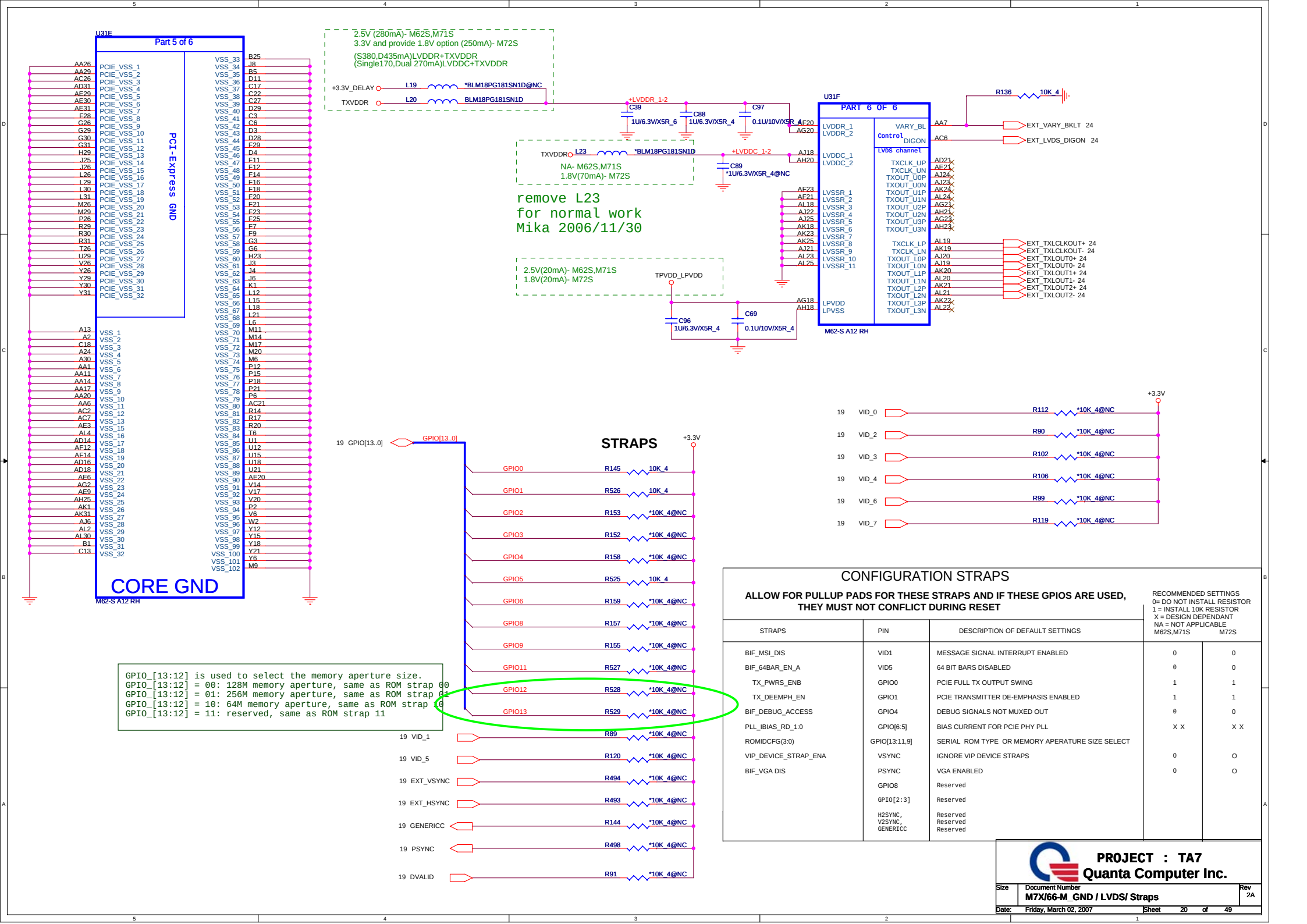

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S,M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	0	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	0	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0	0
PLL_IBIAS_RD_1:0	GPIO[6:5]	BIAS CURRENT FOR PCIE PHY PLL	X X	X X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERATURE SIZE SELECT		
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
	GPIO8	Reserved		
	GPIO[2:3]	Reserved		
	H2SYNC, V2SYNC, GENERICC	Reserved Reserved Reserved		

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Quanta Computer Inc.

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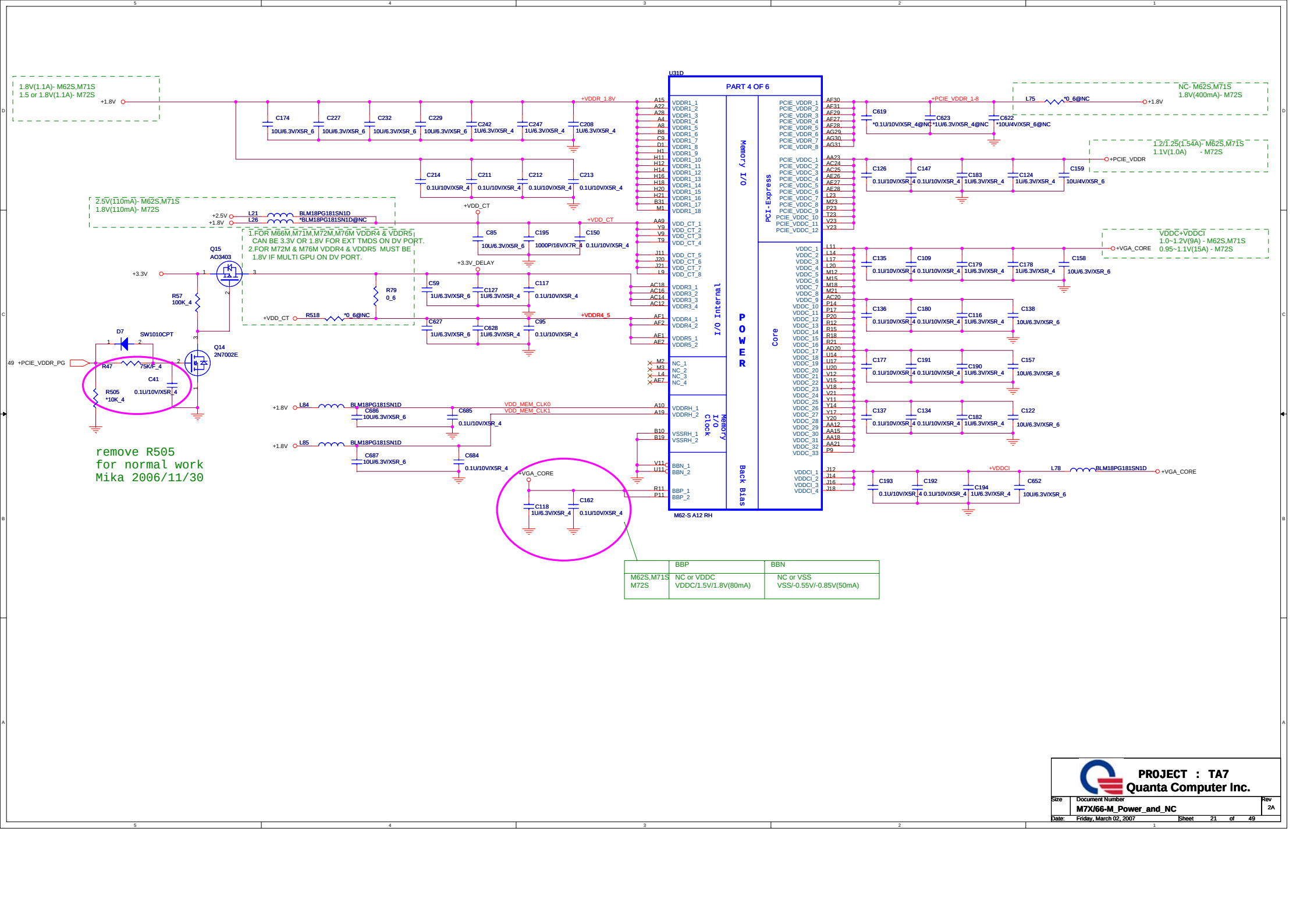
1.8V(1.1A)- M62S,M71S
1.5 or 1.8V(1.1A)- M72S
+1.8V
+VDDR_1.8V
C174 10U/6.3V/X5R_6
C227 10U/6.3V/X5R_6
C232 10U/6.3V/X5R_6
C229 10U/6.3V/X5R_6
C242 1U/6.3V/X5R_4
C247 1U/6.3V/X5R_4
C208 1U/6.3V/X5R_4
C214 0.1U/10V/X5R_4
C211 0.1U/10V/X5R_4
C212 0.1U/10V/X5R_4
C213 0.1U/10V/X5R_4
U31D
PART 4 OF 6
Memory I/O
PCI-Express
I/O Internal
POWER
Core
Memory Clock I/O
Back Bias
M62-S A12 RH
NC- M62S,M71S
1.8V(400mA)- M72S
L75 *0_6@NC
+PCIE_VDDR_1-8
C619 *0.1U/10V/X5R_4@NC
C623 *1U/6.3V/X5R_4@NC
C622 *10U/4V/X5R_6@NC
1.2/1.25(1.54A)- M62S,M71S
1.1V(1.0A) - M72S
+PCIE_VDDR
C126 0.1U/10V/X5R_4
C147 0.1U/10V/X5R_4
C183 1U/6.3V/X5R_4
C124 1U/6.3V/X5R_4
C159 10U/4V/X5R_6
2.5V(110mA)- M62S,M71S
1.8V(110mA)- M72S
+2.5V
+1.8V
L21 BLM18PG181SN1D
L26 *BLM18PG181SN1D@NC
+VDD_CT
C85 10U/6.3V/X5R_6
C195 1000P/16V/X7R_4
C150 0.1U/10V/X5R_4
1.FOR M66M,M71M,M72M,M76M VDDR4 & VDDR5
CAN BE 3.3V OR 1.8V FOR EXT TMDS ON DV PORT.
2.FOR M72M & M76M VDDR4 & VDDR5 MUST BE
1.8V IF MULTI GPU ON DV PORT.
Q15
AO3403
+3.3V
R57 100K_4
R79 0_6
+3.3V_DELAY
C59 1U/6.3V/X5R_6
C127 1U/6.3V/X5R_4
C117 0.1U/10V/X5R_4
+VDD_CT
R518 *0_6@NC
C627 1U/6.3V/X5R_6
C628 1U/6.3V/X5R_4
C95 0.1U/10V/X5R_4
+VDDR4_5
D7
SW1010CPT
Q14
2N7002E
49 +PCIE_VDDR_PG
R47 75K/F_4
C41 0.1U/10V/X5R_4
R505 *10K_4
remove R505
for normal work
Mika 2006/11/30
L84 BLM18PG181SN1D
C686 10U/6.3V/X5R_6
C685 0.1U/10V/X5R_4
VDD_MEM_CLK0
VDD_MEM_CLK1
L85 BLM18PG181SN1D
C687 10U/6.3V/X5R_6
C684 0.1U/10V/X5R_4
+VGA_CORE
C118 1U/6.3V/X5R_4
C162 0.1U/10V/X5R_4
VDDC+VDDCI
1.0~1.2V(9A) - M62S,M71S
0.95~1.1V(15A) - M72S
+VGA_CORE
C135 0.1U/10V/X5R_4
C109 0.1U/10V/X5R_4
C179 1U/6.3V/X5R_4
C178 1U/6.3V/X5R_4
C158 10U/6.3V/X5R_6
C136 0.1U/10V/X5R_4
C180 0.1U/10V/X5R_4
C116 1U/6.3V/X5R_4
C138 10U/6.3V/X5R_6
C177 0.1U/10V/X5R_4
C191 0.1U/10V/X5R_4
C190 1U/6.3V/X5R_4
C157 10U/6.3V/X5R_6
C137 0.1U/10V/X5R_4
C134 0.1U/10V/X5R_4
C182 1U/6.3V/X5R_4
C122 10U/6.3V/X5R_6
+VDDCI
L78 BLM18PG181SN1D
C193 0.1U/10V/X5R_4
C192 0.1U/10V/X5R_4
C194 1U/6.3V/X5R_4
C652 10U/6.3V/X5R_6
BBP
BBN
M62S,M71S
M72S
NC or VDDC
VDDC/1.5V/1.8V(80mA)
NC or VSS
VSS/-0.55V/-0.85V(50mA)
PROJECT : TA7
Quanta Computer Inc.
Size
Document Number
M7X/66-M_Power_and_NC
Rev
2A
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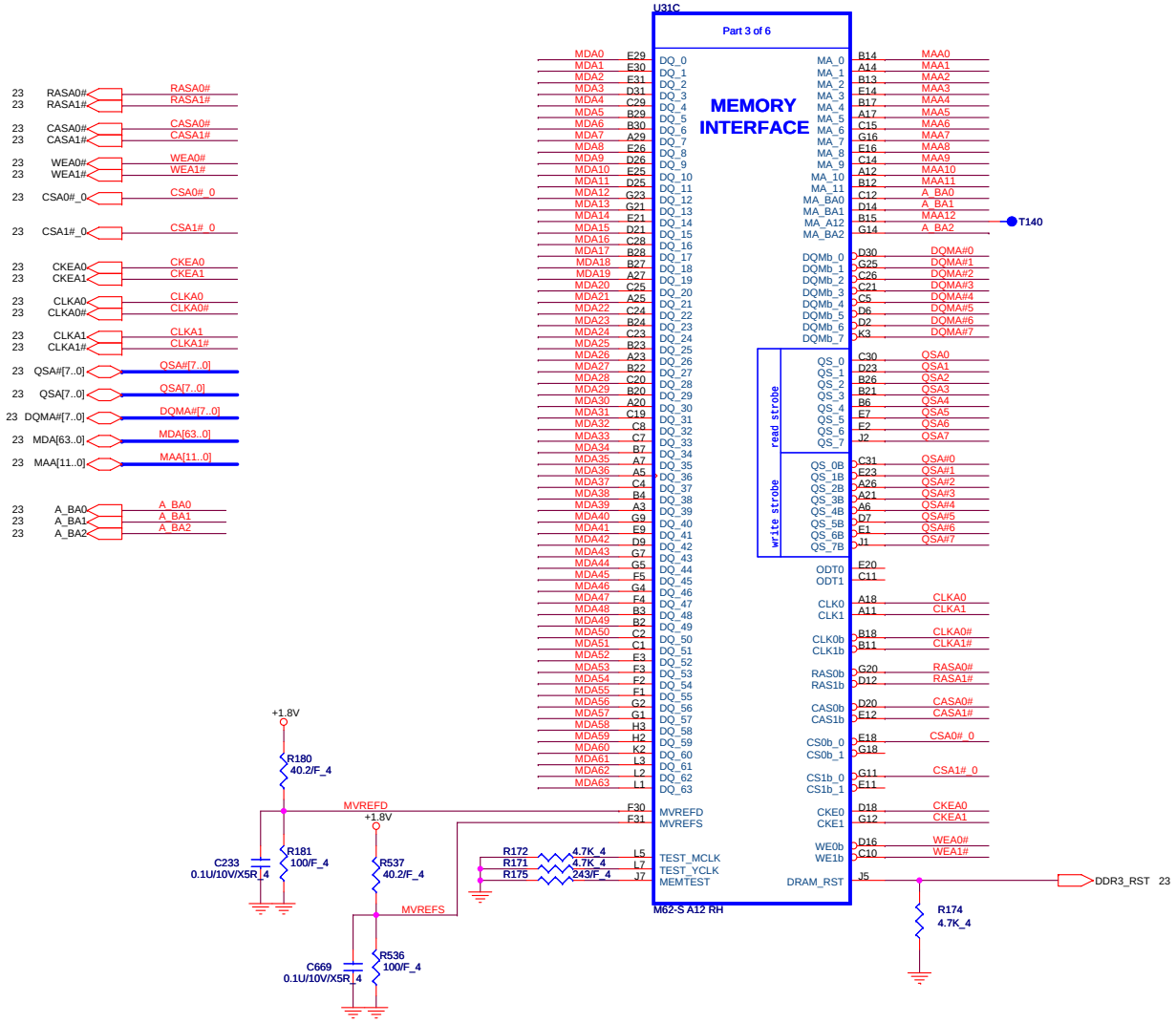

PROJECT : TA7

Quanta Computer Inc.

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	M7X/66-M MEM_Interface	1A

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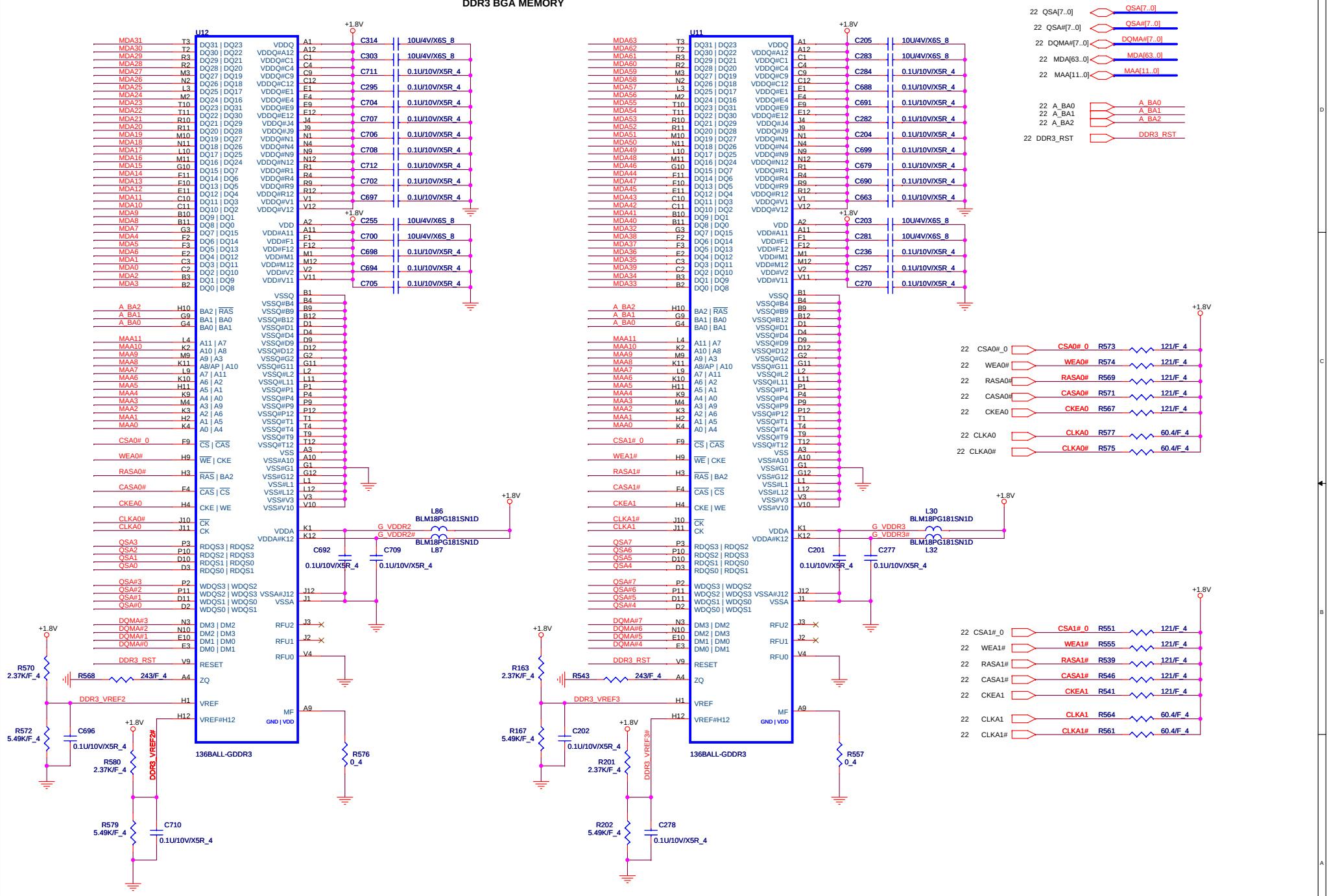
DDR3 BGA MEMORY



PROJECT : TA7			
Quanta Computer Inc.			
Size	Document Number		Rev
	MEM_A0		1A
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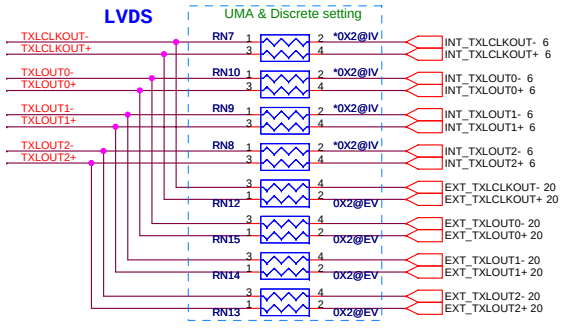
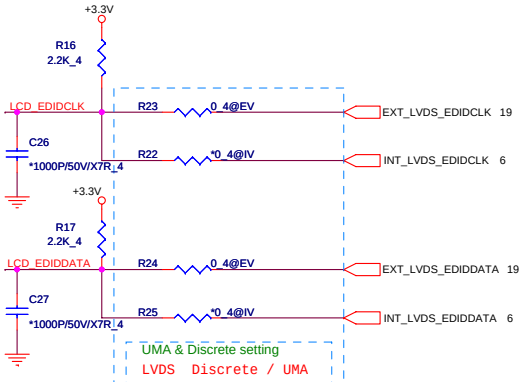


External VGA with @EV part,
Internal VGA with @IV part.

UMA & Discrete setting

LVDS Discrete / UMA

RN7	NC	0
RN10	NC	0
RN9	NC	0
RN8	NC	0
RN12	0	NC
RN15	0	NC
RN14	0	NC
RN13	0	NC

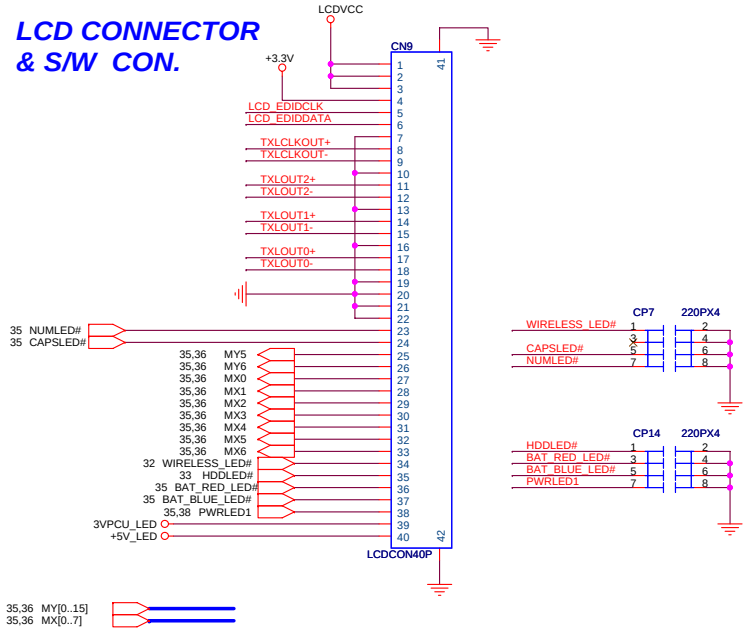


UMA & Discrete setting

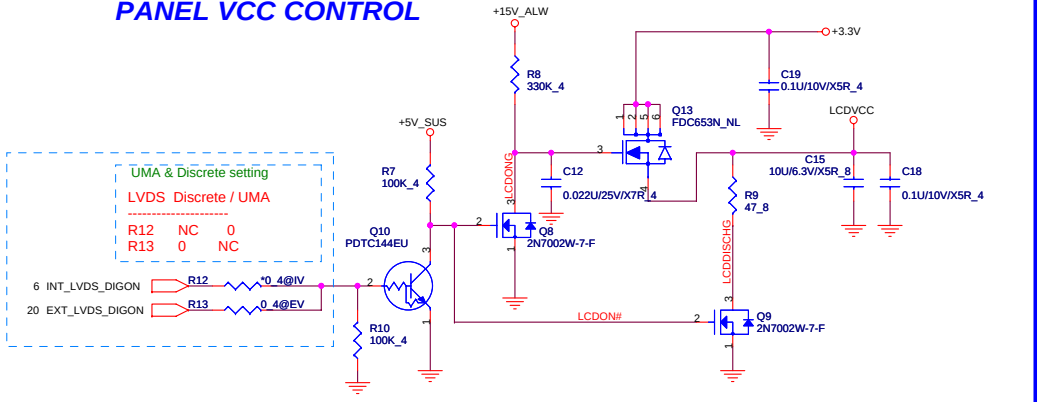
LVDS Discrete / UMA

R23	0	NC
R22	NC	0
R24	0	NC
R25	NC	0

LCD CONNECTOR & S/W CON.



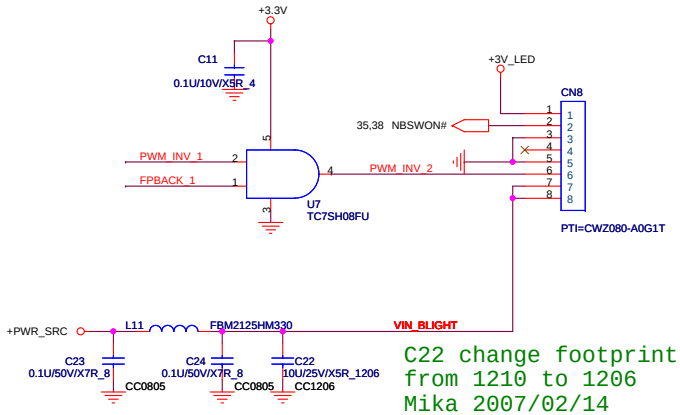
PANEL VCC CONTROL



UMA & Discrete setting

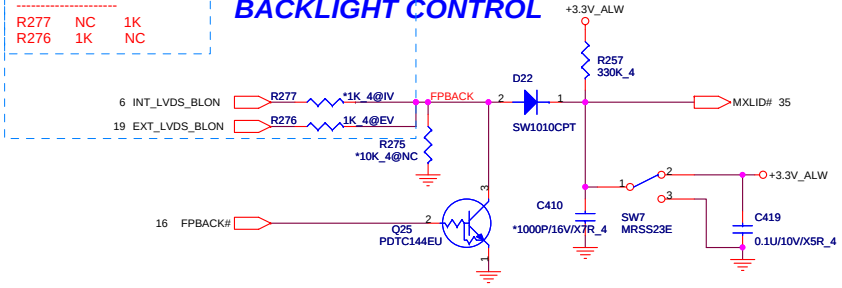
LVDS Discrete / UMA

R12	NC	0
R13	0	NC



C22 change footprint
from 1210 to 1206
Mika 2007/02/14

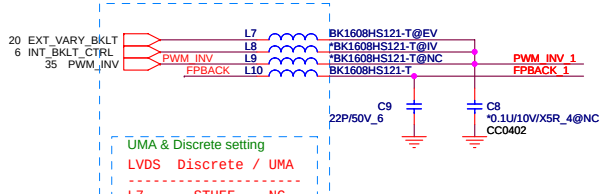
BACKLIGHT CONTROL



UMA & Discrete setting

LVDS Discrete / UMA

R277	NC	1K
R276	1K	NC



UMA & Discrete setting

LVDS Discrete / UMA

L7	STUFF	NC
L8	NC	STUFF

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/HDMI	1A

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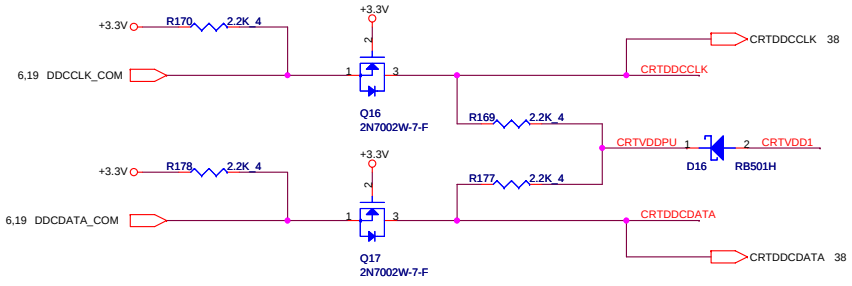
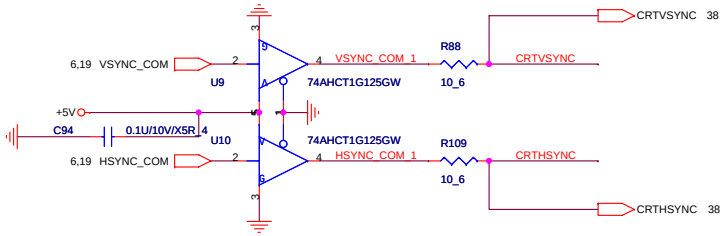
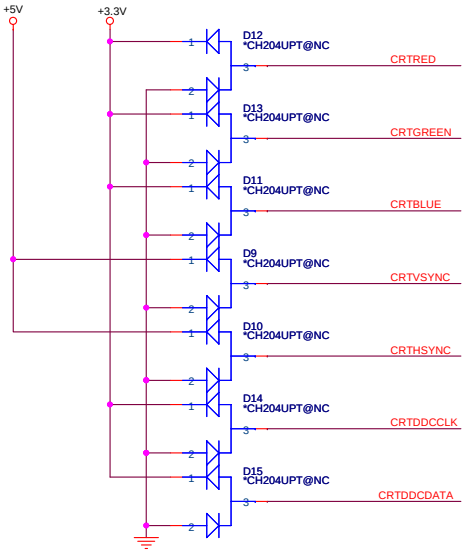
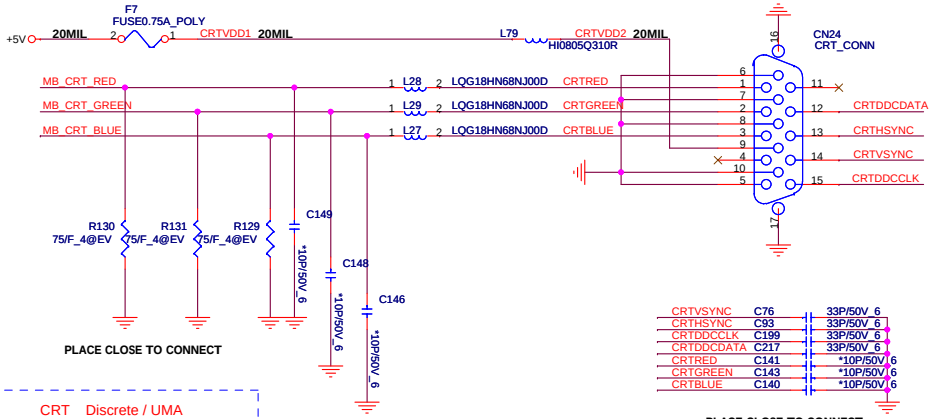




PLACE CLOSE TO CONNECT



CRT PORT

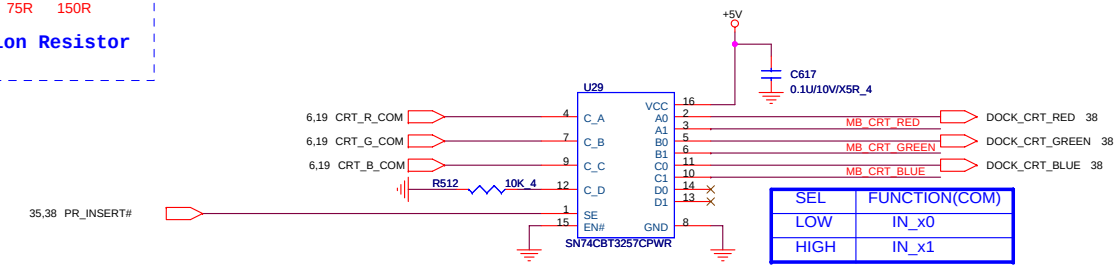


PLACE CLOSE TO CONNECT

PLACE CLOSE TO CONNECT

CRT	Discrete / UMA
R130	75R 150R
R131	75R 150R
R129	75R 150R

Termination Resistor



SEL	FUNCTION(COM)
LOW	IN_x0
HIGH	IN_x1

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	CRT	1A

Date: Friday, March 02, 2007 Sheet 25 of 49

LAN

JKCLK Pin	
Power down	0MHz
10Mbps	5MHz
100Mbps	50MHz
1000Mbps	62.5MHz

Layout Note:
Place series resistor close to LAN controller.

Link Speed	LCI	GLCI
1000Mbps	Runing	Runing
100Mbps	Runing	Idle
10Mbps	Runing	Idle
No Link	Runing or power down	Idle
Power down	Power down	Power down

add R781 30 ohm
for Intel suggestion
Mika 2007/02/14

Layout Note:
Place the resistors less than 1" from LAN controller.

Layout Note:
Connect the resistor
to GND near ball E6

Test Mode Enable
Strap low for normal operation
82566 100~200 pull down for normal operation
82562 200 pull down for normal operaiton

82562V and 82566MM
R245,R254 NC

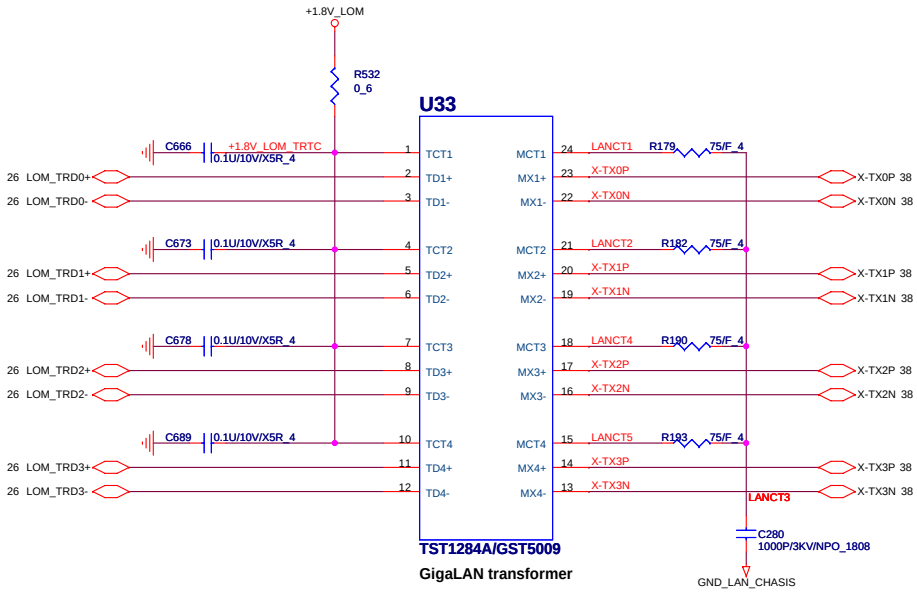
82566MM
1. R232~R235 , R237~R240 --- 49.9/F (CS04992FB31).
2. C330~C333 --- 0.1U.

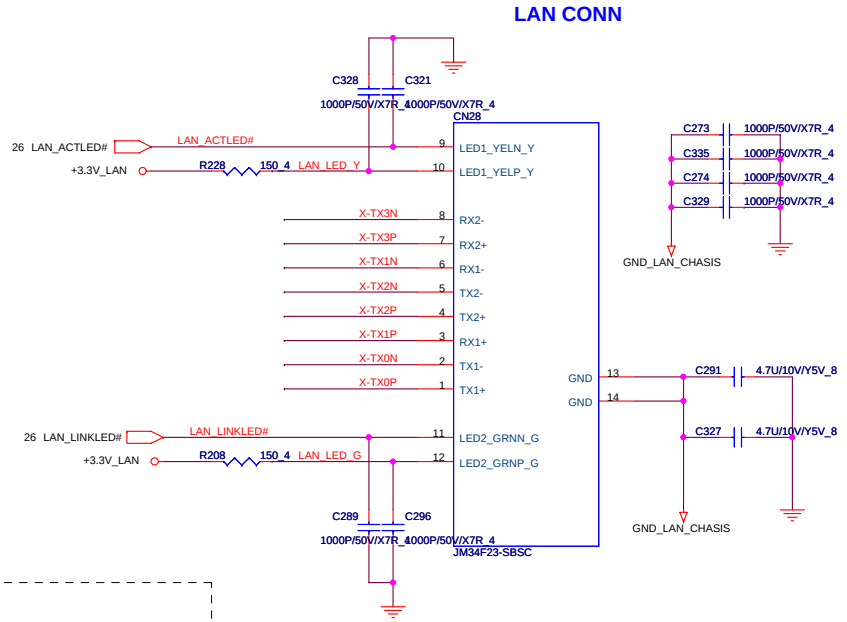
need FAE support
82562 question
(mode select)

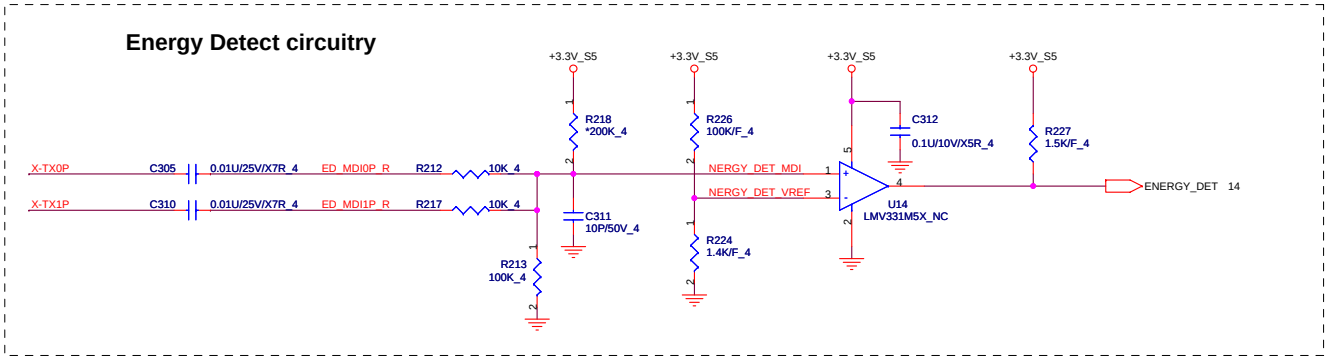
Place termination resistors and caps as close to LAN controller as possible

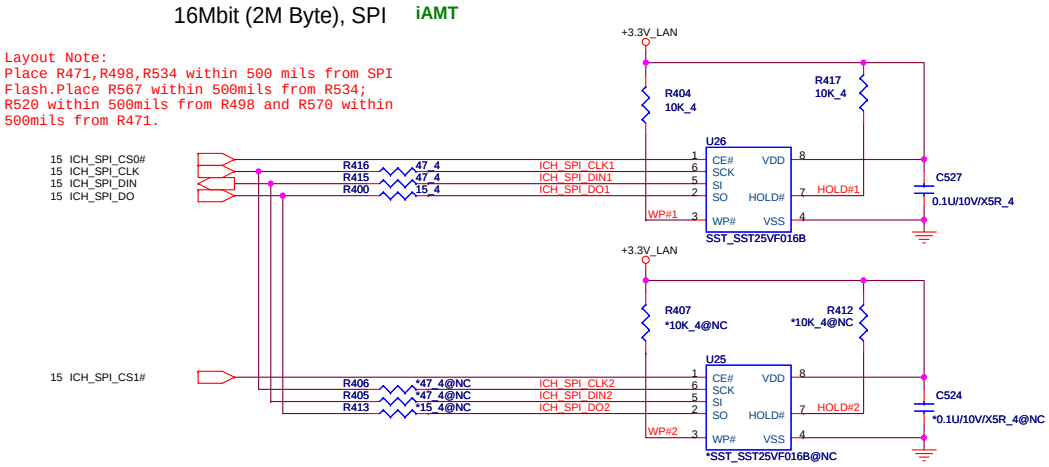
PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	LAN-NINEVEH-EKRON_N	1A
Date: Friday, March 02, 2007	Sheet 26 of 49	









PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45	1A
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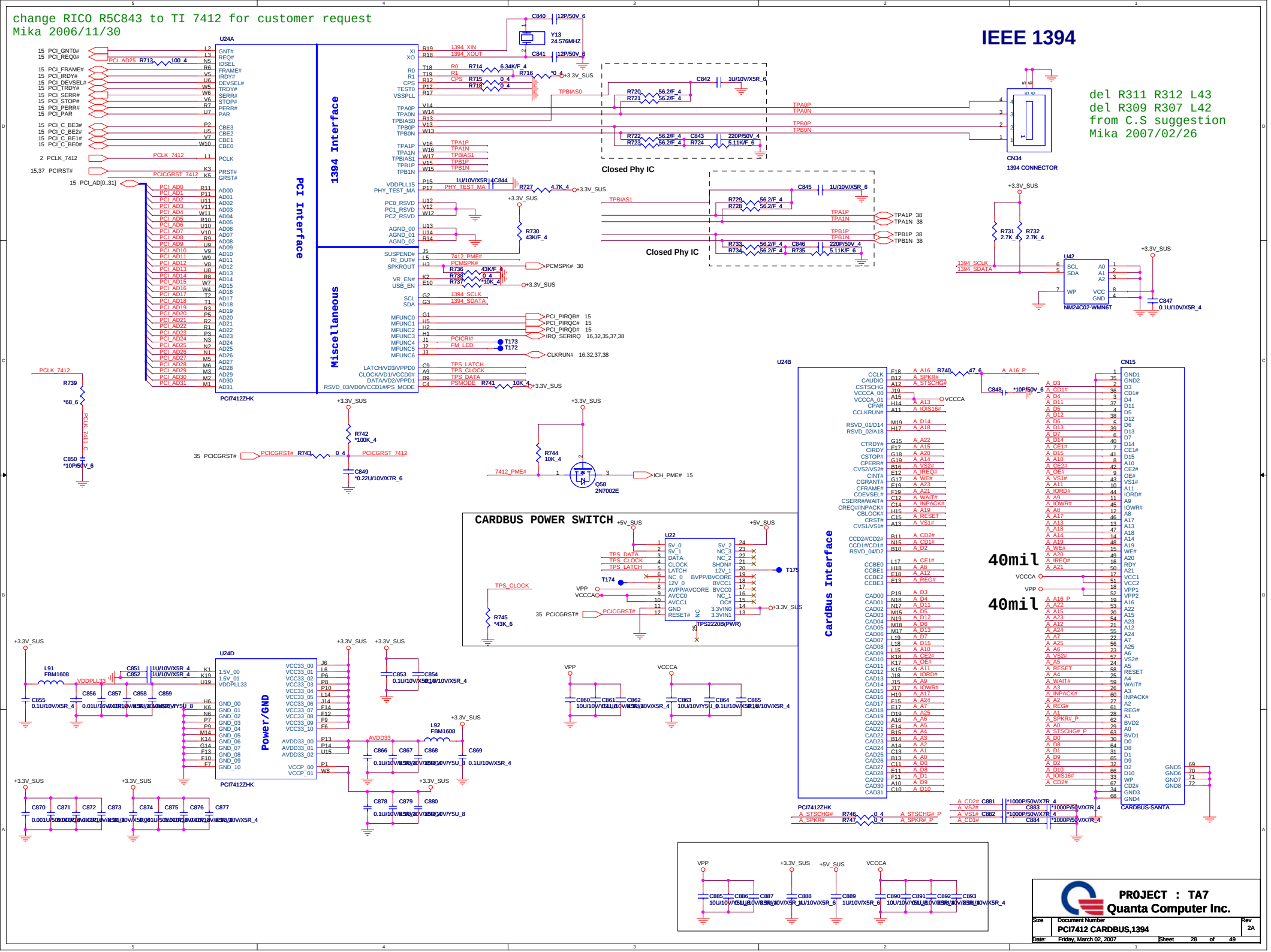
change RICO R5C843 to TI 7412 for customer request
Mika 2006/11/30

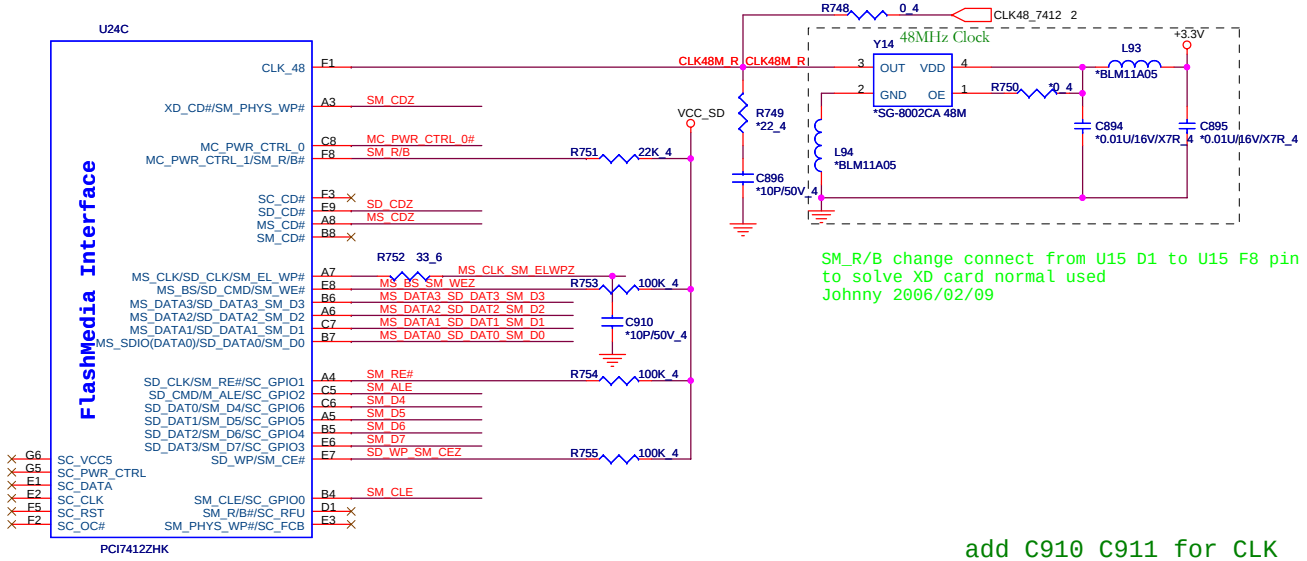
IEEE 1394

del R311 R312 L43
del R309 R307 L42
from C.S suggestion
Mika 2007/02/26

U24A
PCI Interface
1394 Interface
Miscellaneous
PCI7412ZHK
Closed Phy IC
Closed Phy IC
CN34
1394 CONNECTOR
U42
NM24C02-WMN6T
U24B
CardBus Interface
CN15
CARDBUS-SANTA
CARDBUS POWER SWITCH
U22
TPS2220B(PWR)
U24D
Power/GND
PCI7412ZHK
40mil
40mil



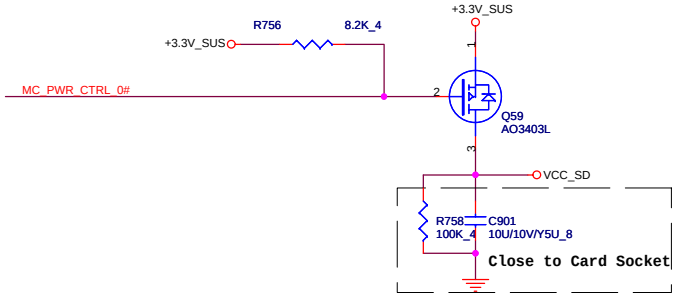
change RICO R5C843 to TI 7412 for customer request
Mika 2006/11/30

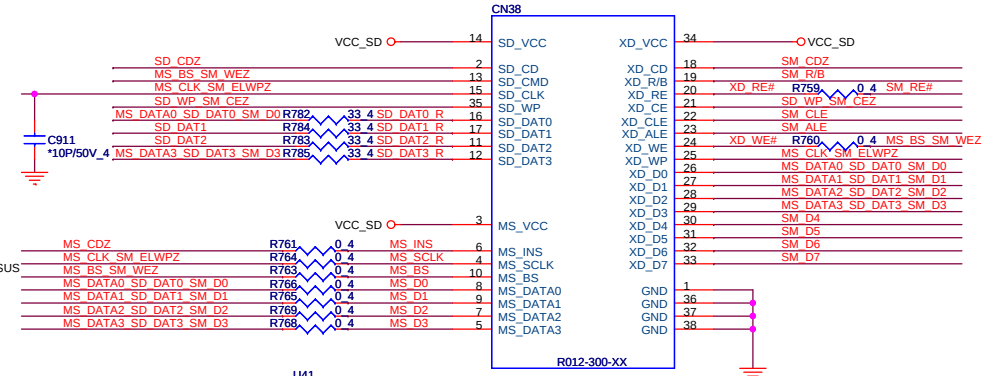


SM_R/B change connect from U15 D1 to U15 F8 pin
to solve XD card normal used
Johnny 2006/02/09

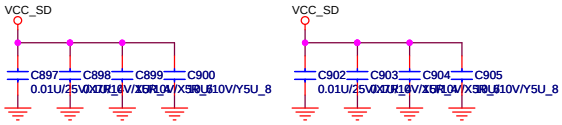
add C910 C911 for CLK
add R782 R783 R784 R785 for DATA
that suggestion is from EMI
Mika 2007/02/14

4 IN1 CARD READER





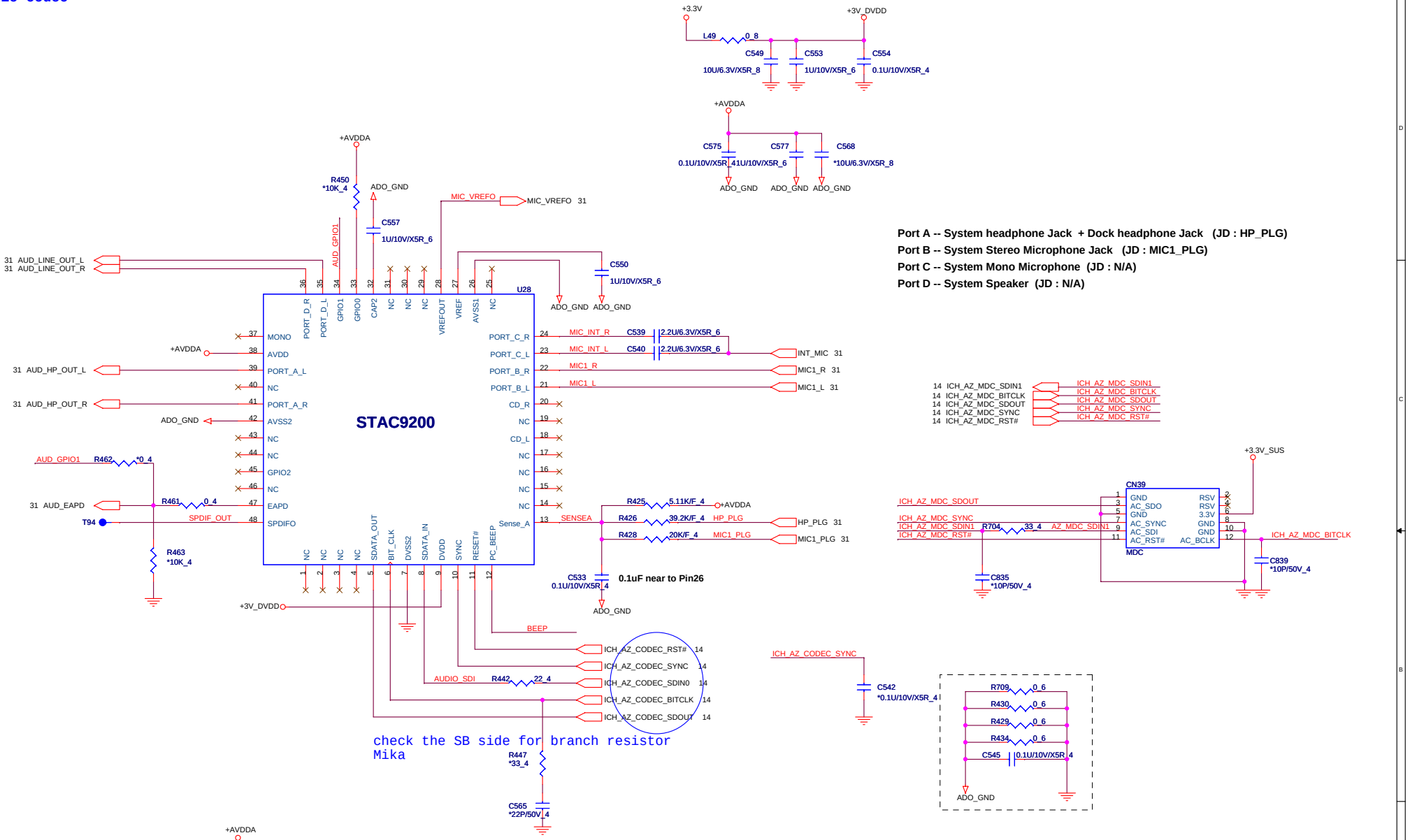
Supporting MMC/SD/MS/XD Cards



PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412_CARD READER	2A
Date: Friday, March 02, 2007	Sheet 29 of 49	

Audio codec



Port A -- System headphone Jack + Dock headphone Jack (JD : HP_PLG)
Port B -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port C -- System Mono Microphone (JD : N/A)
Port D -- System Speaker (JD : N/A)

PROJECT : TA7		
Quanta Computer Inc.		
Size	Document Number	Rev
	ALC268 CONN	1A
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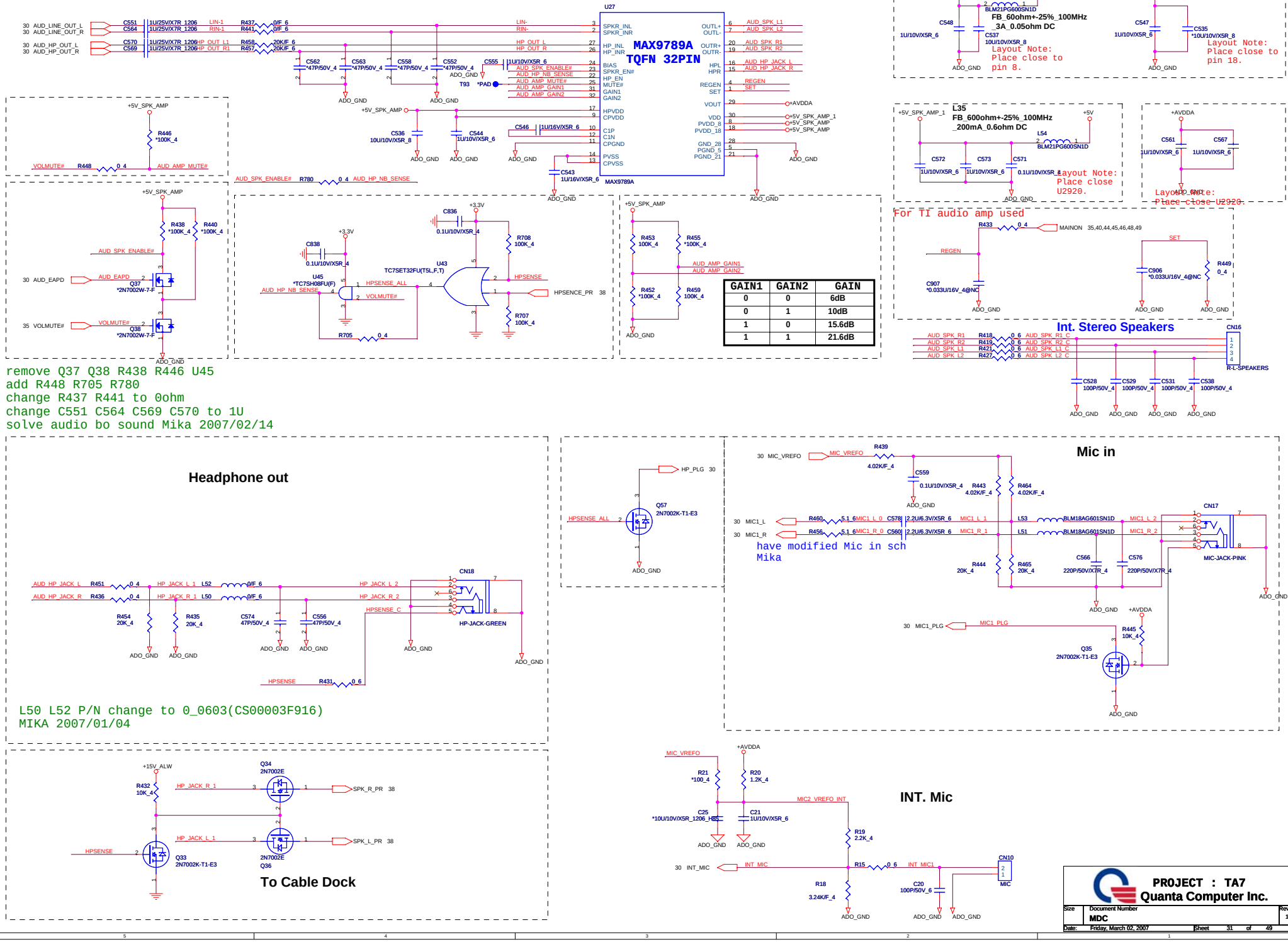
AUDIO AMPLIFIER



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

remove Q37 Q38 R438 R446 U45
add R448 R705 R780
change R437 R441 to 0ohm
change C551 C564 C569 C570 to 1U
solve audio bo sound Mika 2007/02/14

Headphone out

L50 L52 P/N change to 0_0603(CS00003F916)
MIKA 2007/01/04

To Cable Dock

Mic in

INT. Mic

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Quanta Computer Inc.		
Size	Document Number: MDC	Rev: 1A
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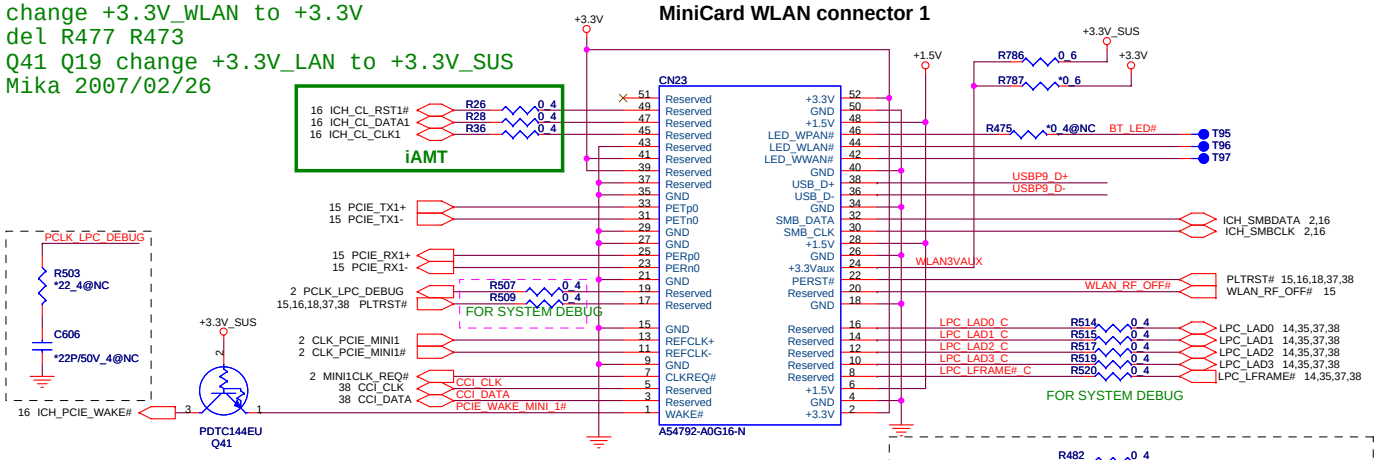
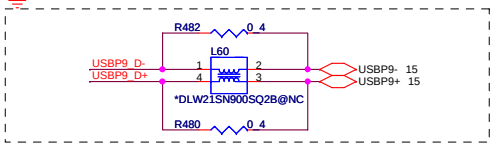
change +3.3V_WLAN to +3.3V
del R477 R473
Q41 Q19 change +3.3V_LAN to +3.3V_SUS
Mika 2007/02/26

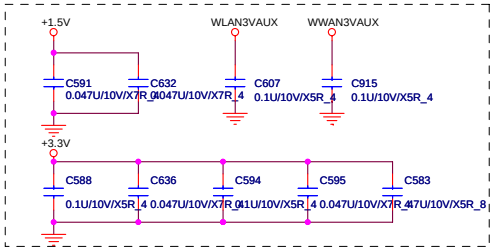
MiniCard WLAN connector 1

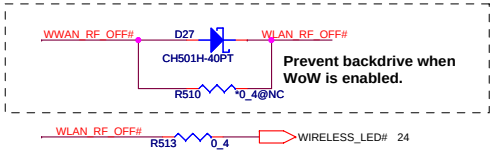




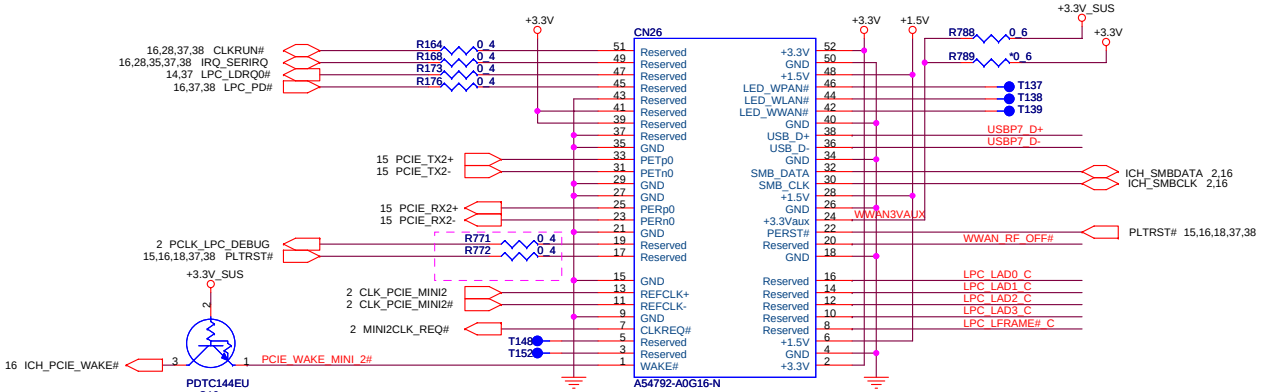
del R491 R486 Q39 Q40
and directly connect both signal
Mika 2007/02/26

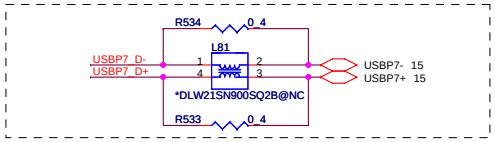
add R786 R787 for select power
Mika 2007/02/26





MiniCard WWAN connector 2

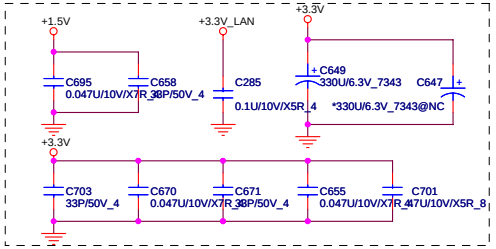




add R771 R772
for Debug card used
Mika 2006/11/30

del R542 R538 Q42 Q43
and directly connect both signal
Mika 2007/02/26

add R788 R789 for select power
add C915 for WWAN3VAUX
Mika 2007/02/26



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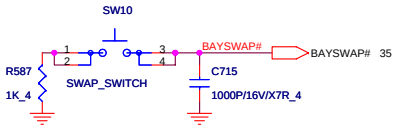
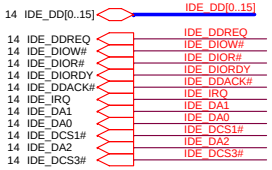
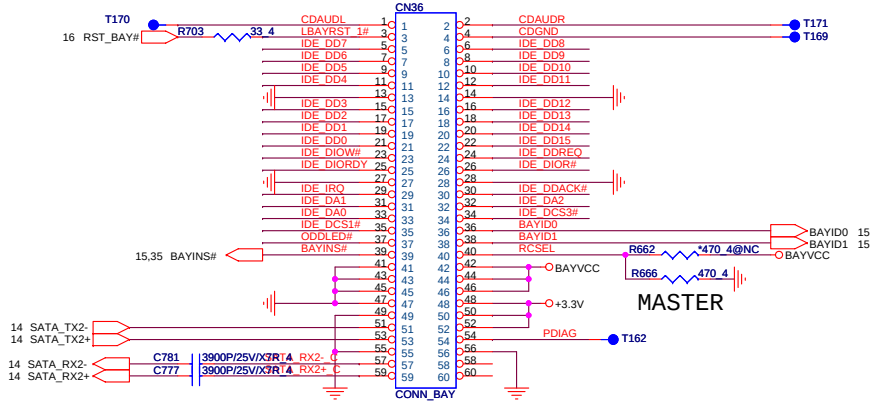
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E Card	2A
Date: Friday, March 02, 2007	Sheet 32 of 49	



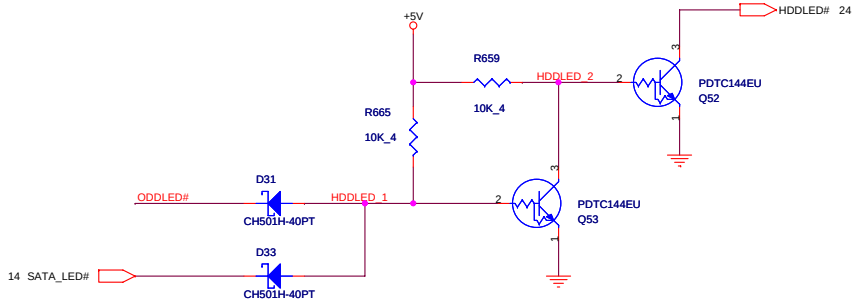


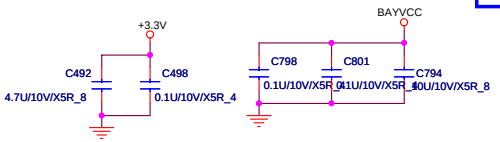


MASTER

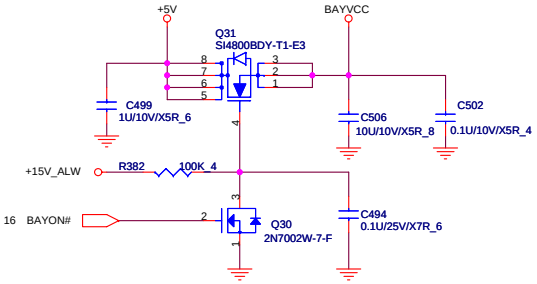
LBAY ID STATUS

LEFT BAYID1	LEFT BAYID0	STATUS
0	0	Reserve
0	1	ODD
1	0	Reserve
1	1	Reserve





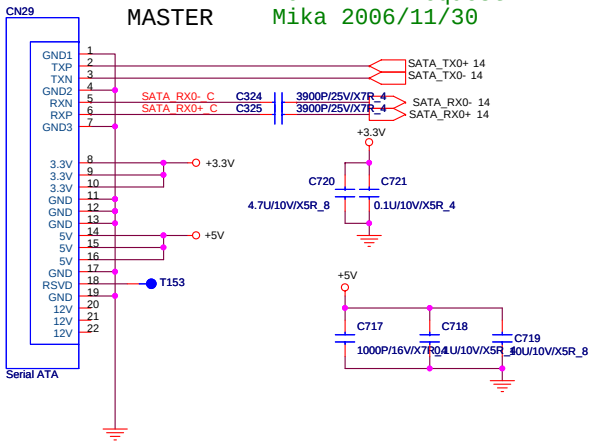
BAY POWER CONTROL



SATA CONNECTOR

change SATA connector
for M1 ME request
Mika 2006/11/30

MASTER



PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	SATA HDD,ODD,USB	2A

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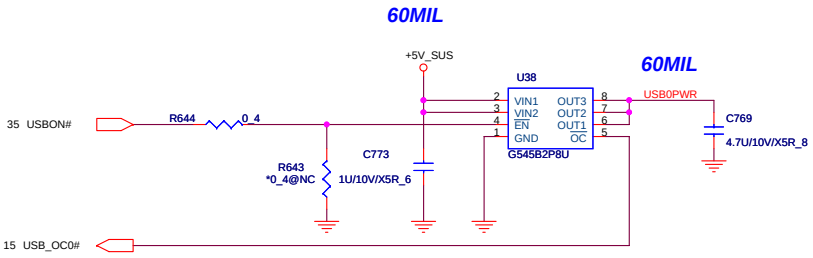
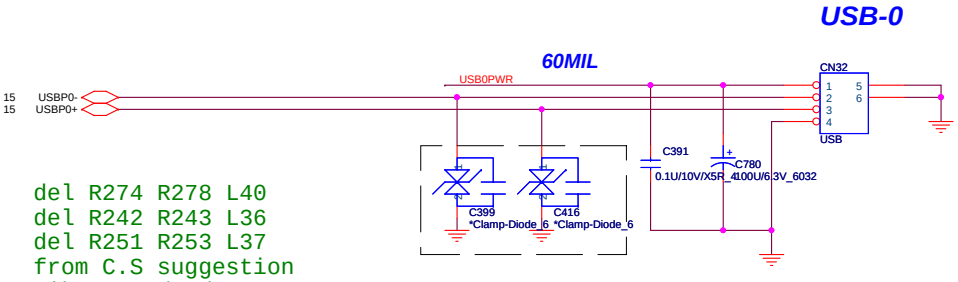
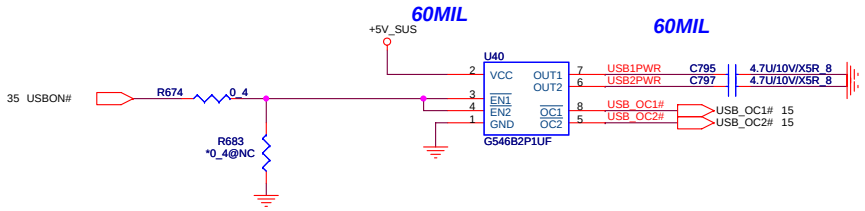
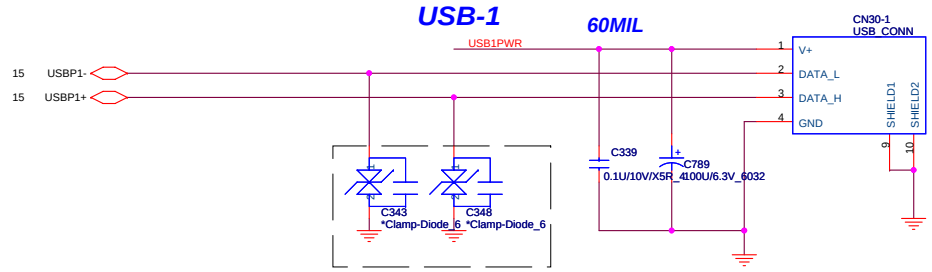
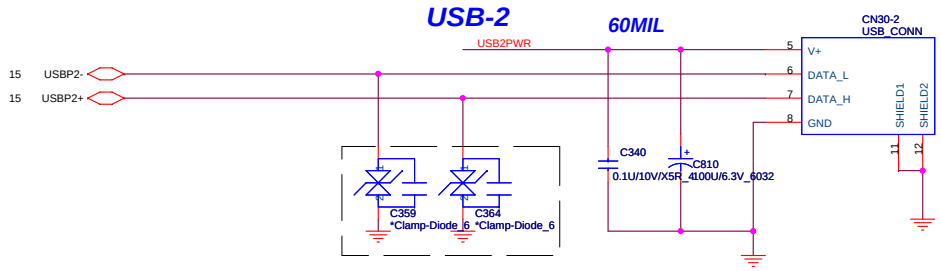




del R274 R278 L40
del R242 R243 L36
del R251 R253 L37
from C.S suggestion
Mika 2007/02/26







PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	USB CONN	1A
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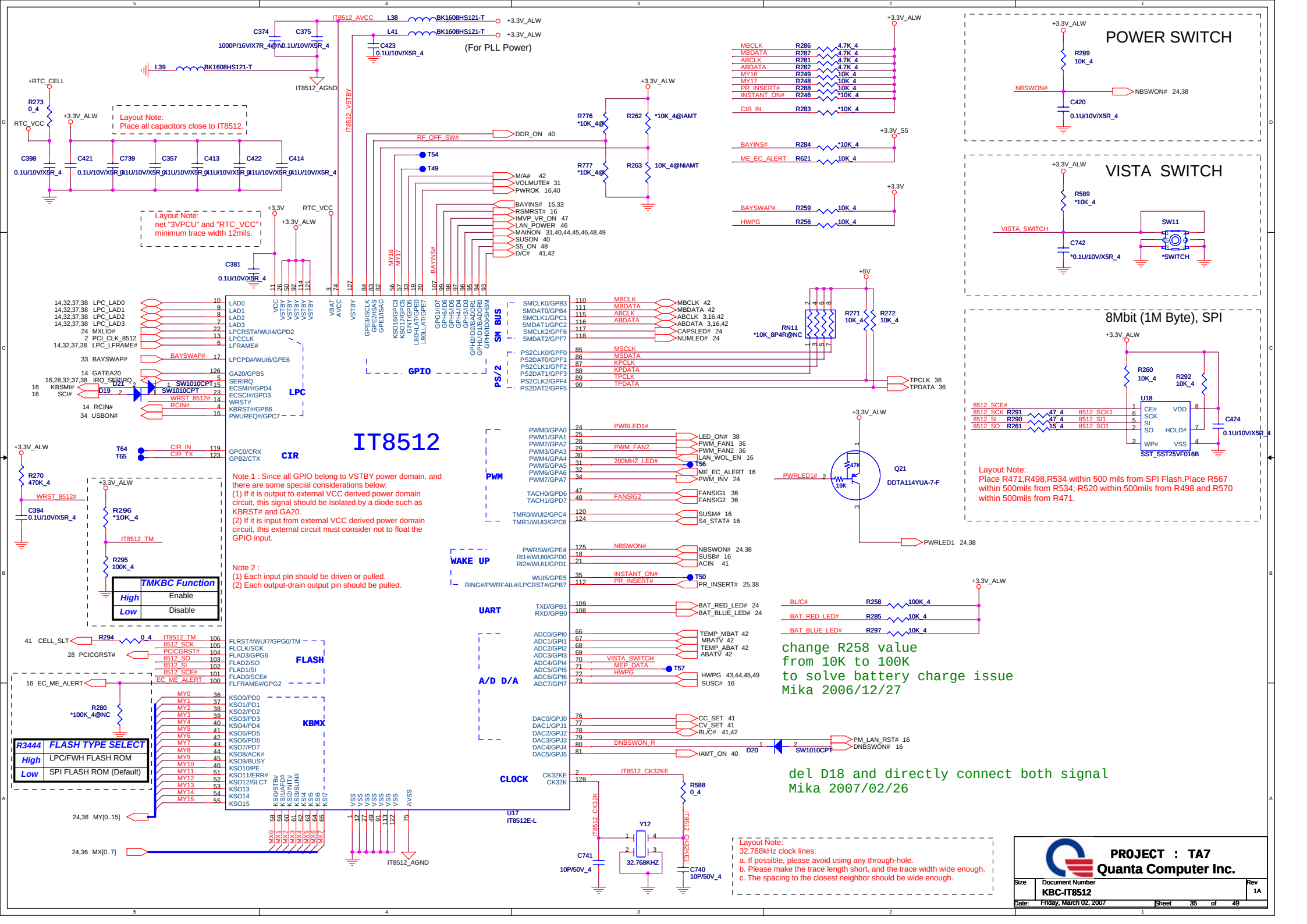
IT8512
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
change R258 value
from 10K to 100K
to solve battery charge issue
Mika 2006/12/27
del D18 and directly connect both signal
Mika 2007/02/26
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
POWER SWITCH
VISTA SWITCH
8Mbit (1M Byte), SPI
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.
PROJECT : TA7
Quanta Computer Inc.
Size
Document Number
KBC-IT8512
Rev
1A
Date: Friday, March 02, 2007
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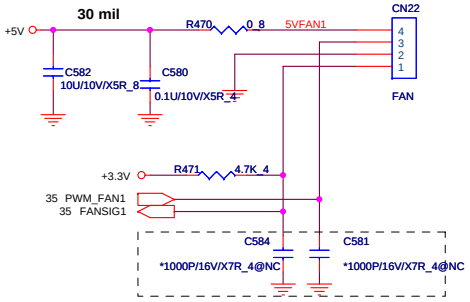
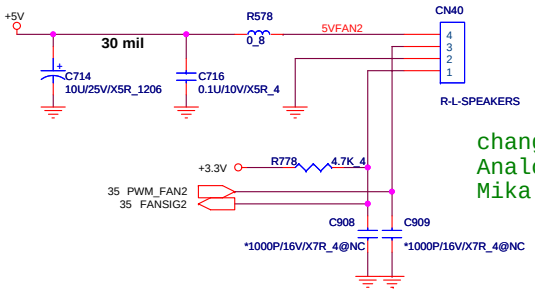
CPU FAN

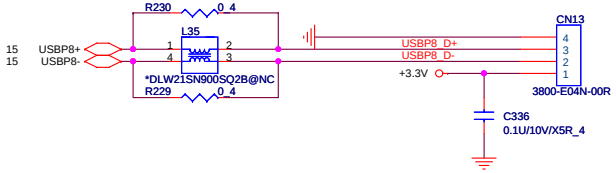


Second FAN for Discrete VGA

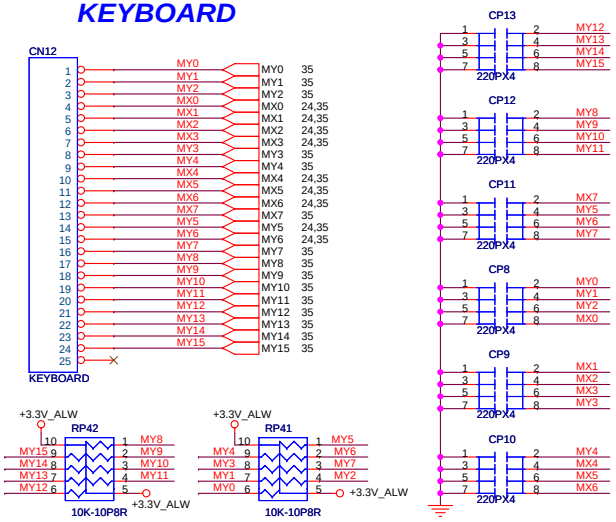


change FAN type from
Analog to PWM
Mika 2006/12/26

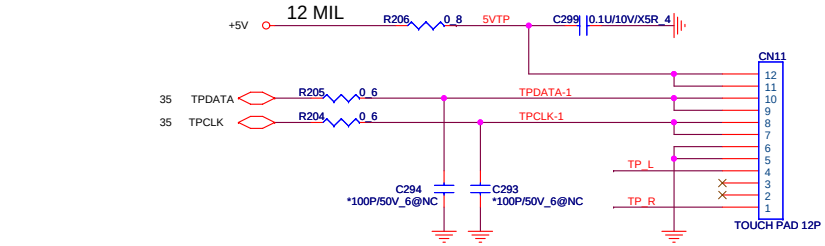
FINGER PRINT CONN

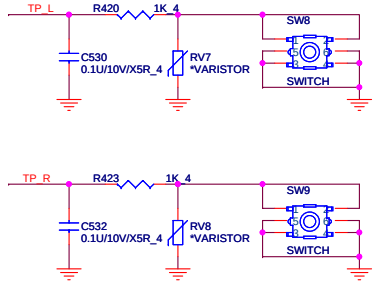


KEYBOARD



TOUCHPAD CONN





PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/TP/KEY/IR/BTB	1A
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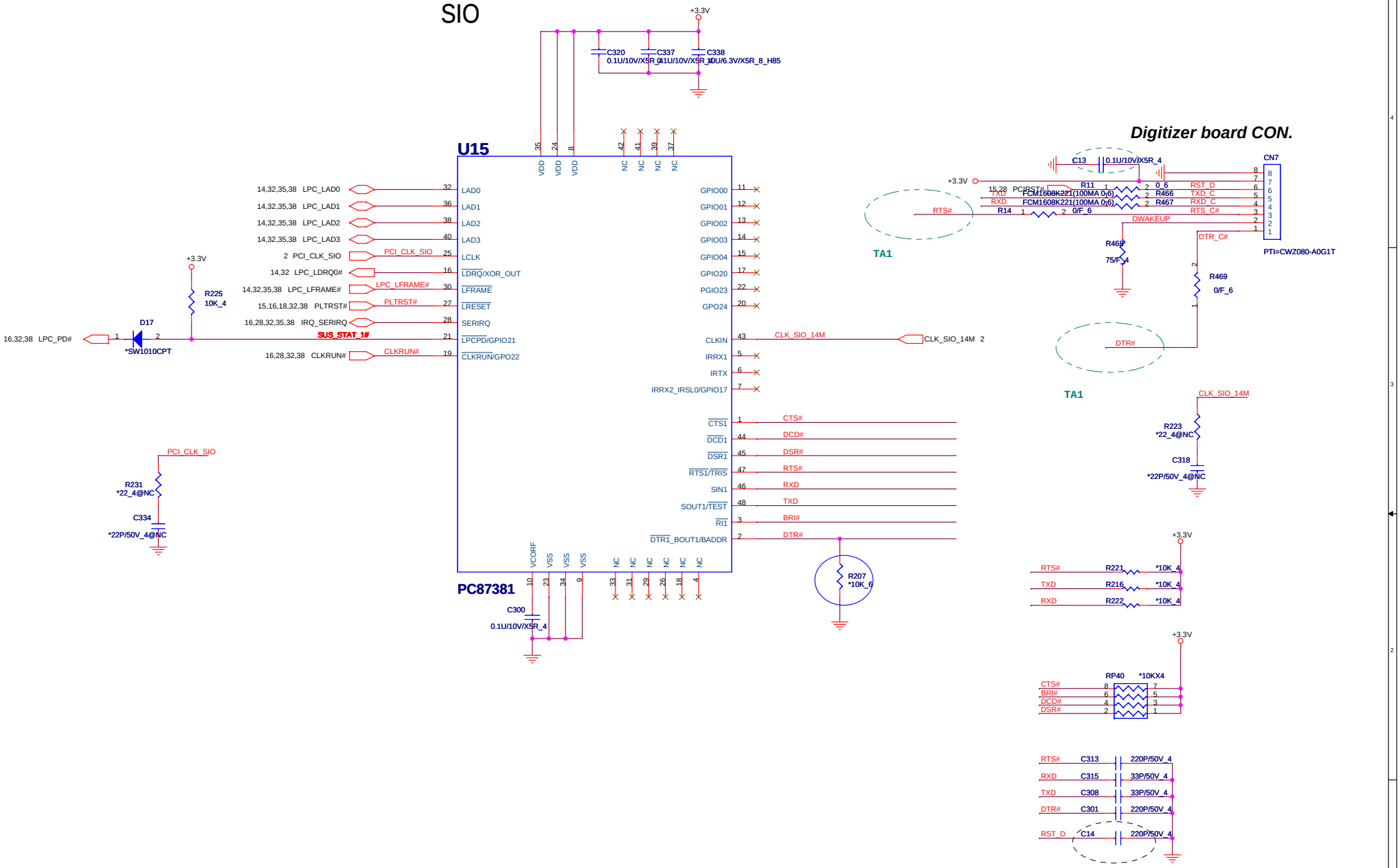
SIO



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Quanta Computer Inc.		
Size	Document Number	Rev
	SUPER I/O - PC87383	1A
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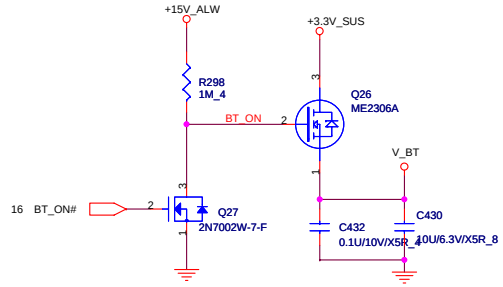
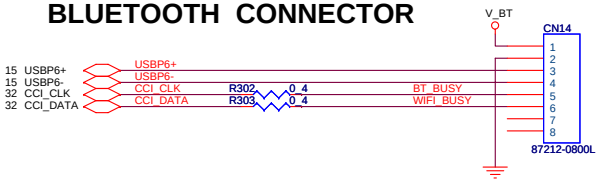
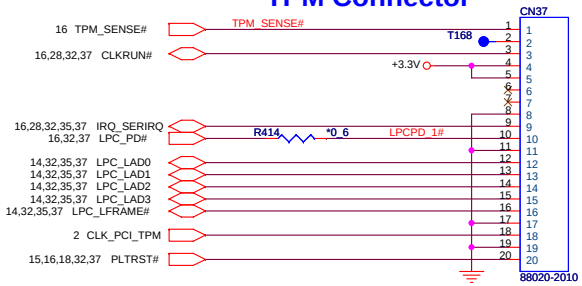


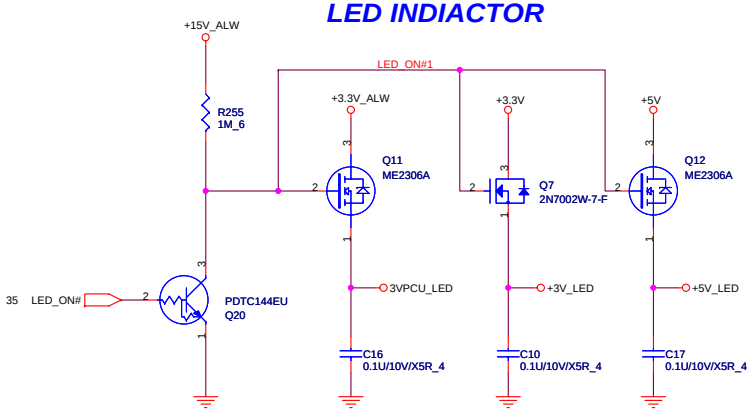
BLUETOOTH CONNECTOR



TPM Connector

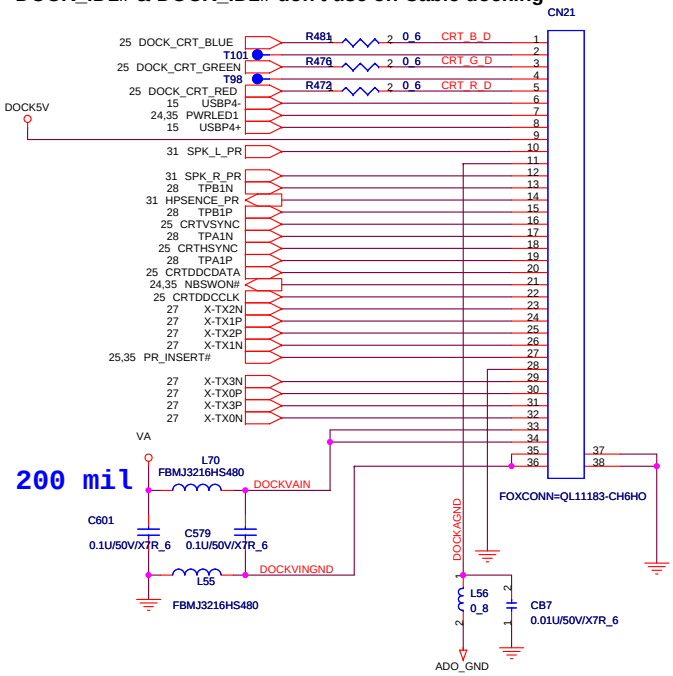


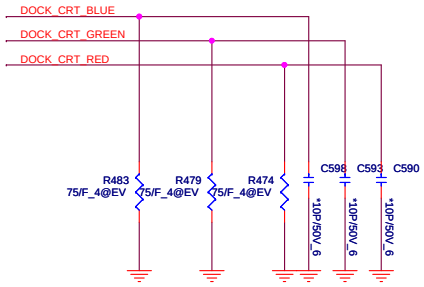
LED INDIACTOR

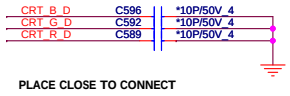


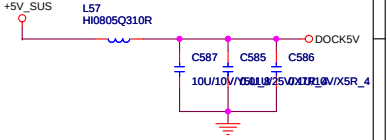
CABLE DOCK

DOCK_ID1# & DOCK_ID2# don't use on Cable docking









CRT	Discrete / UMA
R483	75R 150R
R479	75R 150R
R474	75R 150R

Termination Resistor

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	PORT REPLICATOR(152P)	1A
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PAD7 FDTM1012019
PAD8 FDTM1012019

HOLE7 *H-C315D106P2
HOLE8 *H-TC315BC236D106P2
HOLE17 *H-C315D106P2
HOLE21 *H-C315D106P2
HOLE20 *H-C315D118P2
HOLE11 *H-C315D118P2
HOLE10 *H-C315D102P2
HOLE26 *H-C315D118P2
HOLE24 *H-C315D118P2
HOLE18 *H-C315D118P2
HOLE15 *H-C315D118P2
HOLE13 *H-C315D118P2
HOLE14 *H-C315D118P2
HOLE25 *H-C315D118P2
HOLE16 *H-C315D118P2
HOLE35 H-C315D118P2
HOLE30 H-C315D118P2
HOLE9 *H-C315D102P2
HOLE23 *H-T315B217D118P2
HOLE22 *H-T315B217D118P2
HOLE12 *H-C236D236N
HOLE29 H-T276B217I158D118P2
HOLE33 H-T276B217I158D118P2
HOLE34 H-T276B217I158D118P2
HOLE28 H-T276B217I158D118P2
HOLE19 *H-C315D118I158P2

HOLE36 H-C217D142P2
HOLE39 H-C217D142P2
HOLE31 H-C217D142P2
HOLE27 H-C217D142P2

Mini PCI-E Card Screw

HOLE32 H-C217D142P2
HOLE38 H-C217D142P2

TPM module Screw

HOLE37 H-C217D146P2
HOLE40 H-C217D146P2

+PWR_SRC
C263 0.1U/50V/X7R_6
C28 0.1U/50V/X7R_6
C29 0.1U/50V/X7R_6
C385 0.1U/50V/X7R_6
C30 0.1U/50V/X7R_6

+5V_SUS
C7 0.1U/50V/X7R_6
C51 0.1U/50V/X7R_6
C113 0.1U/50V/X7R_6
C451 0.1U/50V/X7R_6
C448 0.1U/50V/X7R_6
C511 0.1U/50V/X7R_6

+1.8V_SUS
C319 0.1U/10V/X5R_4
C396 0.1U/10V/X5R_4
C434 0.1U/10V/X5R_4

+5V_ALW
C316 0.1U/10V/X5R_4
C439 0.1U/10V/X5R_4
C317 0.1U/10V/X5R_4
C912 0.1U/10V/X5R_4
C913 0.1U/10V/X5R_4

+1.05V_VCCP
C279 0.1U/10V/X5R_4
C326 0.1U/10V/X5R_4
C268 0.1U/10V/X5R_4

+1.25V_M
C288 0.1U/50V/X7R_6
C722 0.1U/50V/X7R_6
C452 0.1U/50V/X7R_6
C526 0.1U/50V/X7R_6

+3.3V
C914 0.1U/10V/X5R_4

add C912 C913 C914
from C.S suggestion
Mika 2007/02/26

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Quanta Computer Inc.

Size	Document Number	Rev
	PAD & SCREW	1A
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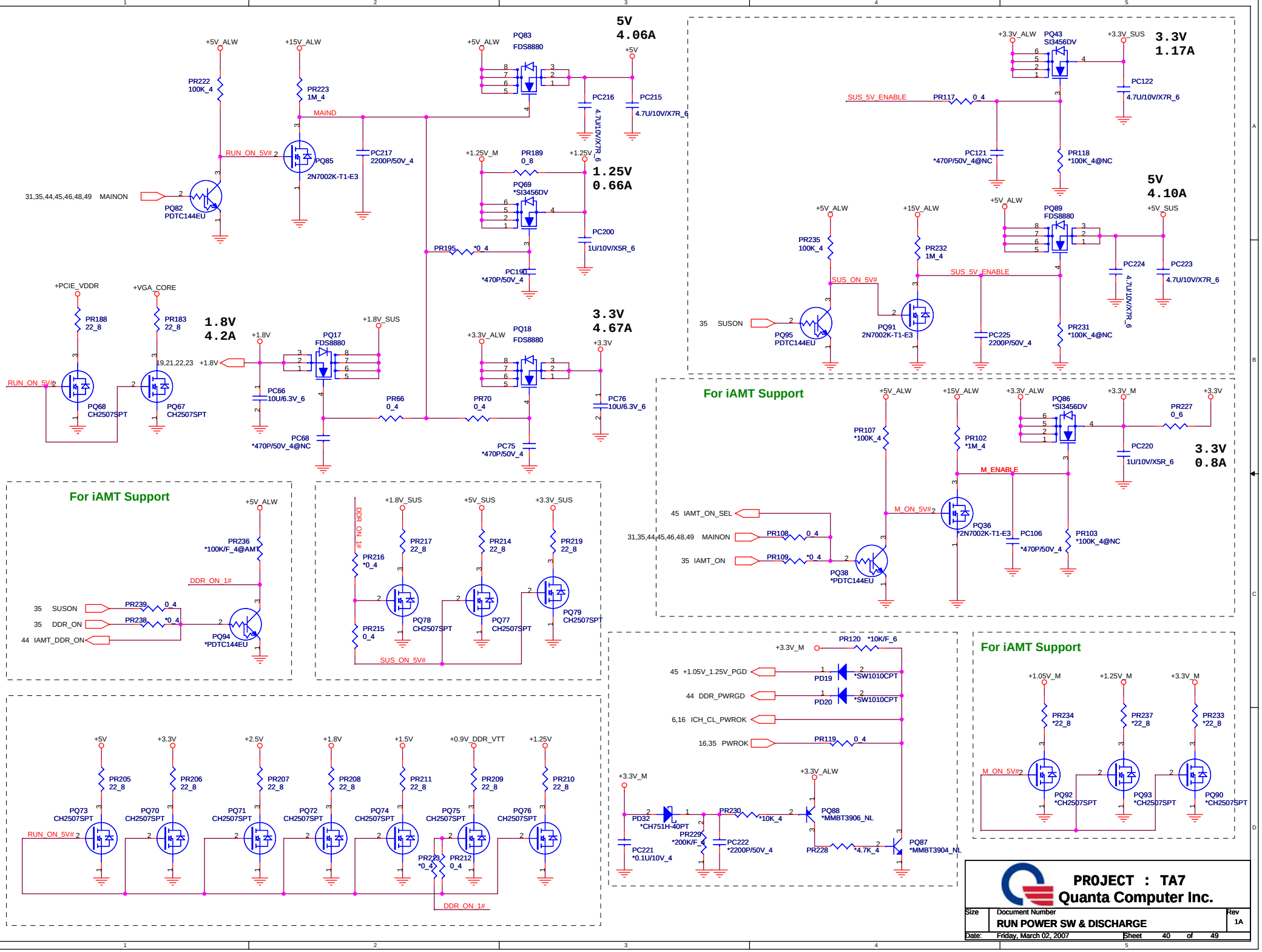
5V
4.06A
1.25V
0.66A
1.8V
4.2A
3.3V
4.67A
3.3V
1.17A
5V
4.10A
3.3V
0.8A
For iAMT Support
For iAMT Support
For iAMT Support
PROJECT : TA7
Quanta Computer Inc.
RUN POWER SW & DISCHARGE
Size
Document Number
Rev
1A
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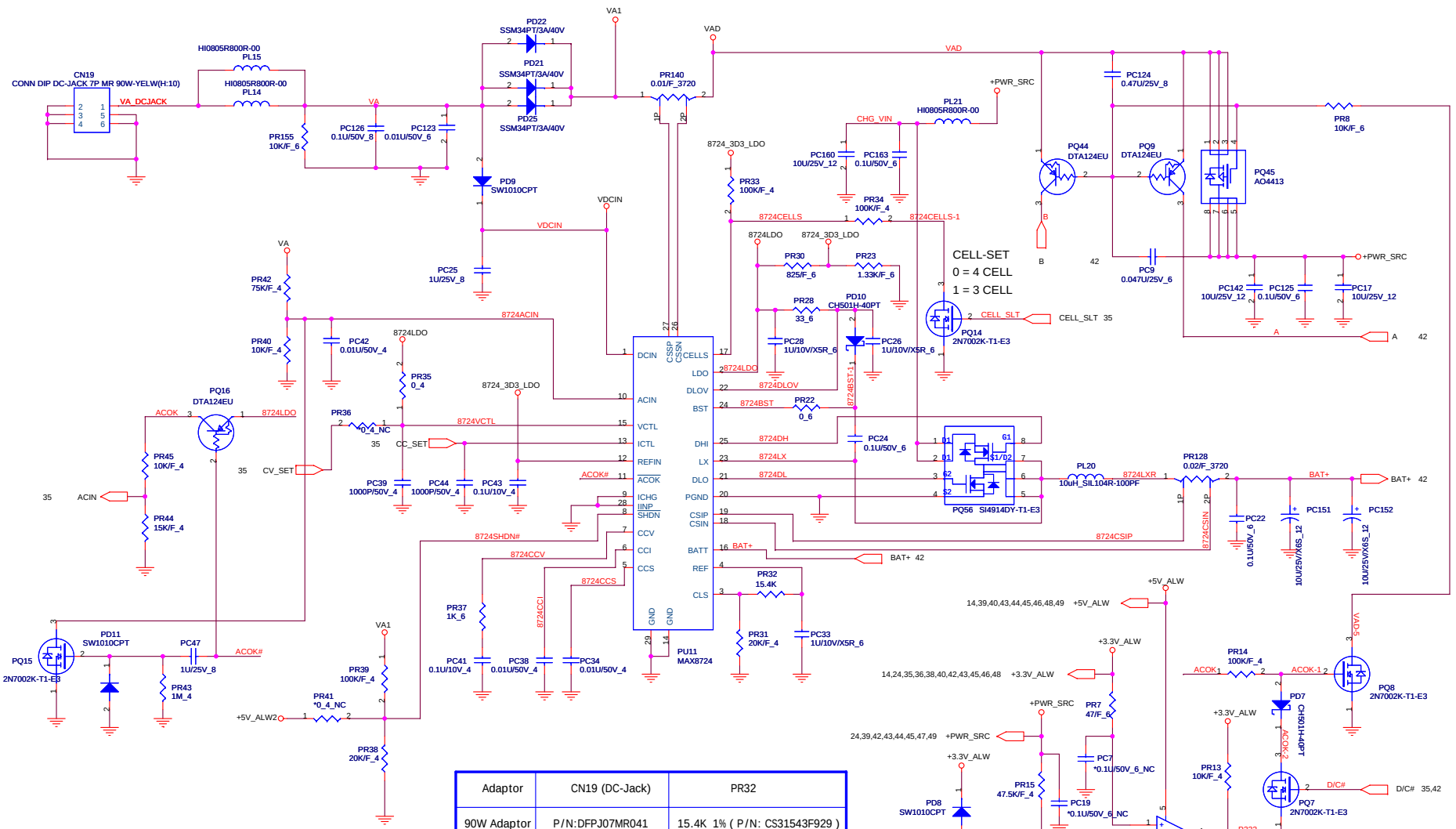

Adaptor	CN19 (DC-Jack)	PR32
90W Adaptor	P/N:DFPJ07MR041	15.4K_1% (P/N: CS31543F929)
65W Adaptor	P/N:DFPJ06MR097	30.9K_1% (P/N: CS33092FB06)

<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

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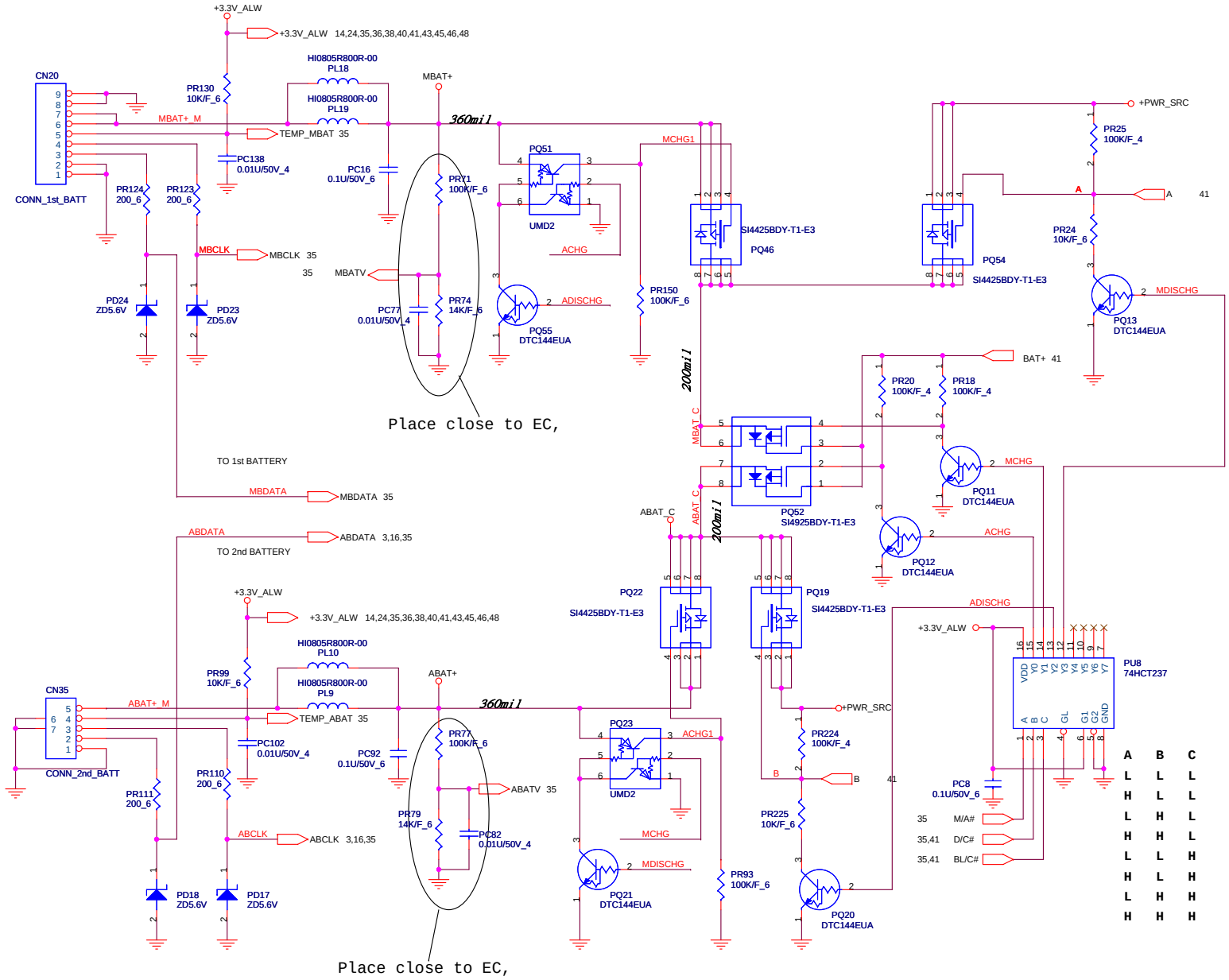
Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER	1A
Date: Friday, March 02, 2007	Sheet 41 of 49	



A	B	C	Y0	Y1	Y2	Y3
L	L	L	H	L	L	L
H	L	L	L	H	L	L
L	H	L	L	L	H	L
H	H	L	L	L	L	H
L	L	H	L	L	L	L
H	L	H	L	L	L	L
L	H	H	L	L	L	L
H	H	H	L	L	L	L

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	BATT SELECTOR	1A

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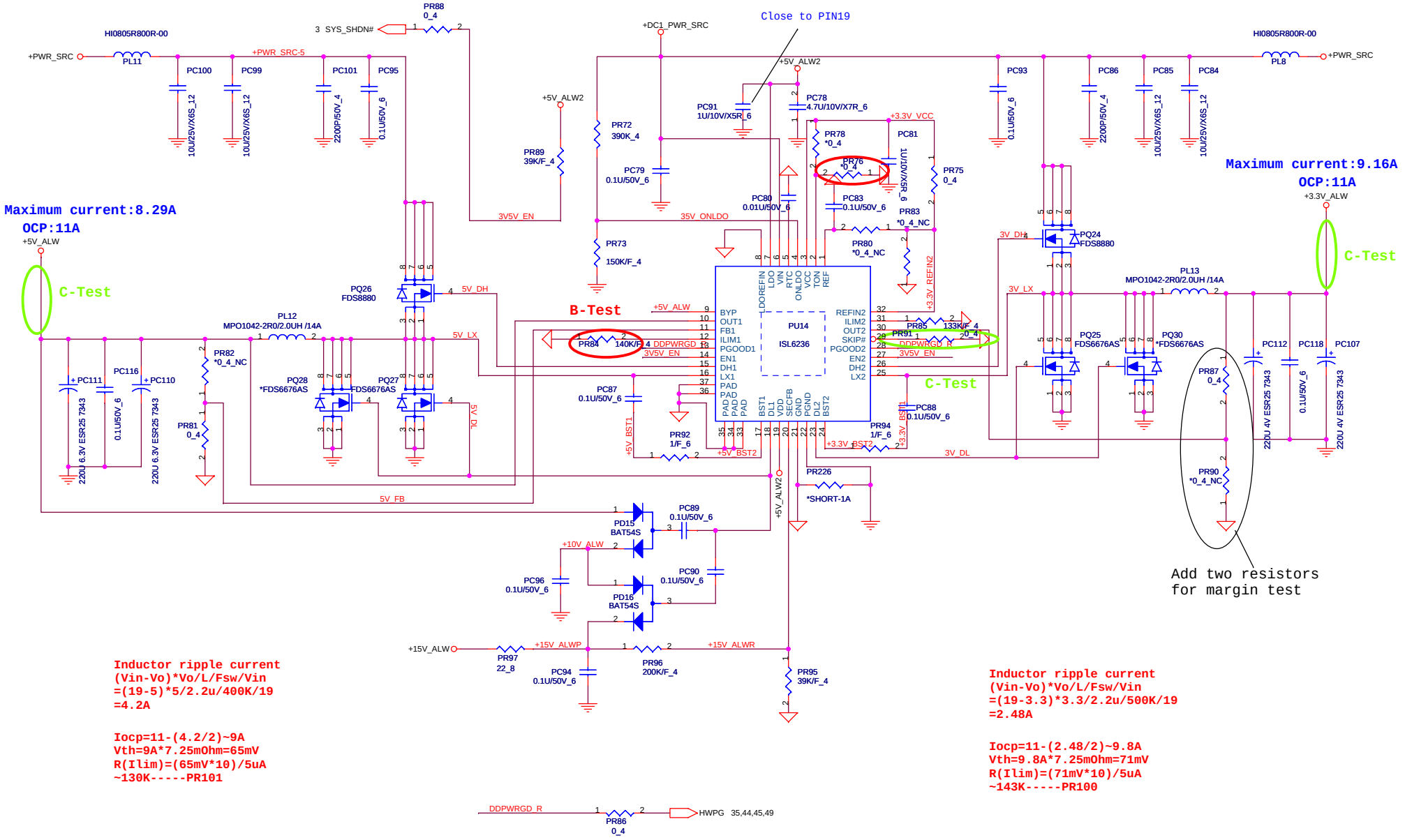

PROJECT : TA7
Quanta Computer Inc.

Size	Document Number	Rev
	+3.3V & +5V	2A
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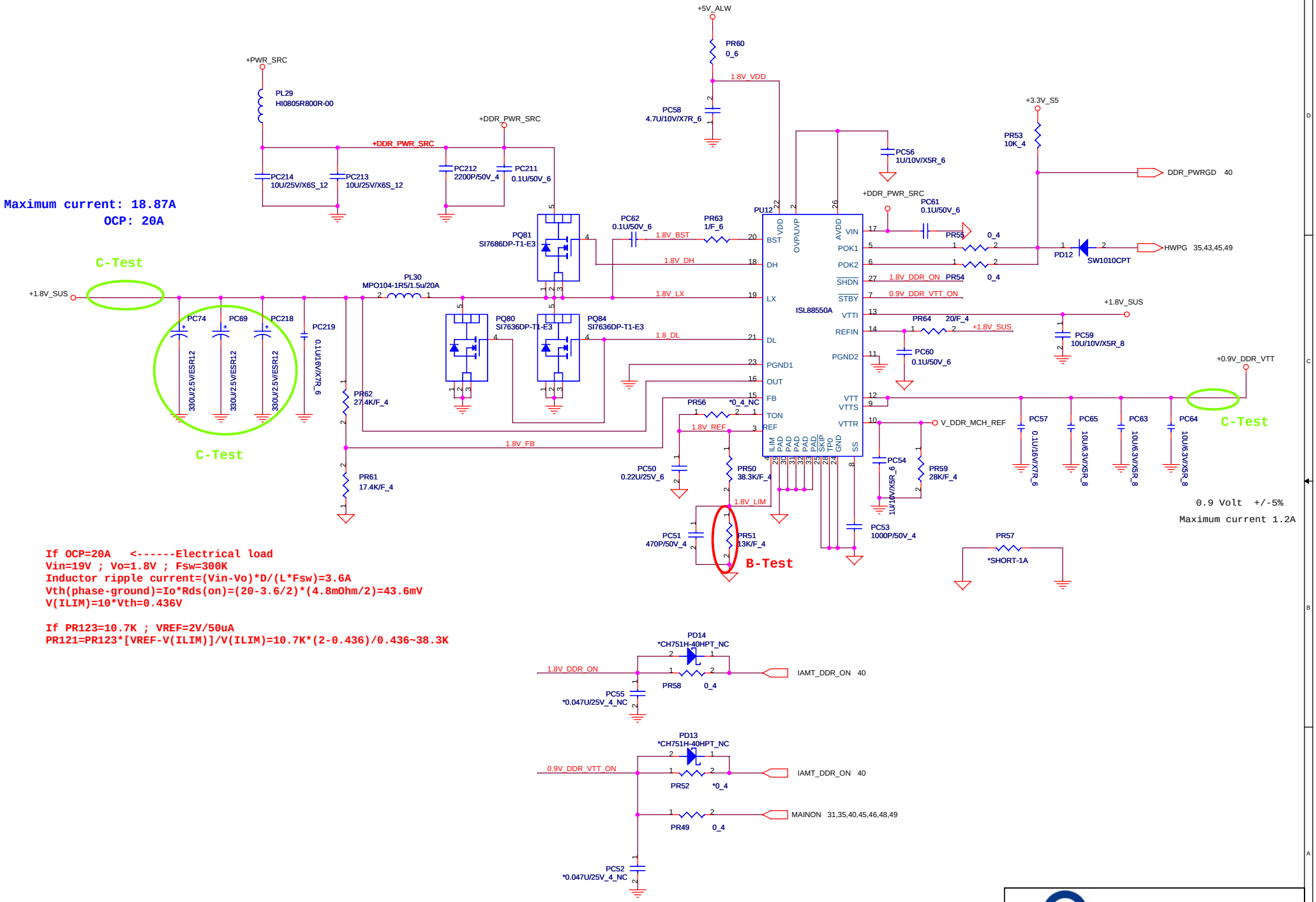

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Quanta Computer Inc.		
Size	Document Number	Rev
	1.8V_SUS & 0.9V_VTT	2A
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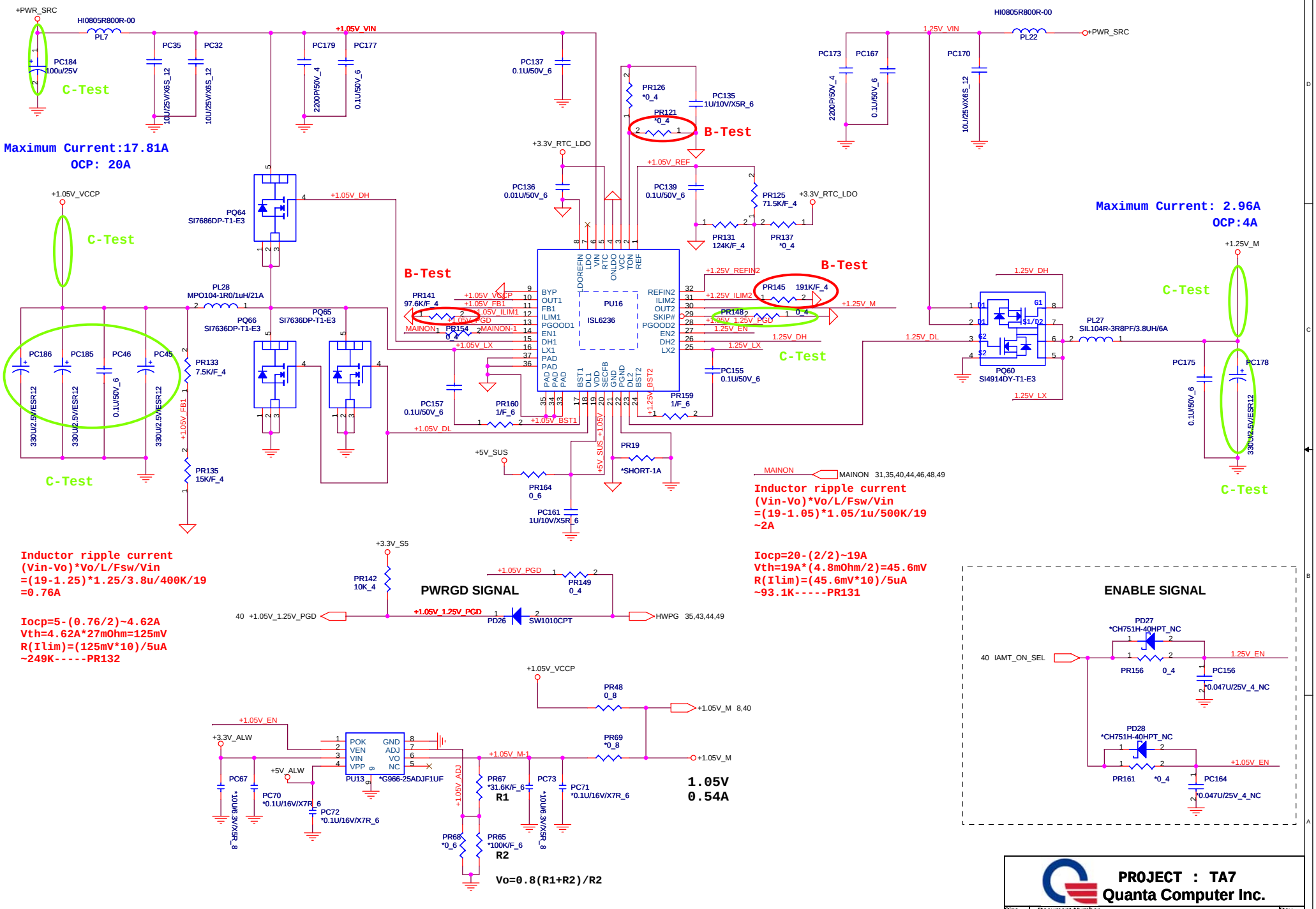

PROJECT : TA7		
Quanta Computer Inc.		
Size	Document Number	Rev
	1.25V & 1.05V	2A
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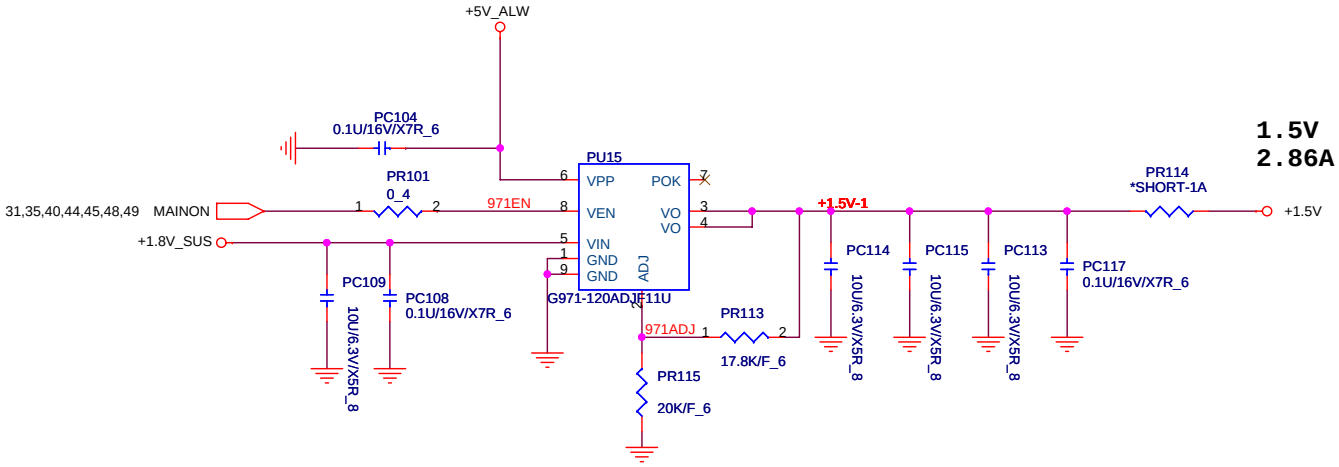
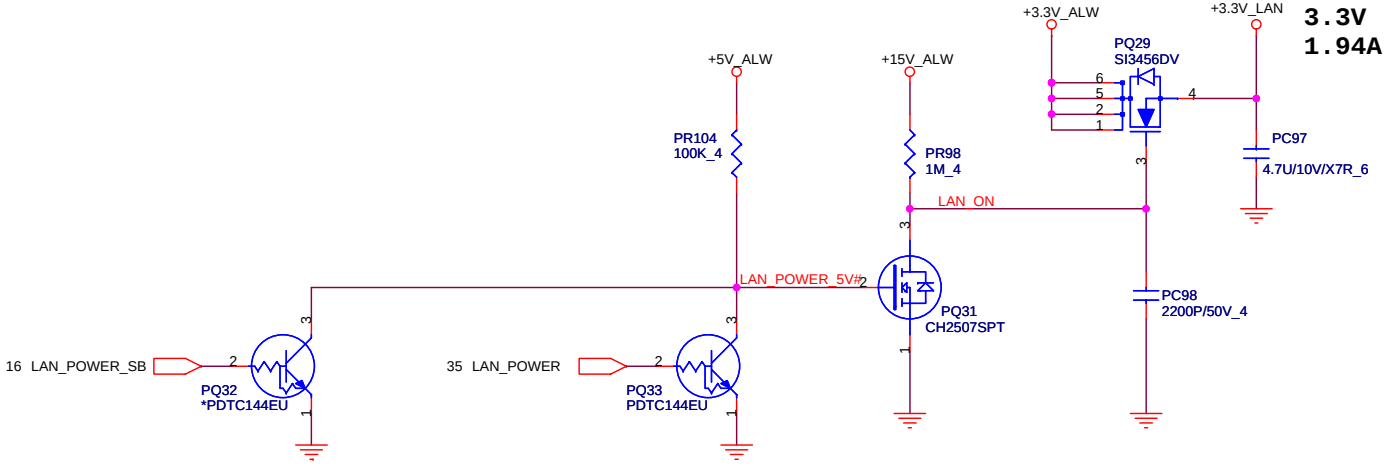


1.5V
2.86A

Vout =0.8(1+R1/R2) =
0.8(1+17.8K/20K) =
1.512V



3.3V
1.94A

<OrgName>	**PROJECT : TA7**	
<OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>	**Quanta Computer Inc.**	
Size	Document Number: **1.5V, +3.3V_LAN**	Rev: 1A
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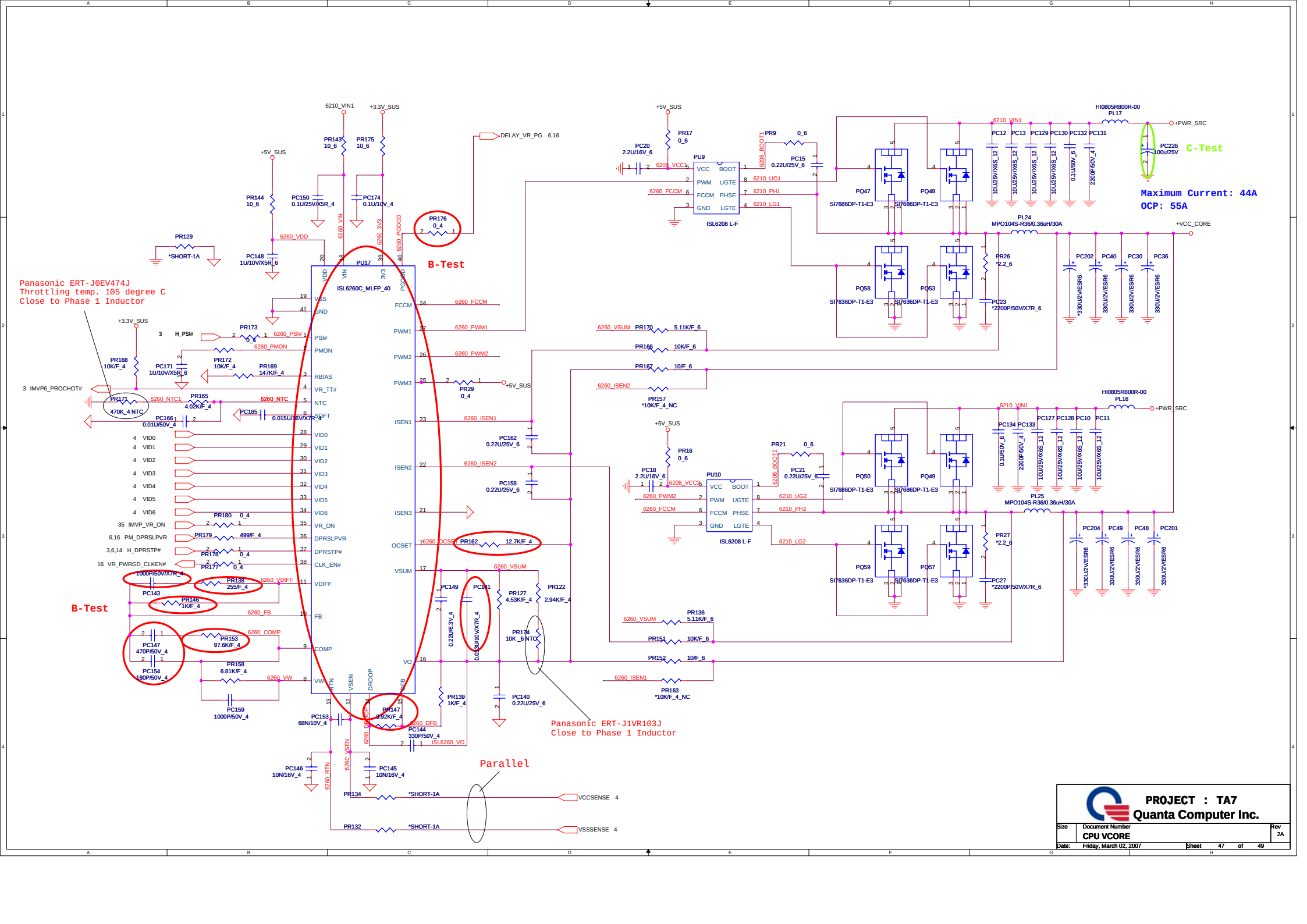
Panasonic ERT-J0EV474J
Throttling temp. 105 degree C
Close to Phase 1 Inductor
B-Test
B-Test
Panasonic ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
C-Test
Maximum Current: 44A
OCP: 55A
ISL6260C_MLFP_40
ISL6208 L-F
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Quanta Computer Inc.
CPU VCORE
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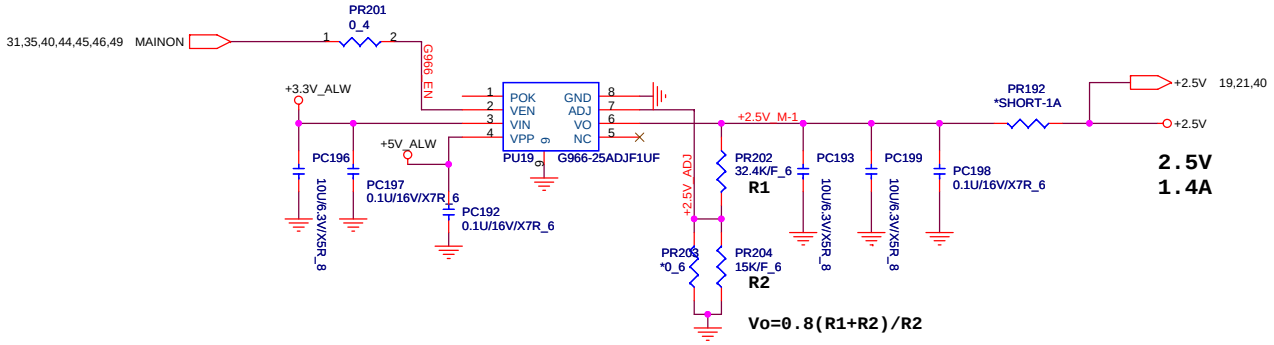
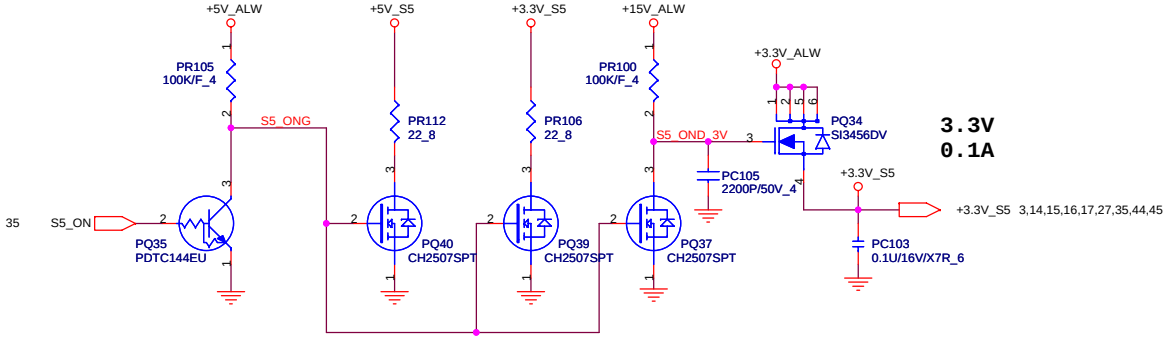
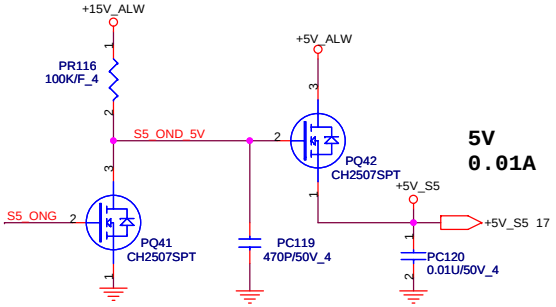
For Discrete M71S Model Only







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Quanta Computer Inc.

Size	Document Number	Rev
	+2.5V/3VS5/5VS5	1A
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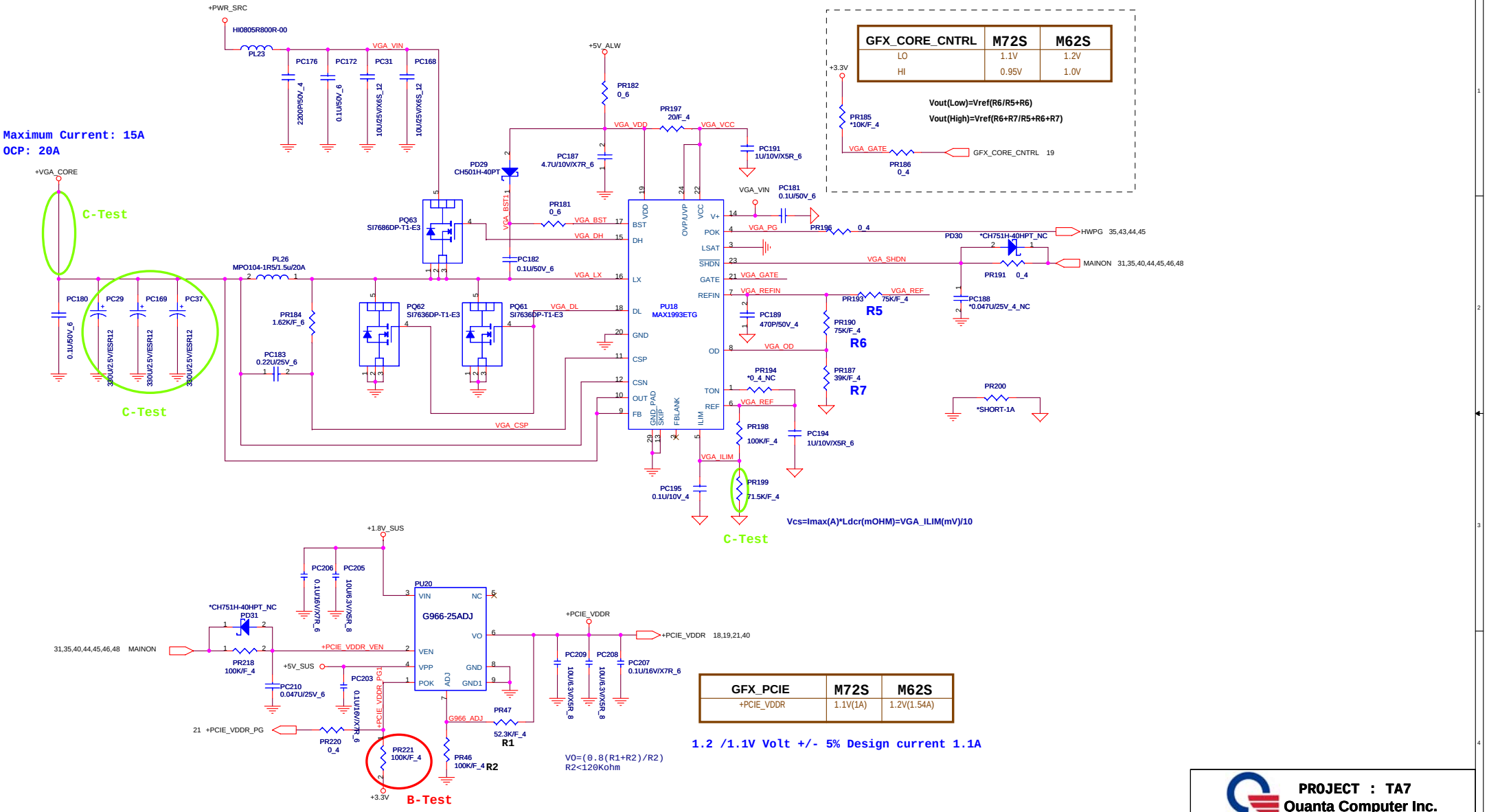
Maximum Current: 15A
OCP: 20A
+PWR_SRC
HI0805R800R-00
PL23
VGA_VIN
PC176
PC172
PC31
PC168
2200P/50V_4
0.1U/50V_6
10U/25V/X6S_12
10U/25V/X6S_12
+VGA_CORE
C-Test
PC180
PC29
PC169
PC37
0.1U/50V_6
330U/2.5V/ESR12
330U/2.5V/ESR12
330U/2.5V/ESR12
C-Test
PL26
MPO104-1R5/1.5u/20A
PR184
1.62K/F_6
PC183
0.22U/25V_6
PQ63
SI7686DP-T1-E3
PQ62
SI7636DP-T1-E3
PQ61
SI7636DP-T1-E3
PD29
CH501H-40PT
VGA_BST1
PC187
4.7U/10V/X7R_6
PR181
0_6
PC182
0.1U/50V_6
VGA_BST
VGA_DH
VGA_LX
VGA_DL
VGA_CSP
+5V_ALW
PR182
0_6
PR197
20/F_4
VGA_VDD
VGA_VCC
PC191
1U/10V/X5R_6
PU18
MAX1993ETG
VDD
BST
DH
LX
DL
GND
CSP
CSN
OUT
FB
GND_PAD
SKIP
FBLANK
ILIM
OV/PUVP
VCC
V+
POK
LSAT
SHDN
GATE
REFIN
OD
TON
REF
VGA_VIN
PC181
0.1U/50V_6
VGA_PG
PR196
0_4
VGA_SHDN
VGA_GATE
VGA_REFIN
VGA_REF
PR193
75K/F_4
R5
PC189
470P/50V_4
PR190
75K/F_4
R6
VGA_OD
PR194
*0_4_NC
PR187
39K/F_4
R7
VGA_REF
PR198
100K/F_4
PC194
1U/10V/X5R_6
VGA_ILIM
PR199
71.5K/F_4
PC195
0.1U/10V_4
Vcs=Imax(A)*Ldcr(mOHM)=VGA_ILIM(mV)/10
C-Test
PD30
*CH751H-40HPT_NC
HWPG 35,43,44,45
MAINON 31,35,40,44,45,46,48
PR191 0_4
PC188
*0.047U/25V_4_NC
PR200
*SHORT-1A
+3.3V
PR185
*10K/F_4
VGA_GATE
GFX_CORE_CNTRL 19
PR186
0_4
GFX_CORE_CNTRL | M72S | M62S
LO | 1.1V | 1.2V
HI | 0.95V | 1.0V
Vout(Low)=Vref(R6/R5+R6)
Vout(High)=Vref(R6+R7/R5+R6+R7)
+1.8V_SUS
PC206
PC205
0.1U/16V/X7R_6
10U/6.3V/X5R_8
PU20
G966-25ADJ
VIN
NC
VO
VEN
VPP
GND
POK
GND1
ADJ
*CH751H-40HPT_NC
PD31
31,35,40,44,45,46,48 MAINON
PR218
100K/F_4
+PCIE_VDDR_VEN
+5V_SUS
PC210
0.047U/25V_6
PC203
0.1U/16V/X7R_6
+PCIE_VDDR_PG1
G966_ADJ
PR47
52.3K/F_4
R1
21 +PCIE_VDDR_PG
PR220
0_4
PR221
100K/F_4
PR46
100K/F_4
R2
+3.3V
B-Test
+PCIE_VDDR
PC209
PC208
PC207
0.1U/16V/X7R_6
10U/6.3V/X5R_8
10U/6.3V/X5R_8
+PCIE_VDDR 18,19,21,40
GFX_PCIE | M72S | M62S
+PCIE_VDDR | 1.1V(1A) | 1.2V(1.54A)
1.2 /1.1V Volt +/- 5% Design current 1.1A
VO=(0.8(R1+R2)/R2)
R2<120Kohm
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Quanta Computer Inc.
Size
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GFX_CORE
Rev
2A
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